



Compal Confidential

KAWG0 Schematics Document

AMD S1g1 / RS690MC / SB600

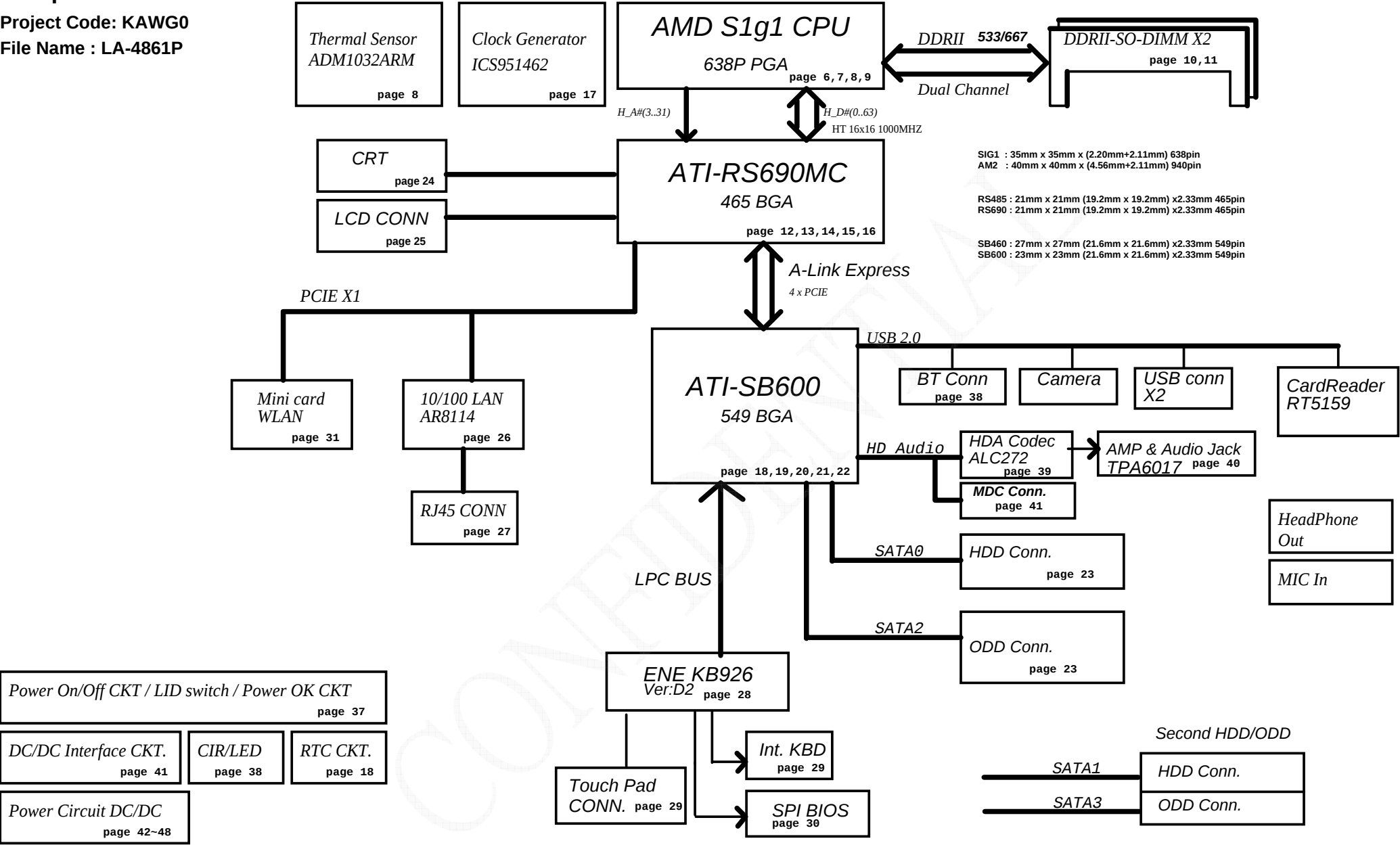
2009 / 04 / 09

Rev:1.0

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Project Code: KAWG0
File Name : LA-4861P



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Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

External PCI Devices

EC SM Bus1 address

EC SM Bus2 address

SB600 SM Bus 2 address

SIGNAL STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

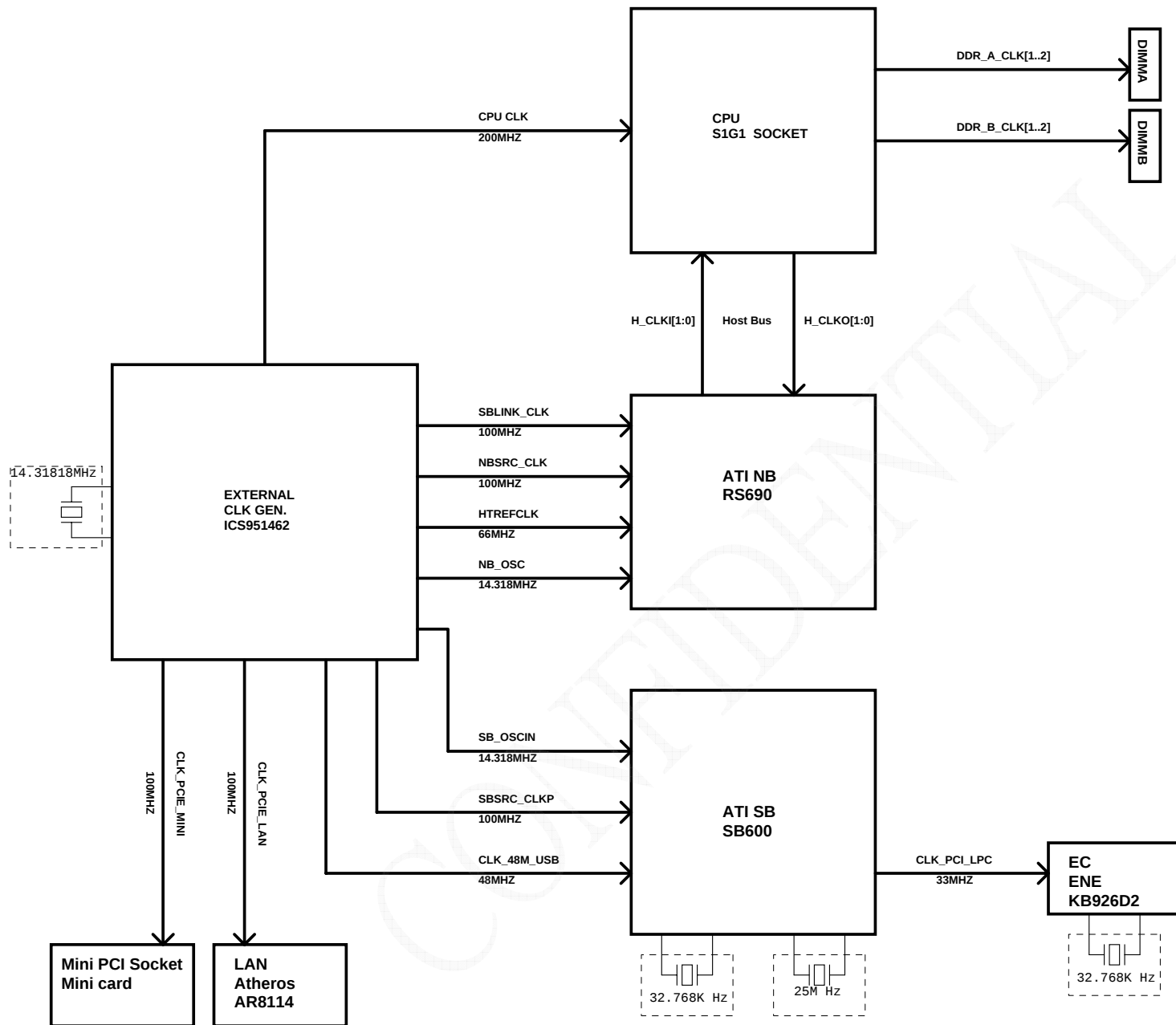
Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

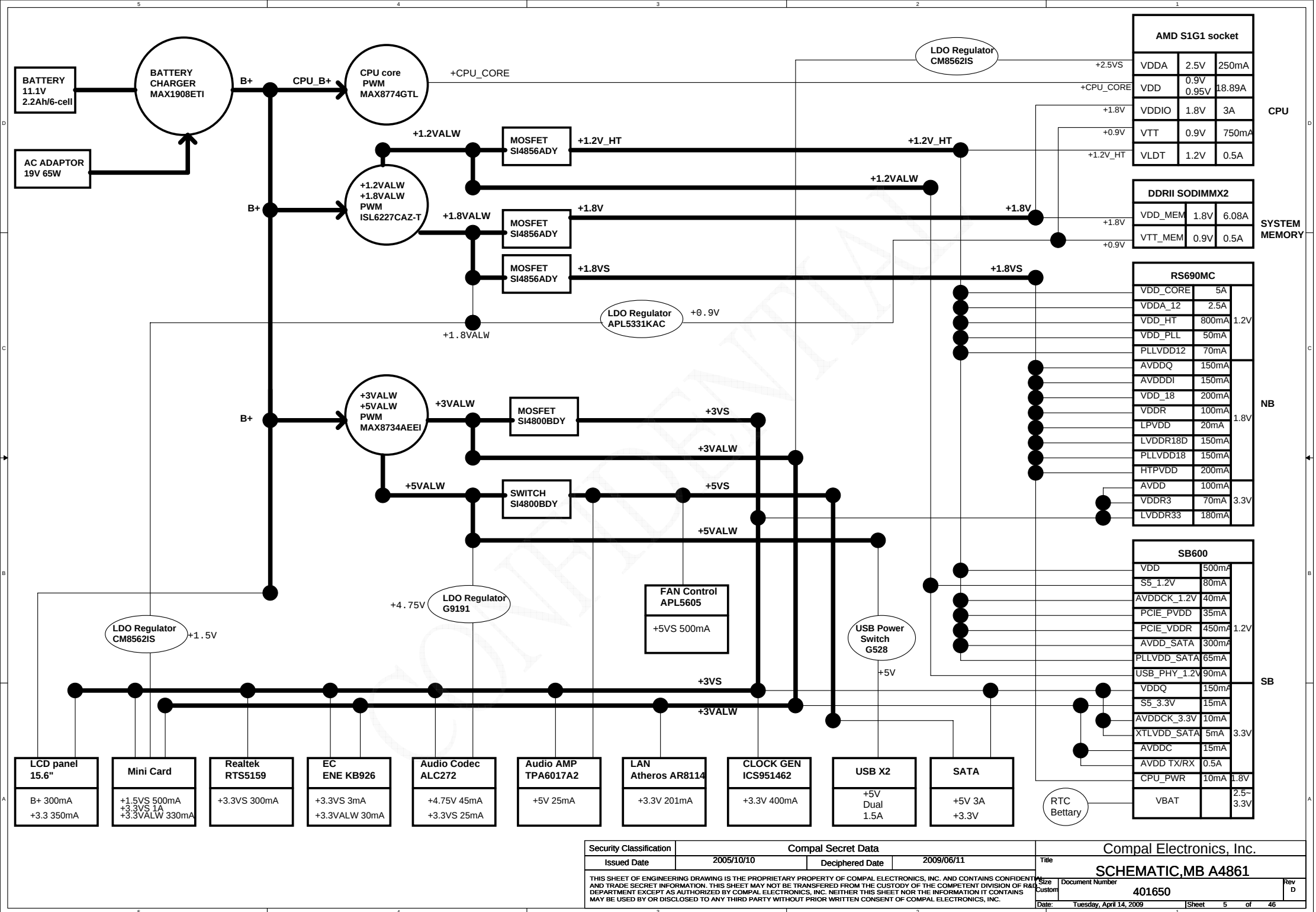
SKU ID	SKU
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2	
3	
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6	
7	

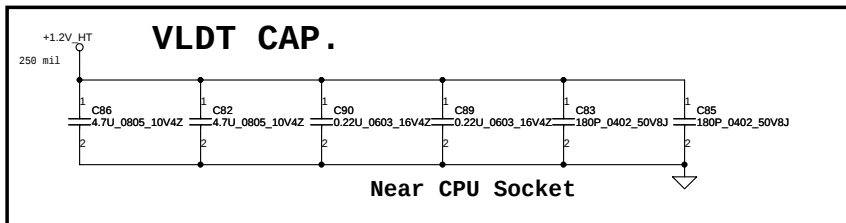
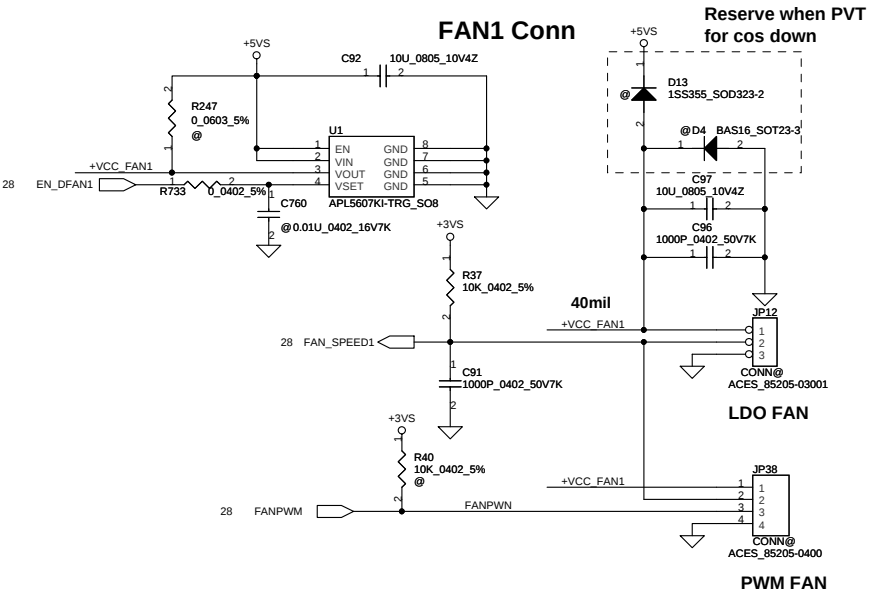
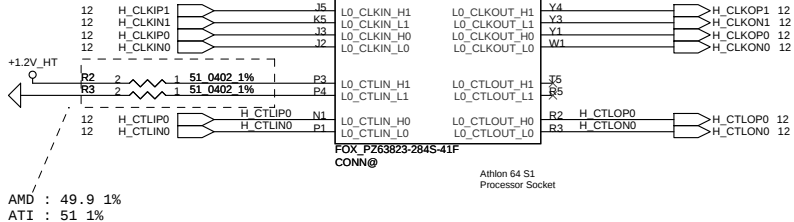
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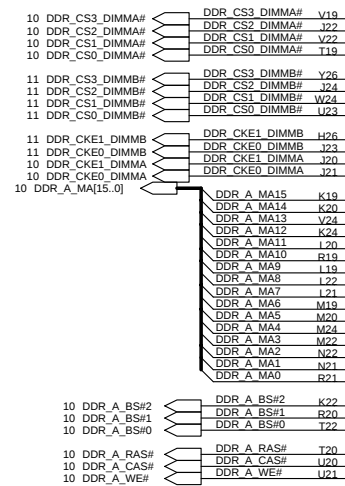
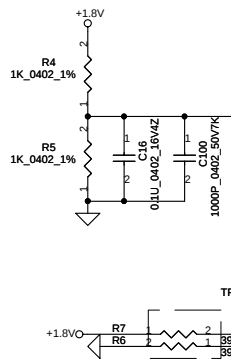


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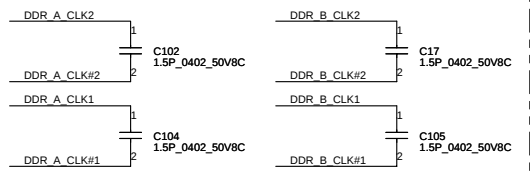


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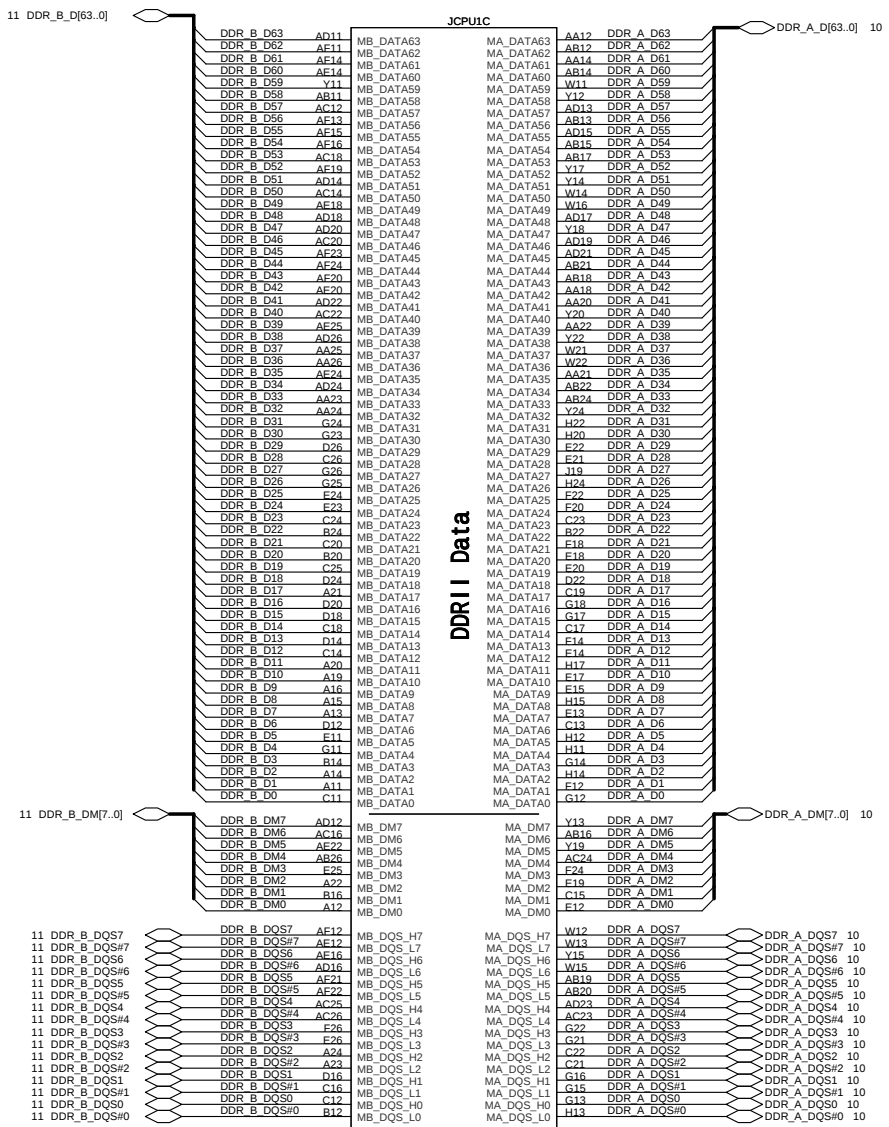


CONN@ FOX P263823-2845-41F
Athlon 64 S1
Processor
Socket

PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



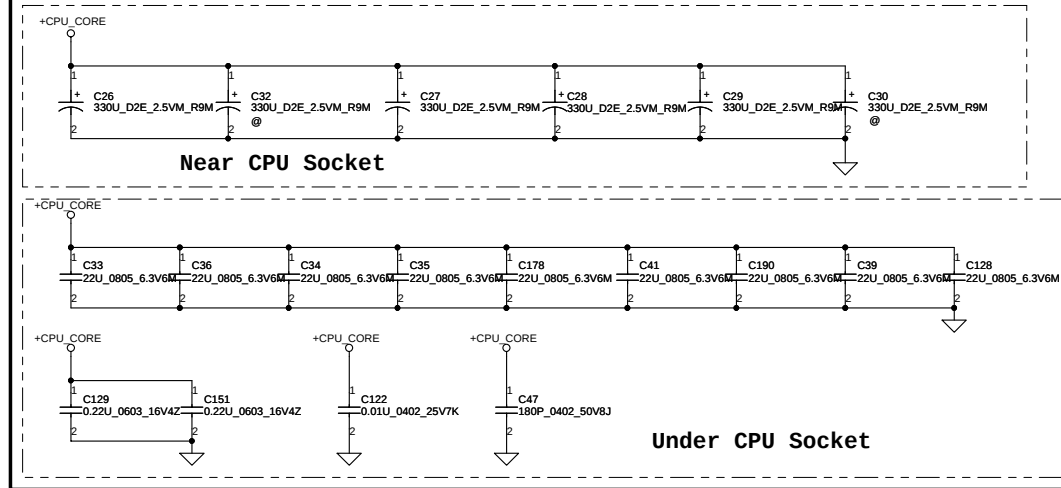
Processor DDR2 Memory Interface



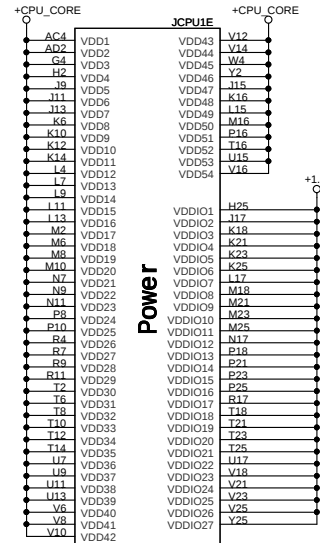
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Athlon 64 S1
Processor
Socket

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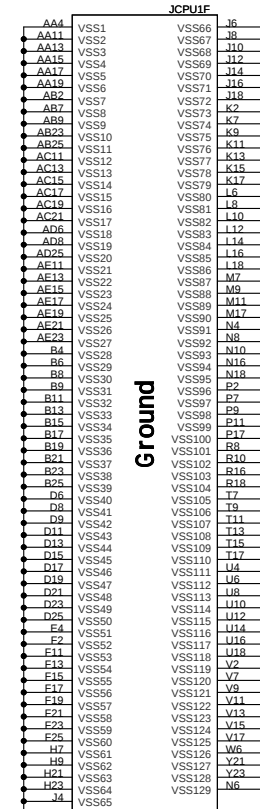
VDD(+CPU_CORE) decoupling.



Power

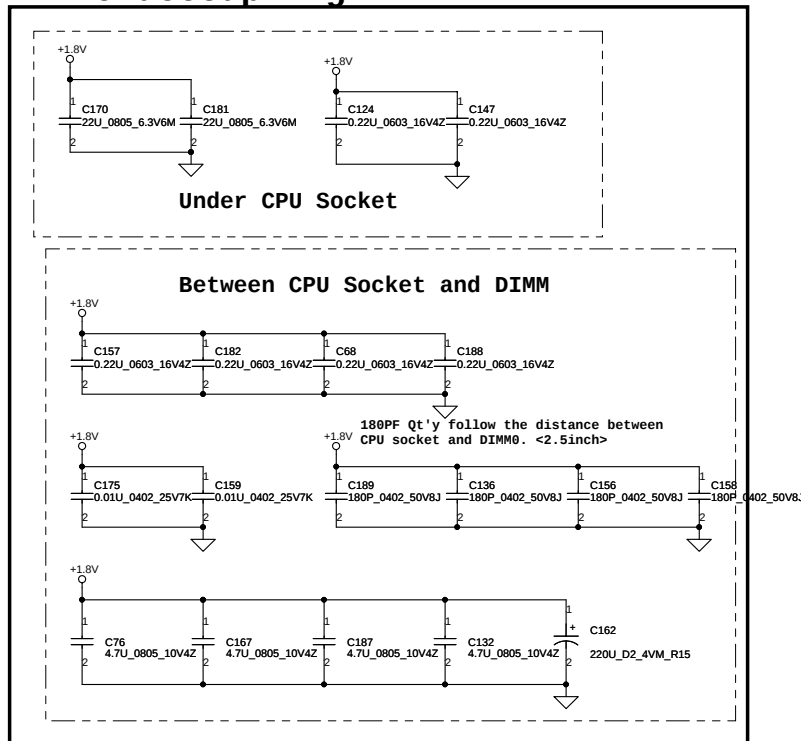


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CONN@
Athlon 64 S1
Processor Socket

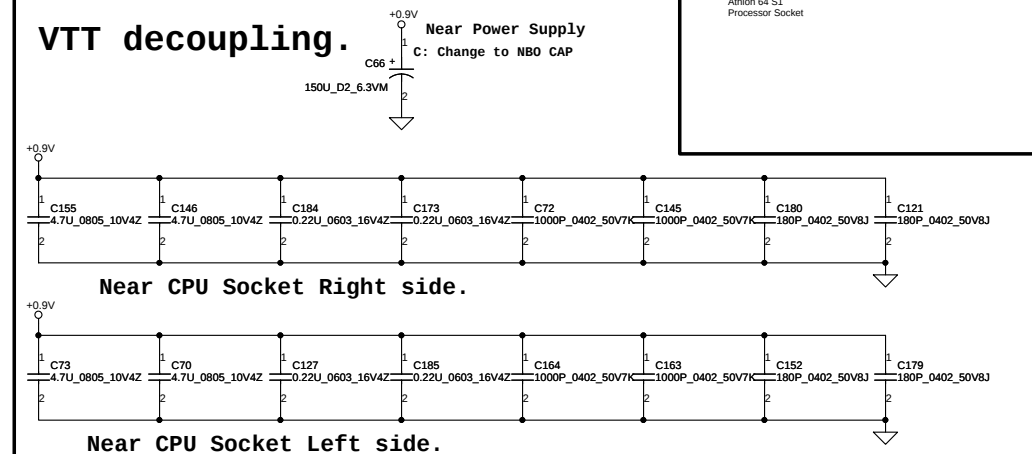


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VDDIO decoupling.

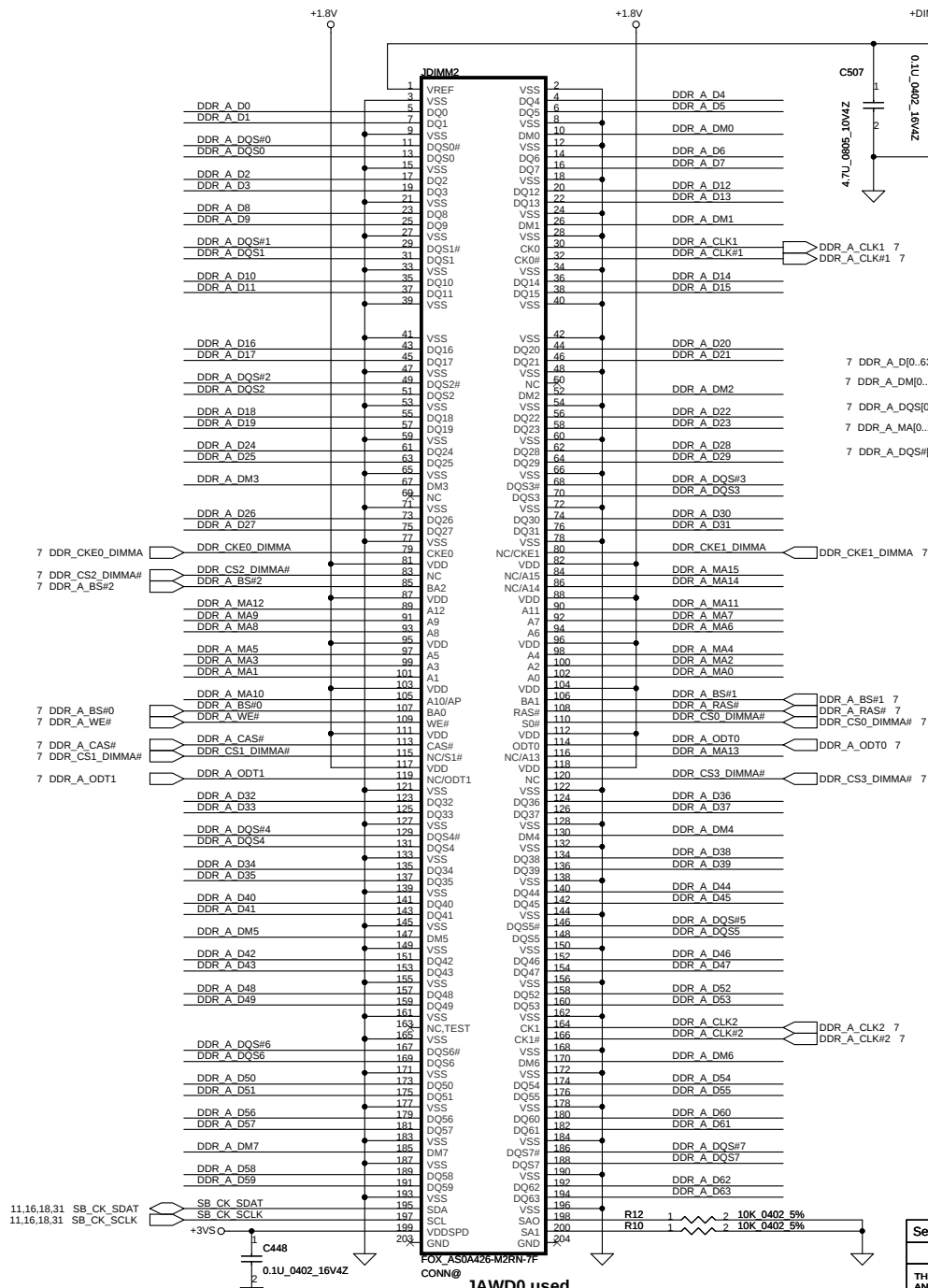


VTT decoupling.

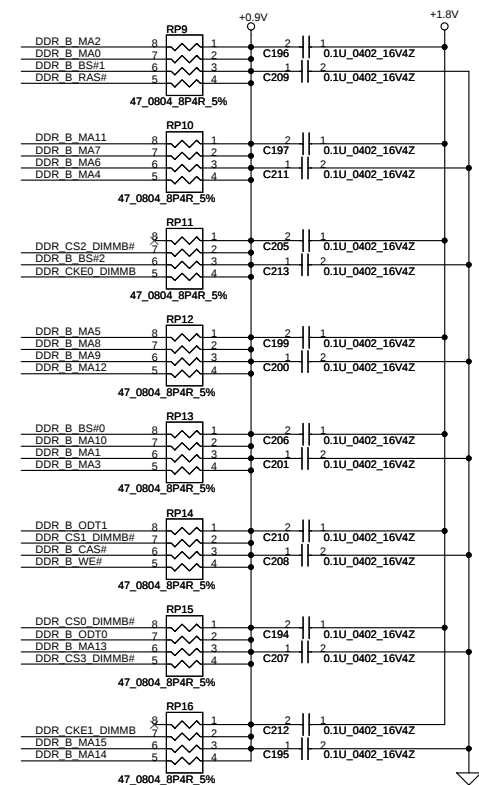
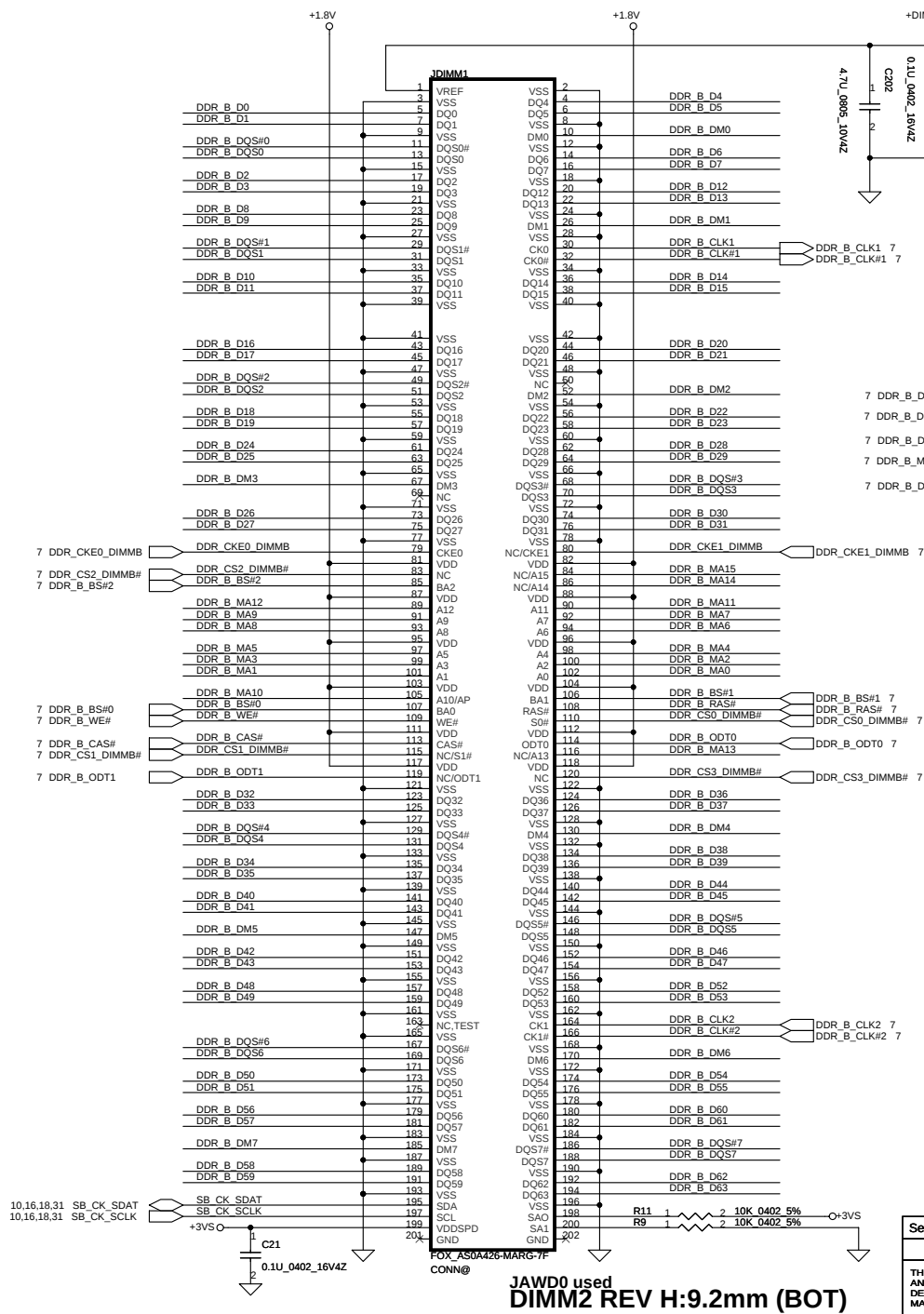


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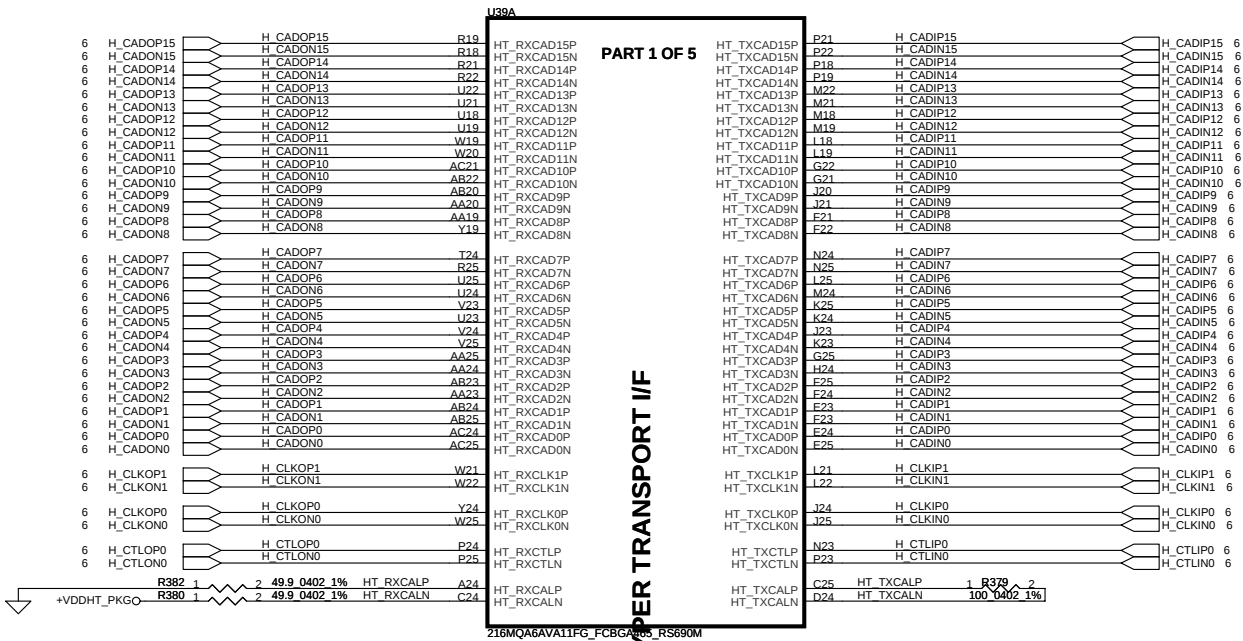
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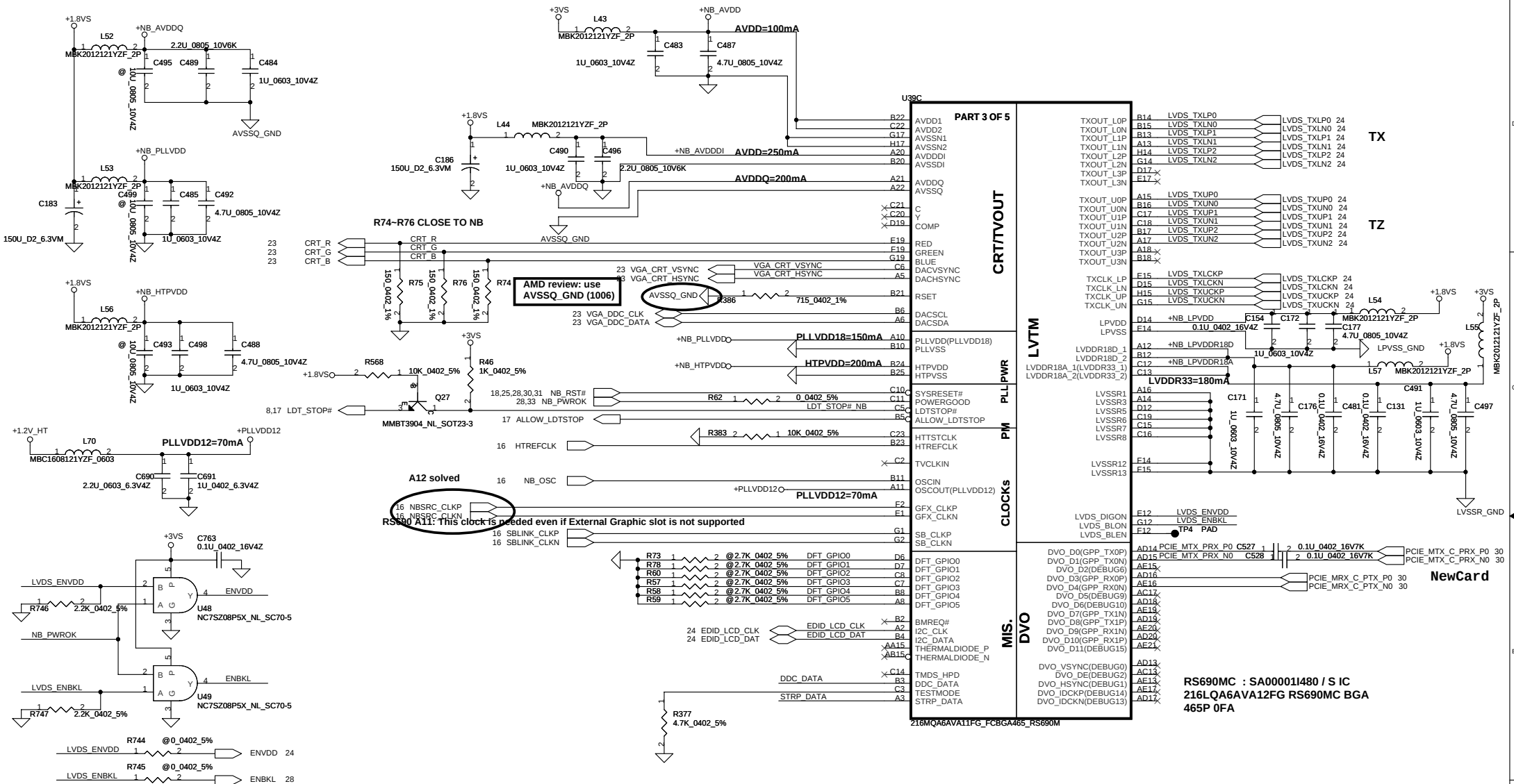


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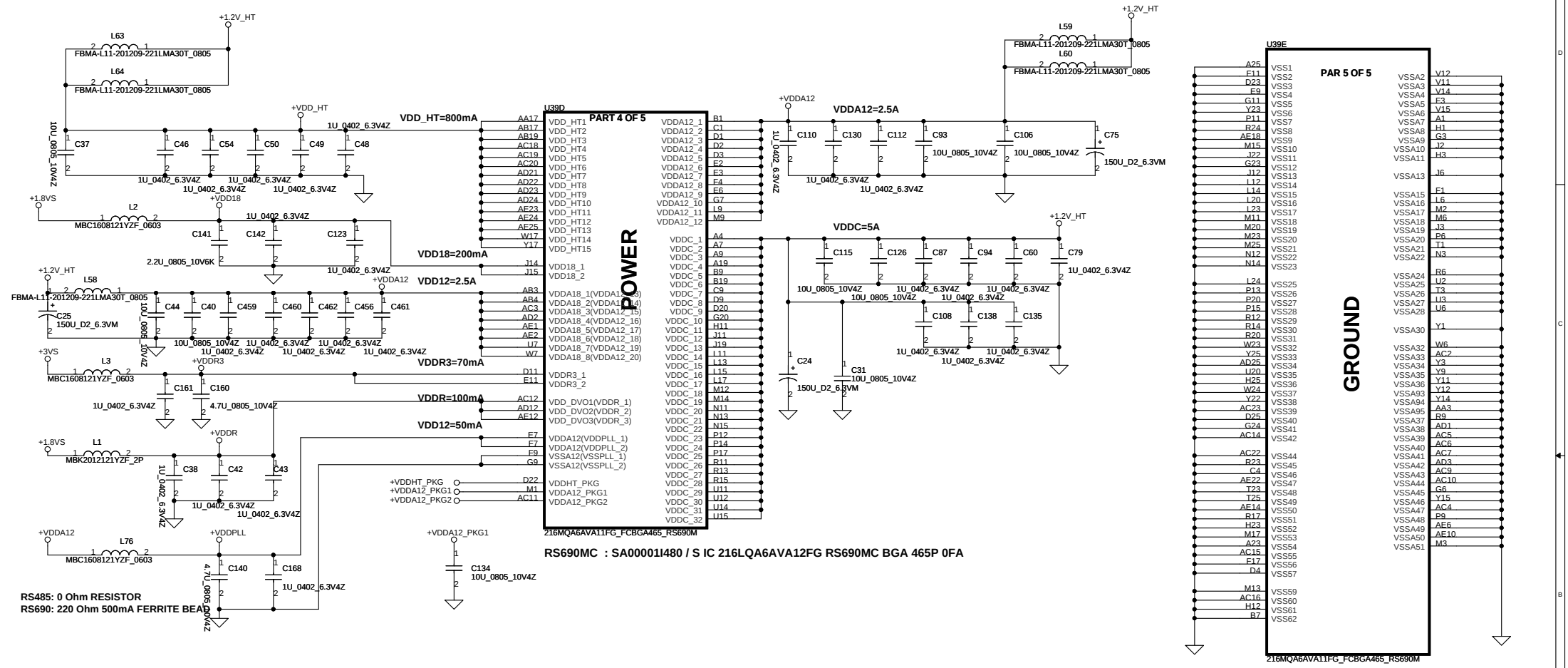
RS690MC : SA000011480 / S IC 216LQA6AVA12FG RS690MC BGA 465P 0FA

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RS690		RS690 only		
PULL HIGH (internally pulled high)	DFT_GPIO0	DFT_GPIO1	DFT_GPIO[4:2]	DFT_GPIO5
	Memory side port not available	Bypass the loading of EEPROM straps and use Hardware default values	These pin straps are used to configure PCI-E GPP mode: 111: register defined (register default to Config E) 110: 4-0-0-0 Config A 101: 4-4 Config B 100: 4-2-2 Config C 011: 4-2-1-1 Config D	Enable debug bus via the memory IO pads, if available in the package use default values
PULL LOW	Memory side port available	I2C Master can load strap values from EEPROM if connected, or use default values if not connected	010: 4-1-1-1 Config E others: register defined (register default to Config E)	DEFAULT

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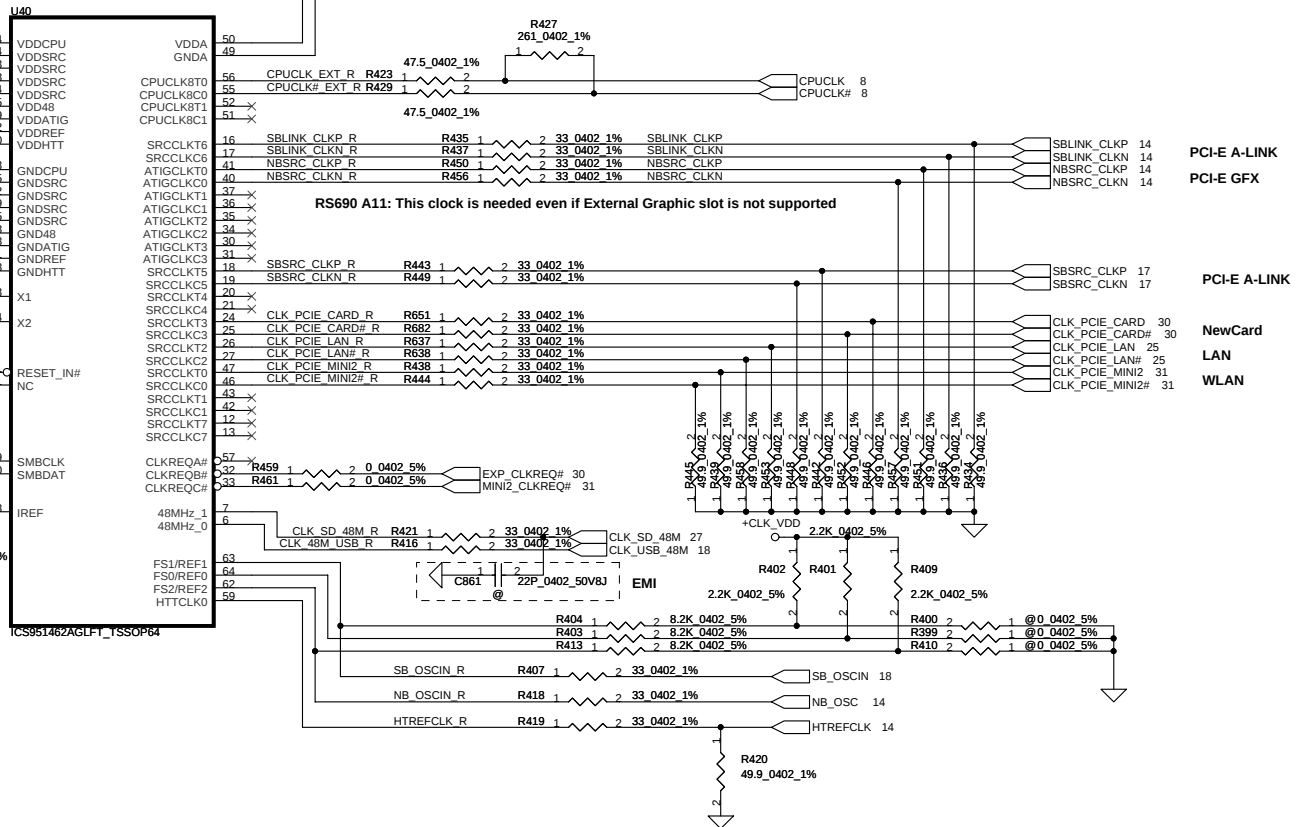
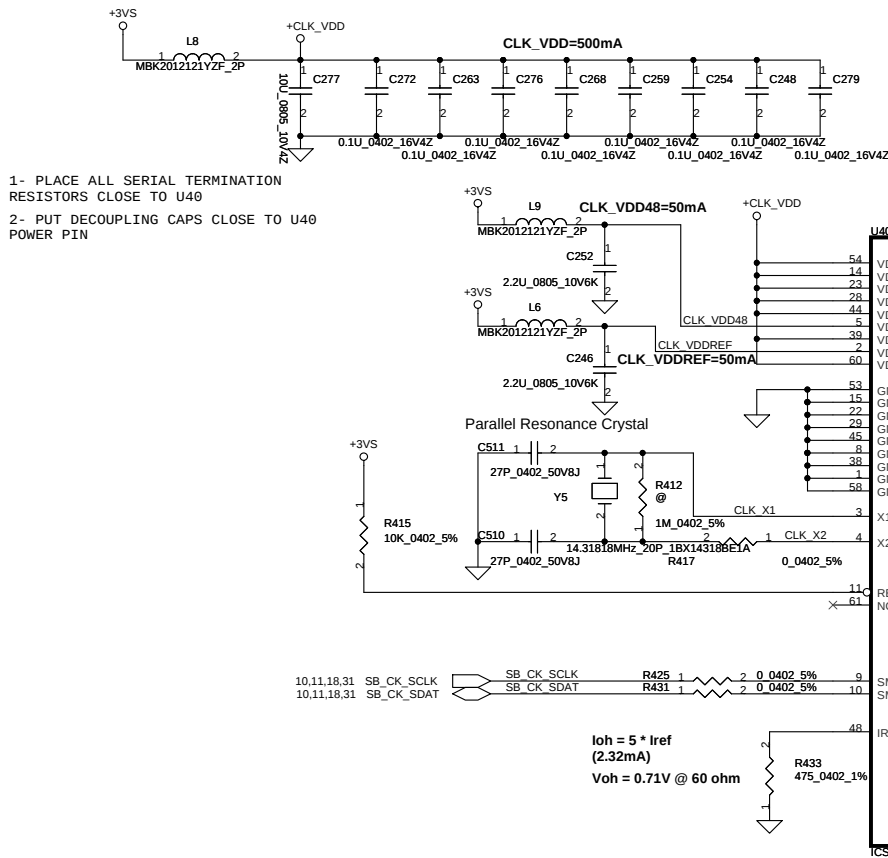
RS485: 0 Ohm RESISTOR
RS690: 220 Ohm 500mA FERRITE BEAD

RS690MC : SA00001I480 / S IC 216LQA6AVA12FG RS690MC BGA 465P 0FA

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GROUND

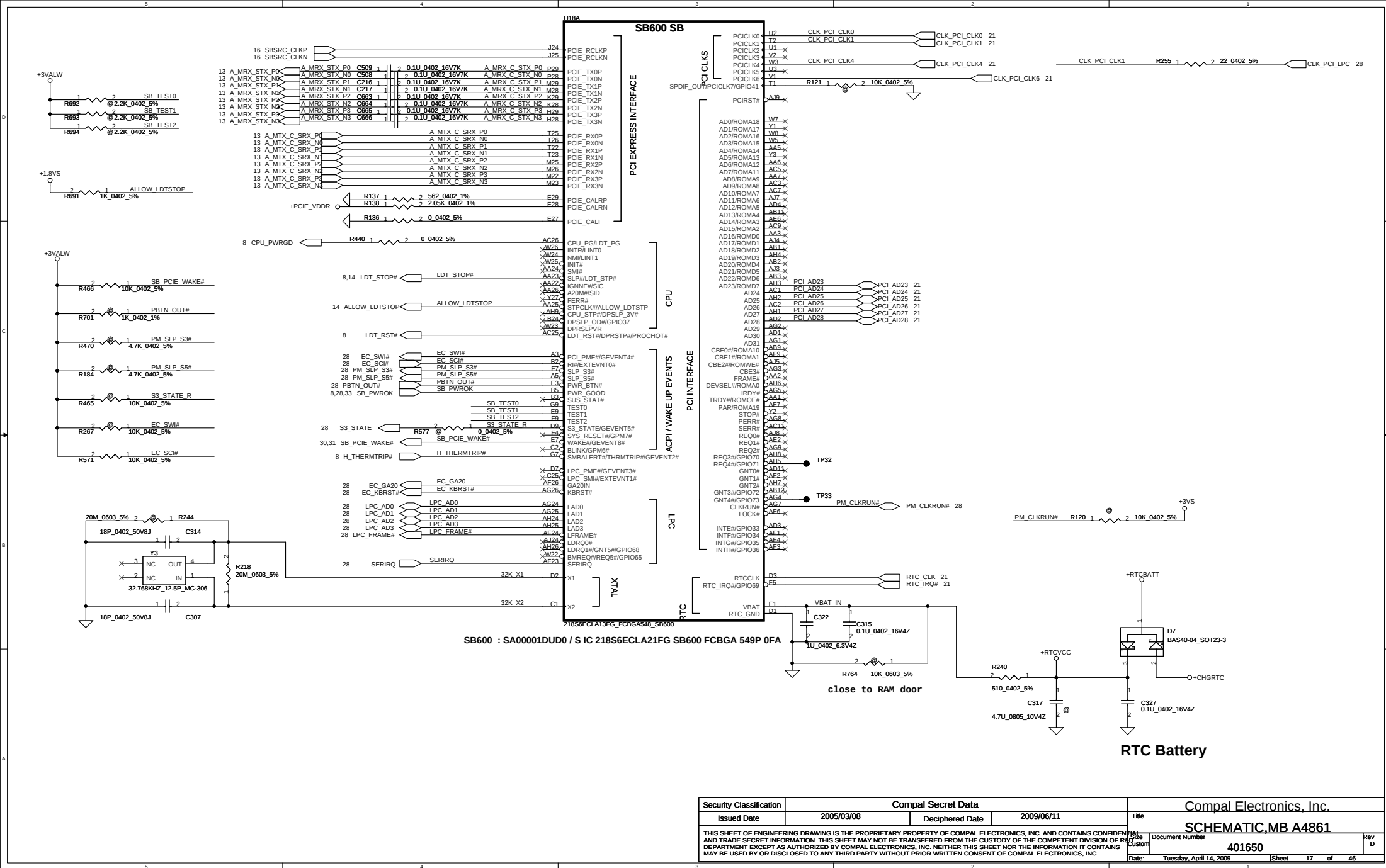
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EXT CLK FREQUENCY SELECT TABLE(MHZ)

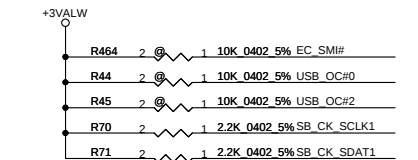
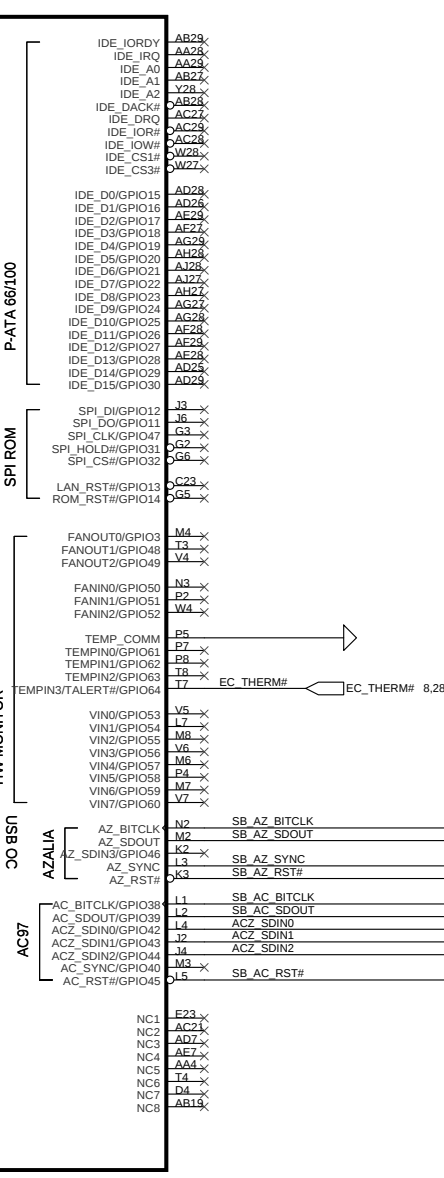
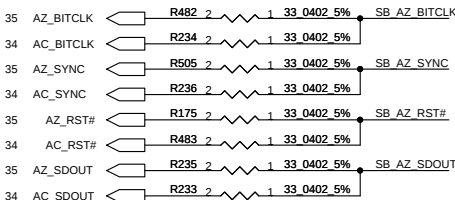
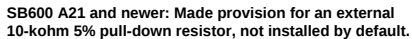
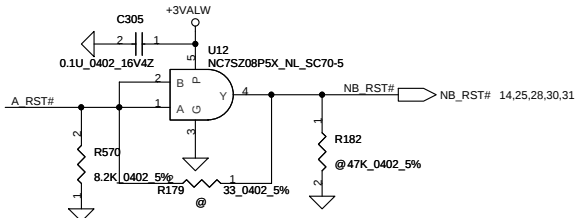
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

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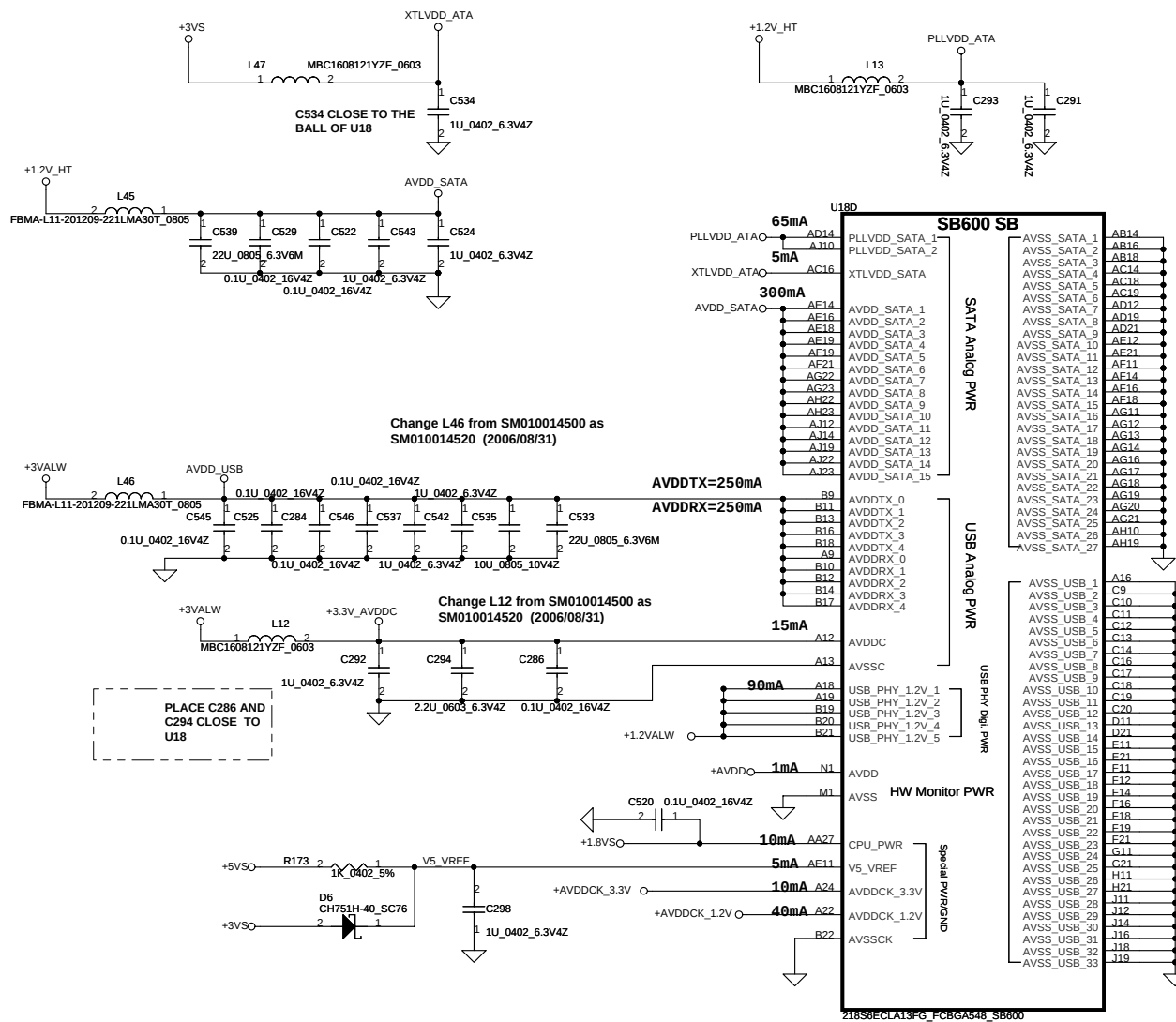


PORT0 : MAIN HDD
PORT1 : SECOND HDD
PORT2 : MAIN ODD
PORT3 : SECOND ODD

22	SATA STX C DRX P0	SATA STX C DRX P0	0.01U 0402 167K 1	2	C554	SATA STX DRX P0	A
22	SATA STX C DRX P0	SATA STX C DRX P0	0.01U 0402 167K 1	2	C554	SATA STX DRX P0	A
22	SATA STX C DRX P1	SATA STX C DRX P1	0.01U 0402 167K 1	2	C556	SATA STX DRX P1	A
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22	SATA DTX C SRX P3	SATA DTX C SRX P3	0.01U 0402 167K 1	2	C585	SATA DTX SRX P3	A
22	SATA DTX C SRX P3	SATA DTX C SRX P3	0.01U 0402 167K 1	2	C585	SATA DTX SRX P3	A
22	SATA DTX C SRX N3	SATA DTX C SRX N3	0.01U 0402 167K 1	2	C586	SATA DTX SRX N3	A

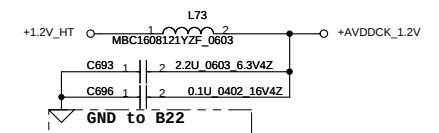
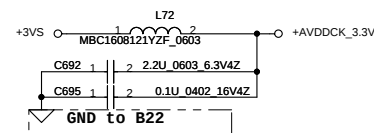
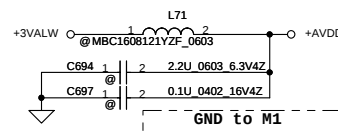
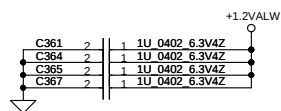


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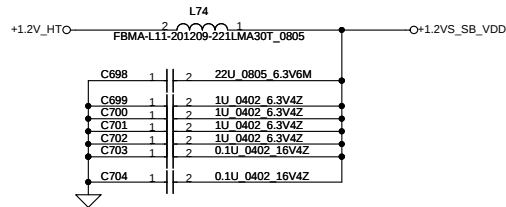
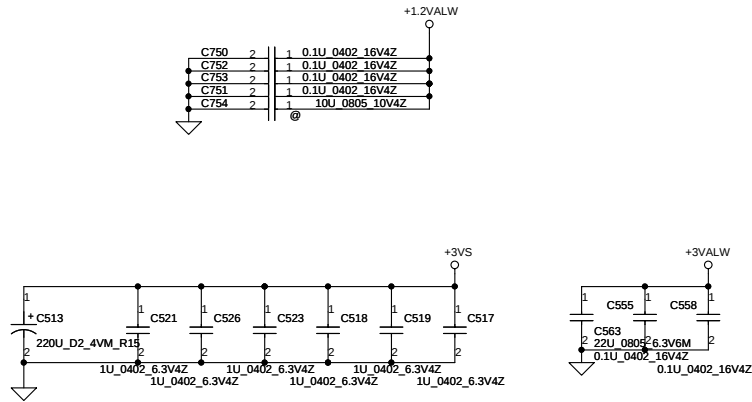


SB600 : SA00001DUD0 / S IC 218S6ECLA21FG SB600 FCBGA 549P 0FA

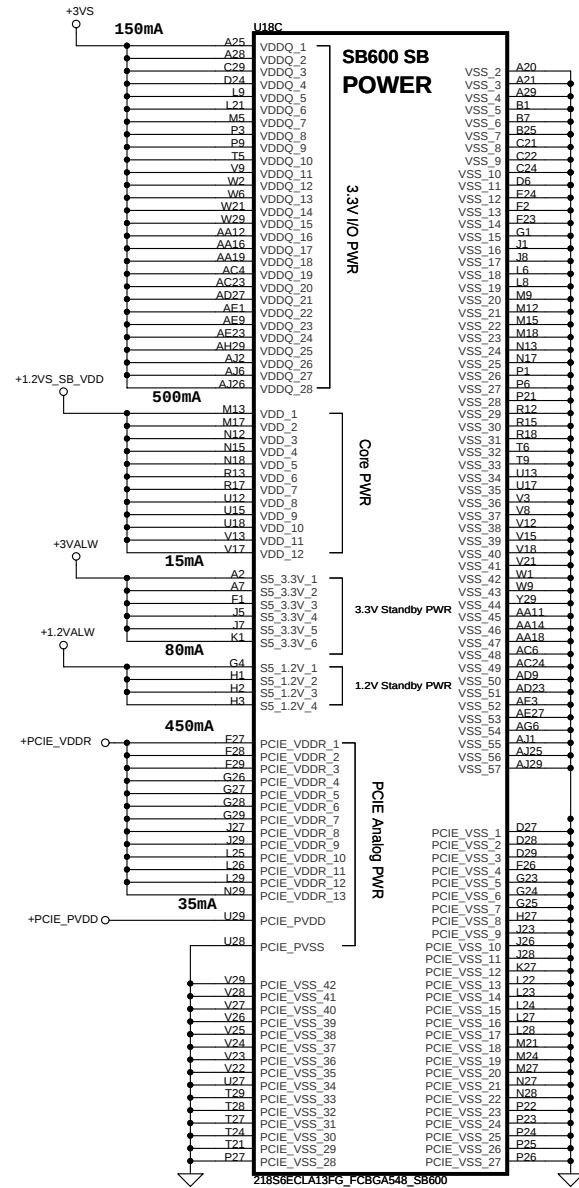
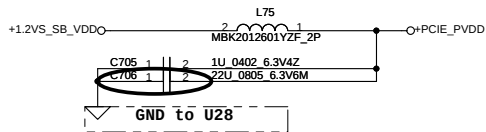
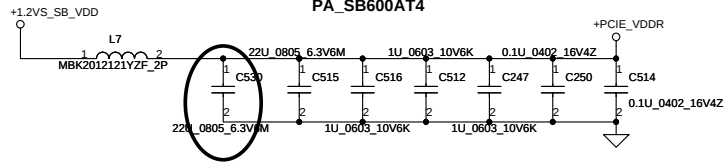
For AMD recommend change to +3.3V_S5



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Delay PCIE_VDDR / PCIE_PVDD
Add C530 to 22u
PA_SB600AT4

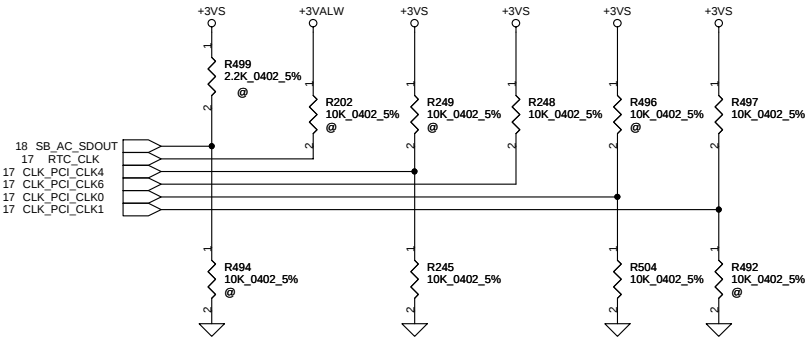


SB600 : SA00001DUD0 / S IC 218S6ECLA21FG SB600 FCBGA 549P 0FA

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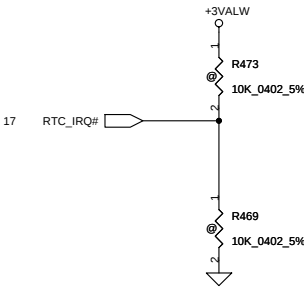
REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED



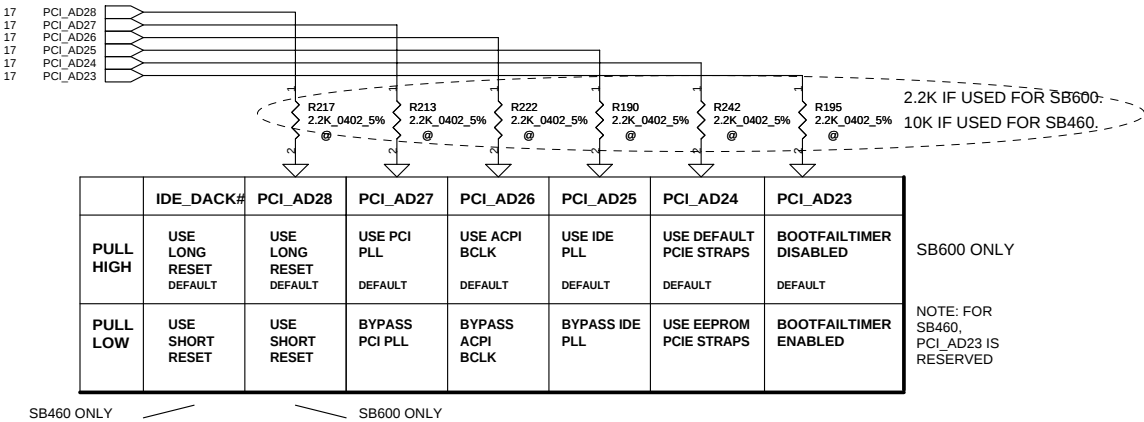
	AC_SDATA_OUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

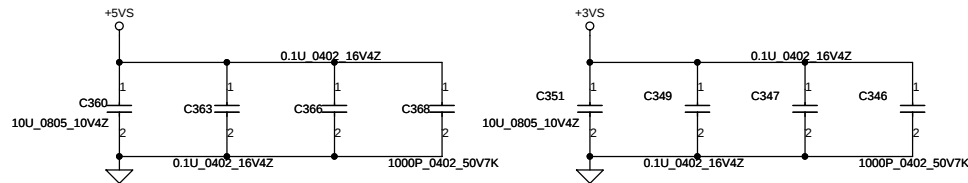
Internal RTC: Not connected. *
External RTC: Connected to IRQ# pin on external RTC.
External RTC supports S5 wake capability (from S5 power rail or battery).



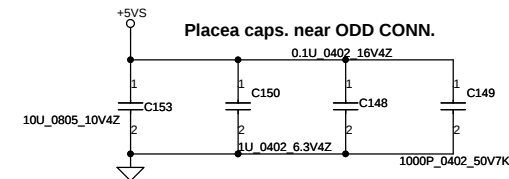
DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

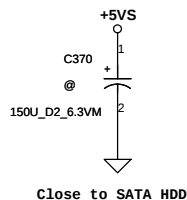
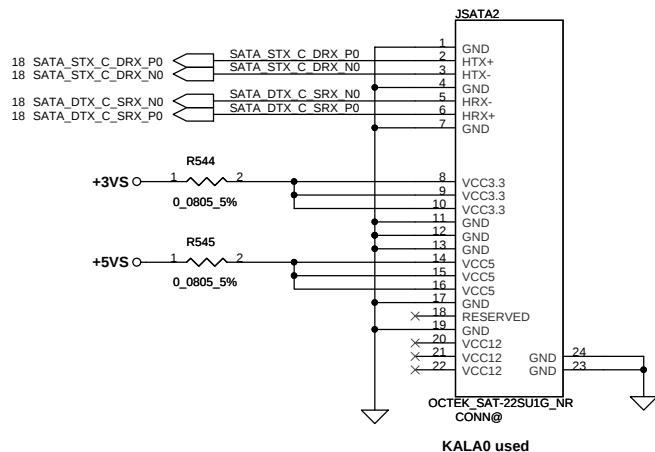




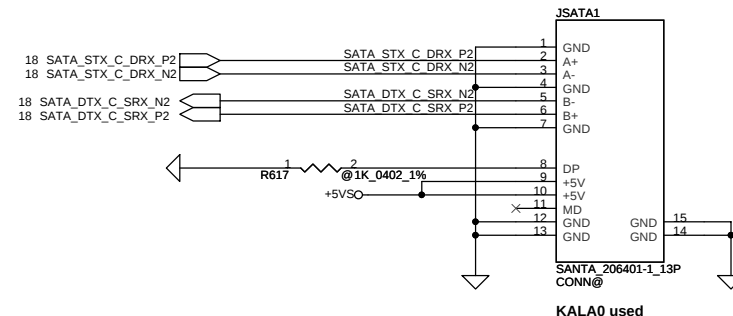
SATA HDD CONN



SATA ODD CONN



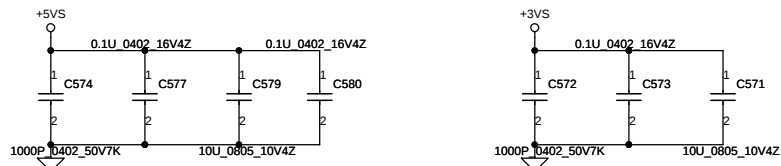
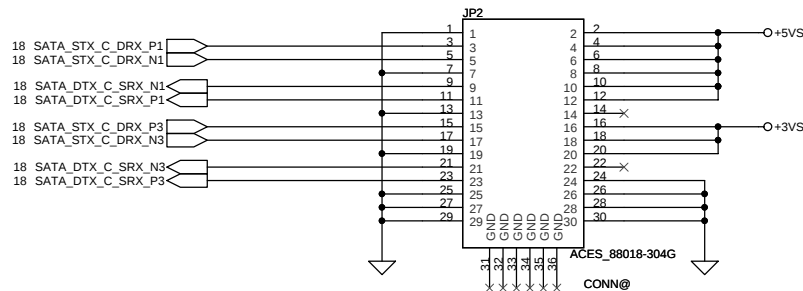
Close to SATA HDD



KALA0 used

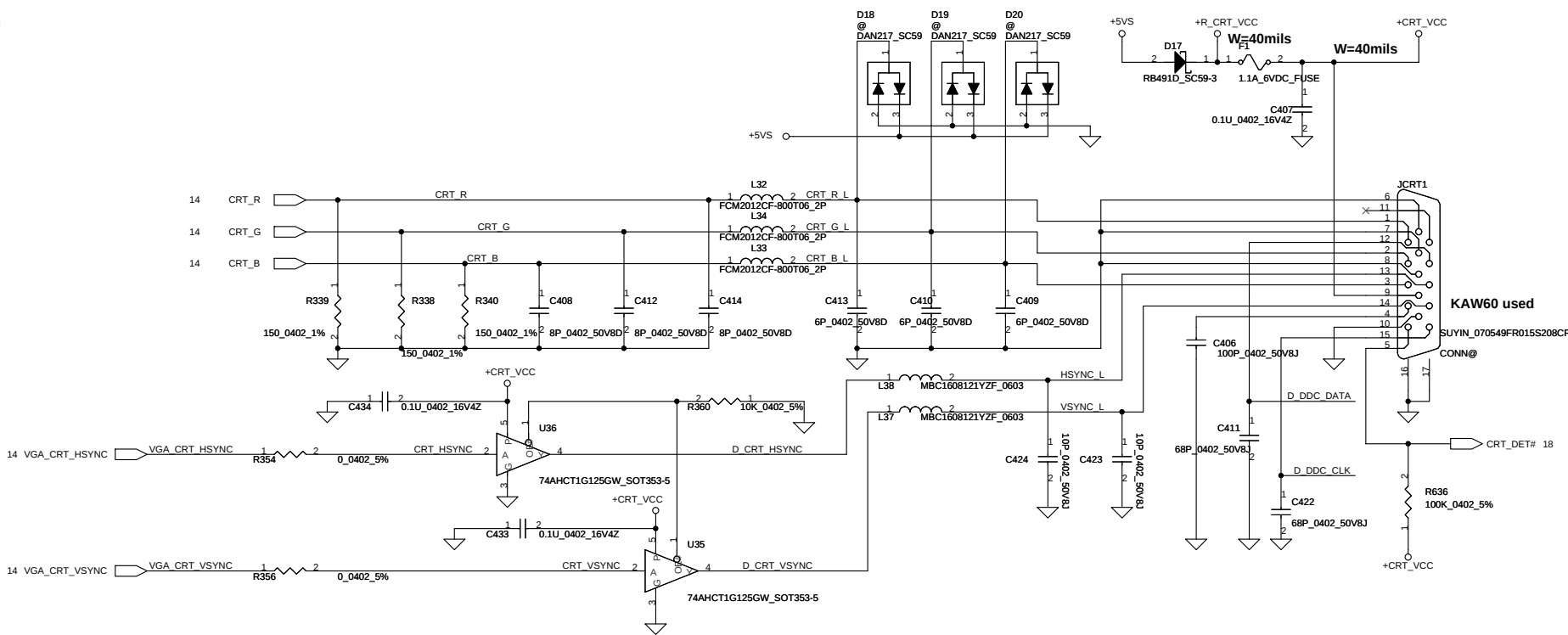
Second HDD

Second ODD

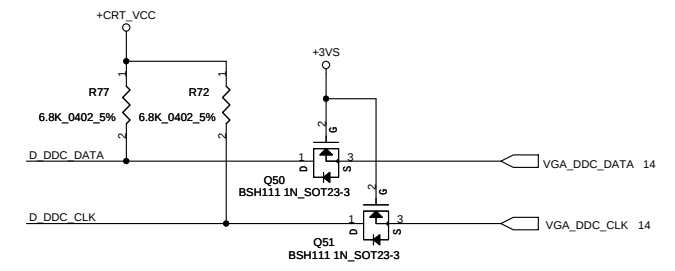


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CRT Connector

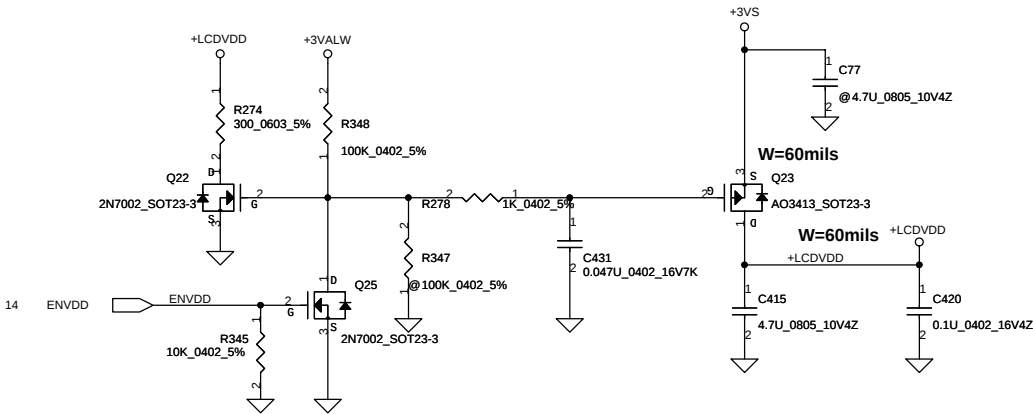


Close to Conn side

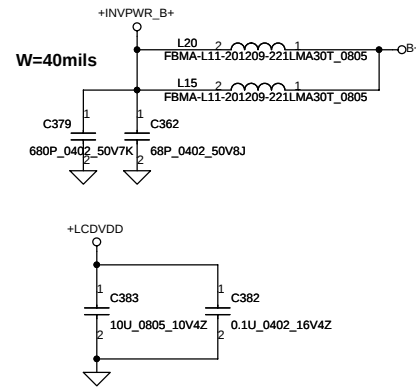
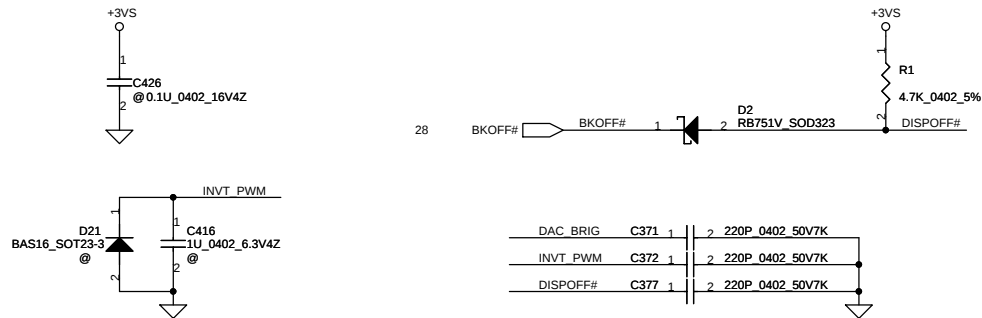
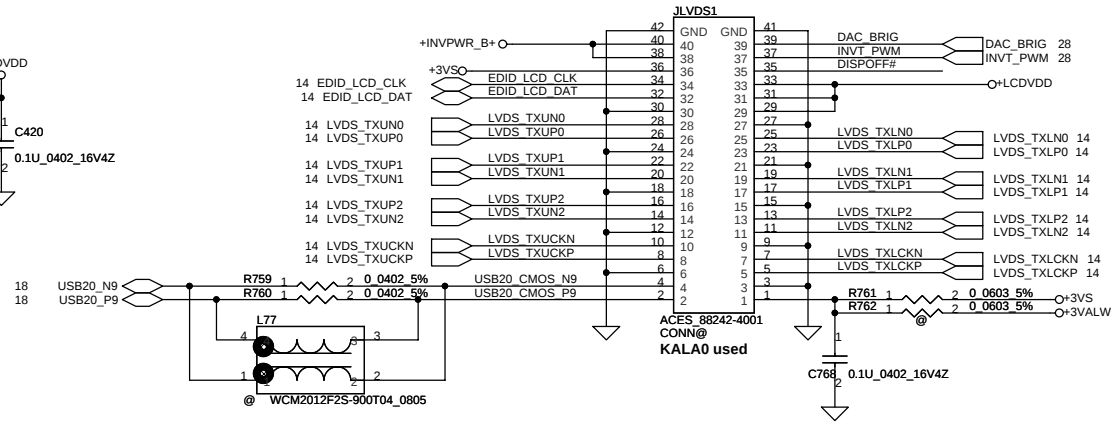


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				Date:	Tuesday, April 14, 2009
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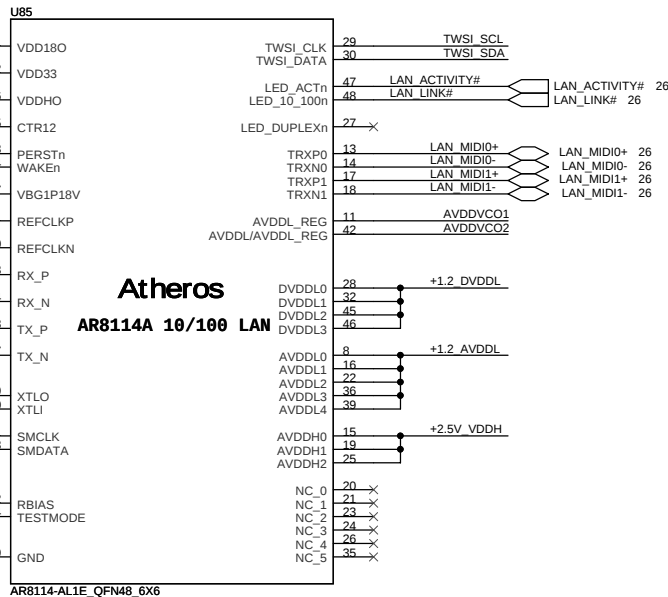
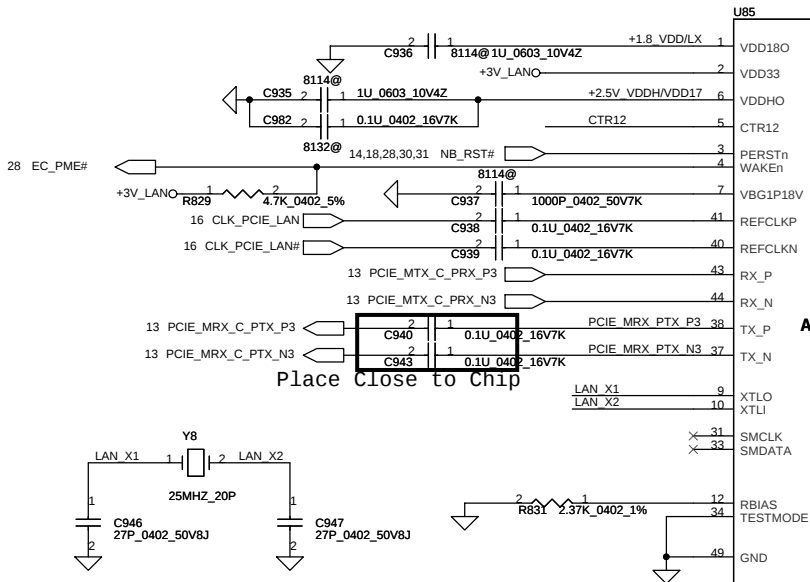
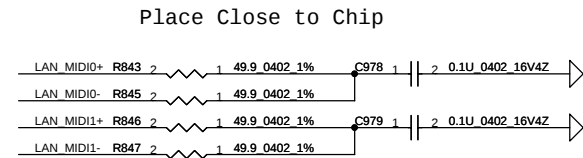
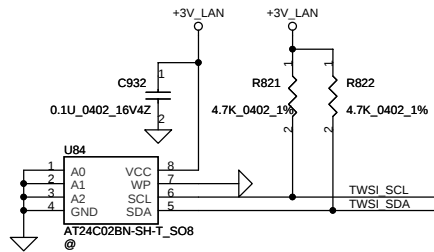
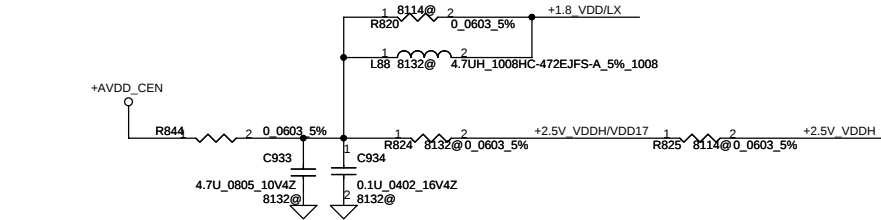
LCD POWER CIRCUIT



LCD/PANEL CONN.

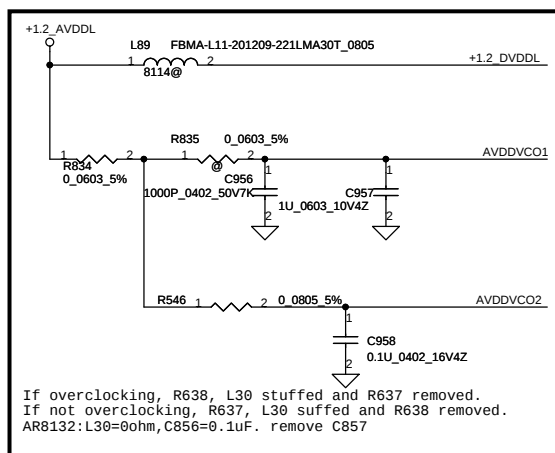


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						Date:	Tuesday, April 14, 2009		Sheet	24	of	46

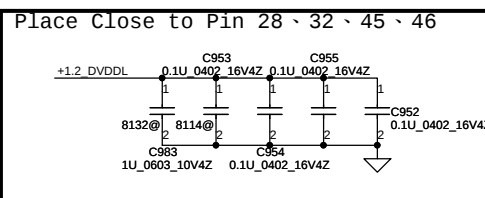


change AR8132-AL1E for pre-PVT

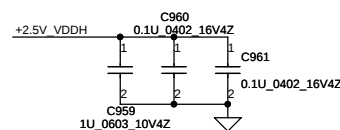
For AR8131V1



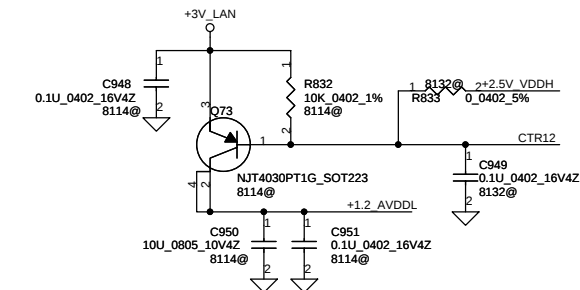
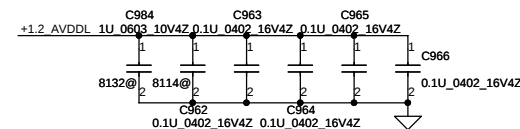
If overclocking, R638, L30 stuffed and R637 removed.
If not overclocking, R637, L30 stuffed and R638 removed.
AR8132: L30=90ohm, C856=0.1uF. remove C857



Place Close to Pin15、19、25

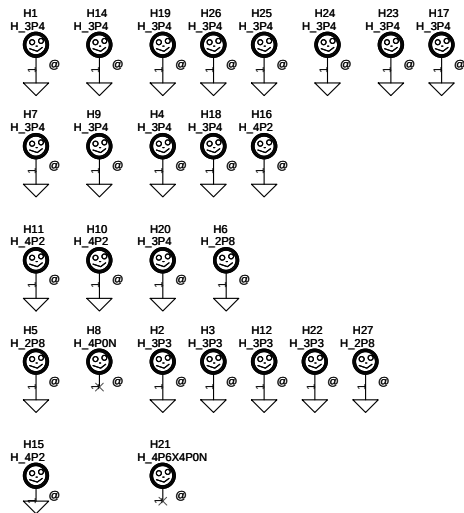
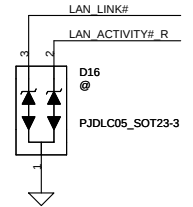
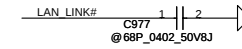
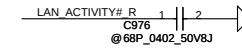
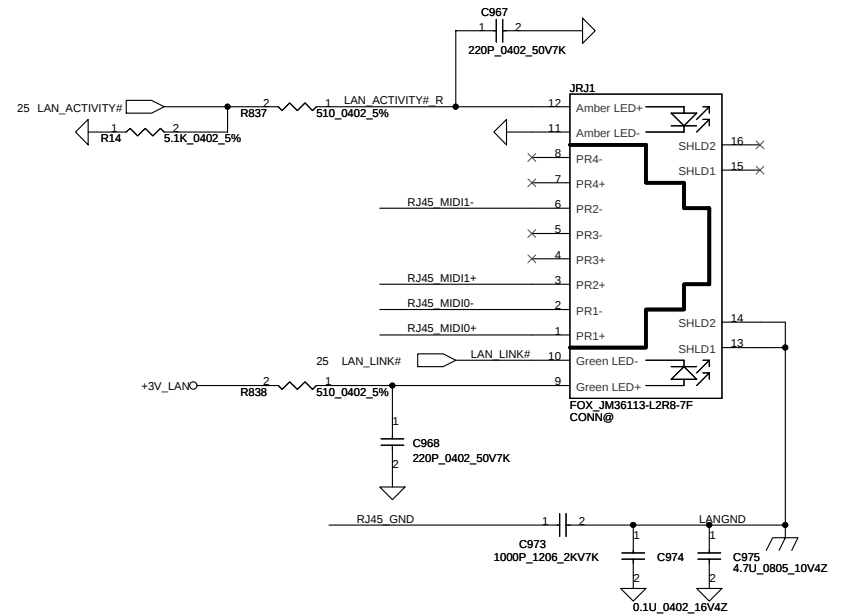
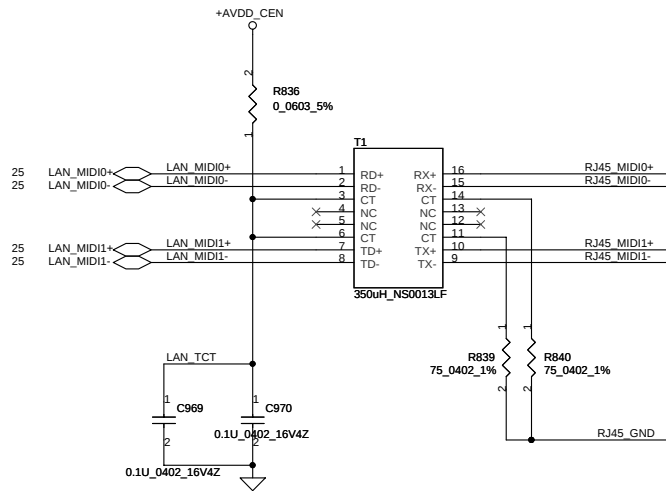


Place Close to Pin8、16、22、36、39

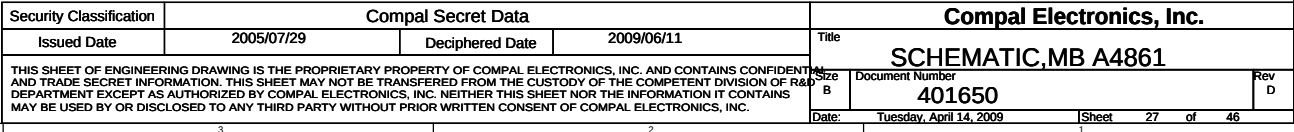


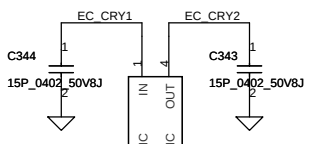
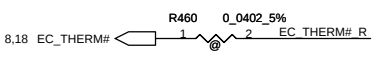
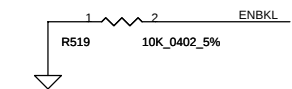
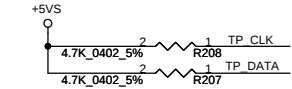
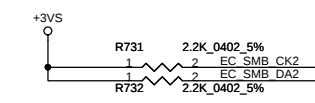
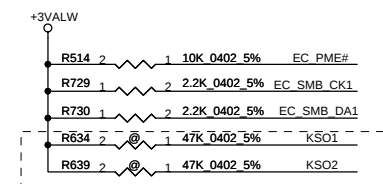
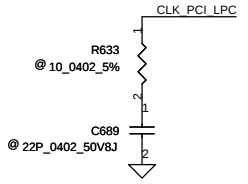
Layout Notice : Close to chip

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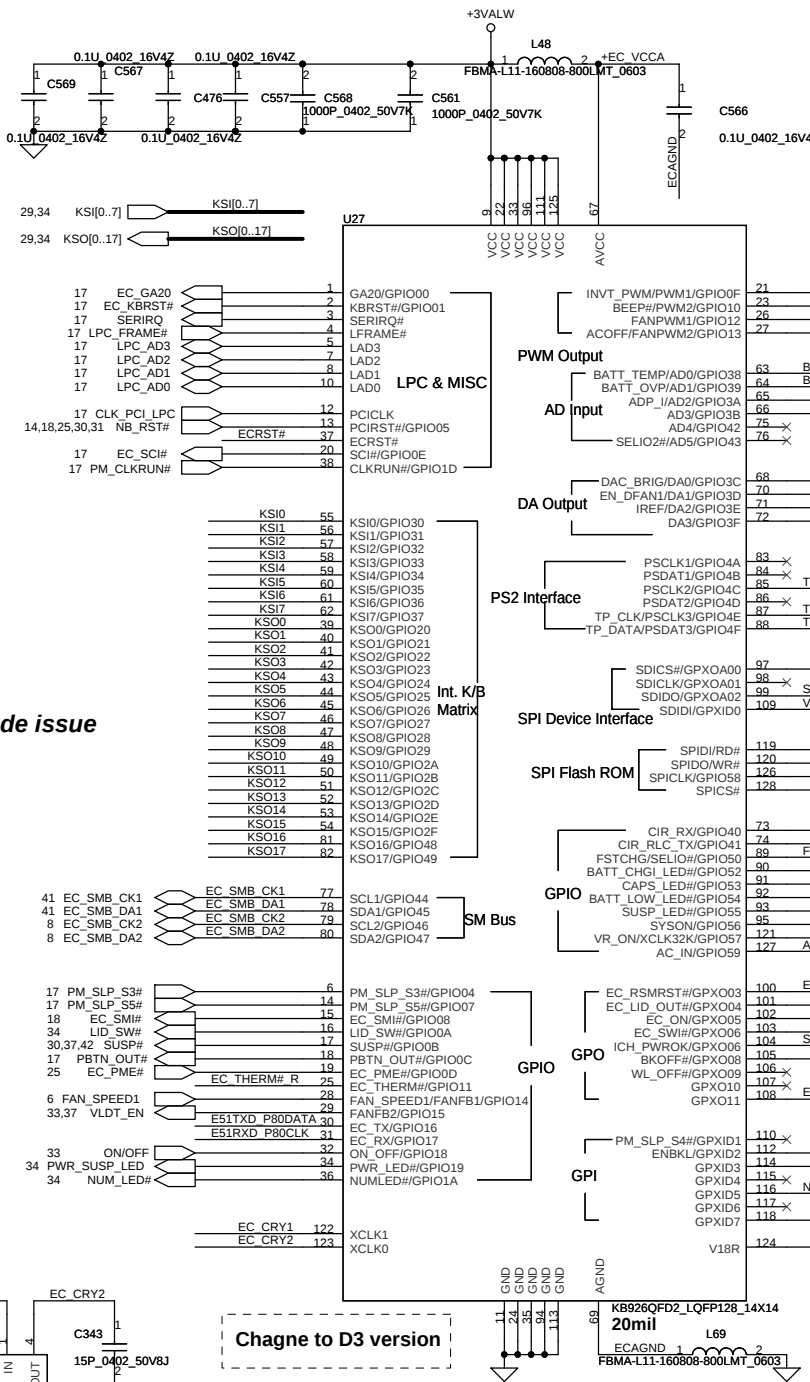


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				Date: Tuesday, April 14, 2009	Sheet 26 of 46

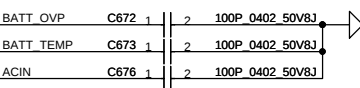




32.768KHZ_12.5P_MC-306

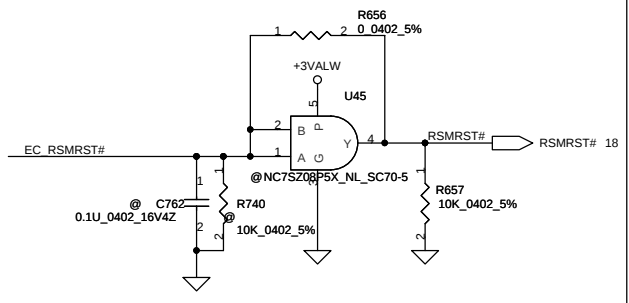
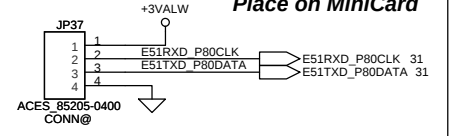


Please close to EC pin

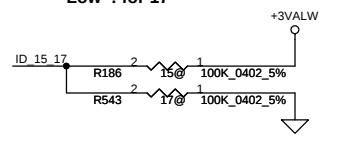


For EC Tools

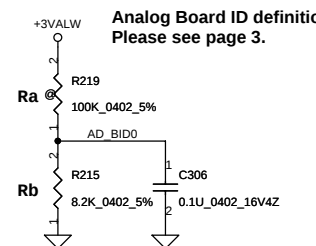
Place on MiniCard



ID DETECT
High : for 15"
Low : for 17"

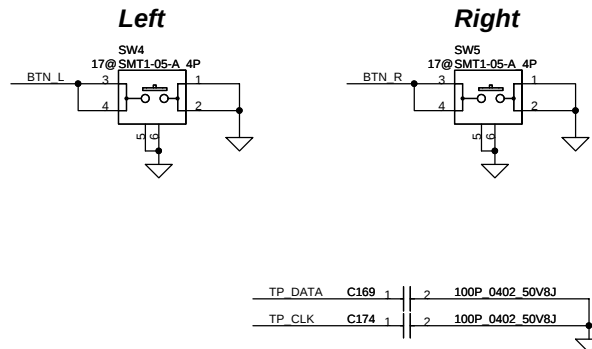


Analog Board ID definition,
Please see page 3.

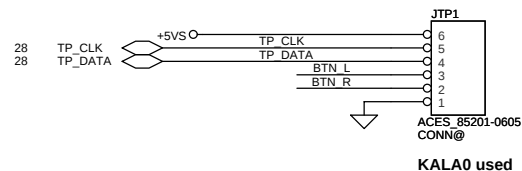


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				Custom	401650
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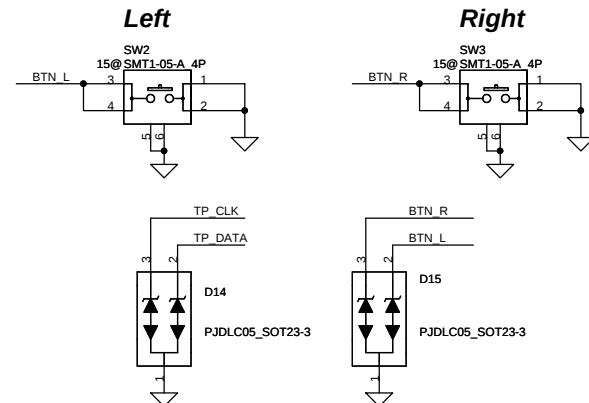
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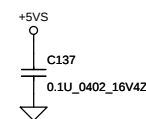
To TP/B Conn.



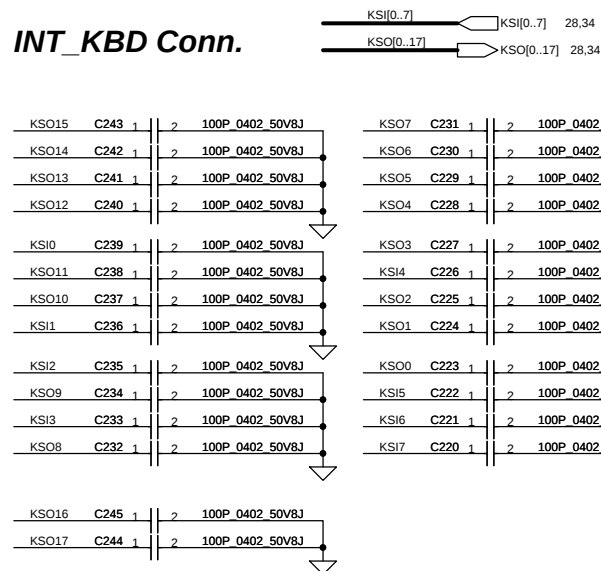
For 15"



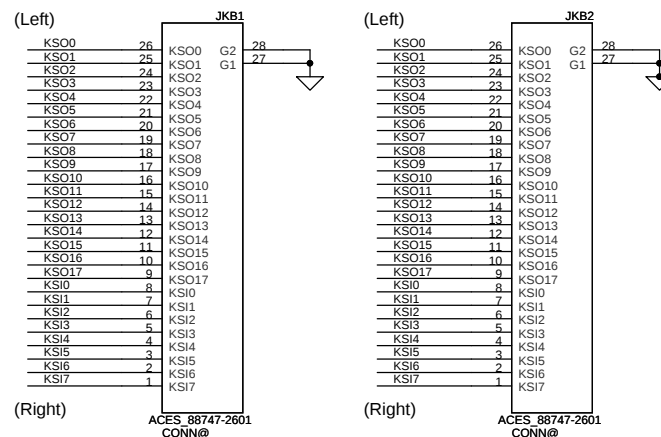
Change to SCA00000200



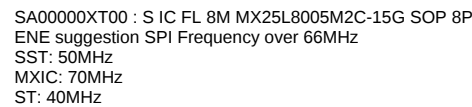
INT_KBD Conn.



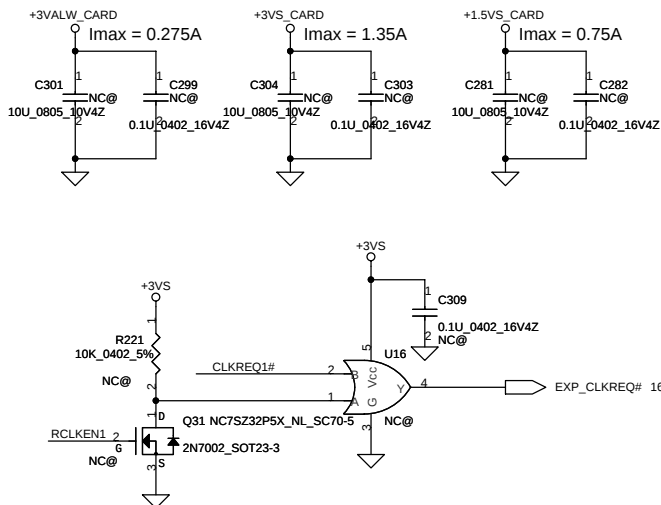
KB1 for 15"
KB2 for 17"



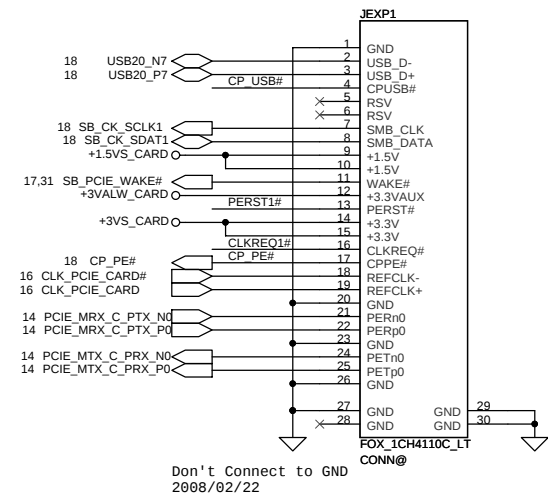
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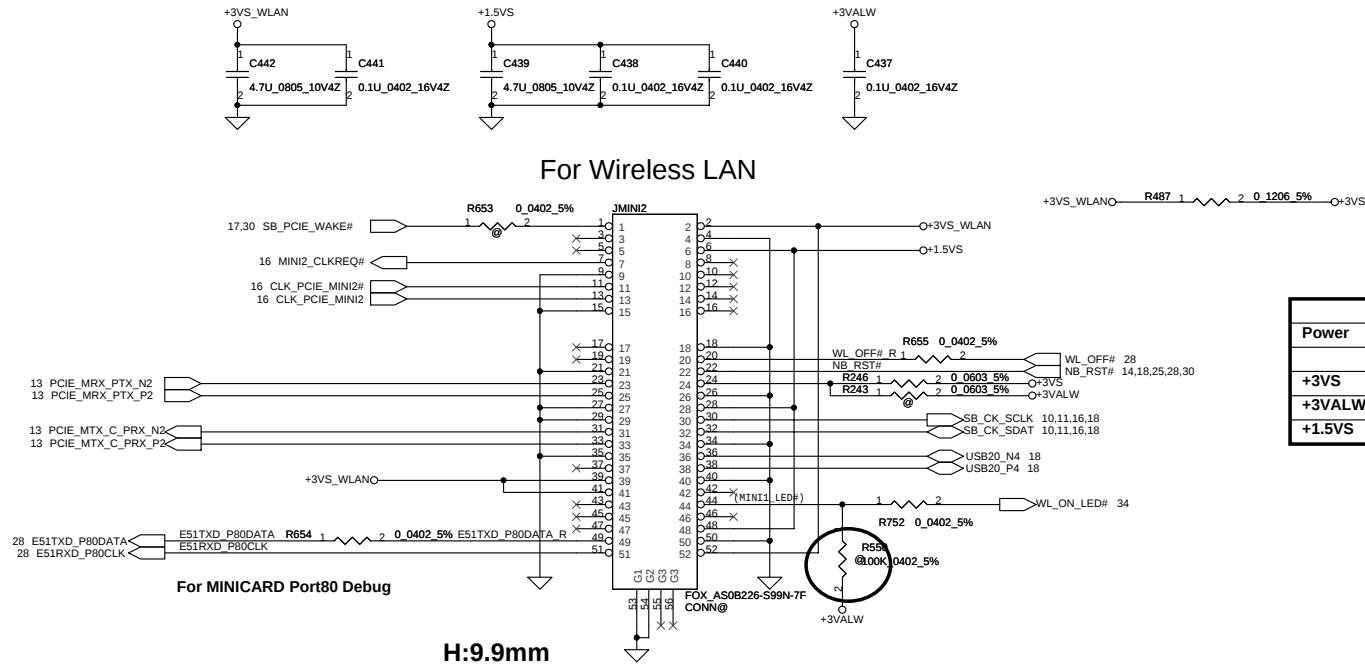
EC_SPICLK 1 2 @22_0402_5% R257 C296 1 2 @10P_0402_50V8J



New Card Socket (Left/TOP)



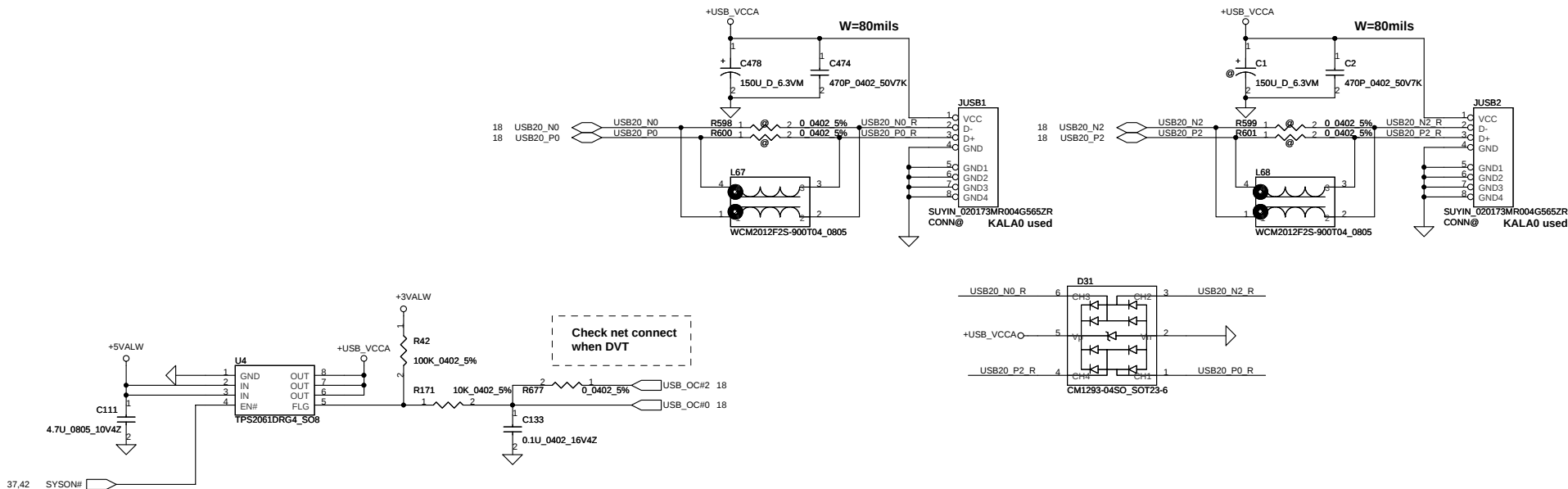
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Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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USB CONN. 1 & 2



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Power ON Circuit

The Power ON Circuit schematic shows a sequence of inverters (U10A, U10B, U10C, U10D, U10E, U10F) connected in series. The circuit starts with a VLDT_EN input, followed by a series of resistors (R100, R106, R109, R111, R112, R113, R104, R105, R108) and capacitors (C203, C204). The final output is SB_PWROK. The circuit is powered by +3V and +3VALW. The components are labeled with their values and tolerances.

Timing diagram showing the relationship between VLDLT_EN, NB_PWRGD, SB_PWRGD, SUSP#, and +1.8VS. The diagram includes two time intervals, T1 and T2, marked by vertical dashed lines. VLDLT_EN is high during T1. NB_PWRGD is high during T1 and T2. SB_PWRGD is high during T2. SUSP# is high during T1 and T2. +1.8VS is high throughout.

Power Button

TOP Side

Bottom Side

34 ON/OFFBTN#

ON/OFFBTN#

1

2

3

51ON#

28

38

3V3LW

R765 10K_0603_5%

R766 10K_0603_5%

D10 DAN202UT106_SC70-3

ON/OFF

51ON#

38

C358 1000P_0402_50V7K

D11 RLZ20A_LL34

Q17 2N7002_SOT23

R290 10K_0402_5%

EC_ON

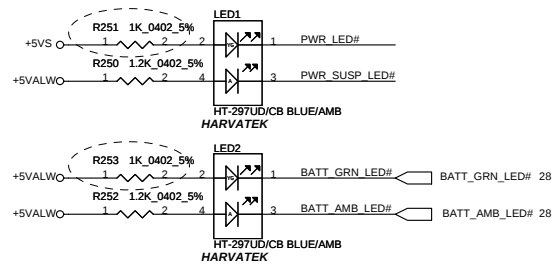
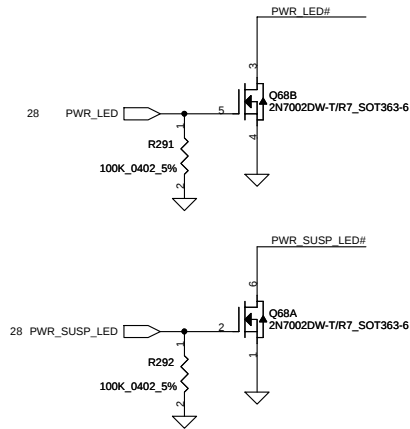
28

SW10 SMT1-05-A 4P

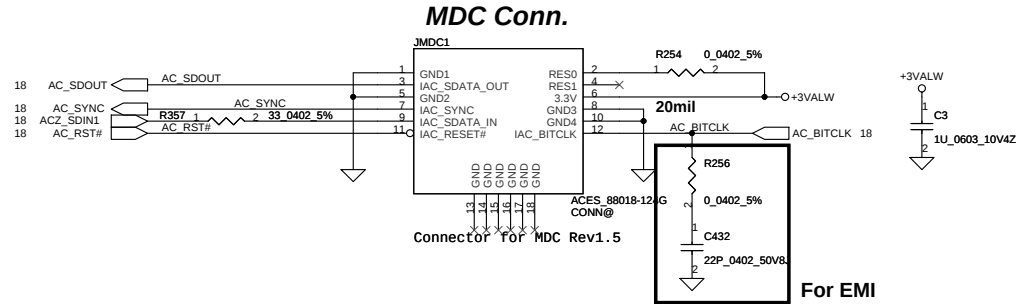
ON/OFFBTN#

MP would remove

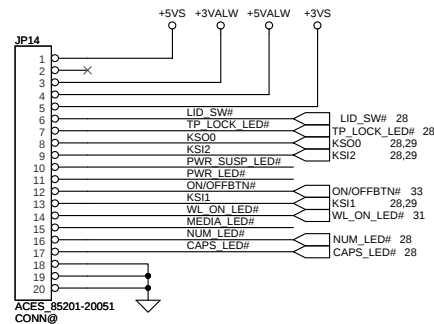
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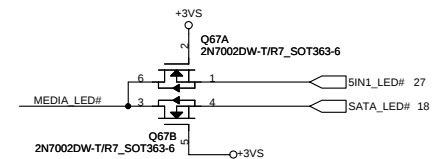
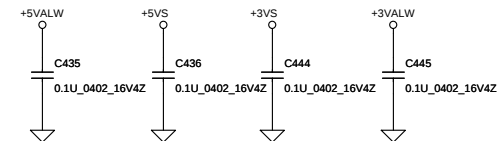
BLUE/AMB LED



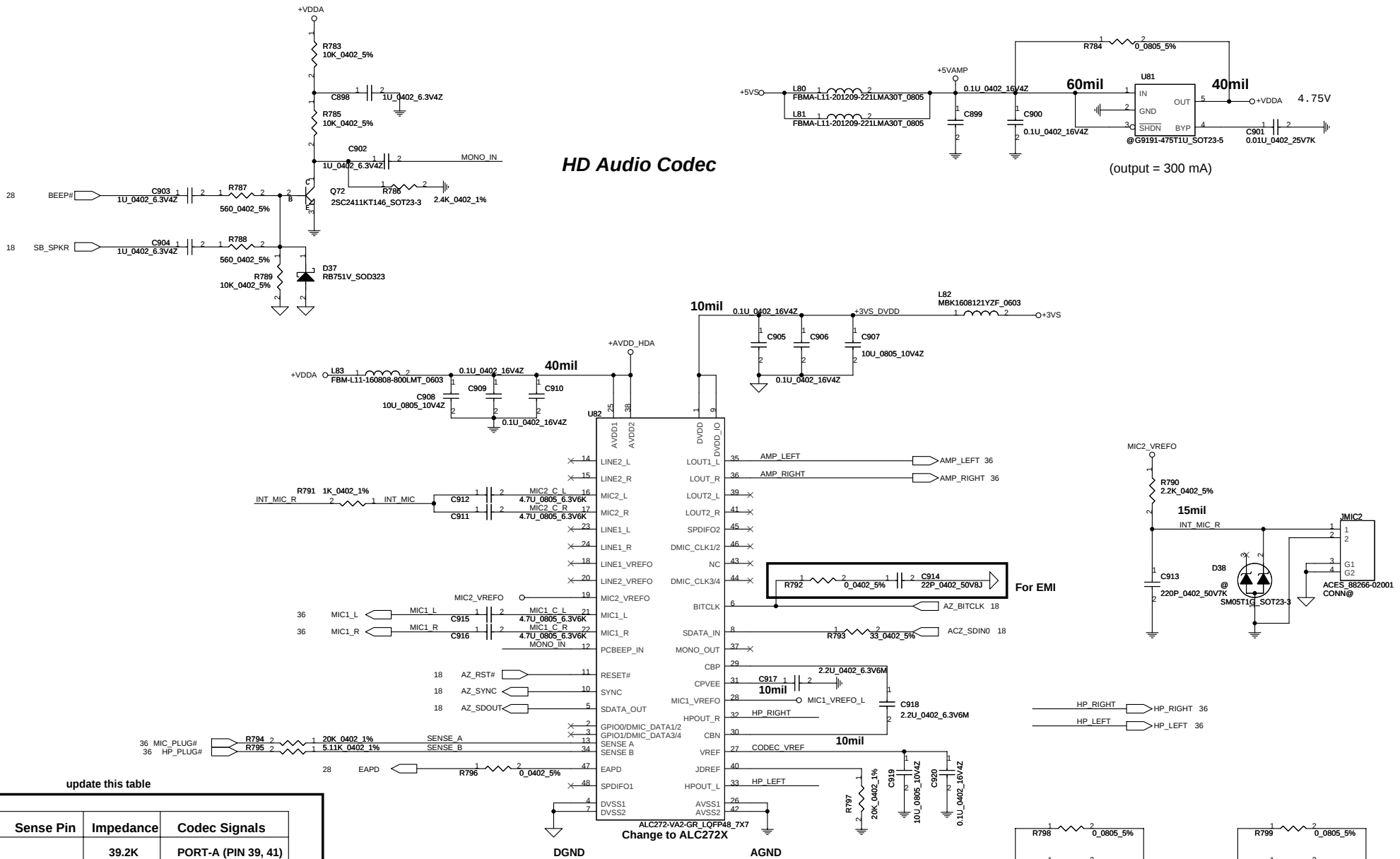
To PWR LED/B



	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



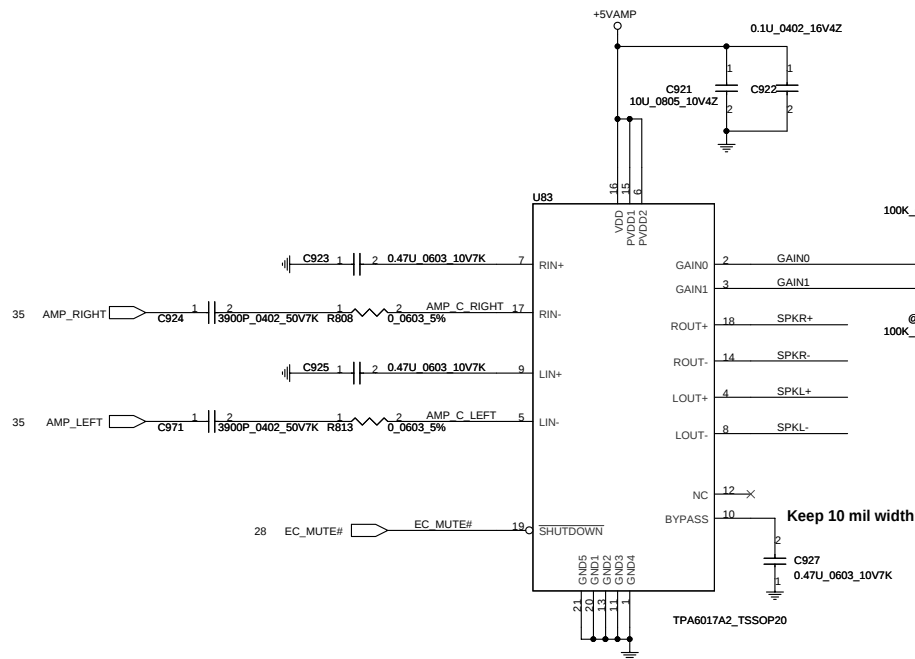
HD Audio Codec



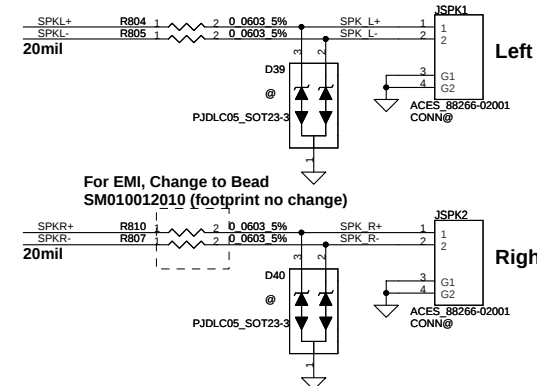
update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

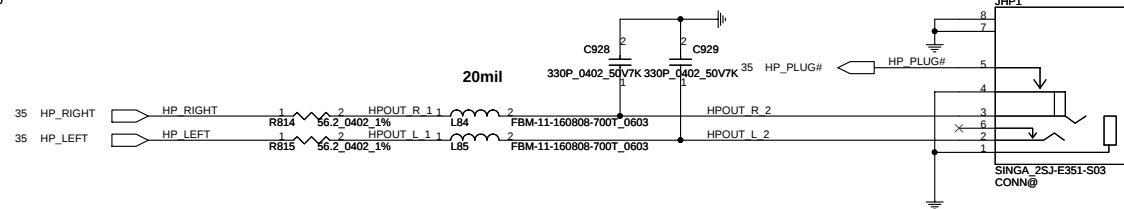
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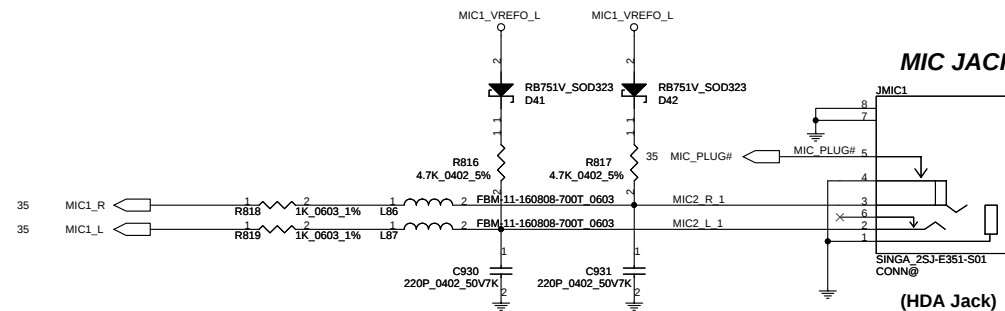
Int. Speaker Conn.



LINE Out/Headphone Out

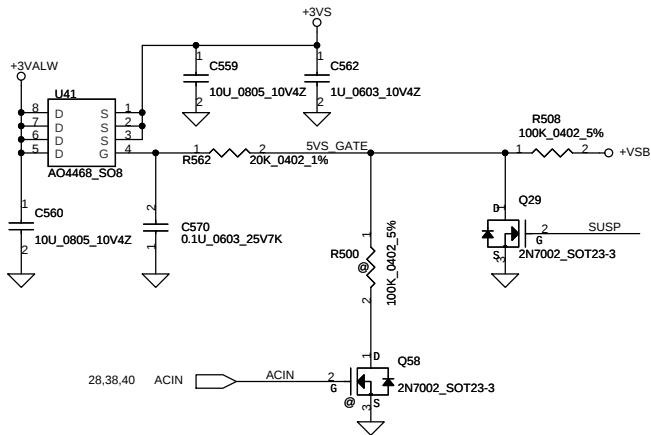


MIC JACK

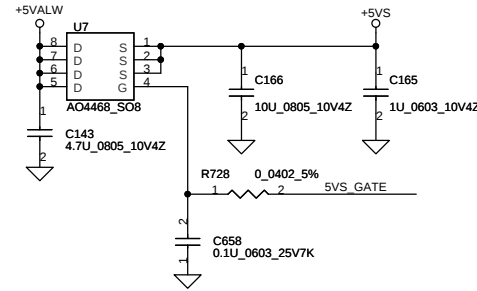


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								Document Number		D	
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								Date		Friday, April 10, 2009	

+3VALW TO +3VS

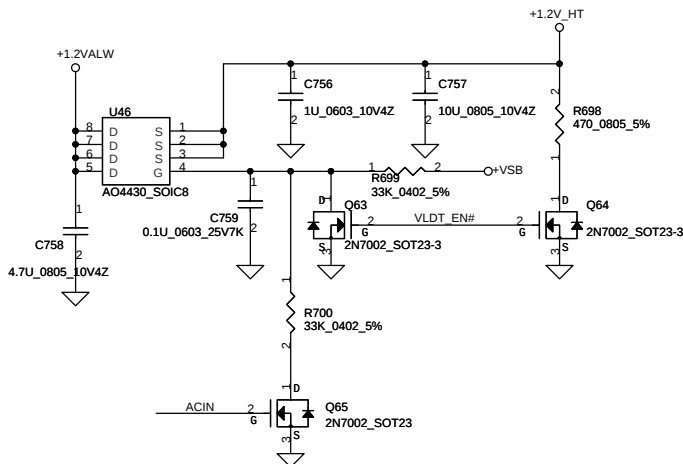


+5VALW TO +5VS

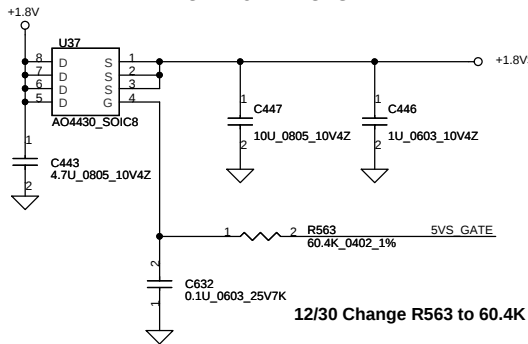


2006/2/22 Add C658 0.1uF

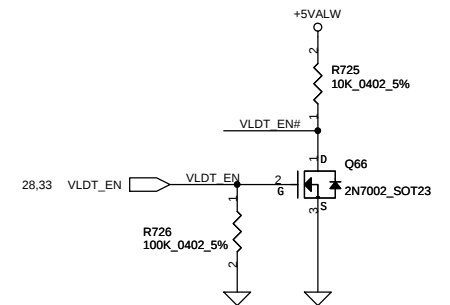
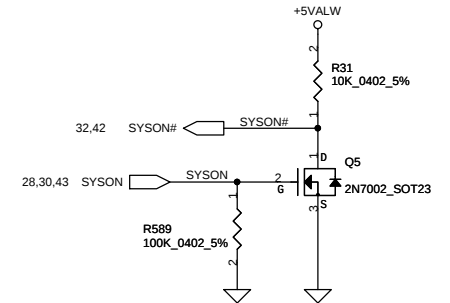
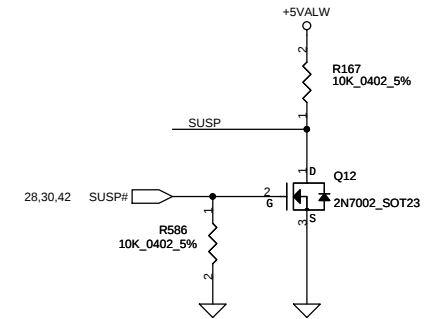
+1.2VALW TO +1.2V_HT



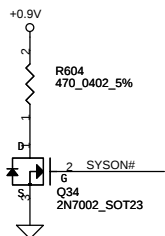
+1.8V TO +1.8VS



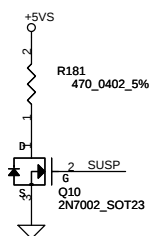
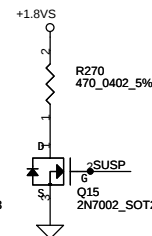
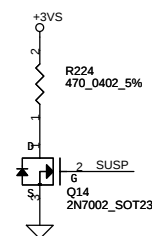
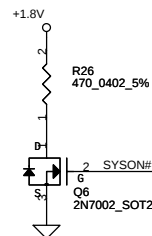
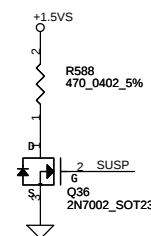
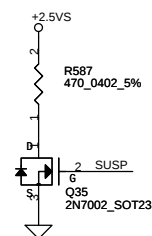
12/30 Change R563 to 60.4K



Near PU8

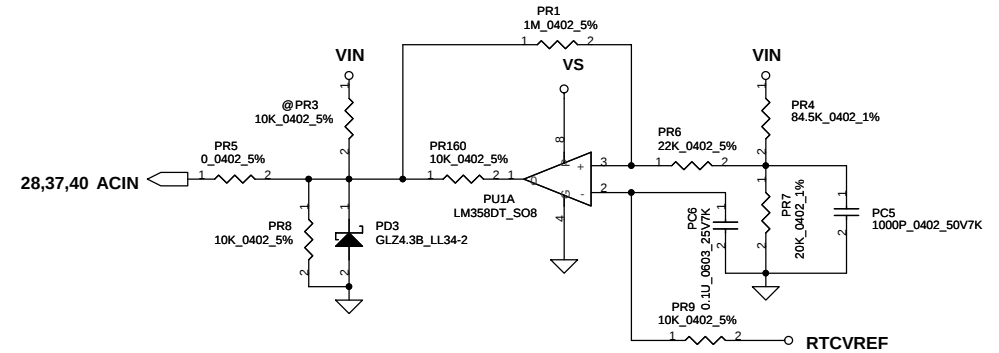
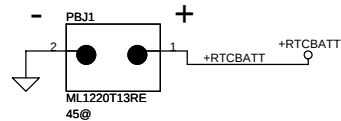
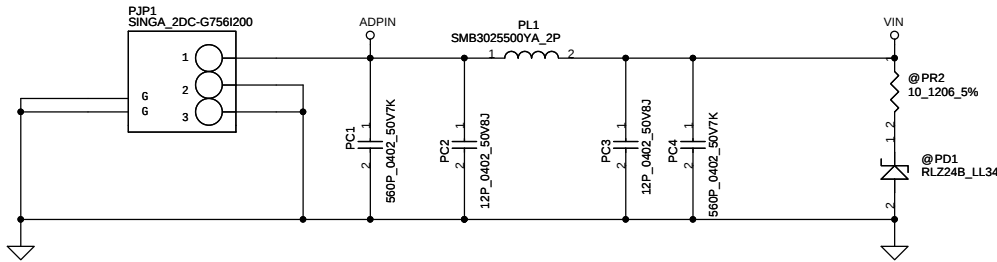


Near PU12

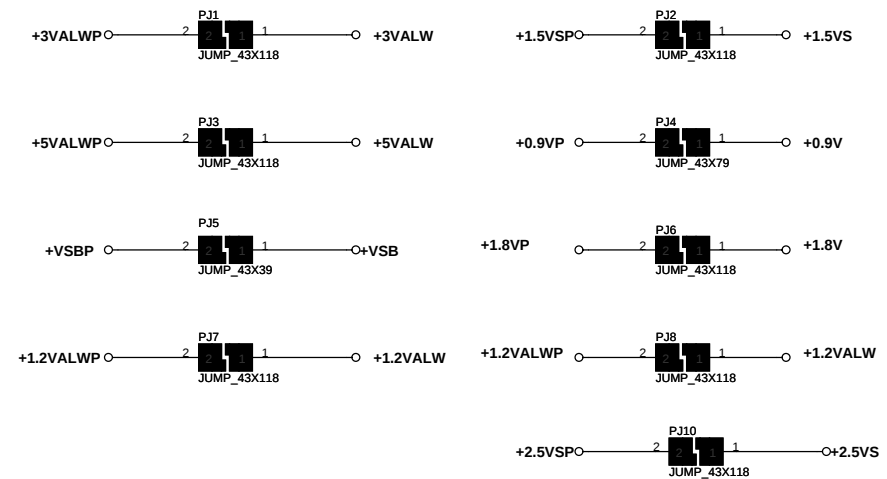
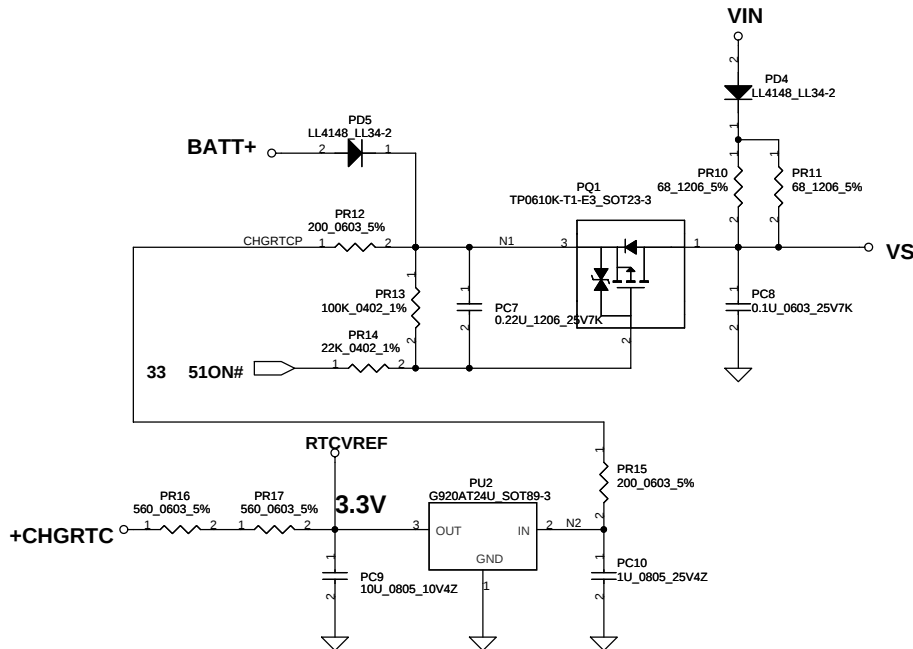


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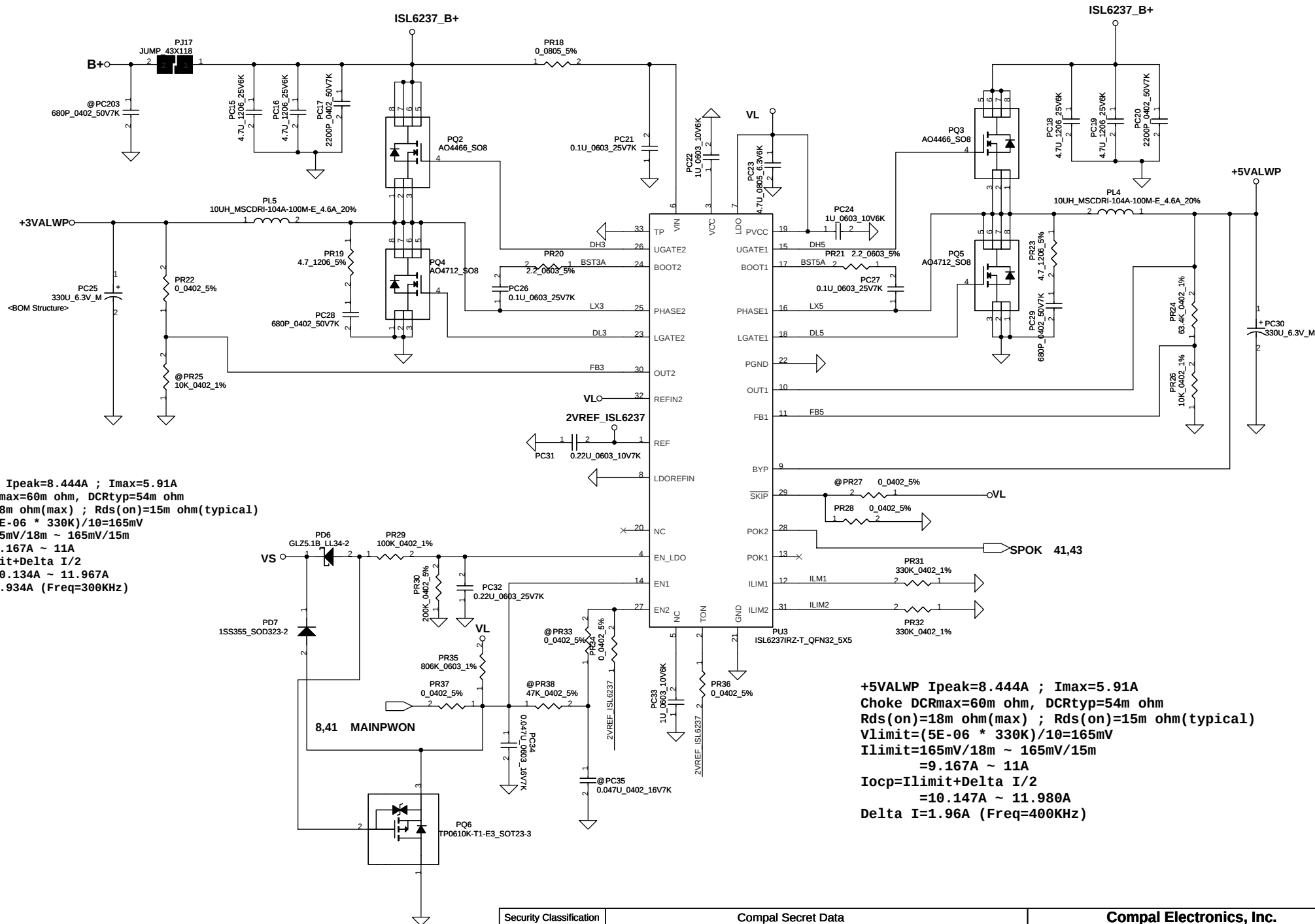
DC231000500



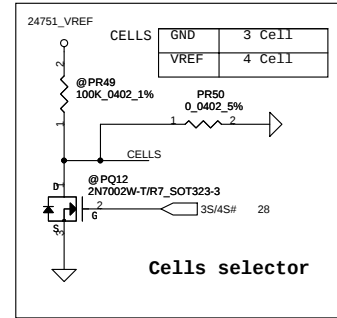
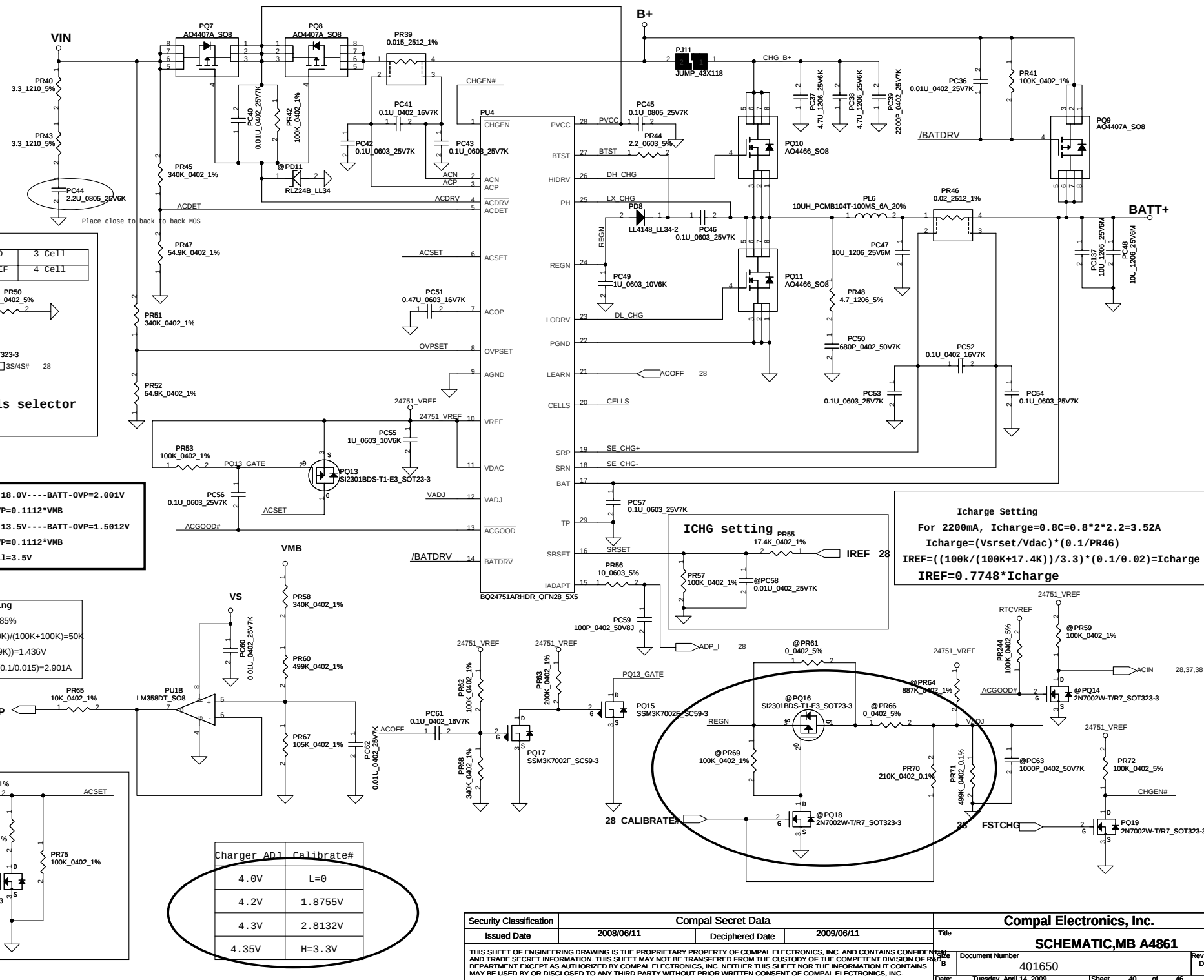
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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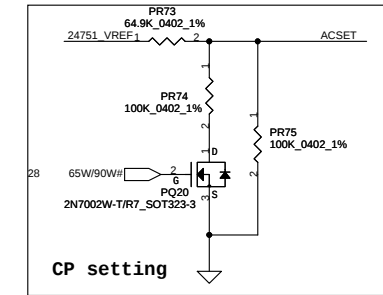
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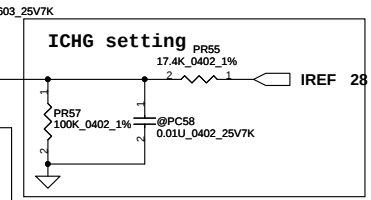
Input OVP : 22.3V
Input UVP : 17.26V
Fsw = 300KHz

LI-4S :18.0V----BATT-OVP=2.001V
BATT-OVP=0.1112*VMB
LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

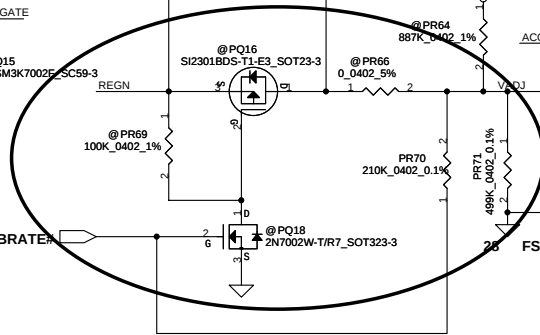
CP Point Setting
CP point=ladapter*85%
65W adapter R=(100K*100K)/(100K+100K)=50K
Vacset=3.3*(50K/(50K+64.9K))=1.436V
CP POINT=(1.436V/3.3V)*(0.1/0.015)=2.901A



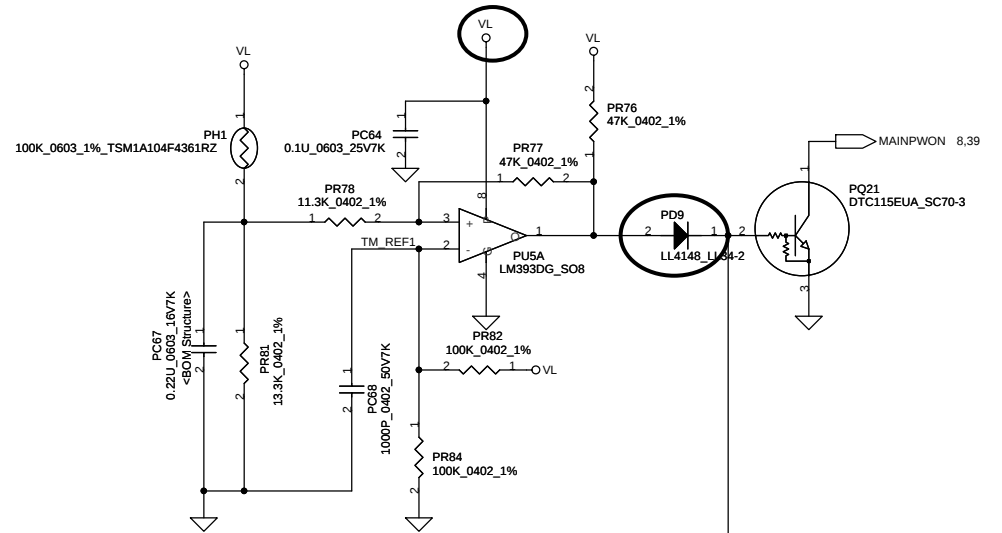
Charger AD1_Calibrate#	
4.0V	L=0
4.2V	1.8755V
4.3V	2.8132V
4.35V	H=3.3V



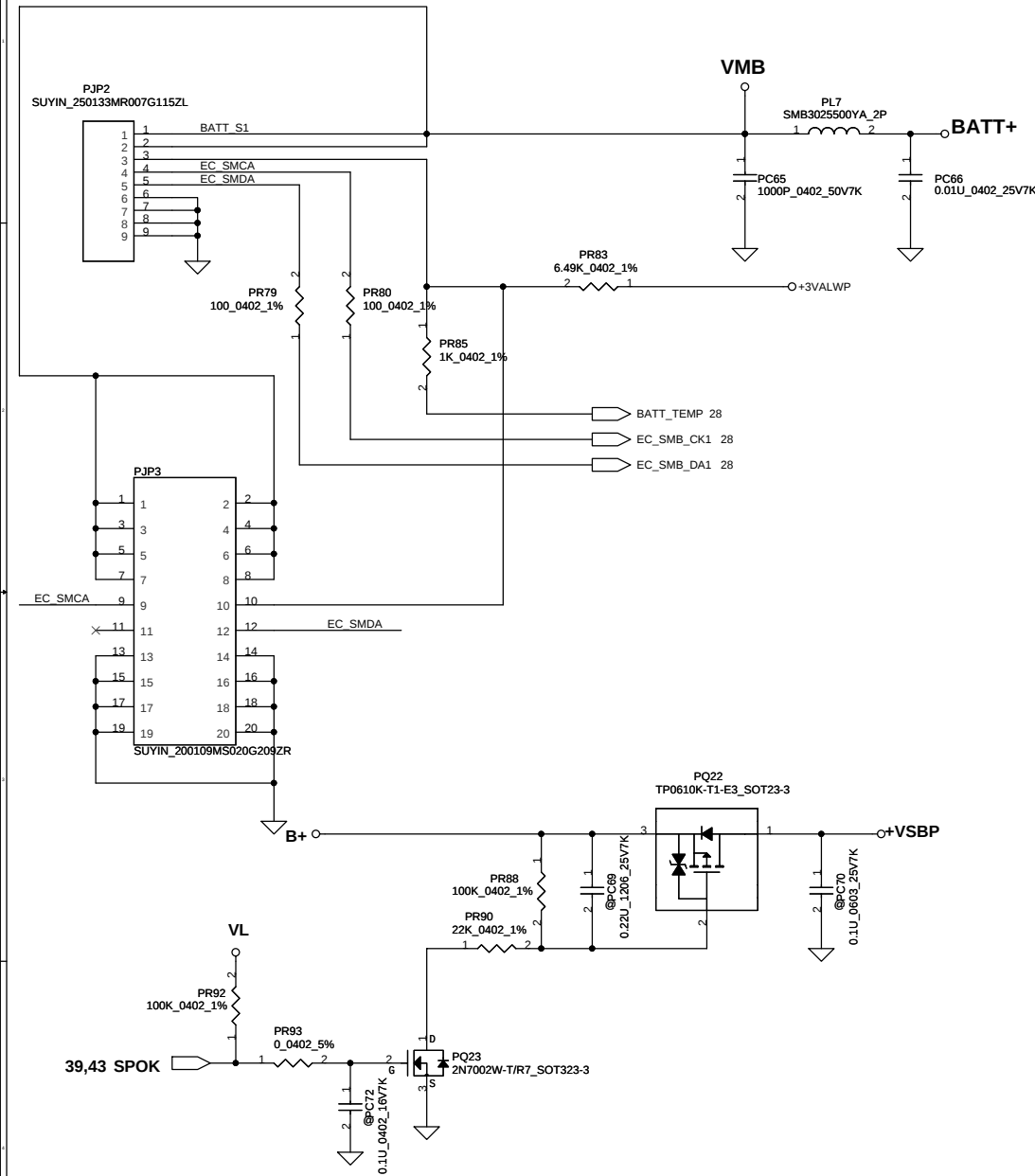
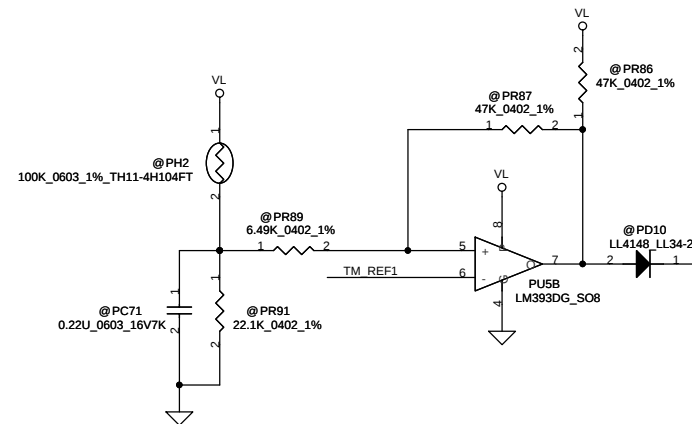
Icharge Setting
For 2200mA, Icharge=0.8C=0.8*2*2.2=3.52A
Icharge=(Vsrset/Vdac)*(0.1/PR46)
IREF=((100k/(100K+17.4K))/3.3)*(0.1/0.02)=Icharge
IREF=0.7748*Icharge



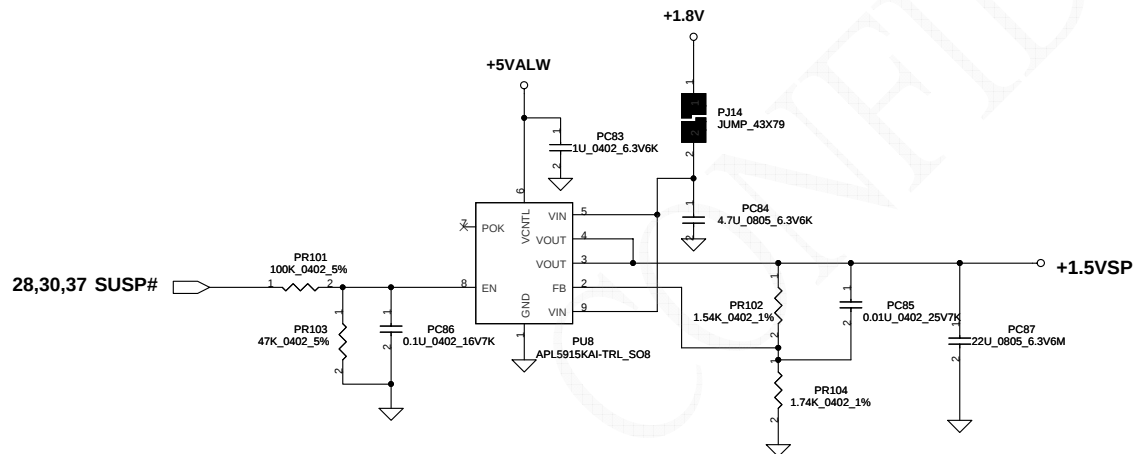
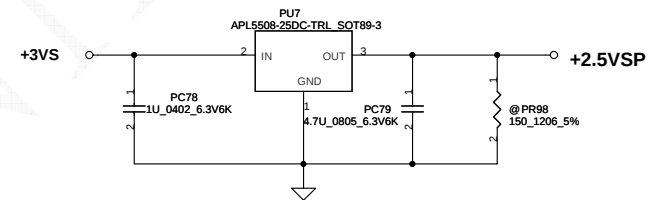
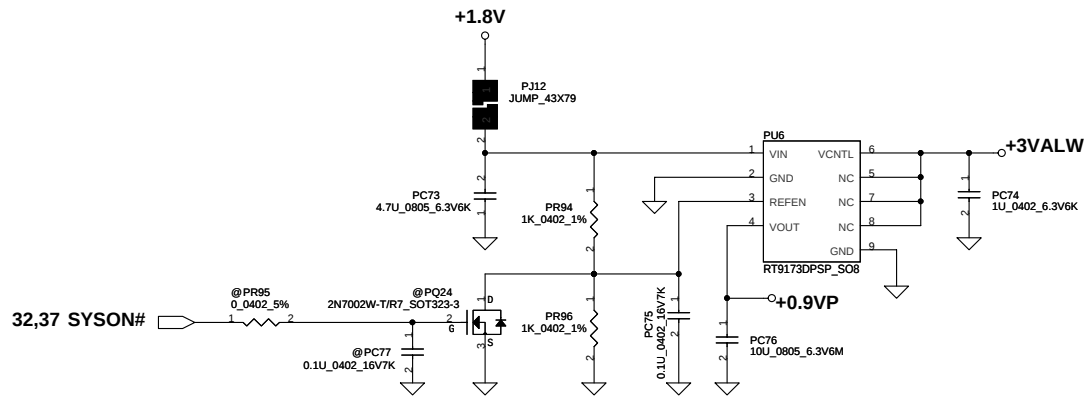
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



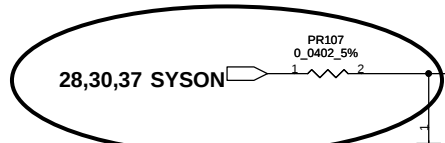
PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C



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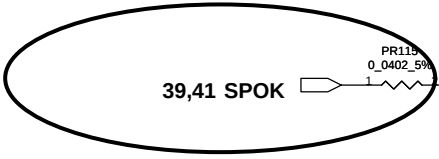
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VFB=0.75V
 $V_o = VFB * (1 + PR111/PR112) = 0.75 * (1 + 14K/10K) = 1.8V$
 $R_{ton} = 267K \Rightarrow F_{aw} = 297KHz$

Cout ESR=15m ohm
 $I_{peak} = 11.96A$, $I_{max} = 8.372A$, $I_{ocp} = 14.352A$
 $\Delta I = ((19-1.8) * (1.8/19)) / (L * F_{sw})$
 $((19-1.8) * (1.8/19)) / (1.8u * 297000) = 3.048A$
 $\Rightarrow 1/2 \Delta I = 1.524A$

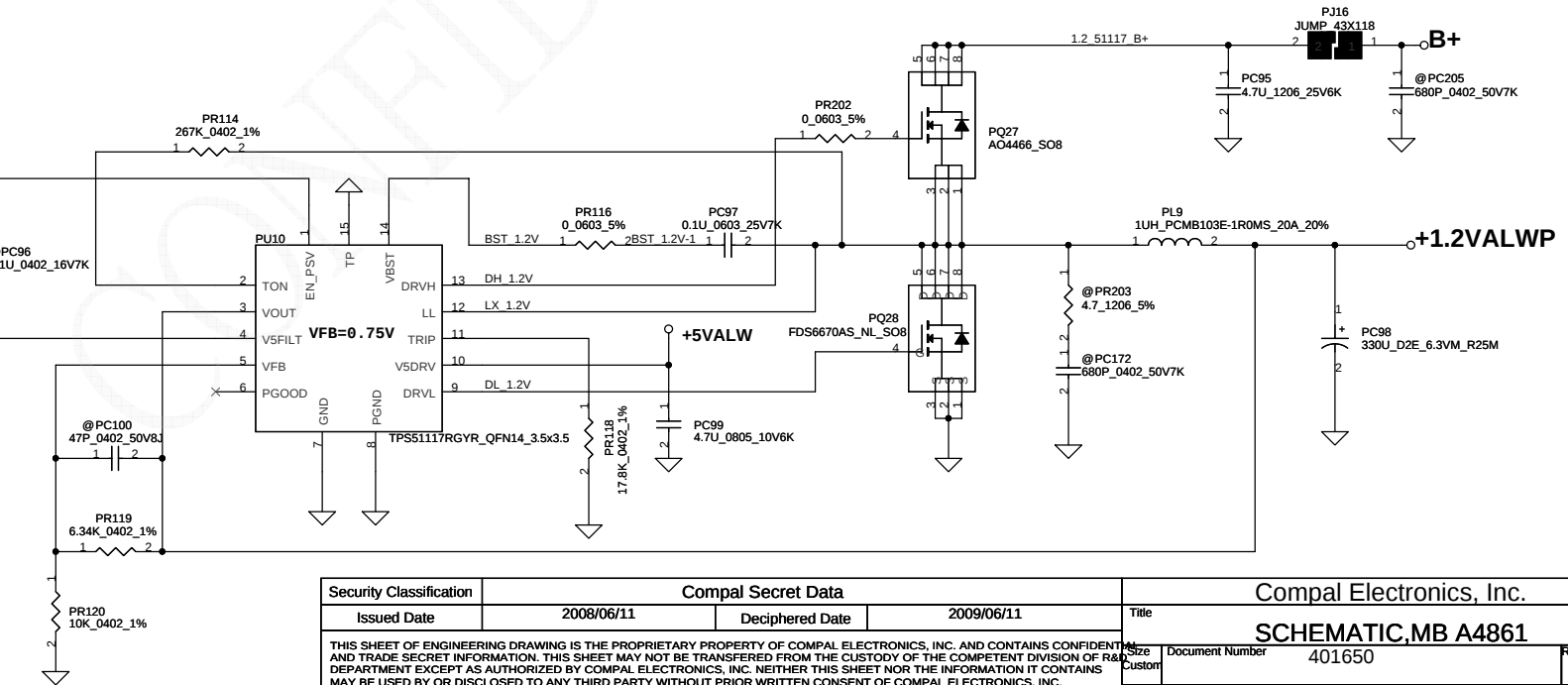
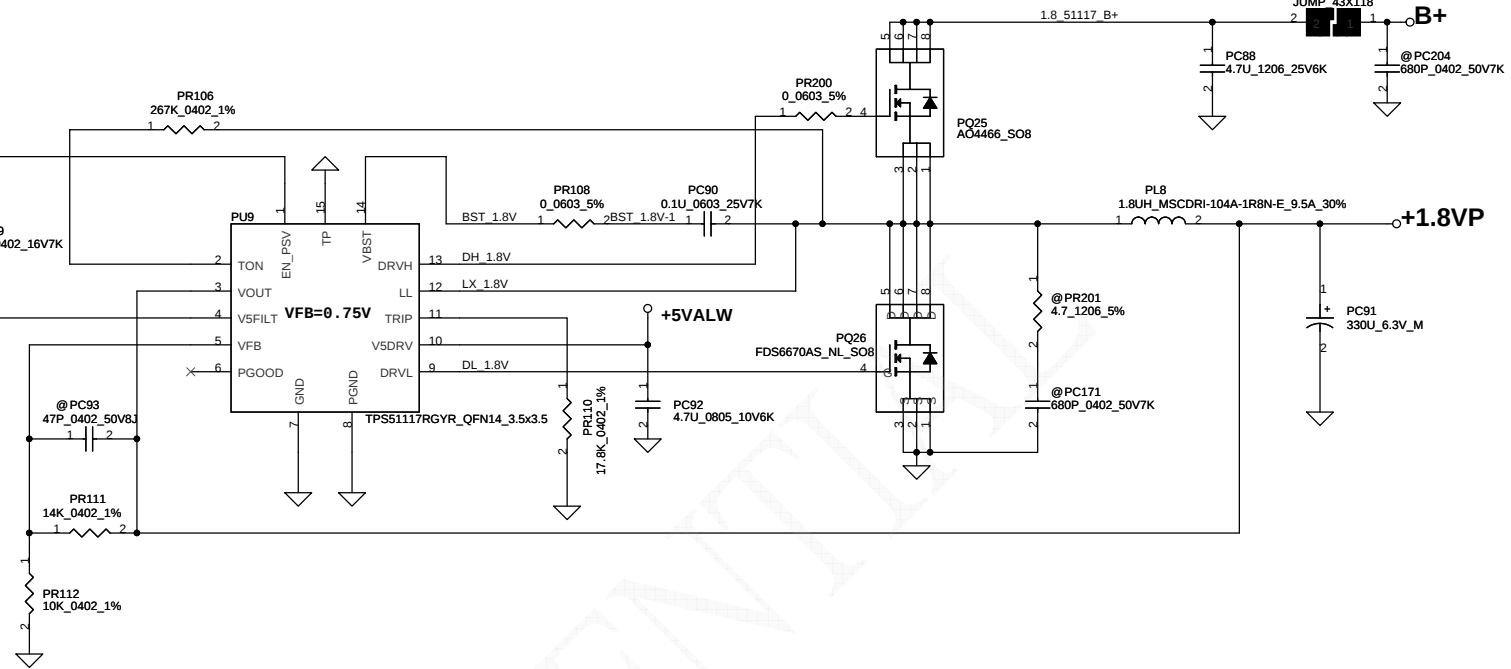
$R_{trip} = 17.8K$
 $I_{ocp} = 13.04A - 21.41A$



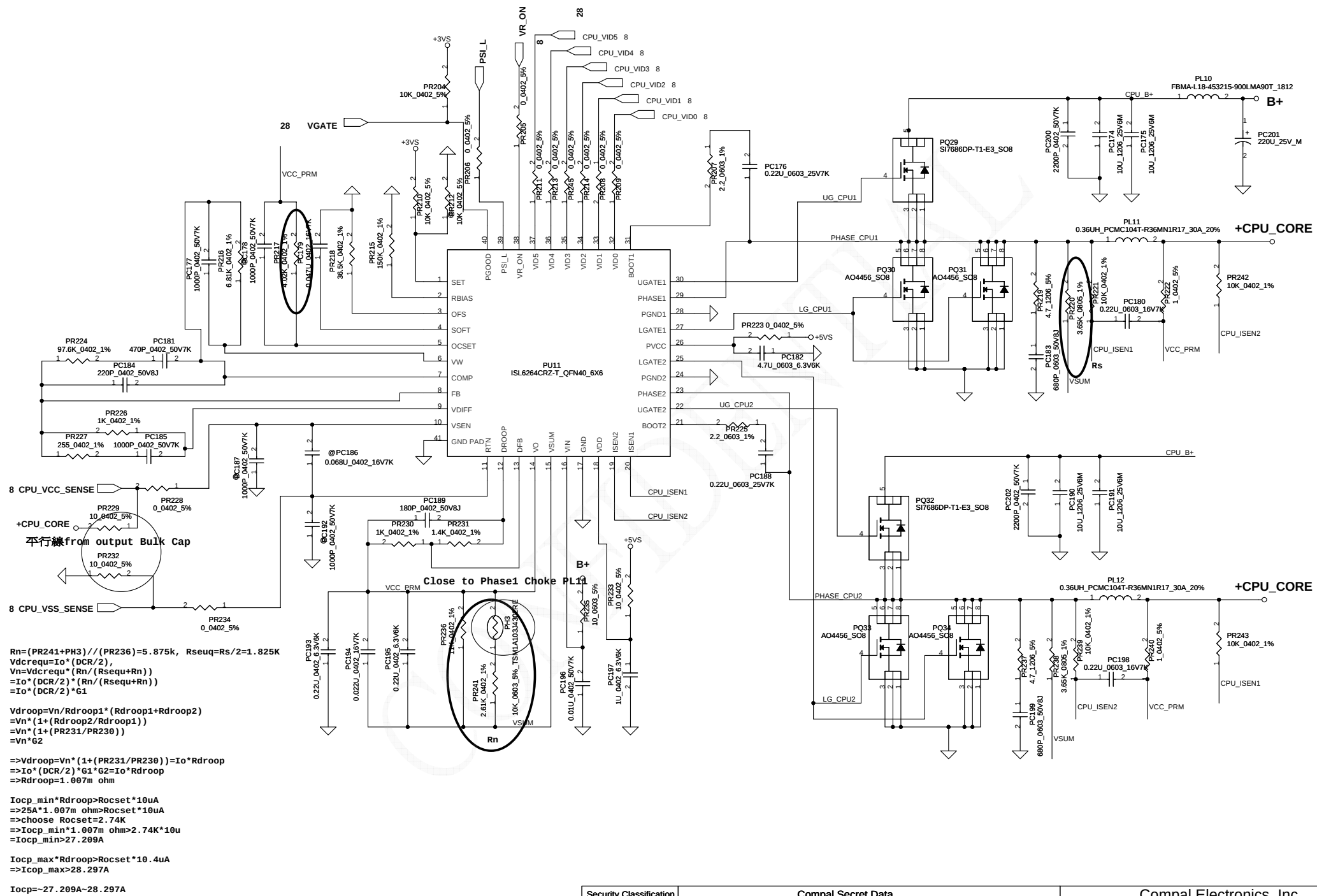
VFB=0.75V
 $V_o = VFB * (1 + PR119/PR120) = 0.75 * (1 + 6.04K/10K) = 1.203V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 298KHz$

Cout ESR=15m ohm
 $I_{peak} = 10.80A$, $I_{max} = 7.56A$, $I_{ocp} = 12.96A$
 $\Delta I = ((19-1.2) * (1.2/19)) / (L * F_{sw})$
 $((19-1.2) * (1.2/19)) / (1.8u * 298000) = 2.10A$
 $\Rightarrow 1/2 \Delta I = 1.05A$

$R_{trip} = 17.8K$
 $I_{ocp} = 12.75A - 20.83A$



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$R_n = (PR241 + PH3) / (PR236) = 5.875k$, $R_{seq} = R_s / 2 = 1.825k$
 $V_{dcreq} = I_o * (DCR / 2)$,
 $V_n = V_{dcreq} * (R_n / (R_{seq} + R_n))$
 $= I_o * (DCR / 2) * (R_n / (R_{seq} + R_n))$
 $= I_o * (DCR / 2) * G1$
 $V_{droop} = V_n / R_{droop1} * (R_{droop1} + R_{droop2})$
 $= V_n * (1 + (R_{droop2} / R_{droop1}))$
 $= V_n * (1 + (PR231 / PR230))$
 $= V_n * G2$
 $=> V_{droop} = V_n * (1 + (PR231 / PR230)) = I_o * R_{droop}$
 $=> I_o * (DCR / 2) * G1 * G2 = I_o * R_{droop}$
 $=> R_{droop} = 1.007m\ ohm$
 $I_{ocp_min} * R_{droop} > Rocset * 10uA$
 $=> 25A * 1.007m\ ohm > Rocset * 10uA$
 $=> choose\ Rocset = 2.74k$
 $=> I_{ocp_min} * 1.007m\ ohm > 2.74k * 10u$
 $=> I_{ocp_min} > 27.209A$
 $I_{ocp_max} * R_{droop} > Rocset * 10.4uA$
 $=> I_{ocp_max} > 28.297A$
 $I_{ocp} = -27.209A - 28.297A$

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	Customer changed CPU to TF36/38.	TF36/38 is 31W CPU, must change MOS to 1H2L.	0.1	44	Add PQ31 and PQ34 SB000009F80(S TR A04456 1N S08)	08, 11/13	to DVT
2	Change CP OCP setting.	TF36/38 CPU OCP setting change.	0.1	44	Change PR198 to SD034402180(S RES 1/16W 4.02K 0402 1%)	08, 11/13	to DVT
3	S3 Mode issue.	Because APL5915 has 0.4V enable voltage, so add PR103 to pull down enable voltage when system in S3 mode	0.1	42	Add PR103 SD028470280(S RES 1/16W 47K 0402 5%)	08, 11/13	to DVT
4	AMD issue.	AMD request add 1.2V to 1.22V for chipset.	0.1	43	Change PR119 from SD034604180 to SD034634180.	08, 11/17	to DVT
5	EMI issue.	EMI request add charger snubber.	0.1	40	Add PR48 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC50 SE074681K80(S CER CAP 680P 50V K X7R 0402)	08, 11/17	to DVT
6	Cost issue.	Cost issue.	0.1	44	Change PC201 from SF000000G80(S ELE CAP 220U 25V M HA0 MVY) to SF22004M210(S ELE CAP 220U 25V M 8X10.2 CE-AX)	08, 11/17	to DVT
7	Support charge voltage.	Support charge voltage.	0.1	40	Delete PQ18 SB000006800(S TR 2N7002W T/R7 1N S0T-323)	08, 11/26	to DVT
8	Support charge voltage.	Support charge voltage.	0.1	40	Delete PQ16 SB923010020(S TR SI2301BDS-T1-E3 1P S0T23)	08, 11/26	to DVT
9	Support charge voltage.	Support charge voltage.	0.1	40	Delete PR66 SD028000080(S RES 1/16W 0 0402 5%)	08, 11/26	to DVT
10	Support charge voltage.	Support charge voltage.	0.1	40	Delete PR69 SD034100380(S RES 1/16W 100K 0402 1%)	08, 11/26	to DVT
11	Support charge voltage.	Support charge voltage.	0.1	40	Delete PC63 SE074102K80(S CER CAP 1000P 50V K X7R 0402)	08, 11/26	to DVT
12	Support charge voltage.	Support charge voltage.	0.1	40	Add PR70 SD034210380(S RES 1/16W 210K 0402 1%)	08, 11/26	to DVT
13	Support charge voltage.	Support charge voltage.	0.1	40	Add PR71 SD034499380(S RES 1/16W 499K 0402 1%)	08, 11/26	to DVT
14							
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