Compal Confidential

NAWF3/F4/H3 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-09-01

REV:0.1

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2009/08/25

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Title: Cover Page

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 1 of 45

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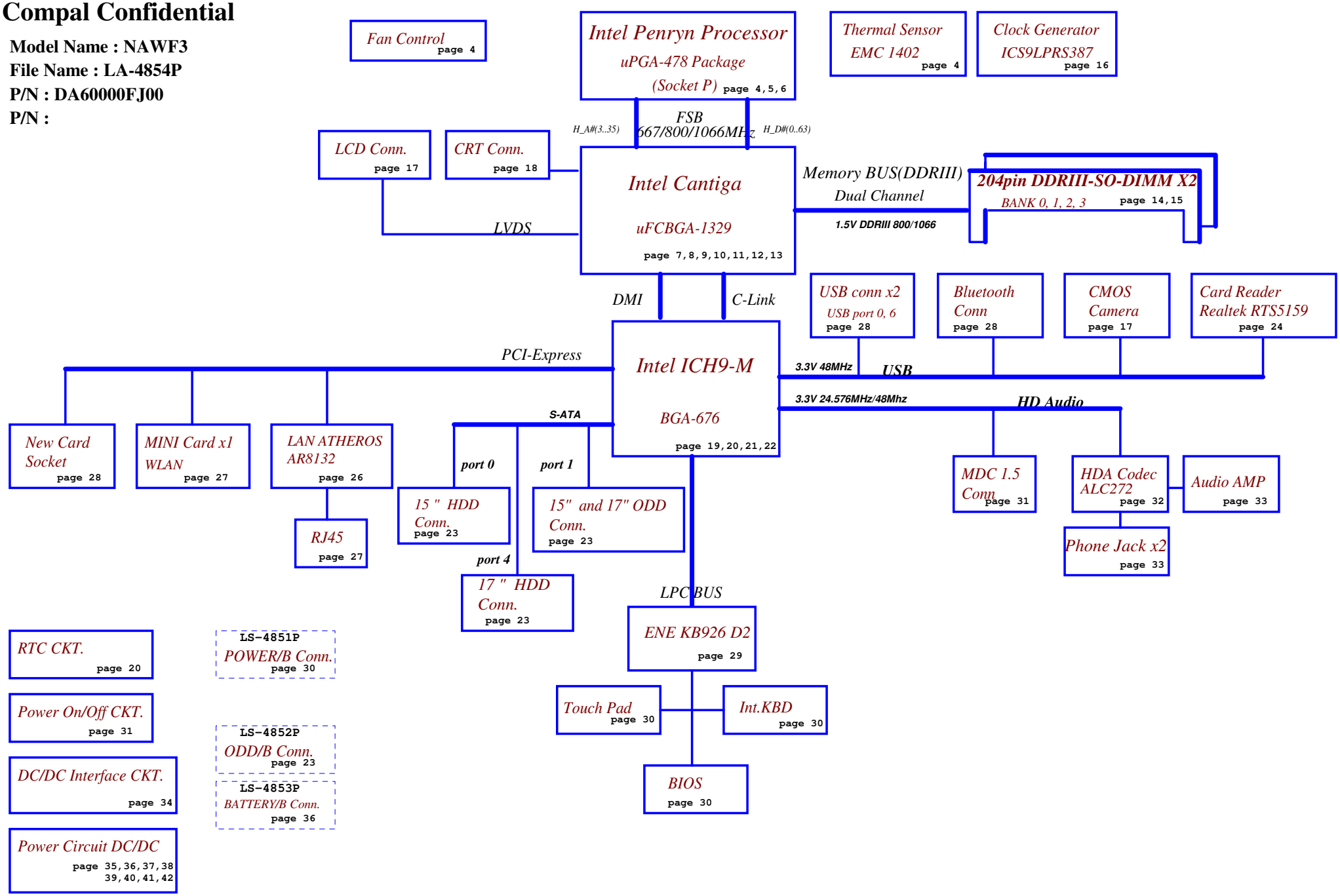
Model Name : NAWF3
File Name : LA-4854P
P/N : DA60000FJ00
P/N :



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			Date: Wednesday, September 02, 2009 / Sheet 2 of 45

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V power rail for DDR	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
ADI ADT7421	1001 100X b

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	0.1 (PVT2)
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
GM45	GM@
GL40	GL@
15"	15@
17"	17@
8114	8114@
8132	8132@

PCIE table

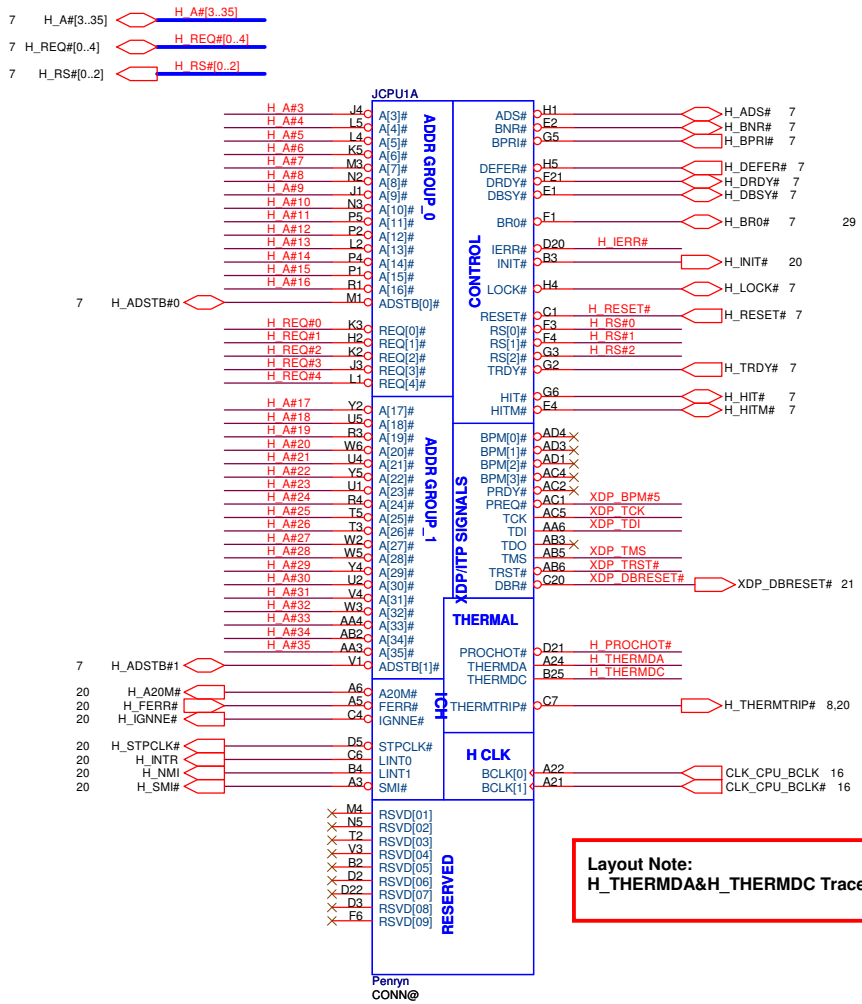
PCIE port1	Express Card(Reserved)
PCIE port2	Wireless Card
PCIE port3	PCIE LAN
PCIE port4	
PCIE port5	
PCIE port6	

USB table

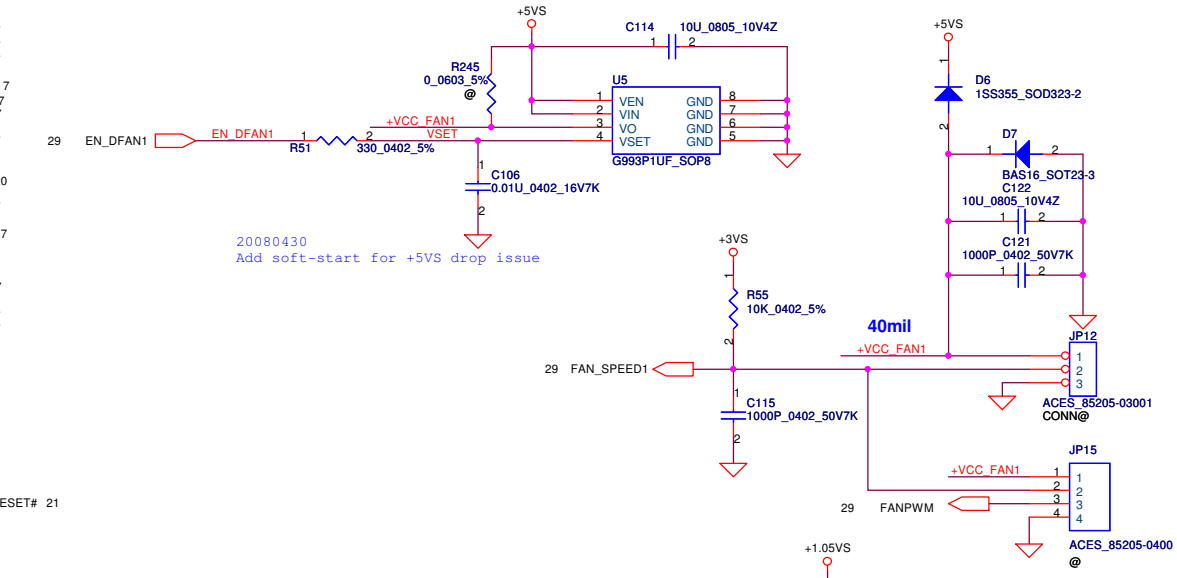
EHCI1	UHCI1	Port0	MB USB Conn.
		Port1	
	UHCI2	Port2	
		Port3	CMOS Camera
	UHCI3	Port4	Card Reader
		Port5	New Card(Reserved)
EHCI2	UHCI4	Port6	MB USB Conn.
		Port7	
	UHCI5	Port8	Blue Tooth
		Port9	
	UHCI6	Port10	Wireless Card
		Port11	

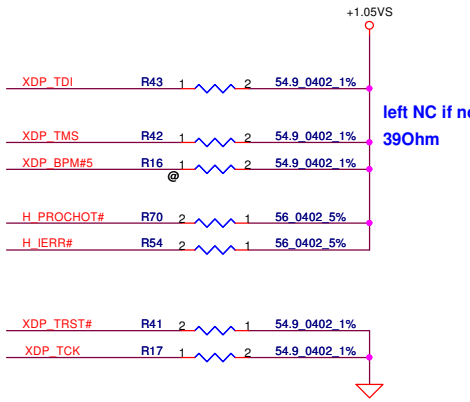
SATA table

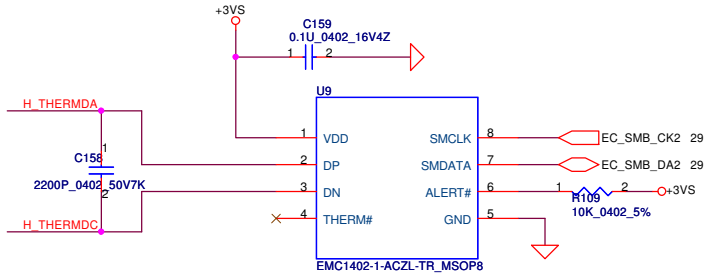
SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	for 17" 2nd HDD
SATA port5	



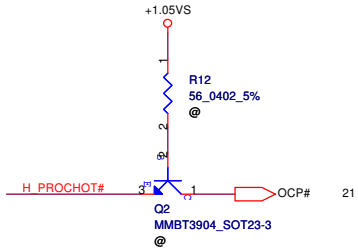
FAN1 Conn







BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166



Layout Note:
H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil

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Compal Electronics, Inc.

Title: Penryn (1/3) & FAN

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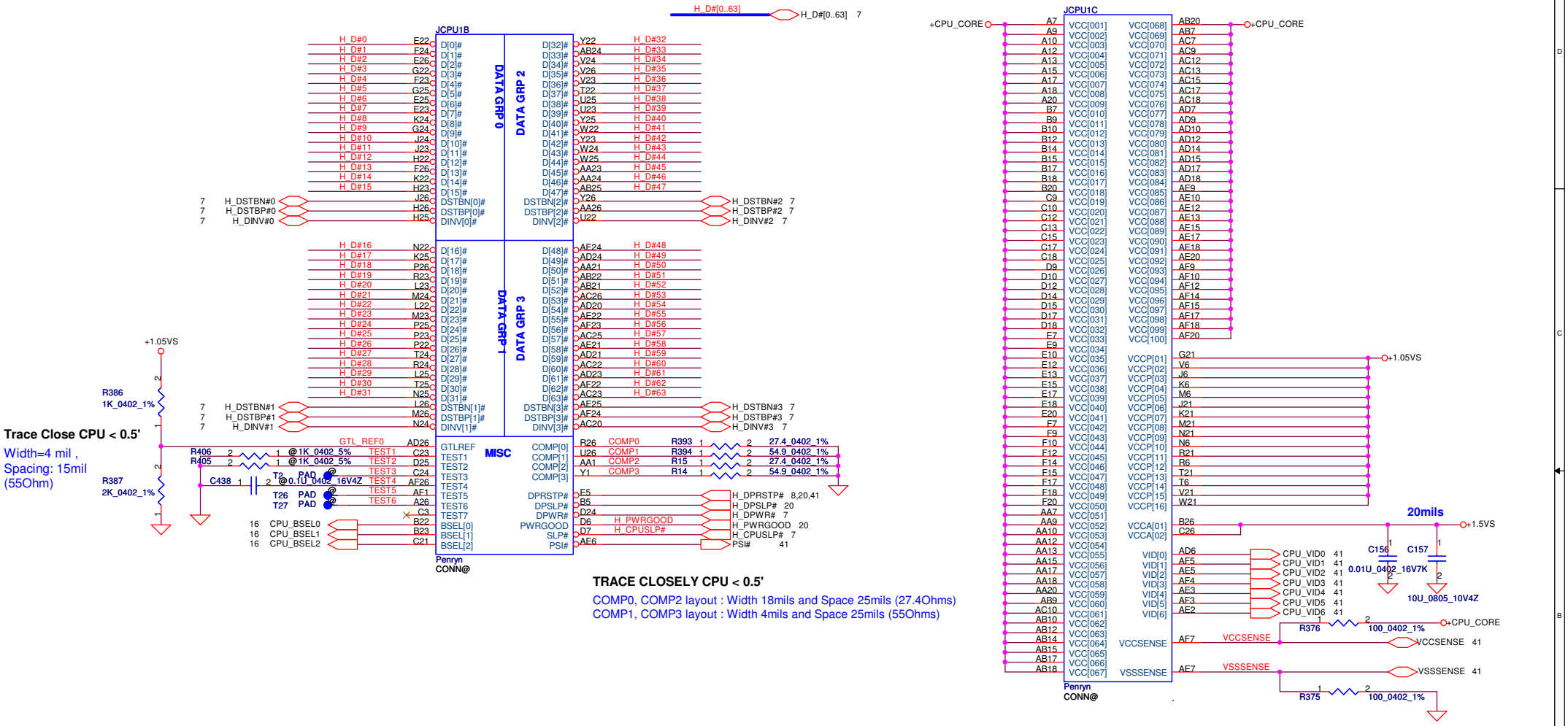
Date: Wednesday, September 02, 2009 | Sheet 4 of 45



Trace Close CPU < 0.5'

Width=4 mil ,
Spacing: 15mil
(55Ohm)

TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

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Compal Electronics, Inc.

Title: Penryn (2/3)

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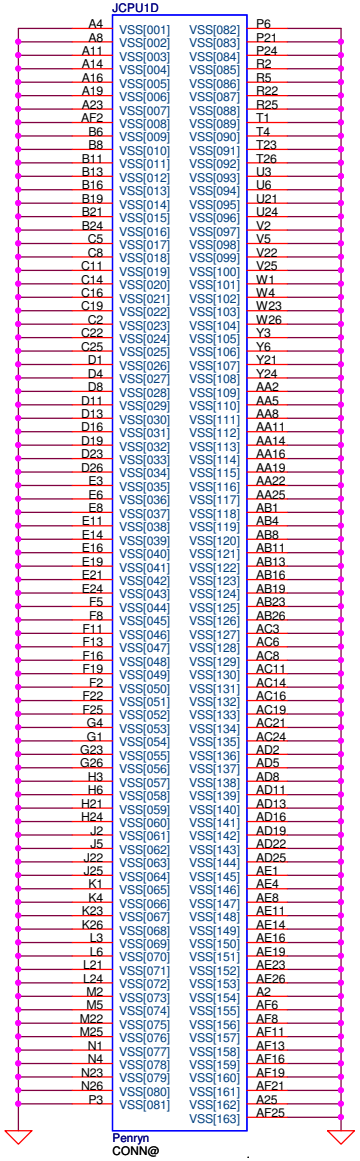
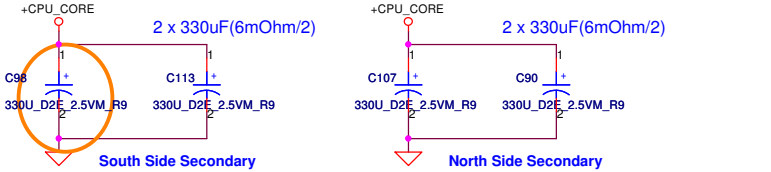
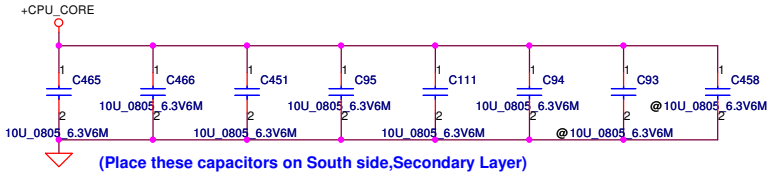
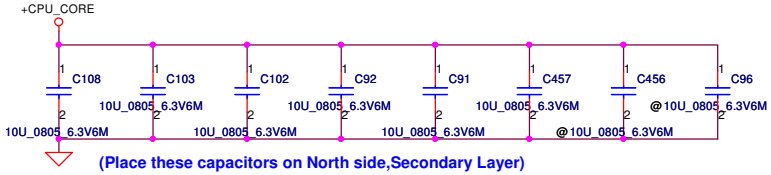


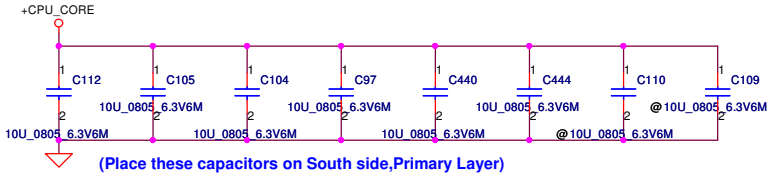




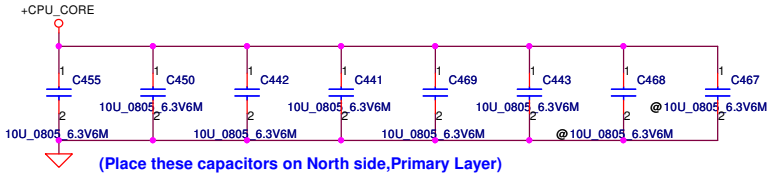
(Place these capacitors on South side,Secondary Layer)



(Place these capacitors on North side,Secondary Layer)

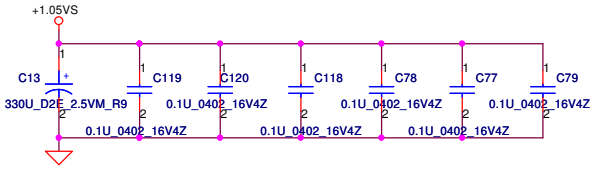


(Place these capacitors on South side,Primary Layer)



(Place these capacitors on North side,Primary Layer)

+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF 32X10uF	3m ohm/32 3m ohm/32	0.6nH/32 0.6nH/32



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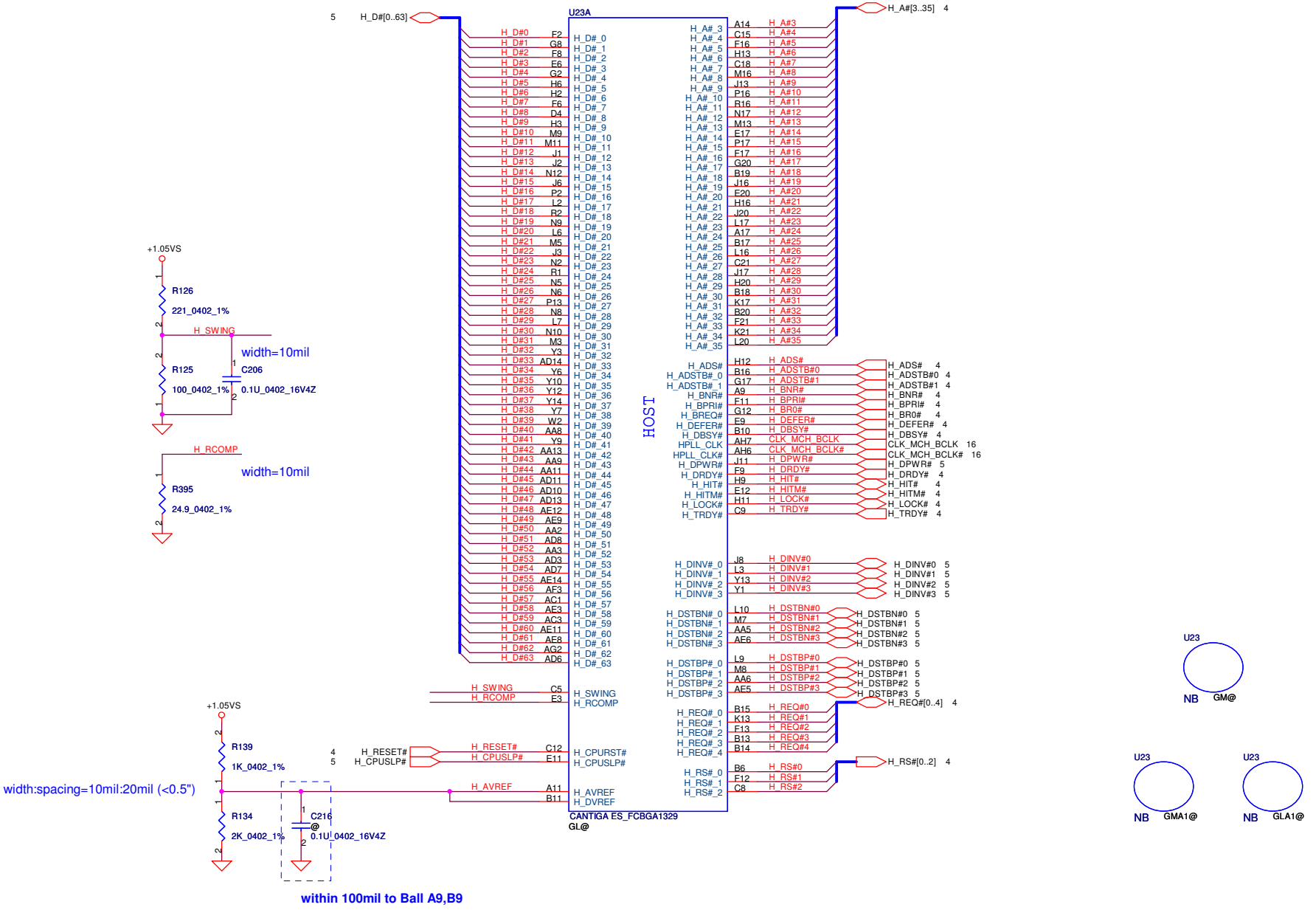
Title: Penryn (3/3)

Size: B | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 6 of 45



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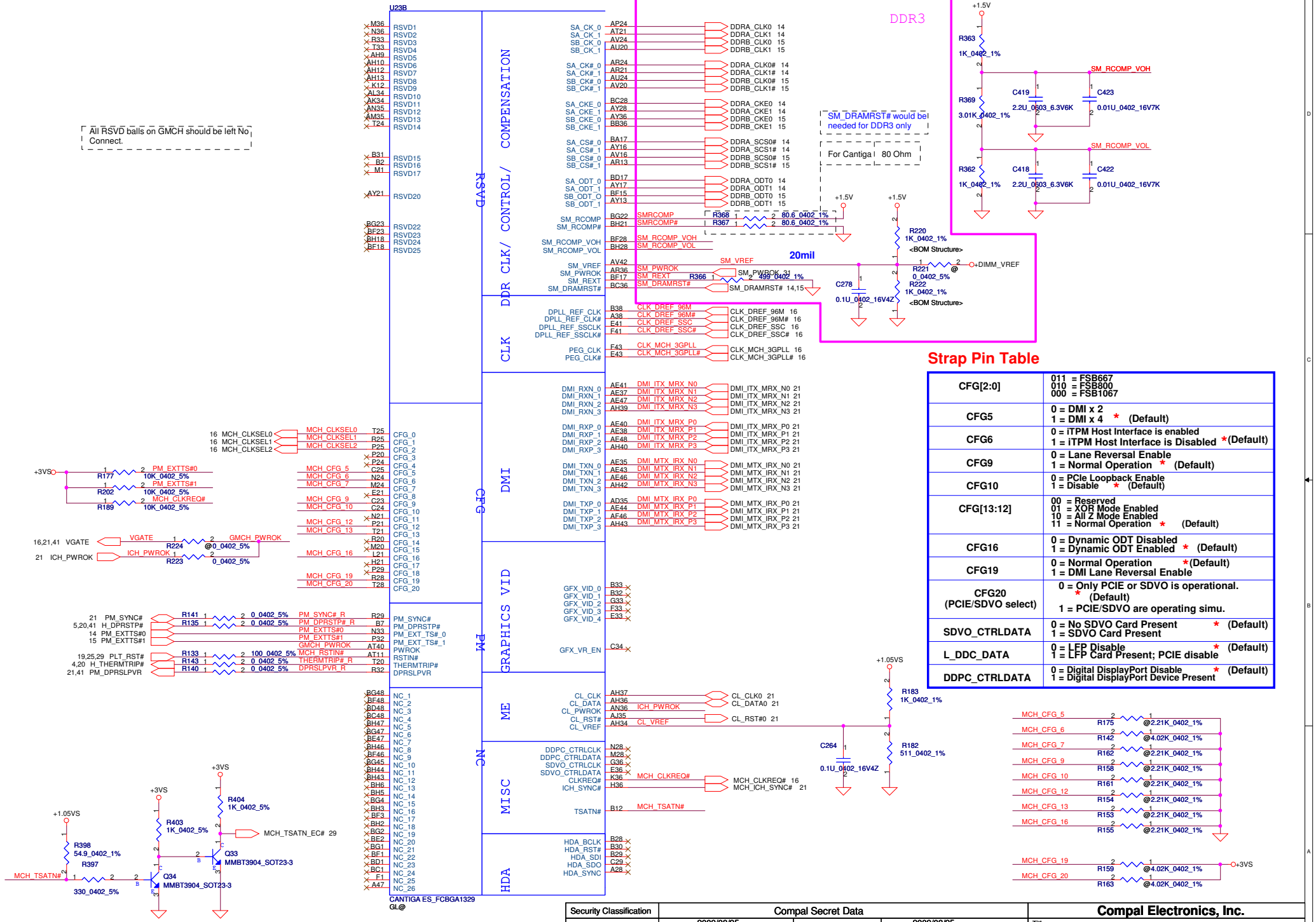
Title: Cantiga GMCH(1/7)-GTL

Size: B | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 7 of 45



Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable * (Default) 1 = LFP Card Present; PCIE disable
DDPC_CTRLDATA	0 = Digital DisplayPort Disable * (Default) 1 = Digital DisplayPort Device Present

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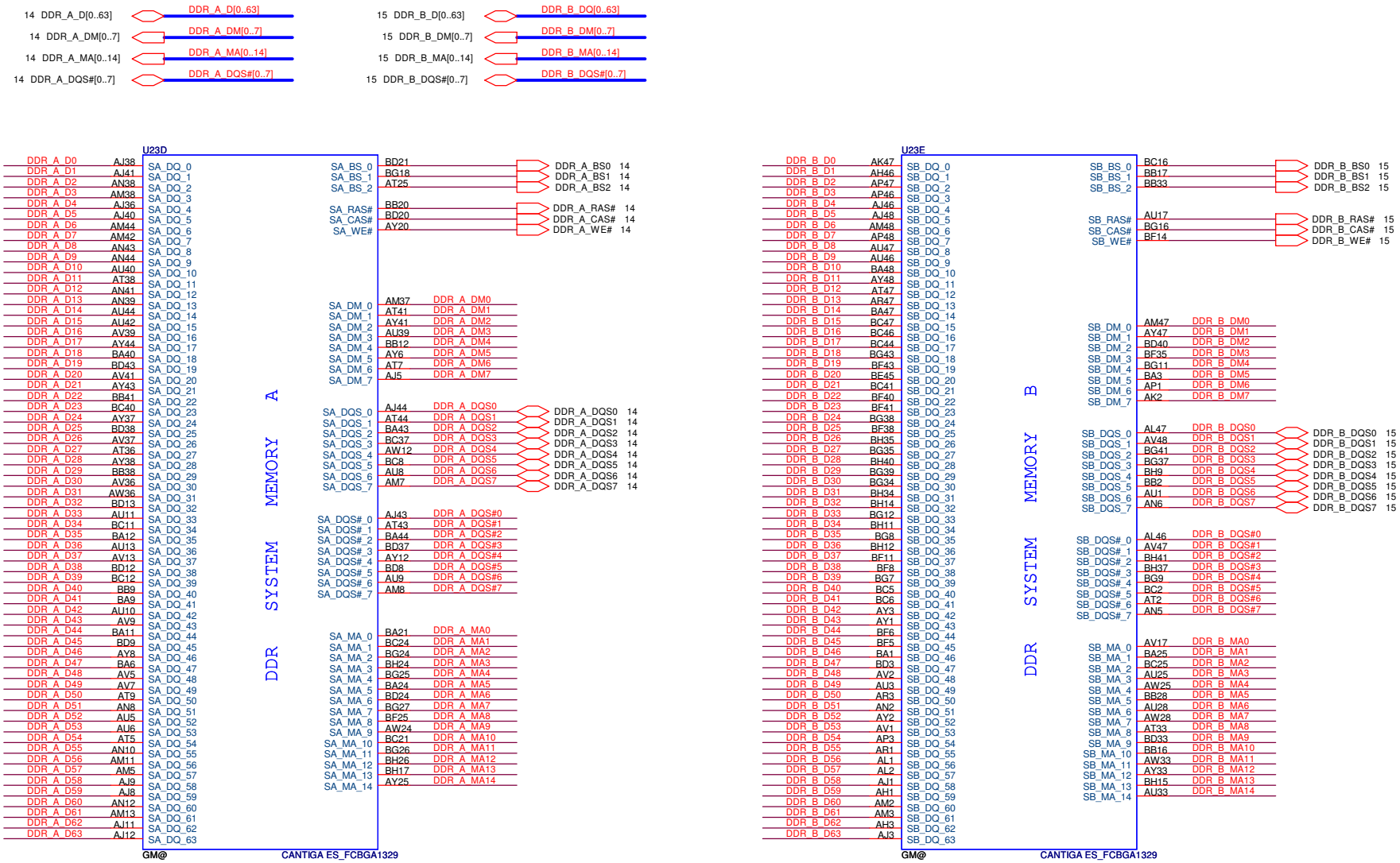
Title	Cantiga GMCH(2/7)-DMI/DDR		
Size	Custom	Document Number	NAWF3 M/B LA-4854P Schematic
Rev	0.1		
Date:	Wednesday, September 02, 2009	Sheet	8 of 45



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Title: Cantiga GMCH(3/7)-DDR

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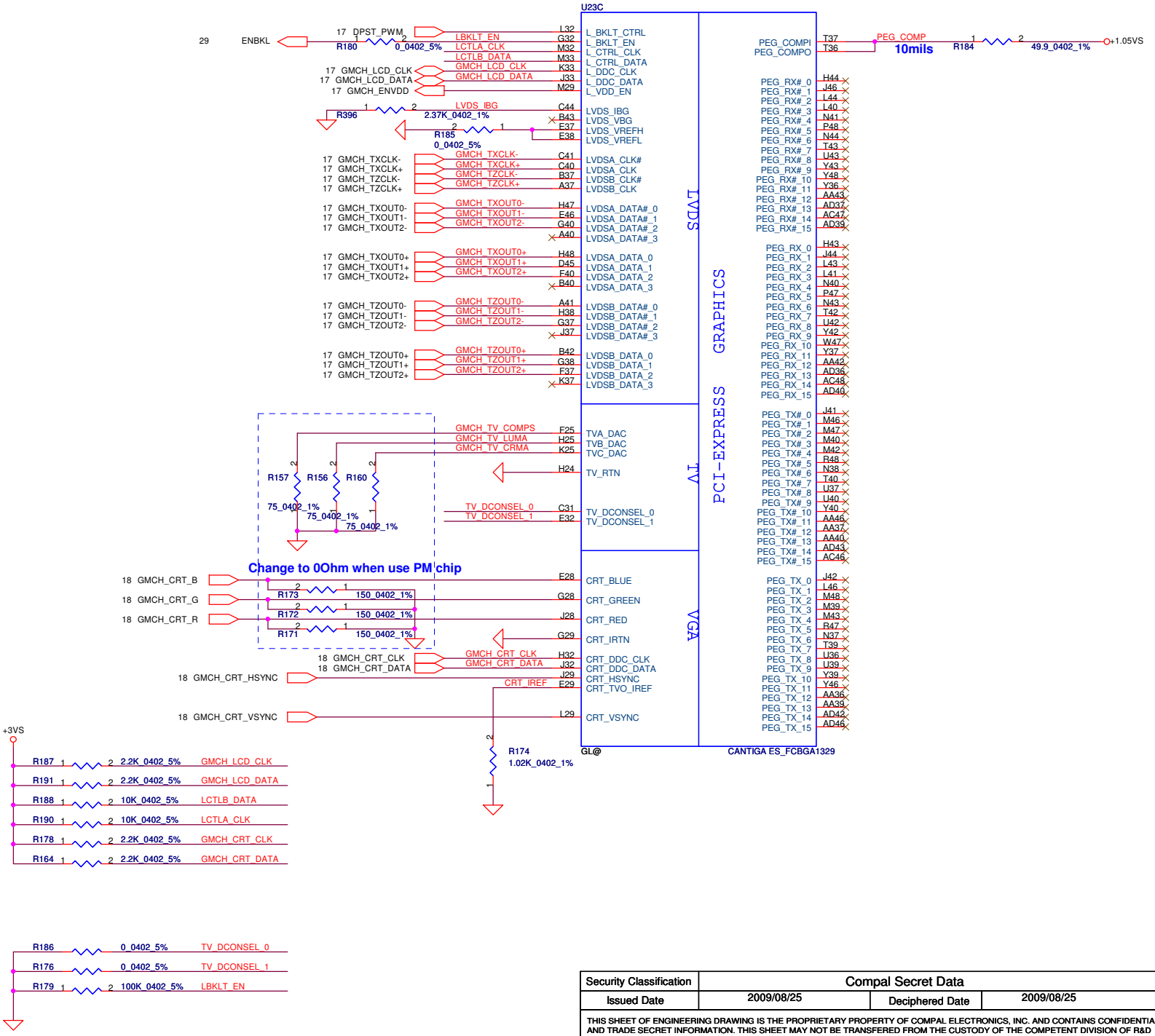
Date: Wednesday, September 02, 2009 | Sheet 9 of 45



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Compal Electronics, Inc.

Title: Cantiga GMCH(4/7)-VGA/LVDS/TV

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

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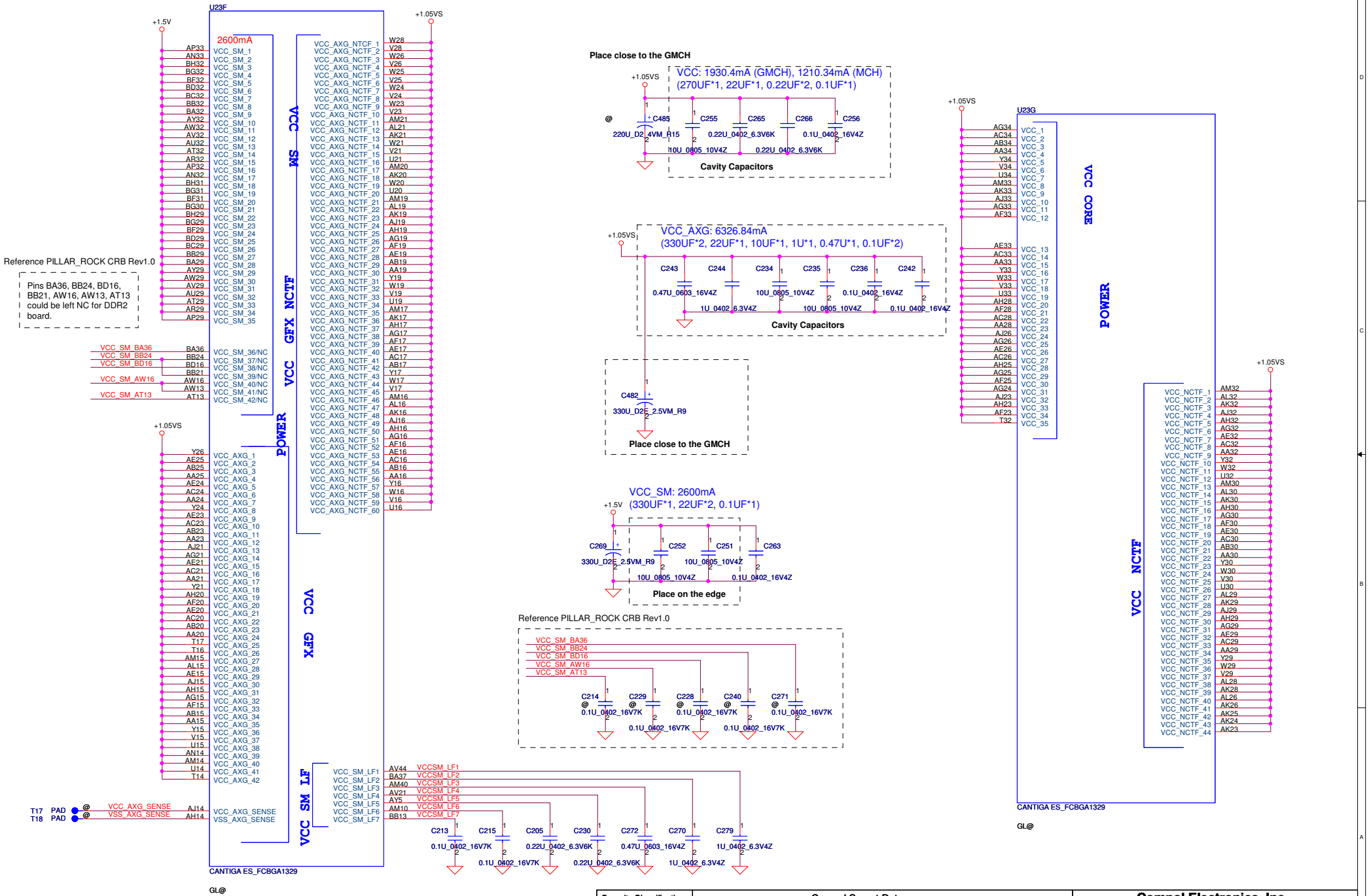

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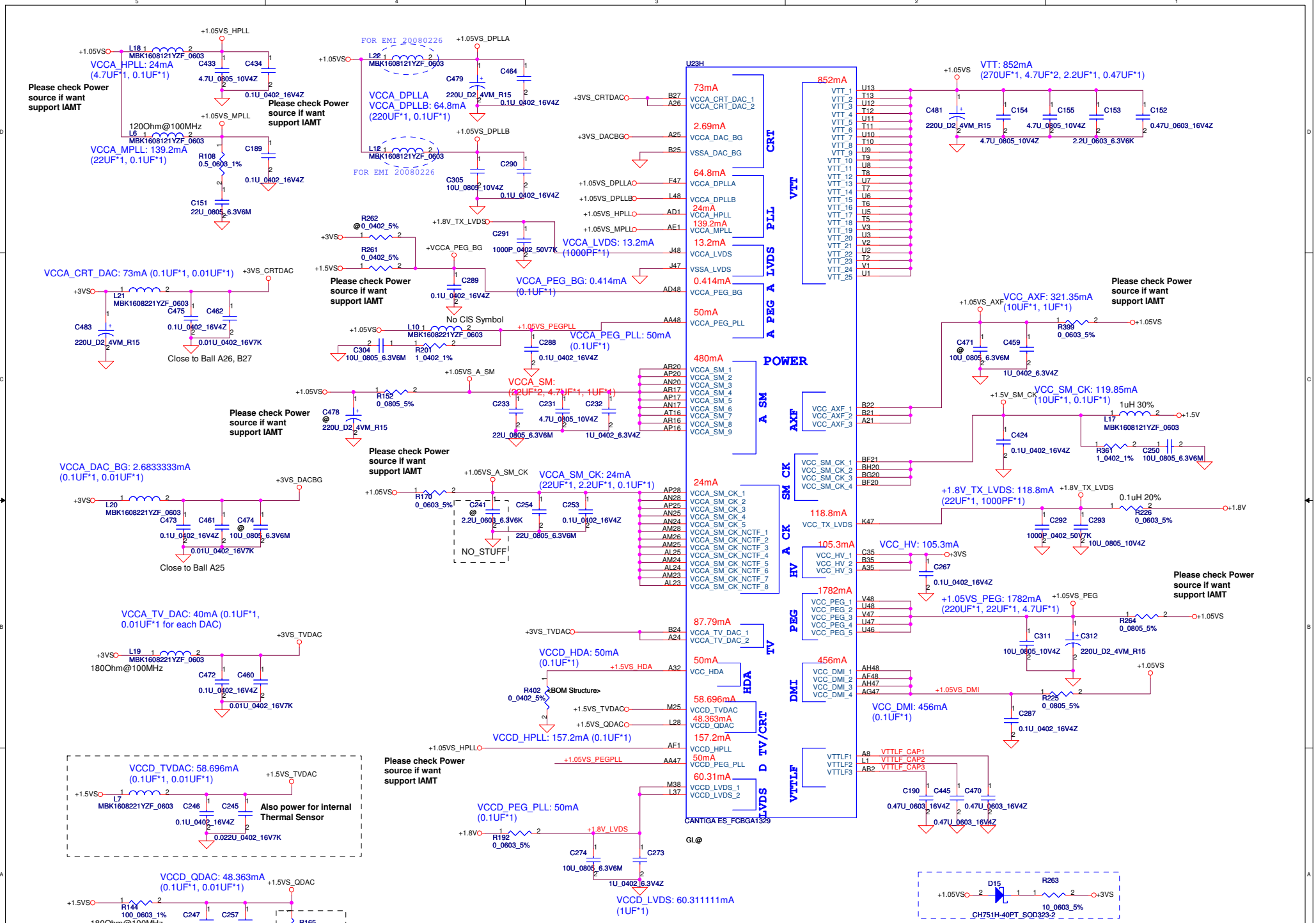
				Date: Wednesday, September 02, 2009; Sheet 11 of 45



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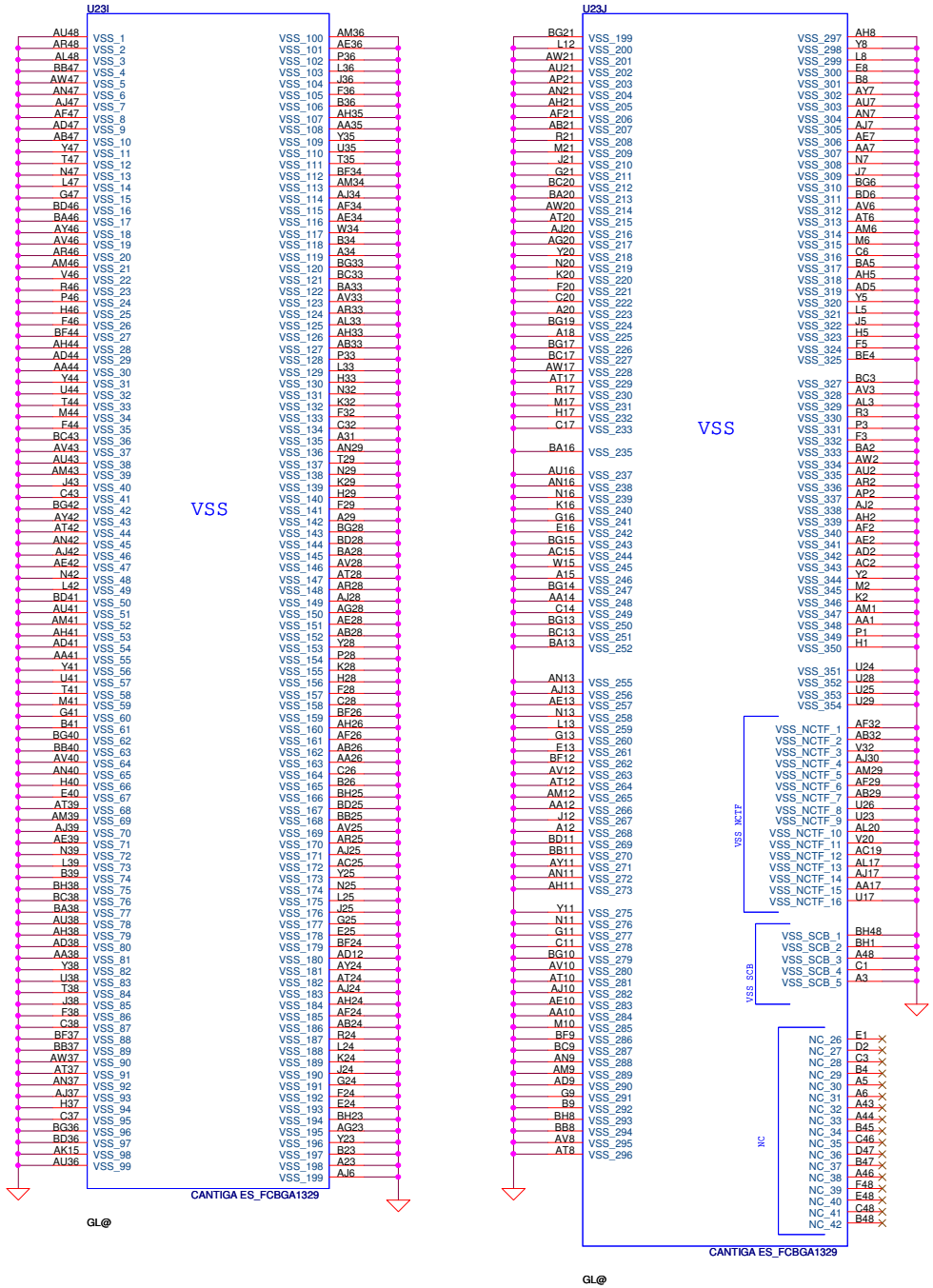

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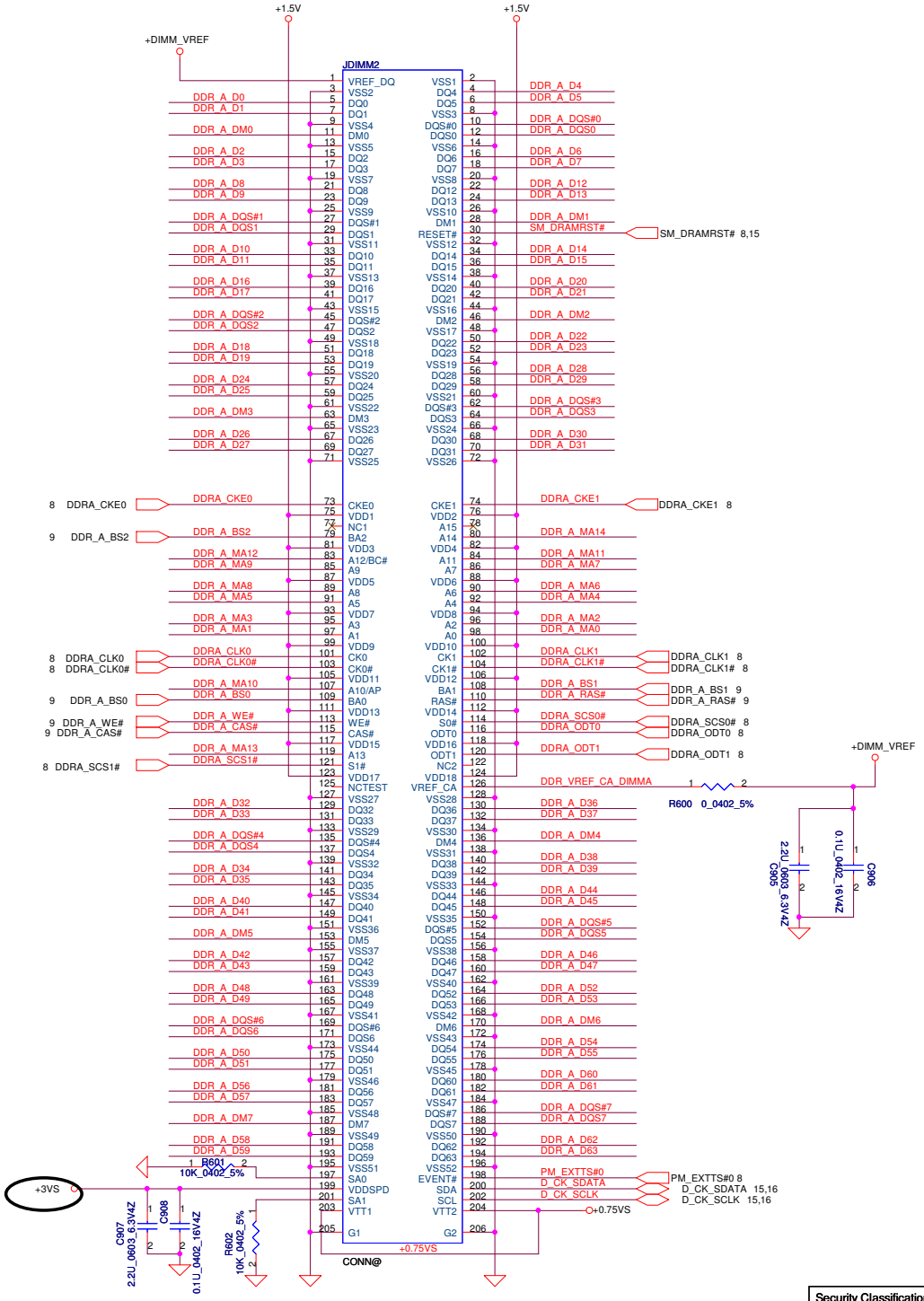
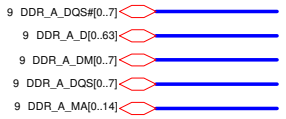
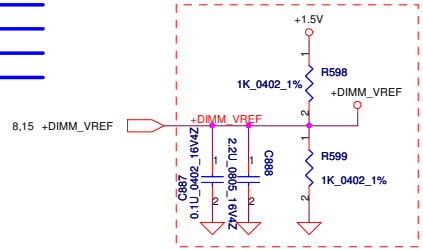
				Date: Wednesday, September 02, 2009; Sheet 13 of 45

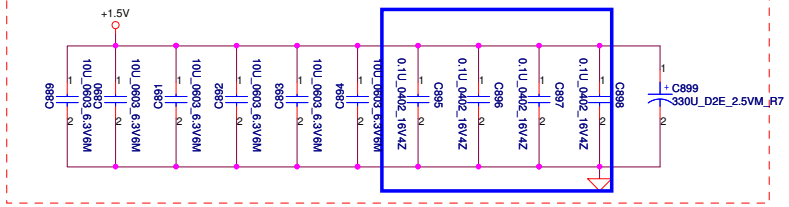




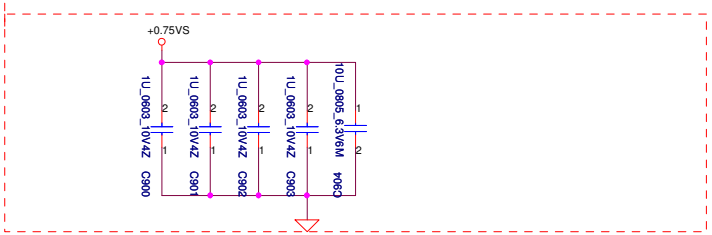


Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JDIMM2.203 & JDIMM2.204



DIMM0 REV H:5.2mm (BOT)

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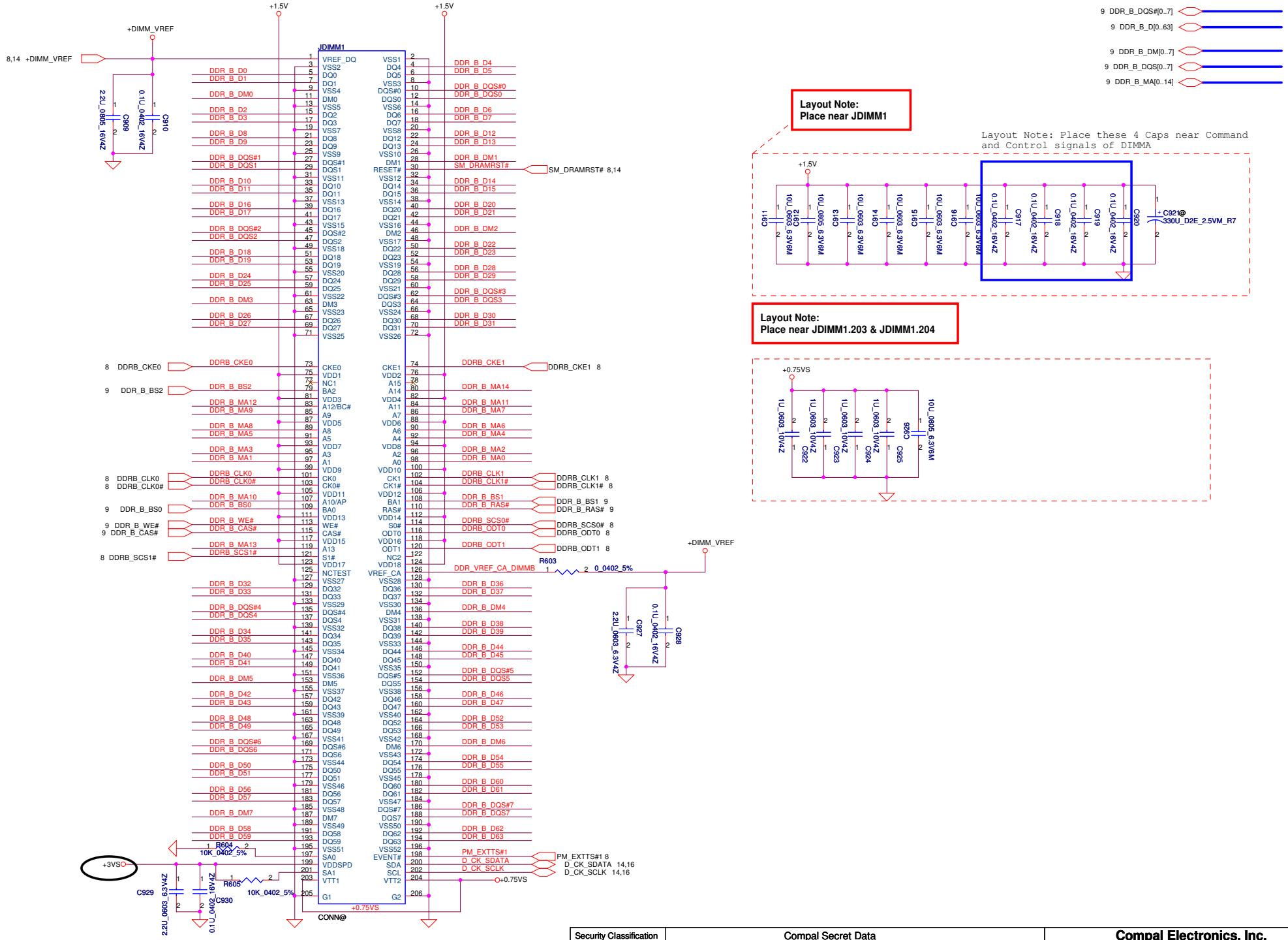
				Date: Wednesday, September 02, 2009; Sheet 14 of 45



DIMM1 REV H:9.2mm (BOT)

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				Date: Wednesday, September 02, 2009; Sheet 15 of 45

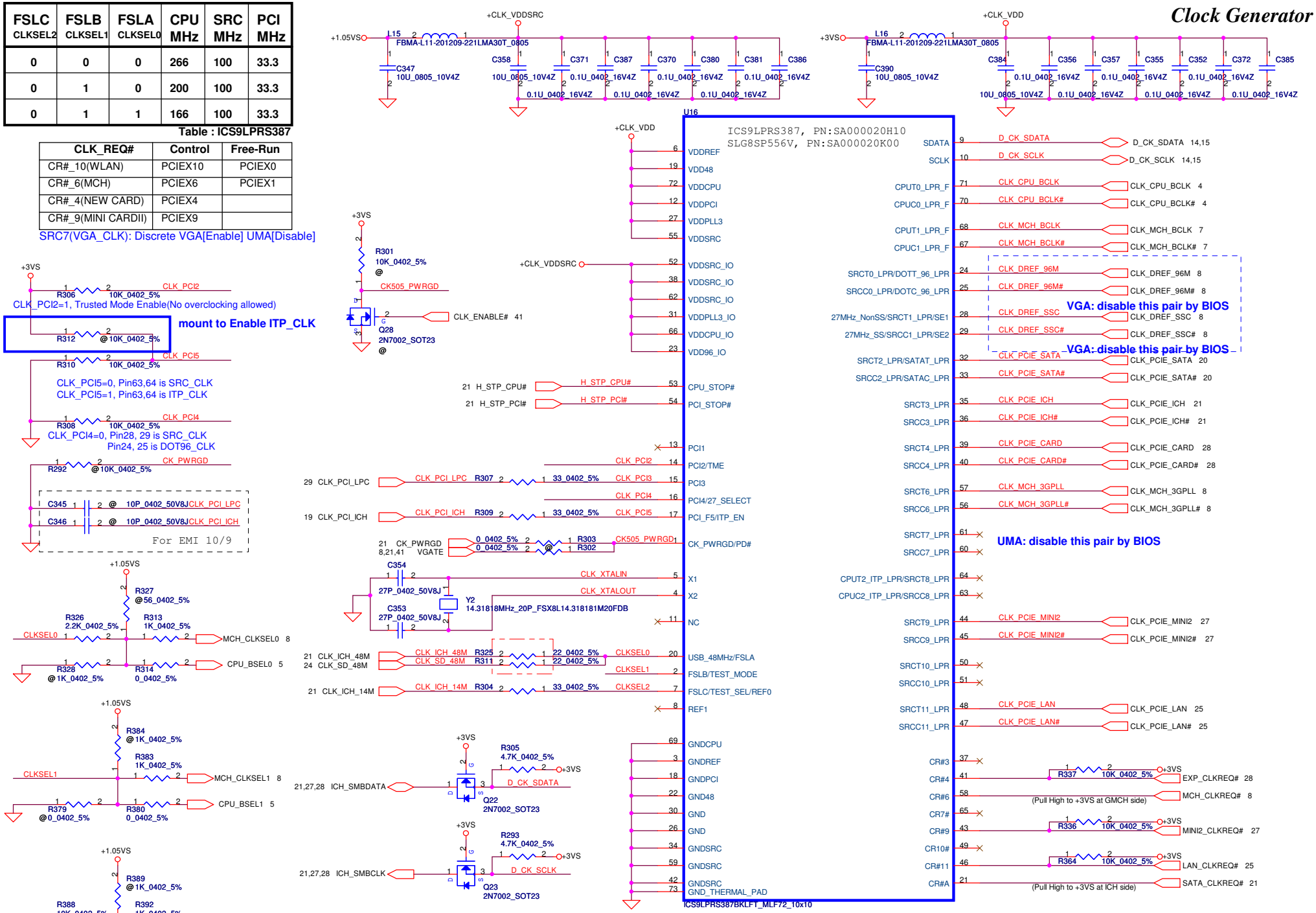
Clock Generator

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]



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Issued Date	2009/08/25	Deciphered Date	2009/08/25

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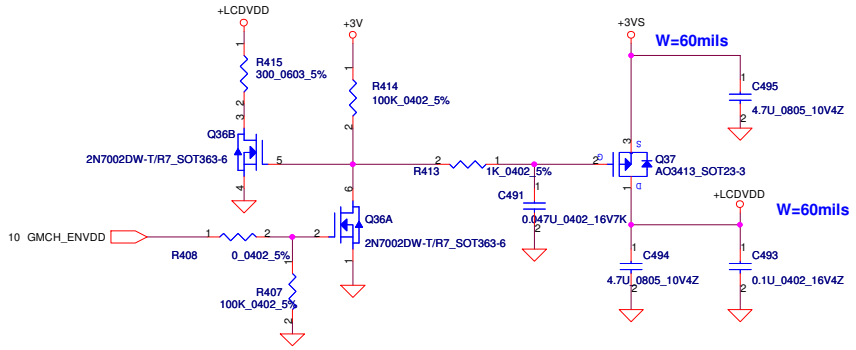
Compal Electronics, Inc.

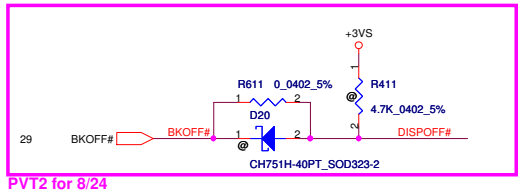
Title: Clock Generator (CK505)

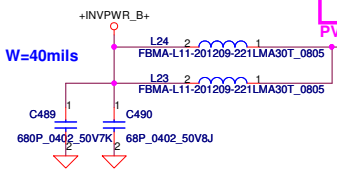
Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

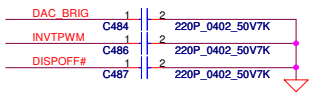
Date: Wednesday, September 02, 2009 | Sheet 16 of 45

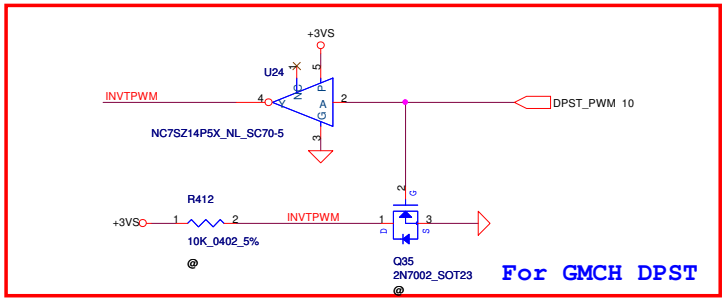
LCD POWER CIRCUIT



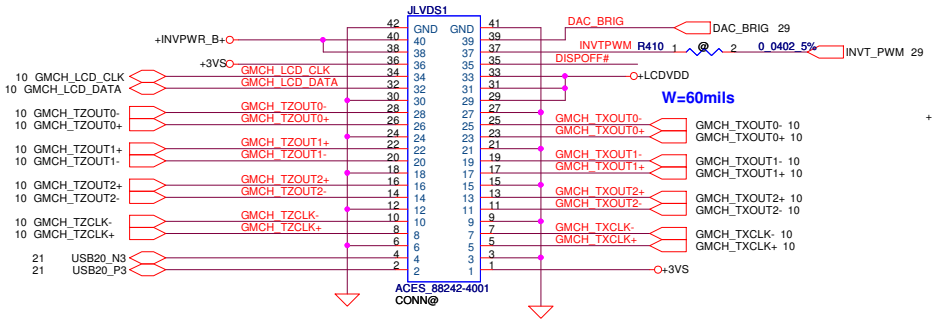


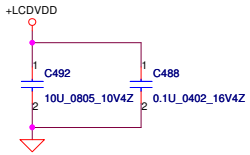






LCD/PANEL BD. Conn.





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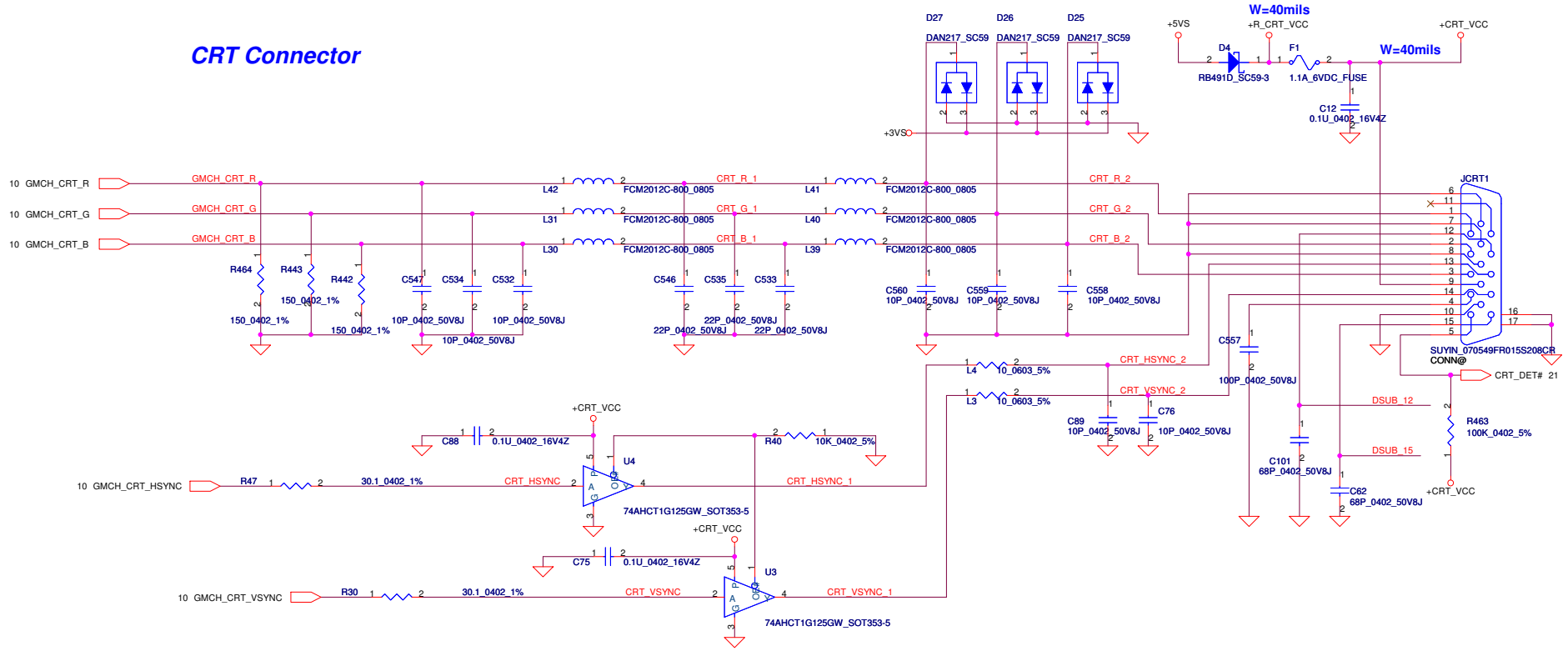
				Date: Wednesday, September 02, 2009; Sheet 17 of 45

CRT Connector



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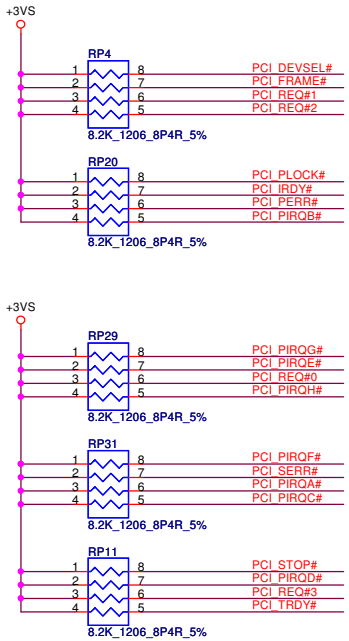
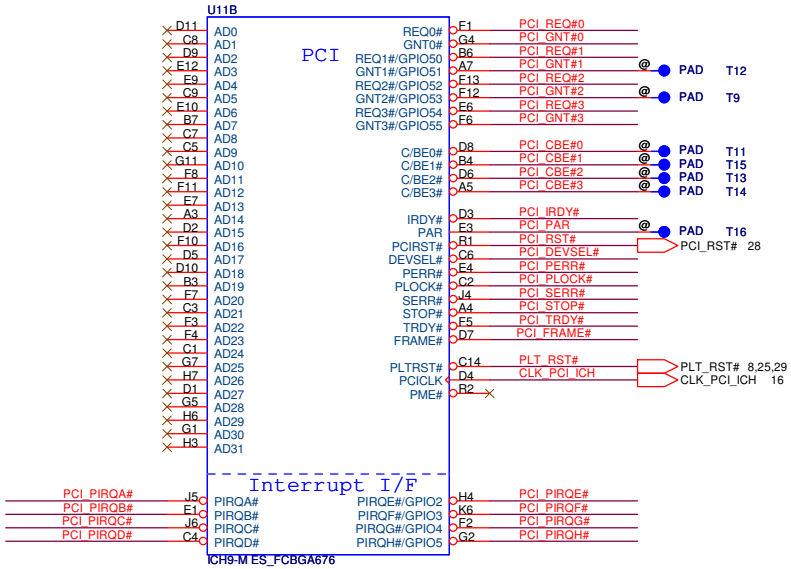
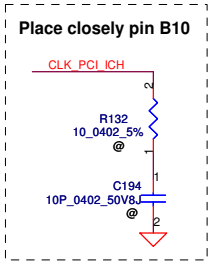
			Date: Wednesday, September 02, 2009; Sheet 18 of 45

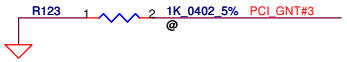
DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)



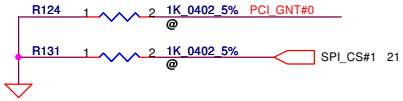


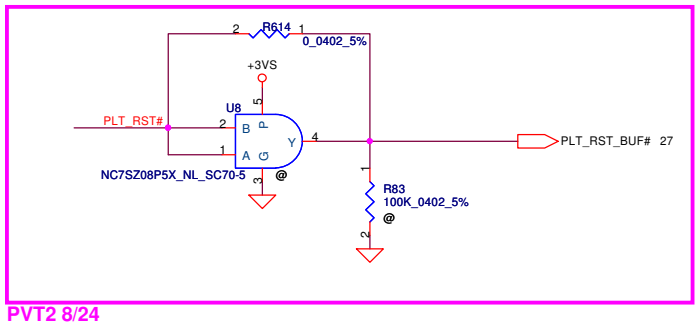


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*



Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*





PVT2 8/24

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2009/08/25

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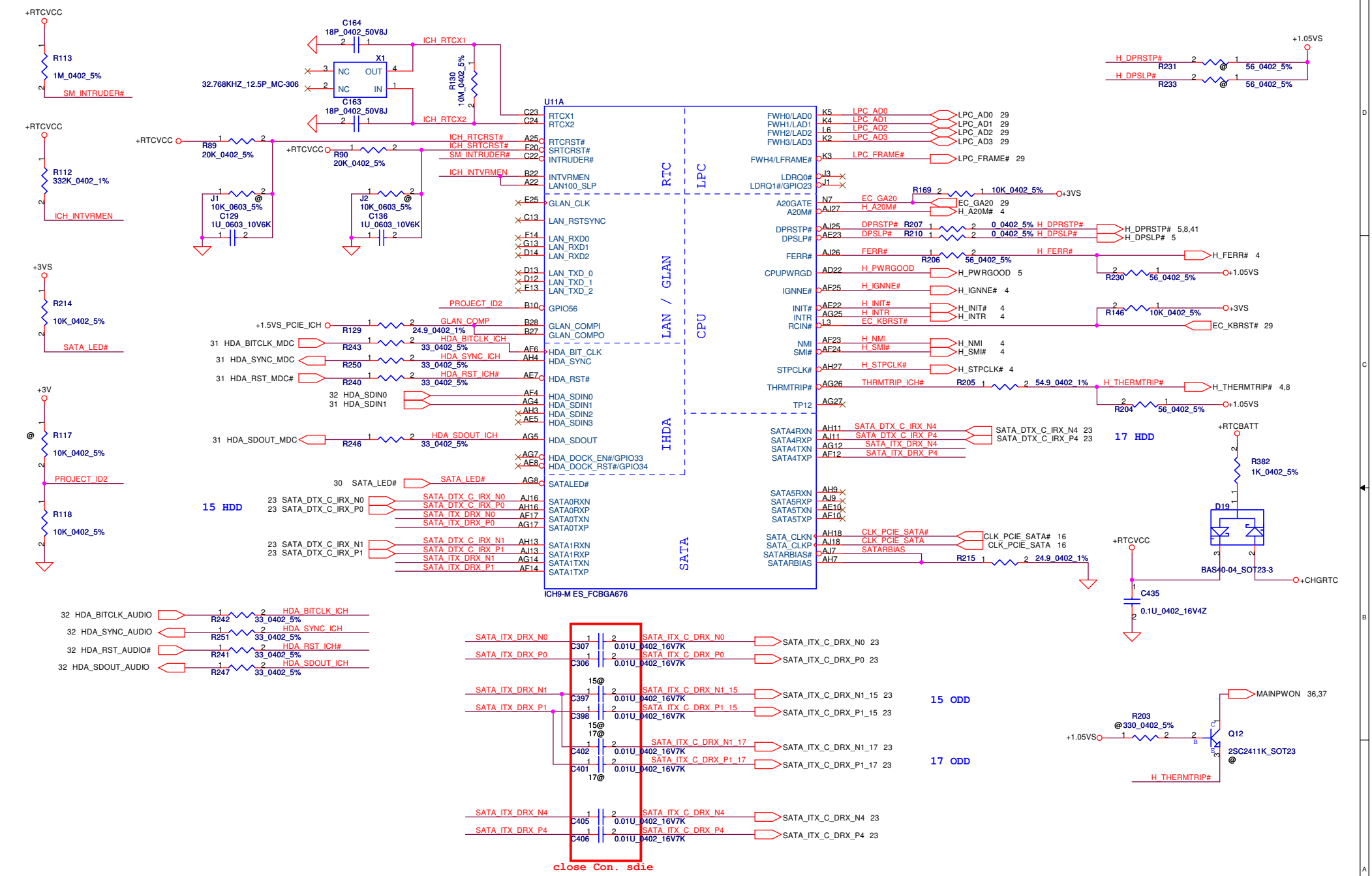
Compal Electronics, Inc.

Title: ICH9M(1/4)-PCI

Size | Document Number: NAWF3 M/B LA-4854P Schematic | Rev 0.1

Date: Wednesday, September 02, 2009 | Sheet 19 of 45



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Issued Date	2009/08/25	Deciphered Date	2009/08/25

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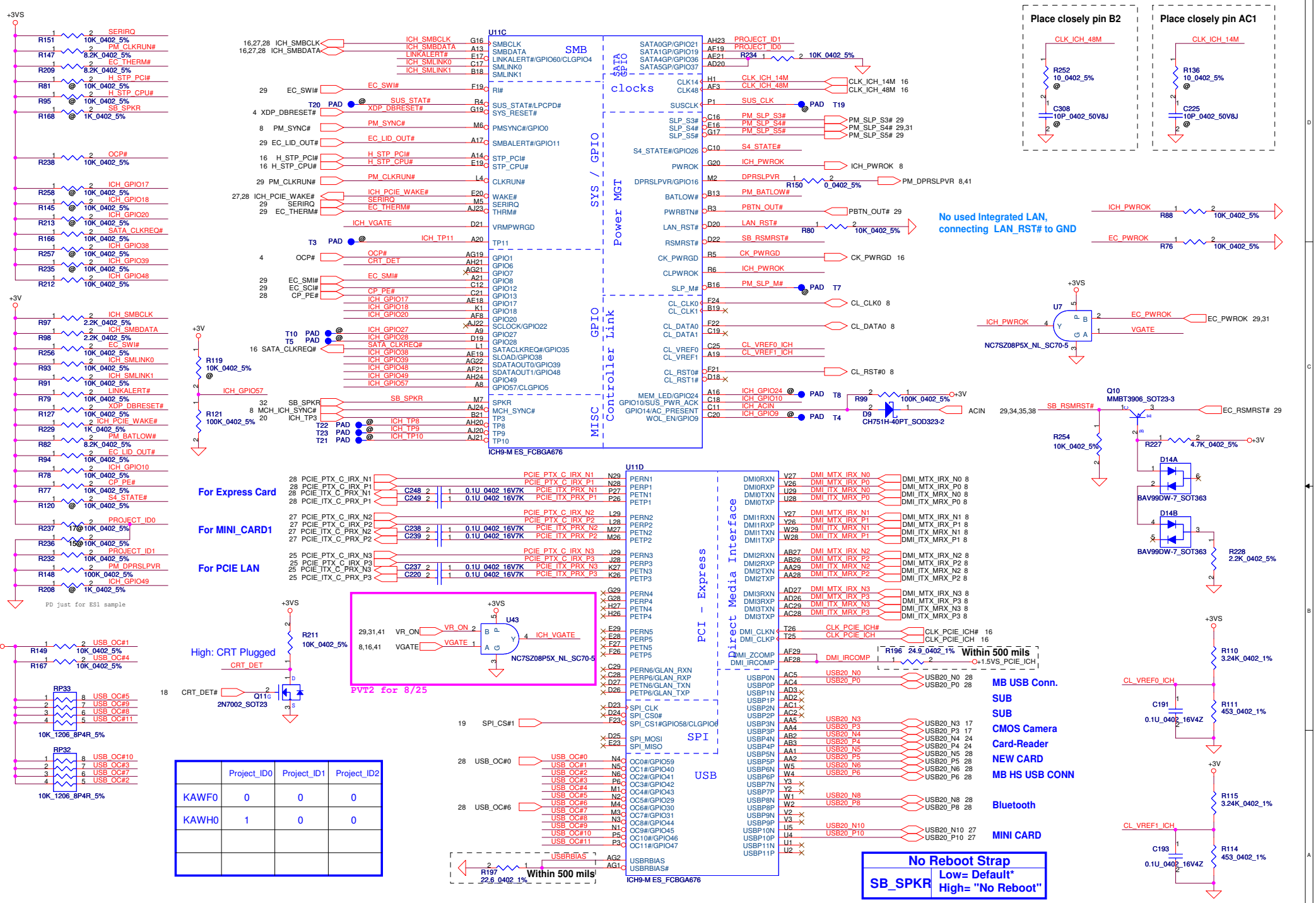
Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 20 of 45



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KAWH0	1	0	0

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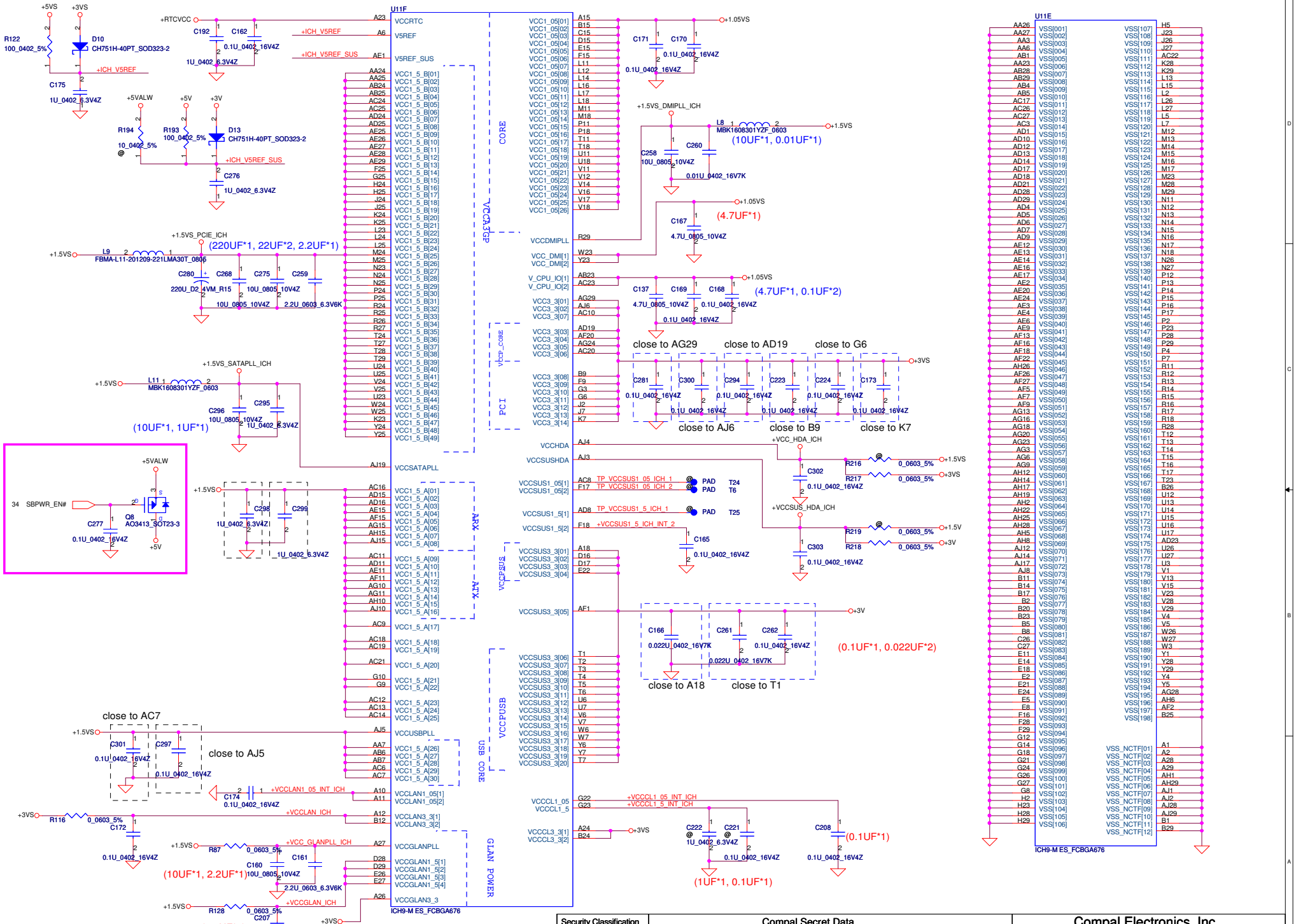

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Issued Date	2009/08/25	Deciphered Date	2009/08/25

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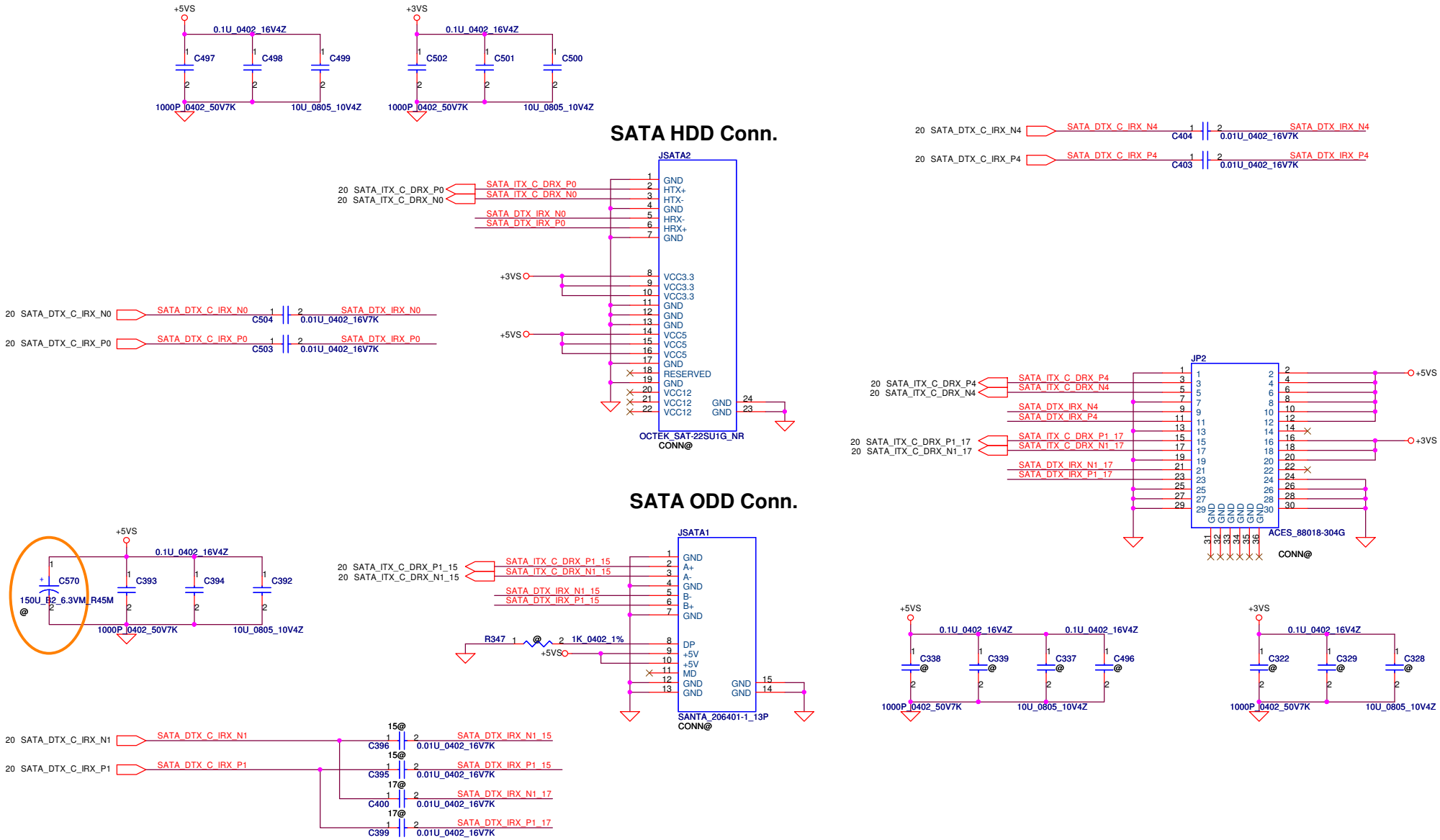
Compal Electronics, Inc.

Title: ICH9M(4/4)-POWER&GND

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 22 of 45



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Issued Date	2009/08/25	Deciphered Date	2009/08/25

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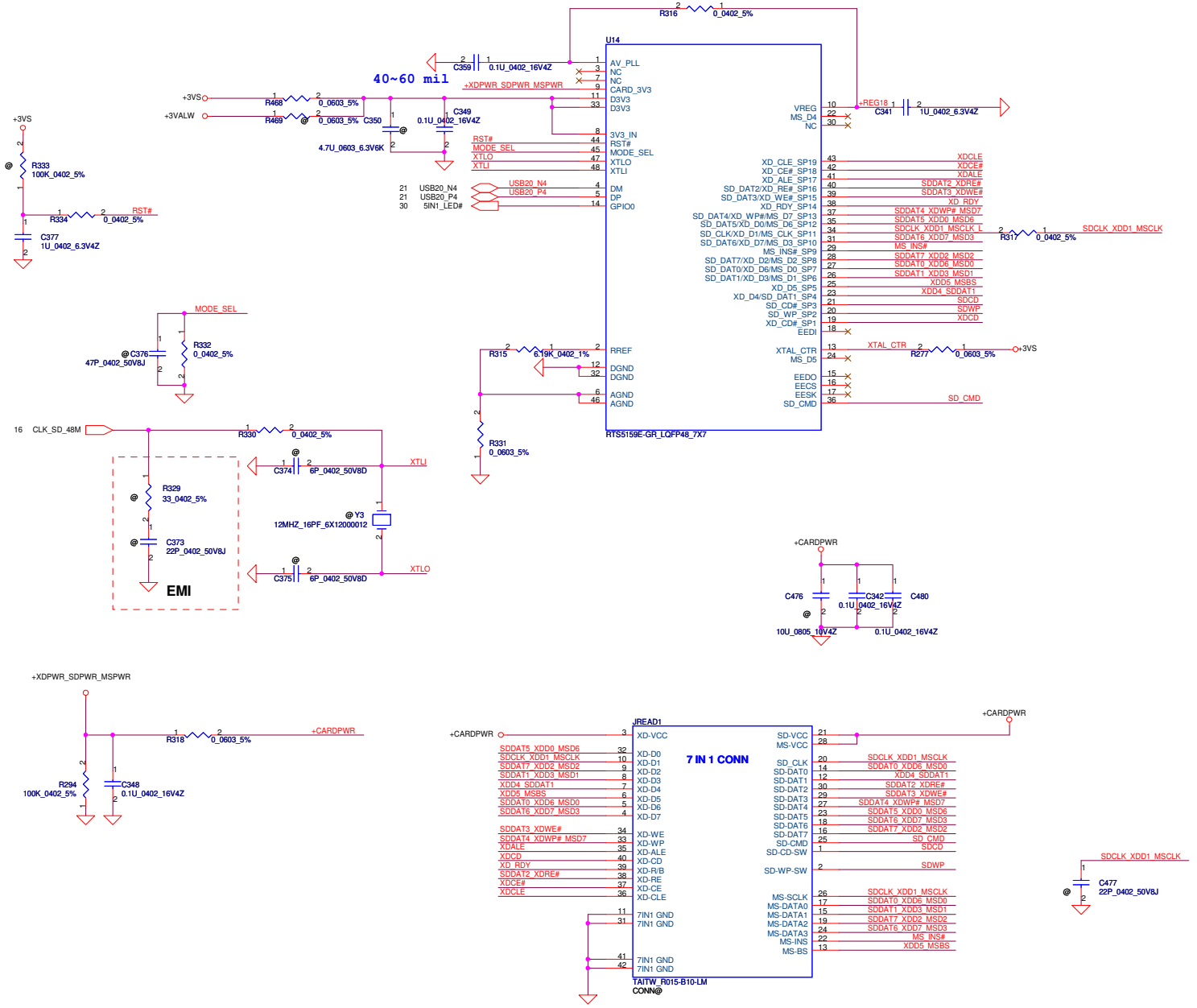
Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 23 of 45



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2009/08/25

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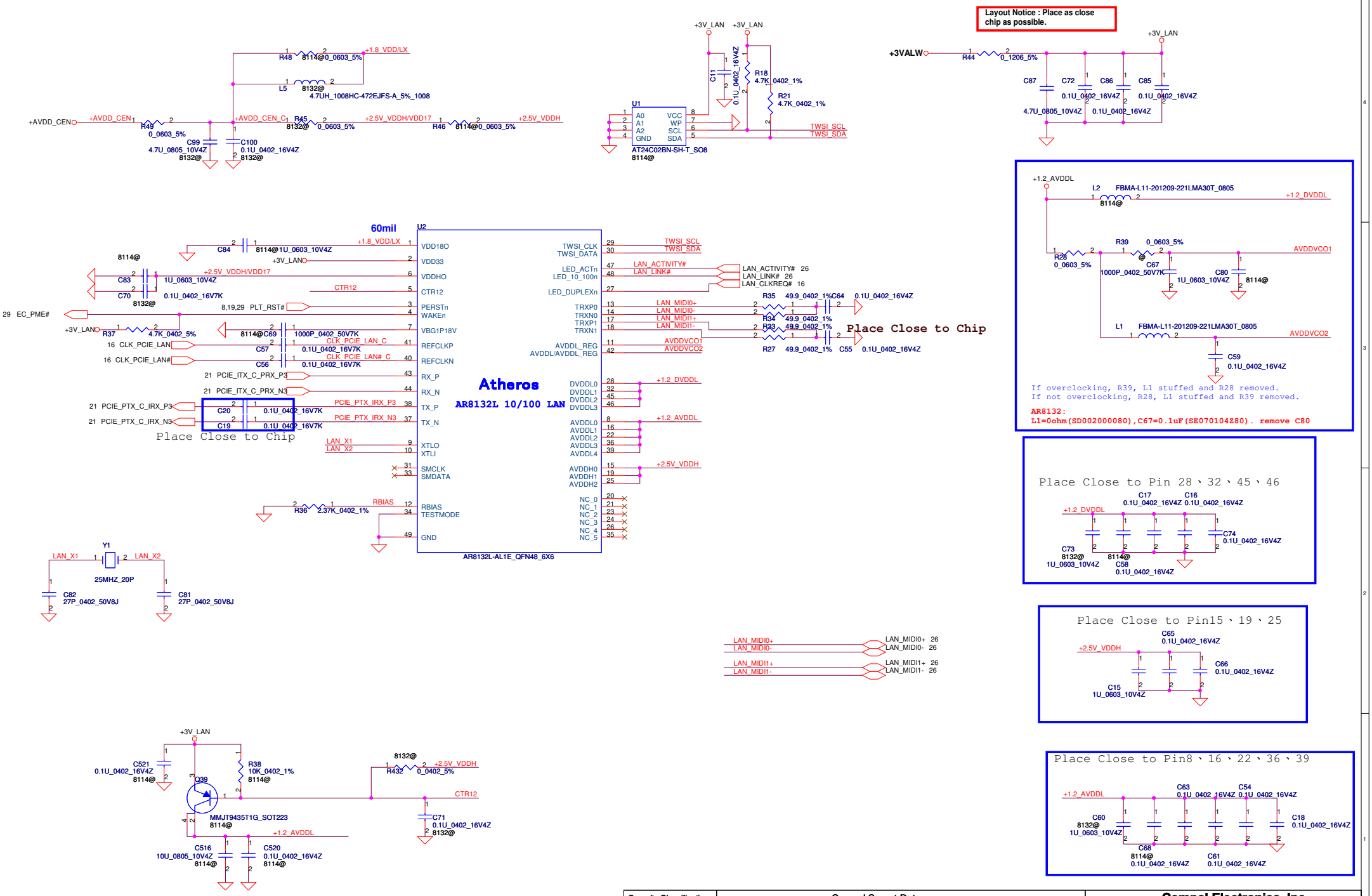
Compal Electronics, Inc.

Title: **5 in 1 Card reader**

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 24 of 45



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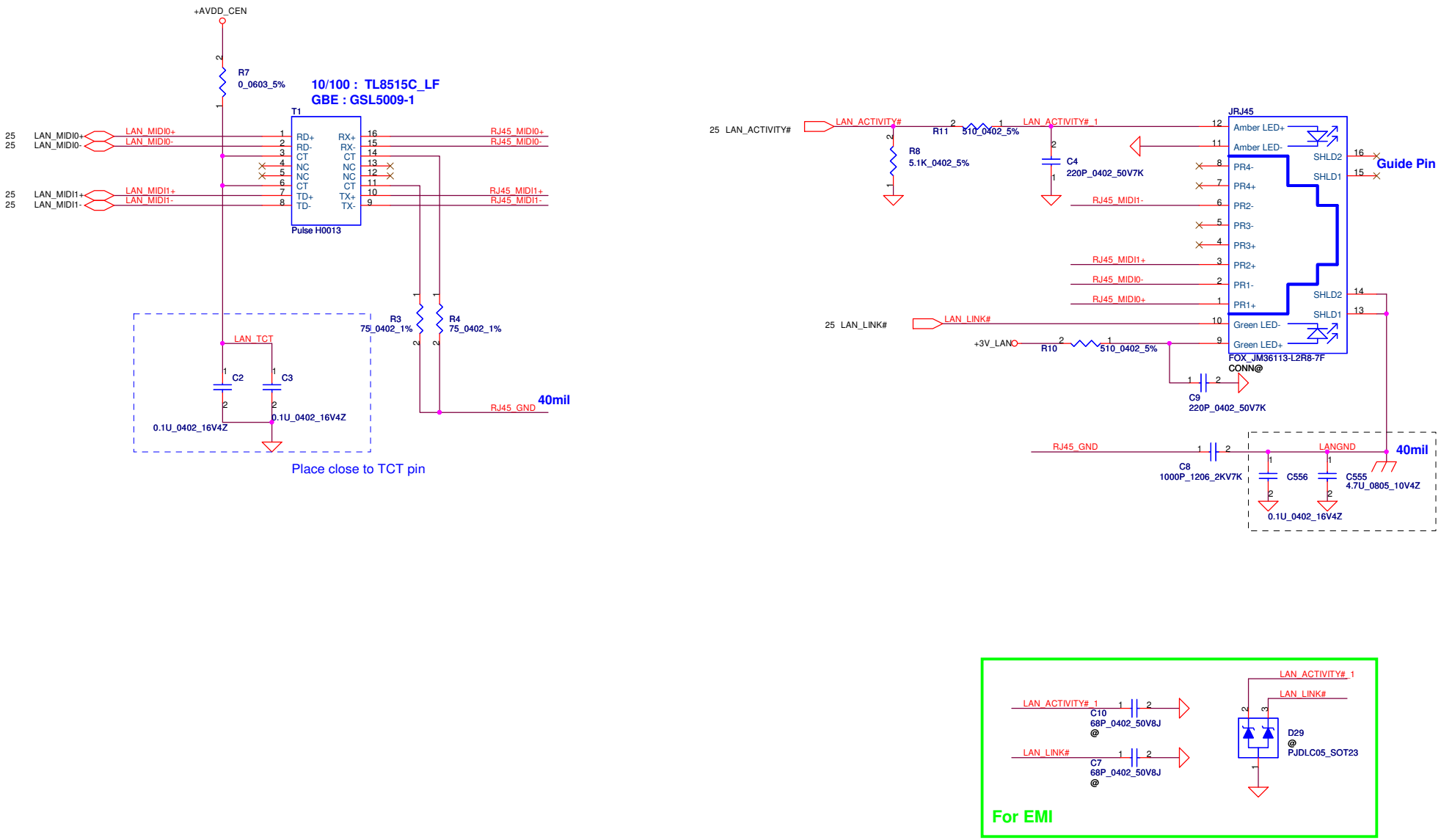
				Date: Wednesday, September 02, 2009; Sheet 25 of 45



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2009/08/25

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Compal Electronics, Inc.

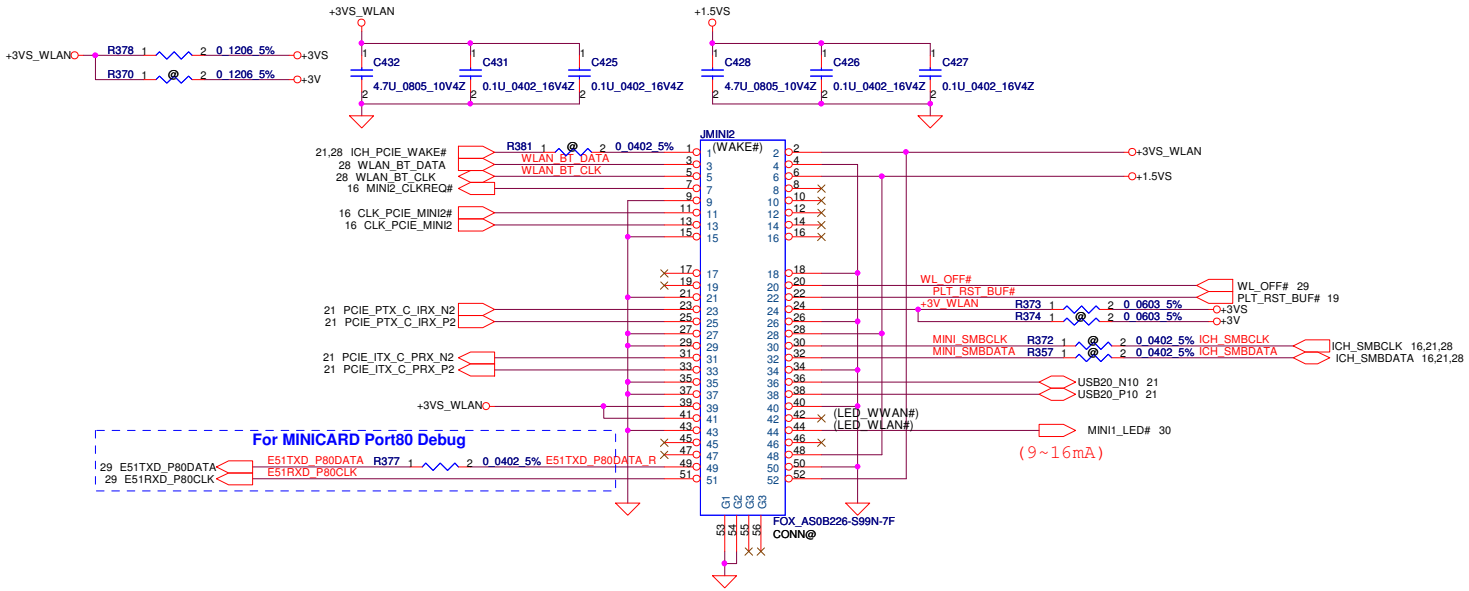
Title: LAN Magnetic & RJ45

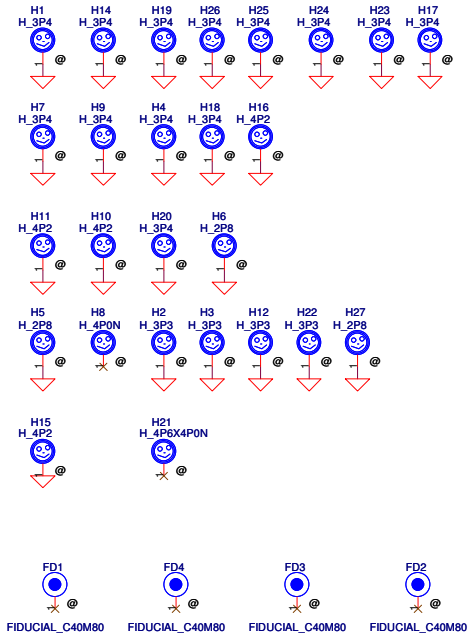
Size: B | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 26 of 45

For Wireless LAN

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)





Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date	2009/08/25	Title: MINI CARD (WLAN & TV-Tuner)
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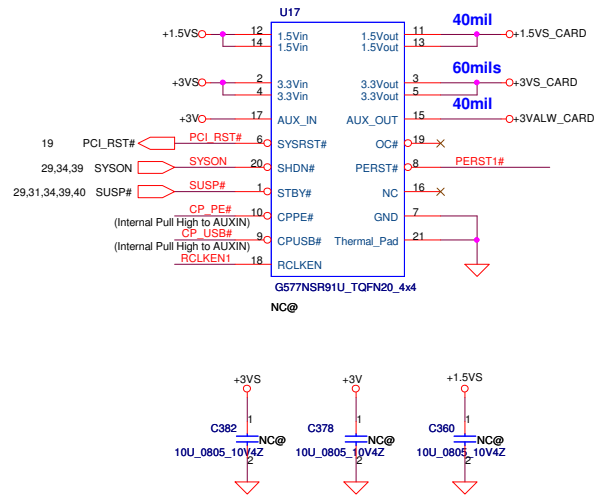
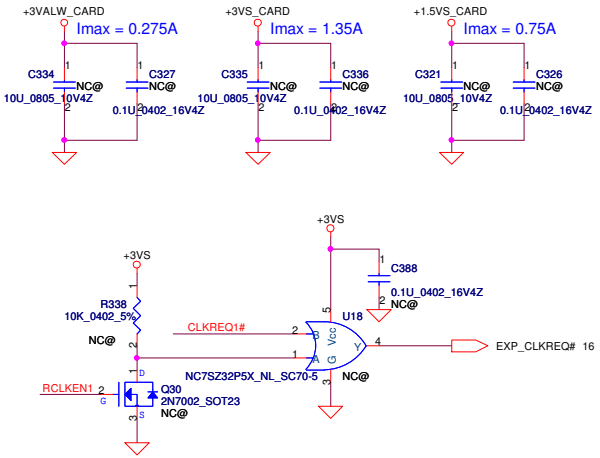
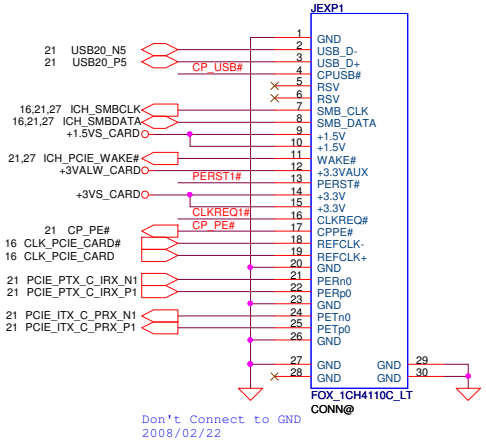
				Date: Wednesday, September 02, 2009; Sheet 27 of 45

New Card Power Switch

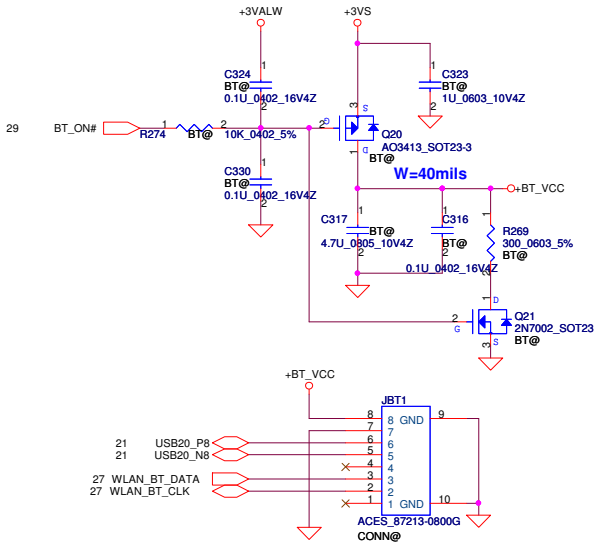




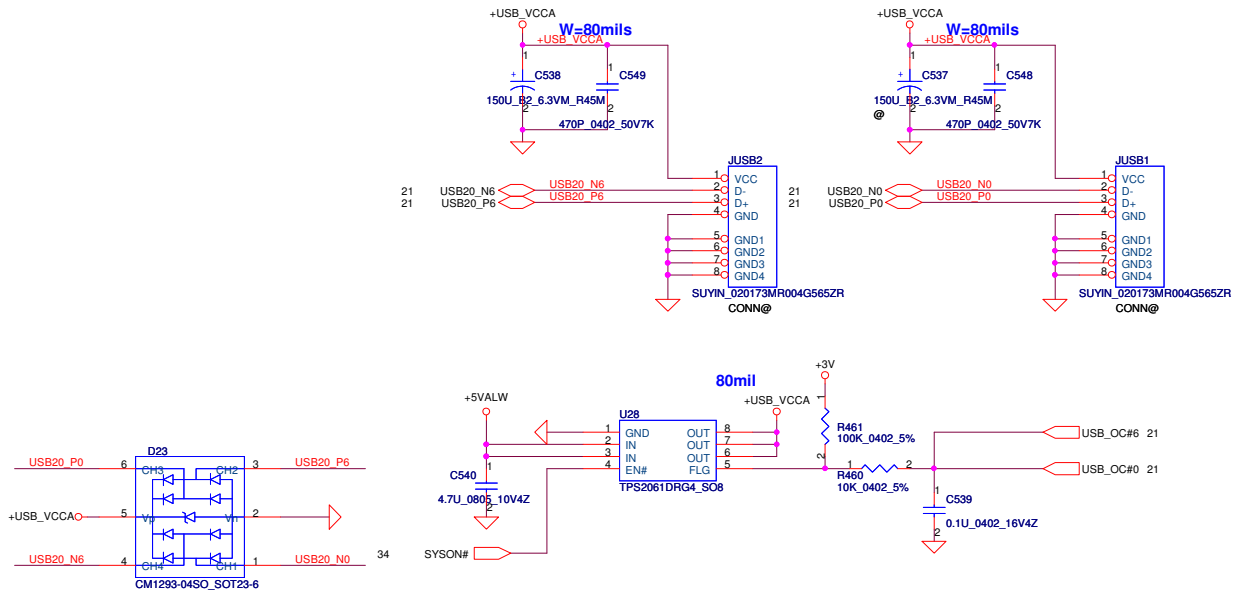
New Card Socket (Left/TOP)



Bluetooth Conn.



USB CONN.



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Issued Date	2009/08/25	Deciphered Date	2009/08/25	Title: NEW CARD & USB Connector
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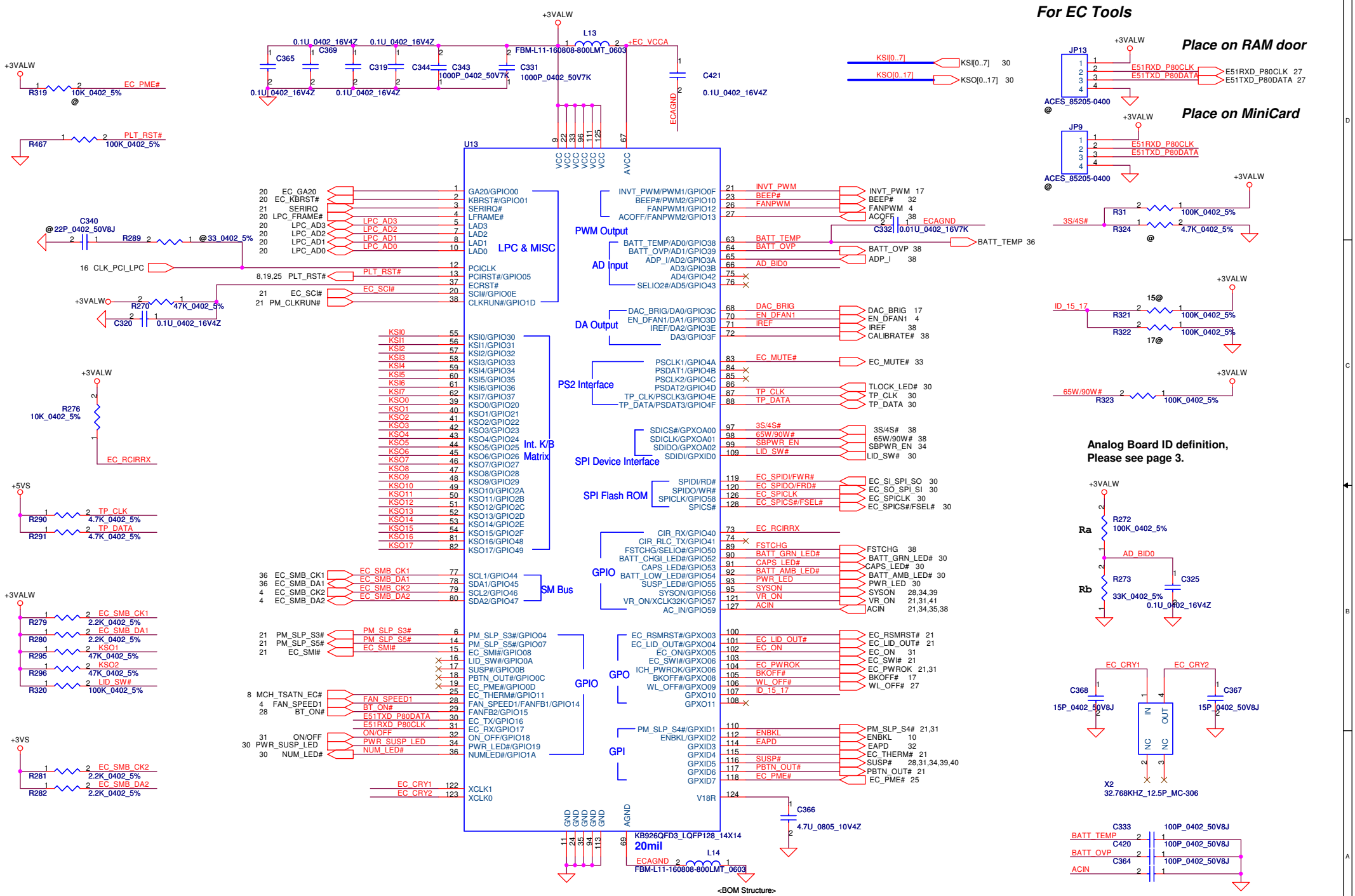
				Date: Wednesday, September 02, 2009; Sheet 28 of 45



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2009/08/25

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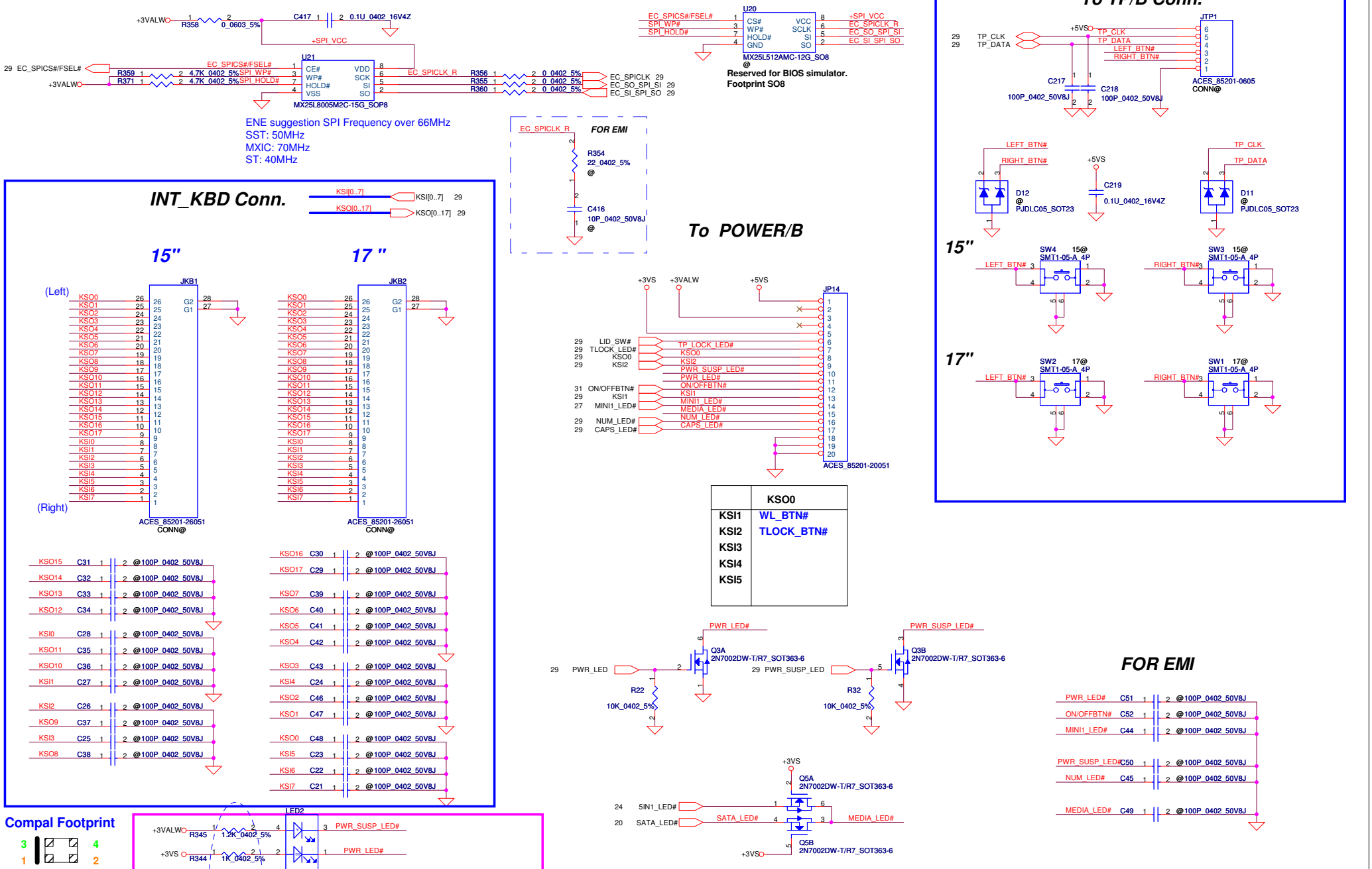
Compal Electronics, Inc.

Title: EC ENE KB926

Size: B | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 29 of 45



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2009/08/25

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Compal Electronics, Inc.

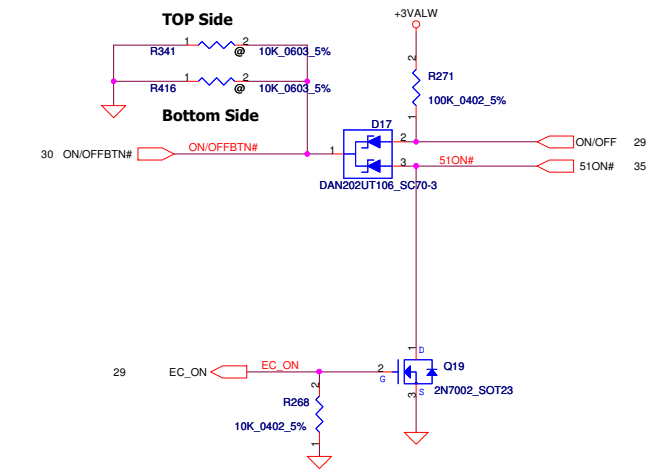
Title: BIOS, I/O Port & K/B Connector

Size: B | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

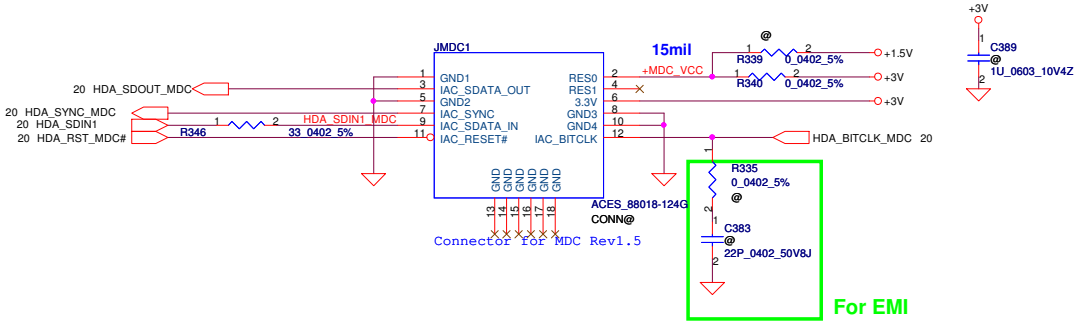
Date: Wednesday, September 02, 2009 | Sheet 30 of 45

Power Button

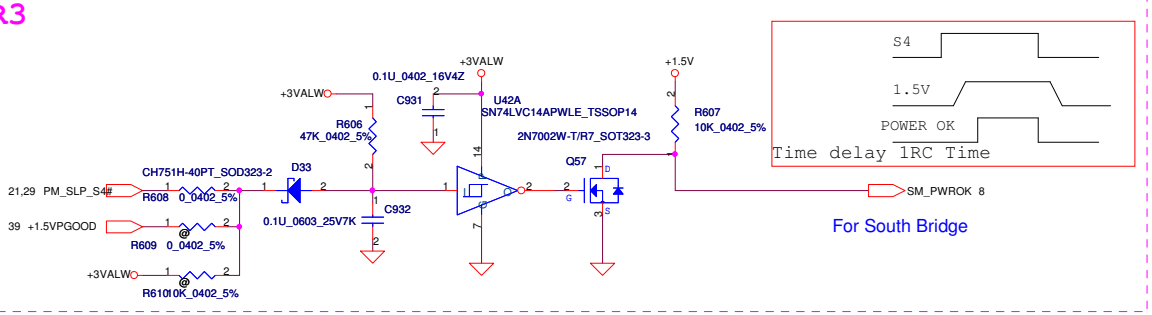
ON/OFF switch



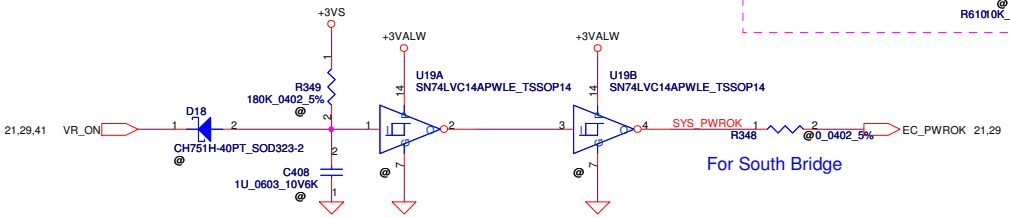
HDA MDC Conn.

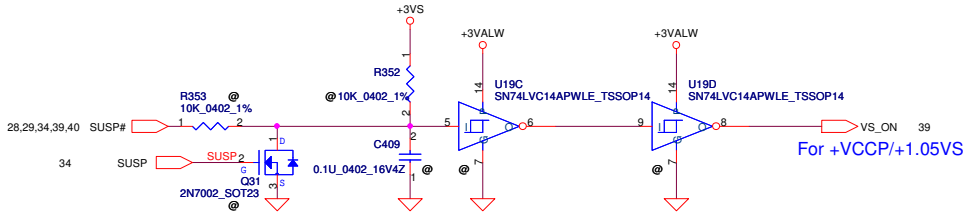


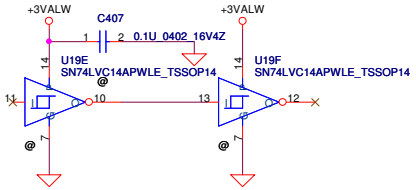
DDR3



Power ON Circuit







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Issued Date	2009/08/25	Deciphered Date 2009/08/25	Title: Power OK, Reset , MDC
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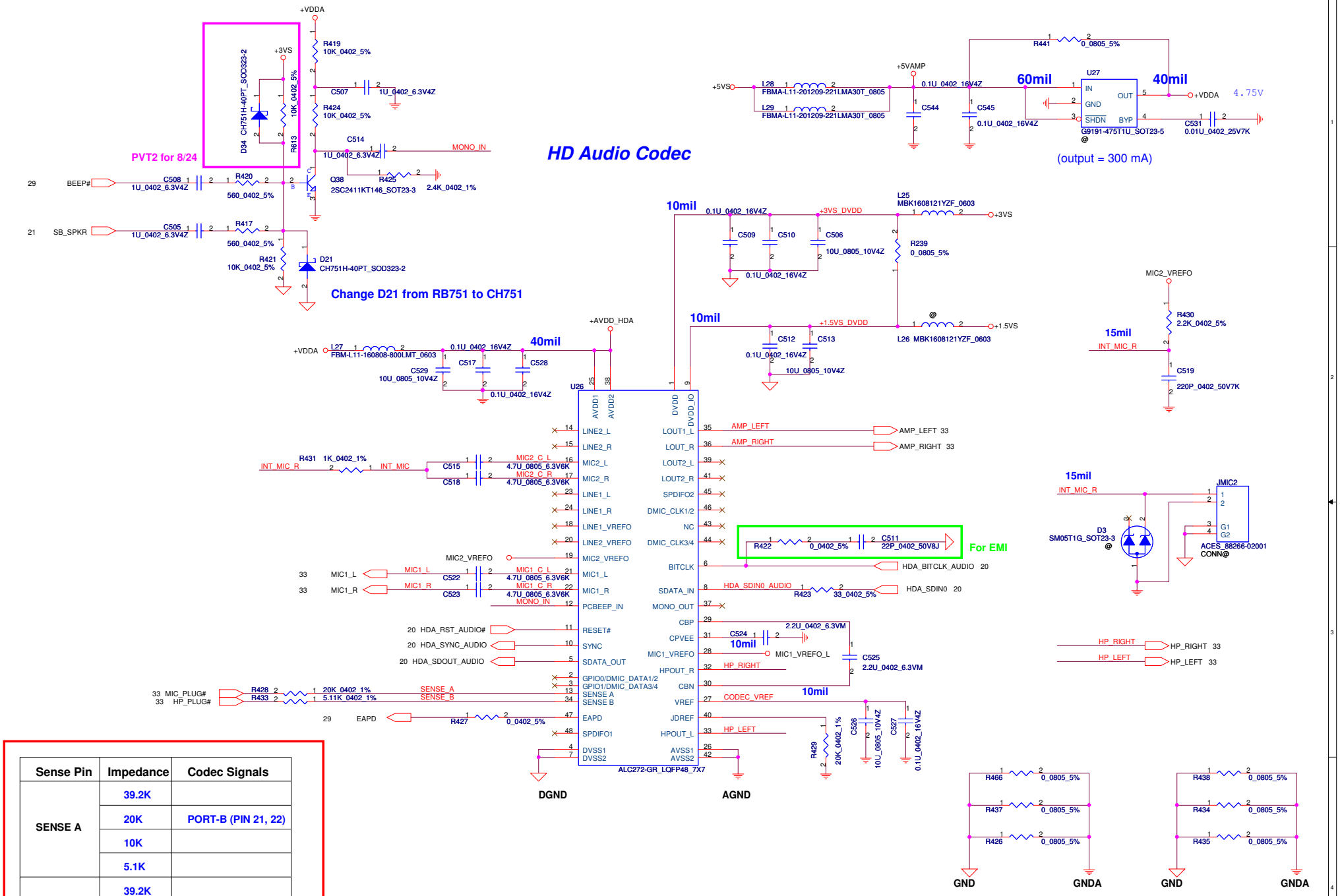
			Date: Wednesday, September 02, 2009 / Sheet 31 of 45



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	
	20K	PORT-B (PIN 21, 22)
	10K	
	5.1K	
SENSE B	39.2K	
	20K	
	10K	
	5.1K	PORT-H (PIN 32,33)

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Issued Date	2009/08/25	Deciphered Date 2009/08/25	Title: HD Audio Codec ALC272
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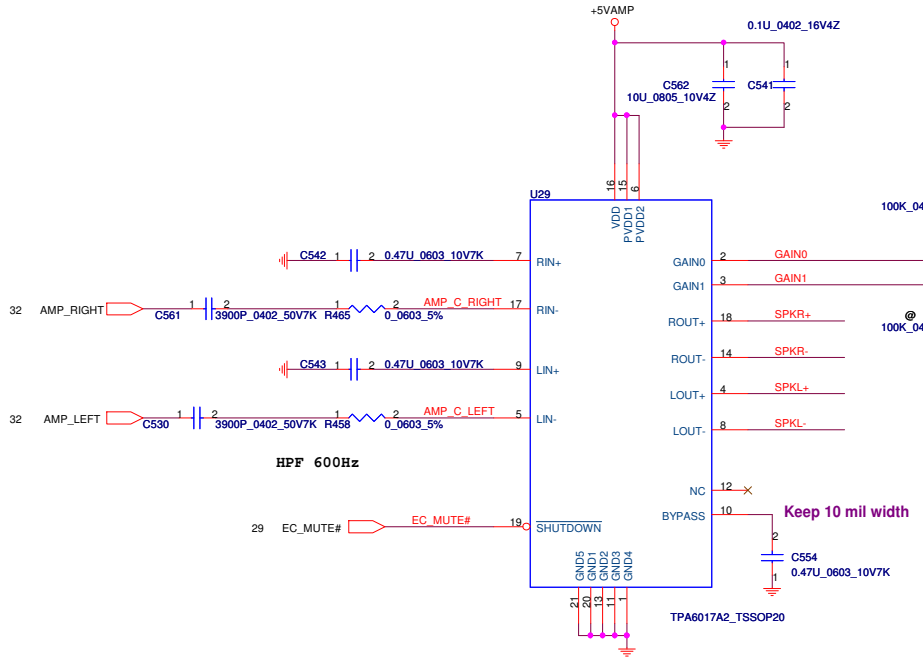
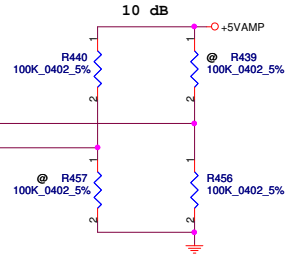
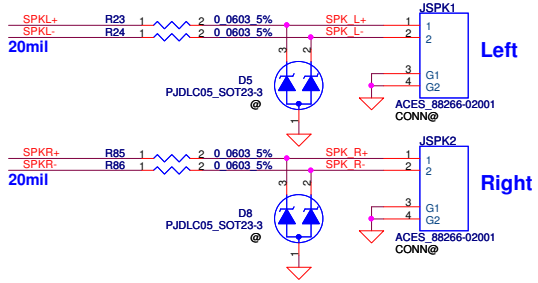
			Date: Wednesday, September 02, 2009; Sheet 32 of 45

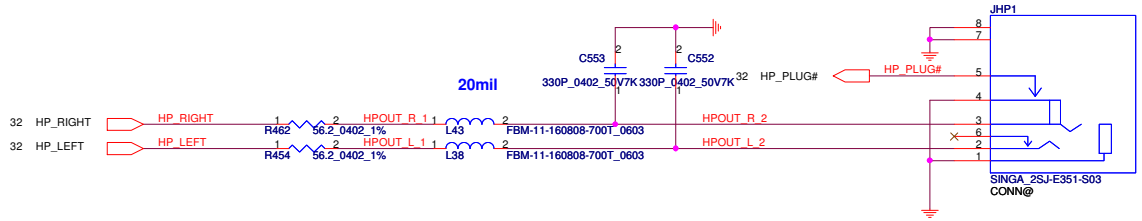




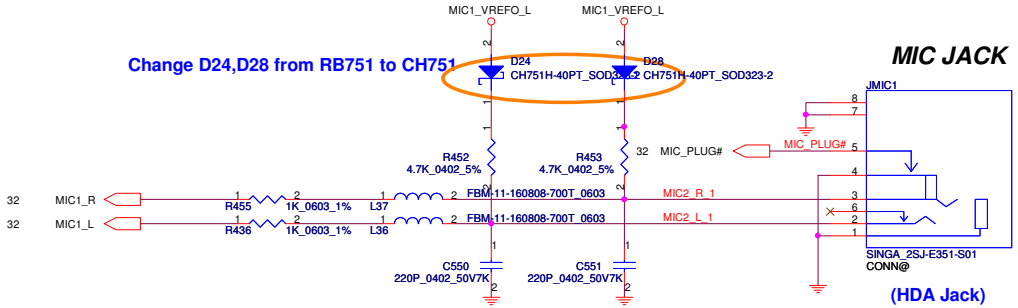
Int. Speaker Conn.



LINE Out/Headphone Out



MIC JACK



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date 2009/08/25	Title: Amplifier & Audio Jack
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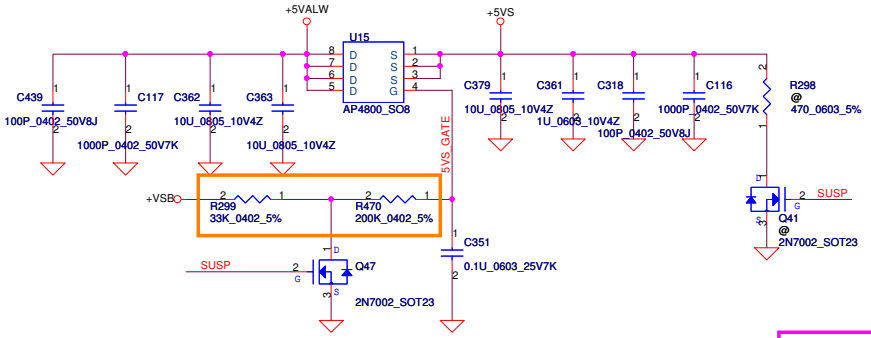
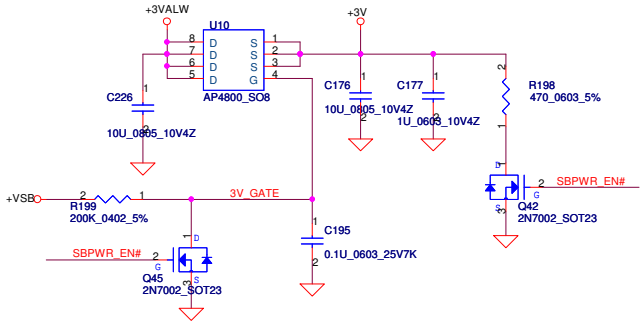
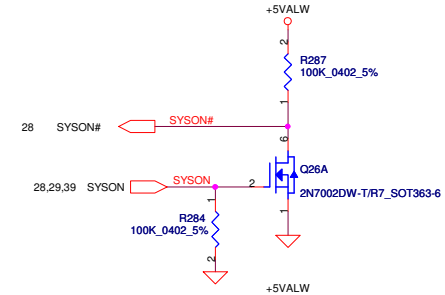
			Date: Wednesday, September 02, 2009; Sheet 33 of 45

+5VALW TO +5VS

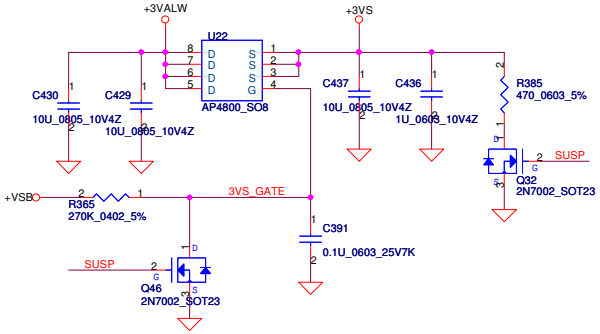


+3VALW TO +3V_SB(ICH8M AUX Power)

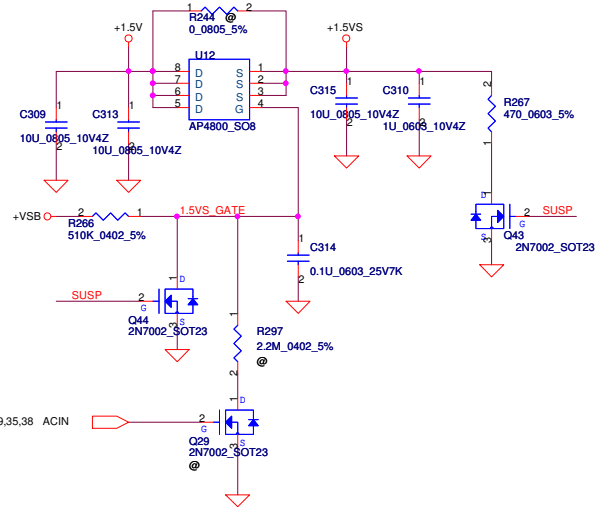




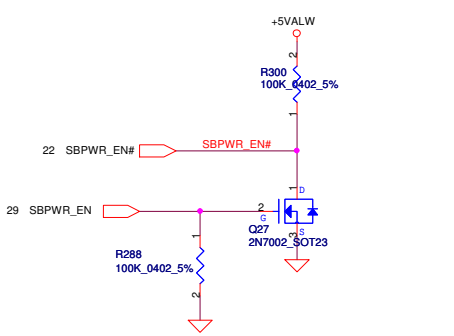
+3VALW TO +3VS

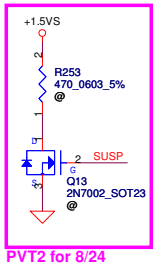


+1.5V to +1.5VS

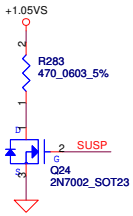


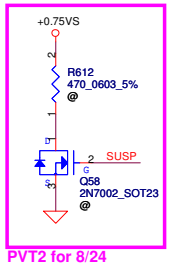
PVT2 for 8/24



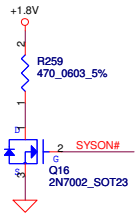


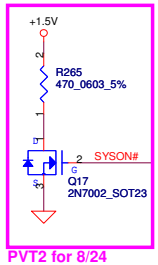
PVT2 for 8/24





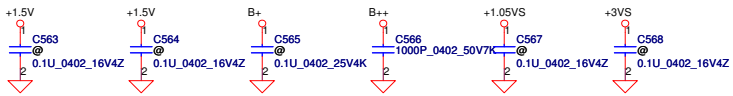
PVT2 for 8/24





PVT2 for 8/24

Reserve for EMI request



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date 2009/08/25	Title: DC Interface
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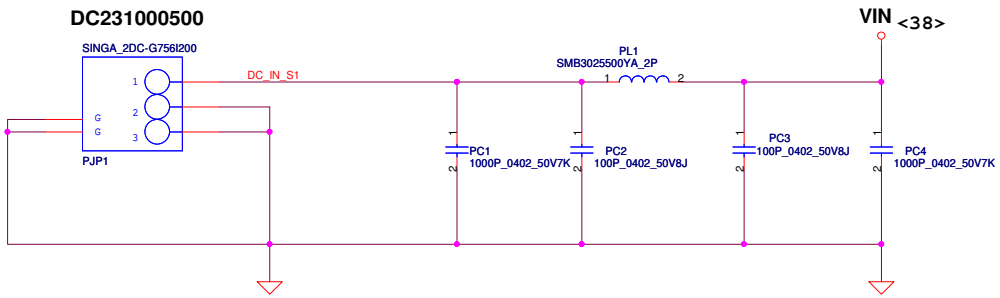
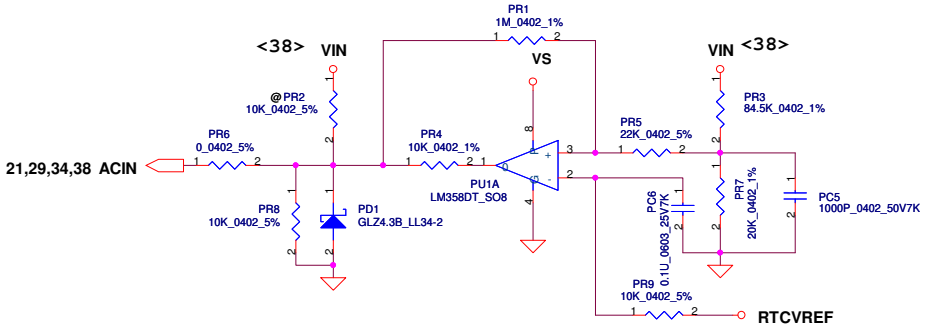
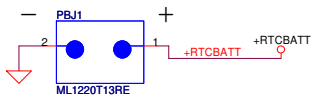
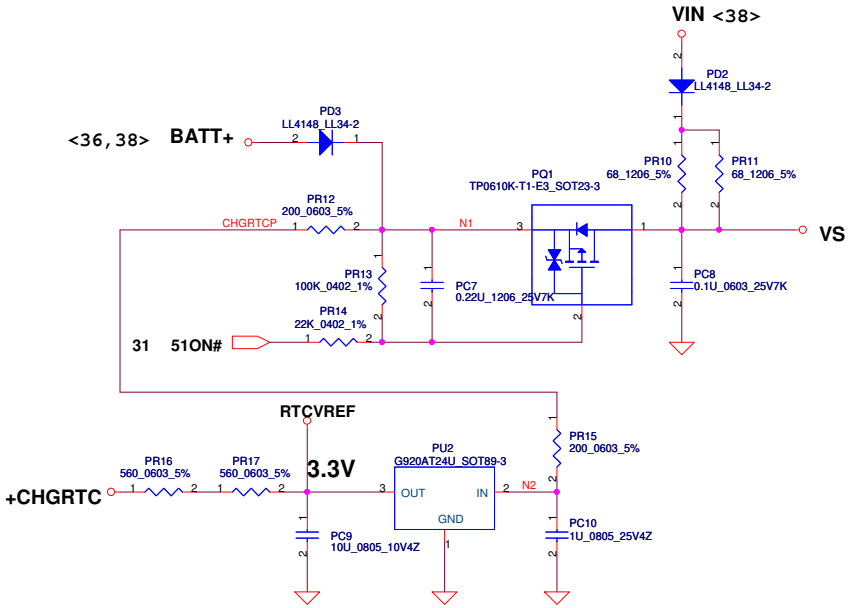
			Date: Wednesday, September 02, 2009; Sheet 34 of 45

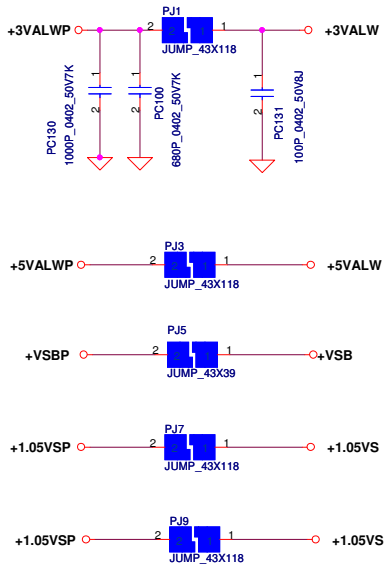




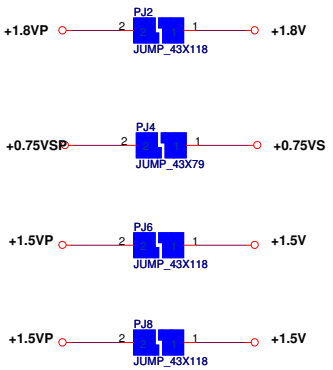
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V







Delete (PJ16/PJ17/PJ18)
1.1VLDO + VGA_CORE JUMPER



Security Classification	Compal Secret Data		
Issued Date	2009/07/17	Deciphered Date	2009/07/17

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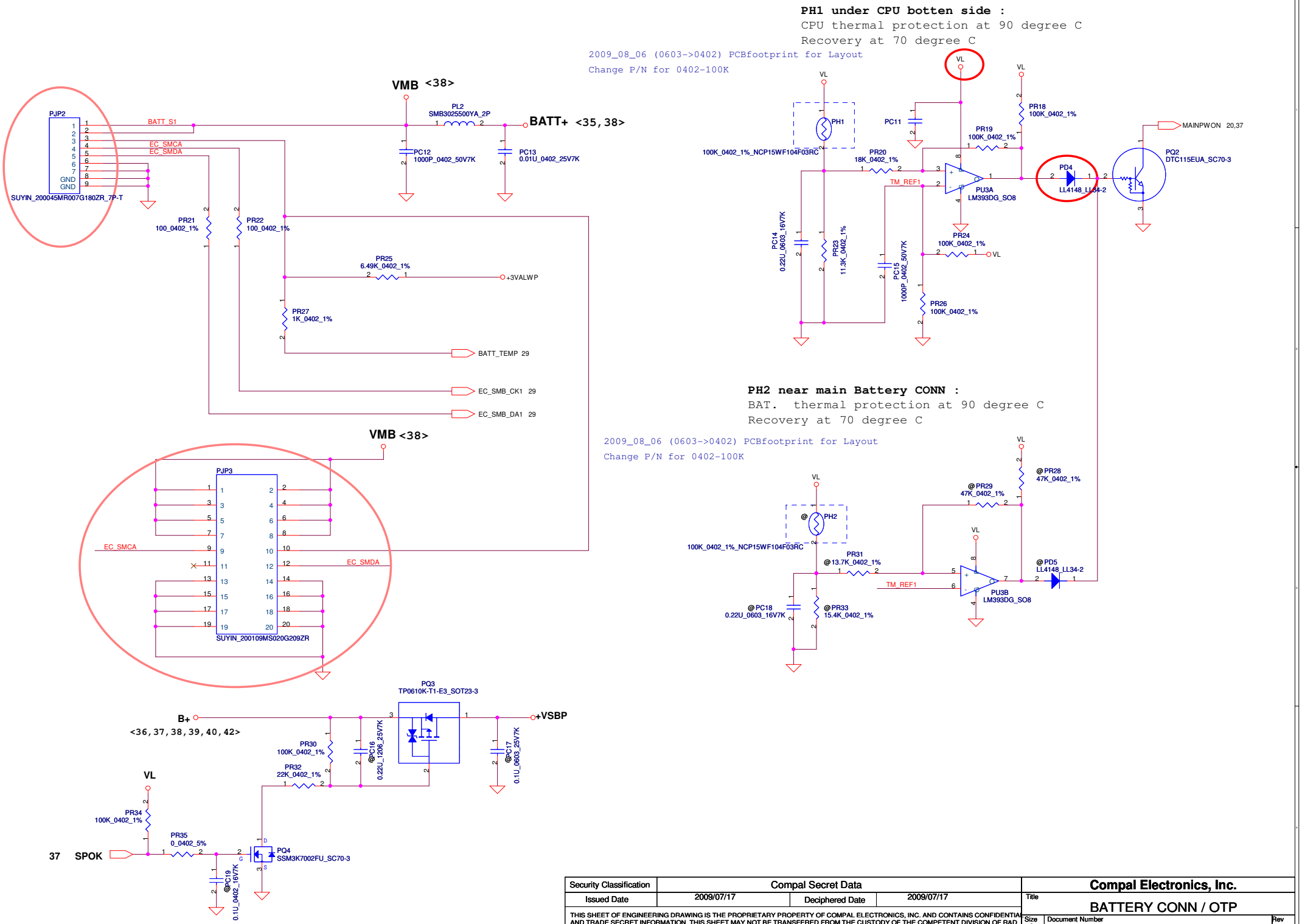
Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 35 of 45



Security Classification	Compal Secret Data		
Issued Date	2009/07/17	Deciphered Date	2009/07/17

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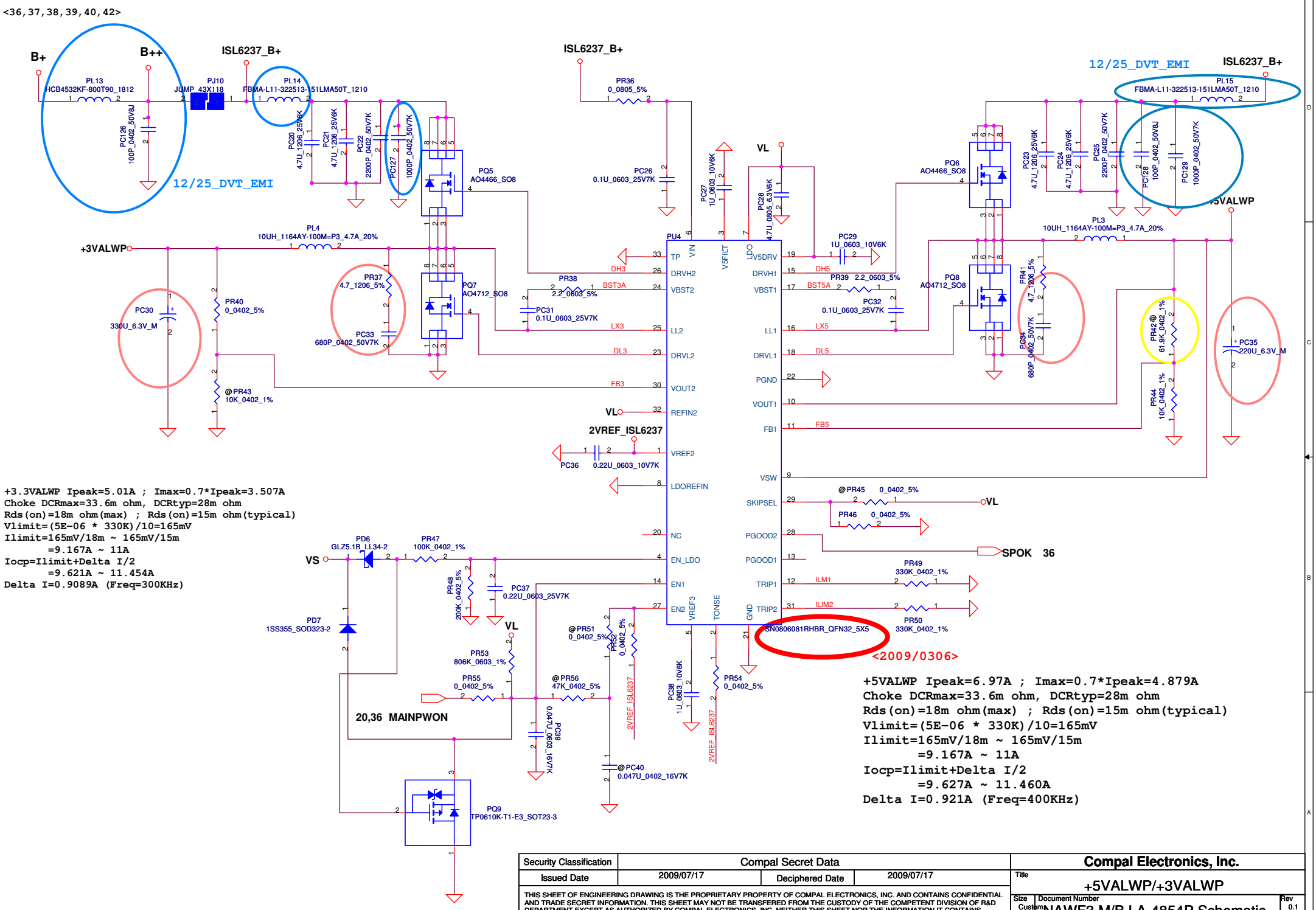
Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 36 of 45



+3.3VALWP Ipeak=5.01A ; Imax=0.7*Ipeak=3.507A
Choke DCRmax=33.6m ohm, DCRtyp=28m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.621A ~ 11.454A
Delta I=0.9089A (Freq=300KHz)

+5VALWP Ipeak=6.97A ; Imax=0.7*Ipeak=4.879A
Choke DCRmax=33.6m ohm, DCRtyp=28m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.627A ~ 11.460A
Delta I=0.921A (Freq=400KHz)

Security Classification	Compal Secret Data		
Issued Date	2009/07/17	Deciphered Date	2009/07/17

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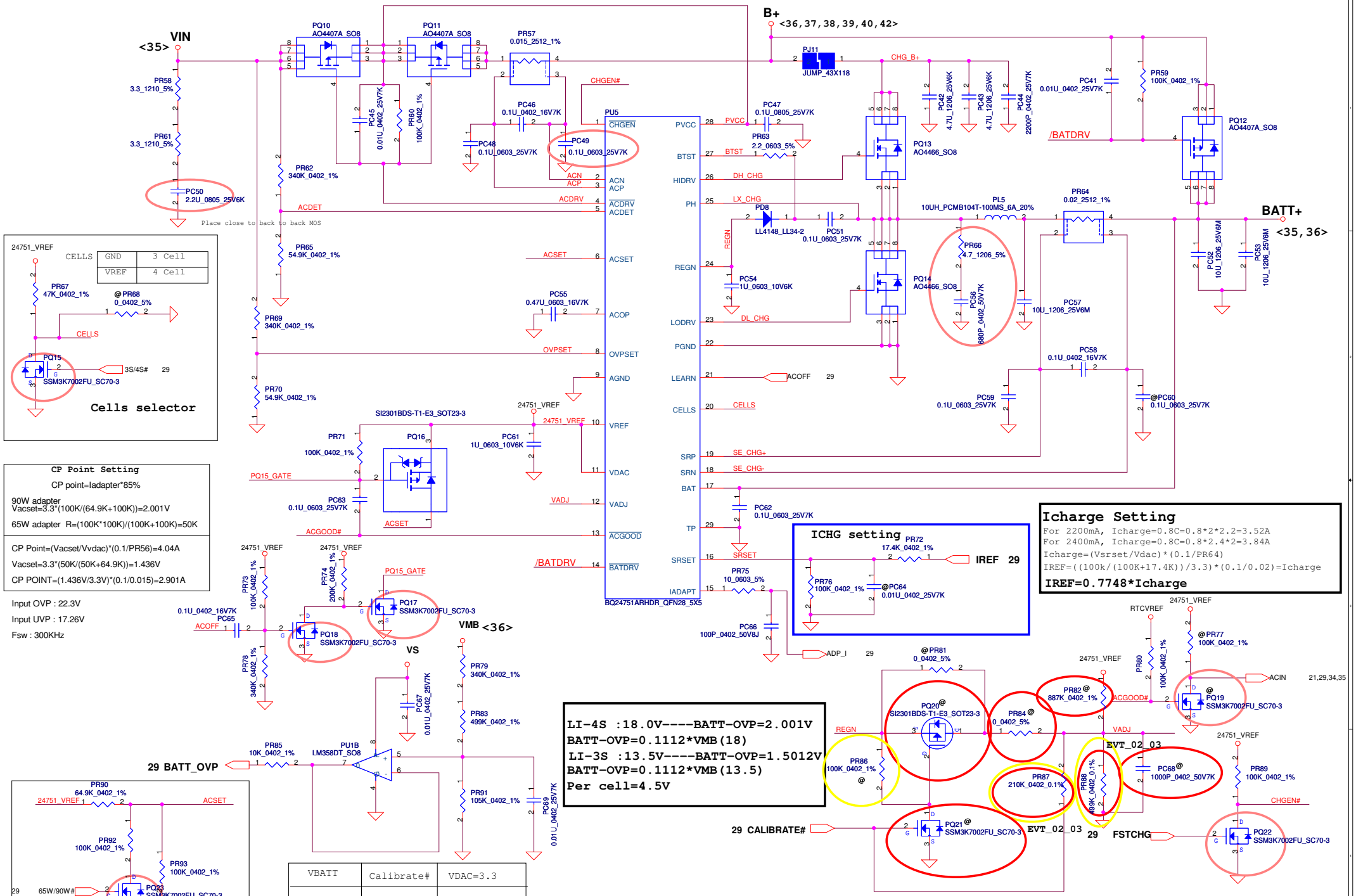
Compal Electronics, Inc.

Title: +5VALWP/+3VALWP

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 37 of 45



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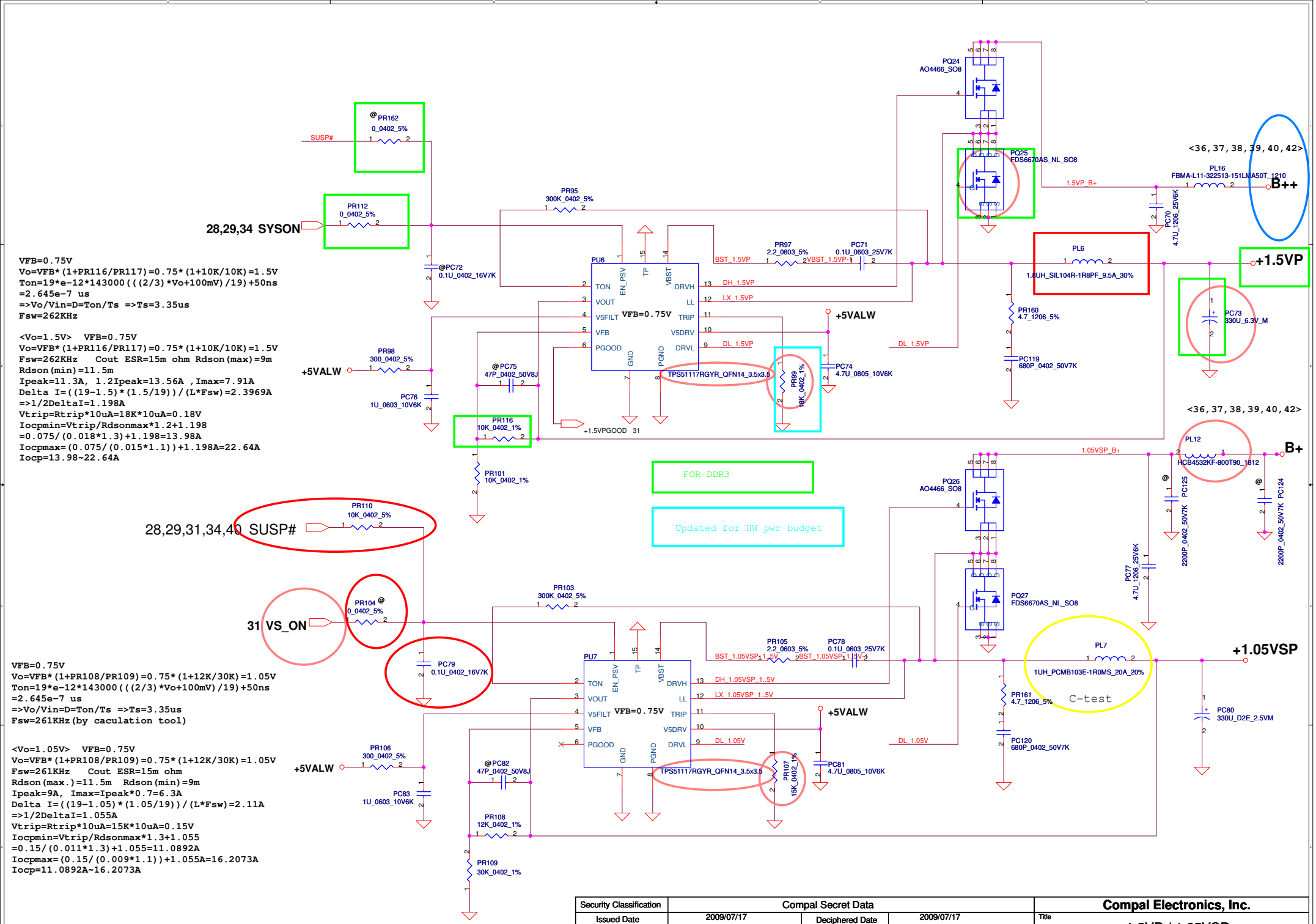

Security Classification	Compal Secret Data		
Issued Date	2009/07/17	Deciphered Date	2009/07/17

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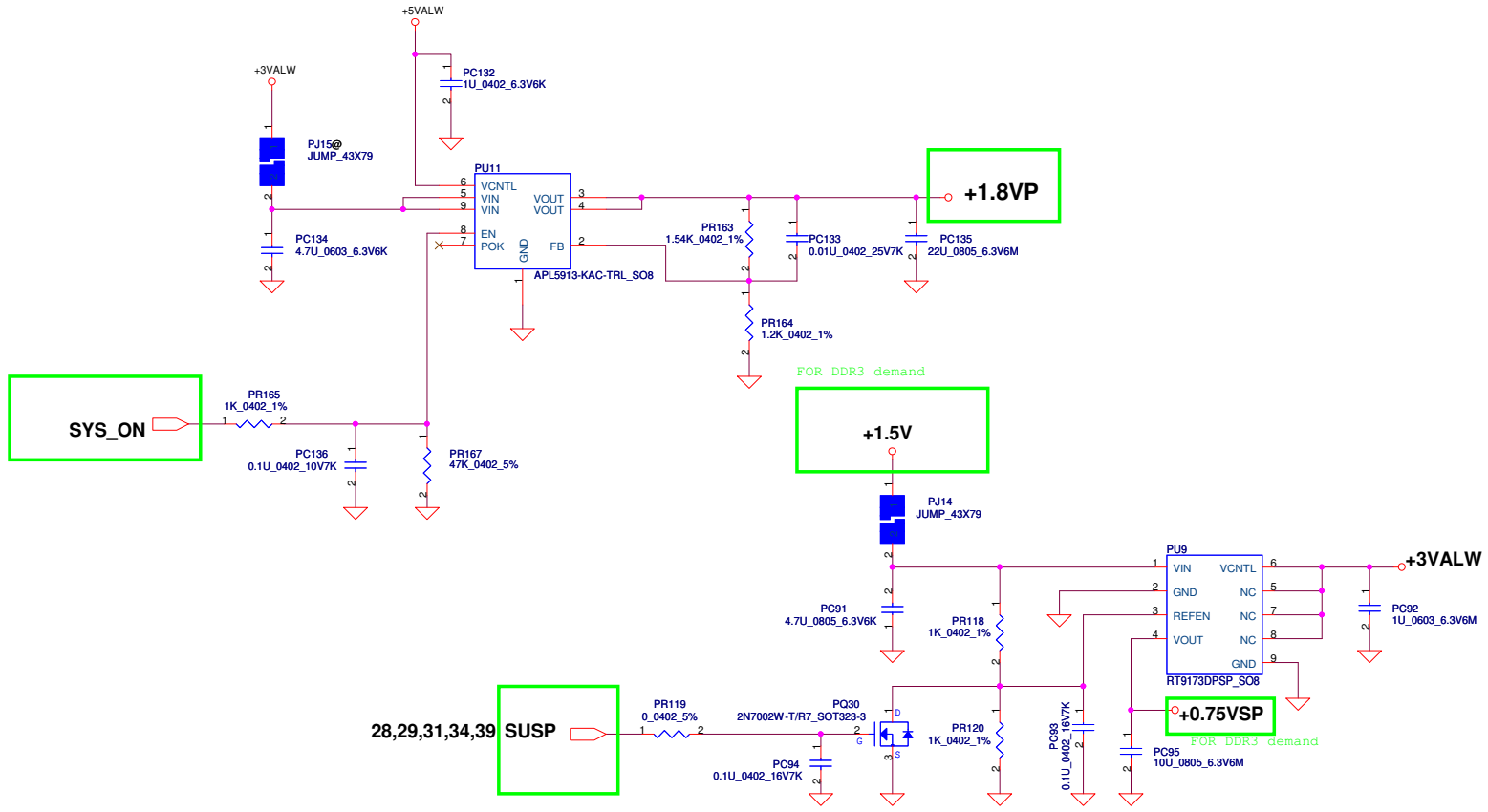
Compal Electronics, Inc.

Title: 1.8VP / 1.05VSP

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 39 of 45



Security Classification	Compal Secret Data		
Issued Date	2009/07/17	Deciphered Date	2009/07/17

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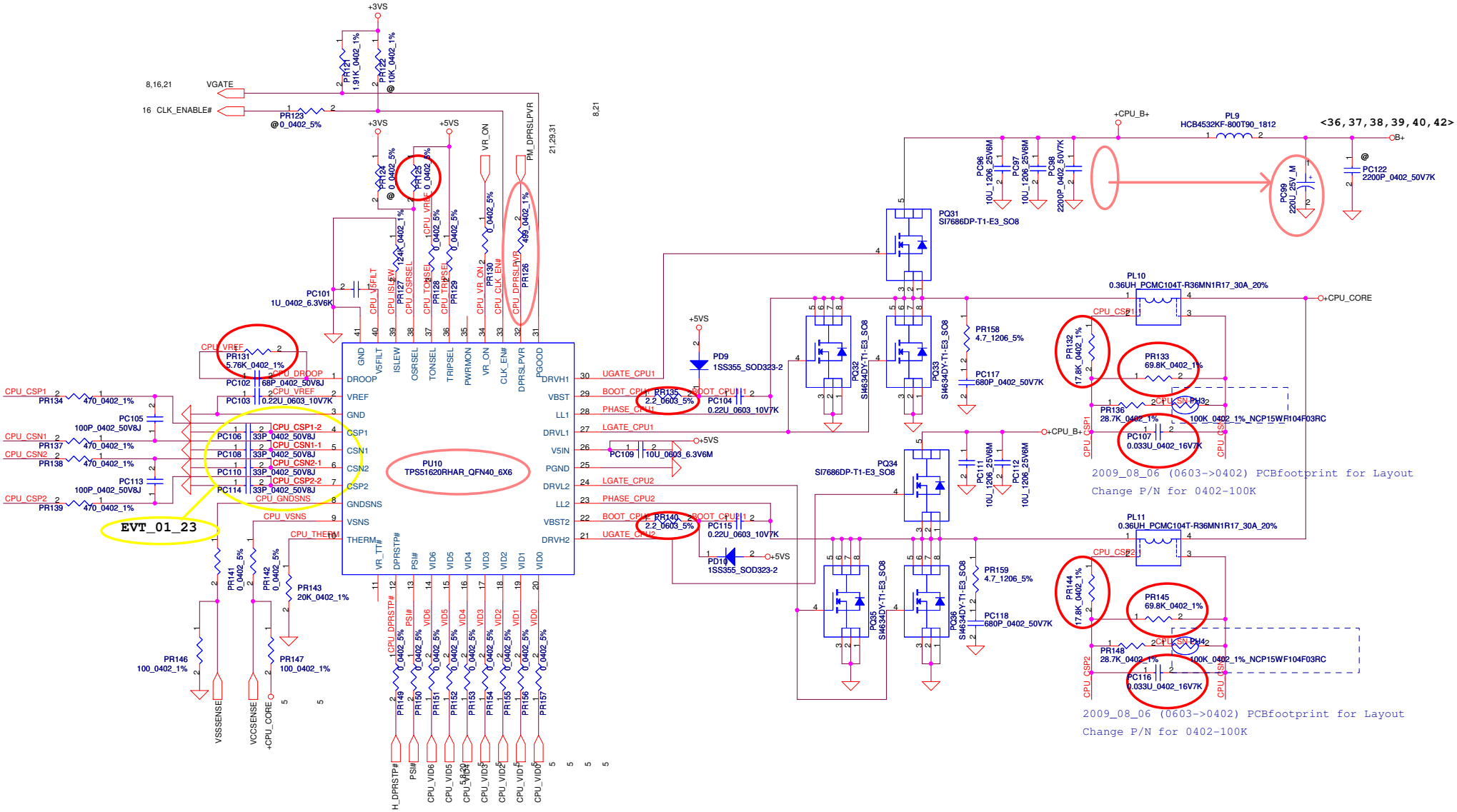
Compal Electronics, Inc.

Title: +1.5VP

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 40 of 45



Security Classification	Compal Secret Data		
Issued Date	2009/07/17	Deciphered Date	2009/07/17

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Compal Electronics, Inc.

Title: +CPU_CORE

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 0.1

Date: Wednesday, September 02, 2009 | Sheet 41 of 45

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add PC57 :10U_1206_25V_6M	0.1	38	Add PC57 :10U_1206_25V_6M	20080902	EVT
2		Add snubber for EMI	0.1	42	Add snubber for EMI	20080915	EVT
3		Shift PC99 from +cpu_B+ to B+	0.1	42	Shift PC99 from +cpu_B+ to B+	20080915	EVT
4		Add PJ15 to B+	0.1	39	Add PJ15 to B+	20080915	EVT
5		PR135 and PR140 change to 0_0603_5%	0.1	42	PR135 and PR140 change to 0_0603_5%	20080915	EVT
6	Charger feedback trace too long	ADD PC49	0.2	38	ADD PC49	20081124	DVT
7	Power sequence error	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	0.2	40	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	20081124	DVT
8	Load line over spec	PR131: change to 5.76K_0402_1%	0.2	42	PR131: change to 5.76K_0402_1%	20081124	DVT
9	3D hang	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	0.2	38	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	20081124	DVT
10	3D hang	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	0.2	39	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	20081124	DVT
11	3D hang	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	0.2	39	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	20081124	DVT
12	EMI solution	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	0.2	37	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	20081124	DVT
13	EMI solution	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	0.2	42	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	20081124	DVT
16	EMI solution	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	0.2	42	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	20081124	DVT
17	EMI solution	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	0.2	39	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	20081124	DVT

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/01/21	Deciphered Date	2010/01/21
Title	PIR (PWR)		
Size Custom	Document Number KAWF0 M/B LA-4431P Schematic		Rev 1.0
Date: Wednesday, September 02, 2009	Sheet 42 of 45		

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
18	Battery & HW solution	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1% +1.05VSP PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K +1.5VP PR112: Reserve(@) 0_0402_5%	0.2	38 39 40	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1% +1.05VSP PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K +1.5VP PR112: Reserve(@) 0_0402_5%	20081124	DVT
19	EMI soultion	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	0.3	35 40	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	20081224	PVT
20	POWER Solution	+3VALWP/+5VALWP RT8206- Fix output 5V for HW no HDMI	0.3	37	+3VALWP/+5VALWP PR42: Reserve 61.9K_0402_1%	20090111	PVT

COMPAL ELECTRONICS

Title: PIR POWER2

Size | Document Number: KAWF0 M/B LA-4431P Schematic | Rev: 0.2

Date: Wednesday, September 02, 2009 | Sheet 43 of 45

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev	PG#	Modify List	Date	Phase
21	EMI solution	Reduce the Noise	0.3	37	Add PL 13 (HCB4532KF-800T90_1812) Add PL 14 (FBMA-L11-322513-151LMA50T_1210) Add PL 15 (FBMA-L11-322513-151LMA50T_1210) Add PC126 (100P_0402_50V8J) Add PC128 (100P_0402_50V8J) Add PC129 (1000P_0402_50V7K)	20090112	PVT
22	Battery solution	Adjust battery voltage	0.3	38	Reserve PR86 (100K_0402_1%)	20090112	PVT
23	Saturation current	1.8u choke saturation current too small	0.3	39	change PL7 to 1UH_PCMB103E-1R0MS_20A_20%	20090113	PVT
24	GP BOM	Tolerance: K:+-10% ; J:+-5%	0.4	42	Change PC106 to 33P_0402_50V8J Change PC108 to 33P_0402_50V8J Change PC110 to 33P_0402_50V8J Change PC114 to 33P_0402_50V8J	20090123	PVT

09/01

Security Classification	Compal Secret Data		
Issued Date	2009/01/21	Deciphered Date	2010/01/21

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Compal Electronics, Inc.

Title: HW (PWR)

Size: Custom | Document Number: KAWF0 M/B LA-4851P Schematic | Rev: 1.0

Date: Wednesday, September 02, 2009 | Sheet 45 of 45