

Compal Confidential

NCWG0/H0 Schematics Document

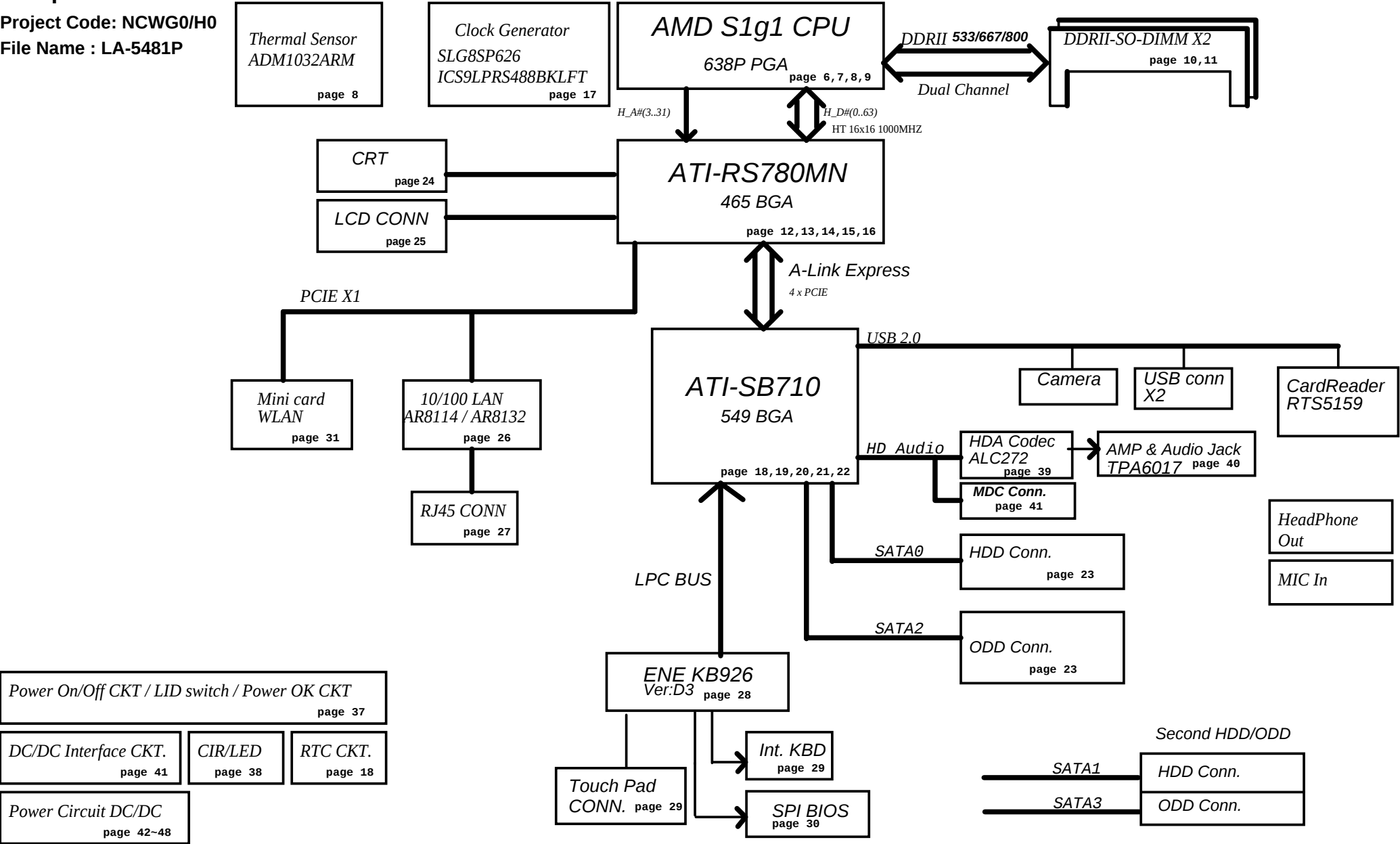
AMD S1g1 / RS780MN/ SB710

2009 / 06 / 24

LA-5481

Rev:1.0

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VIN	Adapter power supply (19V)			
B+	AC or battery power rail for power circuit.			
+CPU_CORE	Core voltage for CPU			
+0.9V	0.9V switched power rail for DDR terminator			
+1.2V_HT	1.2V switched power rail	ON	OFF	
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON		ON*
+1.8VS	1.8V switched power rail		OFF	
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

SB600 SM Bus 1 address		SB600 SM Bus 2 address	
Device	Address	Device	Address
Clock Generator	1101 001Xb	New Card	
DDR DIMM0	1001 000Xb		
DDR DIMM2	1001 010Xb		
Wireless Lan			

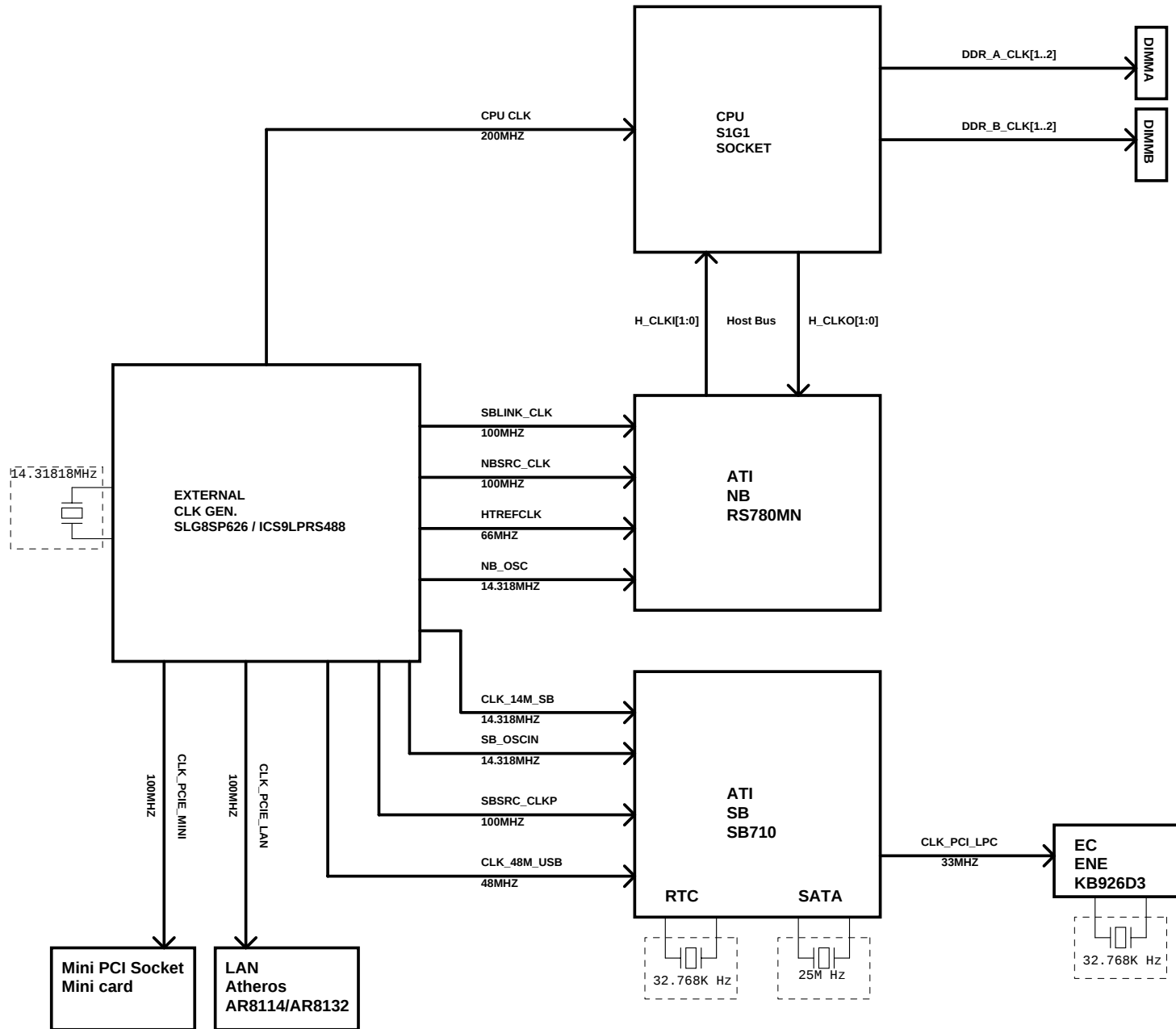
Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	No Support VaryBright
1	
2	
3	Support VaryBright
4	
5	
6	
7	

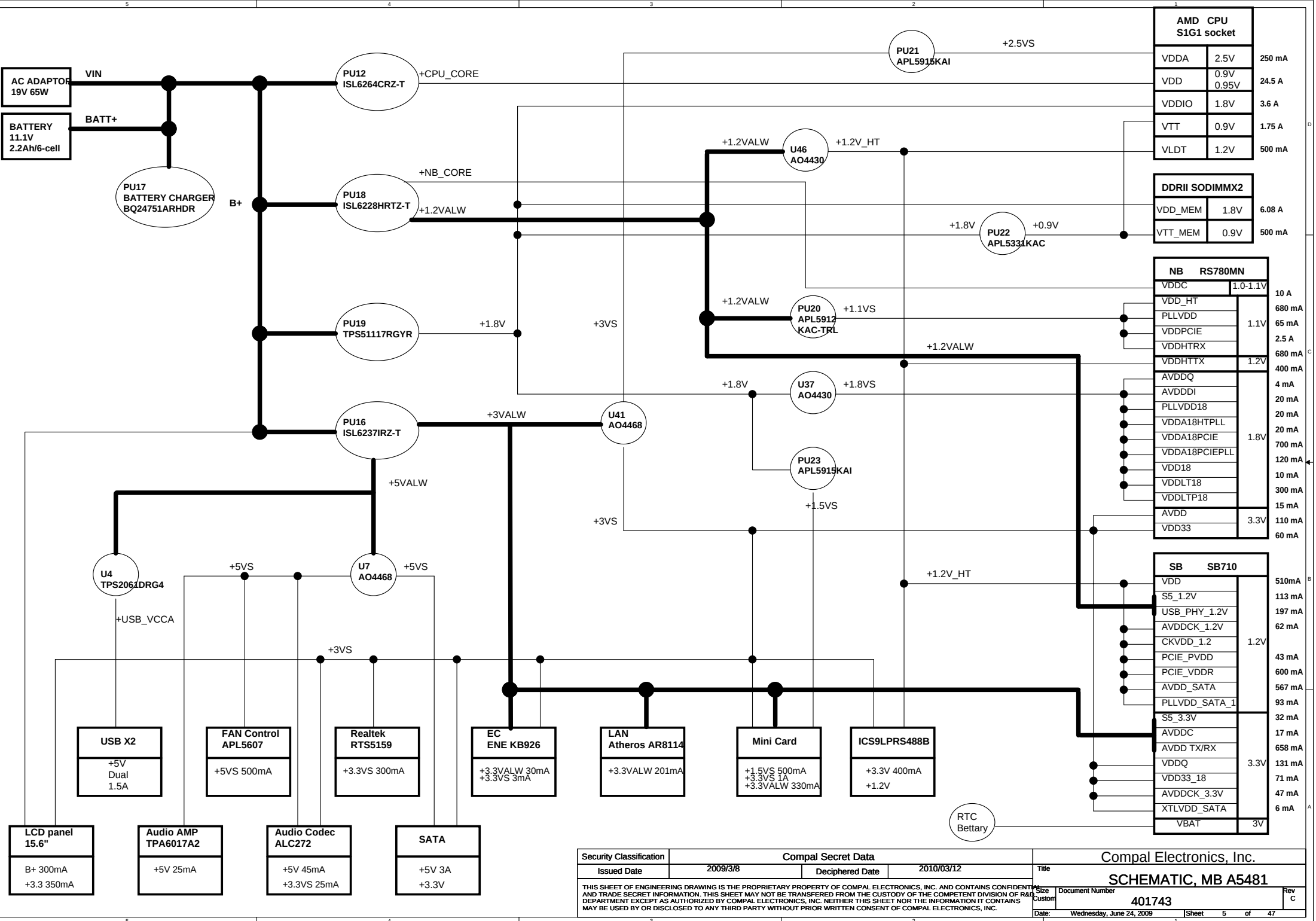
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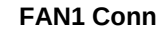
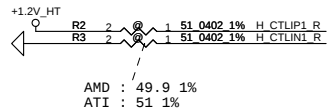
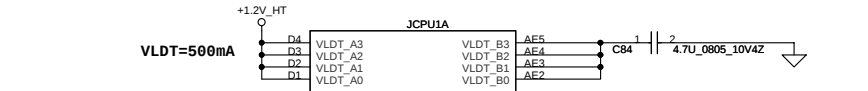
SKU ID	SKU
0	NCWG0
1	
2	
3	NAL00
4	
5	
6	
7	NCWH0

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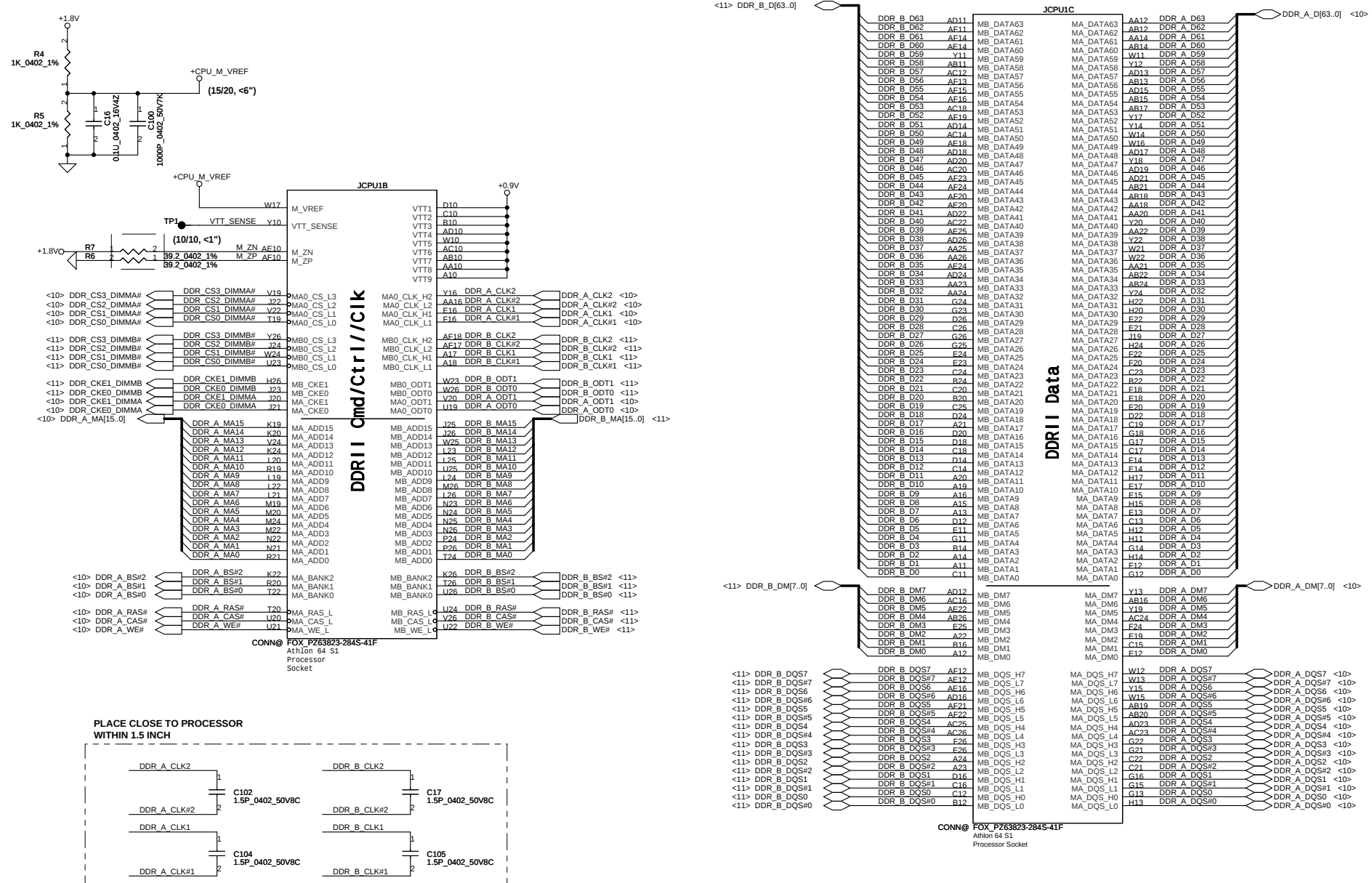
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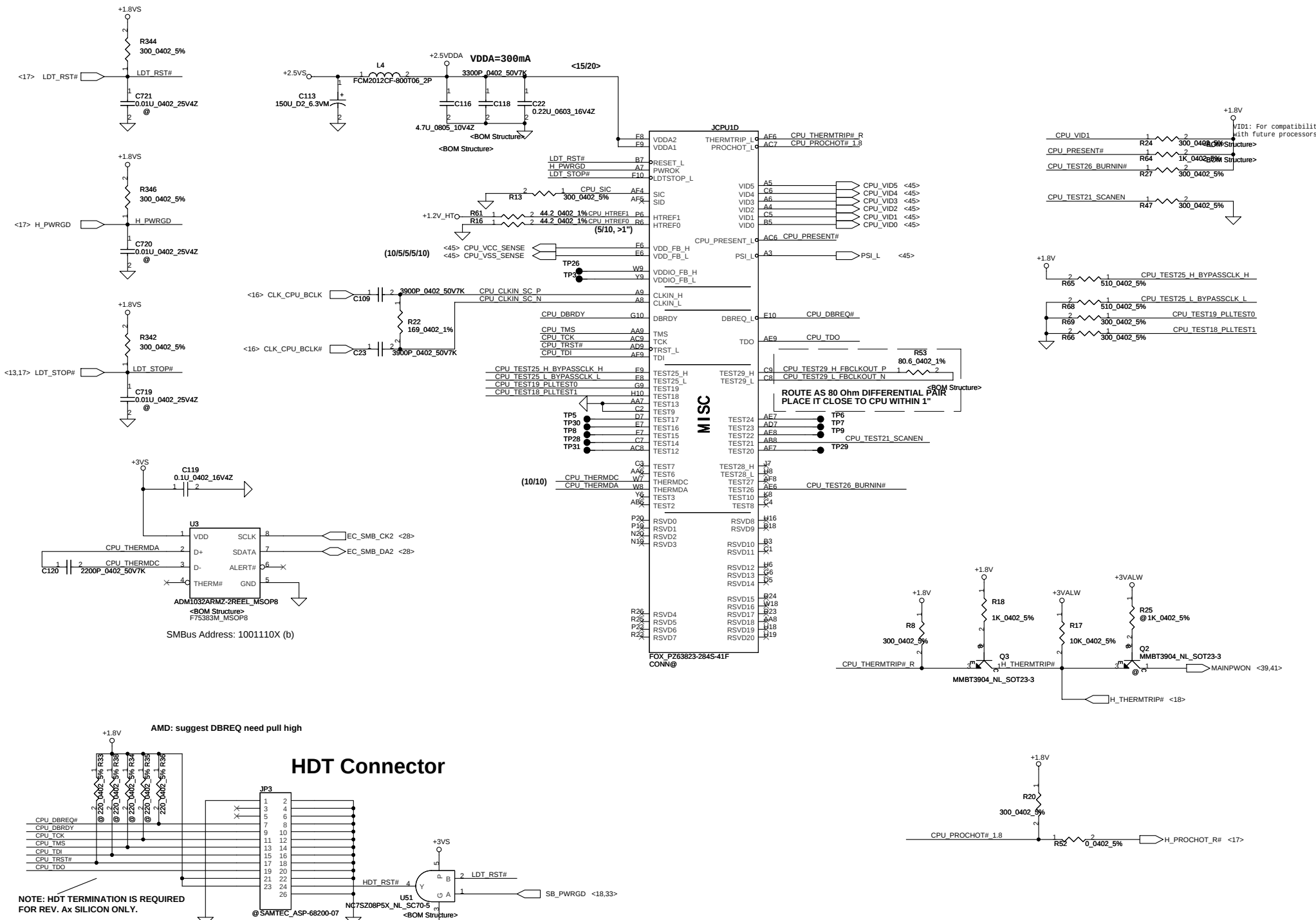
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Processor DDR2 Memory Interface

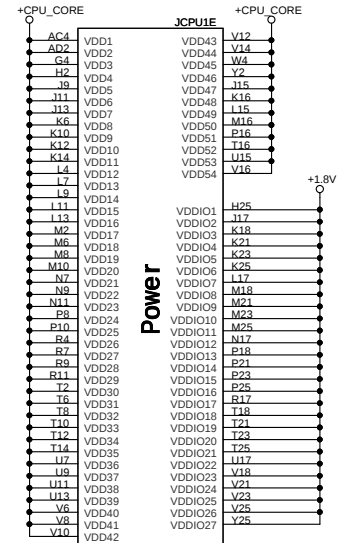




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VDD(+CPU_CORE) decoupling.

The image displays two PCB layout diagrams for VDD(+CPU_CORE) decoupling. The top diagram, labeled 'Near CPU Socket', shows a series of capacitors (C26, C32, C27, C28, C29) connected to the +CPU_CORE supply line. The bottom diagram, labeled 'Under CPU Socket', shows capacitors (C33, C36, C34, C35, C178, C41, C190, C39, C128) connected to the +CPU_CORE supply line, and three additional capacitors (C129, C151, C122, C47) connected to the +CPU_CORE supply line. The diagrams illustrate the placement of decoupling capacitors to ensure stable power delivery to the CPU core.



JCPU1F			
A4A	V5S1	V5S6	J6
A4A1	V5S2	V5S67	J8
A4A15	V5S3	V5S68	J10
A4A2	V5S4	V5S70	J12
A4A17	V5S5	V5S70	J14
A4A18	V5S6	V5S71	J16
AB7	V5S7	V5S72	J18
AB9	V5S8	V5S73	K2
AB23	V5S9	V5S74	K7
AB25	V5S10	V5S75	K9
AC11	V5S12	V5S76	K13
AC13	V5S13	V5S78	K15
AC15	V5S14	V5S79	K17
AC19	V5S15	V5S80	L6
AC21	V5S16	V5S81	L8
AD6	V5S18	V5S83	L10
AD25	V5S19	V5S84	L12
AE11	V5S20	V5S84	L14
AE13	V5S21	V5S86	L16
AE17	V5S22	V5S87	L18
AE19	V5S23	V5S88	M7
AE21	V5S24	V5S90	M9
B4	V5S26	V5S91	M11
B6	V5S27	V5S92	M17
B8	V5S28	V5S92	N3
B9	V5S29	V5S94	N8
B11	V5S30	V5S95	N10
B13	V5S31	V5S96	N16
B15	V5S32	V5S97	N18
B19	V5S33	V5S98	P2
B21	V5S34	V5S99	P7
B23	V5S35	V5S100	P9
B25	V5S36	V5S101	P11
D3	V5S37	V5S102	P17
D6	V5S38	V5S103	R8
D9	V5S39	V5S104	R10
D13	V5S40	V5S105	R16
D15	V5S41	V5S106	R18
D17	V5S42	V5S107	T7
D19	V5S43	V5S108	T11
D13	V5S44	V5S108	T13
D15	V5S45	V5S109	T15
D17	V5S46	V5S110	T17
D21	V5S47	V5S111	U4
D23	V5S48	V5S112	U6
D25	V5S49	V5S113	U8
E2	V5S50	V5S114	U10
F11	V5S51	V5S115	U12
F13	V5S52	V5S116	U14
F15	V5S53	V5S118	U16
F17	V5S54	V5S119	U18
F19	V5S55	V5S120	V2
F23	V5S56	V5S121	V7
F25	V5S57	V5S122	V9
H7	V5S58	V5S123	V11
H9	V5S59	V5S124	V13
H11	V5S60	V5S125	V15
H13	V5S61	V5S126	V17
H21	V5S62	V5S127	W6
H23	V5S63	V5S128	Y21
J4	V5S65	V5S129	Y23
			N6

VTT decoupling.

Near Power Supply

C: Change to NBO CAP

150U_D2_6.3VM

0.9V

C66

1

2

0.9V

C155

4.7U_0805_10V4Z

1

2

<BOM Structure>

<BOM Structure>

<BOM Structure>

<BOM Structure>

<BOM Structure>

<BOM Structure>

<BOM Structure>

0.9V

C146

4.7U_0805_10V4Z

1

2

C184

0.22U_0603_16V4Z

1

2

C173

0.22U_0603_16V4Z

1

2

C72

1000P_0402_50V7K

1

2

C145

1000P_0402_50V7K

1

2

C180

180P_0402_50V8J

1

2

C121

180P_0402_50V8J

1

2

<BOM Structure>

Near CPU Socket Right side.

0.9V

C73

4.7U_0805_10V4Z

1

2

<BOM Structure>

<BOM Structure>

<BOM Structure>

<BOM Structure>

0.9V

C70

4.7U_0805_10V4Z

1

2

C127

0.22U_0603_16V4Z

1

2

C185

0.22U_0603_16V4Z

1

2

C164

1000P_0402_50V7K

1

2

C163

1000P_0402_50V7K

1

2

C152

180P_0402_50V8J

1

2

C179

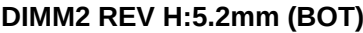
180P_0402_50V8J

1

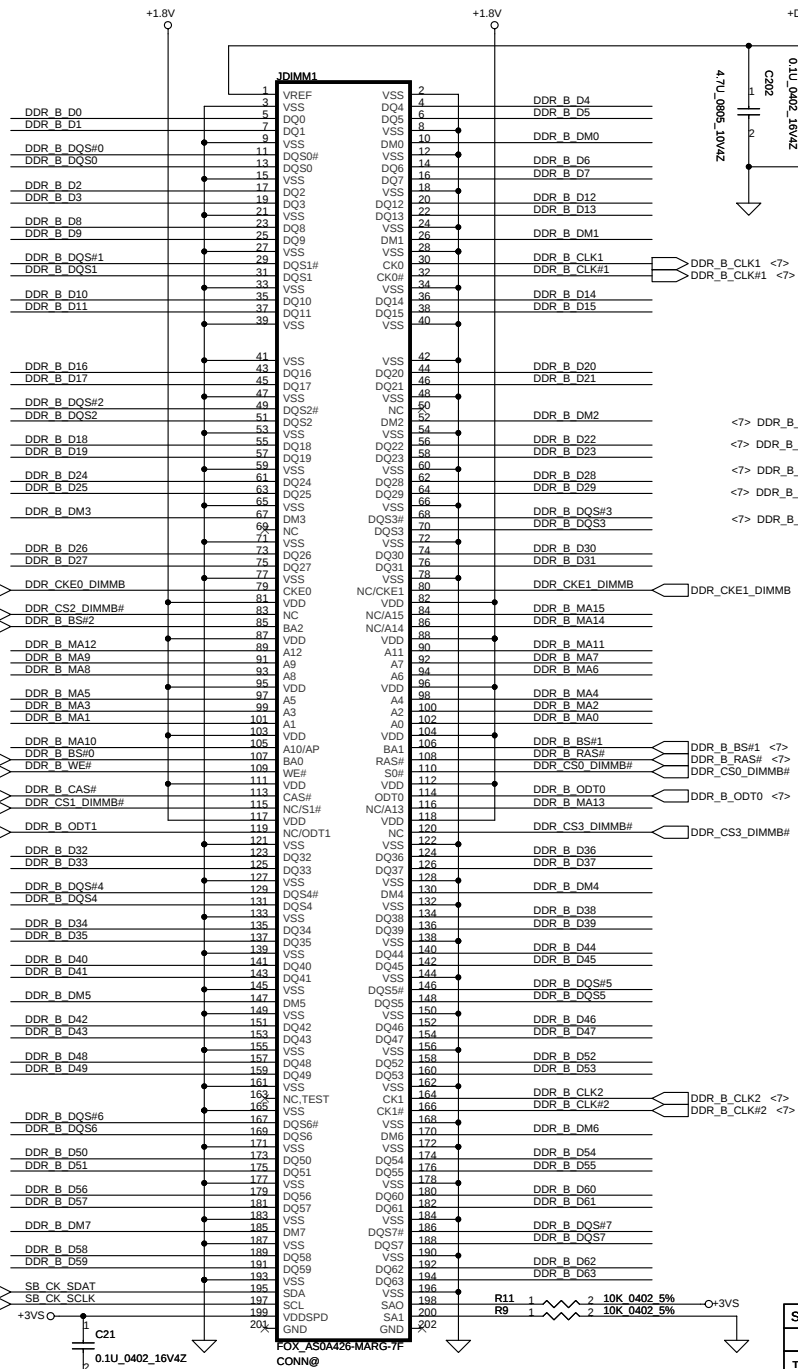
2

Near CPU Socket Left side.

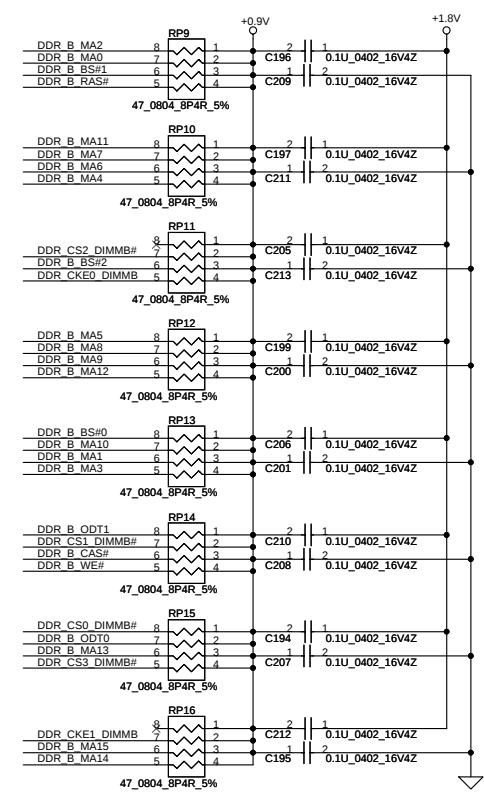
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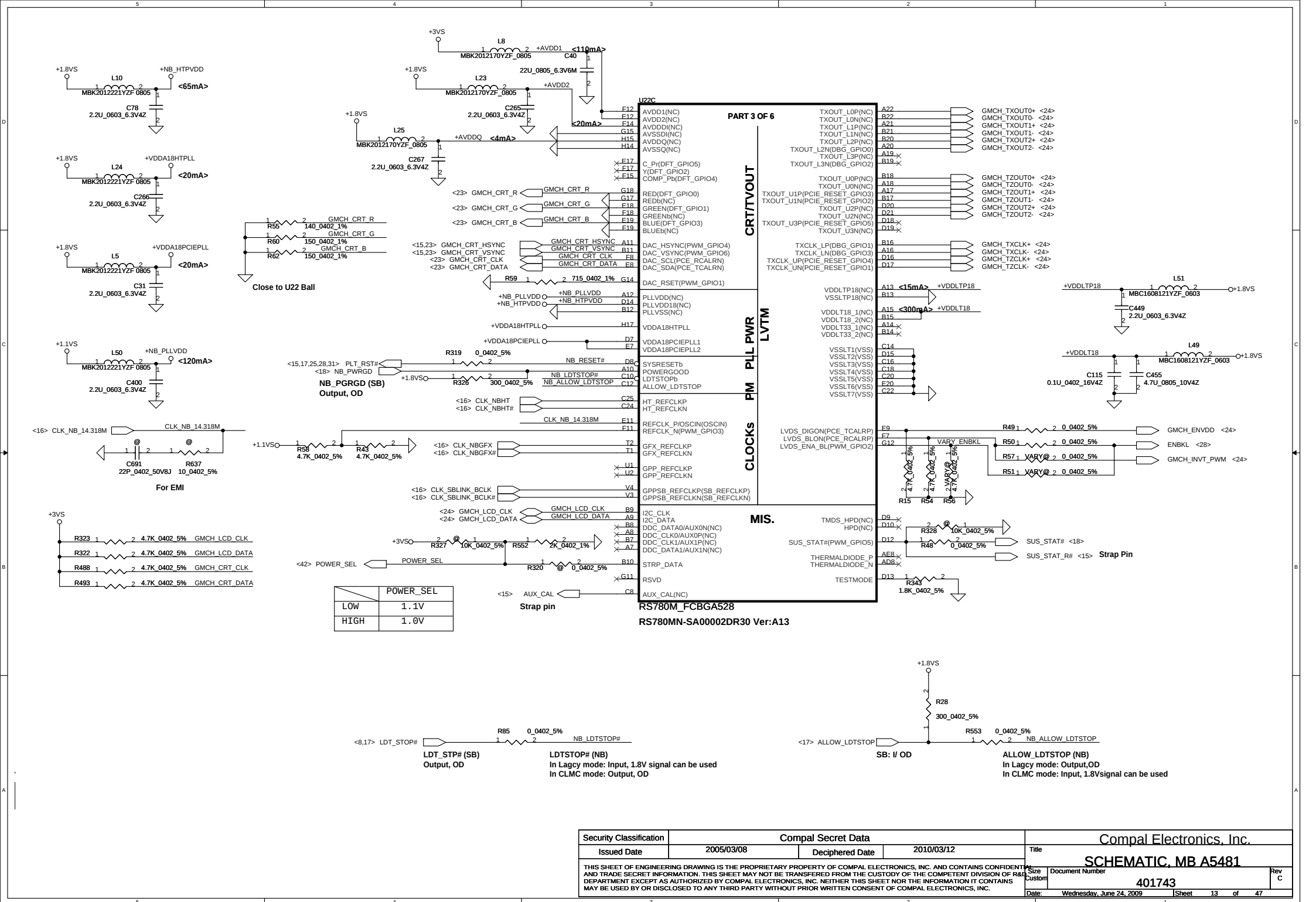
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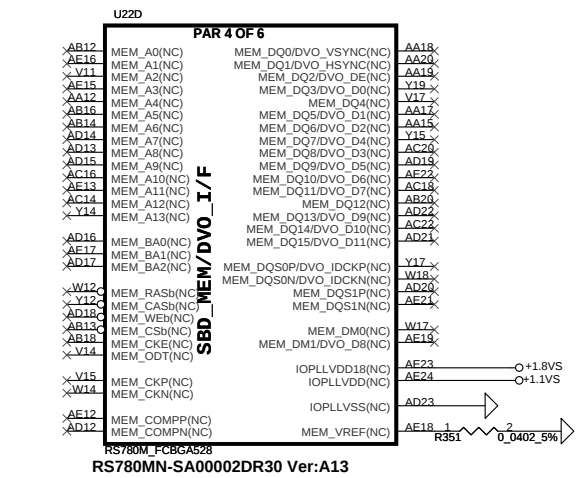
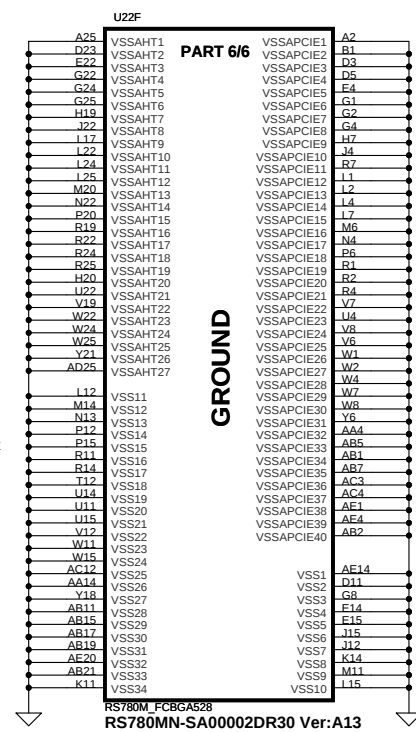
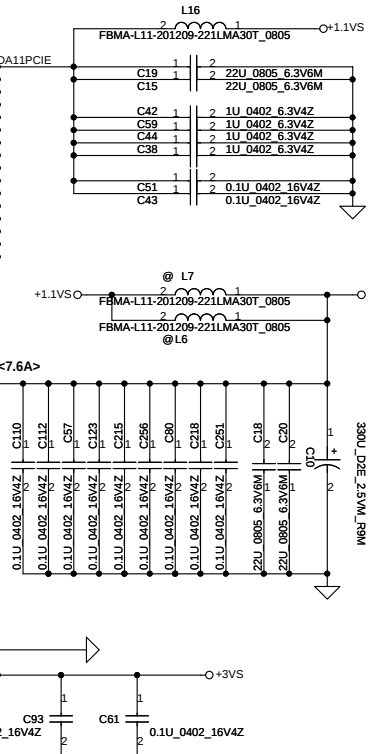
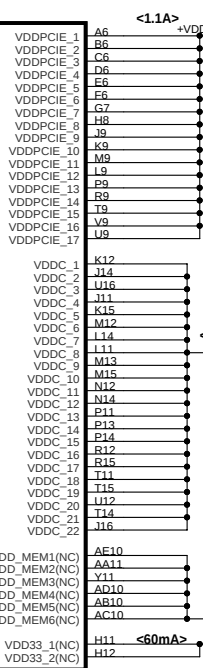
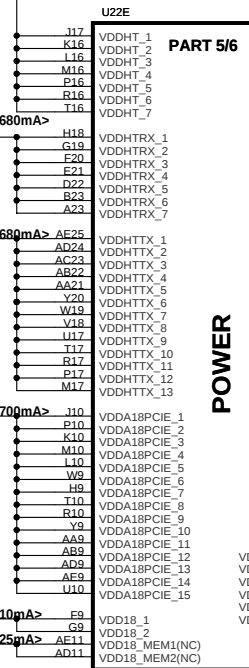
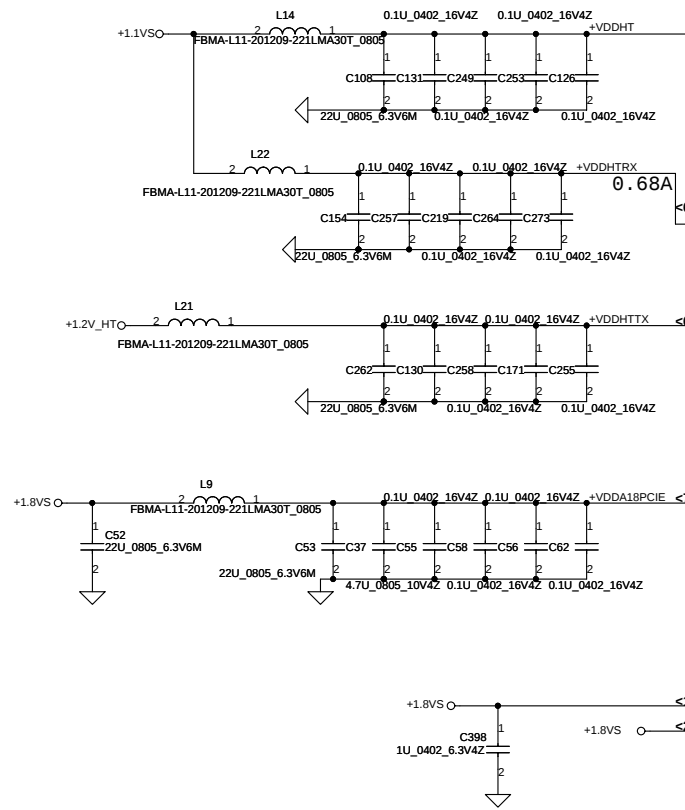
DIMM1 REV H:9.2mm (BOT)



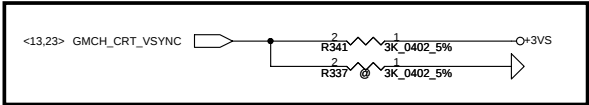
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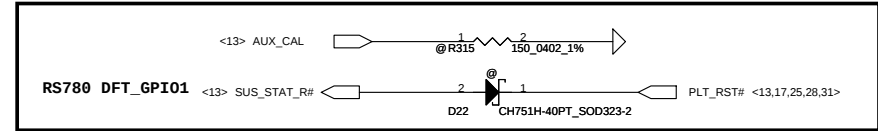


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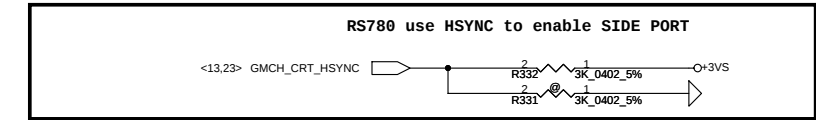
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)



DFT_GPIO1: LOAD_EEPROM_STRAPS

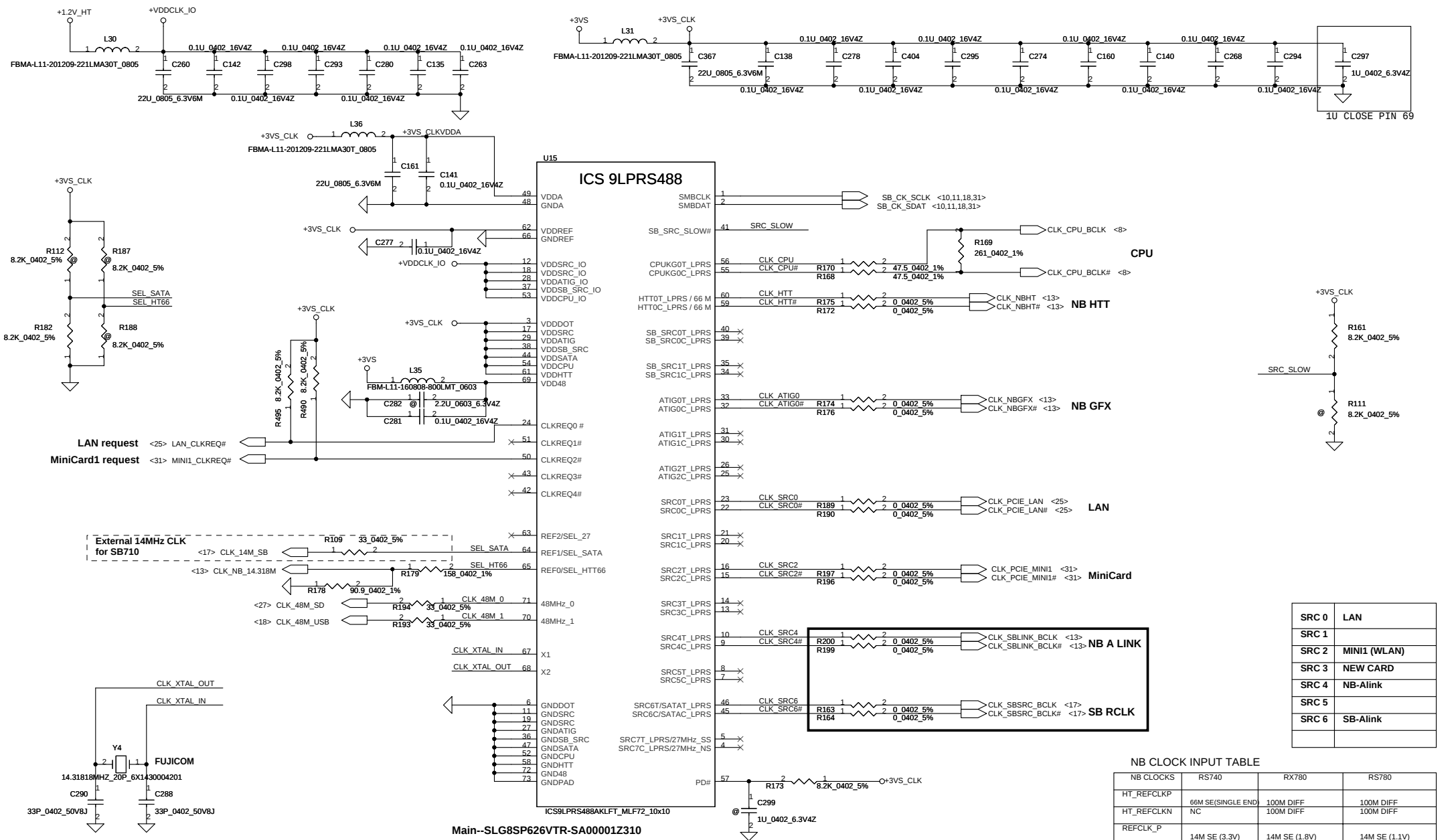
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
0. Enable (RS780)
1 : Disable(RS780)

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SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	SS 100M SATA SRC6 output
	0	SS 100M SATA SRC6 output

* default

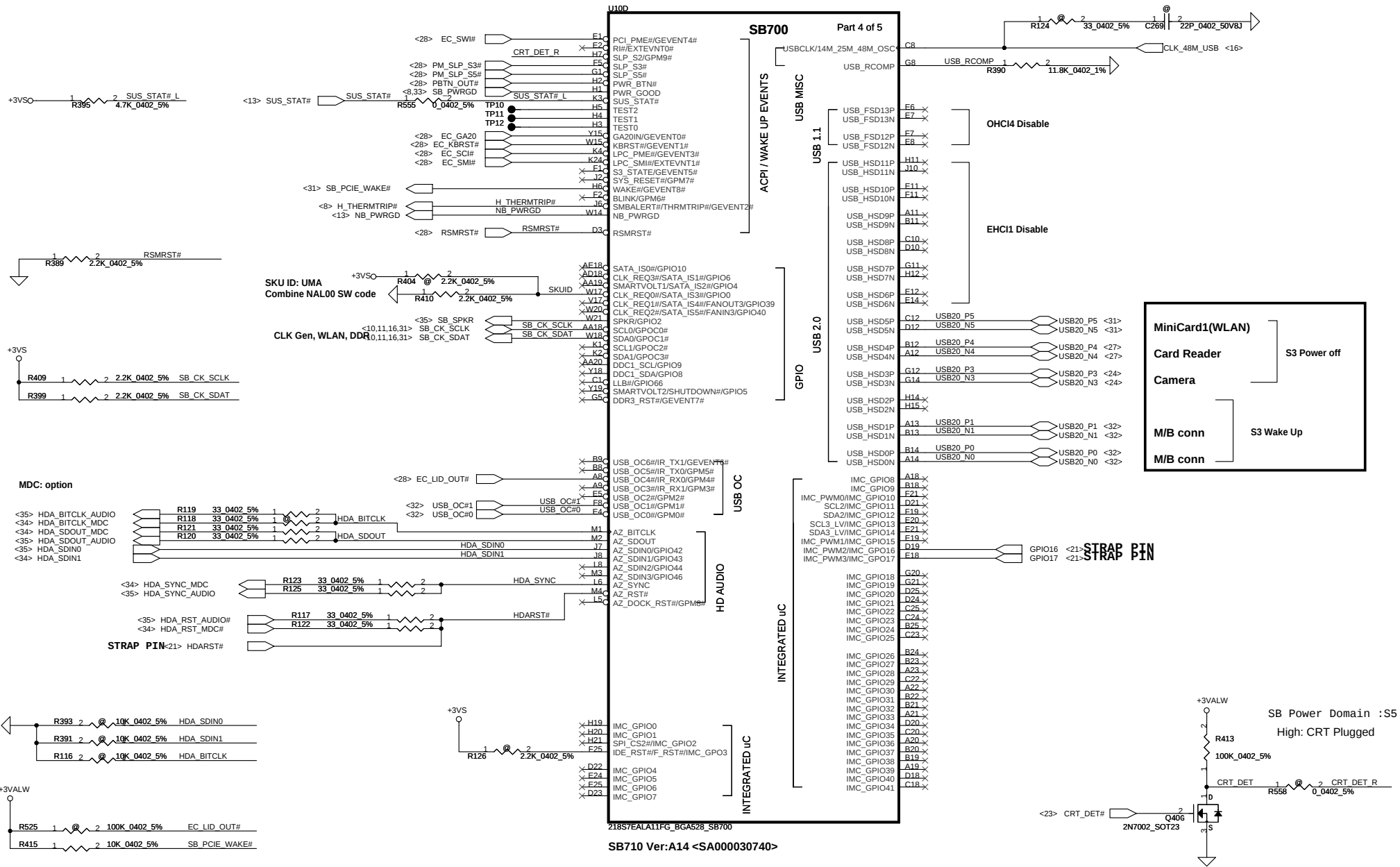
SEL_27M No used	1	configure as 27M and 27M_SS output
	0	configure as SRC_7 output

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SRC 0	LAN
SRC 1	
SRC 2	MINI1 (WLAN)
SRC 3	NEW CARD
SRC 4	NB-Alink
SRC 5	
SRC 6	SB-Alink

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF

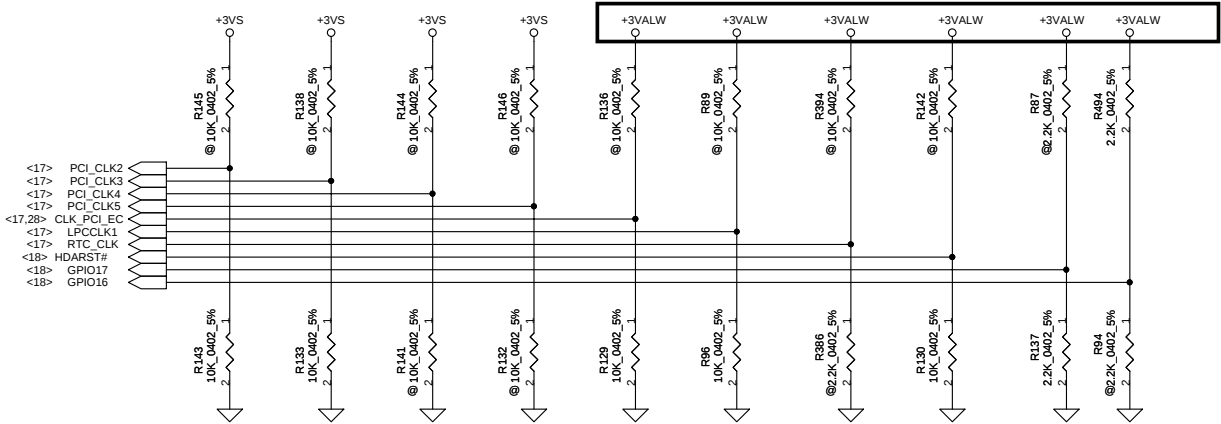


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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default L,NC) L,L = FWH ROM

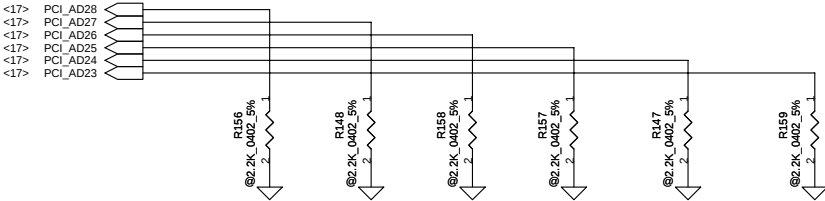


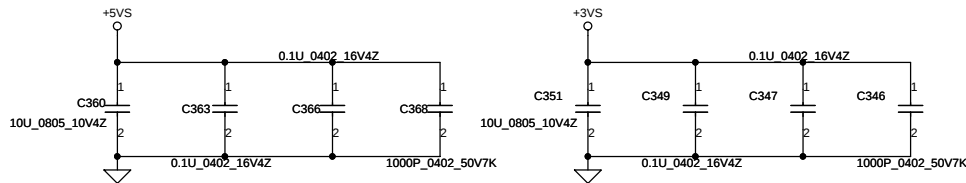
DEBUG STRAPS

DEBUG STRAPS

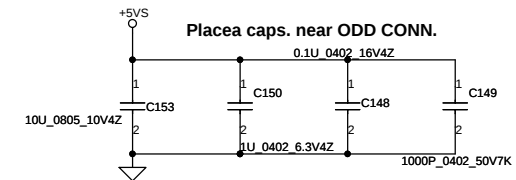
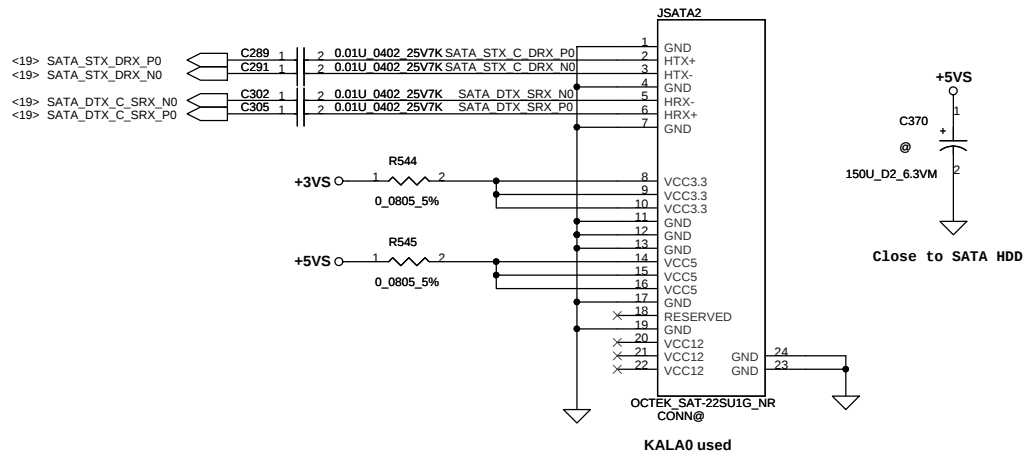
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

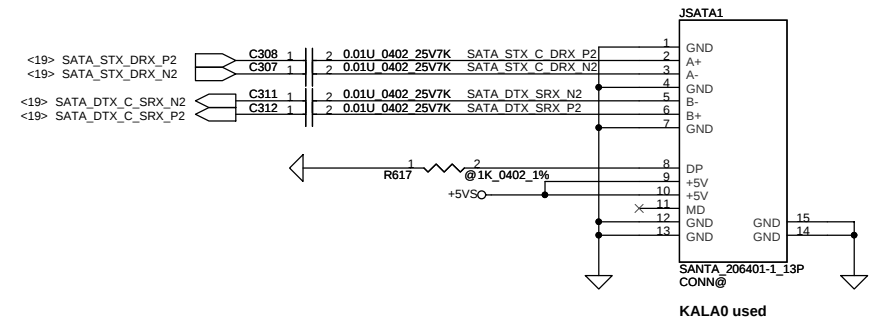




SATA HDD CONN

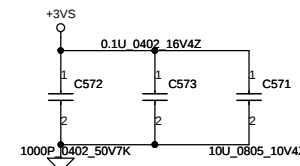
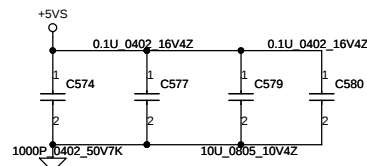
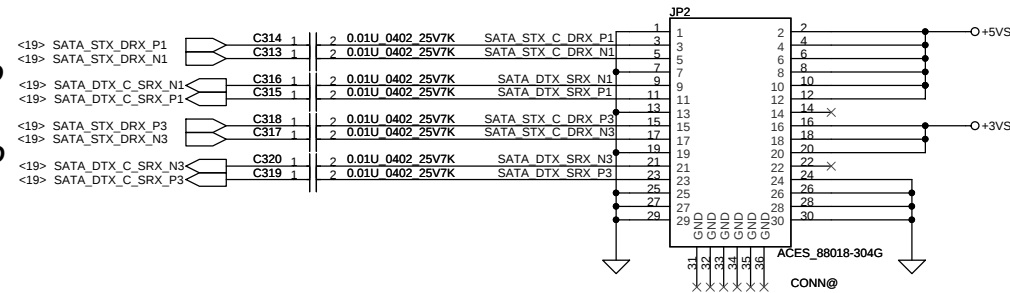


SATA ODD CONN



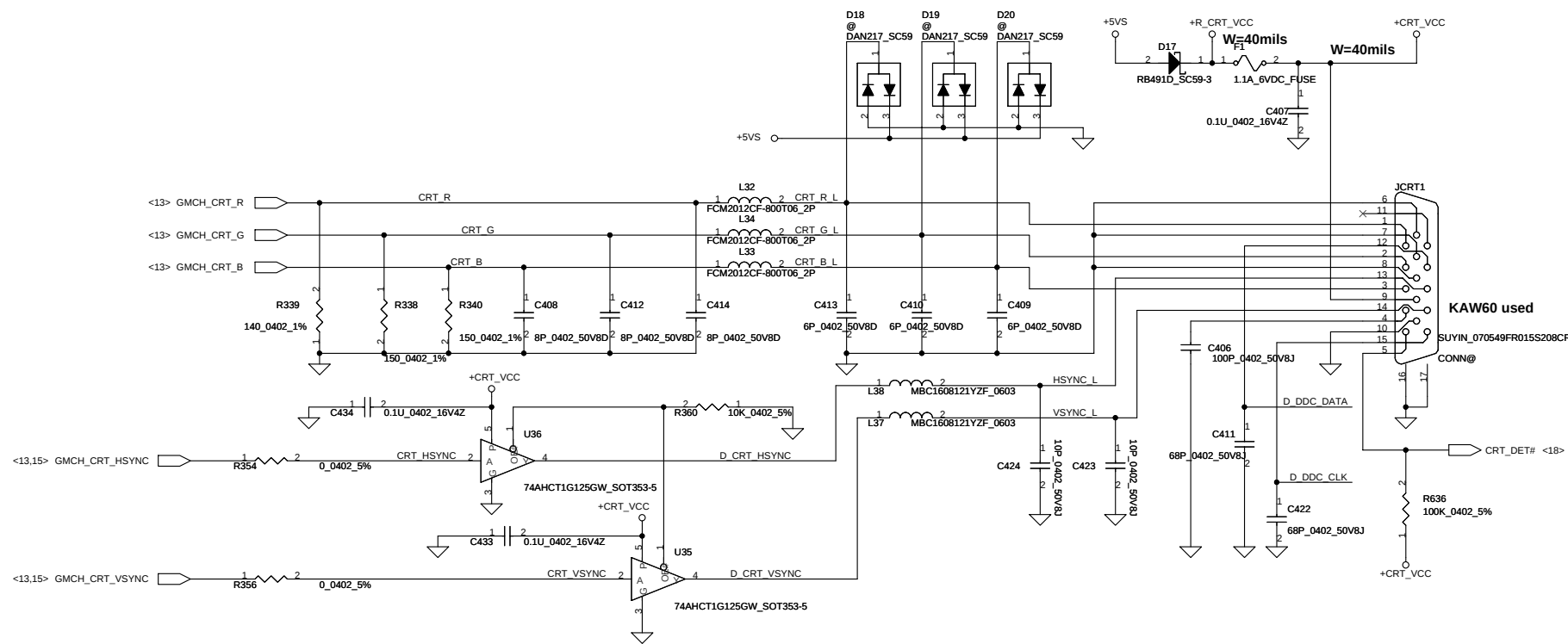
Second HDD

Second ODD

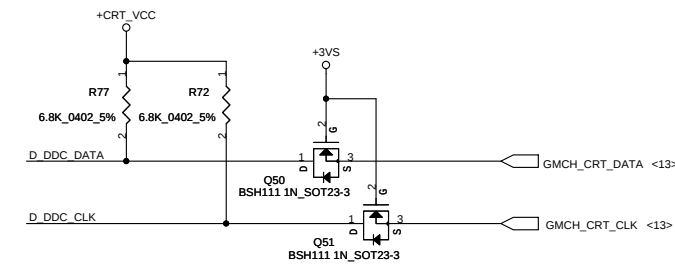


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CRT Connector



Close to Conn side



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LCD POWER CIRCUIT

LCD/PANEL CONN.

VARYBRIGHT FUNCTION

Security Classification

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Deciphered Date	2010/03/12

Title

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Size

Custom

Document Number

401743

Date

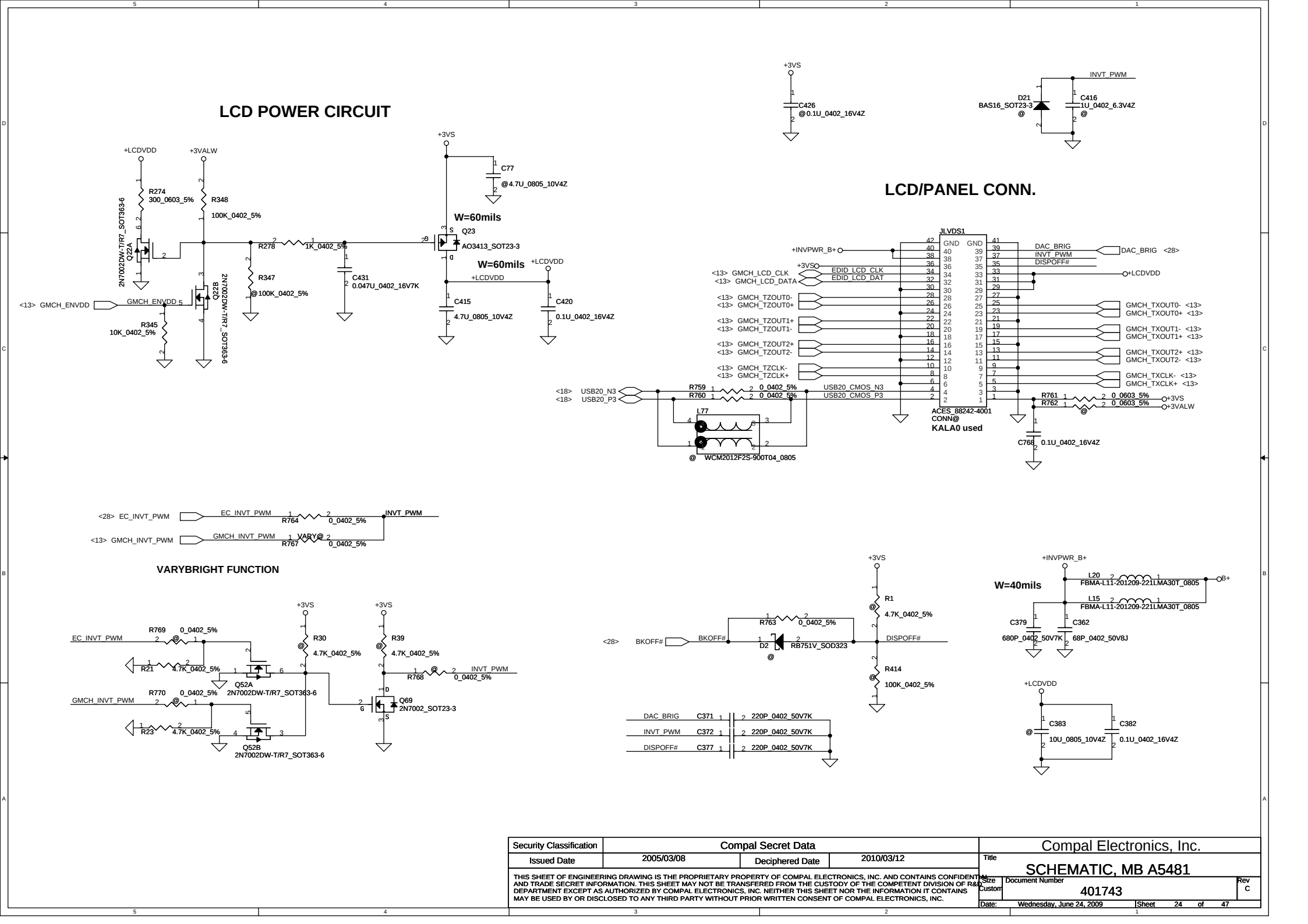
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Rev

C



LCD POWER CIRCUIT

LCD/PANEL CONN.

VARYBRIGHT FUNCTION

USB20 CMOS

Signal	Pin	Value
DAC_BRIG	C371	220P 0402 50V7K
INVT_PWM	C372	220P 0402 50V7K
DISPOFF#	C377	220P 0402 50V7K

Signal	Pin	Value
USB20_N3	R759	0 0402 5%
USB20_P3	R760	0 0402 5%

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Issued Date: 2005/03/08

Deciphered Date: 2010/03/12

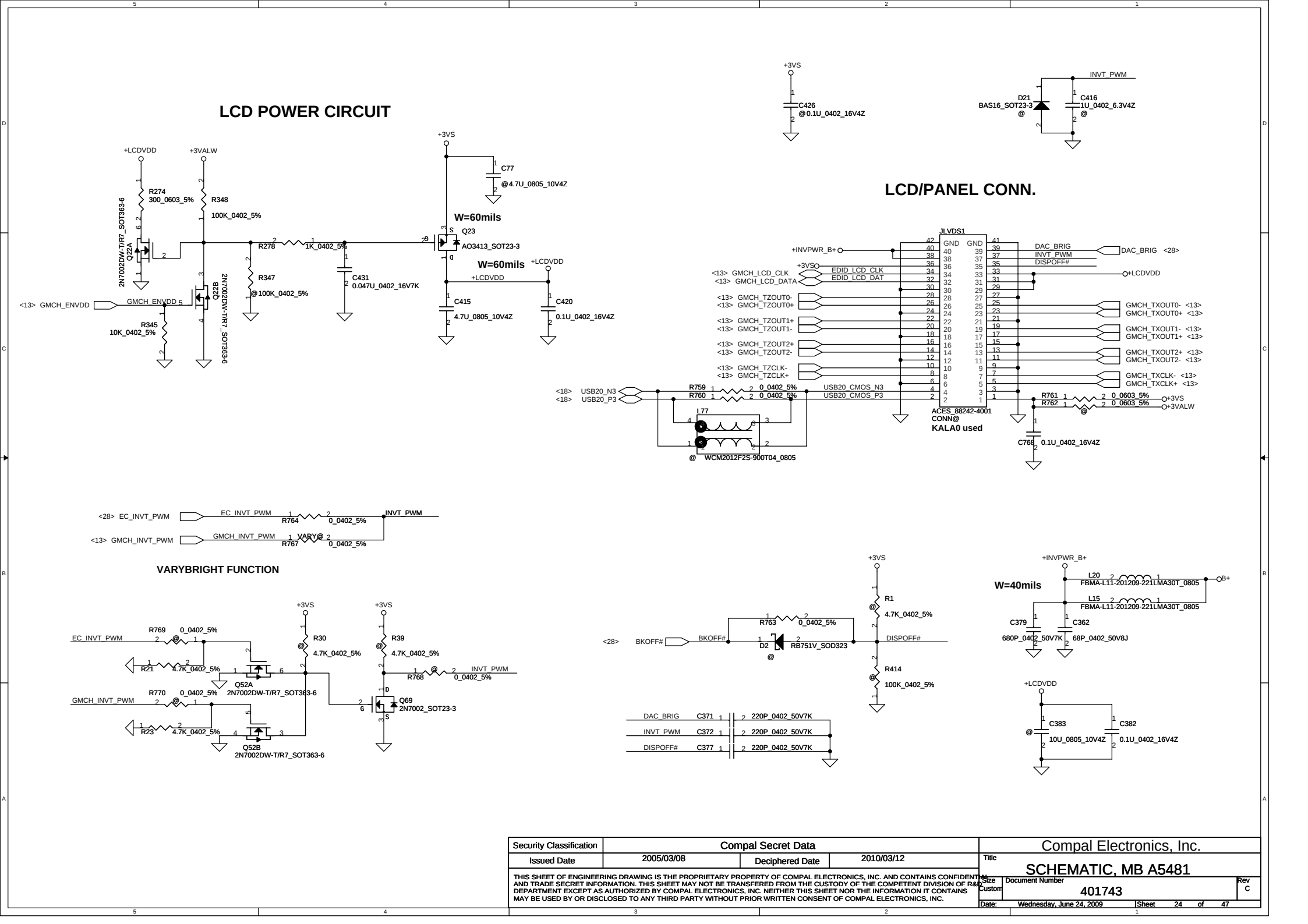
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LCD POWER CIRCUIT

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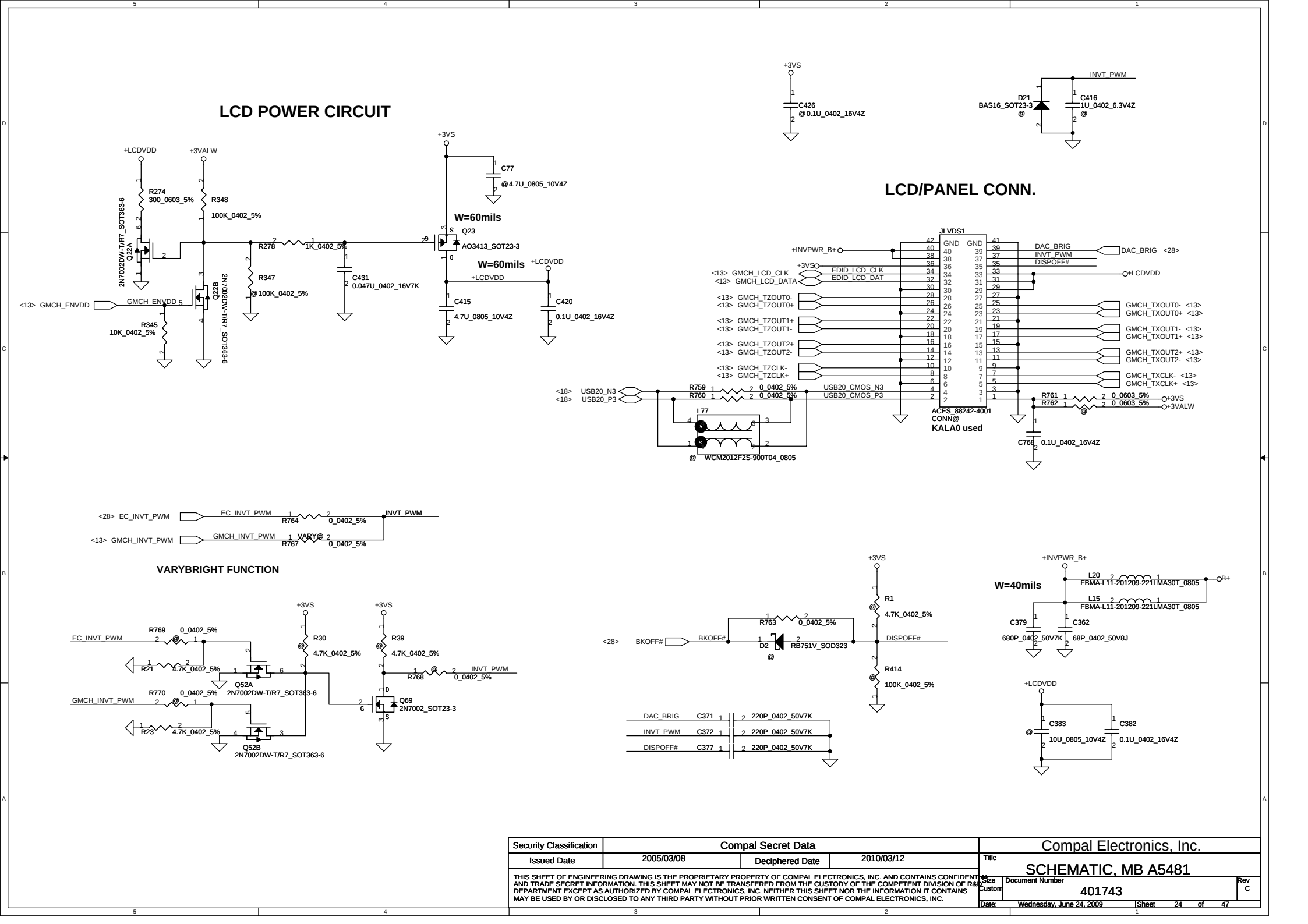
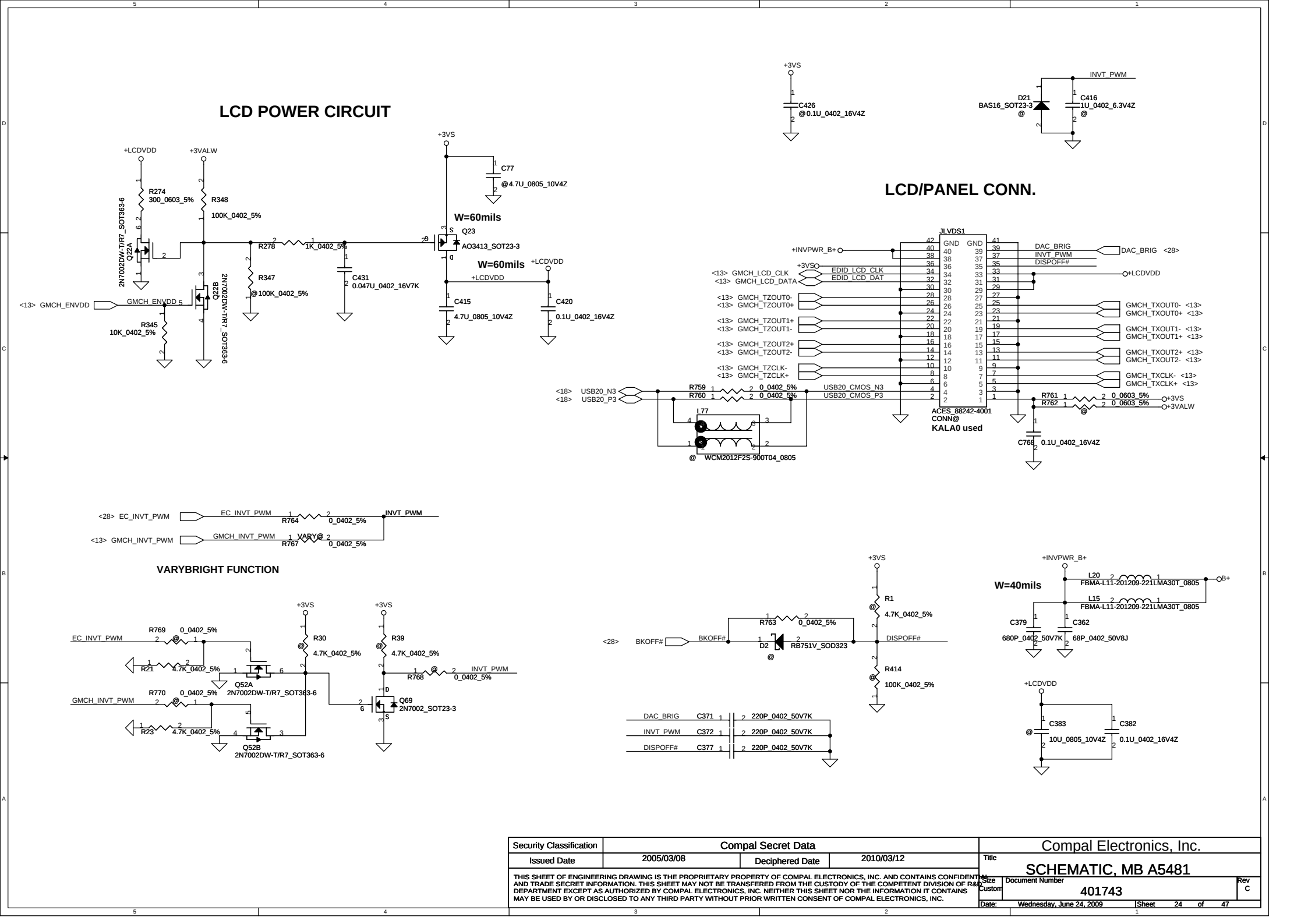
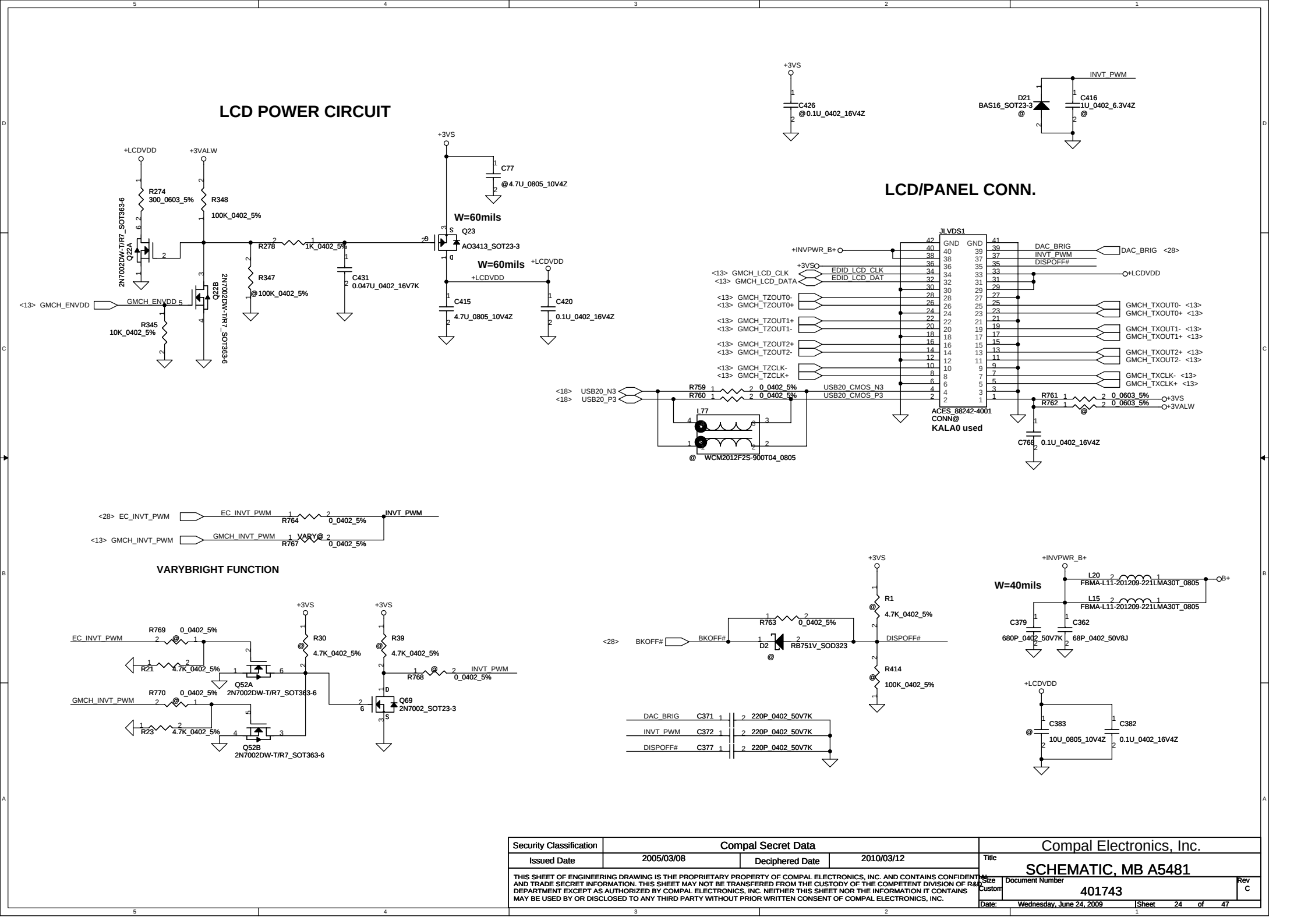
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Rev

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LCD POWER CIRCUIT

LCD/PANEL CONN.

VARYBRIGHT FUNCTION

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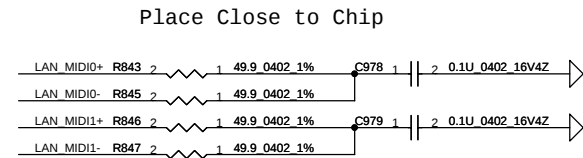
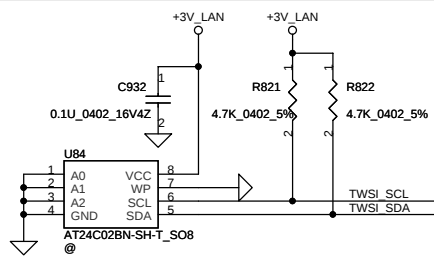
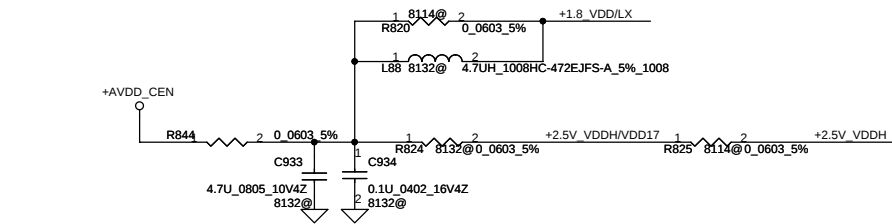
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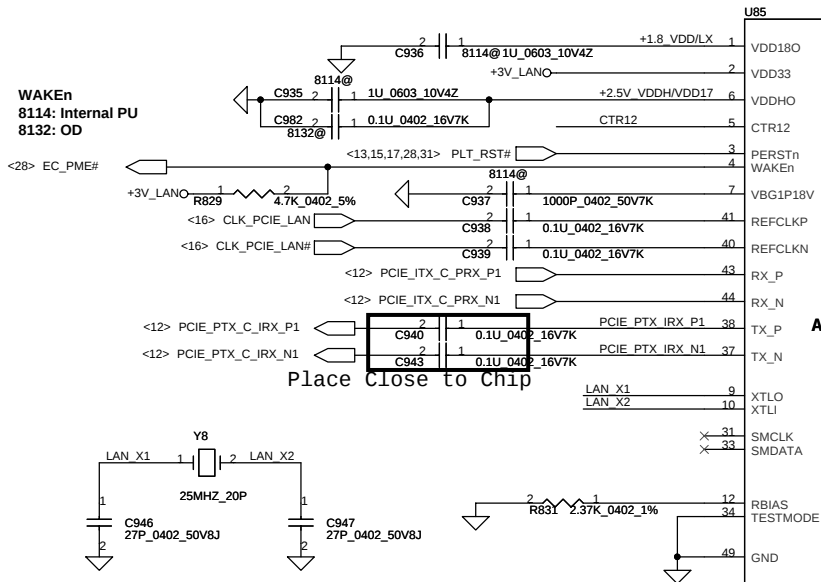
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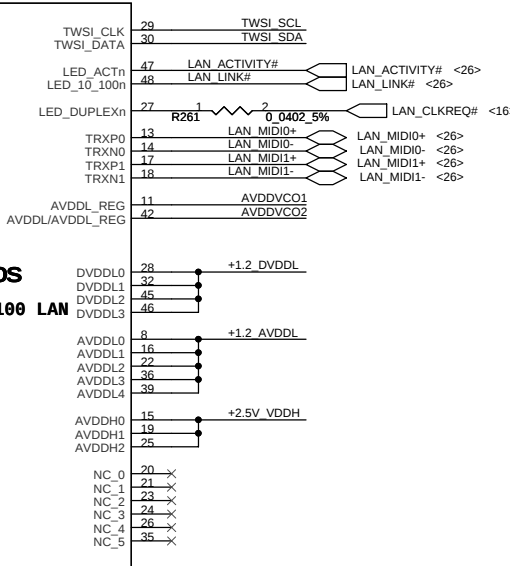
C



WAKEn
8114: Internal PU
8132: OD



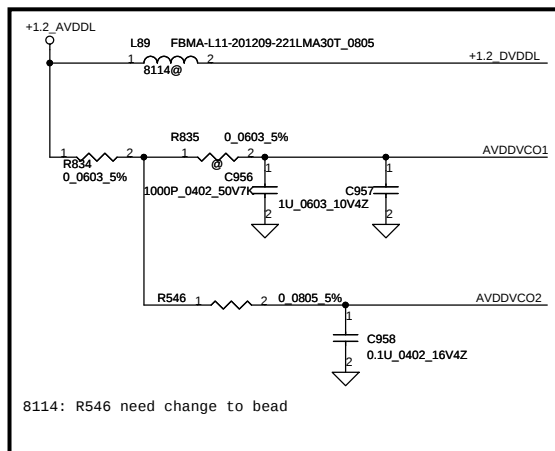
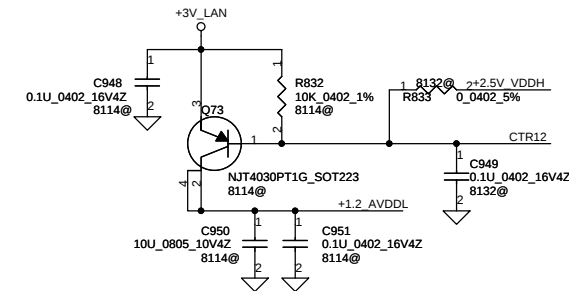
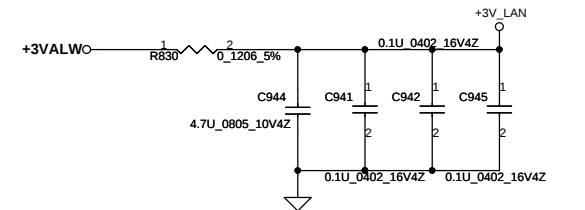
Atheros
AR8114A 10/100 LAN



change to AR8132L-AL1E

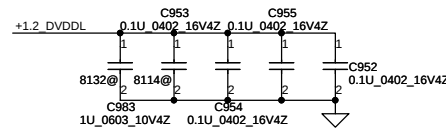
Place Close to Chip

Layout Notice : Close to chip

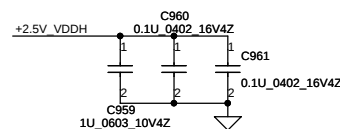


8114: R546 need change to bead

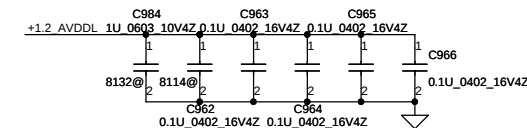
Place Close to Pin 28、32、45、46



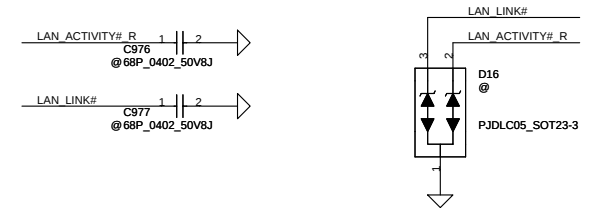
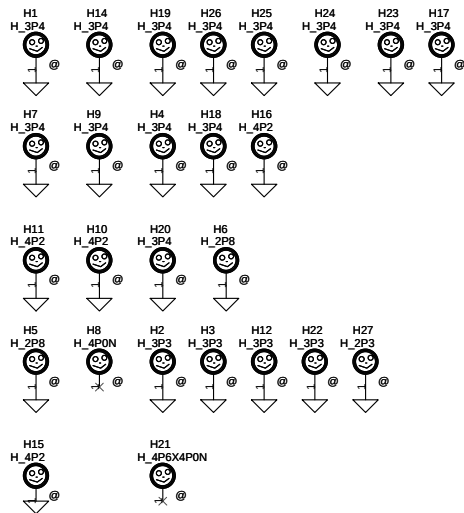
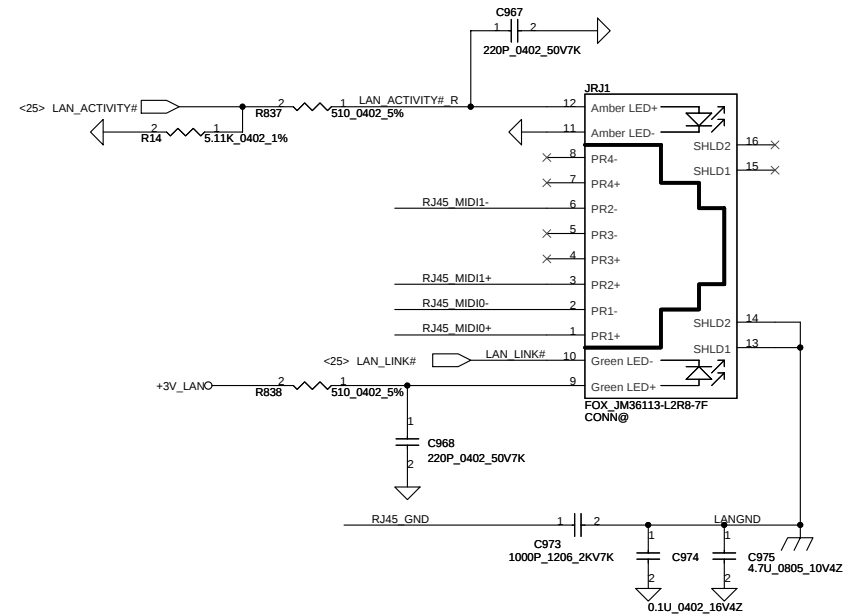
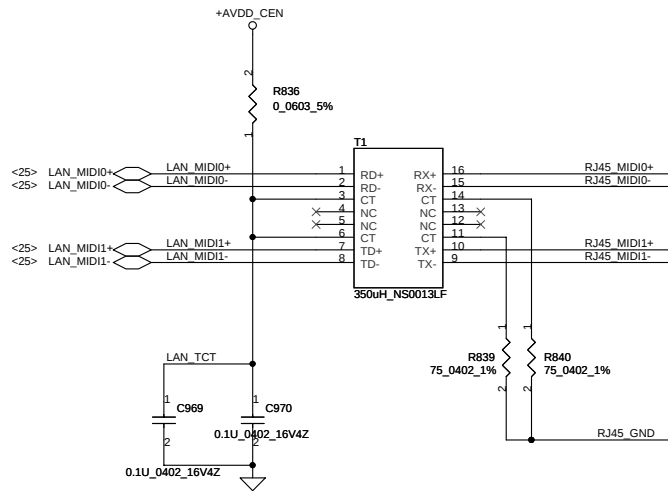
Place Close to Pin15、19、25



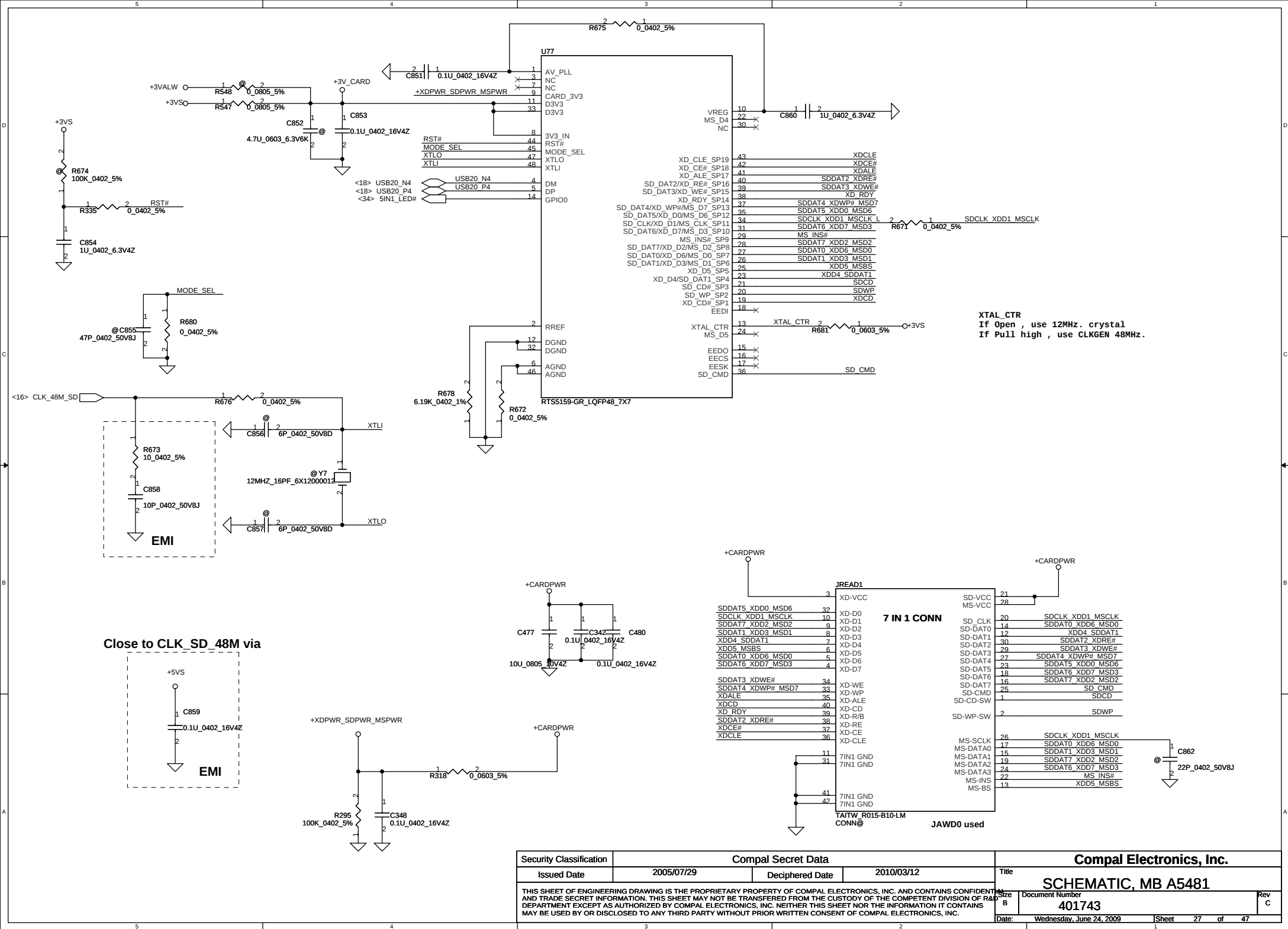
Place Close to Pin8、16、22、36、39



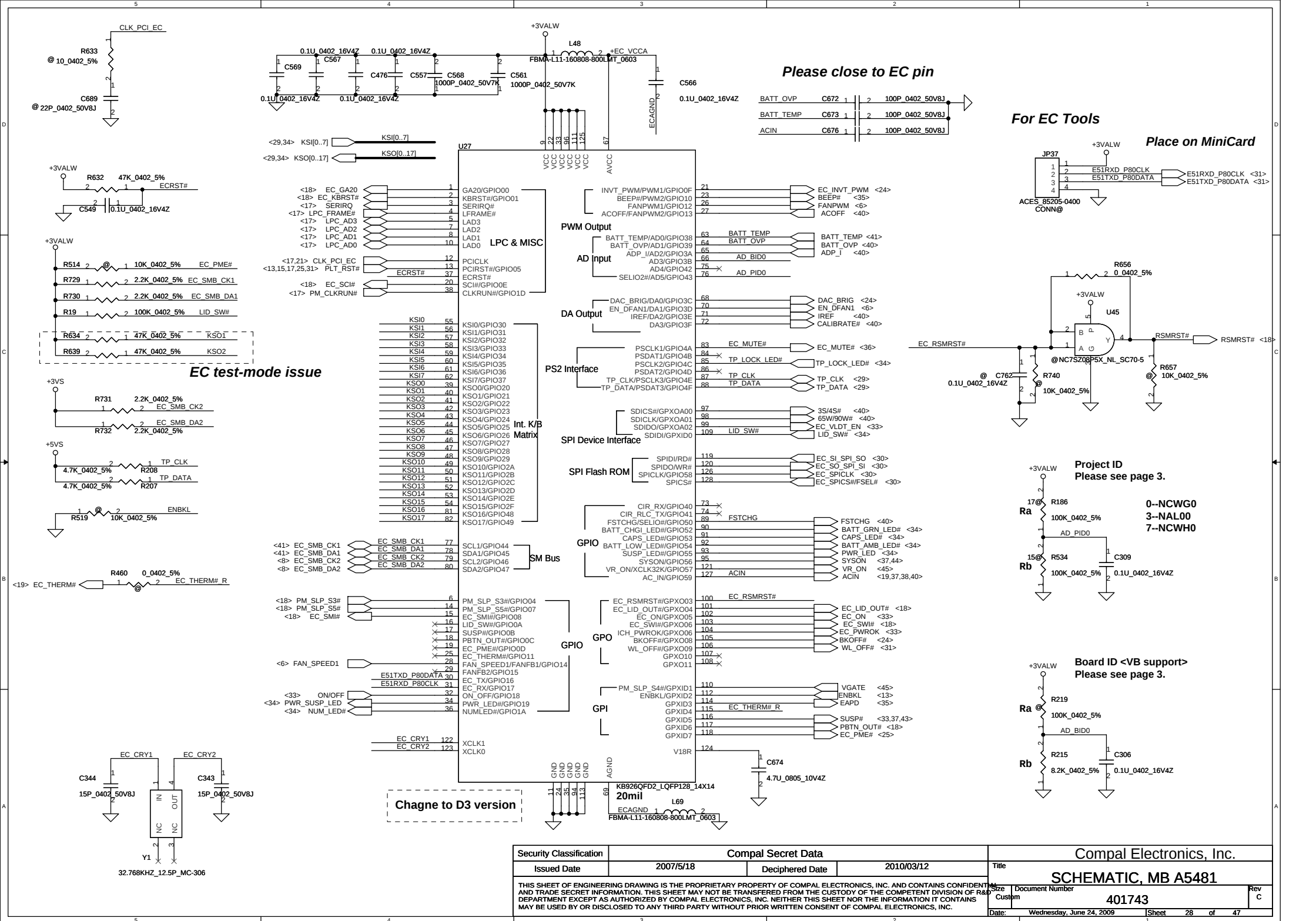
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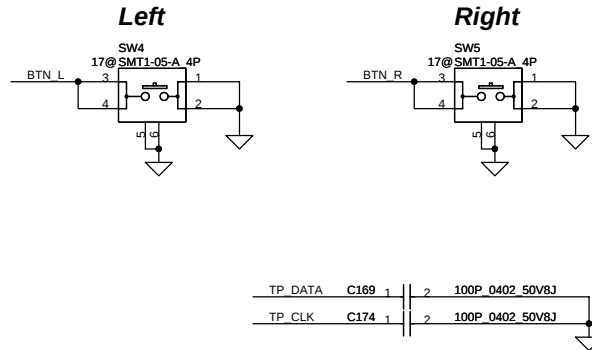
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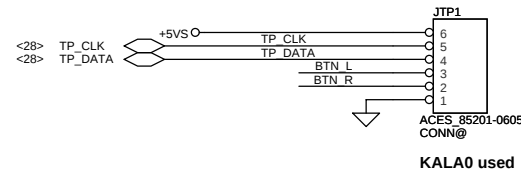
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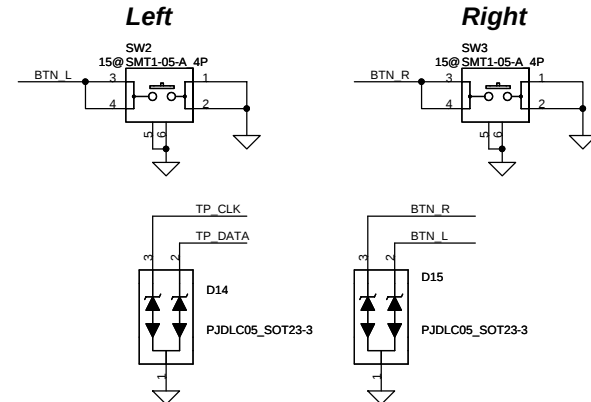
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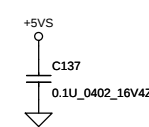
To TP/B Conn.



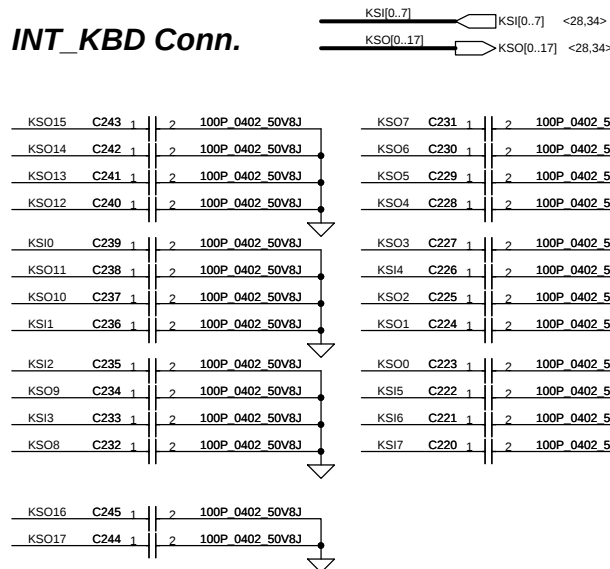
For 15"



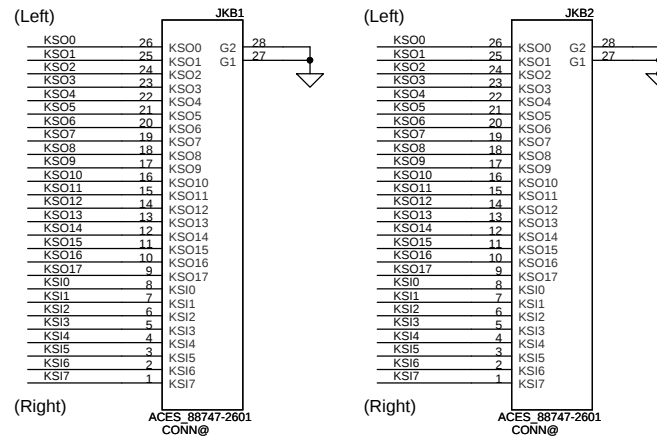
Change to SCA00000200



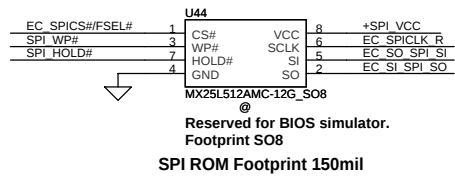
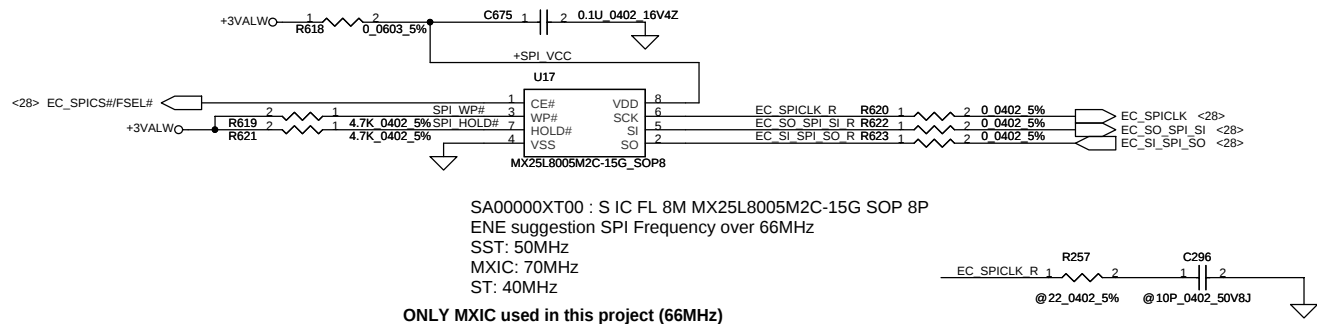
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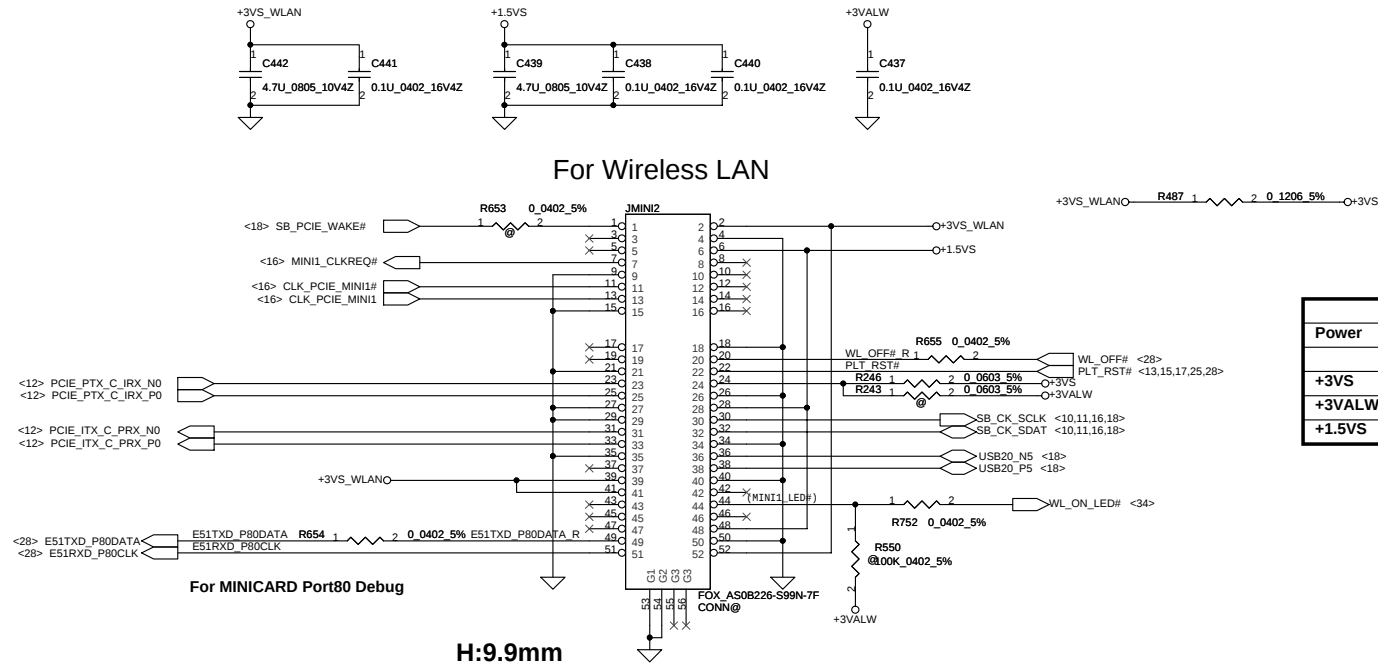
KB1 for 15"
KB2 for 17"



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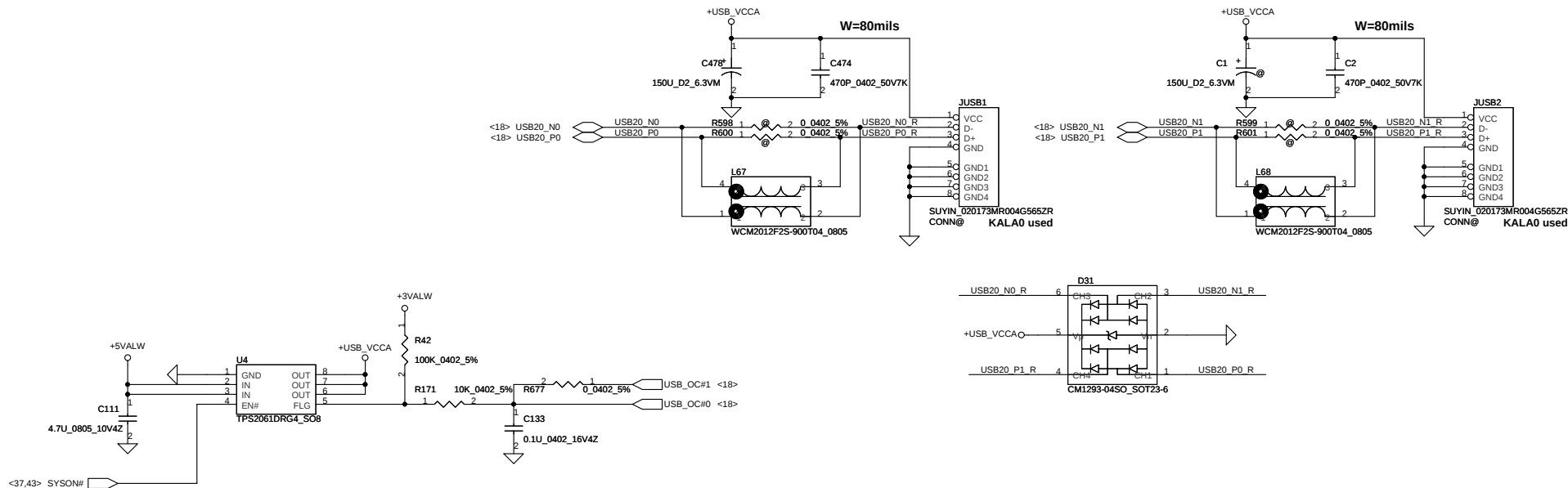
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Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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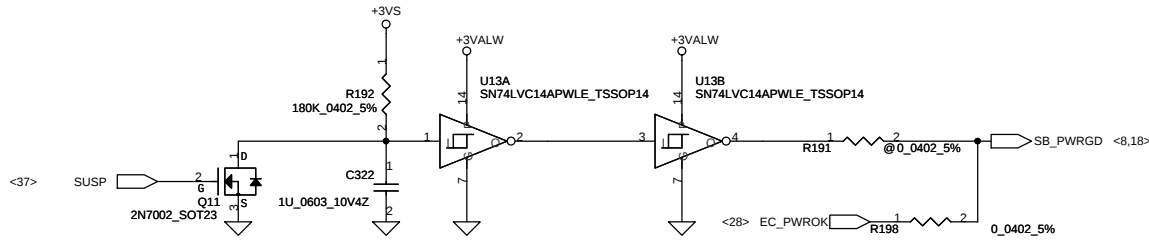
USB CONN. 1 & 2



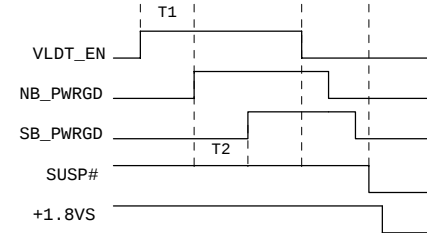
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Power ON Circuit

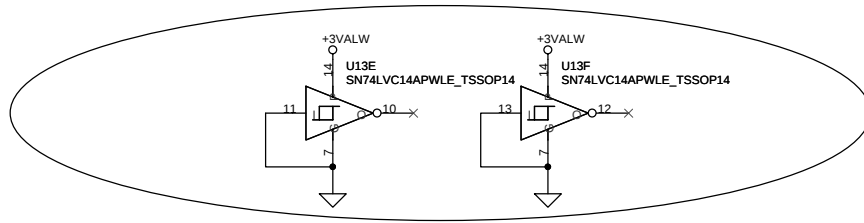
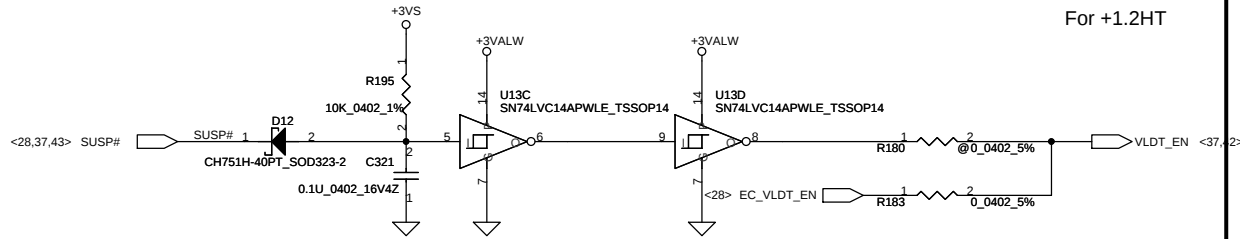
For South Bridge



note: T1 minimum 15ms, T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



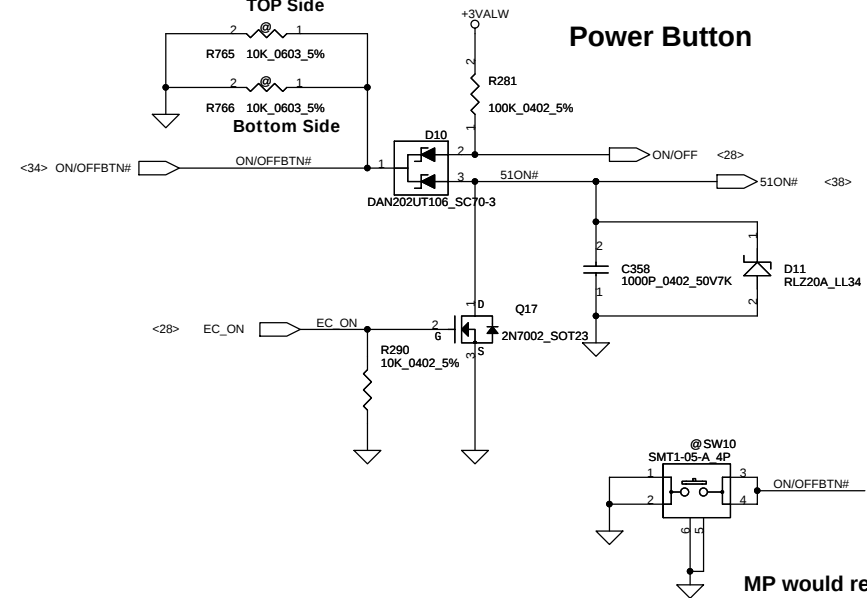
For +1.2HT



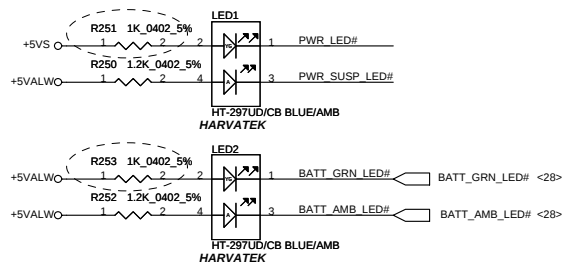
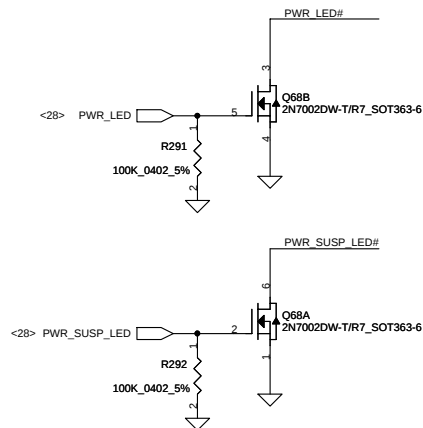
TOP Side

Bottom Side

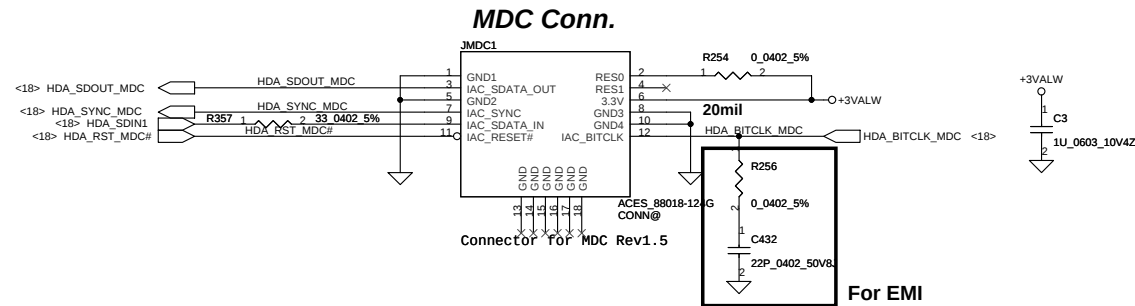
Power Button



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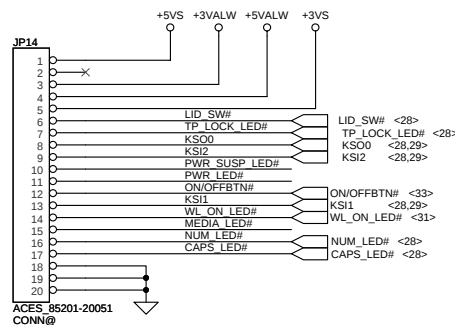


BLUE/AMB LED

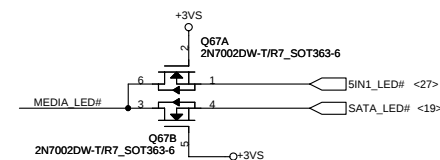
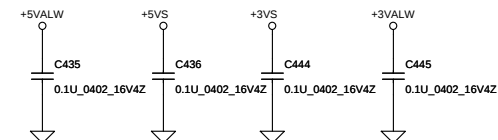


For EMI

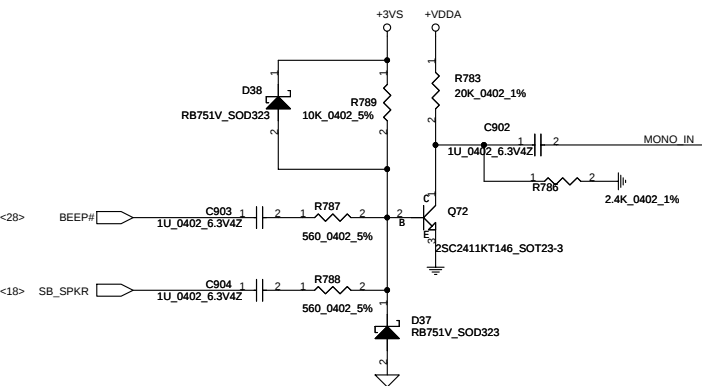
To PWR LED/B



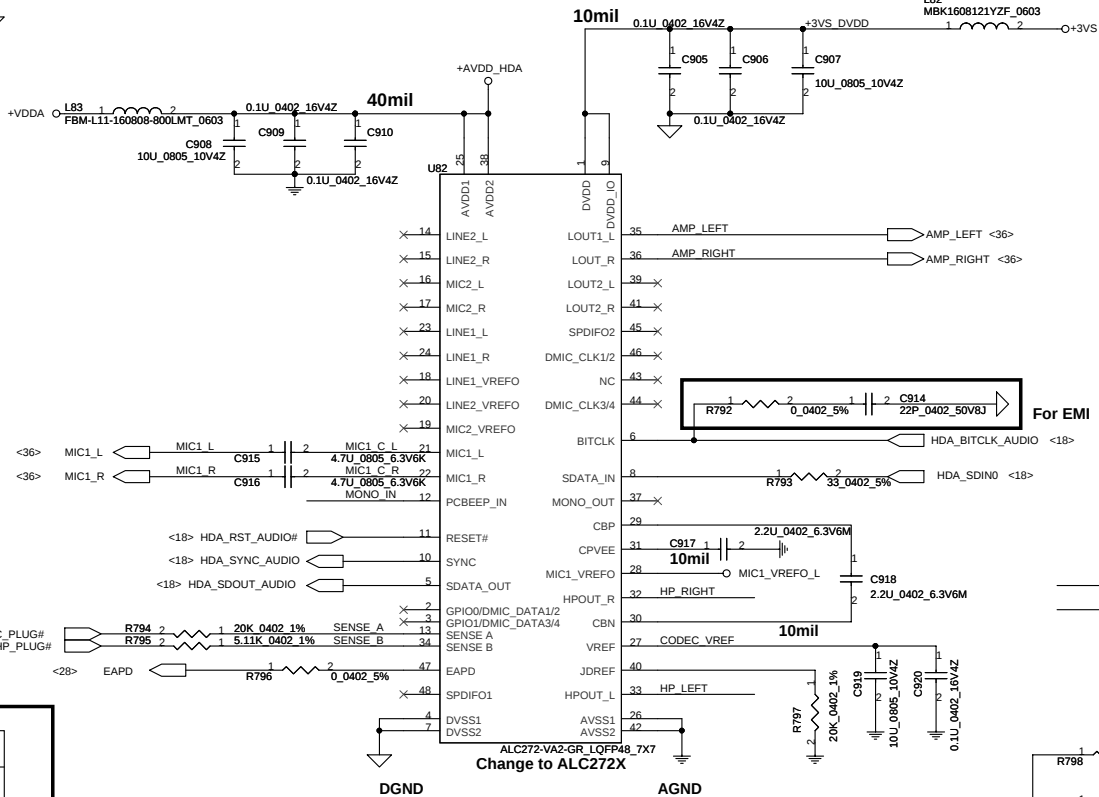
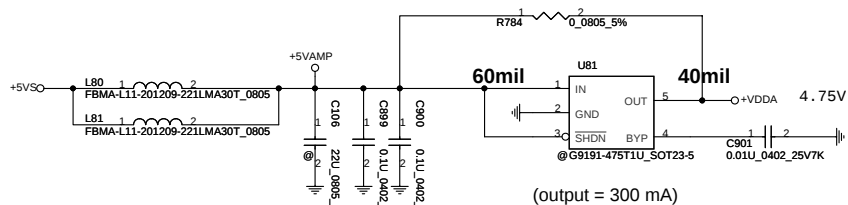
	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



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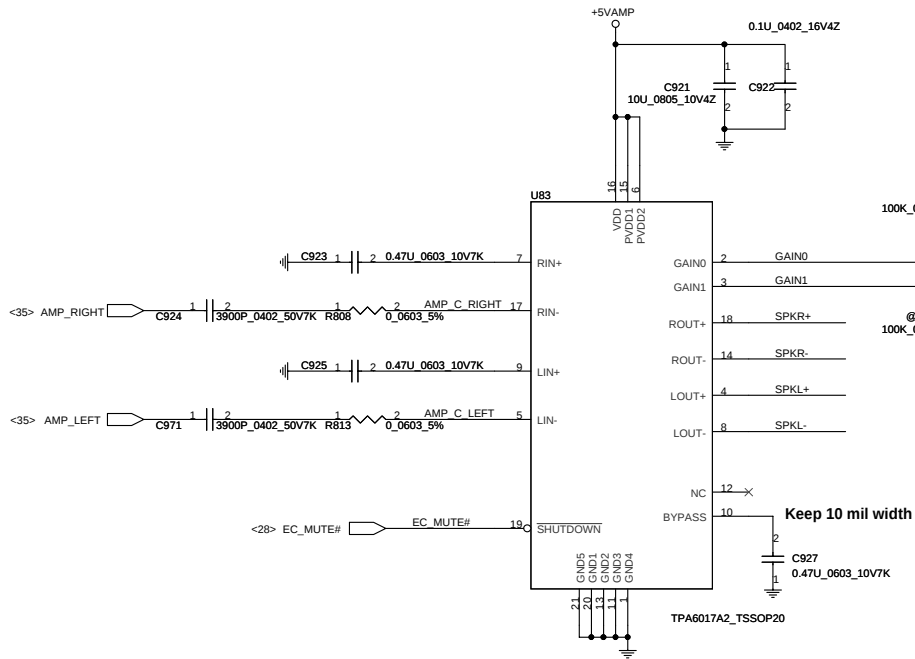


HD Audio Codec

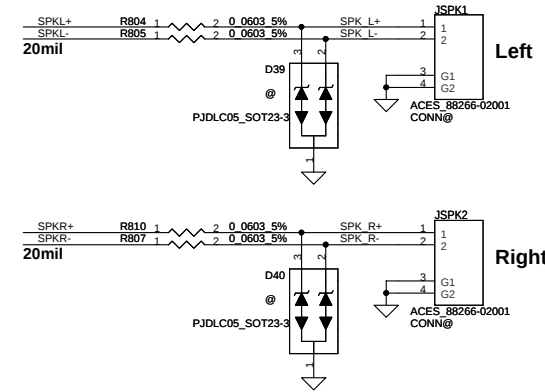


update this table

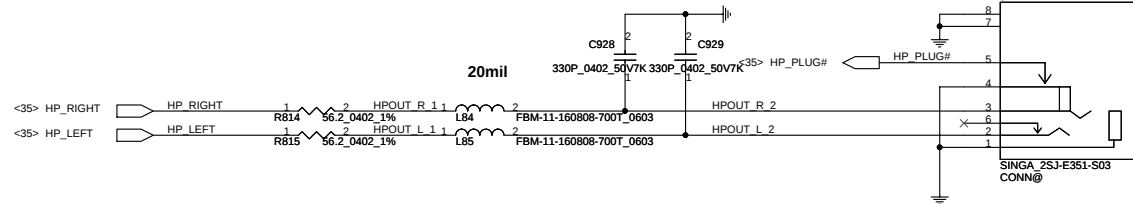
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



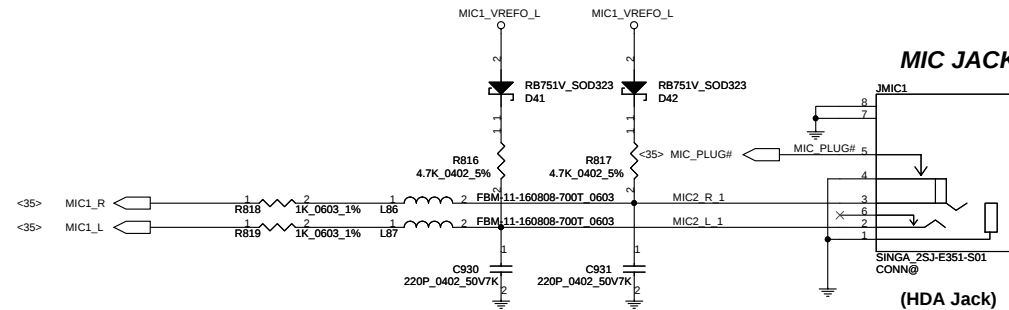
Int. Speaker Conn.



LINE Out/Headphone Out

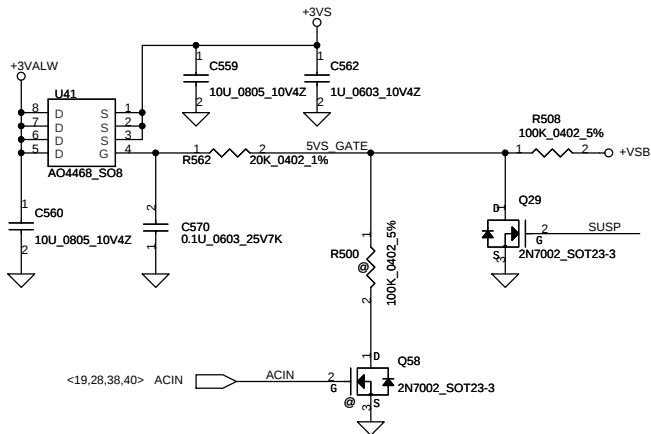


MIC JACK

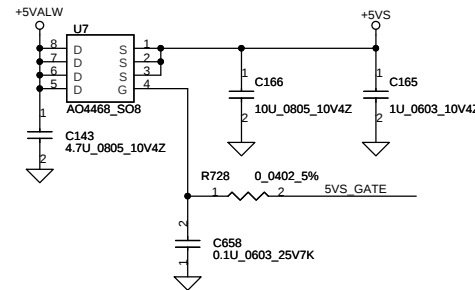


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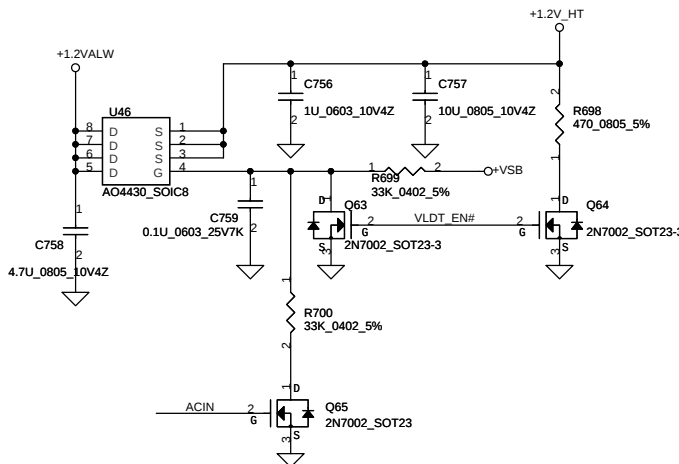
+3VALW TO +3VS



+5VALW TO +5VS

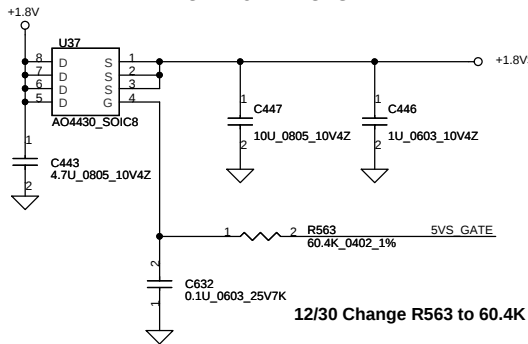


+1.2VALW TO +1.2V_HT

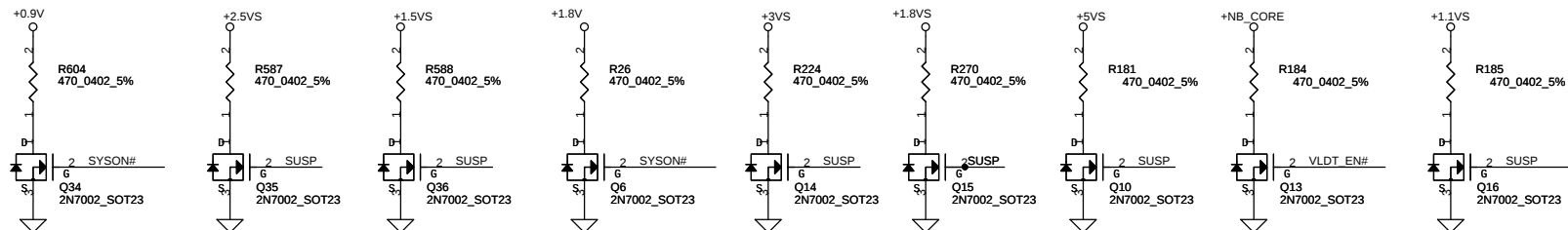
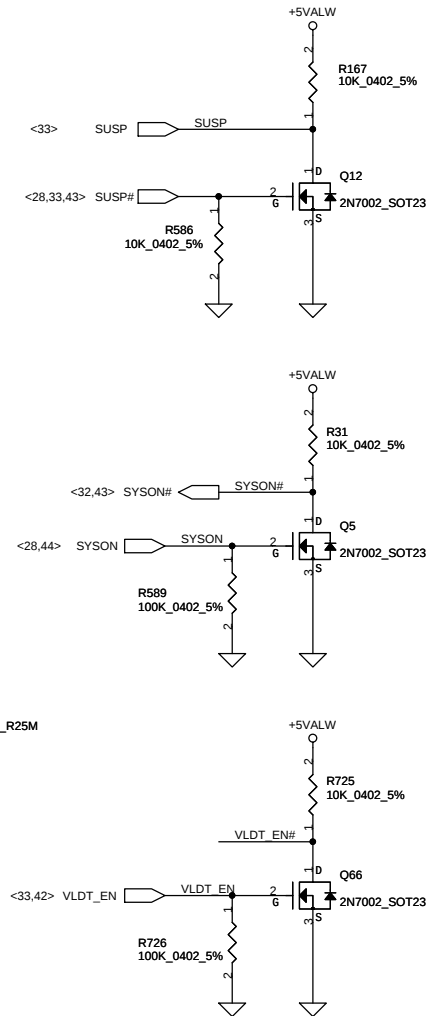


For PWR request

+1.8V TO +1.8VS

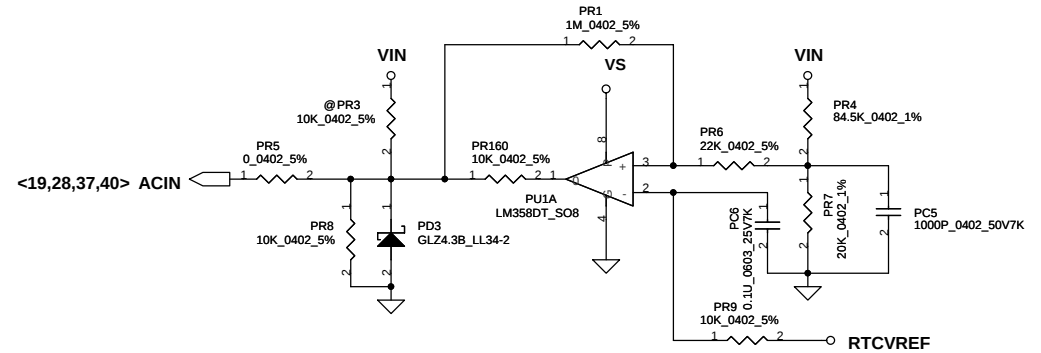
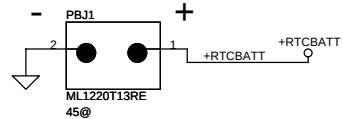
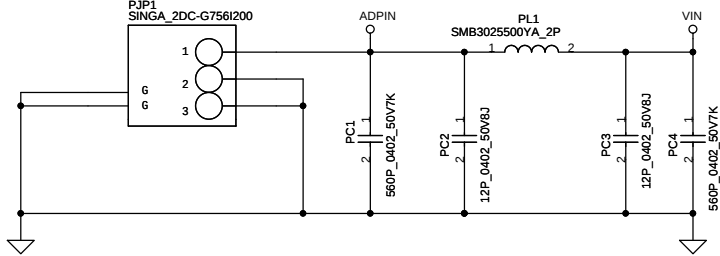


12/30 Change R563 to 60.4K

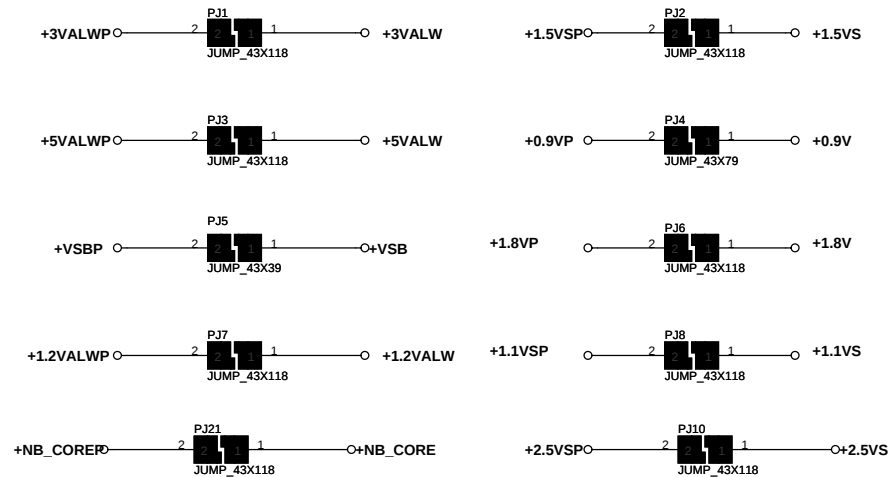
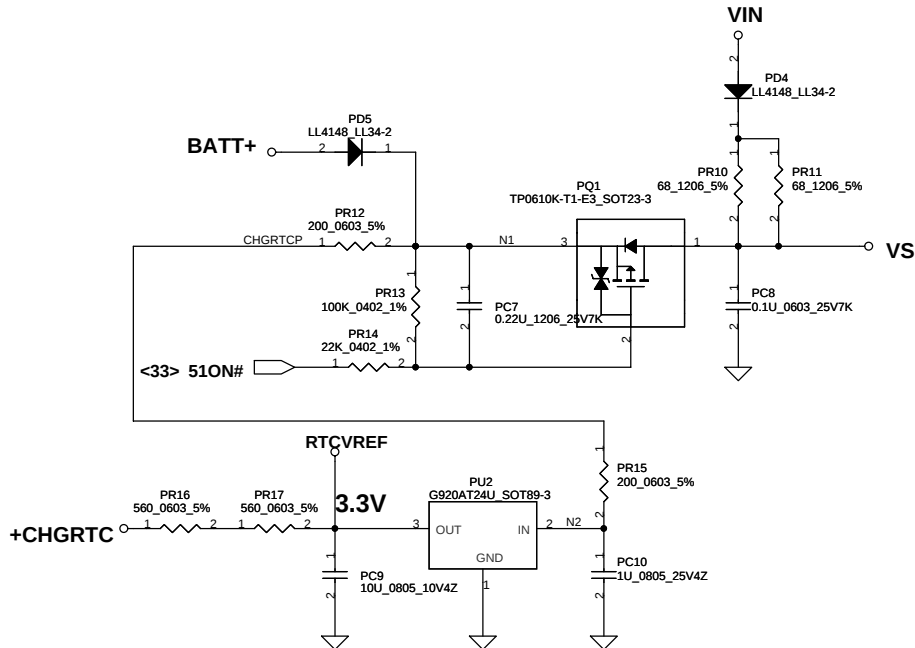


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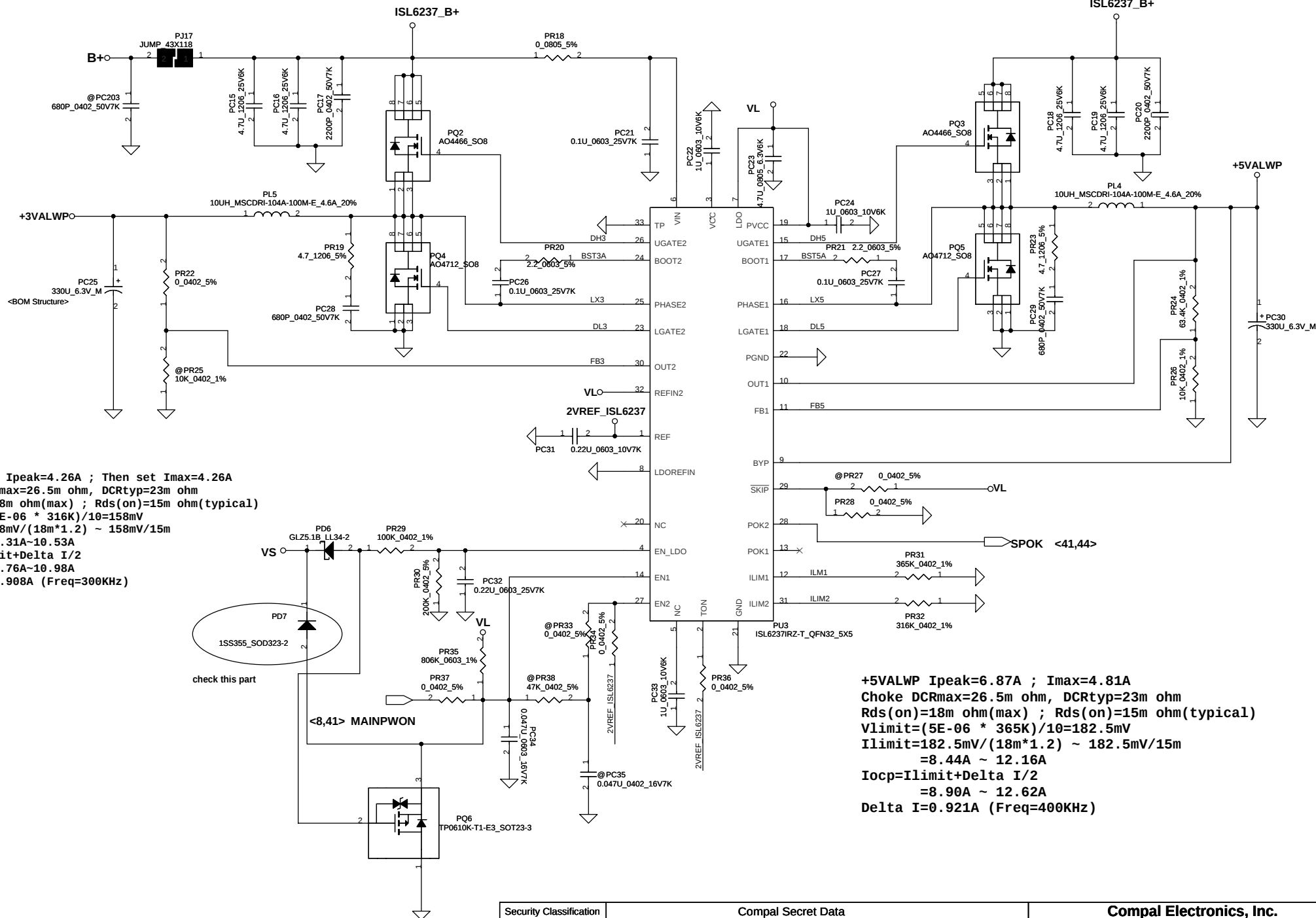
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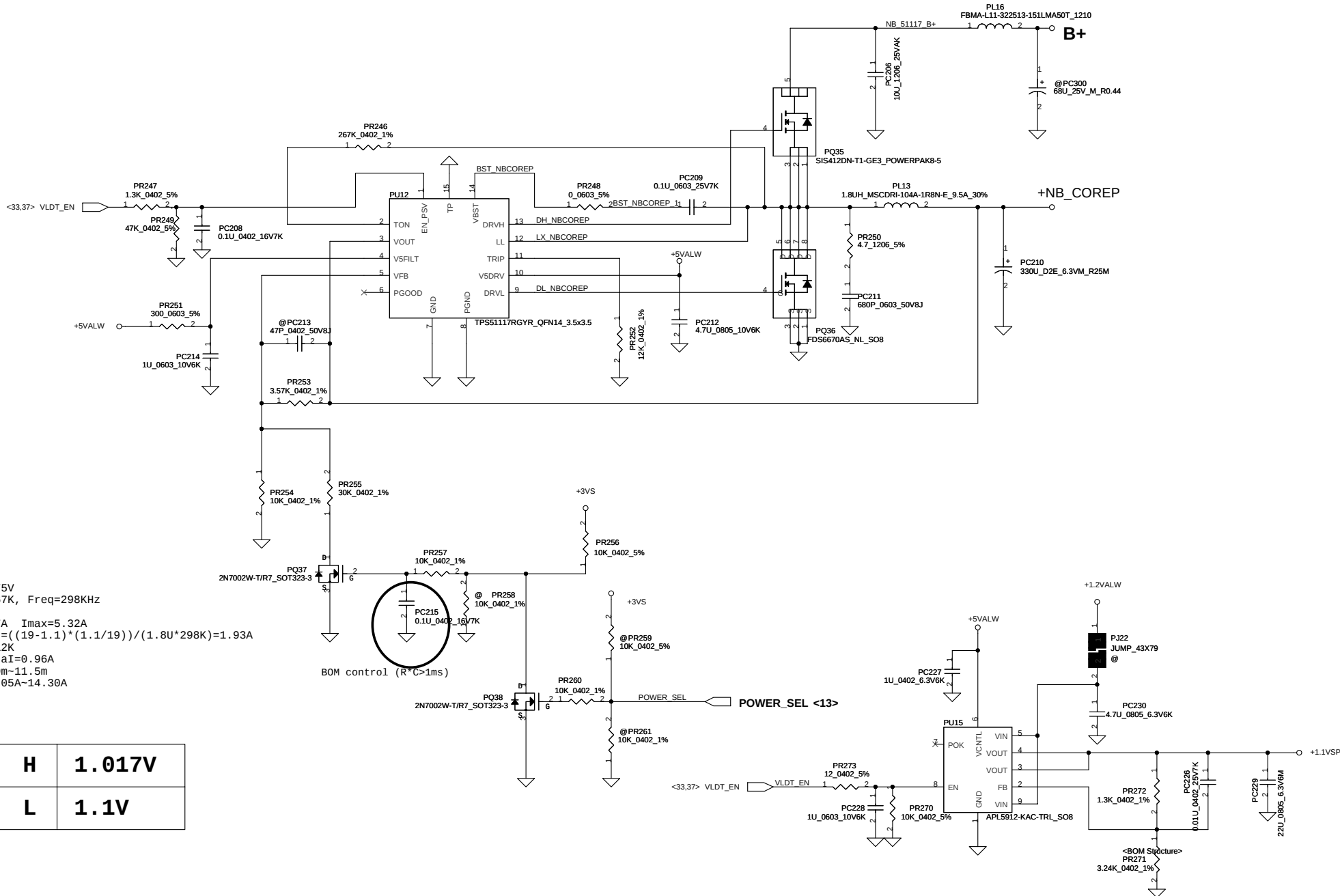
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



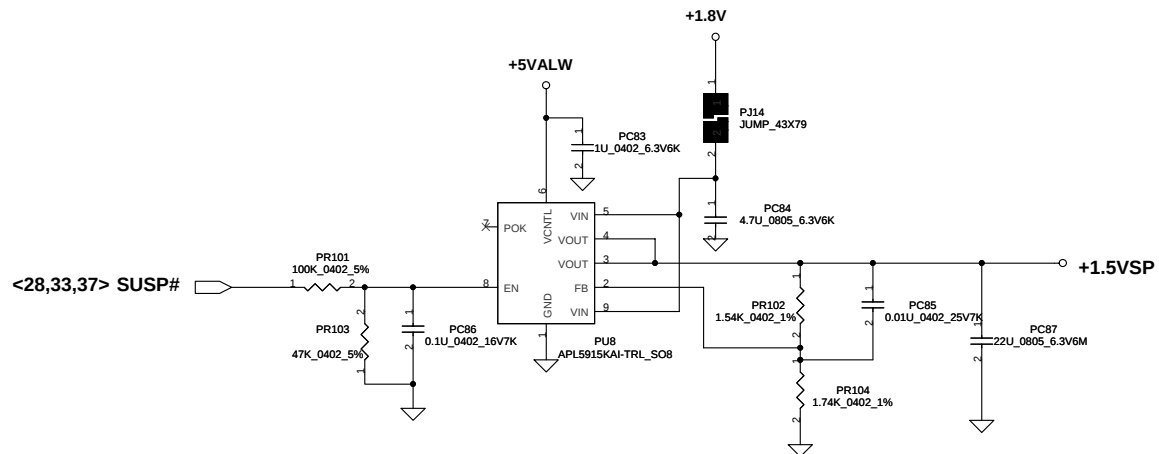
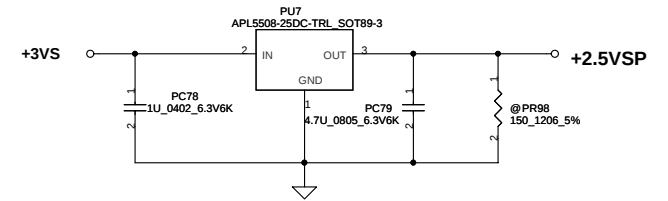
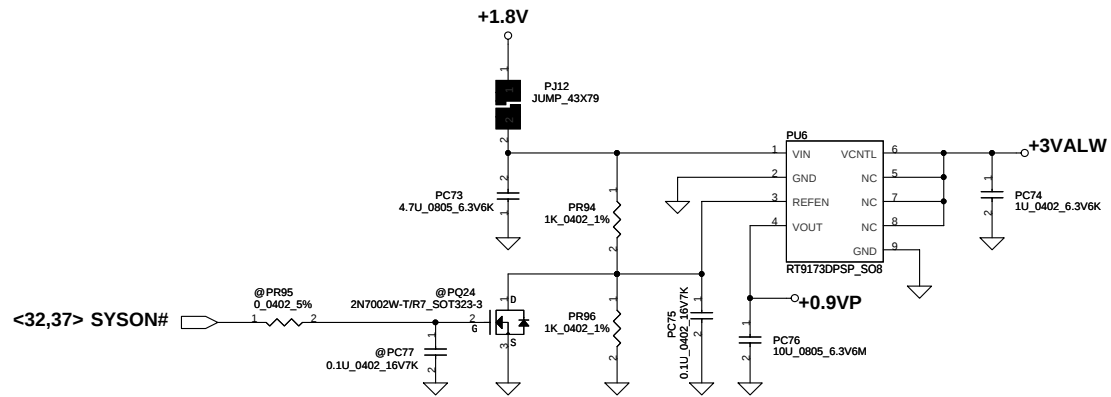
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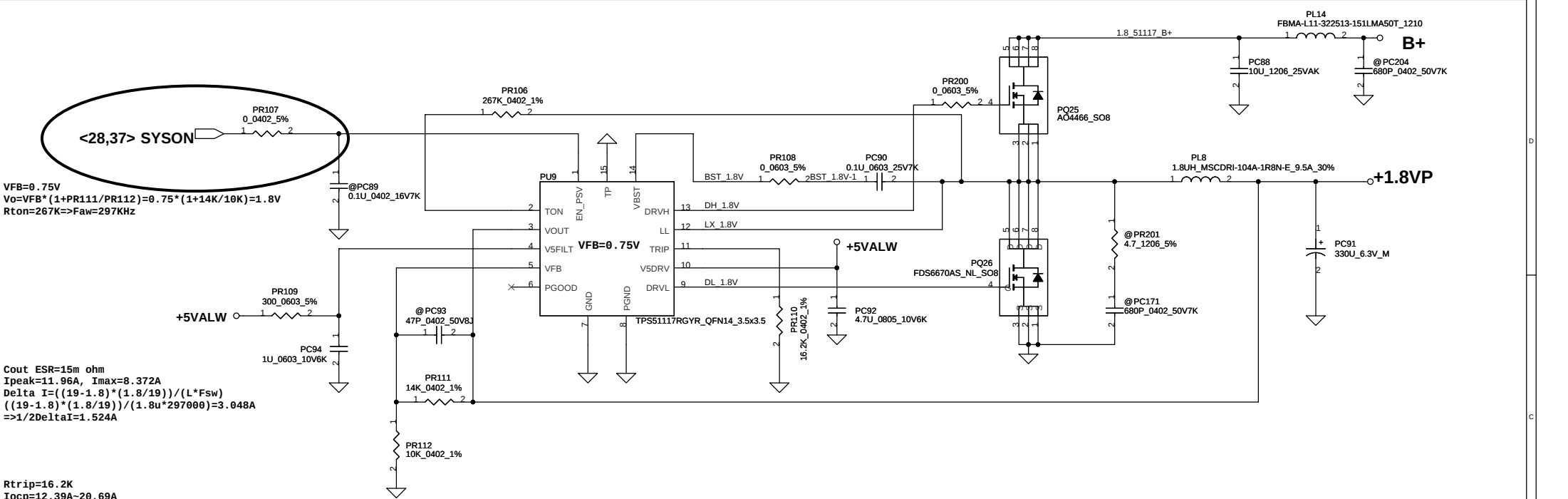
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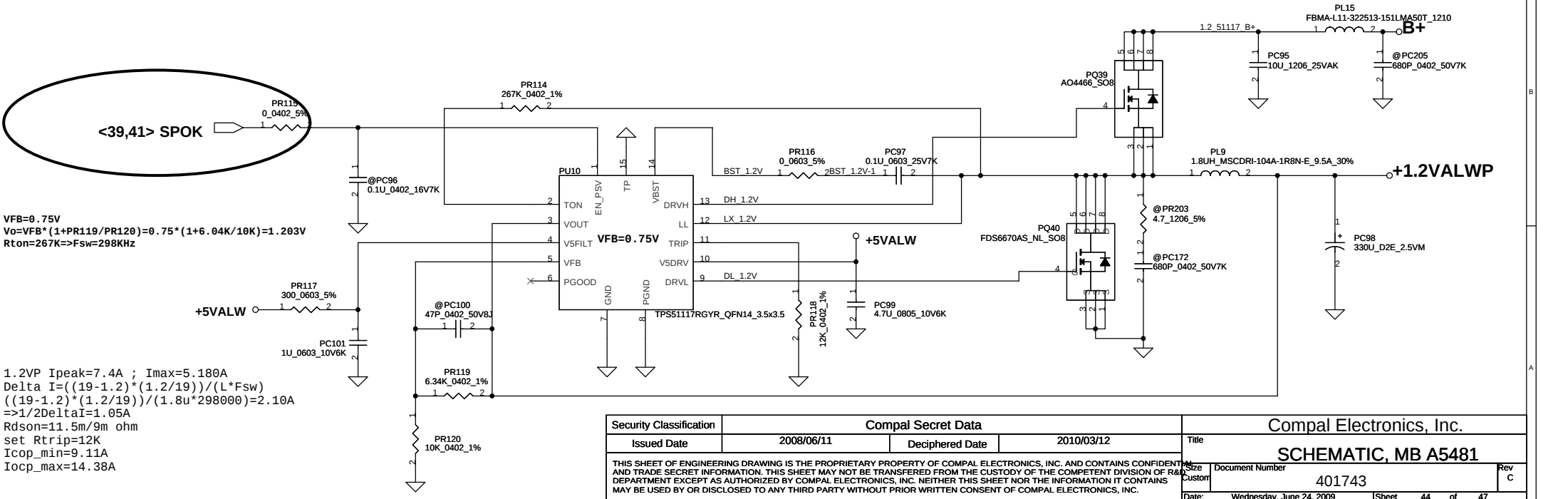
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VFB=0.75V
Vo=VFB*(1+PR111/PR112)=0.75*(1+14K/10K)=1.8V
Rton=267K=>Faw=297KHz

Cout ESR=15m ohm
Ipeak=11.96A, Imax=8.372A
Delta I=((19-1.8)*(1.8/19))/(L*Fsw)
((19-1.8)*(1.8/19))/(1.8u*297000)=3.048A
=>1/2DeltaI=1.524A

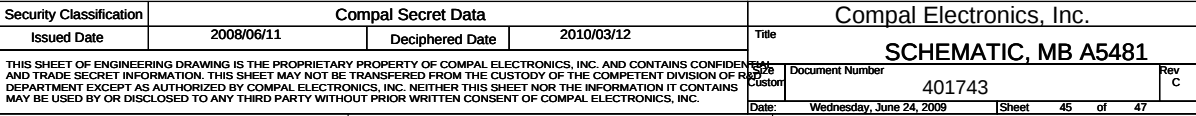
Rtrip=16.2K
Iocp=12.39A-20.69A



VFB=0.75V
Vo=VFB*(1+PR119/PR120)=0.75*(1+6.04K/10K)=1.203V
Rton=267K=>Fsw=298KHz

1.2VP Ipeak=7.4A ; Imax=5.180A
Delta I=((19-1.2)*(1.2/19))/(L*Fsw)
((19-1.2)*(1.2/19))/(1.8u*298000)=2.10A
=>1/2DeltaI=1.05A
Rdson=11.5m/9m ohm
set Rtrip=12K
Icop_min=9.11A
Iocp_max=14.38A

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	HW required to adjust from 1.14V to 1.12V	HW required to adjust from 1.14V to 1.12V	0.1	42	Change PR271 from SD034300180 (S RES 1/16W 3K +-1% 0402) to SD034324180 (S RES 1/16W 3.24K 0402 1%)	09, 05/07	to PVT
2	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Add PC208 SE076104K80 (S CER CAP .1U 16V K X7R 0402)	09, 05/07	to PVT
3	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Change PR247 from SD028000080 (S RES 1/16W 0 +-5% 0402) to SD028130180 (S RES 1/16W 1.3K 0402 5%)	09, 05/07	to PVT
4	NB_COREP working frequency has issue.	Because NB_COREP working frequency will be glifter while system at heavy loading. Change to larger ESR Cap will be solve.	0.1	42	Change PC210 from SGA19331D00 (S POLY C 330U 2.5V M D2 TPE LESR15M H1.8) to SGA00002B00 (S POLY C 330U 6.3V M D2E ESR25M TPE H1.8)	09, 05/07	to PVT
5	BOM error	BOM error	0.1	42	Add PR270 SD28100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
6	BOM error	BOM error	0.1	42	Change PR103 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							

Version change list (P.I.R. List) for HW									
Item	Reason for change	Modify List	PG#	Date	Item	Reason for change	Modify List	Rev.	PG#
1	PWR update circuit			4/9	26				
2	BOM change	R118 reserve	P.18	4/9	27				
3	BOM change	Change R178, R179 to 90.9/158 ohm	P.16	4/9	28				
4	BOM change	R30, R39 reserve	P.24	4/9	29				
5	BOM change	Add C30	P.38	4/9	30				
6	BOM change	Add R634, R639	P.28	4/9	31				
7	BOM change	C383 Reserve	P.24	4/9	32				
8		Pop R419	P.20	4/10	33				
9	PWR update circuit			5/15					
10	For Panel flash issue	R1,D2 Reserve, pop R763	P.24	5/18					
11	For Panel flash issue	Add R414 and non-pop	P.24	5/18					
12	Lid_SW intial issue	Add R19	P.28	5/18					
13	HPET timer issue	Change C288,C290 to 33P	P.16	5/18					
14	BOM change	change C276,C279 10P to 27P	P.19	5/19					
15									
16									
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Version change list (P.I.R. List) for HW									
Item	Reason for change	Modify List	PG#	Date	Item	Reason for change	Modify List	Rev.	PG#
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4	BOM change	R30, R39 reserve	P.24	4/9	29				
5	BOM change	Add C30	P.38	4/9	30				
6	BOM change	Add R634, R639	P.28	4/9	31				
7	BOM change	C383 Reserve	P.24	4/9	32				
8		Pop R419	P.20	4/10	33				
9	PWR update circuit			5/15					
10	For Panel flash issue	R1,D2 Reserve, pop R763	P.24	5/18					
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3	BOM change	Change R178, R179 to 90.9/158 ohm	P.16	4/9	28				
4	BOM change	R30, R39 reserve	P.24	4/9	29				
5	BOM change	Add C30	P.38	4/9	30				
6	BOM change	Add R634, R639	P.28	4/9	31				
7	BOM change	C383 Reserve	P.24	4/9	32				
8		Pop R419	P.20	4/10	33				
9	PWR update circuit			5/15					
10	For Panel flash issue	R1,D2 Reserve, pop R763	P.24	5/18					
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13	HPET timer issue	Change C288,C290 to 33P	P.16	5/18					
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