

Compal Confidential

NEW50/70/80/90 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M
ATI Madision/Park

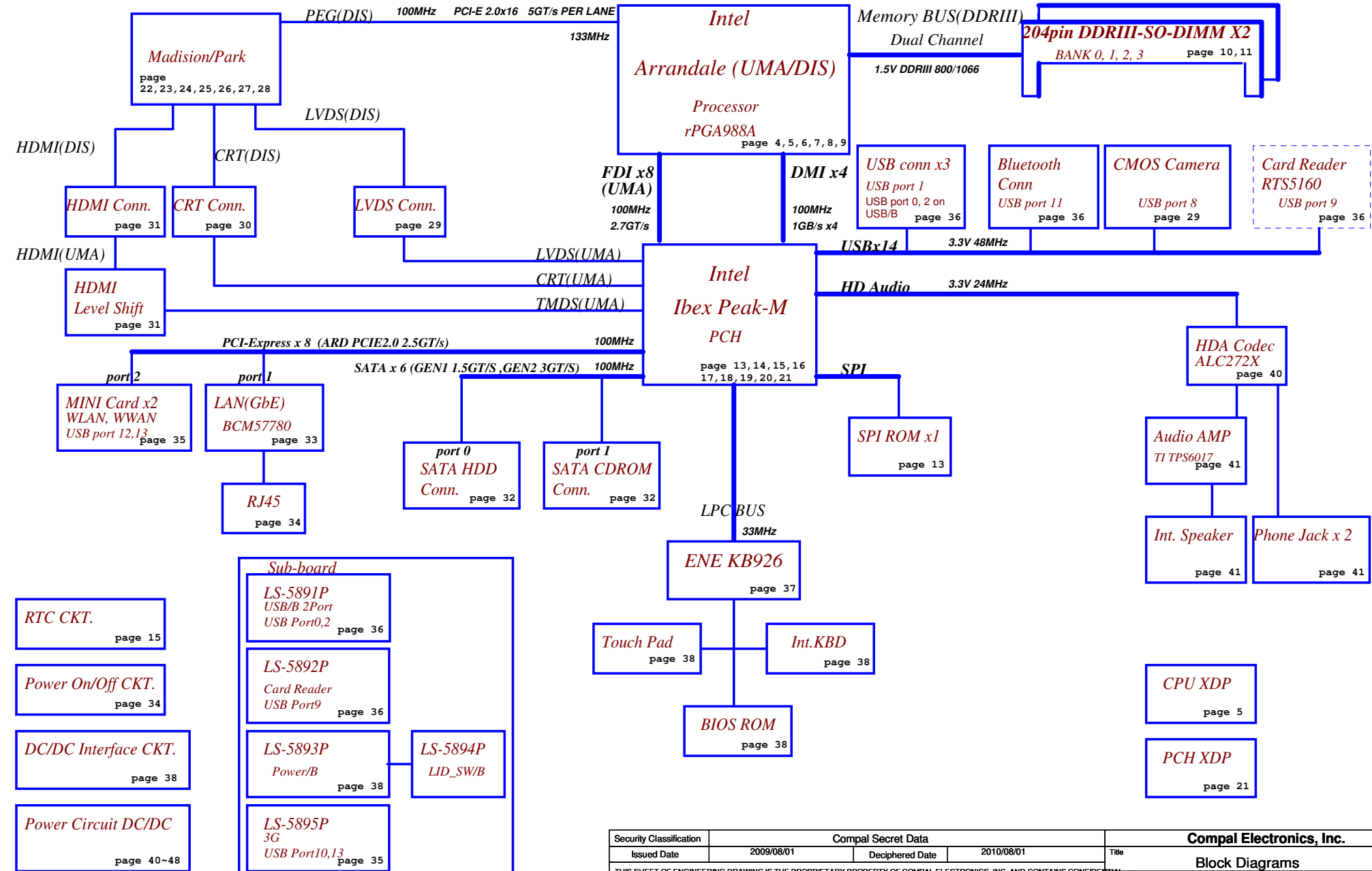
2010-01-07

REV: 1.0

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Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	Cover Page	
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Fan Control
page 38

Clock Generator
IDT: 9LVS3199AKLFT
Realtek: RTM890N-631-VB-GRT
133/120/100/96/14.318MHZ to PCH
page 12



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address	
Clock Generator (9LVS3199AKFLT, RTM890N-631-VB-GRT)	1101 0010b	3G & BT Config
DDR DIMM0	1001 000Xb	3G SKU: 3G@
DDR DIMM2	1001 010Xb	BT SKU: BT@
GPU BOM Config		
UMAHD@	VGAHD@	HDMI@
UMA	V	X
VGA	X	V
SG	X	V
NO HDMI	X	X
VRAM BOM Config		
X761@:	X76198BOL01	Park Samsung 512MB
X762@:	X76198BOL02	Park Hynix 512MB
X763@:	X76198BOL03	Madision Samsung 1024MB
X764@:	X76198BOL04	Madision Hynix 1024MB
X765@:	X76198BOL05	Park AMD 512MB
X766@:	X76198BOL06	Madision AMD 1024MB
LED BOM config		
NEW70,80 SKU:	7080@	
NEW50,90 SKU:	5090@	

BOM Config	
UMA W/O HDMI SKU:	BT@/3G@/UMA@/UMAO@
UMA W/ HDMI SKU:	BT@/3G@/UMA@/UMAO@/HDMI@/UMAHD@
Discrete W/O HDMI SKU:	BT@/3G@/DIS@/DISO@/VGA@
Discrete W/ HDMI SKU:	BT@/3G@/DIS@/DISO@/VGA@/HDMI@/VGAHD@
Switchable W/O HDMI SKU:	BT@/3G@/DIS@/UMA@/VGA@/SG@
Switchable W HDMI SKU:	BT@/3G@/DIS@/UMA@/VGA@/SG@/HDMI@/VGAHD@

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

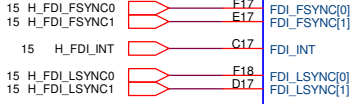
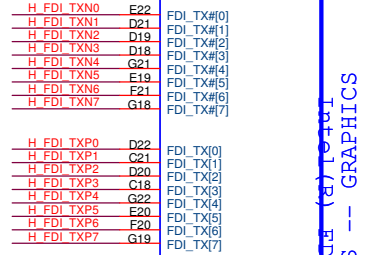
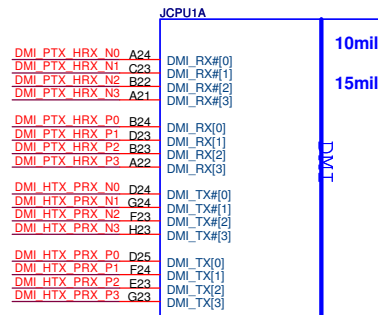
BTO Item	BOM Structure
UMA	UMA@
UMA Only	UMAO@
Discrete	DIS@
Discrete Only	DISO@
GPU ALL Components	VGA@
VRAM	X76@
Switchable	SG@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
Unpop	@
UMA HDMI	UMAHD@
Discrete HDMI	VGAHD@
UMA & DIS POP HDMI	HDMI@
GPU Madision	MADI@
GPU Park	PARK@
NEW70,80 LED	7080@
NEW50,90 LED	5090@

USB Port Table

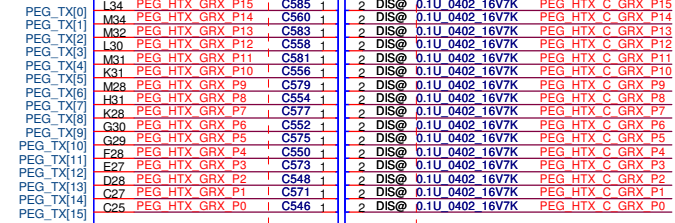
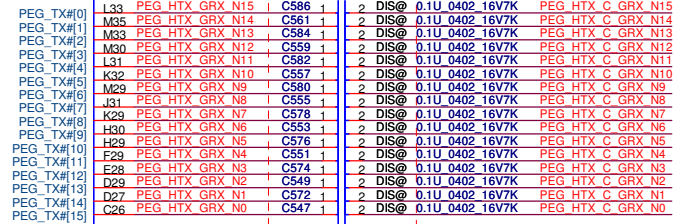
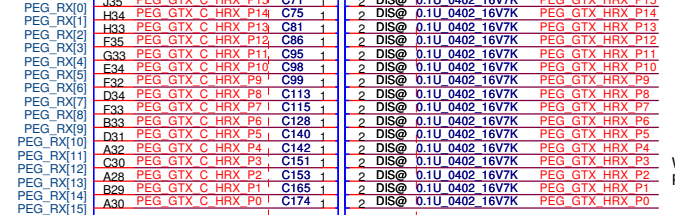
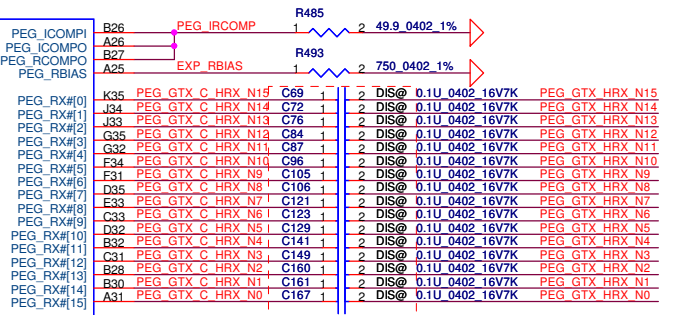
USB 2.0	USB 1.1	Port	3 External USB Port
EHC11	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
EHC12	UHCI4	7	
		8	Camera
	UHCI5	9	Card Reader
		10	SIM Card
	UHCI6	11	Blue Tooth
		12	Mini Card(WLAN)
		13	Mini Card(GPS)

X76@			ID2: VRAM Size		
ID3 , ID1 : VRAM Vender			Location		
VRAM			VRAM_ID1		
Samsung			VRAM_ID2		
HYNIX			8PCS 64Mx16		
AMD			4PCS 64Mx16		
VRAM P/N :			R482		
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)			R483		
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)					
AMD : SA00003PF20 (S IC D3 23EY2387MB-12)					

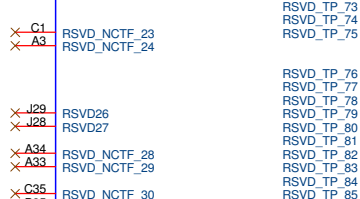
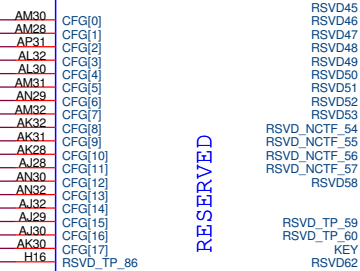
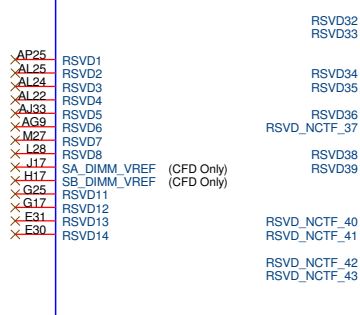
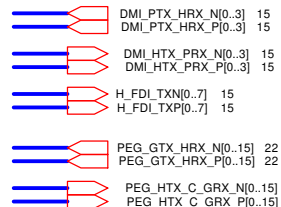
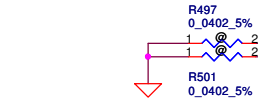
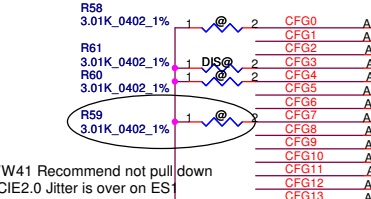
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IC:AUB_CFD_rPGA,R1P0
CONN@

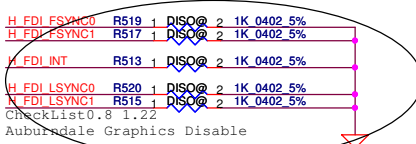


IC:AUB_CFD_rPGA,R1P0
CONN@



IC:AUB_CFD_rPGA,R1P0
CONN@

eDP Signals Mapping		
eDP Signal	PEG Signals	Lane Reversal
eDP_TX0	PEG HTX_C_GRX_P15	PEG HTX_C_GRX_P0
eDP_TX#0	PEG HTX_C_GRX_N15	PEG HTX_C_GRX_N0
eDP_TX1	PEG HTX_C_GRX_P14	PEG HTX_C_GRX_P1
eDP_TX#1	PEG HTX_C_GRX_N14	PEG HTX_C_GRX_N1
eDP_TX2	PEG HTX_C_GRX_P13	PEG HTX_C_GRX_P2
eDP_TX#2	PEG HTX_C_GRX_N13	PEG HTX_C_GRX_N2
eDP_TX3	PEG HTX_C_GRX_P12	PEG HTX_C_GRX_P3
eDP_TX#3	PEG HTX_C_GRX_N12	PEG HTX_C_GRX_N3
eDP_AUX	PEG GTX_C_HRX_P13	PEG GTX_C_HRX_P2
eDP_AUX#	PEG GTX_C_HRX_N13	PEG GTX_C_HRX_N2
eDP_HPD#	PEG GTX_C_HRX_P12	PEG GTX_C_HRX_P3



CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

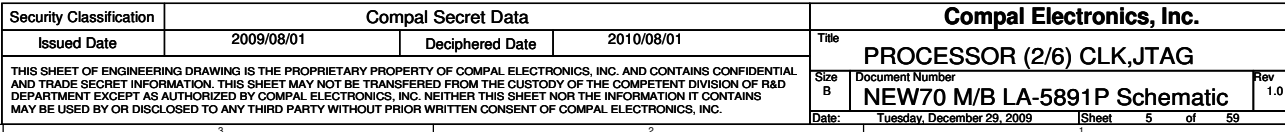
*1 :Normal Operation
0 :Lane Numbers Reversed
15 > 0, 14 > 1, ...

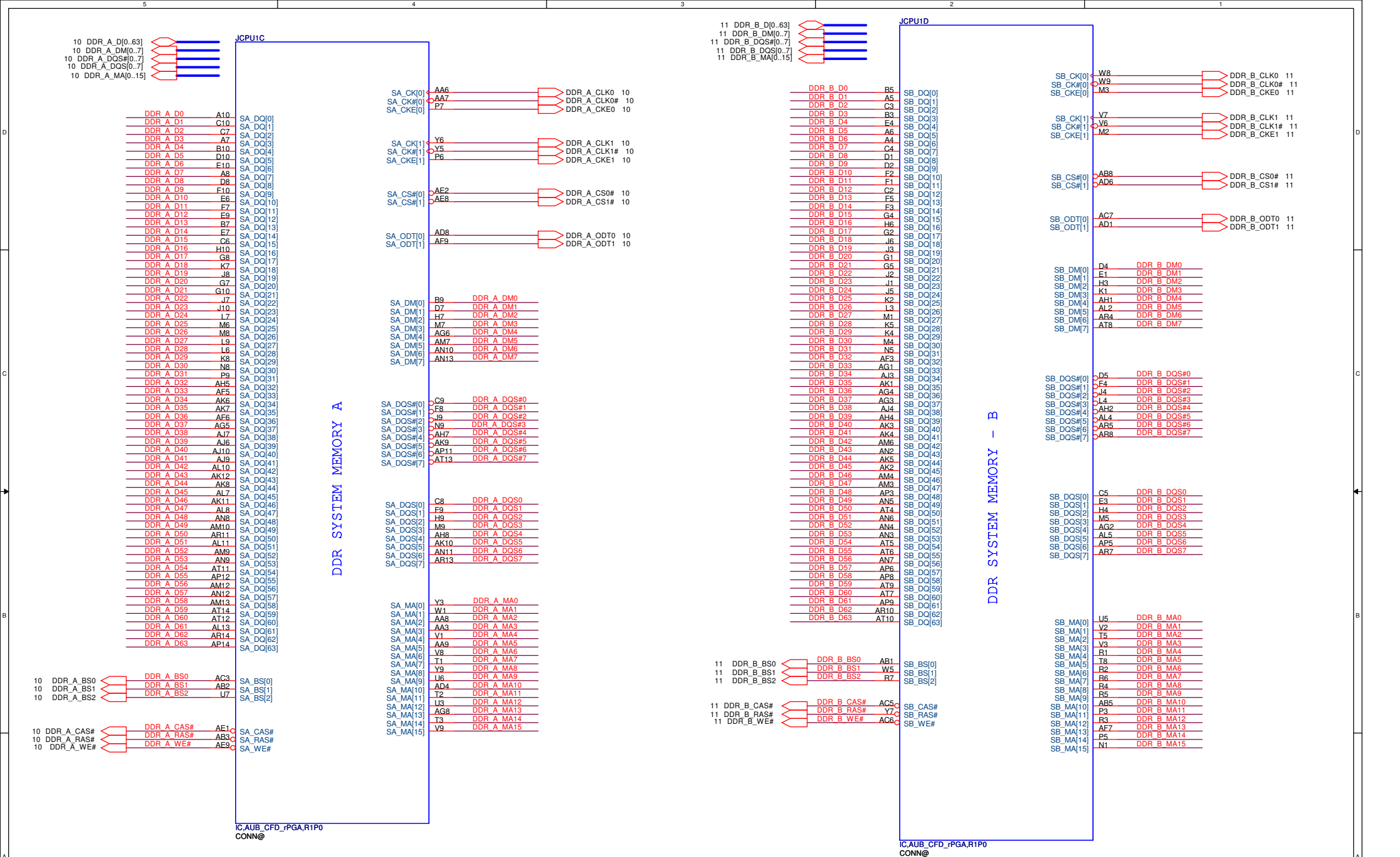
CFG4 - Display Port Presence

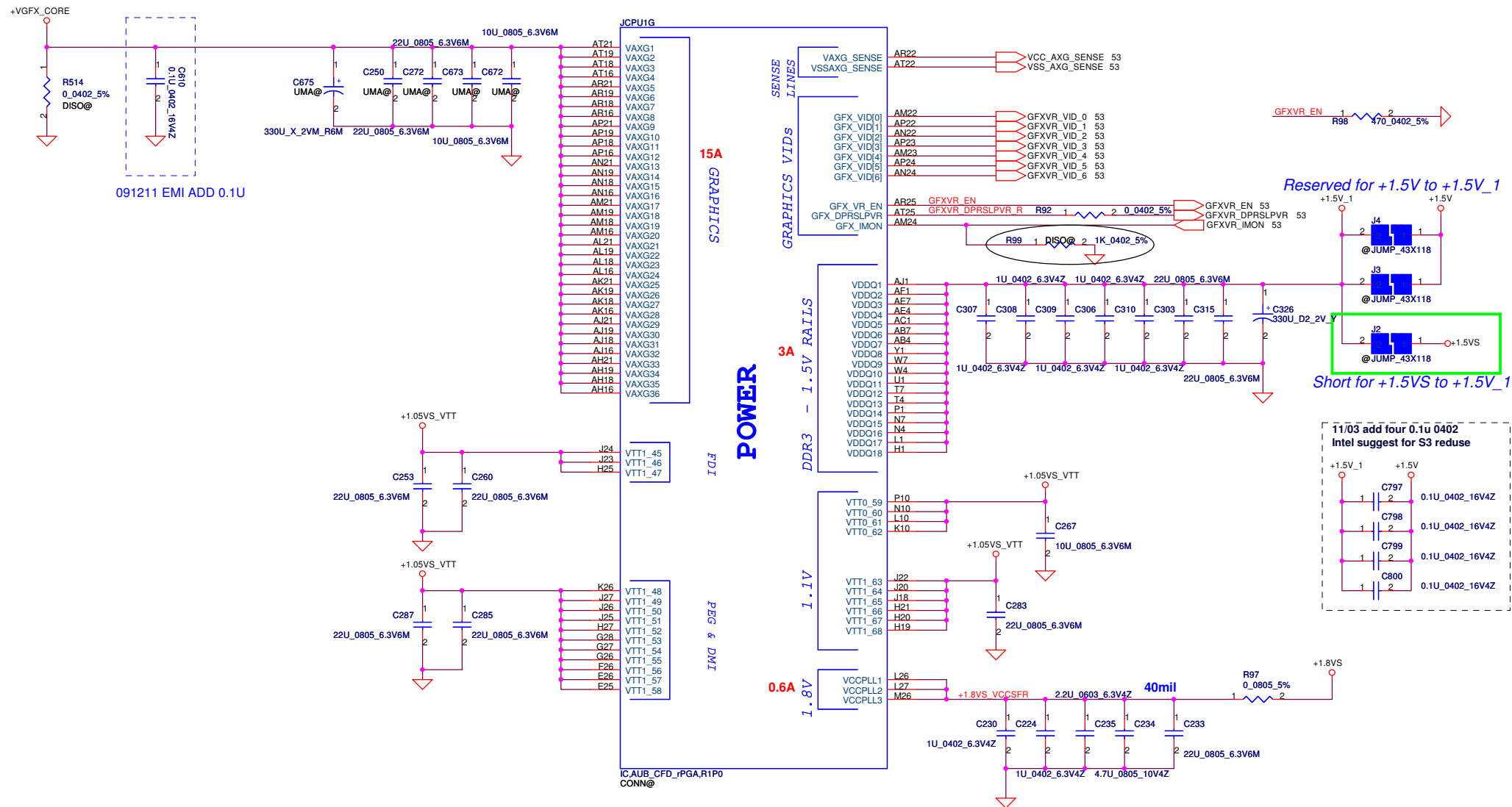
*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

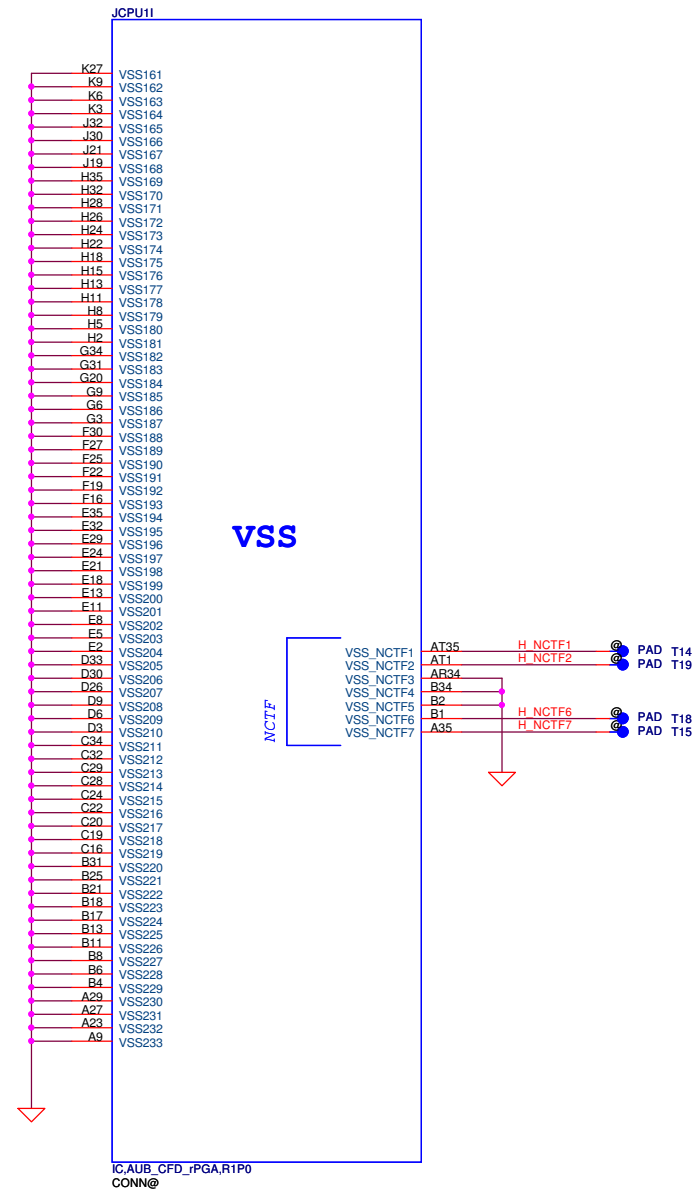
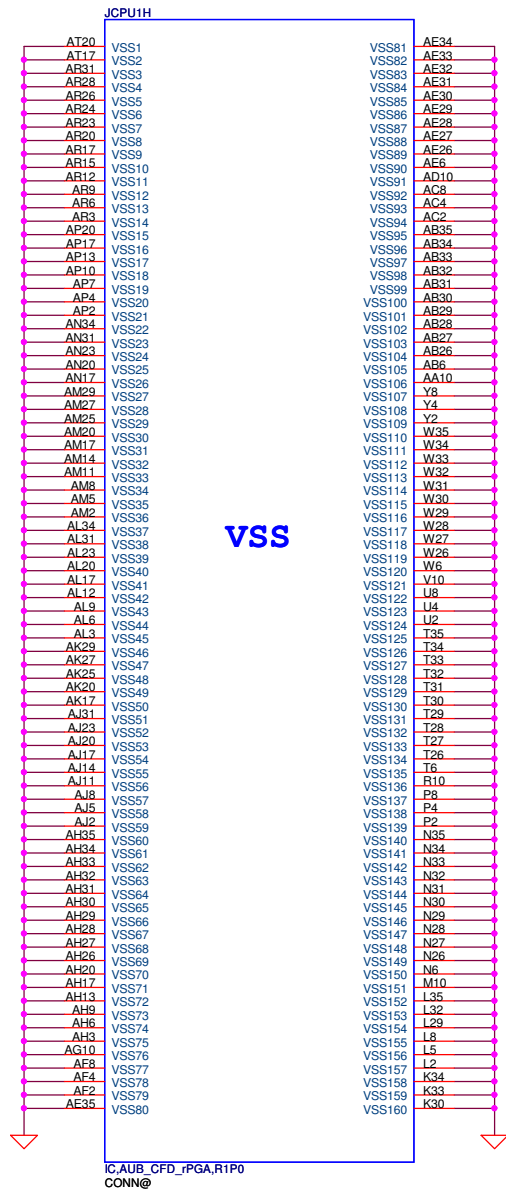
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						Size	Document Number			Rev		
						NEW70	M/B LA-5891P Schematic			1.0		
						Date:	Tuesday, December 29, 2009		Sheet	4	of	59



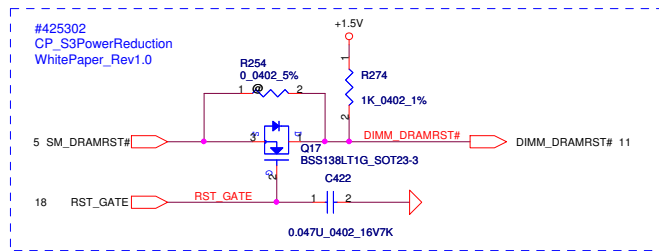
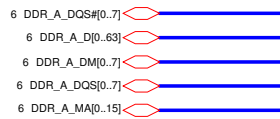




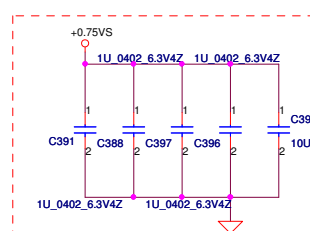
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						Customer		NEW70 M/B LA-5891P Schematic		1.0	
						Date:		Tuesday, December 29, 2009		Sheet 8 of 59	



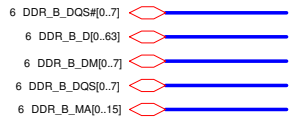
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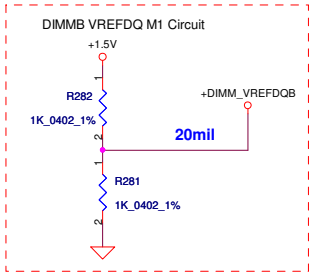
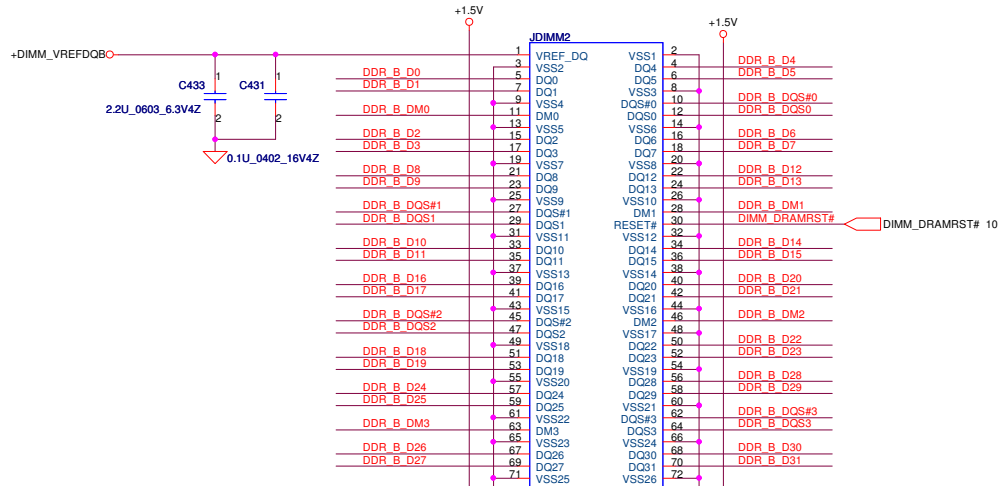
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



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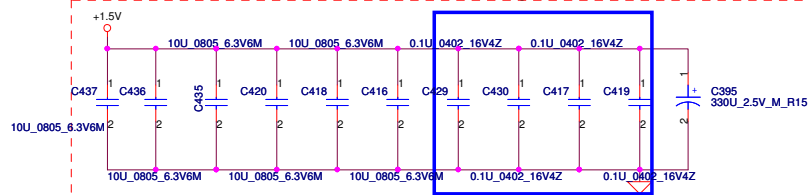


2008/9/8 #400755
Calpella Clarkfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

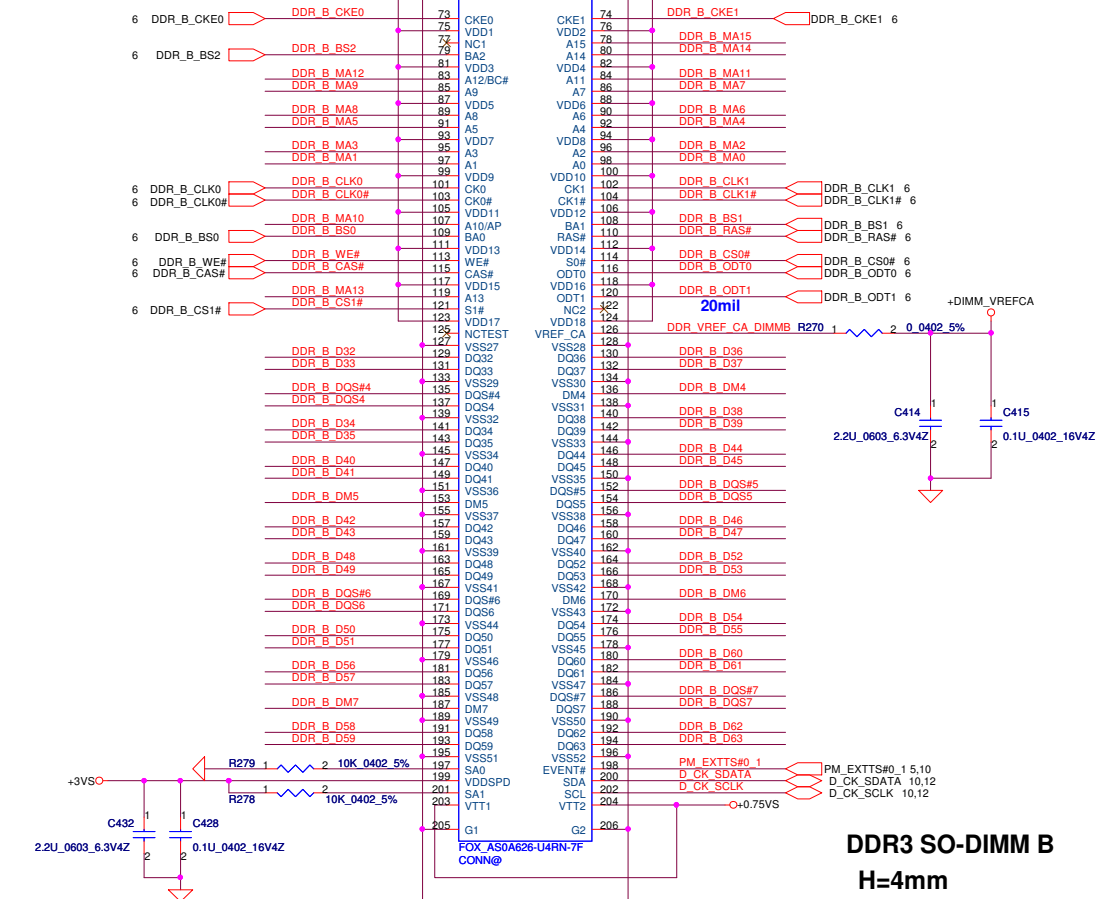
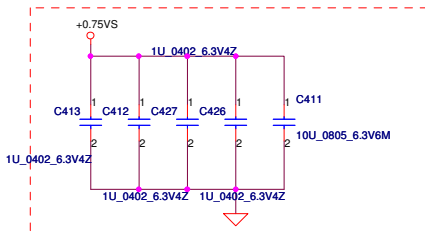


Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMB



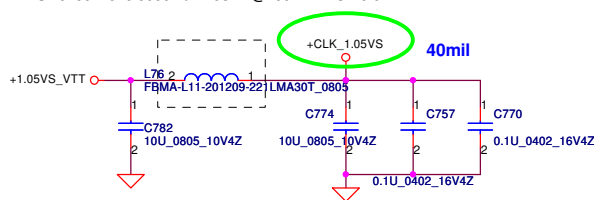
Layout Note:
Place near JDIMM2.203 & JDIMM2.204



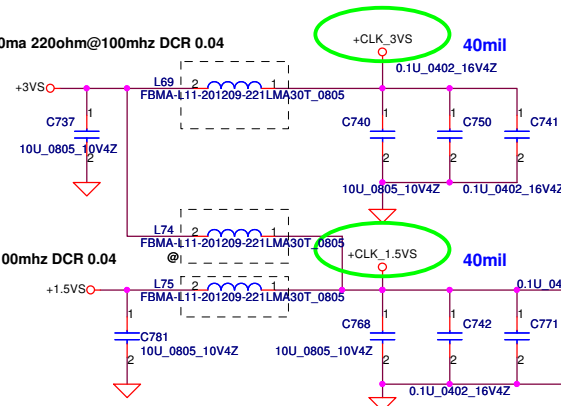
DDR3 SO-DIMM B
H=4mm

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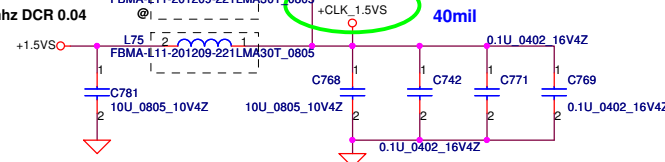
SM010014520 3000ma 220ohm@100mhz DCR 0.04



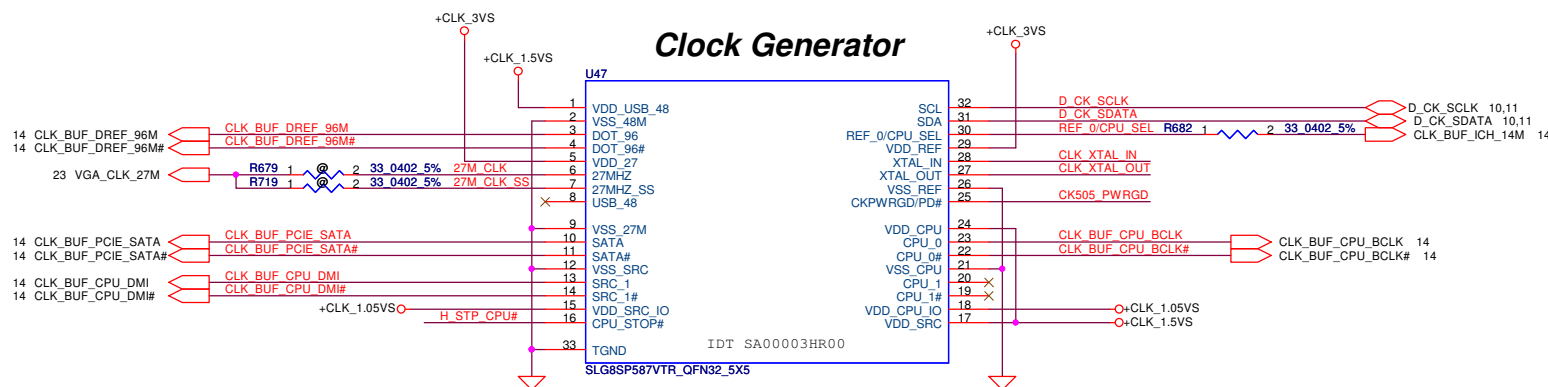
SM010014520 3000ma 220ohm@100mhz DCR 0.04



SM010014520 3000ma 220ohm@100mhz DCR 0.04



Clock Generator



IDT: 9LRS3199AKLFT, SA000030P00
SILEGO: SLG8SP587V(WF), SA00002XY10

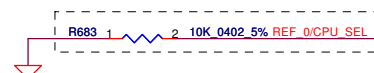
Low Power:

IDT: 9LVS3199AKLFT, SA00003HR00
Realtek: RTM890N-631-VB-GRT, SA00003HQ10

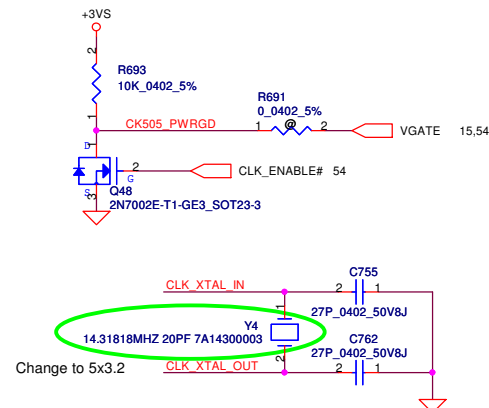
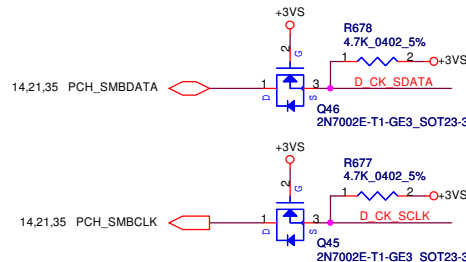
IDT 9LVS3199AKLFT NC



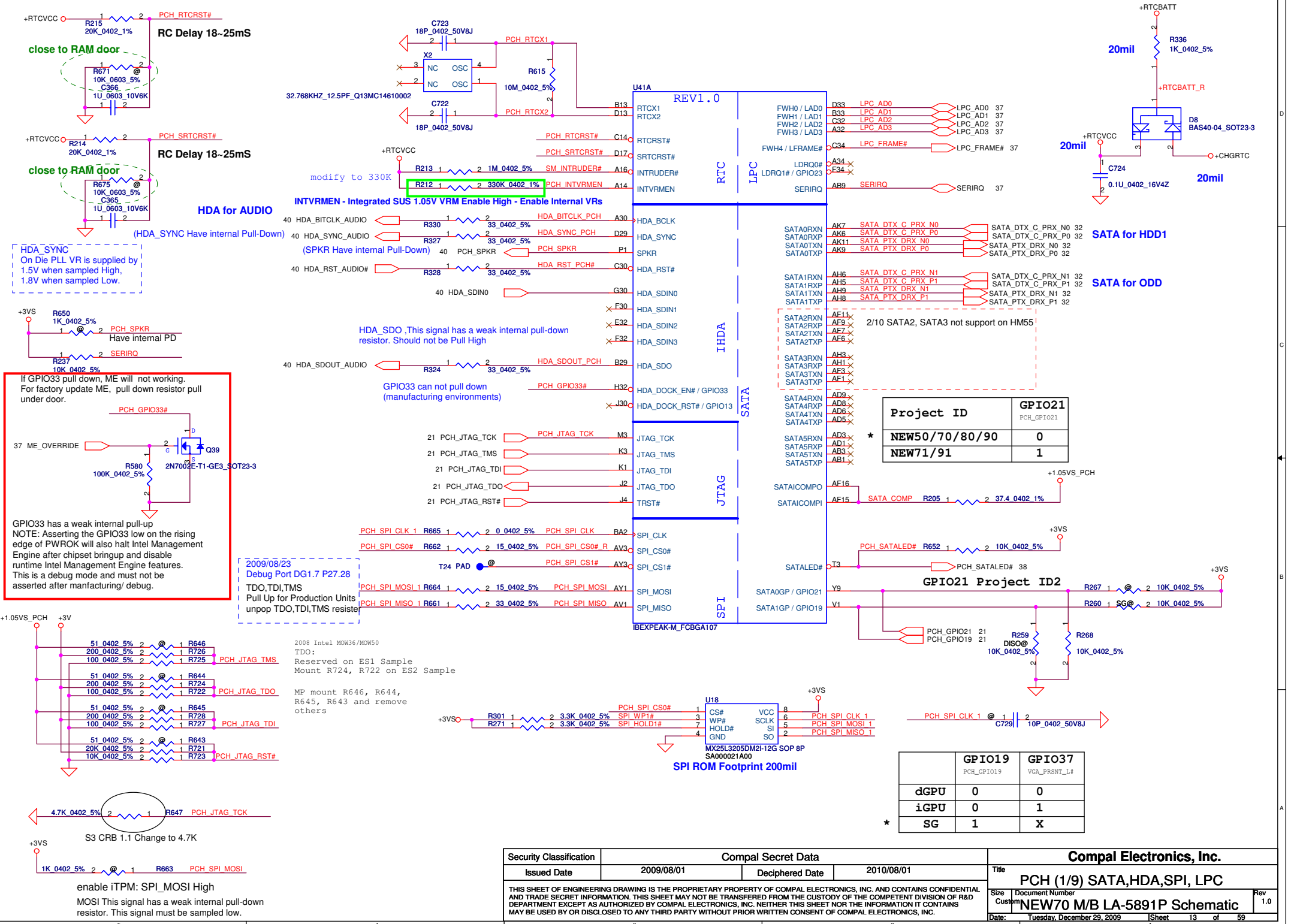
IDT Have Internal Pull-Down
FOR Realtek



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



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2010/08/01				Title				Clock Generator (CK505)			
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				NEW70 M/B LA-5891P Schematic				Rev			
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								Size	Document Number	Rev
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	59									

For PCIE LAN

For Wireless LAN

For Mini2

For PCIE LAN

For Wireless LAN

1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS
3. Level Shift2, Pull-Up to +3VS
4. Level Shift3, Pull-Up to +3VS

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

Change to 5x3.2

REV1.0

PCI-E*

From CLK BUFFER

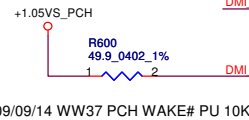
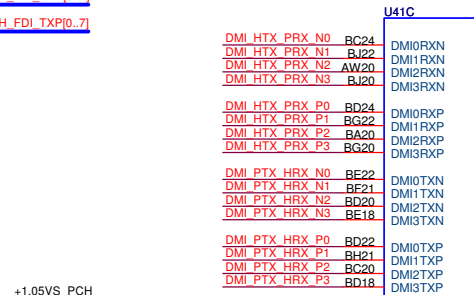
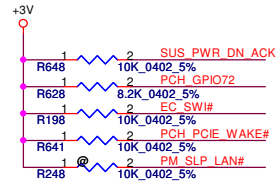
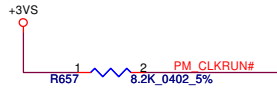
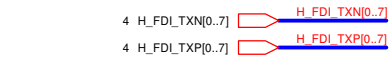
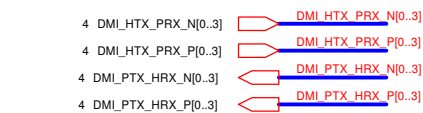
Clock Flex

1222 GPIO66
PULL HIGH:8L
PULL DOWN:6L

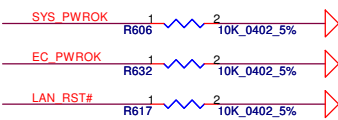
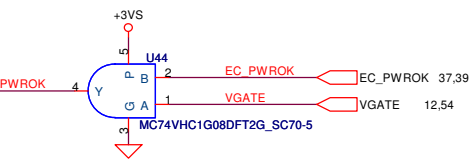
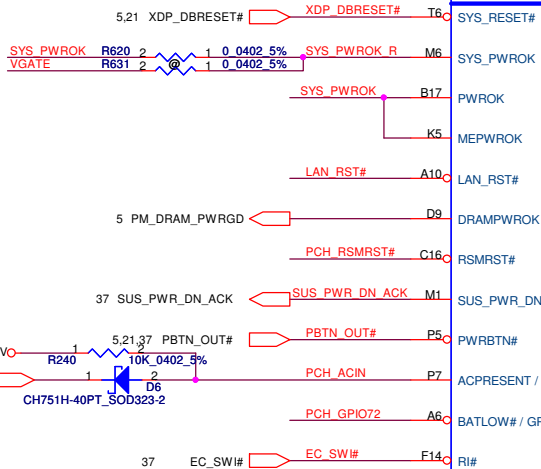
Project Structure

GPIO21	GPIO65	GPIO66	Structure
ID2	ID1	ID0	Structure
0	0	0	DVT
0	0	1	
0	1	0	PVT

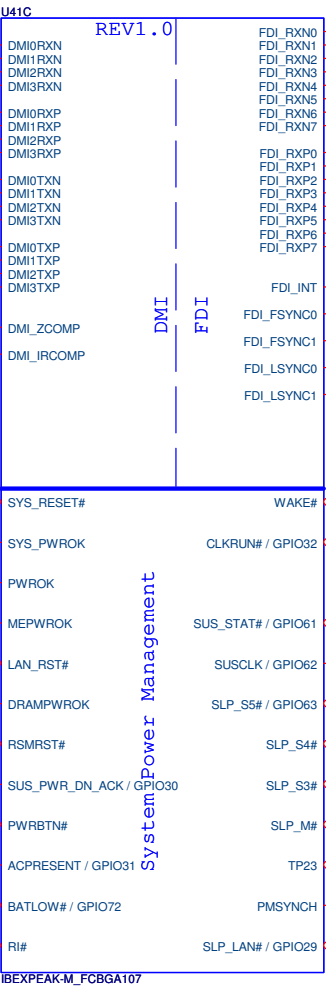
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						Size	Document Number			NEW70 M/B LA-5891P Schematic		Rev 1.0
						Customer						
						Date:		Friday, January 08, 2010		Sheet 14 of 59		



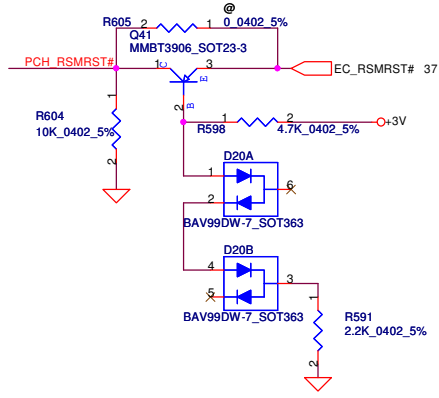
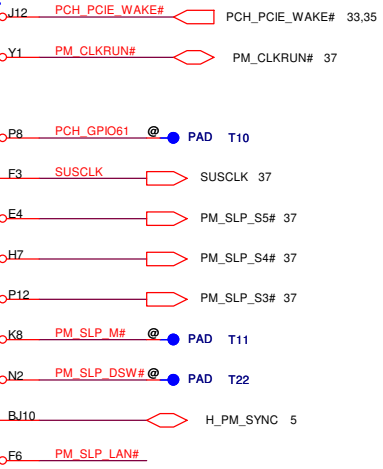
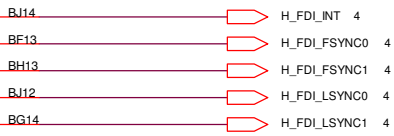
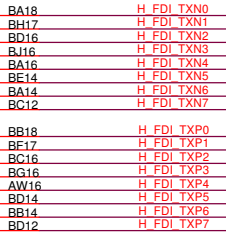
09/09/14 WW37 PCH WAKE# PU 10K



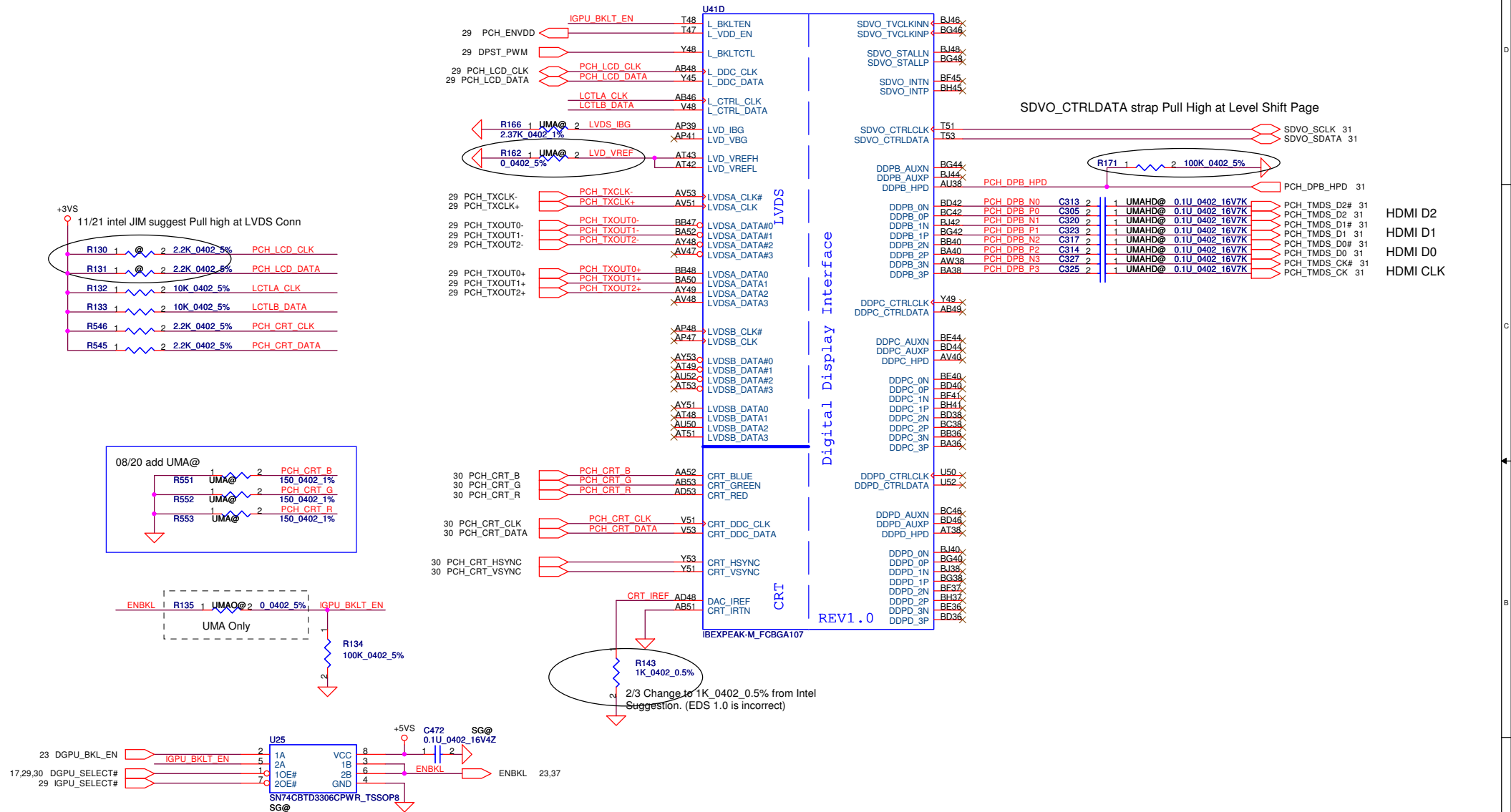
No used Integrated LAN,
connecting LAN_RST# to GND



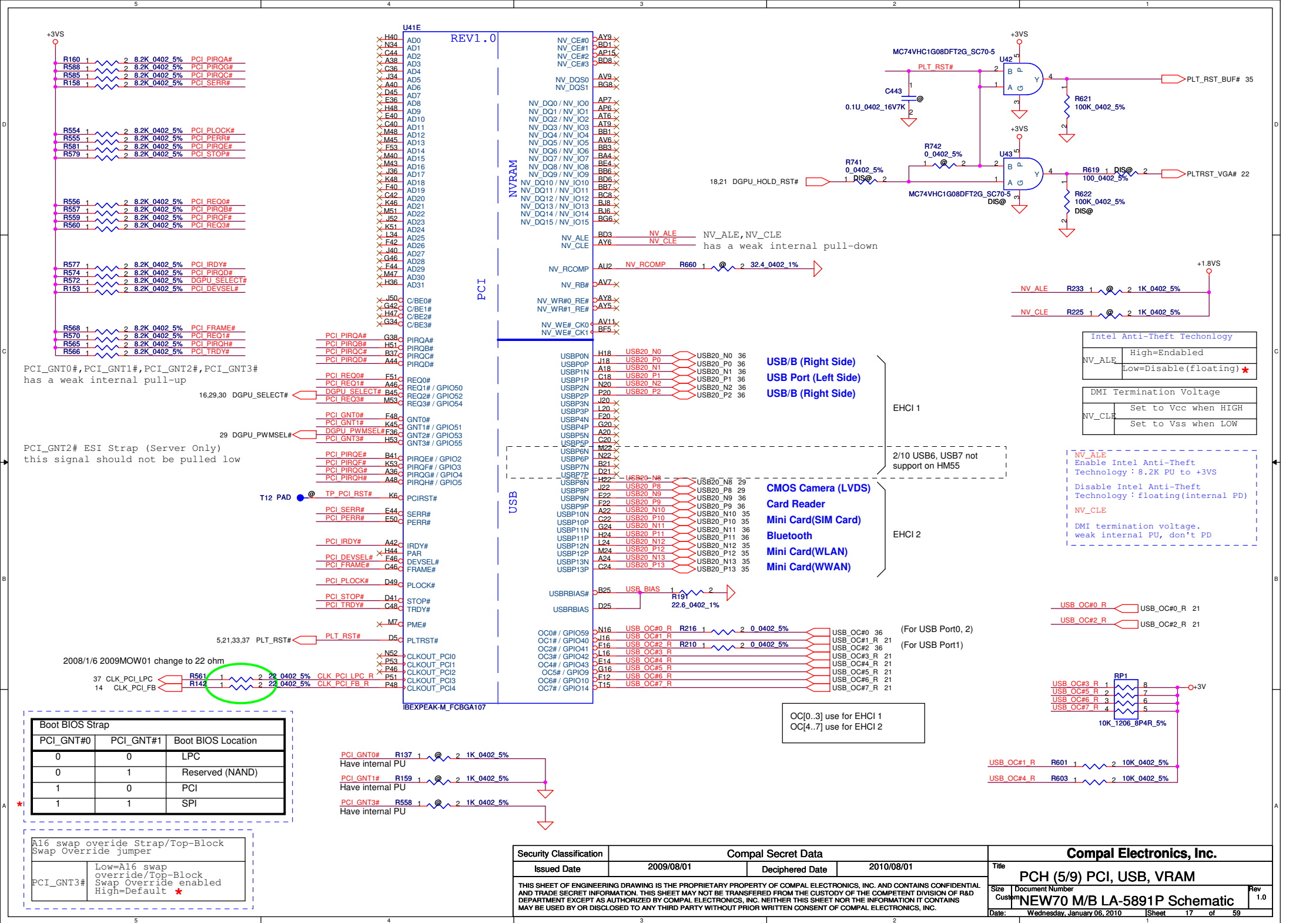
System Power Management

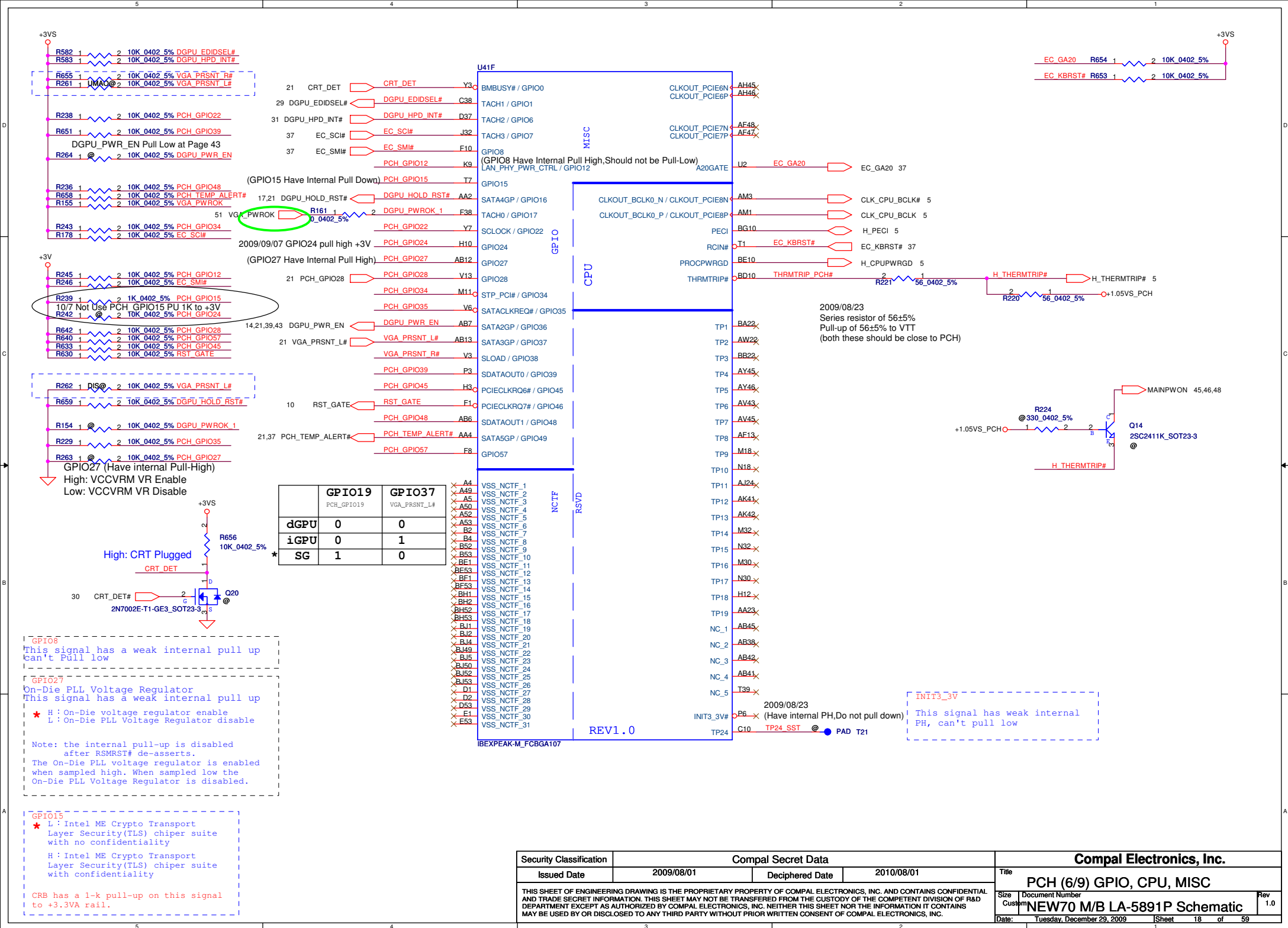


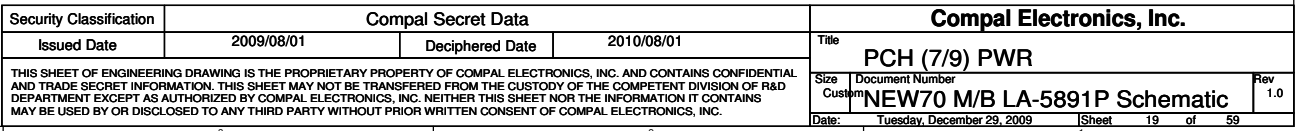
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Size	Custom	Document Number	NEW70 M/B LA-5891P Schematic	Rev	1.0
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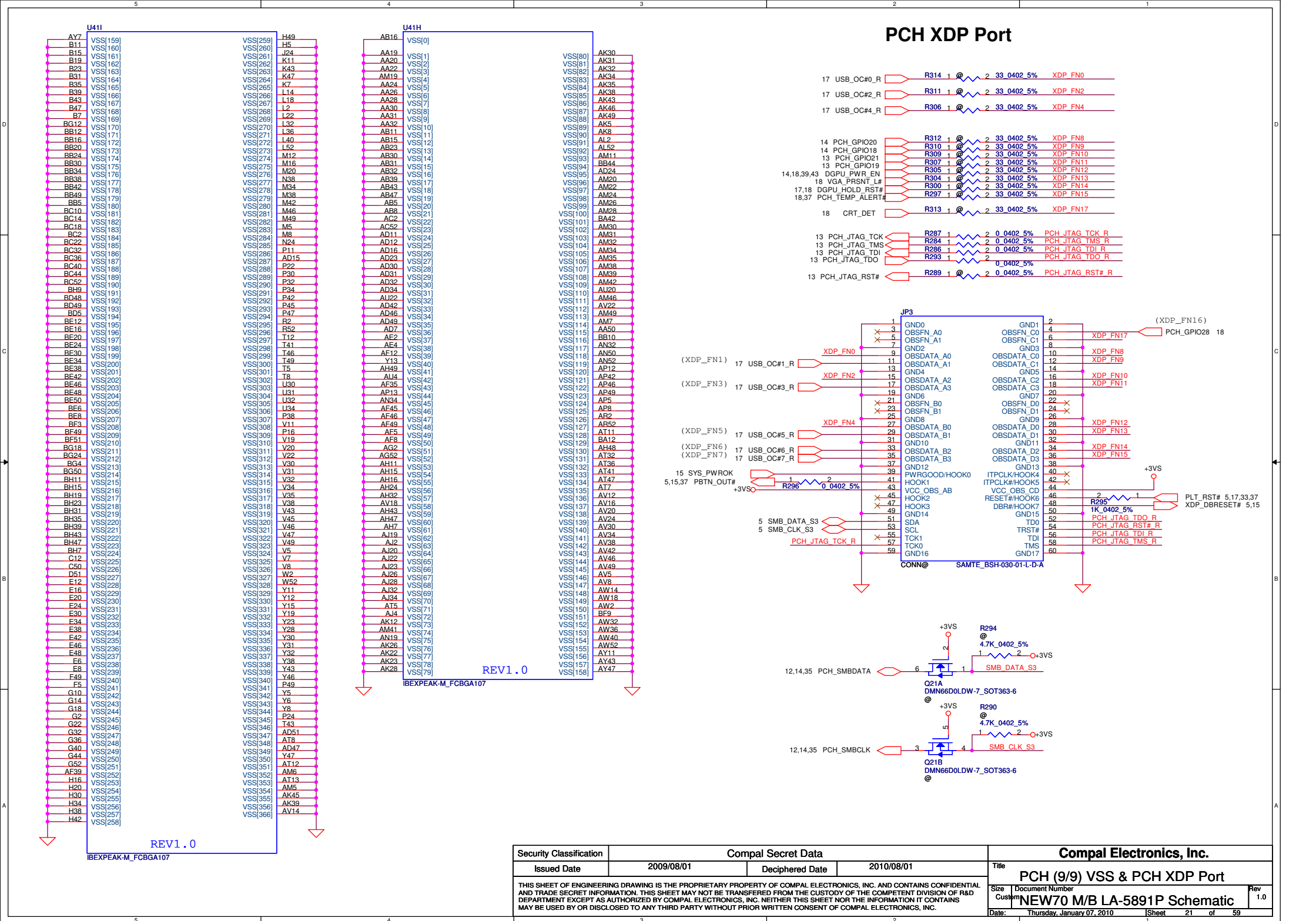


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Size		Document Number		Customer		NEW70 M/B LA-5891P Schematic		Date		Tuesday, December 29, 2009	
								Sheet		16 of 59	
								Rev		1.0	



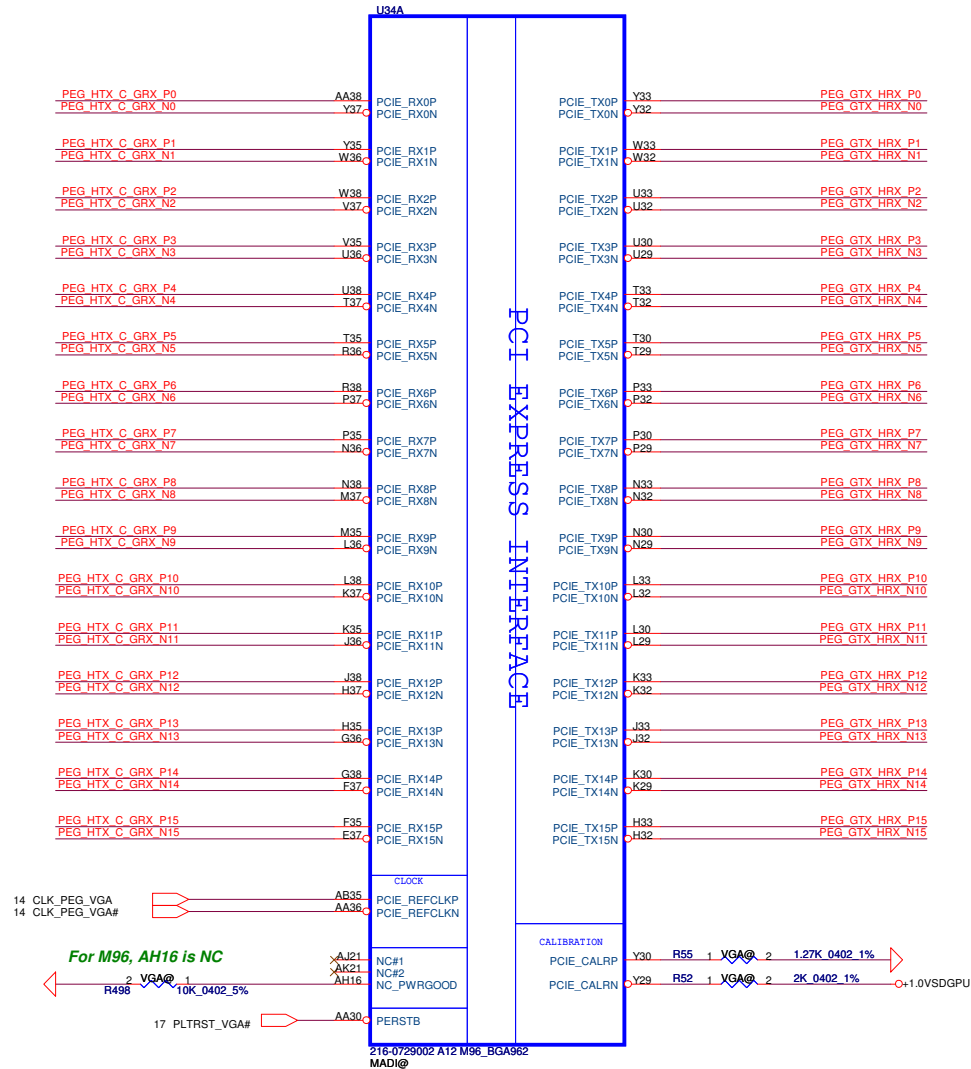






4 PEG GTX_HRX_N[0..15]
4 PEG GTX_HRX_P[0..15]
4 PEG HTX_C_GRX_N[0..15]
4 PEG HTX_C_GRX_P[0..15]

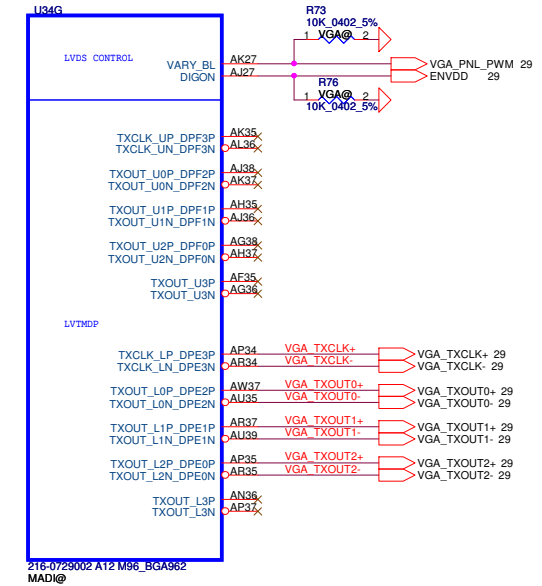
GFX PCIE LANE REVERSAL



Park XT P/N : SA00003M500 (S IC 216-0774009 A11 PARK XT S3 631P C38)

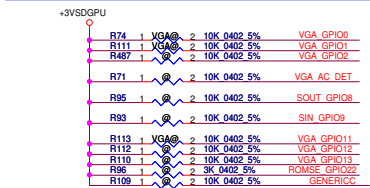
Madison Pro P/N : SA00003M300 (S IC 216-0772000 MADISON PRO FCBGA 0FA)

add for VB support.



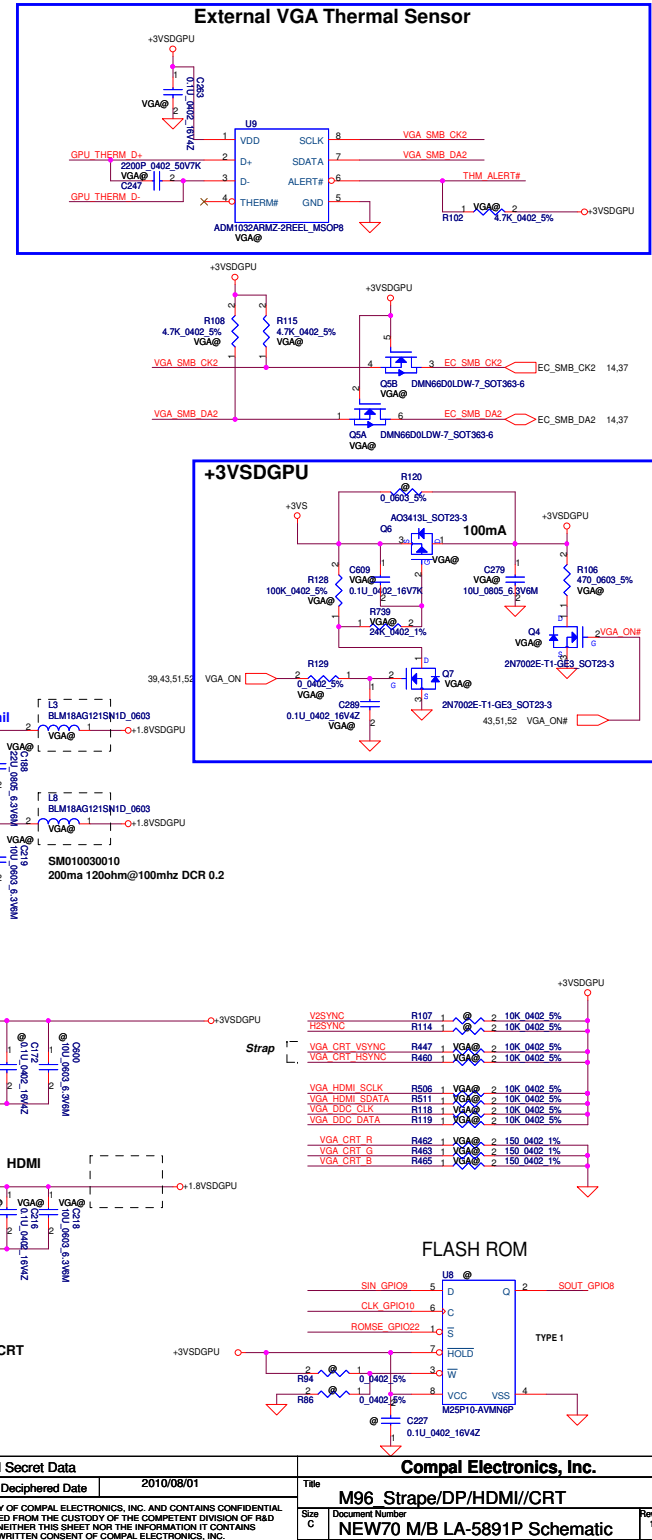
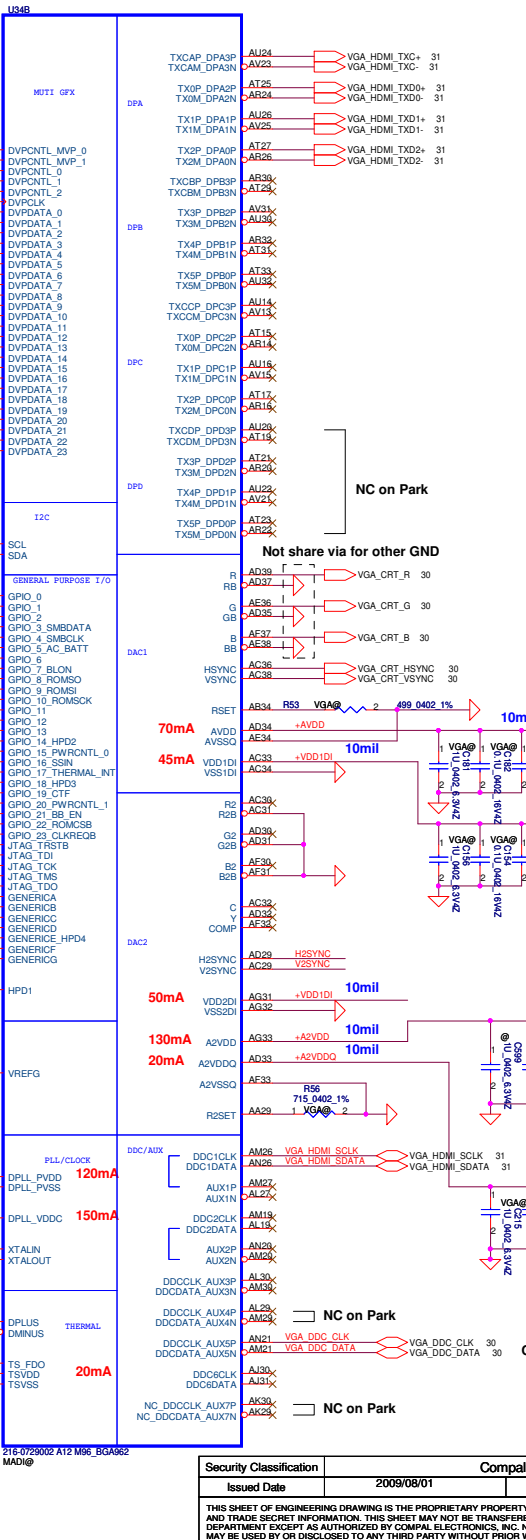
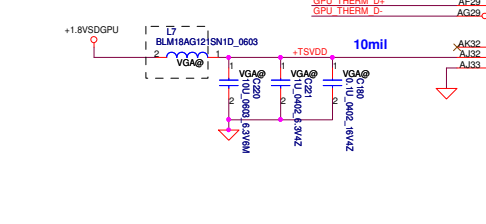
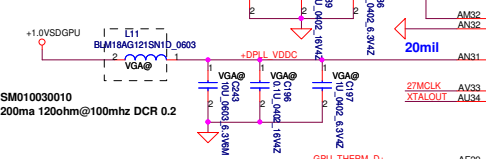
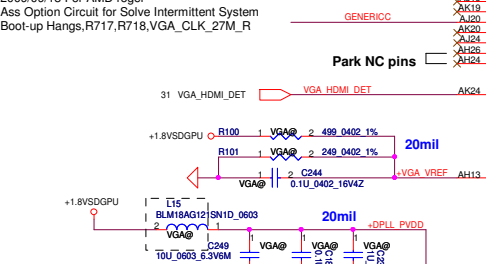
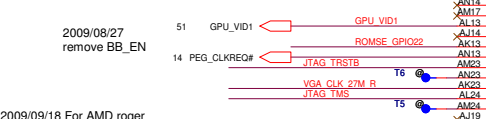
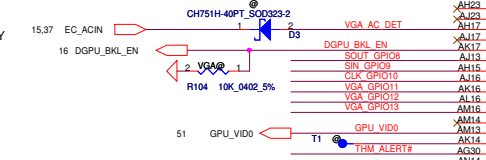
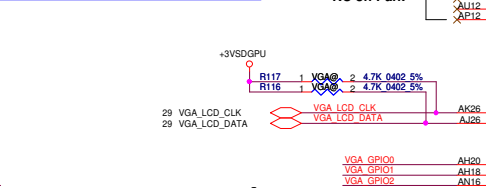
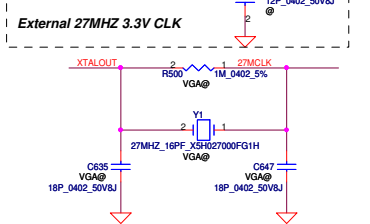
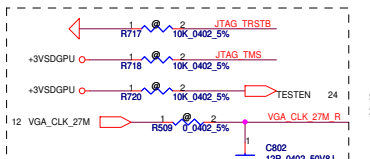
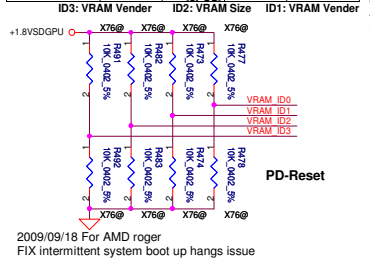
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Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	M96 PCIE / LVDS
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Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRNS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0): a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 001 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	Advertises the PCIe device as 2.5 GT/s capable at power-on 1: Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	



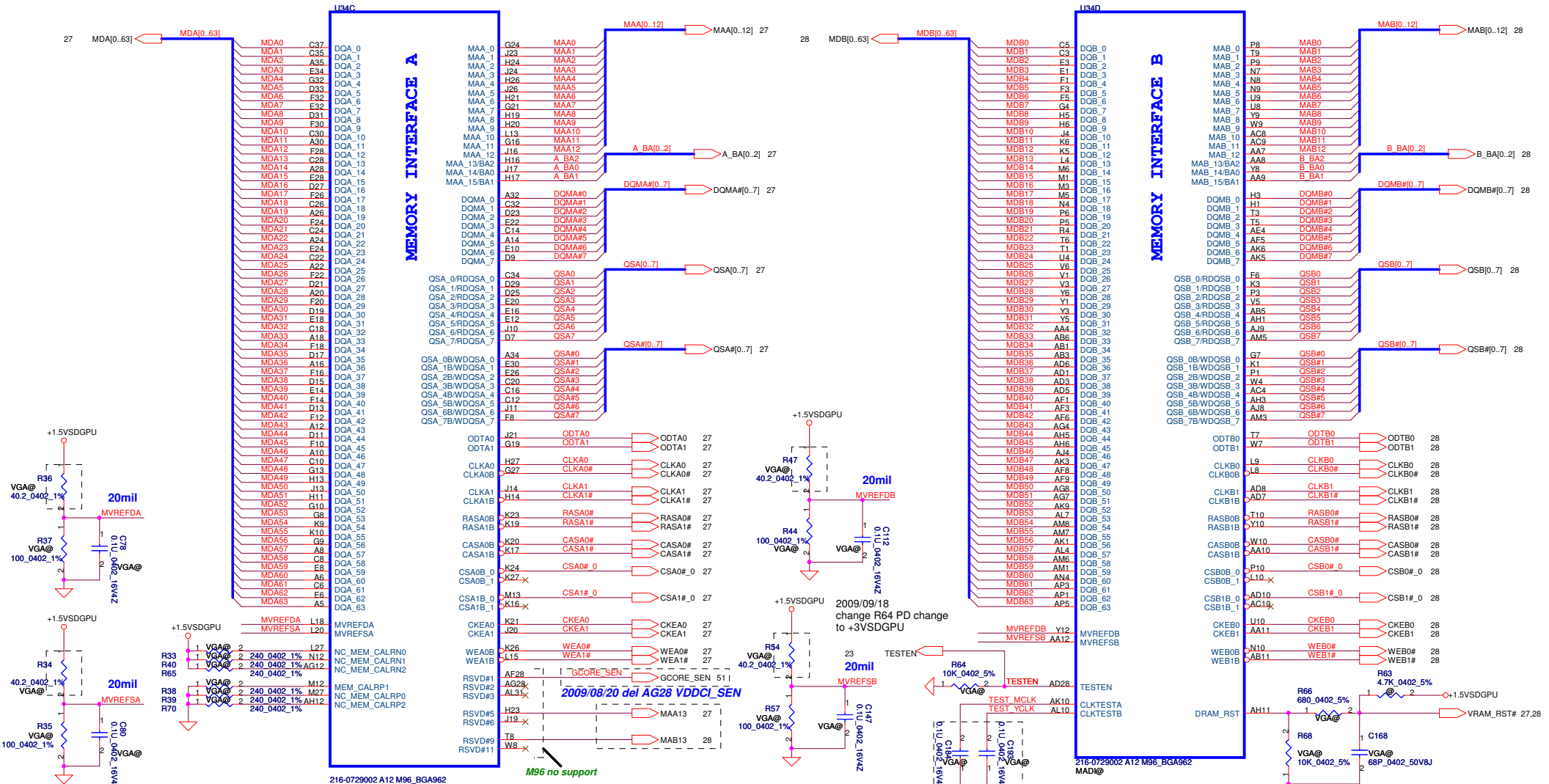
Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung	64Mx16	64Mx16	0	0
HYNIX	1	<4PCS>	0	0
AMD	1	<4PCS>	1	0

Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung	64Mx16	64Mx16	0	0
HYNIX	1	<4PCS>	0	0
AMD	1	<4PCS>	1	0



Security Classification	Compal Secret Data	Deciphered Date	2010/08/01
Issued Date	2009/08/01	Deciphered Date	2010/08/01
Title M96 Strape/DP/HDMI/CRT			
Size	Document Number	Date: Thursday, January 07, 2010 Sheet: 23 of 59	
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Park is single channel for memory (channel B only)



If use M96 upper resistor will change to 100ohm for MVREFDA/B and MVREFSA/B

In M97, Madison and Park, AF28 is FB_VDDC, AG28 is FB_VDDCI, AH29 is FB_GND. GCORE_SEN and FB_GND should route as differential pair Same as VDDCI_SEN and FB_GND

M96 no support

2009/08/20 del AG28 VDDCI_SEN

2009/09/18 change R64 PD change to +3VSDGPU

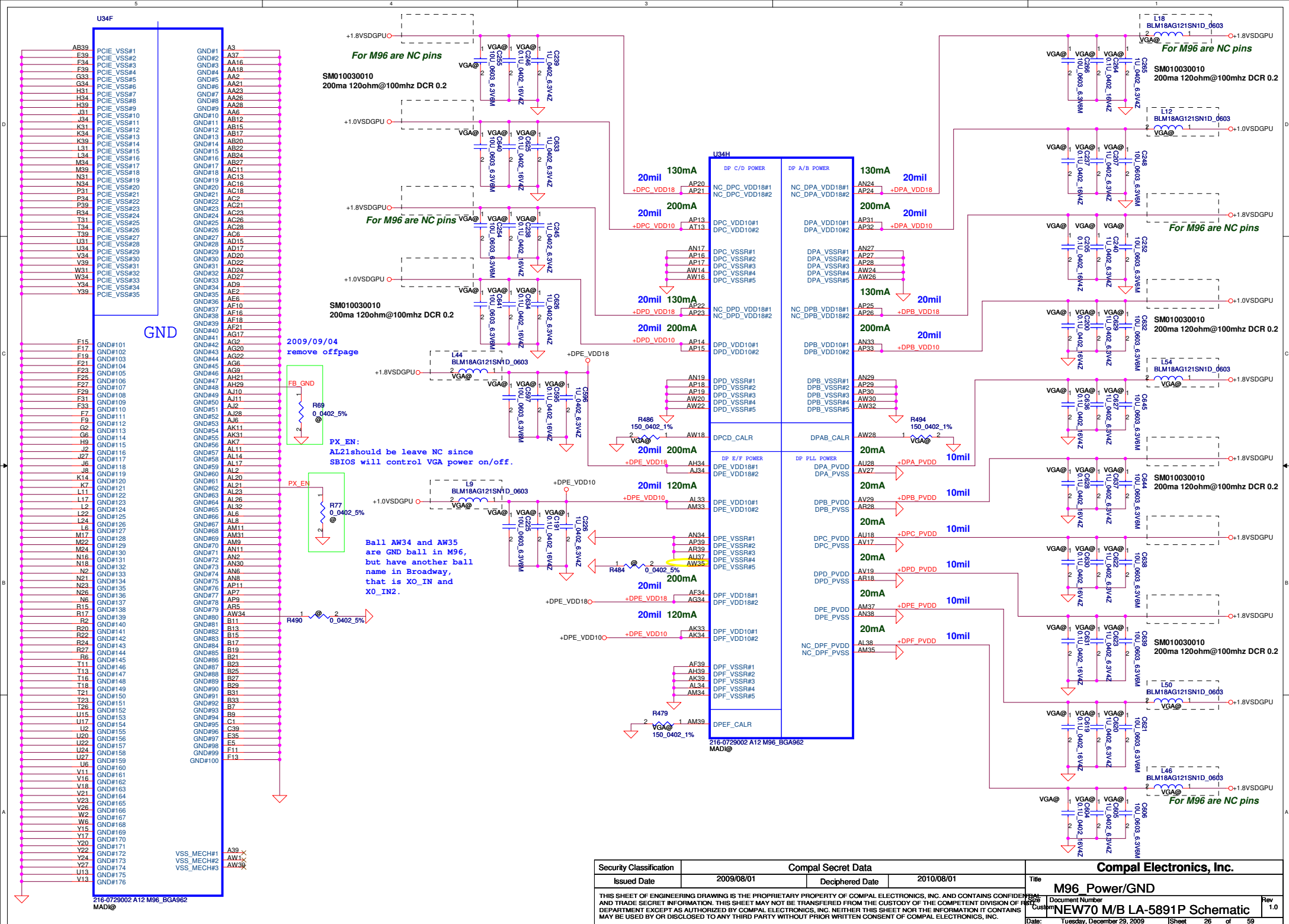
If use M96 upper resistor will change to 100ohm for MVREFDA/B and MVREFSA/B

M96 use 4.7K to PD directly.

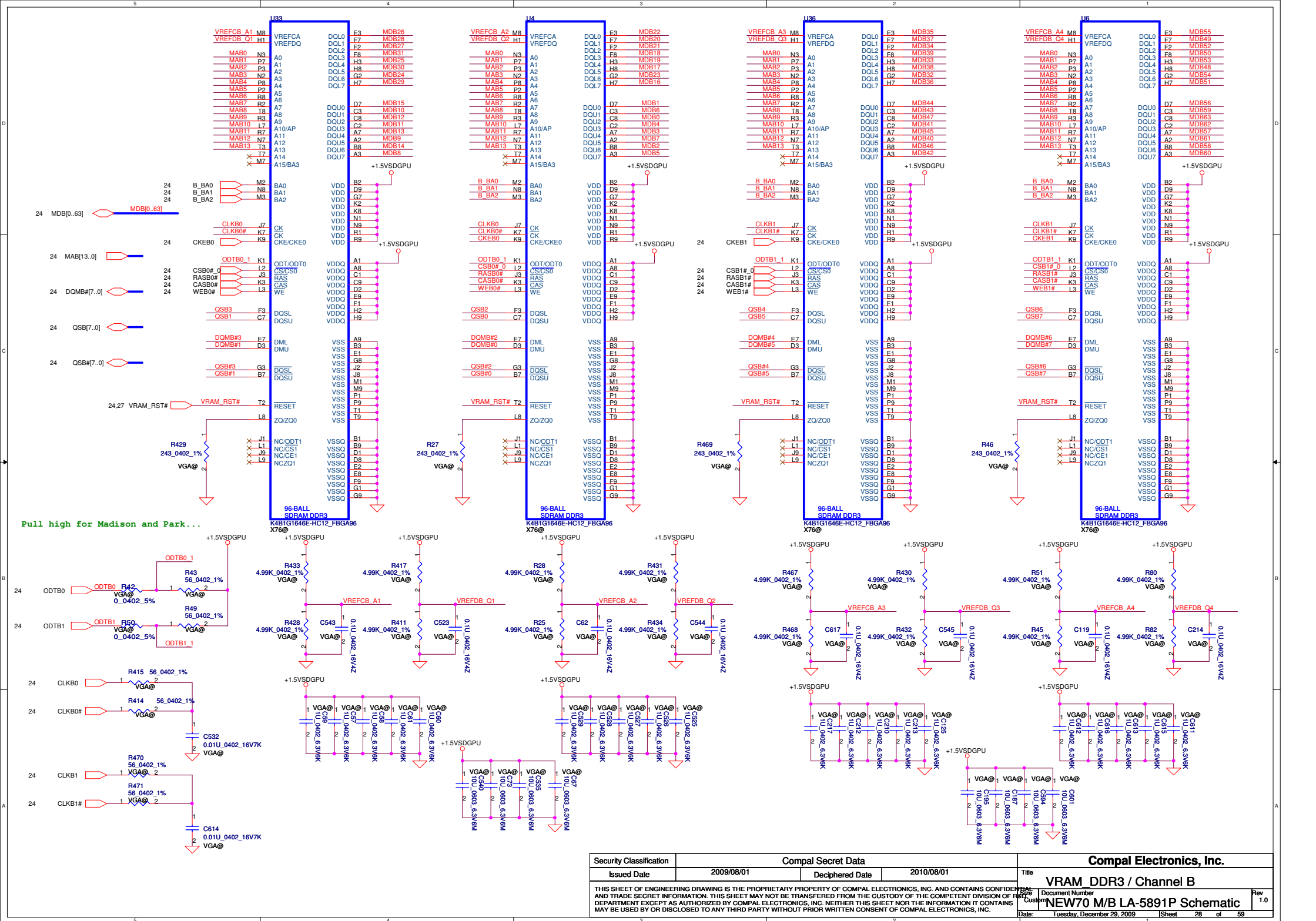
	M96	Broadway
R228	4.7k Ohm	10k Ohm
R159	SD028470180	SD028600080
R159	SD028600080	SD028600080
R159	SD028470180	SD028470180
C659	1000 pf	68 pf
C659	SD074102K80	SD071680J80



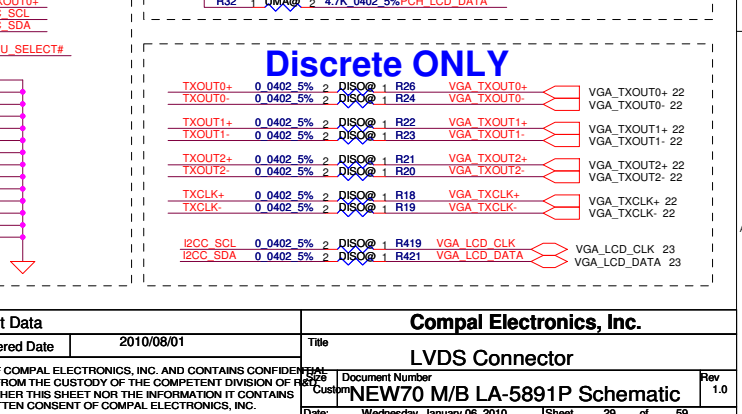
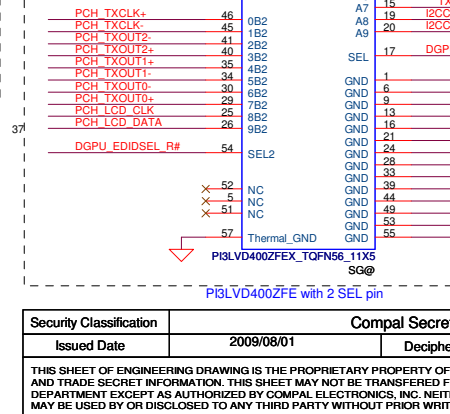
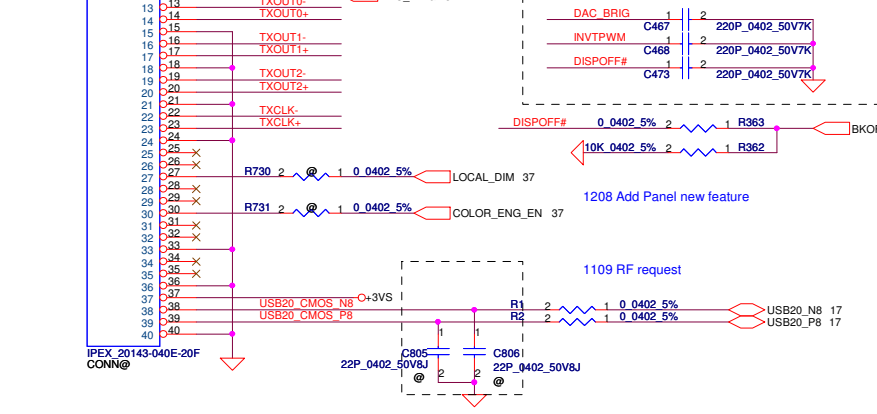
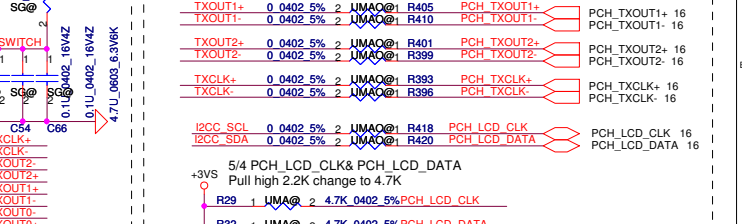
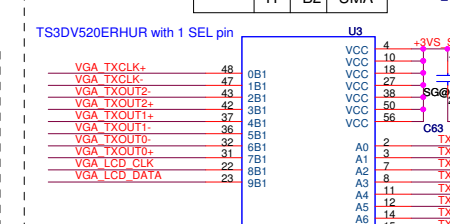
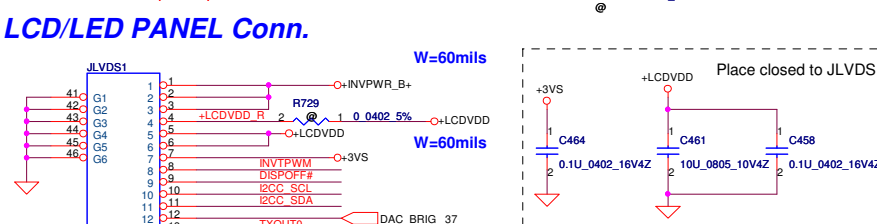
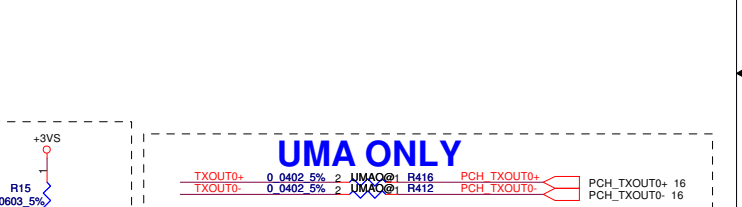
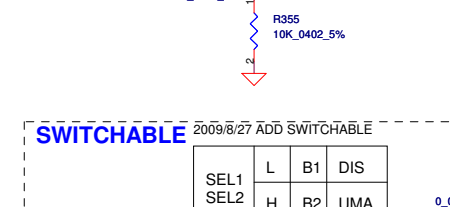
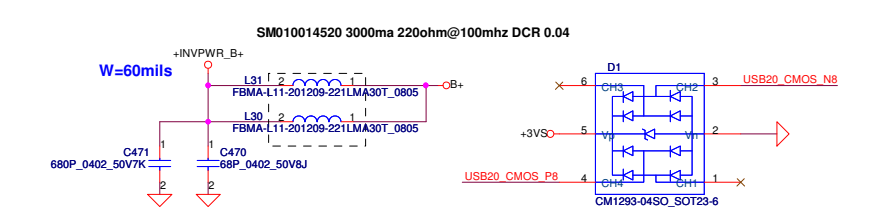
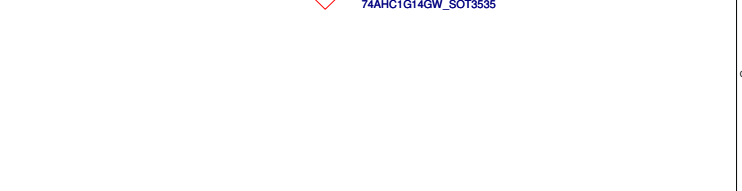
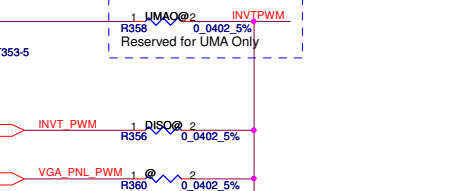
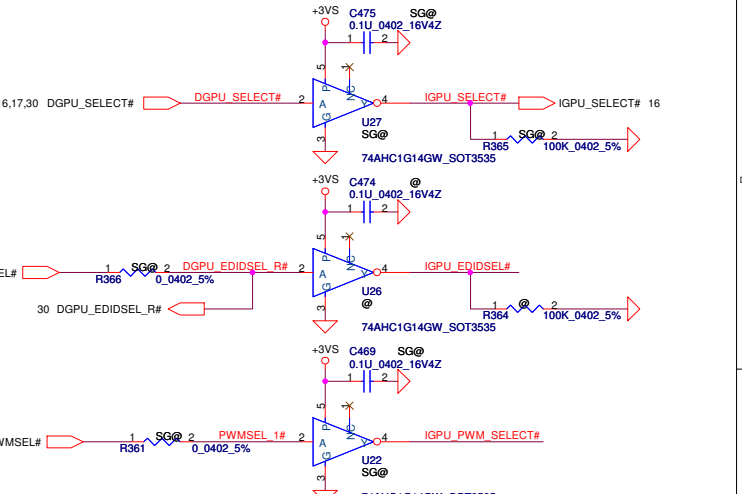
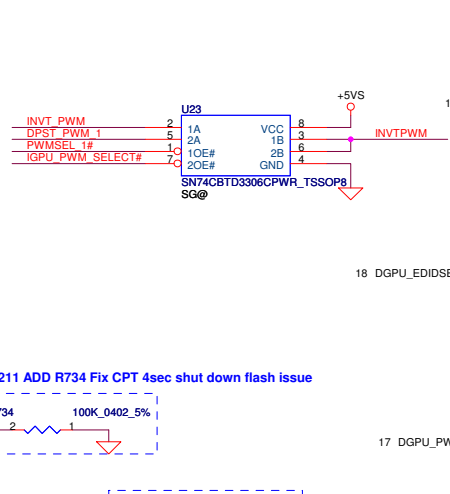
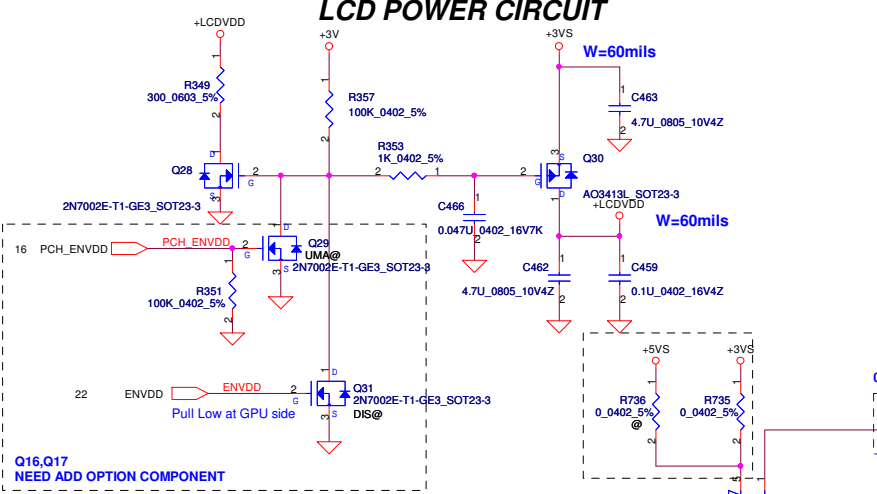
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Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	M96 Power/GND
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				NEW70 M/B LA-5891P Schematic		
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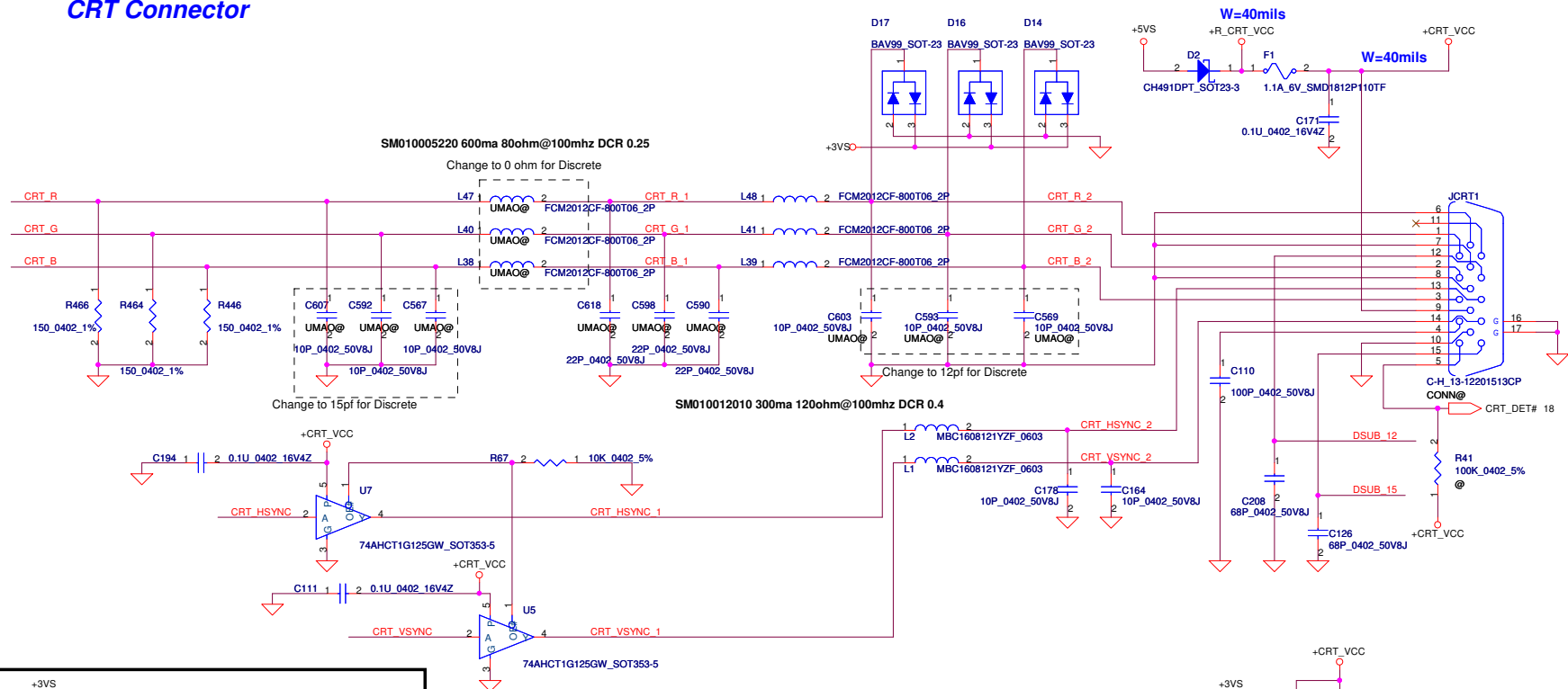


LCD POWER CIRCUIT



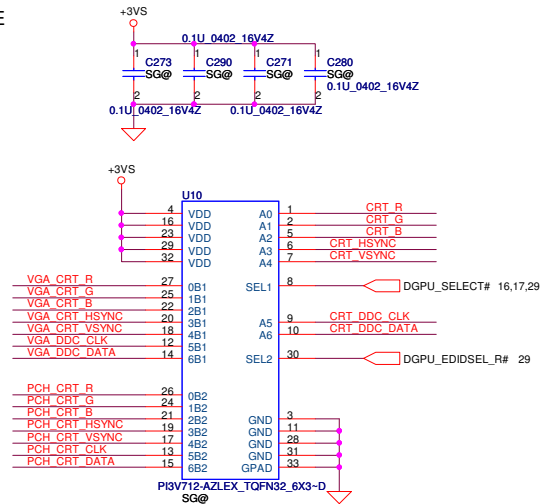
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Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title
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				1.0

CRT Connector



SWITCHABLE

2009/08/27



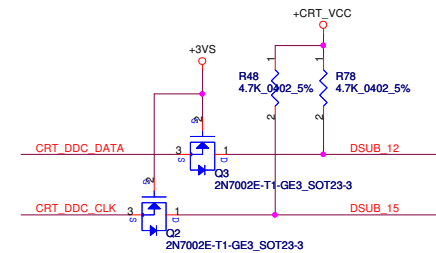
L	B1	DIS
H	B2	UMA

UMA only

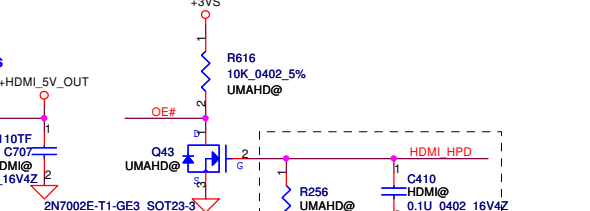
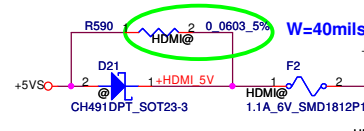
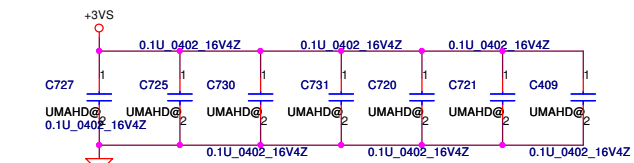
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16	PCH_CRT_G		PCH CRT G	R534	2	U4A00	@1	0	0.0402	5%	CRT G
16	PCH_CRT_B		PCH CRT B	R532	2	U4A00	@1	0	0.0402	5%	CRT B
16	PCH_CRT_HSYNC		PCH CRT HSYNC	R530	2	U4A00	@1	0	0.0402	5%	CRT HSYNC
16	PCH_CRT_VSYNC		PCH CRT VSYNC	R528	2	U4A00	@1	0	0.0402	5%	CRT VSYNC
16	PCH_CRT_CLK		PCH CRT CLK	R544	2	U4A00	@1	0	0.0402	5%	CRT DDC CLK
16	PCH_CRT_DATA		PCH CRT DATA	R543	2	U4A00	@1	0	0.0402	5%	CRT DDC DATA

Discrete only

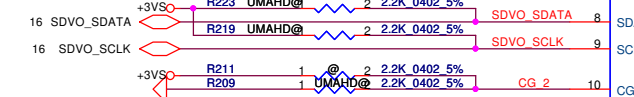
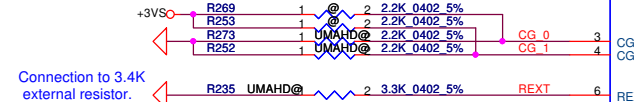
23	VGA_CRT_R		VGA CRT R	R537	2	DISC	1	0.0402	5%	CRT R
23	VGA_CRT_G		VGA CRT G	R535	2	DISC	1	0.0402	5%	CRT G
23	VGA_CRT_B		VGA CRT B	R536	2	DISC	1	0.0402	5%	CRT B
	VGA_CRT_HSYNC		VGA CRT HSYNC	R531	2	DISC	1	0.0402	5%	CRT HSYNC
	VGA_CRT_VSYNC		VGA CRT VSYNC	R529	2	DISC	1	0.0402	5%	CRT VSYNC
23	VGA_DDC_CLK		VGA DDC CLK	R527	2	DISC	1	0.0402	5%	CRT DDC CLK
23	VGA_DDC_DATA		VGA DDC DATA	R526	2	DISC	1	0.0402	5%	CRT DDC DATA



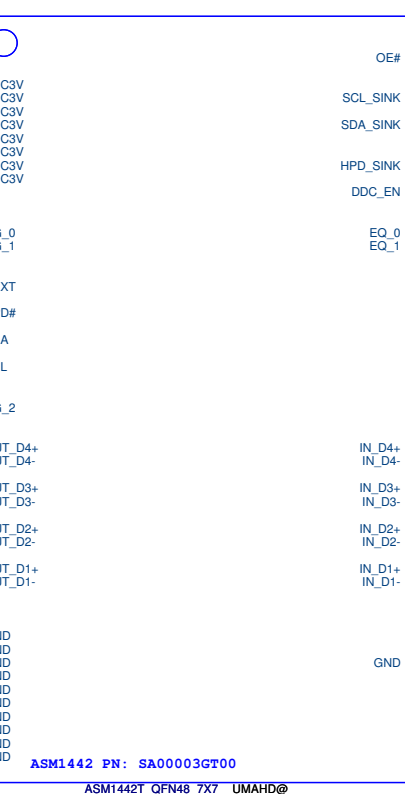
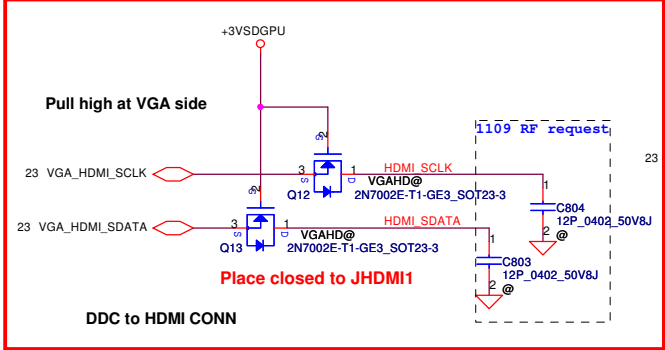
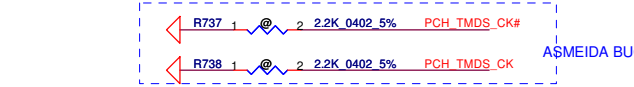
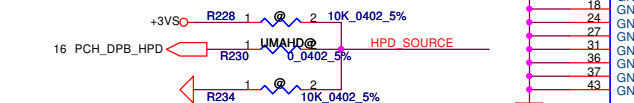
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								Document Number		Rev	
								NEW70 M/B LA-5891P Schematic		1.0	
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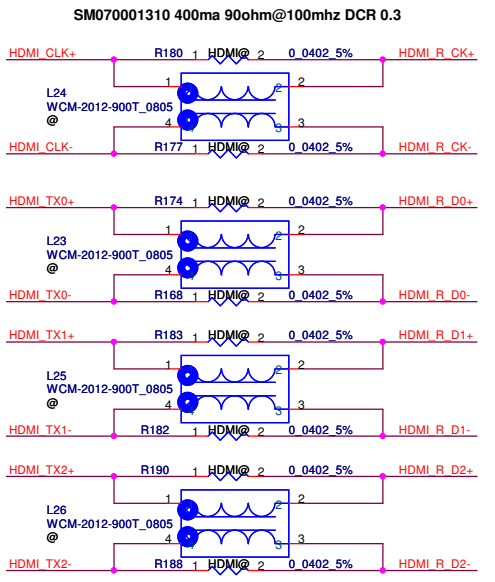
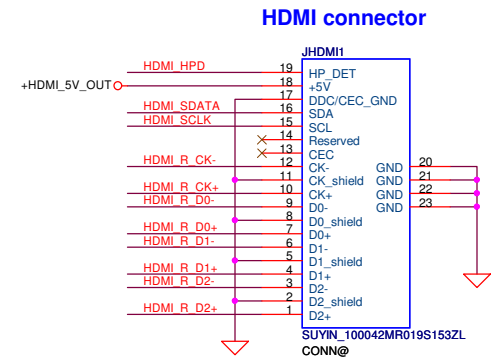
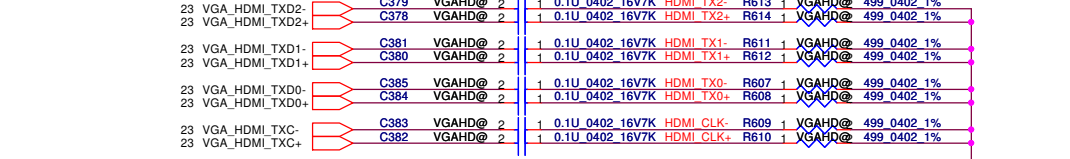
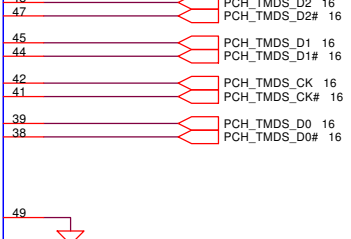
Option	UMAHD@	VGAHD@	HDMI@	@	SG@
UMA	V	X	V	X	X
VGA	X	V	V	X	X
SG	X	V	V	X	V
NO HDMI	X	X	X	X	X



CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

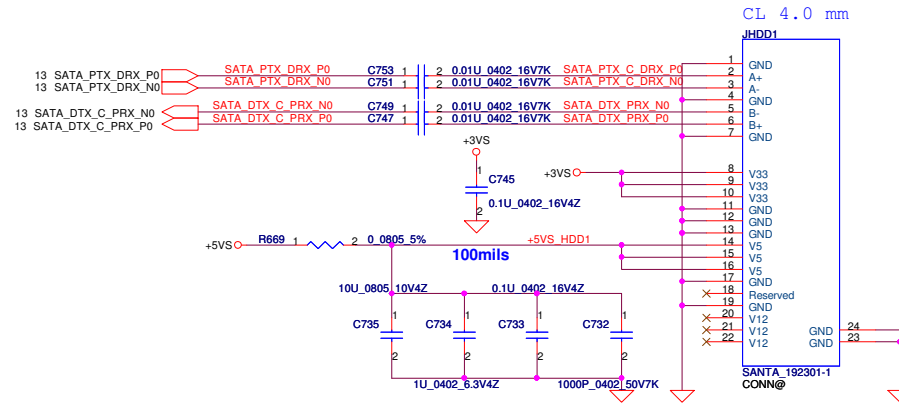


EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

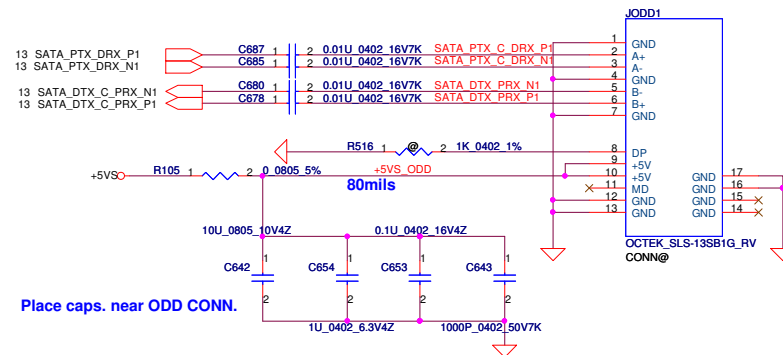


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						Size		Document Number		Rev	
						Custom		NEW70 M/B LA-5891P Schematic		1.0	
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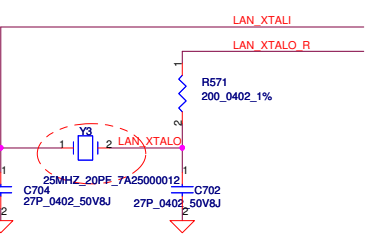
SATA HDD1 Conn.



SATA ODD Conn.

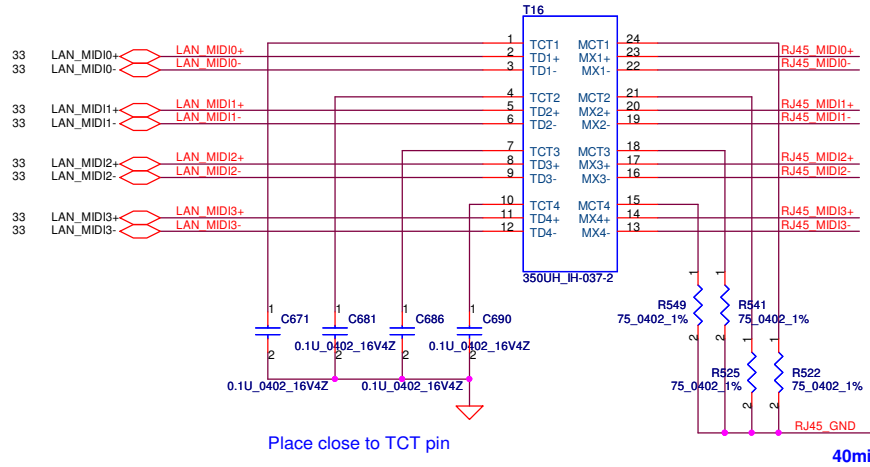


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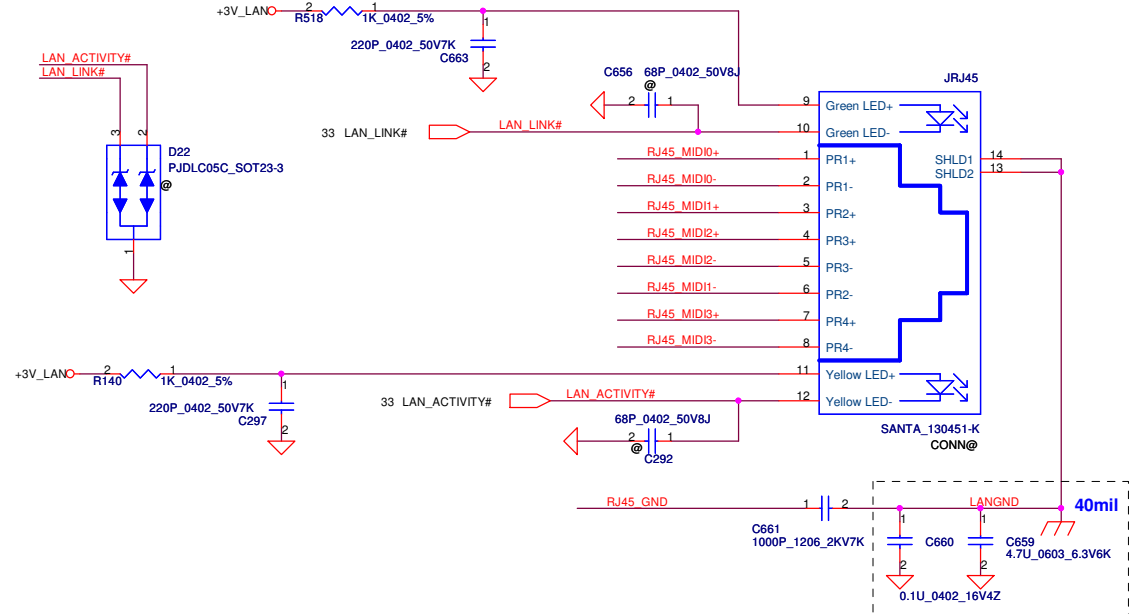
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LAN Connector

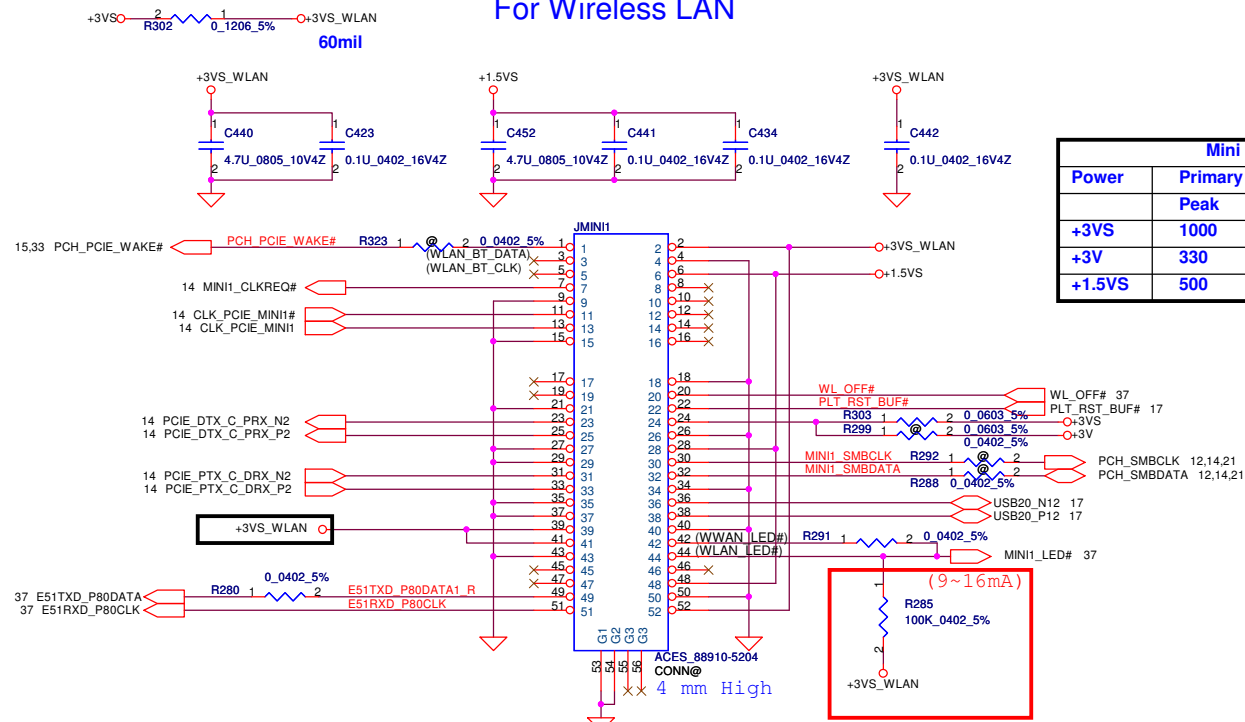


BOTH HAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG: S X'FORM_ IH-160 LAN, SP050006F00

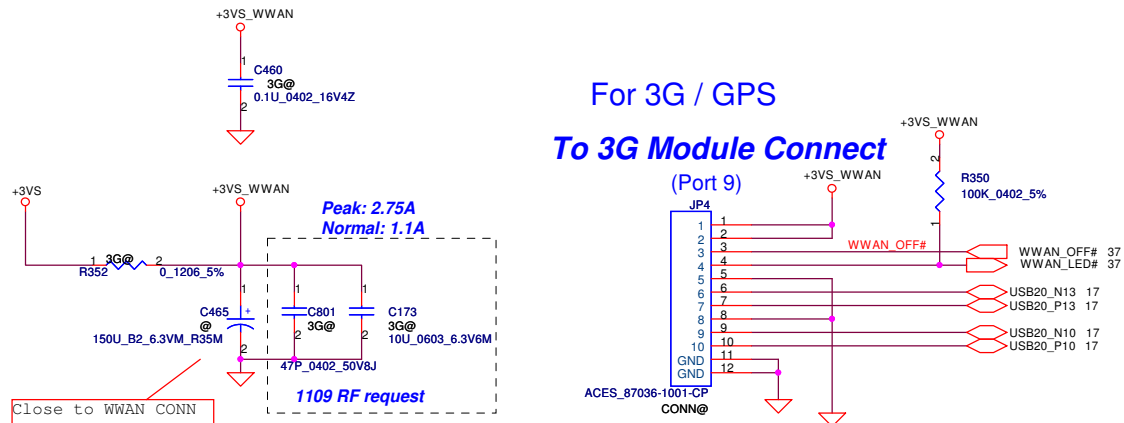


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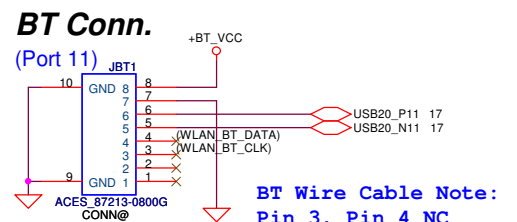
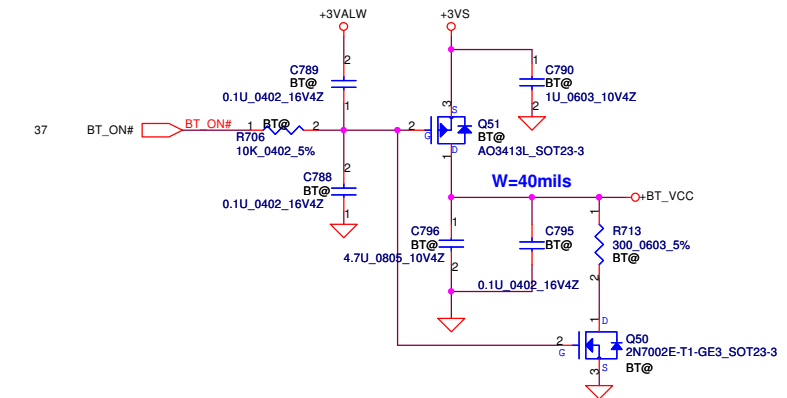
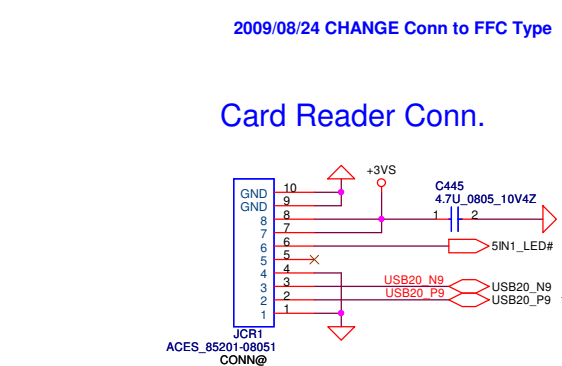
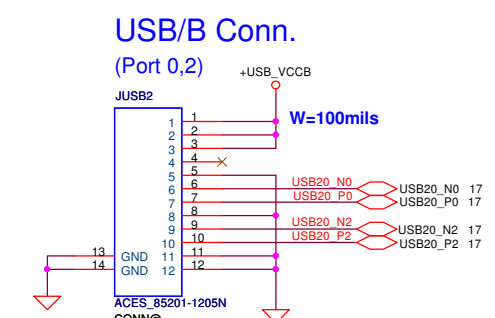
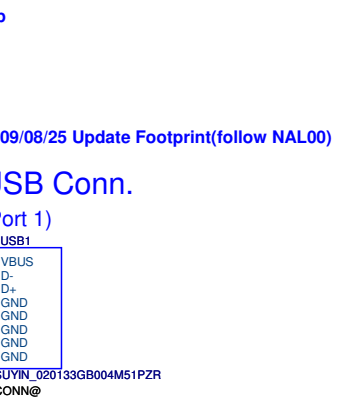
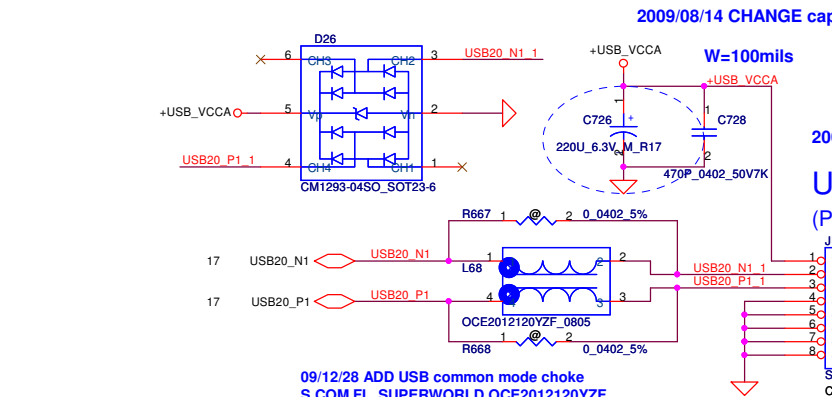
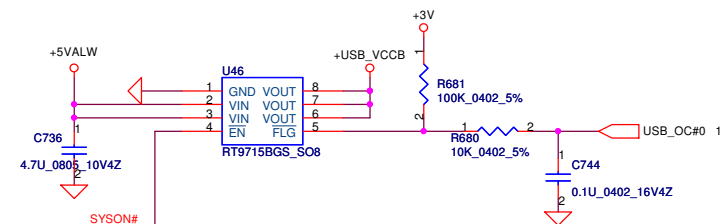
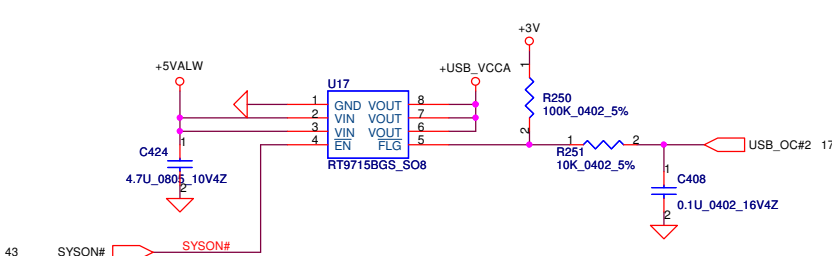
For Wireless LAN



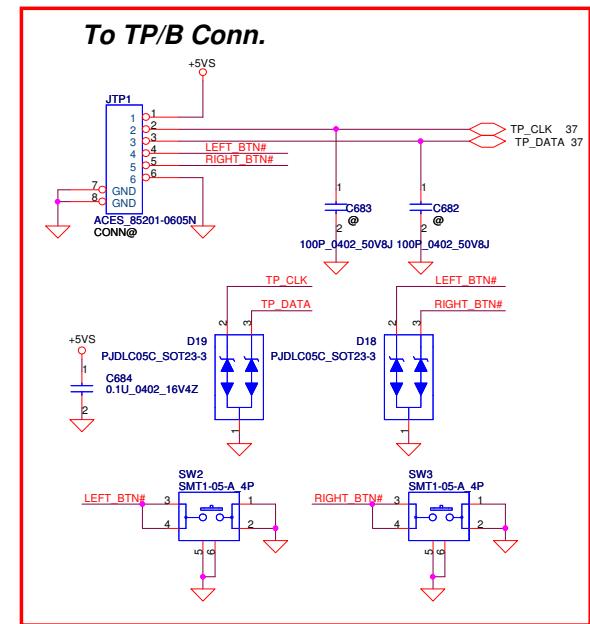
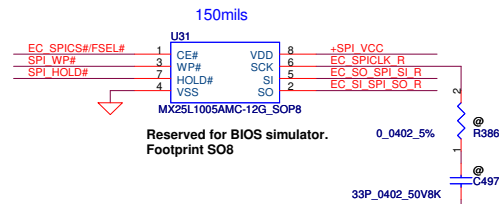
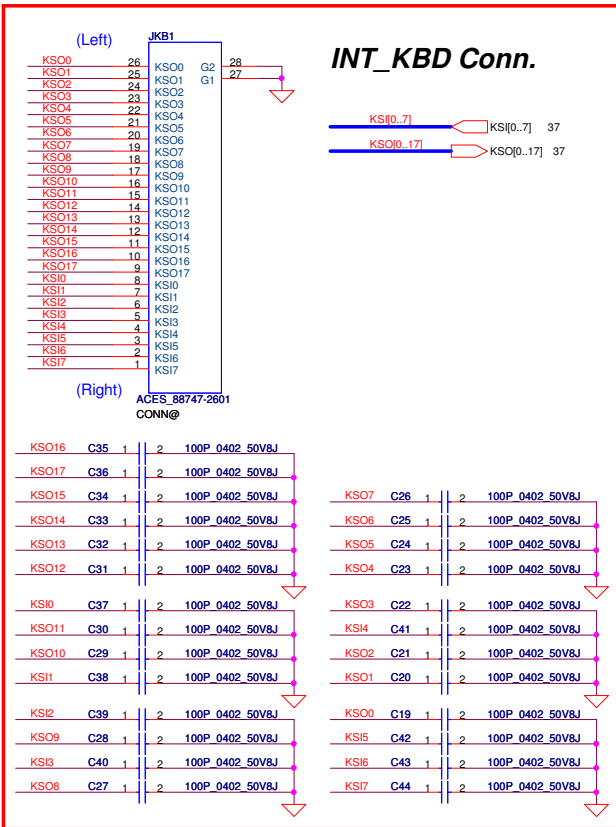
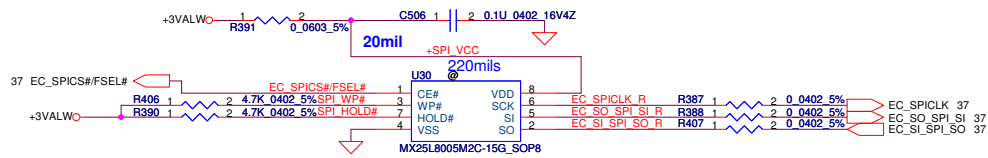
For 3G / GPS To 3G Module Connect



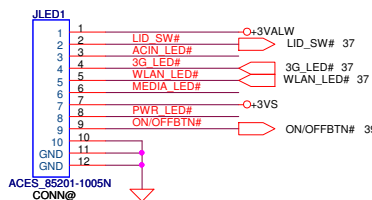
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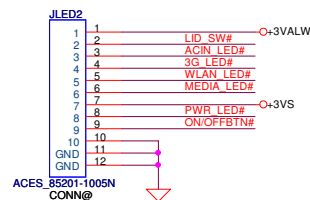
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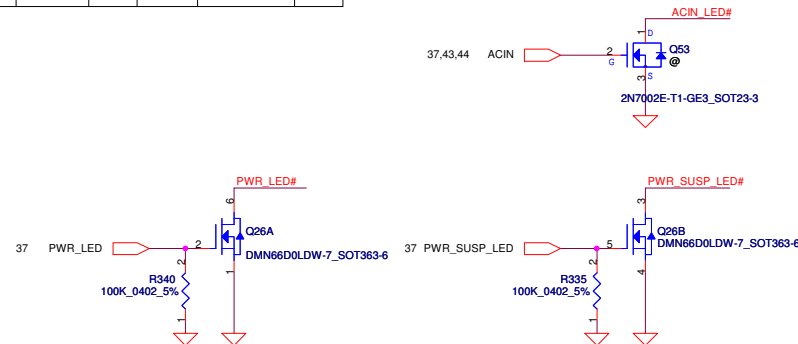
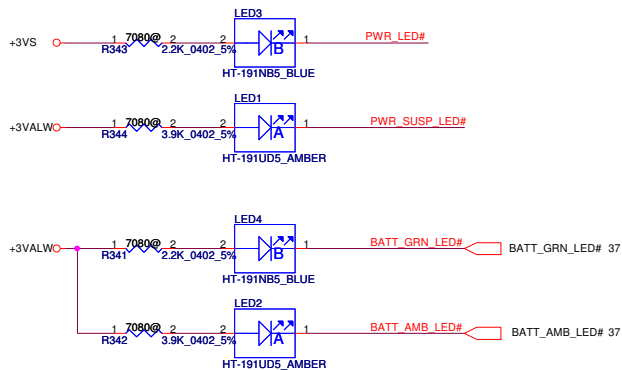
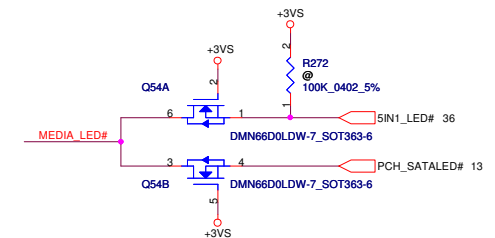
LED/B RIGHT



LED/B LEFT



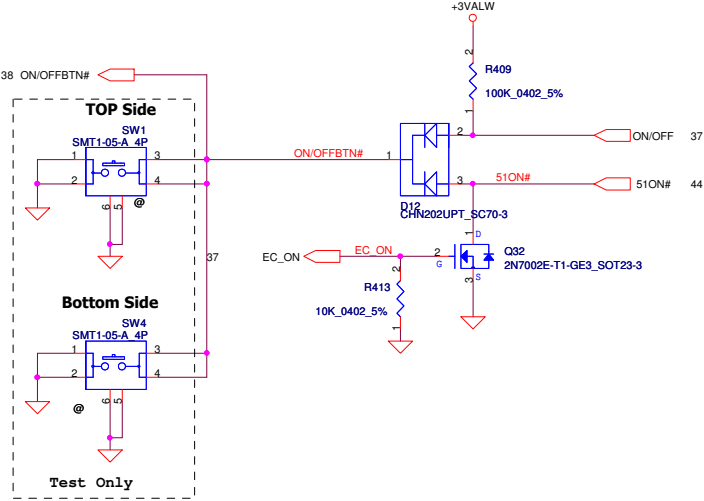
LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		



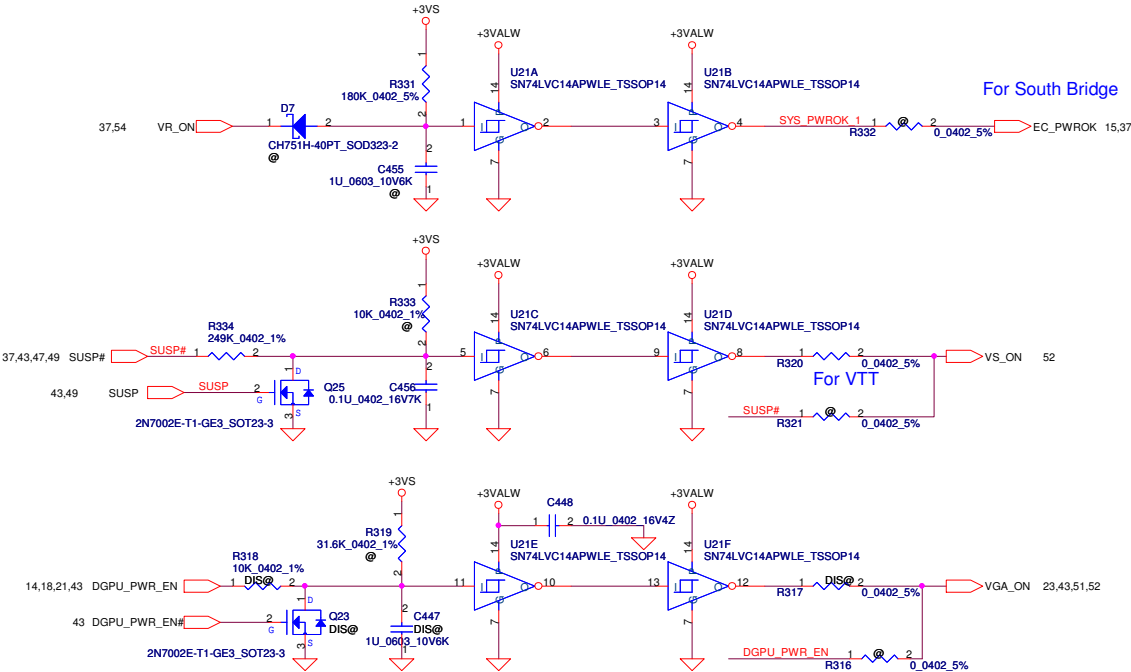
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Power Button

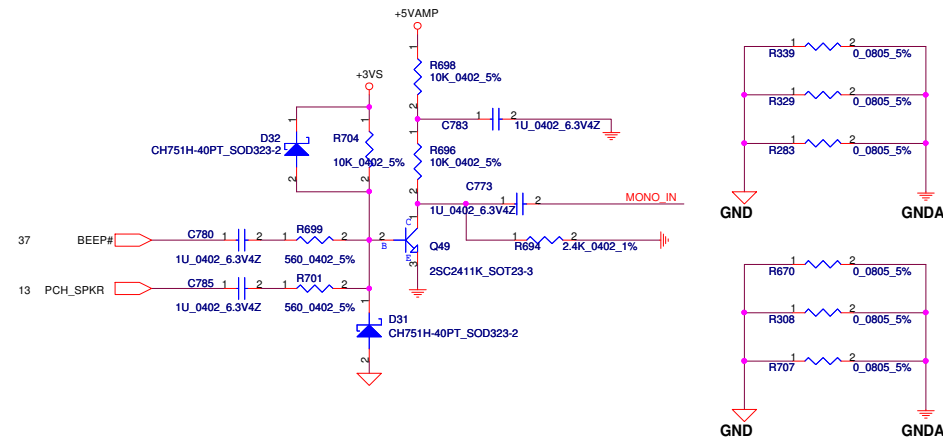
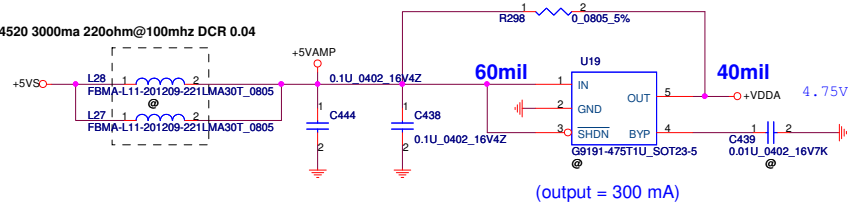
ON/OFF switch



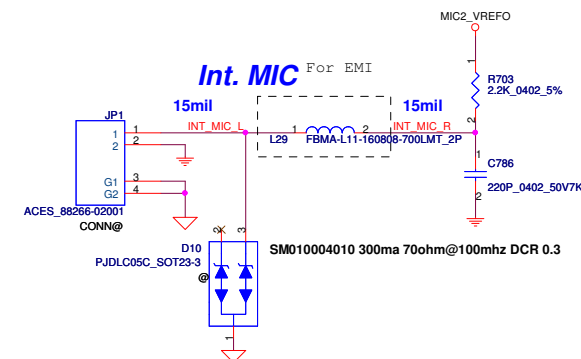
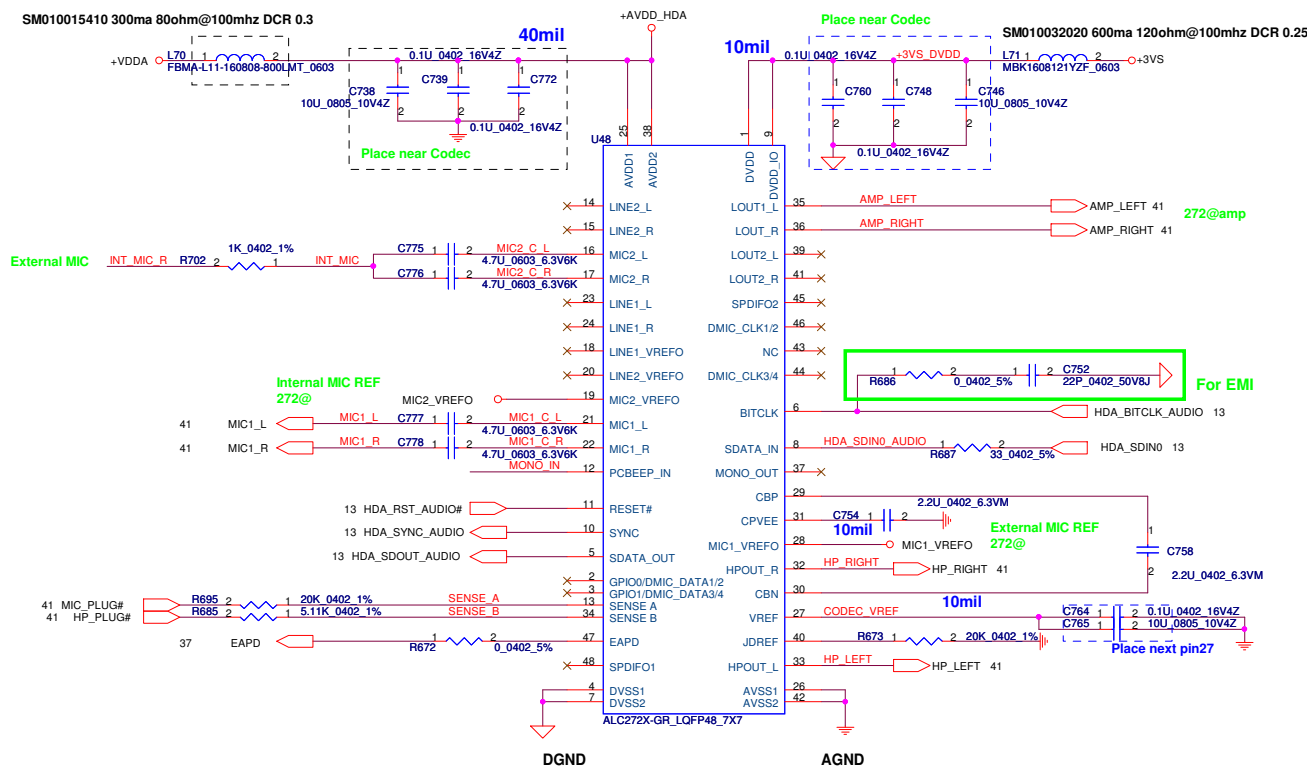
Power ON Circuit



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								2010/08/01			
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				Document Number				NEW70 M/B LA-5891P Schematic			
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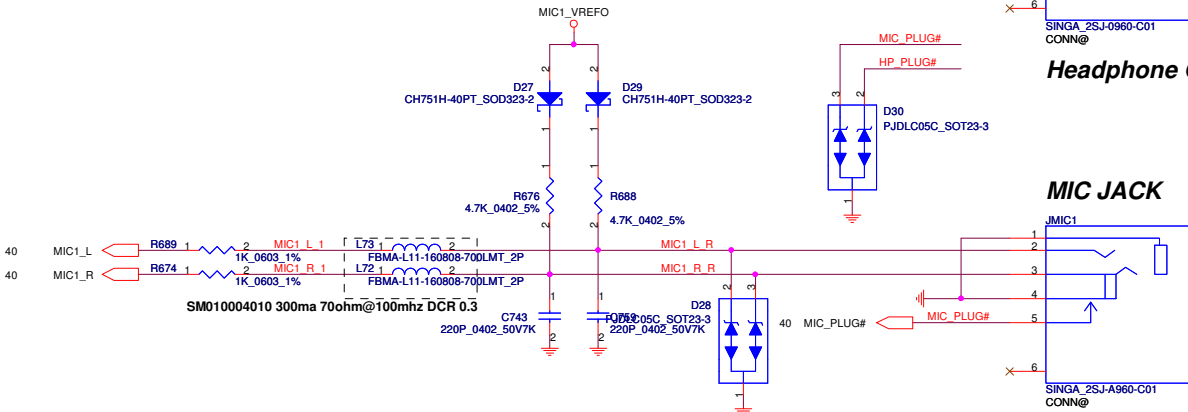
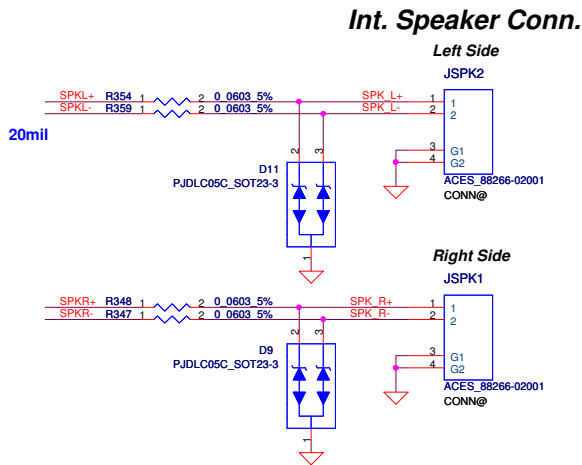
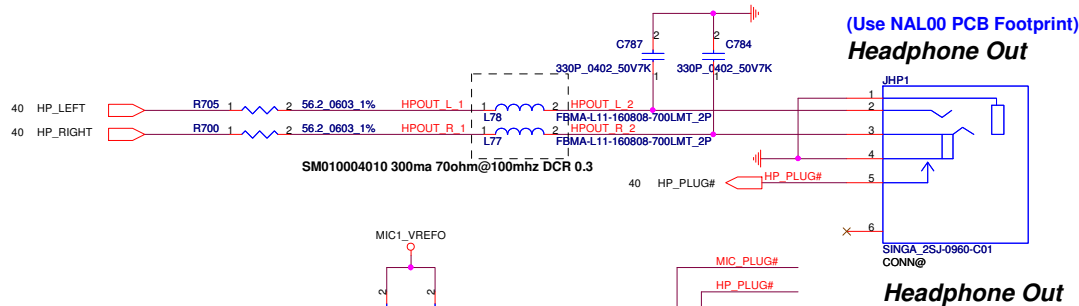
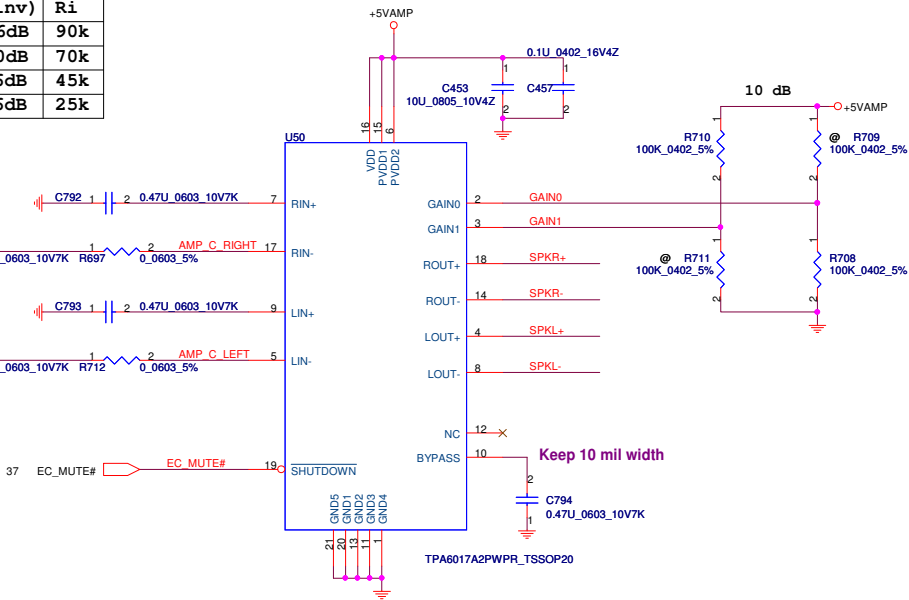


SM010015410 300ma 80ohm@100mhz DCR 0.3



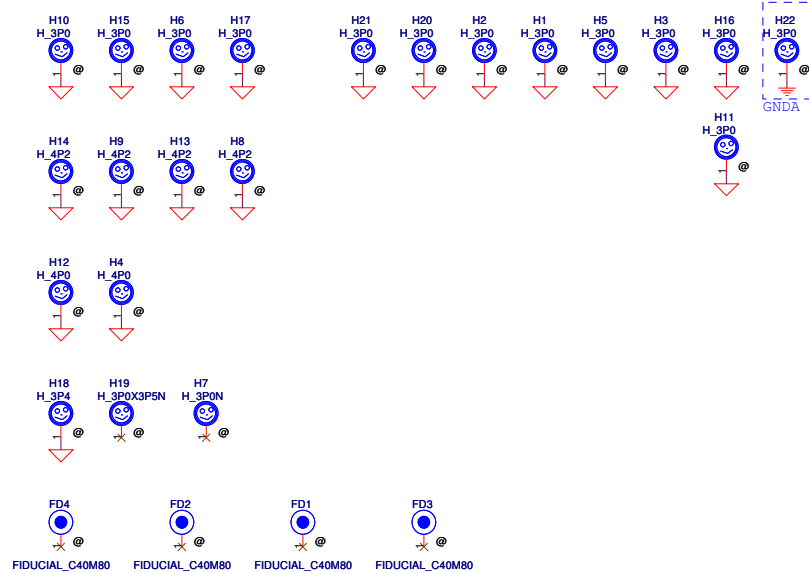
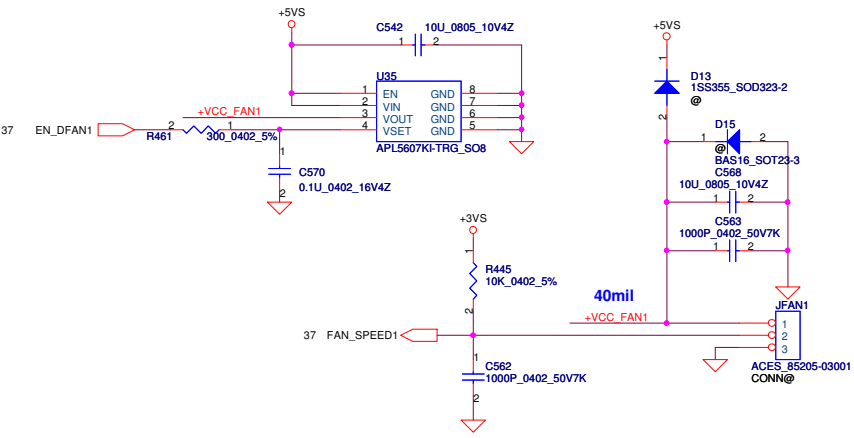
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Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title	HD Audio Codec ALC272X
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GAIN0	GAIN1	AV (inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



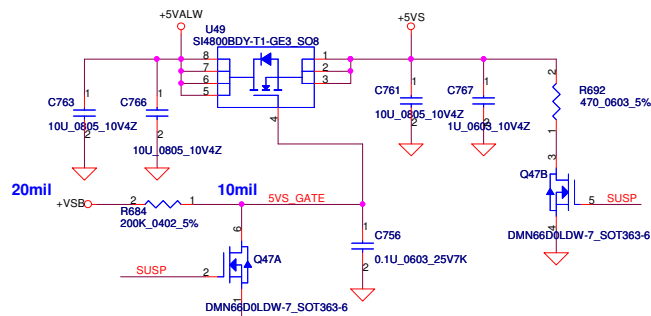
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2008/08/10				Title			
Deciphered Date				2010/08/01				Amplifier & Audio Jack			
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Document Number				NEW70 M/B LA-5891P Schematic				Rev 1.0			
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FAN1 Conn

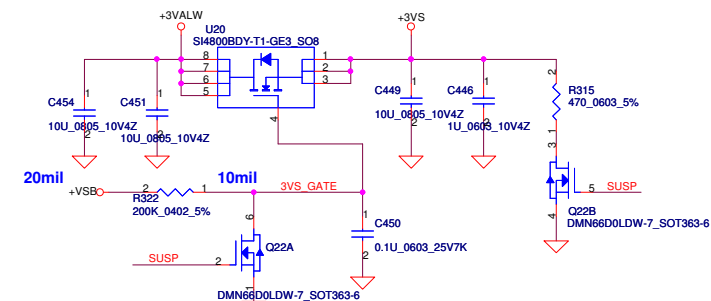


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				FAN & Screw Hole			
				Document Number			
				NEW70 M/B LA-5891P Schematic			
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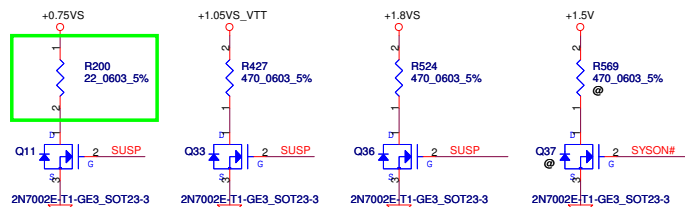
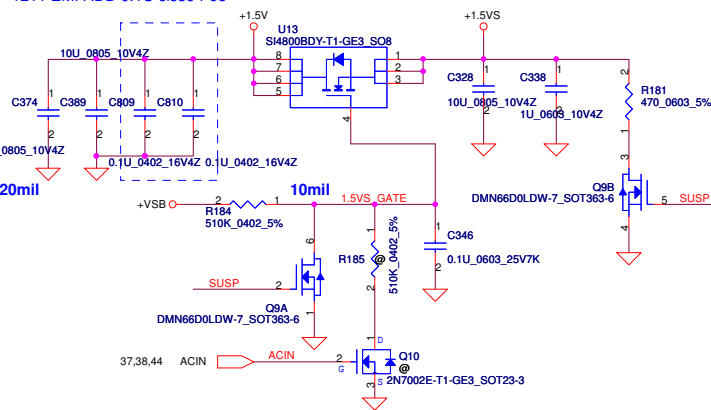
+5VALW TO +5VS



+3VALW TO +3VS

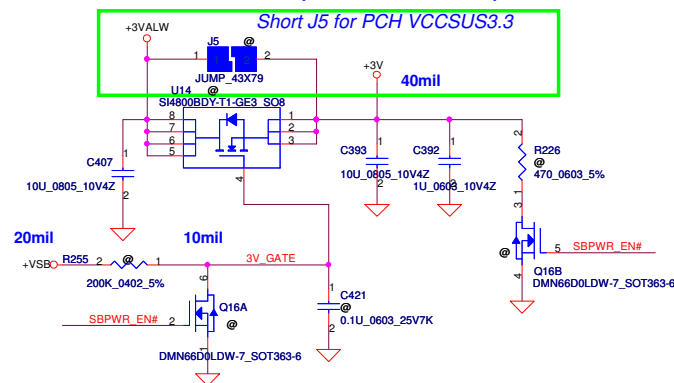


+1.5V to +1.5VS

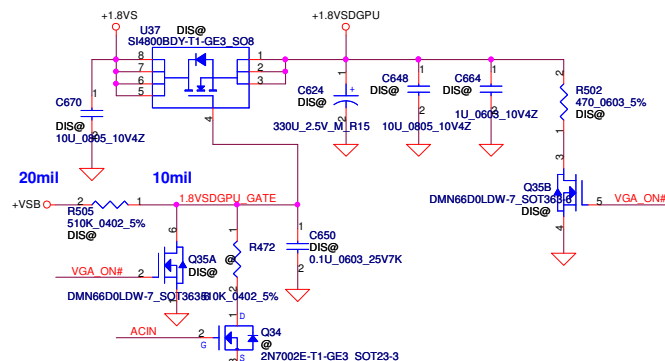


2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

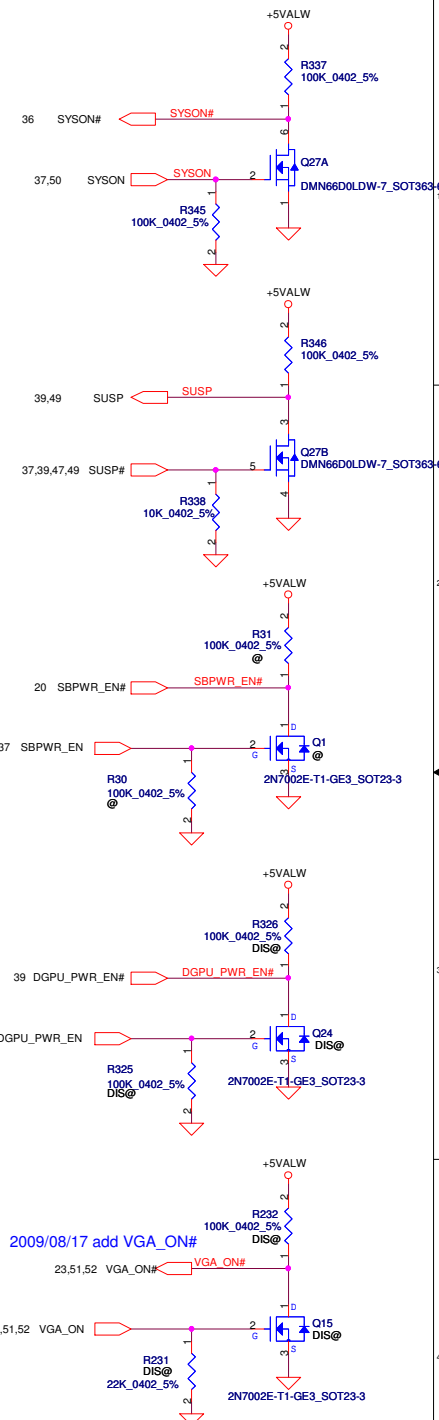
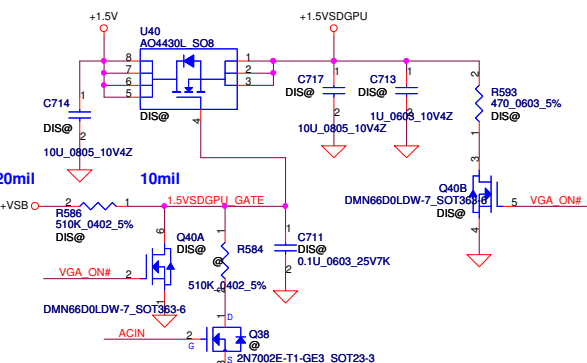
+3VALW TO +3V(PCH AUX Power)



+1.8VS to +1.8VSDGPU for GPU

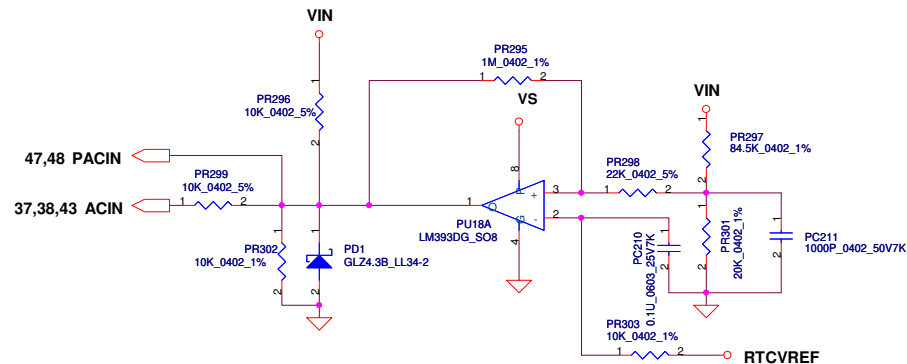
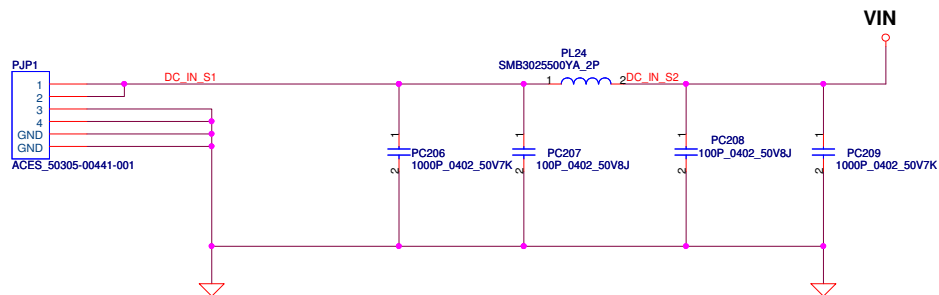


+1.5V to +1.5VSDGPU for GPU



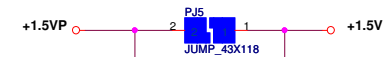
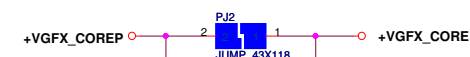
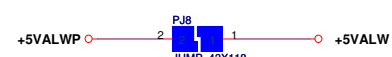
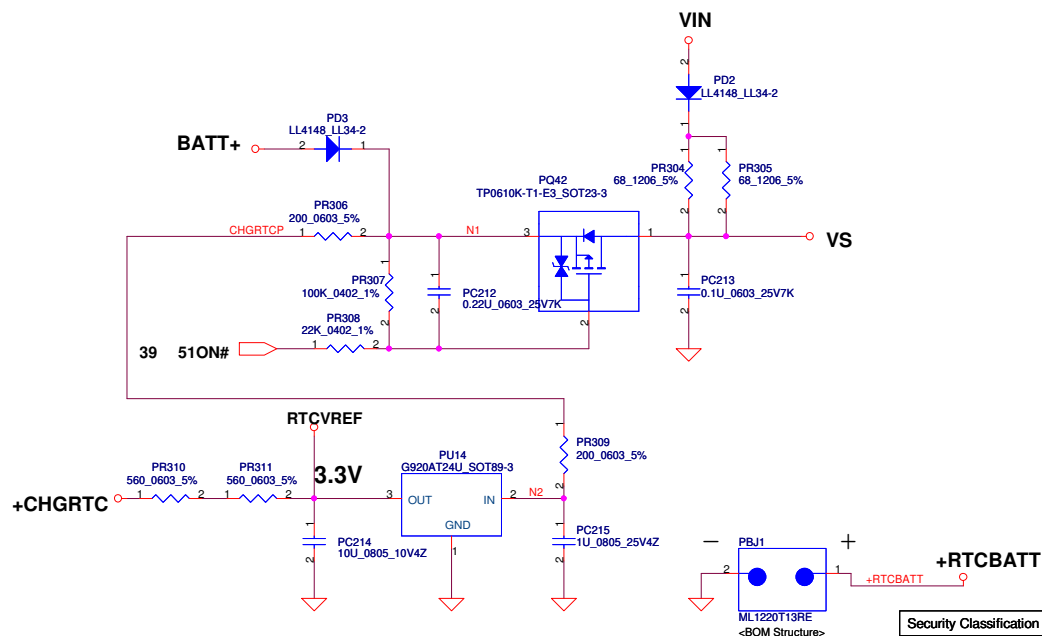
2009/08/17 add VGA_ON#

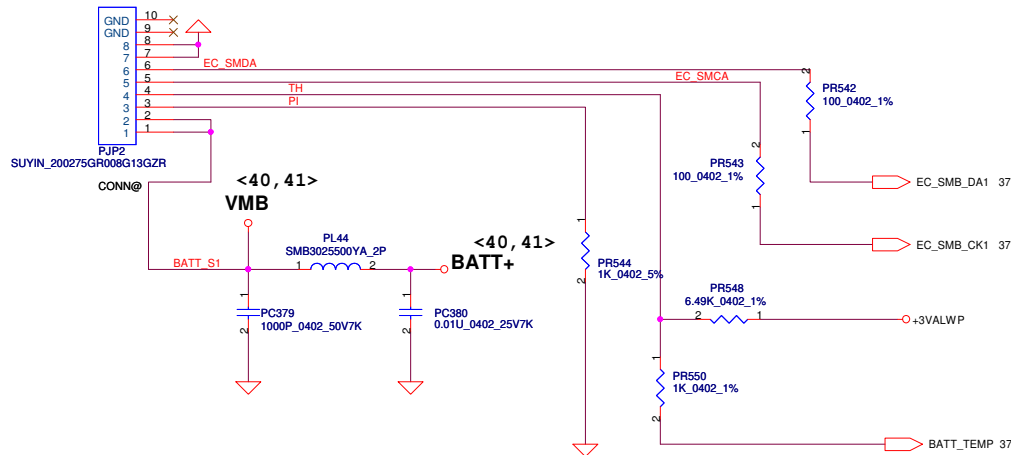
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Issued Date				2008/08/10				Title			
				Deciphered Date				2010/08/01			
								DC Interface			
								Document Number			
								NEW70 M/B LA-5891P Schematic			
								Rev 1.0			
								Date: Thursday, January 07, 2010			
								Sheet 43 of 59			



Vin Dectector

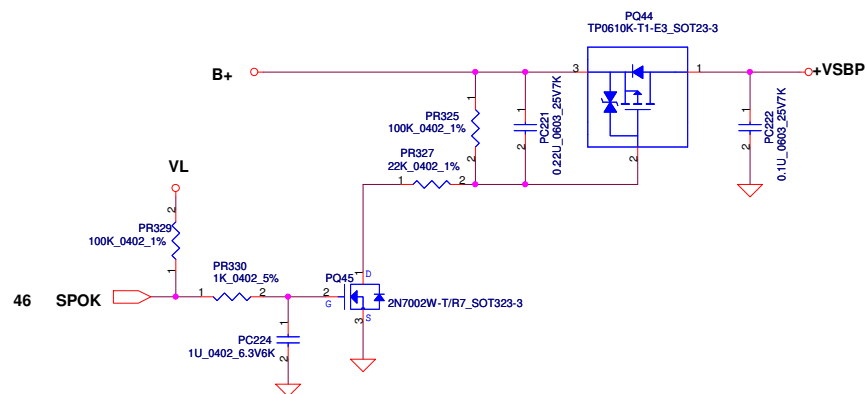
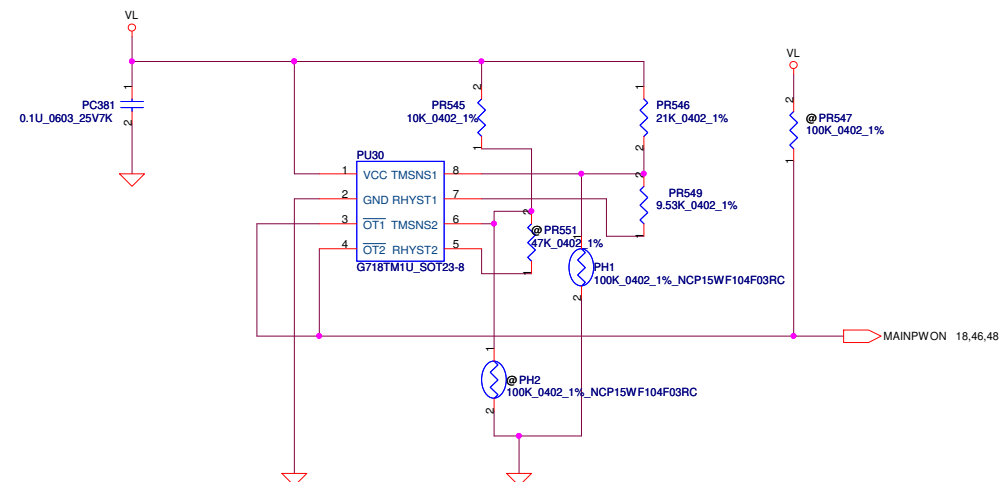
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 56 degree C

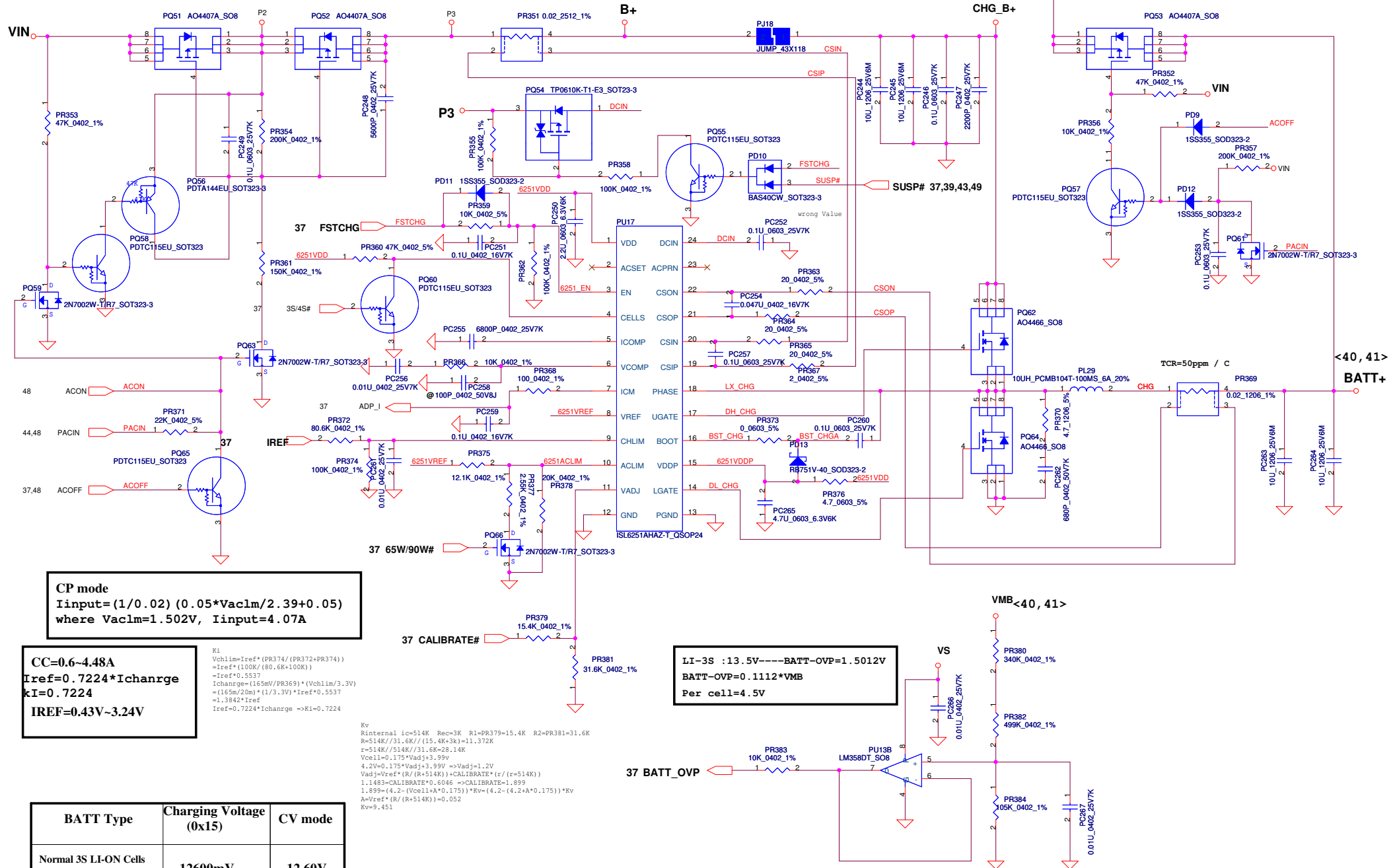


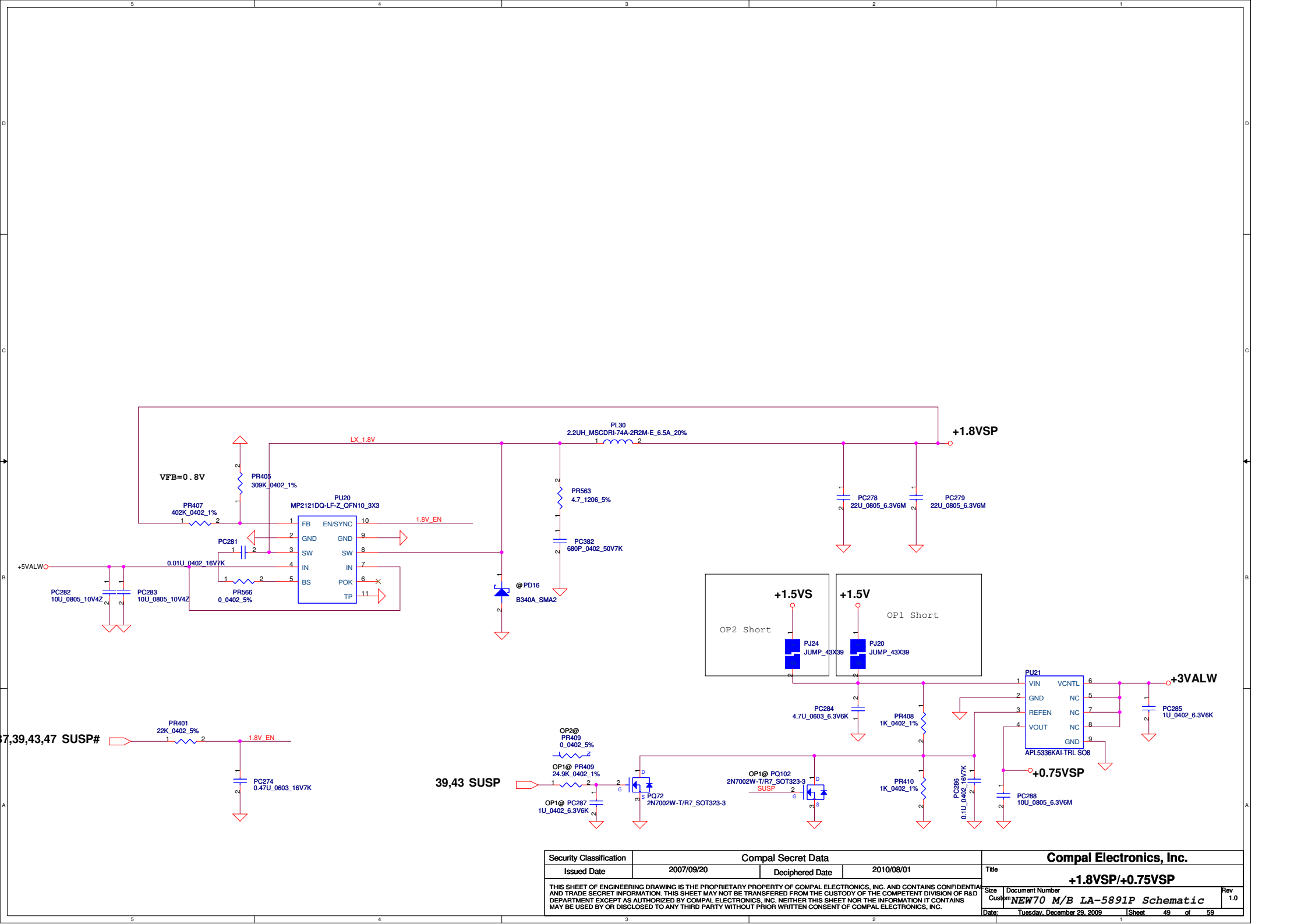
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Issued Date		2007/09/20		Deciphered Date	2010/08/01		Title					
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							Size	Document Number			Rev	
								NEW70 M/B LA-5891P Schematic			1.0	
							Date:	Tuesday, December 29, 2009		Sheet	45	of

Iada=0~4.74A (90W/19V=4.736A)
Iada=0~3.42A (90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A

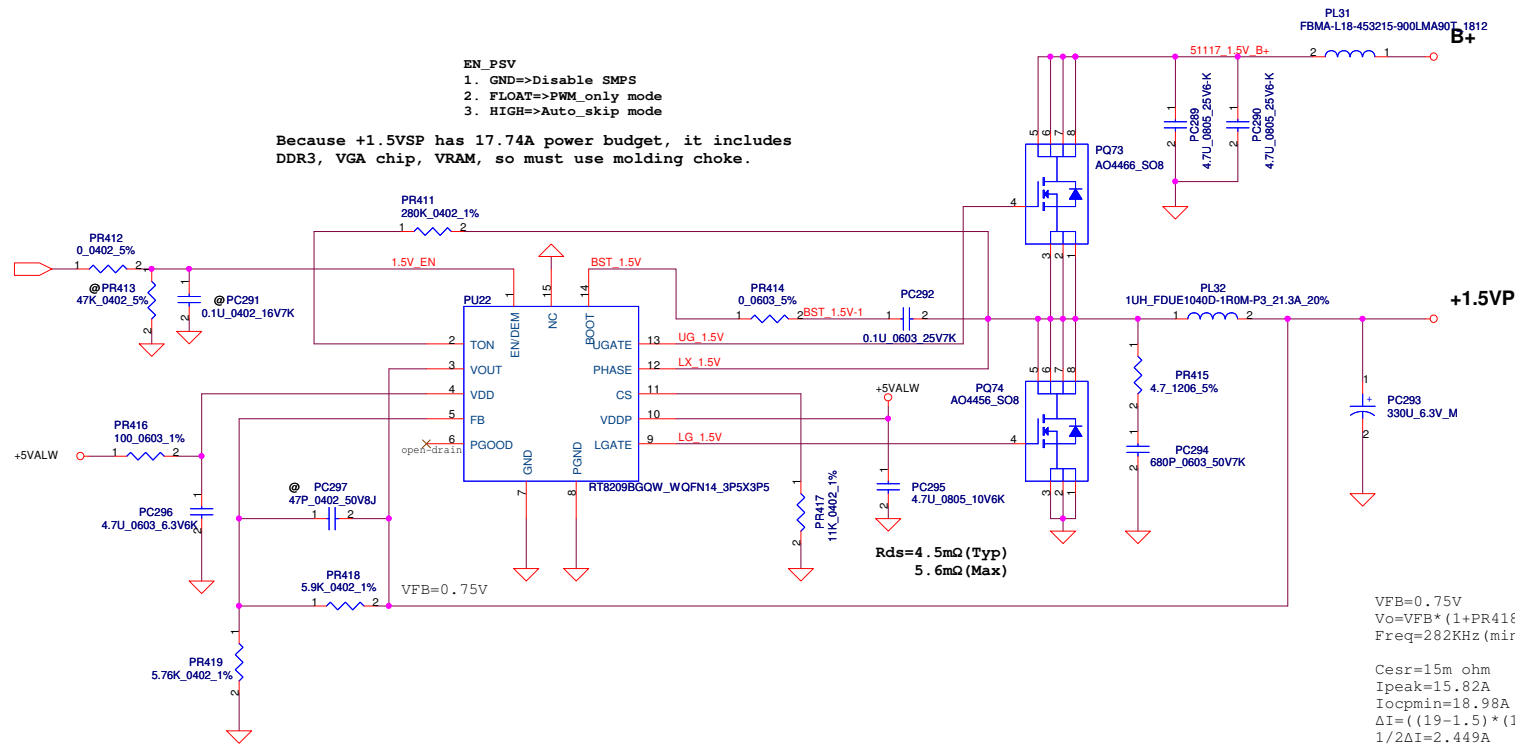




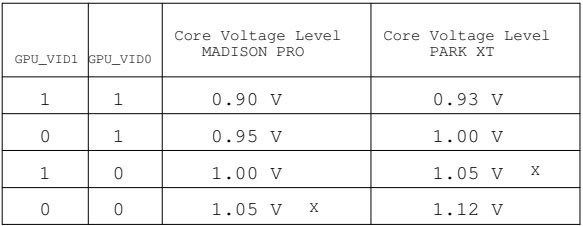
EN_PSV
 1. GND=>Disable SMPS
 2. FLOAT=>PWM_only mode
 3. HIGH=>Auto_skip mode

Because +1.5VSP has 17.74A power budget, it includes
 DDR3, VGA chip, VRAM, so must use molding choke.

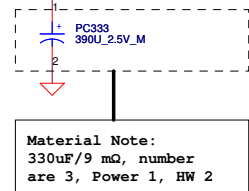
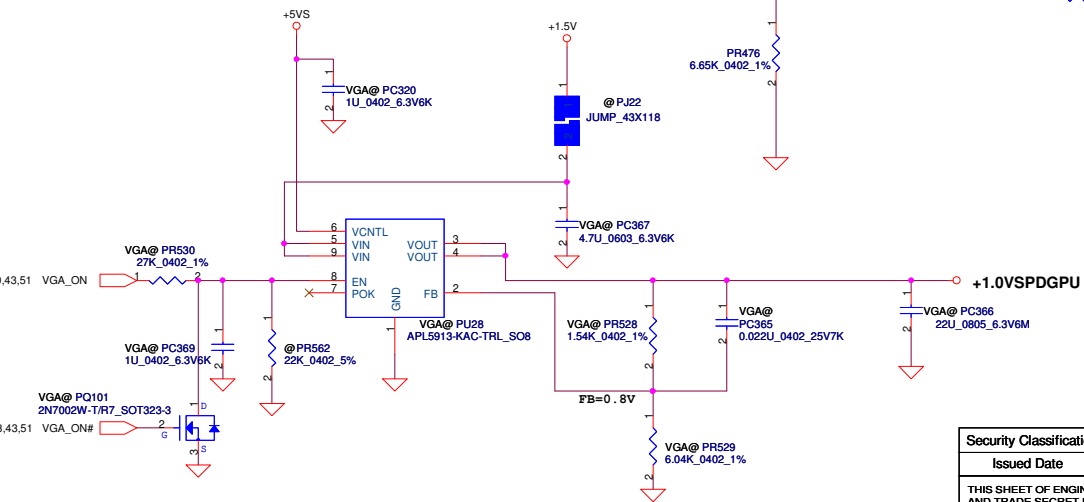
37,43 SYSON



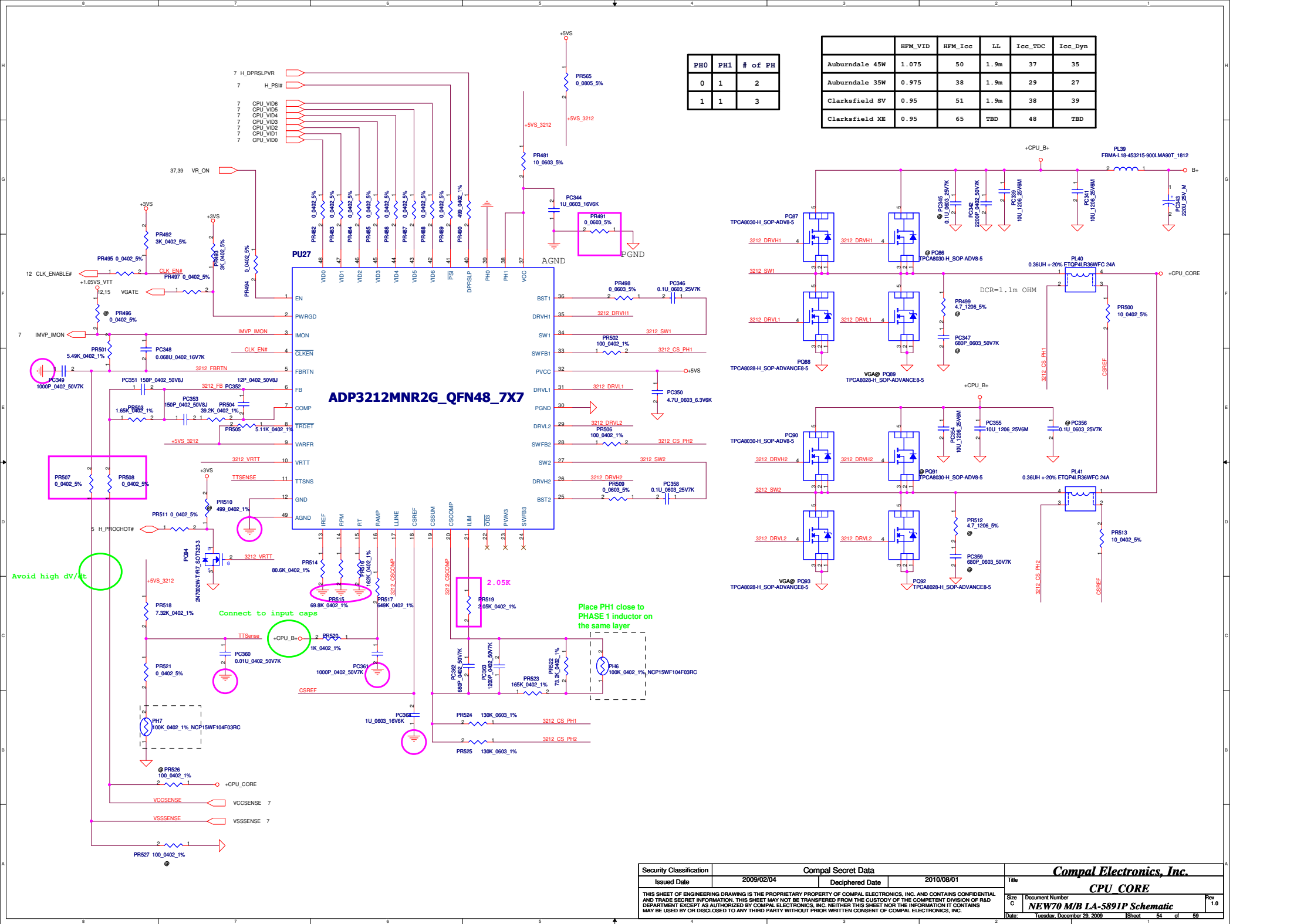
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Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title	
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Customer		NEW70 M/B LA-5891P Schematic		1.0	
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Issued Date	2009/4/15	Deciphered Date	2010/08/01	+1.05VS VTTP	
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				Customer	1.0
NEW70 M/B LA-5891P Schematic				Date:	Tuesday, December 29, 2009
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	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD

PH0	PH1	# of PH
0	1	2
1	1	3

Security Classification		Compal Secret Data		Title	
Issued Date	2009/02/04	Deciphered Date	2010/08/01	CPU CORE	
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					NEW70 M/B LA-5891P Schematic
				Rev 1.0	60

Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	For BOM unique.	For BOM unique.	0.1	46	Change PD8 from SC1SS355003(S DIO 1SS355) to SC100001K00(DIO 1SS355 SOD323 T/R-5K)	2009-1021	to DVT
2	For BOM unique.	For BOM unique.	0.1	54	Delete PQ86/PQ91 SB00000HL00(S TR TPCA8030-H 1N SOP). Add PQ87/PQ90 SB00000HL00(S TR TPCA8030-H 1N SOP).	2009-1021	to DVT
3	For UMA Arrandale CPU common design.	For UMA Arrandale CPU, we just only pop 1 HS MOS and 1 LS MOS.	0.1	54	Delete PQ89/PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
4	For VTT Power rail common design.	For VTT Power rail common design, we pop 1 HS MOS and 1LS MOS.	0.1	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
5	CIS link error.	CIS link error.	0.1	54	Change PR500 from SD028100A00(S RES 1/16W 10 +-5% 0402) to SD028100A80(S RES 1/16W 10 +-5% 0402)	2009-1021	to DVT
6	BOM unique.	BOM unique.	0.1	47	Chnage PC265 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
7	BOM unique.	BOM unique.	0.1	49	Chnage PC284 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
8	BOM unique.	BOM unique.	0.1	54	Chnage PC350 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
9	BOM unique.(For Madison/Park SKU)	BOM unique.(For Madison/Park SKU)	0.1	52	Chnage PC367 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
10	BOM unique.	BOM unique.	0.1	46	Change PC225/PC227 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
11	BOM unique.	BOM unique.	0.1	54	Change PC339/PC341 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206) Change PC354/PC355 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
12	+1.05VS_VTTP Cost down 1 LS MOS. HW request.	+1.05VS_VTTP Cost down 1 LS MOS. Because +1.05VS_VTT has voltage drop issue, HW request, remote sense to close to PCH.	0.2	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP) Delete PR471 SD028000080(S RES 0 0402 5%) Delete PR473 from SD034100A80(S RES 10 0402 5%) Add PR564 SD028000080(S RES 1/16W 0 0402 5%)	2009-1029	to DVT
14	Adjust +1.05VS_VTTP OCP.	Because we remove a LS MOS, so OCP must adjust.	0.2	52	Change PR467 from SD000004080(S RES 1/16W 2.2K +-1% 0402) to SD034499180(S RES 1/16W 4.99K 0402 1%)	2009-1029	to DVT
15	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PU19 SA00001NC00 (S IC APL5913-KAC-TRL SO 8P)	2009-1029	to DVT
16	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PR402 SD034150280, PR404 SD034120280.	2009-1029	to DVT
17	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PC273 SE075103K80 PC275 SE000000I10 Delete PC272 SE107475K80, PC271 SE107105M80	2009-1029	to DVT
18	+VGA_COREP, efficiency issue.	Increase Freq, decrease choke, to improve efficiency.	0.2	51	Delete PR401 and PR403 SD028220280, PC274 SE026474K80 Change PR196 from SD034442280 to SD034365280.	2009-1029	to DVT
19	+VGA_COREP, OVP issue.	Becasue if PR199/PR202 pop 0ohm, it will cause OVP when VID change from 00 to 11)	0.2	51	Change PL14 from SL200000V00 to SH000005680 Change PR199/PR202 from SD028000080 to SD028100280 (S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
20	+VGA_COREP, cost issue.	Cost down.	0.2	51	Change PQ75/PQ78 from SB00000GL00(S TR TPCA8028-H 1N SOP) to SB000009F80(S TR AO4456 1N SO8)	2009-1029	to DVT
21	+VGA_COREP, satndard design.	+VGA_COREP, satndard design, pop 1HS MOS and 2LS MOS, so remove one HS MOS PQ79.	0.2	51	Delete PQ79 SB000008L80 (S TR SI7686DP-TI-E3 1N POWERPAK SO8)	2009-1029	to DVT
22	+GFX_COREP, spike issue.	Because +GFX_COREP has spike voltage issue, add schottky diode across GFXVR_EN and VS_ON to solve it.	0.2	51	Add PD17 SCS00000Z00 (S SCH DIO RB751V-40 SOD-323)	2009-1029	to DVT
23	+VGA_COREP, OCP caaculation erroe issue.	Because VGA_CORE has 2 LS MOS, APW7138 detect LS Rdson, so when caculate OCP, Rdson must reduce 1/2.	0.2	51	Change PR190 from SD034649180 to SD034511180 (S RES 1/16W 5.11K 0402 1%)	2009-1029	to DVT

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				NEW70 M/B LA-5891P Schematic	
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Version change list (P.I.R. List)

Page 2 of 3 for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	CPU choke TOHO quality issue.	Because TOHO has quality issue before, change to Panasonic choke.	0.2	54	Change PL40/PL41 from SHSH00000F000 S COIL 0.36UH +-20% SF-I104-R36 23A to SH000005680 S COIL 0.36UH +-20% PCMC104T-R36MN1R17	2009-1029	to DVT
2	+VGA_COREP, voltage change.	ATI updated Park output voltage.	0.2	51	Change PR197 from SD034649280 to SD034432280.	2009-1029	to DVT
3	+VGA_COREP, voltage change.	ATI updated Park output voltage.	0.2	51	Chnage PR198 from SD034953180 to SD034887180.	2009-1029	to DVT
4	+VGA_COREP, voltage change.	ATI updated Park output voltage.	0.2	51	CHange PR201 from SD034316280 to SD034255280.	2009-1029	to DVT
5	+VGA_COREP, initial state unknow.	When VGA_CORE start up, but VBIOS doesn't ready, the VID is unknow, add pull down R.	0.2	51	Add PR557/PR560 SD028100280 (S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
6	+1.0VSPDGPU,adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	52	Change PC369 from SE076104K80 to SE000000K80 (S CER CAP 1U 0402 X7R)	2009-1029	to DVT
7	+1.0VSPDGPU,adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	52	Change PR530 from SD028150380 to SD034270280 (S RES 1/16W 27K 0402 1%)	2009-1029	to DVT
8	+1.0VSPDGPU,adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	52	Delete PR562 SD028220280 (S RES 1/16W 22K +-5% 0402)	2009-1029	to DVT
9	+0.75VSP,adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	49	Change PR409 SD028000080 to SD034249280 (24.9K 0402 1%)	2009-1029	to DVT
10	=1.8VSP, voltage too small.	Because +1.8VSP drop in HW side, increase +1.8VSP.	0.2	49	Change PC287 from SE076104K80 to SE000000K80 Change PR405 from SD034316380 (S RES 1/16W 316K +-1% 0402) to SD034309380 (S RES 1/16W 309K 0402 1%)	2009-1029	to DVT
11	+GFX_COREP, spike voltage issue.	Because GFX_COREP has spike voltage issue, originally we add a schottcky diode to solve it, but Intel's command is that do not add it, because of overdriving, so delete it now.	0.3	53	Delete PD17 SCS00000Z00 (S SCH DIO RB751V-40 SOD-323)	2009-1104	to DVT
12	+GFX_COREP, EMI request.	EMI request to add snubber.	0.3	53	Add PR268 SD001470B80 (S RES 1/4W 4.7 +-5% 1206) Add PC199 SE025681K80 (S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
13	+1.05VSV_VTTP, EMI request.	EMI request to add snubber.	0.3	52	Add PR465 SD001470B80 (S RES 1/4W 4.7 +-5% 1206) Add PC332 SE025681K80 (S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
14	+VGA_COREP, EMI request.	EMI request to add snubber.	0.3	51	Add PR191 SD001470B80 (S RES 1/4W 4.7 +-5% 1206) Add PC171 SE025681K80 (S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
15	+1.5VP, EMI request.	EMI request to add snubber.	0.3	50	Add PR415 SD001470B80 (S RES 1/4W 4.7 +-5% 1206) Add PC294 SE025681K80 (S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
16	Charger, EMI request.	EMI request to add snubber.	0.3	47	Add PR370 SD001470B80 (S RES 1/4W 4.7 +-5% 1206) Add PC262 SE074681K80 (S CER CAP 680P 50V K X7R 0402)	2009-1104	to DVT
17	CPU_COREP, transient, load line modify.	CPU_COREP, transient, load line modify.	0.3	54	Change PR524/PR525 from SD014120380 to SD014130380. Change PR501 from SD034536180 to SD034549180 Change PC362 from SE074391K80 to SE074681K80 Change PL40/PL41 from SH000005680 to SH12036BM00.	2009-1104	to DVT
18	+VSBP, EMI request.	EMI request to add cap to reduce EMI noise on B+	0.3	45	Add PC221 SE000005280 S CER CAP .22U 25V K X7R 0603. Add PC222 SE042104K80 S CER CAP .1U 25V K X7R 0603	2009-1104	to DVT
19	+1.8VSP BOM error.	Loss +1.8VSP enable circiut.	0.3	49	Add PR401 SD014220280 S RES 1/16W 22K 0402 5% Add PC274 SE026474K80 S CER CAP 0.47U 16V K X7R 0603	2009-1104	to DVT
20	+VGA_COREP, output voltage change.	Because ATI change Park output voltage, we saperate Park and Madison by PAK@ and MAD@. And Change Madison X63 BOM.	0.4	51	Change PR197 from SD034432280 to SD034681280. Chnage PR198 from SD034887180 to SD034953180. Change PR201 SD034255280 to SD034316280.	2009-1113	to DVT
21	+CPU_COREP, power measure.	Because HW want to measure CPU_CORE IC power loss, Add 0805 R to saperate +5VS.	0.4	54	Add PR565 SD002000080 S RES 1/8W 0 +-5% 0805	2009-1113	to DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	+CPU_COREP, IMON design change.	Intel release IMON RC time constant new request, change PC348 to 0.068u to meet spec.	0.4	54	Change PC348 from SE076103K80 S CER CAP .01U 16V K X7R 0402 to SE0000003J80 S CER CAP 0.068U 16V K X7R 0402	2009-1113	to DVT
2	+CPU_COREP, cost issue.	SF000000G80 will cost up, change to SF22004M210.	0.4	54	Change PC343 from SF000000G80 to SF22004M210.	2009-1113	to DVT
3	+3V/+5V cost issue.	Because Nippon cost up thier OS-CON cap, so we change Nippon cap to Sanyo cap by sourcer request.	0.5	46	Change PC233/PC237 from SF22001M300 S ELE CAP 220U 6.3V M F60(6.3X5.7) PXC to SF22001M200 S ELE CAP 220U 6.3V M B C6 SVPC_ESR15	2009-1118	to DVT
4	+1.05VS_VTTP issue.	+1.05VS_VTTP choke unique to +1.5VP.	0.5	52	Change PL38 from SH000008V80 S COIL 1UH +-20% PCMB103E-1R0M20A to SH000009U00 S COIL 1UH +-20% FDUE1040D-1R0M=P3 21.3A	2009-1118	to DVT
5	+VGA_COREP 2nd source issue.	In order to phase in 2nd source of APW7138, must add Pin6 components to meet ISL6268 requirement.	0.6	51	Add PC172 SE071220J80 S CER CAP 22P 50V J NPO 0402 Add PC174 SE075682K80 S CER CAP 6800P 25V K X7R 0402 Add PR195 SD034909280 S RES 1/16W 90.9K 0402 1%	2009-1208	to PVT
6	+VGA_COREP 2nd source issue.	In order to phase in 2nd source of APW7138, must add Pin6 components to meet ISL6268 requirement.	0.6	51	Change location PU23 to PU998.	2009-1208	to PVT
7	+1.05VS_VTTP 2nd source issue.	In order to phase in 2nd source, change ISL6268 to APW7138.	0.6	52	Change PU26 from SA00001HT80 S IC ISL6268CAZ-T SSOP 16P to PU999 SA000020600 S IC APW7138NITRL SSOP 16P	2009-1208	to PVT
8	+1.05VS_VTTP 2nd source issue.	APW7138 needn't pop PC335.	0.6	52	Delete PC335 SE075103K80 S CER CAP .01U 25V K X7R 0402 and change location to PC999.	2009-1208	to PVT
9	HDD LED flash issue.	HDD LED will flash when plug in adapter, because +3VS rise a little. HW request add PC224 to solve it.	0.6	45	Add PC224 SE000000K80 S CER CAP 1U 6.3V K X5R 0402	2009-1208	to PVT
10	HDD LED flash issue.	If add PC224, must change PR330 from 0 to 1K to avoid SPOK pin fail. that is add a current limit R on SPOK pin.	0.6	45	Chnage PR330 from SD028000080 to SD028100180.	2009-1208	to PVT
11	BOM error.	+1.8VSP choke use wrong material.	0.6	49	Change PL30 from SH000006I80 S COIL 2.2UH +-20% PCMC063T-2R2MN 8A to SH000009Q00 S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A	2009-1208	to PVT
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A --> B Change List

1012:-----
Page 29,30 Update F1,F2 symbol to SP04301P120(F_SMD1812P110TF)
Page 36,38 C789,C788,C684 symbol update (have pin define)
Page 31, U3 P/N change from SA00001RM00 to SA00003O900
1102:-----
Page 7,8 C97,C675,C134,C136,C251,C268,C541,C667 symbol update from SGA00002380 to SGA00002U00
Page 23. Add C609 0.1u_0402(SE076104K80) R739 24K_0402(SD034240280) fix +3VSDGPU Ramp up issue
Page 17,35 Add 1 more USB trace to 3G/B connector from PCH USB20_P10 & USB20_N10
1103:-----
Page 43 R200 change symbol from 22_0402_5% to 22_0603_5%
Page 39 SW1,SW4 BOM structure change to @
Page 36 C789.2 power source +3VS change to +3VALW
1104:-----
Page 8, Add C797,C798,C799,C800 0.1u_0402 at between +1.5V&+1.5V_1(Intel suggest)
Page 15,37 U41.F3 modify net from GPIO62 to susclk
Page 37 Add R740(@) close U32.123
1105:-----
Page 8 R98 change from 4.7K_0402_5% to 330ohm_0402_5% (Intel feekback VGFX_CORE issue solution)
1109:-----
Page 23 Change R717,R718,R720,R509 BOM structure from VGA@ to @ (Madison&Park prodution remove JTAG option2)
Page 24 Change R64 BOM structure from @ to VGA@ (Madison&Park prodution remove JTAG option2)
Page 23 Remove and short R729 (A2VDD)
Page 23 Change C600,C172,C599 BOM structure from VGA@ to @ (+A2VDD)
Page 23 Remove and short L6 (+A2VDDQ)
Page 26 Remove and short R730,R731,R732,R733,R734,R735,R736,R737,R738, (DPB,DPC,DPD power source)
Page 37 Add R508 100K_0402 Pull down to GND(EC E51TXD_P80DATA)(fix Intel WLAN Card reset issue)
RF request:-----
Page 35 Add C801 (SE071470J80 47P_0402) and C173(SE000005T80 10U_0603)(+3VS_WWAN)
Page 23 Remove R508 (100_0402) change to C802(@) (12P_0402_50V8J)(SE071120J80) (VGA_CLK_27M)
Page 29 Add two shunt C804,C803 12P_0402_50V8J(SE071120J80)(P31.DDC to HDMI conn)
Page 29 Add two shunt C805,C806 22P_0402_50V8J(SE071220J80)(P29.LCD Conn)
pop R403(47_0402) and C516 (22P_0402)(CLK_PCI_LPC)
pop R163 (10_0402)and C319 (10P_0402) (CLK_BUF_ICH_14M)
EMI request:-----
Page 36 POP D26, CM1293-04SO(SC300000O00)
Page 38,40,41 POP D18,D19,D10,D9,D11,D28,D30 PJDLC05C(SCA00001100)
1110:-----
Page 38 Add Q53(ACIN_LED#)
1111:-----
Page 40 C775,C776,C777,C778 change Symbol from SE093475K80(4.7U_0805) to SE107475M80(4.7U_0603)
Page 38 R341,R343 100_0402_5% change to 680_0402_5%(BLUE LED Bright)
Page 38 R342,R344 300_0402_5% change to 3.9K_0402_5%(Orange LED Bright)
1113:-----
Page 8 R98 change from 330_0402_5% to 470_0402_5%(SD028470080)
Page 23 Change back R717,R718,R720,R509 BOM structure from @ to VGA@ (Madison&Park prodution remove JTAG option2)
Page 24 Change back R64 BOM structure from VGA@ to @ (Madison&Park prodution remove JTAG option2)
1116:-----
Page 13 U41 change P/N from SA00003N700 to SA00003N7B0
Page 34 T16 change P/N from SP050006C00 to SP050006B00
1117:-----
Page 58 Add HW PIR

B --> C Change List

1209:-----
R679 change BOM structure to @
D13,D15 change BOM structure to @
Change R717,R718,R720,R509 BOM structure from VGA@ to @ (Madison&Park prodution remove JTAG option2)
Change R64 BOM structure from @ to VGA@ (Madison&Park prodution remove JTAG option2)
Add R729 0_0402(SD028000080,@)
Add R730 0_0402(SD028000080,@) LOCAL_DIM for Panel new feature
Add R731 0_0402(SD028000080,@) COLOR_ENG_EN for Panel new feature
Add R732 100K_0402(SD028100380)LOCAL_DIM PD to GND
Add R733 100K_0402(SD028100380)COLOR_ENG_EN PD to GND
Q53 change BOM structure to @
ADD Q54 2N7002DWH_SOT363-6(SB00000AR10) for AC PLUG HDD LED flash issue
DEL U16 for AC PLUG HDD LED flash issue
C97,C134,C136,C251,C541,C268,C675,C667 symbol update from SGA00002U00 to SGA00001Q80
C775,C776,C777,C778 change P/N SE107475M80 to SE107475K80(4.7U_0603_6.3V6K)
R272(100K PU +3VS) change BOM structure to @
Add U32.85 WWAN_LED# (input)
Add U32.17 MINI1_LED# (input)
ADD R734 PD to GND (fix CPT Panel Flash issue)

1211:-----
ADD C807,C808 1000P_0402(SE074102K80) LAN EMI
ADD C610 0.1U_0402 Y5V(SE070104Z80) VGFX_CORE EMI
ADD C809 C810 0.1U_0402 Y5V(SE070104Z80) +1.5V EMI
1211B:-----
Add U32.36 WLAN_LED# (output)
Add U32.91 3G_LED# (output)
Add U32.85 WWAN_LED# (input)
1214:-----
ADD R735 For U24 power source +3VS (POP)
ADD R736 For U24 power source +5VS (@)
1215:-----
ADD R737 asmedia CLK-
ADD R738 asmedia CLK+
U24 PN change to SA00000U500 (74AHC1G125GW_SOT353-5)
1216:-----
C465 change BOM structure to @(3G 150U)
R41 change BOM structure to @(CRT DET)
Q20 change BOM structure to @(CRT DET)
R343,R341 change to 2.2K_0402_5%(SD028220180) (LED)
R334 change to 249K_0402_1%(SD034249380)
1217:-----
R253 2.2K_0402_5% change to @
R252 2.2K_0402_5% change to UMAHD@
R343 change to 2.2K_0402_5%(7080@) 680_0402_5%(90@)
R344 change to 3.9K_0402_5%(7080@) 680_0402_5%(90@)
R341 change to 2.2K_0402_5%(7080@) 680_0402_5%(90@)
R342 change to 3.9K_0402_5%(7080@) 680_0402_5%(90@)
1219:
R382 change to 18K_0402(SD028180280)(Board ID)
R389 ADD 100K_0402_5%(SD028100380) PH +3VALW(Board ID)
1223:
R157 change to R167 10K_0402_5% (GPIO66: L:6L H:8L)
GPIO21 define to Project ID (L:NEW50/70/80/90 H:NEW71/91)

C --> MP Change List

1228:
MB PCB P/N (DA80000H700)change to (DAZ0C900100)
Q5,Q9,Q16,Q19,Q21,Q22,Q26,Q27,Q35,Q40,Q47,Q54 change SB00000AR10 to SB00000D900
DEL D10 (Int. MIC ESD Diode PASS Can remove)
R382 change to 18K_0402_5%(SD028180280 Board ID rev0.3)
DEL R667,R668(SD028000080) USb common mode choke
DEL R167,(SD028100280)(GPIO66 PH 8L,PD 6L) 10K_0402_5%
ADD R157 (SD028100280)(GPIO66 PH 8L,PD 6L) 10K_0402_5%
ADD R389 (SD028100380)(Board ID)100K_0402_5%
ADD L68(SM070001600 12ohm bead) USB common mode choke
Modify U24 Symbol

0104:
ADD R350 100K_0402_5%(SD028100380)(3G PH +3VS_WWAN)
0107:
Q5,Q9,Q16,Q19,Q21,Q22,Q26,Q27,Q35,Q40,Q47,Q54 change SB00000D900 to SB00000DH00

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VGA

U34
PARK@
216-0774007 A11 PARK XT M2
PARK XT M2 A11: SA00003MC10

PCB

ZZZ
LA-5891P MB Rev0: DA80000H700
LA-5891P MB Rev1: DA80000H710
LA-5891P MB with Small Board Rev1: DAZ0C900100
LA-5891P REV1 M/B

X76

ZZZ
X761@
X76198BOL01
X76198BOL01 VRAM 512M SAM NEW70
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)

ZZZ
X762@
X76198BOL02
X76198BOL02 VRAM 512M HYN NEW70
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

ZZZ
X763@
X76198BOL03
X76198BOL03 VRAM 1G SAM NEW70
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)

ZZZ
X764@
X76198BOL04
X76198BOL04 VRAM 1G HYN NEW70
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

ZZZ
X765@
X76198BOL05
X76198BOL05 VRAM 512M AMD NEW70
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

ZZZ
X766@
X76198BOL06
X76198BOL06 VRAM 1G AMD NEW70
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

CRT Option Components

C607 C592 C567
DIS@2 DIS@2 DIS@2
15P_0402_50V8J 15P_0402_50V8J 15P_0402_50V8J

C603 C593 C569
DIS@2 DIS@2 DIS@2
12P_0402_50V8J 12P_0402_50V8J 12P_0402_50V8J

15P_0402_50V8J: SE071150J80
12P_0402_50V8J: SE071120J80

L47 DIS@ 0_0805_5%
L40 DIS@ 0_0805_5%
L38 DIS@ 0_0805_5%

0_0805_5%: SD002000080

NEW90 LED Option

2 5090@1
R343 680_0402_5%
2 5090@1
R344 680_0402_5%
2 5090@1
R341 680_0402_5%
2 5090@1
R342 680_0402_5%

PCH SKU Option

2 10K_0402_5%
R259 UMAO@

GPIO19

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