Compal Confidential

PEW71/91/51 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M
NV N11P-GV2H and N11P-GE

2010-06-07

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

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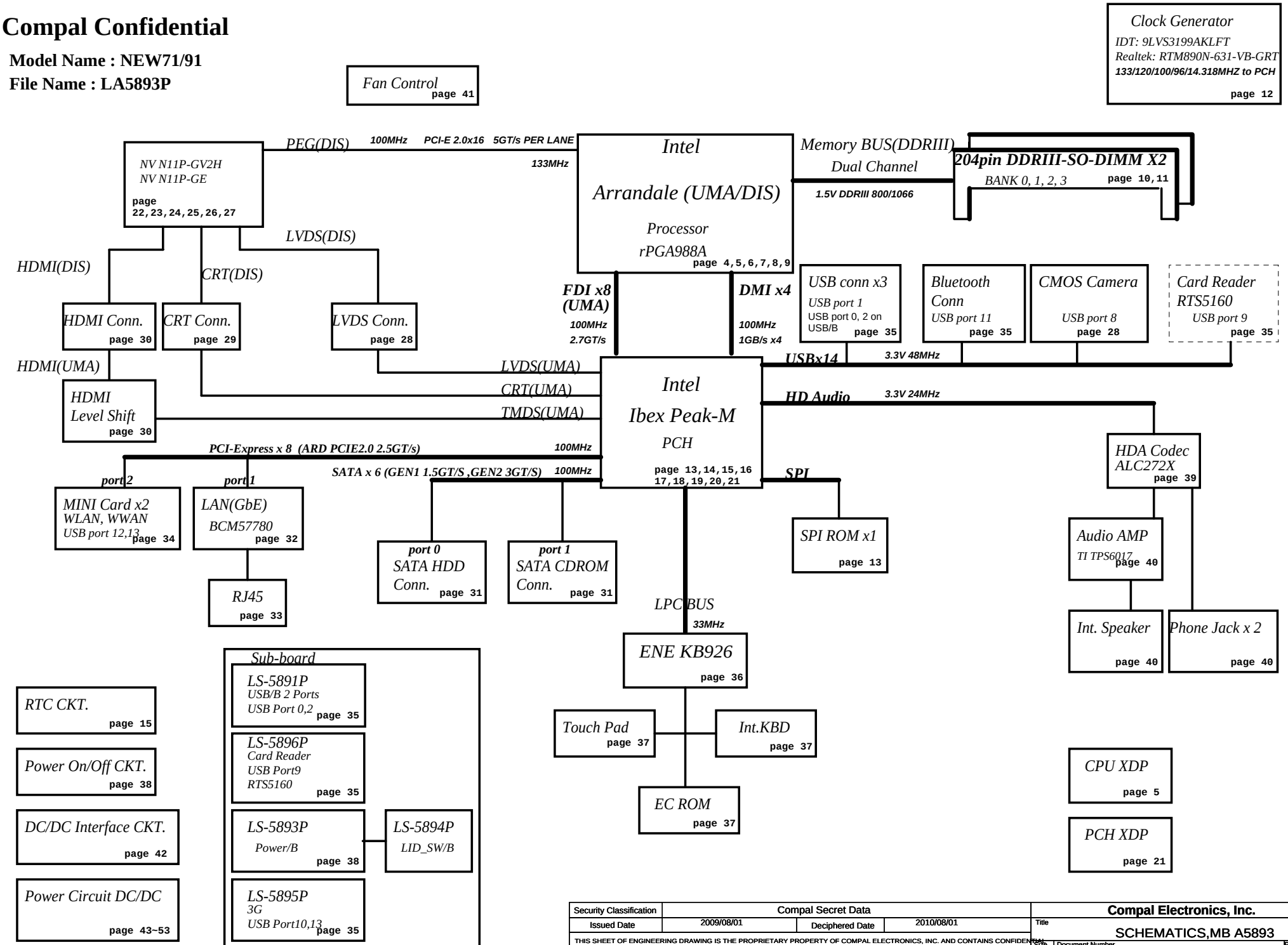
Model Name : NEW71/91
File Name : LA5893P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA ONLY	UMA ONLY@
Discrete	DIS@
Discrete Only	DIS ONLY@
VRAM	X76@
Switchable	SG@
UMA ONLY & OPTIMUS	UMOP@
3G	3G@
Blue Tooth	BT@
OPTIMUS	OPT@
NonSG SKU	NonSG@
NEW71	71@
NEW91	91@
N11P-GV2H	GV2H@
N11P-GE1	GE1@
N11P-GV2H-A2	GV2HA2@
N11P-GV2H-A3	GV2HA3@
Non OPT SKU	NonOPT@
SG or OPT	SGOPT@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Card Reader
	UHCI5	10	SIM Card
		11	Blue Tooth
	UHCI6	12	Mini Card(WLAN)
		13	Mini Card(GPS)

VRAM P/N :
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)

BOM Config move to page 56

VRAM BOM Config
X7621@: X76198BOL21 ALT. GROUP PARTS 1G SAM
X7622@ X76198BOL22 ALT. GROUP PARTS 1G HYN

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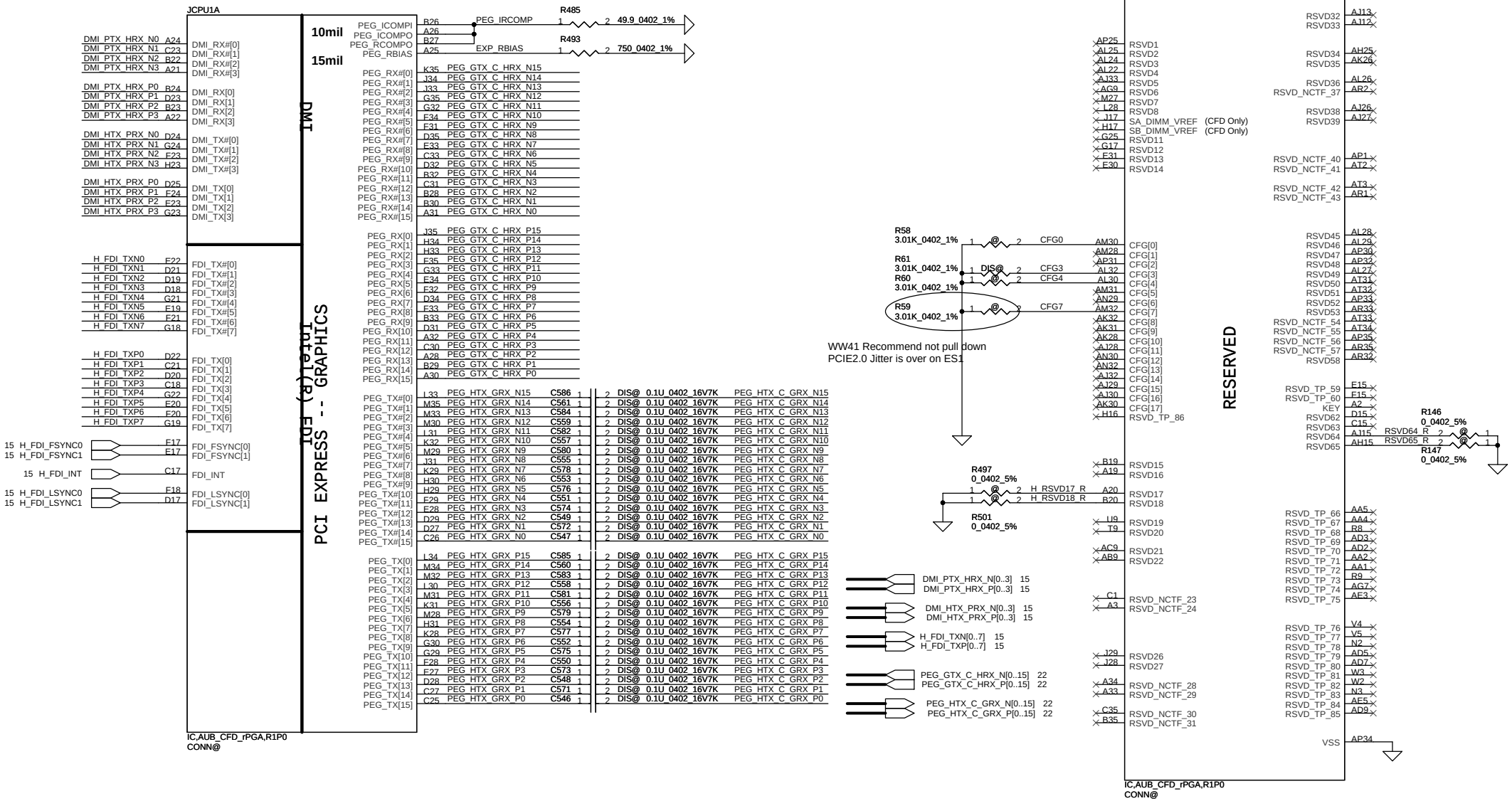
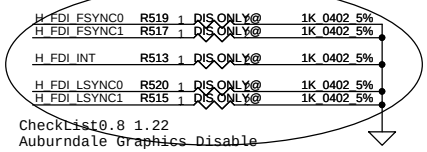


eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3



CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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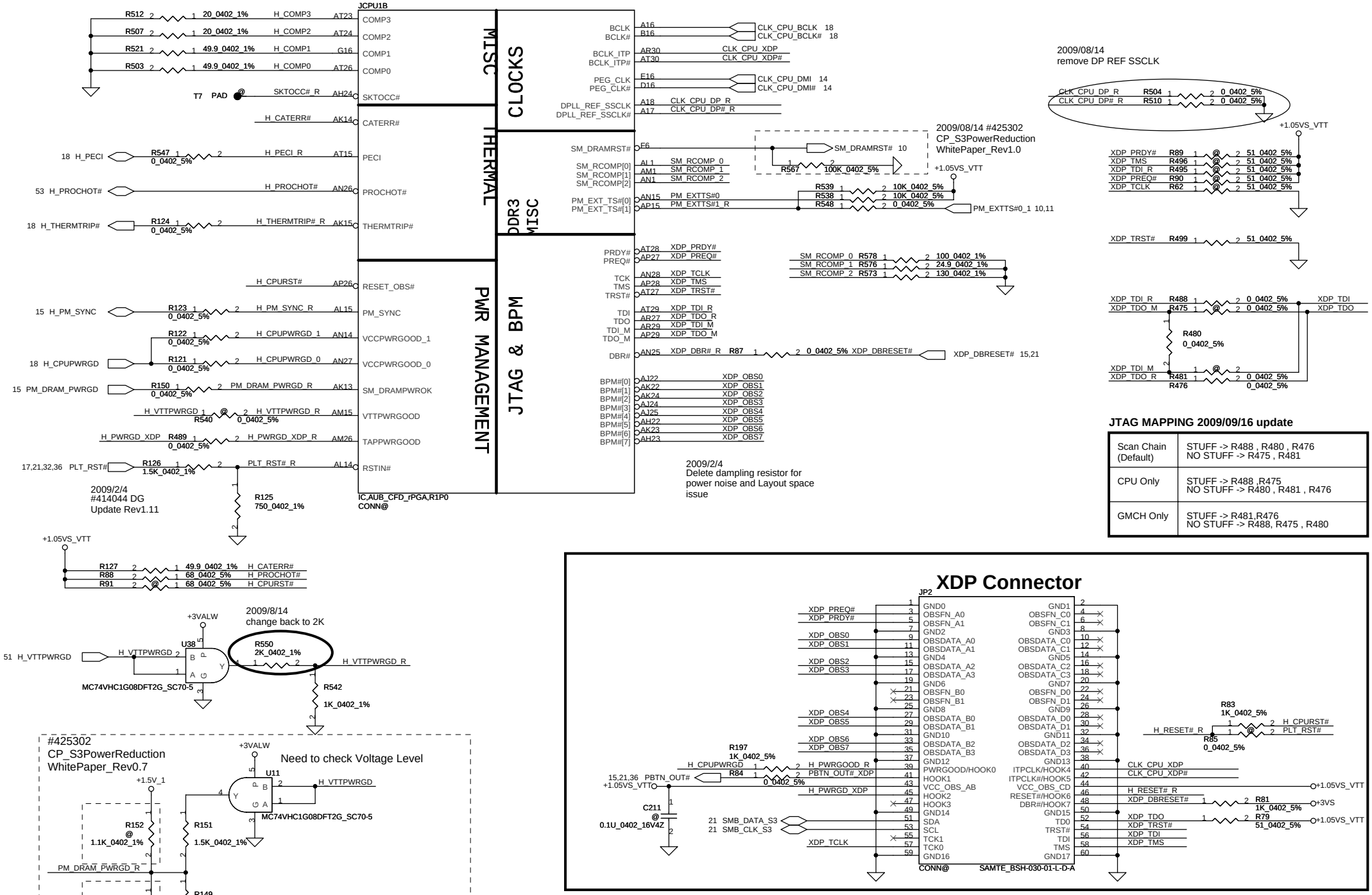

JTAG MAPPING 2009/09/16 update

Scan Chain (Default)	STUFF -> R488 , R480 , R476 NO STUFF -> R475 , R481
CPU Only	STUFF -> R488 ,R475 NO STUFF -> R480 , R481 , R476
GMCH Only	STUFF -> R481,R476 NO STUFF -> R488, R475 , R480

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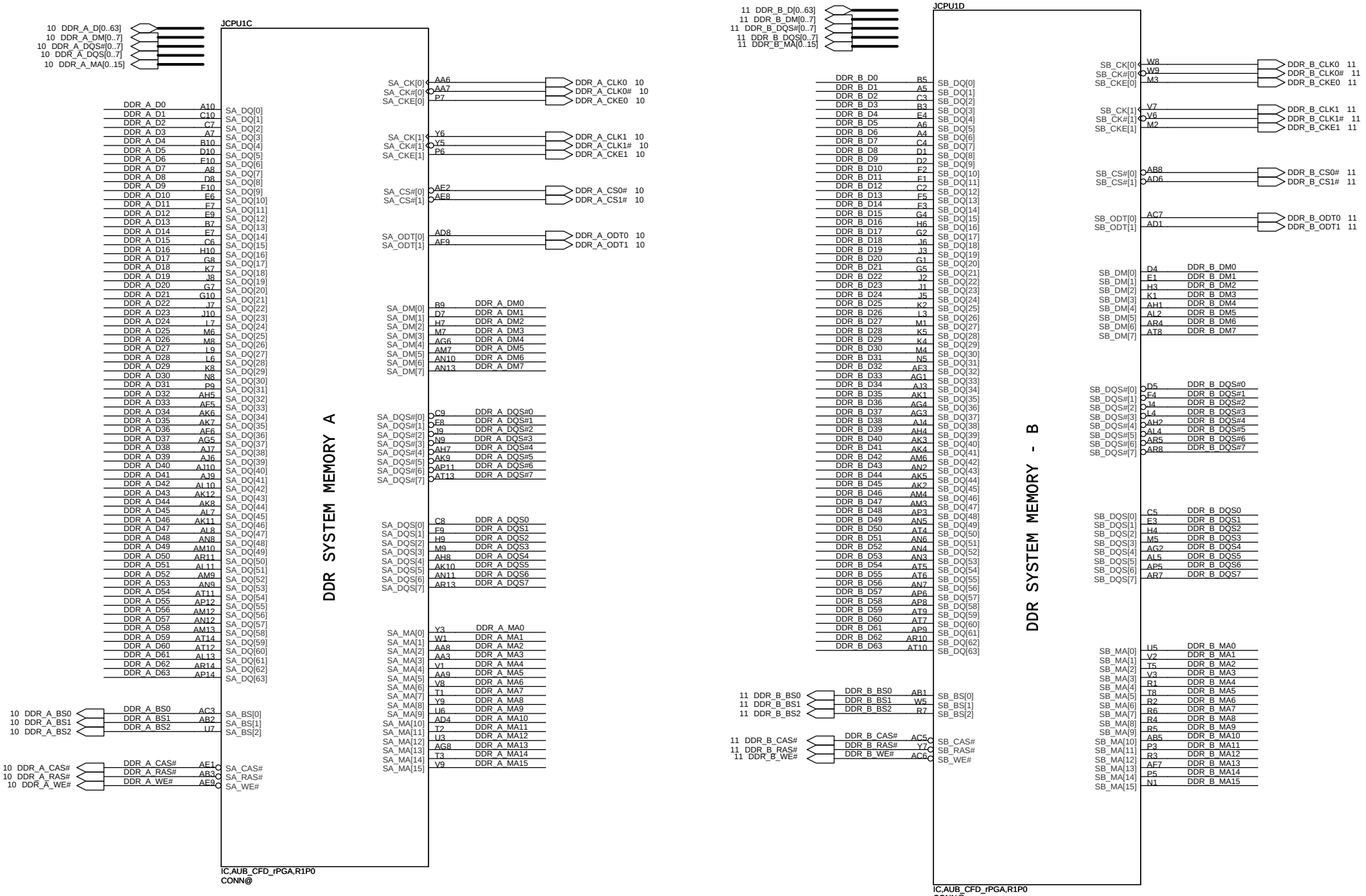

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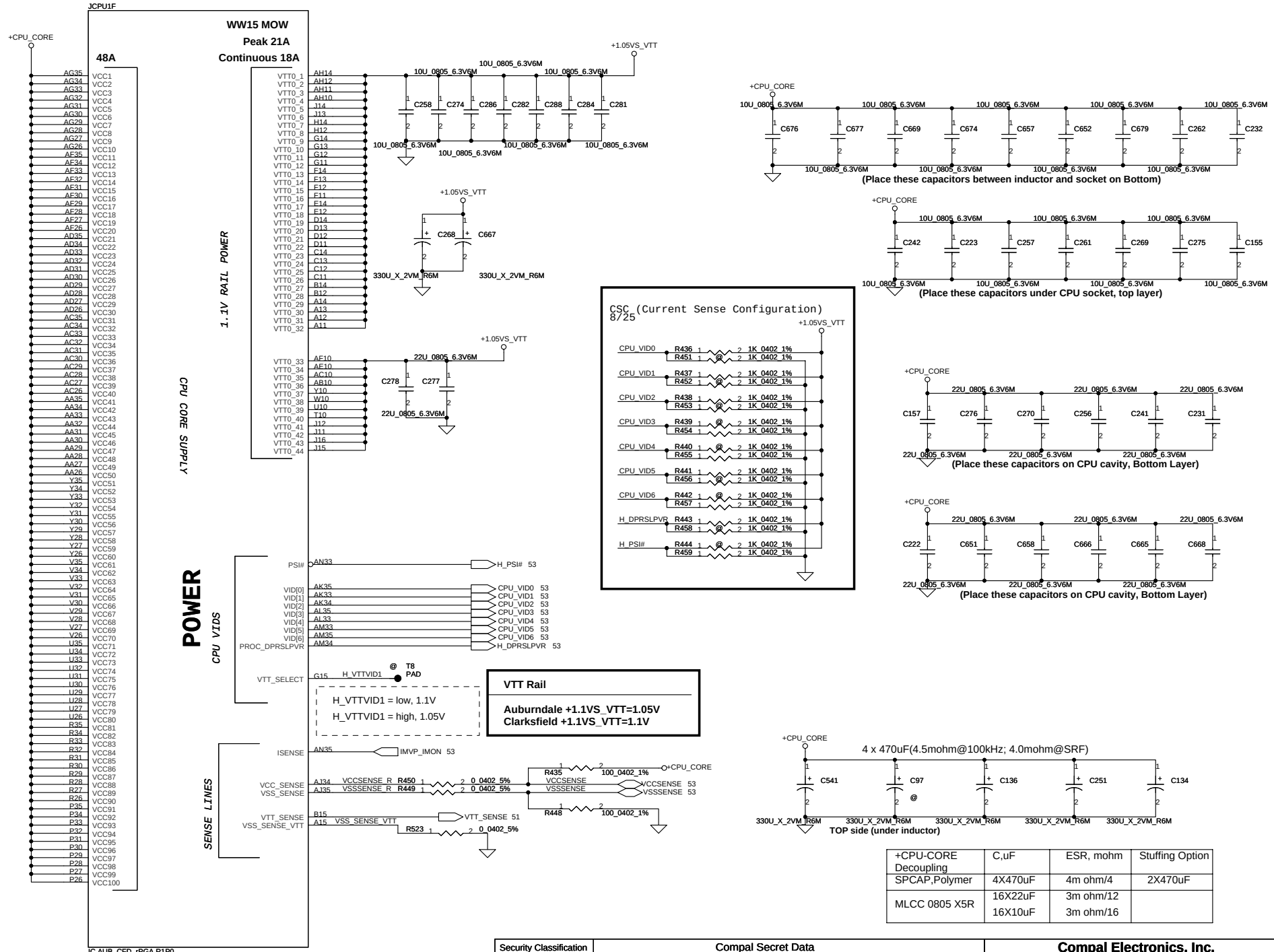

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

CSC (Current Sense Configuration)
8/25

(Place these capacitors between inductor and socket on Bottom)

(Place these capacitors under CPU socket, top layer)

(Place these capacitors on CPU cavity, Bottom Layer)

(Place these capacitors on CPU cavity, Bottom Layer)

TOP side (under inductor)

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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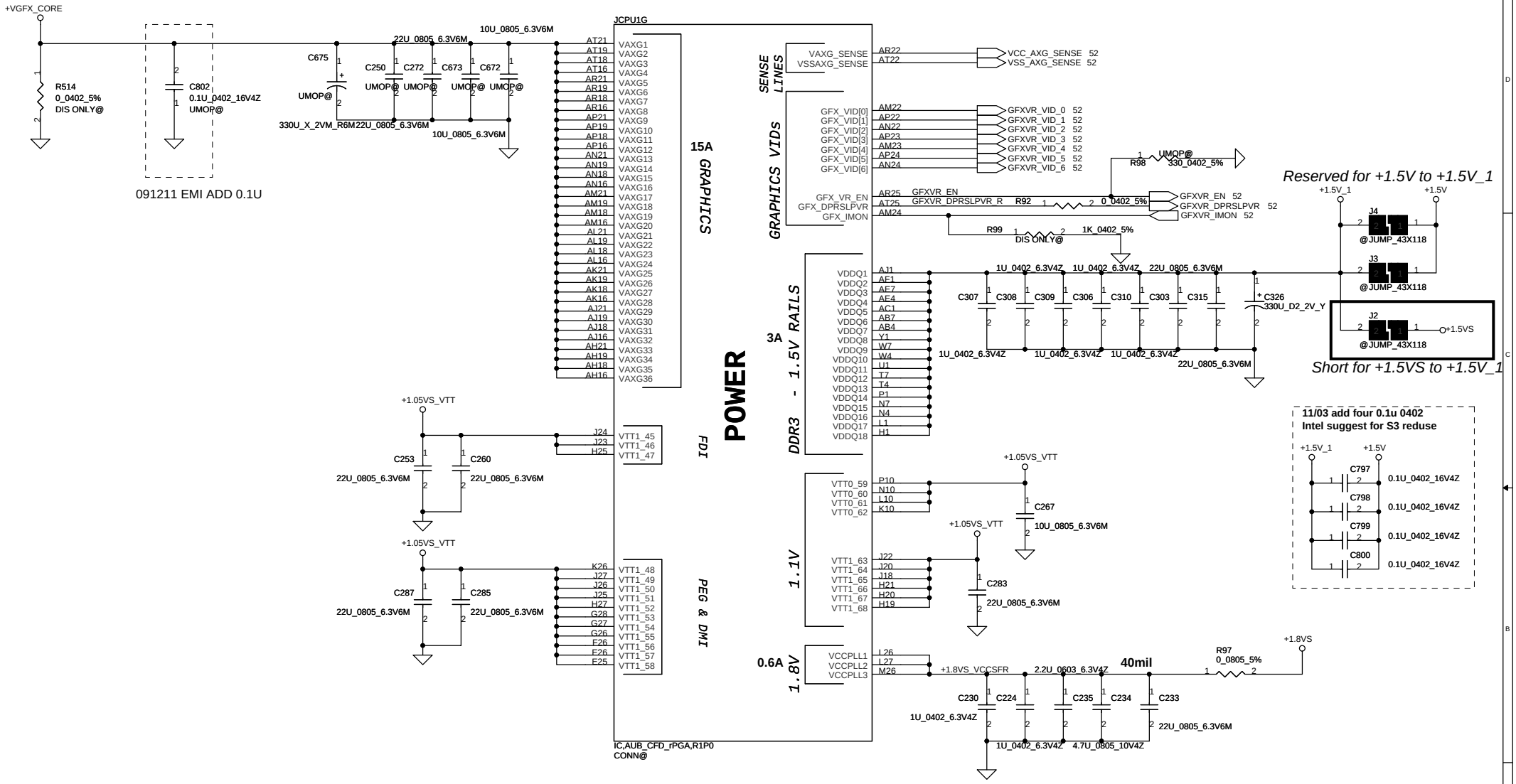

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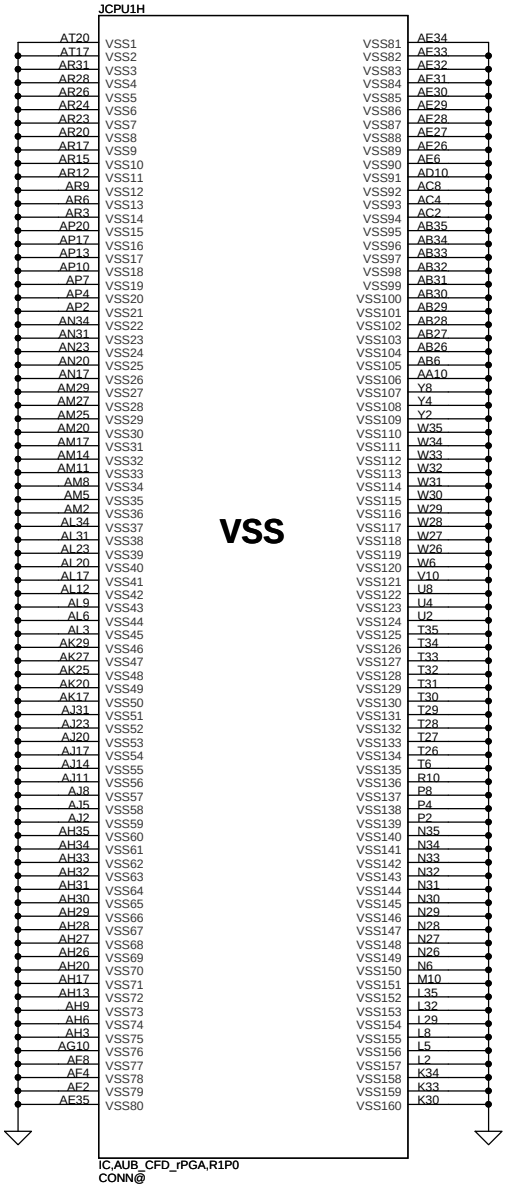

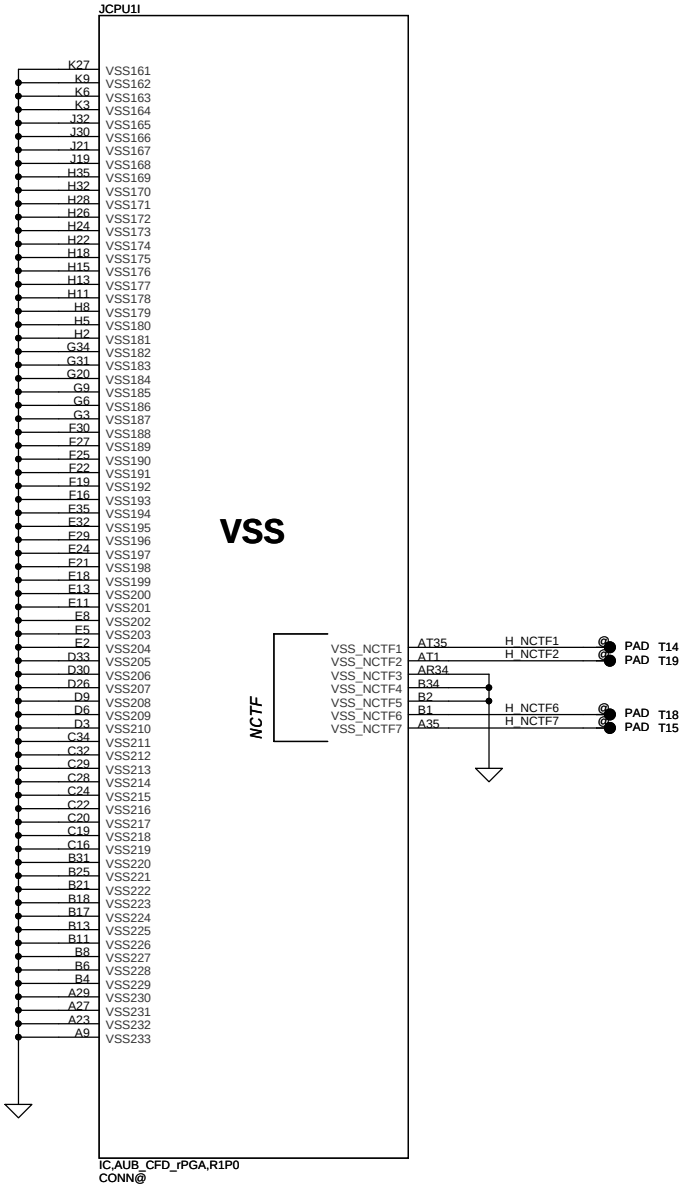

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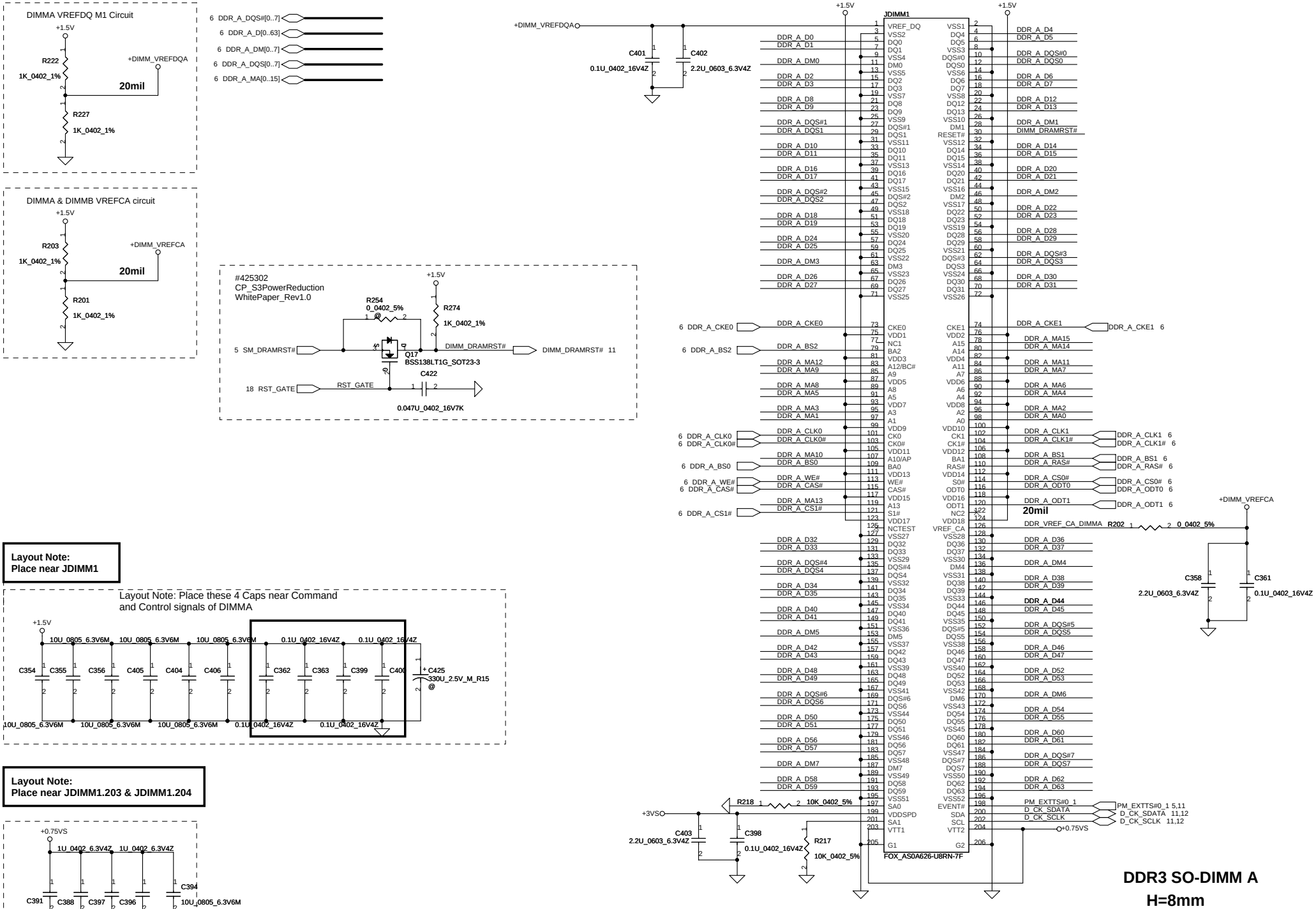

DDR3 SO-DIMM A
H=8mm

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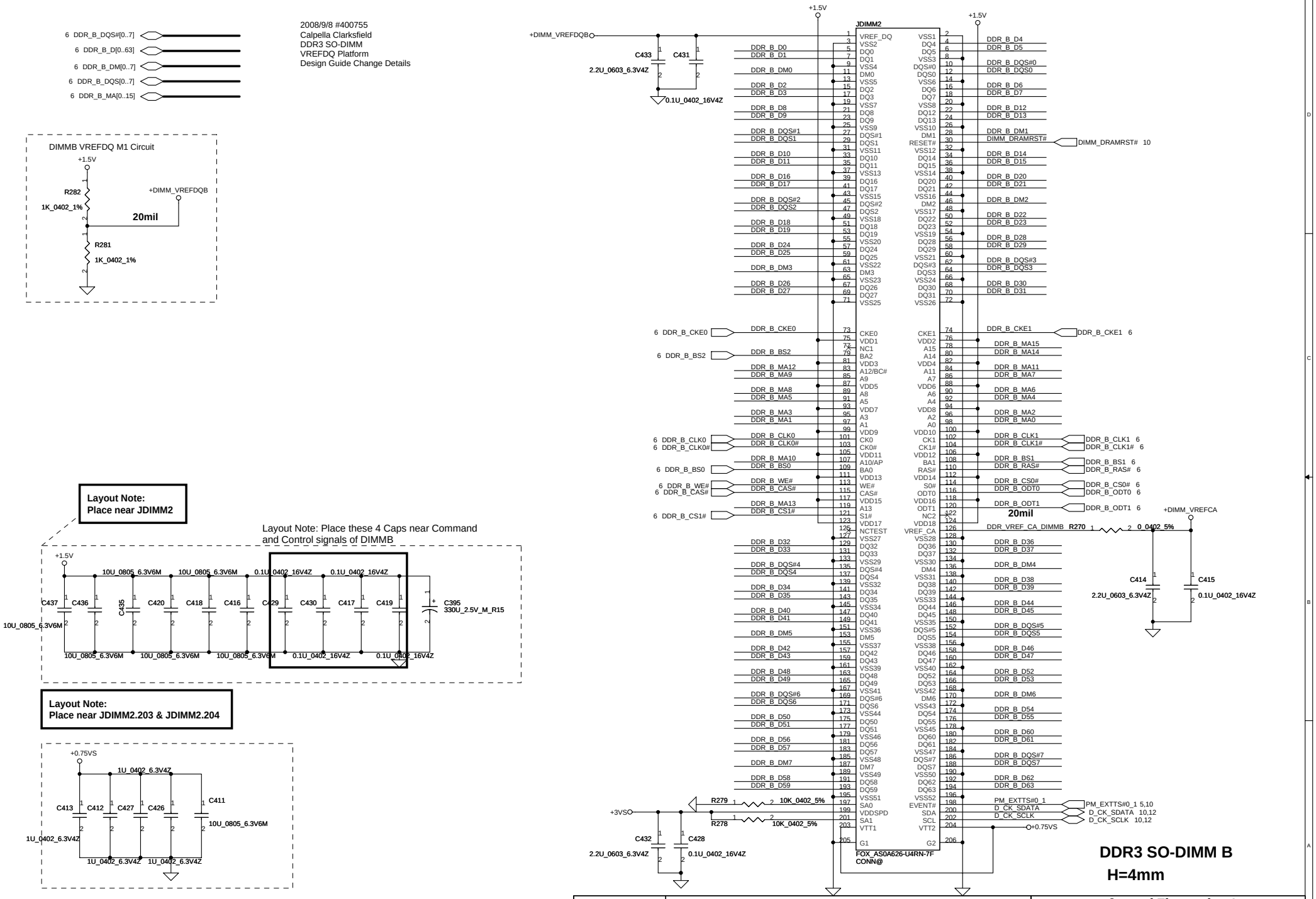

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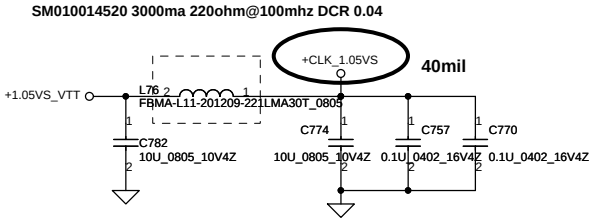
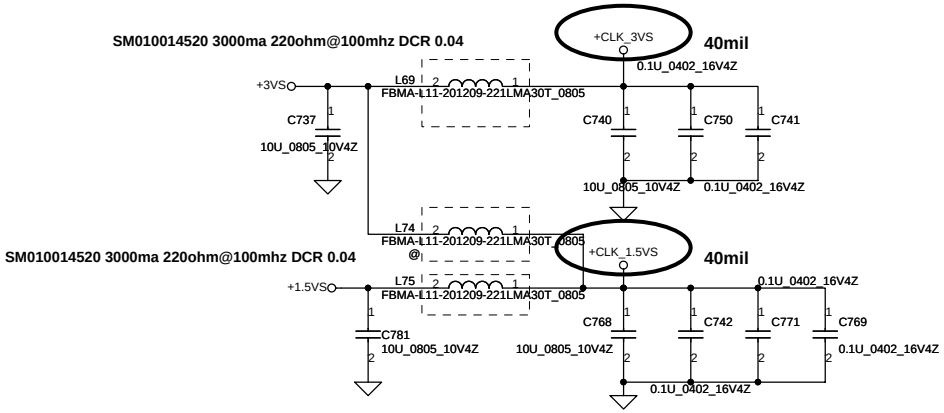
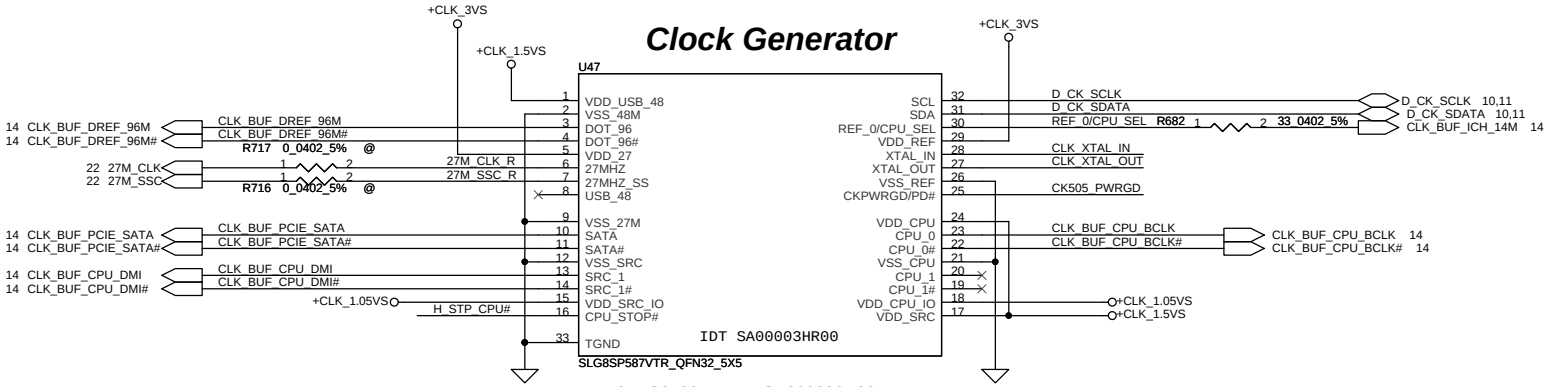




Clock Generator



IDT: 9LRS3199AKLFT, SA000030P00

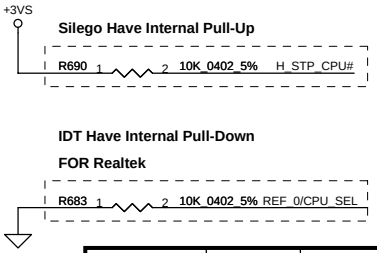
SILEGO: SLG8SP587V(WF), SA00002XY10

Low Power:

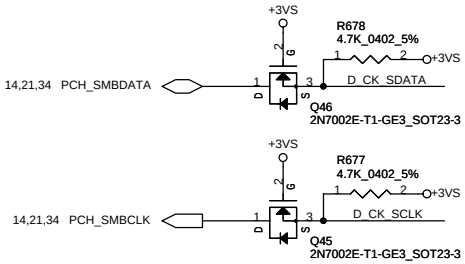
IDT: 9LVS3199AKLFT, SA00003HR00

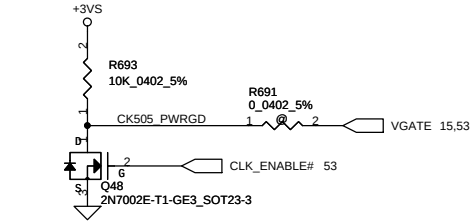
Realtek: RTM890N-631-VB-GRT, SA00003HQ10

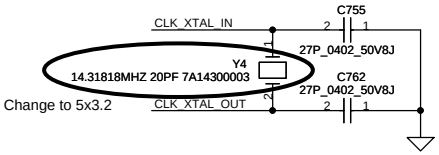
IDT 9LVS3199AKLFT NC



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz







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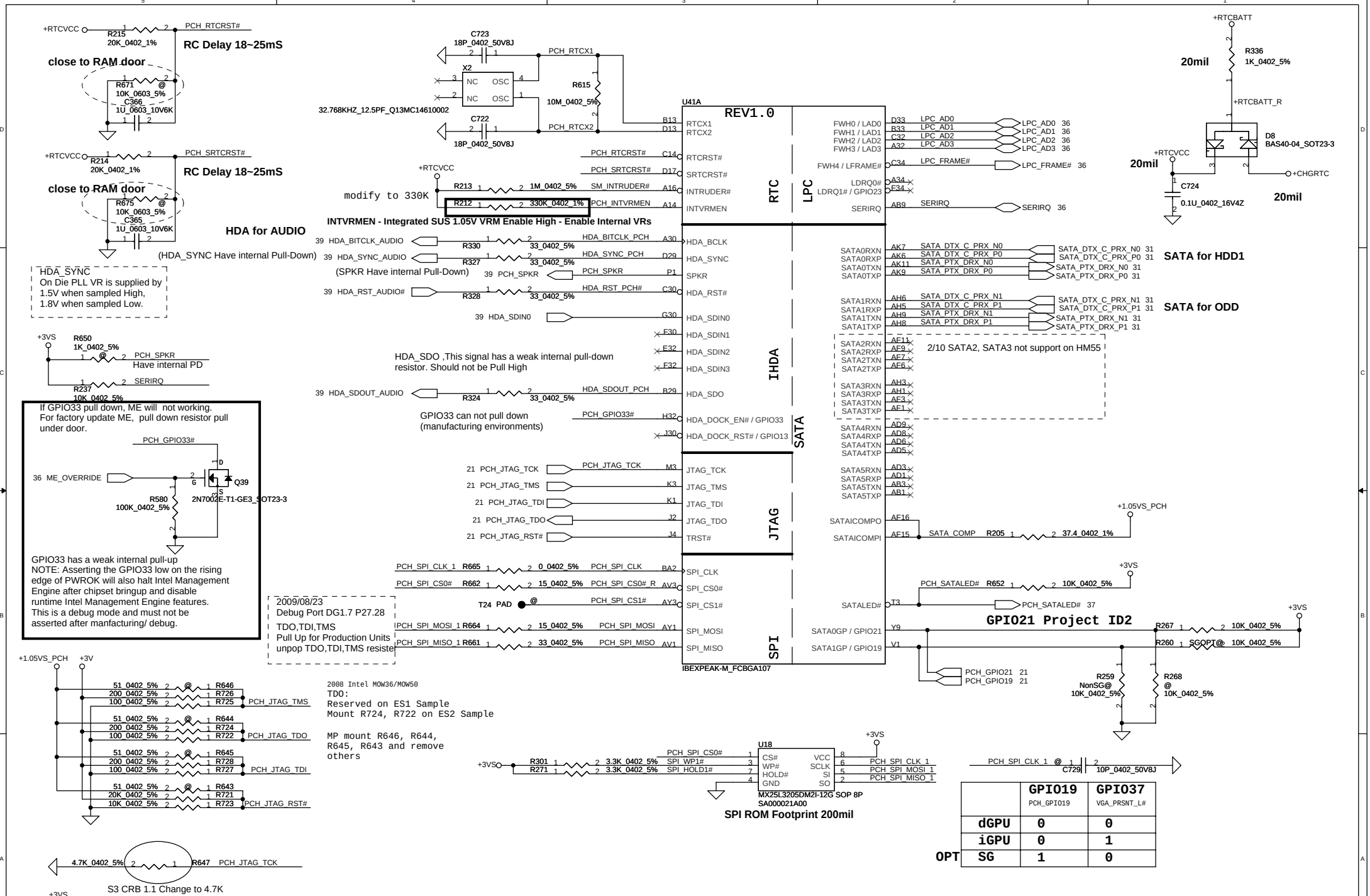

	GPIO19 PCH_GPIO19	GPIO37 VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
OPT SG	1	0

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Issued Date	2009/08/01	Deciphered Date	2010/08/01

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1. Connect Directly
   EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS
   CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS
   LAN
4. Level Shift3, Pull-Up to +3VS
   CPU & PCH XDP

U41B REV1.0 — PCI-E* / SMBus / Controller Link / PEG / From CLK BUFFER / Clock Flex — IBEXPEAK-M_FCBGA107

For PCIE LAN

32 PCIE_DTX_C_PRX_N1 — PCIE_DTX_C_PRX_N1 BG30 — PERN1
32 PCIE_DTX_C_PRX_P1 — PCIE_DTX_C_PRX_P1 BJ30 — PERP1
32 PCIE_PTX_C_DRX_N1 — C335 0.1U_0402_16V7K — PCIE_PTX_DRX_N1 BF29 — PETN1
32 PCIE_PTX_C_DRX_P1 — C339 0.1U_0402_16V7K — PCIE_PTX_DRX_P1 BH29 — PETP1

For Wireless LAN

34 PCIE_DTX_C_PRX_N2 — PCIE_DTX_C_PRX_N2 AW30 — PERN2
34 PCIE_DTX_C_PRX_P2 — PCIE_DTX_C_PRX_P2 BA30 — PERP2
34 PCIE_PTX_C_DRX_N2 — C332 0.1U_0402_16V7K — PCIE_PTX_DRX_N2 BC30 — PETN2
34 PCIE_PTX_C_DRX_P2 — C334 0.1U_0402_16V7K — PCIE_PTX_DRX_P2 BD30 — PETP2

AU30 PERN3, AT30 PERP3, AU32 PETN3, AV32 PETP3
BA32 PERN4, BB32 PERP4, BD32 PETN4, BE32 PETP4

For Mini2

2009/08/25: remove PCIE5

BE33 PERN5, BH33 PERP5, BG32 PETN5, BJ32 PETP5
BA34 PERN6, AW34 PERP6, BC34 PETN6, BD34 PETP6

2/10 PCIE7, PCIE8 not support on HM55

AT34 PERN7, AU34 PERP7, AU36 PETN7, AV36 PETP7
BG34 PERN8, BJ34 PERP8, BG36 PETN8, BJ36 PETP8

For PCIE LAN

32 CLK_PCIE_LAN# — AK48 — CLKOUT_PCIE0N
32 CLK_PCIE_LAN — AK47 — CLKOUT_PCIE0P
32 LAN_CLKREQ# — R258 1 2 0_0402_5% — PCH_GPIO73 — P9 — PCIECLKRQ0# / GPIO73

For Wireless LAN

34 CLK_PCIE_MINI1# — AM43 — CLKOUT_PCIE1N
34 CLK_PCIE_MINI1 — AM45 — CLKOUT_PCIE1P
34 MINI1_CLKREQ# — R266 1 2 0_0402_5% — PCH_GPIO18 — U4 — PCIECLKRQ1# / GPIO18
21 PCH_GPIO18

AM47 CLKOUT_PCIE2N, AM48 CLKOUT_PCIE2P
21 PCH_GPIO20 — PCH_GPIO20 — N4 — PCIECLKRQ2# / GPIO20

AH42 CLKOUT_PCIE3N, AH41 CLKOUT_PCIE3P
PCH_GPIO25 — A8 — PCIECLKRQ3# / GPIO25

2009/08/25: remove mini2 clk

AM51 CLKOUT_PCIE4N, AM53 CLKOUT_PCIE4P
MINI2_CLKREQ#_1 — M9 — PCIECLKRQ4# / GPIO26

AJ50 CLKOUT_PCIE5N, AJ52 CLKOUT_PCIE5P
PCH_GPIO44 — H6 — PCIECLKRQ5# / GPIO44

AK53 CLKOUT_PEG_B_N, AK51 CLKOUT_PEG_B_P
PCH_GPIO56 — P13 — PEG_B_CLKRQ# / GPIO56

SMBALERT# / GPIO11 — B9 — EC_LID_OUT# — EC_LID_OUT# 36
SMBCLK — H14 — PCH_SMBCLK — PCH_SMBCLK 12,21,34
SMBDATA — C8 — PCH_SMBDATA — PCH_SMBDATA 12,21,34
SML0ALERT# / GPIO60 — J14 — PCH_GPIO60
SML0CLK — C6
SML0DATA — G8
SML1ALERT# / GPIO74 — M14 — PCH_GPIO74
SML1CLK / GPIO58 — E10 — PCH_SML1CLK
SML1DATA / GPIO75 — G12 — PCH_SML1DAT

CL_CLK1 — T13
CL_DATA1 — T11
CL_RST1# — T9

PEG_A_CLKRQ# / GPIO47 — H1 — PEG_CLKREQ#_R — PEG_CLKREQ# 22
CLKOUT_PEG_A_N — AD43 — CLK_PEG_VGA# 22
CLKOUT_PEG_A_P — AD45 — CLK_PEG_VGA 22
CLKOUT_DMI_N — AN4 — CLK_CPU_DMI# 5
CLKOUT_DMI_P — AN2 — CLK_CPU_DMI 5

CLKOUT_DP_N / CLKOUT_BCLK1_N — AT1
CLKOUT_DP_P / CLKOUT_BCLK1_P — AT3

CLKIN_DMI_N — AW24 — CLK_BUF_CPU_DMI# 12
CLKIN_DMI_P — BA24 — CLK_BUF_CPU_DMI 12
CLKIN_BCLK_N — AP3 — CLK_BUF_CPU_BCLK# 12
CLKIN_BCLK_P — AP1 — CLK_BUF_CPU_BCLK 12
CLKIN_DOT_96N — F18 — CLK_BUF_DREF_96M# 12
CLKIN_DOT_96P — F18 — CLK_BUF_DREF_96M 12
CLKIN_SATA_N / CKSSCD_N — AH13 — CLK_BUF_PCIE_SATA# 12
CLKIN_SATA_P / CKSSCD_P — AH12 — CLK_BUF_PCIE_SATA 12
REFCLK14IN — P41 — CLK_BUF_ICH_14M 12 — R163 10_0402_5% — C319 10P_0402_50V8J
CLKIN_PCILOOPBACK — J42 — CLK_PCI_FB 17

1109 RF request

XTAL25_IN — AH51 — XTAL25_IN
XTAL25_OUT — AH53 — XTAL25_OUT
XCLK_RCOMP — AF38 — XCLK_RCOMP — R170 1 2 90.9_0402_1% — +1.05VS_PCH

CLKOUTFLEX0 / GPIO64 — T45
CLKOUTFLEX1 / GPIO65 — P43 — PROJECT_ID1
CLKOUTFLEX2 / GPIO66 — T42 — PROJECT_ID0
CLKOUTFLEX3 / GPIO67 — N50

+3V — R636 10K_0402_5%

DGPU_PWR_EN 18,21,38,42 — R275 DIS@ 10K_0402_5% — Q18 DIS@ (2N7002E-T1-GE3_SOT23-3) — R247 @ 2.2K_0402_5% — R276 @ 2.2K_0402_5%

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

R563 DIS ONLY@ 0_0402_5%
C693 UMOP@ 27P_0402_50V8J
R564 1M_0402_5% UMOP@
Y2 25MHZ_20PF_7A25000012 UMOP@
C694 27P_0402_50V8J UMOP@
Change to 5x3.2

2009/08/25: Change back to +3V remove mini2

+3V — R241 10K_0402_5% — MINI2_CLKREQ#_1

+3VS — 10K_0402_5% R265 MINI1_CLKREQ# — 10K_0402_5% R649 PCH_GPIO20

Project Structure ID

+3VS — R156 10K_0402_5% — OPT@ — R144 10K_0402_5% — NonOPT@ — R157 10K_0402_5% — @ — R167 10K_0402_5%

Schematic_Checklist_Rev1.6

GPIO18	Main (core) power well (+V3.3S)	Muxed with PCIECLKRQ1#. If not used, requires 8.2-k to 10-k pull-up to +Vcc_3.3 (+V3.3S)
GPIO25	Resume (Sus) well (+V3.3A)	Muxed with PCIECLKREQ3# If not used, requires 8.2-k to 10-k pull-up to +V3.3A rail.

+3V
10K_0402_5% R623 EC_LID_OUT#
2.2K_0402_5% R602 PCH_SMBCLK
2.2K_0402_5% R626 PCH_SMBDATA
10K_0402_5% R208 PCH_GPIO60
2.2K_0402_5% R639 PCH_SML1CLK
2.2K_0402_5% R249 PCH_SML1DAT
10K_0402_5% R207 PCH_GPIO74
10K_0402_5% R244 PCH_GPIO44
10K_0402_5% R206 PCH_GPIO56
10K_0402_5% R257 PCH_GPIO73

+3VS — PCH_SML1CLK — Q19A 2N7002DWH_SOT363-6 — EC_SMB_CK2 — EC_SMB_CK2 22,36

+3VS — Pull high +3VS at KB926 side

PCH_SML1DAT — Q19B 2N7002DWH_SOT363-6 — EC_SMB_DA2 — EC_SMB_DA2 22,36

+3V — 9/1: Change to +3VS
2009/08/13: Change back to +3V
10K_0402_5% R624 PCH_GPIO25

Project Structure

	GPIO21 ID2	GPIO65 ID1	GPIO66 ID0	Structure
	0	0	0	NEW70
	0	0	1	NEW80
	0	1	0	NEW90
*Discrete	1	0	0	NEW71/91
*Optimus	1	1	0	NEW71/91

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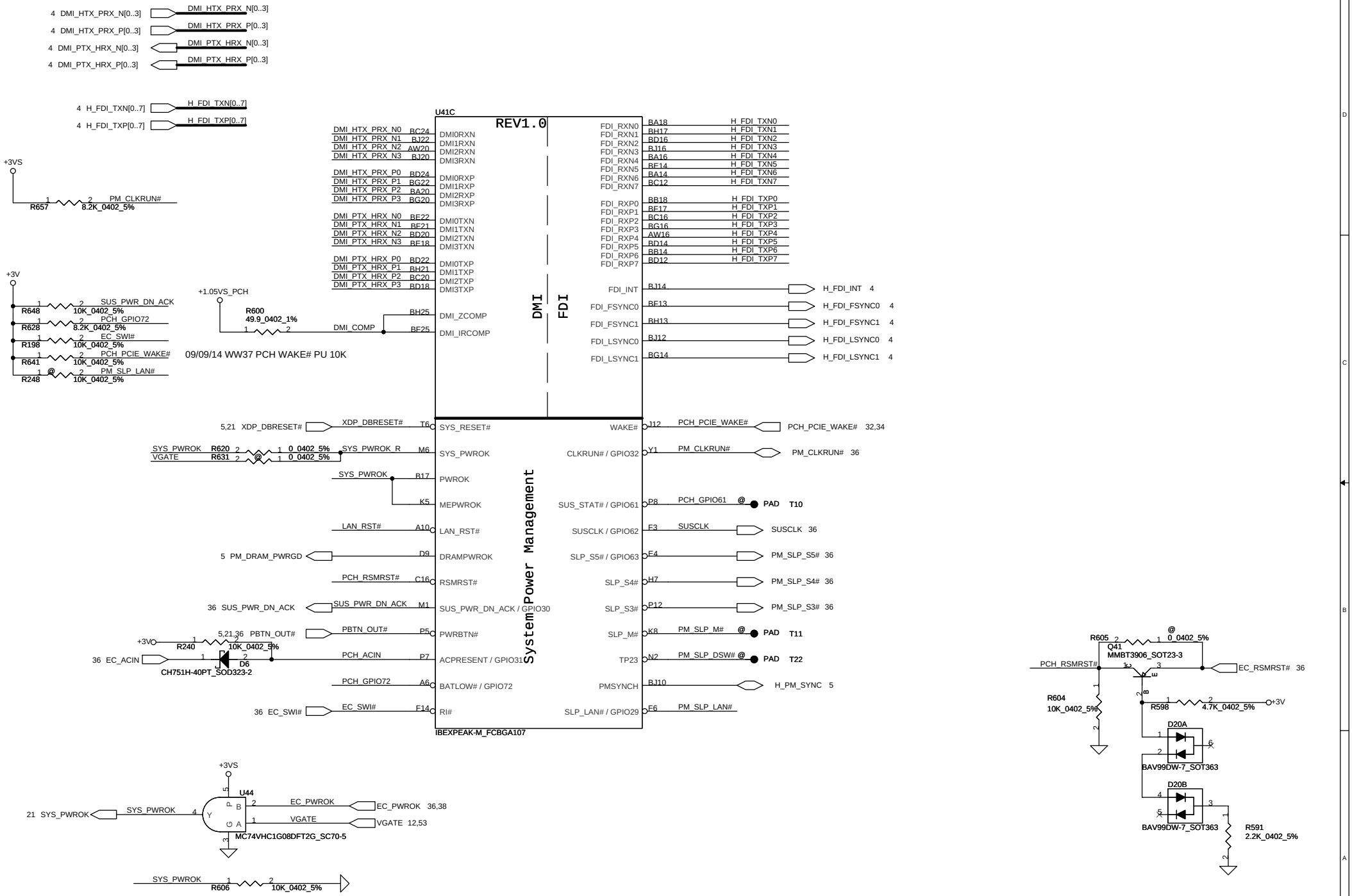

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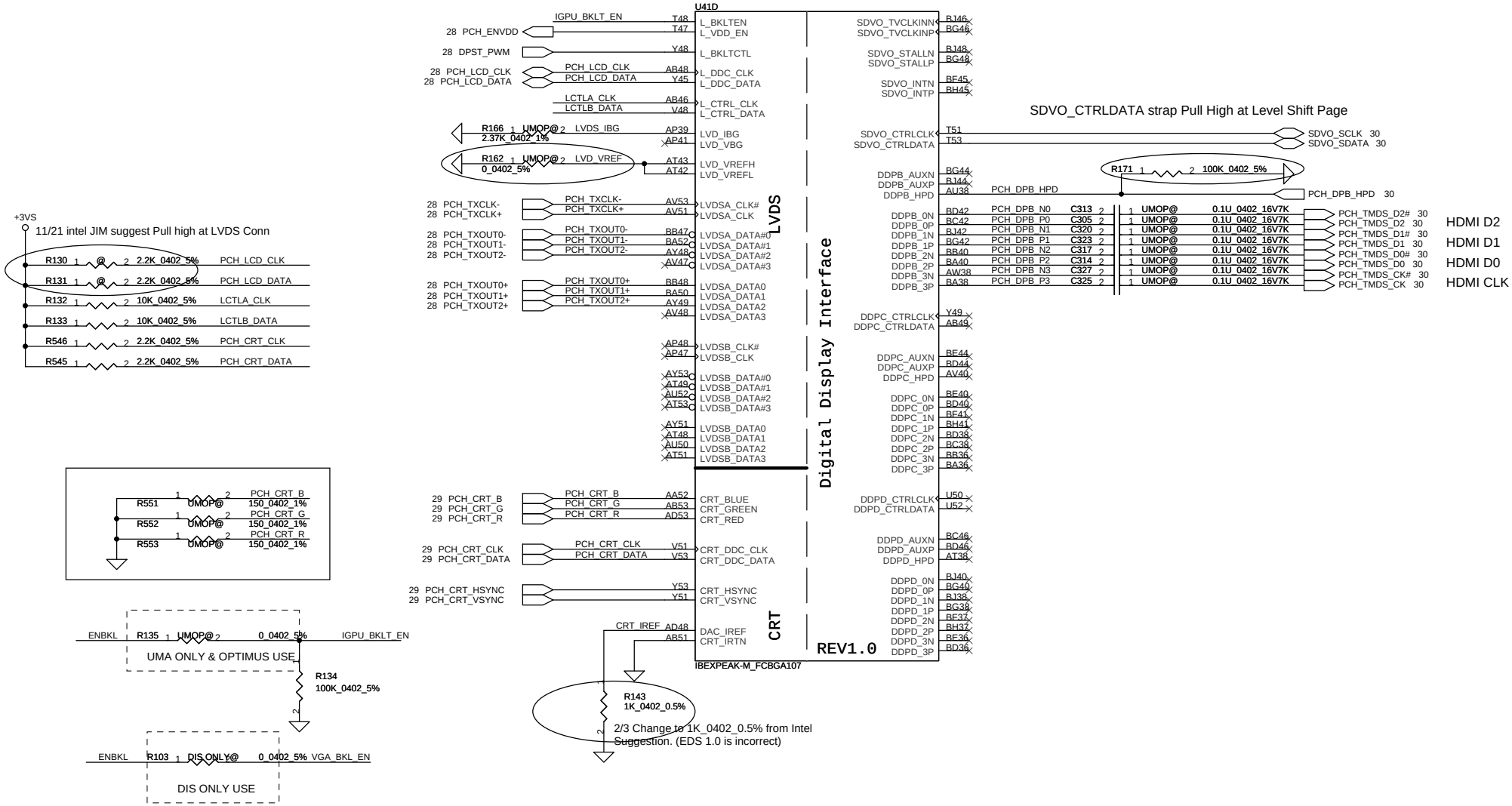

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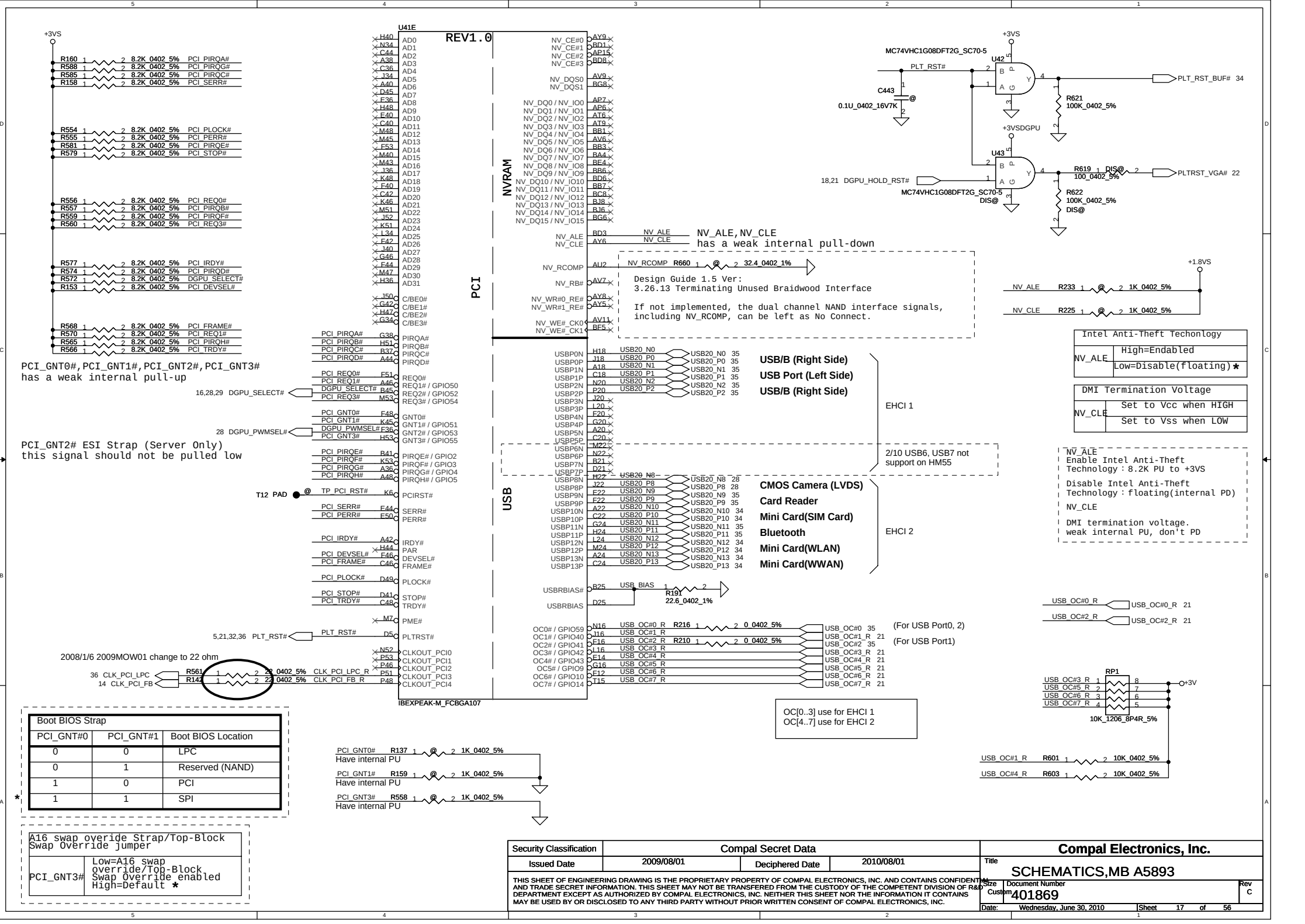

Intel Anti-Theft Techonlogy	
NV_ALE	High=Endabled
	Low=Disable(floating)*

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

NV_ALE
Enable Intel Anti-Theft
Technology : 8.2K PU to +3VS

Disable Intel Anti-Theft
Technology : floating(internal PD)

NV_CLE

DMI termination voltage.
weak internal PU, don't PD

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

*

A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default *

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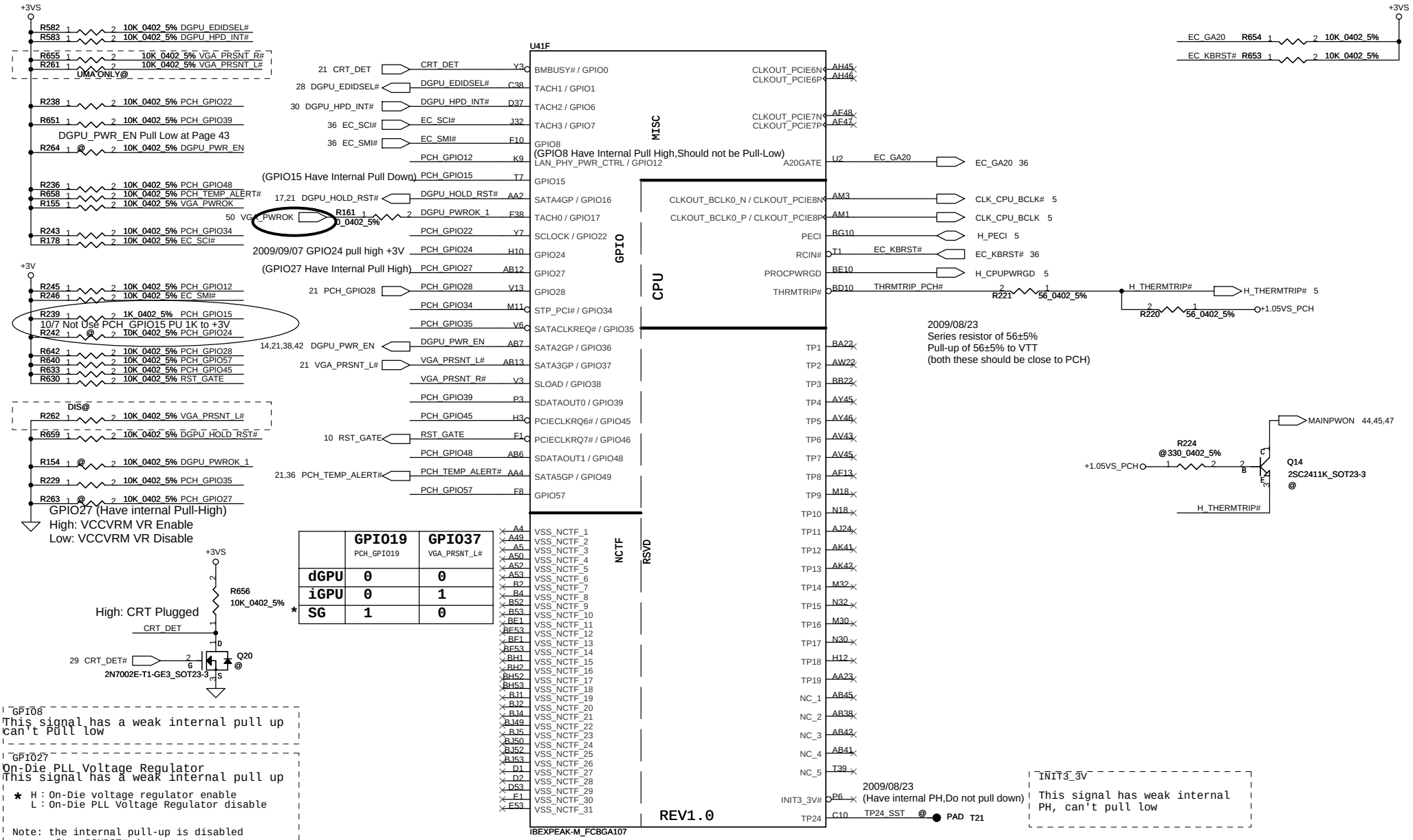

	GPIO19 PCH_GPIO19	GPIO37 VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
* SG	1	0

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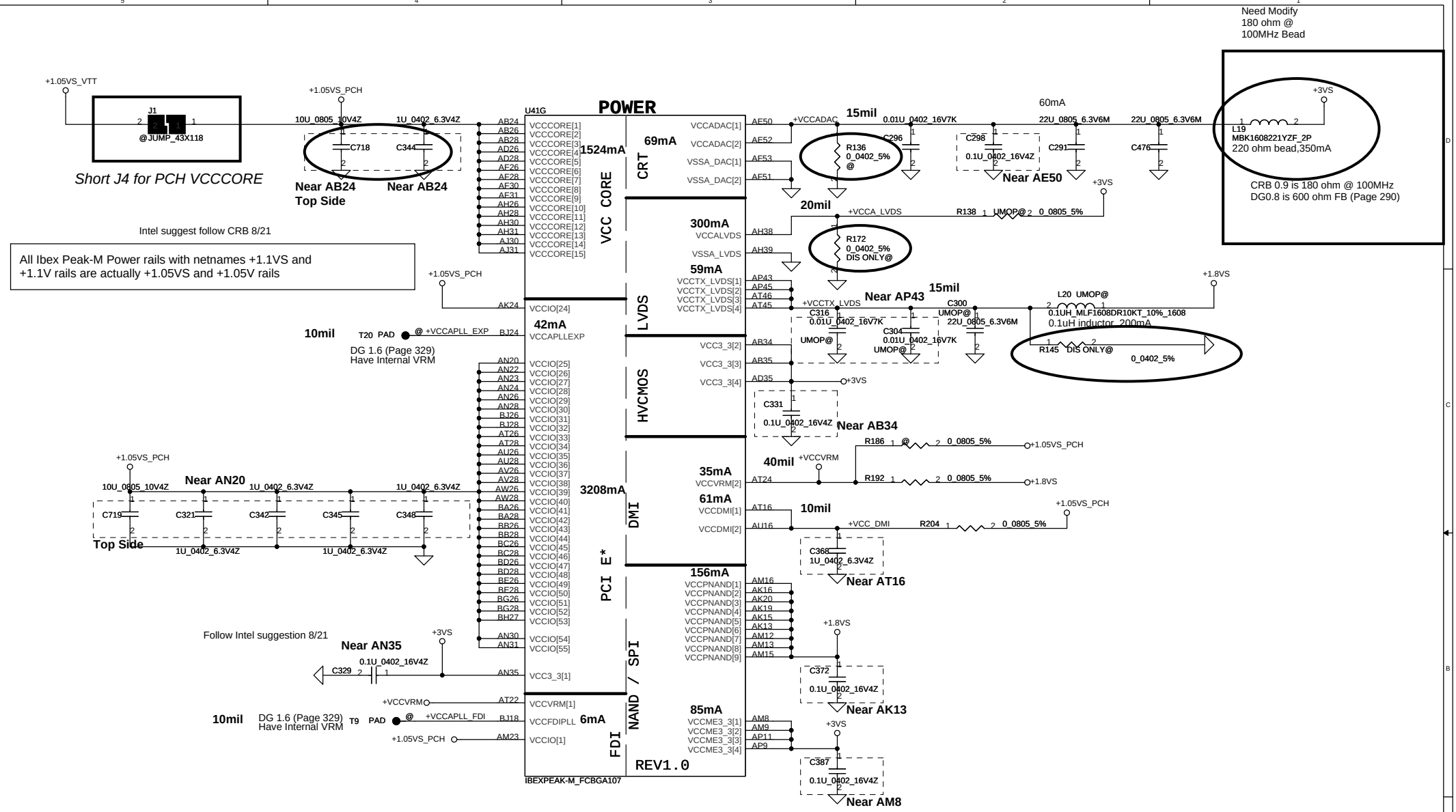

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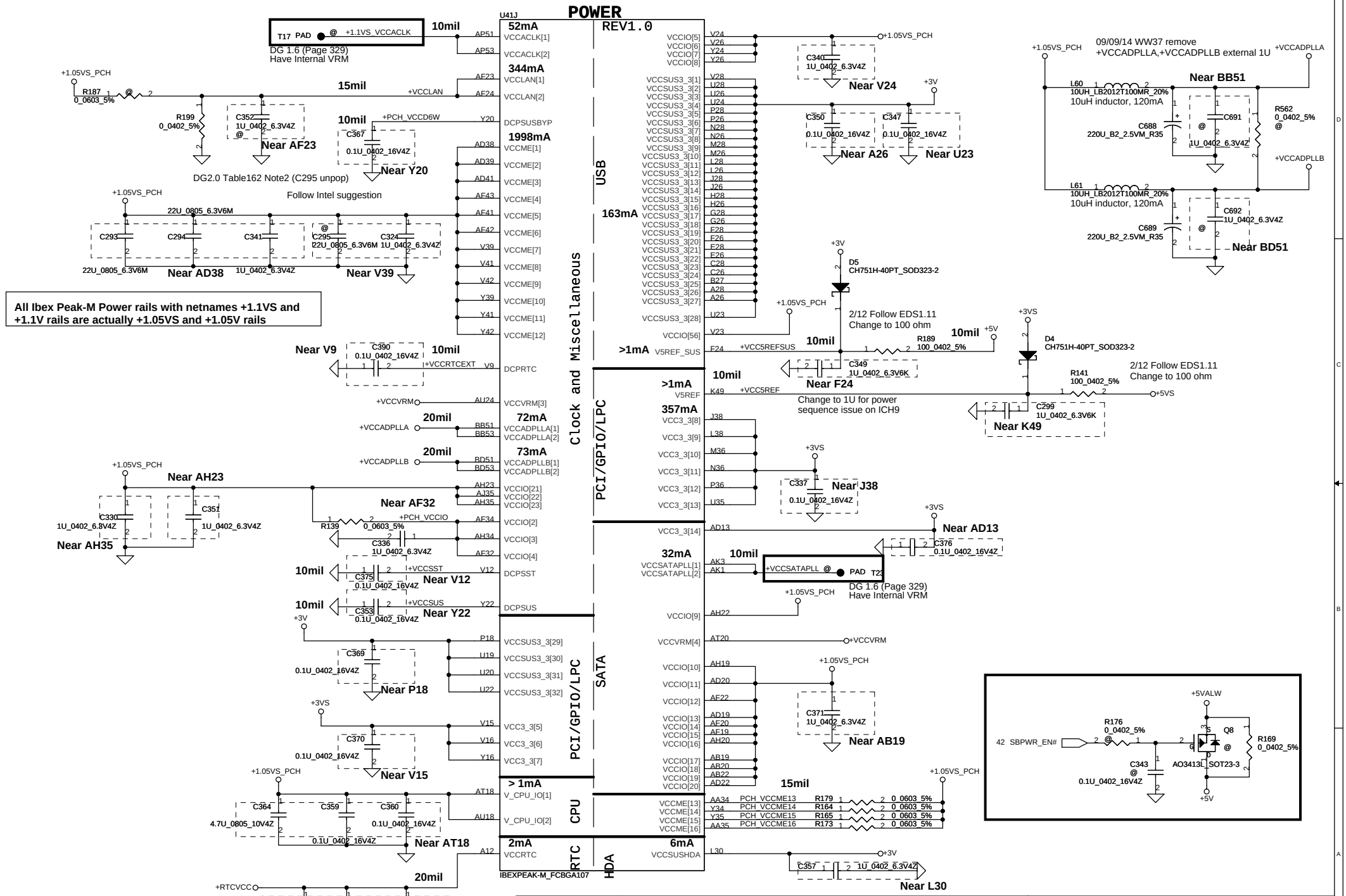

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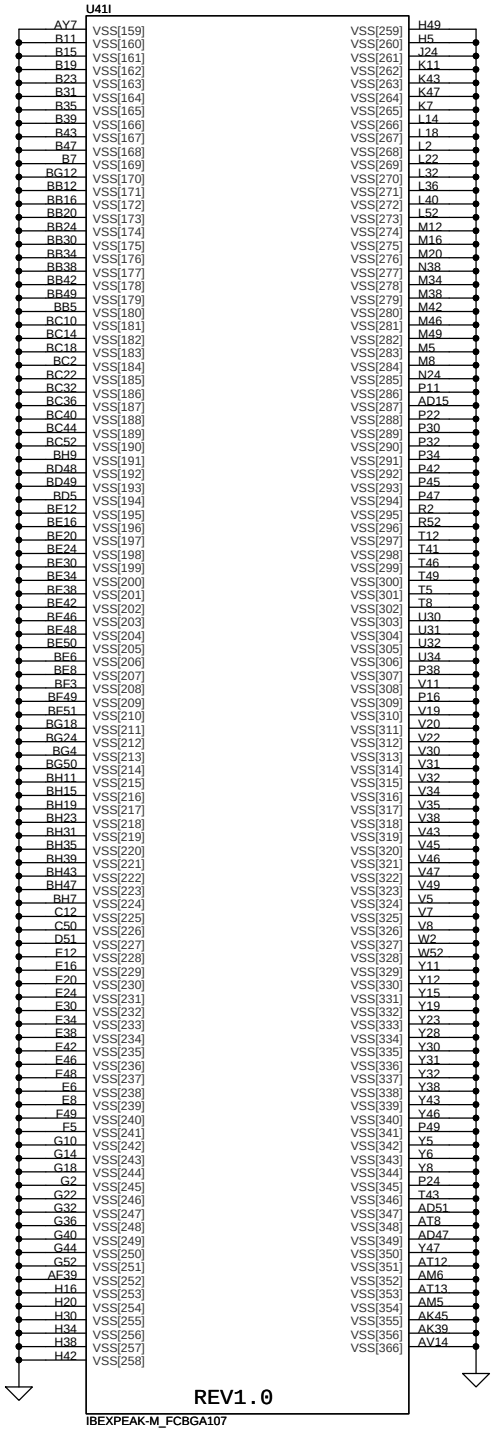
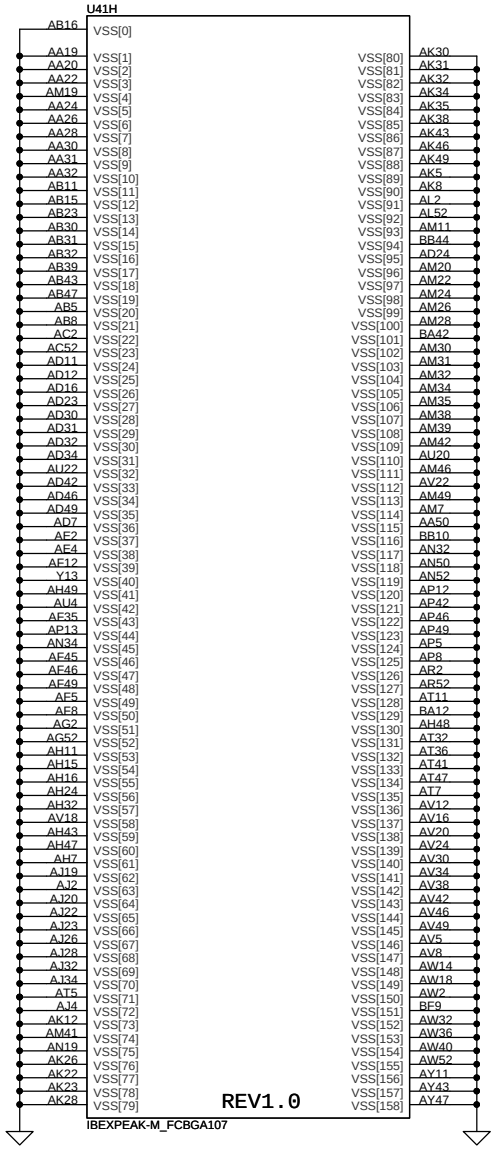
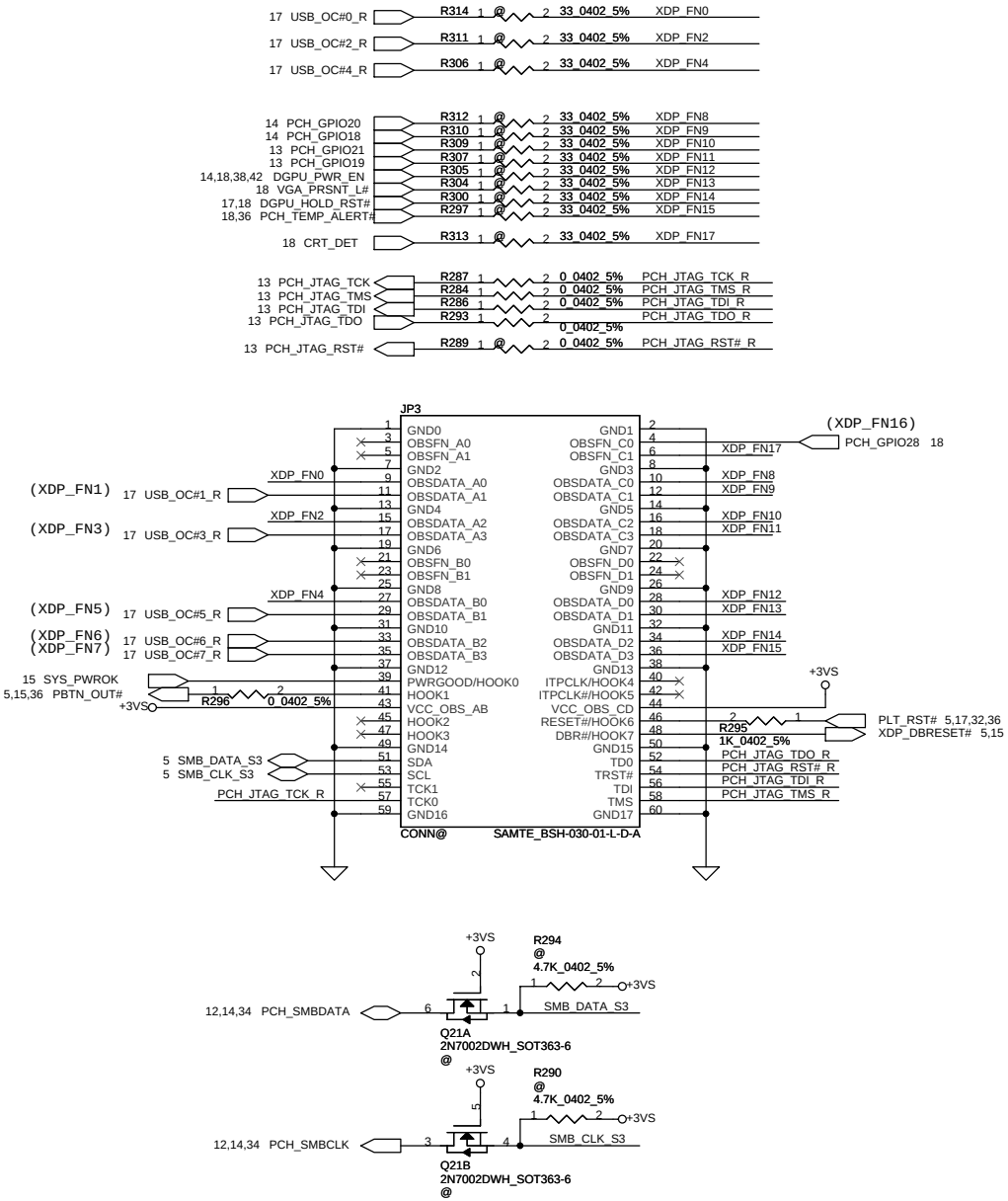
PCH XDP Port







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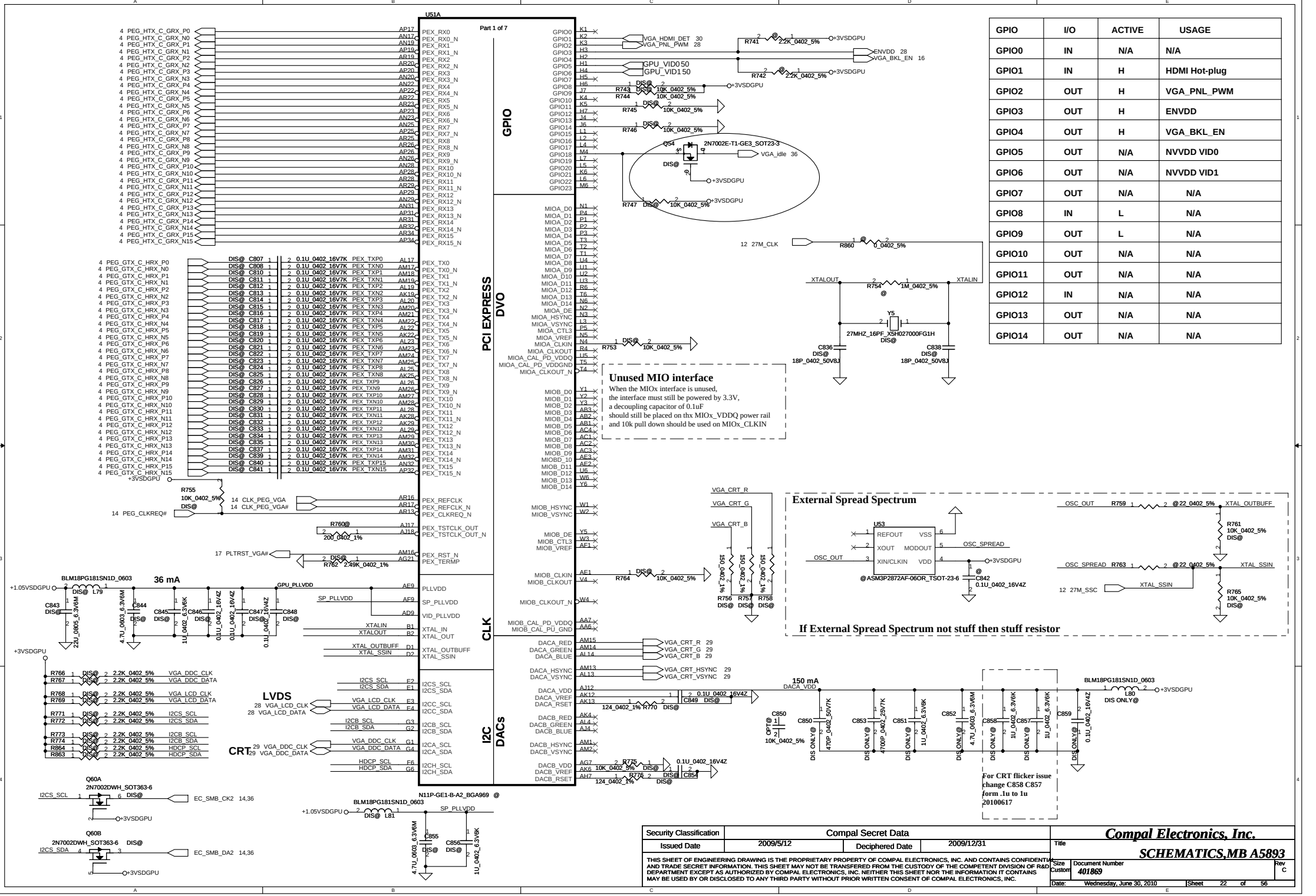

GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_PWM
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	N/A
GPIO8	IN	L	N/A
GPIO9	OUT	L	N/A
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

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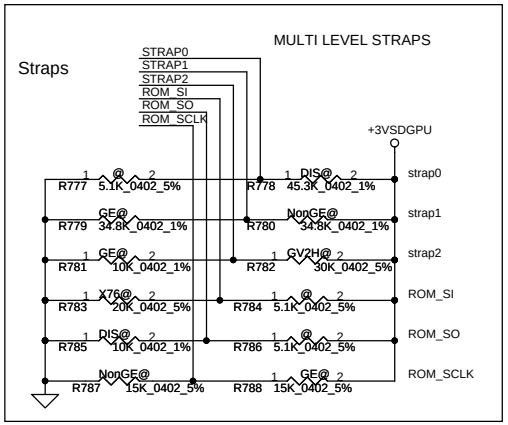
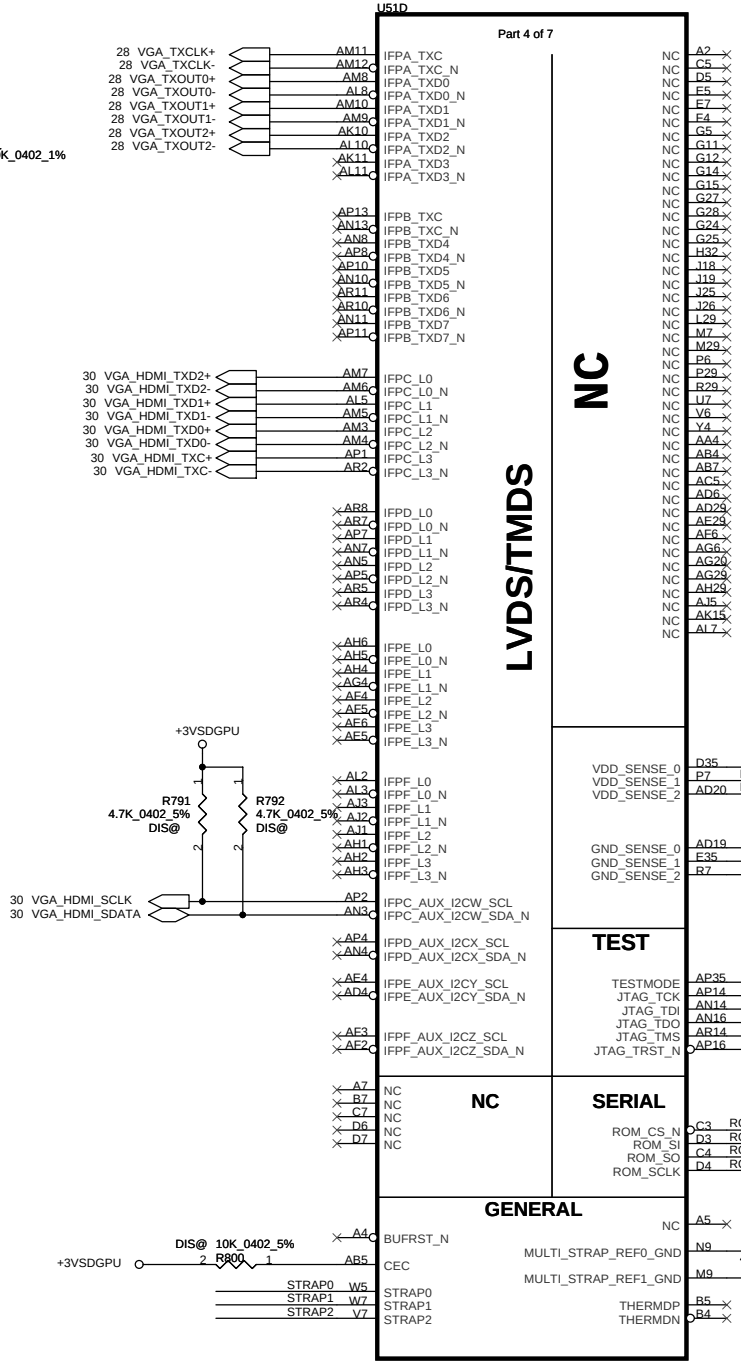


2 GE1@ 1
R782 10K_0402_1%



N11P-GE1-B-A2_BGA969 @

20091214 Modify For GV2H	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035720	H 45K	H 35K	H 30K	L 20K	L 10K	L 15K
64MX16 Hynix SA000032490	H 45K	H 35K	H 30K	L 15K	L 10K	L 15K
20100113 Modify For GE1	**strap0**	**strap1**	**strap2**	**ROM_SI**	**ROM_SO**	**ROM_SCLK**
64MX16 Samsung SA000035720	H 45K	H 35K	H 10K	L 20K	L 10K	L 15K
64MX16 Hynix SA000032490	H 45K	H 35K	H 10K	L 15K	L 10K	L 15K
20100601 Modify For GE	**strap0**	**strap1**	**strap2**	**ROM_SI**	**ROM_SO**	**ROM_SCLK**
64MX16 Samsung SA000035720	H 45K	L 35K	L 10K	L 20K	L 10K	H 15K
64MX16 Hynix SA000032490	H 45K	L 35K	L 10K	L 15K	L 10K	H 15K
128MX16 Samsung SA00003MQ40	H 45K	L 35K	L 10K	L 45K	L 10K	H 15K
128MX16 Hynix SA00003VS10	H 45K	L 35K	L 10K	L 35K	L 10K	H 15K

Mode E Command Mapping GB2-128 Package Femi	Mode C Command Mapping GB1-128 Package	Data Bit	0..31	32..63
FBx_CMD3	FBx_CMD0	CKE_L		
FBx_CMD8	FBx_CMD1	A8	A8	
FBx_CMD2	FBx_CMD2	CS0_L*		
FBx_CMD21	FBx_CMD3	A7	A6	
FBx_CMD24	FBx_CMD4	A2	A1	
FBx_CMD23	FBx_CMD5	A11	A9	
FBx_CMD26	FBx_CMD6	A5	A4	
FBx_CMD7	FBx_CMD7	A0	A12	
FBx_CMD15	FBx_CMD8	CAS*	CAS*	
FBx_CMD13	FBx_CMD9	BA1	A3	
FBx_CMD4	FBx_CMD10	A9	A11	
FBx_CMD18	FBx_CMD11		CS0_H	
FBx_CMD29	FBx_CMD12	BA0	BA0	
FBx_CMD27	FBx_CMD13	BA2	A15	
FBx_CMD6	FBx_CMD14	A3	BA1	
FBx_CMD17	FBx_CMD15		CS1_H	
FBx_CMD19	FBx_CMD16		ODT_H	
FBx_CMD22	FBx_CMD17	A4	A5	
FBx_CMD12	FBx_CMD18	A13	A14	
FBx_CMD28	FBx_CMD19	WE*	A10	
FBx_CMD10	FBx_CMD20	A1	A2	
FBx_CMD25	FBx_CMD21	A10	WE*	
FBx_CMD9	FBx_CMD22	A12	A0	
FBx_CMD1	FBx_CMD23	CS1_L*		
FBx_CMD11	FBx_CMD24	RAS*	RAS*	
FBx_CMD0	FBx_CMD25	ODT_L		
FBx_CMD5	FBx_CMD26	A6	A7	
FBx_CMD16	FBx_CMD27		CKE_H	
FBx_CMD20	FBx_CMD28	RST	RST	
FBx_CMD14	FBx_CMD29	A14	A13	
FBx_CMD30	FBx_CMD30	A15	BA2	
FBx_CMD31				
			LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

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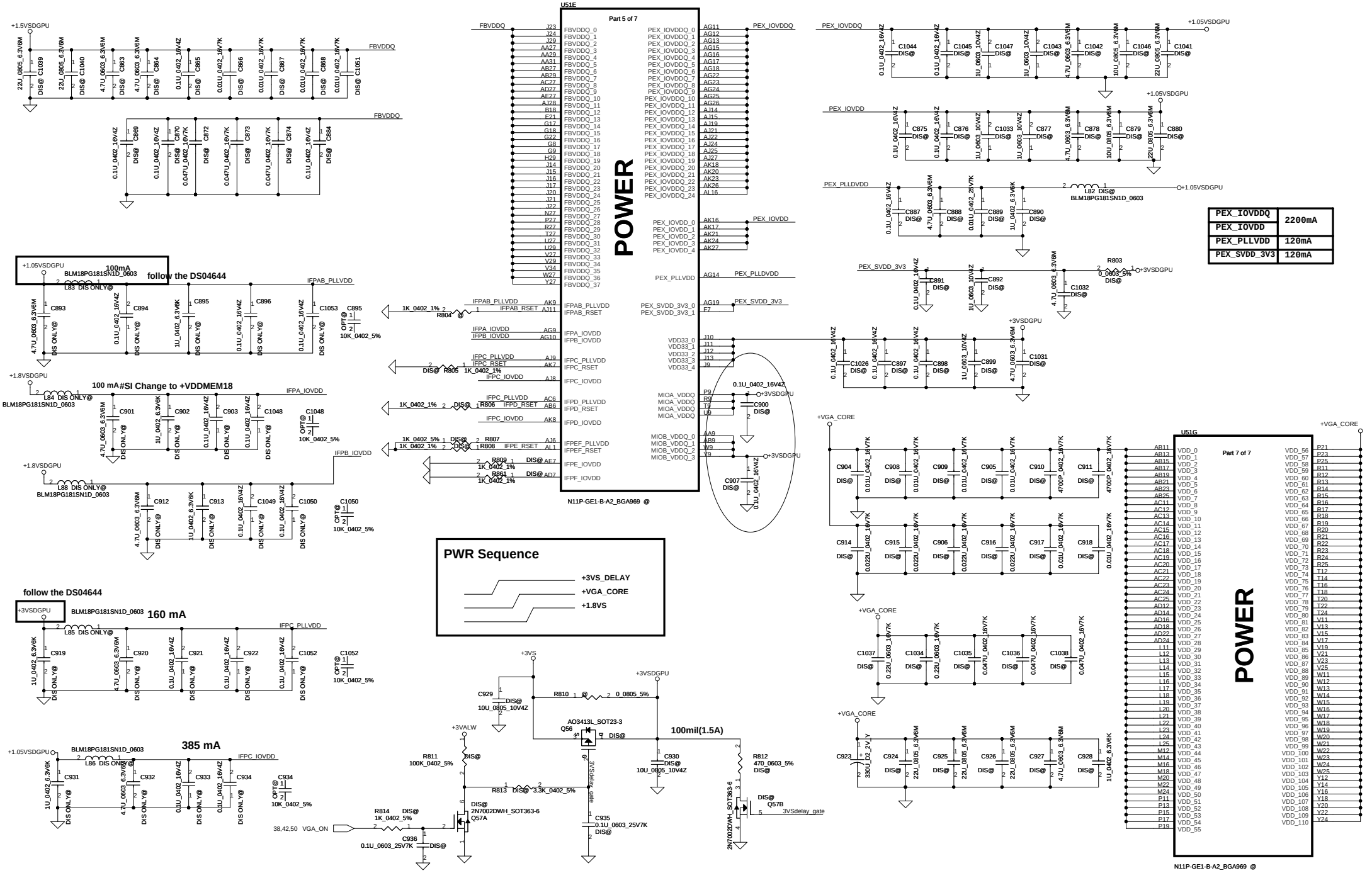
Date: Wednesday, June 30, 2010 | Sheet 23 of 56



PEX_IOVDDQ	2200mA
PEX_IOVDD	
PEX_PLLVDD	120mA
PEX_SVDD_3V3	120mA

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Issued Date	2009/5/12	Deciphered Date	2009/12/31

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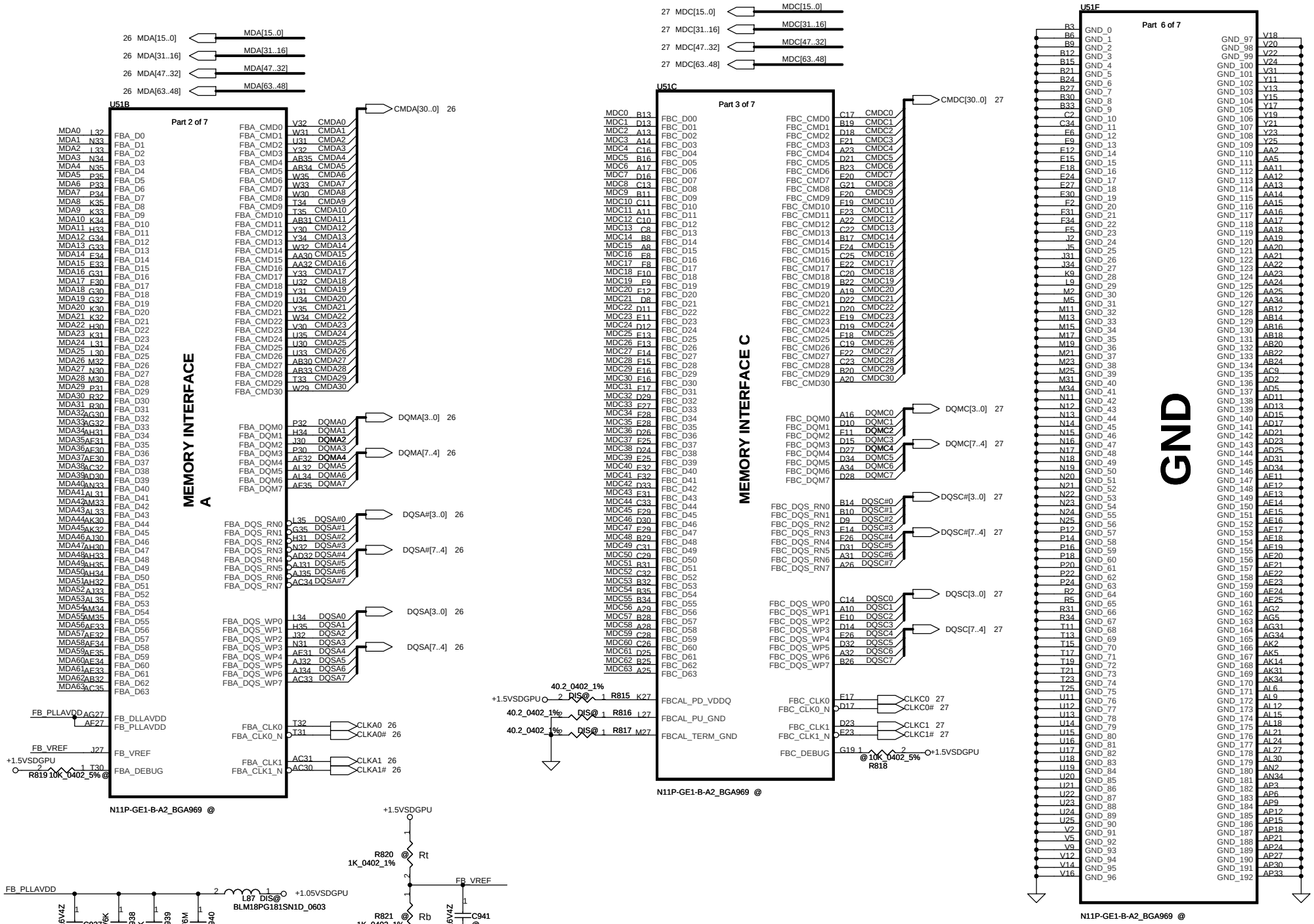
Date: Wednesday, June 30, 2010 | Sheet 24 of 56

VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

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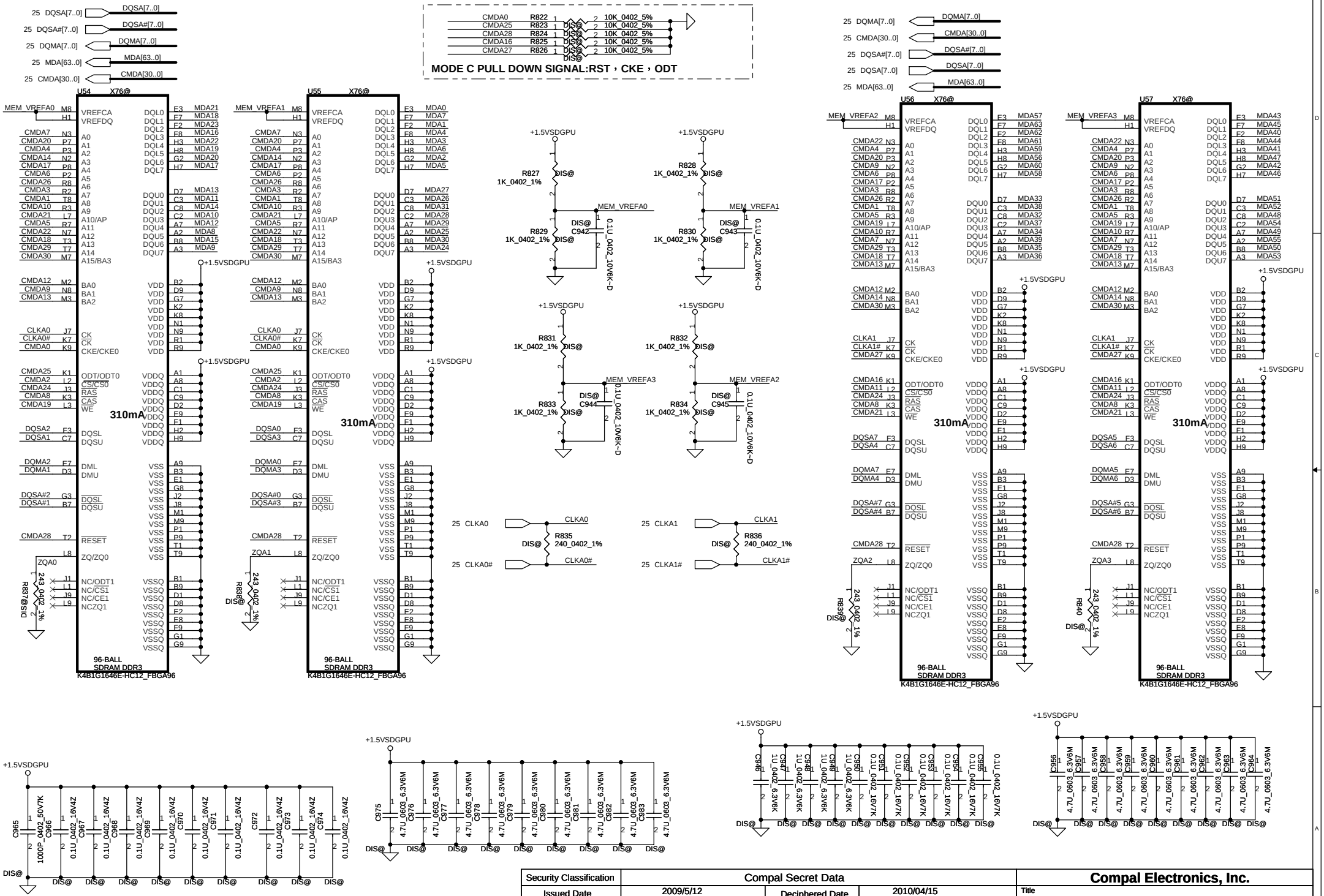
Date: Wednesday, June 30, 2010 | Sheet 25 of 56



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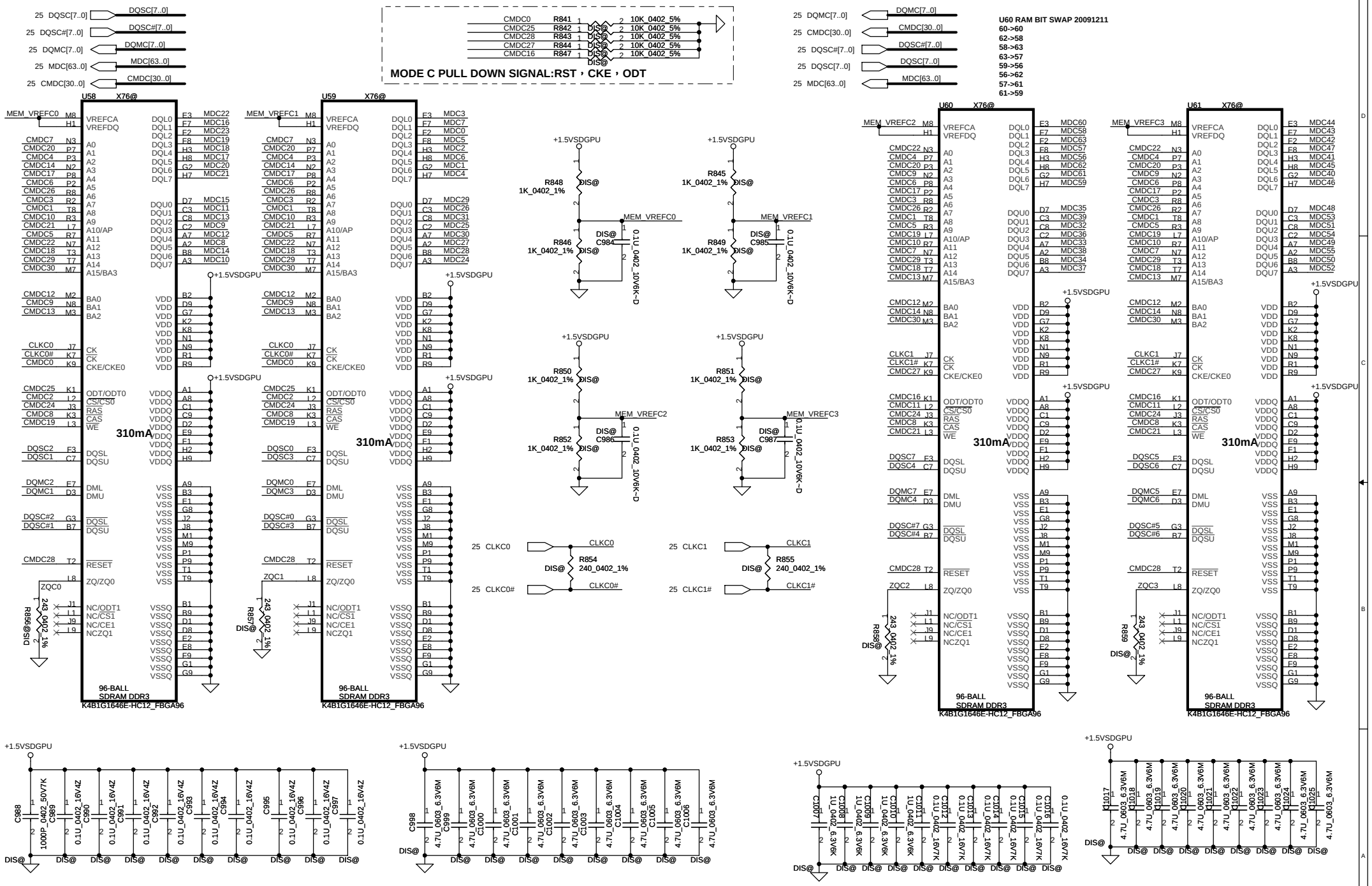
Date: Wednesday, June 30, 2010 | Sheet 26 of 56



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Issued Date	2009/5/12	Deciphered Date	2010/04/15

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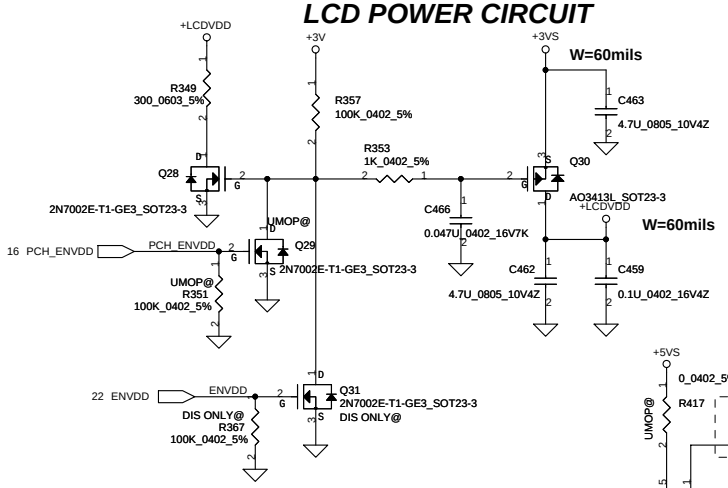
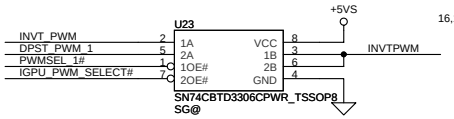
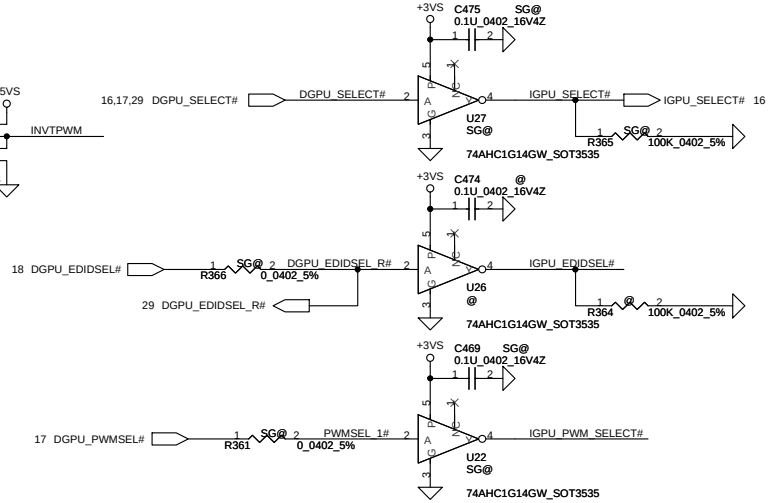
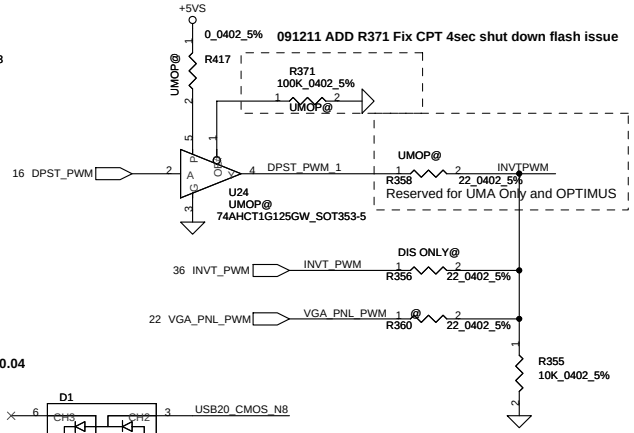
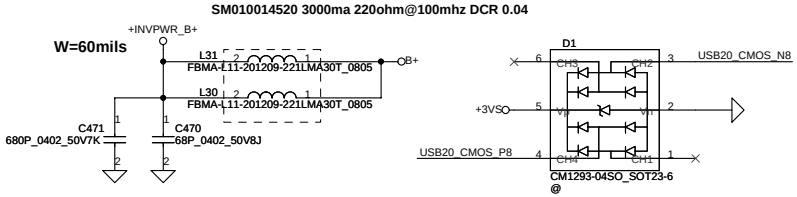
LCD POWER CIRCUIT



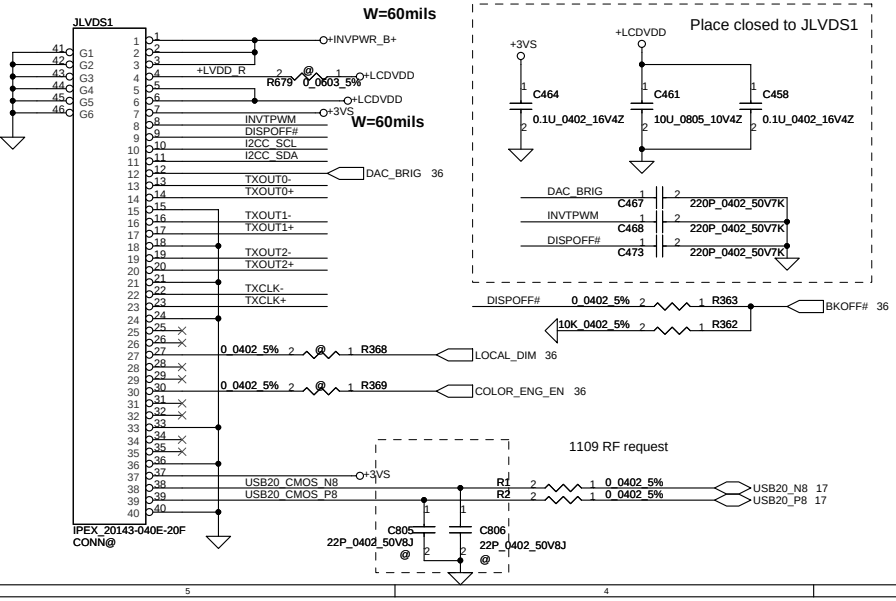








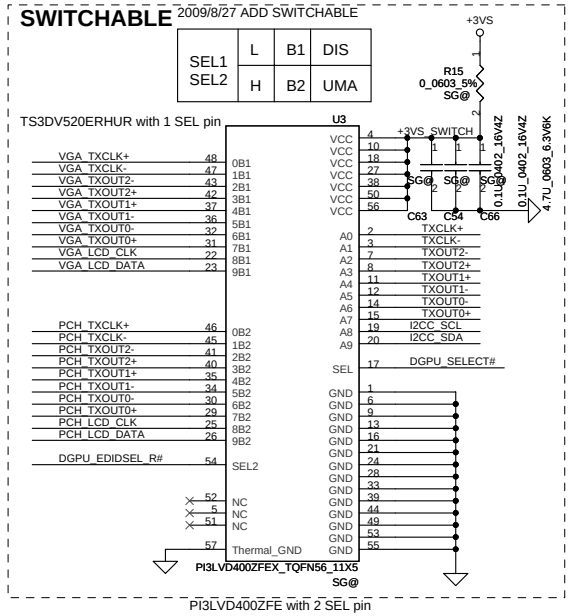
LCD/LED PANEL Conn.



SWITCHABLE

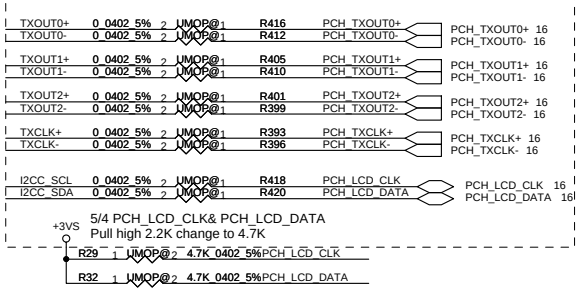
2009/8/27 ADD SWITCHABLE

SEL1	L	B1	DIS
SEL2	H	B2	UMA



PI3LVD400ZFE with 2 SEL pin

UMA ONLY / Optimus



Discrete ONLY

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Issued Date	2009/08/01	Deciphered Date	2010/08/01

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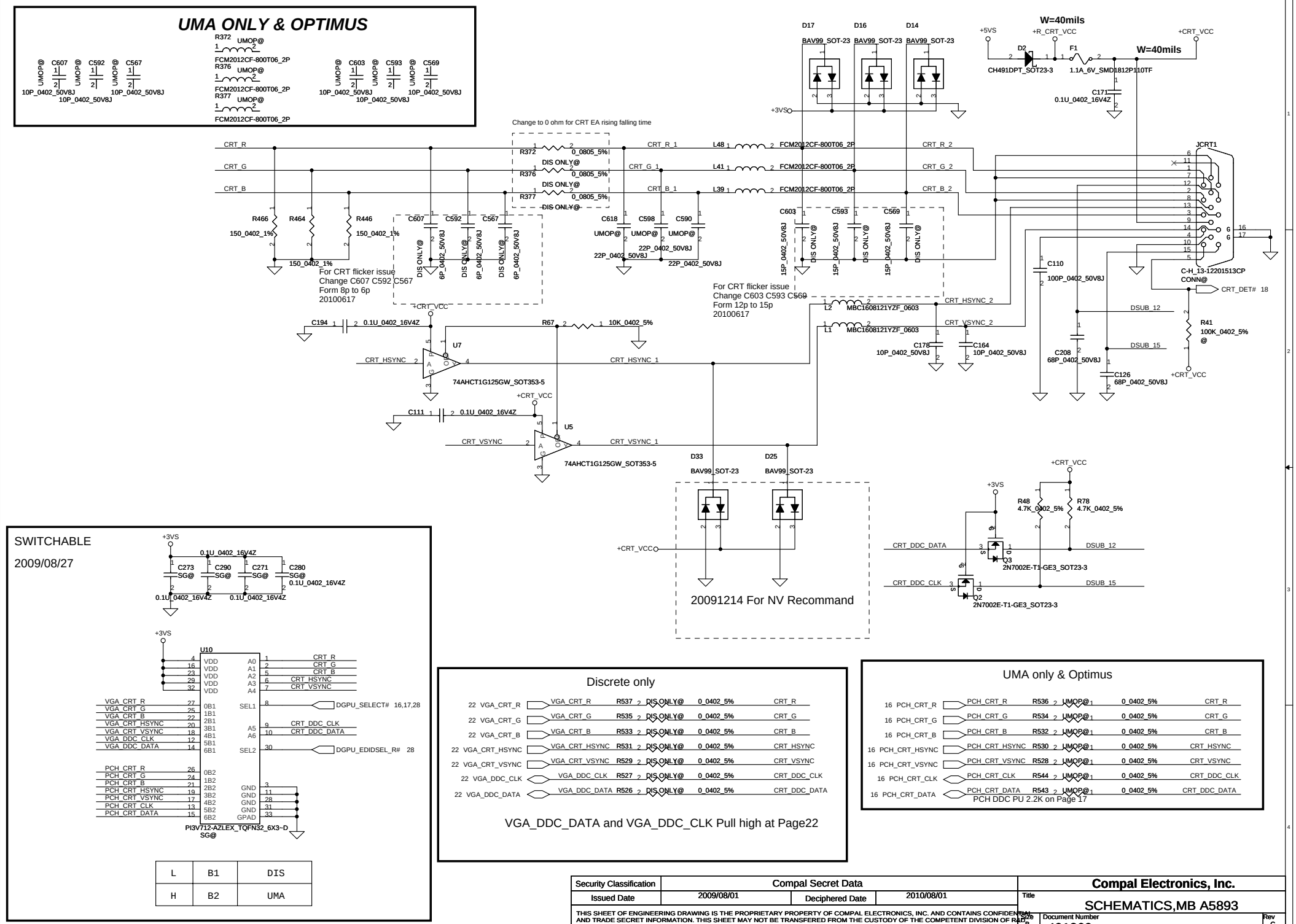
UMA ONLY & OPTIMUS
R372 UMOP@ FCM2012CF-800T06_2P
R376 UMOP@ FCM2012CF-800T06_2P
R377 UMOP@ FCM2012CF-800T06_2P
C607 UMOP@ 10P_0402_50V8J
C592 UMOP@ 10P_0402_50V8J
C567 UMOP@ 10P_0402_50V8J
C603 UMOP@ 10P_0402_50V8J
C593 UMOP@ 10P_0402_50V8J
C569 UMOP@ 10P_0402_50V8J
Change to 0 ohm for CRT EA rising falling time
R372 0_0805_5% DIS ONLY@
R376 0_0805_5% DIS ONLY@
R377 0_0805_5% DIS ONLY@
CRT_R
CRT_G
CRT_B
CRT_R_1
CRT_G_1
CRT_B_1
L48 FCM2012CF-800T06_2P
L41 FCM2012CF-800T06_2P
L39 FCM2012CF-800T06_2P
CRT_R_2
CRT_G_2
CRT_B_2
D17 BAV99_SOT-23
D16 BAV99_SOT-23
D14 BAV99_SOT-23
+3VS
+5VS
+R_CRT_VCC
+CRT_VCC
W=40mils
D2 CH491DPT_SOT23-3
F1 1.1A_6V_SMD1812P110TF
C171 0.1U_0402_16V4Z
JCRT1
C-H_13-12201513CP
CONN@
CRT_DET# 18
R466 150_0402_1%
R464 150_0402_1%
R446 150_0402_1%
C607 DIS ONLY@ 6P_0402_50V8J
C592 DIS ONLY@ 6P_0402_50V8J
C567 DIS ONLY@ 6P_0402_50V8J
For CRT flicker issue
Change C607 C592 C567
Form 8p to 6p
20100617
C618 UMOP@ 22P_0402_50V8J
C598 UMOP@ 22P_0402_50V8J
C590 UMOP@ 22P_0402_50V8J
C603 DIS ONLY@ 15P_0402_50V8J
C593 DIS ONLY@ 15P_0402_50V8J
C569 DIS ONLY@ 15P_0402_50V8J
For CRT flicker issue
Change C603 C593 C569
Form 12p to 15p
20100617
C110 100P_0402_50V8J
C208 68P_0402_50V8J
C126 68P_0402_50V8J
DSUB_12
DSUB_15
R41 100K_0402_5% @
C194 0.1U_0402_16V4Z
R67 10K_0402_5%
U7 74AHCT1G125GW_SOT353-5
CRT_HSYNC
CRT_HSYNC_1
CRT_HSYNC_2
L2 MBC1608121YZF_0603
L1 MBC1608121YZF_0603
CRT_VSYNC_2
C178 10P_0402_50V8J
C164 10P_0402_50V8J
C111 0.1U_0402_16V4Z
U5 74AHCT1G125GW_SOT353-5
CRT_VSYNC
CRT_VSYNC_1
D33 BAV99_SOT-23
D25 BAV99_SOT-23
20091214 For NV Recommand
R48 4.7K_0402_5%
R78 4.7K_0402_5%
CRT_DDC_DATA
CRT_DDC_CLK
Q3 2N7002E-T1-GE3_SOT23-3
Q2 2N7002E-T1-GE3_SOT23-3
SWITCHABLE
2009/08/27
C273 SG@ 0.1U_0402_16V4Z
C290 SG@ 0.1U_0402_16V4Z
C271 SG@ 0.1U_0402_16V4Z
C280 SG@ 0.1U_0402_16V4Z
U10 PI3V712-AZLEX_TQFN32_6X3-D SG@
VGA_CRT_R
VGA_CRT_G
VGA_CRT_B
VGA_CRT_HSYNC
VGA_CRT_VSYNC
VGA_DDC_CLK
VGA_DDC_DATA
PCH_CRT_R
PCH_CRT_G
PCH_CRT_B
PCH_CRT_HSYNC
PCH_CRT_VSYNC
PCH_CRT_CLK
PCH_CRT_DATA
DGPU_SELECT# 16,17,28
DGPU_EDIDSEL_R# 28
L B1 DIS
H B2 UMA
Discrete only
22 VGA_CRT_R R537 DIS ONLY@ 0_0402_5% CRT_R
22 VGA_CRT_G R535 DIS ONLY@ 0_0402_5% CRT_G
22 VGA_CRT_B R533 DIS ONLY@ 0_0402_5% CRT_B
22 VGA_CRT_HSYNC R531 DIS ONLY@ 0_0402_5% CRT_HSYNC
22 VGA_CRT_VSYNC R529 DIS ONLY@ 0_0402_5% CRT_VSYNC
22 VGA_DDC_CLK R527 DIS ONLY@ 0_0402_5% CRT_DDC_CLK
22 VGA_DDC_DATA R526 DIS ONLY@ 0_0402_5% CRT_DDC_DATA
VGA_DDC_DATA and VGA_DDC_CLK Pull high at Page22
UMA only & Optimus
16 PCH_CRT_R R536 UMOP@ 0_0402_5% CRT_R
16 PCH_CRT_G R534 UMOP@ 0_0402_5% CRT_G
16 PCH_CRT_B R532 UMOP@ 0_0402_5% CRT_B
16 PCH_CRT_HSYNC R530 UMOP@ 0_0402_5% CRT_HSYNC
16 PCH_CRT_VSYNC R528 UMOP@ 0_0402_5% CRT_VSYNC
16 PCH_CRT_CLK R544 UMOP@ 0_0402_5% CRT_DDC_CLK
16 PCH_CRT_DATA R543 UMOP@ 0_0402_5% CRT_DDC_DATA
PCH DDC PU 2.2K on Page 17
Security Classification Compal Secret Data
Issued Date 2009/08/01 Deciphered Date 2010/08/01
Compal Electronics, Inc.
Title SCHEMATICS,MB A5893
Size B Document Number 401869 Rev C
Date: Wednesday, June 30, 2010 Sheet 29 of 56
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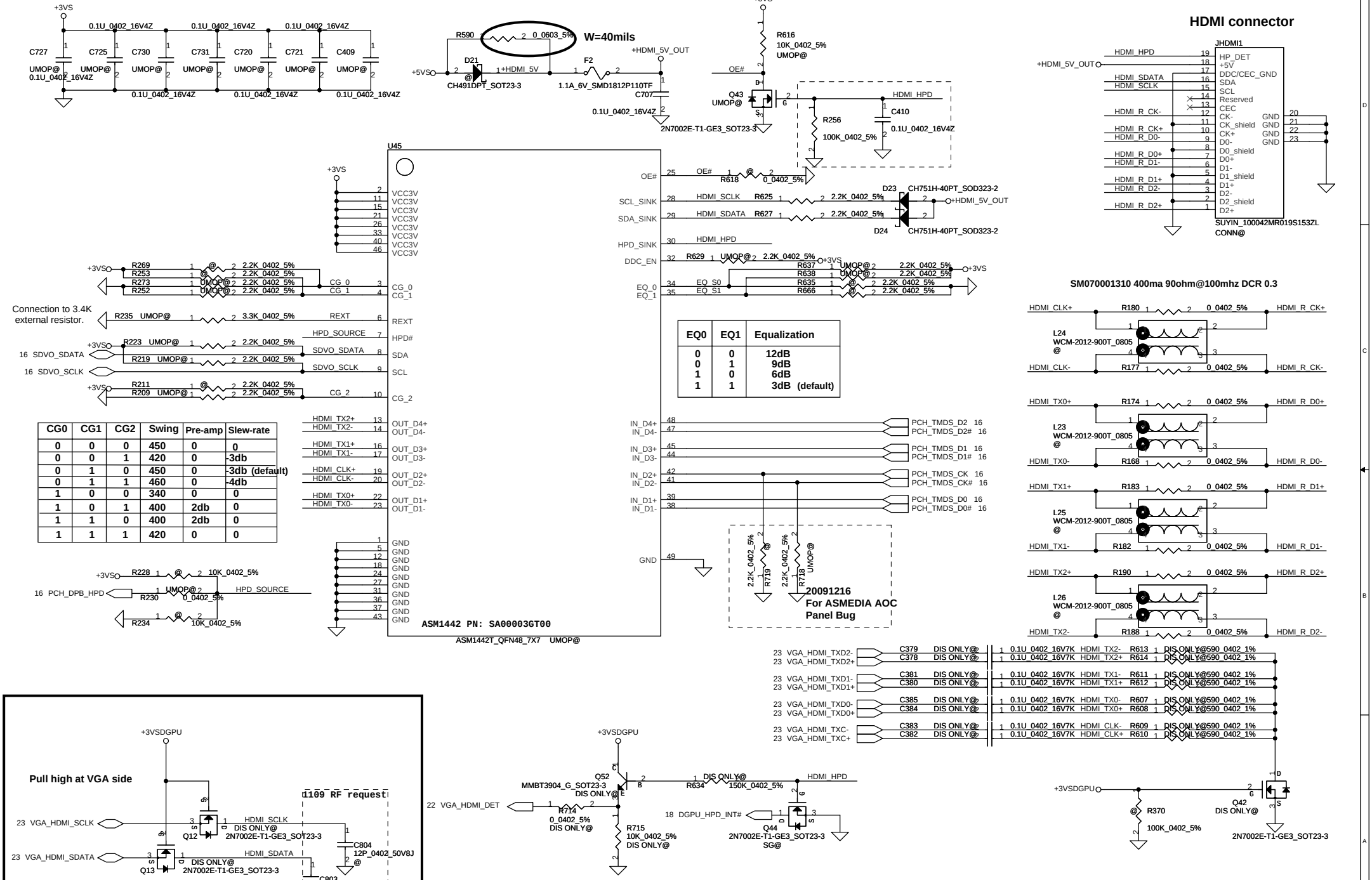

EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

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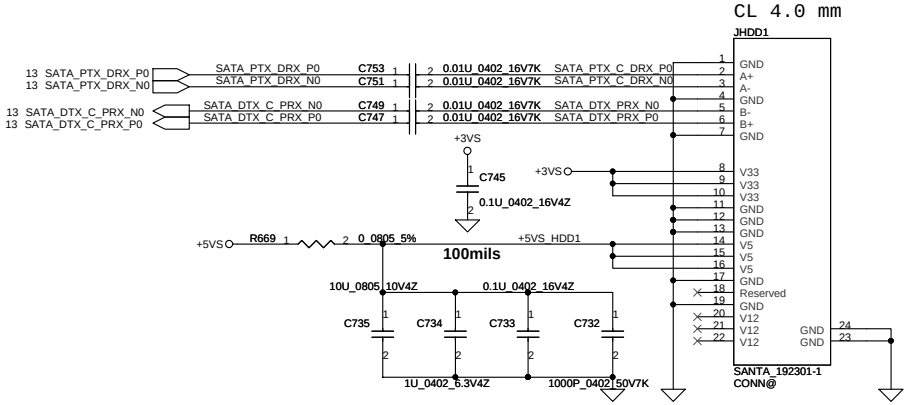
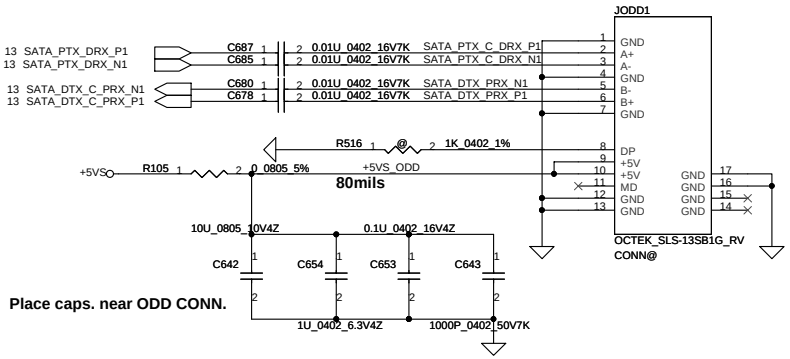
SATA HDD1 Conn.



SATA ODD Conn.



Place caps. near ODD CONN.

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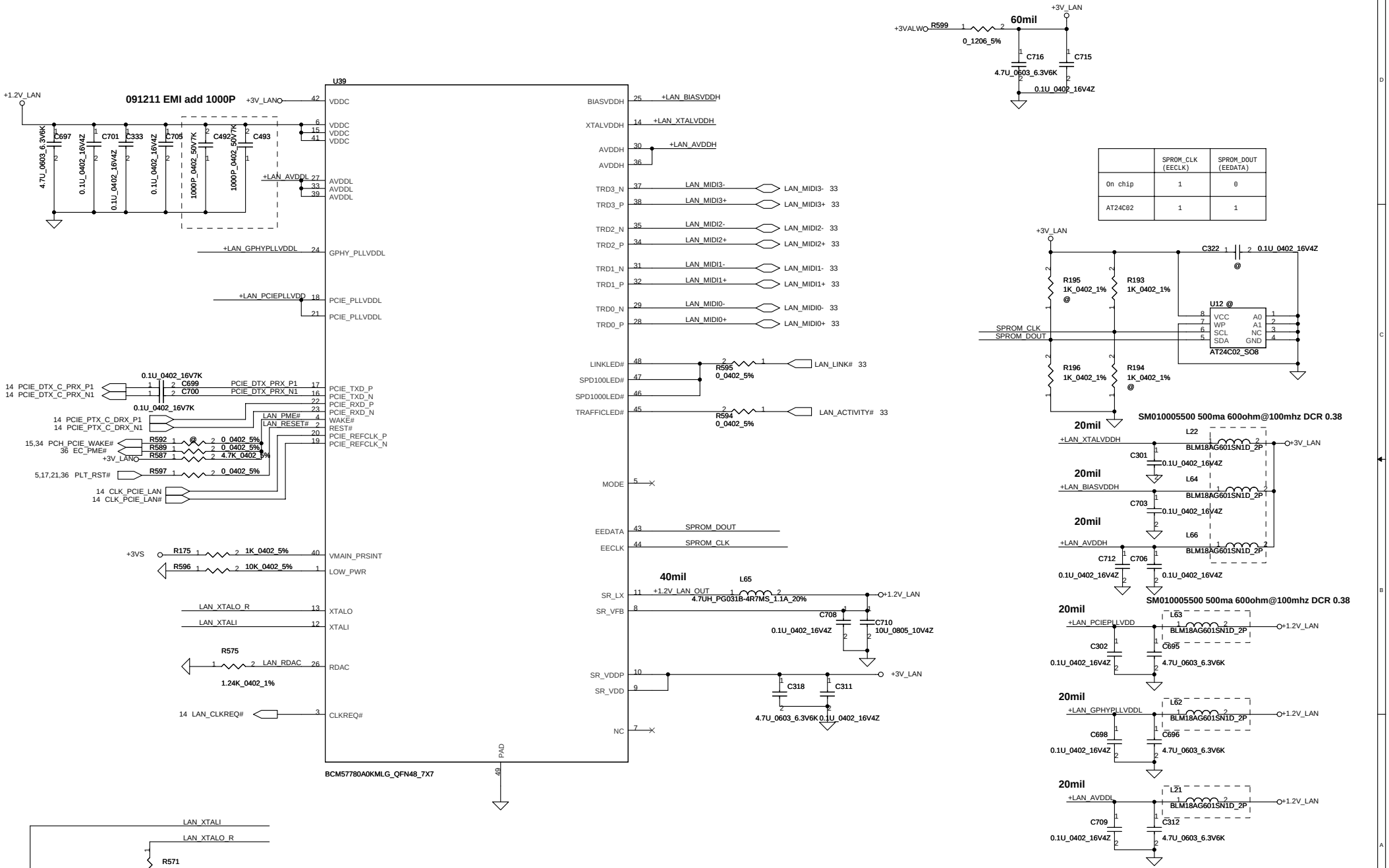
				Date: Wednesday, June 30, 2010 / Sheet 31 of 56



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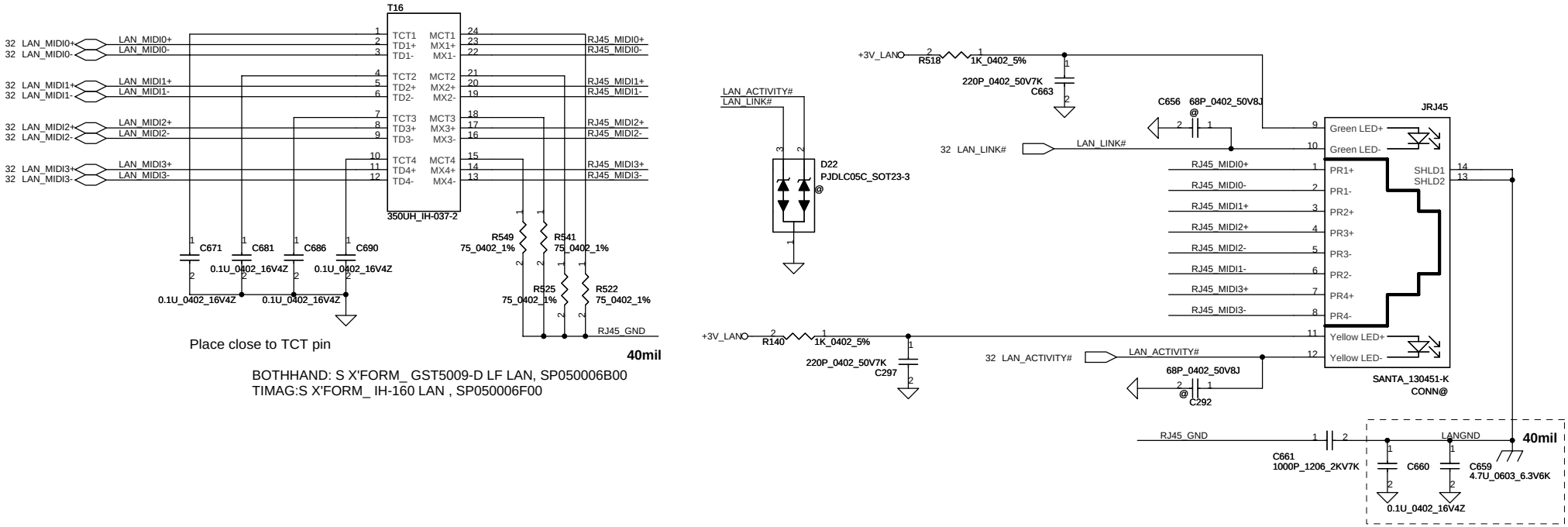
LAN Connector



Place close to TCT pin

BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00

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				Size: Custom; Document Number: 401869; Rev: C
				Date: Wednesday, June 30, 2010; Sheet 33 of 56

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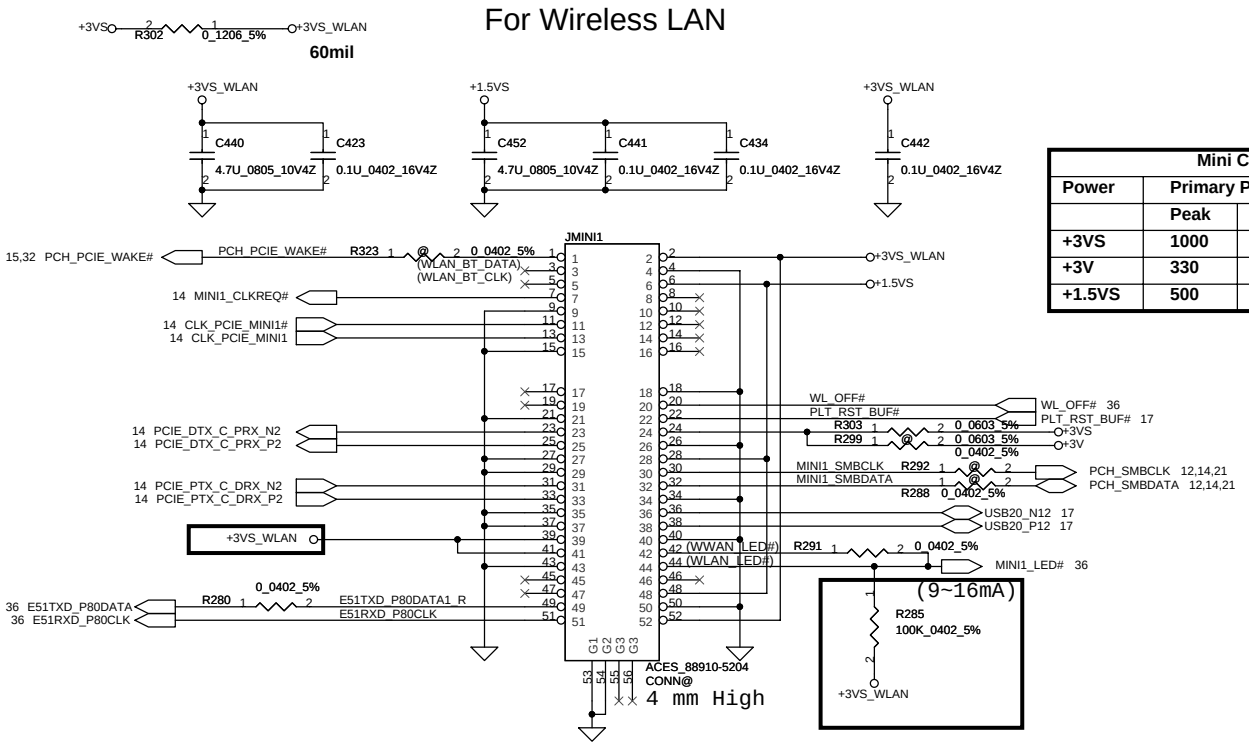
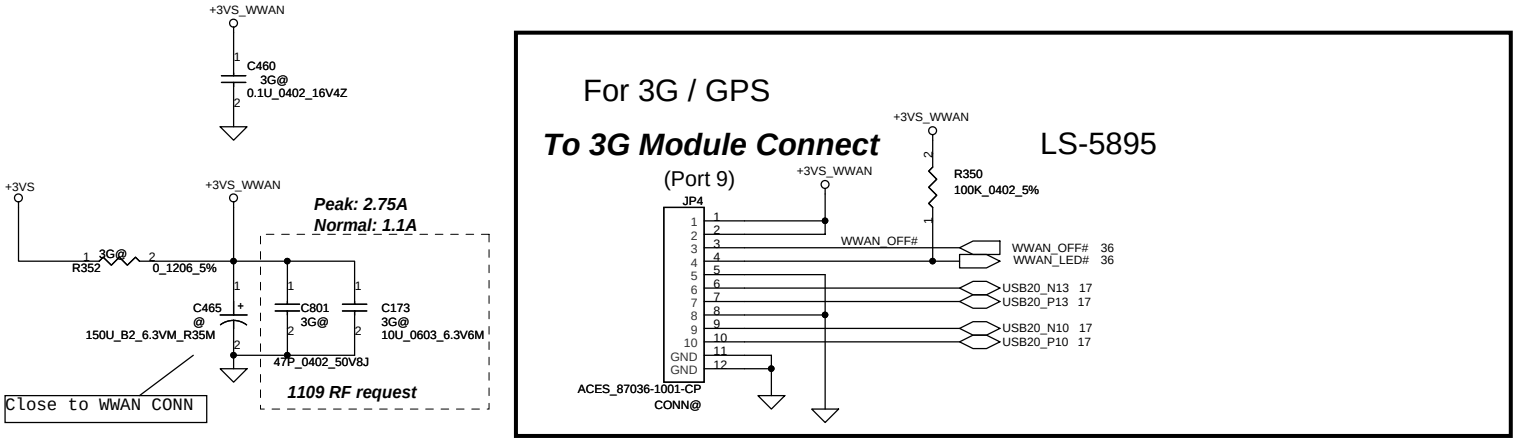
For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



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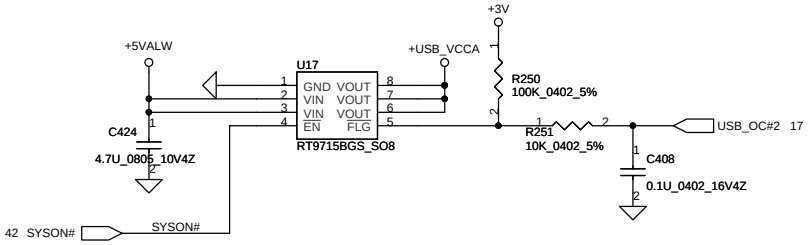
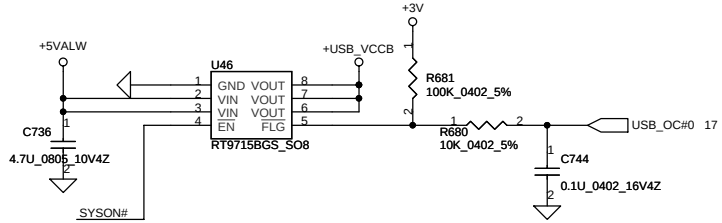
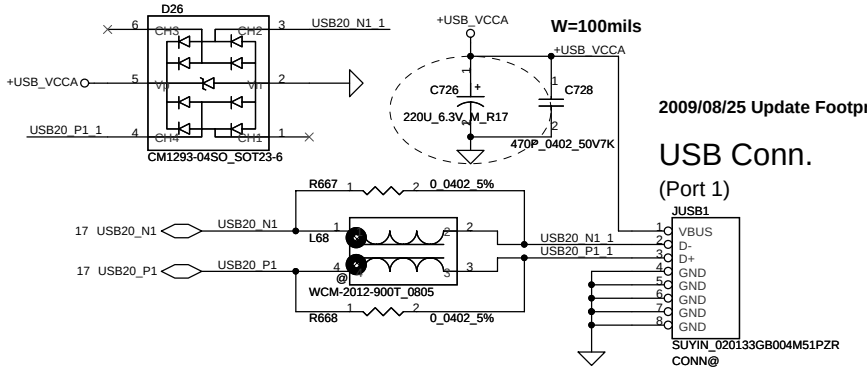




2009/08/14 CHANGE cap



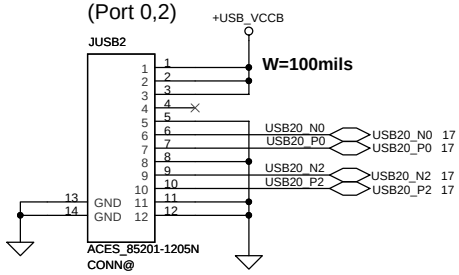
2009/08/25 Update Footprint(follow NAL00)

USB Conn.

(Port 1)

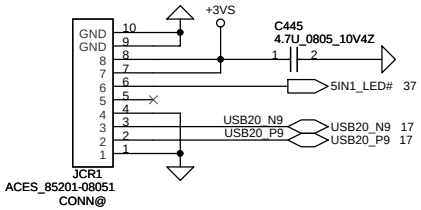
USB/B Conn. LS-5891

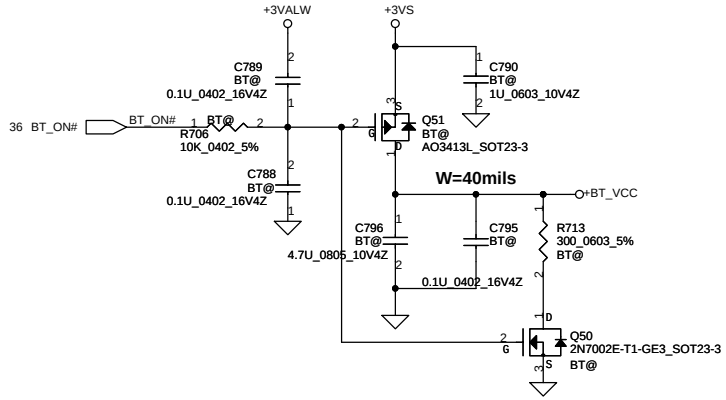
(Port 0,2)



2009/08/24 CHANGE Conn to FFC Type

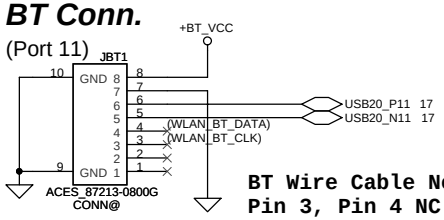
Card Reader Conn. LS-5896





BT Conn.

(Port 11)



BT Wire Cable Note:
Pin 3, Pin 4 NC

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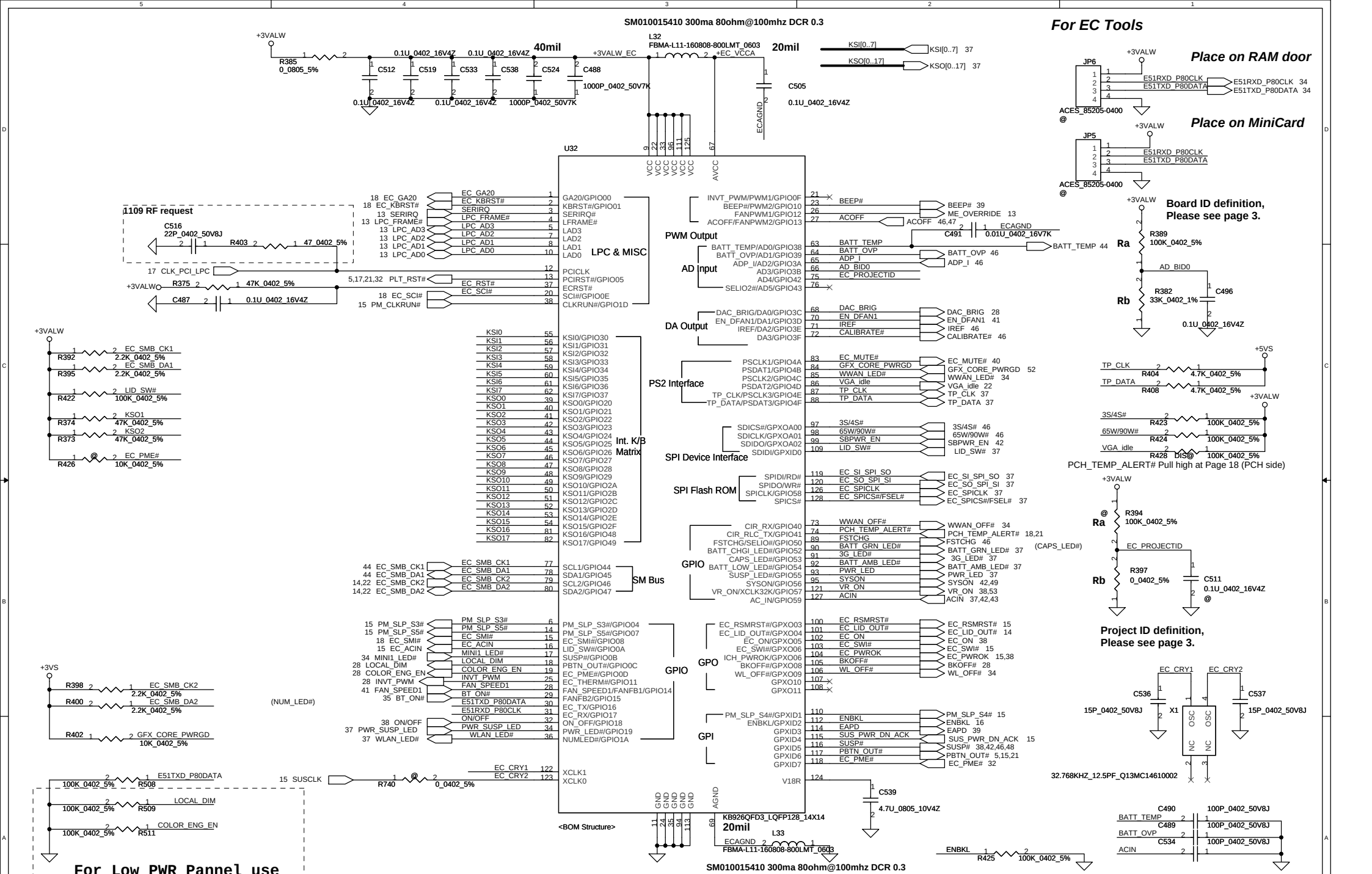

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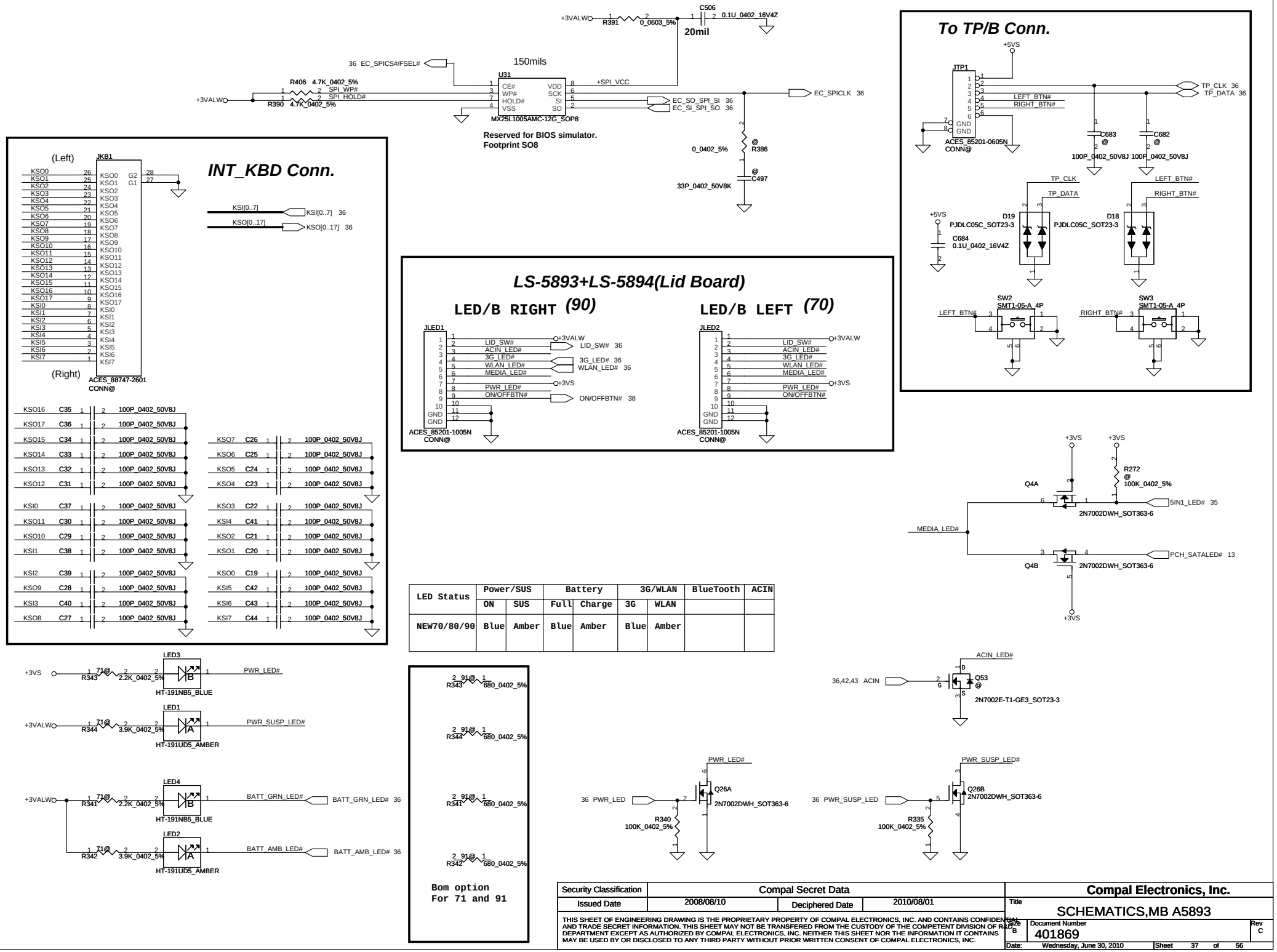

LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		

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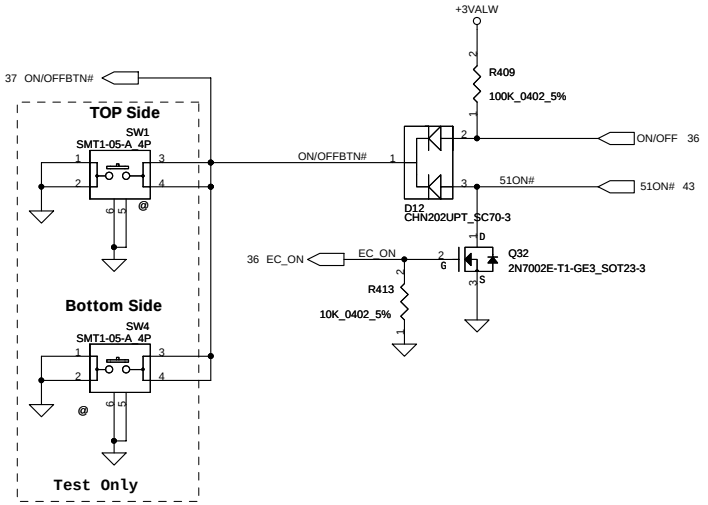
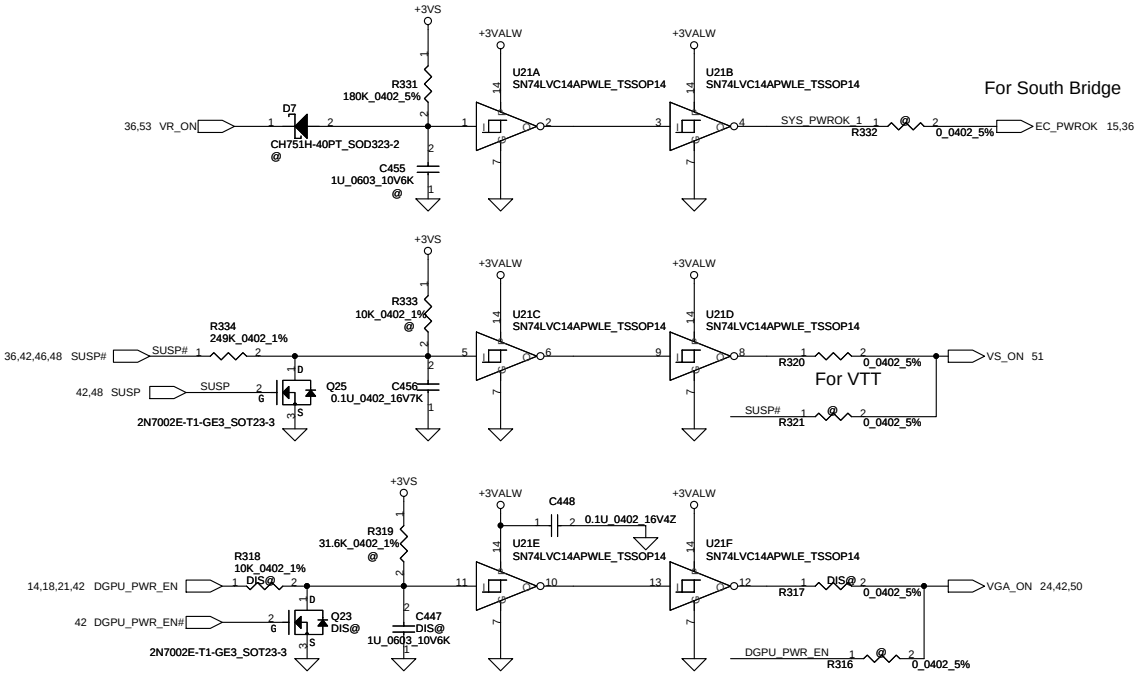
Power Button

ON/OFF switch



Power ON Circuit



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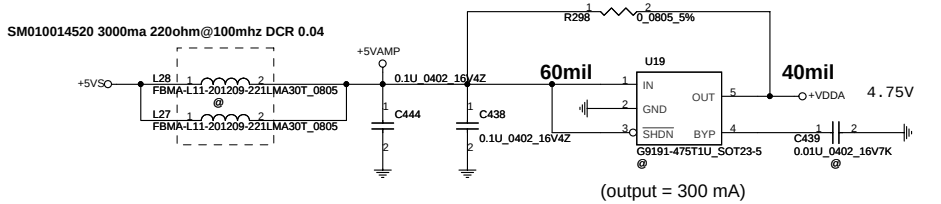
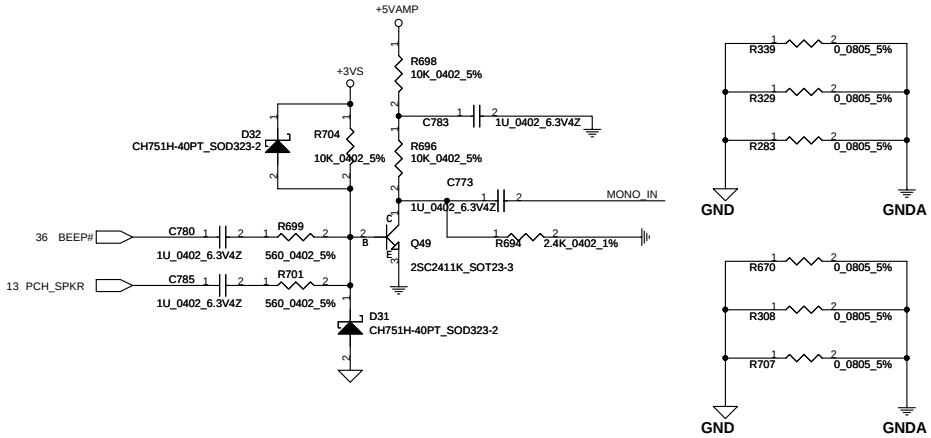
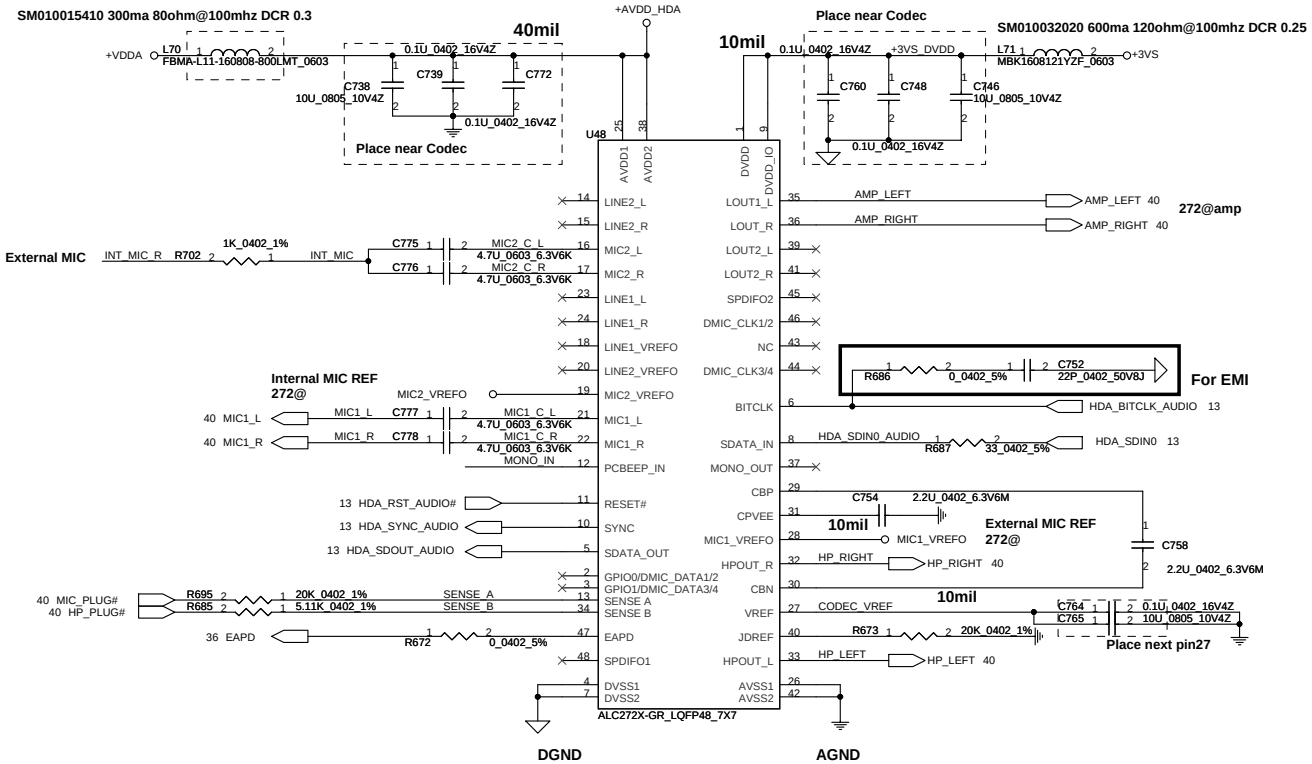
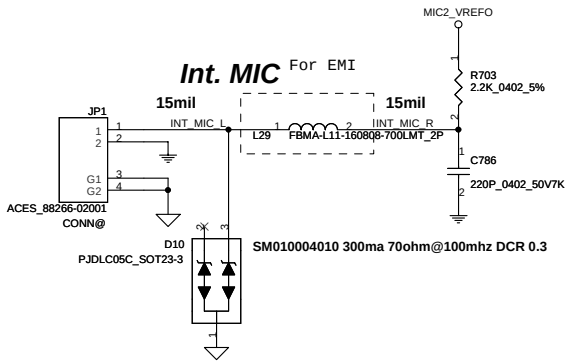




HD Audio Codec





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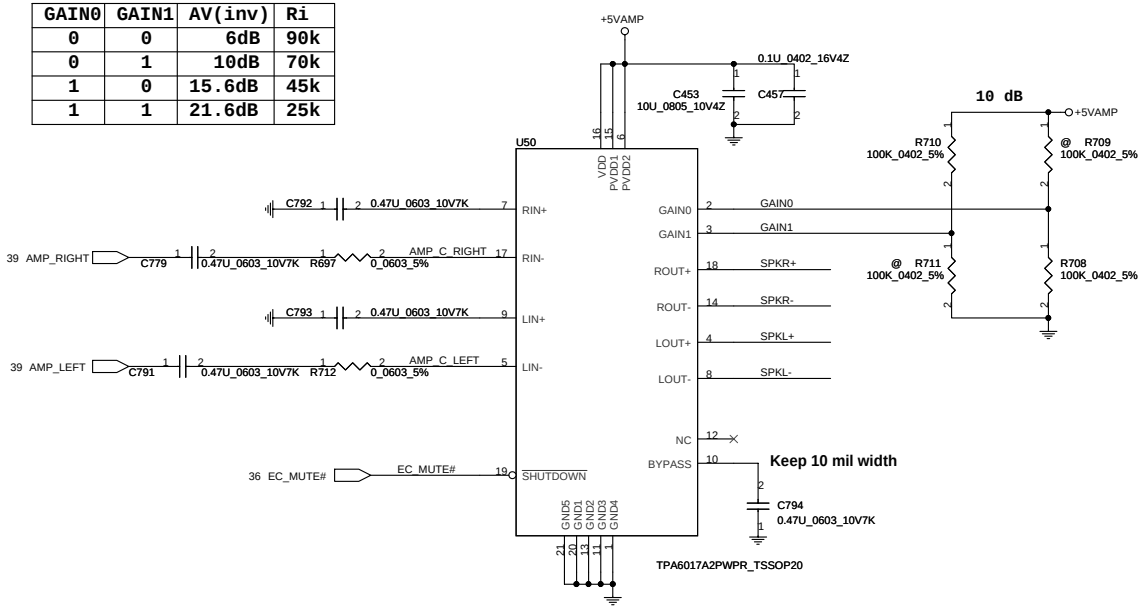
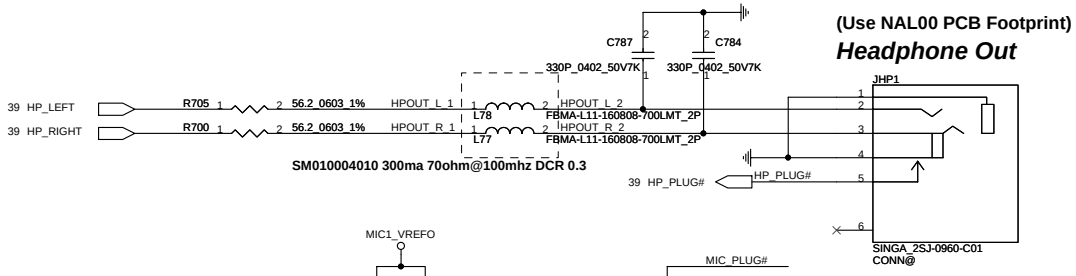
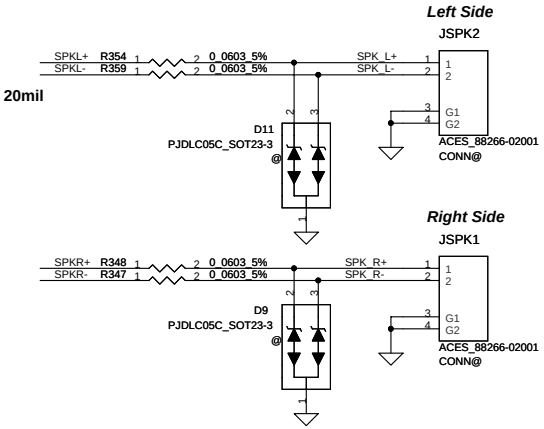
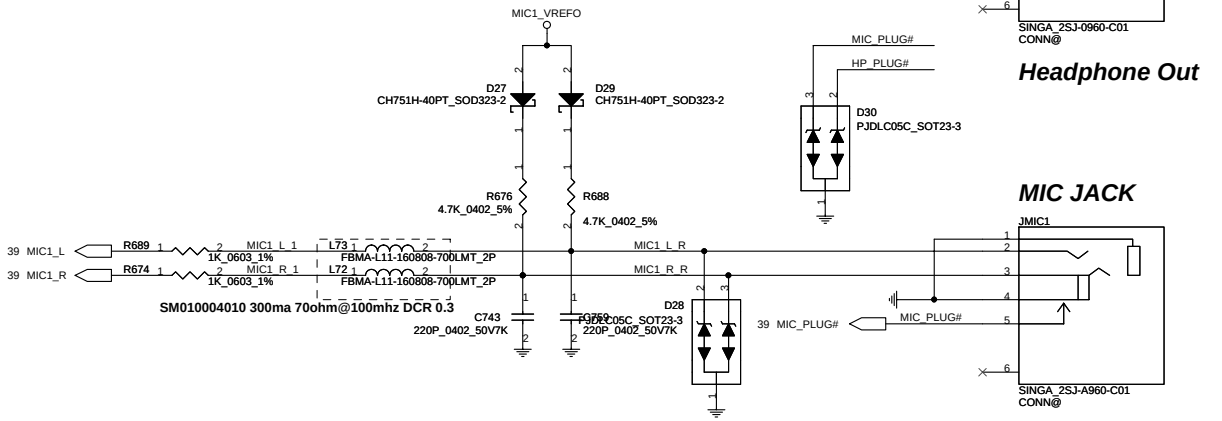
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k





Int. Speaker Conn.





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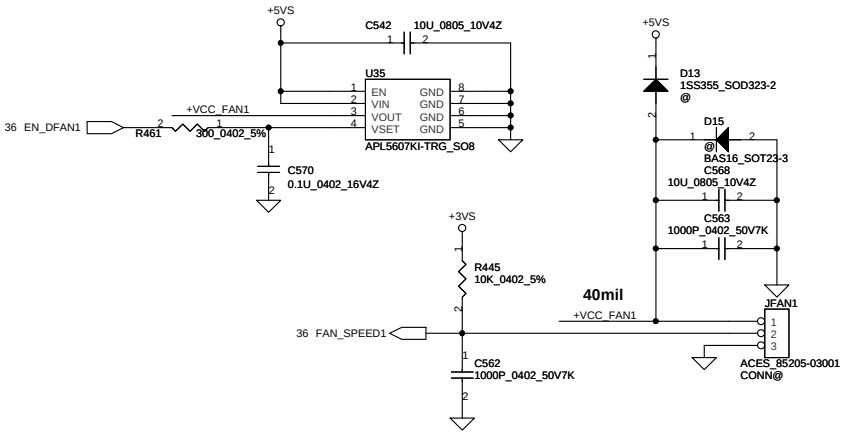
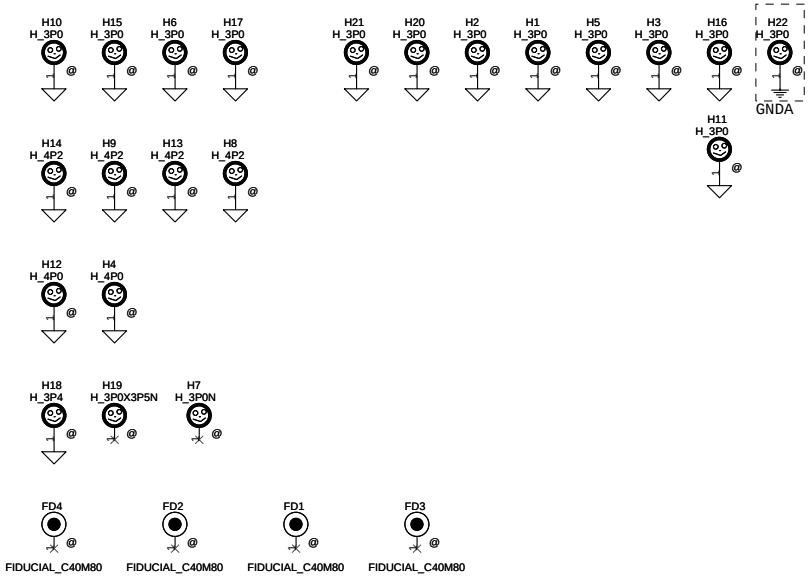
FAN1 Conn





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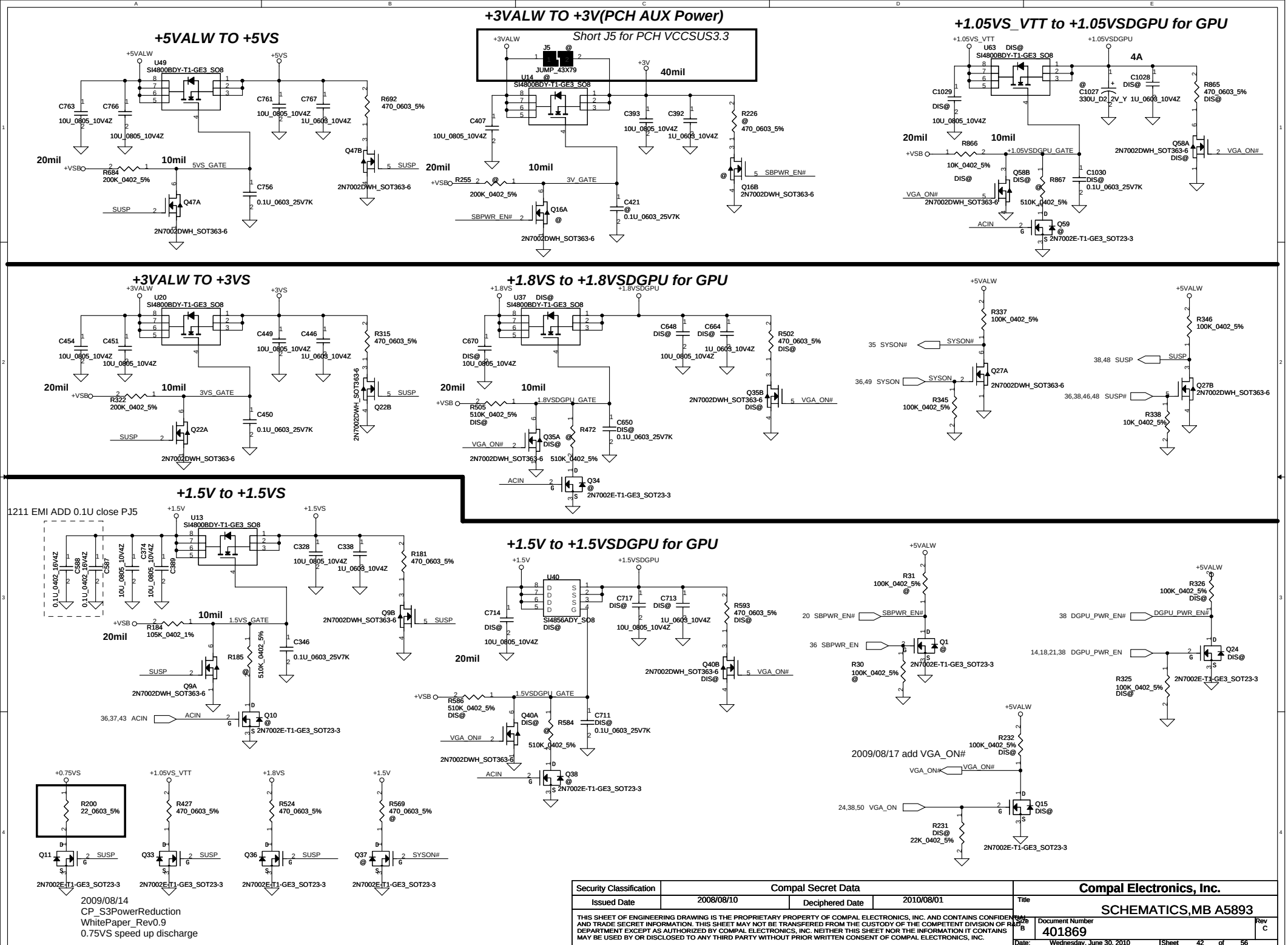
+5VALW TO +5VS
+3VALW TO +3V(PCH AUX Power)
Short J5 for PCH VCCSUS3.3
+1.05VS_VTT to +1.05VSDGPU for GPU
+3VALW TO +3VS
+1.8VS to +1.8VSDGPU for GPU
+1.5V to +1.5VS
1211 EMI ADD 0.1U close PJ5
+1.5V to +1.5VSDGPU for GPU
2009/08/17 add VGA_ON#
2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge
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2008/08/10
Deciphered Date
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B
Document Number
401869
Rev
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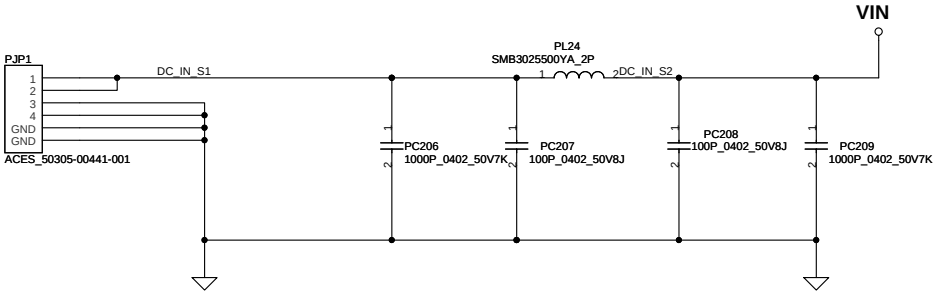
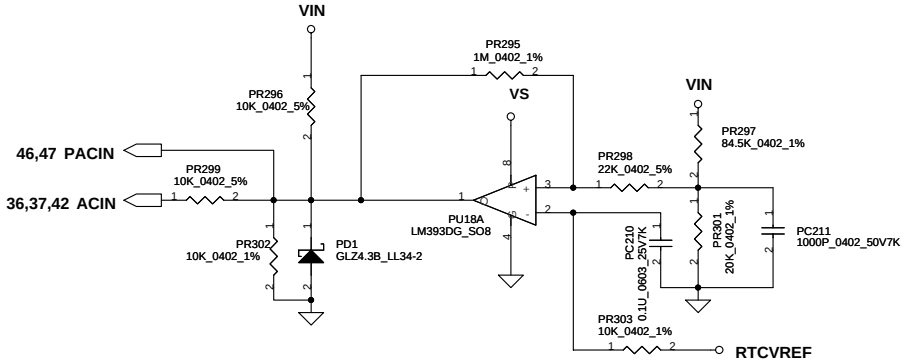
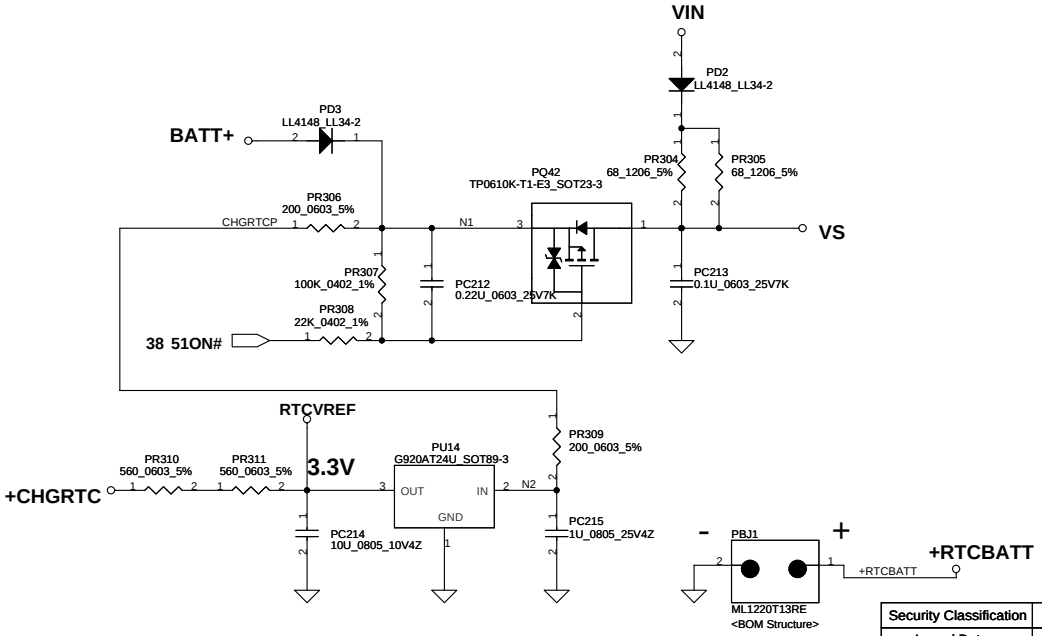
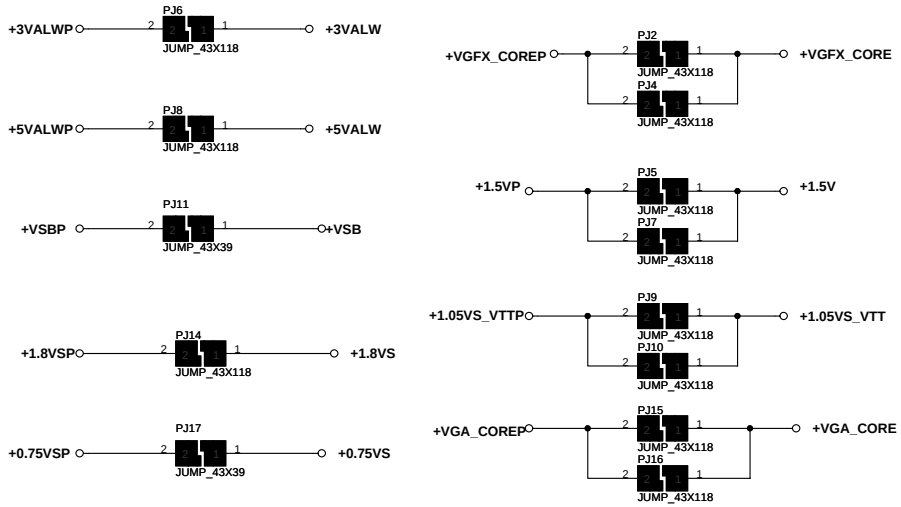




Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





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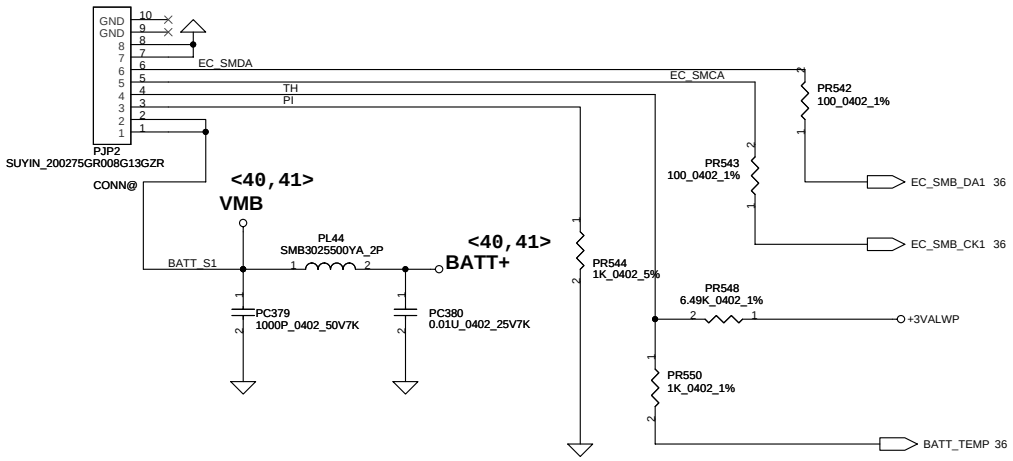
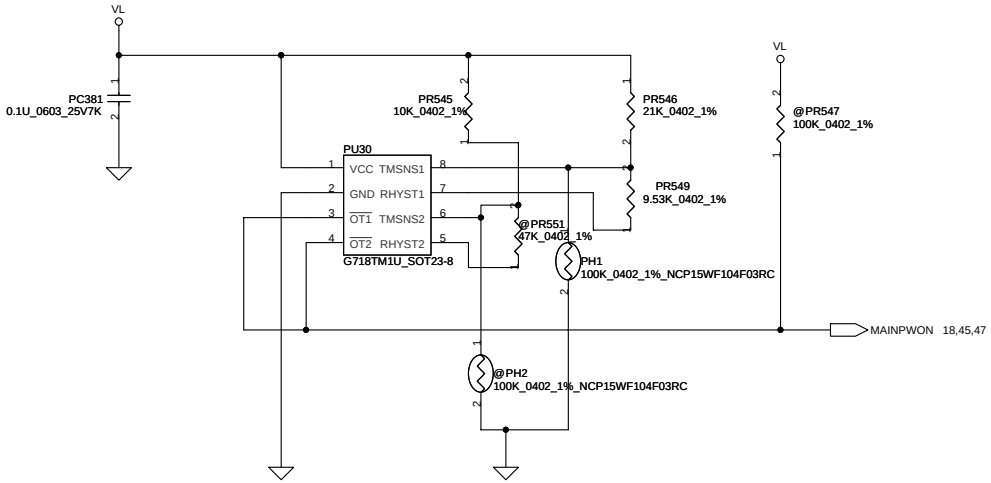
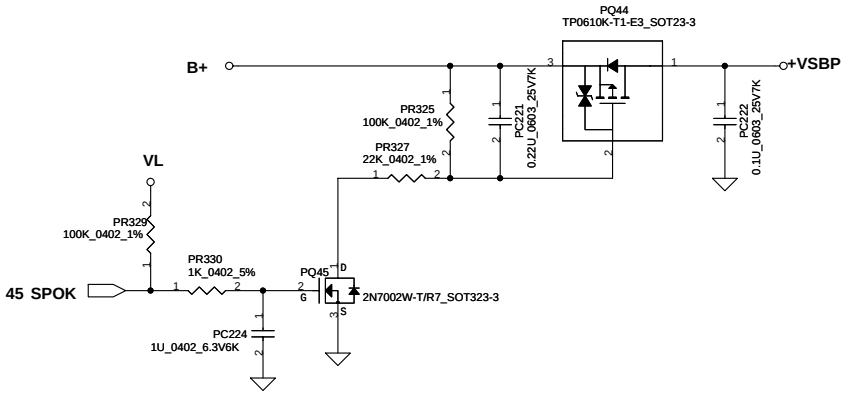


PH1 under CPU botten side :
CPU thermal protection at 92 degree C





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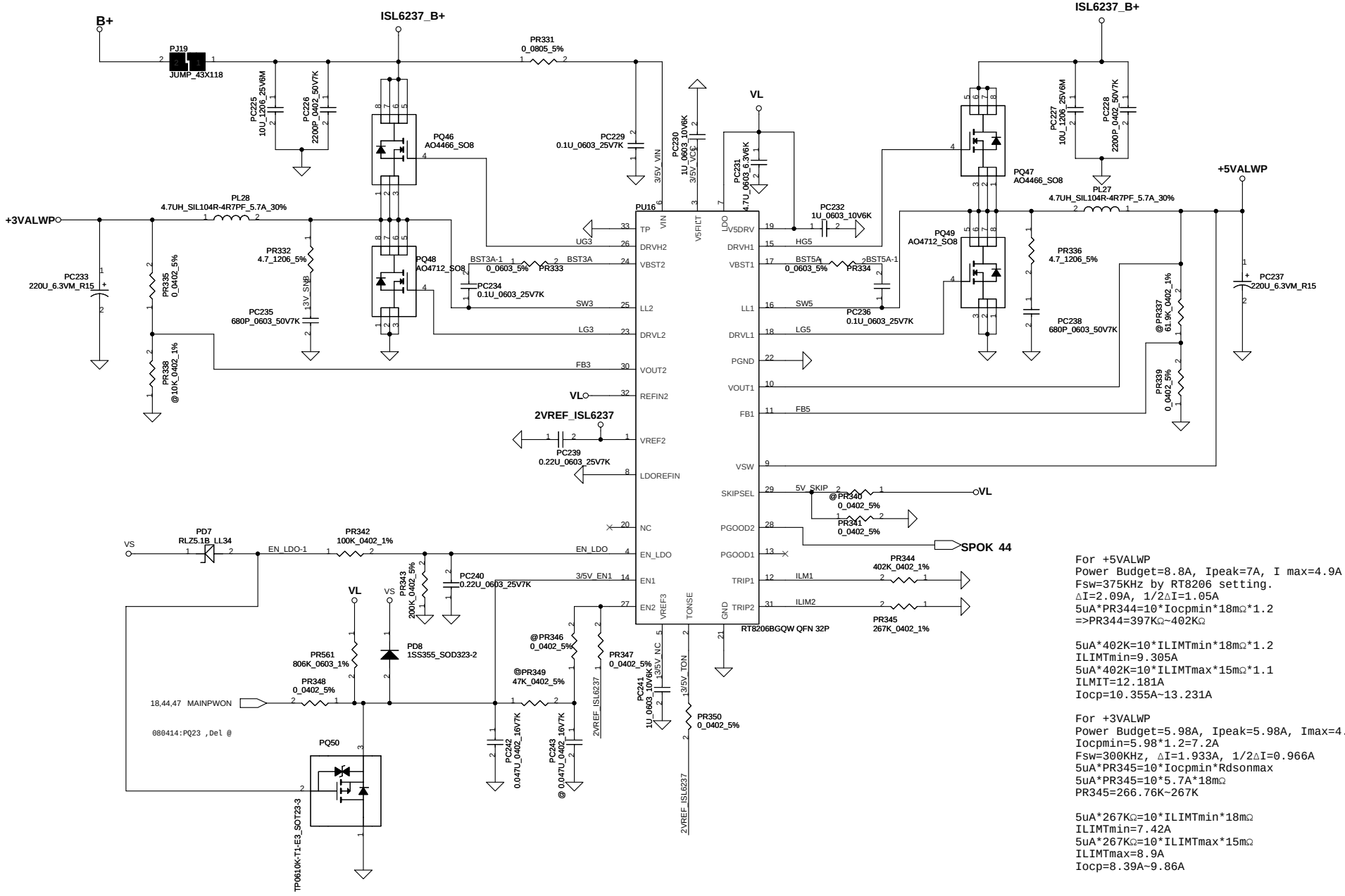

For +5VALWP
Power Budget=8.8A, Ipeak=7A, I max=4.9A
Fsw=375KHz by RT8206 setting.
ΔI=2.09A, 1/2ΔI=1.05A
5uA*PR344=10*Iocpmin*18mΩ*1.2
=>PR344=397KΩ~402KΩ

5uA*402K=10*ILIMTmin*18mΩ*1.2
ILIMTmin=9.305A
5uA*402K=10*ILIMTmax*15mΩ*1.1
ILMIT=12.181A
Iocp=10.355A~13.231A

For +3VALWP
Power Budget=5.98A, Ipeak=5.98A, Imax=4.2A
Iocpmin=5.98*1.2=7.2A
Fsw=300KHz, ΔI=1.933A, 1/2ΔI=0.966A
5uA*PR345=10*Iocpmin*Rdsonmax
5uA*PR345=10*5.7A*18mΩ
PR345=266.76K~267K

5uA*267KΩ=10*ILIMTmin*18mΩ
ILIMTmin=7.42A
5uA*267KΩ=10*ILIMTmax*15mΩ
ILIMTmax=8.9A
Iocp=8.39A~9.86A

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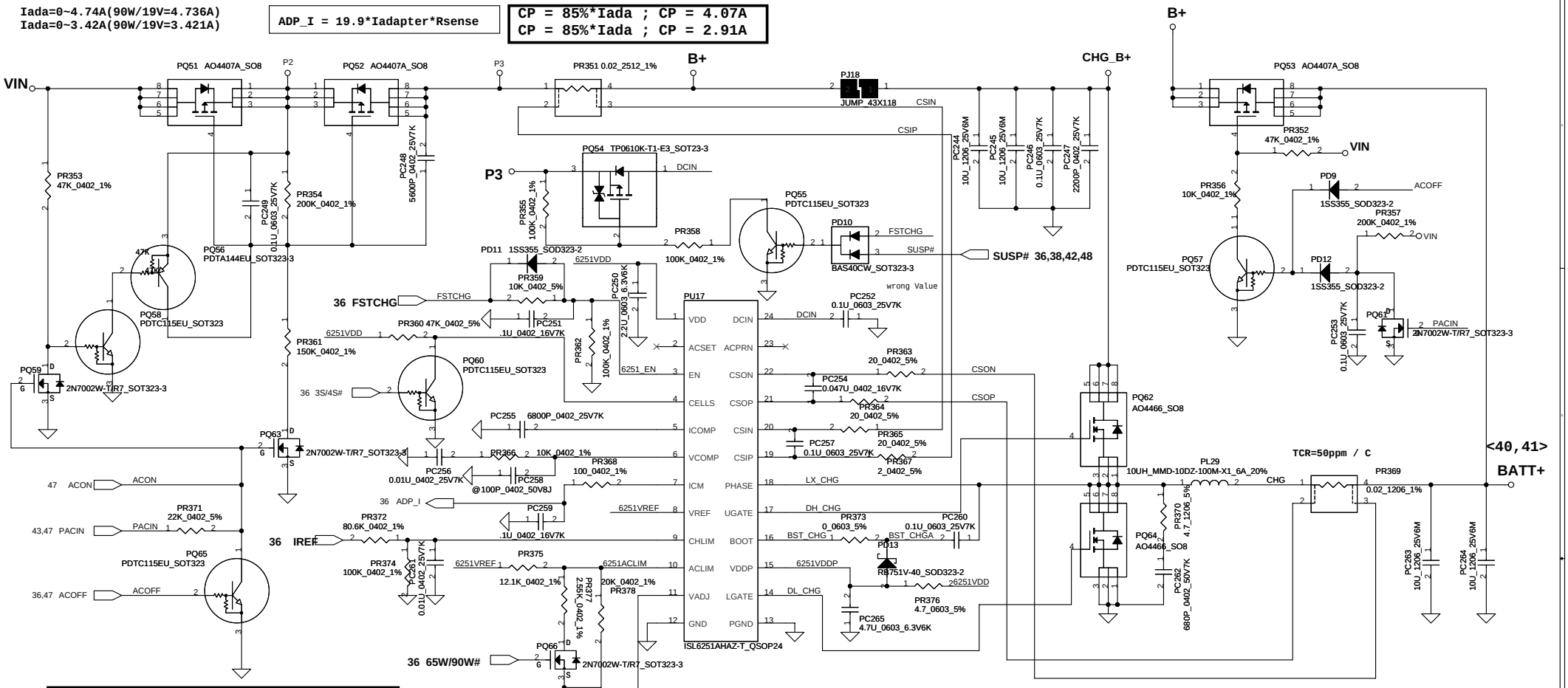
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A
Iref=0.7224*Ichanrge
kI=0.7224
IREF=0.43V~3.24V

```
Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224
```

```
Kv
Rinternal ic=514K  Rec=3K  R1=PR379=15.4K  R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451
```

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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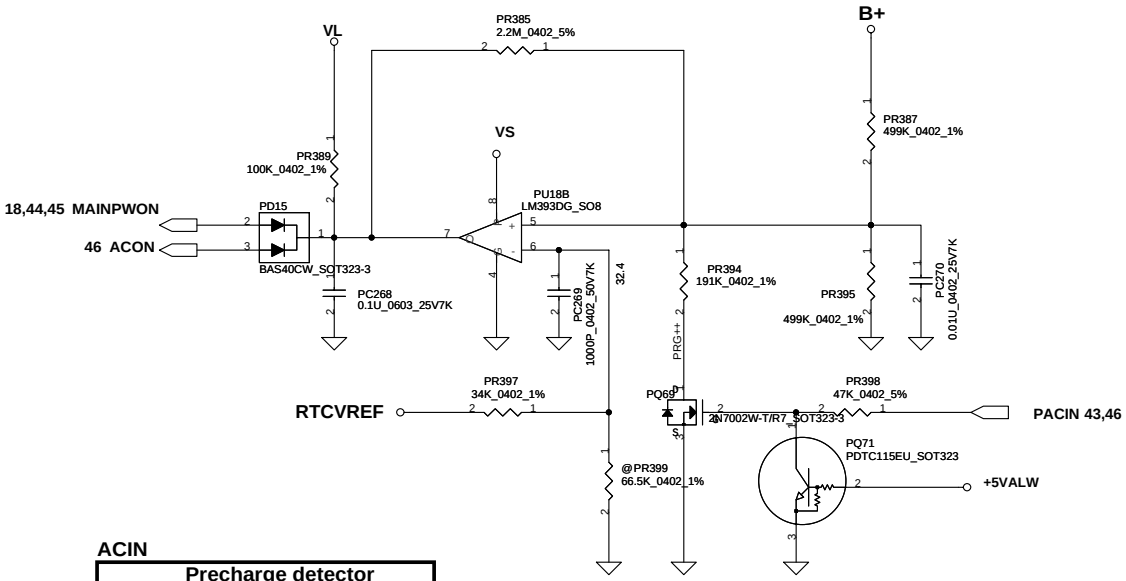

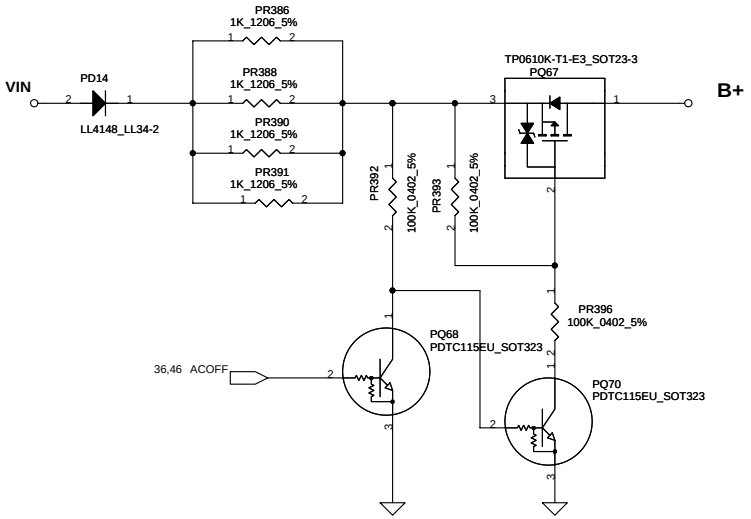

ACIN

Precharge detector			
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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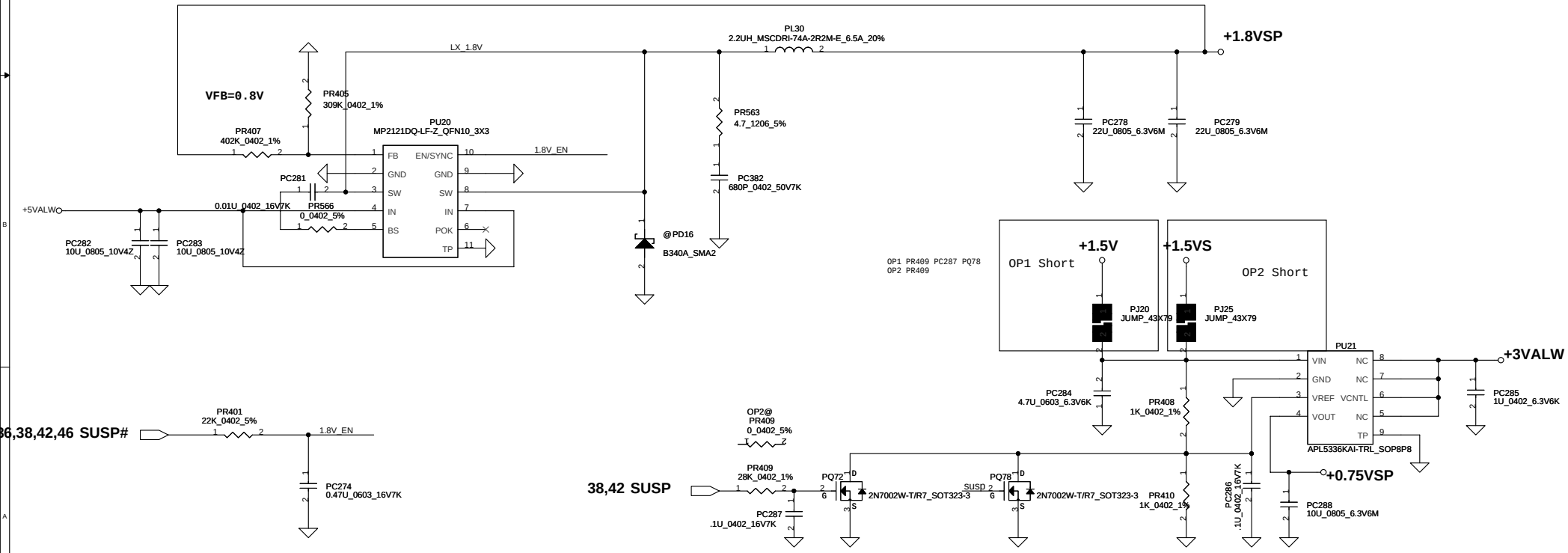

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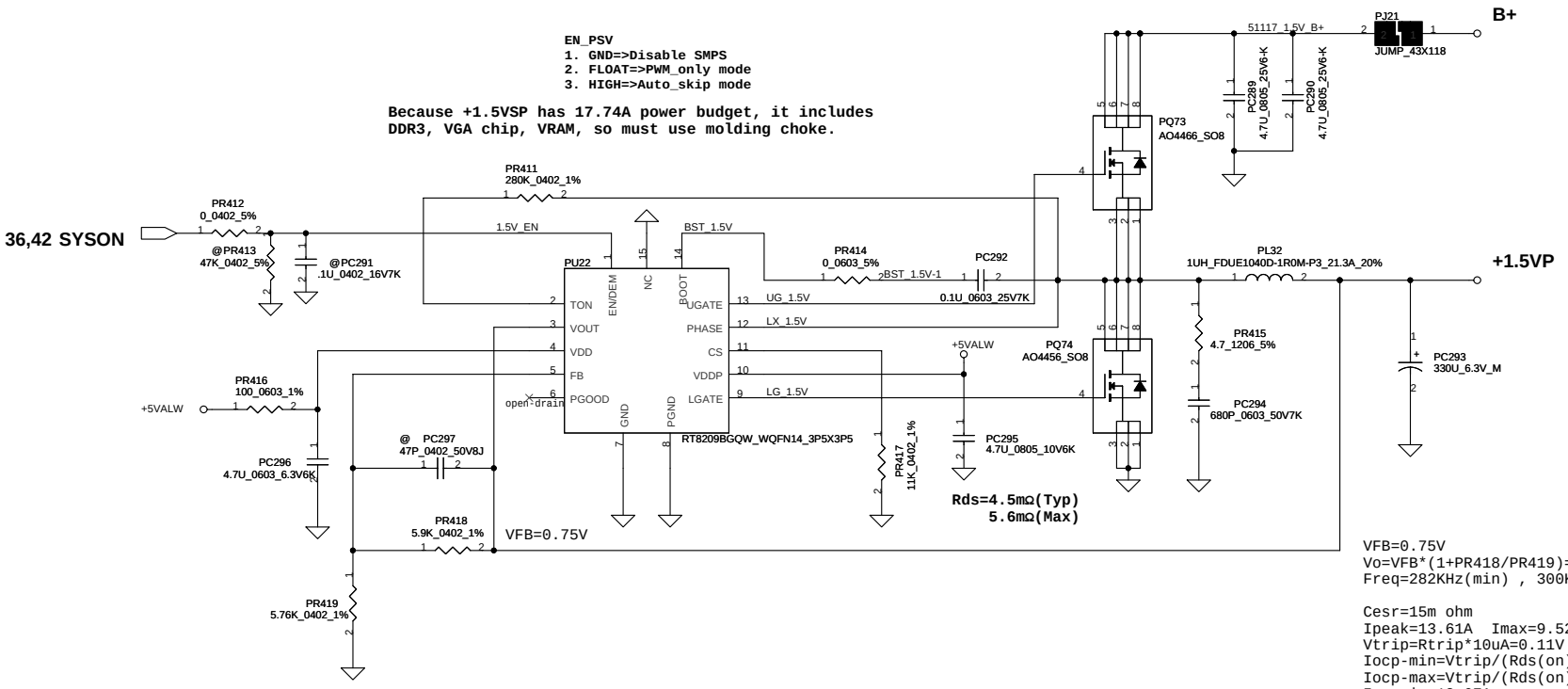

VFB=0.75V
Vo=VFB*(1+PR418/PR419)=1.52V
Freq=282KHz(min) , 300KHz(typ)

Cesr=15m ohm
Ipeak=13.61A Imax=9.527A
Vtrip=Rtrip*10uA=0.11V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+Delta I / 2= 18.67A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+Delta I / 2=22.67A
Iocpmin=18.67A
△I=((19-1.5)*(1.5/19))/(L*Freq)=4.605A
1/2△I=2.3A

Iocp=18.67A~22.67A

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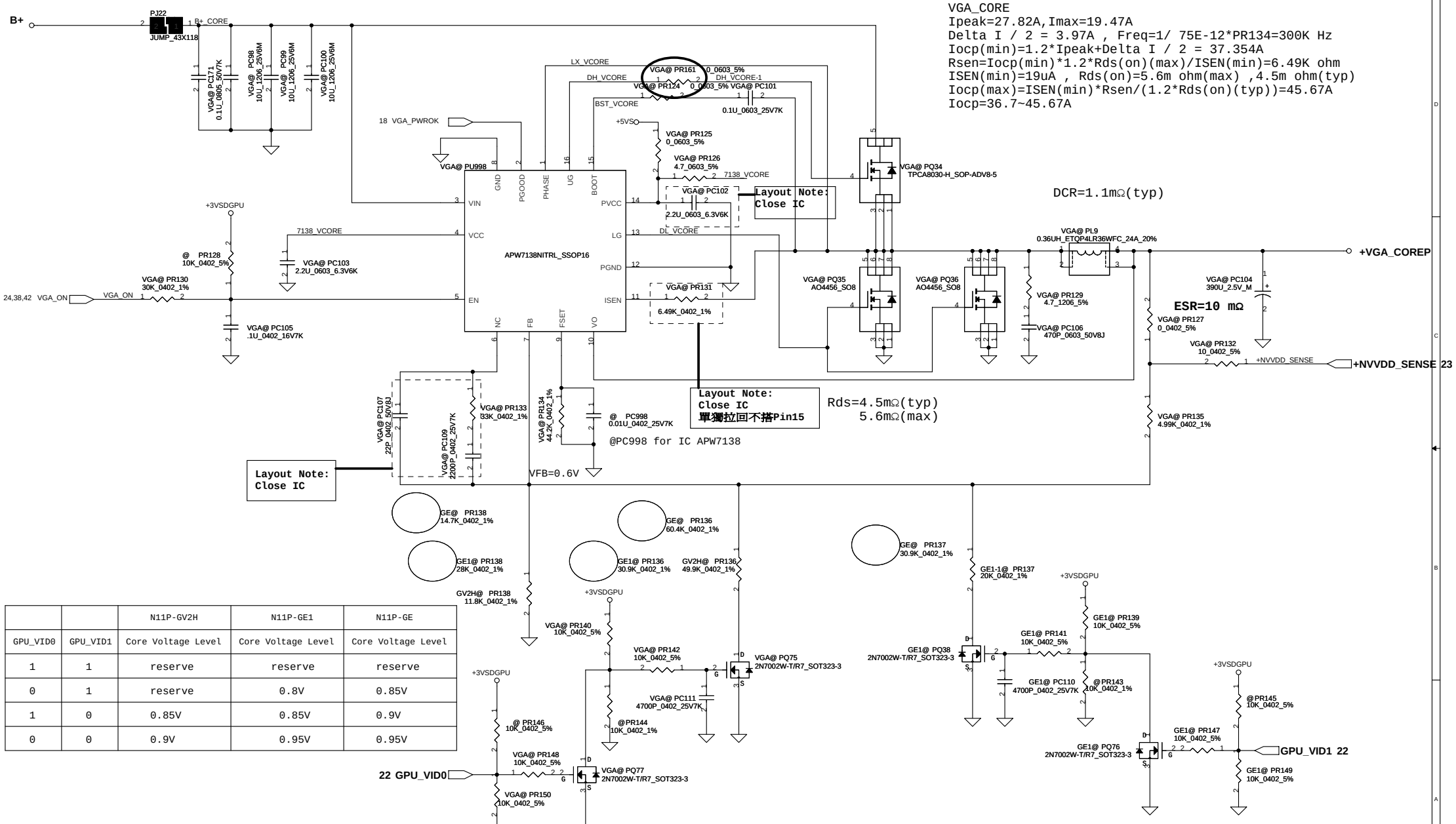

		N11P-GV2H	N11P-GE1	N11P-GE
GPU_VID0	GPU_VID1	Core Voltage Level	Core Voltage Level	Core Voltage Level
1	1	reserve	reserve	reserve
0	1	reserve	0.8V	0.85V
1	0	0.85V	0.85V	0.9V
0	0	0.9V	0.95V	0.95V

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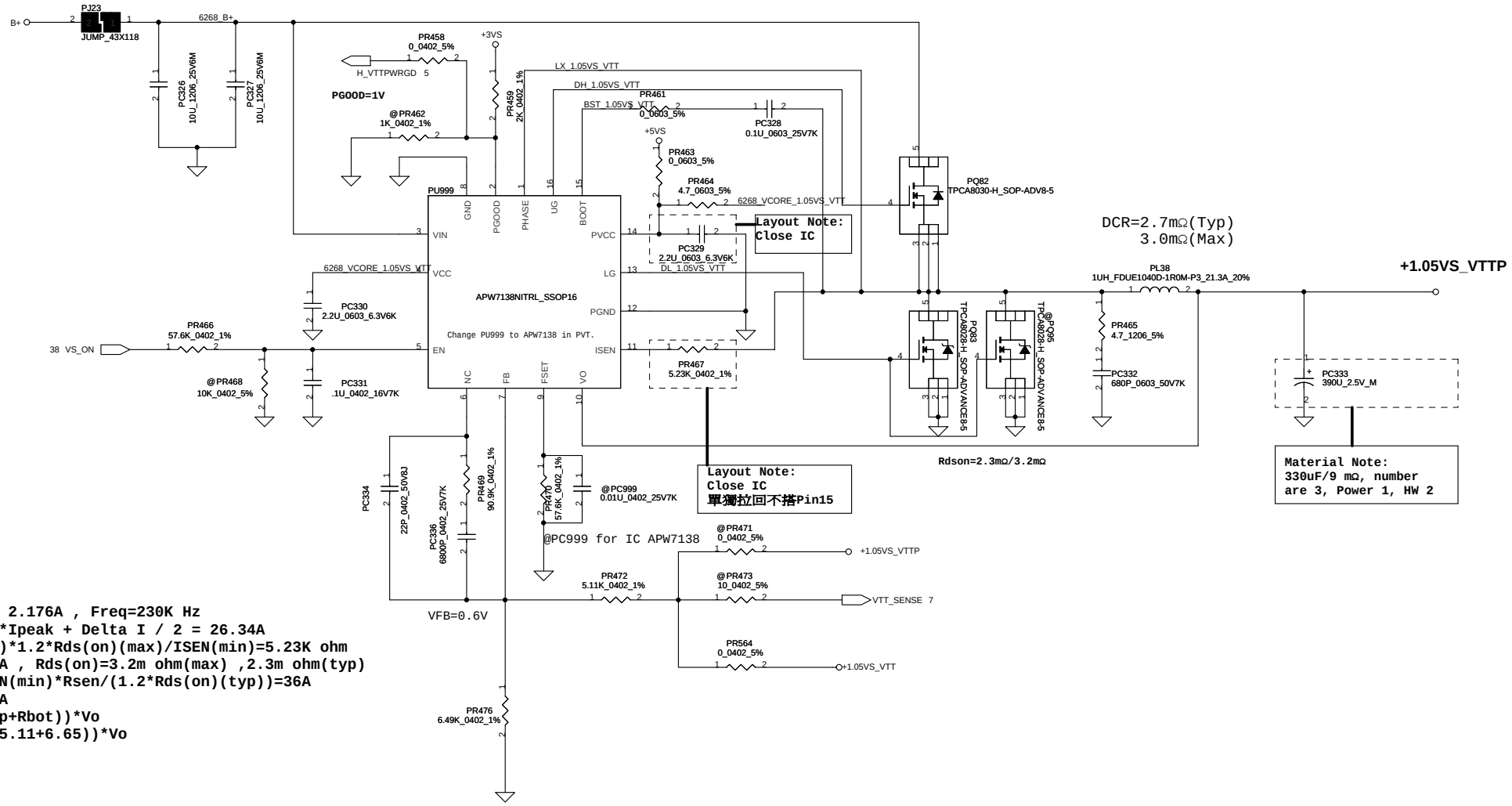

+1.05VS_VTT
Ipeak=20.14A
Imax=14.10A
Delta I / 2 = 2.176A , Freq=230K Hz
Iocp(min)=1.2*Ipeak + Delta I / 2 = 26.34A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=5.23K ohm
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) ,2.3m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=36A
Iocp=26.34~36A
Vref=(Rb/(Rtop+Rbot))*Vo
=>0.6=(6.65/(5.11+6.65))*Vo
Vo=1.061V

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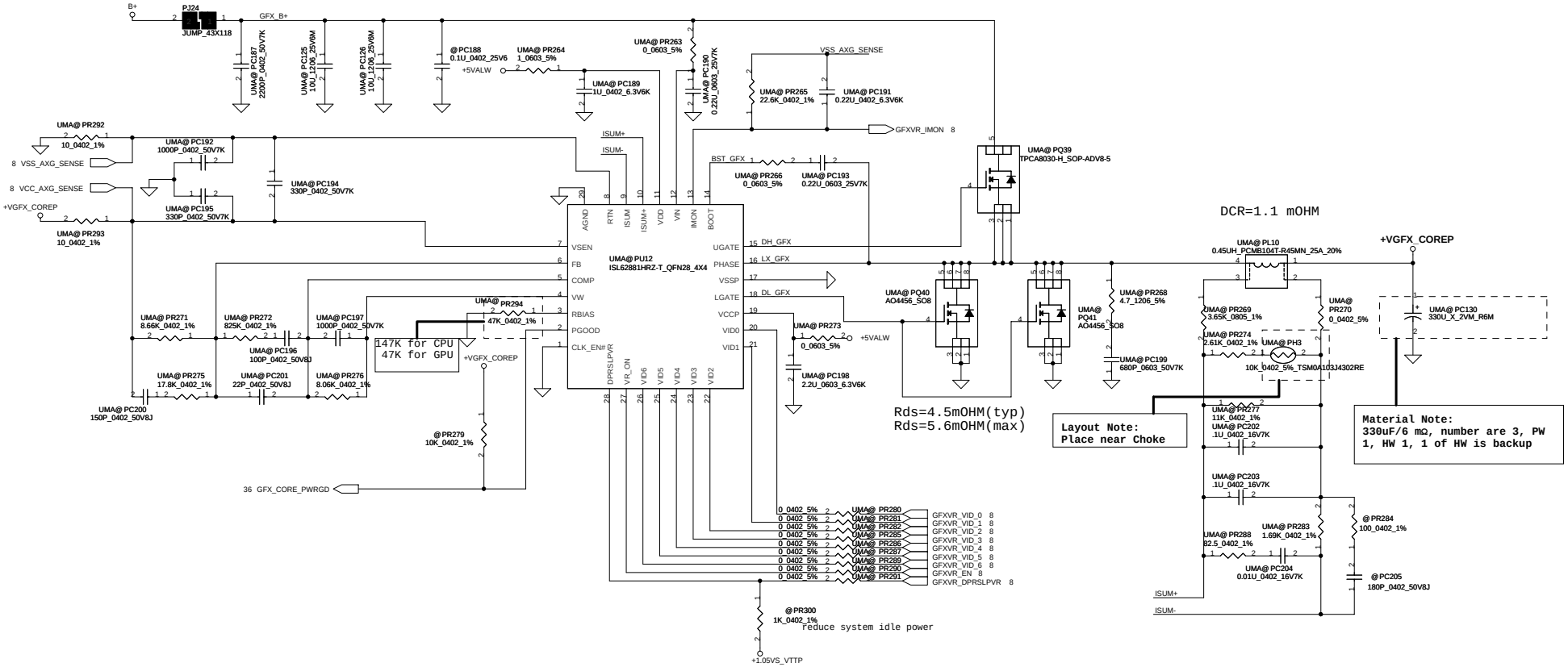
Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A



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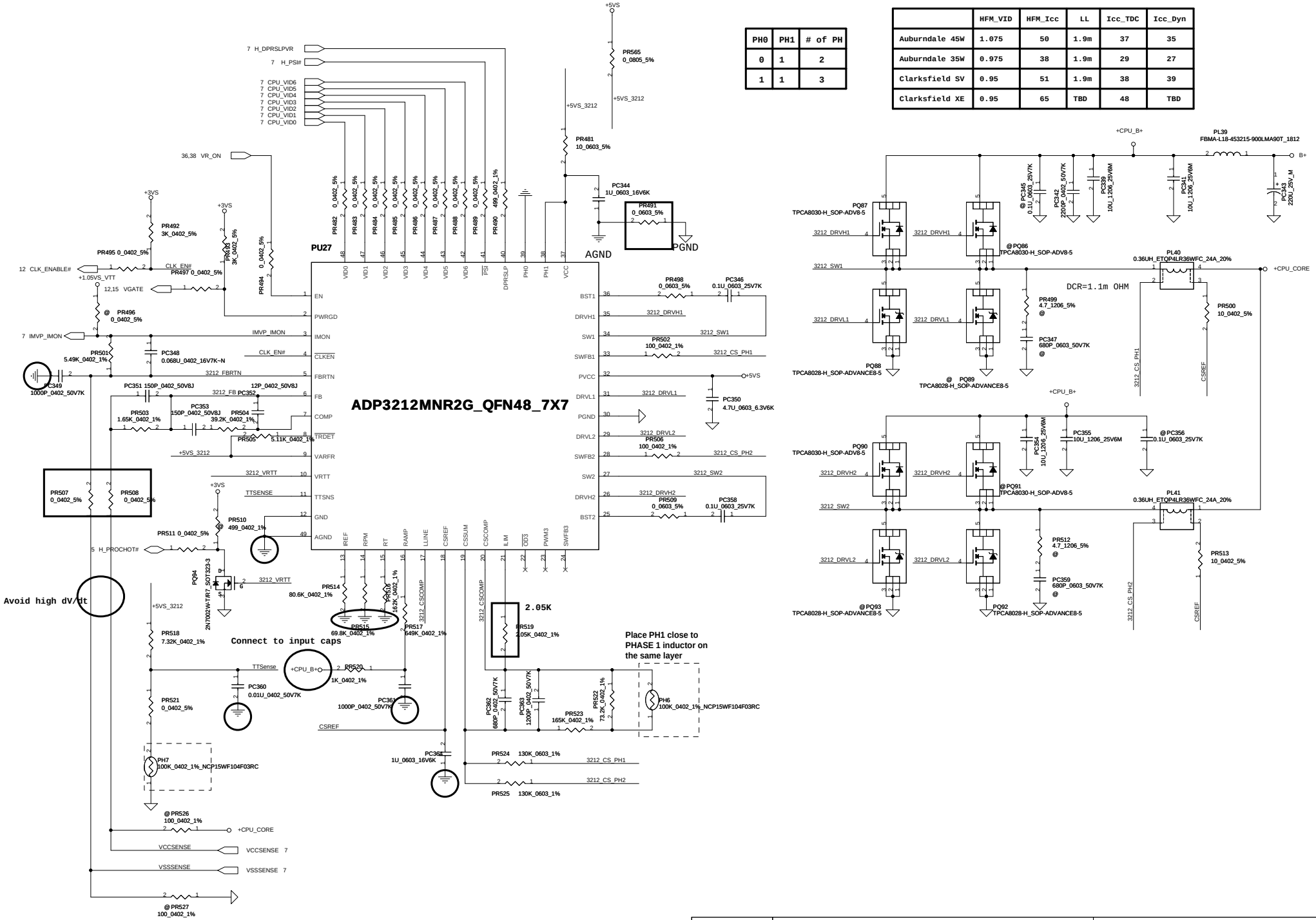
PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify VGA_COREP circuit	Reduce component quantity	0.1	50	Change PL9 to SH12036BM00(S COIL .36UH +-20% ETQP4LR36WFC 24A)	2009-1222	PVT
2	Modify CPU_COREP circuit	Arrandale CPU commond design(1 HS, 1LS MOS)	0.1	53	Change PQ89/PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP ADVANCE) BOM structure to @	2009-1222	PVT
3	Modify VGA_COREP circuit	PVT-2 add N11P-GE1 VGA, change VID setting.	0.2	50	Change PR136/PR138 BOM structure to GV2H@ Change PR137/139/141/143/147/149, PC110 and PQ38/76 BOM structure to GE1@	2010-0113	PVT-2
4	Modify +VSBP circuit	Add PC224 for 3VS spike issue	0.2	44	add PC224 to SE000000K80(S CER CAP 1U 6.3V K X5R 0402)	2010-0113	PVT-2
5	Modify +1.05VS_VTTP circuit	Change voltage level from 1.061V to 1.072V.	0.2	51	Change PR476 to SD034649180(S RES 1/16W 6.49K +-1% 0402)	2010-0201	PVT-2
6	Modify +0.75VSP circuit	Change RC for HW timing.(S3 shutdown issue)	0.2	48	Change PR409 to SD034280280(S RES 1/16W 28K +1% 0402) Change PC287 to SE076104K80(S CER CAP .1U 16V K X7R 0402)	2010-0201	PVT-2
7							
8							
9							
10							
11							
12							
13							
14							
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17							
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23							

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A -->Modify item

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BOM Config		
PEW71 SKU N11P-GE DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GE@,NonOPT@	431869B0L21
PEW71 SKU N11P-GV2H-A3 DISCTETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GV2H@,GV2HA3@,NonOPT@,NonGE@	431869B0L22

PCB

ZZZ

LA-5893P REV0 M/B

GV2HA2@

U51

N11P-GV2H-A2_BGA969

GV2HA3@

U51

N11P-GV2H-A3_BGA969

GE1@

U51

N11P-GE1-A3 BGA 969P

GE@

U51

N11P-GE-A1 BGA 969P

ZZZ2

X7622@

X76198B0L22

ZZZ1

X7621@

X76198B0L21

ALT. GROUP PARTS 2G HYN **ALT. GROUP PARTS 1G HYN** **ALT. GROUP PARTS 1G SAM**

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