Compal Confidential

PEW71_81_91 UMA <LA-6582P> M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

2010-06-18
REV:0.2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/5/12	Deciphered Date	2010/04/15
Title	SCHEMATIC,MB A6582		
Size: Custom	Document Number: 401939		Rev: A
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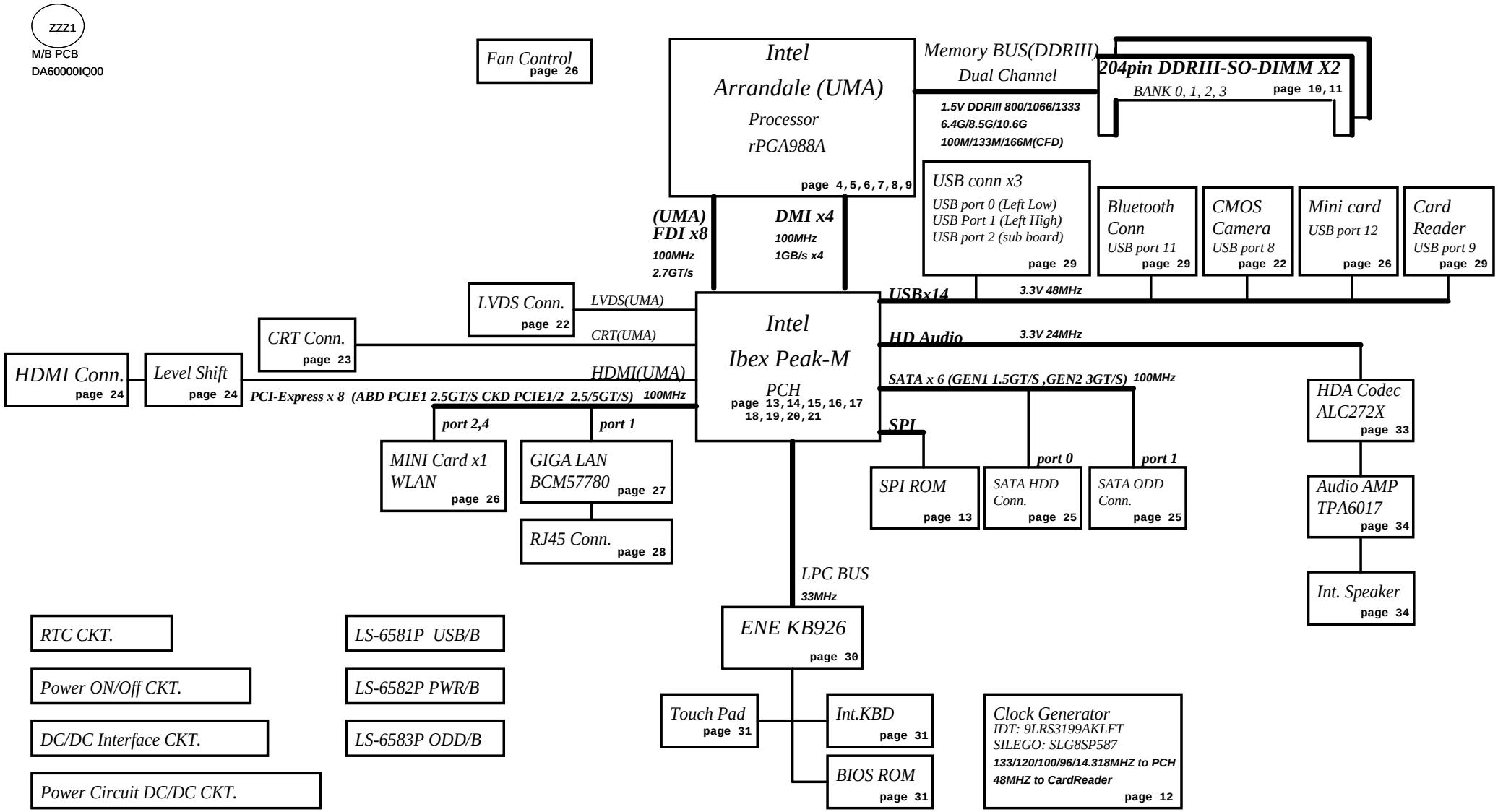
Model Name PEW71_81 UMA

File Name : LA-6582P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.05VS_VTT	1.05V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Project ID / Board ID Table for EC-AD channel

Vcc	3.3V +/- 5%
Ra/Rc	100K +/- 5%

	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Board ID	Project ID
0	0	0 V	0 V	0 V	0.1	Original NEW70/80/90/50/71/91
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2	PEW71/81/91 Audio Mono/Crystal
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	0.3	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	1.0	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V		
5	100K +/- 5%	1.453 V	1.650 V	1.759 V		
6	200K +/- 5%	1.935 V	2.200 V	2.341 V		PEW71/81/91 Audio Mono/SUSCLK
7	NC	2.500 V	3.300 V	3.300 V		NEW71/91 Optumis

BTO Option Table

BTO Item	BOM Structure
HDMI	HDMI@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port
EHCI1	UHCI0	0	Ext1 Left Low USB	Ext1 Left Low USB
		1	Ext2 Left High USB	Ext2 Left High USB
	UHCI1	2	Ext3 Right USB	Ext3 Right USB
		3		
	UHCI2	4		
		5		
	UHCI3	6		
		7		
EHCI2	UHCI4	8	Camera	Camera
		9	Card Reader	Card Reader
	UHCI5	10		
		11	Blue Tooth	Blue Tooth
	UHCI6	12	1st Min-Card	1st Min-Card
		13		

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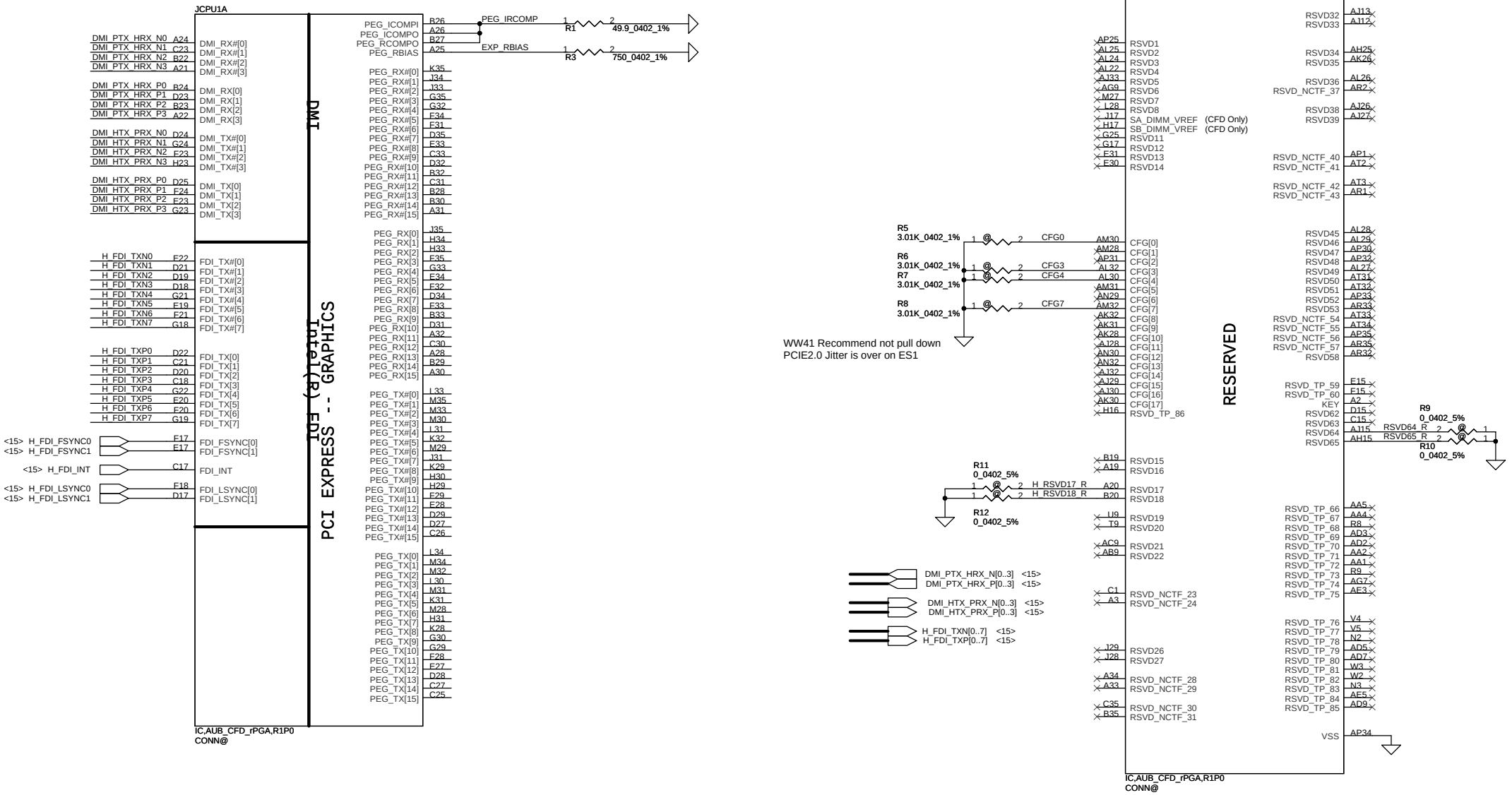

eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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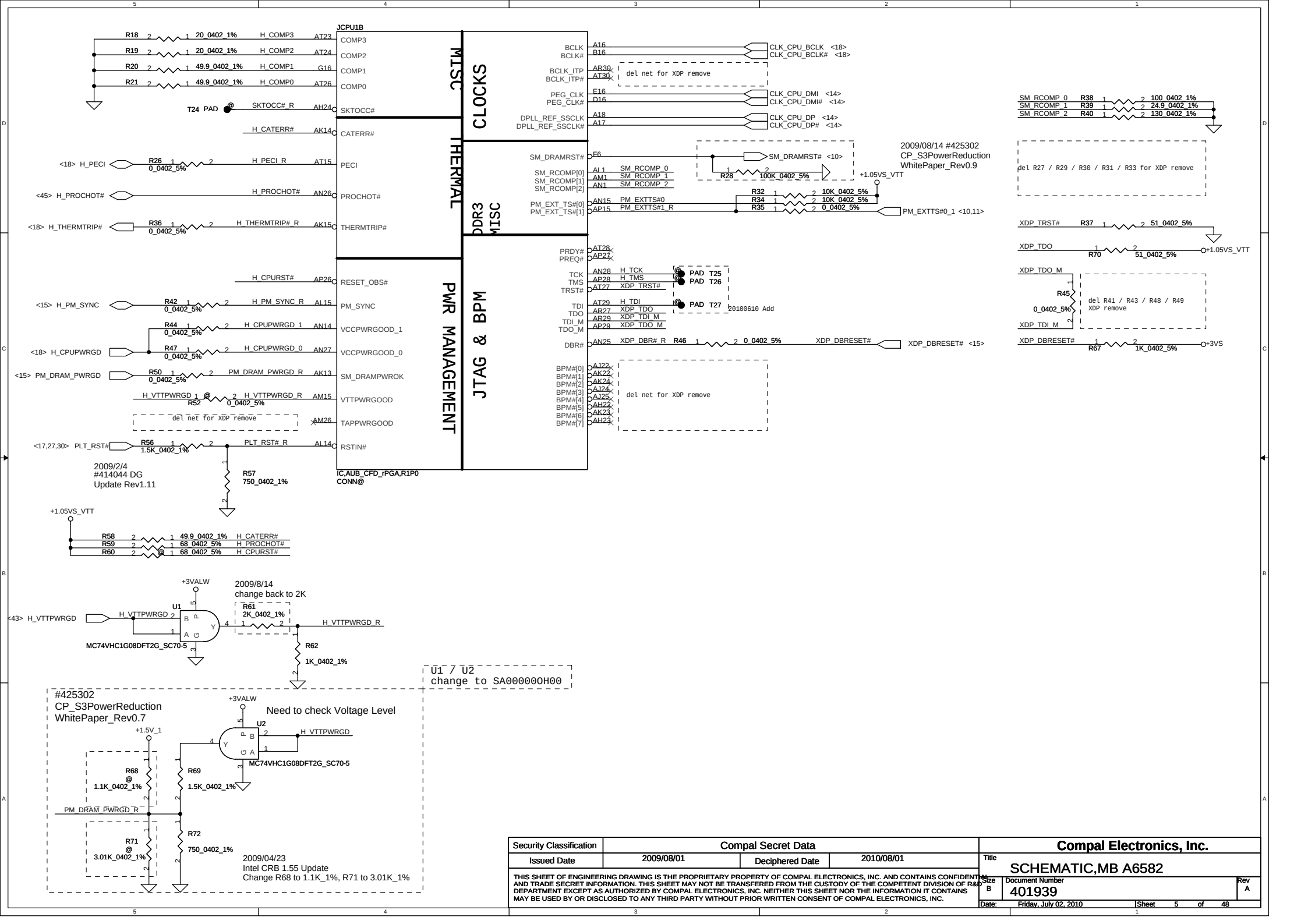

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JCPU1F

WW15 MOW
Peak 21A
Continuous 18A

48A

+CPU_CORE

CPU CORE SUPPLY

1.1V RAIL POWER

POWER

CPU VIDS

SENSE LINES

IC,AUB_CFD_rPGA,R1P0
CONN@

10U_0805_6.3V6M
22U_0805_6.3V6M
330U_2.5V_M_R15
Change to OS-CON 20100414

+1.05VS_VTT

CSC (Current Sense Configuration) 8/25

1K_0402_1%

H_VTTVID1 @ PAD T14 20090915 Modify

H_VTTVID1 = low, 1.1V
H_VTTVID1 = high, 1.05V

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

(Place these capacitors between inductor and socket on Bottom)

(Place these capacitors under CPU socket, top layer)

(Place these capacitors on CPU cavity, Bottom Layer)

(Place these capacitors on CPU cavity, Bottom Layer)

4 x 470uF(4.5mohm@100kHz; 4.0mohm@SRF)

330U_D2E_2.5VM_R6M

Del C106

TOP side (under inductor)

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	

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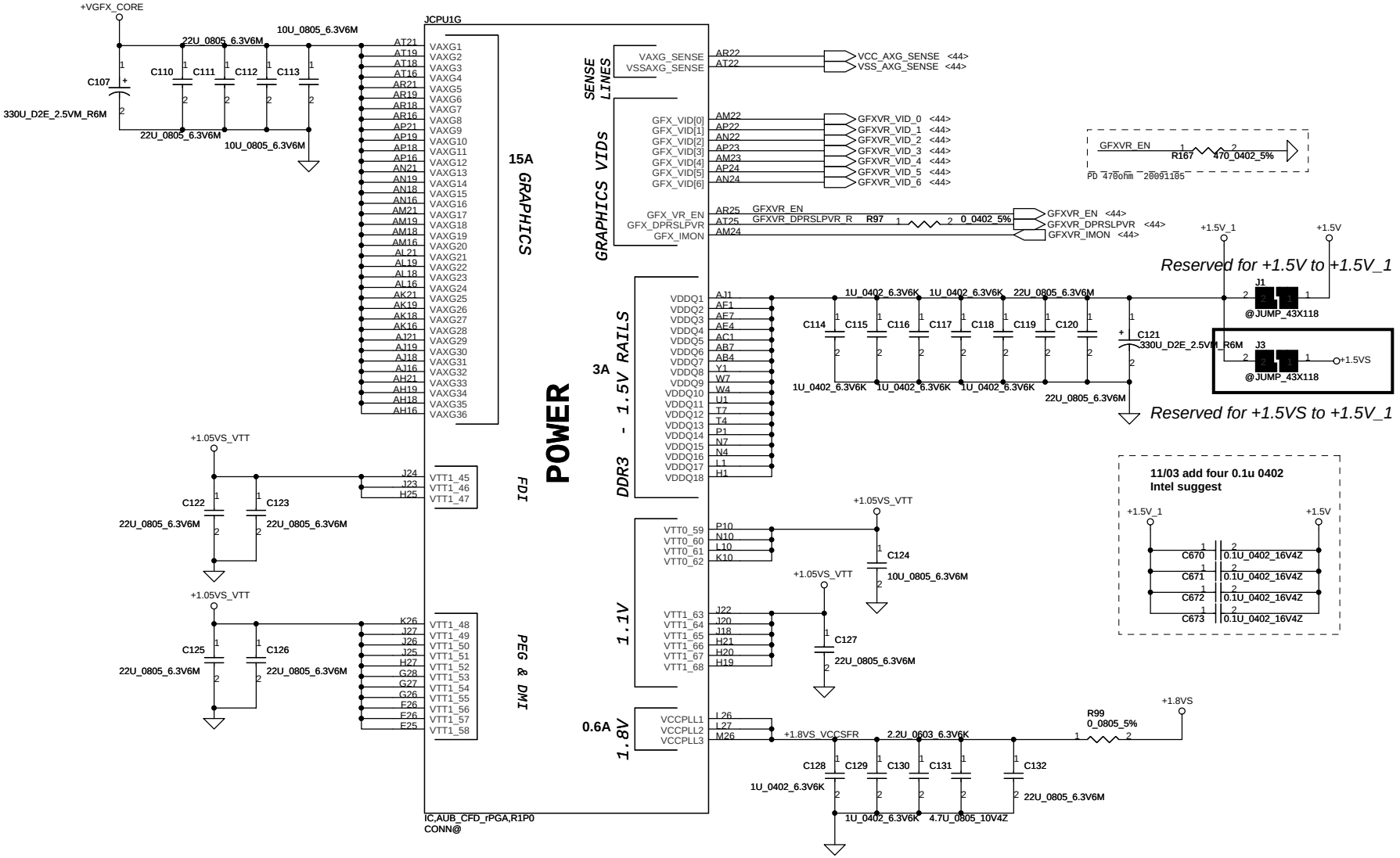

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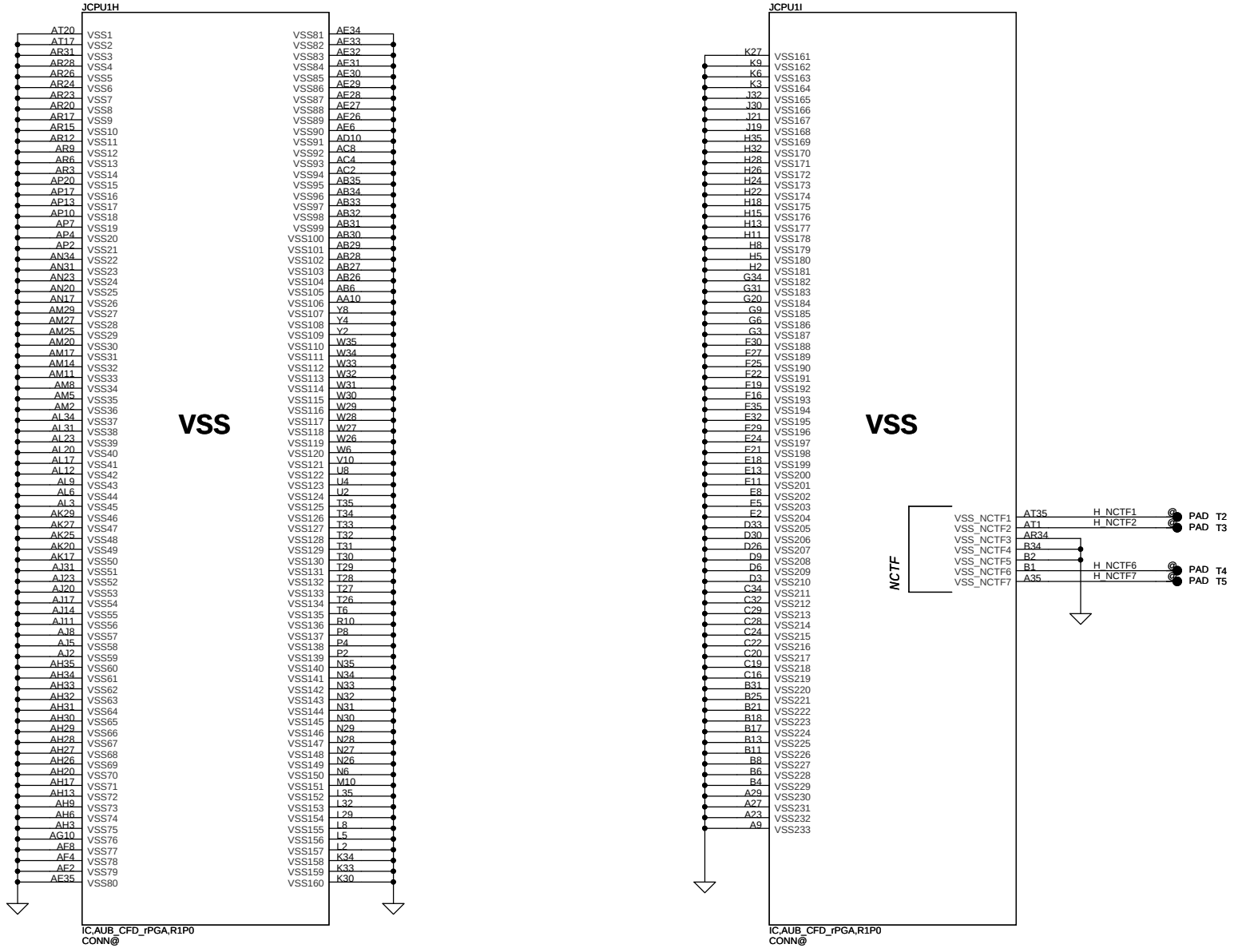

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DIMMA VREFDQ M1 Circuit

+1.5V

R101 1K_0402_1%

+DIMM_VREFDQA

R104 1K_0402_1%

DIMMA & DIMMB VREFCA circuit

+1.5V

R106 1K_0402_1%

+DIMM_VREFCA

R107 1K_0402_1%

<6> DDR_A_DQS#[0..7]

<6> DDR_A_D[0..63]

<6> DDR_A_DM[0..7]

<6> DDR_A_DQS[0..7]

<6> DDR_A_MA[0..15]

M1 Circuit

+DIMM_VREFDQA

C134 0.1U_0402_16V4Z

C133 2.2U_0603_6.3V6K

#425302
CP_S3PowerReduction
WhitePaper_Rev1.0

+1.5V

R102 0_0402_5% @

R103 1K_0402_1%

<5> SM_DRAMRST#

Q2 BSS138LT1G_SOT23-3

DIMM_DRAMRST#

DIMM_DRAMRST# <11>

C617 0.047U_0402_16V7K

<18> RST_GATE

RST_GATE

JDIMM1

		+DIMM_VREFDQA	1	VREF_DQ	VSS1	2	
		DDR_A_D0	3	VSS2	DQ4	4	DDR_A_D4
		DDR_A_D1	5	DQ0	DQ5	6	DDR_A_D5
			7	DQ1	VSS3	8	
		DDR_A_DM0	9	VSS4	DQS#0	10	DDR_A_DQS#0
			11	DM0	DQS0	12	DDR_A_DQS0
		DDR_A_D2	13	VSS5	DQ6	14	DDR_A_D6
		DDR_A_D3	15	DQ2	DQ7	16	DDR_A_D7
		DDR_A_D8	17	DQ3	VSS8	18	
		DDR_A_D9	19	VSS7	DQ12	20	DDR_A_D12
			21	DQ8	DQ13	22	DDR_A_D13
		DDR_A_DQS#1	23	DQ9	VSS10	24	
		DDR_A_DQS1	25	VSS9	DM1	26	DDR_A_DM1
			27	DQS#1	RESET#	28	DIMM_DRAMRST#
		DDR_A_D10	29	DQS1	VSS12	30	
		DDR_A_D11	31	VSS11	DQ14	32	DDR_A_D14
			33	DQ10	DQ15	34	DDR_A_D15
		DDR_A_D16	35	DQ11	VSS14	36	
		DDR_A_D17	37	VSS13	DQ20	38	DDR_A_D20
			39	DQ16	DQ21	40	DDR_A_D21
		DDR_A_DQS#2	41	DQ17	VSS16	42	
		DDR_A_DQS2	43	VSS15	DM2	44	DDR_A_DM2
			45	DQS#2	VSS17	46	
		DDR_A_D18	47	DQS2	DQ22	48	DDR_A_D22
		DDR_A_D19	49	VSS18	DQ23	50	DDR_A_D23
			51	DQ18	VSS19	52	
		DDR_A_D24	53	DQ19	DQ28	54	DDR_A_D28
		DDR_A_D25	55	VSS20	DQ29	56	DDR_A_D29
			57	DQ24	VSS21	58	
		DDR_A_DM3	59	DQ25	DQS#3	60	DDR_A_DQS#3
			61	VSS22	DQS3	62	DDR_A_DQS3
		DDR_A_D26	63	DM3	VSS24	64	
		DDR_A_D27	65	VSS23	DQ30	66	DDR_A_D30
			67	DQ26	DQ31	68	DDR_A_D31
			69	DQ27	VSS26	70	
			71	VSS25		72	
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			75	VDD1	VDD2	76	
			77	NC1	A15	78	DDR_A_MA15
<6> DDR_A_BS2		DDR_A_BS2	79	BA2	A14	80	DDR_A_MA14
			81	VDD3	VDD4	82	
		DDR_A_MA12	83	A12/BC#	A11	84	DDR_A_MA11
		DDR_A_MA9	85	A9	A7	86	DDR_A_MA7
			87	VDD5	VDD6	88	
		DDR_A_MA8	89	A8	A6	90	DDR_A_MA6
		DDR_A_MA5	91	A5	A4	92	DDR_A_MA4
			93	VDD7	VDD8	94	
		DDR_A_MA3	95	A3	A2	96	DDR_A_MA2
		DDR_A_MA1	97	A1	A0	98	DDR_A_MA0
			99	VDD9	VDD10	100	
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<6> DDR_A_CLK0#		DDR_A_CLK0#	103	CK0#	CK1#	104	DDR_A_CLK1# DDR_A_CLK1# <6>
			105	VDD11	VDD12	106	
		DDR_A_MA10	107	A10/AP	BA1	108	DDR_A_BS1 DDR_A_BS1 <6>
<6> DDR_A_BS0		DDR_A_BS0	109	BA0	RAS#	110	DDR_A_RAS# DDR_A_RAS# <6>
			111	VDD13	VDD14	112	
<6> DDR_A_WE#		DDR_A_WE#	113	WE#	S0#	114	DDR_A_CS0# DDR_A_CS0# <6>
<6> DDR_A_CAS#		DDR_A_CAS#	115	CAS#	ODT0	116	DDR_A_ODT0 DDR_A_ODT0 <6>
			117	VDD15	VDD16	118	
		DDR_A_MA13	119	A13	ODT1	120	DDR_A_ODT1 DDR_A_ODT1 <6>
<6> DDR_A_CS1#		DDR_A_CS1#	121	S1#	NC2	122	
			123	VDD17	VDD18	124	
			125	NCTEST	VREF_CA	126	DDR_VREF_CA_DIMMA R108 1 2 0_0402_5%
			127	VSS27	VSS28	128	
		DDR_A_D32	129	DQ32	DQ36	130	DDR_A_D36
		DDR_A_D33	131	DQ33	DQ37	132	DDR_A_D37
			133	VSS29	VSS30	134	
		DDR_A_DQS#4	135	DQS#4	DM4	136	DDR_A_DM4
		DDR_A_DQS4	137	DQS4	VSS31	138	
			139	VSS32	DQ38	140	DDR_A_D38
		DDR_A_D34	141	DQ34	DQ39	142	DDR_A_D39
		DDR_A_D35	143	DQ35	VSS33	144	
			145	VSS34	DQ44	146	**DDR_A_D44**
		DDR_A_D40	147	DQ40	DQ45	148	DDR_A_D45
		DDR_A_D41	149	DQ41	VSS35	150	
			151	VSS36	DQS#5	152	DDR_A_DQS#5
		DDR_A_DM5	153	DM5	DQS5	154	DDR_A_DQS5
			155	VSS37	VSS38	156	
		DDR_A_D42	157	DQ42	DQ46	158	DDR_A_D46
		DDR_A_D43	159	DQ43	DQ47	160	DDR_A_D47
			161	VSS39	VSS40	162	
		DDR_A_D48	163	DQ48	DQ52	164	DDR_A_D52
		DDR_A_D49	165	DQ49	DQ53	166	DDR_A_D53
			167	VSS41	VSS42	168	
		DDR_A_DQS#6	169	DQS#6	DM6	170	DDR_A_DM6
		DDR_A_DQS6	171	DQS6	VSS43	172	
			173	VSS44	DQ54	174	DDR_A_D54
		DDR_A_D50	175	DQ50	DQ55	176	DDR_A_D55
		DDR_A_D51	177	DQ51	VSS45	178	
			179	VSS46	DQ60	180	DDR_A_D60
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		DDR_A_D57	183	DQ57	VSS47	184	
			185	VSS48	DQS#7	186	DDR_A_DQS#7
		DDR_A_DM7	187	DM7	DQS7	188	DDR_A_DQS7
			189	VSS49	VSS50	190	
		DDR_A_D58	191	DQ58	DQ62	192	DDR_A_D62
		DDR_A_D59	193	DQ59	DQ63	194	DDR_A_D63
			195	VSS51	VSS52	196	
		R109 1 2 10K_0402_5%	197	SA0	EVENT#	198	PM_EXTTS#0_1 PM_EXTTS#0_1 <5,11>
+3VSO			199	VDDSPD	SDA	200	D_CK_SDATA D_CK_SDATA <11,12>
			201	SA1	SCL	202	D_CK_SCLK D_CK_SCLK <11,12>
			203	VTT1	VTT2	204	+0.75VS
			205	G1	G2	206	

FOX_AS0A626-U8RN-7F

+1.5V

+1.5V

+DIMM_VREFCA

C135 2.2U_0603_6.3V6K

C136 0.1U_0402_16V4Z

C148 2.2U_0603_6.3V6K

C149 0.1U_0402_16V4Z

R110 10K_0402_5%

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V

C137 10U_0805_6.3V6M

C138 10U_0805_6.3V6M

C139 10U_0805_6.3V6M

C140 10U_0805_6.3V6M

C141 10U_0805_6.3V6M

C142 10U_0805_6.3V6M

C143 0.1U_0402_16V4Z

C144 0.1U_0402_16V4Z

C145 0.1U_0402_16V4Z

C146 0.1U_0402_16V4Z

@C147 330U_2.5V_M_R15

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.75VS

C150 1U_0402_6.3V6K

C151 1U_0402_6.3V6K

C152 1U_0402_6.3V6K

C153 1U_0402_6.3V6K

C154 10U_0805_6.3V6M

DDR3 SO-DIMM A
Change to Reverse Type
8mm High

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

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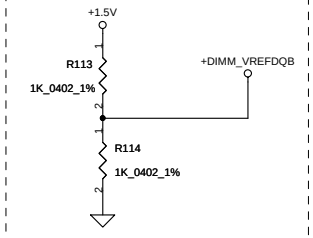
2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

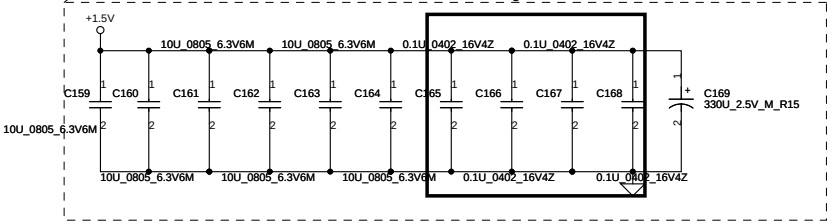
<6> DDR_B_DQS#[0..7]
<6> DDR_B_D[0..63]
<6> DDR_B_DM[0..7]
<6> DDR_B_DQS[0..7]
<6> DDR_B_MA[0..15]

DIMMB VREFDQ M1 Circuit

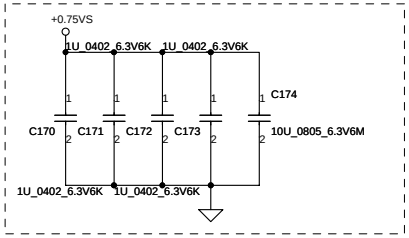


Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



Layout Note:
Place near JDIMM2.203 & JDIMM2.204



M1 Circuit
+DIMM_VREFDQB
C155 2.2U_0603_6.3V6K
C156 0.1U_0402_16V4Z

JDIMM2

		+DIMM_VREFDQB	1	VREF_DQ	VSS1	2	
			3	VSS2	DQ4	4	DDR_B_D4
		DDR_B_D0	5	DQ0	DQ5	6	DDR_B_D5
		DDR_B_D1	7	DQ1	VSS3	8	
		DDR_B_DM0	9	VSS4	DQS#0	10	DDR_B_DQS#0
			11	DM0	DQS0	12	DDR_B_DQS0
		DDR_B_D2	13	VSS5	DQ6	14	DDR_B_D6
		DDR_B_D3	15	DQ2	DQ7	16	DDR_B_D7
		DDR_B_D8	17	DQ3	VSS8	18	
		DDR_B_D9	19	VSS7	DQ12	20	DDR_B_D12
		DDR_B_DQS#1	21	DQ8	DQ13	22	DDR_B_D13
		DDR_B_DQS1	23	DQ9	VSS10	24	
		DDR_B_D10	25	VSS9	DM1	26	DDR_B_DM1
		DDR_B_D11	27	DQS#1	RESET#	28	DIMM_DRAMRST#
		DDR_B_D16	29	DQS1	VSS12	30	DIMM_DRAMRST# <10>
		DDR_B_D17	31	VSS11	DQ14	32	DDR_B_D14
		DDR_B_DQS#2	33	DQ10	DQ15	34	DDR_B_D15
		DDR_B_DQS2	35	DQ11	VSS14	36	
		DDR_B_D18	37	VSS13	DQ20	38	DDR_B_D20
		DDR_B_D19	39	DQ16	DQ21	40	DDR_B_D21
		DDR_B_D24	41	DQ17	VSS16	42	
		DDR_B_D25	43	VSS15	DM2	44	DDR_B_DM2
		DDR_B_DM3	45	DQS#2	VSS17	46	
			47	DQS2	DQ22	48	DDR_B_D22
		DDR_B_D26	49	VSS18	DQ23	50	DDR_B_D23
		DDR_B_D27	51	DQ18	VSS19	52	
			53	DQ19	DQ28	54	DDR_B_D28
			55	VSS20	DQ29	56	DDR_B_D29
			57	DQ24	VSS21	58	
			59	DQ25	DQS#3	60	DDR_B_DQS#3
			61	VSS22	DQS3	62	DDR_B_DQS3
			63	DM3	VSS24	64	
			65	VSS23	DQ30	66	DDR_B_D30
			67	DQ26	DQ31	68	DDR_B_D31
			69	DQ27	VSS26	70	
			71	VSS25		72	
<6> DDR_B_CKE0		DDR_B_CKE0	73	CKE0	CKE1	74	DDR_B_CKE1
			75	VDD1	VDD2	76	DDR_B_CKE1 <6>
			77	NC1	A15	78	DDR_B_MA15
<6> DDR_B_BS2		DDR_B_BS2	79	BA2	A14	80	DDR_B_MA14
			81	VDD3	VDD4	82	
		DDR_B_MA12	83	A12/BC#	A11	84	DDR_B_MA11
		DDR_B_MA9	85	A9	A7	86	DDR_B_MA7
			87	VDD5	VDD6	88	
		DDR_B_MA8	89	A8	A6	90	DDR_B_MA6
		DDR_B_MA5	91	A5	A4	92	DDR_B_MA4
			93	VDD7	VDD8	94	
		DDR_B_MA3	95	A3	A2	96	DDR_B_MA2
		DDR_B_MA1	97	A1	A0	98	DDR_B_MA0
			99	VDD9	VDD10	100	
<6> DDR_B_CLK0		DDR_B_CLK0	101	CK0	CK1	102	DDR_B_CLK1
<6> DDR_B_CLK0#		DDR_B_CLK0#	103	CK0#	CK1#	104	DDR_B_CLK1 <6>
			105	VDD11	VDD12	106	DDR_B_CLK1# <6>
		DDR_B_MA10	107	A10/AP	BA1	108	DDR_B_BS1
<6> DDR_B_BS0		DDR_B_BS0	109	BA0	RAS#	110	DDR_B_BS1 <6>
			111	VDD13	VDD14	112	DDR_B_RAS#
		DDR_B_WE#	113	WE#	S0#	114	DDR_B_RAS# <6>
<6> DDR_B_WE#							DDR_B_CS0#
<6> DDR_B_CAS#		DDR_B_CAS#	115	CAS#	ODT0	116	DDR_B_CS0# <6>
			117	VDD15	VDD16	118	DDR_B_ODT0
		DDR_B_MA13	119	A13	ODT1	120	DDR_B_ODT0 <6>
<6> DDR_B_CS1#		DDR_B_CS1#	121	S1#	NC2	122	DDR_B_ODT1
			123	VDD17	VDD18	124	DDR_B_ODT1 <6>
			125	NCTEST	VREF_CA	126	+DIMM_VREFCA
			127	VSS27	VSS28	128	DDR_VREF_CA_DIMMB R115 1 2 0_0402_5%
		DDR_B_D32	129	DQ32	DQ36	130	DDR_B_D36
		DDR_B_D33	131	DQ33	DQ37	132	DDR_B_D37
			133	VSS29	VSS30	134	
		DDR_B_DQS#4	135	DQS#4	DM4	136	DDR_B_DM4
		DDR_B_DQS4	137	DQS4	VSS31	138	
			139	VSS32	DQ38	140	DDR_B_D38
		DDR_B_D34	141	DQ34	DQ39	142	DDR_B_D39
		DDR_B_D35	143	DQ35	VSS33	144	
			145	VSS34	DQ44	146	DDR_B_D44
		DDR_B_D40	147	DQ40	DQ45	148	DDR_B_D45
		DDR_B_D41	149	DQ41	VSS35	150	
			151	VSS36	DQS#5	152	DDR_B_DQS#5
		DDR_B_DM5	153	DM5	DQS5	154	DDR_B_DQS5
			155	VSS37	VSS38	156	
		DDR_B_D42	157	DQ42	DQ46	158	DDR_B_D46
		DDR_B_D43	159	DQ43	DQ47	160	DDR_B_D47
			161	VSS39	VSS40	162	
		DDR_B_D48	163	DQ48	DQ52	164	DDR_B_D52
		DDR_B_D49	165	DQ49	DQ53	166	DDR_B_D53
			167	VSS41	VSS42	168	
		DDR_B_DQS#6	169	DQS#6	DM6	170	DDR_B_DM6
		DDR_B_DQS6	171	DQS6	VSS43	172	
			173	VSS44	DQ54	174	DDR_B_D54
		DDR_B_D50	175	DQ50	DQ55	176	DDR_B_D55
		DDR_B_D51	177	DQ51	VSS45	178	
			179	VSS46	DQ60	180	DDR_B_D60
		DDR_B_D56	181	DQ56	DQ61	182	DDR_B_D61
		DDR_B_D57	183	DQ57	VSS47	184	
			185	VSS48	DQS#7	186	DDR_B_DQS#7
		DDR_B_DM7	187	DM7	DQS7	188	DDR_B_DQS7
			189	VSS49	VSS50	190	
		DDR_B_D58	191	DQ58	DQ62	192	DDR_B_D62
		DDR_B_D59	193	DQ59	DQ63	194	DDR_B_D63
			195	VSS51	VSS52	196	
			197	SA0	EVENT#	198	PM_EXTTS#0_1
+3VSO		R116 1 2 10K_0402_5%	199	VDDSPD	SDA	200	PM_EXTTS#0_1 <5,10>
		R117 1 2 10K_0402_5%	201	SA1	SCL	202	D_CK_SDATA <10,12>
			203	VTT1	VTT2	204	D_CK_SCLK <10,12>
			205	G1	G2	206	+0.75VS

C175 2.2U_0603_6.3V6K
C176 0.1U_0402_16V4Z
FOX_AS0A626-U4RN-7F
CONN@

C157 2.2U_0603_6.3V6K
C158 0.1U_0402_16V4Z

DDR3 SO-DIMM B
Reverse Type
4mm High

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Issued Date	2009/08/01	Deciphered Date	2010/08/01

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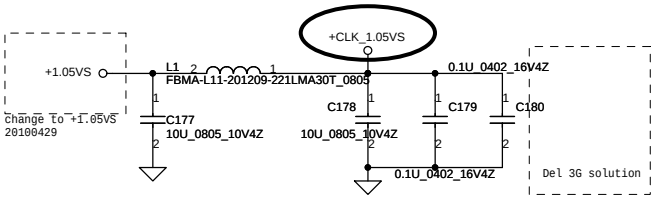
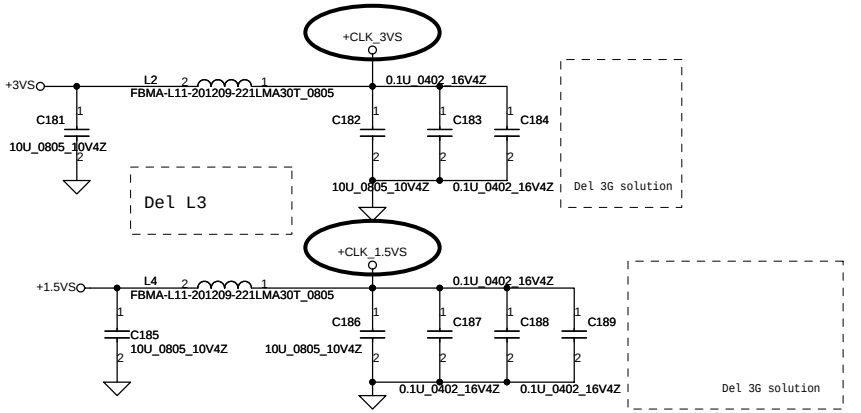
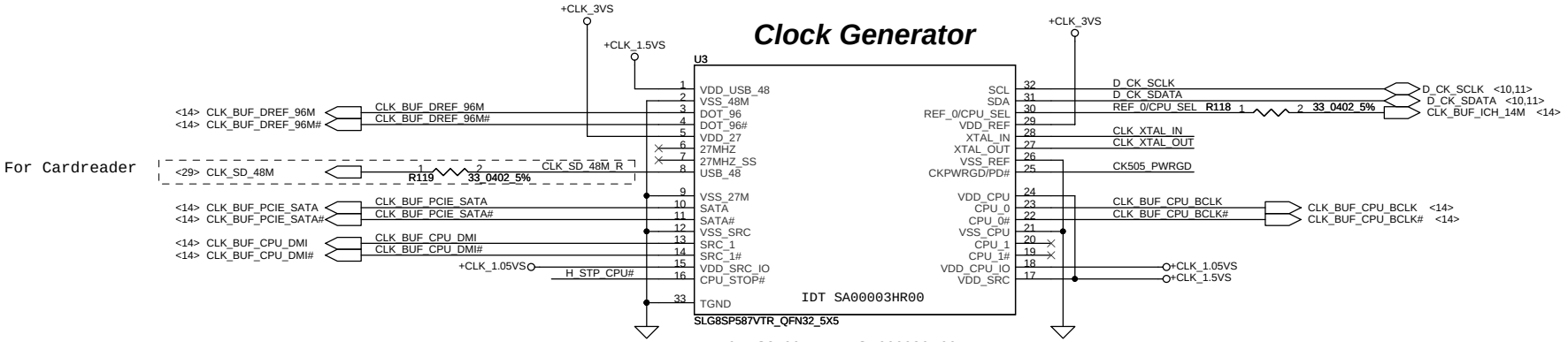




Clock Generator



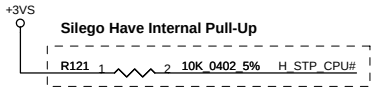
IDT: 9LRS3199AKLFT, SA000030P00

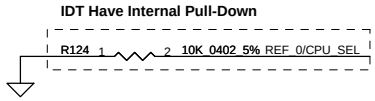
SILEGO: SLG8SP587V(WF), SA00002XY10

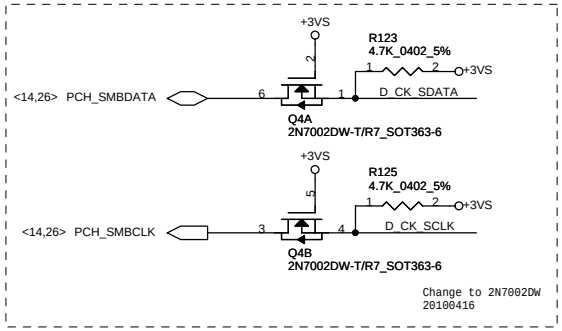
Low Power:

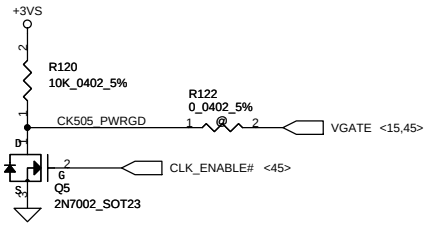
IDT: 9LVS3199AKLFT, SA00003HR00

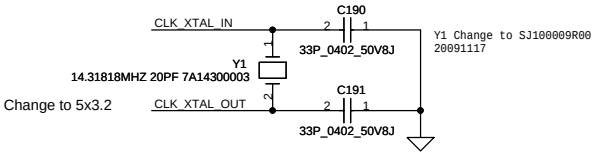
Realtek: RTM890N-631-GRT, SA00003HQ00











PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

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Issued Date	2009/08/01	Deciphered Date	2010/08/01

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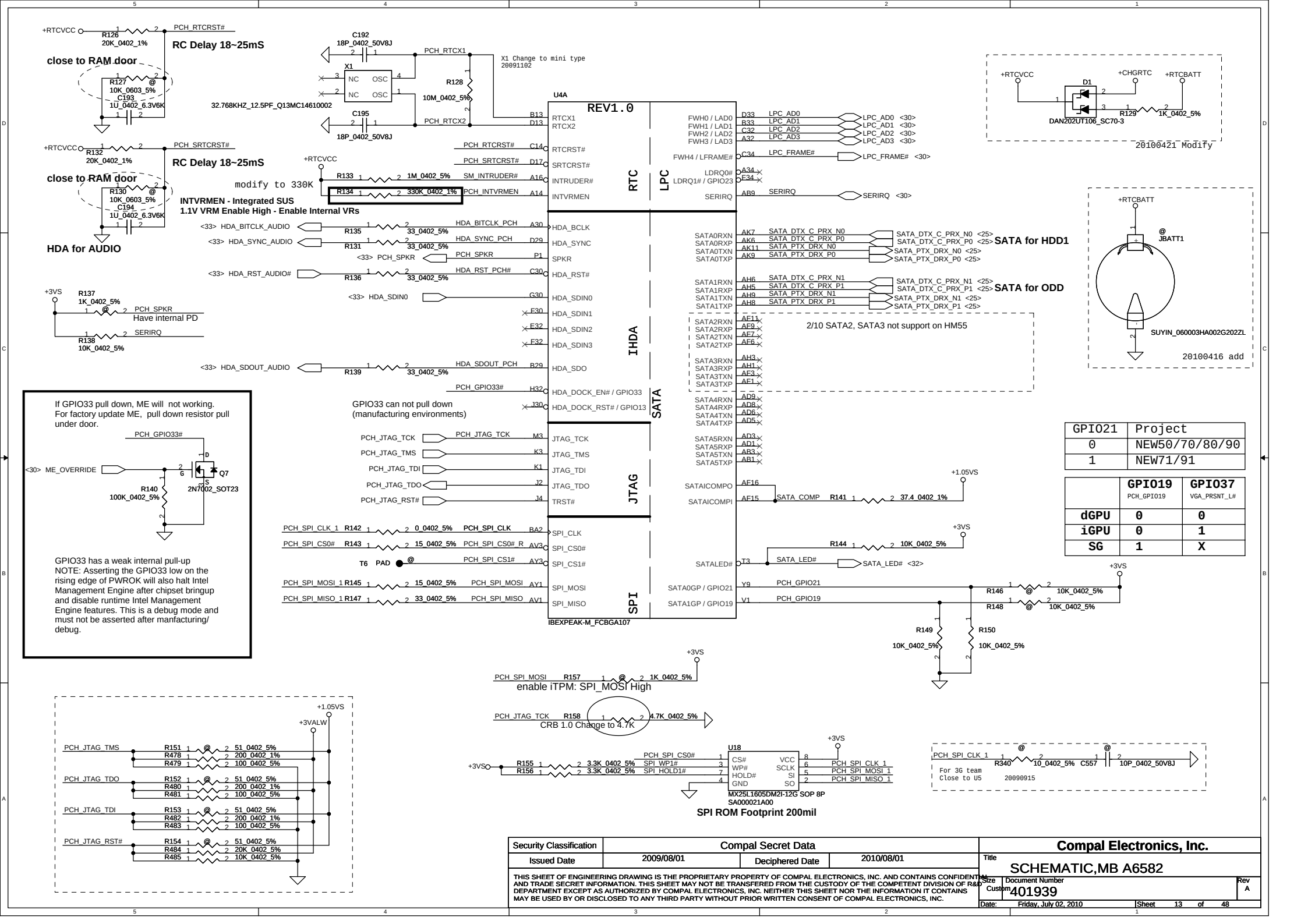

GPIO21	Project
0	NEW50/70/80/90
1	NEW71/91

	GPIO19 PCH_GPIO19	GPIO37 VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
SG	1	X

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1. Connect Directly
   EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS
   CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS
   LAN
4. Level Shift3, Pull-Up to +3VS
   CPU & PCH XDP

U4B

REV1.0

PCI-E*

SMBus

Controller Link

PEG

From CLK BUFFER

Clock Flex

IBEXPEAK-M_FCBGA107

For PCIE LAN

<27> PCIE_DTX_C_PRX_N1 — PCIE_DTX_C_PRX_N1 BG30 — PERN1
<27> PCIE_DTX_C_PRX_P1 — PCIE_DTX_C_PRX_P1 BJ30 — PERP1
<27> PCIE_PTX_C_DRX_N1 — C197 2 1 0.1U_0402_16V7K — PCIE_PTX_DRX_N1 BF29 — PETN1
<27> PCIE_PTX_C_DRX_P1 — C198 2 1 0.1U_0402_16V7K — PCIE_PTX_DRX_P1 BH29 — PETP1

For Wireless LAN

<26> PCIE_DTX_C_PRX_N2 — PCIE_DTX_C_PRX_N2 AW30 — PERN2
<26> PCIE_DTX_C_PRX_P2 — PCIE_DTX_C_PRX_P2 BA30 — PERP2
<26> PCIE_PTX_C_DRX_N2 — C199 2 1 0.1U_0402_16V7K — PCIE_PTX_DRX_N2 BC30 — PETN2
<26> PCIE_PTX_C_DRX_P2 — C200 2 1 0.1U_0402_16V7K — PCIE_PTX_DRX_P2 BD30 — PETP2

AU30 PERN3
AT30 PERP3
AU32 PETN3
AV32 PETP3

BA32 PERN4
BB32 PERP4
BD32 PETN4
BE32 PETP4

BE33 PERN5
BH33 PERP5
BG32 PETN5
BJ32 PETP5

BA34 PERN6
AW34 PERP6
BC34 PETN6
BD34 PETP6

2/10 PCIE7, PCIE8 not support on HM55

AT34 PERN7
AU34 PERP7
AU36 PETN7
AV36 PETP7

BG34 PERN8
BJ34 PERP8
BG36 PETN8
BJ36 PETP8

For PCIE LAN

<27> CLK_PCIE_LAN# — AK48 — CLKOUT_PCIE0N
<27> CLK_PCIE_LAN — AK47 — CLKOUT_PCIE0P

<27> LAN_CLKREQ# — R164 1 2 0_0402_5% — PCH_GPIO73 — P9 — PCIECLKRQ0# / GPIO73

For Wireless LAN

<26> CLK_PCIE_MINI1# — AM43 — CLKOUT_PCIE1N
<26> CLK_PCIE_MINI1 — AM45 — CLKOUT_PCIE1P

<26> MINI1_CLKREQ# — R165 1 2 0_0402_5% — PCH_GPIO18 — U4 — PCIECLKRQ1# / GPIO18

AM47 CLKOUT_PCIE2N
AM48 CLKOUT_PCIE2P

PCH_GPIO20 — N4 — PCIECLKRQ2# / GPIO20

AH42 CLKOUT_PCIE3N
AH41 CLKOUT_PCIE3P

PCH_GPIO25 — A8 — PCIECLKRQ3# / GPIO25

AM51 CLKOUT_PCIE4N
AM53 CLKOUT_PCIE4P

PCH_GPIO26 — M9 — PCIECLKRQ4# / GPIO26

AJ50 CLKOUT_PCIE5N
AJ52 CLKOUT_PCIE5P

PCH_GPIO44 — H6 — PCIECLKRQ5# / GPIO44

AK53 CLKOUT_PEG_B_N
AK51 CLKOUT_PEG_B_P

PCH_GPIO56 — P13 — PEG_B_CLKRQ# / GPIO56

SMBALERT# / GPIO11 — B9 — EC_LID_OUT# — EC_LID_OUT# <30>
SMBCLK — H14 — PCH_SMBCLK — PCH_SMBCLK <12,26>
SMBDATA — C8 — PCH_SMBDATA — PCH_SMBDATA <12,26>

SML0ALERT# / GPIO60 — J14 — PCH_GPIO60
SML0CLK — C6
SML0DATA — G8

SML1ALERT# / GPIO74 — M14 — PCH_GPIO74
SML1CLK / GPIO58 — E10 — PCH_SML1CLK
SML1DATA / GPIO75 — G12 — PCH_SML1DAT

CL_CLK1 — T13
CL_DATA1 — T11
CL_RST1# — T9

+3VALW
R159 10K_0402_5%
20090915 Add

PEG_A_CLKRQ# / GPIO47 — H1 — PEG_CLKREQ#

CLKOUT_PEG_A_N — AD43
CLKOUT_PEG_A_P — AD45

CLKOUT_DMI_N — AN4 — CLK_CPU_DMI# <5>
CLKOUT_DMI_P — AN2 — CLK_CPU_DMI <5>

CLKOUT_DP_N / CLKOUT_BCLK1_N — AT1 — CLK_CPU_DP# <5>
CLKOUT_DP_P / CLKOUT_BCLK1_P — AT3 — CLK_CPU_DP <5>

CLKIN_DMI_N — AW24 — CLK_BUF_CPU_DMI# <12>
CLKIN_DMI_P — BA24 — CLK_BUF_CPU_DMI <12>

CLKIN_BCLK_N — AP3 — CLK_BUF_CPU_BCLK# <12>
CLKIN_BCLK_P — AP1 — CLK_BUF_CPU_BCLK <12>

CLKIN_DOT_96N — F18 — CLK_BUF_DREF_96M# <12>
CLKIN_DOT_96P — F18 — CLK_BUF_DREF_96M <12>

CLKIN_SATA_N / CKSSCD_N — AH13 — CLK_BUF_PCIE_SATA# <12>
CLKIN_SATA_P / CKSSCD_P — AH12 — CLK_BUF_PCIE_SATA <12>

REFCLK14IN — P41 — R338 10_0402_5% C555 10P_0402_50V8J — CLK_BUF_ICH_14M <12>

CLKIN_PCILOOPBACK — J42 — CLK_PCI_FB <17>

XTAL25_IN — AH51 — XTAL25_IN
XTAL25_OUT — AH53 — XTAL25_OUT

XCLK_RCOMP — AF38 — XCLK_RCOMP — R169 1 2 90.9_0402_1% — +1.05VS

CLKOUTFLEX0 / GPIO64 — T45

Project Port ID

CLKOUTFLEX1 / GPIO65 — P43 — PROJECT_ID1
R171 1 2 10K_0402_5%
@R172 1 2 10K_0402_5%

CLKOUTFLEX2 / GPIO66 — T42 — PROJECT_ID0
@R174 1 2 10K_0402_5%
R175 1 2 10K_0402_5%

+3VS

CLKOUTFLEX3 / GPIO67 — N50

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

C203 27P_0402_50V8J
R170 1M_0402_5%
Y2 25MHZ_20PF_7A25000012
C204 27P_0402_50V8J
Change to 5x3.2

+3VS

MINI1_CLKREQ# R177 1 2 10K_0402_5%
PCH_GPIO20 R178 1 2 10K_0402_5%

+3VALW

EC_LID_OUT# R179 1 2 10K_0402_5%
PCH_SMBCLK R180 1 2 2.2K_0402_5%
PCH_SMBDATA R181 1 2 2.2K_0402_5%
PCH_GPIO60 R182 1 2 10K_0402_5%
PCH_SML1CLK R183 1 2 2.2K_0402_5%
PCH_SML1DAT R184 1 2 2.2K_0402_5%
PCH_GPIO74 R185 1 2 10K_0402_5%
PCH_GPIO44 R187 1 2 10K_0402_5%
PCH_GPIO56 R188 1 2 10K_0402_5%
PCH_GPIO73 R189 1 2 10K_0402_5%

+3VALW

2009/09/23:Change to +3VALW
PCH_GPIO26 R166 1 2 10K_0402_5%
PCH_GPIO25 R186 1 2 10K_0402_5%
2009/08/13: Change back to +3VALW

+3VS

PCH_SML1CLK — 6 — 1 — EC_SMB_CK2 — EC_SMB_CK2 <30>
2N7002DW-T/R7_SOT363-6
Q9A

+3VS — Pull high +3VS at KB926 side

PCH_SML1DAT — 3 — 4 — EC_SMB_DA2 — EC_SMB_DA2 <30>
2N7002DW-T/R7_SOT363-6
Q9B

0602 GPIO65 no use
PULL HIGH:PVT
PULL DOWN:DVT

GPIO66 6L/8L SATA register separe		
GPIO66	0	6L *
	1	8L

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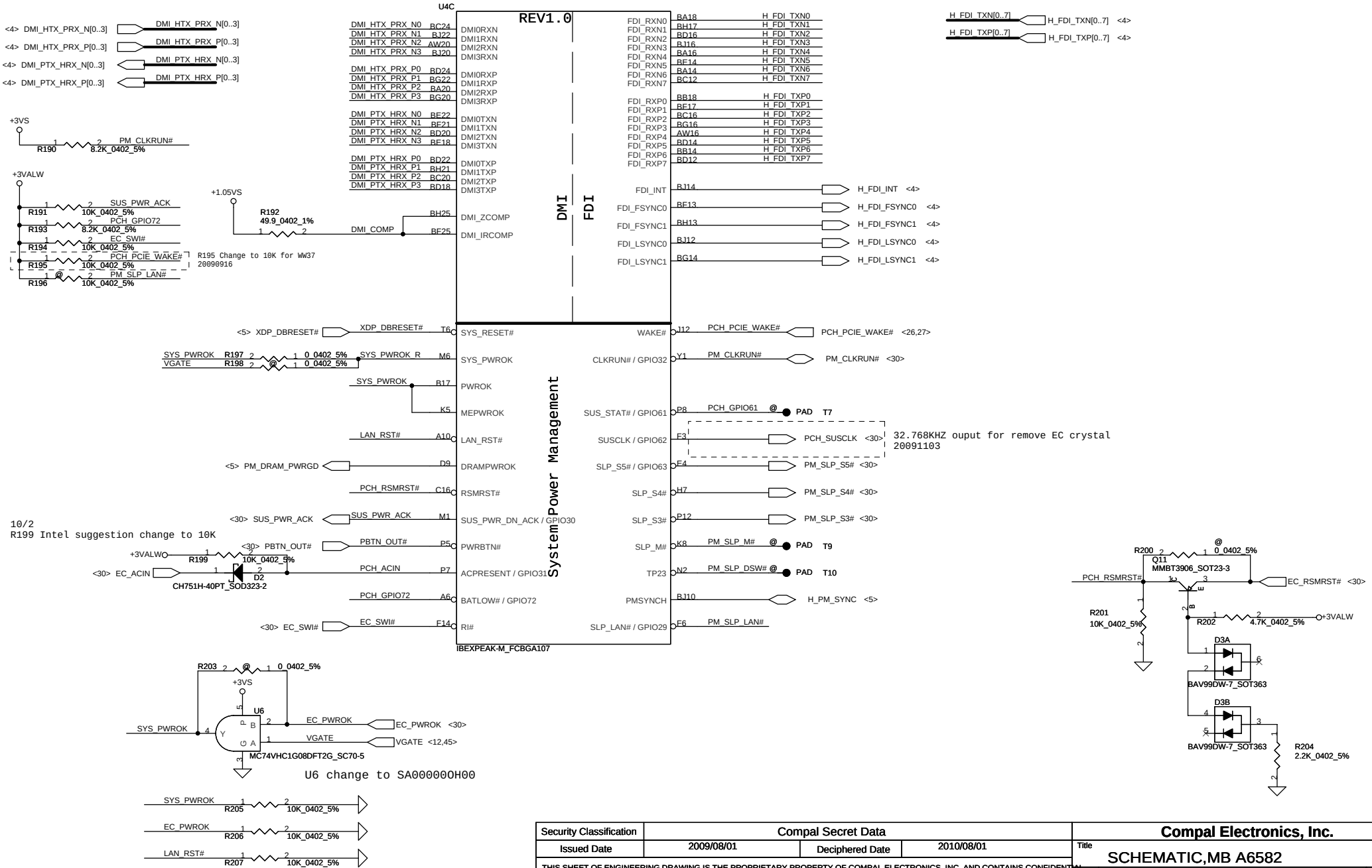

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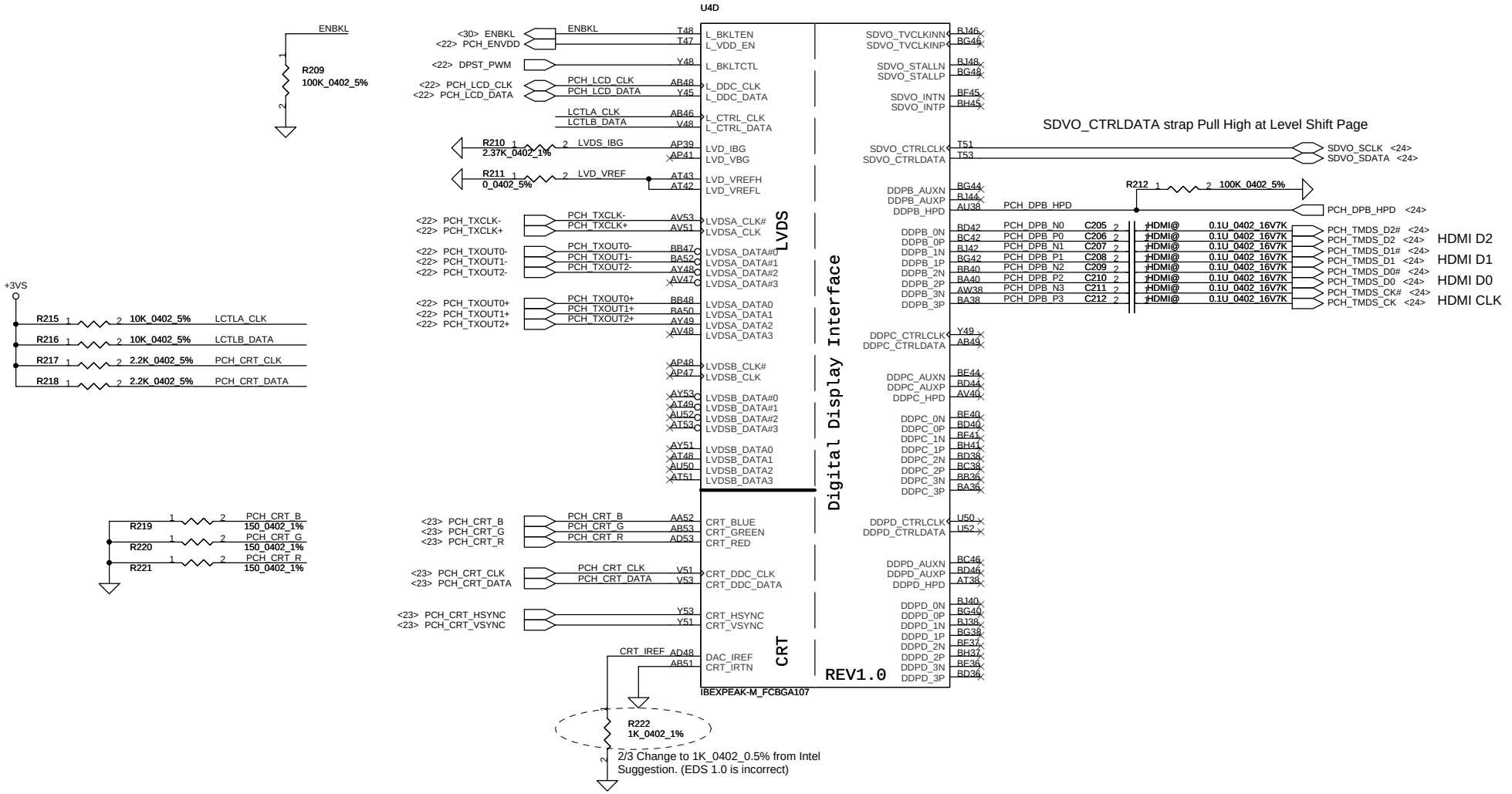

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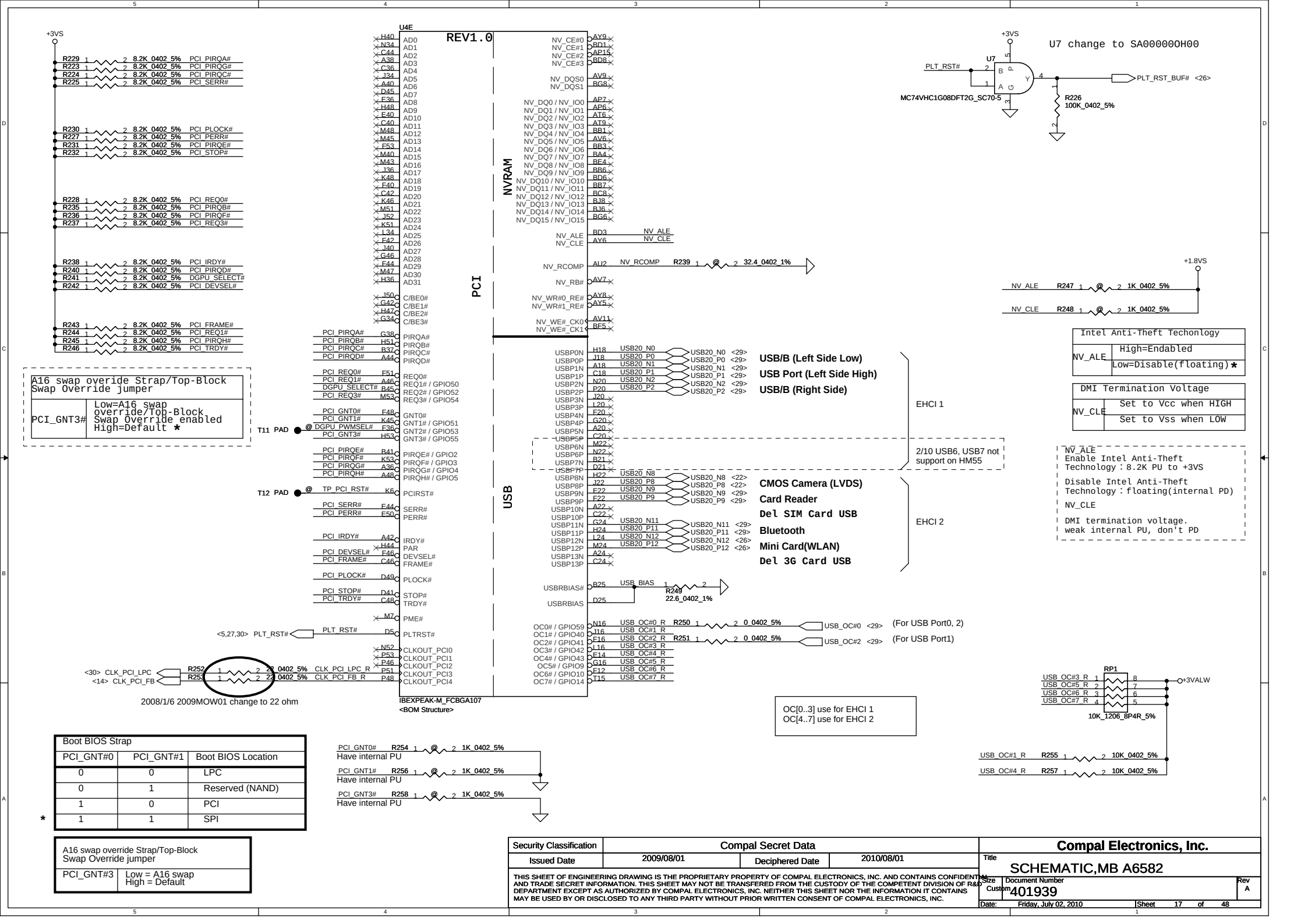

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
* 1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

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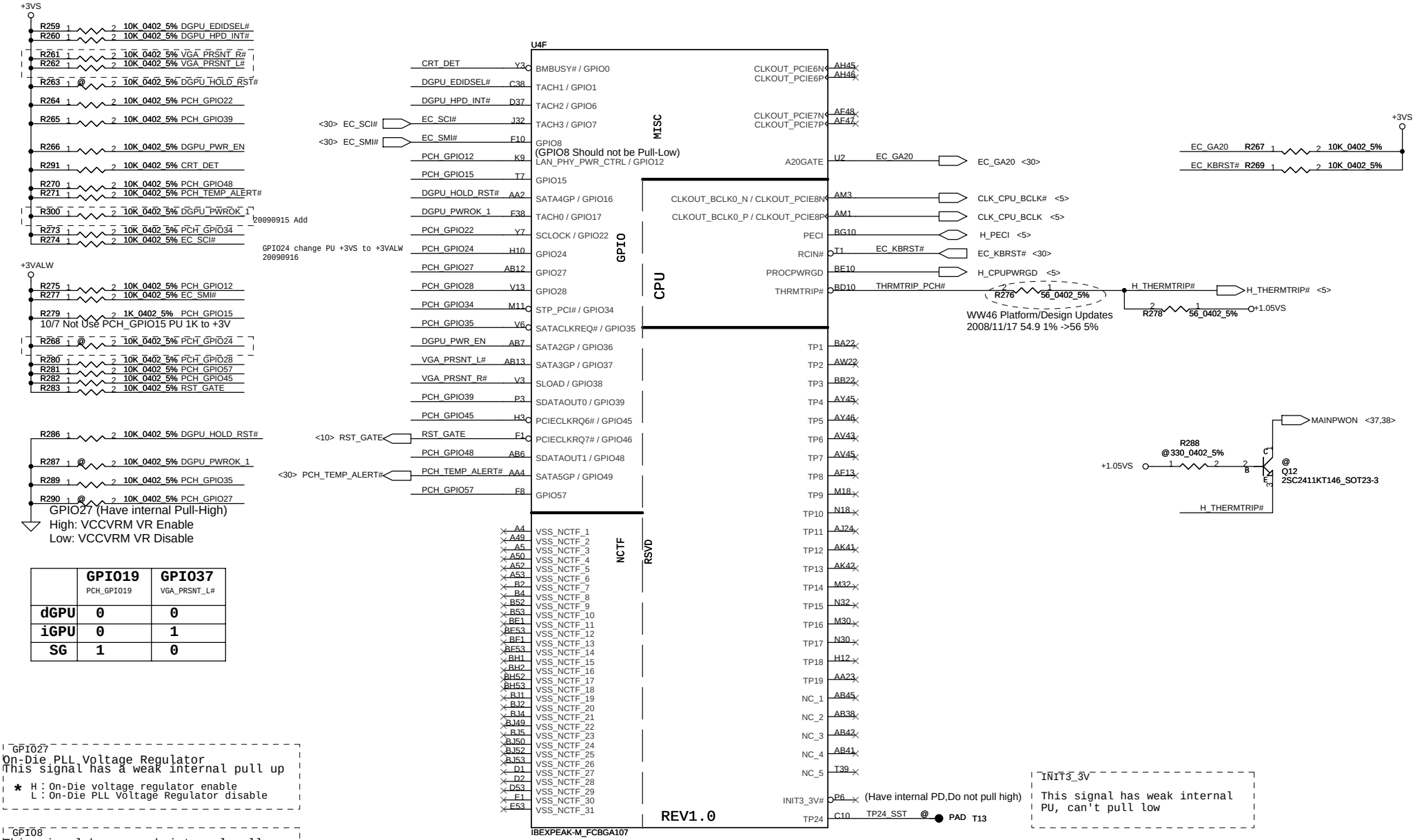

	GPIO19 PCH_GPIO19	GPIO37 VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
SG	1	0

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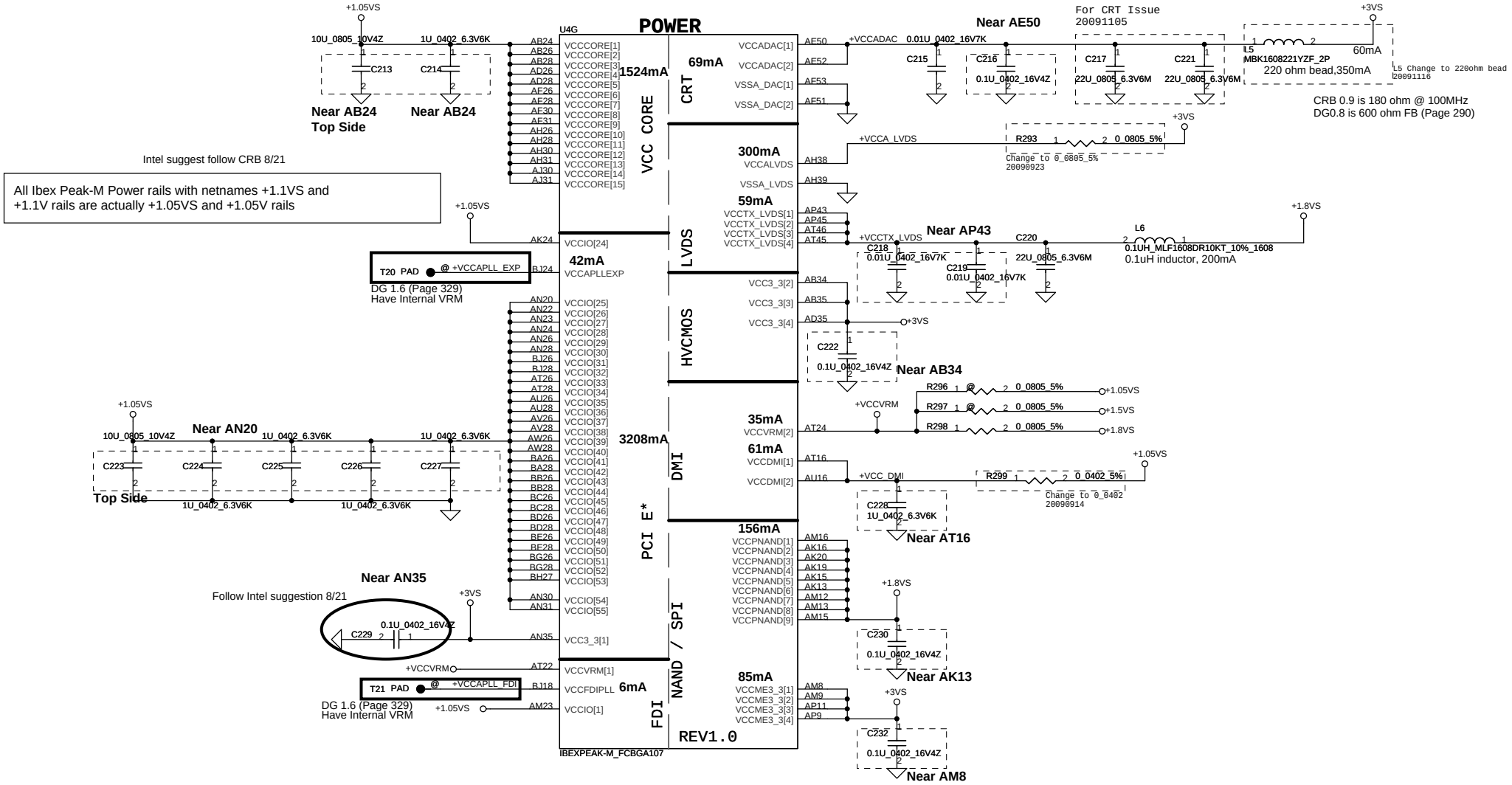

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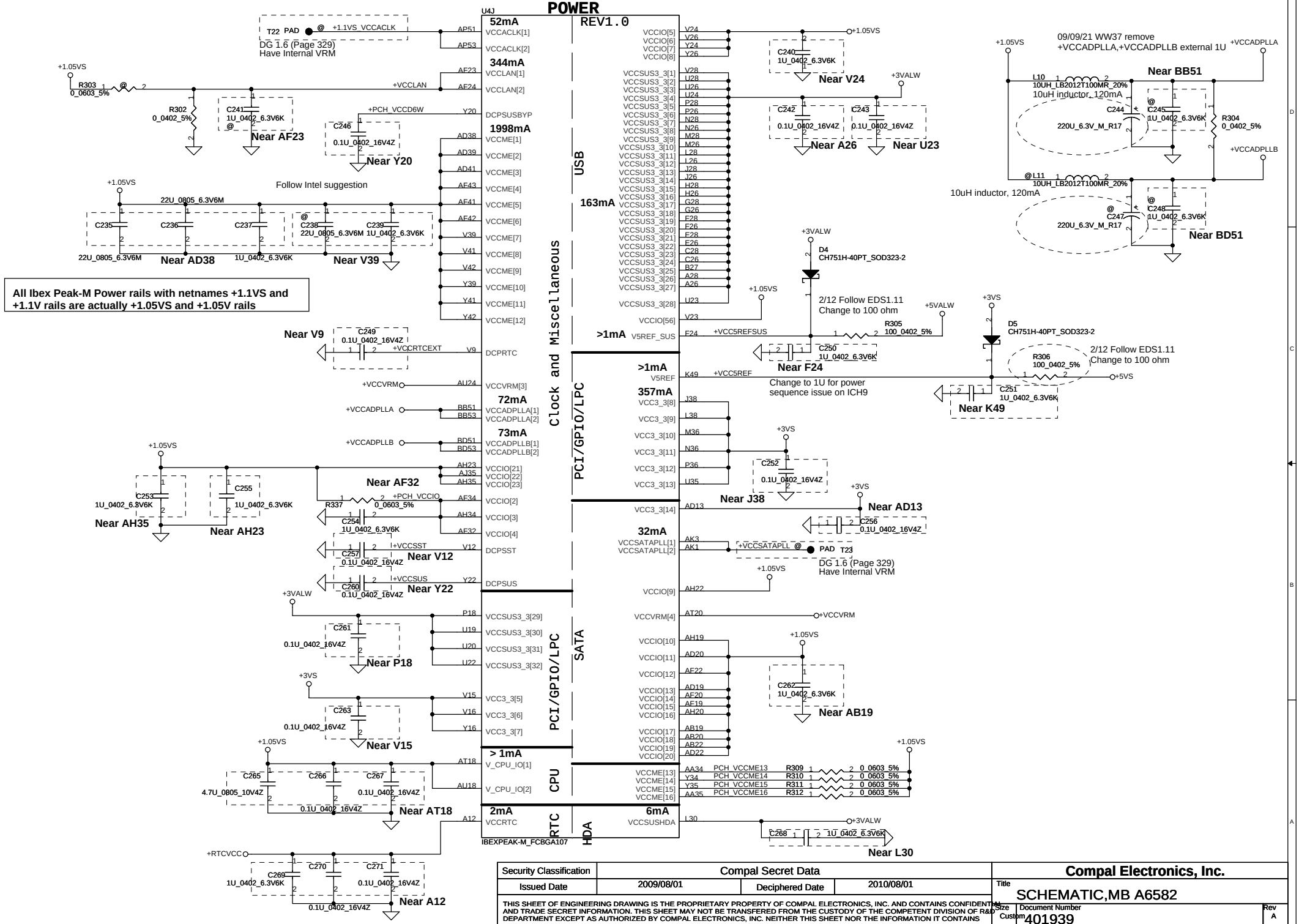

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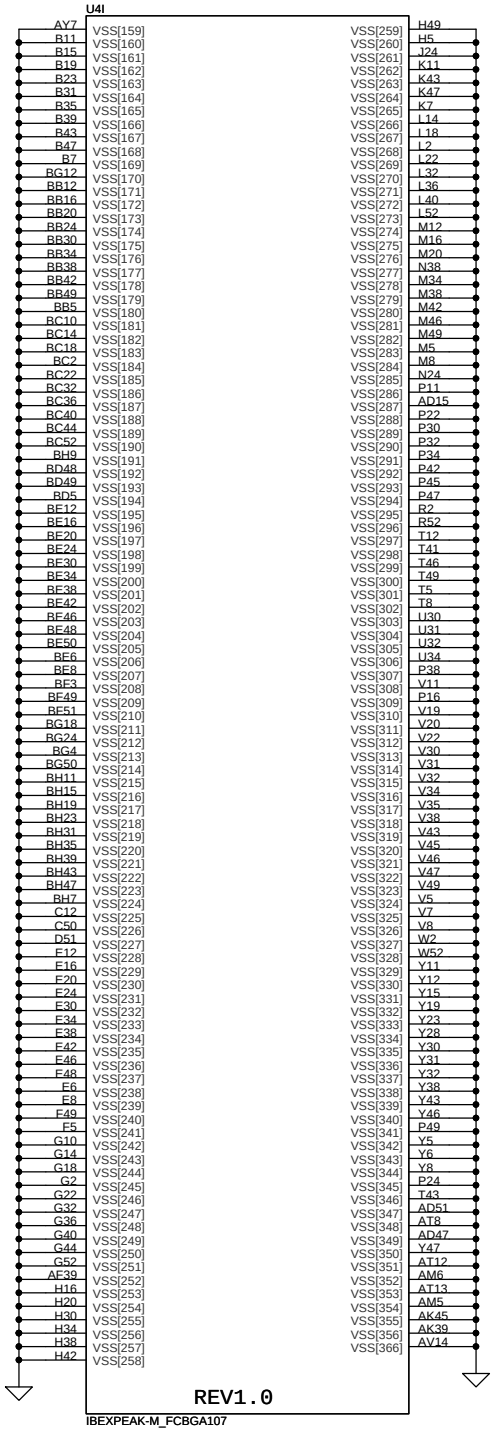

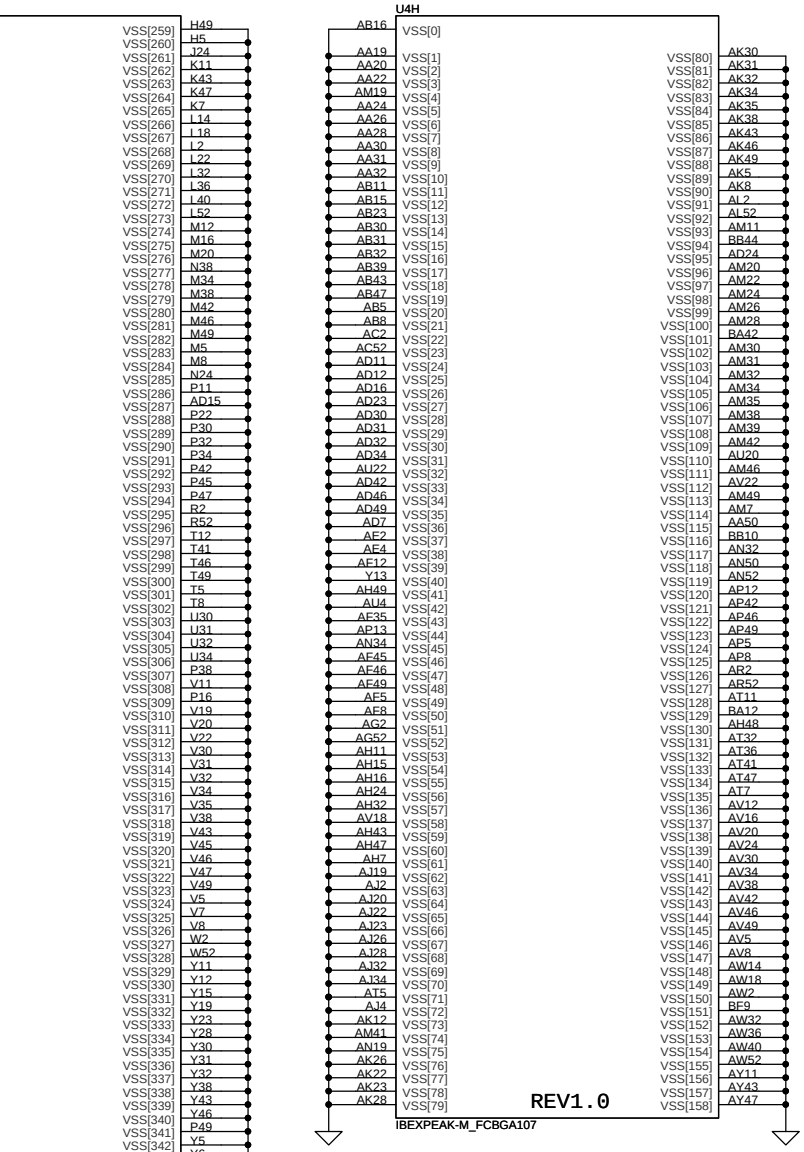

Del PCH XDP

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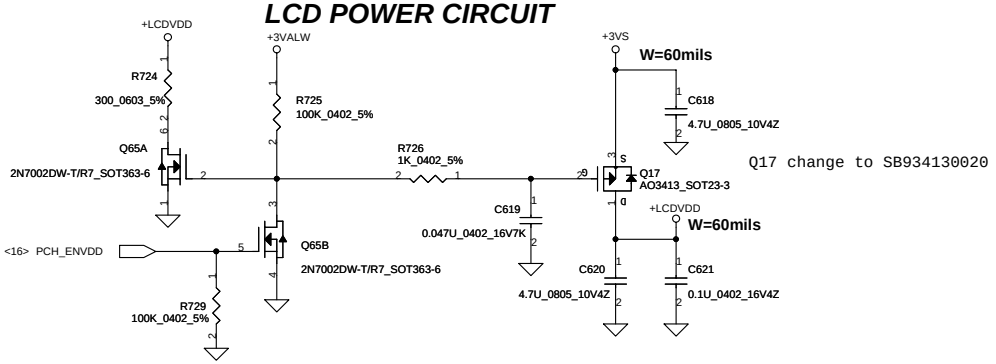
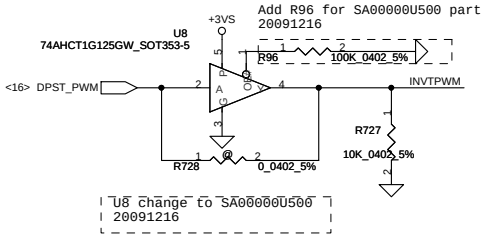
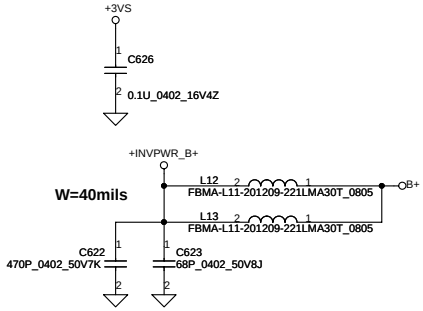
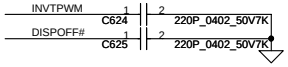
LCD POWER CIRCUIT

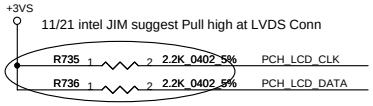


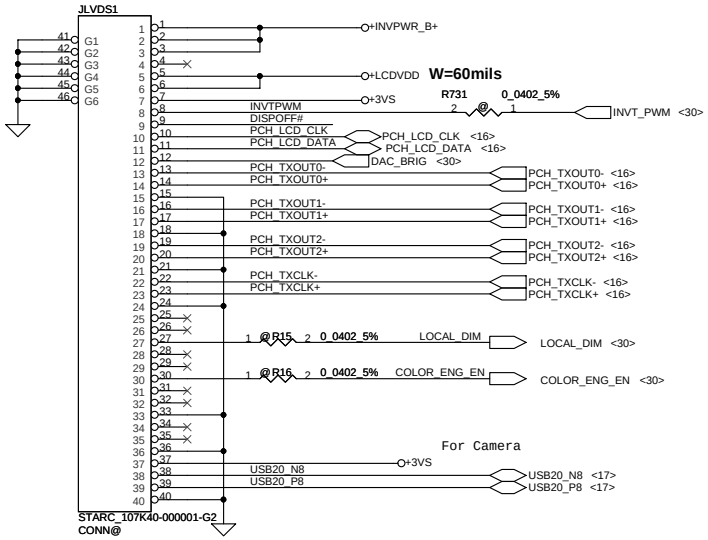


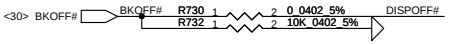
LED PANEL Conn.

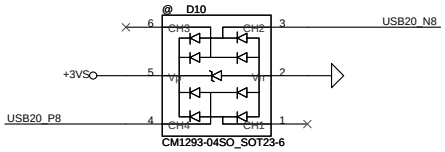












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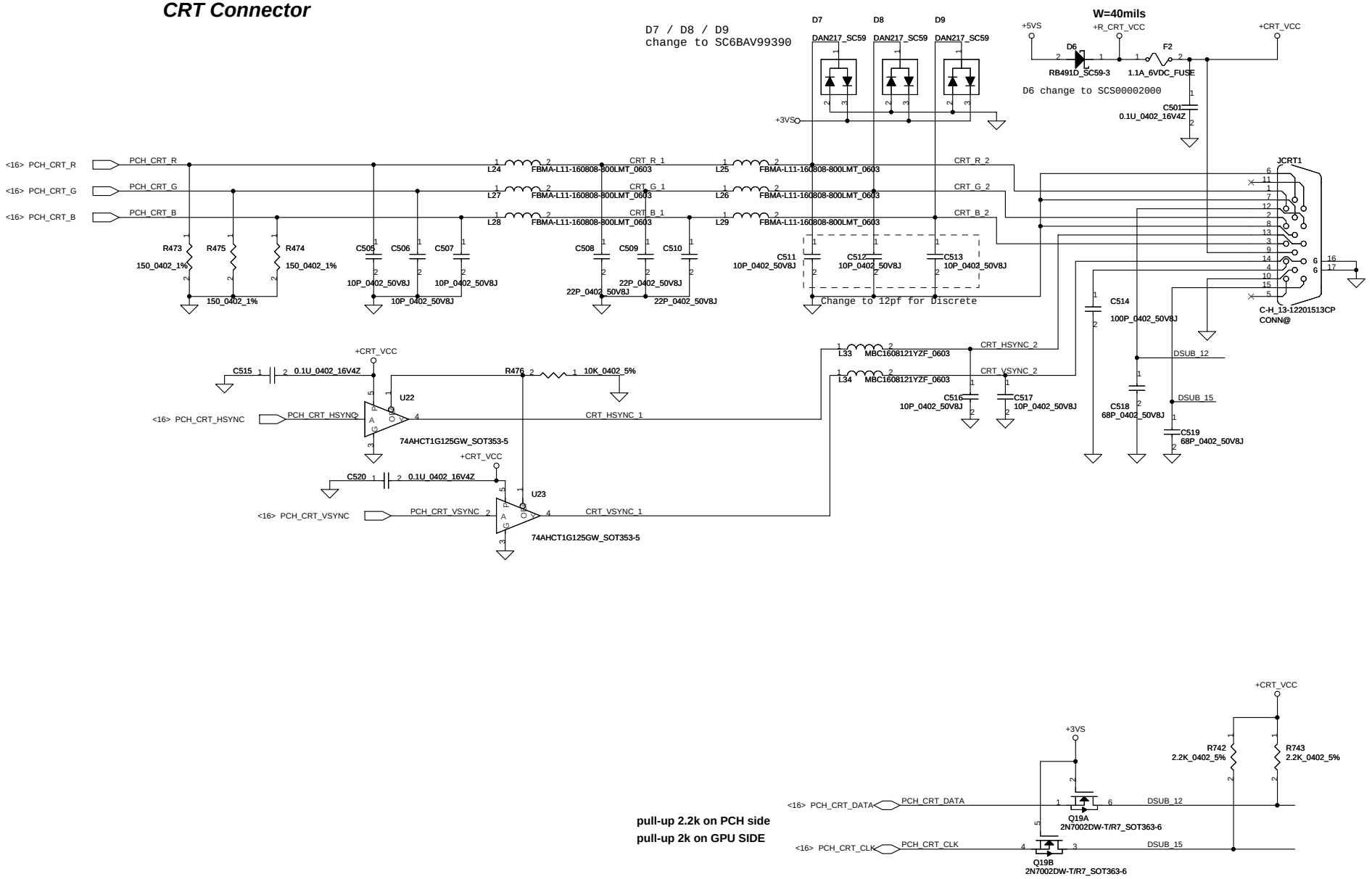
CRT Connector



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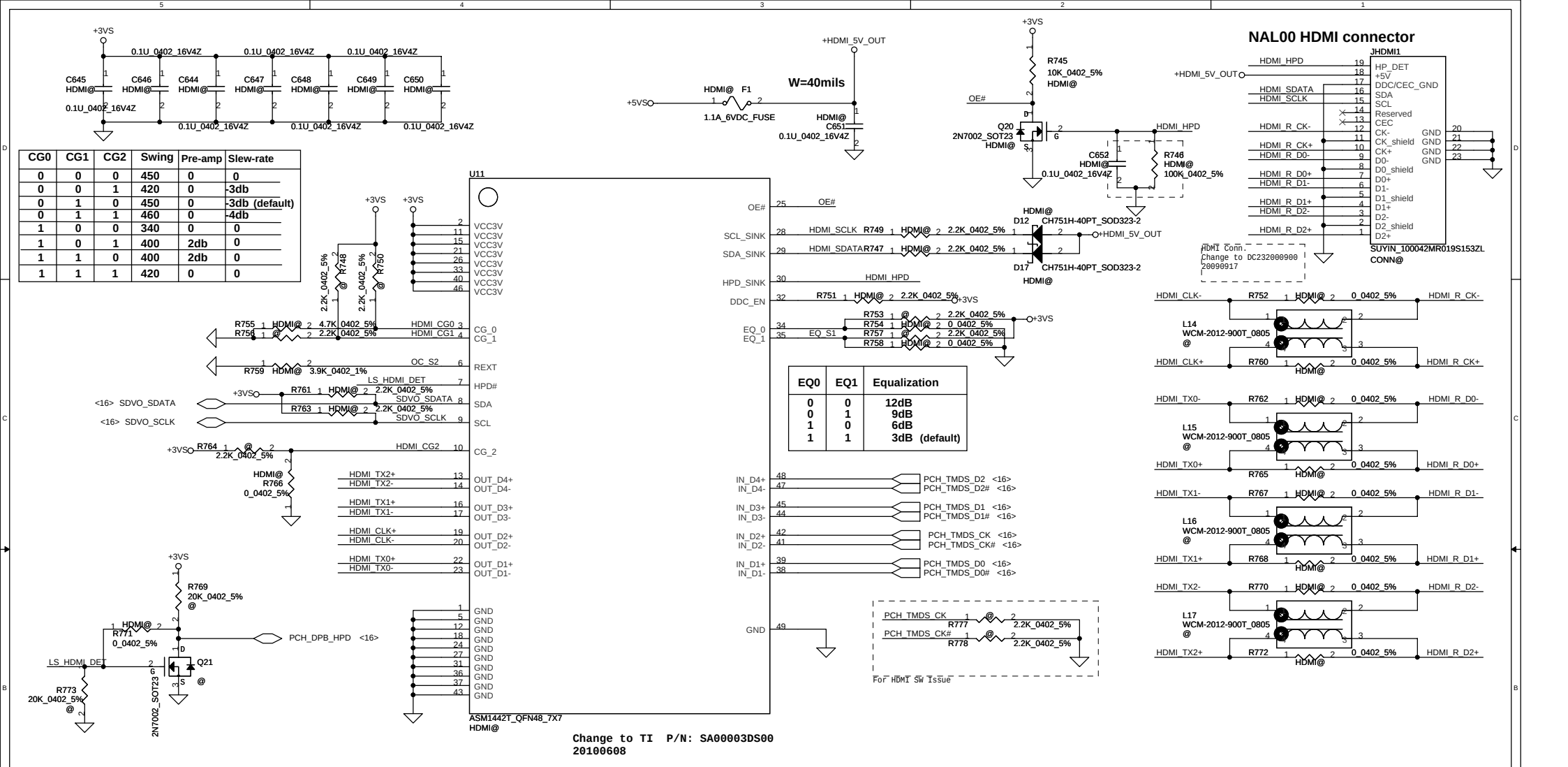

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

Change to TI P/N: SA00003DS00
20100608

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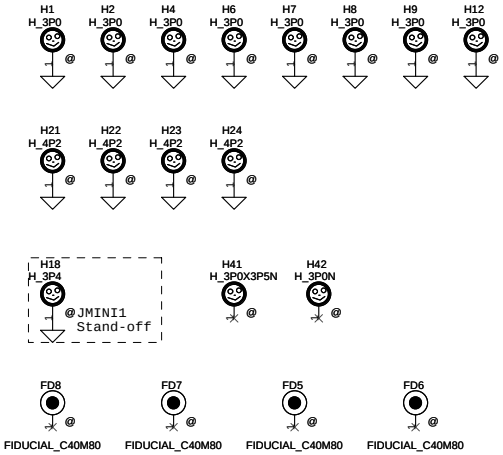
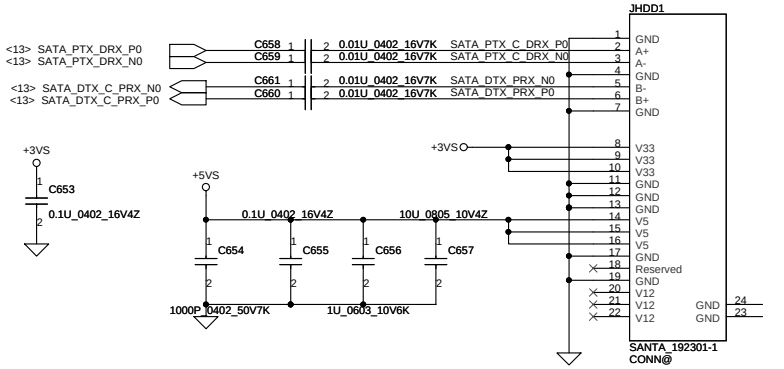


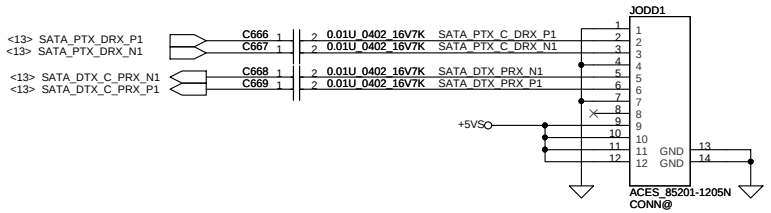
SATA HDD1 Conn.

CL 4.0 mm



20090915 Update to SANTA

SATA ODD FFC Conn.



Change to 12P conn. for FFC
20100413

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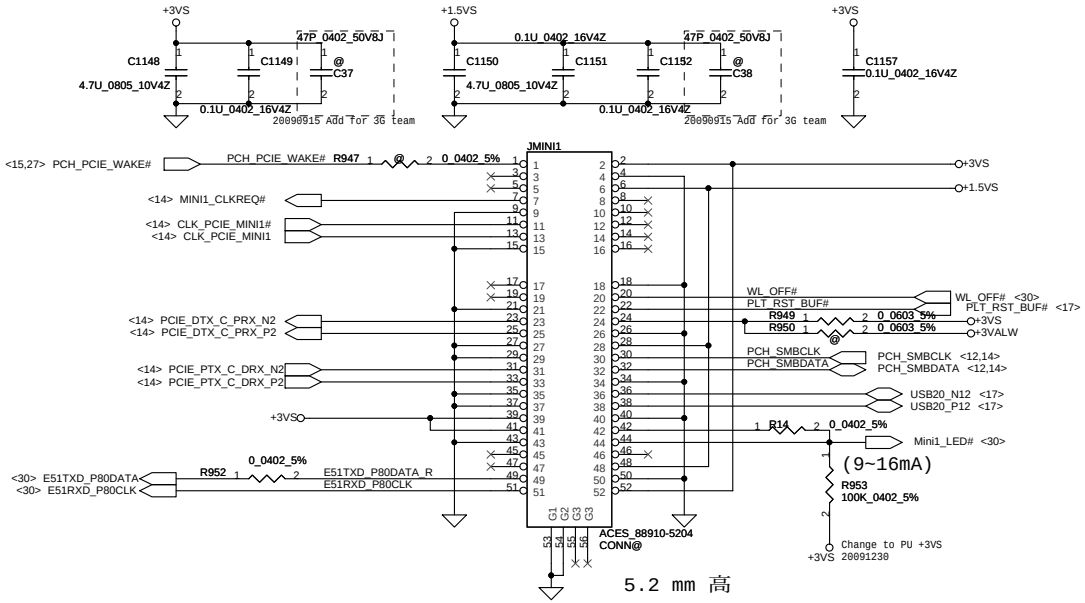
For Wireless LAN

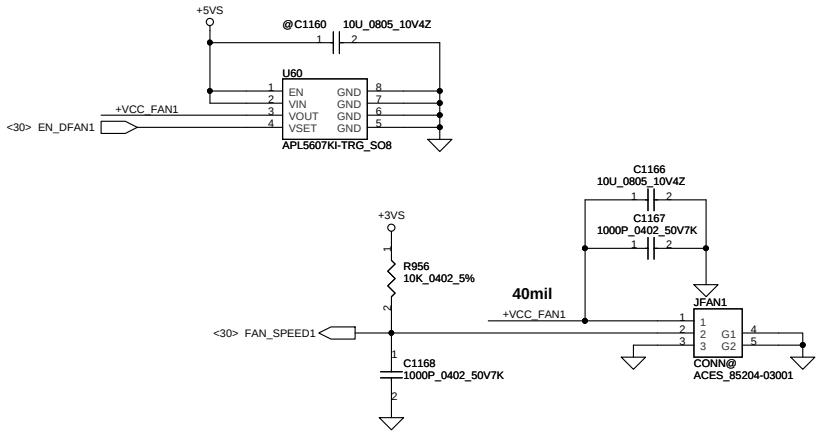


5.2 mm 高

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Del 3G / GPS Module Connect

FAN1 Conn



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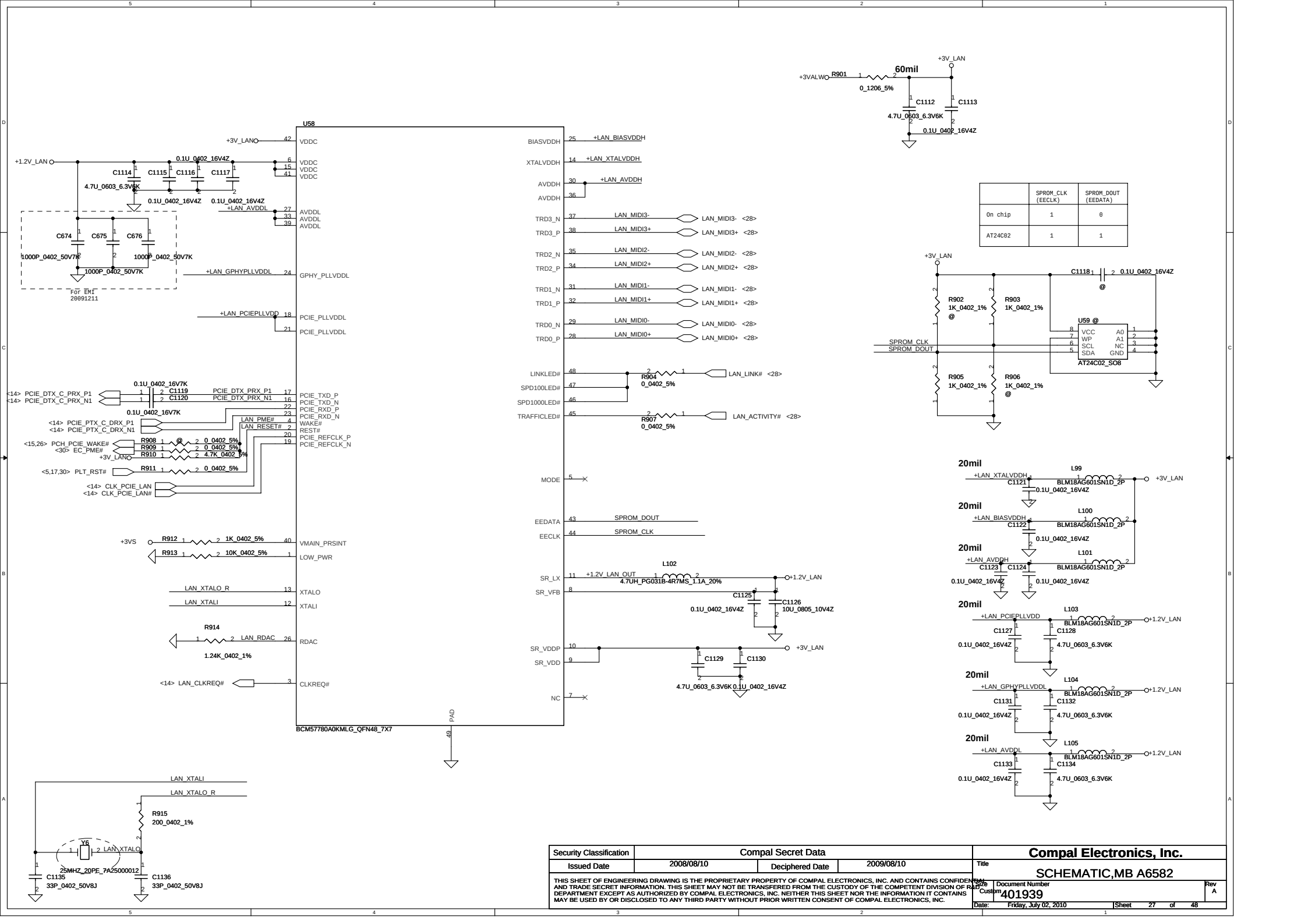

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

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Issued Date	2008/08/10	Deciphered Date	2009/08/10

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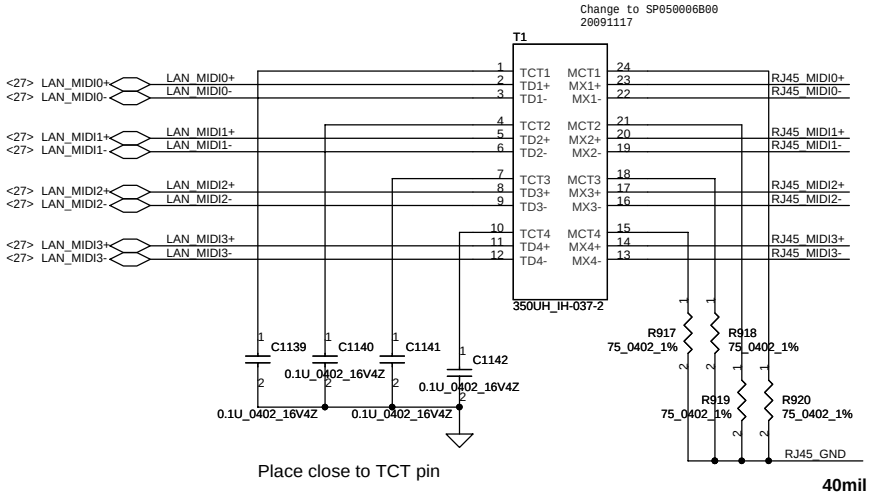
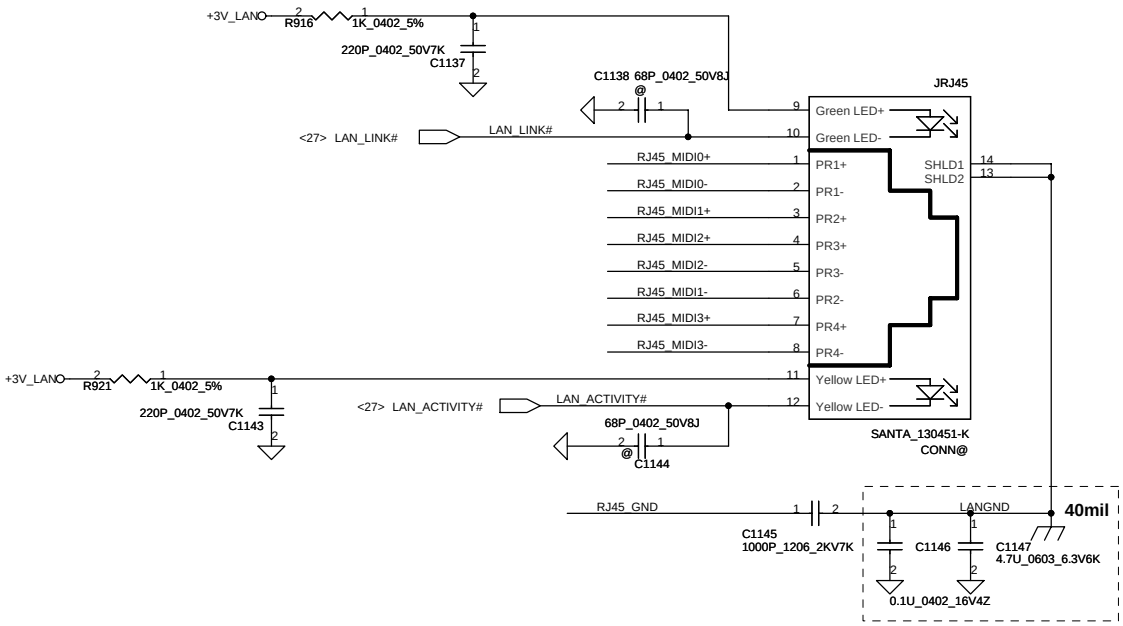
LAN Connector





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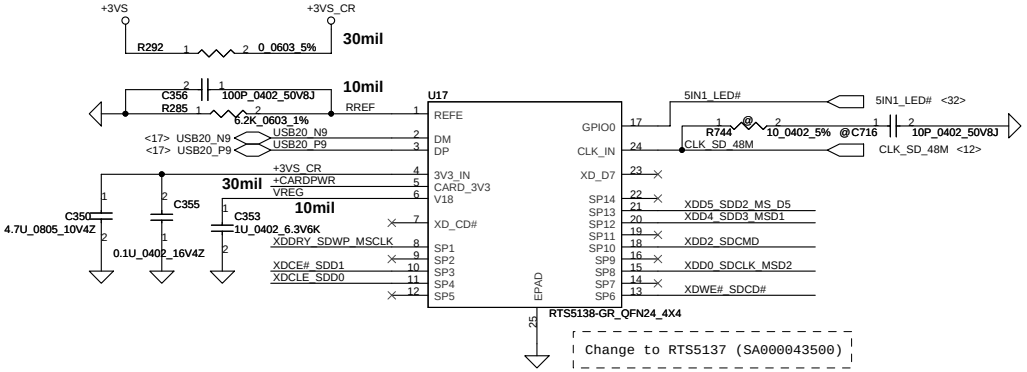
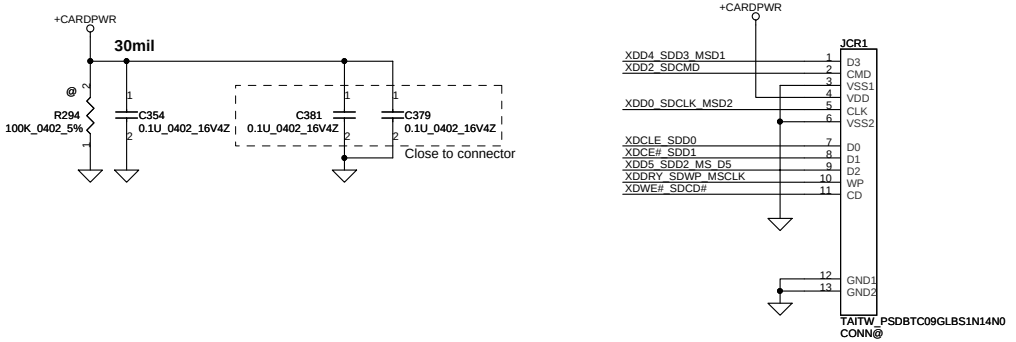
Card Reader RTS5138 / RTS5137
(only SD+MMC function)

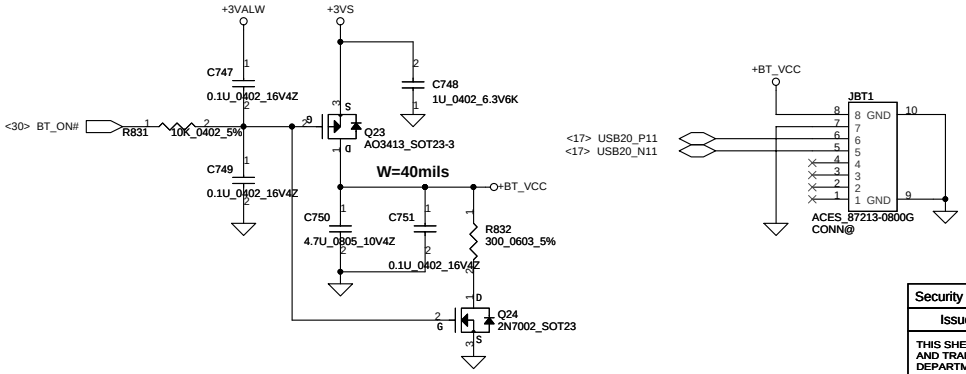


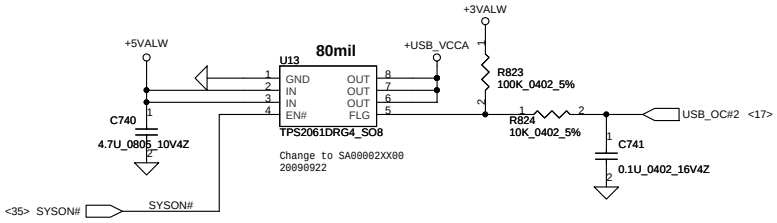
Card Reader Connector

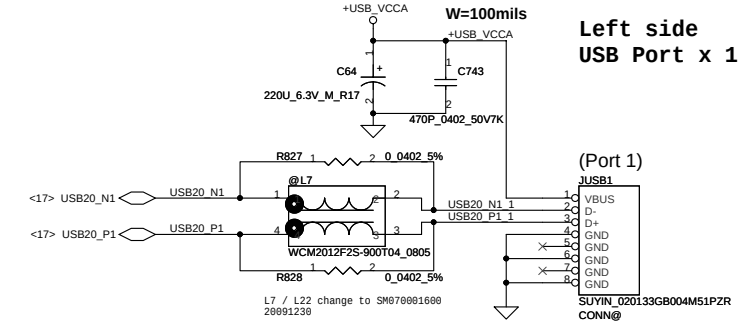


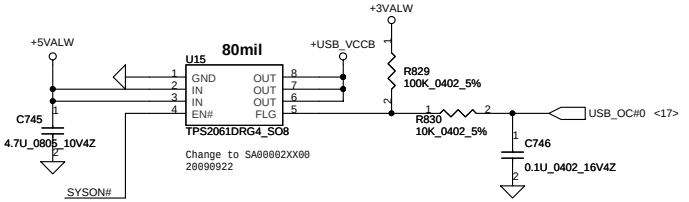
Bluetooth Conn.

Q23 change to SB934130020



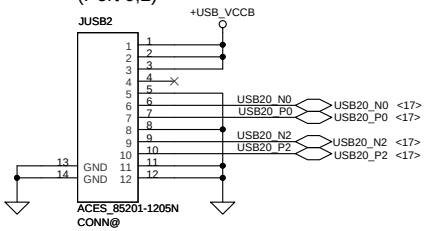






USB/B Conn.

(Port 0,2)



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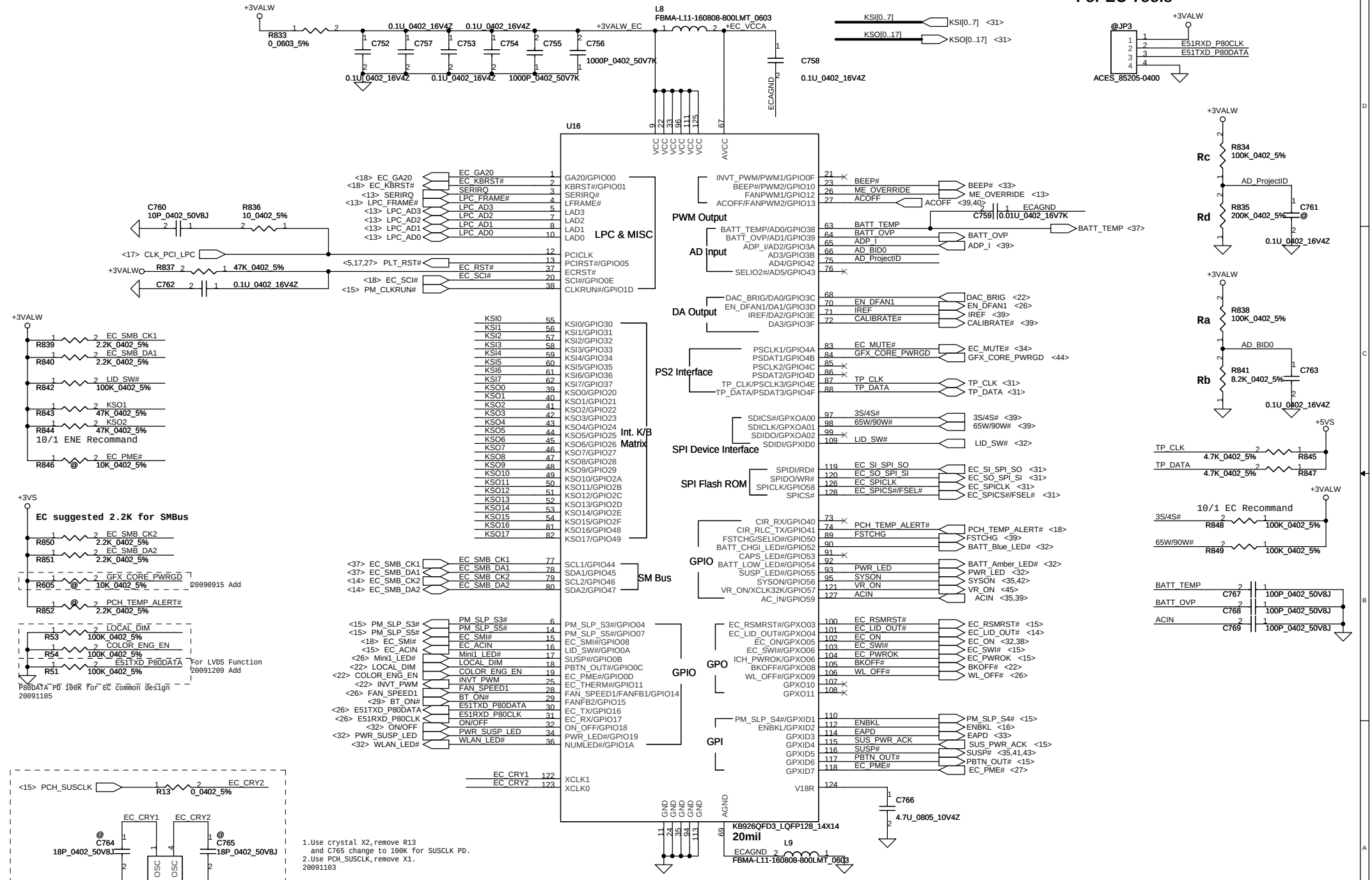
For EC Tools



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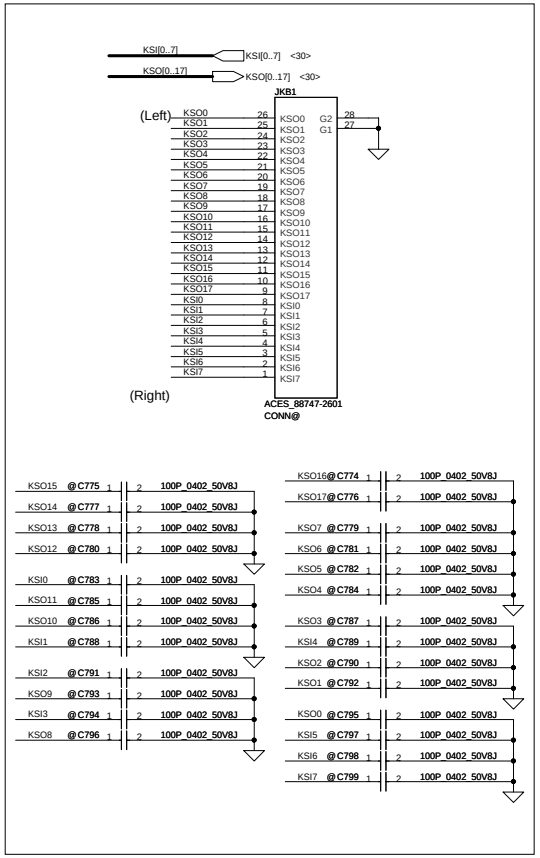

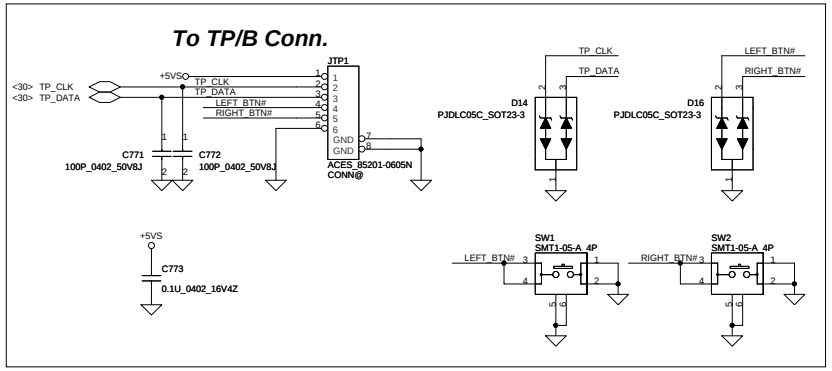

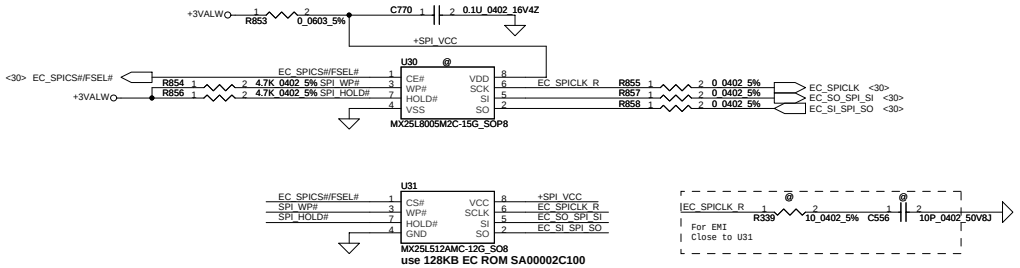

ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

To BTN/B Conn.

	KSO0	KSO3
KSI1	WL_BTN#	Program_BTN#
KSI2	T/P lock_BTN#	
KSI3	Back up_BTN#	Volum up_BTN#
KSI4	BT_BTN#	Volum down_BTN#
KSI5	Power save_BTN#	

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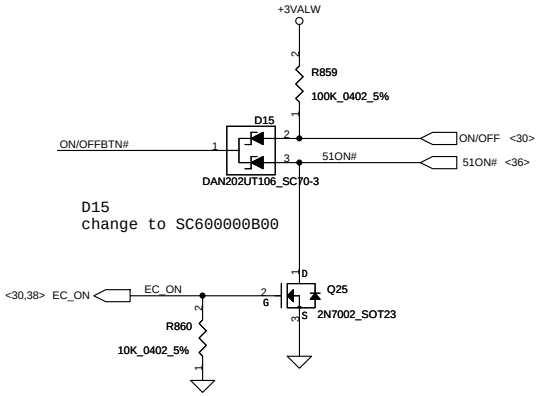
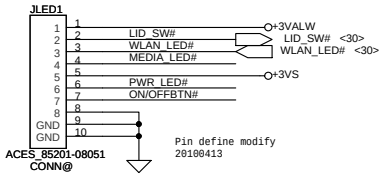
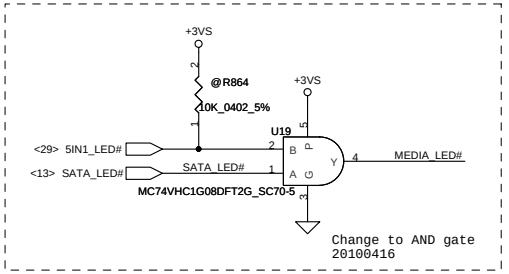
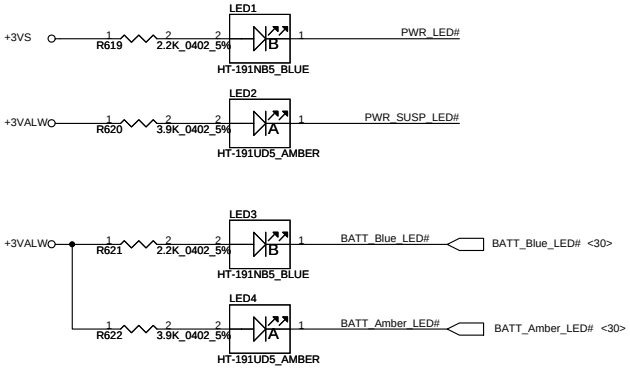
Power Button

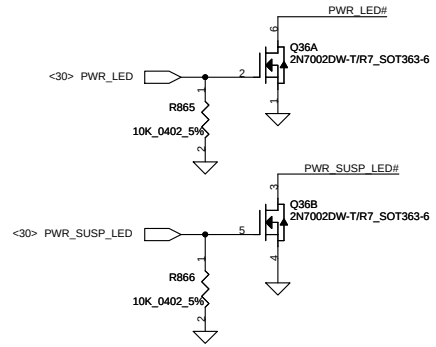


LED/B LEFT









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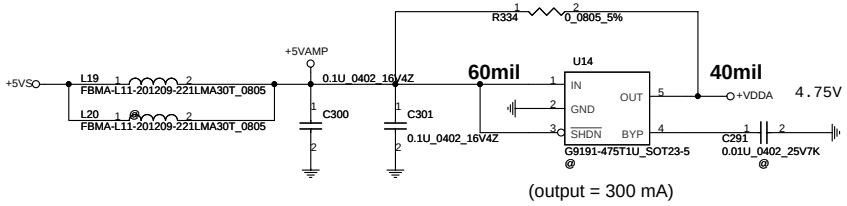
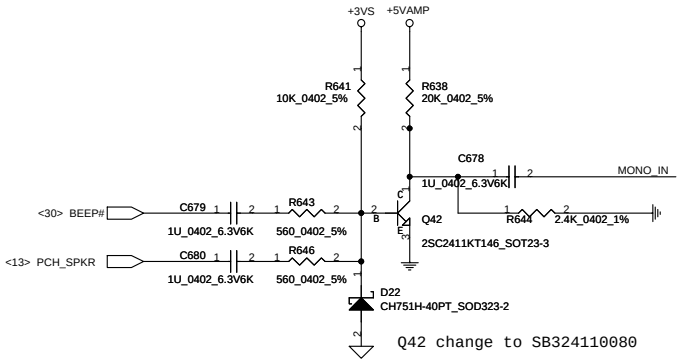
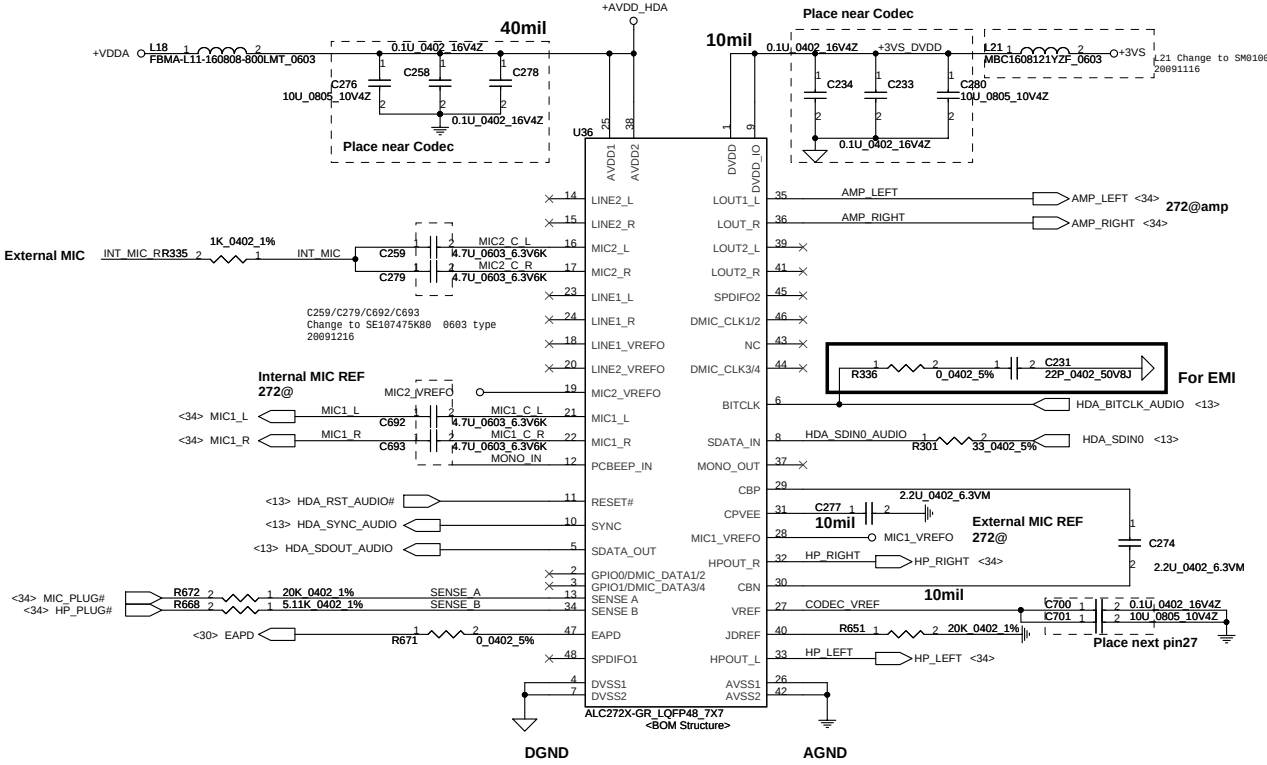


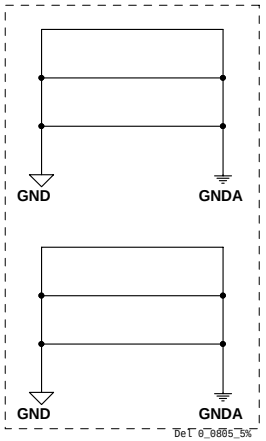
(output = 300 mA)

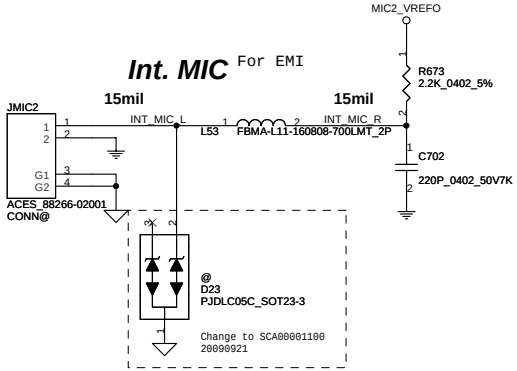


Q42 change to SB324110080

HD Audio Codec







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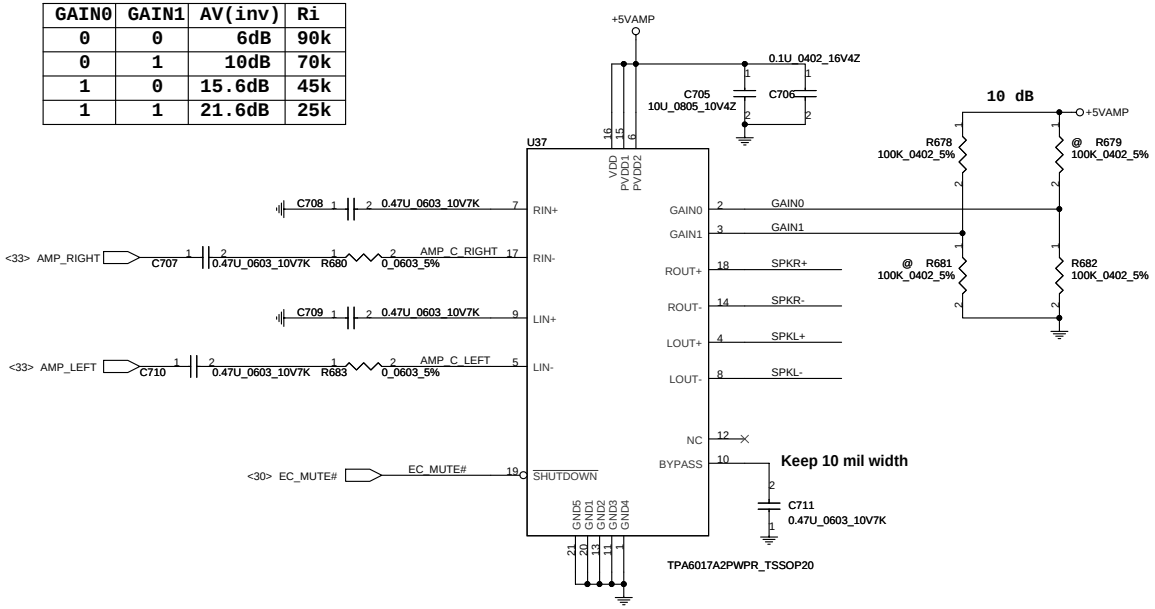
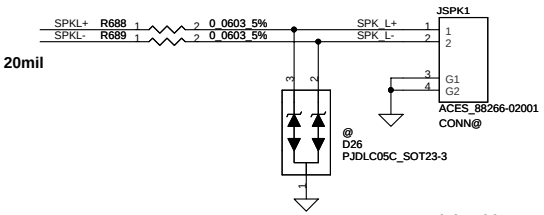
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

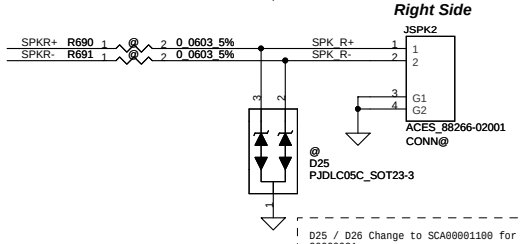


Int. Speaker Conn.

Left Side



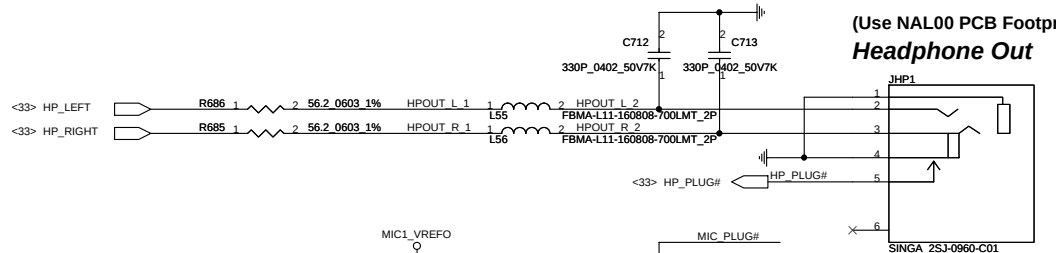
Right Side



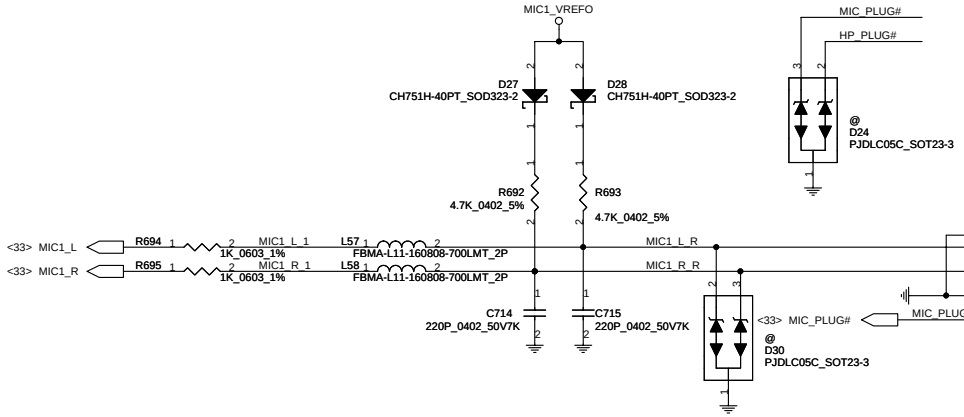
D25 / D26 Change to SCA00001100 for ESD 20090921

(Use NAL00 PCB Footprint)

Headphone Out



Headphone Out



MIC JACK

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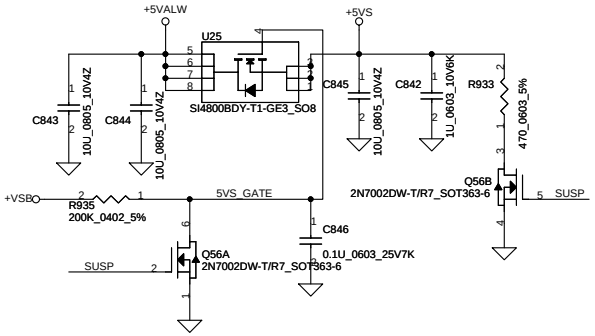
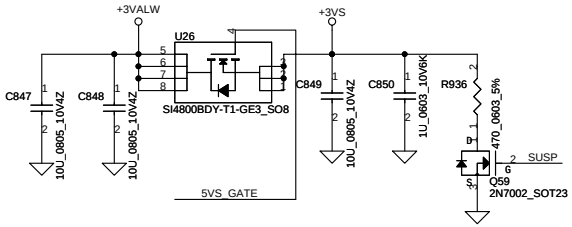
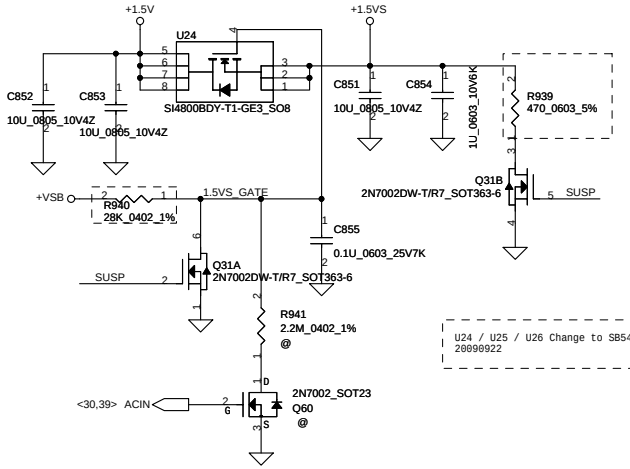
+5VALW TO +5VS



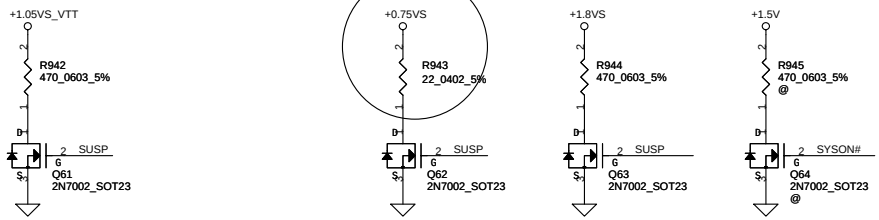
+3VALW TO +3VS

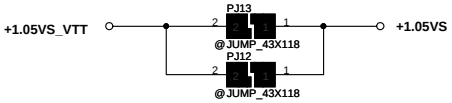


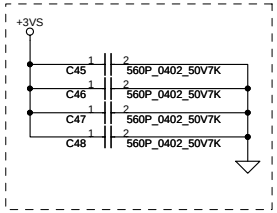
+1.5V to +1.5VS



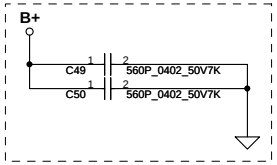
U24 / U25 / U26 Change to SB548000320
20090922



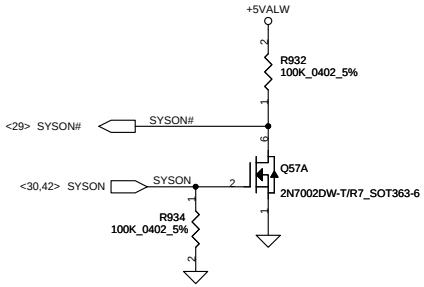


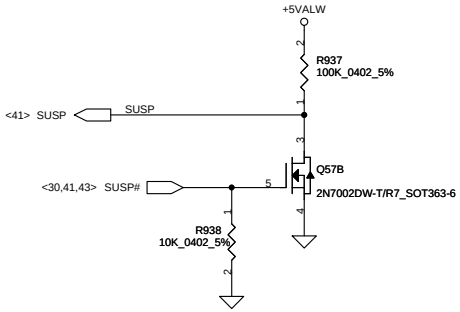


For LAM Common mode noise
200911102330



For EC B+
20100507





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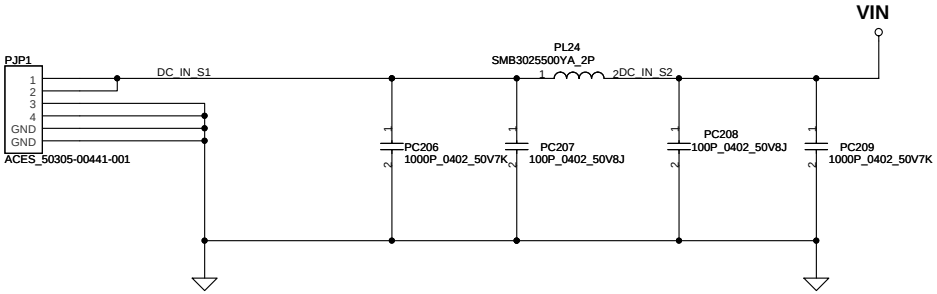

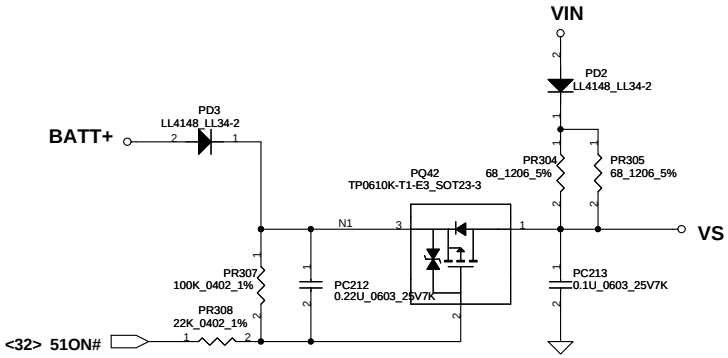

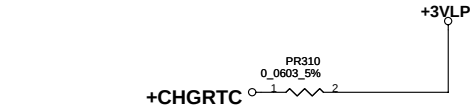

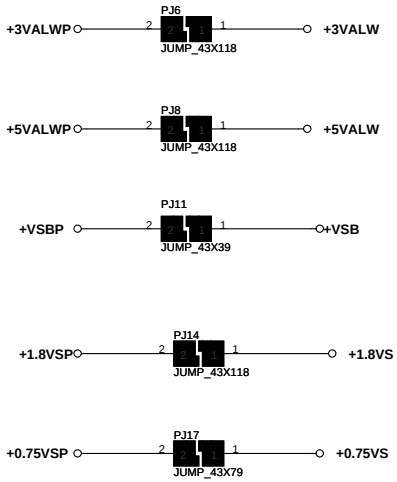

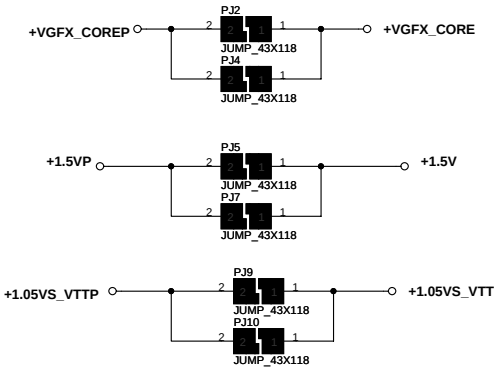

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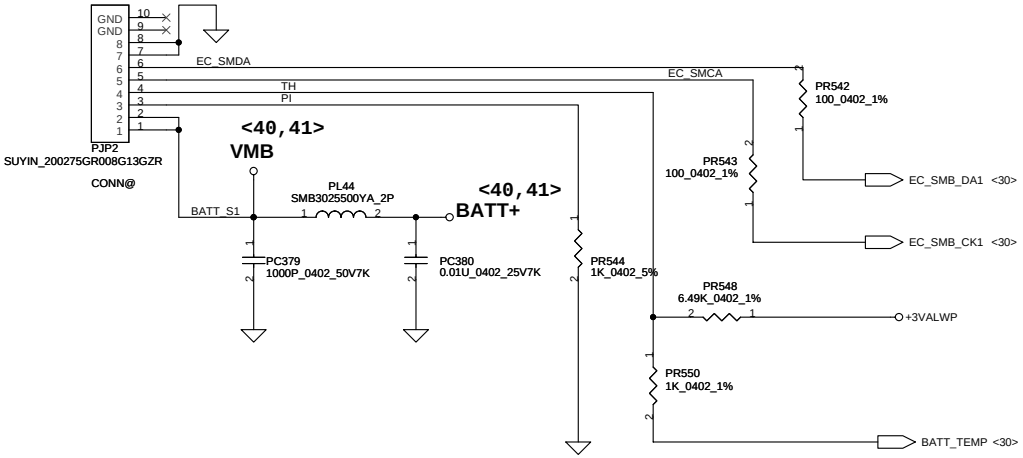
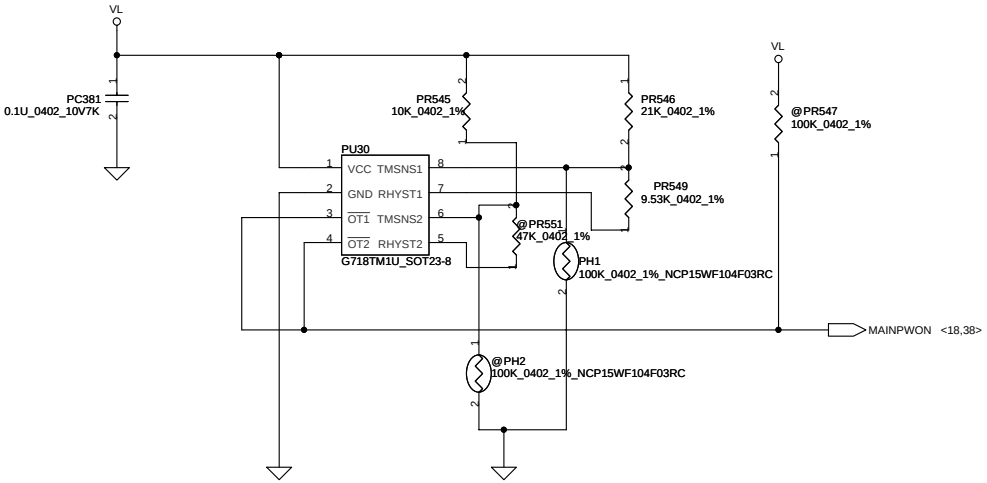
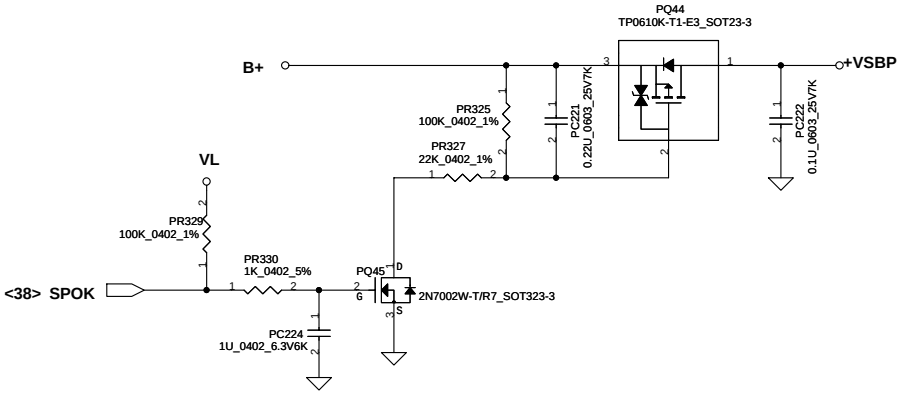


PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





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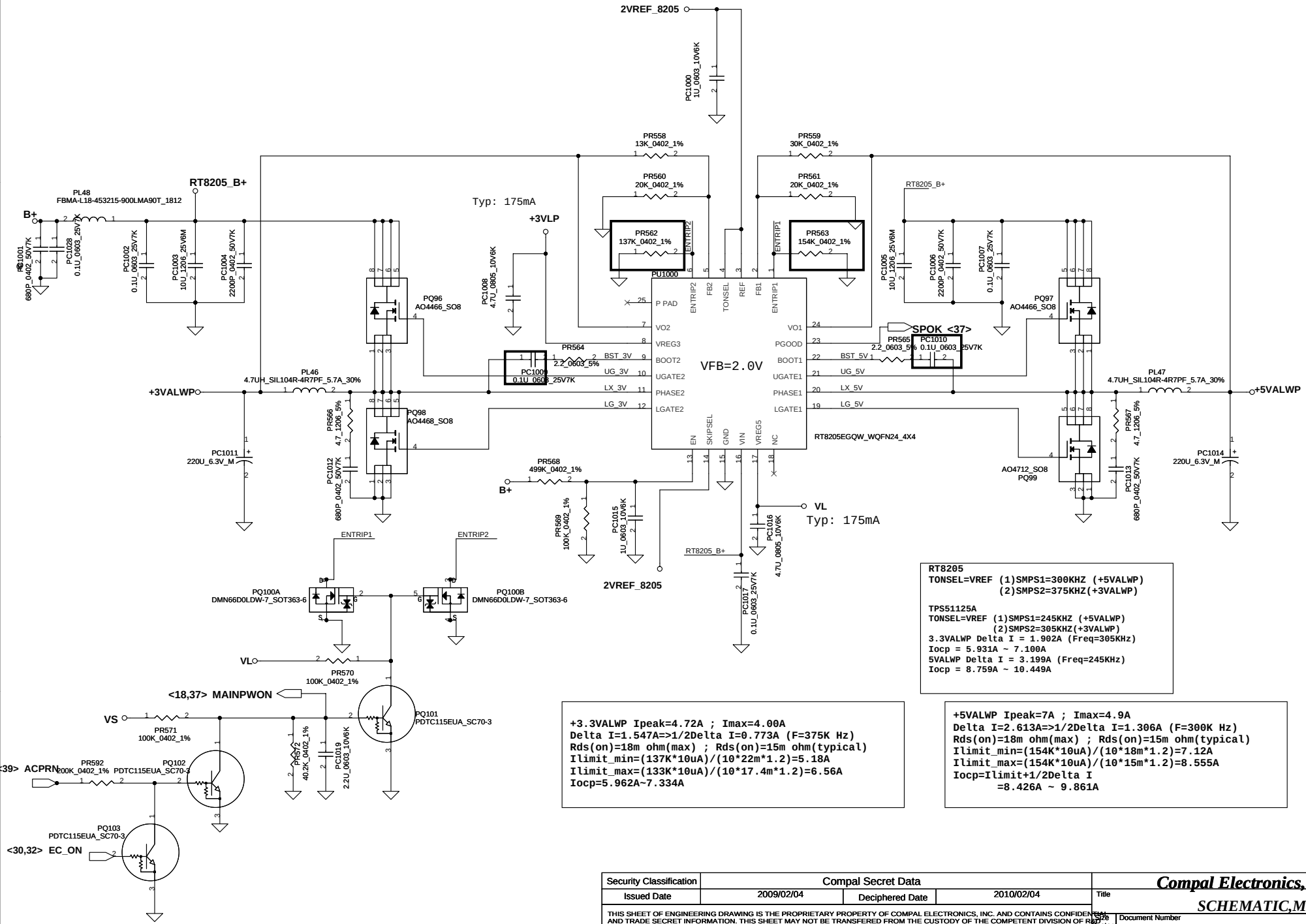
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)

TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
(2)SMPS2=305KHZ(+3VALWP)
3.3VALWP Delta I = 1.902A (Freq=305KHz)
Iocp = 5.931A ~ 7.100A
5VALWP Delta I = 3.199A (Freq=245KHz)
Iocp = 8.759A ~ 10.449A

+3.3VALWP Ipeak=4.72A ; Imax=4.00A
Delta I=1.547A=>1/2Delta I=0.773A (F=375K Hz)
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=(137K*10uA)/(10*22m*1.2)=5.18A
Ilimit_max=(133K*10uA)/(10*17.4m*1.2)=6.56A
Iocp=5.962A~7.334A

+5VALWP Ipeak=7A ; Imax=4.9A
Delta I=2.613A=>1/2Delta I=1.306A (F=300K Hz)
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=(154K*10uA)/(10*18m*1.2)=7.12A
Ilimit_max=(154K*10uA)/(10*15m*1.2)=8.555A
Iocp=Ilimit+1/2Delta I
=8.426A ~ 9.861A

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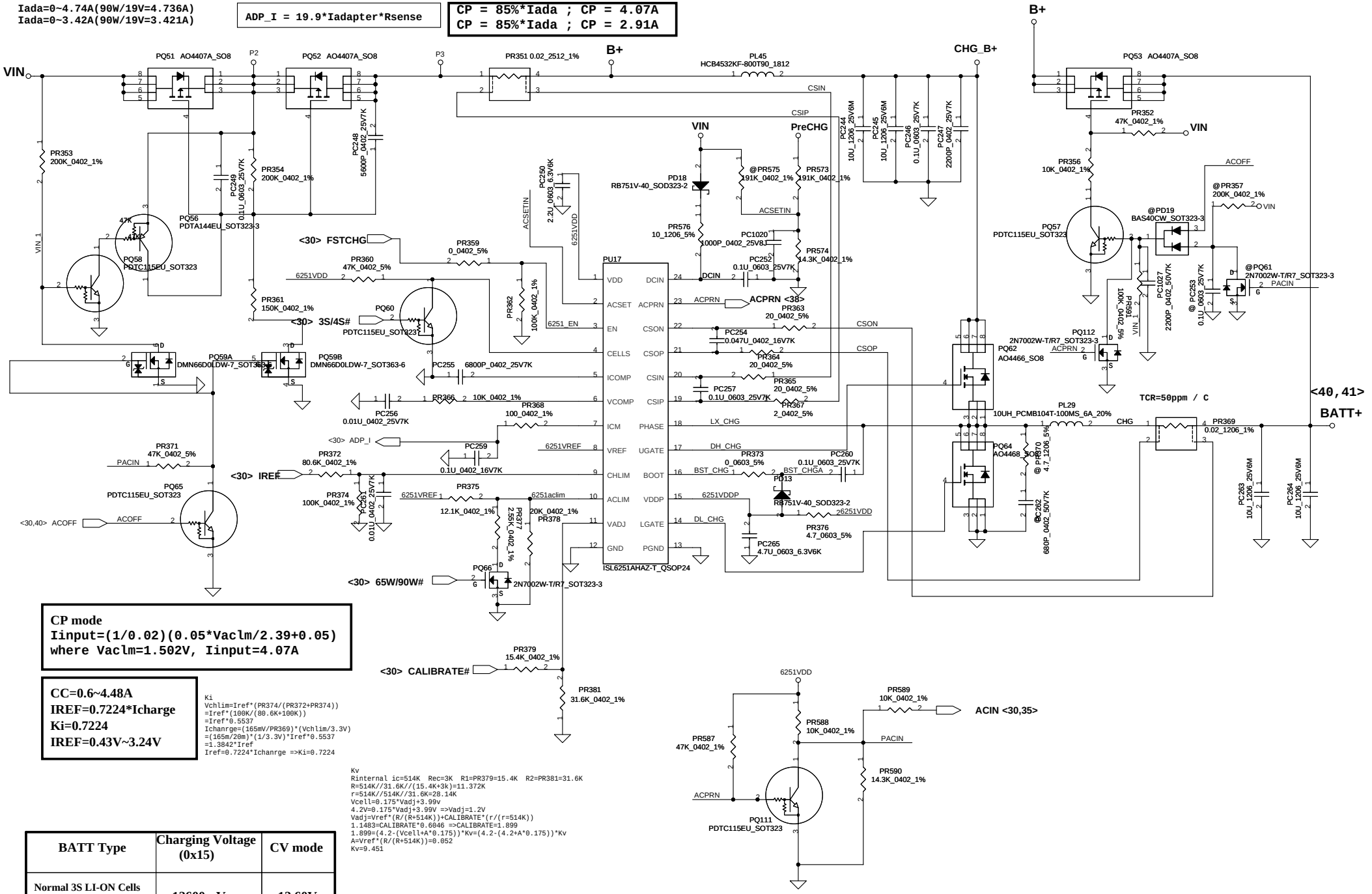
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A
IREF=0.7224*Icharge
Ki=0.7224
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

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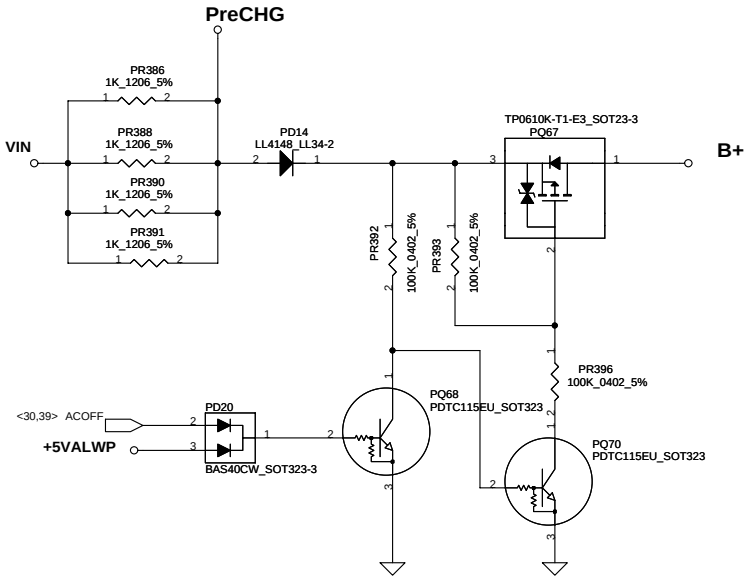

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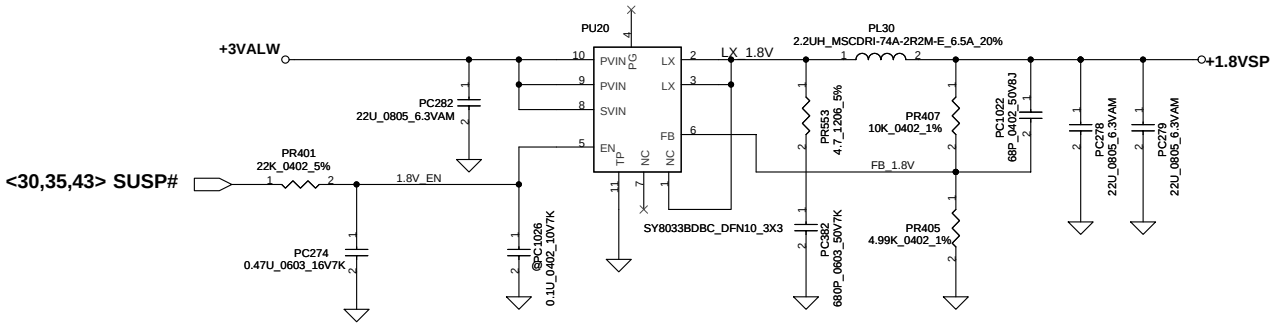
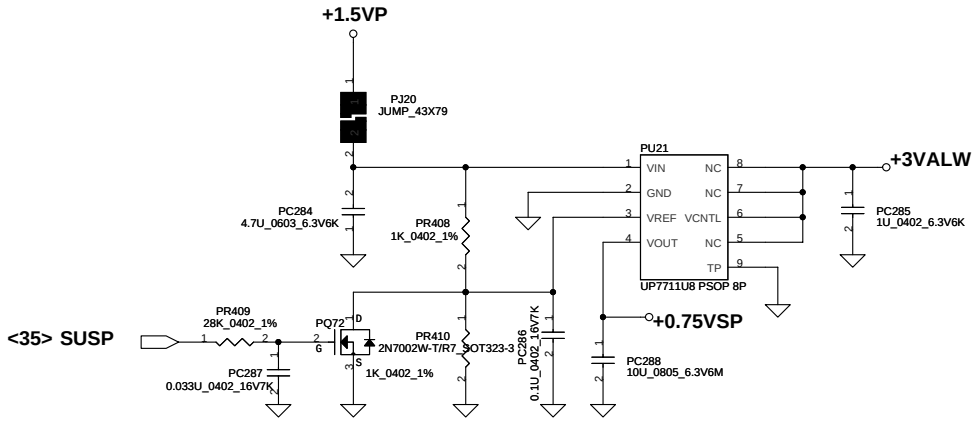
FB=0.6V
Note:Iload(max)=3.5A





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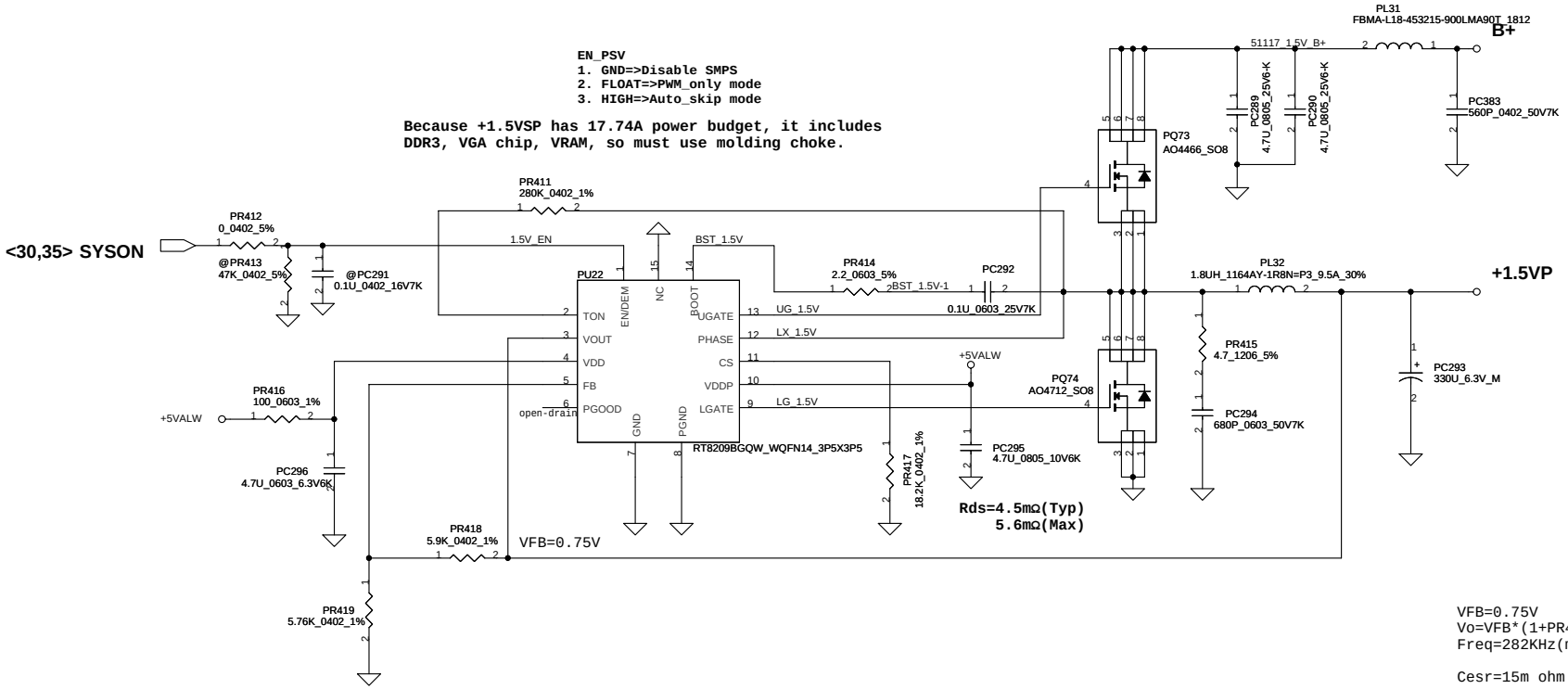

VFB=0.75V
Vo=VFB*(1+PR418/PR419)=1.52V
Freq=282KHz(min) , 300KHz(typ)

Cesr=15m ohm

Iocp=9.94A~13A

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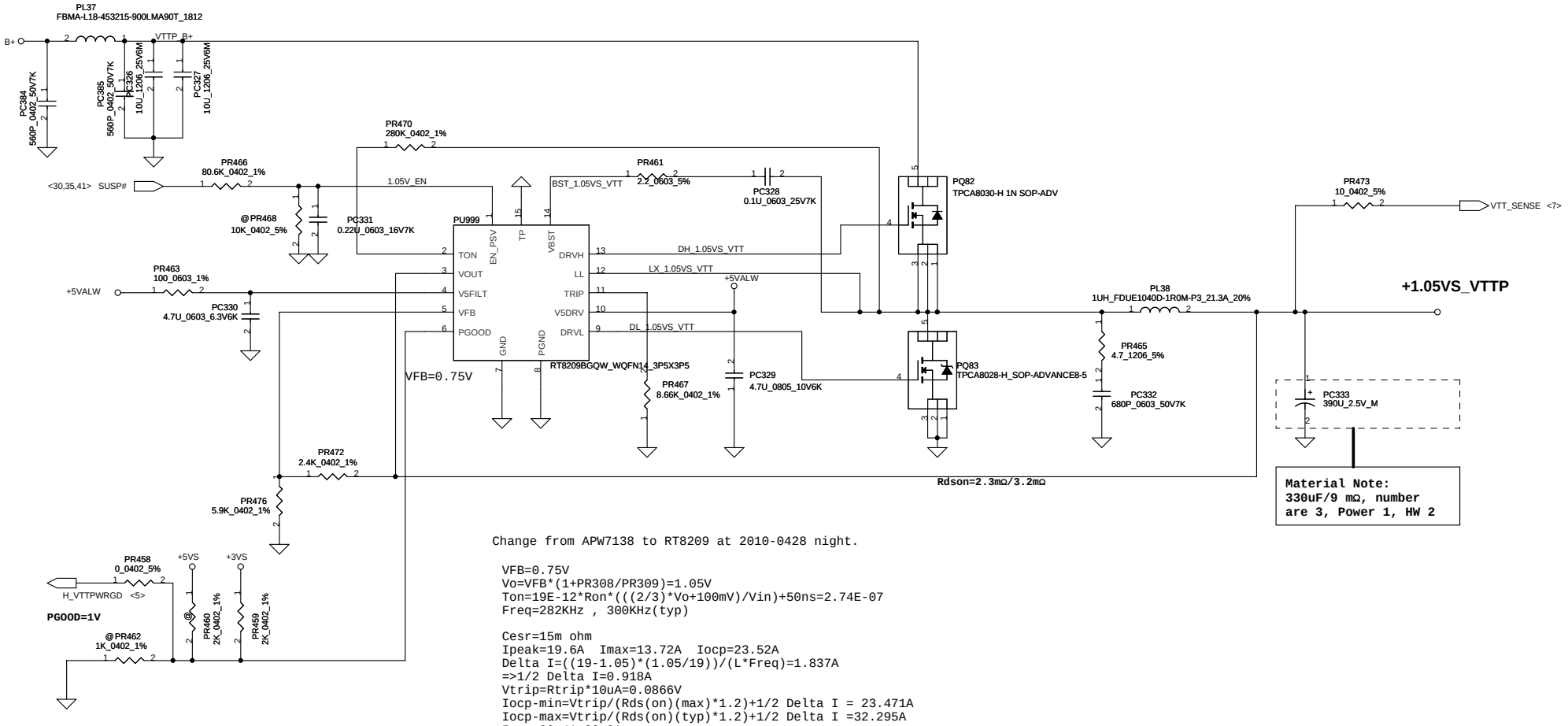

Change from APW7138 to RT8209 at 2010-0428 night.

VFB=0.75V
Vo=VFB*(1+PR308/PR309)=1.05V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/Vin)+50ns=2.74E-07
Freq=282KHz , 300KHz(typ)

Cesr=15m ohm
Ipeak=19.6A Imax=13.72A Iocp=23.52A
Delta I=((19-1.05)*(1.05/19))/(L*Freq)=1.837A
=>1/2 Delta I=0.918A
Vtrip=Rtrip*10uA=0.0866V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+1/2 Delta I = 23.471A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+1/2 Delta I =32.295A
Iocp=22.4A~30.8A

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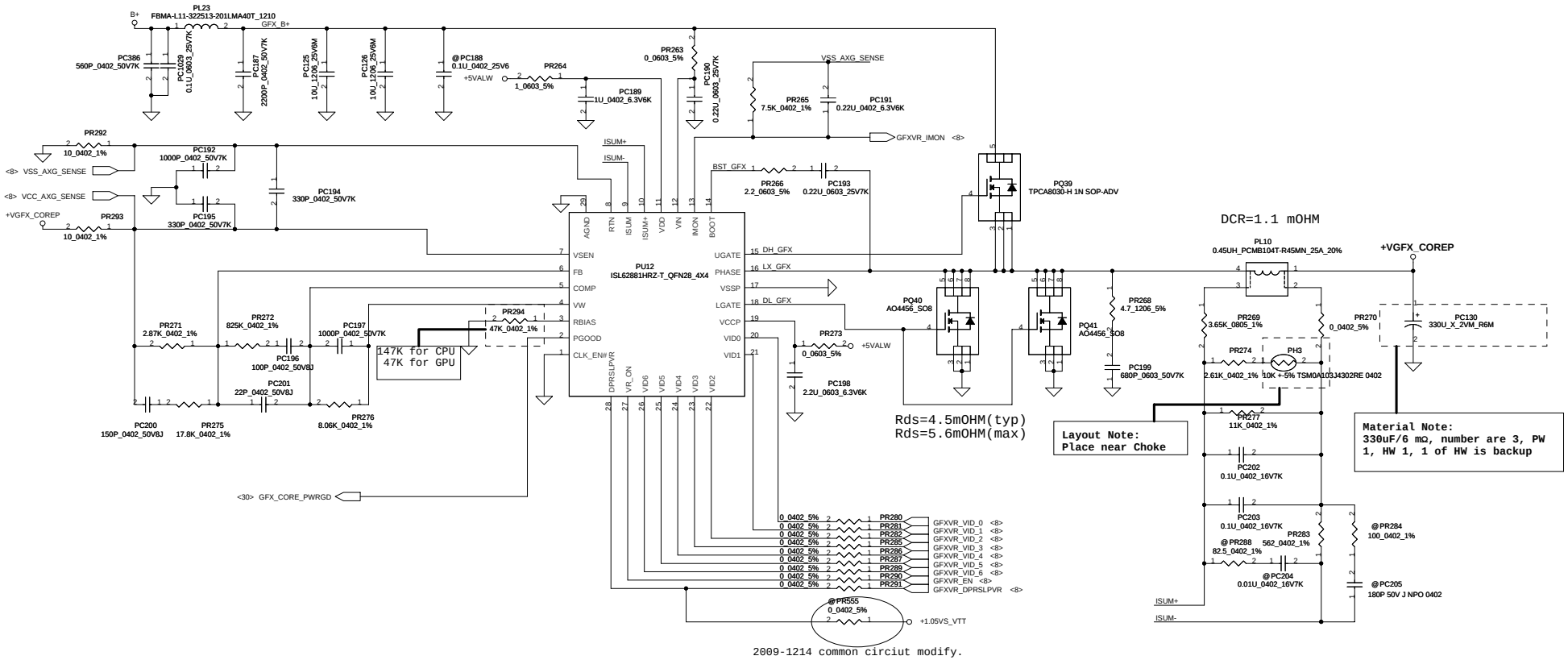
Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A



2009-1214 common circiut modify.

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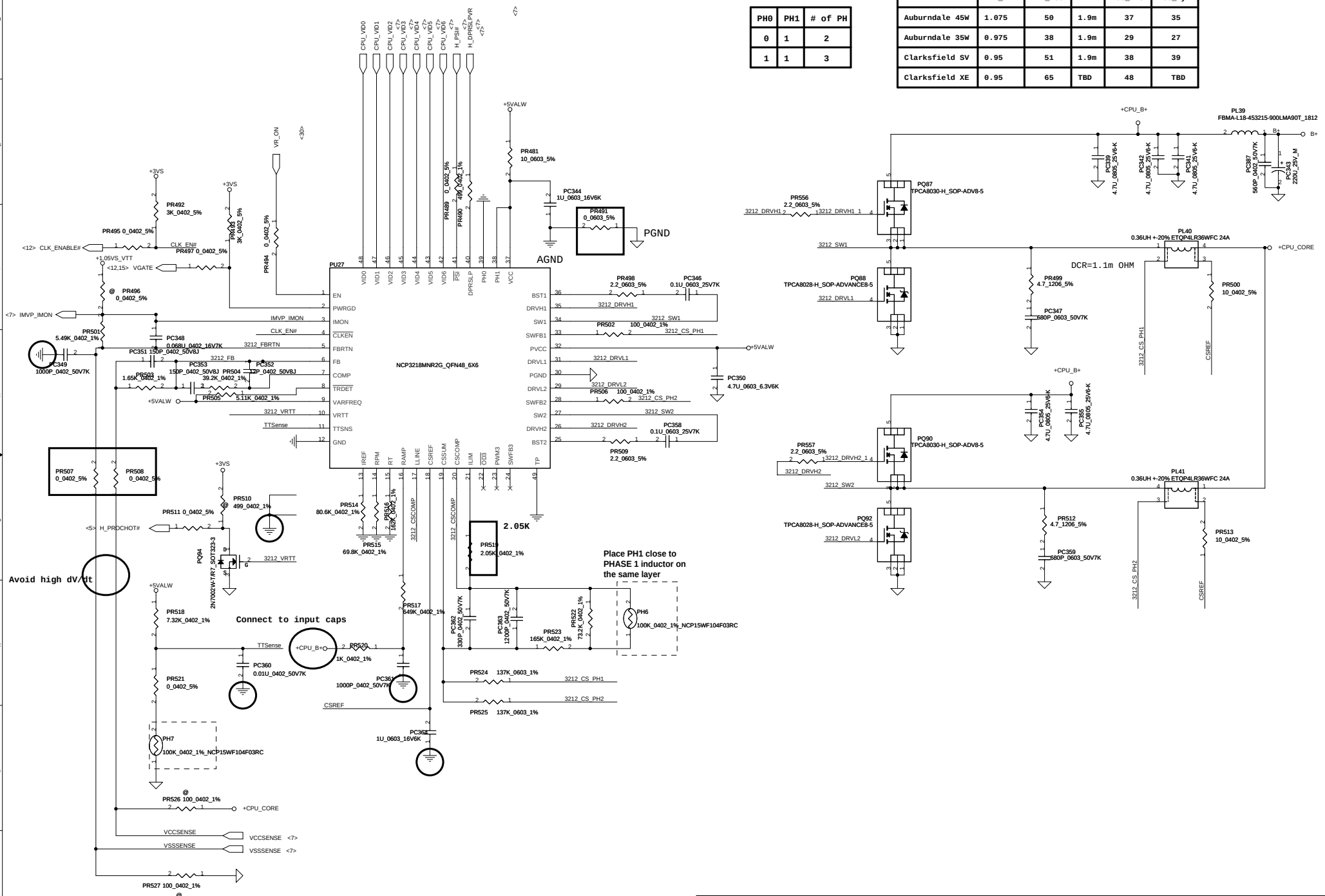
PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1 2 3	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	39	Change PR353 from SD034470280 to SD034200380. Change PR371 from SD034220280 to SD034470280. Change PR587 from SD034100380 to SD034470280. Change PR590 from SD034200280 to SD034143280. Change PR591 from SD028470280 to SD028100380. Add PC1027 SE074222K80(S CER CAP 2200P 0402 50V7K) Change PQ111 from SB000006800 to SB301150200	2010/06/08	to PVT
4	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	38	Add PQ102 and PQ103 SB301150200. Add PR592 SD034200380.	2010/06/08	to PVT
5 6	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	40	Change PR386 from SD011000080 to SD011100180. Add PR388, PR390, PR391 SD011100180. Add PD14 SC100001Y80 LL4148_LL34-2	2010/06/08	to PVT
7 8	EMI fail, add 3/5V snubber and Boost Resister to silve it.	EMI request to solve EMI issue.	0.1	38	Add PR566 and PR567 SD001470B80 S RES 4.7 1206 5% Add PC1012 and PC1013 SE074681K80 S CER CAP 680P 0402 50V7K Change PR564 and PR565 from SD013000080 to SD013220B80	2010/06/08	to PVT
	EMI fail, add 1.5V snubber.	EMI request to solve EMI issue.	0.1	42	Add PR415 SD001470B80 4.7 1206 5%. Add PC294 SE025681K80 S CER CAP 680P 50V K X7R 0603	2010/06/08	to PVT
9 10	EMI fail, add 1.05V snubber. and Boost Resister.	EMI request to solve EMI issue.	0.1	43	Add PR465 SD001470B80 4.7 1206 5%. Add PC332 SE025681K80 S CER CAP 680P 50V K X7R 0603 Change PR461 from SD013000080 to SD013220B80	2010/06/08	to PVT
11	EMI fail, add GFX_CORE snubber.	EMI request to solve EMI issue.	0.1	44	Add PR268 SD001470B80 4.7 1206 5%. Add PC199 SE025681K80 S CER CAP 680P 50V K X7R 0603	2010/06/08	to PVT
12 13	HW power sequence modify.	HW request.	0.1	43	Change PR466 from SD034576280 S RES 1/16W 57.6K +-1% 0402 to SD034806280 S RES 80.6K 0402 1%) Change PC331 from SE076104K80 S CER CAP .1U 16V K X7R to SE00000R700 S CER CAP 0.22U 16V K X7R 0402	2010/06/08	to PVT
14	BOM unique.	BOM unique.	0.1	38	Chnage PQ101 from SB301150000 to SB301150200.	2010/06/08	to PVT
15	EMI request.	EMI request.	0.1	38	Add PC1028 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
16	EMI request.	EMI request.	0.1	44	Add PC1029 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
17	Sourcer request to change a common part.	Sourcer request.	0.1	38	Change PC1019 from SE00000GC00 S CER CAP 2.2U 10V K X7R 0603 to SE000003H00 S CER CAP 2.2UF 10V K X5R 0603	2010/06/08	to PVT
18	Per sourcer request.	Sourcer request to change PC331 from SE00000R700 to SE026224K80 for common part.	0.1	43	change PC331 from SE00000R700 to SE026224K80	2010/06/08	to PVT
19	CPU transient issue.	Need modify PC362 to 330P due to transient fail.	0.1	45	Change PC362 from SE074561K80 S CER CAP 560P 50V K X7R 0402 to SE074331K80 S CER CAP 330P 50V K X7R 0402	2010/06/08	to PVT
20	Per sourcer request.	Per sourcer request.	0.1	43 44	Chnage PQ39/PQ82 from SB000008L80 to SB00000HL00.	2010/06/08	to PVT
21	Cost down.	Cost down 3VALWP and Charger Low Side MOS.	0.1	38 39	Change PQ98 from SB00000AJ00 to SB000009580(AO4468). Change PQ64 from SB00000CG00 to SB000009580(AO4468).	2010/06/08	to PVT
22	Cost down.	Cost down +1.5VP Low side MOS and choke.	0.1	42	Chnage PQ74 from SB000009F80 to SB00000AJ00(AO4712). CHnage PL32 from SH000009U00 to SH000009680.	2010/06/08	to PVT
23	Cost down.	re-caculate 1.5VP OCP.	0.1	42	Change PR417 from SD034110280 to SD034182280.	2010/06/08	to PVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Cost down.	re-caculate +3VALWP OCP.	0.1	38	Change PR562 from SD034107380 to SD034137380.	2010/06/08	to PVT
25							
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Issued Date	2007/09/20	Deciphered Date	2008/09/20

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Version change list (P.I.R. List)

Item	Phase	PAGE	DATE	Modifycatio list	Purpose
1	EVT		04 / 08	N/A	
			04 / 16	Modify RTC SCH Change LAN to AR8152 Update Power SCH	
			04 / 21	Update AND Gate symbol - U1 / U2 / U6 / U7 / U19 Update Power MOS symbol - U24 / U25 / U26 C196 change to 1U for INTEL disign CLK GEN del C35 / C36 / C30 / C31 / C32 / C33 / C34 / L3 (for 3G@ and @ function) Q4+Q6 change to 2N7002DW Update U8 symbol Add DMIC function Modify USB define.	
			04 / 26	Update Power SCH	
			04 / 27	Add R17 for DMIC power	
			04 / 29	Update Power SCH Change LAN to GIGA&10/100 co-lay Del R307 (LVDS conn.) Change +1.05VS_VTT to +1.05VS (CLK GEN) Change C842 / C850 / C854 / C656 to SE080105K80 1U_0603_10V6K Change R940 to 28K (S3 Power sequence)	
			04 / 29	SW T1 pin define (LAN)	
			05 / 03	Change R907 (0_0603) to 0_1206 5% Remove C40 / C41 / C42 / C43 / C44 Change FAN Conn.	
			05 / 03	Update Power SCH Change LAN to BCM57780 GIGA	
			05 / 06	Del R637 / R639 / R640 / R645 / R647 / R648 (AUDIO) Del DMIC Update Power SCH	
			05 / 07	Update Power SCH Add C49 / C50 (EC B+)	
			05 / 10	Update Power SCH	
			05 / 11	C764 / C765 change to 18P_0402_50V8J (EC) Reserve D13 / D24 / D30 (ESD)	
			05 / 12	U17 change to RTS5137 (SA000043500) Card reader	
			05 / 13	Update Power SCH	
			06 / 01	Unpop L11 / C247 & Pop R304 for cost down Unpop C764 / X2 & Pop R13 & C765 Change to 100K for EC remove Crystal Pop R834 & R835 change to 200K for Project ID	
			06 / 02	Unpop D24 / D30 Unpop R690 / R691 Pop C49 / C50 For HDMI Unpop R753 / R757 , Add R754 / R758 to 0 ohm. Change R759 to 3.9K. Change R755 to 4.7K ohm , Unpop R748. Unpop R778. R833 / R292 0_0805 change to 0_0603.	
			06 / 03	C190 / C191 & C1135 / C1136 change to 33P 0402 50V8J for Vender test report	
			06 / 04	Unpop C774~C799 for EMI cost down. Update Power SCH	
			06 / 10	Add T25 / T26 / T27	

Security Classification	Compal Secret Data		
Issued Date	2008/07/01	Deciphered Date	2009/12/31

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