

Compal Confidential

PEW71_81_91 UMA <LA-6582P> M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

2010-07-08

REV:1.0

<http://shop36609371.taobao.com/>
QQ:52643956

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				Custom	PEW71 M/B LA-6582P Schematic	1.0
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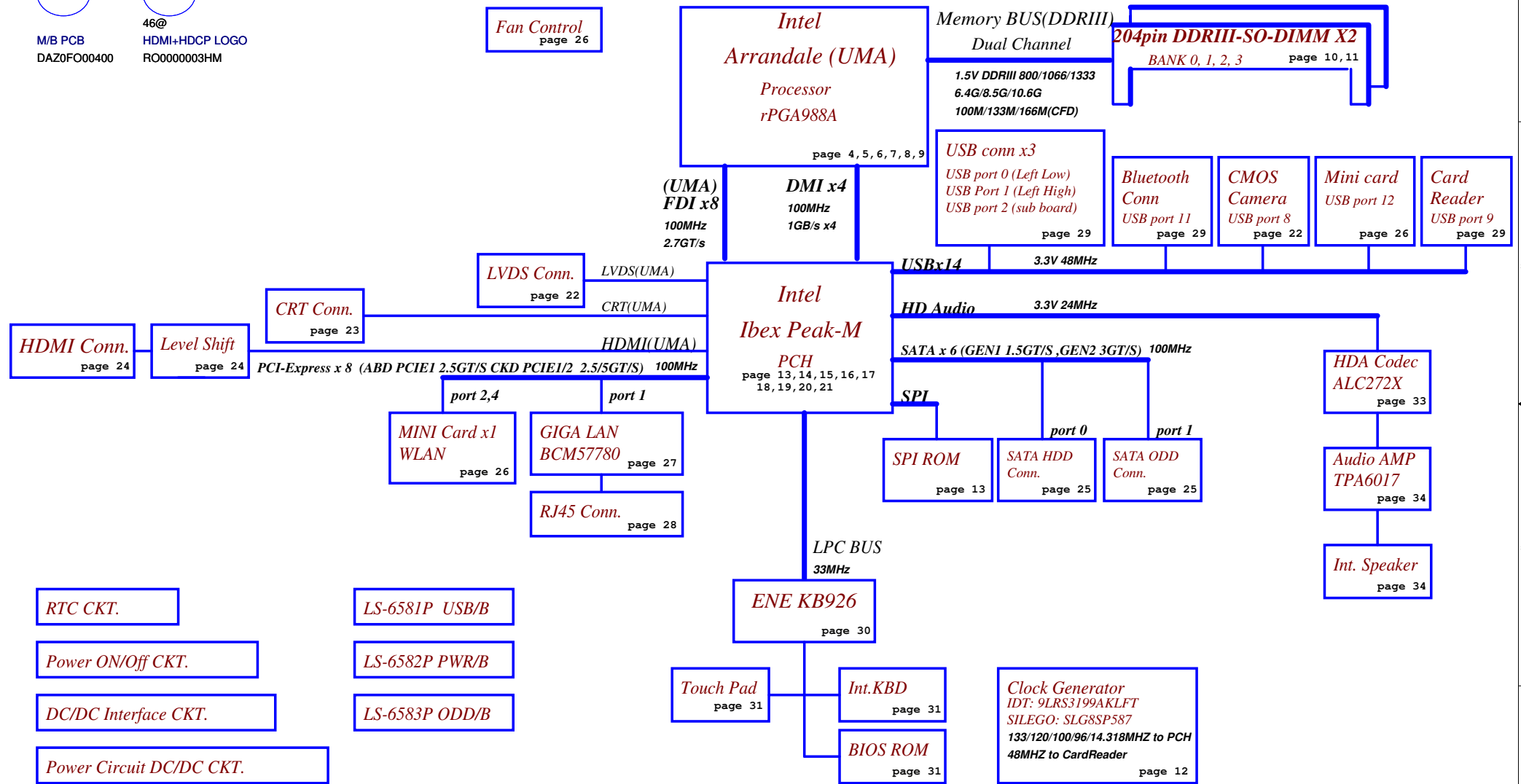
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Model Name PEW71_81_91 UMA

File Name : LA-6582P

ZZZ1
M/B PCB
DAZ0FO00400

ZZZ2
46@
HDMI+HDCP LOGO
RC0000003HM



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								Size B	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.05VS_VTT	1.05V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Project ID / Board ID Table for EC-AD channel

Vcc	3.3V +/- 5%					
Ra/Rc	100K +/- 5%					
	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max	Board ID	Project ID
0	0	0 V	0 V	0 V	0.1	Original NEW70/80/90/50/71/91
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2	PEW71/81/91 Audio Mono/Crystal
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	0.3	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	1.0	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V		
5	100K +/- 5%	1.453 V	1.650 V	1.759 V		
6	200K +/- 5%	1.935 V	2.200 V	2.341 V		PEW71/81/91 Audio Mono/SUSCLR
7	NC	2.500 V	3.300 V	3.300 V		NEW71/91 Optumis

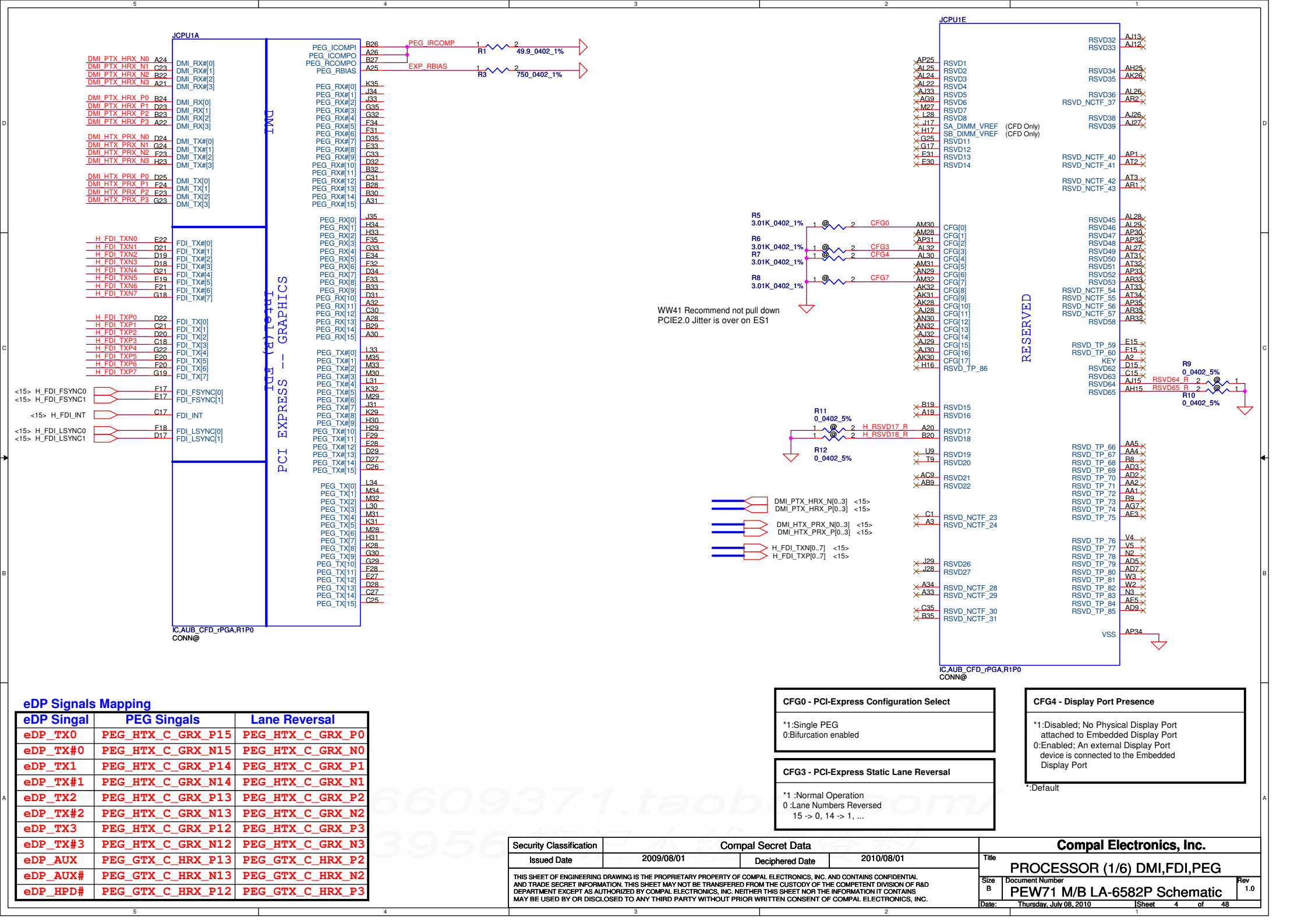
BTO Option Table

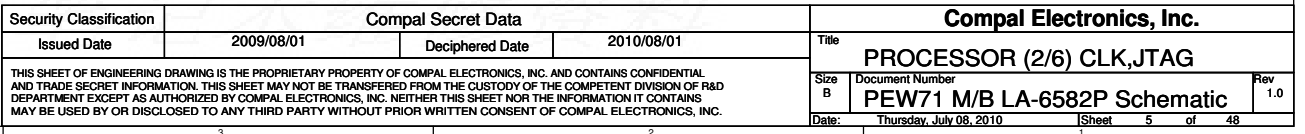
BTO Item	BOM Structure
HDMI	HDMI@

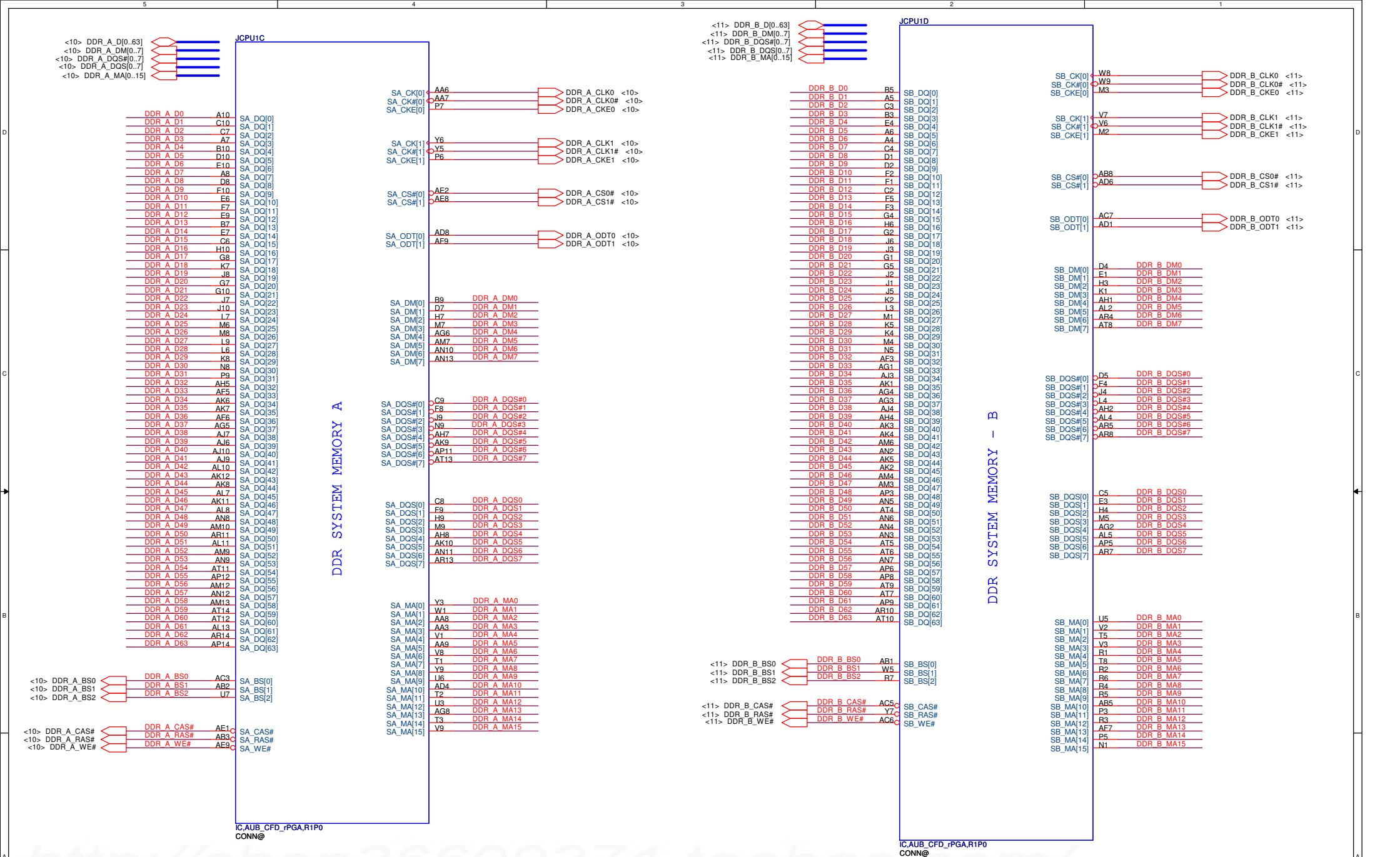
USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port
EHCI1	UHCI0	0	Ext1 Left Low USB	Ext1 Left Low USB
		1	Ext2 Left High USB	Ext2 Left High USB
		2	Ext3 Right USB	Ext3 Right USB
	UHCI1	3		
		4		
		5		
EHCI2	UHCI2	6		
		7		
	UHCI3	8	Camera	Camera
		9	Card Reader	Card Reader
		10		
	UHCI4	11	Blue Tooth	Blue Tooth
		12	1st Min-Card	1st Min-Card
		13		

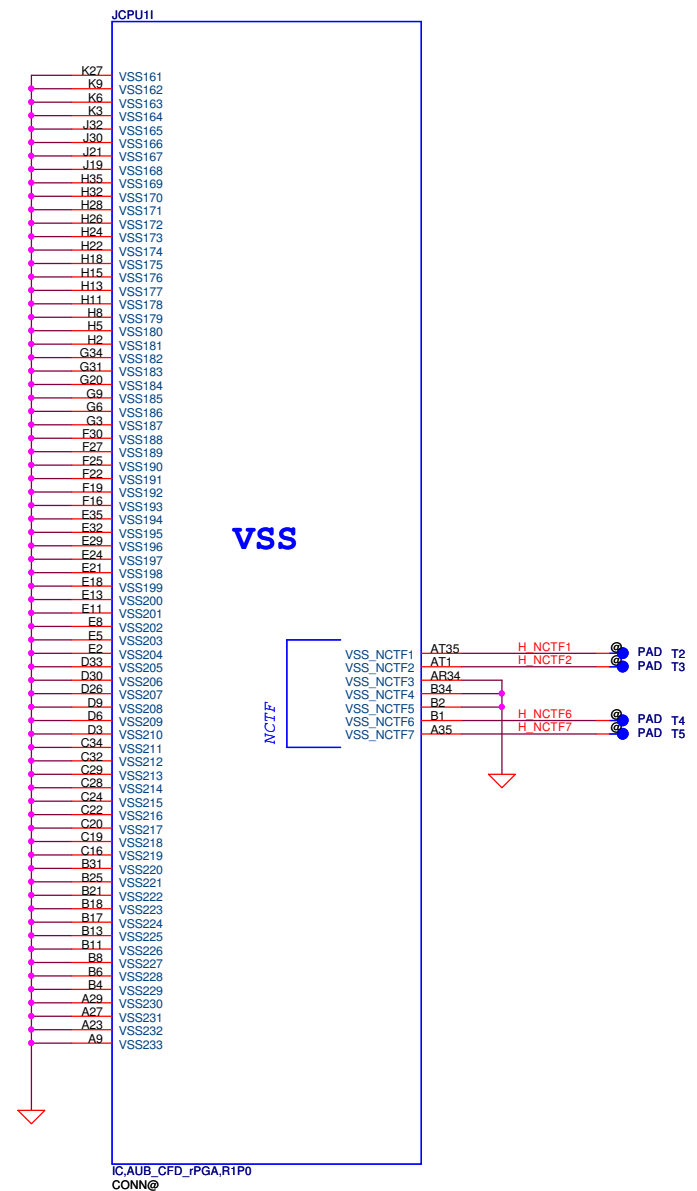
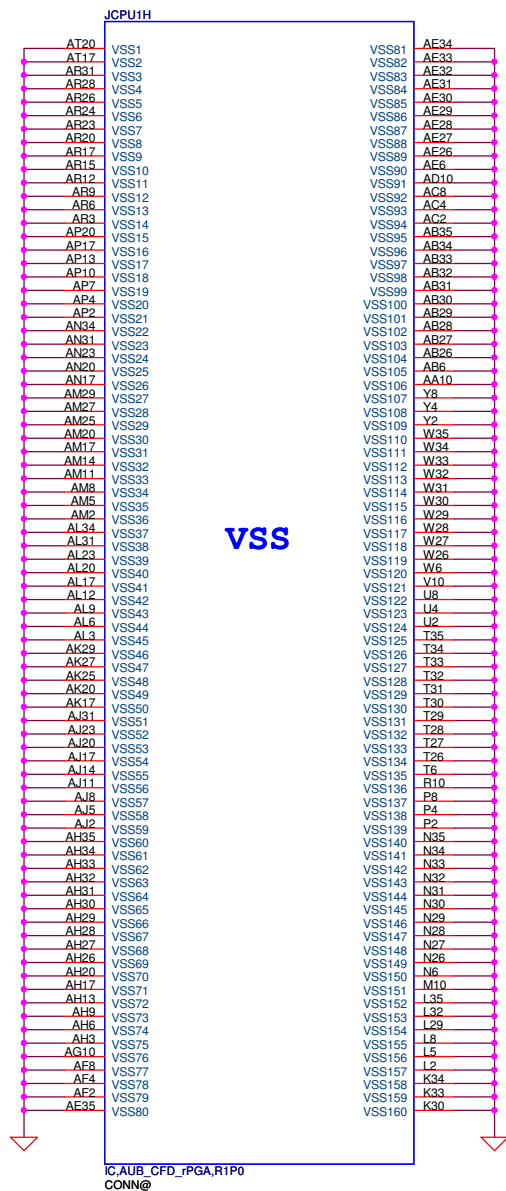
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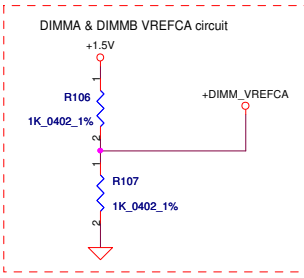
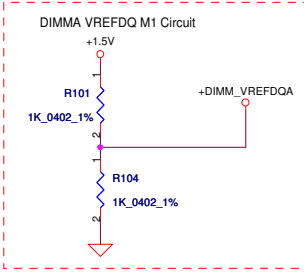




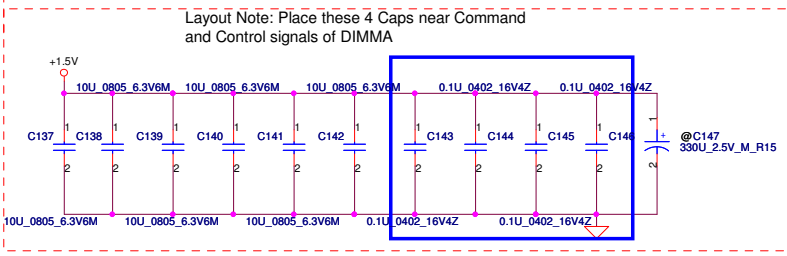
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								Size	
								Document Number	
								PEW71 M/B LA-6582P Schematic	
								Rev	
								1.0	
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								Thursday, July 08, 2010	
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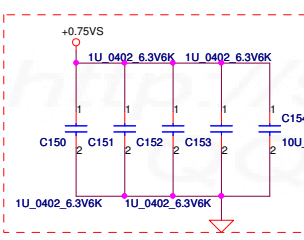
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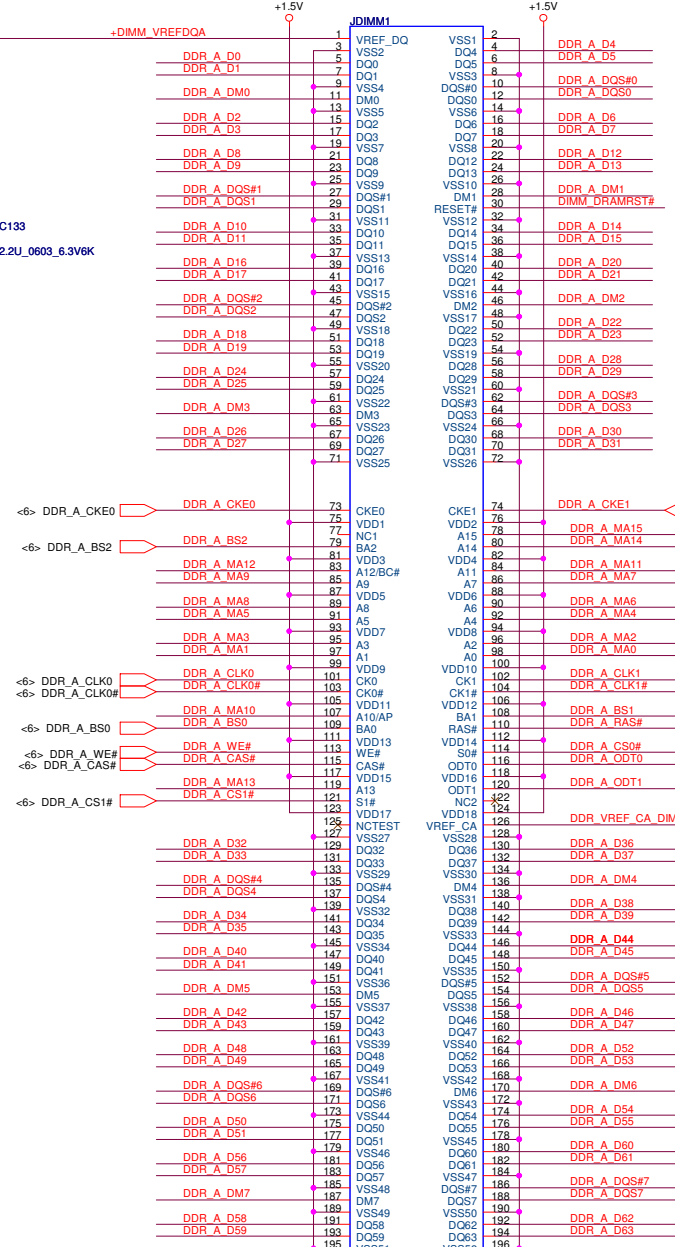
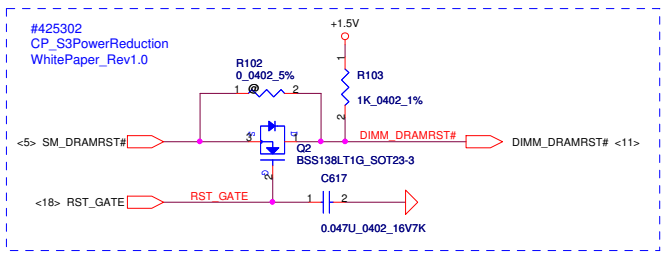
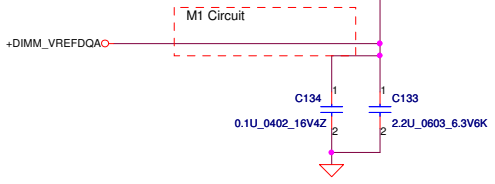
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203 & JDIMM1.204

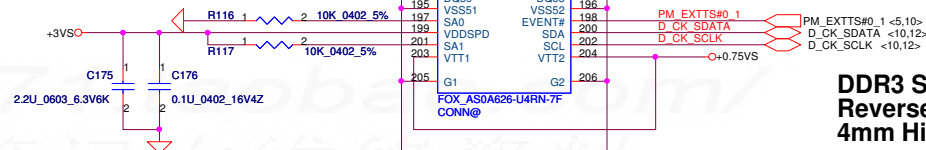
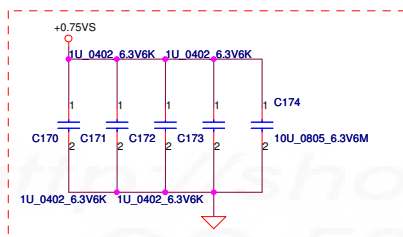
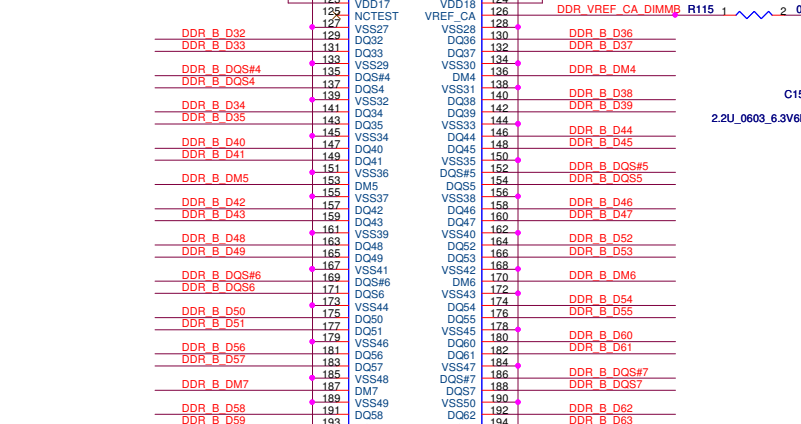
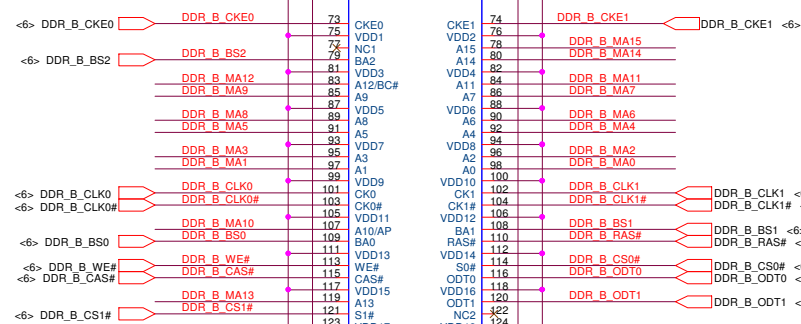
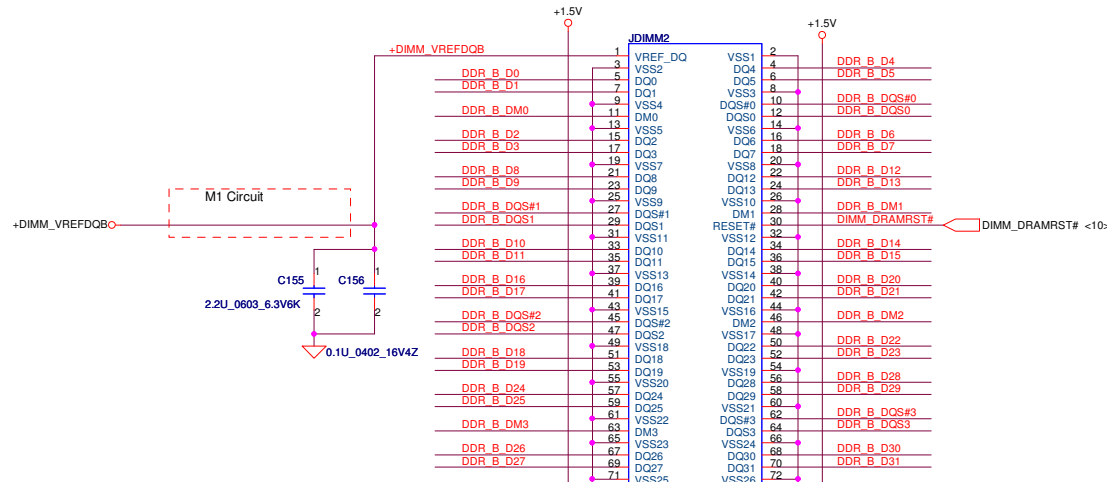
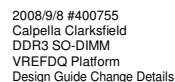


<6> DDR_A_DQS#[0..7]
<6> DDR_A_D[0..63]
<6> DDR_A_DM[0..7]
<6> DDR_A_DQS[0..7]
<6> DDR_A_MA[0..15]



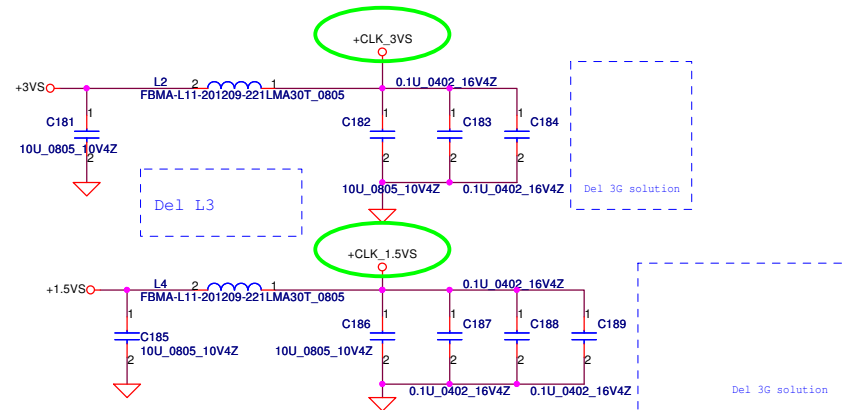
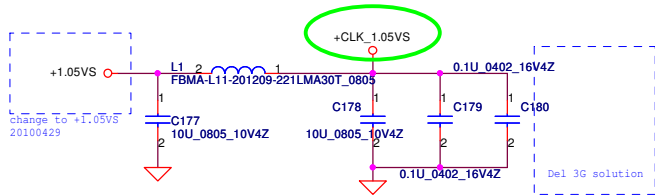
DDR3 SO-DIMM A
Change to Reverse Type
8mm High

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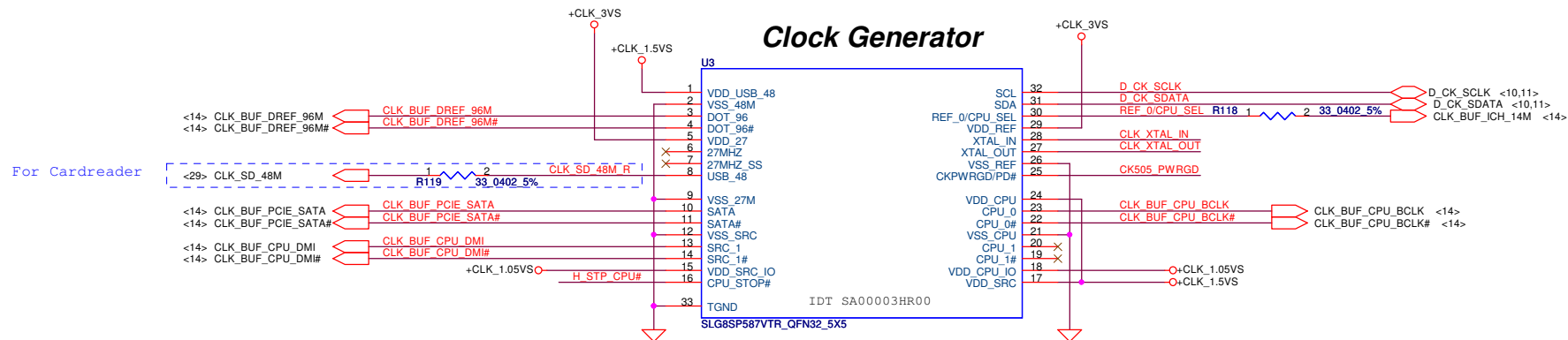


DDR3 SO-DIMM B
Reverse Type
4mm High

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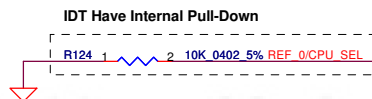
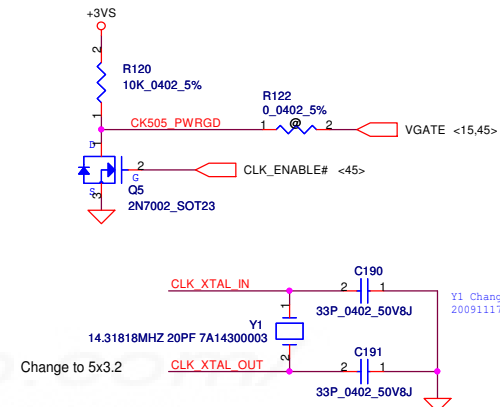
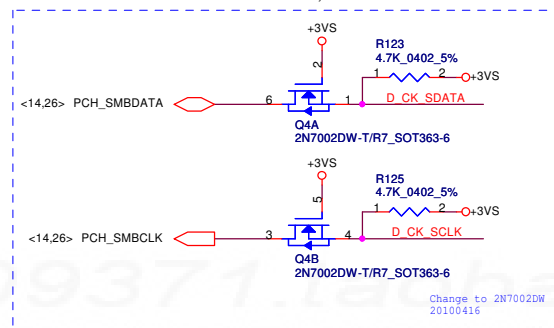
Clock Generator



IDT: 9LRS3199AKLFT, SA000030P00
SILEGO: SLG8SP587V(WF), SA00002XY10

Low Power:

IDT: 9LVS3199AKLFT, SA00003HR00
Realtek: RTM890N-631-GRT, SA00003HQ00

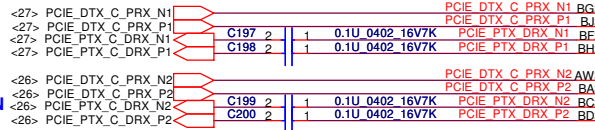


PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

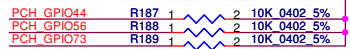
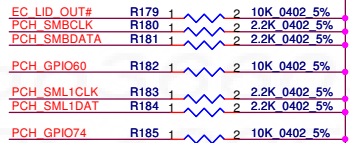
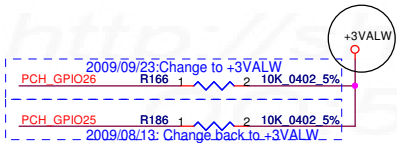
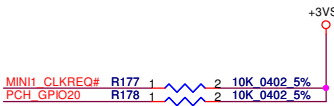
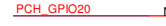
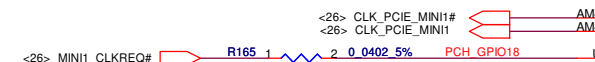
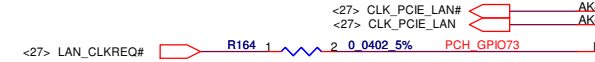
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For PCIE LAN

For Wireless LAN



2/10 PCIE7, PCIE8 not support on HM55



U4B

REV1.0

PCI-E*

Controller

Link

PEG

From CLK BUFFER

Clock Flex

IBEXPEAK-M_FCBGA107

SMBus

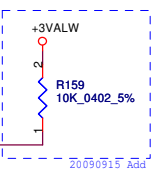
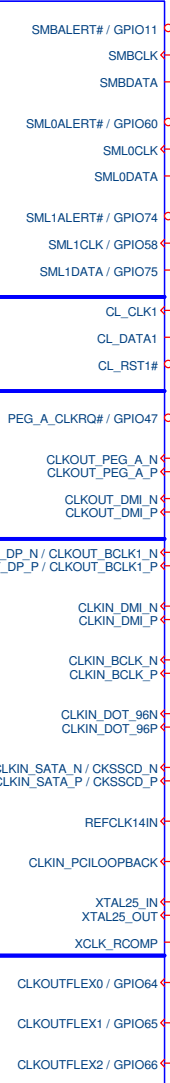
Controller

Link

PEG

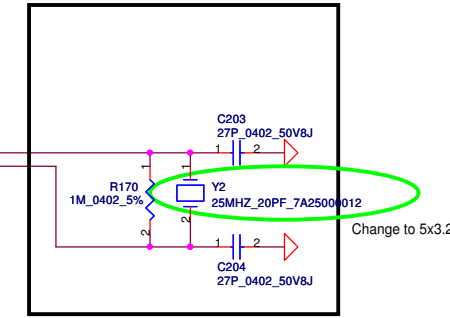
From CLK BUFFER

Clock Flex



1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

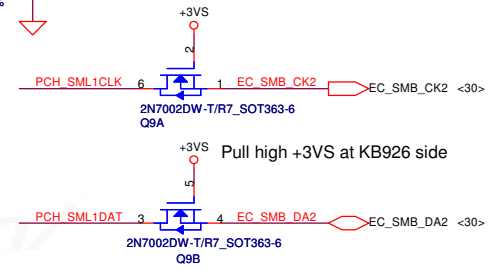
6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics



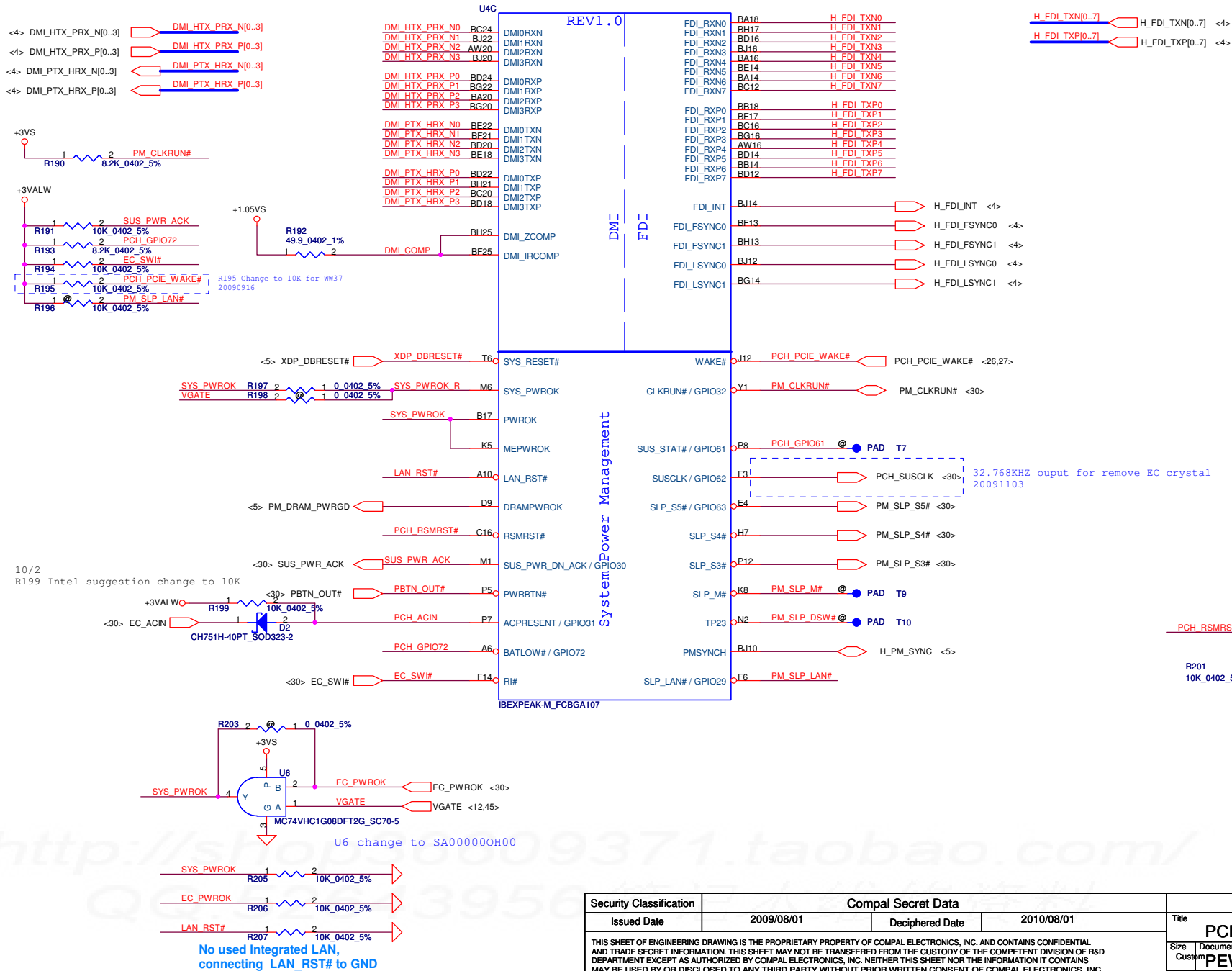
Change to 5x3.2

0602 GPIO65 no use
PULL HIGH:PVT
PULL DOWN:DVT

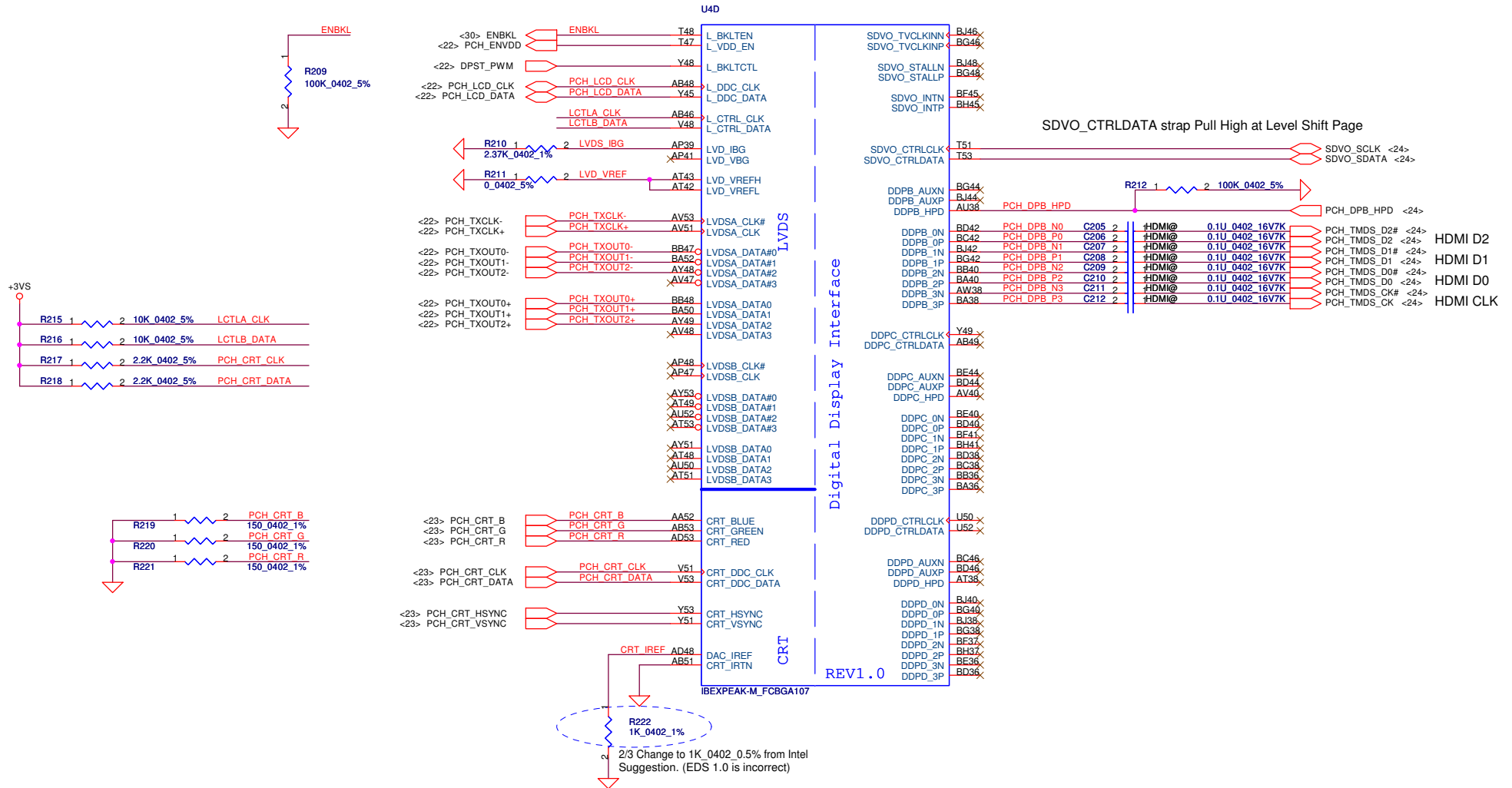
GPIO66 6L/8L	
SATA register separe	
GPIO66	
0	6L *
1	8L

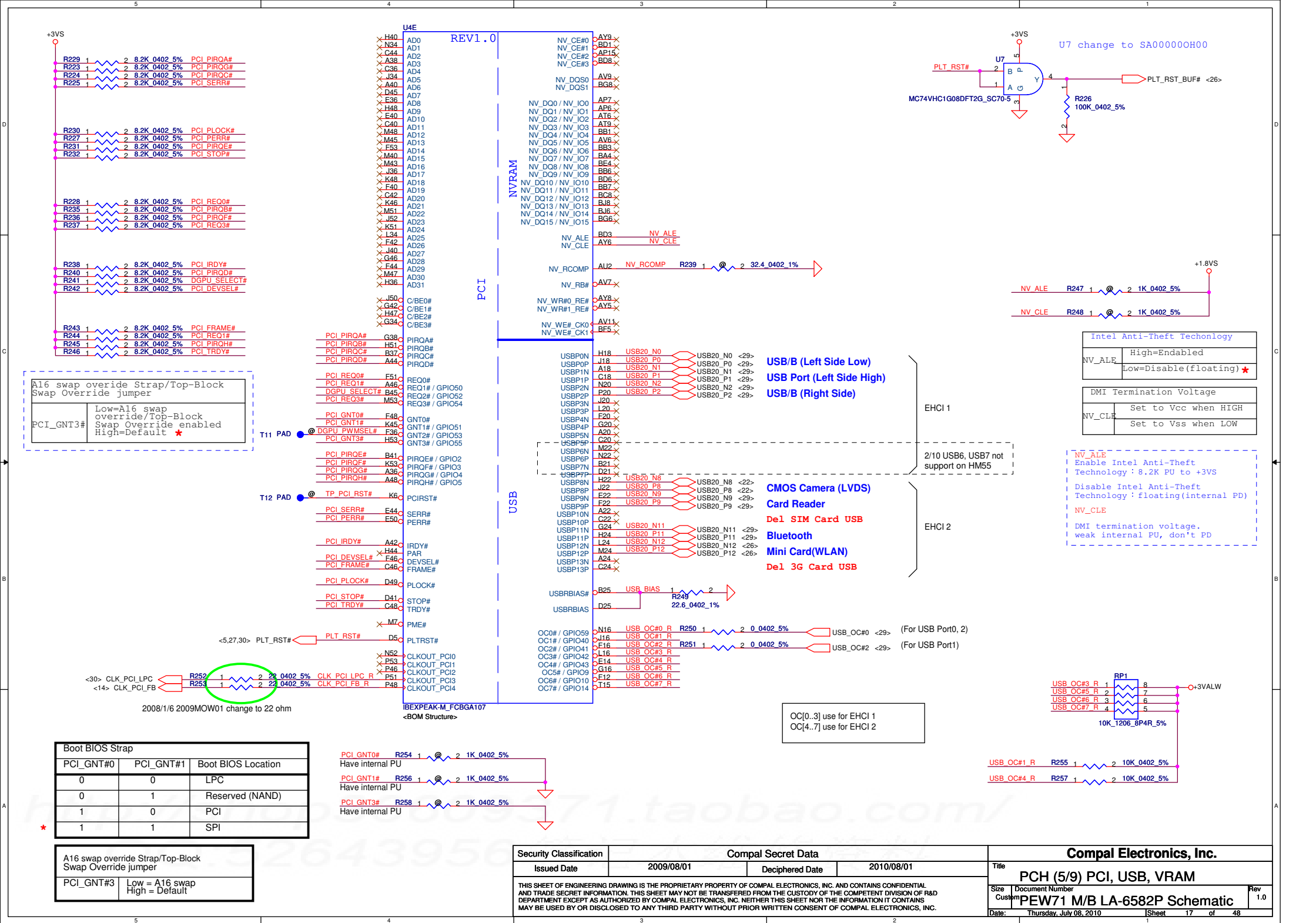


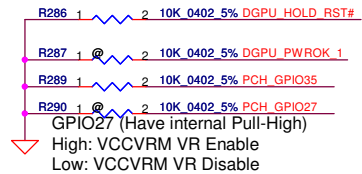
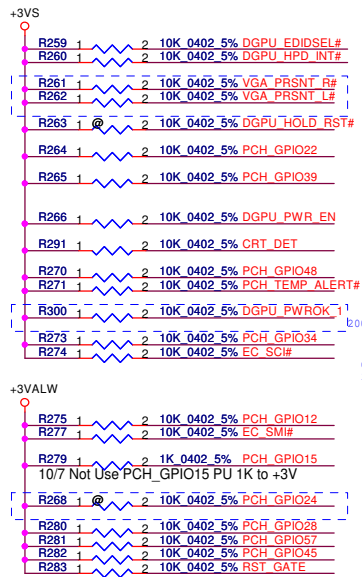
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	GPIO19	GPIO37
	PCH_GPIO19	VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
SG	1	0

GPIO27
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H: On-Die voltage regulator enable
L: On-Die PLL Voltage Regulator disable

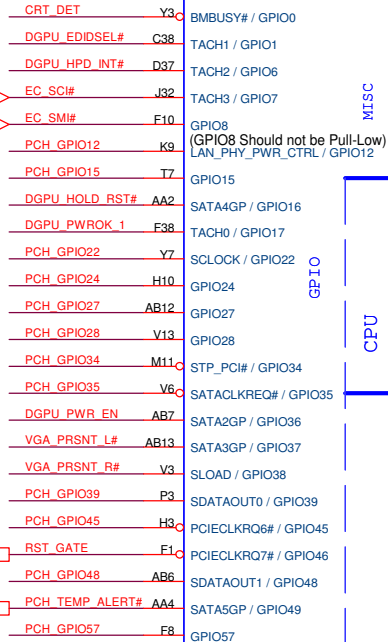
GPIO8
This signal has a weak internal pull up
Can't Pull low

GPIO15
U: Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality
H: Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality
It have weak internal PU 20K

0090915 Add

GPIO24 change PU +3VS to +3VALW
20090916

<10> RST_GATE
<30> PCH_TEMP_ALERT#



- A4 VSS_NCTF_1
- A49 VSS_NCTF_2
- A5 VSS_NCTF_3
- A50 VSS_NCTF_4
- A52 VSS_NCTF_5
- A53 VSS_NCTF_6
- B2 VSS_NCTF_7
- B4 VSS_NCTF_8
- B52 VSS_NCTF_9
- B53 VSS_NCTF_10
- BE1 VSS_NCTF_11
- BE53 VSS_NCTF_12
- BF1 VSS_NCTF_13
- BF53 VSS_NCTF_14
- BH1 VSS_NCTF_15
- BH2 VSS_NCTF_16
- BH52 VSS_NCTF_17
- BH53 VSS_NCTF_18
- BJ1 VSS_NCTF_19
- BJ2 VSS_NCTF_20
- BJ4 VSS_NCTF_21
- BJ49 VSS_NCTF_22
- BJ5 VSS_NCTF_23
- BJ50 VSS_NCTF_24
- BJ52 VSS_NCTF_25
- BJ53 VSS_NCTF_26
- D1 VSS_NCTF_27
- D2 VSS_NCTF_28
- D53 VSS_NCTF_29
- E1 VSS_NCTF_30
- E53 VSS_NCTF_31

REV1.0

IBEXPEAK-M_FCBGA107

MISC

GPIO

CPU

NCTF

RSVD

REV1.0

IBEXPEAK-M_FCBGA107

UAF

MISC

GPIO

CPU

NCTF

RSVD

REV1.0

IBEXPEAK-M_FCBGA107

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REV1.0

IBEXPEAK-M_FCBGA107

UAF

MISC

GPIO

CPU

NCTF

RSVD

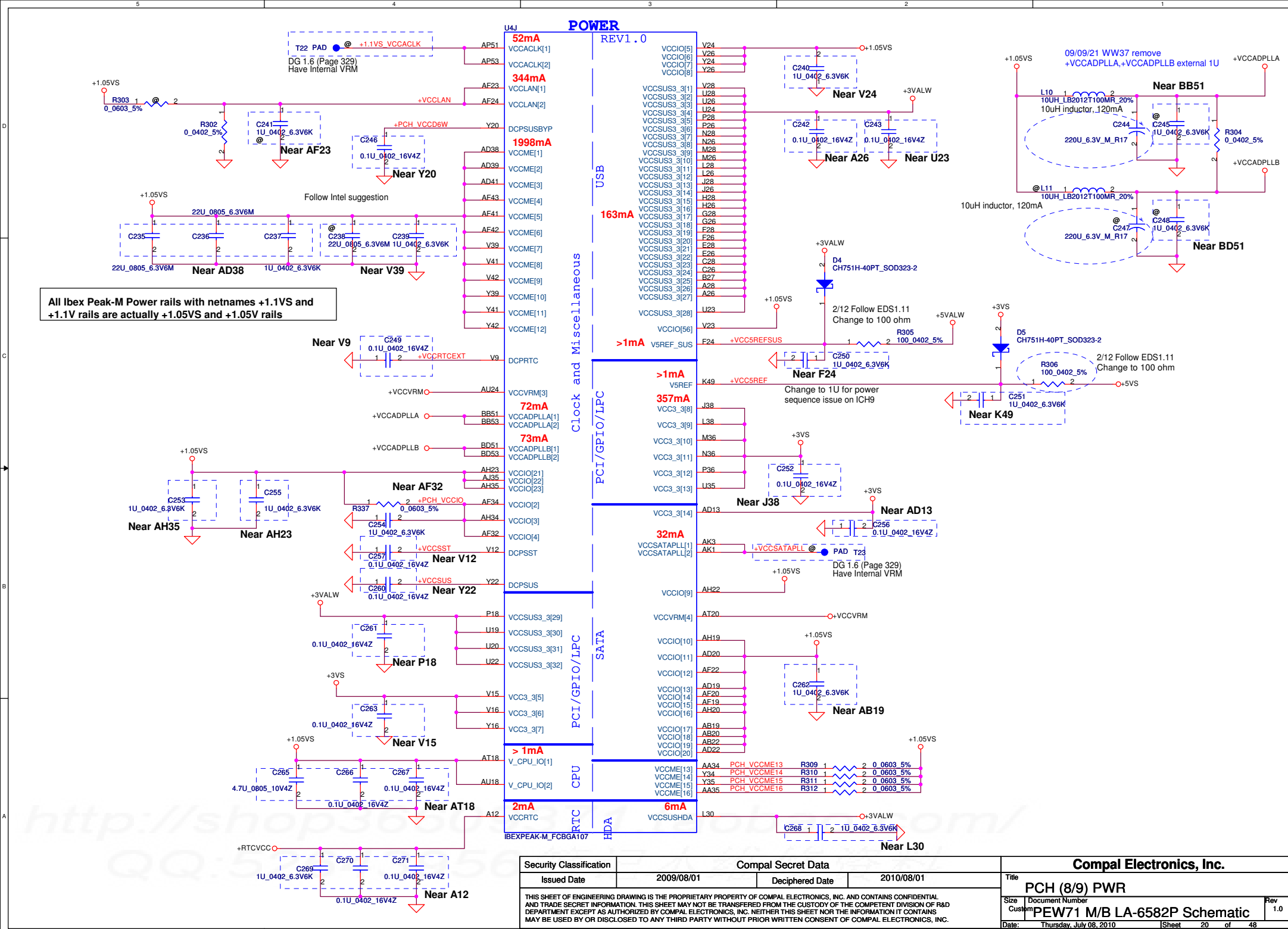
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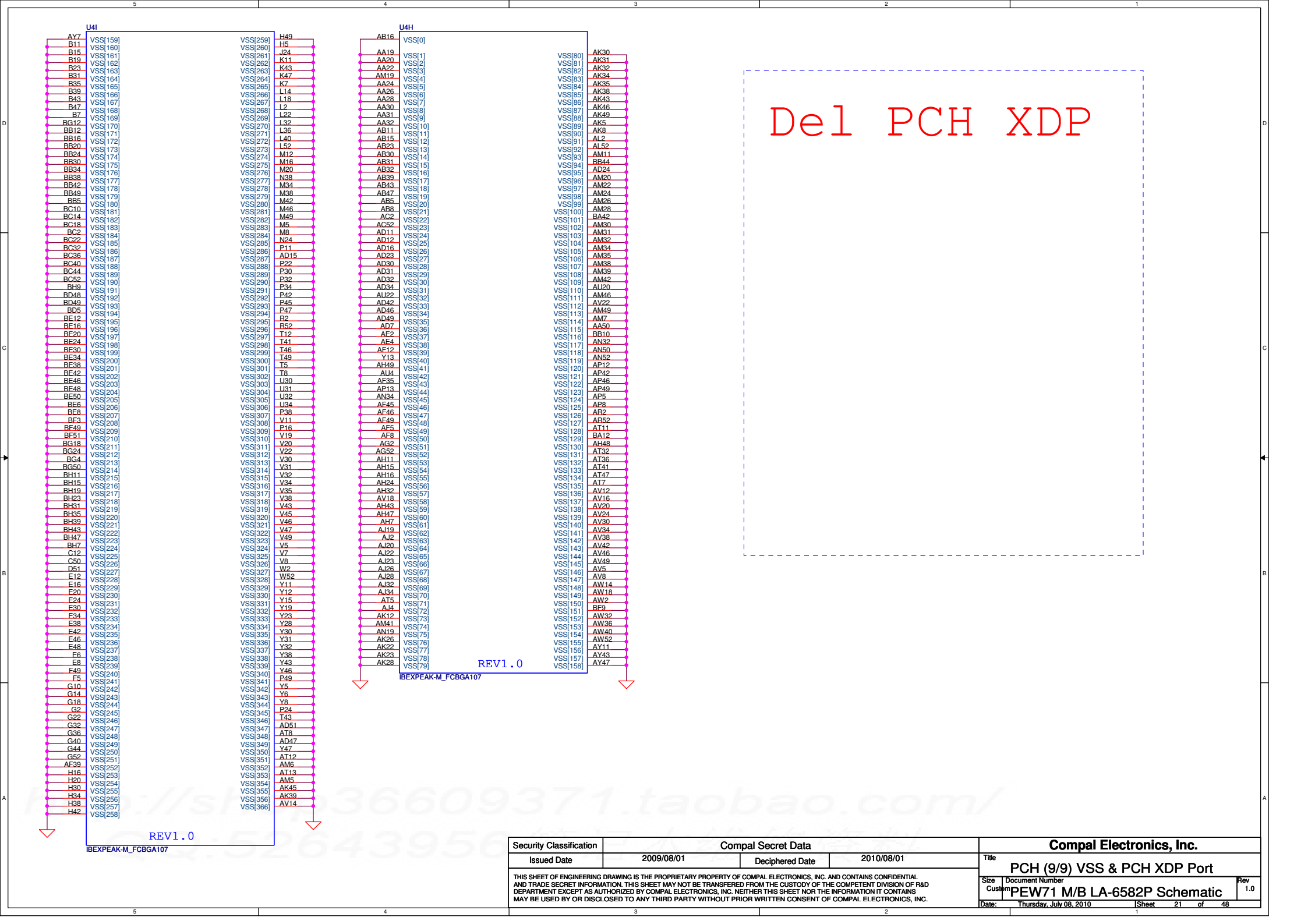
IBEXPEAK-M_FCBGA107

All Ixex Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

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Compal Electronics, Inc.			
Title PCH (8/9) PWR			
Size Custom	Document Number PEW71 M/B LA-6582P Schematic	Rev 1.0	
Date	Thursday, July 08, 2010	Sheet	20 of 48





Del PCH XDP

REV1.0

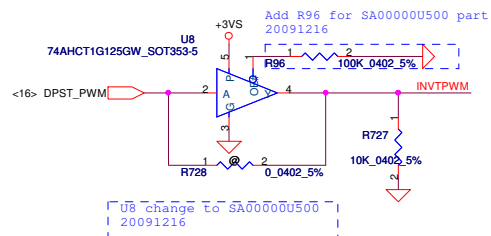
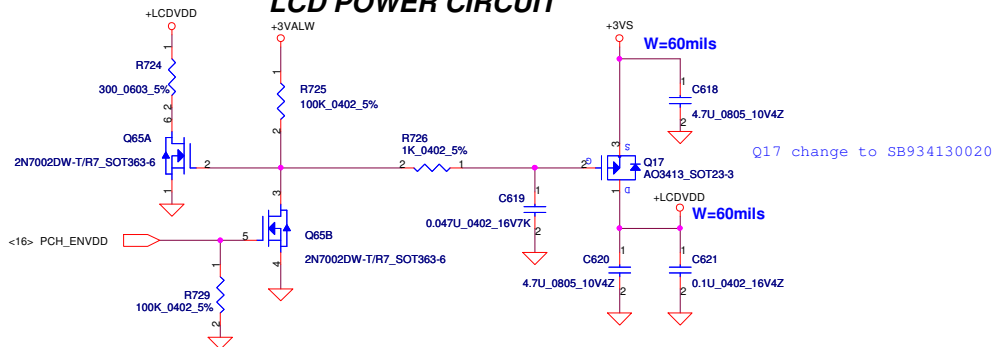
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REV1.0

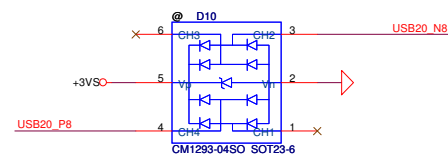
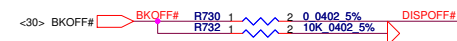
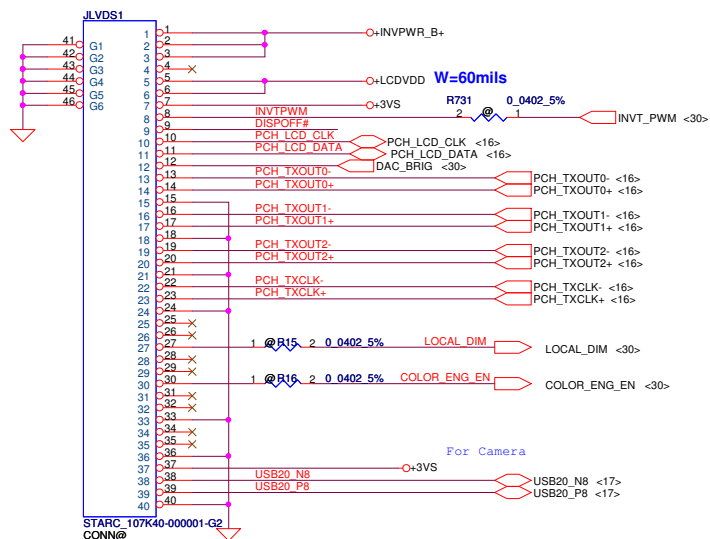
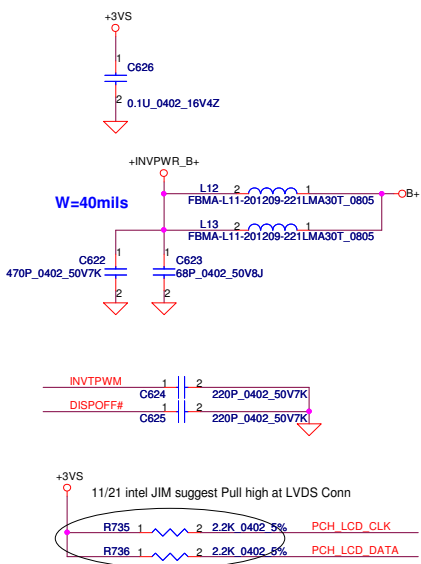
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Issued Date		2009/08/01		Deciphered Date		2010/08/01		Title			
								PCH (9/9) VSS & PCH XDP Port			
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								Customer	PEW71 M/B LA-6582P Schematic		
								Date:	Thursday, July 08, 2010	Sheet	21 of 48

LCD POWER CIRCUIT

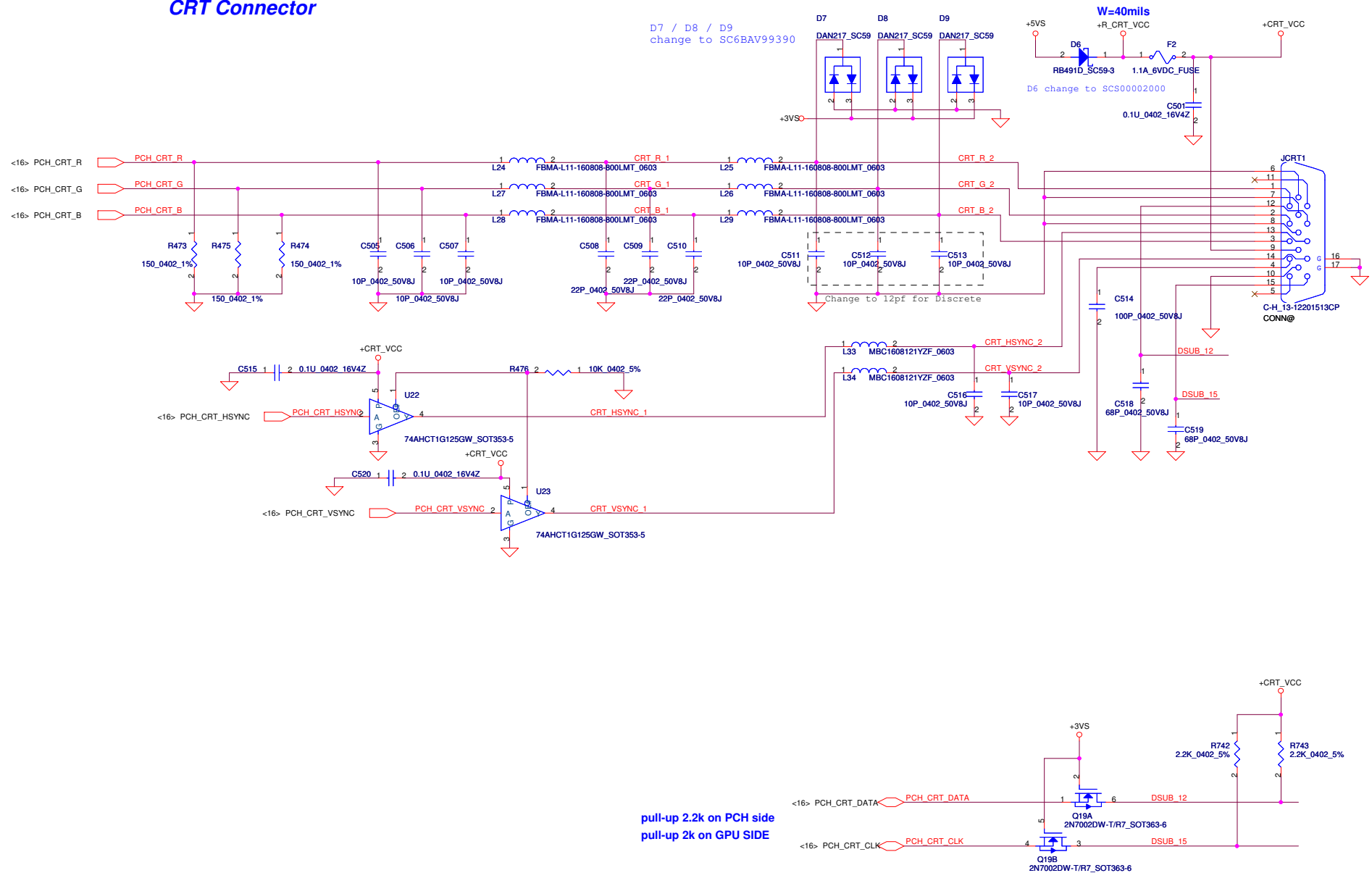


LED PANEL Conn.



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						Size		Document Number		PEW71 M/B LA-6582P Schematic		Rev 1.0	
						Custom							
						Date		Thursday, July 08, 2010		Sheet		22 of 48	

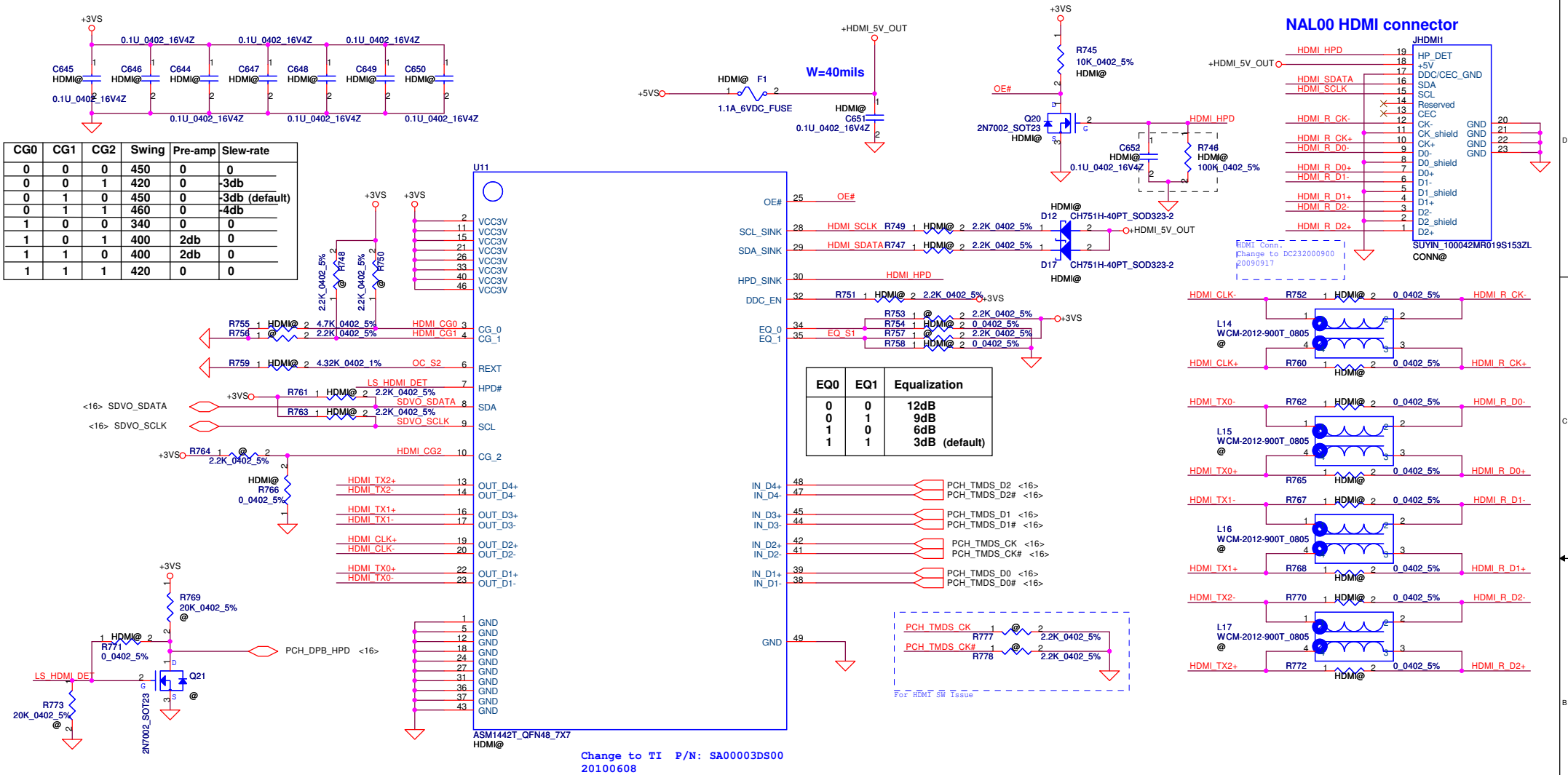
CRT Connector



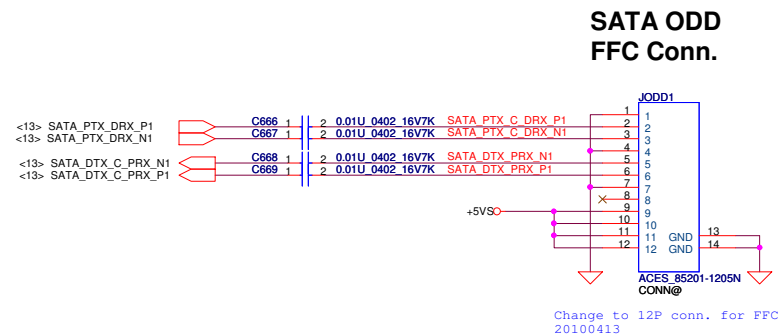
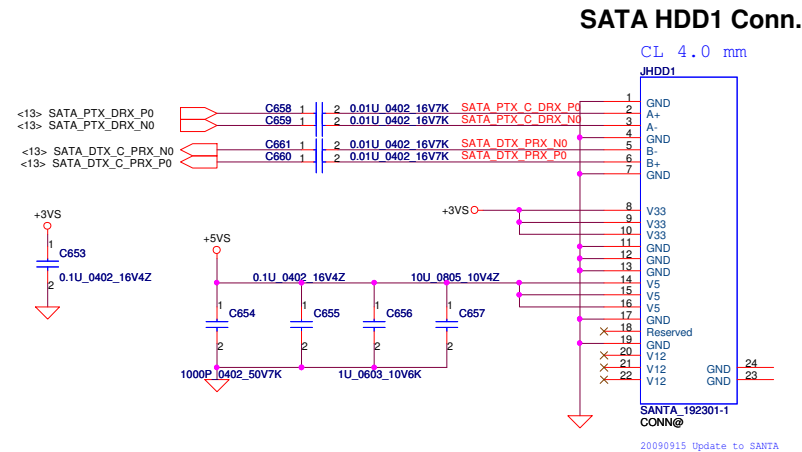
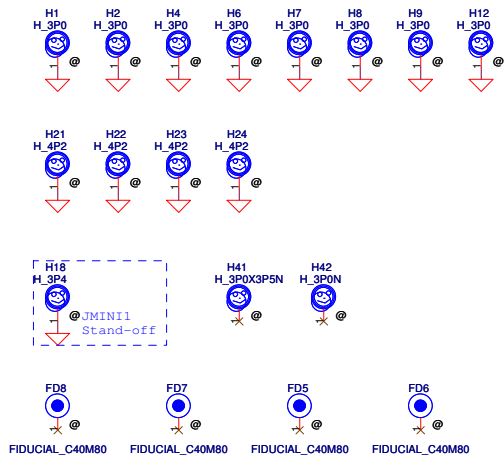
http://shop36609371.taobao.com/
QQ:52643956

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						Size B		Document Number		Rev 1.0	
						PEW71 M/B LA-6582P Schematic					
						Date: Thursday, July 08, 2010					
						Sheet 23 of 48					

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

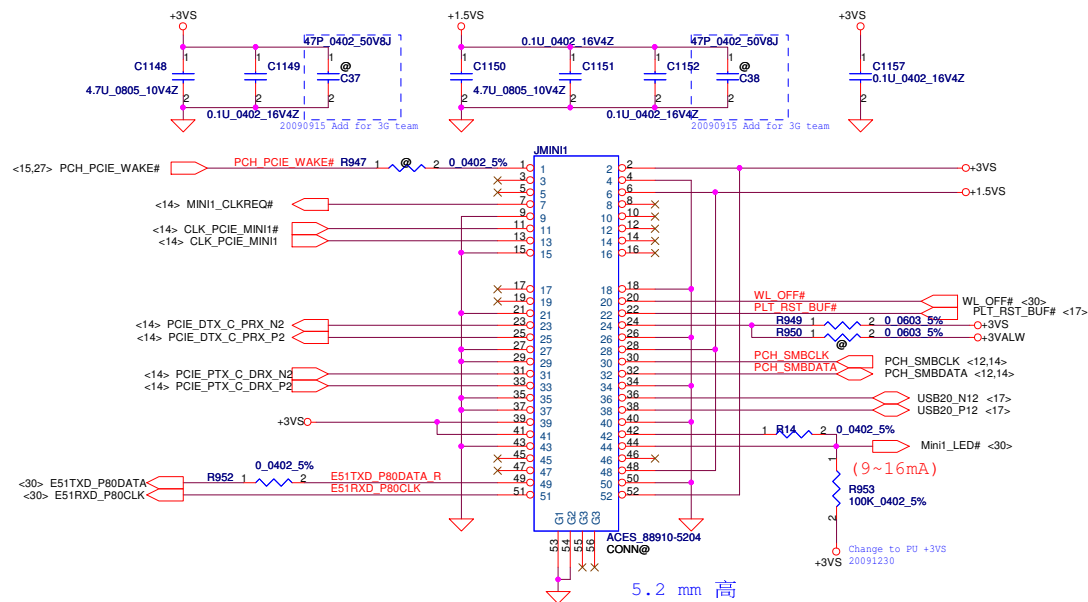


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/4/15		Deciphered Date		2010/04/15		Title	
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										Size	
										Document Number	
										PEW71 M/B LA-6582P Schematic	
										Date	
										Thursday, July 08, 2010	
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						HDD & ODD & Screw Hole			
						Size		Document Number	
						B		PEW71 M/B LA-6582P Schematic	
						Date:		Thursday, July 08, 2010	
						Sheet		25 of 48	
						Rev		1.0	

For Wireless LAN

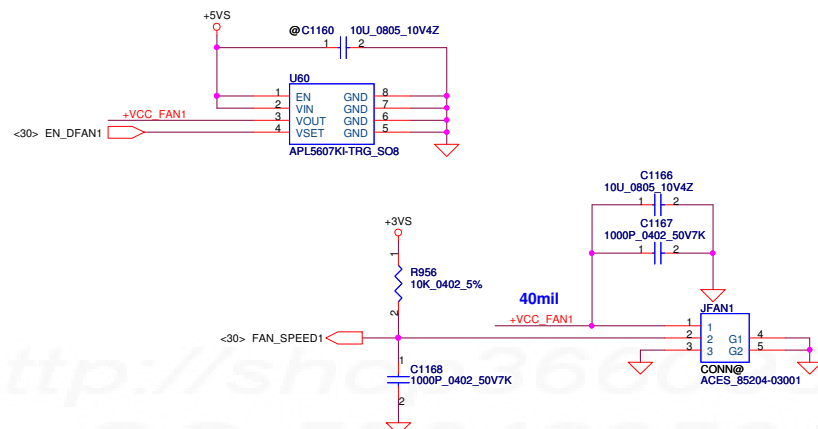


Mini Card Power Rating

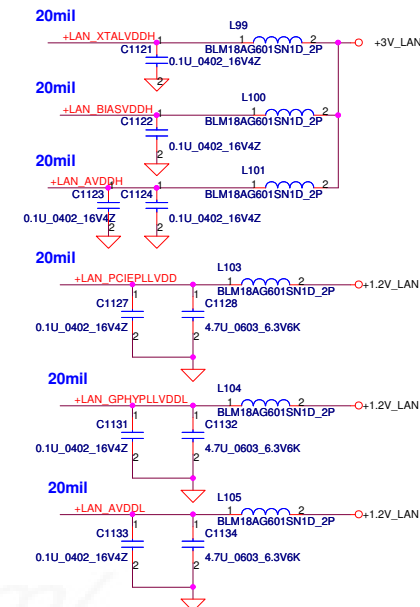
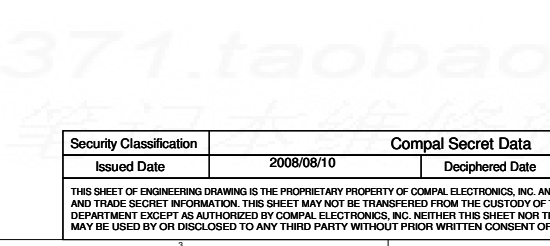
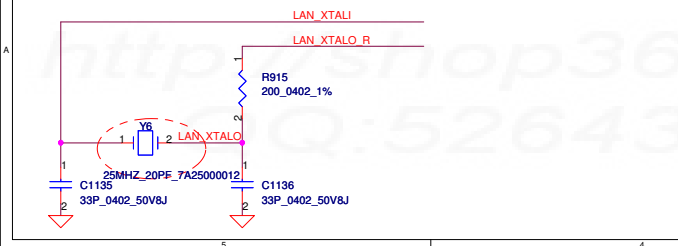
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Del 3G / GPS Module Connect

FAN1 Conn

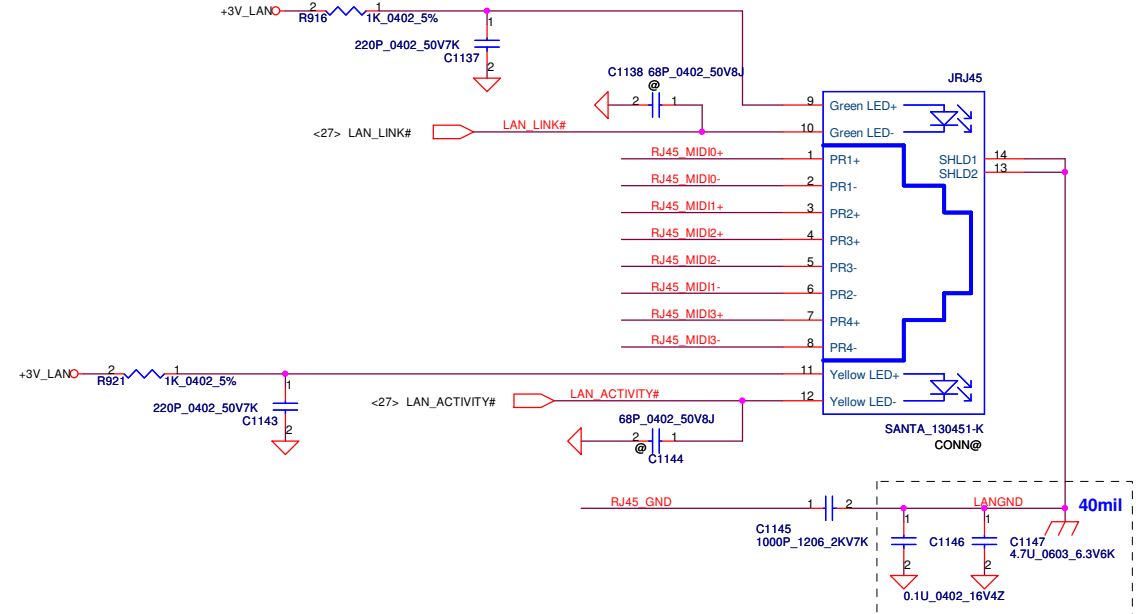
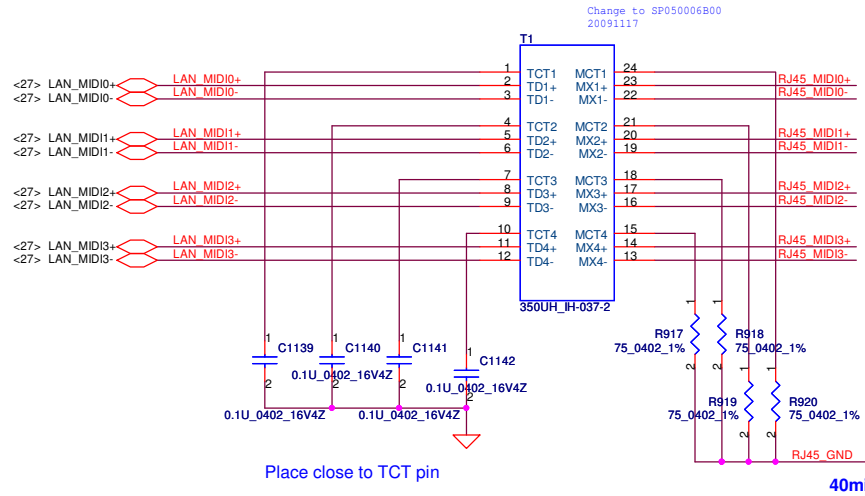


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				PEW71 M/B LA-6582P Schematic	Rev 1.0
				Date: Thursday, July 08, 2010	Sheet 26 of 48



	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

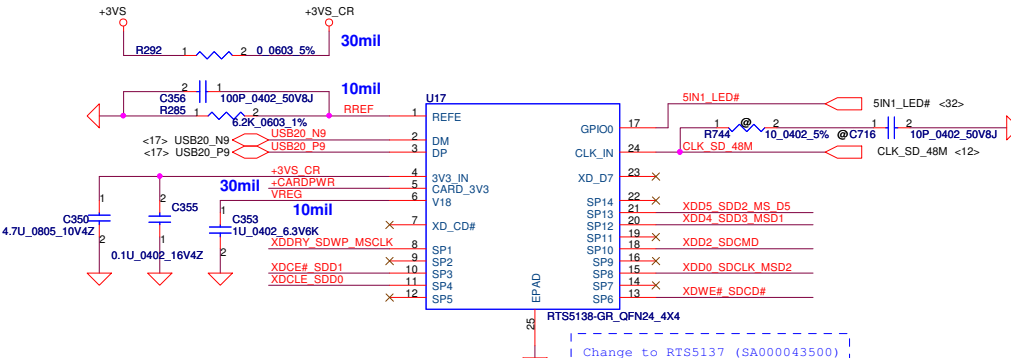
LAN Connector



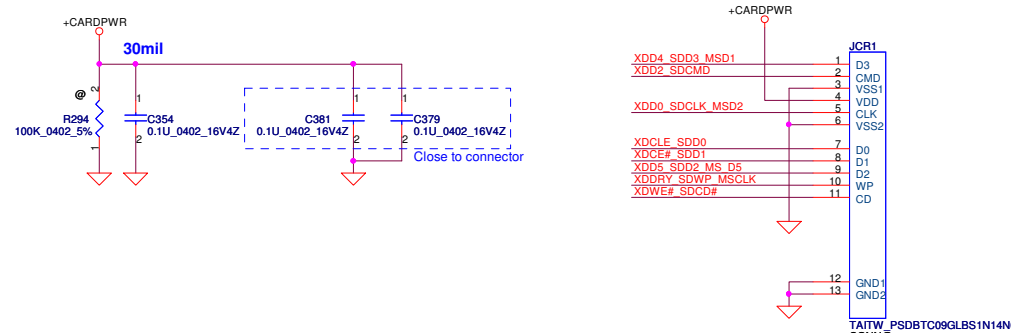
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Issued Date	2008/08/10	Deciphered Date	2009/08/10		Title

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2008/08/10	Deciphered Date	2009/08/10	Title	LAN Magnetic & RJ45	
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				Customer	PEW71 M/B LA-6582P Schematic	1.0
				Date:	Thursday, July 08, 2010	Sheet 26 of 48

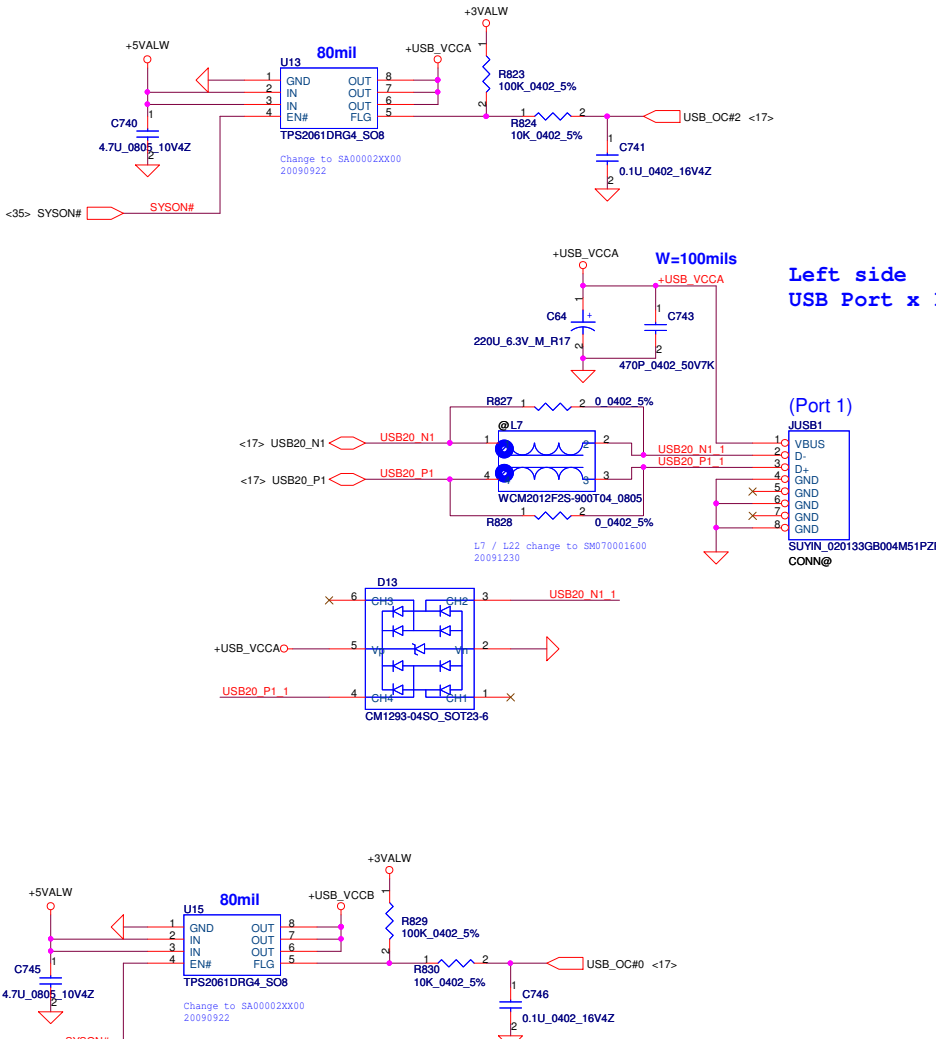
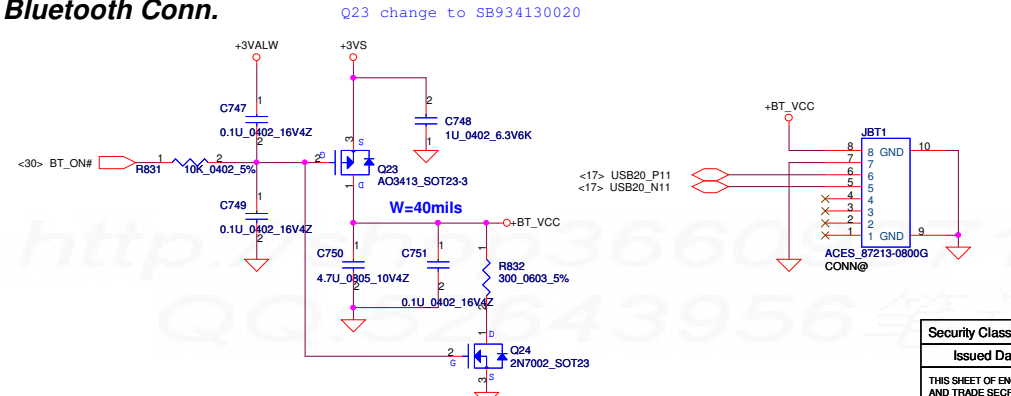
Card Reader RTS5138 / RTS5137
(only SD+MMC function)



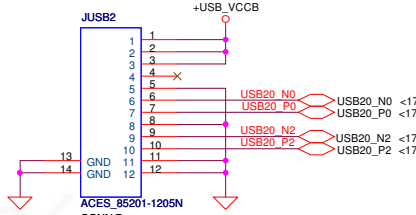
Card Reader Connector



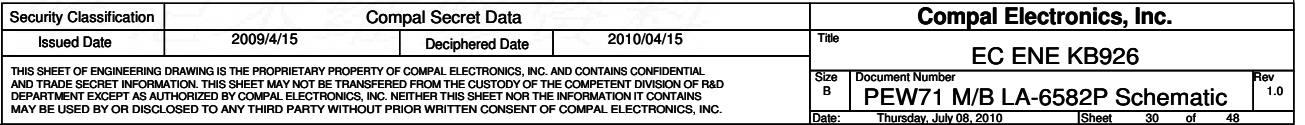
Bluetooth Conn.



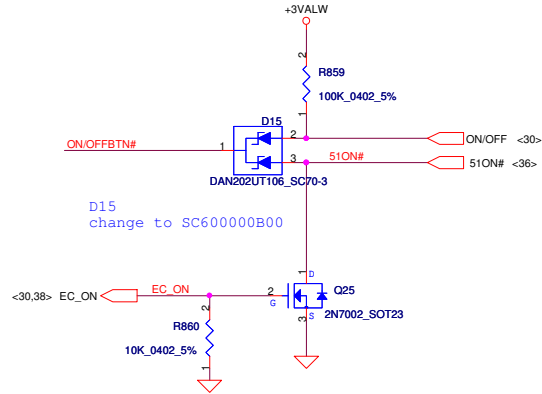
USB/B Conn.
(Port 0,2)



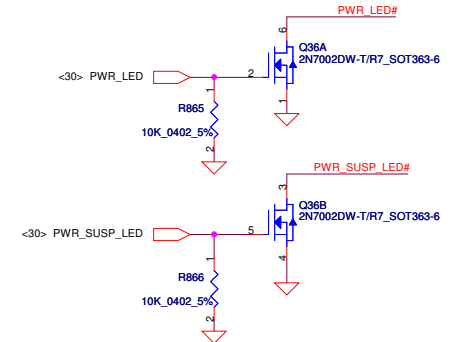
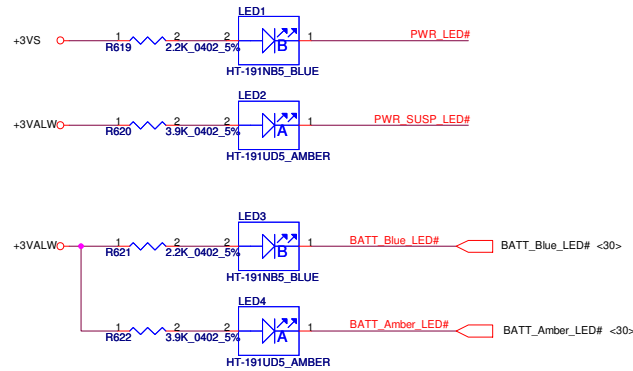
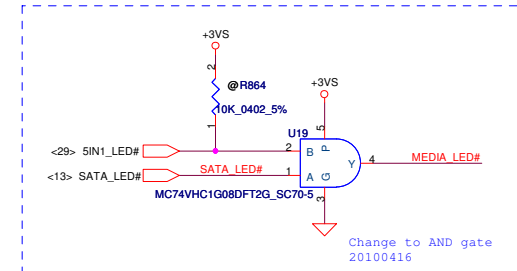
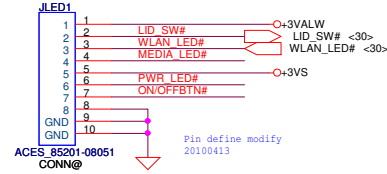
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Issued Date	2009/5/12	Deciphered Date	2009/12/31	Title	USB & Card reader& BT Connector	
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				PEW71 M/B LA-6582P Schematic		
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Power Button



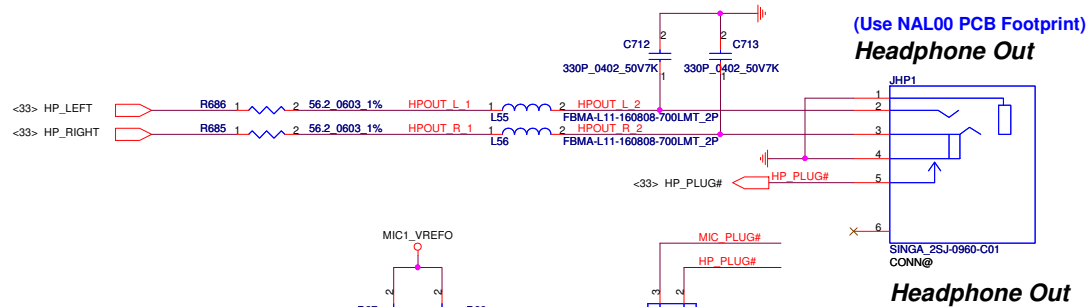
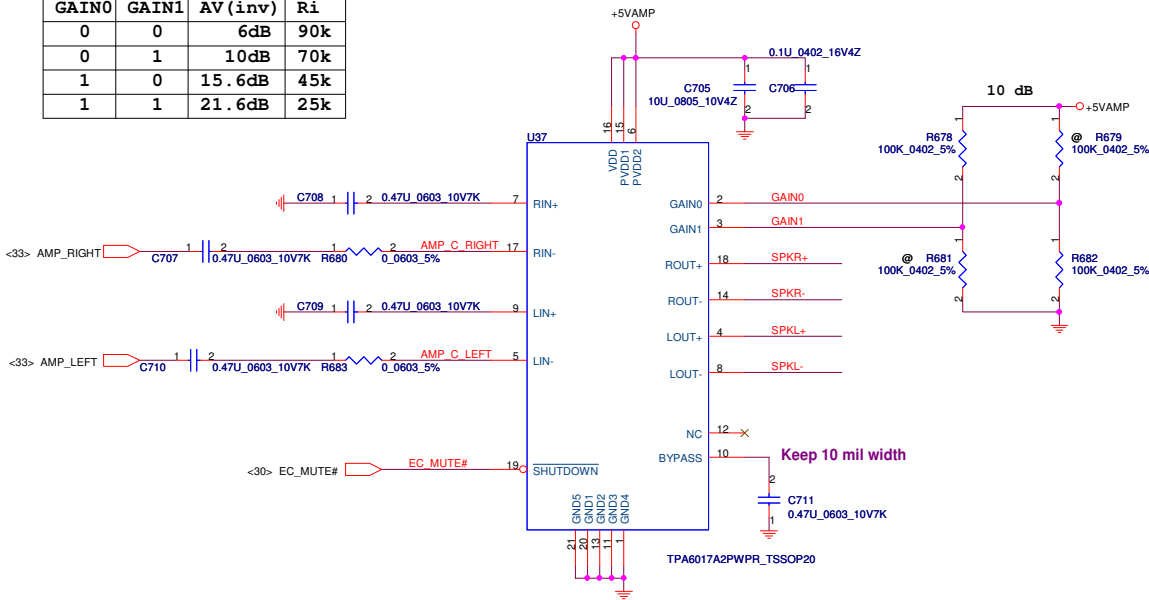
LED/B LEFT



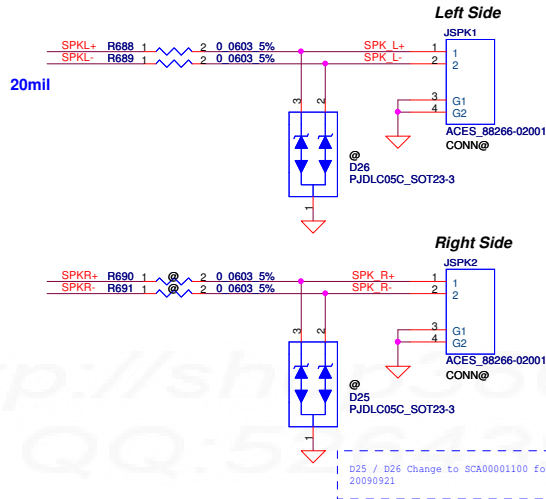
<http://shop36609371.taobao.com/>
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								Size B	Document Number			PEW71 M/B LA-6582P Schematic			Rev 1.0
								Date		Thursday, July 08, 2010		Sheet 32 of 48			

GAIN0	GAIN1	AV (inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

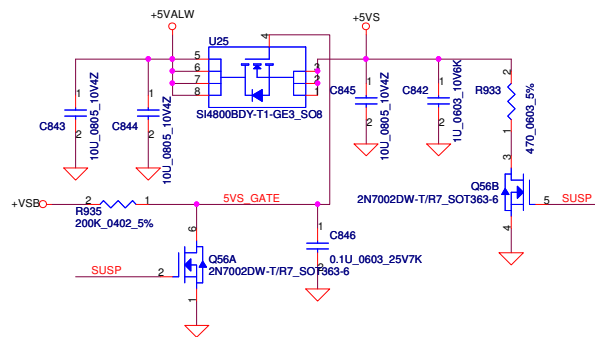


Int. Speaker Conn.

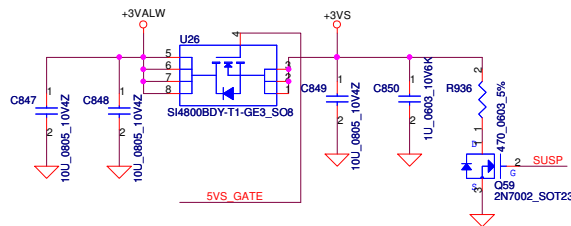


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				Date	Thursday, July 08, 2010
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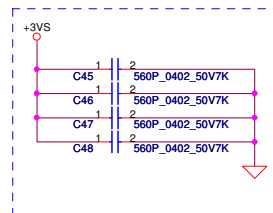
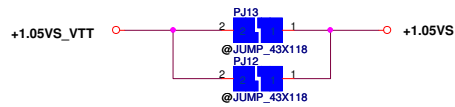
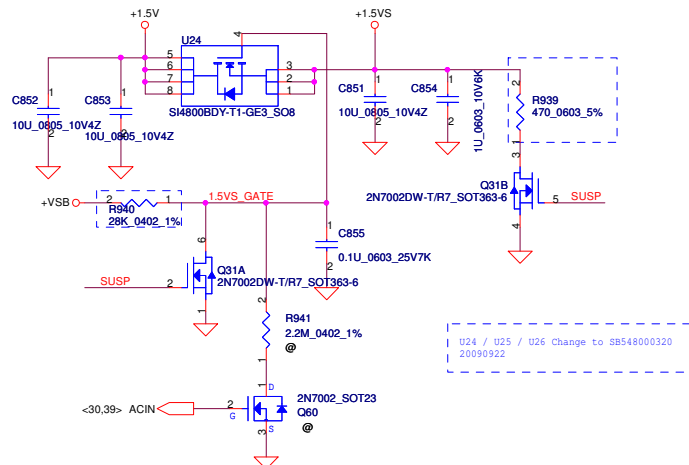
+5VALW TO +5VS



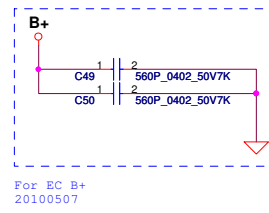
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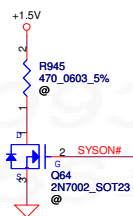
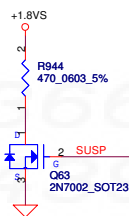
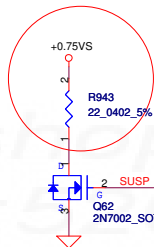
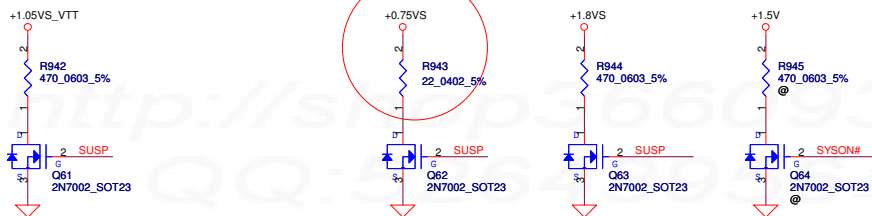
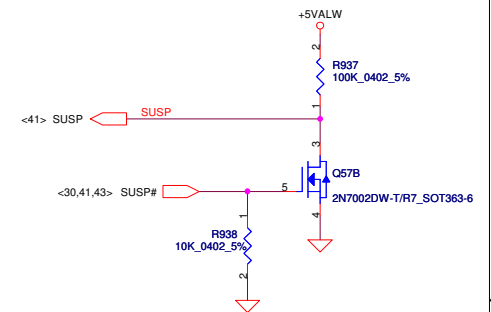
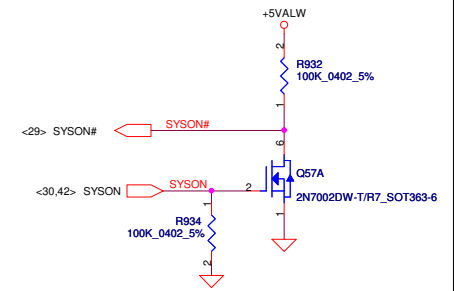
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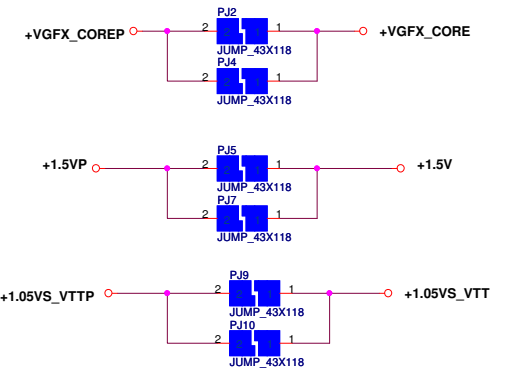
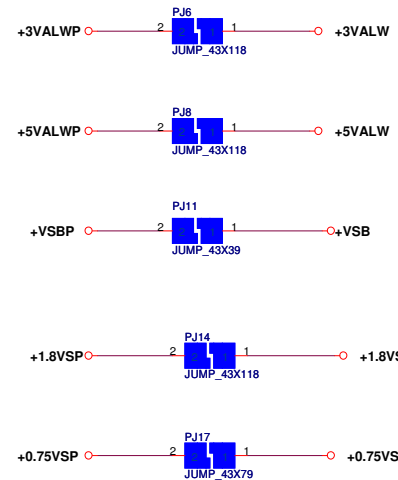
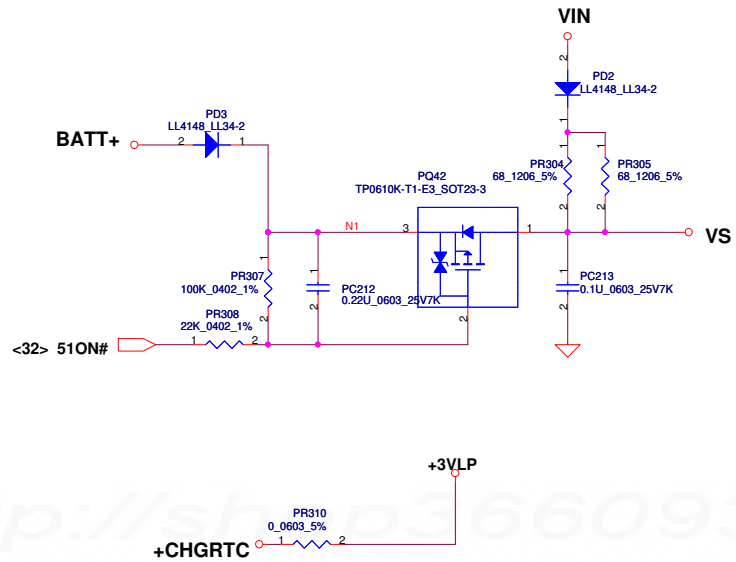
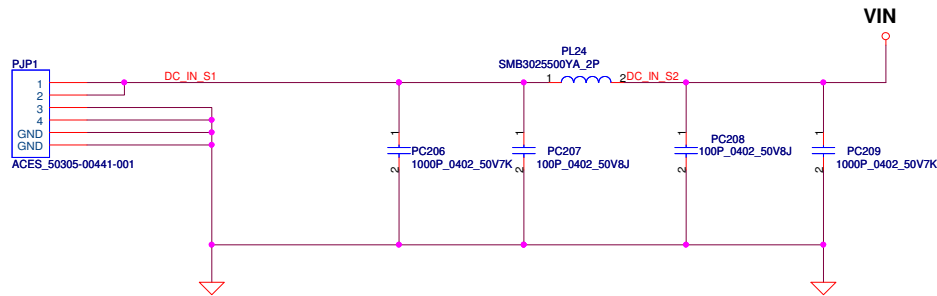
For LAM Common mode noise
200911102330



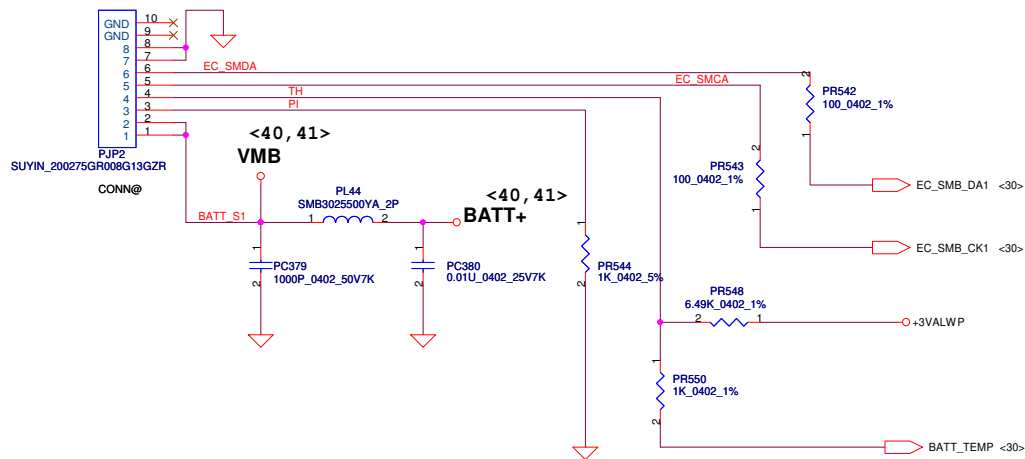
For EC B+
20100507



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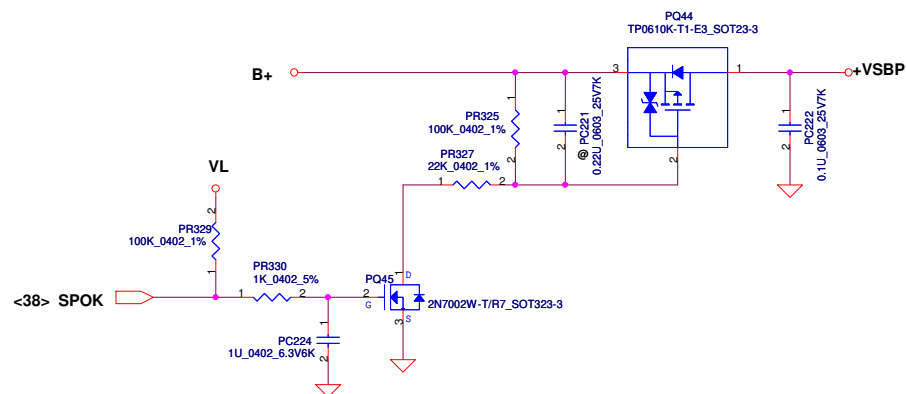
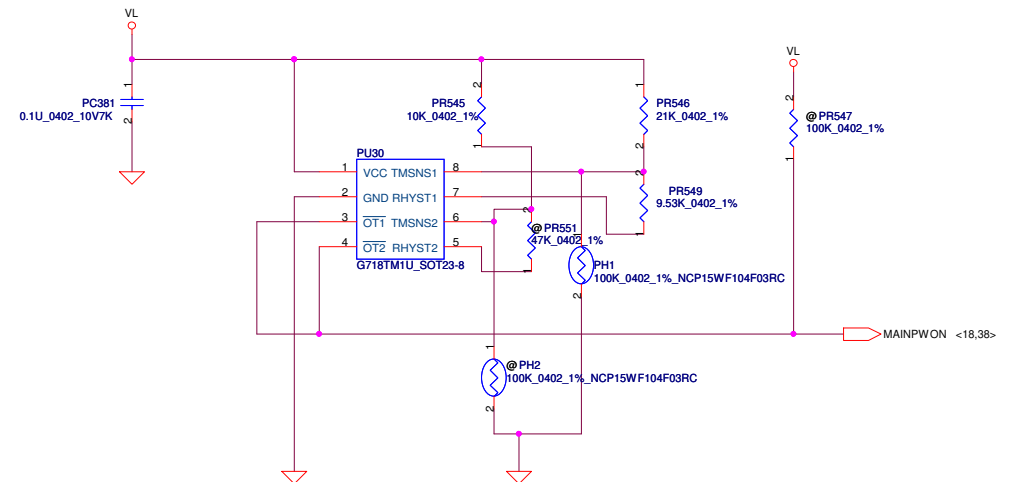
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Size	Document Number	Customer	Part Number	Rev	Rev
100mm	PEW71	M/B	LA-6582P Schematic	1.0	1.0
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PH1 under CPU botten side :

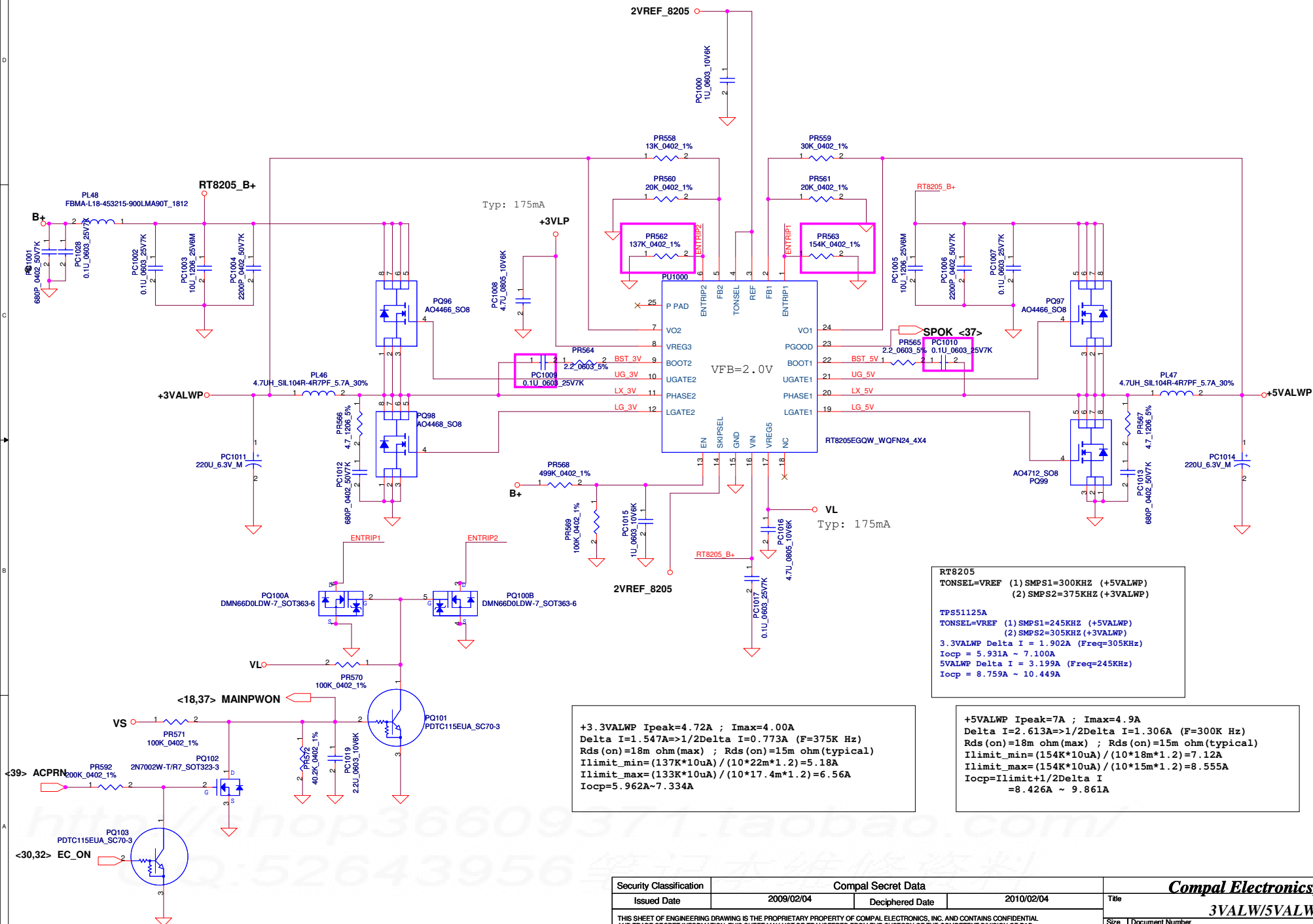
CPU thermal protection at 92 degree C

Recovery at 56 degree C



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Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

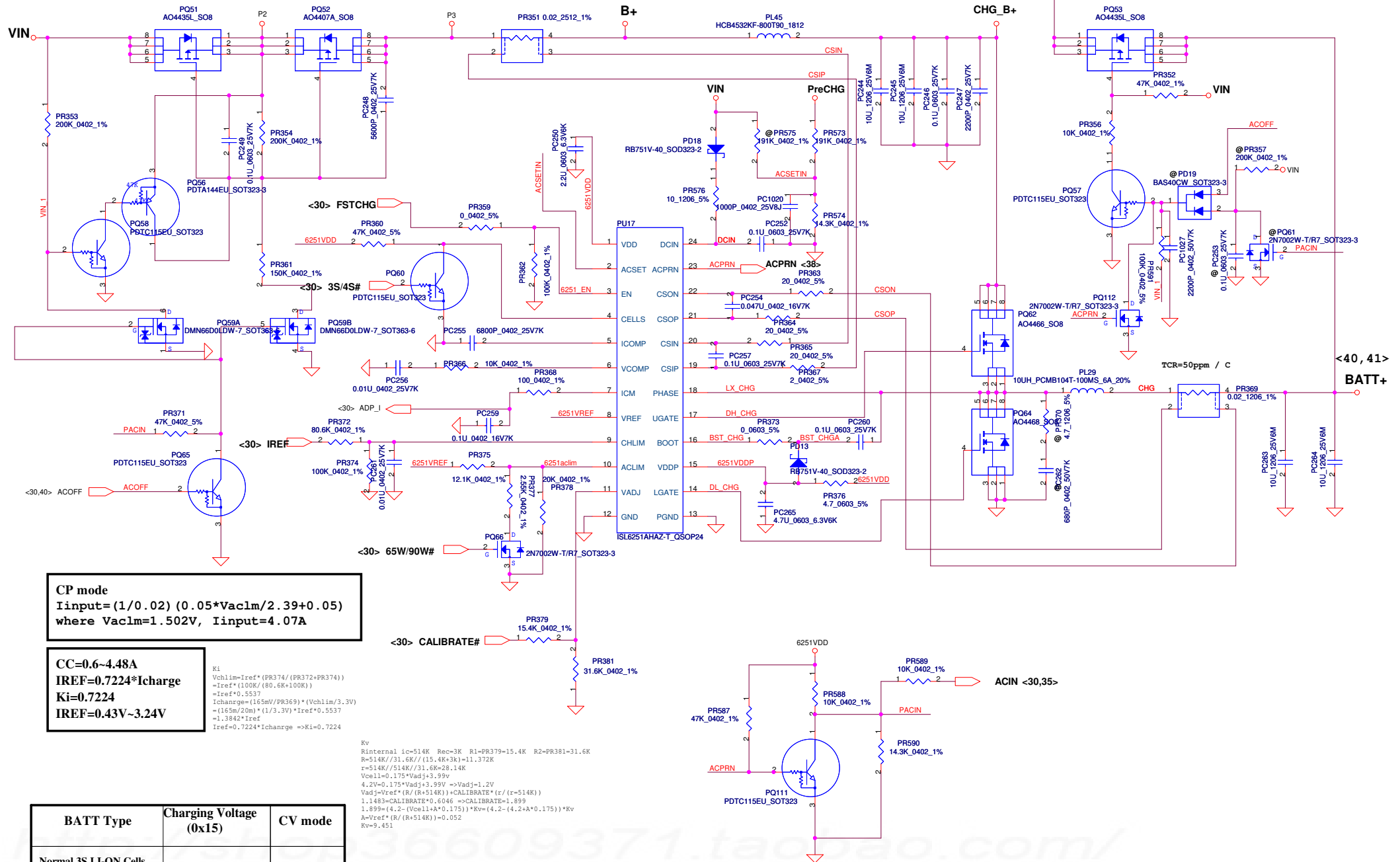


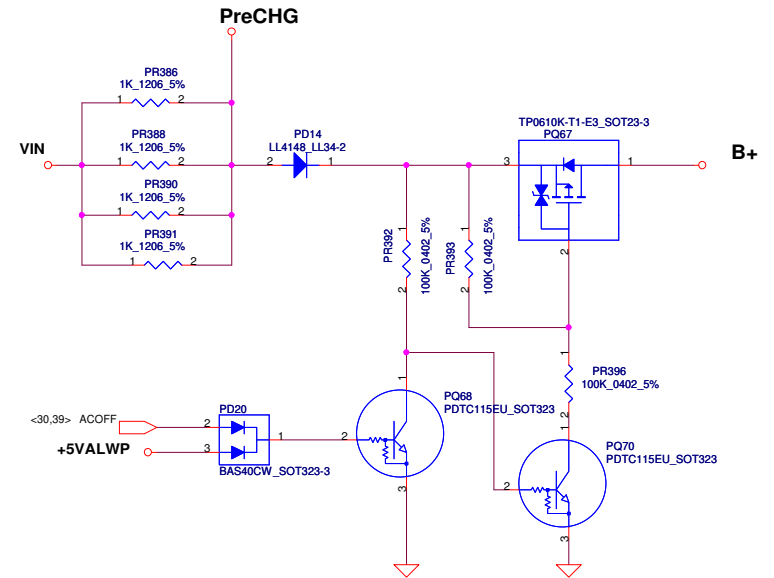
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Iada=0~4.74A (90W/19V=4.736A)
Iada=0~3.42A (90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A

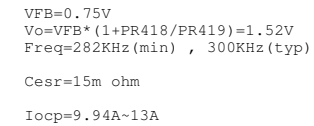


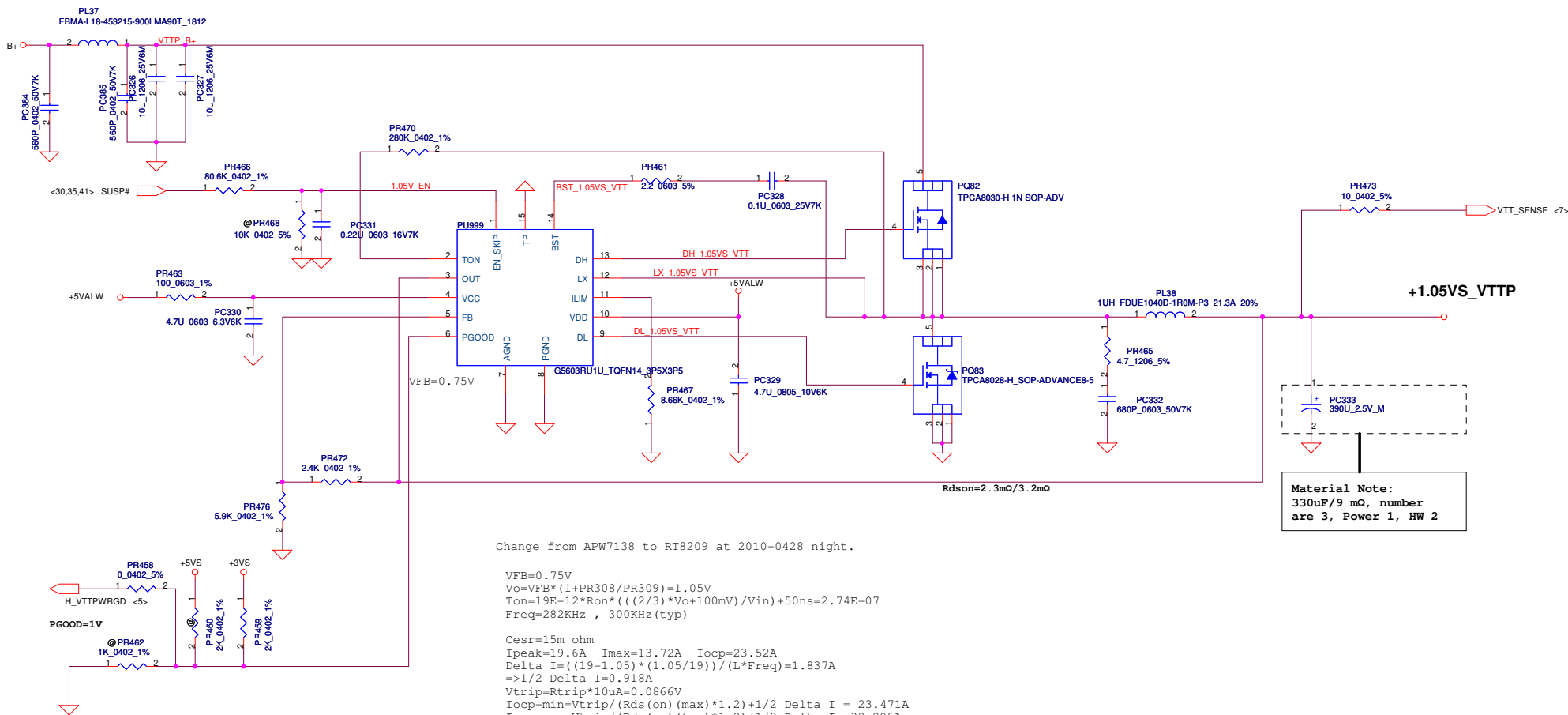


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Because +1.5VSP has 17.74A power budget, it includes DDR3, VGA chip, VRAM, so must use molding choke.





Change from APW7138 to RT8209 at 2010-0428 night.

VFB=0.75V
 $V_o = VFB * (1 + PR308 / PR309) = 1.05V$
 $Ton = 19E-12 * Ron * ((2/3) * Vo + 100mV) / Vin + 50ns = 2.74E-07$
Freq=282KHz , 300KHz (typ)

Cesr=15m ohm
Ipeak=19.6A Imax=13.72A Iocp=23.52A
 $\Delta I = ((19 - 1.05) * (1.05 / 19)) / (L * Freq) = 1.837A$
 $\Rightarrow 1/2 \Delta I = 0.918A$
 $V_{trip} = R_{trip} * I_{0uA} = 0.0866V$
 $I_{ocp-min} = V_{trip} / (R_{ds(on)}(max) * 1.2) + 1/2 \Delta I = 23.471A$
 $I_{ocp-max} = V_{trip} / (R_{ds(on)}(typ) * 1.2) + 1/2 \Delta I = 32.295A$
 $I_{ocp} = 22.4A \sim 30.8A$

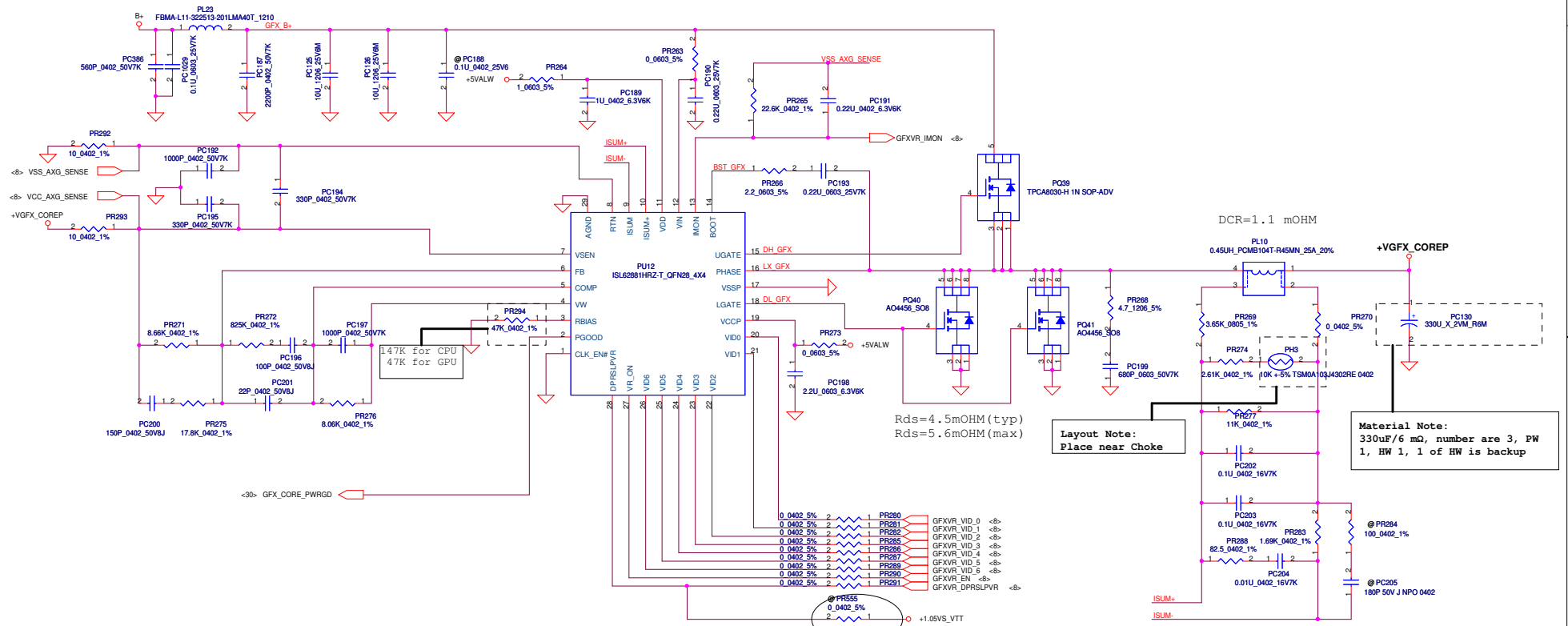
Material Note:
330uF/9 mQ, number
are 3, Power 1, HW 2

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								+1.1VS_VTTP						
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Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 9.66m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A

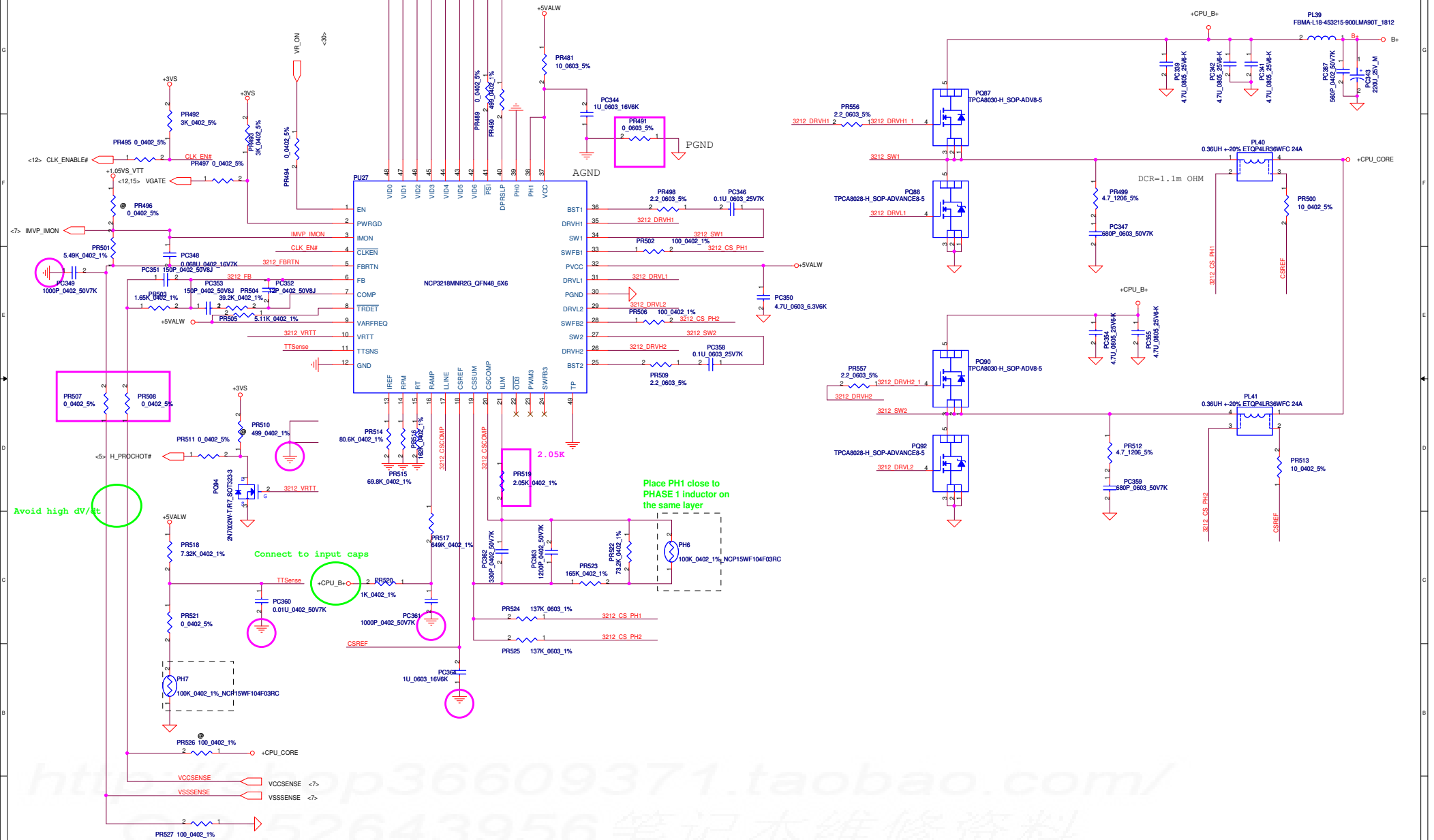
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2009-1214 common circiut modify.

PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Version change list (P.I.R. List)

Page 1 of 2 for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1					Change PR353 from SD034470280 to SD034200380.		
2	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	39	Change PR371 from SD034220280 to SD034470280.		
3					Change PR587 from SD034100380 to SD034470280.		
4	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	38	Change PR590 from SD034200280 to SD034143280.	2010/06/08	to PVT
5	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	40	Change PR591 from SD028470280 to SD028100380.		
6	EMI fail, add 3/5V snubber and Boost Resister to silve it.	EMI request to solve EMI issue.	0.1	38	Add PC1027 SE074222K80 (S CER CAP 2200P 0402 50V7K)		
7					Change PQ111 from SB000006800 to SB301150200		
8	EMI fail, add 1.5V snubber.	EMI request to solve EMI issue.	0.1	42	Add PQ102 and PQ103 SB301150200.	2010/06/08	to PVT
9	EMI fail, add 1.05V snubber. and Boost Resister.	EMI request to solve EMI issue.	0.1	43	Add PR592 SD034200380.		
10					Change PR386 from SD011000080 to SD011100180.	2010/06/08	to PVT
11	EMI fail, add GFX_CORE snubber.	EMI request to solve EMI issue.	0.1	44	Add PR388, PR390, PR391 SD011100180.		
12	HW power sequence modify.	HW request.	0.1	43	Add PD14 SC100001Y80 LL4148_LL34-2		
13					Add PR566 and PR567 SD001470B80 S RES 4.7 1206 5%		
14	BOM unique.	BOM unique.	0.1	38	Add PC1012 and PC1013 SE074681K80 S CER CAP 680P 0402 50V7K	2010/06/08	to PVT
15	EMI request.	EMI request.	0.1	38	Change PR564 and PR565 from SD013000080 to SD013220B80		
16	EMI request.	EMI request.	0.1	44	Add PR415 SD001470B80 4.7 1206 5%.	2010/06/08	to PVT
17	Sourcer request to change a common part.	Sourcer request.	0.1	38	Add PC294 SE025681K80 S CER CAP 680P 50V K X7R 0603		
18	Per sourcer request.	Sourcer request to change PC331 from SE00000R700 to SE026224K80 for common part.	0.1	43	Add PR465 SD001470B80 4.7 1206 5%.		
19	CPU transient issue.	Need modify PC362 to 330P due to transient fail.	0.1	45	Add PC332 SE025681K80 S CER CAP 680P 50V K X7R 0603	2010/06/08	to PVT
20	Per sourcer request.	Per sourcer request.	0.1	43	Change PR461 from SD013000080 to SD013220B80		
21	Cost down.	Cost down 3VALWP and Charger Low Side MOS.	0.1	39	Add PR268 SD001470B80 4.7 1206 5%.	2010/06/08	to PVT
22	Cost down.	Cost down +1.5VP Low side MOS and choke.	0.1	42	Add PC199 SE025681K80 S CER CAP 680P 50V K X7R 0603		
23	Cost down.	re-caculate 1.5VP OCP.	0.1	42	Change PR466 from SD034576280 S RES 1/16W 57.6K +-1% 0402 to SD034806280 S RES 80.6K 0402 1%)	2010/06/08	to PVT
					Change PC331 from SE076104K80 S CER CAP .1U 16V K X7R to SE00000R700 S CER CAP 0.22U 16V K X7R 0402		
					Chnage PQ101 from SB301150000 to SB301150200.	2010/06/08	to PVT
					Add PC1028 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
					Add PC1029 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
					Change PC1019 from SE00000GC00 S CER CAP 2.2U 10V K X7R 0603 to SE000003H00 S CER CAP 2.2UF 10V K X5R 0603	2010/06/08	to PVT
					change PC331 from SE00000R700 to SE026224K80	2010/06/08	to PVT
					Change PC362 from SE074561K80 S CER CAP 560P 50V K X7R 0402 to SE074331K80 S CER CAP 330P 50V K X7R 0402	2010/06/08	to PVT
					Chnage PQ39/PQ82 from SB000008L80 to SB00000HL00.	2010/06/08	to PVT
					Change PQ98 from SB00000AJ00 to SB000009580 (AO4468).	2010/06/08	to PVT
					Change PQ64 from SB00000CG00 to SB000009580 (AO4468).		
					Chnage PQ74 from SB000009F80 to SB00000AJ00 (AO4712).	2010/06/08	to PVT
					Chnage PL32 from SH000009U00 to SH000009680.		
					Change PR417 from SD034110280 to SD034182280.	2010/06/08	to PVT

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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Cost down.	re-caculate +3VALWP OCP.	0.1	38	Change PR562 from SD034107380 to SD034137380.	2010/06/08	to PVT
25							
26							
27							
28							
29							
30							
31							
32							
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				Size Custom	Document Number
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Version change list (P.I.R. List)

Item	Phase	PAGE	DATE	Modifycatio list	Purpose
1	EVT		04 / 08 04 / 16 04 / 21 04 / 26 04 / 27 04 / 29 04 / 29 05 / 03 05 / 03 05 / 06 05 / 07 05 / 10 05 / 11 05 / 12 05 / 13	N/A Modify RTC SCH Change LAN to AR8152 Update Power SCH Update AND Gate symbol - U1 / U2 / U6 / U7 / U19 Update Power MOS symbol - U24 / U25 / U26 C196 change to 1U for INTEL design CLK GEN del C35 / C36 / C30 / C31 / C32 / C33 / C34 / L3 (for 3G@ and @ function) Q4+Q6 change to 2N7002DW Update U8 symbol Add DMIC function Modify USB define. Update Power SCH Add R17 for DMIC power Update Power SCH Change LAN to GIGA&10/100 co-lay Del R307 (LVDS conn.) Change +1.05VS VTT to +1.05VS (CLK GEN) Change C842 / C850 / C854 / C656 to SE080105K80 1U_0603_10V6K Change R940 to 28K (S3 Power sequence) SW 1 bin define (LAN) Change R907 (O_0603) to O_1206 5% Remove C40 / C41 / C42 / C43 / C44 Change FAN Conn. Update Power SCH Change LAN to BCM57780 GIGA Del R637 / R639 / R640 / R645 / R647 / R648 (AUDIO) Del DMIC Update Power SCH Update Power SCH Add C49 / C50 (EC B+) Update Power SCH C764 / C765 change to 18P 0402_50V8J (EC) Reserve D13 / D24 / D30 (ESB) U17 change to RTS5137 (SA000043500) Card reader Update Power SCH	
			06 / 01 06 / 02 06 / 03 06 / 04 06 / 10	Unpop L11 / C247 & Pop R304 for cost down Unpop C764 / X2 & Pop R13 & C765 Change to 100K for EC remove Crystal Pop R834 & R835 change to 200K for Project ID Unpop D24 / D30 Unpop R690 / R691 Pop C49 / C50 For HDMI Unpop R753 / R757 , Add R754 / R758 to 0 ohm. Change R759 to 3.9K. Change R755 to 4.7K ohm , Unpop R748. Unpop R778. R833 / R292 0.0805 change to 0.0603. C190 / C191 & C1135 / C1136 change to 33P 0402 50V8J for Vender test report Unpop C774~C799 for EMI cost down. Update Power SCH Add T25 / T26 / T27	
			07 / 07 07 / 08	Update Power SCH Change R759 to 4.32K_1% SD00000J280	

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				Date: Thursday, July 08, 2010	Rev 1.0
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