

Compal Confidential

PAV70 Schematics Document

Intel Pineview Processor with Tigerpoint + DDRII

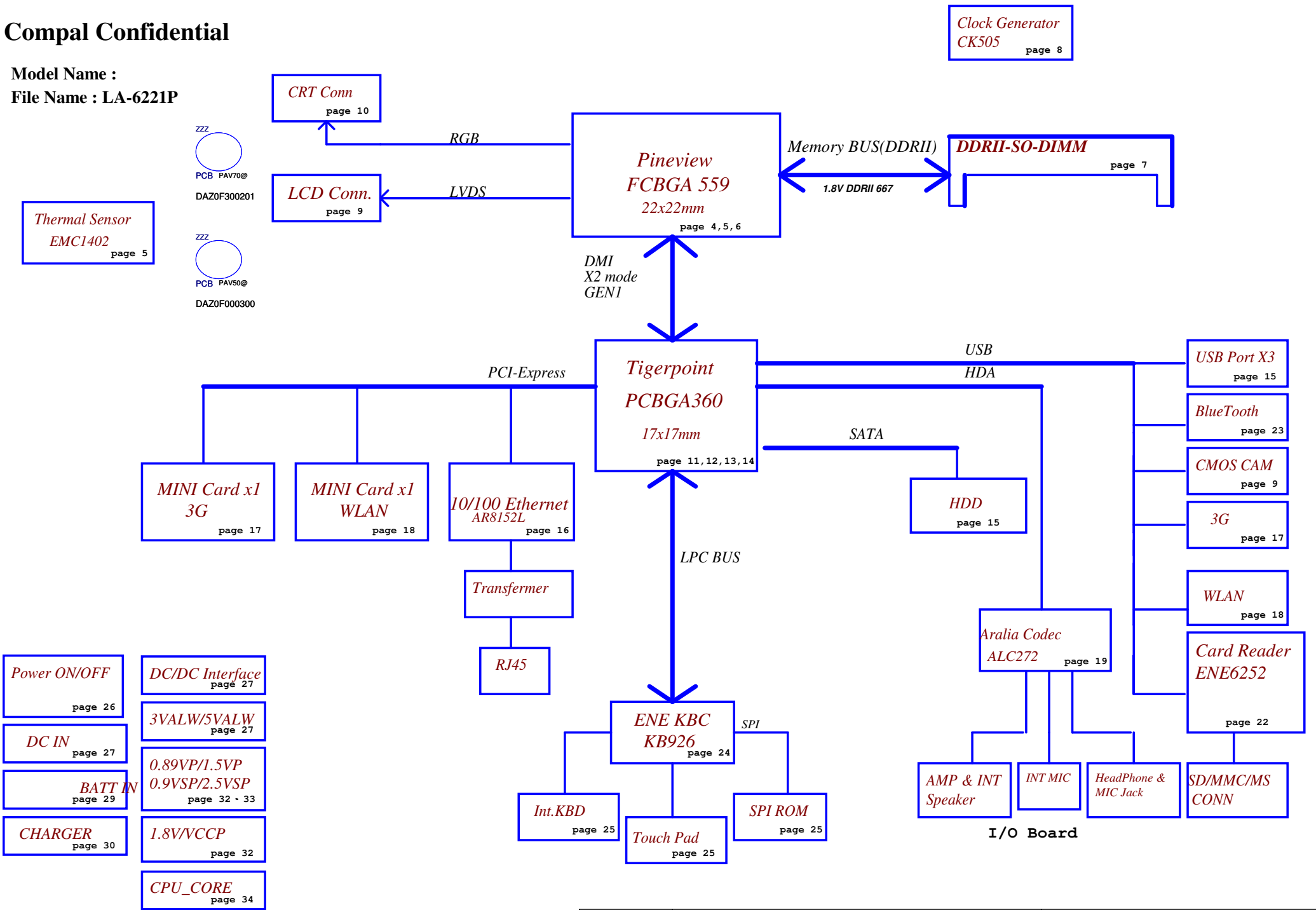
2010-07-01

REV: 1.0

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Model Name :
File Name : LA-6221P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89V	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 17)

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0 (EVT)	0	0 V	0 V	0 V
1 (DVT)	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2 (PVT)	18K +/- 5%	0.436 V	0.503 V	0.538 V
3 (MP)	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	100_1100

Tiger Point SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

USB table

EHCI1	UHCI1	Port0	MB USB Conn1.
		Port1	MB USB Conn2.
	UHCI2	Port2	MB USB Conn3.
		Port3	CMOS
EHCI2	UHCI3	Port4	Card Reader
		Port5	WWAN
	UHCI4	Port6	BT
		Port7	WLAN
	UHCI5	Port8	
		Port9	
	UHCI6	Port10	
		Port11	

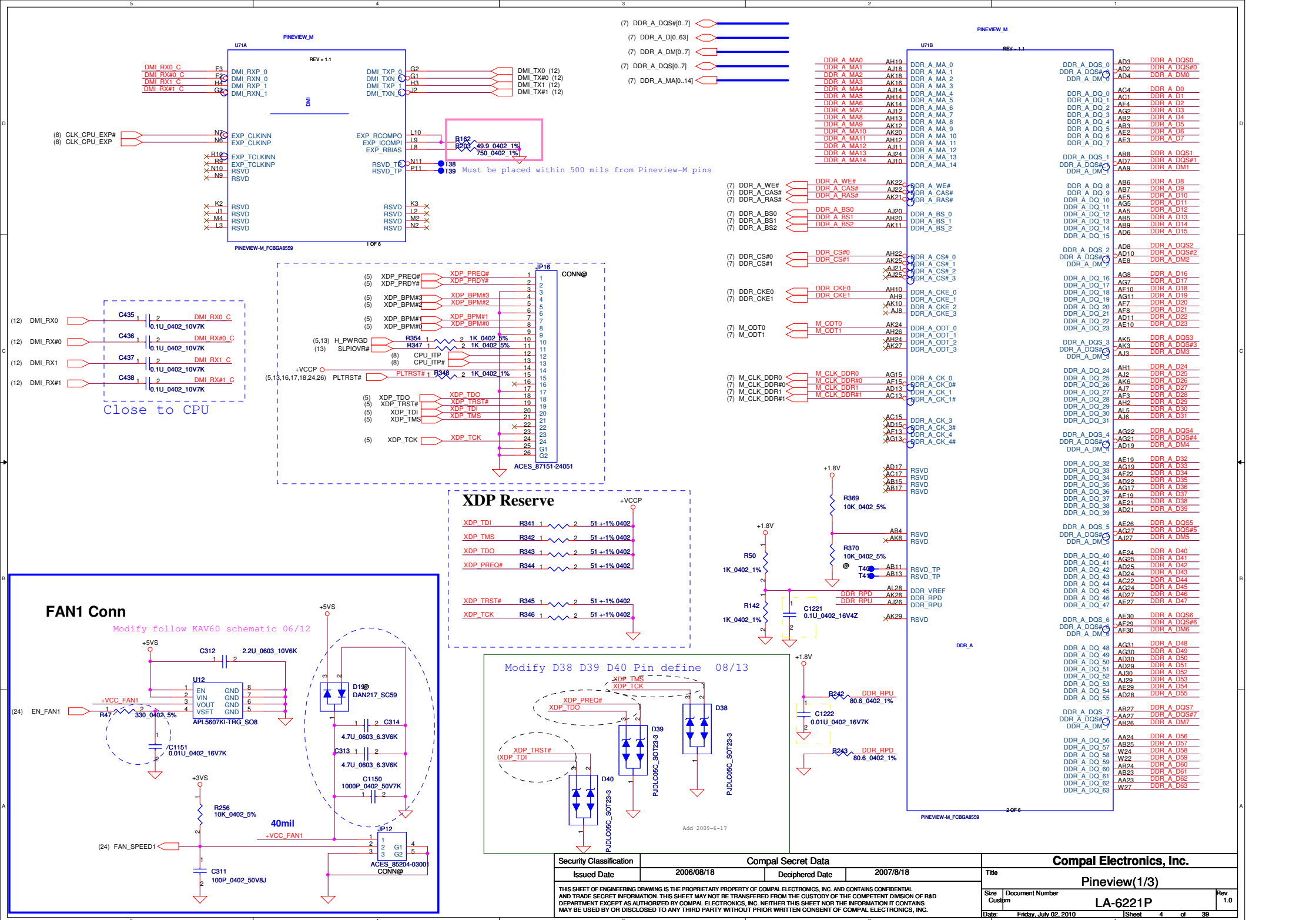
PCIE table

PCIE port1	LAN
PCIE port2	Wireless Card
PCIE port3	3G
PCIE port4	
PCIE port5	
PCIE port6	

SATA table

SATA port0	HDD
SATA port1	
SATA port2	
SATA port3	
SATA port4	
SATA port5	

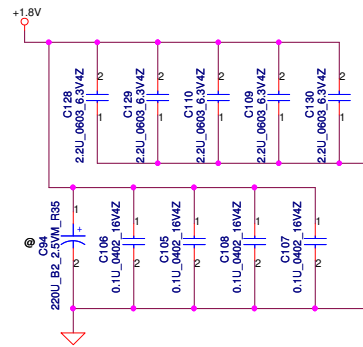
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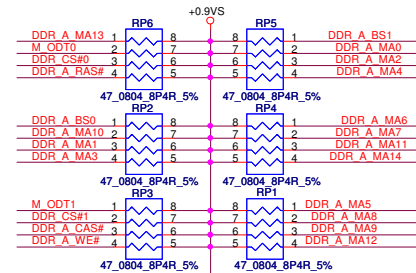
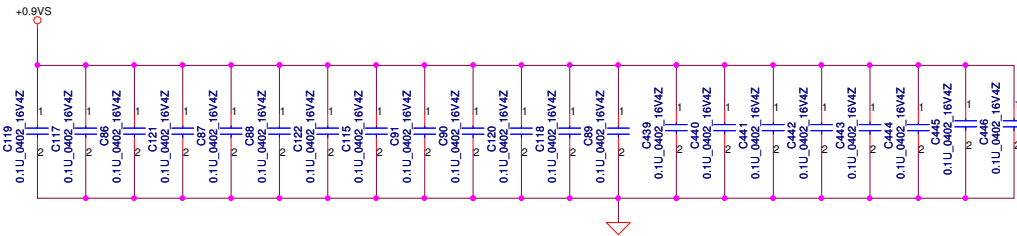
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- (4) DDR_A_DQS[0..7]
(4) DDR_A_D[0..63]
(4) DDR_A_DM[0..7]
(4) DDR_A_DQS[0..7]
(4) DDR_A_MA[0..14]

Layout Note:
Place near JDIM1

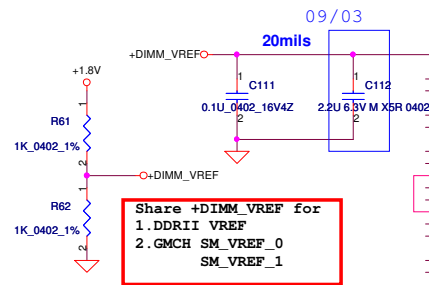


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely DIMMA, all trace length<750 mll

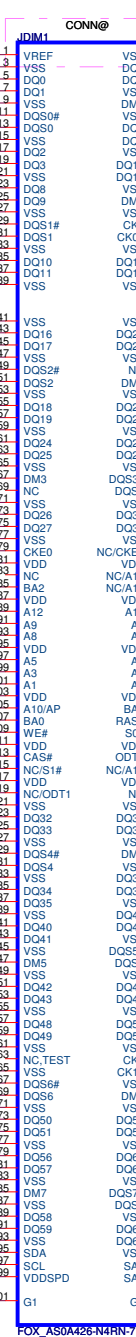
Layout Note:
Place these resistor closely DIMMA, all trace length Max=1.3"



Share +DIMM_VREF for
1.DDRII VREF
2.GMCH SM_VREF_0
SM_VREF_1

- (4) DDR_CKE0
(4) DDR_A_BS2
(4) DDR_A_BS0
(4) DDR_A_WE#
(4) DDR_A_CAS#
(4) DDR_CS#1
(4) M_ODT1

- DDR A D0
DDR A D1
DDR A DQS#0
DDR A DQS0
DDR A D2
DDR A D3
DDR A D8
DDR A D9
DDR A DQS#1
DDR A DQS1
DDR A D10
DDR A D11
DDR A D16
DDR A D17
DDR A DQS#2
DDR A DQS2
DDR A D18
DDR A D19
DDR A D24
DDR A D25
DDR A DM3
DDR A D26
DDR A D27
DDR_CKE0
DDR_A_BS2
DDR_A_MA12
DDR_A_MA9
DDR_A_MA8
DDR_A_MA5
DDR_A_MA3
DDR_A_MA1
DDR_A_MA10
DDR_A_BS0
DDR_A_WE#
DDR_A_CAS#
DDR_CS#1
M_ODT1
DDR A D32
DDR A D33
DDR A DQS#4
DDR A DQS4
DDR A D34
DDR A D35
DDR A D40
DDR A D41
DDR A DM5
DDR A D42
DDR A D43
DDR A D48
DDR A D49
DDR A DQS#6
DDR A DQS6
DDR A D50
DDR A D51
DDR A D56
DDR A D57
DDR A DM7
DDR A D58
DDR A D59
CLK_SMBDATA
CLK_SMBCLK



Change to SP07F001720 04/30

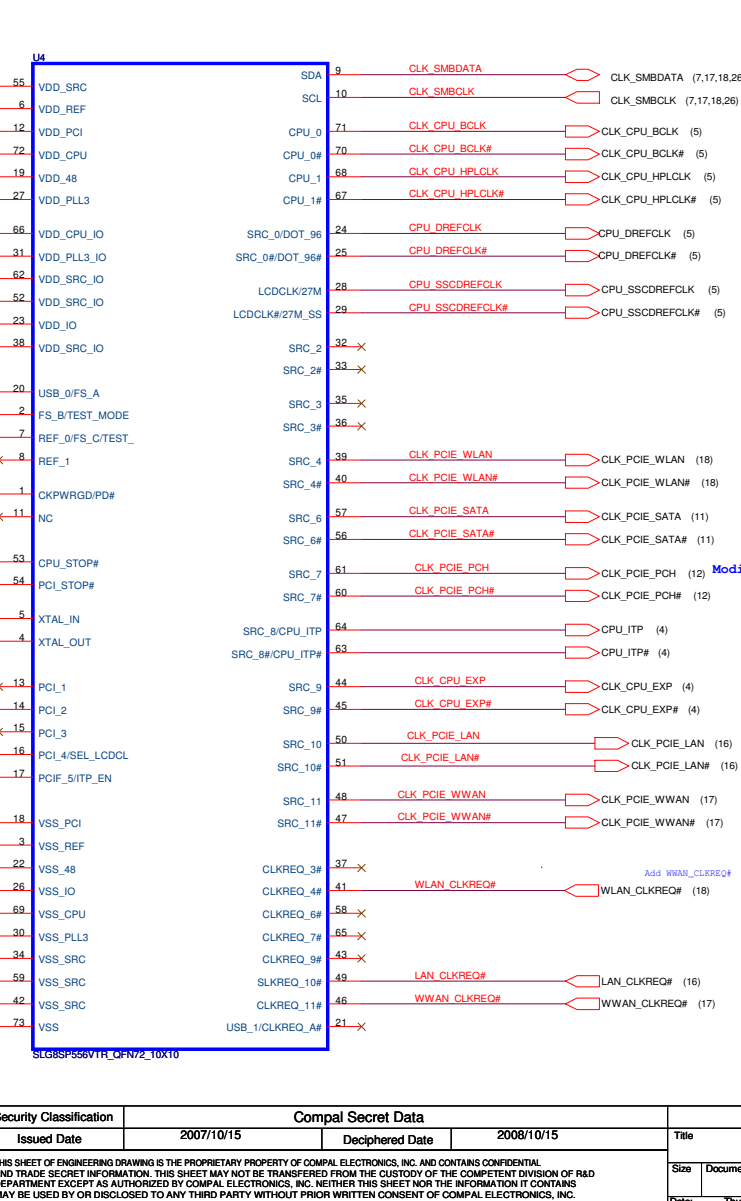
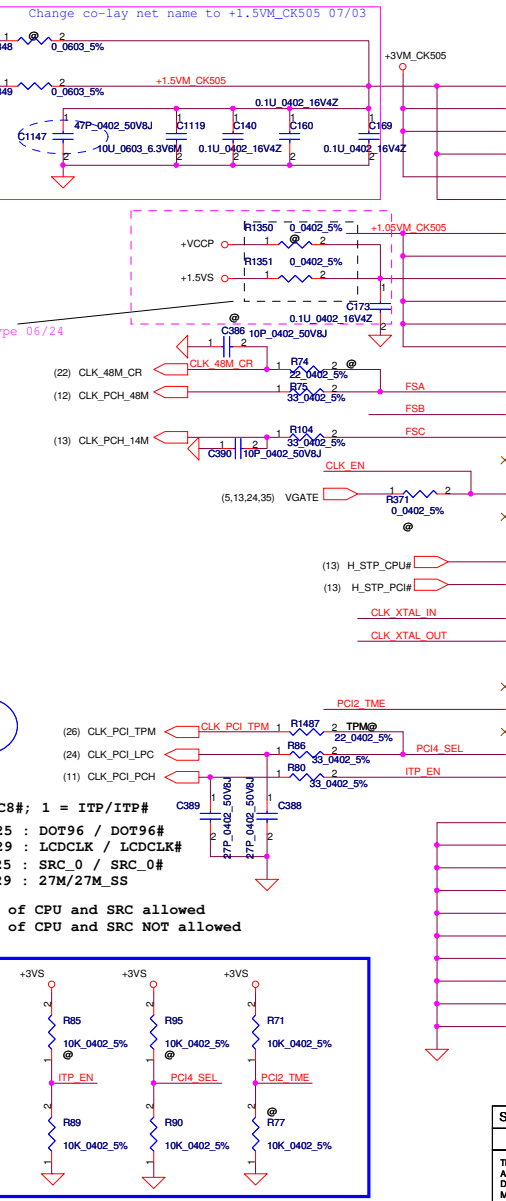
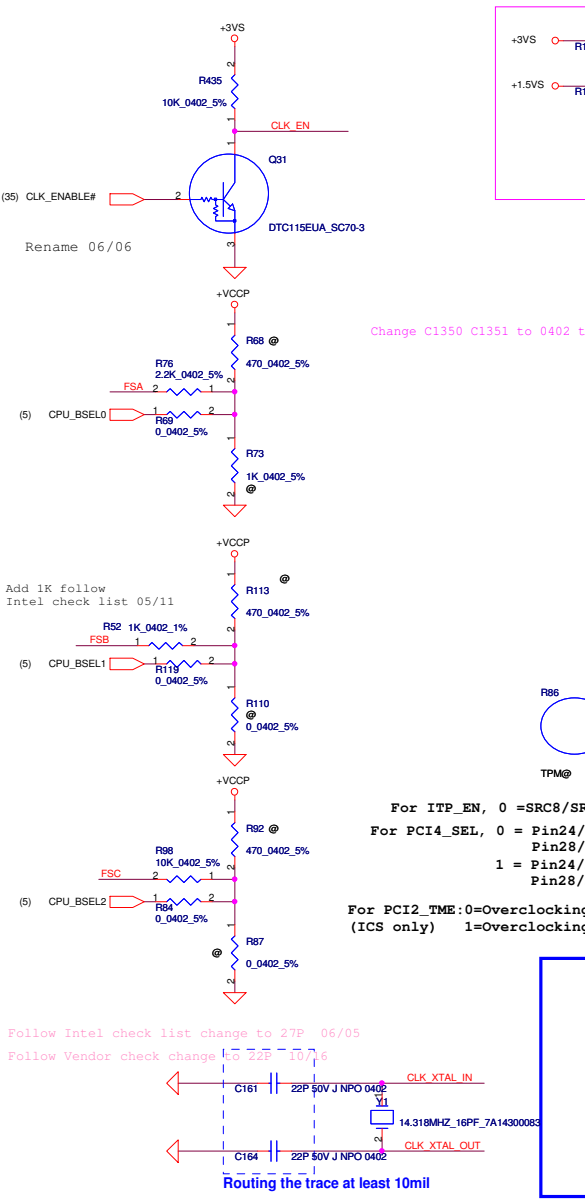
- DDR A D4
DDR A D5
DDR A DM0
DDR A D6
DDR A D7
DDR A D12
DDR A D13
DDR A DM1
M_CLK_DDR0
M_CLK_DDR#0
DDR A D14
DDR A D15
DDR A D20
DDR A D21
DDR A DM2
DDR A D22
DDR A D23
DDR A D28
DDR A D29
DDR A DQS#3
DDR A DQS3
DDR A D30
DDR A D31
DDR_CKE1
DDR_A_MA14
DDR_A_MA11
DDR_A_MA7
DDR_A_MA6
DDR_A_MA4
DDR_A_MA2
DDR_A_MA0
DDR_A_BS1
DDR_A_RAS#
DDR_CS#0
M_ODT0
DDR_A_MA13
DDR A D36
DDR A D37
DDR A DM4
DDR A D38
DDR A D39
DDR A D44
DDR A D45
DDR A DQS#5
DDR A DQS5
DDR A D46
DDR A D47
DDR A D52
DDR A D53
M_CLK_DDR1
M_CLK_DDR#1
DDR A DM6
DDR A D54
DDR A D55
DDR A D60
DDR A D61
DDR A DQS#7
DDR A DQS7
DDR A D62
DDR A D63
M_CLK_DDR1
M_CLK_DDR#1
DDR A DM6
DDR A D54
DDR A D55
DDR A D60
DDR A D61
DDR A DQS#7
DDR A DQS7
DDR A D62
DDR A D63

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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								

Add C1145 C1146 C1147 for EMI 06/12

Low Power (Silego : SA00003H730) IDT SA00003H610

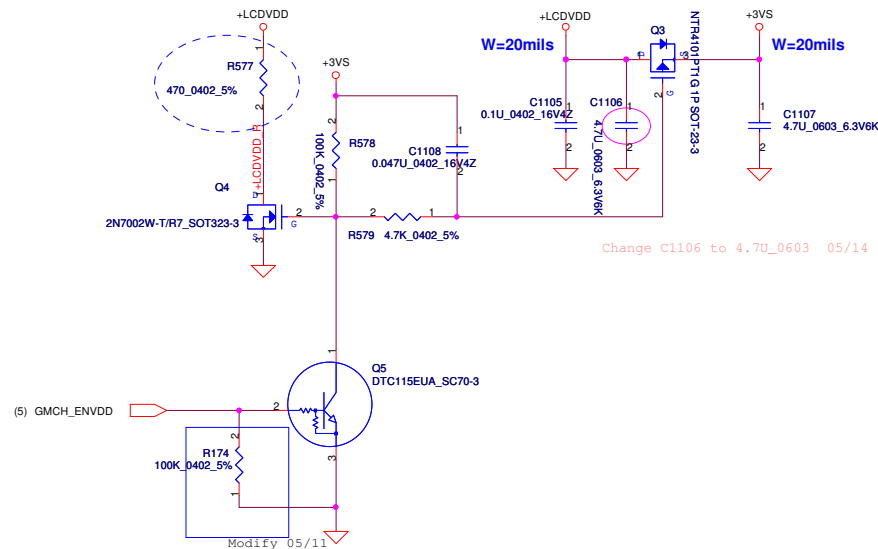


PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	PCIE_WWAN

PORT	DEVICE
REQ_3#	
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	PCIE_LAN
REQ_11#	PCIE_WWAN
REQ_A#	

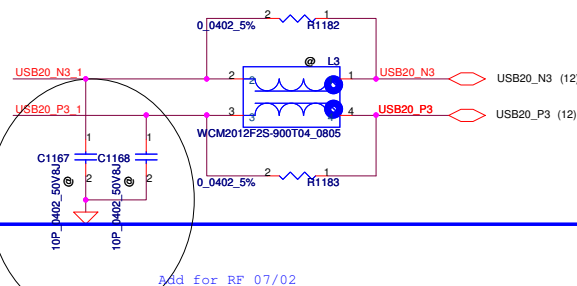
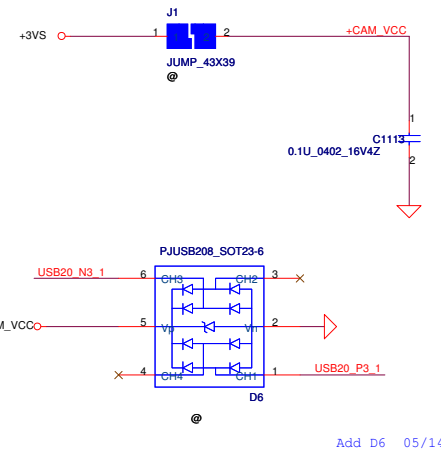
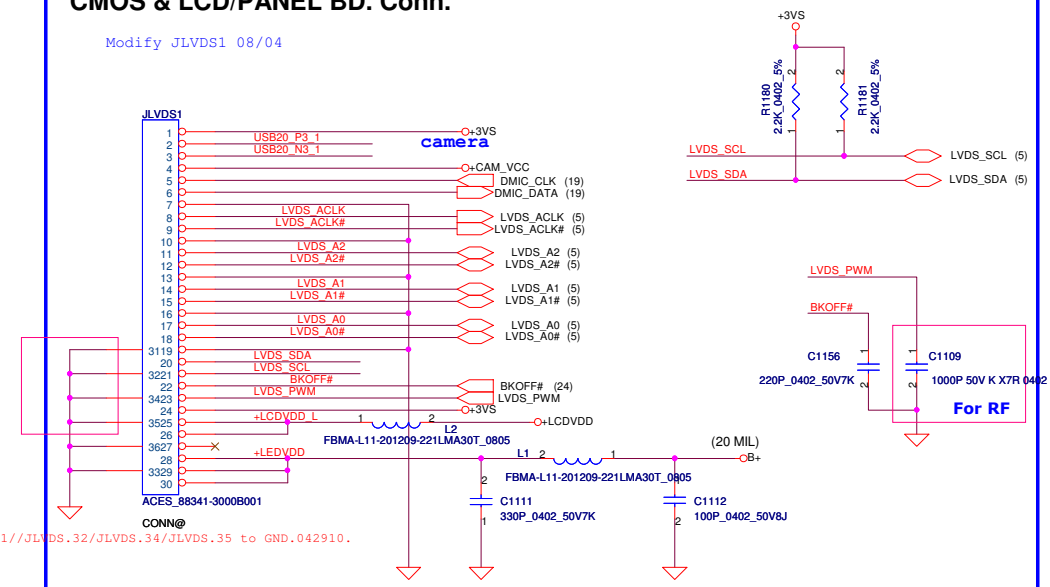
LCD POWER CIRCUIT

Change R577 to 0402 SIZE 06/16

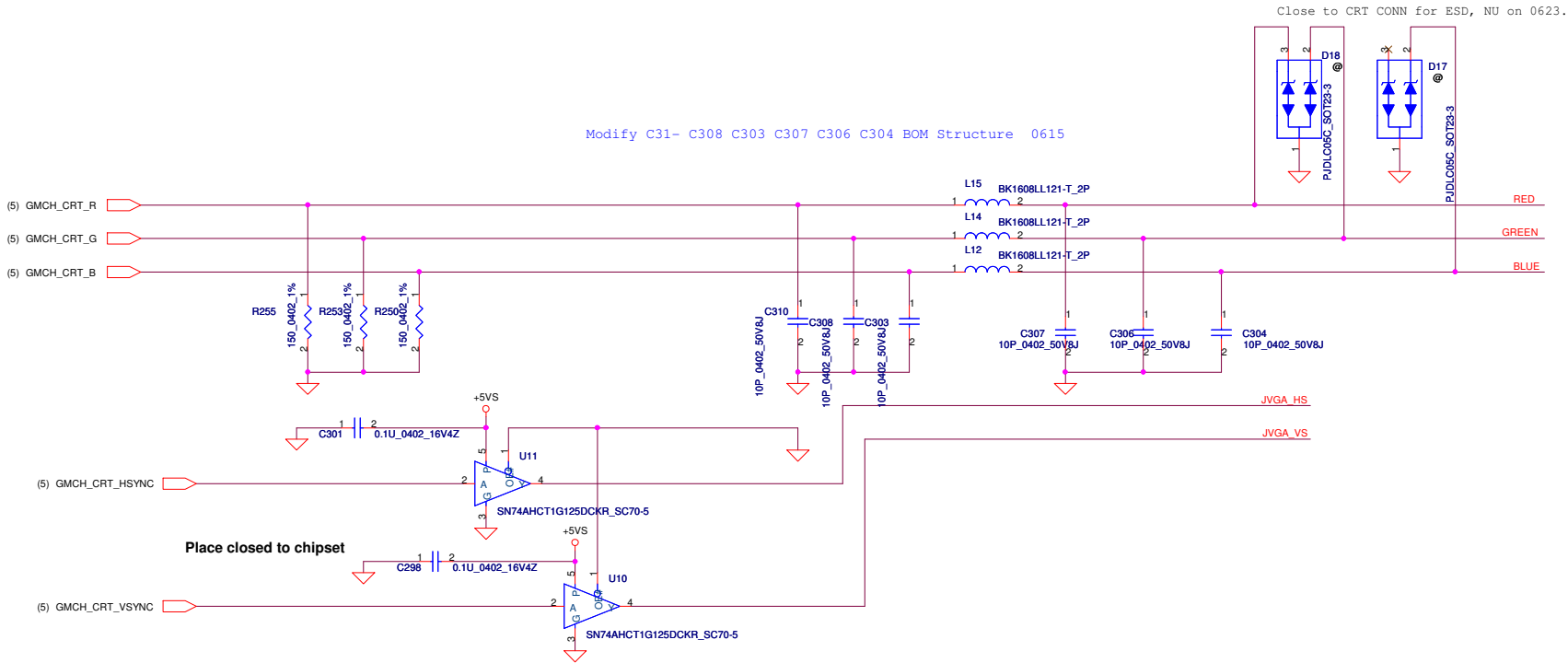


CMOS & LCD/PANEL BD. Conn.

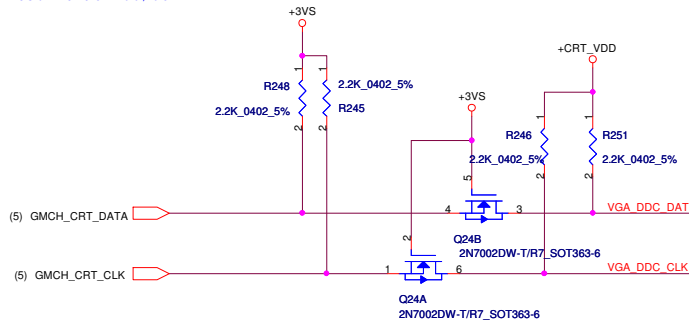
Modify JLVDS1 08/04



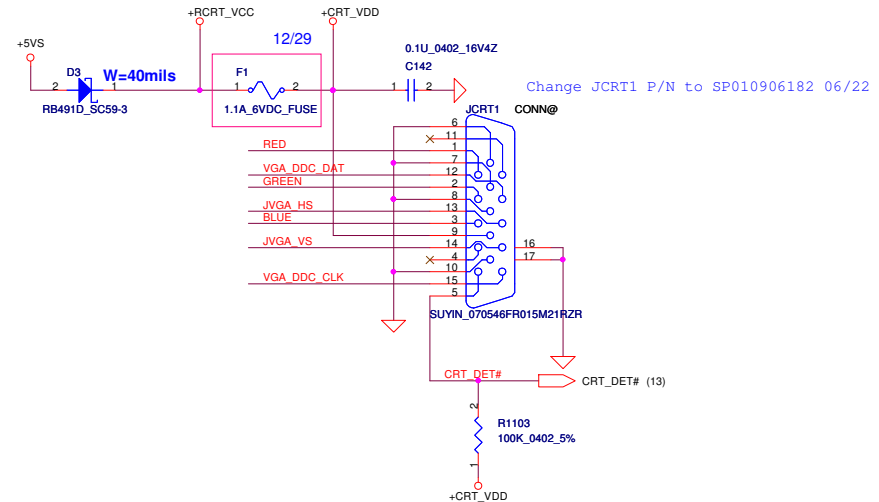
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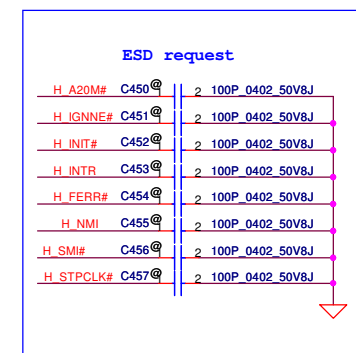
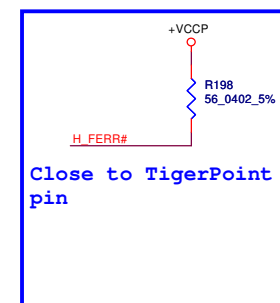
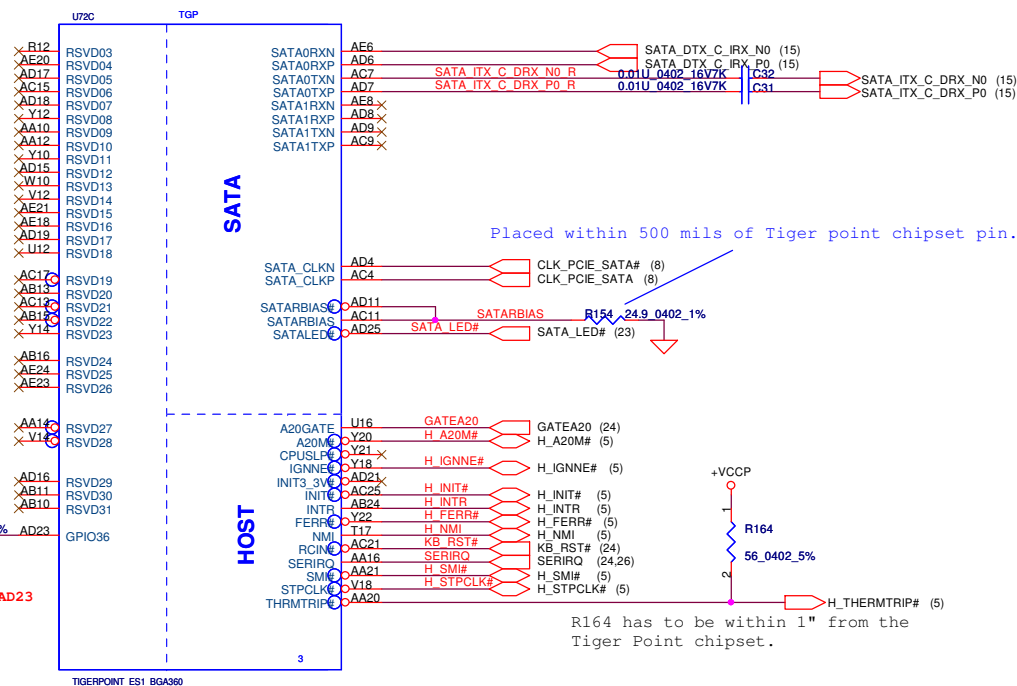
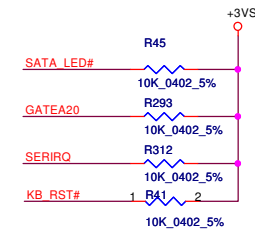
Add R1283 R1284
Change R247 R249 to 10 ohm
Add @ on U10 U11 C301 C298 06/08



CRT PORT



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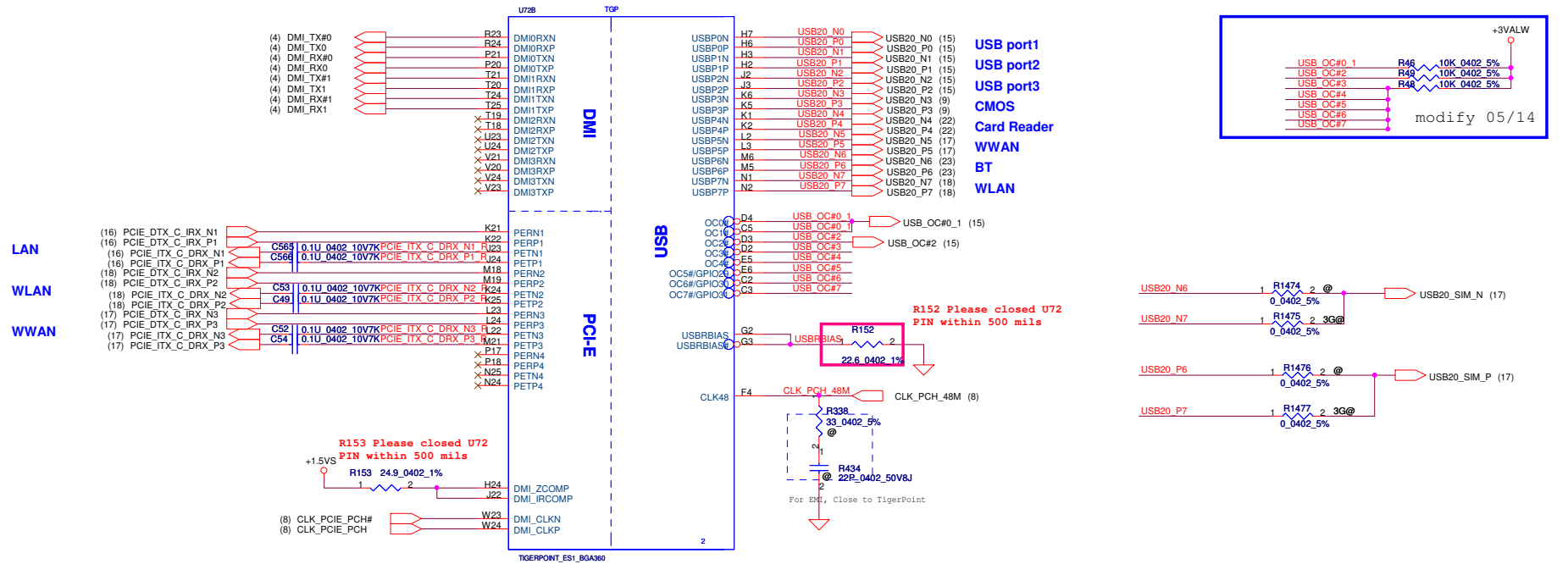


STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC

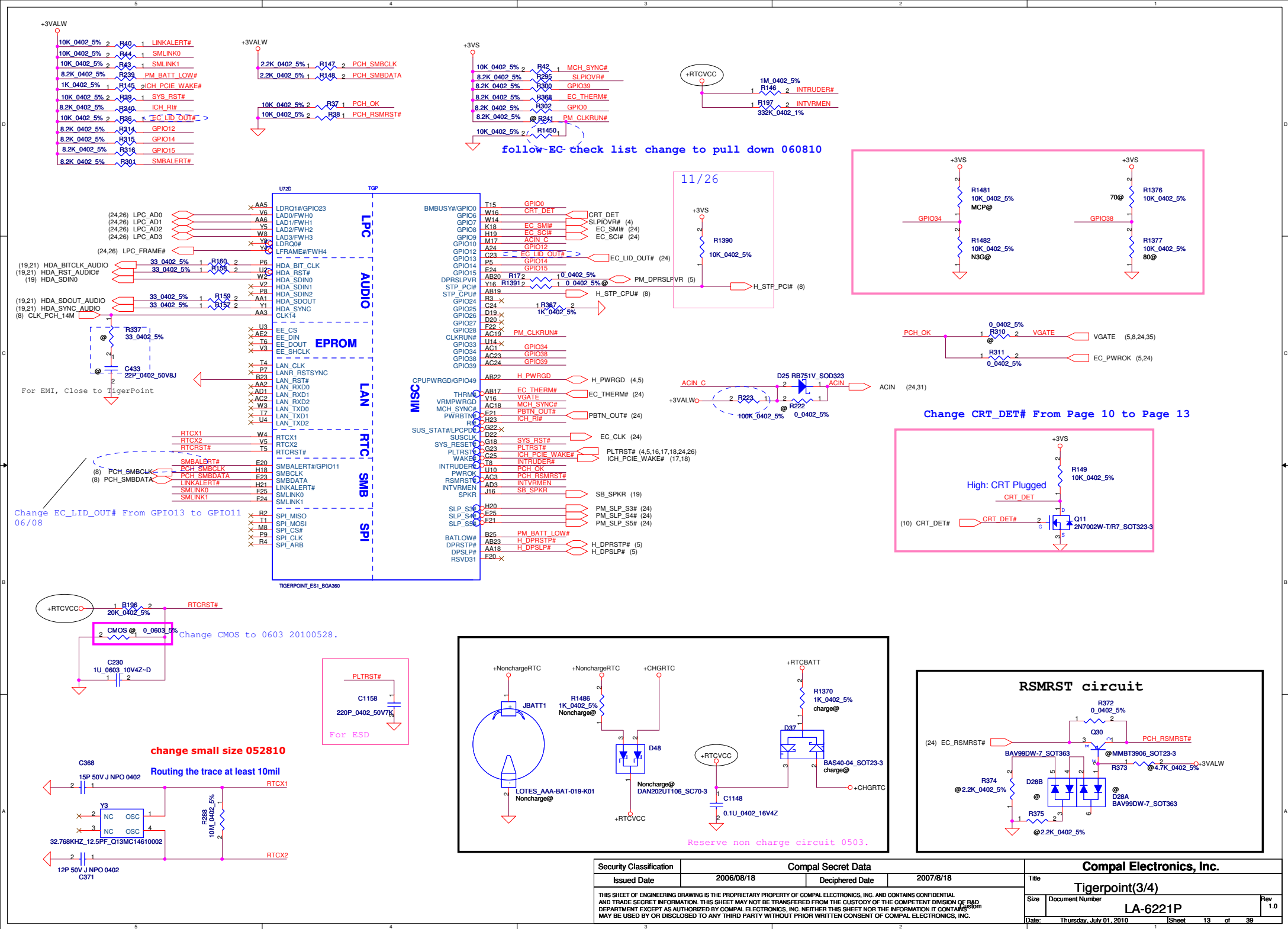
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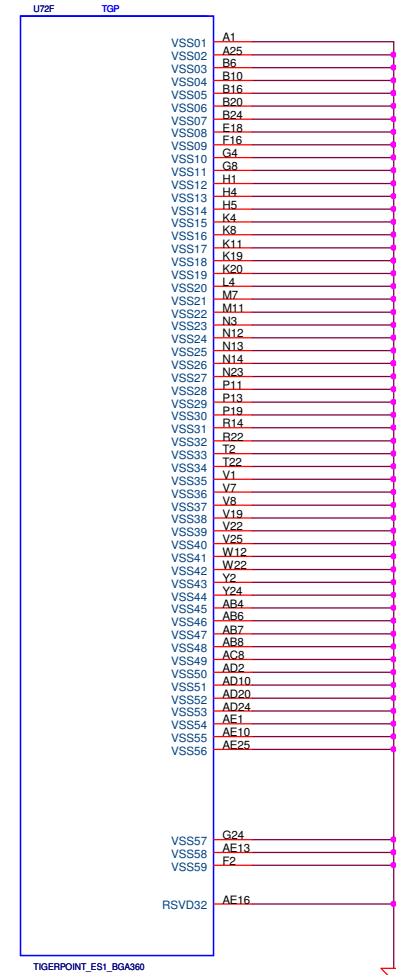
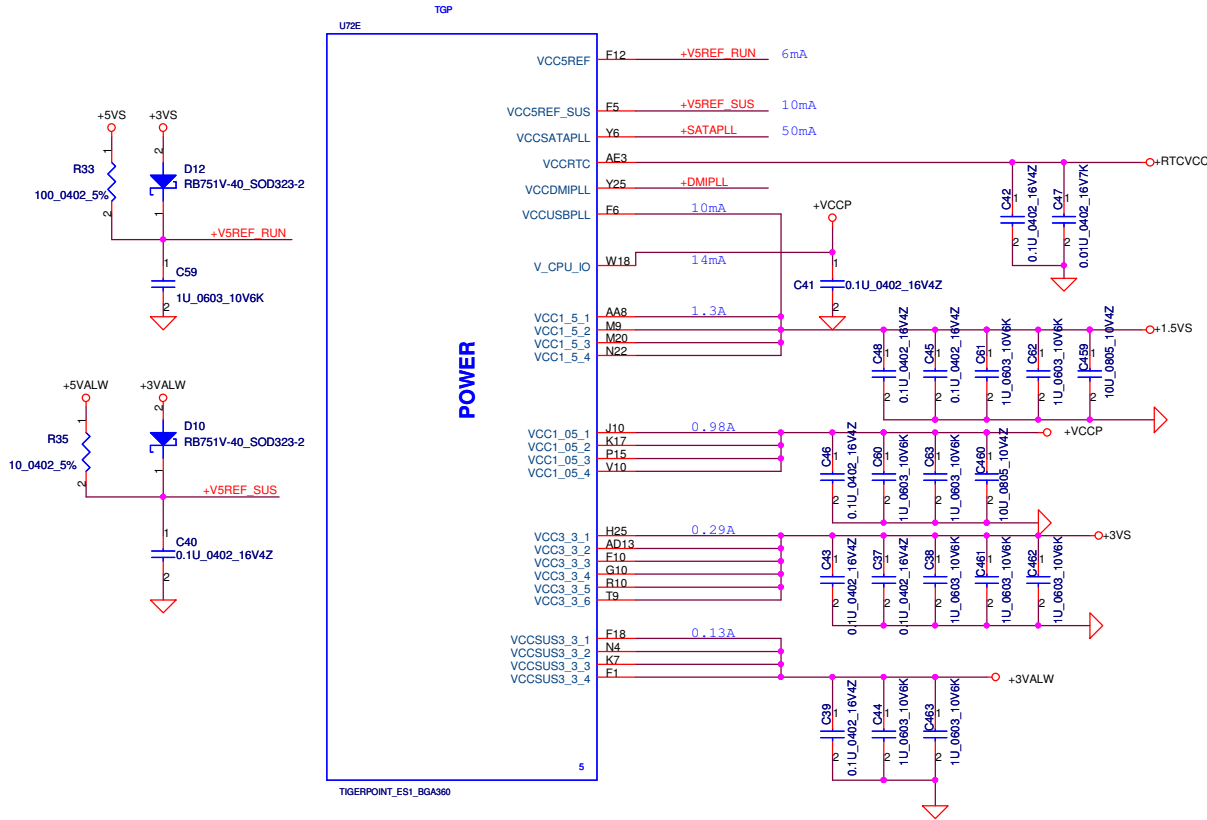
PCIe Port List	
1	LAN
2	WLAN
3	WWAN
4	

USB Port List	
0	USB Left1
1	USB Left2
2	USB Right2
3	CMOS
4	CardReader
5	WWAN
6	BT
7	WIMAX

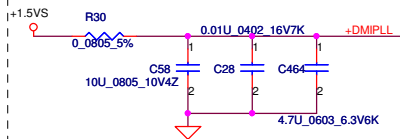


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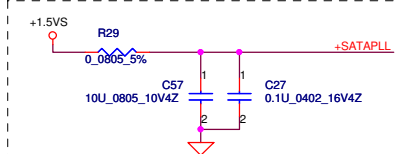




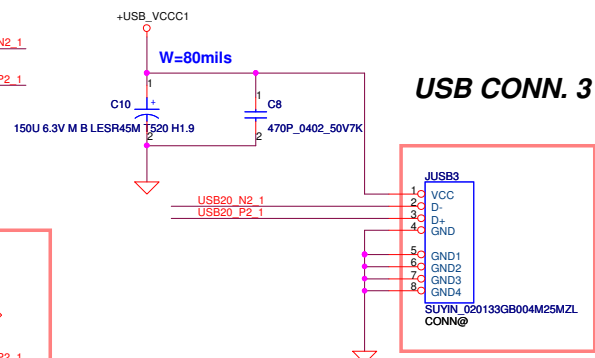
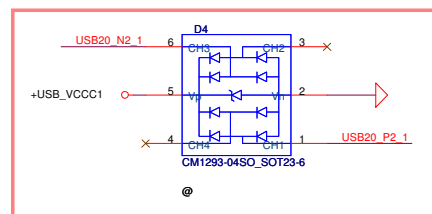
Place closely pin Y25 within 100mils.



Place closely pin Y6 within 100mils.

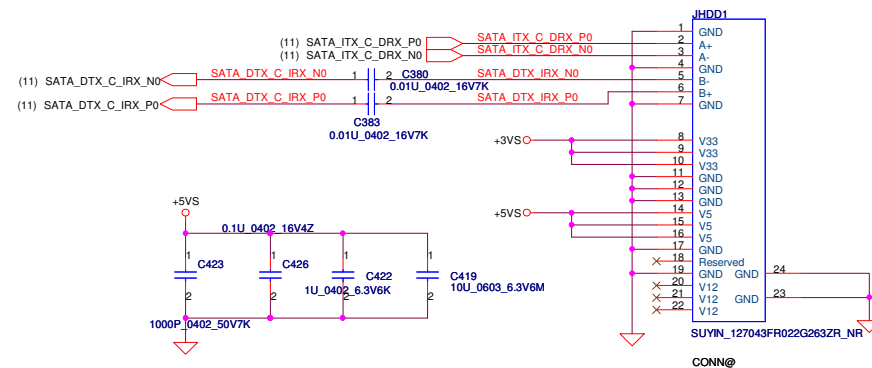


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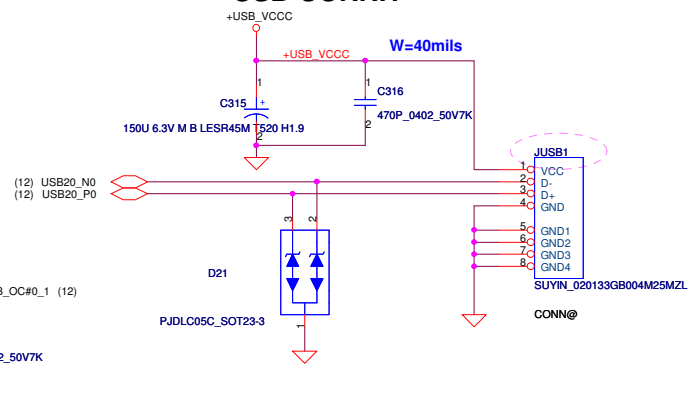
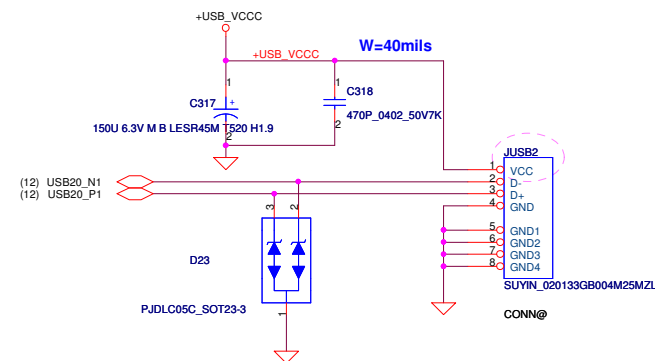


5/12 Revised USB connector
6/23 Update USB connector

SATA HDD Conn.

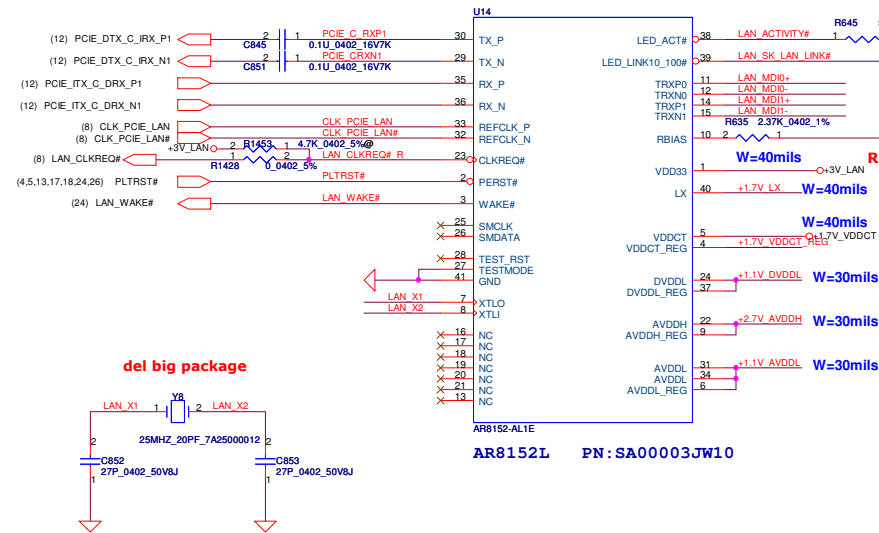
**USB CONN.1**

Change JUSB1 JUSB2 to NEW P/N SP010906181 06/23

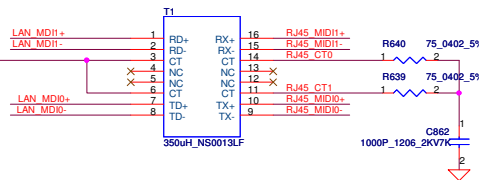
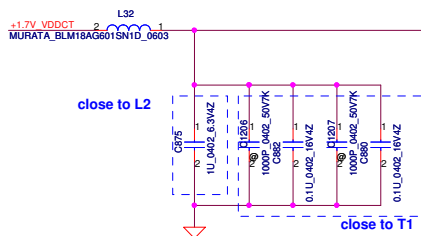
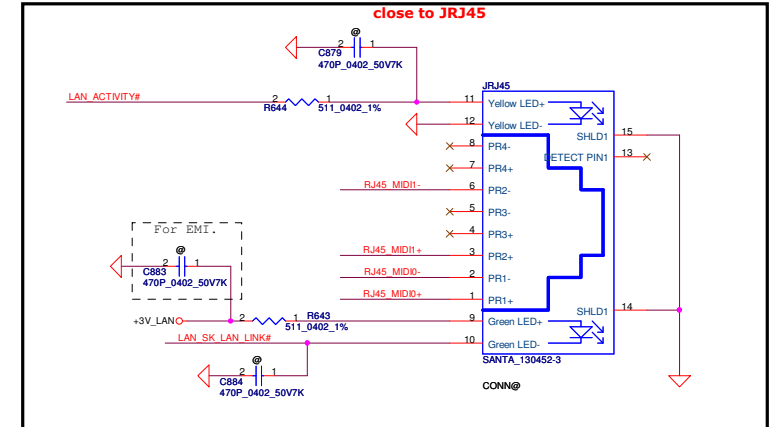
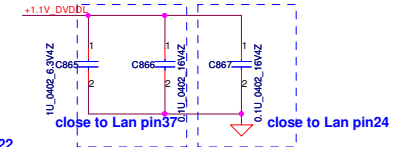
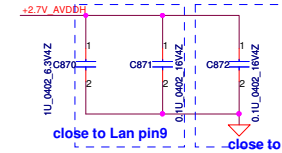
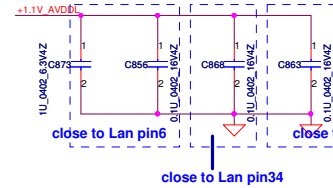
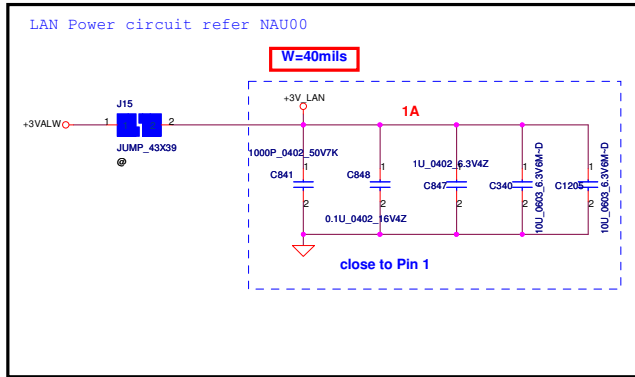
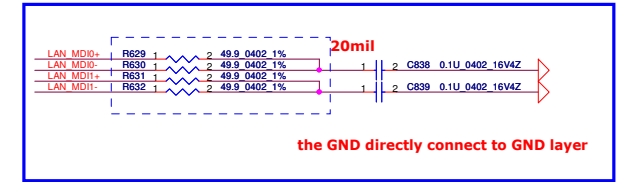
**USB CONN.2**

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				LA-6221P	
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Change LAN chip to AR8152-L for NAV70/80 DDR3 2010/01/22

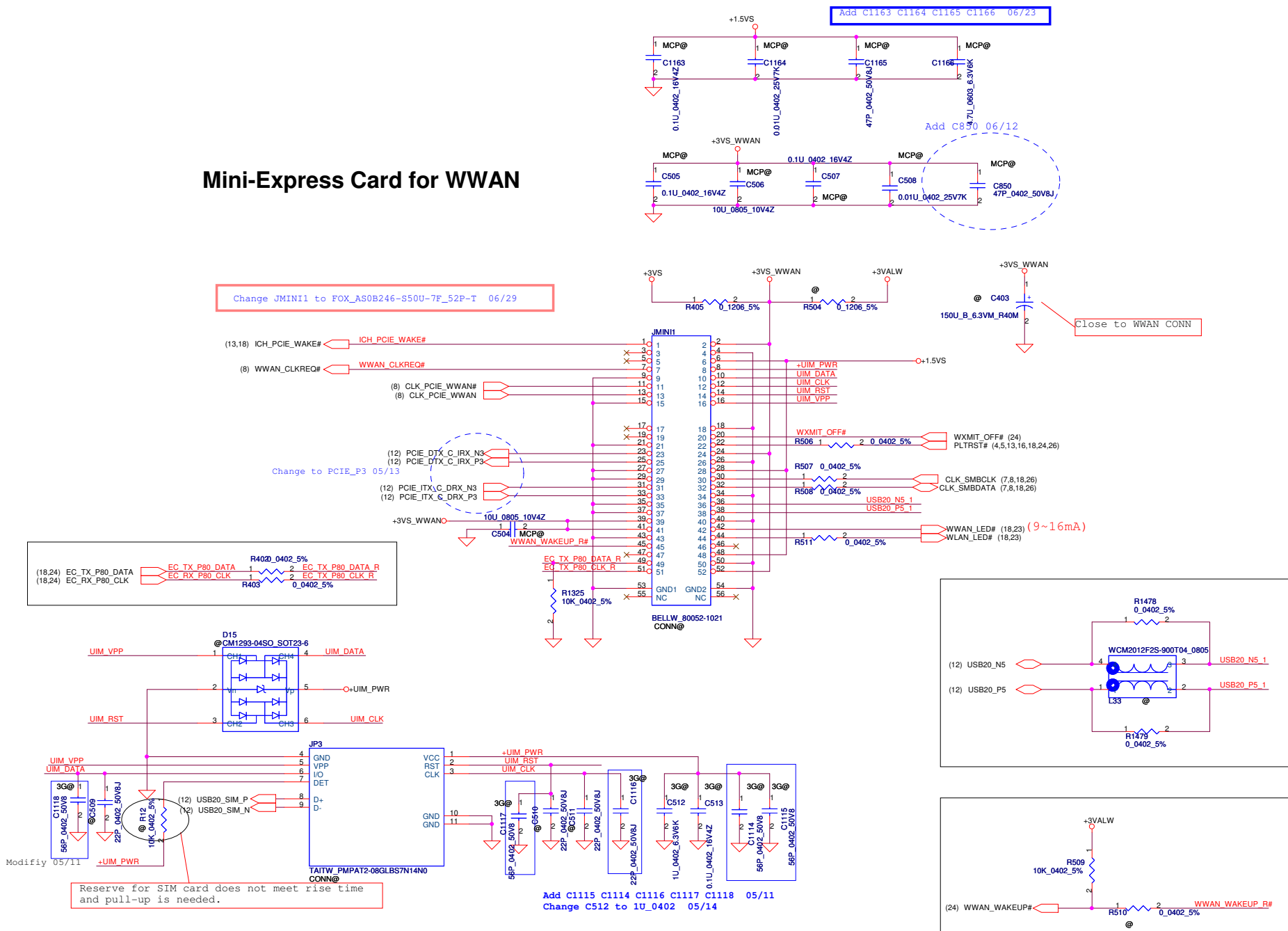


Switch mode:由+1.7V_LX供給+VDDCT pin39 need to pull high resistor of 5.1k
LDO mode:由+1.7V_VDDCT_REG供給+VDDCT pin39 need to pull low resistor of 5.1k



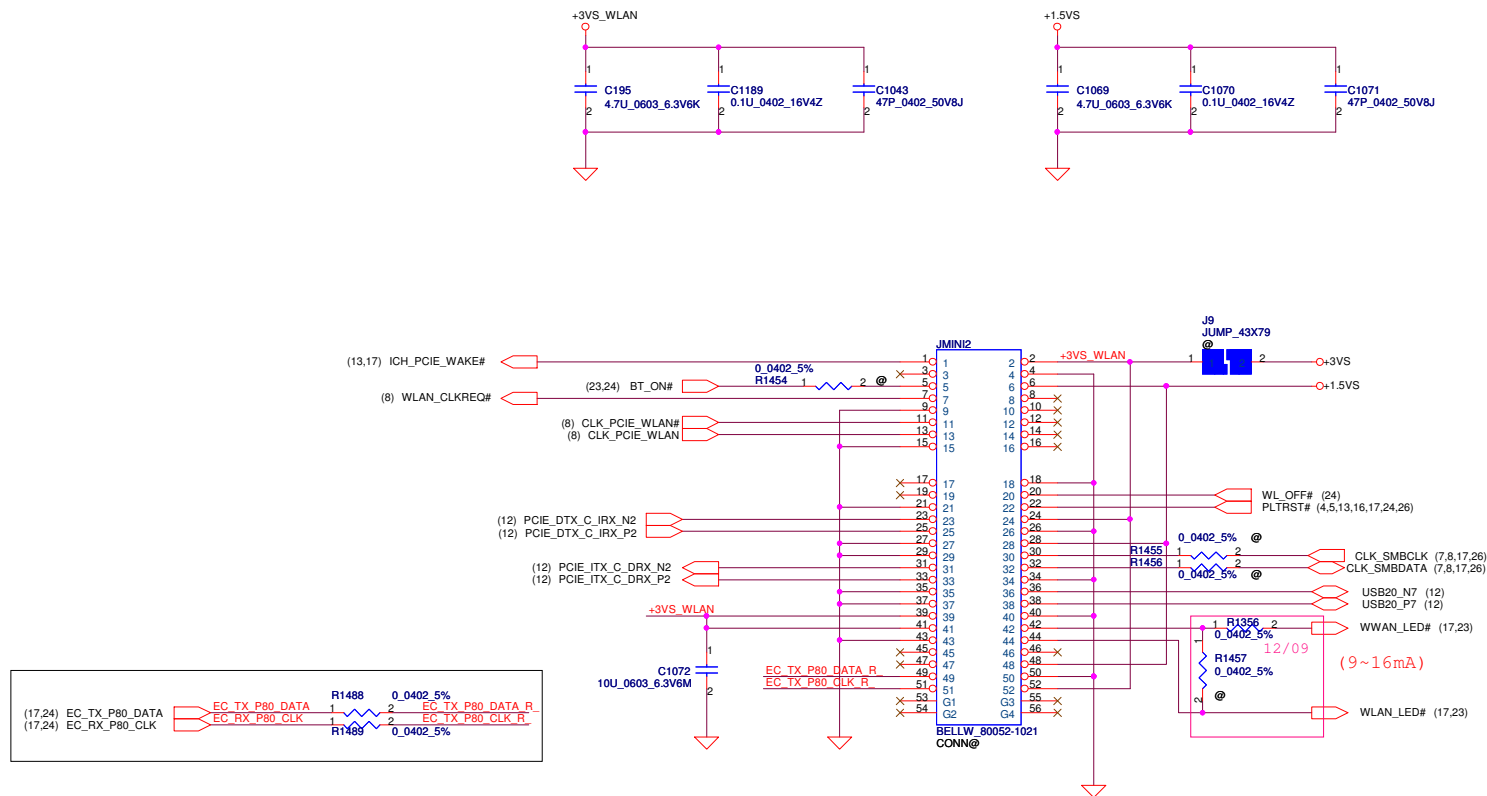
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/7/7	Deciphered Date	2010/7/7	Title
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Size	Custom	Document Number	LA-6221P	Rev
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Mini-Express Card for WWAN

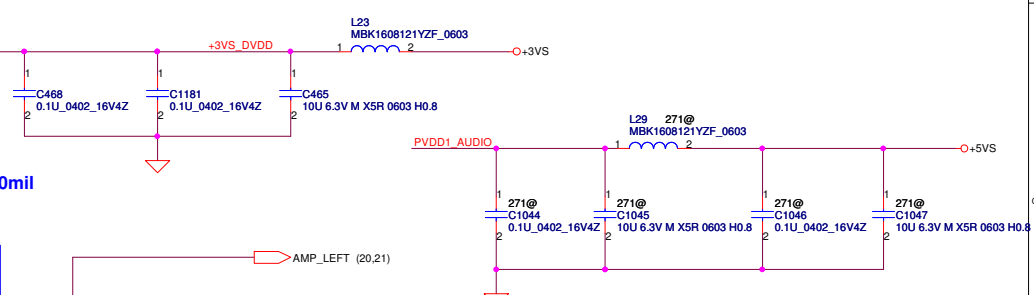
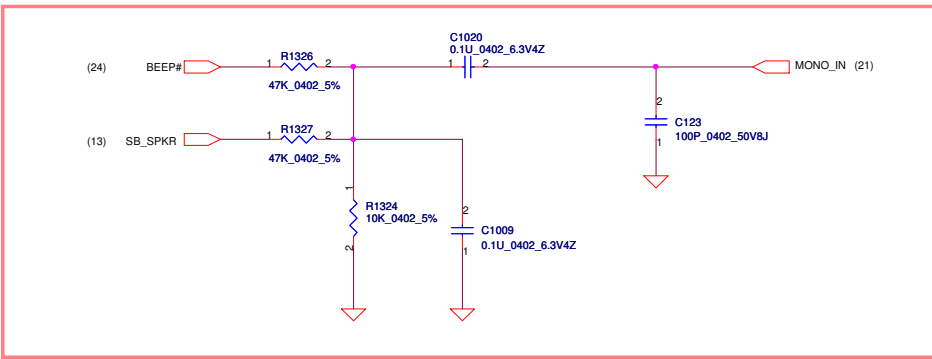


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Issued Date	2006/08/05	Deciphered Date	2007/8/18	Title	Mini-Card
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				Date:	Thursday, July 01, 2010
				Sheet	17 of 39
				Rev	0.2
				LA-6221P	

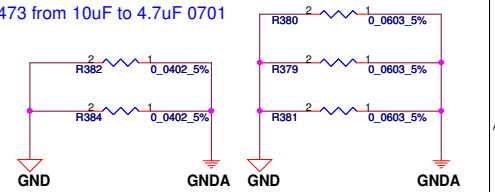
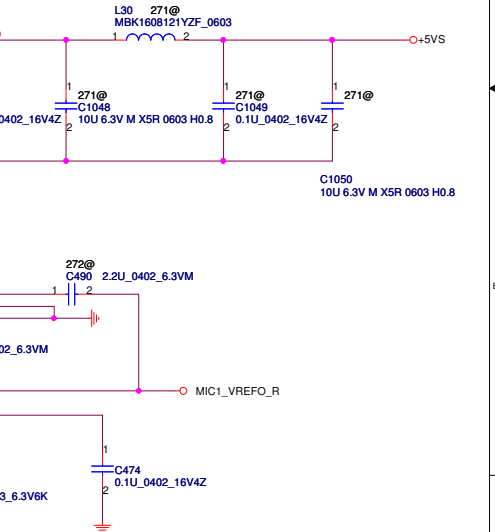
Mini-Express Card for WLAN



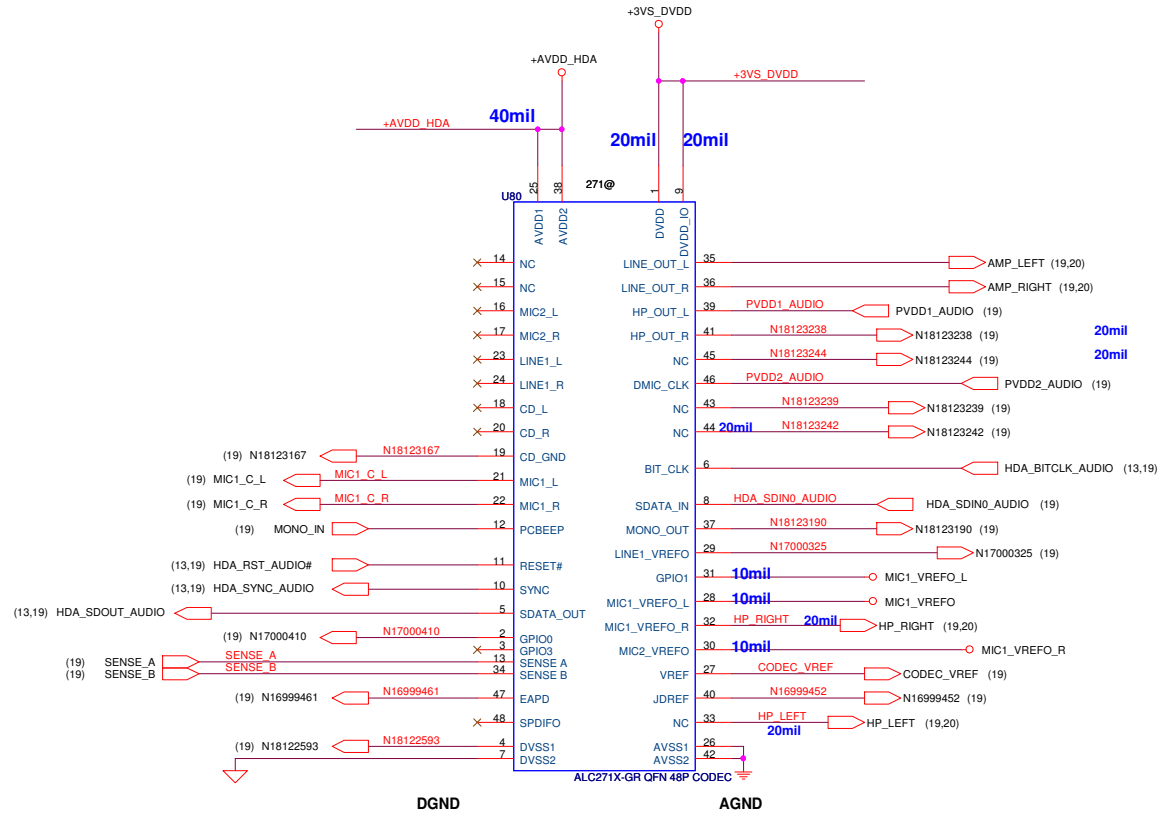
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Issued Date	2006/08/05	Deciphered Date	2007/8/18	Title	
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				Size	Document Number
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PVDD1_AUDIO

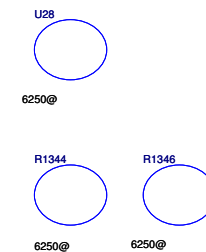
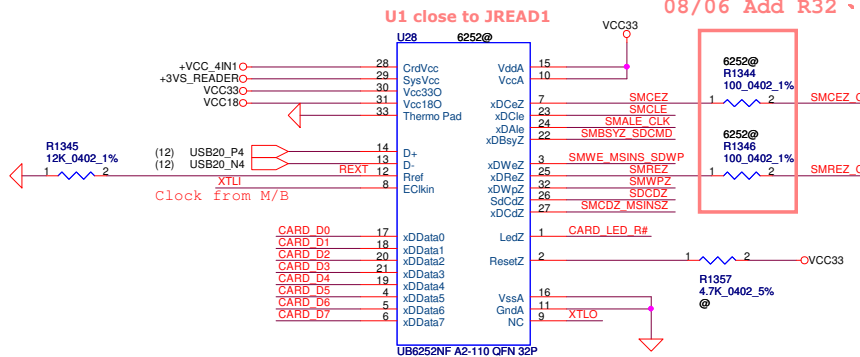
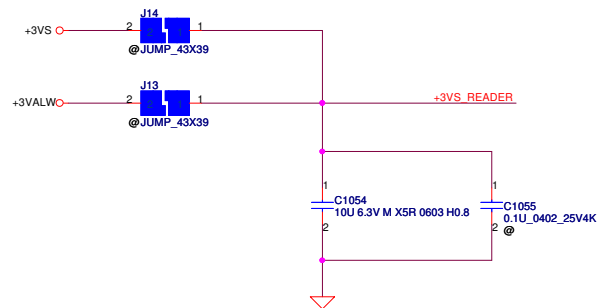


HD Audio Codec



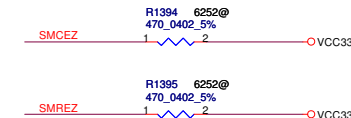
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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				Rev	0.2



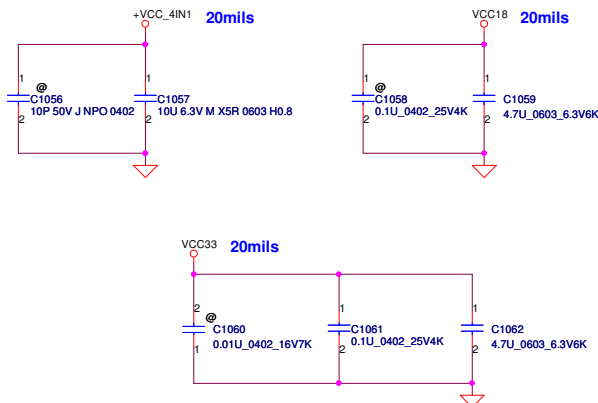
08/06 Add R1347 - R1348

HW TRAP JUMPER 0: NC, 1: Short



when you use UB6250 ,R1347 - R1348 is NC

C1056 - C1057 close to U1

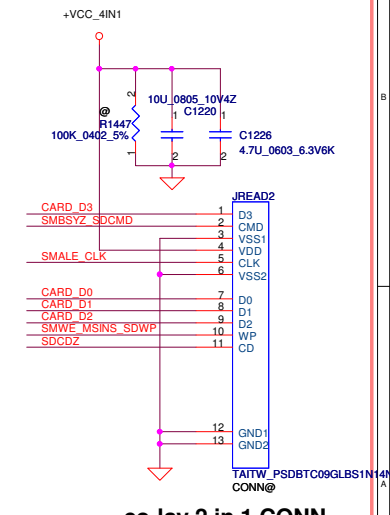
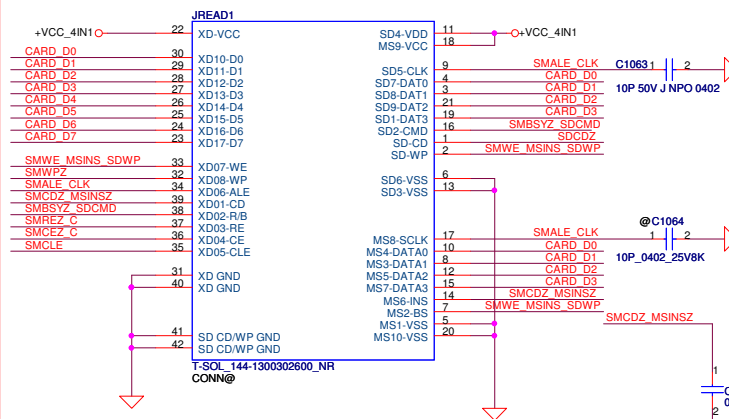


07/02 Revised C1053 to 0.01u

ByPass Capacitors

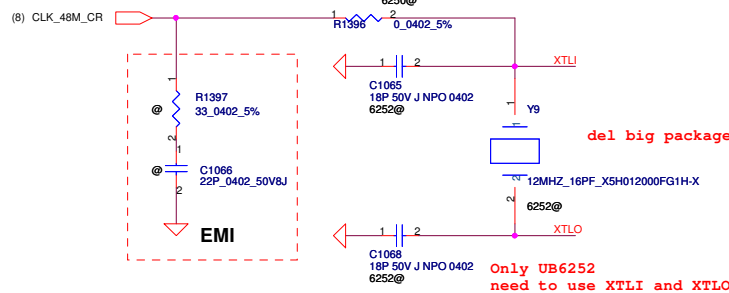
07/02 Update JREAD1

Card Reader Connector



co-layer 2 in 1 CONN

4/30 Add CLK_SD_48M

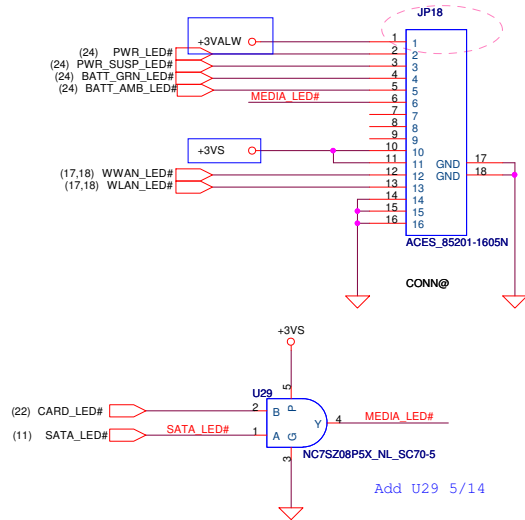


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Issued Date	2009/01/22	Deciphered Date	2009/11/20	Card reader	
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				LA-6221P	
				Date: Thursday, July 01, 2010	1 Sheet of 39

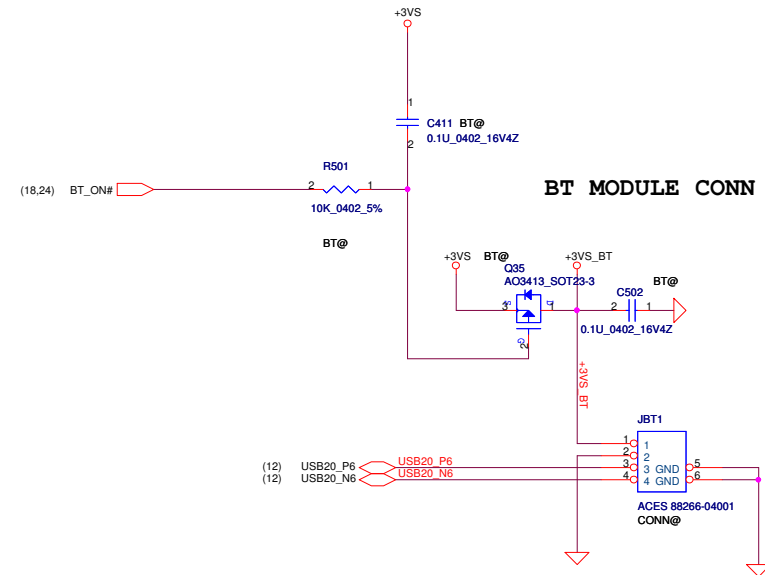
LED PCB CONN

ADD LED PCB CONN 06/12

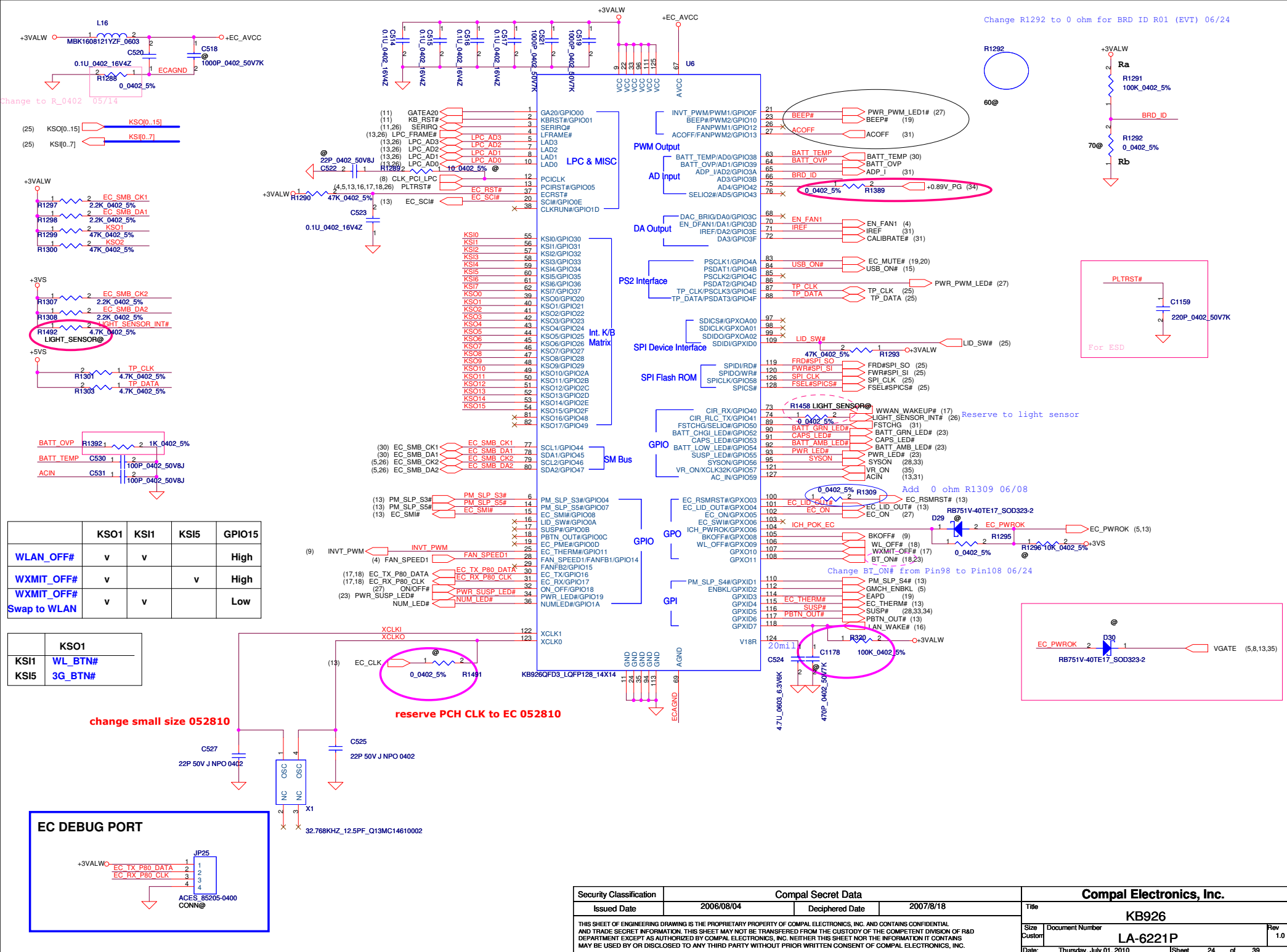
Change JP18 to NEW P/N 06/23
09/03 Change +5VALW , +5VS to +3VALW +3VS



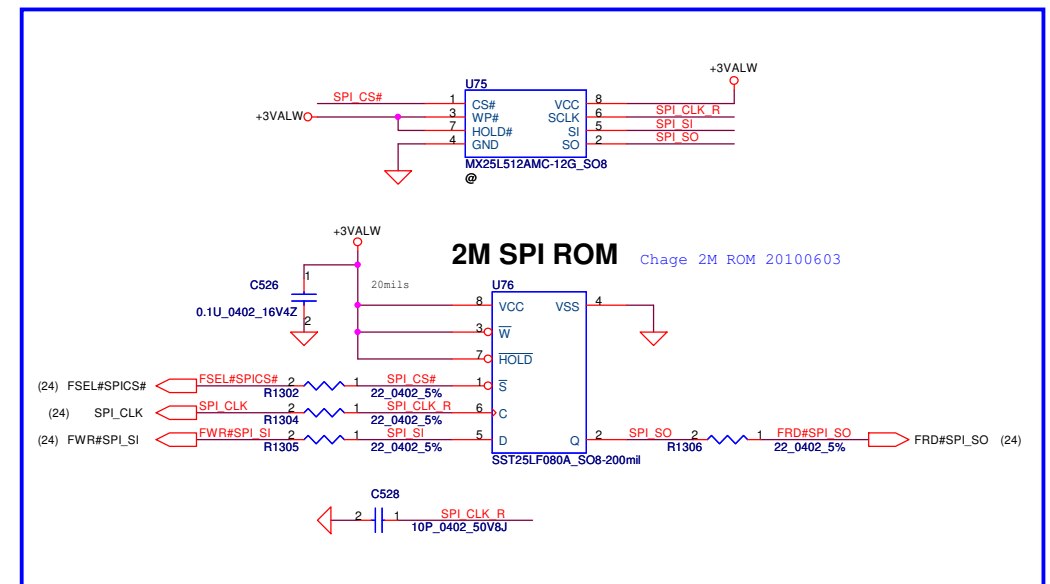
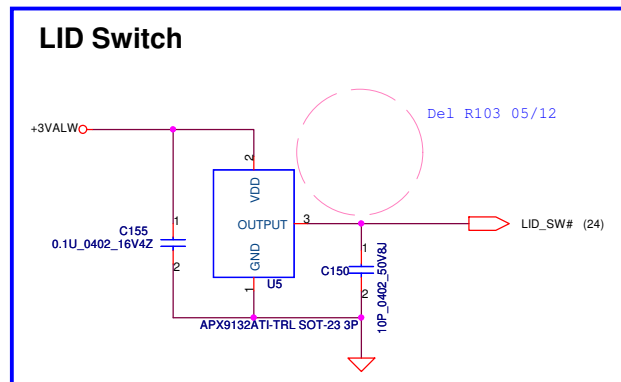
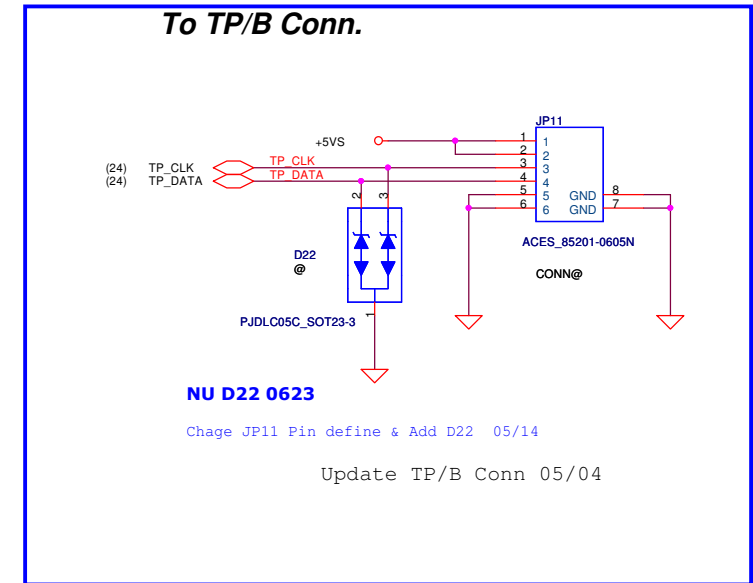
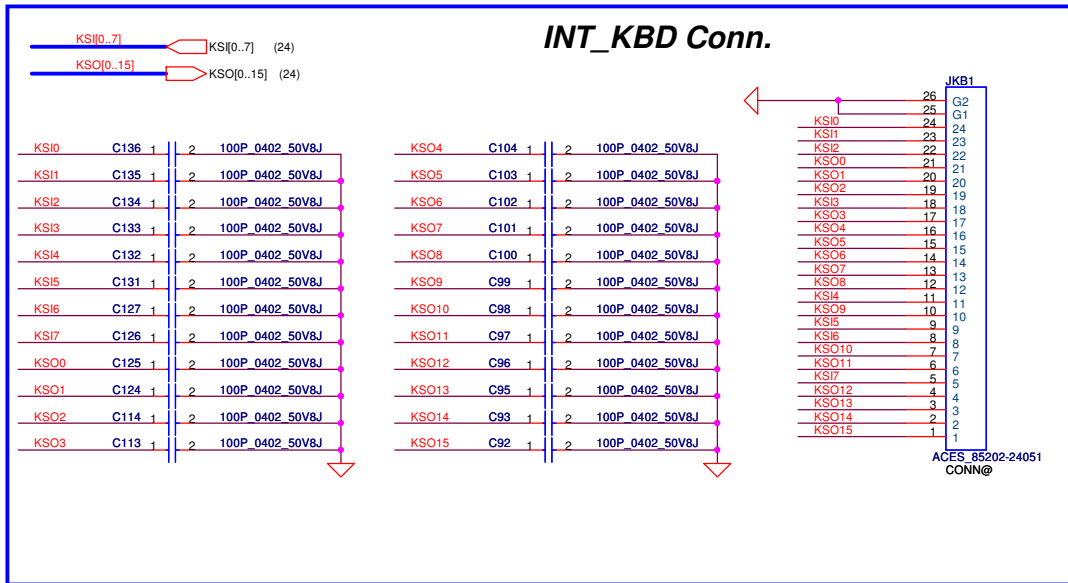
BT MODULE CONN



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				Date Thursday, July 01, 2010	Sheet 24 of 39	



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								KB/TP/LID SW/ SPI	
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						Date:	Friday, July 02, 2010		Sheet

[illegible]

Diagram showing the connection for JP26:

- Pin 1: +3VSD
- Pin 2: (5,24) EC_SMB_CLK2
- Pin 3: (5,24) EC_SMB_DA2
- Pin 4: (24) LIGHT_SENSOR_INT2
- Pin 5: GND1
- Pin 6: GND2

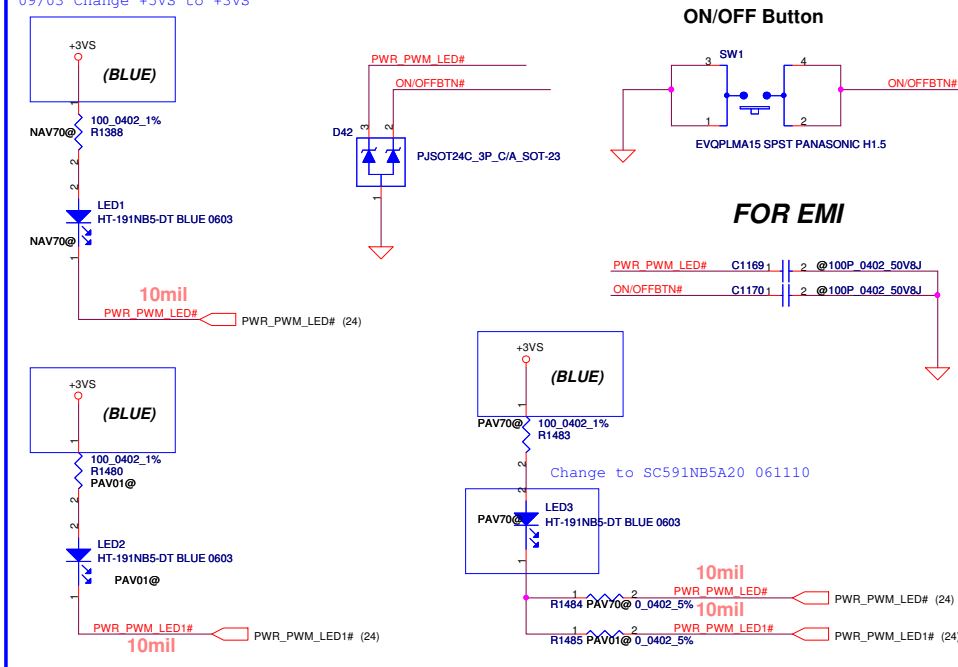
Connector: ACES_88266-05001

Label: CONN@

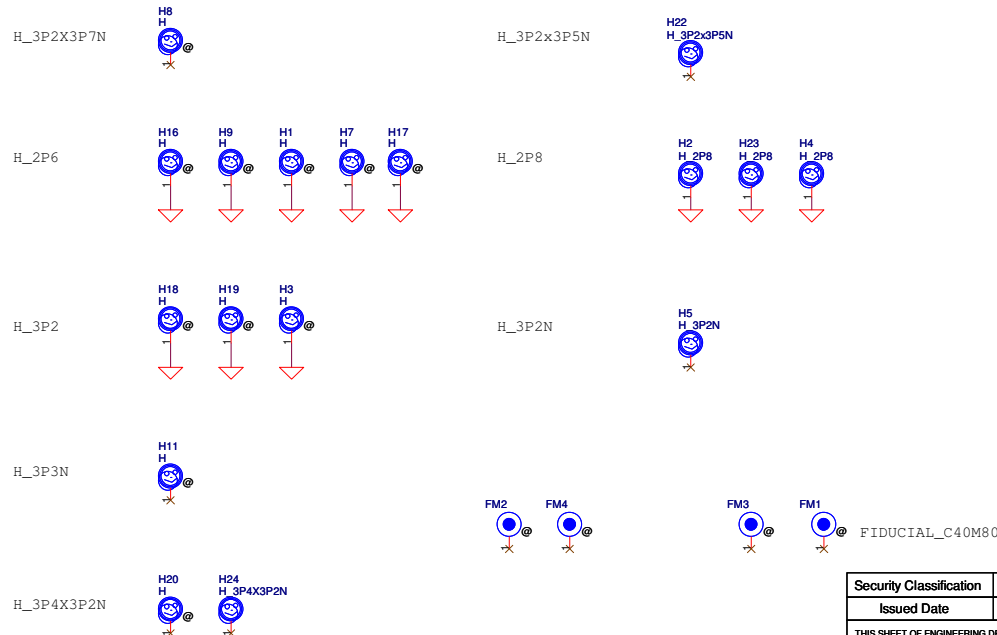
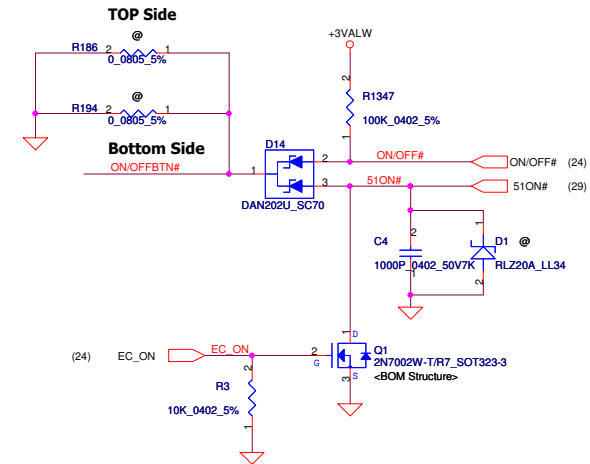
LIS33DE(G-Sensor)

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Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title	
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				Document Number	0.1
				LA-6221P	
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Add For NAV50 07/06
09/03 Change +5VS to +3VS



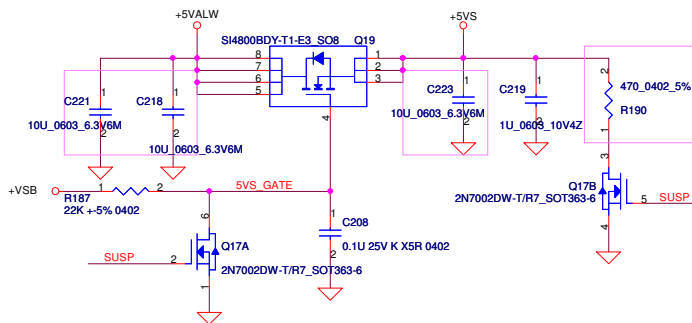
Power Button Logic



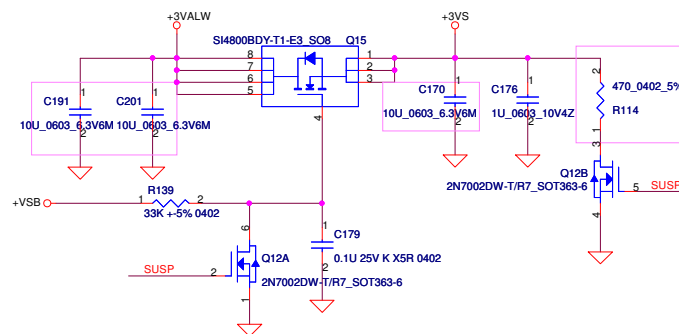
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Issued Date		2006/08/04		Deciphered Date		2007/8/18		Title								
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								Size	Document Number	LA-6221P						Rev
								Custom								1.0
								Date:	Thursday, July 01, 2010			Sheet	27	of	39	

Change R51 R57 R70 R63 R317 R114 R190 to 0402 SIZE 04/30
 Change C221 C218 C223 C 191 C201 C170 C392 C393 C394 to 0603 SIZE 04/30

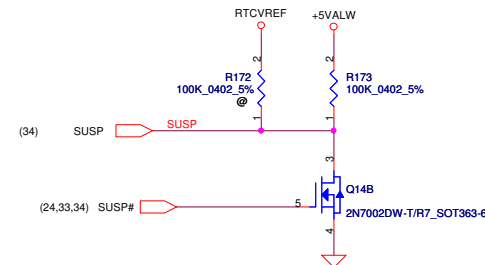
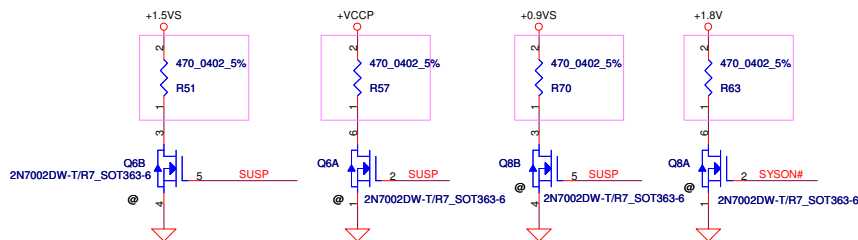
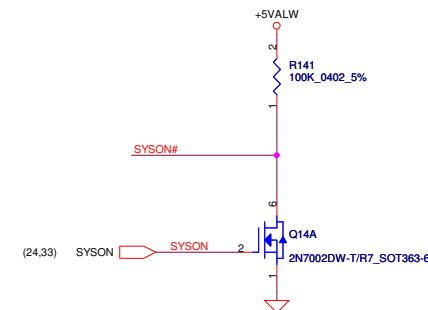
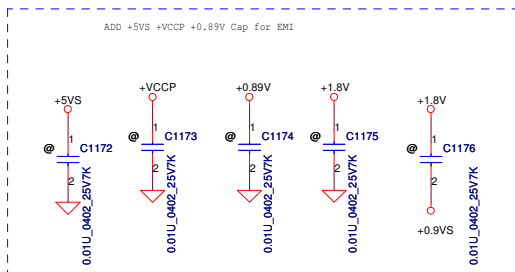
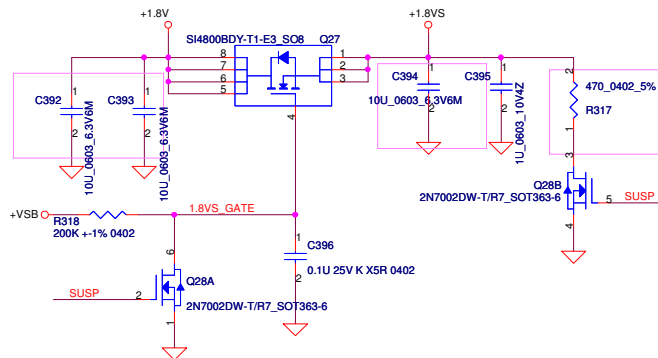
+5VALW TO +5VS



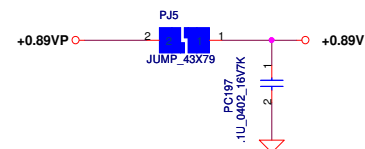
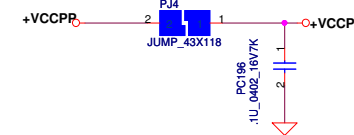
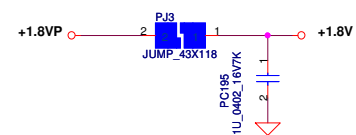
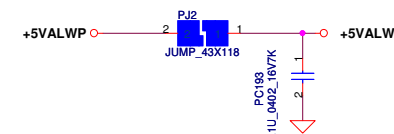
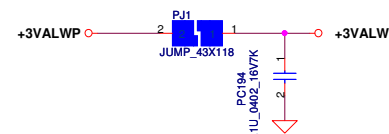
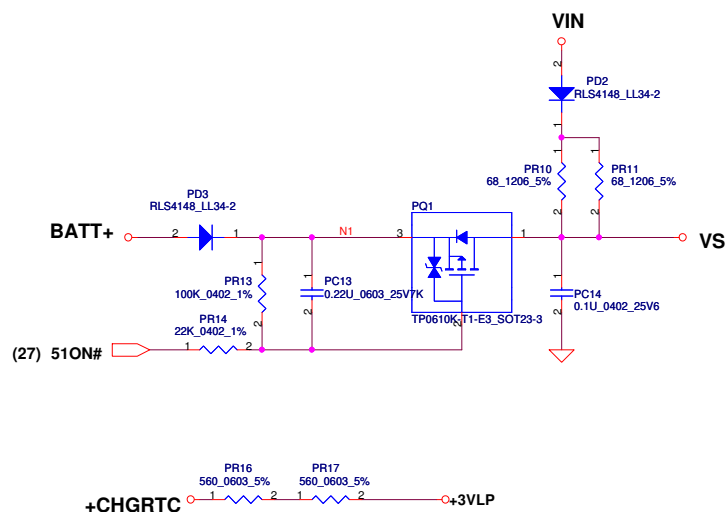
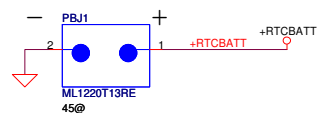
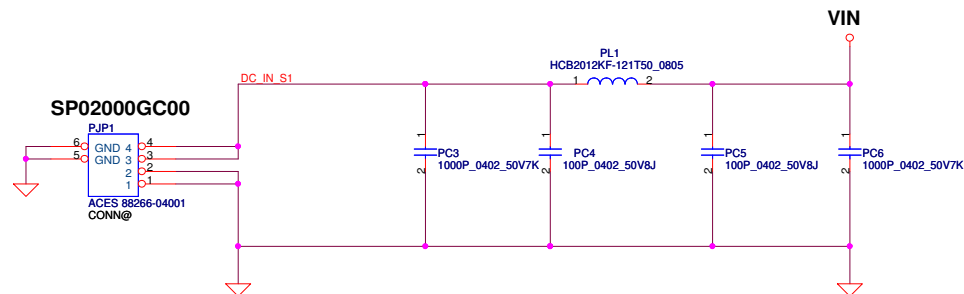
+3VALW TO +3VS



+1.8V to +1.8VS

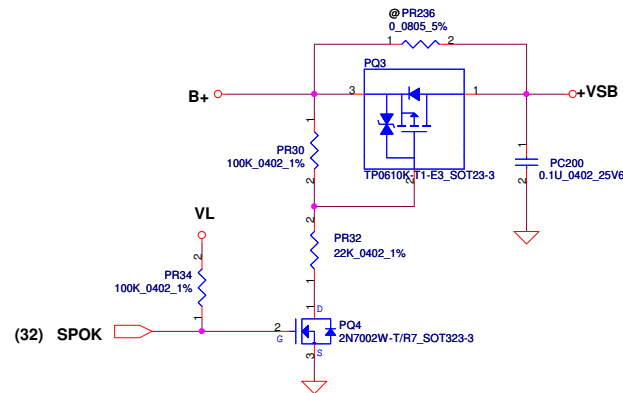
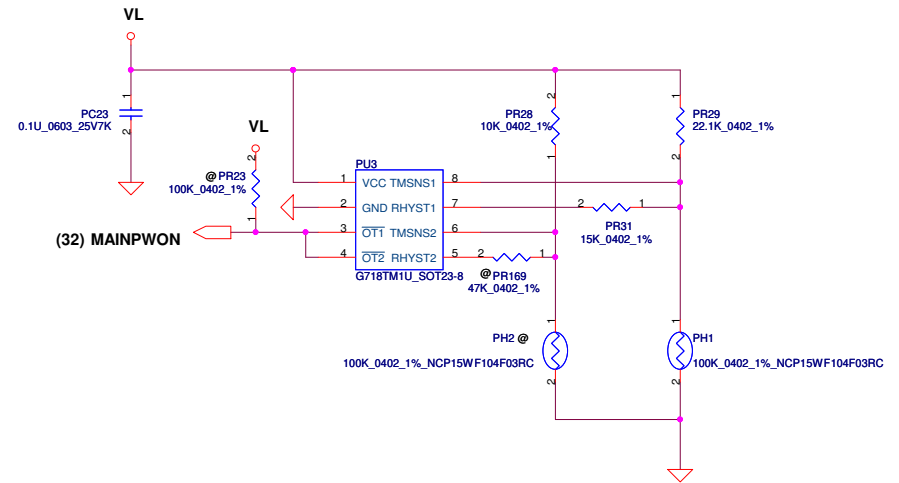
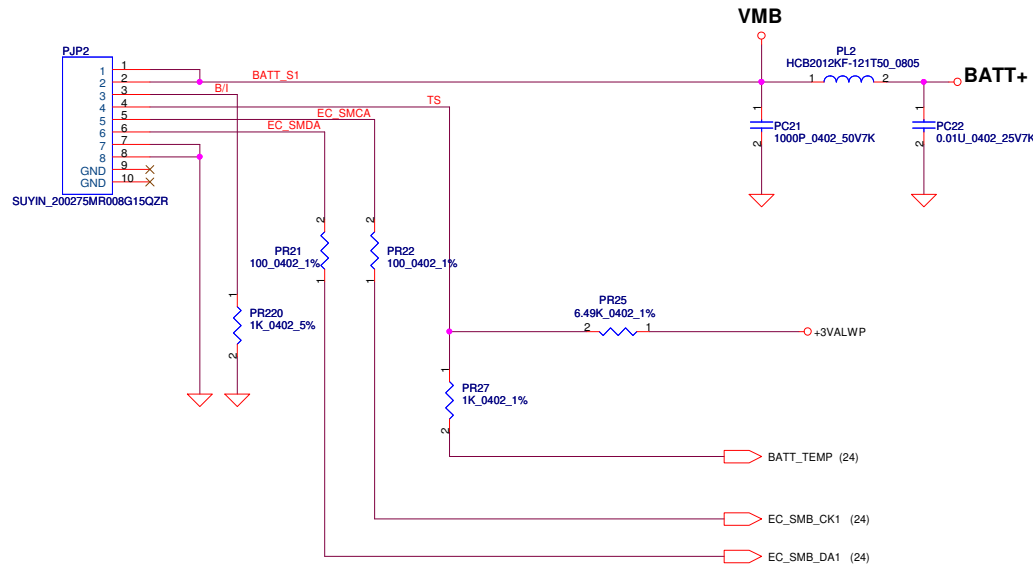


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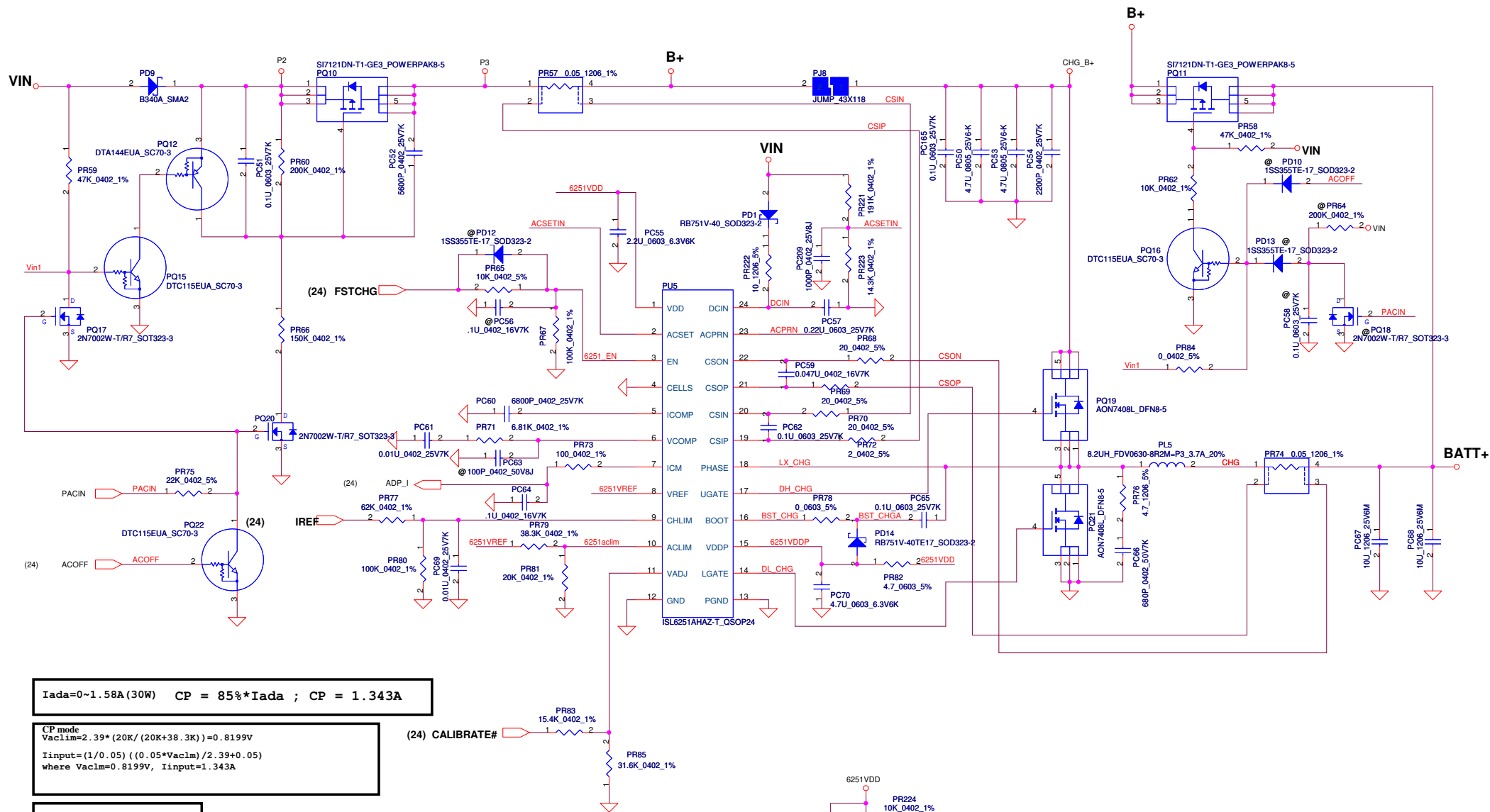


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PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C



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$I_{ada} = 0 \sim 1.58A (30W)$ CP = $85\% \cdot I_{ada}$; CP = 1.343A

CP mode
 $V_{ac1m} = 2.39 \cdot (20K / (20K + 38.3K)) = 0.8199V$
 $I_{input} = (1 / 0.05) \cdot ((0.05 \cdot V_{ac1m}) / 2.39 + 0.05)$
 where $V_{ac1m} = 0.8199V$, $I_{input} = 1.343A$

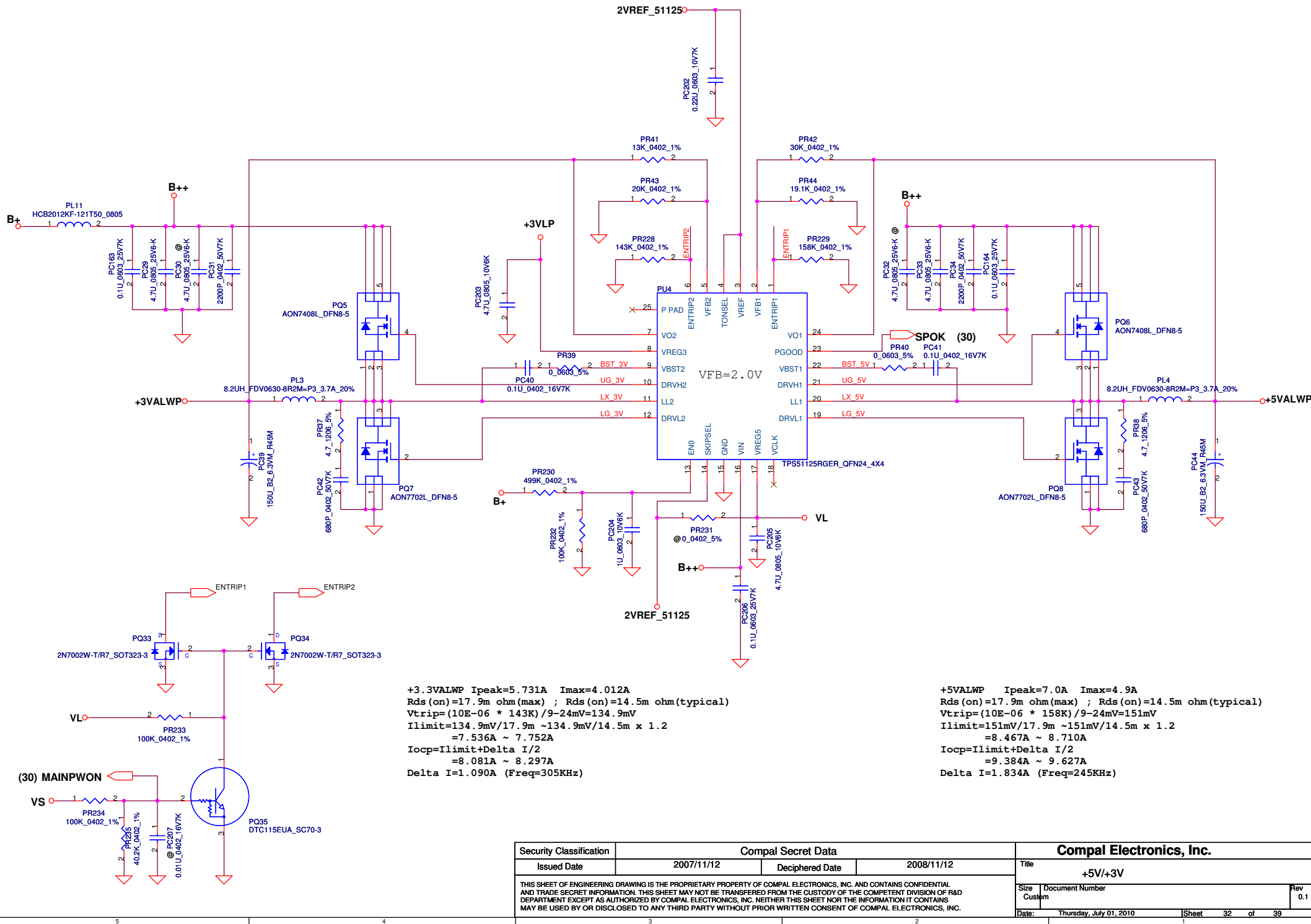
CC=0.3~1.76A
 $I_{REF} = 1.62 \cdot I_{charge}$
 $I_{REF} = 0.486V \sim 2.85V$
 $3.24V \Rightarrow 2A$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

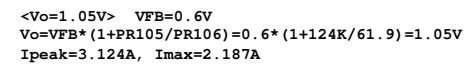
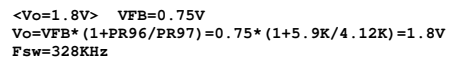
$V_{ADJ} \rightarrow V_{REF} \rightarrow 4.41V$
 $V_{ADJ} \rightarrow \text{Ground} \rightarrow 3.59V$
 $V_{cell} = (0.175 \cdot V_{ADJ} + 3.99)$

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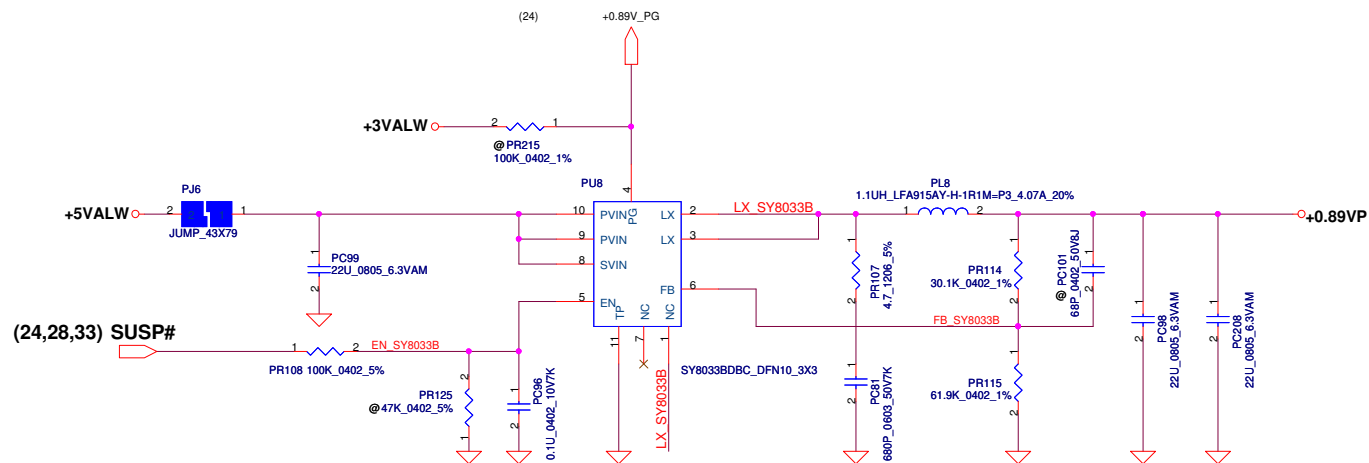
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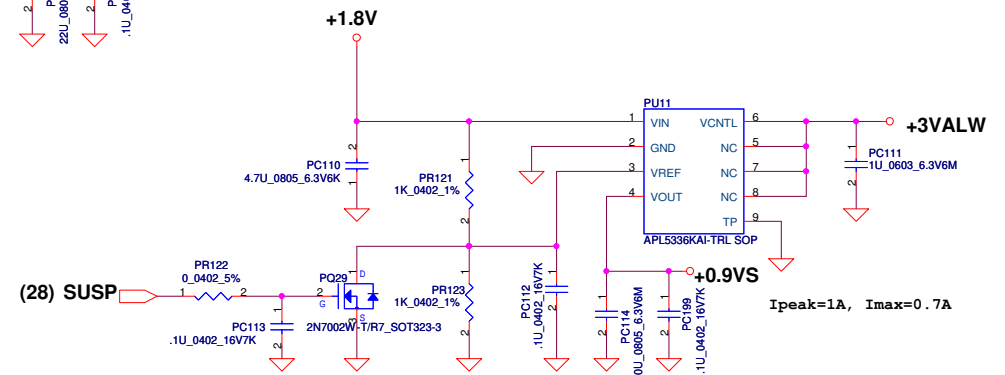
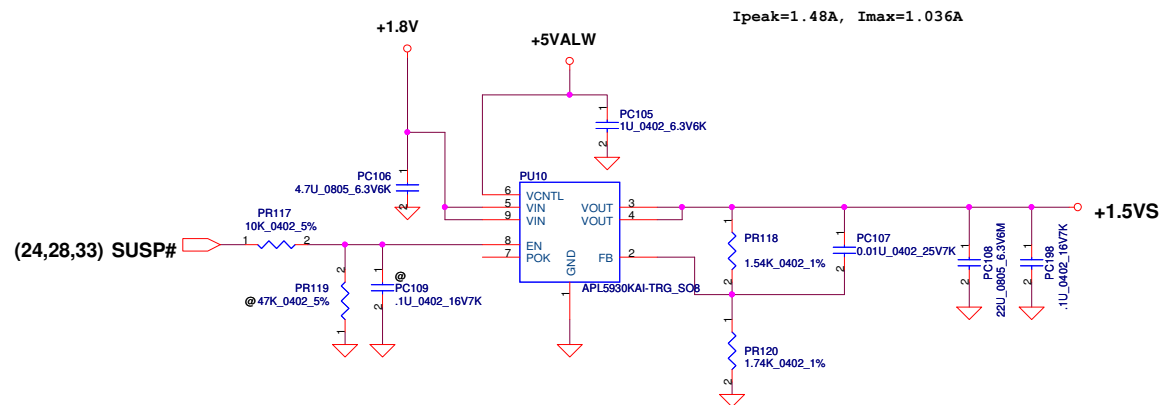
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$$\begin{aligned} <V_o=0.89V> \quad V_{FB}=0.6V \\ V_o &= V_{FB} * (1 + PR114 / PR115) = 0.6 * (1 + 30.1K / 61.9K) = 0.89V \\ I_{peak} &= 2.64A, \quad I_{max} = 1.848A \end{aligned}$$



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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add PR84	For design change	0.1	30	add PR84 (SD028000080 , S RES 1/16W 0 +-5% 0402)	2010.4.10	EVT
2	Change power solution	For design change	0.1	32	Change PU7 from SA000031D00(S IC RT8209BGQW WQFN 14P PWM) to SA00003RU00(S IC SY8033BDBC DFN 10P SINGLE BUCK)	2010.4.12	EVT
3	Change SY8033B Pin1 net	For design change	0.1	32,33	Change SY8033B Pin1 connect Pin2 & Pin3	2010.4.13	EVT
4	Change PC101 & PC119	For design change	0.1	32,33	Change PC101 & PC119 to SE071680J80 (S CER CAP 68P 50V J NPO 0402)	2010.4.13	EVT
5	Change PR105	For design change	0.1	32	Change PR105 from SD034100200(S RES 1/16W 10K +-1% 0402) to SD034100280 (S RES 1/16W 10K +-1% 0402)	2010.5.13	DVT
6	Change PC30 & PC32 to non-pop	For cost down plan	0.1	32		2010.6.1	PVT
7	Change PL3,PL4,PL5,PL6,PL7,PL8,PL10	For TMP choke shortage issue	0.1	32	Change PL3,PL4,PL5 from SH00000JI00 to SH00000BS00 Change PL6,PL10 from SH00000FD10 to SH000000700 Change PL7,PL8 from SH00000J300 to SH000007N00	2010.6.1	PVT
8	Change PD10.PD13.PC58.PR64. PQ18 to non-pop Change PR84 to pop	For cost down plan	0.1	31		2010.6.11	PVT
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