

Compal Confidential

PAV70 DDR3 Schematics Document

Intel Pineview Processor with Tigerpoint + DDRIII

2010-06-25

REV: 1.0

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Model Name : PAV50
File Name : LA-6421P



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CONN

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+0.89V	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 17)

	VCC	3.3V				
	Ra	100K				
	ID	BRD ID	Rb	Vab-Min	Vab-Typ	Vab-Max
PAV50	0	R01 (EVT)	0	0V	0V	0V
	1	R02 (DVT)	8.2K	0.216V	0.250V	0.289V
	2	R03 (PVT)	18K	0.436V	0.503V	0.538V
	3	R10A (MP)	33K	0.712V	0.819V	0.875V
	4	R01 (EVT)	56K	1.036V	1.185V	1.264V
	5	R02 (DVT)	100K	1.453V	1.650V	1.759V
	6	R03 (PVT)	200K	1.935V	2.200V	2.341V
	7	R10A (MP)	NC	2.500V	3.3V	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
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No PCI Device

EC SM Bus1 address

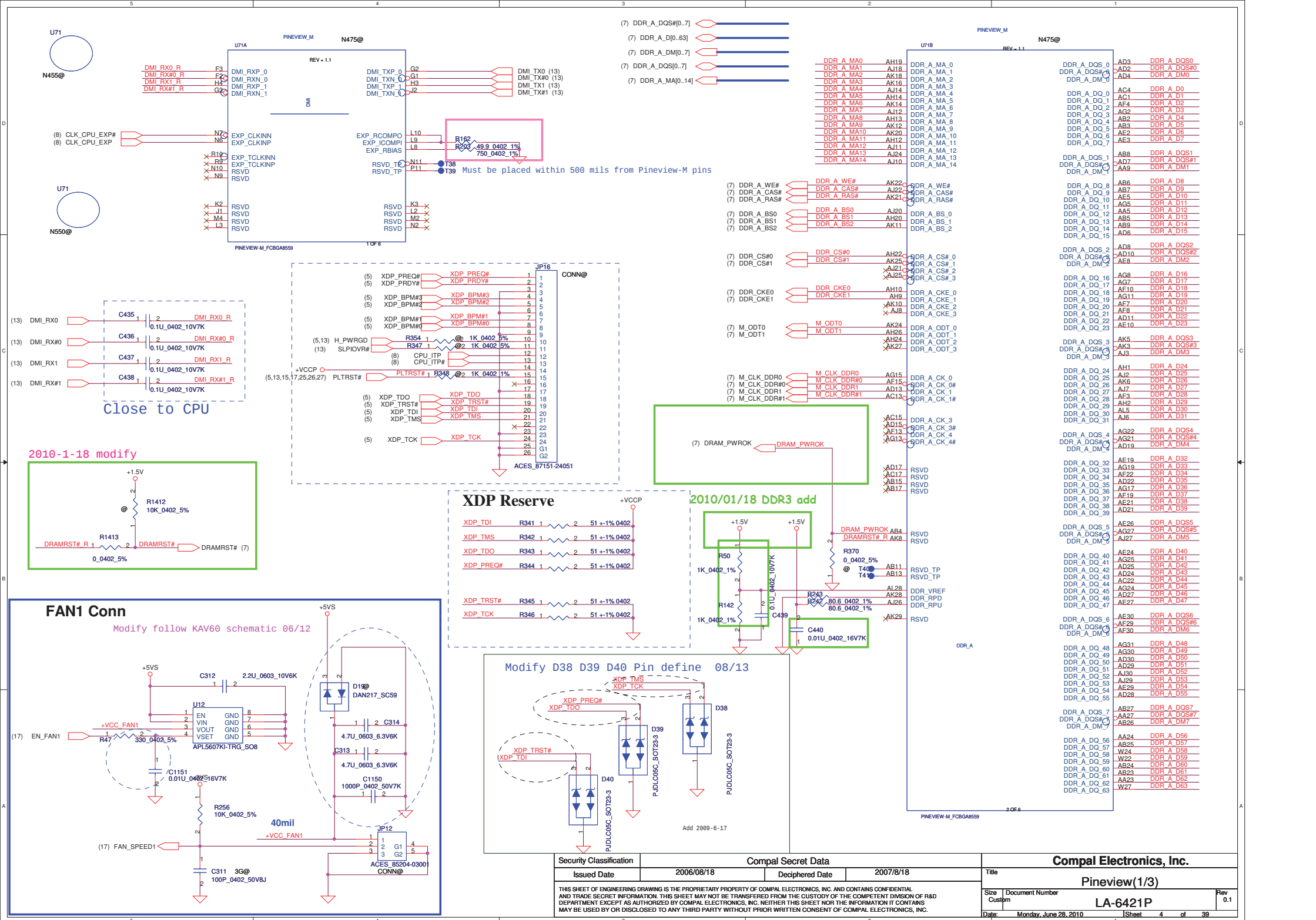
Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	100_1100

EC SM Bus2 address

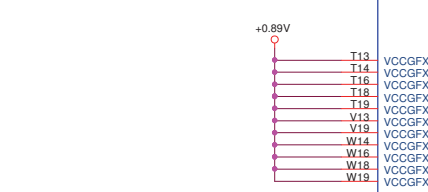
ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

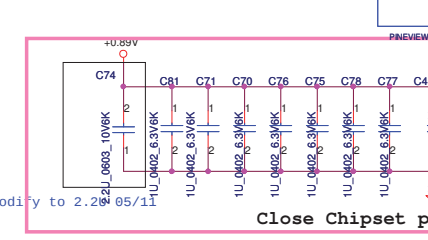
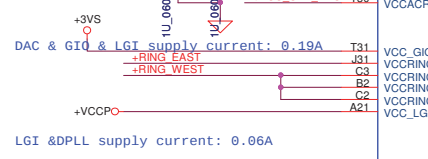
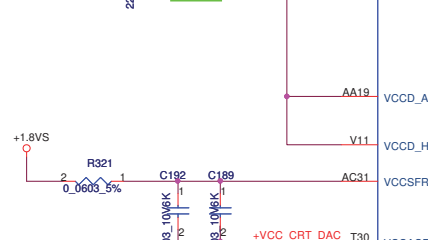
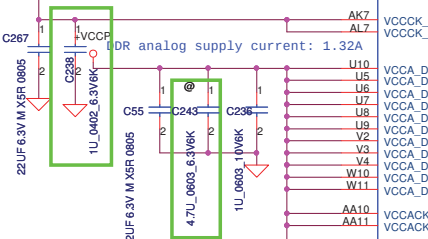
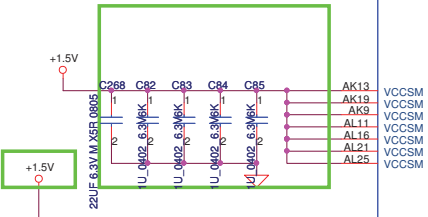
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GFX supply current: 2.64A

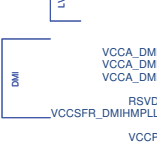
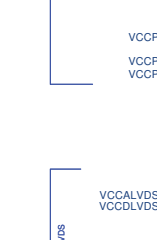
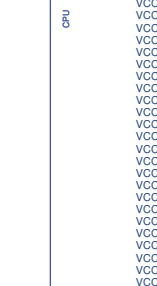
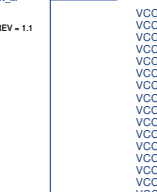


DDR supply current 2.27A



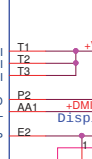
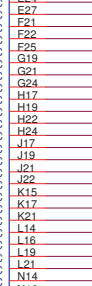
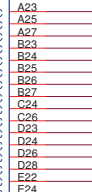
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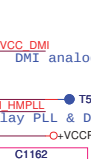
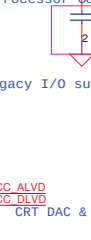
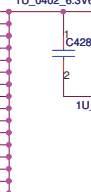
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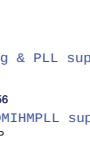
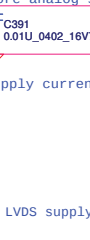
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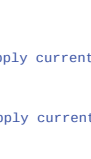
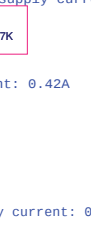
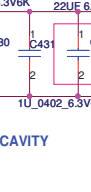
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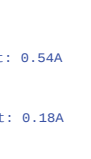
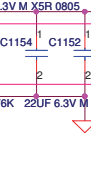
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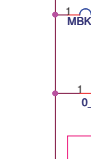
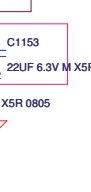
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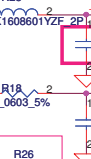
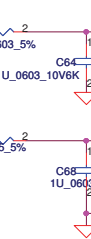
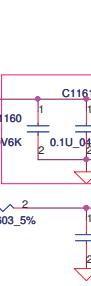
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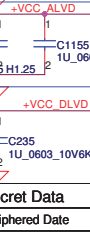
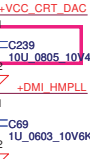
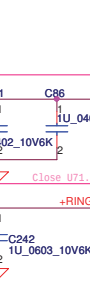
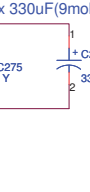
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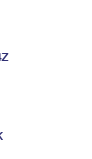
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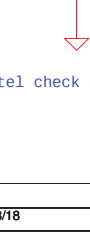
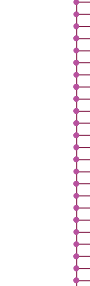
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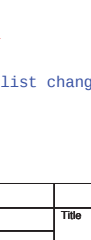
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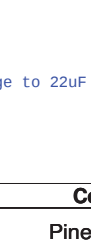
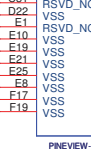
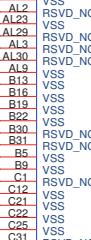
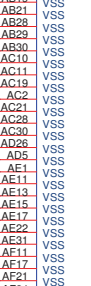
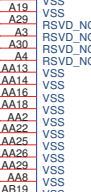
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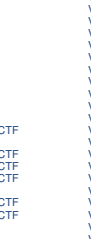
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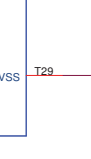
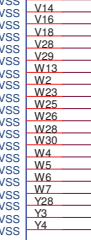
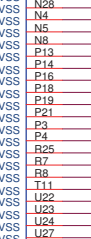
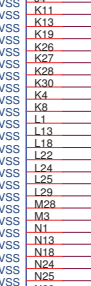
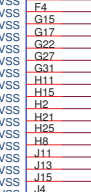
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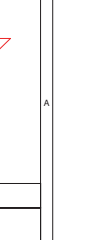
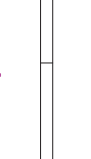
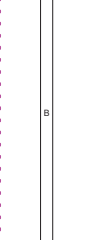
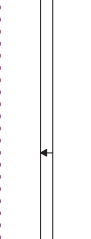
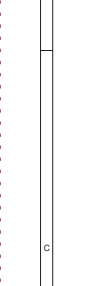
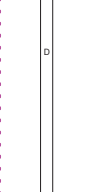
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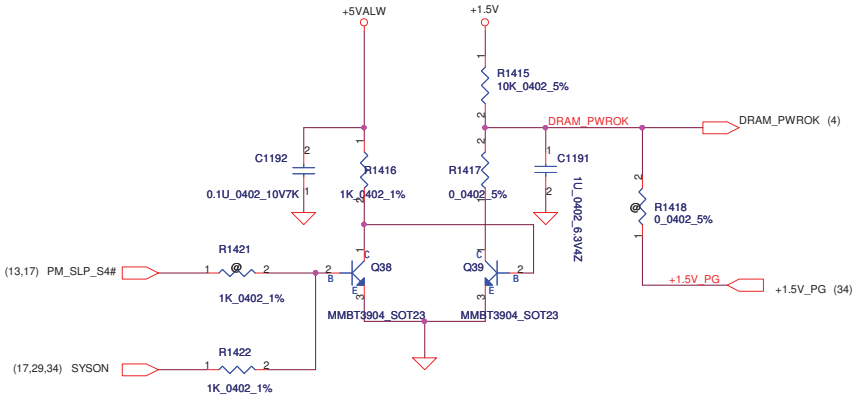
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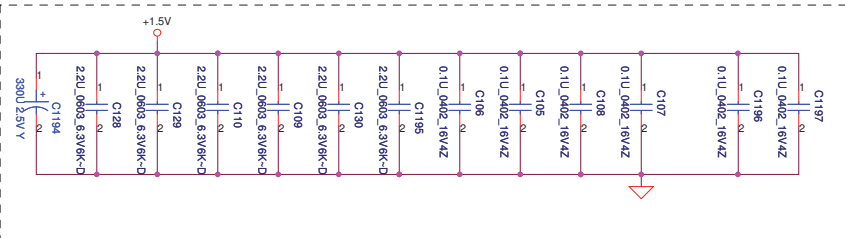


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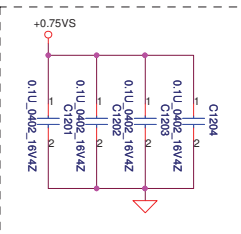
2010/01/18 DDR3 modify



Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203 & JDIMM1.204



FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								

Add C1145 C1146 C1147 for EMI 06/12

IDT: SA00003H610

Change Q10 to SB00000DH00 2010/04/06

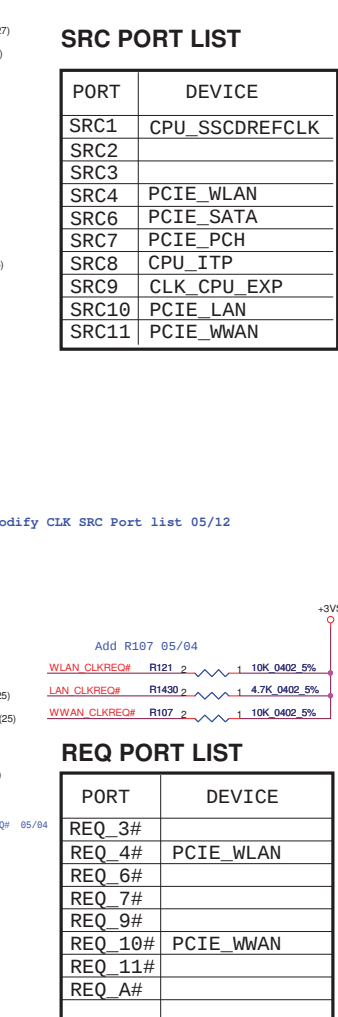
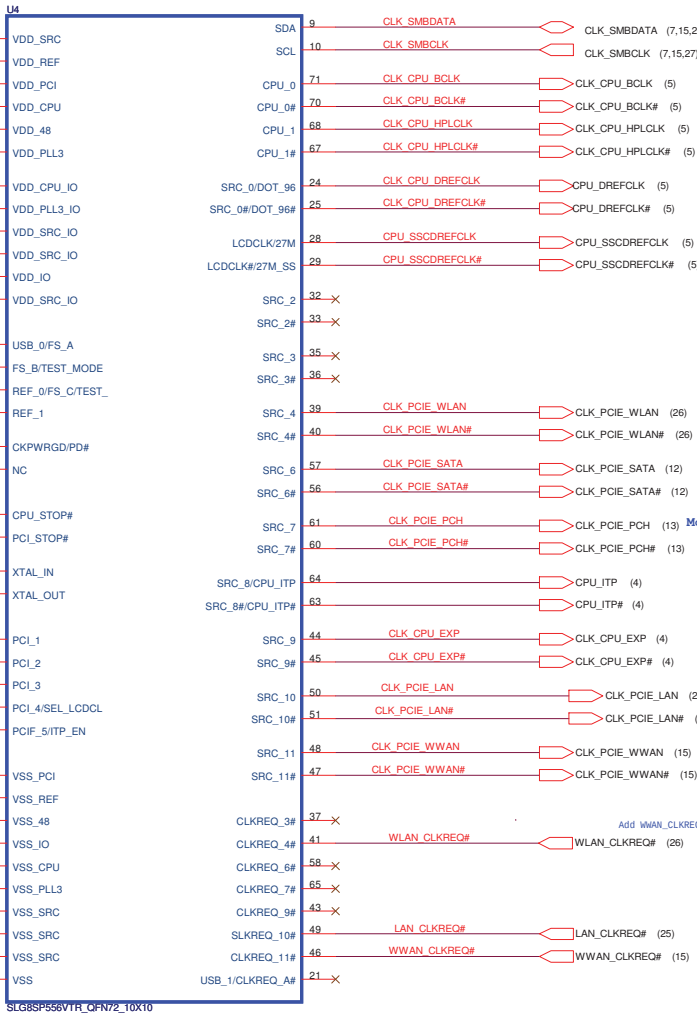
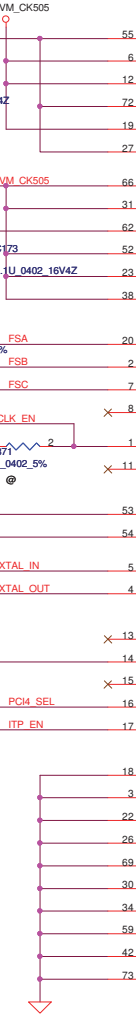
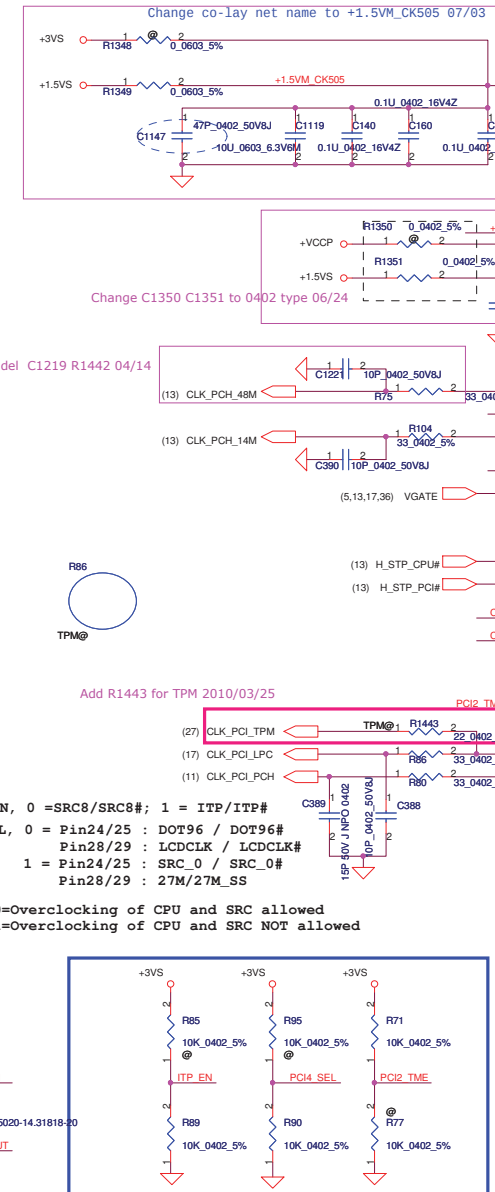
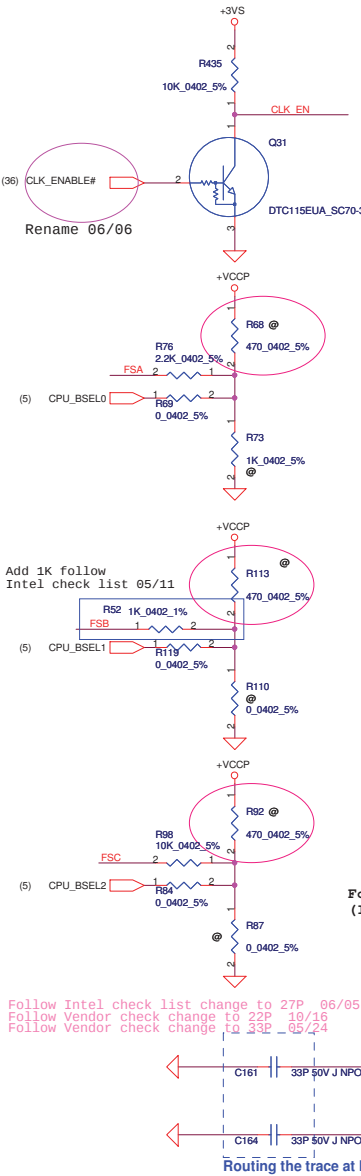
Realtek: SA00003H730

SRC PORT LIST

PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	PCIE_WWAN

REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	PCIE_WWAN
REQ_11#	
REQ_A#	



Change R577 to 0402 SIZE 06/16



Modify JLVDS1 08/04

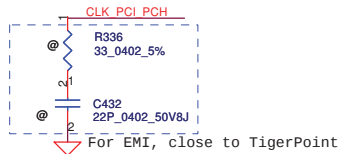


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				LA-6421P	
				Date:	Friday, June 25, 2010
				Sheet	9 of 39

Change L12. L14, L15 to SM01000C600 2010/04/06

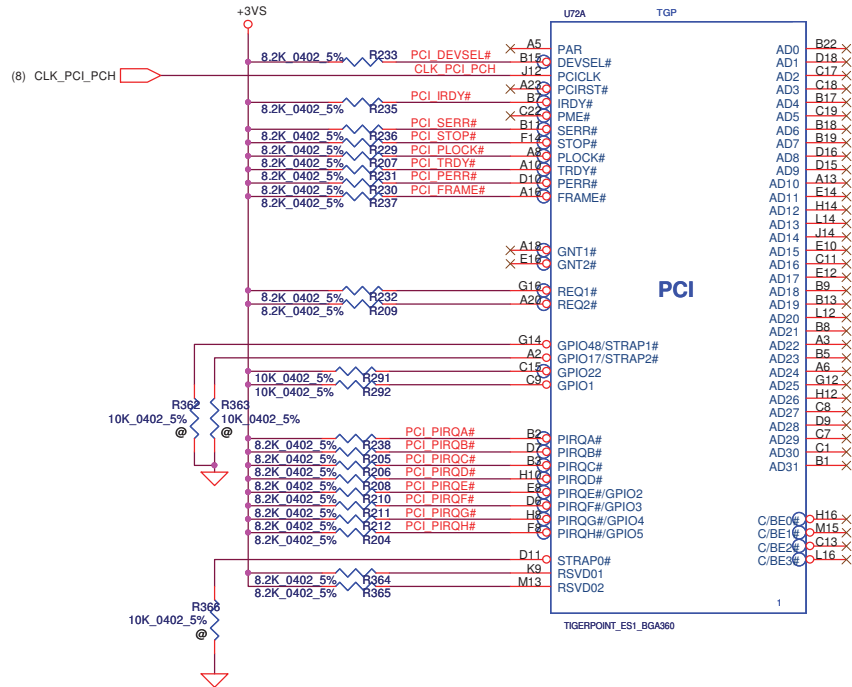


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Issued Date		2006/08/18		Deciphered Date		2007/8/18		
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				CRT PORT				
				Size B	Document Number		Rev	
				LA-6421P		0.1		
Date: Tuesday, June 22, 2010				Sheet 10 of 39				

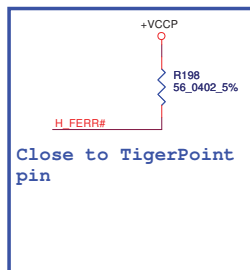
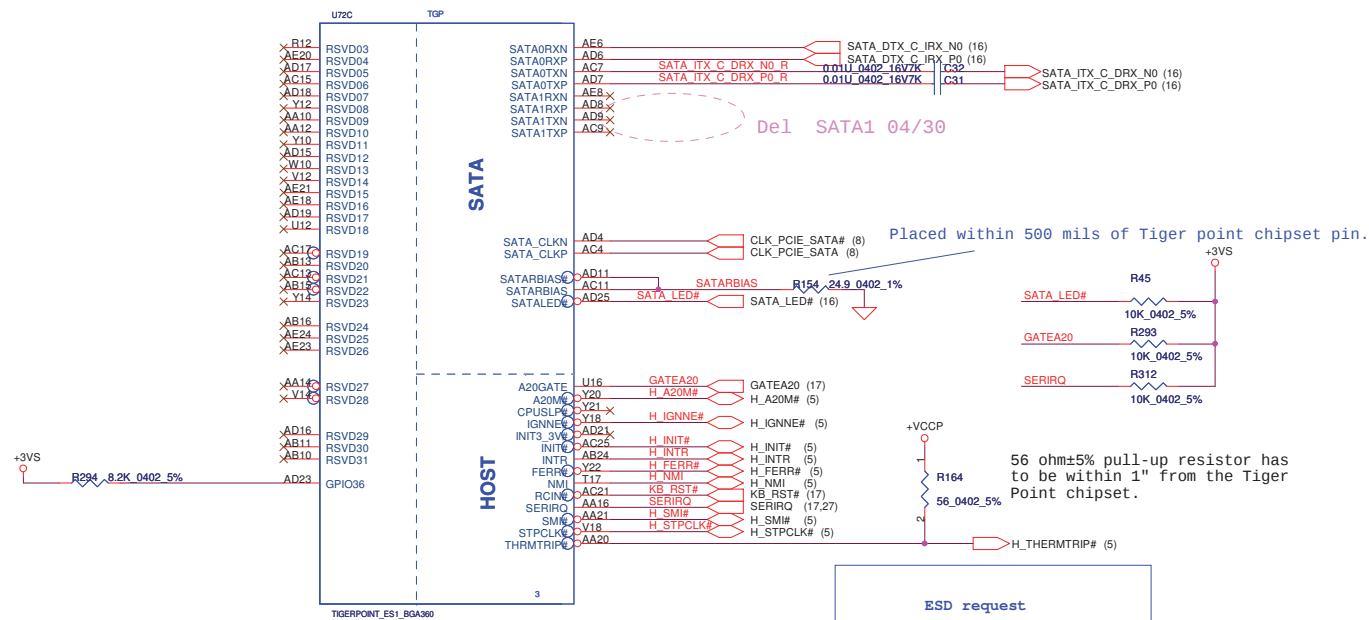


(27) G_SENSOR_INT PCI_PIRQ#

Add for G-sensor interrupt 2010/03/11



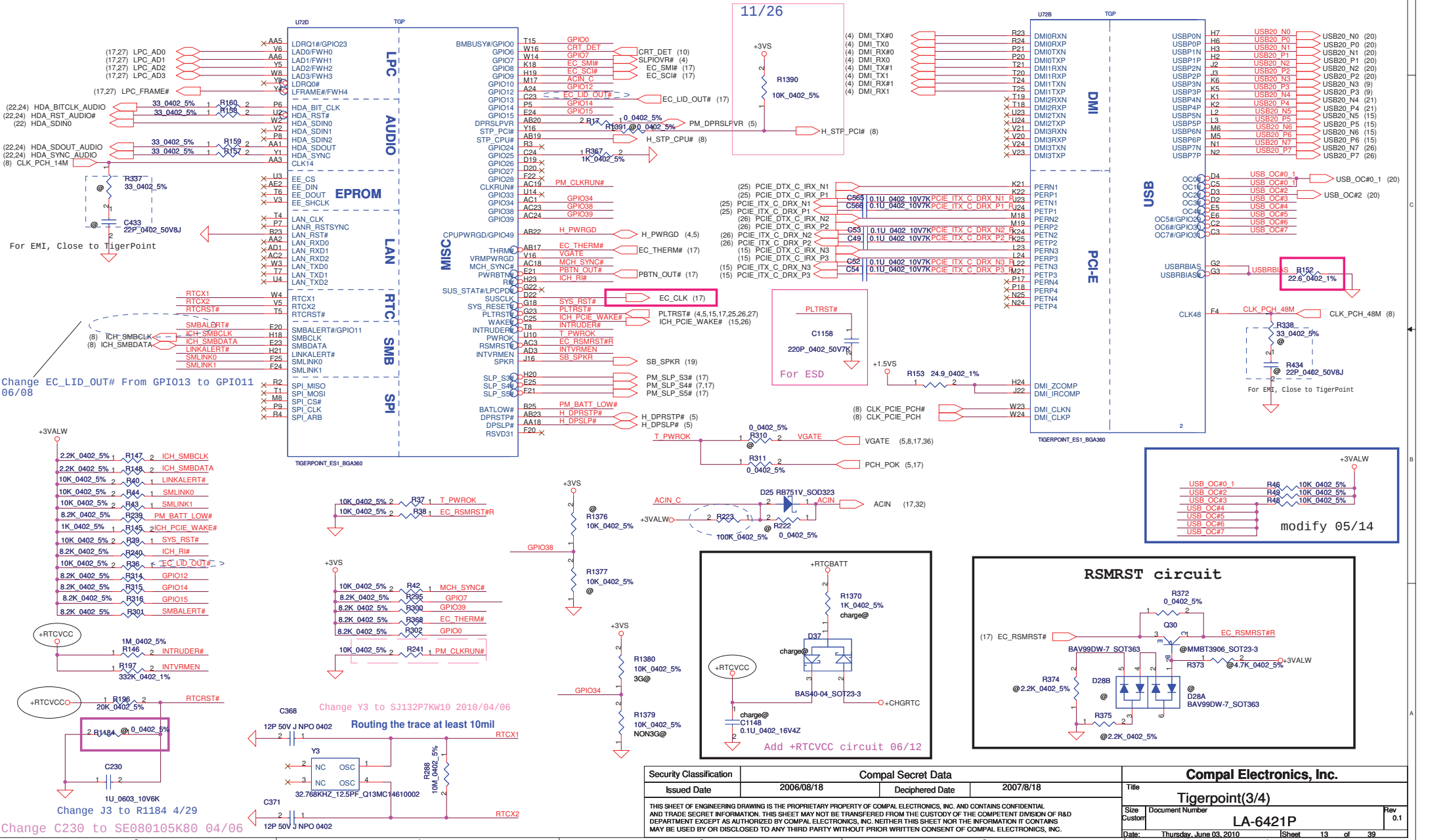
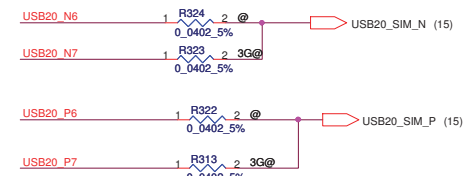
STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC



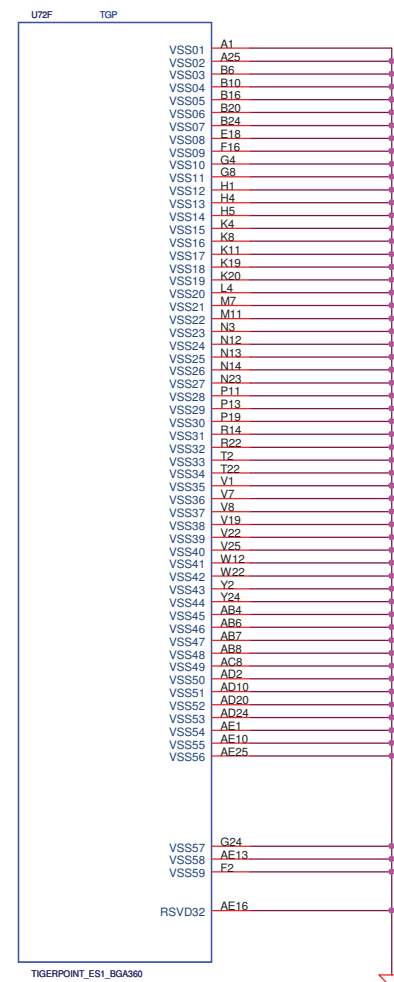
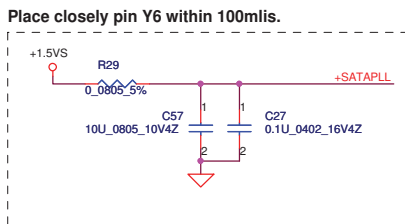
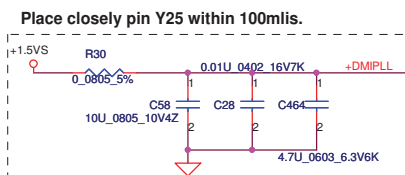
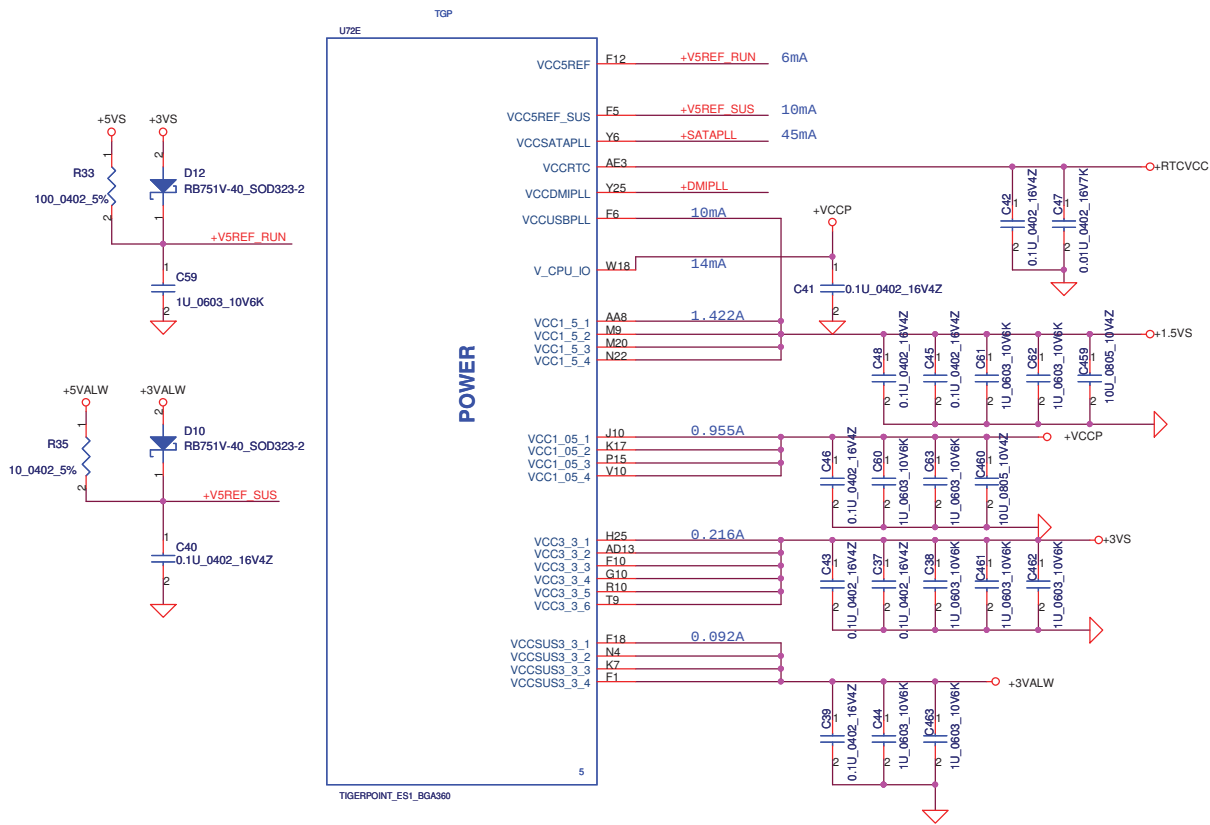
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Issued Date		2006/08/18		Deciphered Date		2007/8/18		Title			
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						Size		Document Number		Rev	
						Custom		LA-6421P		0.1	
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PCIE Port List	
1	LAN
2	WLAN
3	WWAN
4	

USB Port List	
0	USB Left1
1	USB Left2
2	USB Right2
3	CMOS
4	CardReader
5	WWAN
6	BT
7	WIMAX



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Size	Document Number	LA-6421P		Rev	0.1
Date:	Thursday, March 25, 2010	Sheet	14	of	39

Change JMINI1 to FOX_AS0B246-S50U-7F_52P-T 06/29

Add C1163 C1164 C1165 C1166 06/23

Add C850 06/12

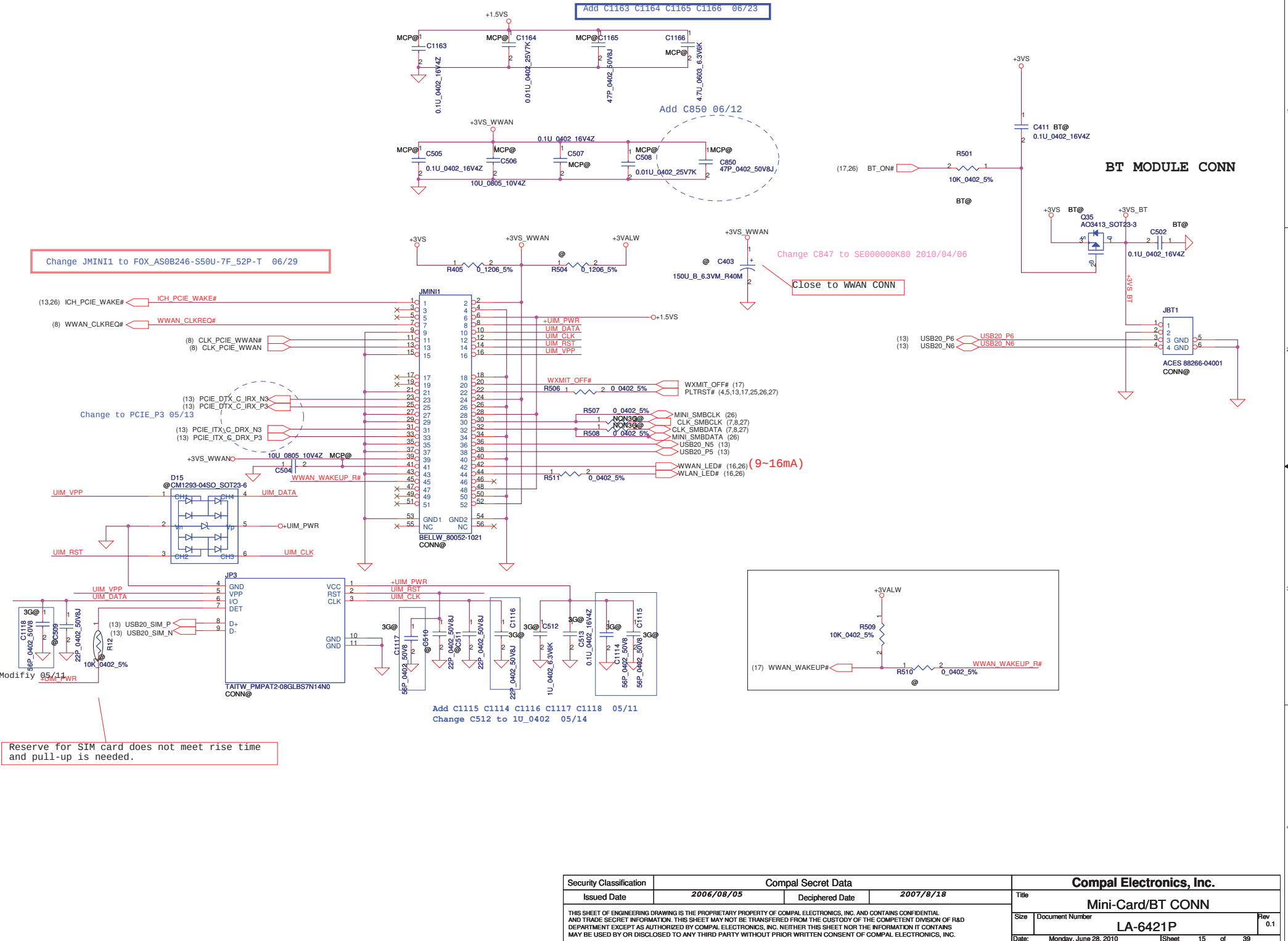
Change C847 to SE000000K80 2010/04/06

Close to WWAN CONN

Change to PCIE_P3 05/13

Add C1115 C1114 C1116 C1117 C1118 05/11
Change C512 to 1U_0402 05/14

Reserve for SIM card does not meet rise time and pull-up is needed.



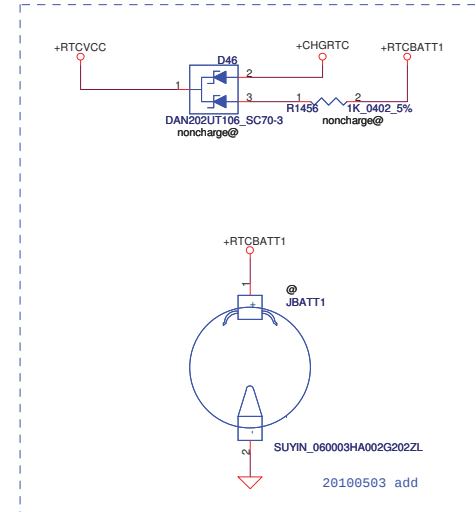
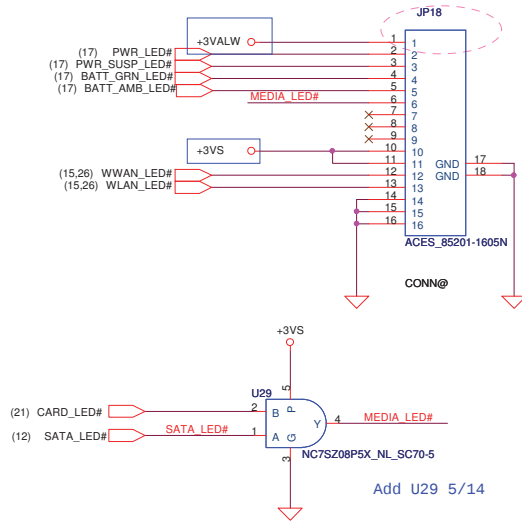
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2006/08/05	Deciphered Date	2007/8/18	Title	
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				Size	Document Number
				LA-6421P	
				Date	Monday, June 28, 2010
				Sheet	15 of 39
				Rev	0.1

ADD LED PCB CONN 06/12

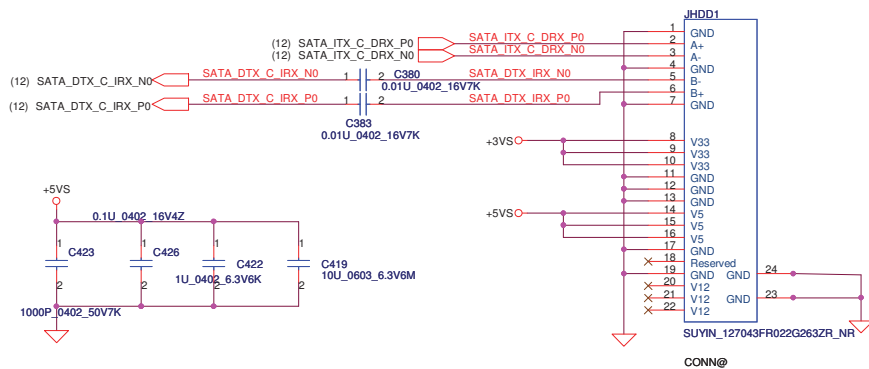
Change JP18 to NEW P/N 06/23

09/03 Change +5VALW , +5VS to +3VALW +3VS

LED PCB CONN



SATA HDD Conn.

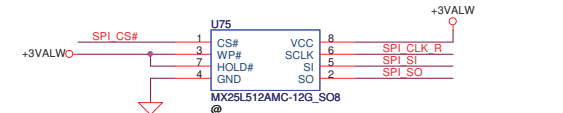


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	SATA CONN./LED/B CONN./BATT CONN.
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				Date: Thursday, June 03, 2010	Sheet 16 of 39

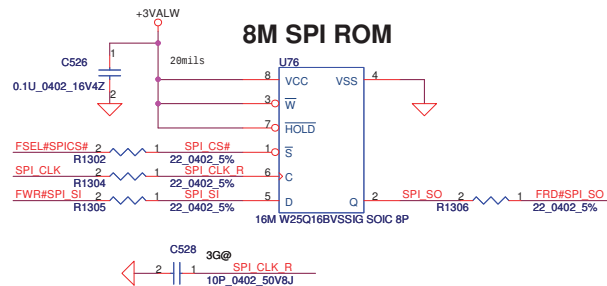


2 —  LIGHT_SENSOR_INT# (27)

Add for Light-sensor interrupt 2010/03/11



8M SPI ROM

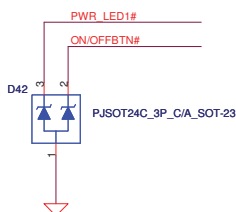


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				Date: Monday, June 28, 2010 11:57 AM		
				Sheet 17 of 39		

A circuit diagram showing a blue LED (LED2, HT-191NB5-DT BLUE 0603) connected to a +3VS power source. The LED is connected in series with a resistor (R1403, 51 ±5% 0402). The current flowing through the circuit is indicated as 50@.

EVQPLMA15 SPST PANASONIC H1.5

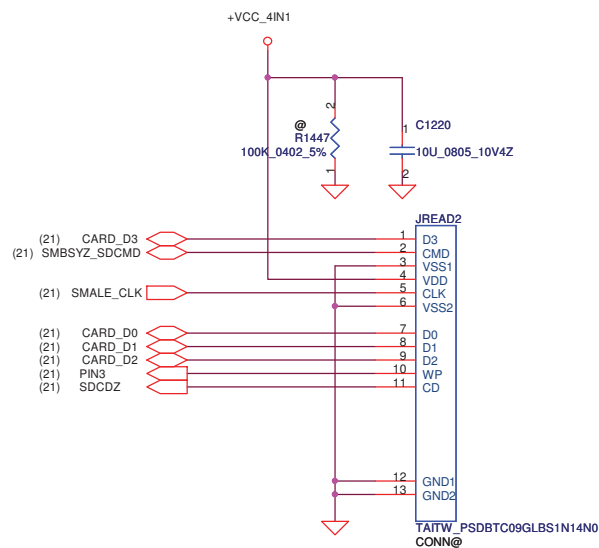
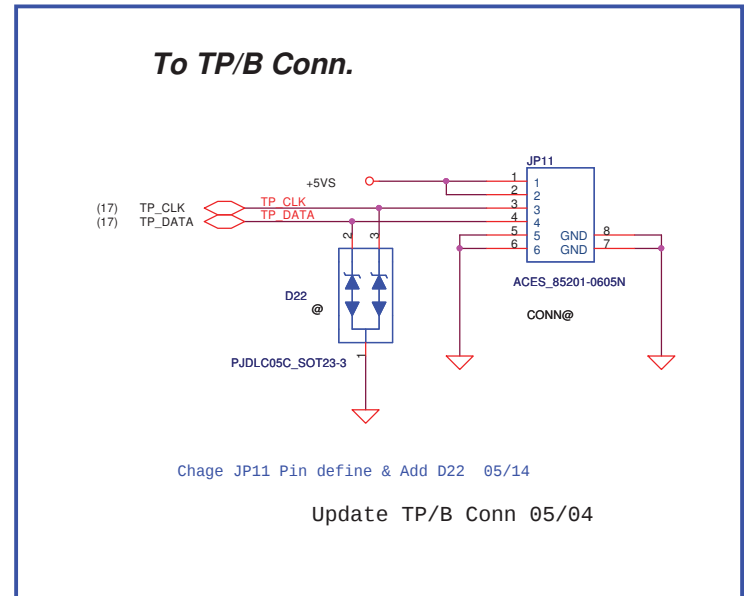
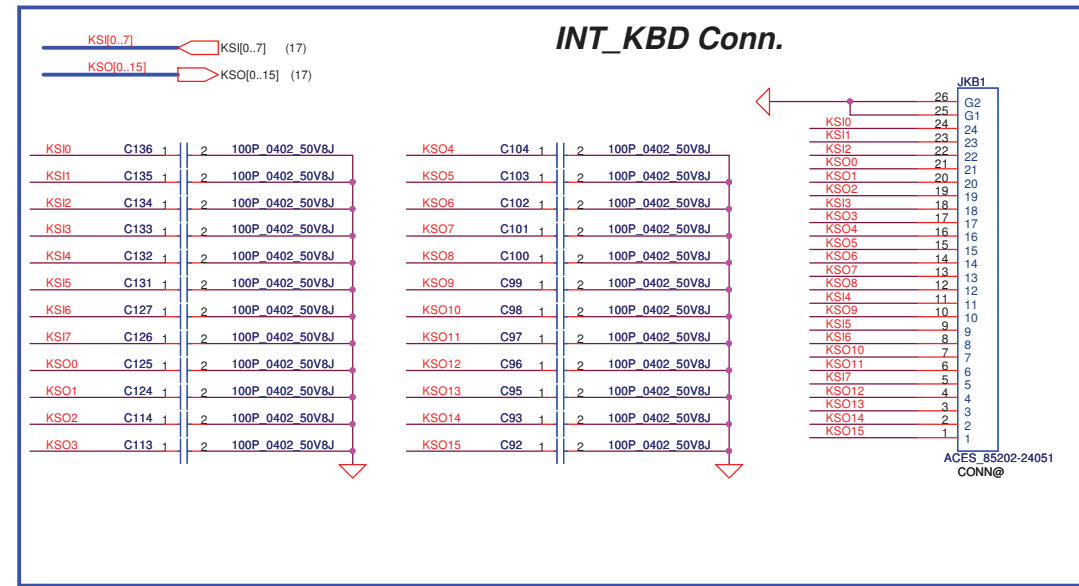
PWR_LED1#	C1169	1	2	@100P_0402_50V8J
ON/OFFBTN#	C1170	1	2	@100P_0402_50V8J



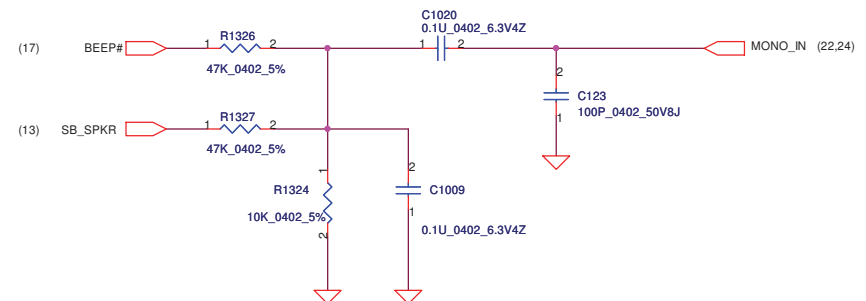
The schematic diagram shows the LED3 circuit. A +3VS supply is connected to a resistor R1454 (51 ±5% 0402). The resistor is connected to the anode of the LED (LED3, HT-191NBS-DT BLUE 0603). The cathode of the LED is connected to a signal trace labeled PWR_LED1# with a 10mil dimension.

[illegible]

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				Date: Thursday, June 03, 2010		
				Sheet 18 of 39		

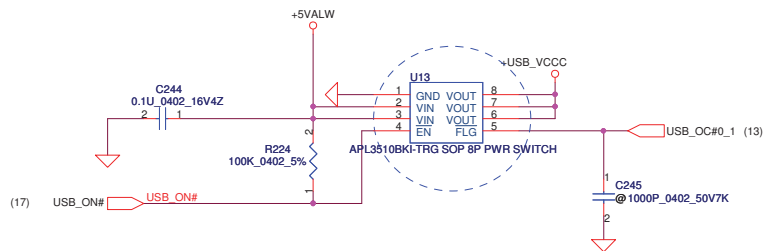


6/26 Add circuit



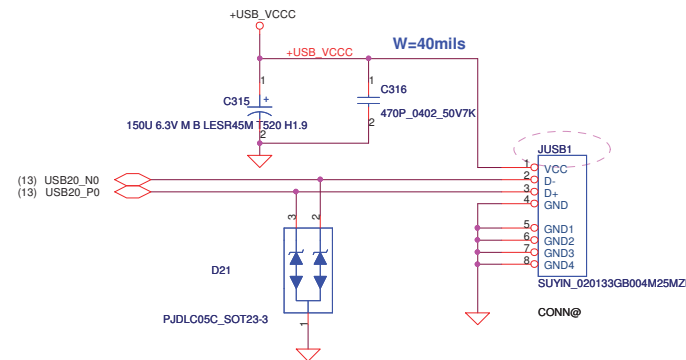
Modify MONO_IN schematic,move some parts to I/O Board , Add the MONO_IN_R on M/B 06/25

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Size		Document Number		Rev	
B		LA-6421P		0.1	
Date:		Tuesday, June 22, 2010		Sheet 19 of 39	

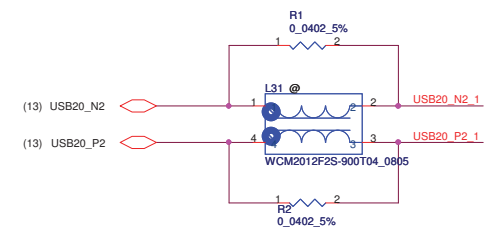
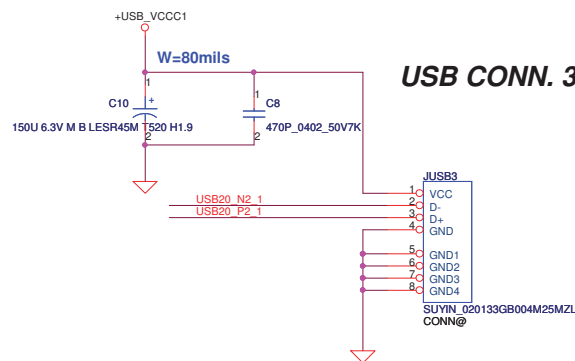
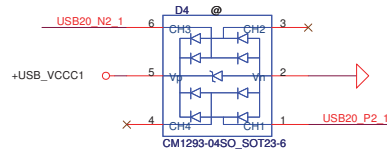
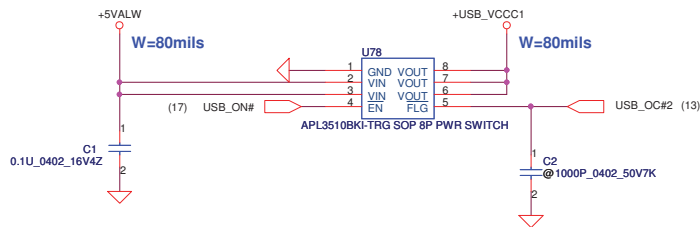
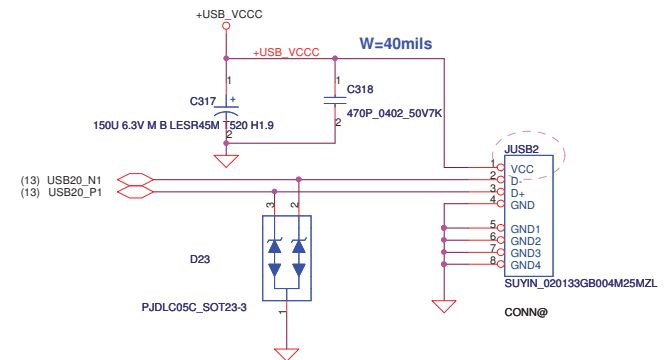


USB CONN.1

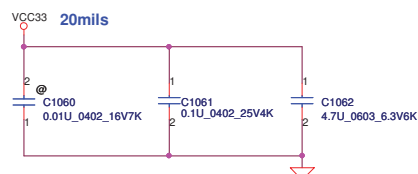
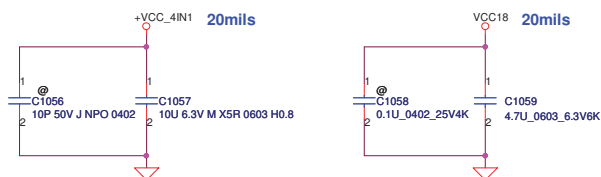
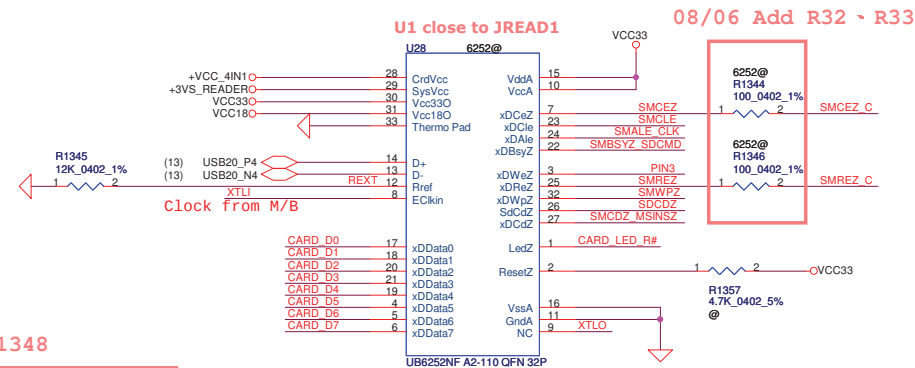
Change JUSB1 JUSB2 to NEW P/N SP010906181 06/23



USB CONN.2



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						Size B	Document Number			LA-6421P		Rev 0.1
						Date:	Thursday, June 03, 2010		Sheet	20	of	39



ByPass Capacitors

R1394 6252@
470_0402_5%

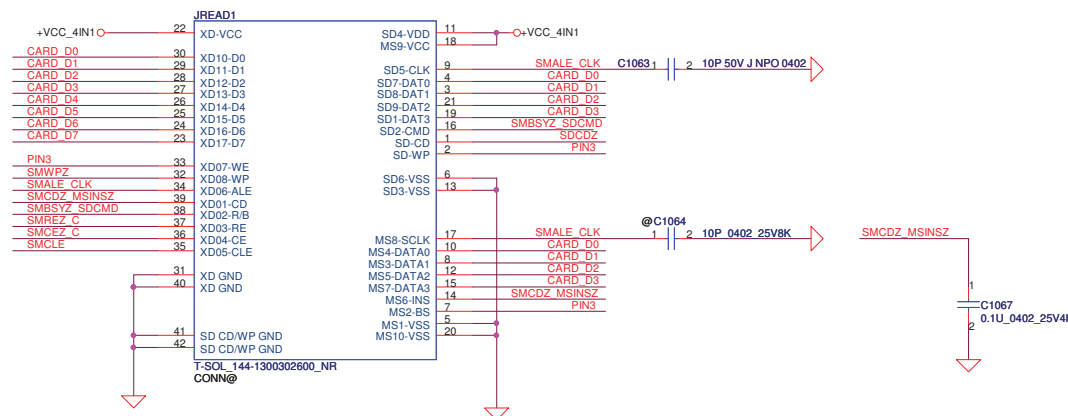
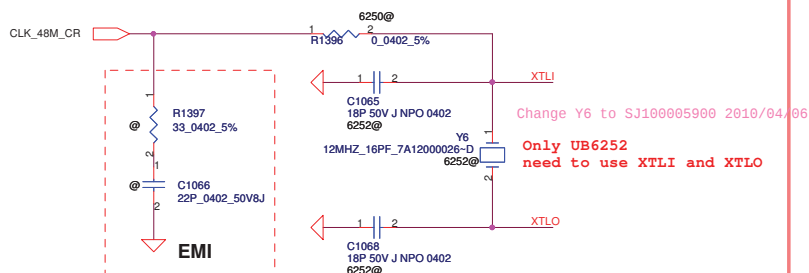
SMCEZ 1 2 VCC33

R1395 6252@
470_0402_5%

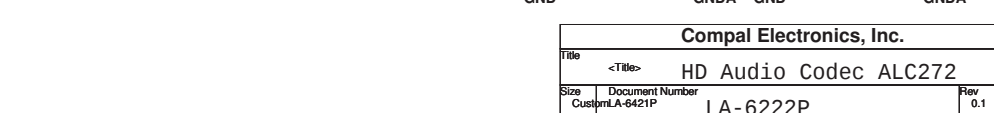
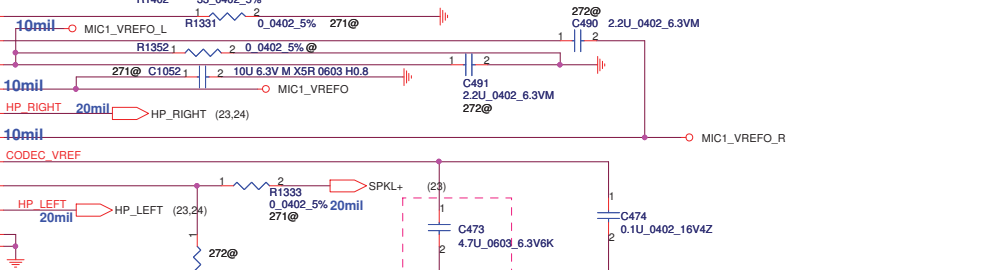
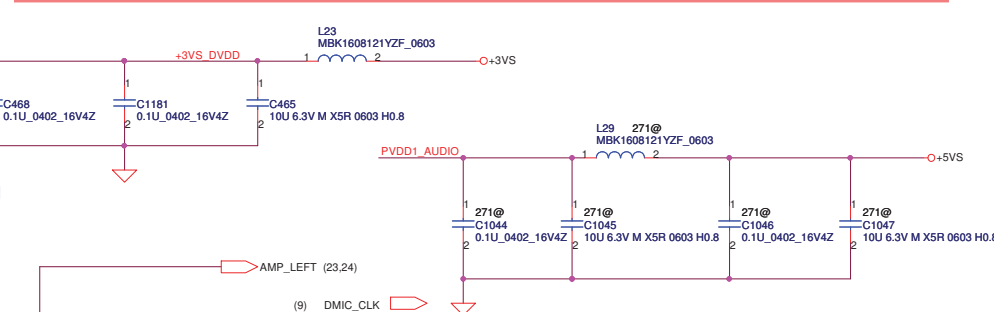
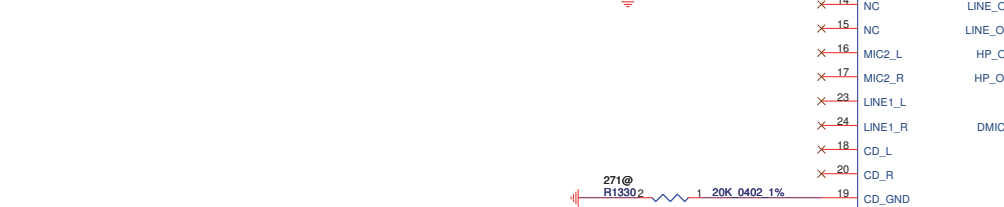
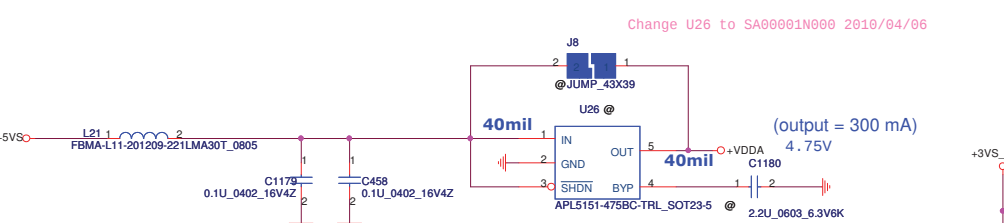
SMREZ 1 2 VCC33



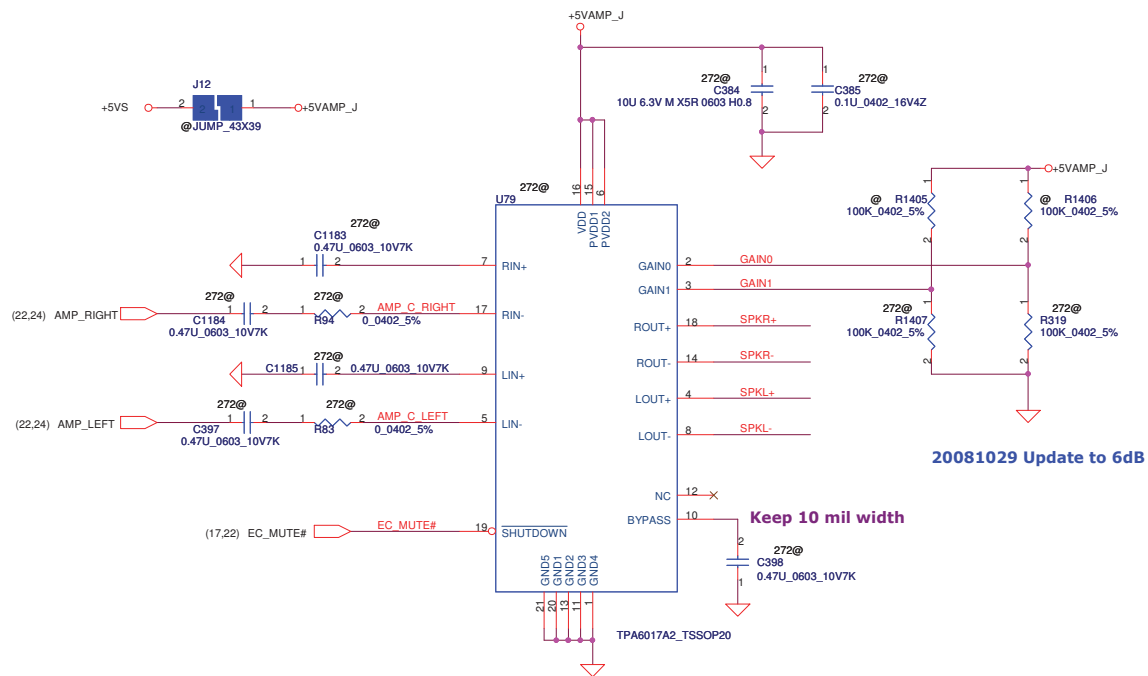
Card Reader Connector



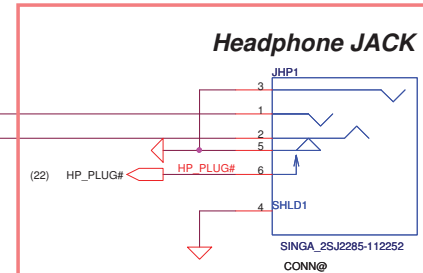
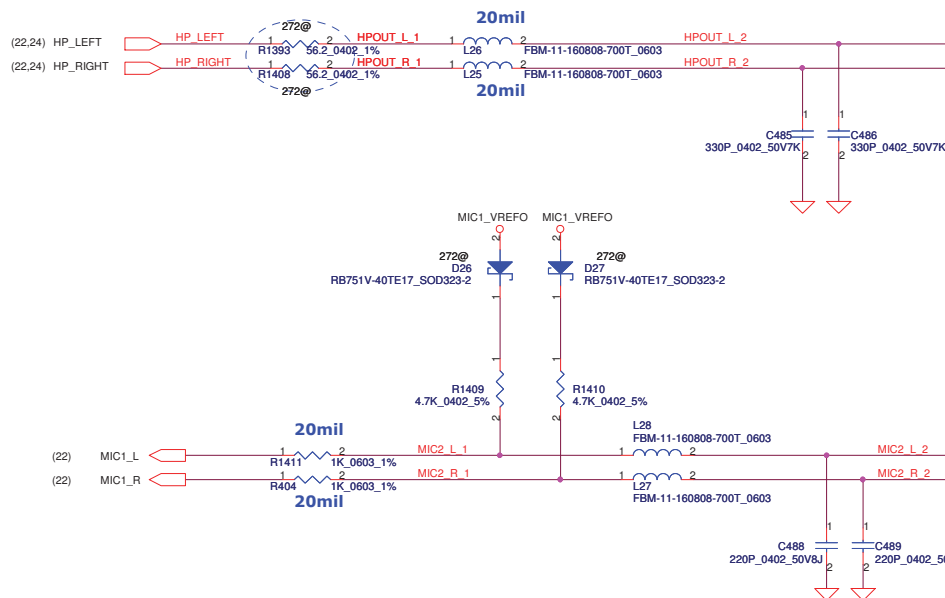
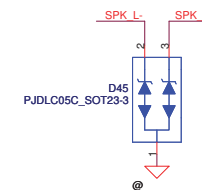
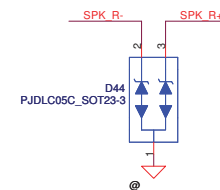
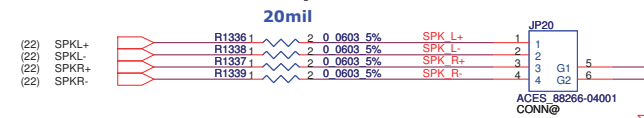
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/22	Deciphered Date	2009/11/20	Title	Card reader
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				Custom	LA-6421P
				Date:	Thursday, June 03, 2010
				Sheet	21 of 39



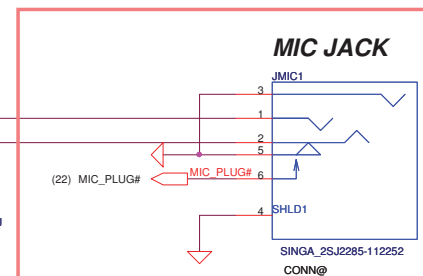
Compal Electronics, Inc.			
Title <Title> HD Audio Codec ALC272			
Size	Document Number	Rev	
Custom	LA-6421P	0.1	
Date:	Thursday, June 03, 2010	Sheet	22 of 39



Int. Speaker Conn.



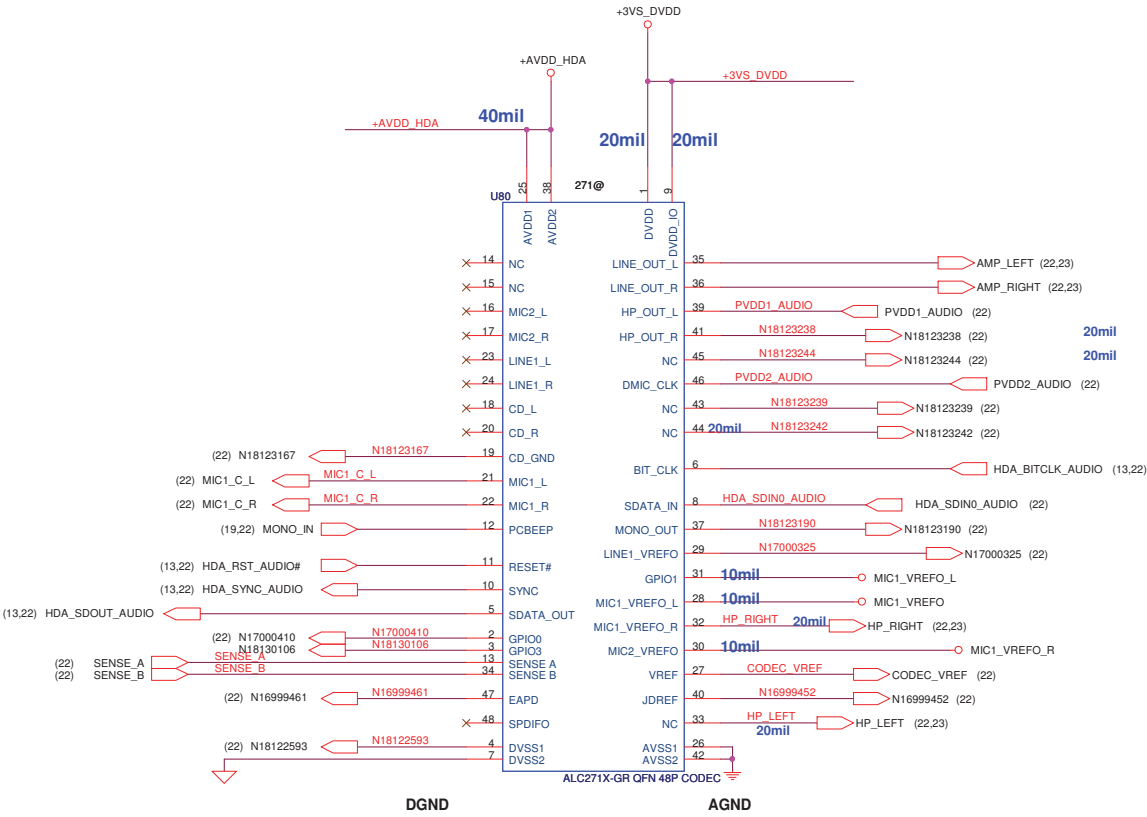
6/19 Update Headphone connector



6/19 Update MIC connector

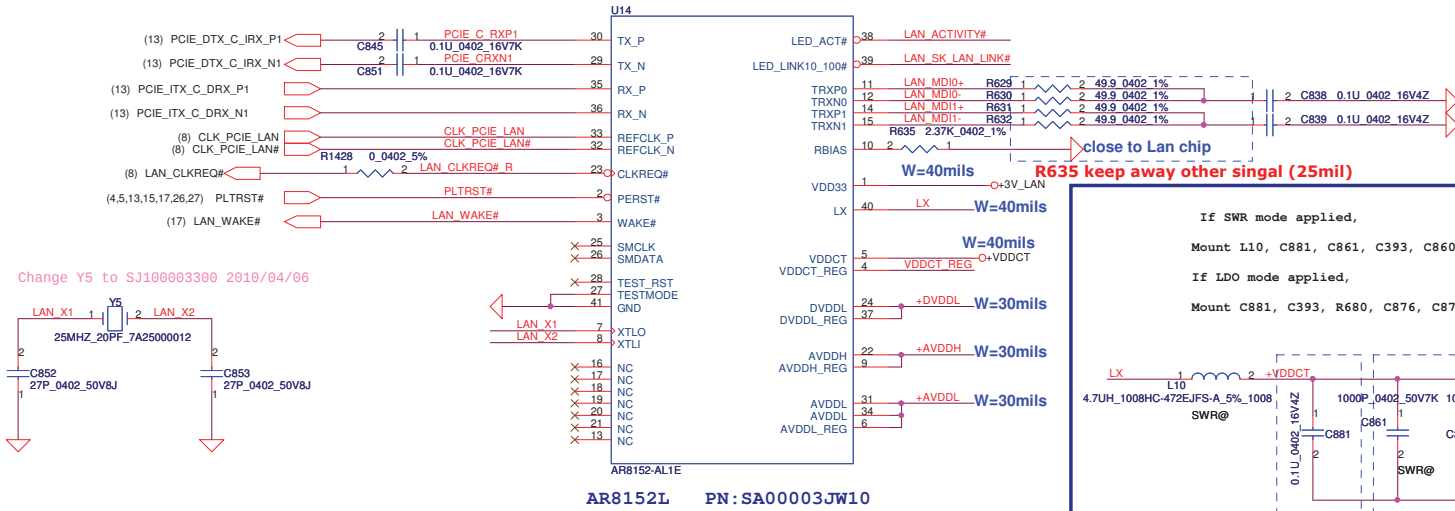
Compal Electronics, Inc.			
Title	<Title> Amplifier & Audio Jack		
Size	Document Number	Rev	
Custom	LA-6421P	LA-6222P	0.1
Date:	Tuesday, June 22, 2010	Sheet	23 of 39

HD Audio Codec

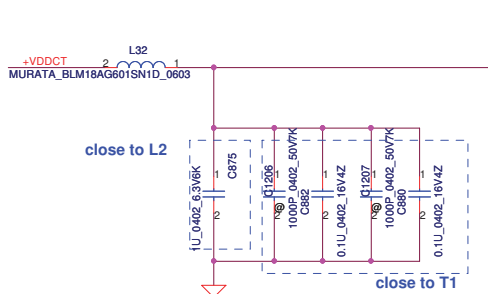
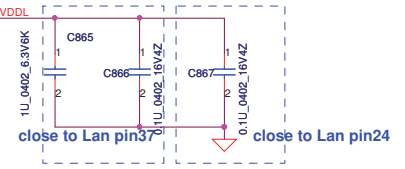
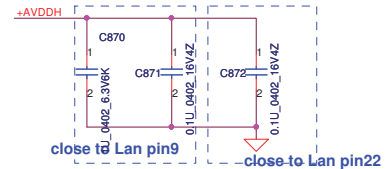
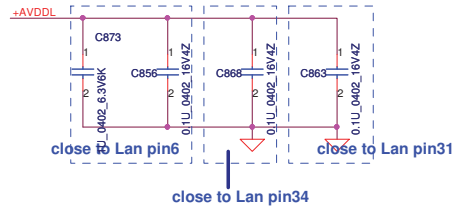
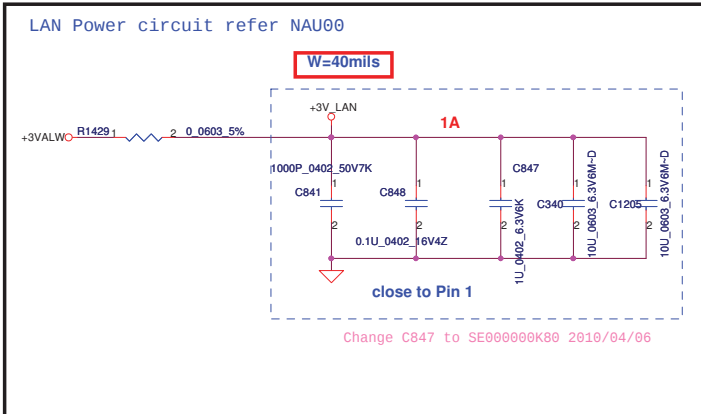


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

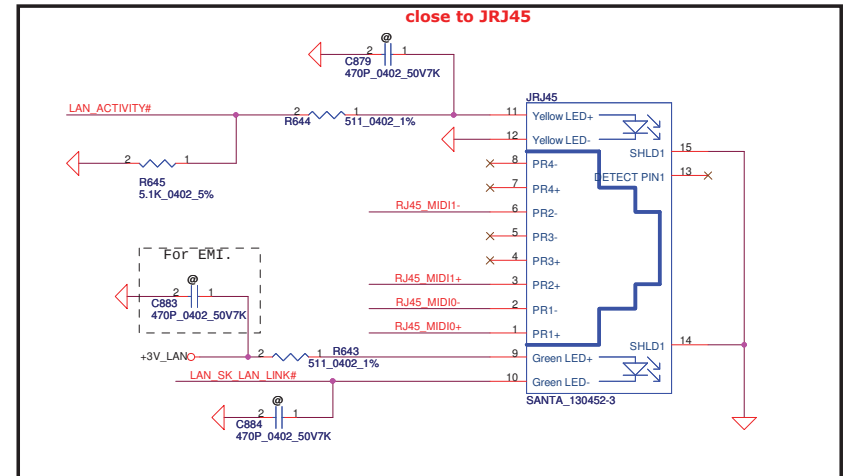
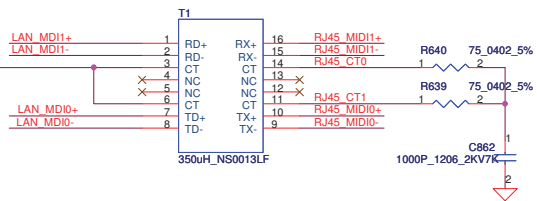
Change LAN chip to AR8152-L for NAV70/80 DDR3 2010/01/22



Change C865,C870,C873,C876 to SE000000K80 2010/04/06



Change C875 to SE000000K80 2010/04/06



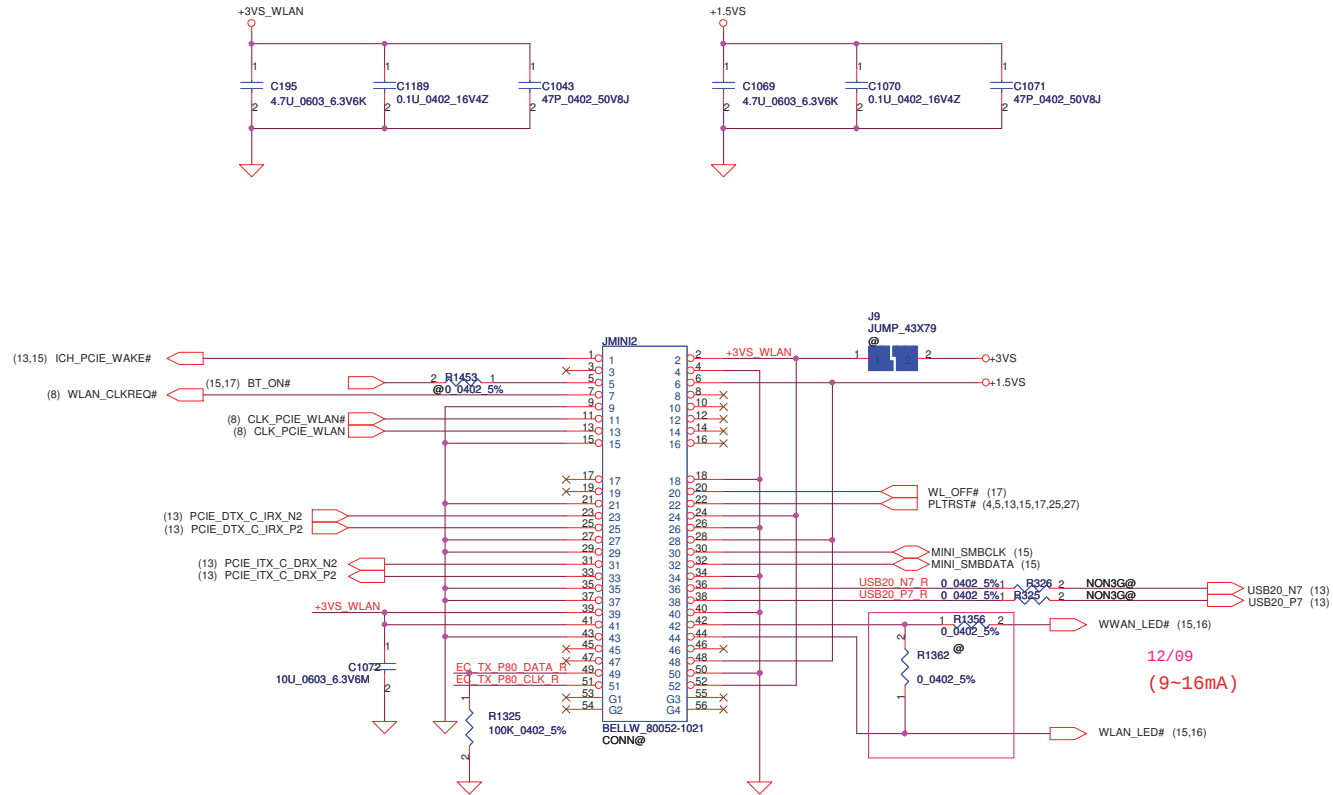
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/7/7	Deciphered Date	2010/7/7	Title	LAN AR8152
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				Custom	0.1
				Document Number LA-6421P	
Date: Thursday, June 03, 2010		Sheet		25	of 39

Mini-Express Card for WWAN

(17) EC_TX_P80_DATA
(17) EC_RX_P80_CLK

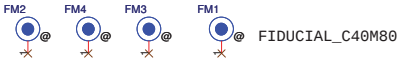
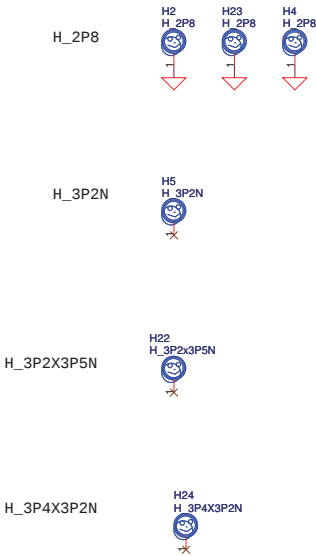
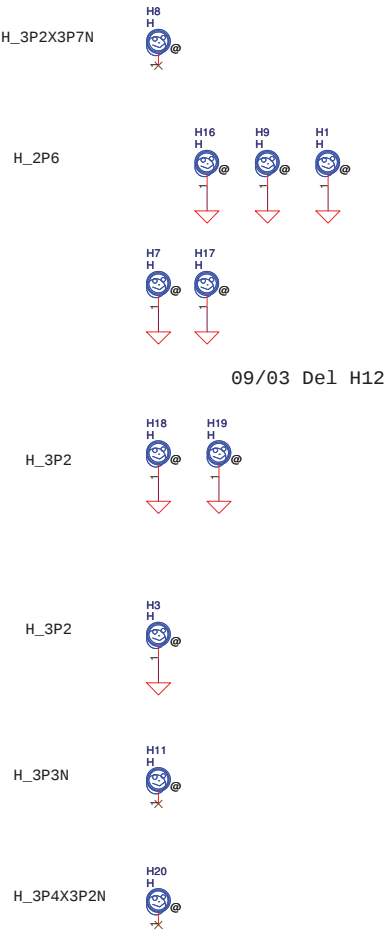
EC_TX_P80_DATA R402 0_0402_5%
EC_RX_P80_CLK R403 0_0402_5%

Mini-Express Card for WLAN



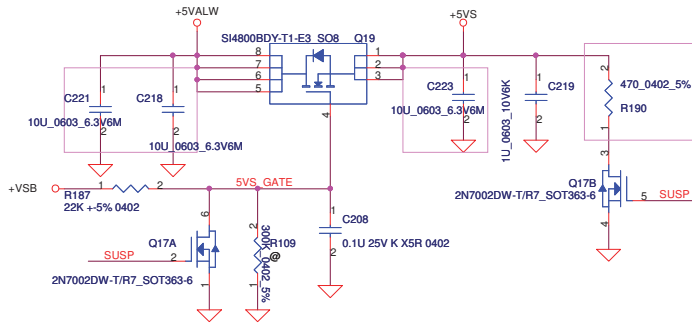
5/12 Update WLAN connector(the same as KAV60)
6/1 Revised 37、39、41、42、43 to NC
6/12 Update connector to DC040006S00
6/26 Update JMINI1 footprint
7/01 update pin 23,25,31,33

Modify Hole location by (ME Drawing 06/12) 0615

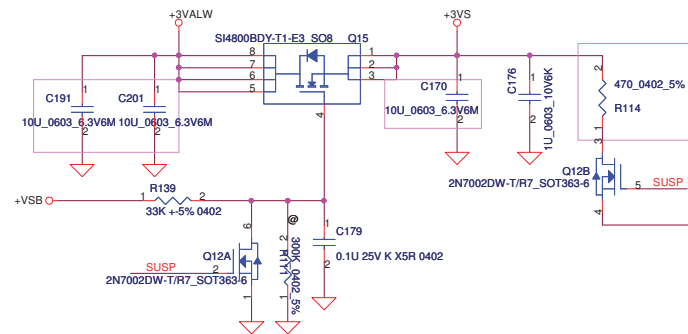


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2006/08/18	Deciphered Date	2007/8/18	Title
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Size B		Document Number		LA-6421P	
Date:		Thursday, March 25, 2010		Sheet 28 of 39	

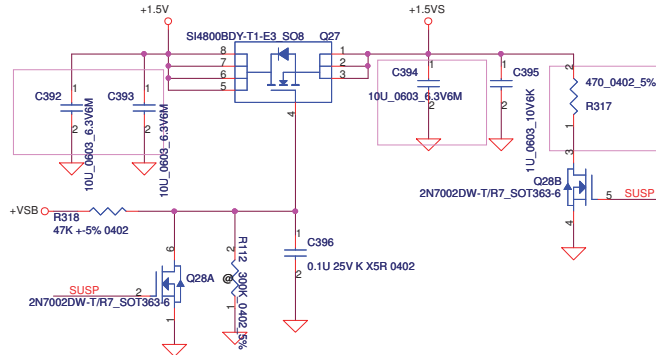
+5VALW TO +5VS



+3VALW TO +3VS

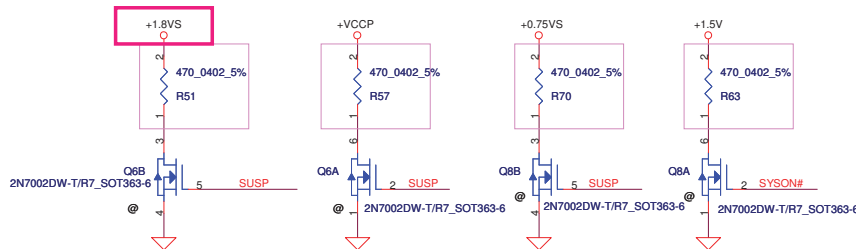
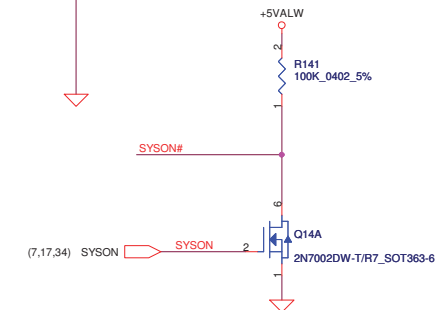
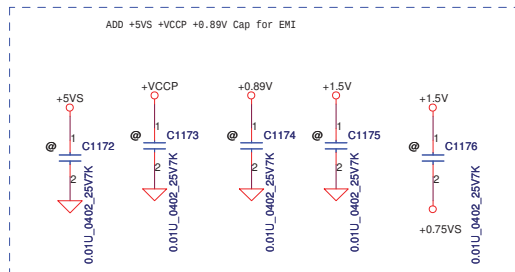


+1.5V to +1.5VS

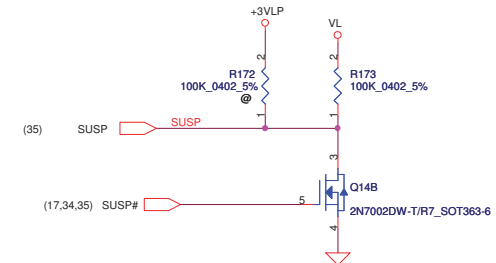


Change Q12,Q14,Q17,Q28 to SB00000DH00 2010/04/06

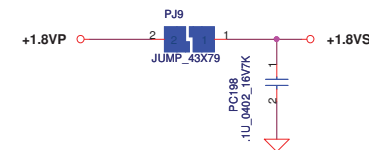
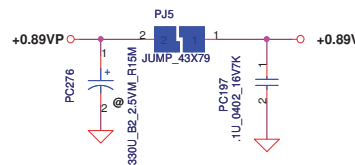
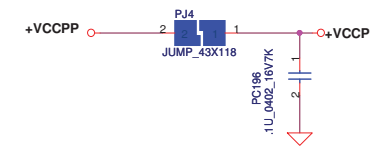
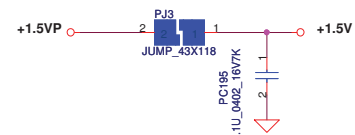
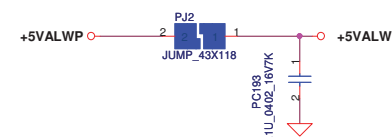
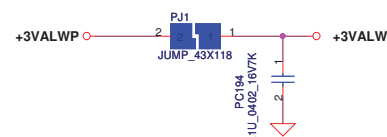
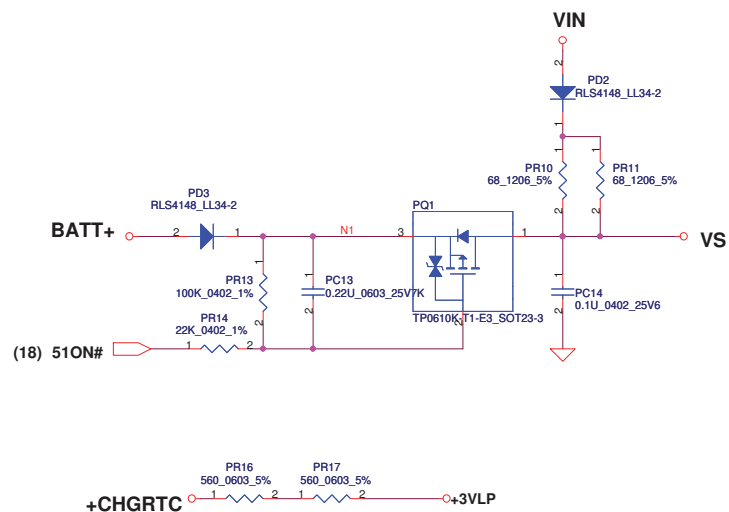
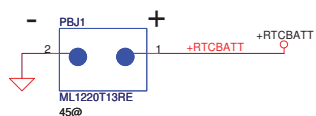
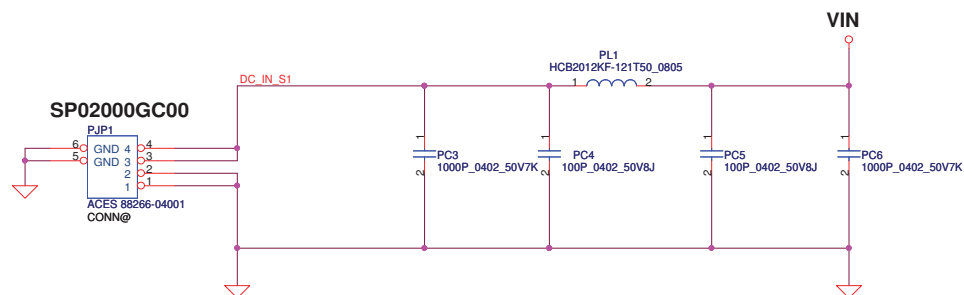
Change C176,C219,C395 to SE080105K80 2010/04/06



Change Q6,Q8 to SB00000DH00 2010/04/06

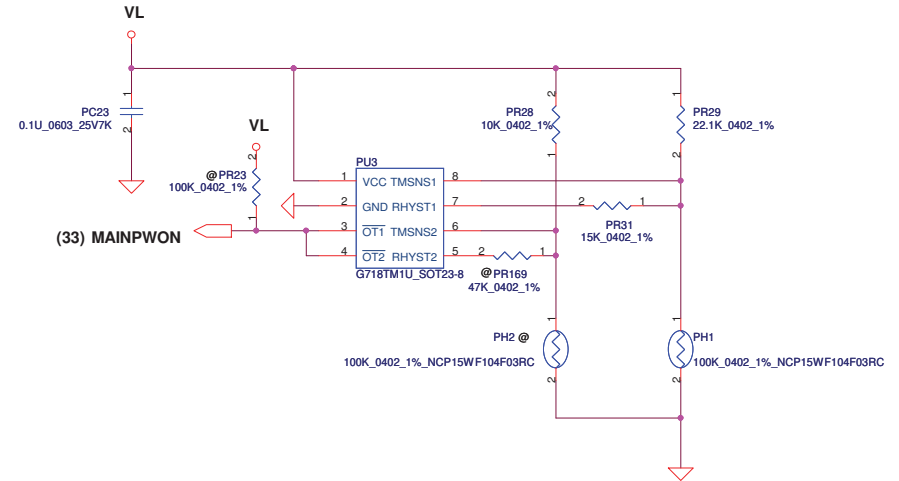
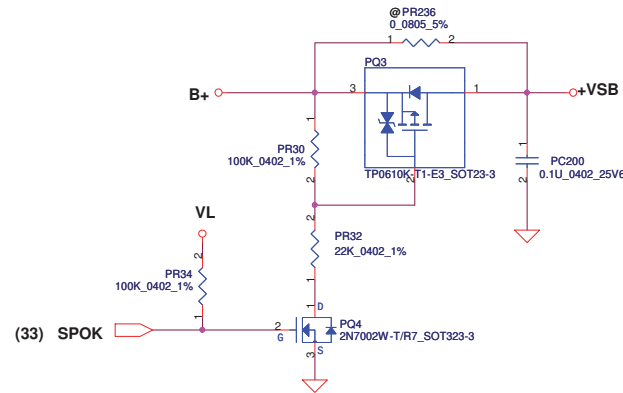
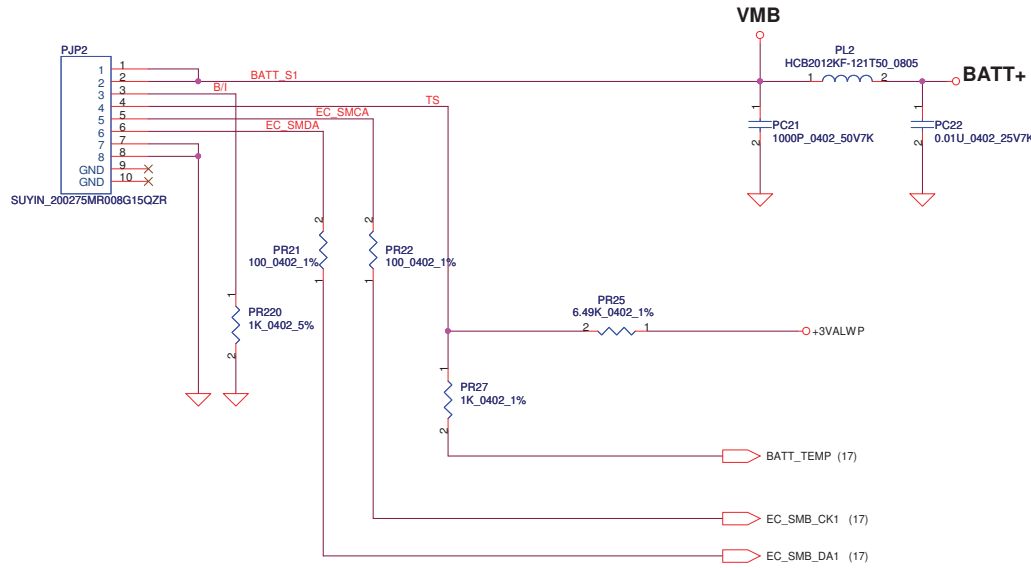


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						Size B	Document Number			LA-6421P		Rev 0.1
						Date	Thursday, June 03, 2010		Sheet	29	of	39

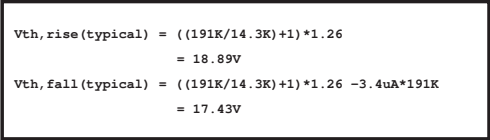


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				DCIN & DETECTOR					
				Size		Document Number		Rev	
				Custom		LA-6421P		0.1	
				Date:		Tuesday, June 22, 2010		Sheet 30 of 39	

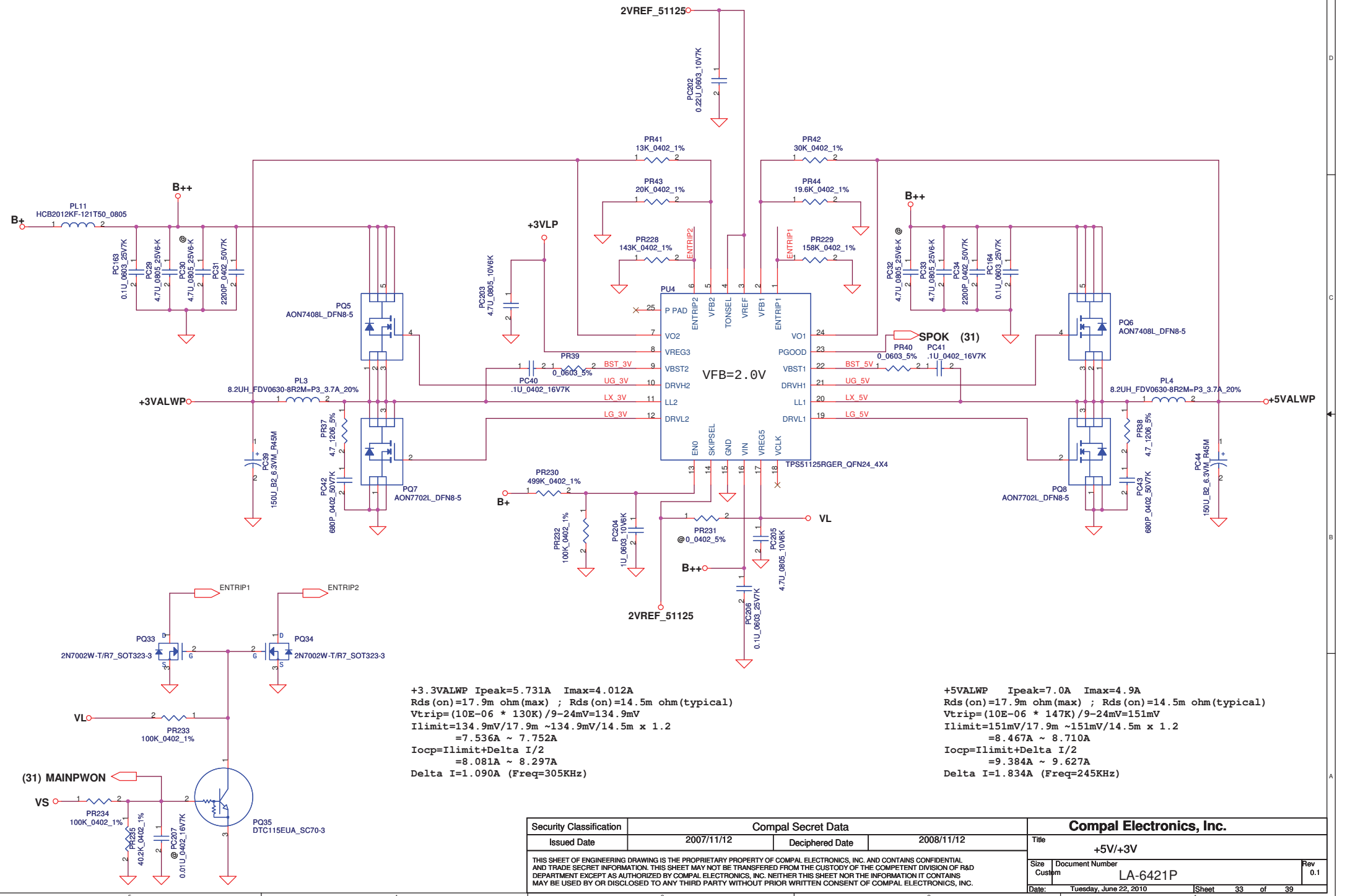
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C



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				Custom	LA-6421P
				Date:	Tuesday, June 22, 2010
				Sheet	31 of 39
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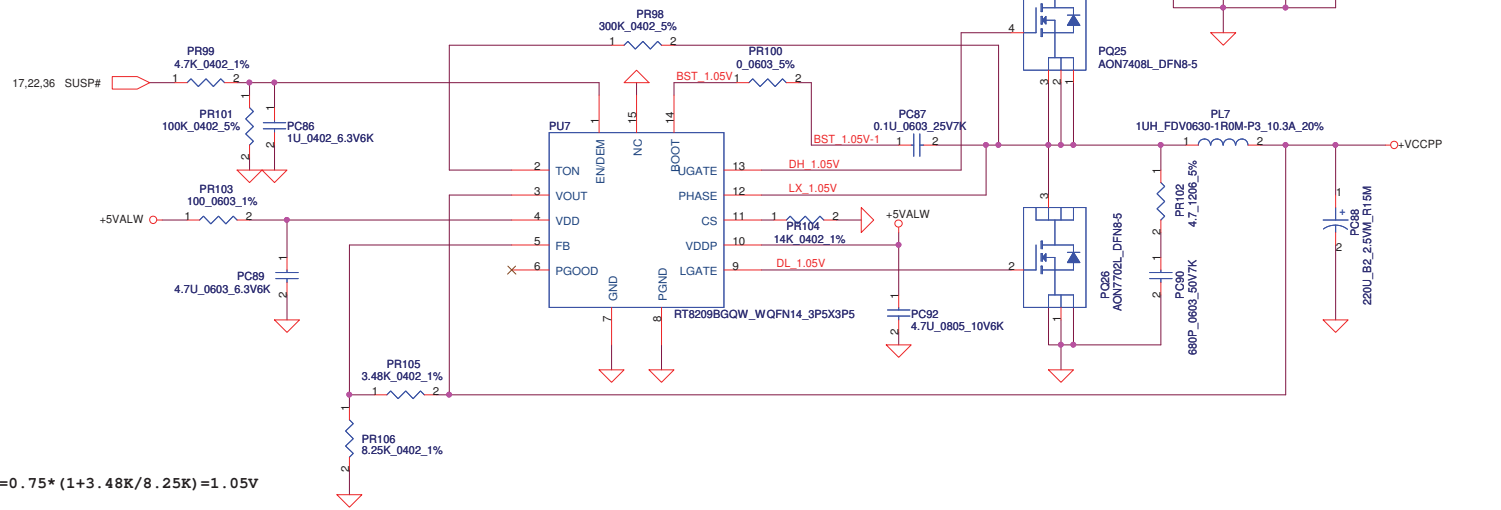
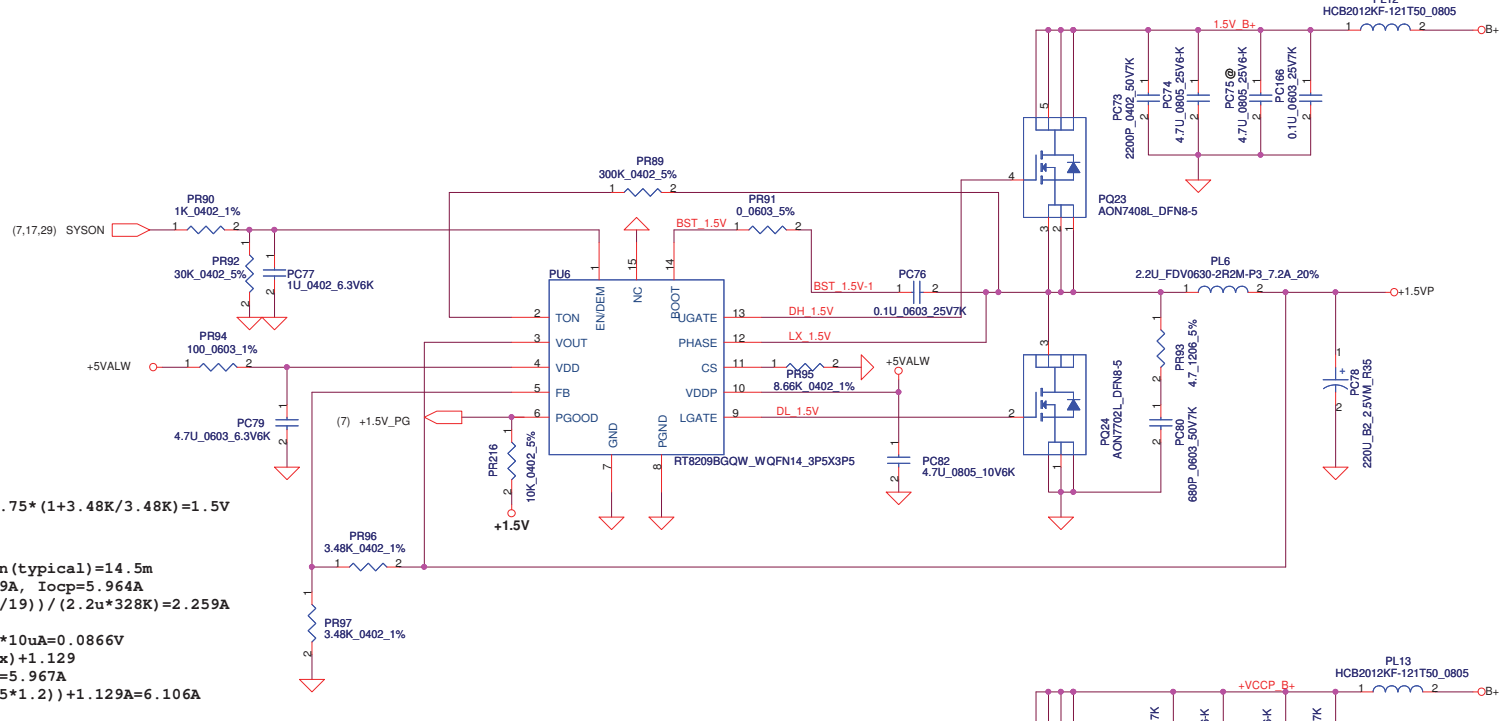
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	CHARGER	
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				Date:	Tuesday, June 22, 2010	Sheet 32 of 39



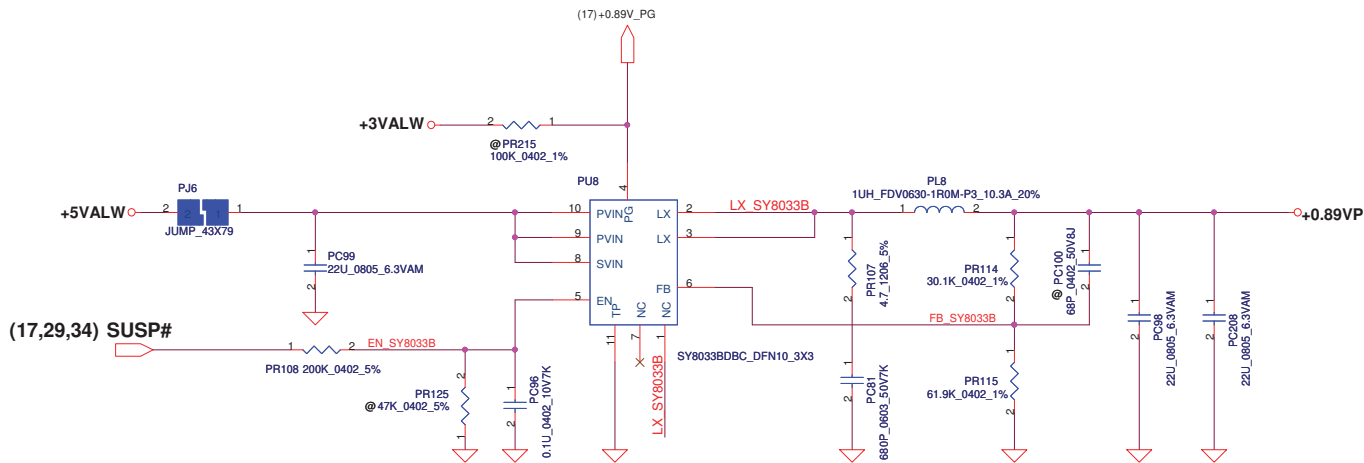
+3.3VALWP Ipeak=5.731A Imax=4.012A
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vtrip=(10E-06 * 130K)/9-24mV=134.9mV
Ilimit=134.9mV/17.9m ~134.9mV/14.5m x 1.2
=7.536A ~ 7.752A
Iocp=Ilimit+Delta I/2
=8.081A ~ 8.297A
Delta I=1.090A (Freq=305KHz)

+5VALWP Ipeak=7.0A Imax=4.9A
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vtrip=(10E-06 * 147K)/9-24mV=151mV
Ilimit=151mV/17.9m ~151mV/14.5m x 1.2
=8.467A ~ 8.710A
Iocp=Ilimit+Delta I/2
=9.384A ~ 9.627A
Delta I=1.834A (Freq=245KHz)

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		Size	Document Number						Rev
		Custom	LA-6421P						0.1
		Date:	Tuesday, June 22, 2010			Sheet	33	of	39



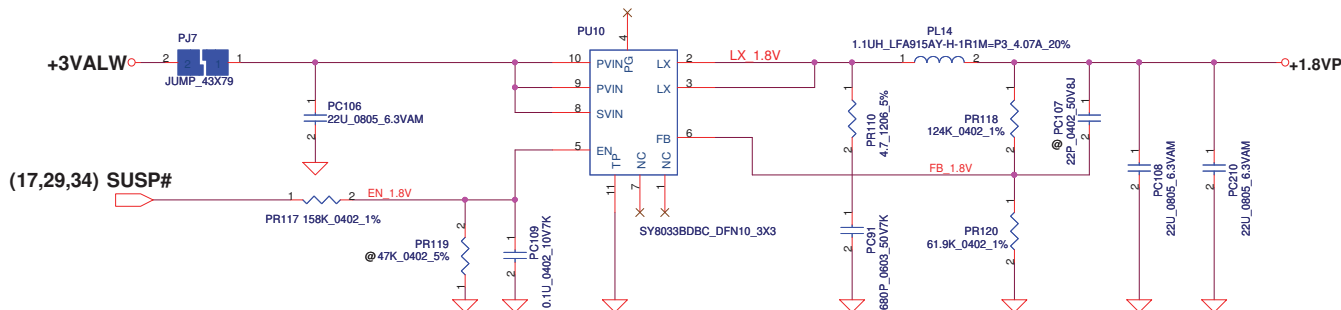
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	1.5VP / +VCCPP		
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$$\langle V_o = 0.89V \rangle \quad V_{FB} = 0.6V$$

$$V_o = V_{FB} * (1 + PR114 / PR115) = 0.6 * (1 + 30.1K / 61.9K) = 0.89V$$

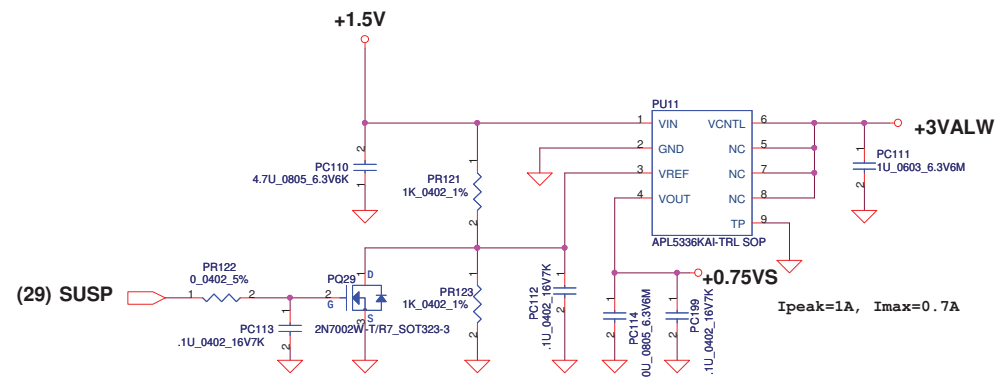
$$I_{peak} = 2.64A, \quad I_{max} = 1.848A$$



$$\langle V_o = 1.8V \rangle \quad V_{FB} = 0.6V$$

$$V_o = V_{FB} * (1 + PR118 / PR120) = 0.6 * (1 + 124K / 61.9K) = 1.8V$$

$$I_{peak} = 0.318A, \quad I_{max} = 0.223A$$



$$I_{peak} = 1A, \quad I_{max} = 0.7A$$

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Size Custom	Document Number	LA-6421P		Rev 0.1
Date:	Tuesday, June 22, 2010	Sheet	35	of 39

Version change list (P.I.R. List)

Page 1 of 1 for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change power solution	For design change	0.1	34	Change PU7 from SA000031D00(S IC RT8209BGQW WQFN 14P PWM) to SA00003RU00(S IC SY8033BDBC DFN 10P SINGLE BUCK)	2010.5.03	DVT
2	Change PU8 SY8033B Pin1 net	For design change	0.1	34	Change PU8 SY8033B Pin1 connect Pin2 & Pin3	2010.5.03	DVT
3	Change PC100	For design change	0.1	34	Change PC100 to SE071680J80 (S CER CAP 68P 50V J NPO 0402)	2010.5.03	DVT
4	Change PR105	For design change	0.1	32	Change PR105 from SD034100200(S RES 1/16W 10K +-1% 0402) to SD034100280 (S RES 1/16W 10K +-1% 0402)	2010.5.13	DVT
5	Change PC30 & PC32 to non-pop	For cost down plan	0.1	33		2010.6.2	PVT
6	Change PL3,PL4,PL5,PL6,PL7,PL8, PL10,PL14	For TMP choke shortage issue	0.1		Change PL3,PL4,PL5 from SH00000J100 to SH00000BS00 Change PL6,PL10 from SH00000FD10 to SH000000700 Change PL7,PL8 from SH00000J300 to SH000007N00 Change PL14 from SH00000IS00 to SH00000HY00	2010.6.2	PVT
7	Change power solution	For design change	0.1	34	Change PU7 from SA00003RU00(S IC SY8033BDBC DFN 10P SINGLE BUCK) to SA000031D00(S IC RT8209BGQW WQFN 14P PWM)	2010.6.8	PVT
8	Change PD10.PD13.PC58.PR64. PQ18 to non-pop Change PR84 to pop	For cost down plan	0.1	33		2010.6.10	PVT
9	Modify CPU CORE OCP for N550	Design change for N550 CPU	0.1	32	Add PR209 = SD034357180 (3.57K_0402_1%) @N550 PR209 = SD034357180 (2.37K_0402_1%) @N4XX series	2010.6.10	PVT
10							
11							
12							
13							
14							
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				Size Custom	Document Number LA-6421P
Date:				Tuesday, June 22, 2010	
				Sheet 37 of 39	

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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<2010/03/25>
. P06 - Add C1217, C1218 for +0.89V
. P08 - Add R1442, R1443
. P09 - Add R1444, R1445 for DMIC
. P10 - L12, L14, L15 change to SM010000200
. P23 - Add JP24 for cardreader connector

<2010/06/28>
. P04 - Change C239 BOM structure to 3G@
. P17 - Change C528, C530, C531 BOM structure to 3G@

<2010/03/26>
. P27 - Add R1448, R1449, R1450,R1451,R1452
JP22 change to SP02000H500

<2010/04/06>
. P10 - Change L12. L14, L15 to SM01000C600
. P26 - Add R1453
. P21 - Change Y6 to SJ100005900
. P25 - Change Y5 to SJ100003300
Change C847,C865,C870,C873,C875,C876 SE000000K80
. P13 - Change X1,Y3,Y7 to SJ132P7KW10
. P22 - Change U26 to SA00001N000
. P29 - Change Q6,Q8,Q10,Q12,Q14,Q17,Q24,Q28 to SB00000DH00
Change C176,C219,C230,C395 to SE080105K80
. P07 - Change C116,C141 to SE076104K80

<2010/04/14>
. P06 - Del C1218 2010/04/14
. P08 - Del C1219, R1442 change Y1 to SJ100009H00
. P27 - Add TPM@ GSEN@ for PAV70

<2010/05/03>
. P04 - R354, R347, R348 nu-mount
. P13 - Change R152 to SD034226A80(22.6ohm_0402)
. P13 - Change R241 to SD028100280(10Kohm_0402)
. P13 - R1376, R1377 nu-mount
. P16 - Add JBATT1 CONN.
. P17 - Change U76 to SA00001V400
. P17 - Change R1292 to SD028820180

<2010/05/04>
. P16 - Change JBATT1 NET to +RTCBATT1
. P27 - Add J15, J16

<2010/05/06>
. P10 - Change L12, L14 and L15 footprint
. P27 - Del J15, J16 ; Add R1457, R1458
. P27 - U81.15 connect to GND

<2010/05/24>
. P04 - Change U71 to SA00003WBA0(N475@) and SA00003WAB0(N455@)
. P08 - Change C161, C164 to SE071330J80(33P 50V J NPO 0402)
. P08 - Change C388 to SE071100J80(10P 50V J NPO 0402)
. P22 - Change C473 to SE107475K80(4.7U 6.3V K X5R 0603)

<2010/06/01>
. P13 - Add NET: EC_CLK
. P17 - Add R1459, R1460 for Reserve EC_CLK
. P17 - Change U6.36 NET to PWR_LED1#
. P18 - Change NET from PWR_LED# to PWR_LED1#

<2010/06/07>
. P06 - Change C239 footprint to 0805 size
. P17 - Del JP23
. P26 - Change R1325 to 100k-ohm

<2010/06/25>
. P04 - Change C311 BOM configure to un-mount
. P09 - Change C1109, C1111, C1112, C1156 BOM configure to 3G@
. P15 - Change C1163-C1166, C504-C508, C850 BOM configure to MCP@
. P17 - Change C528, C530, C531 BOM configure to un-mount
. P10 - Change D17, D18 BOM configure to un-mount
. P22 - Change D22 BOM configure to un-mount
. P23 - Change D44, D45 BOM configure to un-mount

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