Compal Confidential

PAU30 M/B Schematics Document

Intel Arrandale Processo SV with DDRIII + Ibex Peak-M

ZZZ
DAZ@
DAZ0F900100
PCB PAU30 LA-6392P LS-6391P/6392P/6393P/6394P

ZZZ1
DA1@
DA80000KE10
PCB 0F9 LA-6392P REV1 M/B

ZZZ2
DA2@
DA20000KT10
PCB 0F9 LS-6391P REV1 POWER_BTN/B

ZZZ3
DA2@
DA20000KU10
PCB 0F9 LS-6392P REV1 SWITCH/B

ZZZ4
DA2@
DA20000KV10
PCB 0F9 LS-6393P REV1 LED/B

ZZZ5
DA2@
DA20000LE10
PCB 0F9 LS-6394P REV1 LID SWITCH/B

2010-11-22

REV:1.0

Security Classification	Compal Secret Data		
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Title: Cover Page

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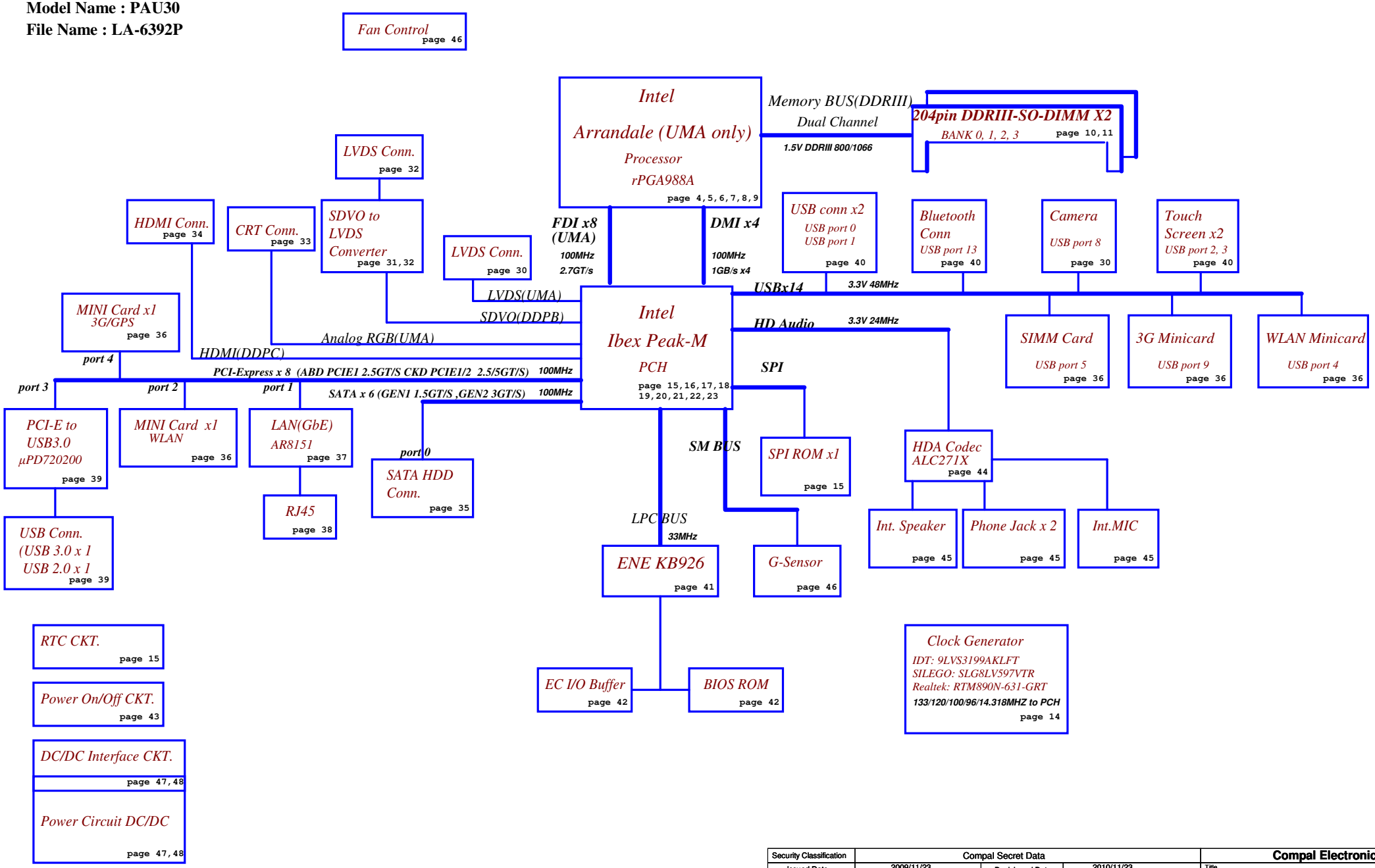
Model Name : PAU30
File Name : LA-6392P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

43level BOM Config

P/N	Des.	BOM Config
431954BOL01	SMT MB A6392 PAU30 W/3G	DAZ@

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VRAM	
VRAM	X76@
Connector	CONN@
Ventura	VENTURA@
Blue Tooth	BT@
Unpop	@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/Touch Screen2
		3	USB/Touch Screen1
	UHCI2	4	Mini Card(WLAN)
		5	SIMM CARD
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Mini Card(3G)
	UHCI5	10	
		11	
	UHCI6	12	
		13	Blue Tooth

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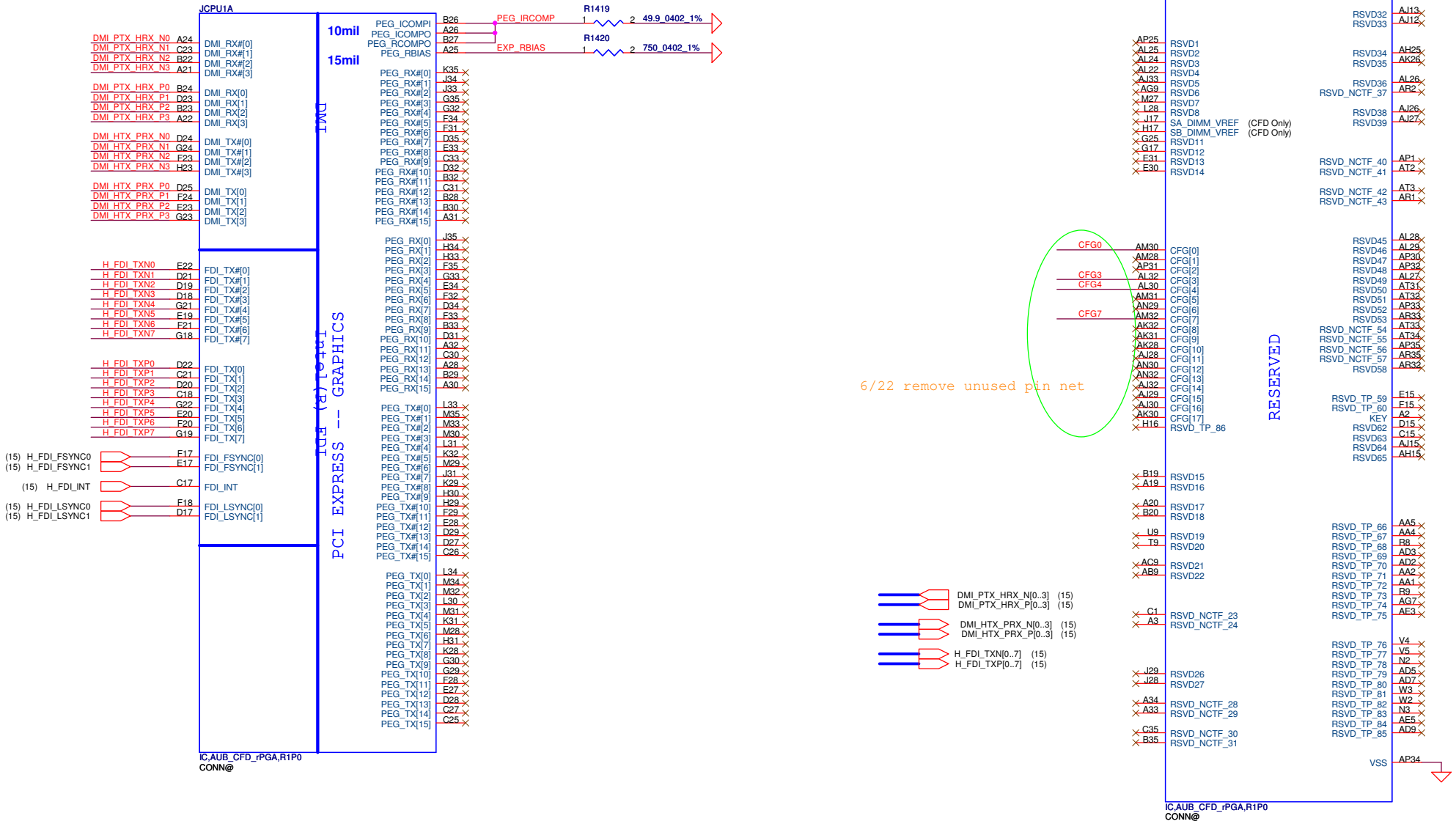

eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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Compal Electronics, Inc.

Title: PROCESSOR (1/6) DMI,FDI,PEG

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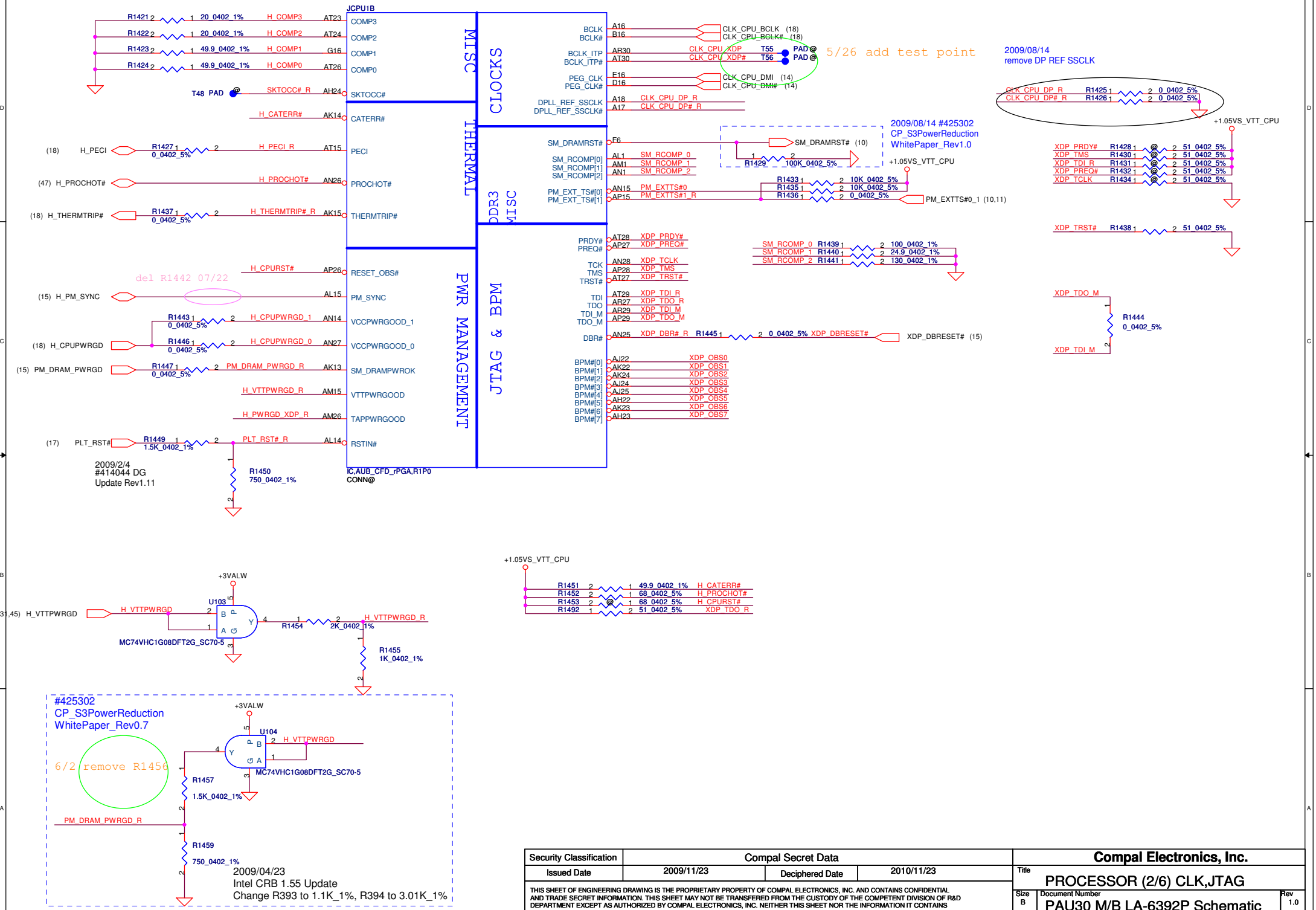

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Compal Electronics, Inc.

Title: PROCESSOR (2/6) CLK,JTAG

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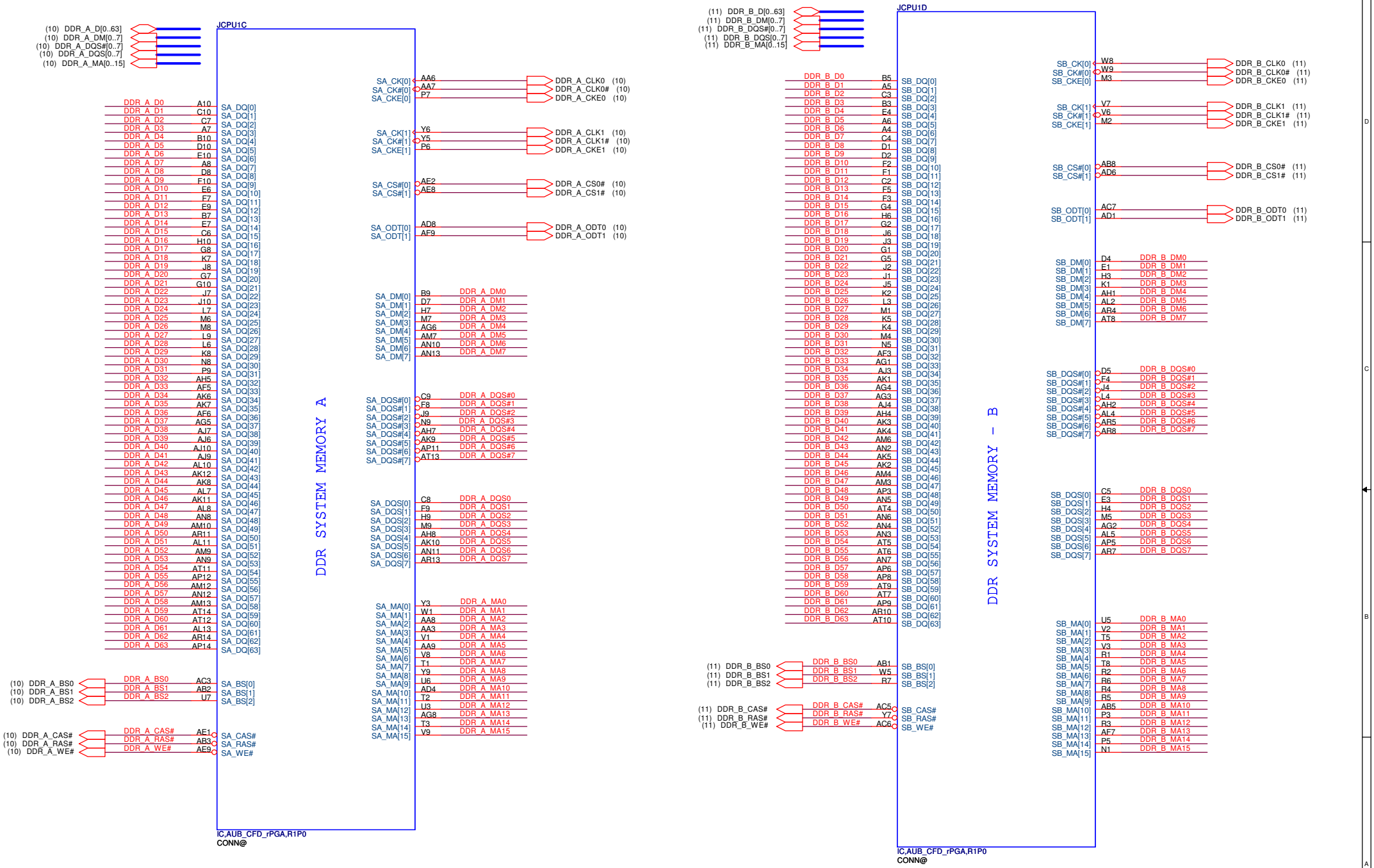

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Compal Electronics, Inc.

Title: PROCESSOR (3/6) DDRIII

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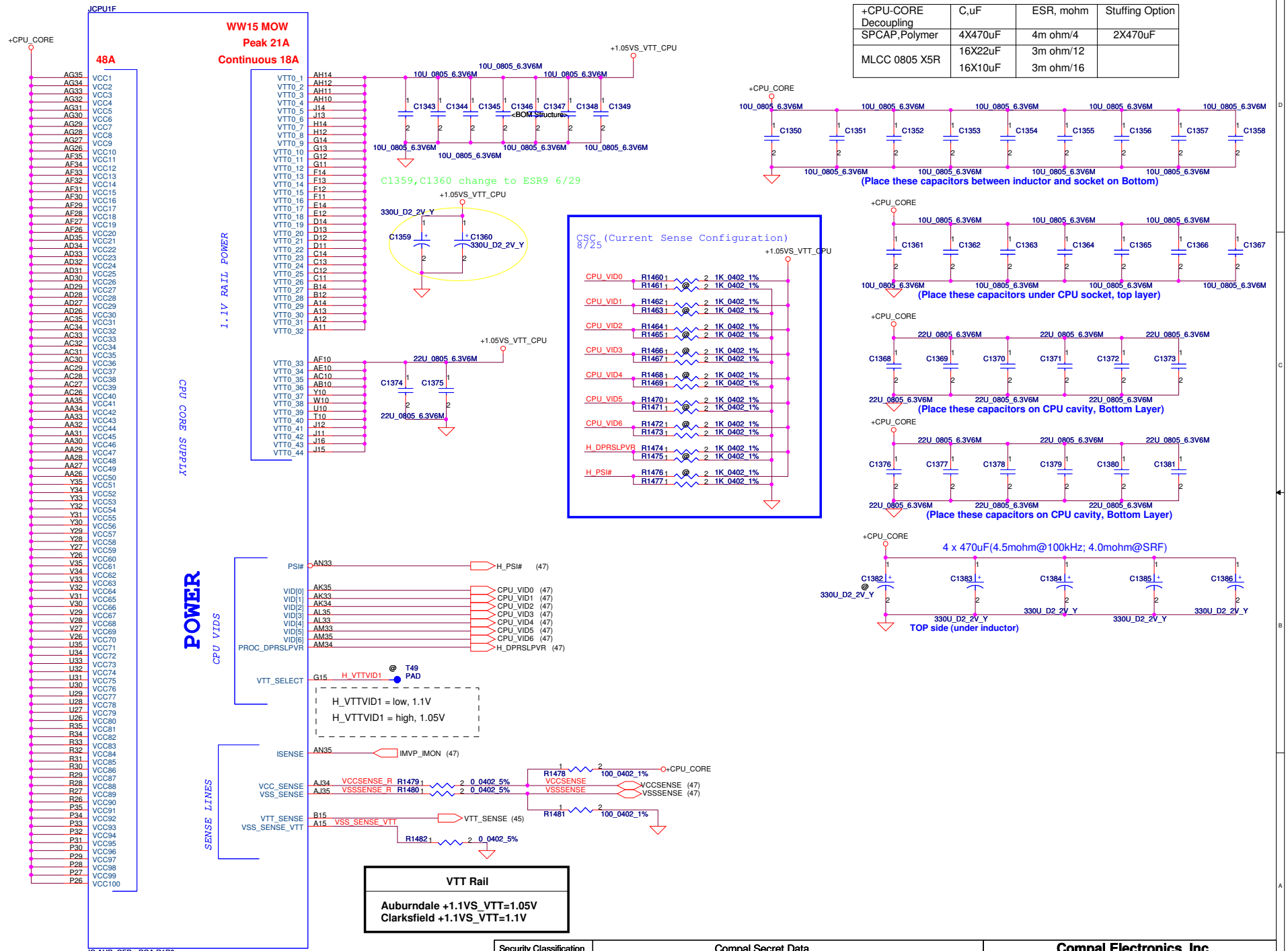

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

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Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

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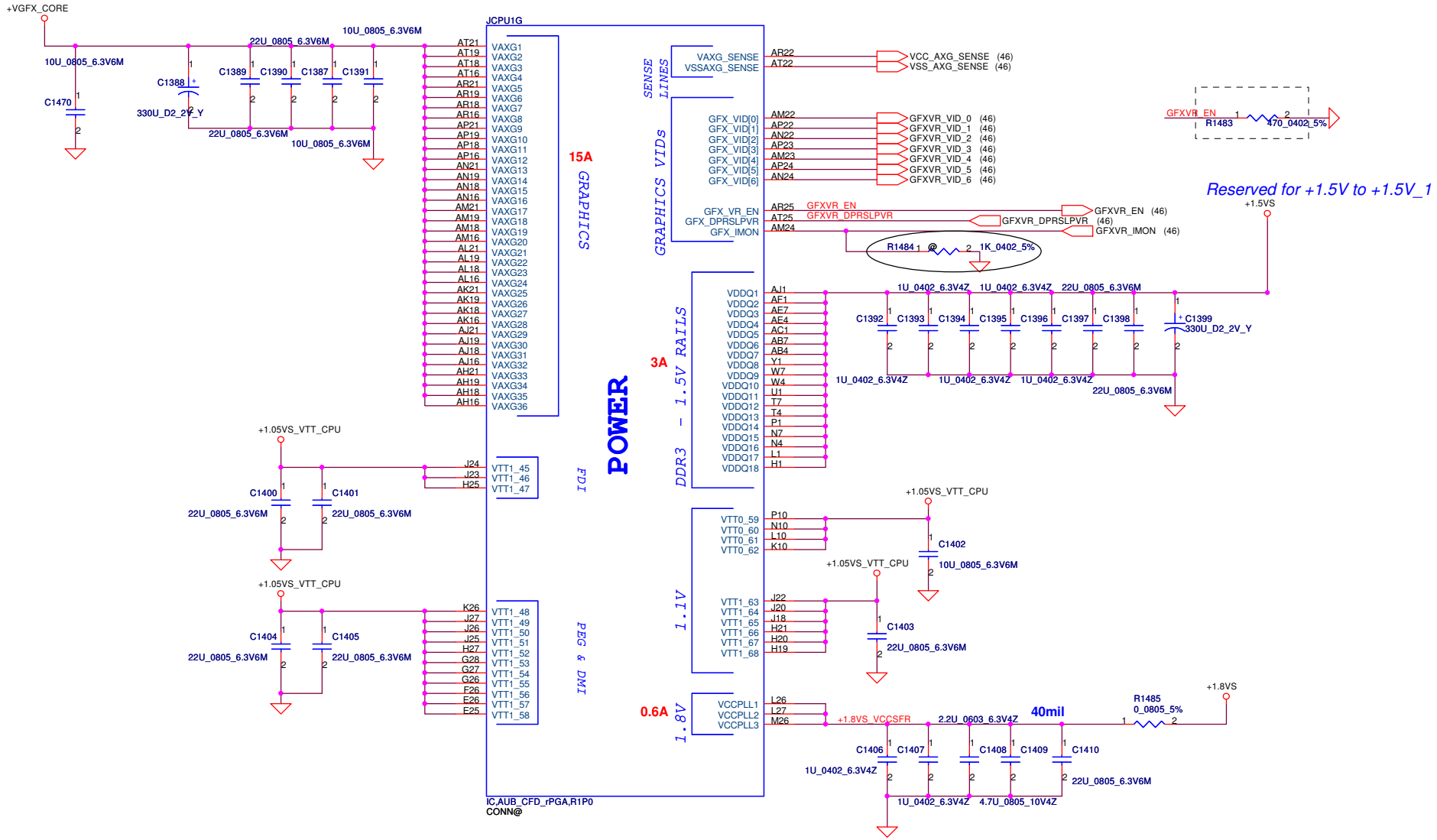

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Compal Electronics, Inc.

Title: PROCESSOR (5/6) PWR

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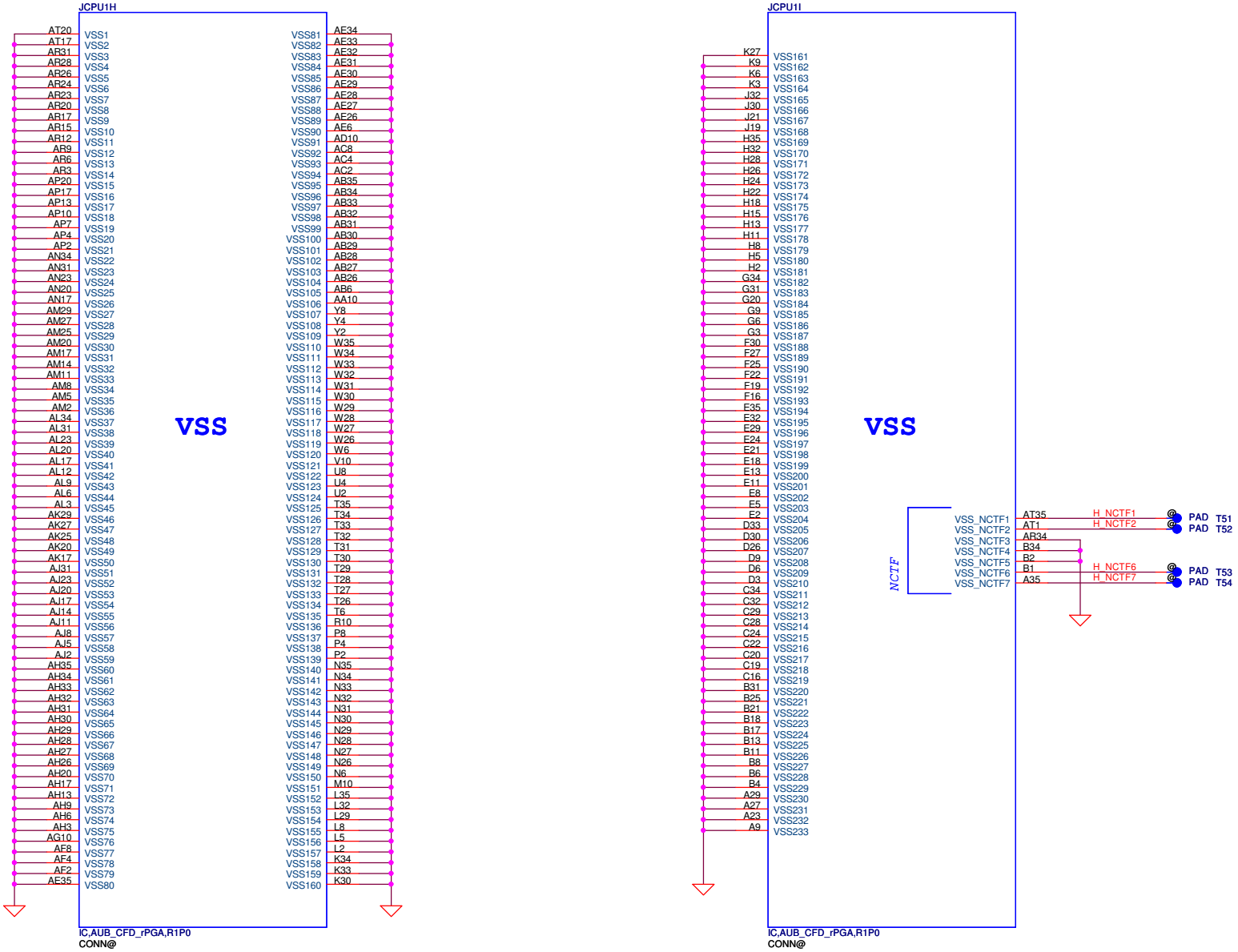

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Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS

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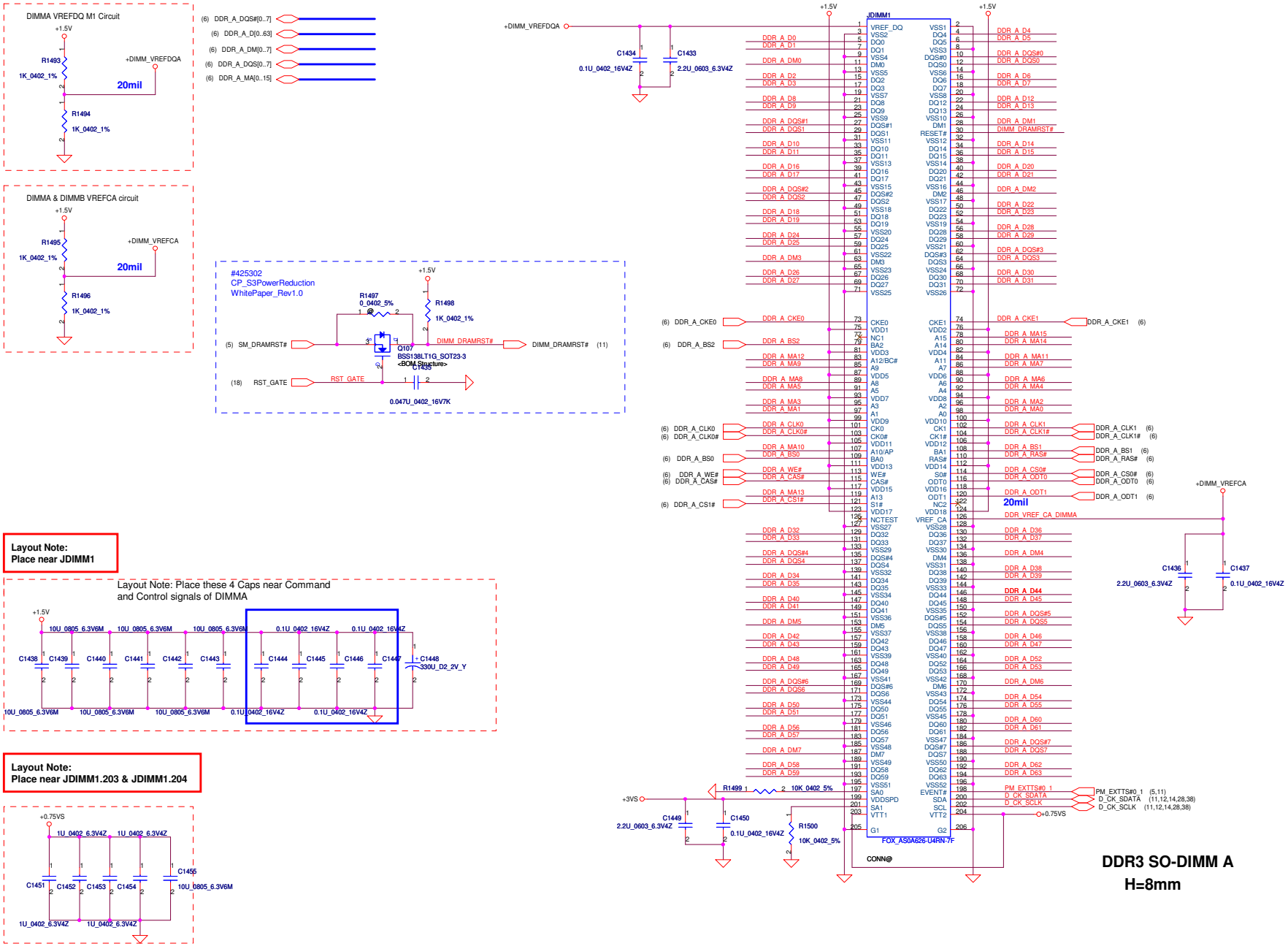

DDR3 SO-DIMM A

H=8mm

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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size: C | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 1.0

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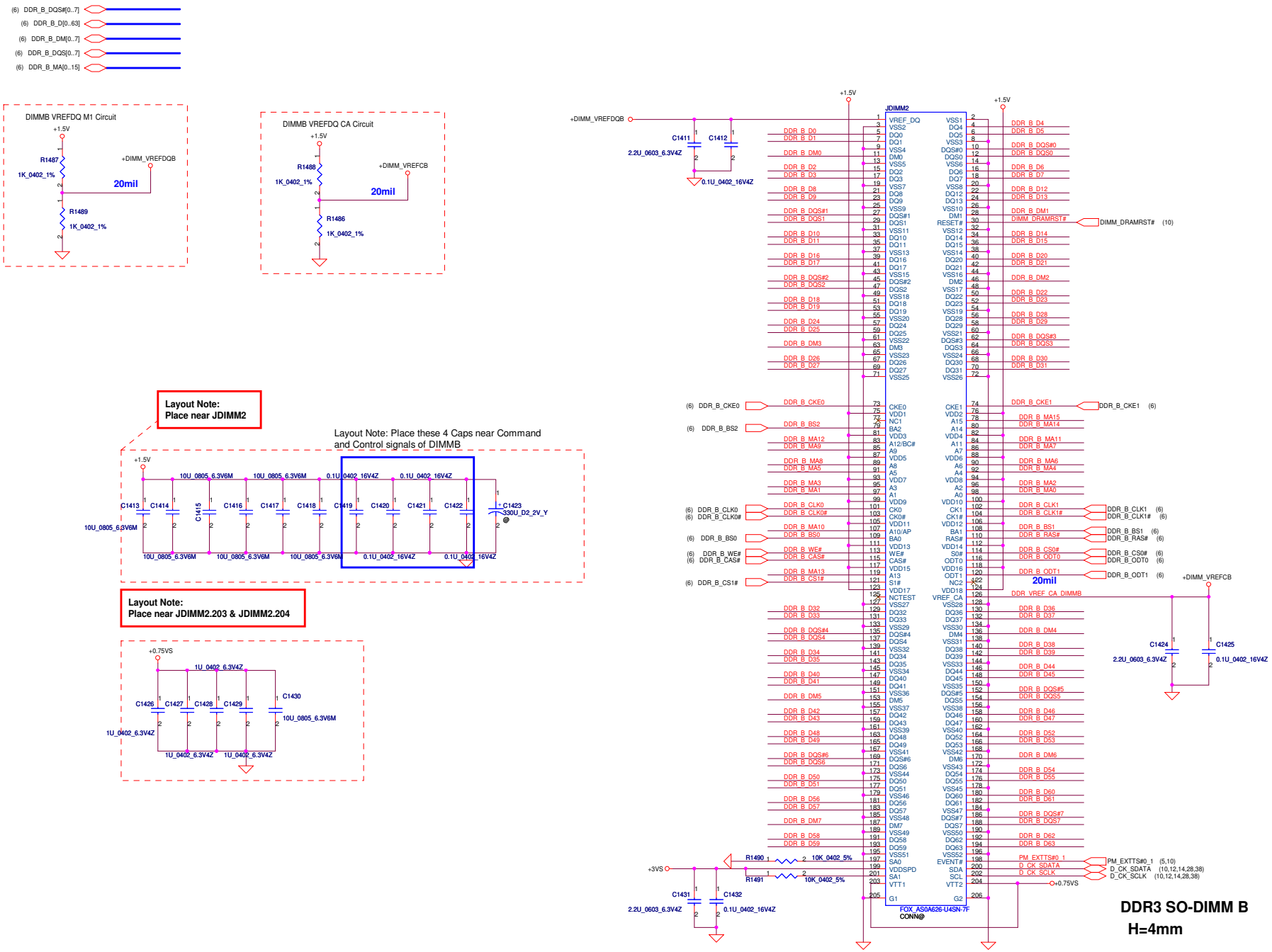

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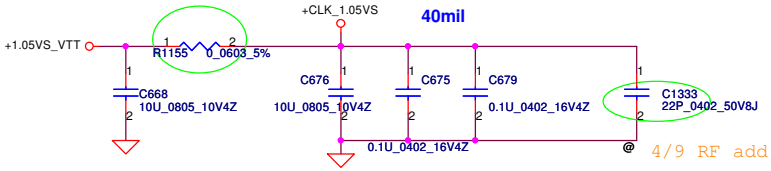
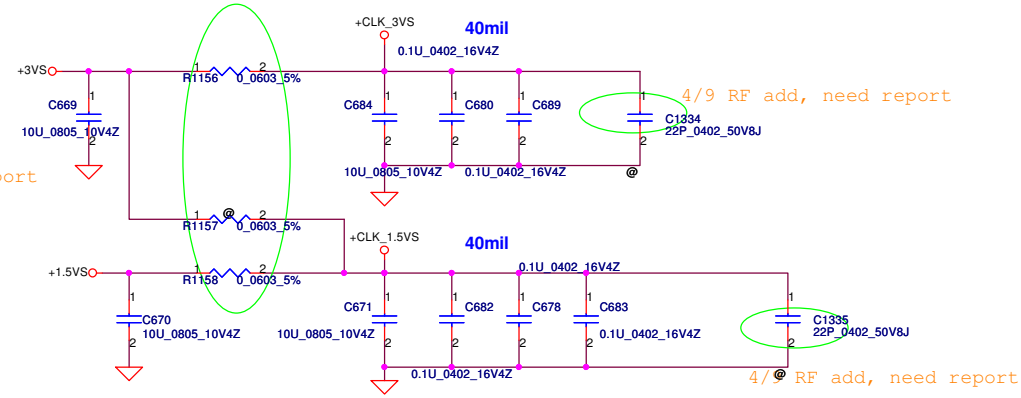
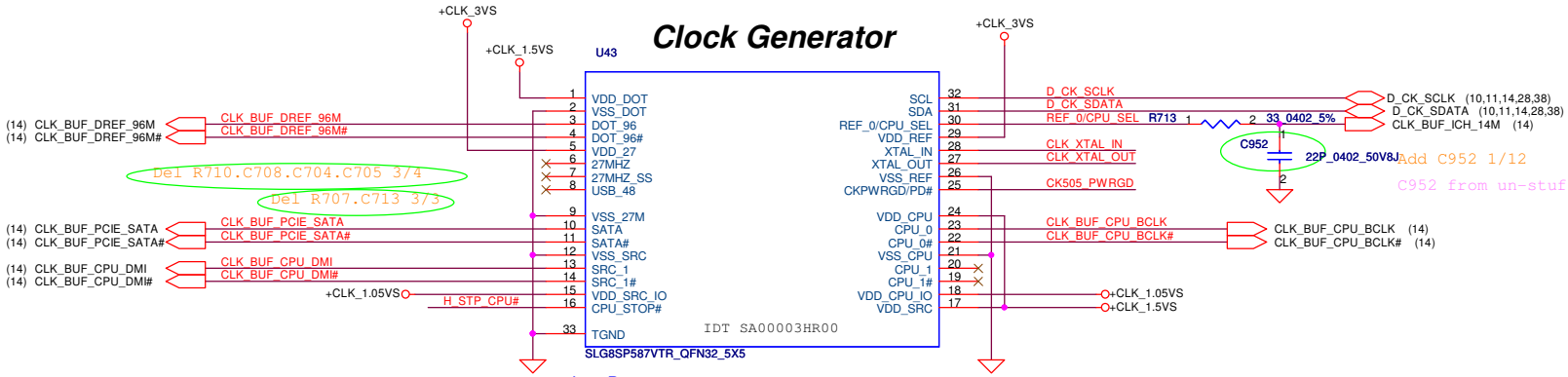


L44 Change 0 Ω 0603 2/1



L45.L46.L48 Change 0 Ω 0603 2/1

Clock Generator



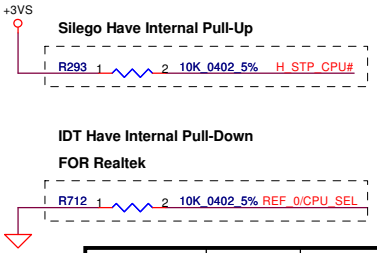
Low Power:

IDT: 9LVS3199AKLFT, SA00003HR00

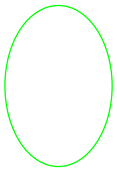
Realtek: RTM890N-631-GRT, SA00003HQ00

Silego: SLG8LV597VTR , SA00003MF00

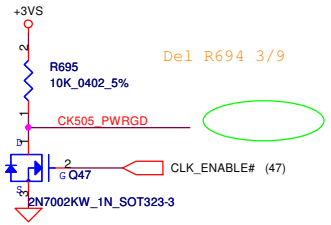
IDT 9LVS3199AKLFT NC



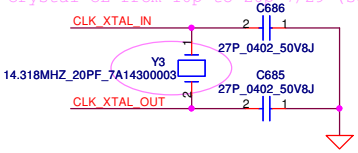
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



Move Q50 and Q51 to PCH Side 1/12



change Crystal CL from 16p to 20p 7/29 (sourcer suggestion)



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Compal Electronics, Inc.

Title: Clock Generator (CK505)

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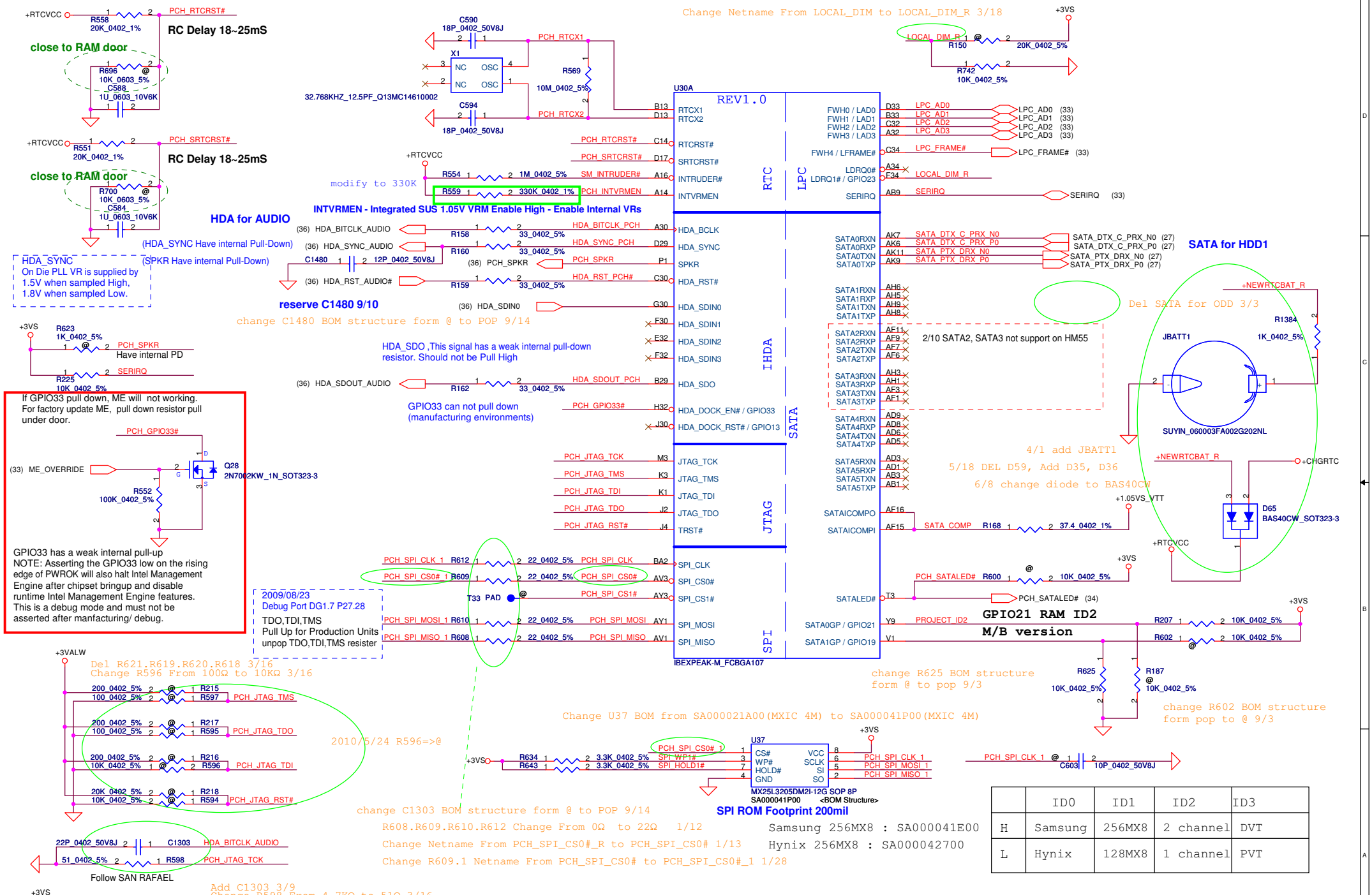

	ID0	ID1	ID2	ID3
H	Samsung	256MX8	2 channel	DVT
L	Hynix	128MX8	1 channel	PVT

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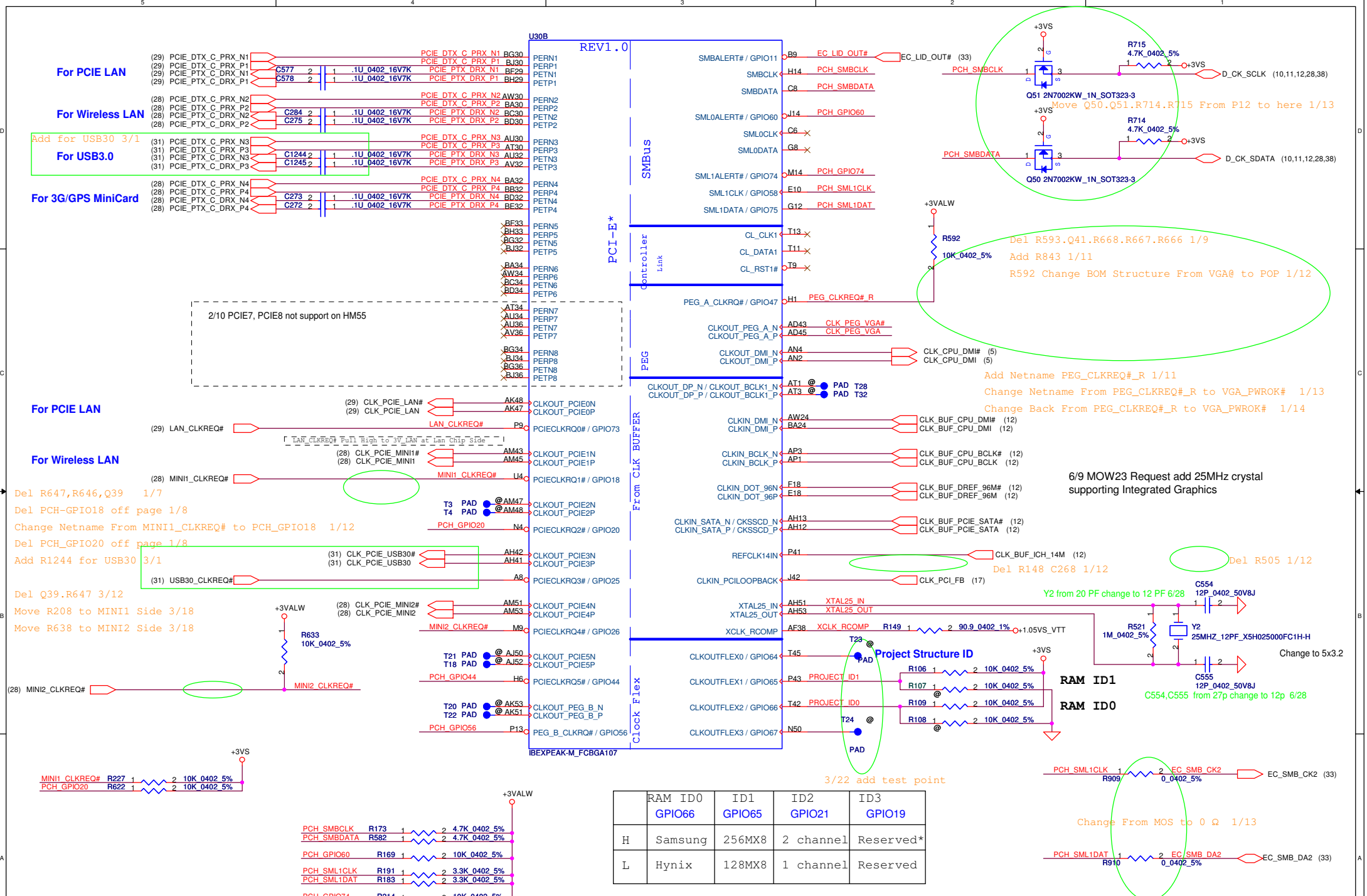
Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 13 of 51



	RAM ID0 GPIO66	ID1 GPIO65	ID2 GPIO21	ID3 GPIO19
H	Samsung	256MX8	2 channel	Reserved*
L	Hynix	128MX8	1 channel	Reserved

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Issued Date	2009/11/23	Deciphered Date	2010/11/23

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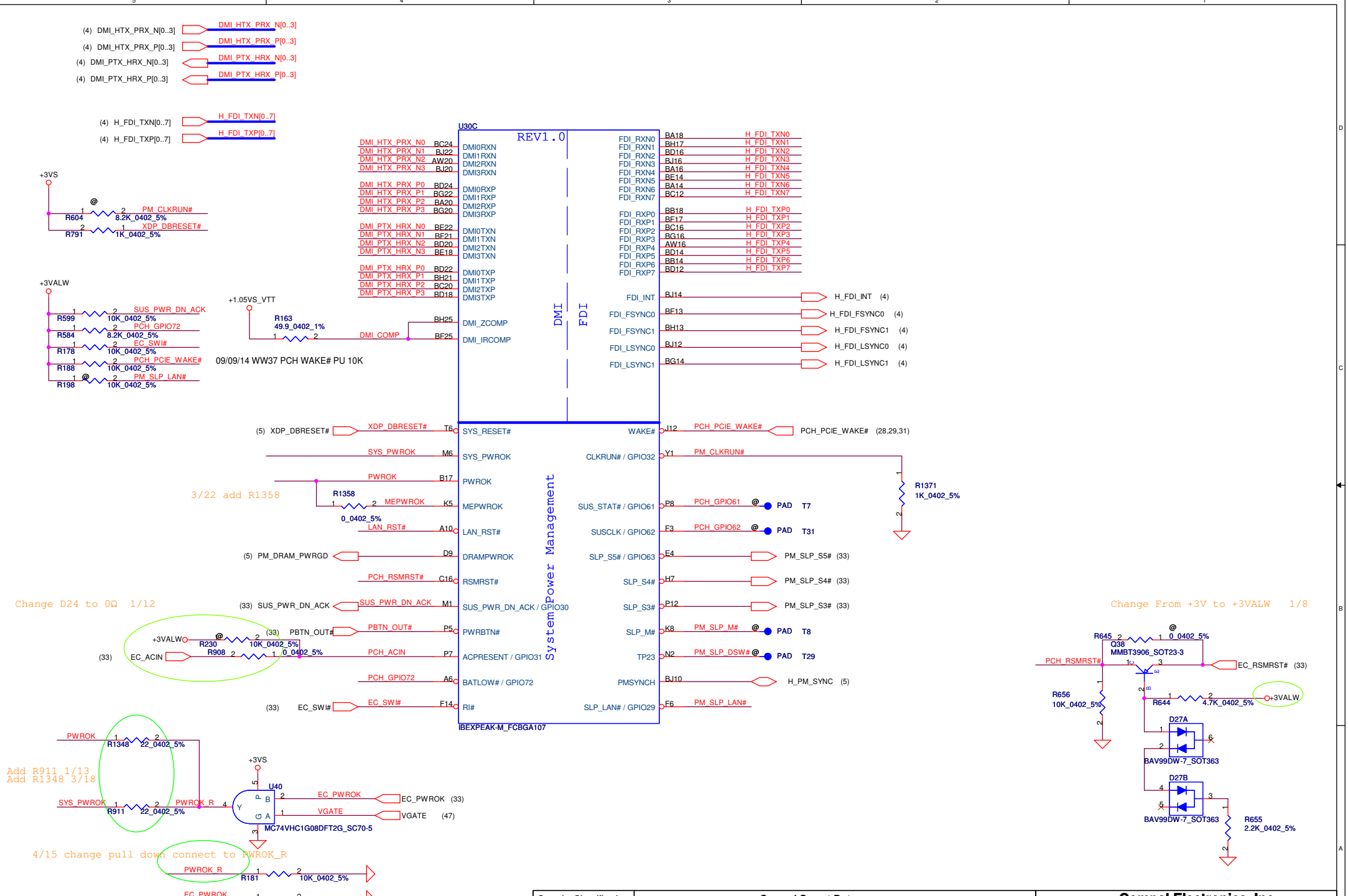
Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 14 of 51



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Issued Date	2009/11/23	Deciphered Date	2010/11/23

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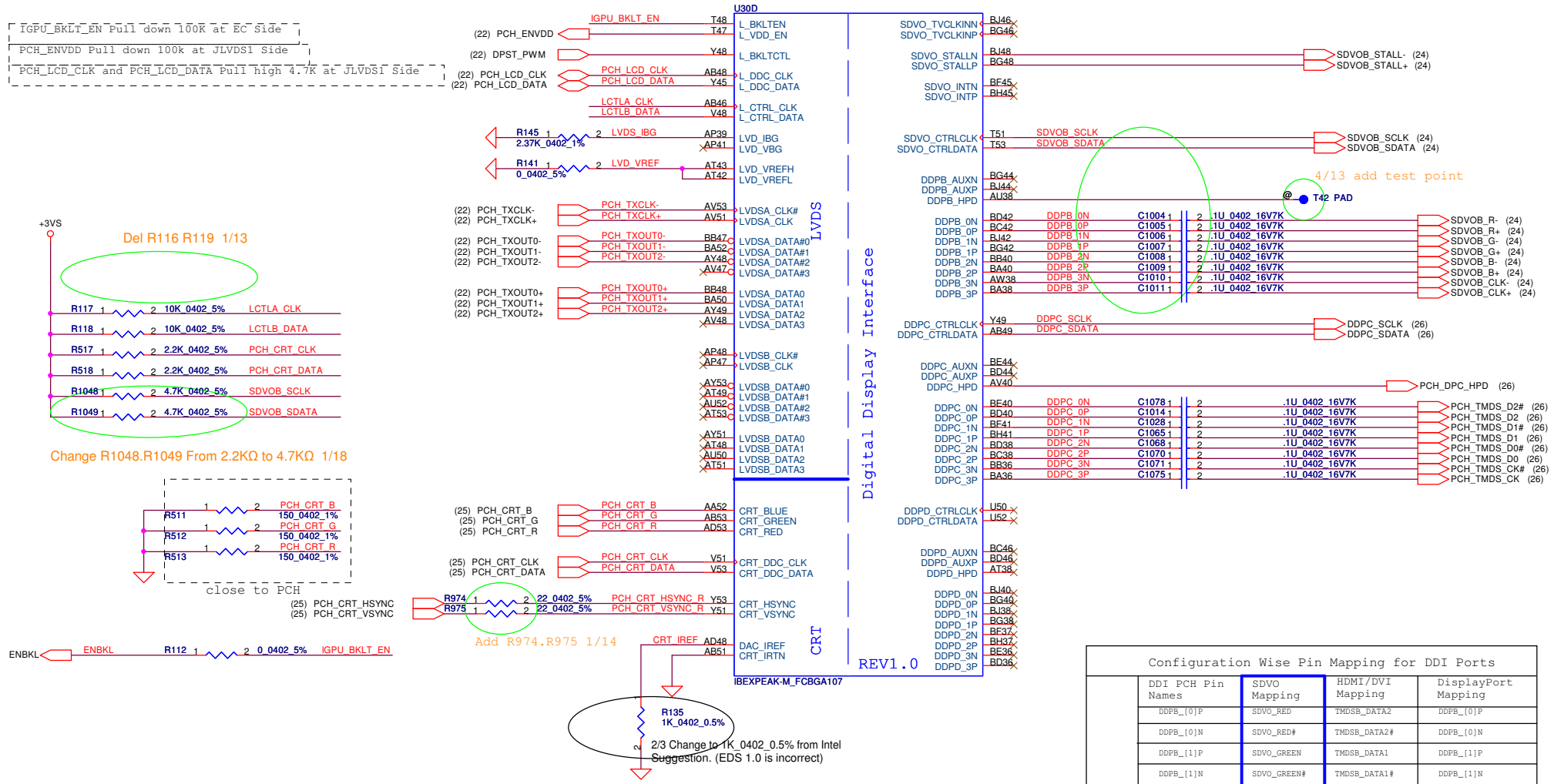
Compal Electronics, Inc.

Title: PCH (3/9) DMI, FDI, PM

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 15 of 51



Configuration Wise Pin Mapping for DDI Ports

	DDI PCH Pin Names	SDVO Mapping	HDMI/DVI Mapping	DisplayPort Mapping
PORT B	DDPB_[0]P	SDVO_RED	TMDSB_DATA2	DDPB_[0]P
	DDPB_[0]N	SDVO_RED#	TMDSB_DATA2#	DDPB_[0]N
	DDPB_[1]P	SDVO_GREEN	TMDSB_DATA1	DDPB_[1]P
	DDPB_[1]N	SDVO_GREEN#	TMDSB_DATA1#	DDPB_[1]N
	DDPB_[2]P	SDVO_BLUE	TMDSB_DATA0	DDPB_[2]P
	DDPB_[2]N	SDVO_BLUE#	TMDSB_DATA0#	DDPB_[2]N
	DDPB_[3]P	SDVO_CLK	TMDSB_CLK	DDPB_[3]P
	DDPB_[3]N	SDVO_CLK#	TMDSB_CLK#	DDPB_[3]N
	DDPB_AUXP	NA	NA	DDPB_AUXP
	DDPB_AUXN	NA	NA	DDPB_AUXN
	DDPB_HPD	NA	HDMIB_HPD	DDPB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	HDMIB_CTRLCLK	NA
	SDVO_CTRLDATA	SDVO_CTRLDATA	HDMIB_CTRLDATA	NA

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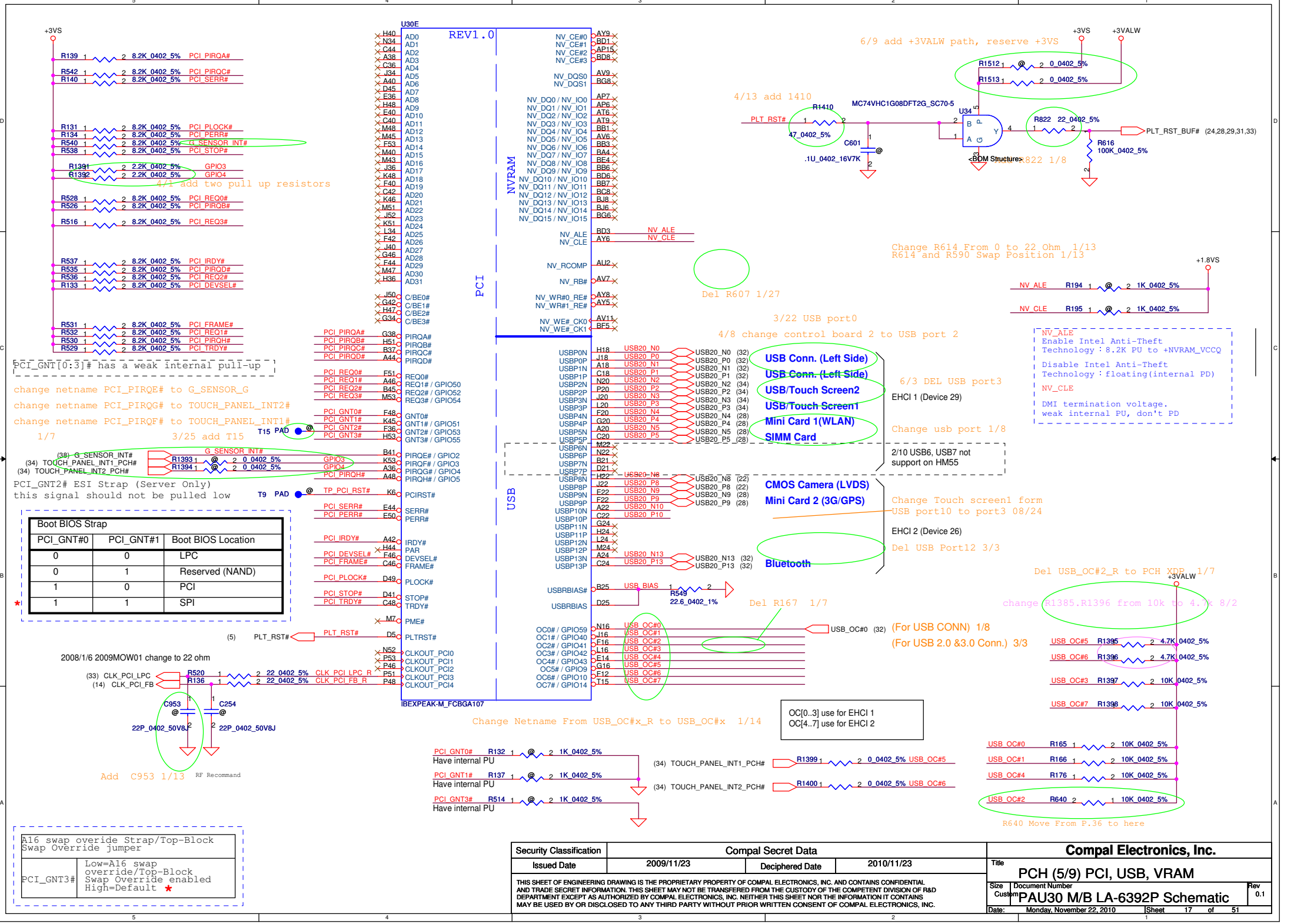
Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 16 of 51


U30E
REV1.0
IBEXPEAK-M_FCBGA107
PCI
NVRAM
USB
+3VS
+3VALW
+1.8VS
6/9 add +3VALW path, reserve +3VS
4/13 add 1410
MC74VHC1G08DFT2G_SC70-5
<BOM Structure>
4/1 add two pull up resistors
PCI_GNT[0:3]# has a weak internal pull-up
change netname PCI_PIRQE# to G_SENSOR_G
change netname PCI_PIRQG# to TOUCH_PANEL_INT2#
change netname PCI_PIRQF# to TOUCH_PANEL_INT1#
1/7
3/25 add T15
PCI_GNT2# ESI Strap (Server Only)
this signal should not be pulled low
Boot BIOS Strap
PCI_GNT#0 | PCI_GNT#1 | Boot BIOS Location
0 | 0 | LPC
0 | 1 | Reserved (NAND)
1 | 0 | PCI
1 | 1 | SPI
2008/1/6 2009MOW01 change to 22 ohm
Add C953 1/13
RF Recommand
Change R614 From 0 to 22 Ohm 1/13
R614 and R590 Swap Position 1/13
Del R607 1/27
3/22 USB port0
4/8 change control board 2 to USB port 2
USB Conn. (Left Side)
USB Conn. (Left Side)
USB/Touch Screen2
USB/Touch Screen1
Mini Card 1(WLAN)
SIMM Card
6/3 DEL USB port3
EHCI 1 (Device 29)
Change usb port 1/8
2/10 USB6, USB7 not support on HM55
CMOS Camera (LVDS)
Mini Card 2 (3G/GPS)
Change Touch screen1 form USB port10 to port3 08/24
EHCI 2 (Device 26)
Del USB Port12 3/3
Bluetooth
Del R167 1/7
Change Netname From USB_OC#x_R to USB_OC#x 1/14
OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2
(For USB CONN) 1/8
(For USB 2.0 &3.0 Conn.) 3/3
Del USB_OC#2_R to PCH XDP 1/7
change R1385.R1396 from 10k to 4.7k 8/2
R640 Move From P.36 to here
NV_ALE
Enable Intel Anti-Theft Technology : 8.2K PU to +NVRAM_VCCQ
Disable Intel Anti-Theft Technology : floating(internal PD)
NV_CLE
DMI termination voltage. weak internal PU, don't PD
A16 swap overide Strap/Top-Block Swap Override jumper
PCI_GNT3# | Low=A16 swap override/Top-Block Swap Override enabled High=Default
Have internal PU
Have internal PU
Have internal PU
Security Classification | Compal Secret Data
Issued Date | 2009/11/23 | Deciphered Date | 2010/11/23
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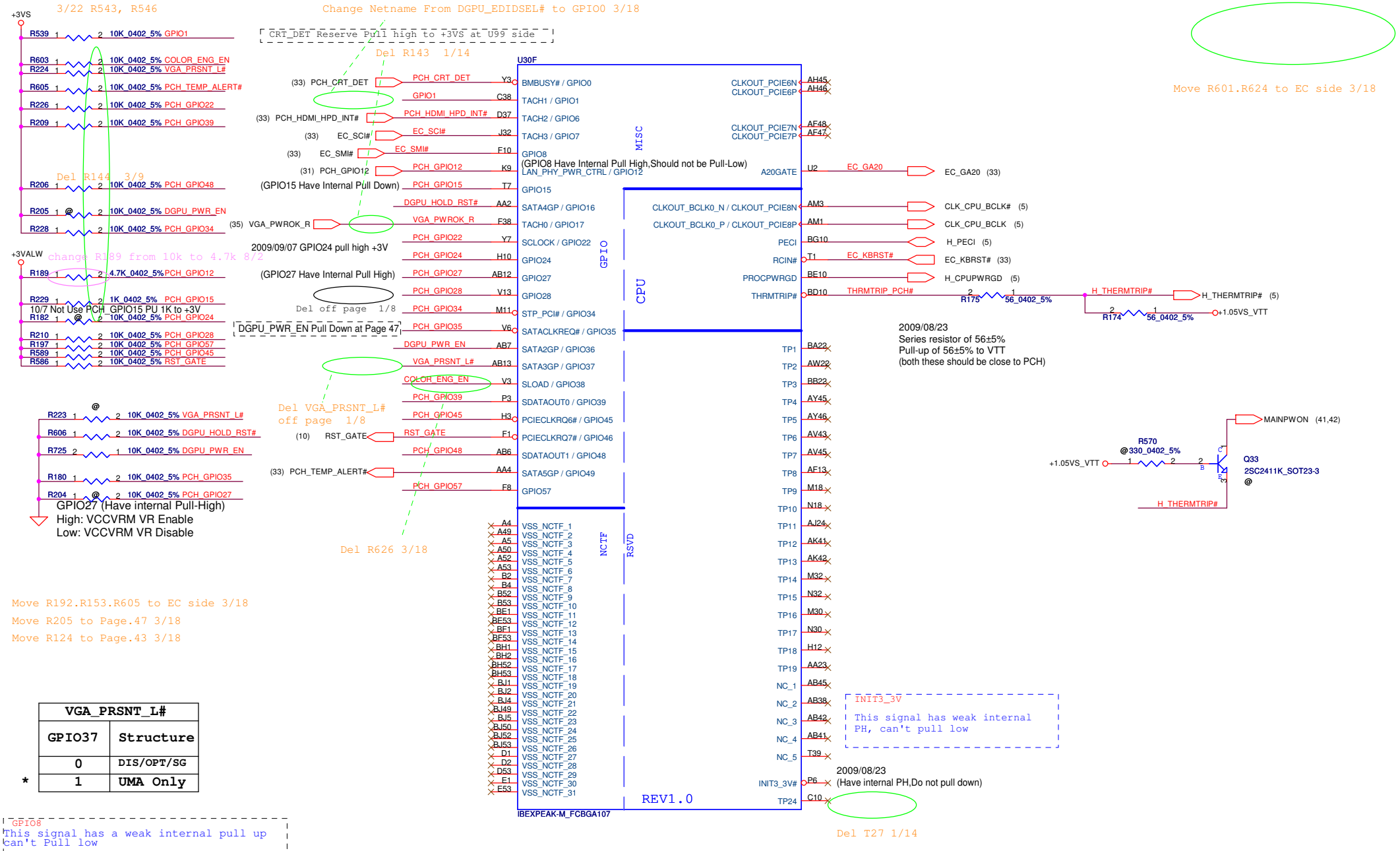
Compal Electronics, Inc.
Title
PCH (5/9) PCI, USB, VRAM
Size Custom
Document Number
PAU30 M/B LA-6392P Schematic
Rev 0.1
Date: Monday, November 22, 2010
Sheet 17 of 51



VGA_PRSNT_L#	
GPIO37	Structure
0	DIS/OPT/SG
* 1	UMA Only

GPIO8
This signal has a weak internal pull up
can't Pull low

GPIO27
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
  L : On-Die PLL Voltage Regulator disable

Note: the internal pull-up is disabled after RSMRST# de-asserts.
The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.

GPIO15
* L : Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality
  H : Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality

CRB has a 1-k pull-up on this signal to +3.3VA rail.

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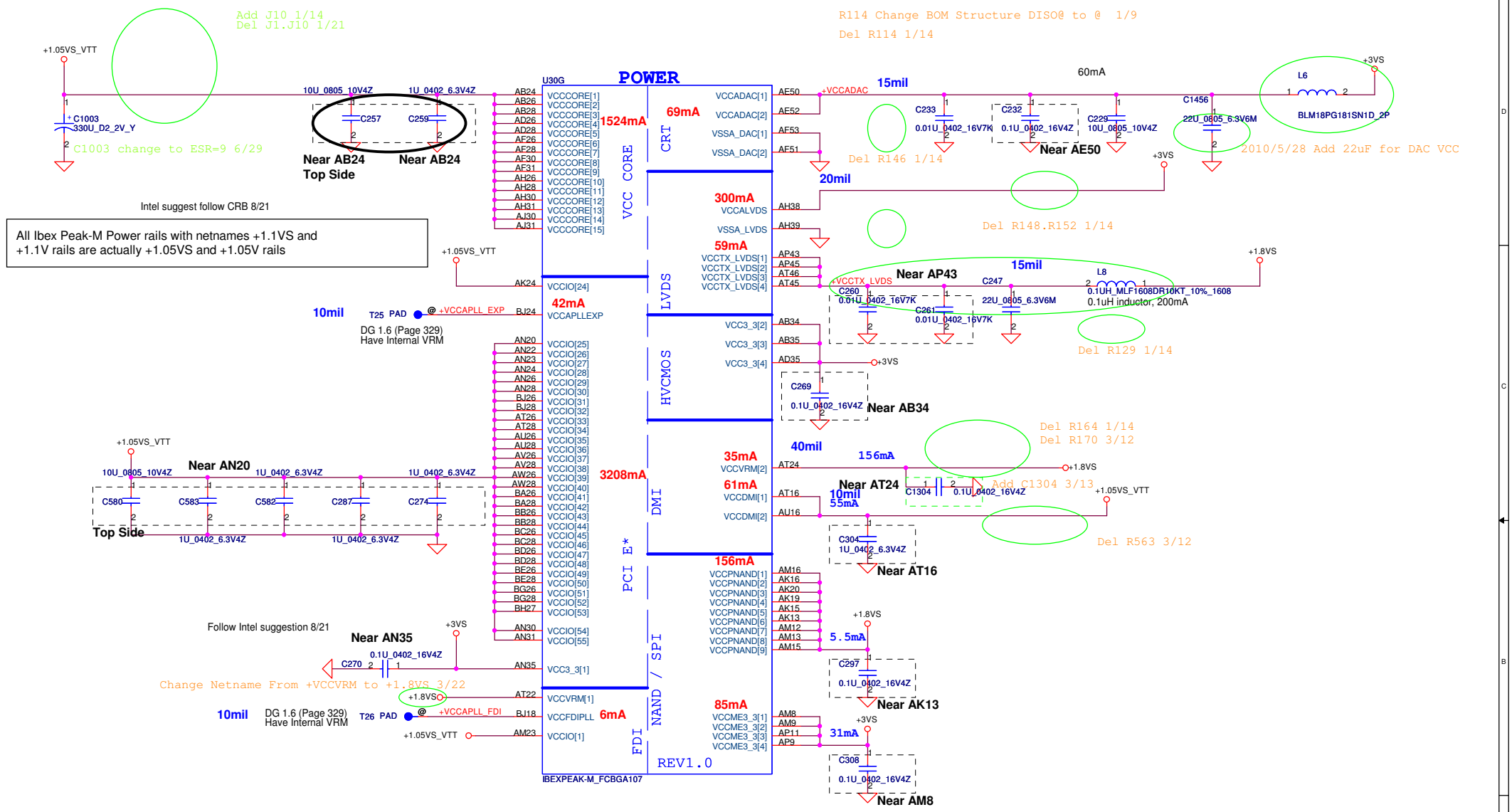
Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 18 of 51



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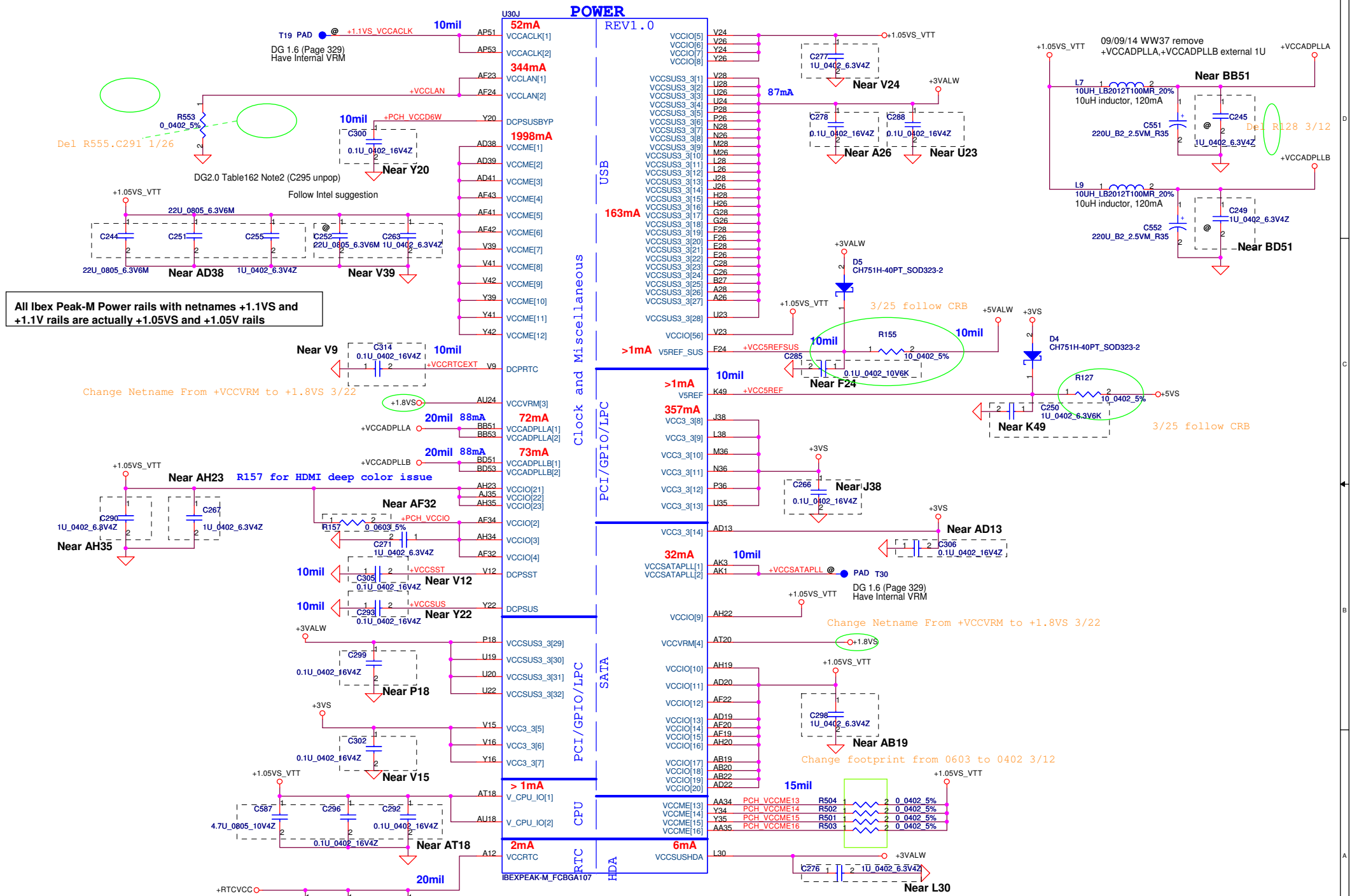
Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Tuesday, September 07, 2010 | Sheet 19 of 51



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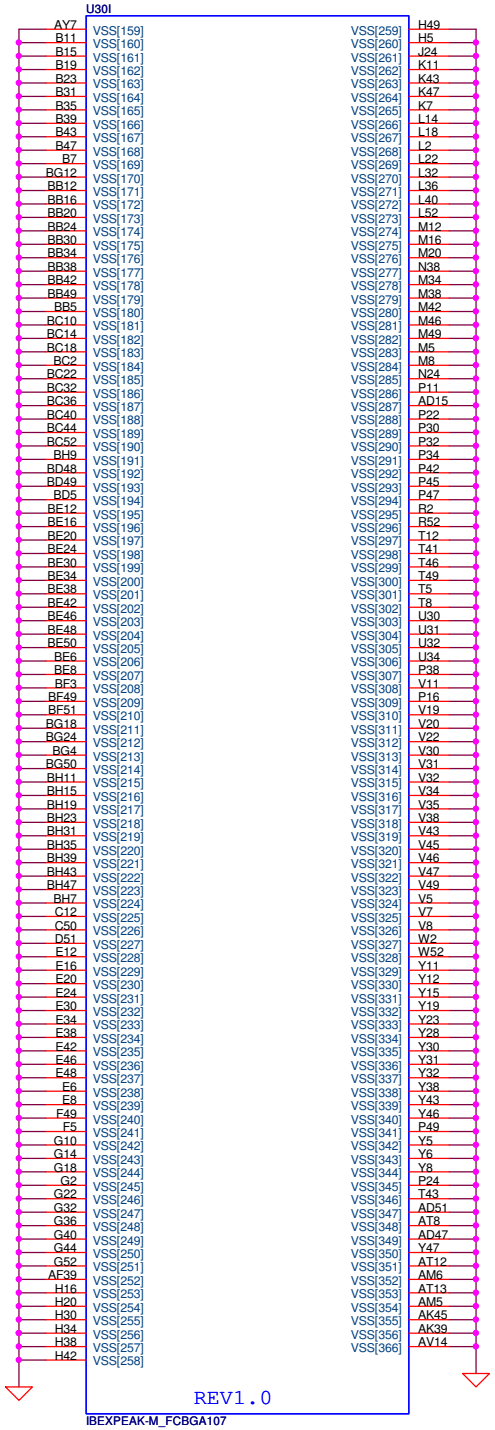
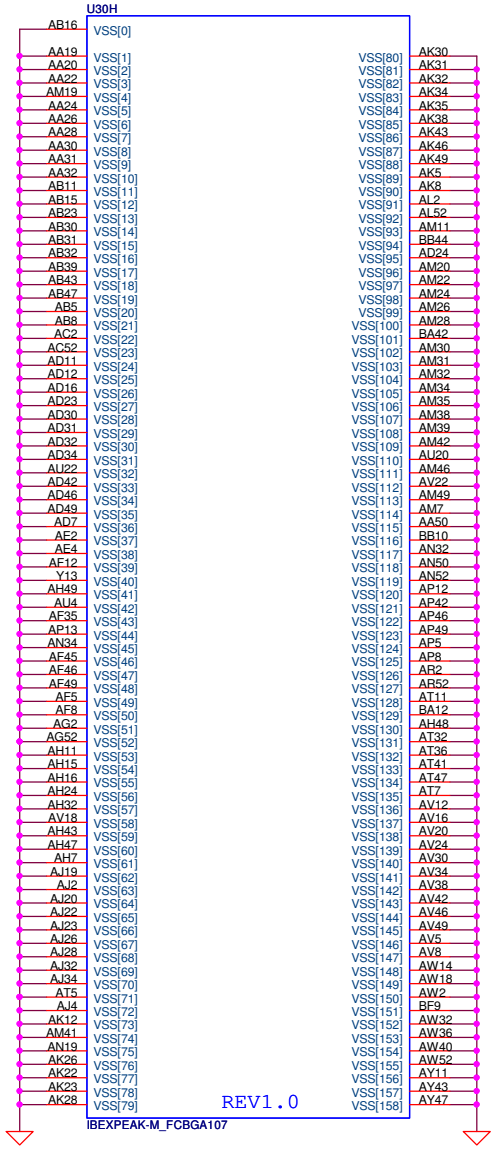
Compal Electronics, Inc.

Title: PCH (8/9) PWR

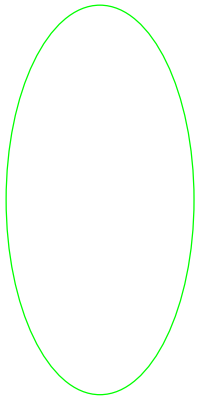
Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Monday, November 01, 2010 | Sheet 20 of 51





Del PCH XDP Port 1/7



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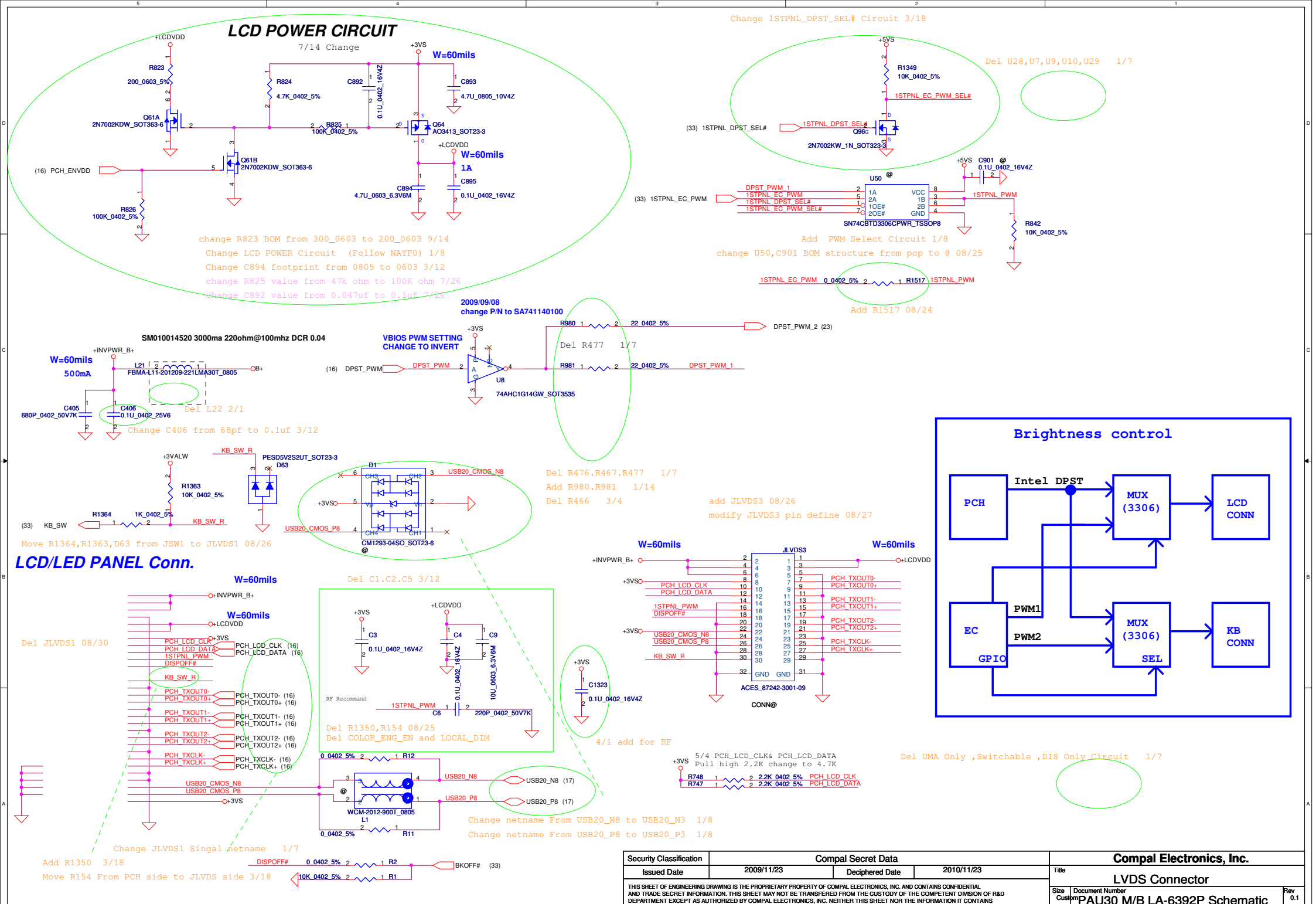
Compal Electronics, Inc.

Title: PCH (9/9) VSS & PCH XDP Port

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Tuesday, September 07, 2010 | Sheet 21 of 51



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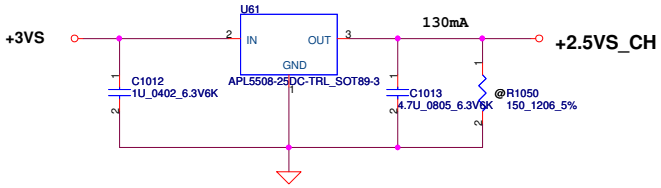
Compal Electronics, Inc.

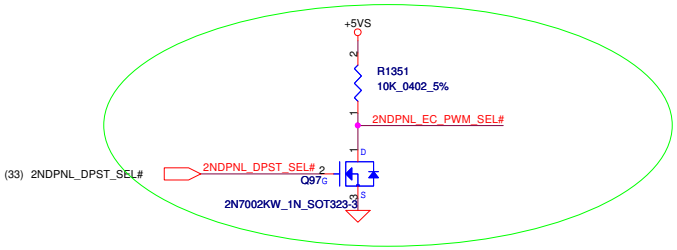
Title: LVDS Connector

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

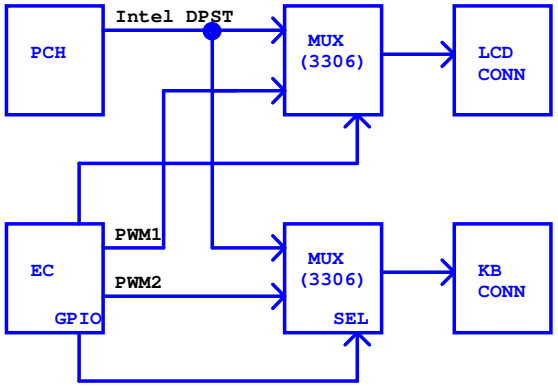
Date: Monday, November 22, 2010 | Sheet 22 of 51



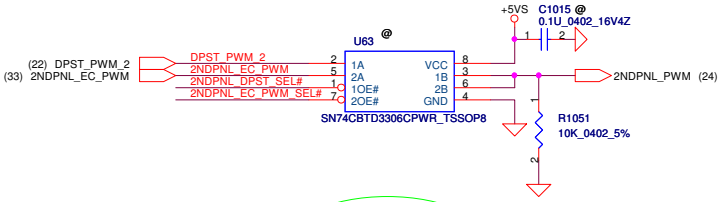
Change 2NDPNL_DPST_SEL# Circuit 3/18

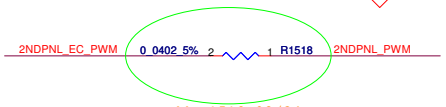


Brightness control



change U63,C1015 BOM structure from pop to @ 08/25





Add R1518 08/24

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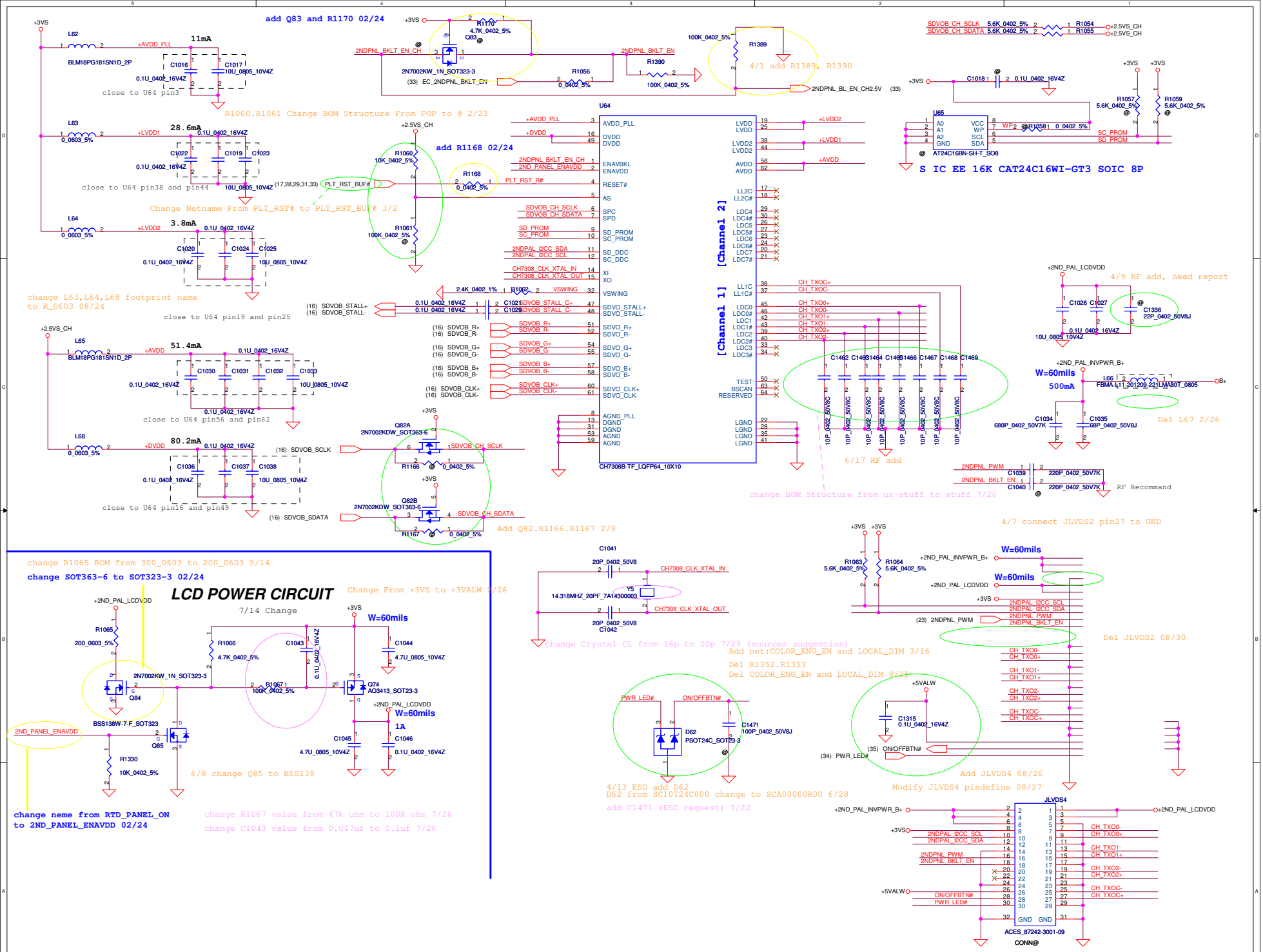
Compal Electronics, Inc.

Title: ***CH7308 SDVO to LVDS***

Size: Custom | Document Number: ***PAU30 M/B LA-6392P Schematic*** | Rev: 1.0

Date: Monday, November 22, 2010 | Sheet 23 of 51



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Compal Electronics, Inc.

Title: *7308 SDVO to LVDS*

Size: Custom | Document Number: *PAU30 M/B LA-6392P Schematic* | Rev: 1.0

Date: Monday, November 22, 2010 | Sheet 24 of 51

CRT Connector

Change ESD protect circuit (follow NAV50) 3/12
Close to CRT CONN for ESD.

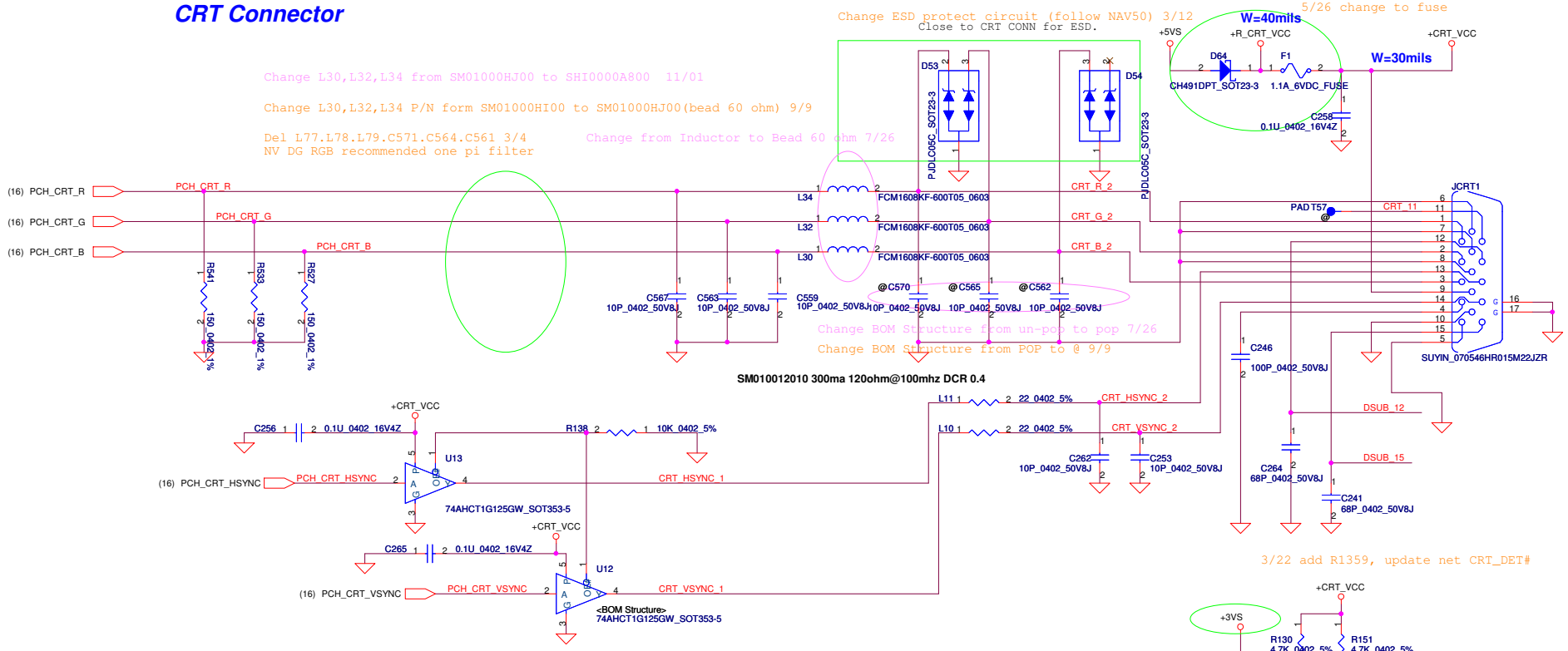
5/26 change to fuse

Change L30,L32,L34 from SM01000HJ00 to SHI0000A800 11/01

Change L30,L32,L34 P/N form SM01000HI00 to SM01000HJ00(bead 60 ohm) 9/9

Del L77.L78.L79.C571.C564.C561 3/4
NV DG RGB recommended one pi filter

Change from Inductor to Bead 60 ohm 7/26



5/24 Change CRT connet to PCH

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Issued Date	2009/11/23	Deciphered Date	2010/11/23

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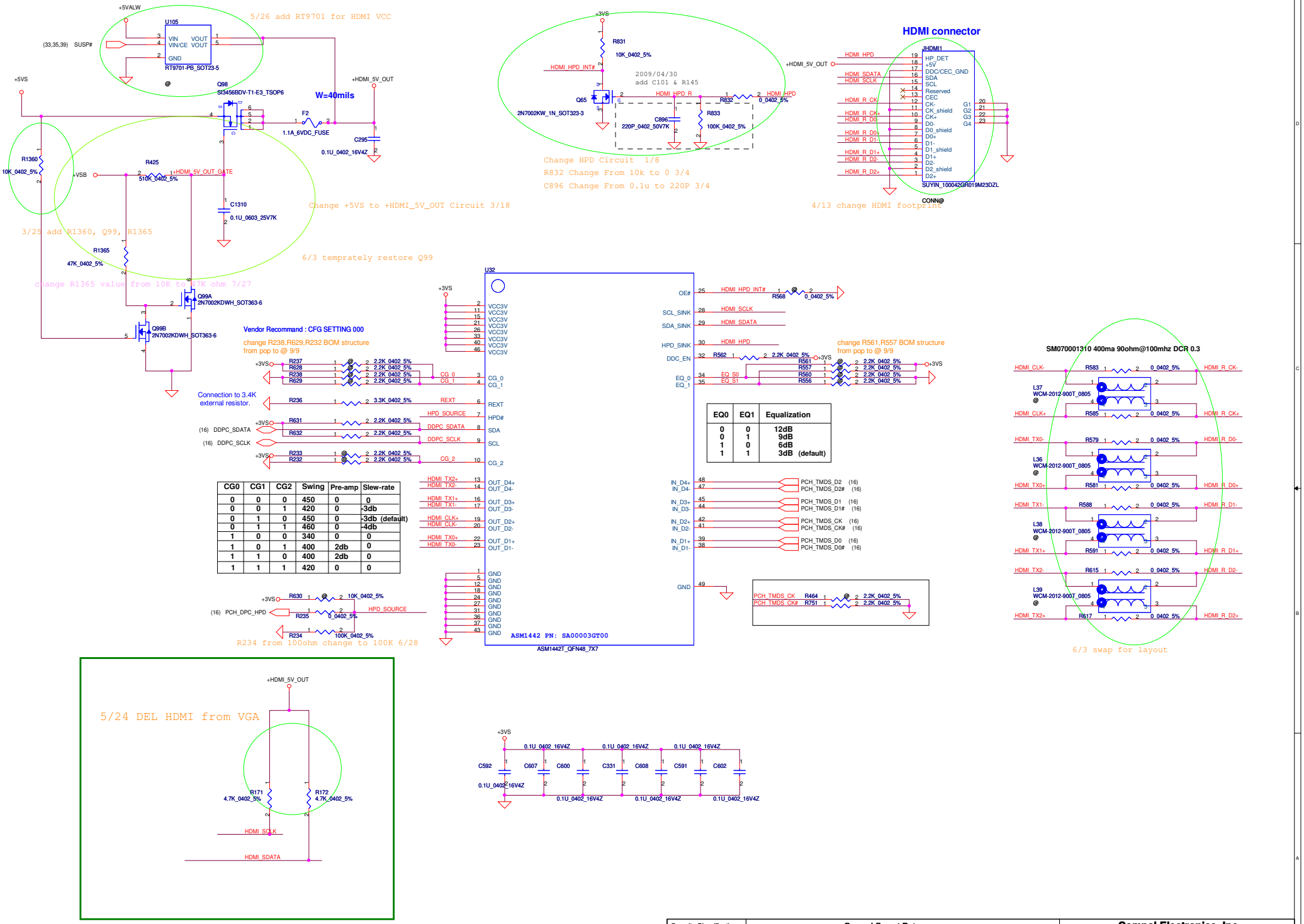
Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 25 of 51



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Compal Electronics, Inc.

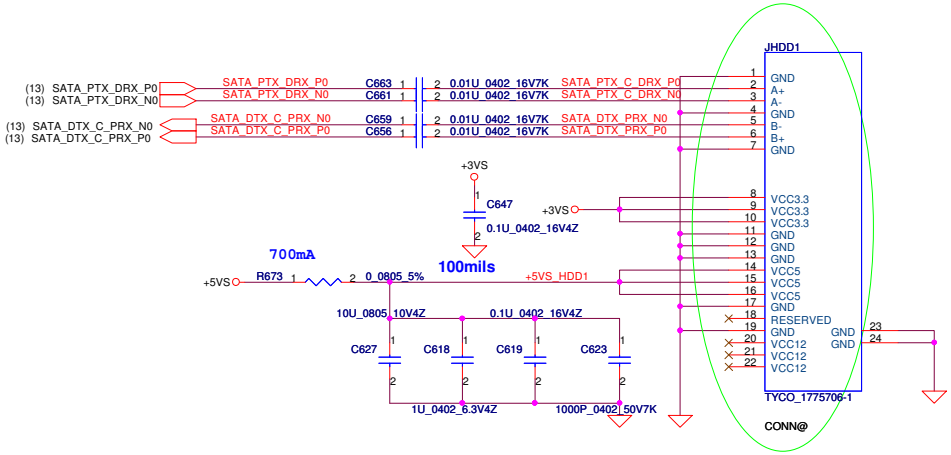
Title: HDMI Conn

Size: C | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 26 of 51

CL 4.0 mm

SATA HDD1 Conn.



6/8 change HDD symbol

change HDD symbol 8/26

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2009/11/23	Deciphered Date	2010/11/23	Title: HDD & ODD Connector
				Size: Custom; Document Number: PAU30 M/B LA-6392P Schematic; Rev: 0.1
				Date: Monday, November 22, 2010; Sheet 27 of 51

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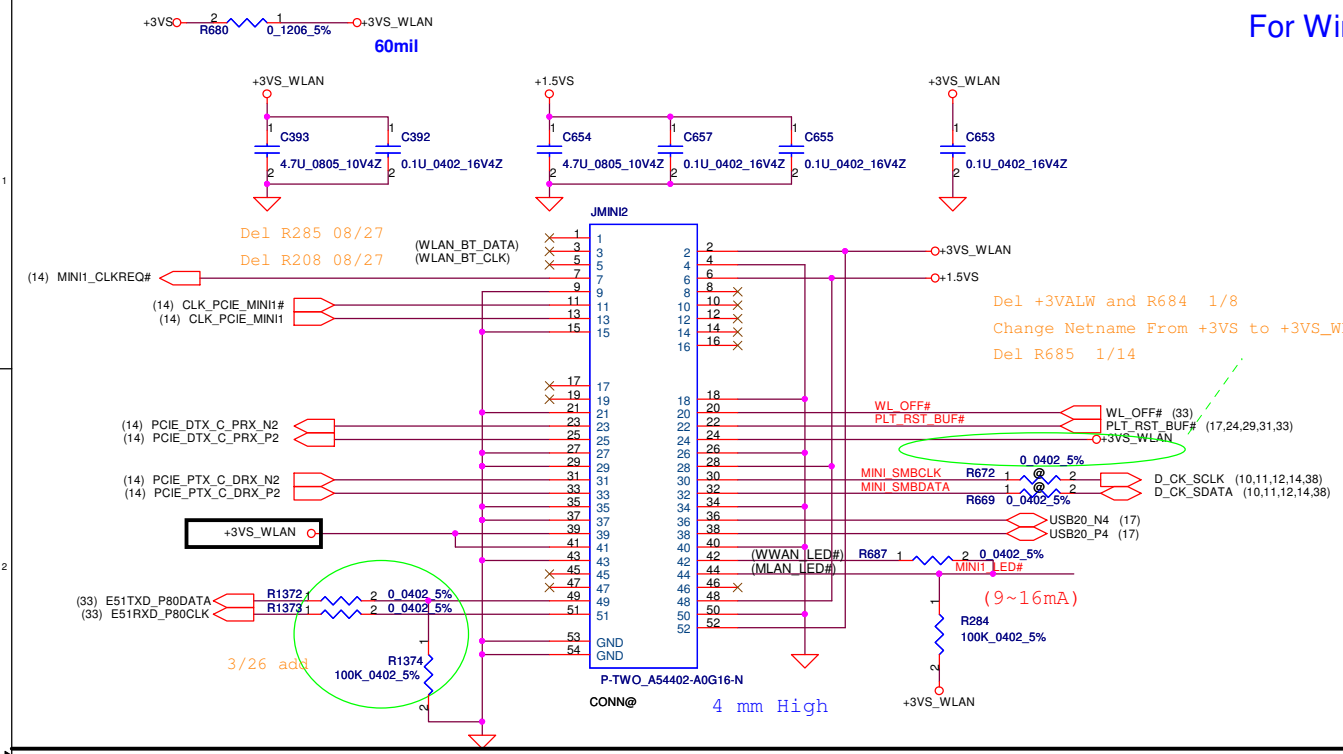
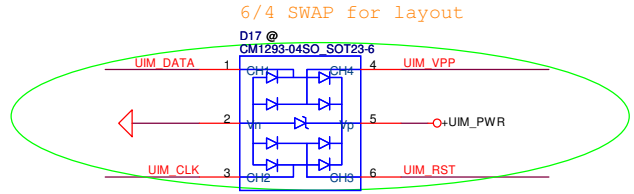
For Wireless LAN (Half Card)



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

For SIMM CARD



Del L41.R661.R663 1/14

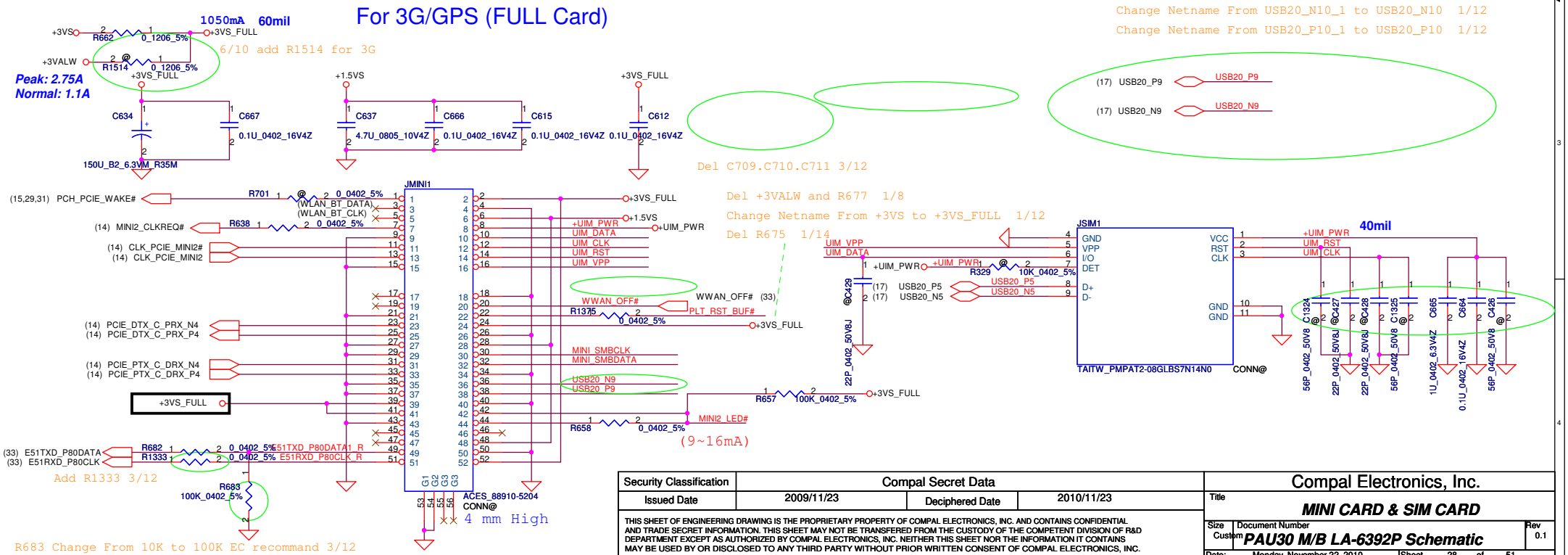
Change Netname From USB20_N10_1 to USB20_N10 1/12

Change Netname From USB20_P10_1 to USB20_P10 1/12

(17) USB20_P9 — USB20_P9

(17) USB20_N9 — USB20_N9

For 3G/GPS (FULL Card)



Security Classification	Compal Secret Data		
Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

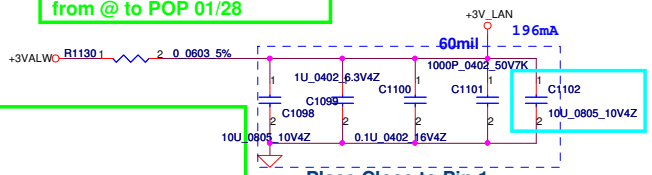
Title: **MINI CARD & SIM CARD**

Size: Custom | Document Number: **PAU30 M/B LA-6392P Schematic** | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 28 of 51

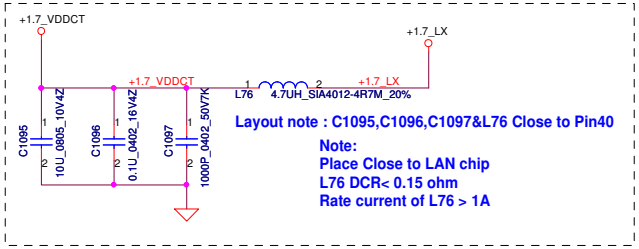
LAN Power Circuit & Refer NTUC0

change R362 BOM structure
from @ to POP 01/28



Place Close to Pin 1
Refer CRB

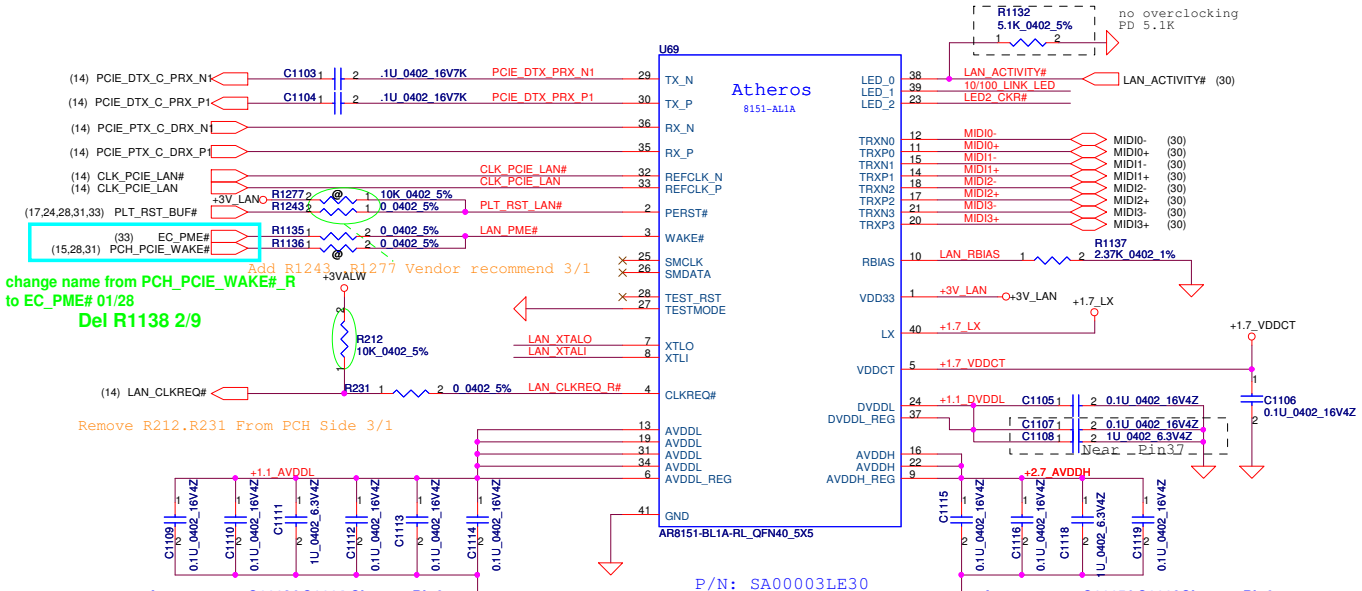
Del Q21,R363,C273
(WOL function) 01/28



Layout note : C1095,C1096,C1097&L76 Close to Pin40

Note:
Place Close to LAN chip
L76 DCR< 0.15 ohm
Rate current of L76 > 1A

10/22 Remove R364



Add R1243, R1277 Vendor recommend 3/1

change name from PCH_PCIE_WAKE#_R
to EC_PME# 01/28

Del R1138 2/9

Remove R212.R231 From PCH Side 3/1

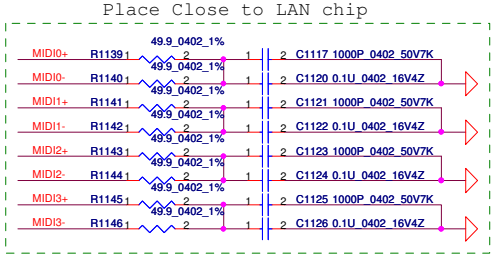
Layout note : C1113&C1114 Close to Pin6
C1109 Close to Pin13
C1110 Close to Pin19
C1111 Close to Pin31
C1112 Close to Pin34

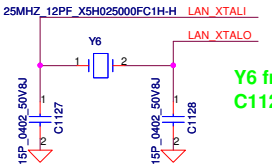
P/N: SA00003LE30

Layout note : C1115&C1116Close to Pin9
C1118 Close to Pin16
C1119 Close to Pin22

10/22 Change R376 from mount to @
11/02 Change R373 from mount to @
11/02 Delete Q3(@),R375(@),R377(@)
11/09 Delete R373(@),R376(@)

Place Close to LAN chip





Y6 from 20 pf change to 12 pf 6/28
C1127,C1128 from 27p change to 15p 6/28

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Issued Date	2009/10/10	Deciphered Date	2010/10/10

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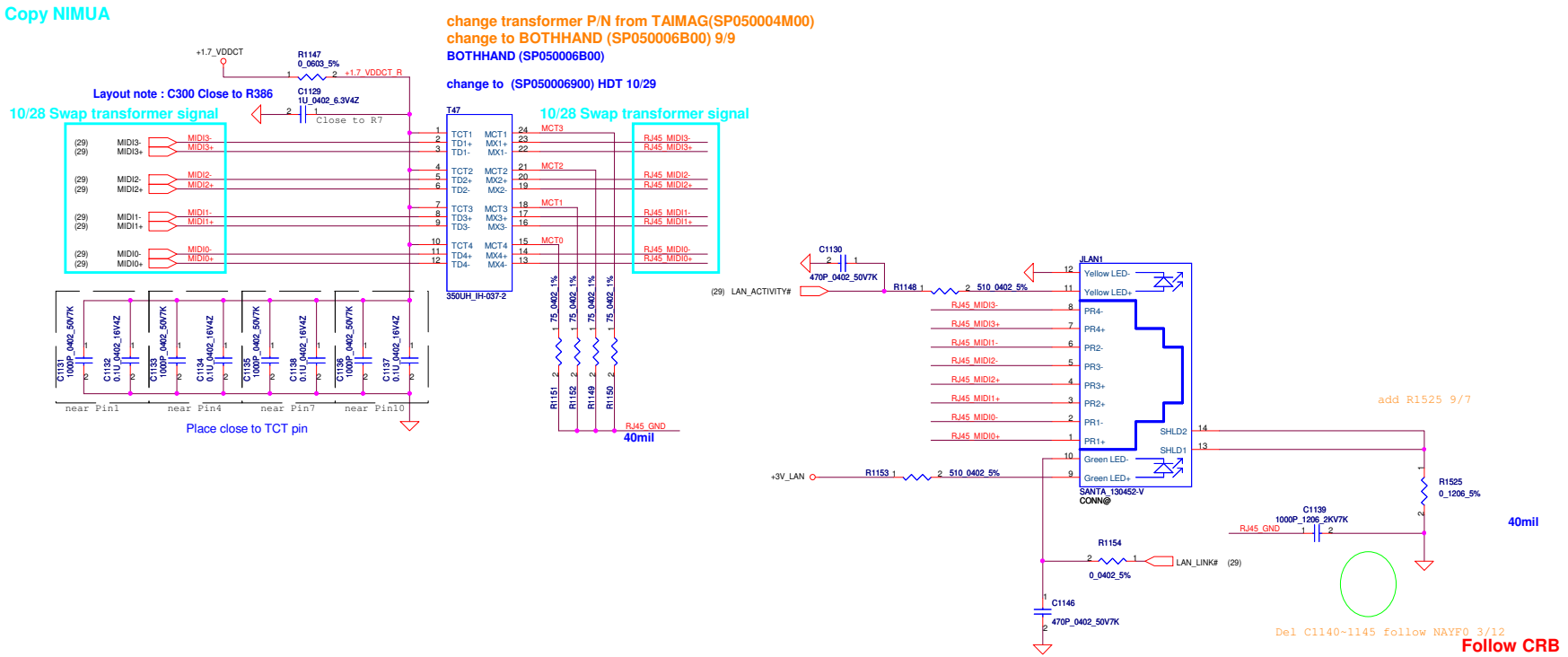
Compal Electronics, Inc.

Title: **LAN AR8151**

Size: Custom | Document Number: **PAU30 M/B LA-6392P Schematic** | Rev: 0.3

Date: Monday, November 22, 2010 | Sheet 29 of 51



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

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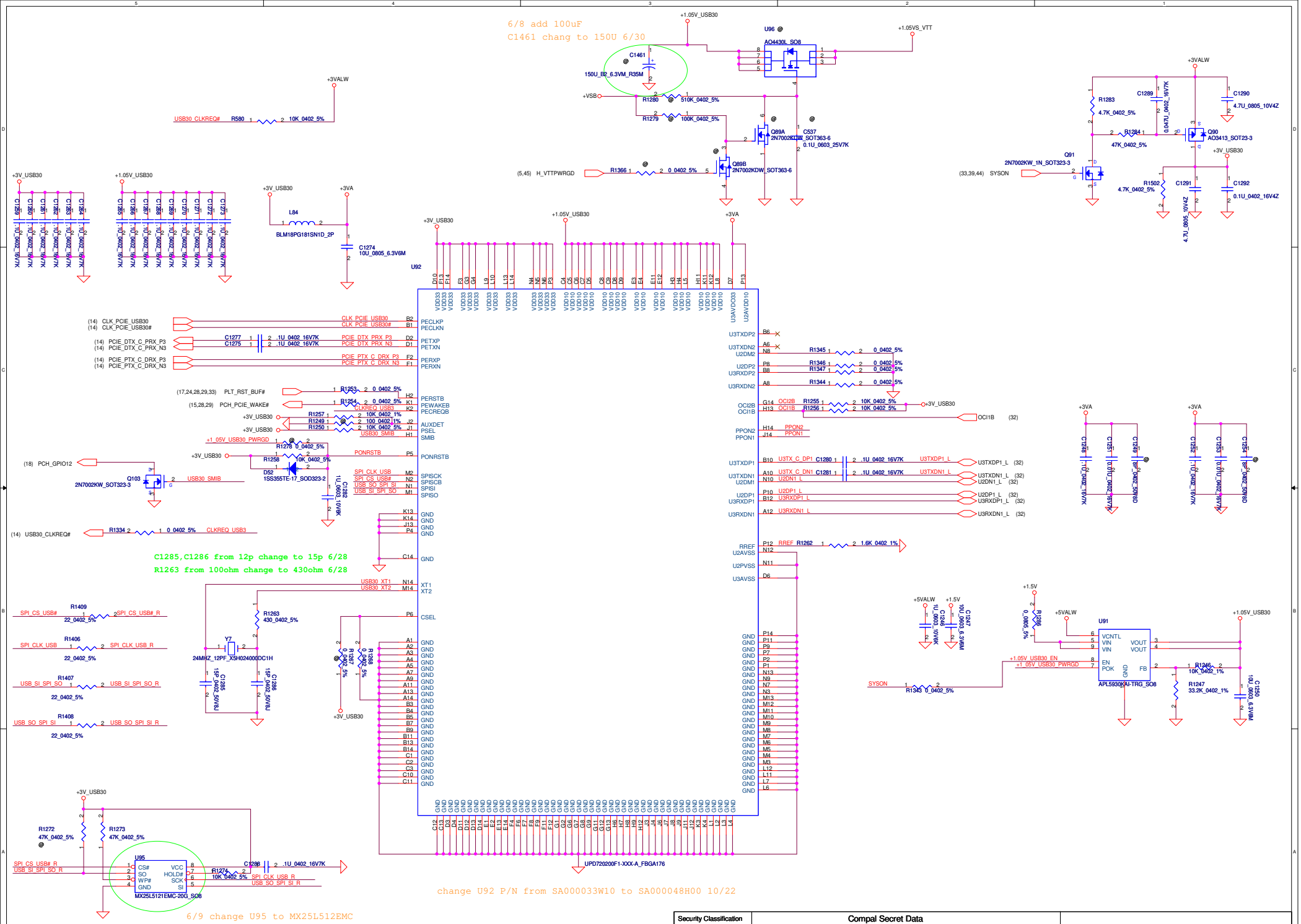
Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size | Document Number: PAU30 M/B LA-6392P Schematic | Rev 0.3

Date: Monday, November 22, 2010 | Sheet 30 of 51


6/8 add 100uF
C1461 chang to 150U 6/30
C1285,C1286 from 12p change to 15p 6/28
R1263 from 100ohm change to 430ohm 6/28
change U92 P/N from SA000033W10 to SA000048H00 10/22
6/9 change U95 to MX25L512EMC
U92
UPD720200F1-XXX-A_FBGA176
U91
APL5930KAI-TRG_SO8
U95
MX25L512EMC-20G_SO8
Q89A 2N7002KDW_SOT363-6
Q89B 2N7002KDW_SOT363-6
Q90 AO3413_SOT23-3
Q91 2N7002KW_1N_SOT323-3
Q103 2N7002KW_SOT323-3
U96 AO4430L_SO8
Y7 24MHZ_12PF_X5H024000DC1H
D52 1SS355TE-17_SOD323-2
L84 BLM18PG181SN1D_2P
C1274 10U_0805_6.3V6M
C1461 150U_B2_6.3VM_R35M
C537 0.1U_0603_25V7K
C1247 10U_0603_6.3V6M
C1250 10U_0603_6.3V6M
+1.05V_USB30
+1.05VS_VTT
+3VALW
+3V_USB30
+3VA
+VSB
+5VALW
+1.5V
+3V_USB30
+1.05V_USB30
+3VALW
+3VA
+3VA
+3VA
+3V_USB30
+3V_USB30
+3V_USB30

Left

R640 Move to P.17 1/12
Del R639 And C614 1/8
Del U36 And C605 3/3

+5VALW
+USB_VCCB
U98
GND VOUT
VIN VOUT
VIN VOUT
EN FLG
RT9715BGS_SO8
C1293
4.7U_0805_10V4Z
USB_OC#0 (17)
USB_OC#1 Pull High at PCH Side
(39) SYSON# SYSON#

6/3 swap for layout
D32 P/N change to SC300001100 6/28

3/22 Change JUSB2 power net
D25 P/N change to SC300001100 6/28

D32
USB20_P1 1
+USB_VCCB
CH6 CH2 CH5 CH3 CH4 CH1
150U_B2_6.3VM_R35M
USB20_N1 1
CM1293-04SO_SOT23-6
C897
C898
470P_0402_50V7K
R836 0_0402_5%
(17) USB20_N1 USB20_N1 L52
(17) USB20_P1 USB20_P1
WCM-2012-900T_0805
R837 0_0402_5%
USB20_N1 1
USB20_P1 1
JUSB1
VBUS
D-
D+
GND
ACON_UARBG-4K1926

D25
USB20_N0 1
USB20_P0 1
C339
C359
R635 0_0402_5%
(17) USB20_N0 USB20_N0 L40
(17) USB20_P0 USB20_P0
R636 0_0402_5%
USB20_N0 1
USB20_P0 1
JUSB2

Right

For EMI request

R1288 0_0402_5%
DLP11TB800UL2C_4P
(31) U3RXDN1_L U3RXDN1_L U3RXDN1
(31) U3RXDP1_L U3RXDP1_L U3RXDP1
L88
R1293 0_0402_5%
R1295 0_0402_5%
DLP11TB800UL2C_4P
(31) U3TXDN1_L U3TXDN1_L U3TXDN1
(31) U3TXDP1_L U3TXDP1_L U3TXDP1
L89
R1299 0_0402_5%
R1302 0_0402_5%
(31) U2DP1_L U2DP1_L U2DP1
(31) U2DN1_L U2DN1_L U2DN1
L86 WCM-2012-670T_4P
R1303 0_0402_5%

6/3 DEL USB port3

For ESD request

+USB3_VCCA
D58
U3TXDP1_L R- VCC
U3TXDN1_L R+ GND
U3RXDP1_L T- D- U2DP1_L
U3RXDN1_L T+ D+ U2DN1_L
LXES4XBAA6-027_MSOP8

4/19 swap for layout

+USB3_VCCA
U3TXDP1 SSTX+
U3TXDN1 VBUS
U2DP1 SSTX-
D+
U2DN1 GND
U3RXDP1 D-
SSRX+
U3RXDN1 GND
SSRX-
JUSB3
GND
ACON_TARA4-9K1311

BT Conn.

+BT_VCC
JBT1 120mA
GND
ACES_87213-0400G
USB20_P13 (17)
USB20_N13 (17)

3/23 change BT conn. symbol

+3VS
C692 0.047U_0402_16V7K
C690 1U_0603_10V4Z
(33) BT_ON# BT_ON# R719 47K_0402_5%
Q48 AO3413_SOT23-3
60mA
+BT_VCC
C695 4.7U_0805_10V4Z
C696 0.1U_0402_16V4Z
R720 300_0603_5%
Q49 2N7002KW_1N_SOT323-3

change R719 value from 100K to 47K ohm 7/28
change C692 value from 0.1uf to 0.047uf 7/28

+5V_TCH2
R1503 300_0603_5%
Q101A 2N7002KDW_SOT363-6
+5VALW W=40mils
R1403 4.7K_0402_5%
C1328 0.047U_0402_16V7K
C1329 4.7U_0805_10V4Z
R1404 47K_0402_5%
Q100 AO3413_SOT23-3
+5V_TCH2 W=40mils
200mA
(33) TOUCH_EN2 Q101B 2N7002KDW_SOT363-6

4/2 add PMOS for +5V_TCH
5/28 add R1503 for discharging path
5/19 change enable pin control by EC

+3V_TCH2
R1504 300_0603_5%
Q106A 2N7002KDW_SOT363-6
+3VALW W=40mils
R1416 4.7K_0402_5%
C1342 0.047U_0402_16V7K
C1341 4.7U_0805_10V4Z
R1417 47K_0402_5%
Q105 AO3413_SOT23-3
+3V_TCH2 W=40mils
200mA
(33) TOUCH_EN2 Q106B 2N7002KDW_SOT363-6

5/28 add R1504 for discharging path
5/18 add PMOS for +3V_TCH, control by EC

+USB3_VCCA
C1284 .1U_0402_16V7K
+5VALW
U93
GND VOUT
VIN VOUT
VIN VOUT
EN FLG
SYSON#
OCI1
RT9715BGS_SO8
(31) OCI1B OCI1B R1528 0_0402_5%

Del R1264 08/27
add R1528 09/10

+5V_TCH1
R1509 300_0603_5%
Q109A 2N7002KDW_SOT363-6
+5VALW W=40mils
R1505 4.7K_0402_5%
C1457 0.047U_0402_16V7K
C1458 4.7U_0805_10V4Z
R1506 47K_0402_5%
Q108 AO3413_SOT23-3
+5V_TCH1 W=40mils
200mA
(33) TOUCH_EN1 Q109B 2N7002KDW_SOT363-6

5/28 add R1503 for discharging path
5/19 change enable pin control by EC

+3VALW W=40mils
R1507 4.7K_0402_5%
C1460 0.047U_0402_16V7K
C1459 4.7U_0805_10V4Z
R1510 47K_0402_5%
Q110 AO3413_SOT23-3
+3V_TCH1 W=40mils
200mA
Q111B 3
(33) TOUCH_EN1 Q111B 2N7002KDW_SOT363-6

5/28 add R1504 for discharging path
5/18 add PMOS for +3V_TCH, control by EC

+3V_TCH1
R1508 300_0603_5%
Q111B 3 Q111A 2N7002KDW_SOT363-6

+USB3_VCCA
C1253 150U_SZ_6.3VM_R35M
C1254 10U_0805_6.3VM

D-case for customer request
can use B-case, either.

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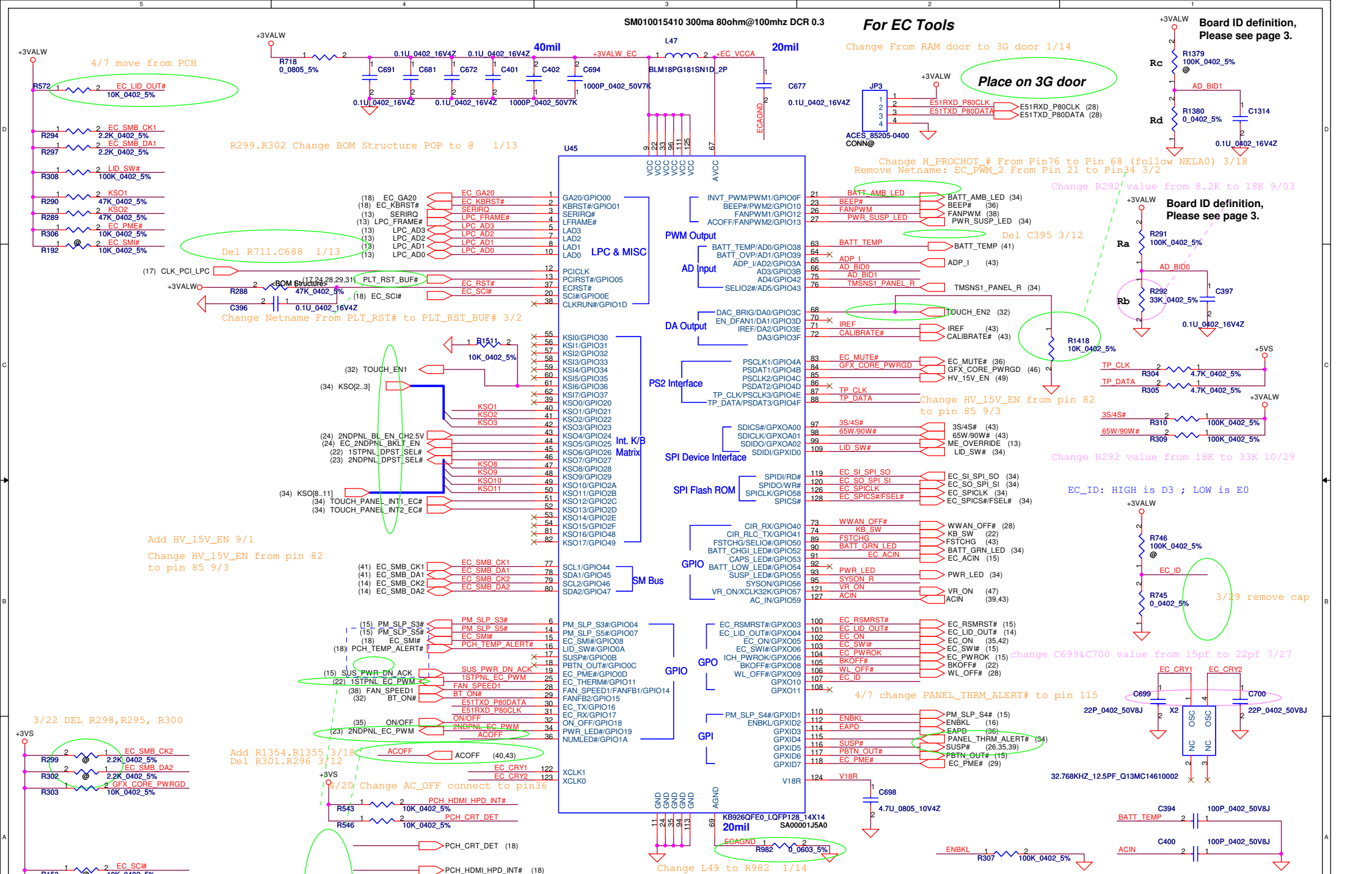
Compal Electronics, Inc.
Title: USB / BT / LAN CON
Size C | Document Number: PAU30 M/B LA-6392P Schematic | Rev 0.1
Date: Monday, November 22, 2010 | Sheet 32 of 51



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Compal Electronics, Inc.

Title: **EC ENE KB926**

Size: B | Document Number: **PAU30 M/B LA-6392P Schematic** | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 33 of 51

Del R702 3/12

Add R838 1/11

del U44 07/21

Change R704.R706.R716 Vaule From 0Ω to 22Ω 1/11

add control top HV_15V 09/07

del control top HV_15V 11/22

change R1523 BOM(4.7k_0402→22K_0402) 9/9

add C1483 11/22

Reserve C1484 11/22

Del R705 1/14

Reserve R1527 9/9

3/24 add connectors

LED/B FRONT

change R1413,LED1 BOM structure from pop to @ 08/25

4/15 JTCH1 change to 10 pin

5/19 ADD C1238, DEL C1317

3/30 add +3V_USB for control board and 2 caps

TOUCH/B RIGHT

Del R1387,R984 08/27

add Q113,R1516 07/22

Del R1516 08/27 Del R1326 08/27

add HV_15V 08/30

3/23 change R1326 => @, short path to PCH

SW/B LEFT (KEYB SW + TOUCH1)

4/21add +3VALW for control board and 2 caps

D63 change to SCA00000J00 6/28

change BOM Structure to @ 9/3

add HV_15V 08/30

Del R1388,R983 08/27

5/19 Add C1239, Del C1316

add Q112,R1515 07/22

Del R1515 8/27 Del R1324 8/27

3/23 change R1324 => @, short path to PCH

4/1 change to +3VALW

change +3V to +3V_TCH1 07/21

P/N: Mulata NXFT15X103F

Typical 4.16K @50 degree

42	5.350	5.437	5.525
43	5.169	5.255	5.342
44	4.995	5.080	5.165
45	4.828	4.911	4.996
46	4.667	4.749	4.832
47	4.512	4.593	4.675
48	4.363	4.443	4.524
49	4.220	4.299	4.379
50	4.083	4.160	4.239
51	3.950	4.027	4.104
52	3.823	3.898	3.974

chang JSW1 pin6,pin7 form USB20_N10/P10 to USB20_N3/P3 08/24

Rset=3*Rtmh

Rhyst=(Rset*Rtml)/(3*Rtml-Rset)

D61 P/N change to SC300001100 6/28

change +3V to +3V_TCH2 07/21

D60 P/N change to SC300001100 6/28

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Issued Date	2009/11/23	Deciphered Date	2010/11/23

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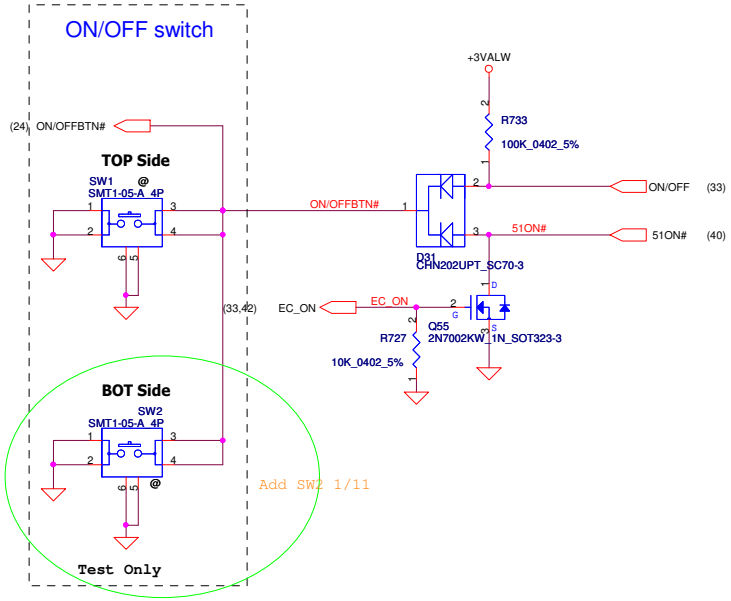
Compal Electronics, Inc.

Title: BIOS, I/O Port

Size: B | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

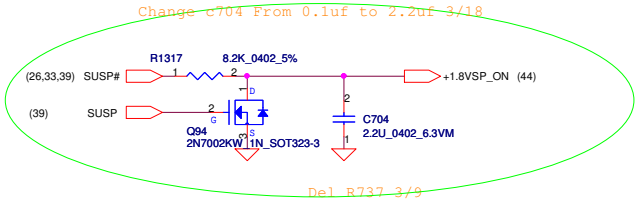
Date: Monday, November 22, 2010 | Sheet 34 of 51

Power Button



Power ON Circuit

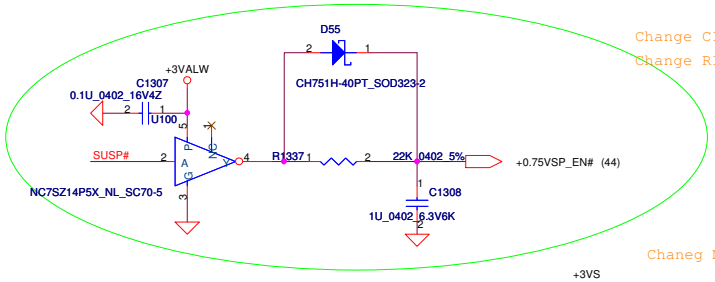
Change R1317 From 1KΩ to 8.2KΩ 3/18
Change c704 From 0.1uf to 2.2uf 3/18



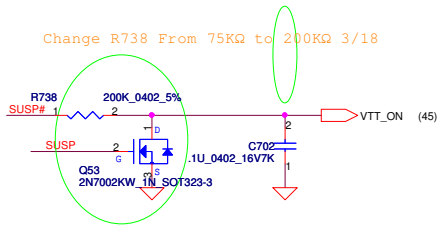
Del R737 3/9

Add +0.75VSP_EN Circuit 3/13
Change +3VS to +3VALW 3/16

Change C1308 From 0.1uf to 1uf 3/18
Change R1337 From 1KΩ to 22KΩ 3/18



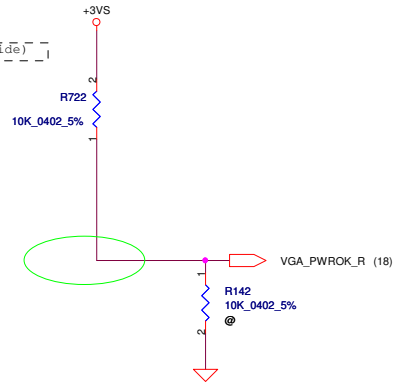
Change R738 From 75KΩ to 200KΩ 3/18



Del U46.R734.R1159.R739.R740.D45.R729.R730.D46 3/9

Chaneg Netname From VGA_PWROK# to PEG_CLKREQ#_R 3/18

VGA_PWROK is Open-Drain (Pull high at HW side)



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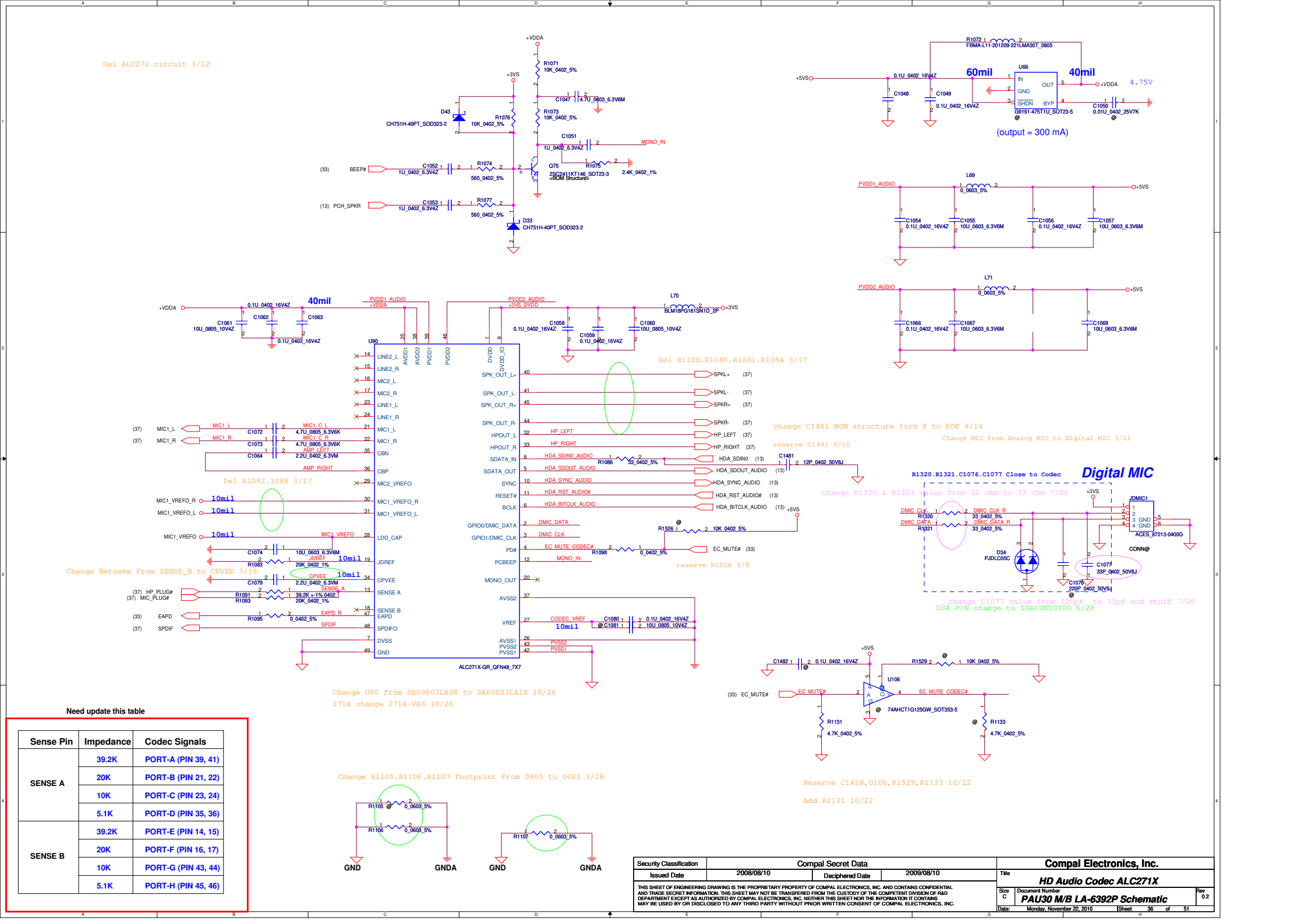
Compal Electronics, Inc.

Title: **Power OK**

Size: B | Document Number: **PAU30 M/B LA-6392P Schematic** | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 35 of 51



Need update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

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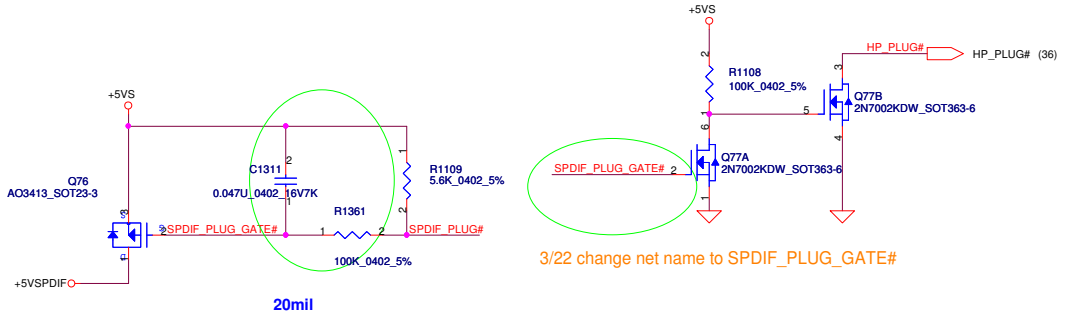
Compal Electronics, Inc.

Title: *HD Audio Codec ALC271X*

Size: C | Document Number: *PAU30 M/B LA-6392P Schematic* | Rev: 0.2

Date: Monday, November 22, 2010 | Sheet 36 of 51



3/22 change net name to SPDIF_PLUG_GATE#

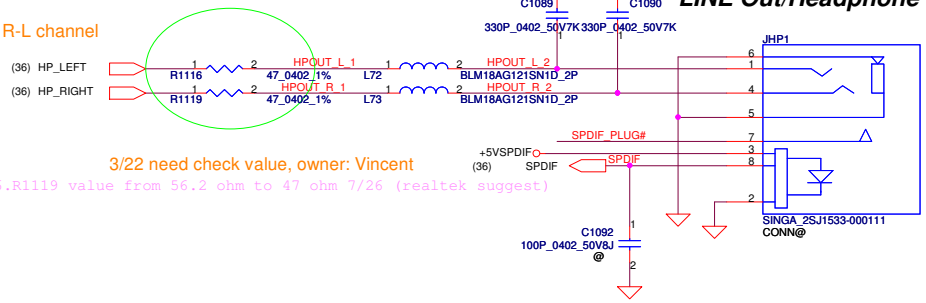
change back R1361 value from 56k ohm to 100K ohm 7/26

change C1311 value from 0.1u to 0.047uf 7/28

S/PDIF Out JACK

LINE Out/Headphone Out

5/19 exchange R-L channel

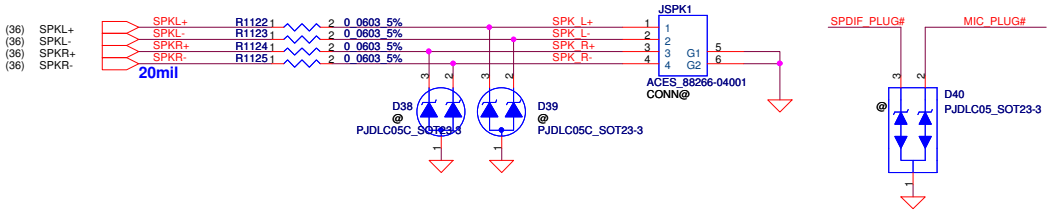


3/22 need check value, owner: Vincent

change R1116.R1119 value from 56.2 ohm to 47 ohm 7/26 (realtek suggest)

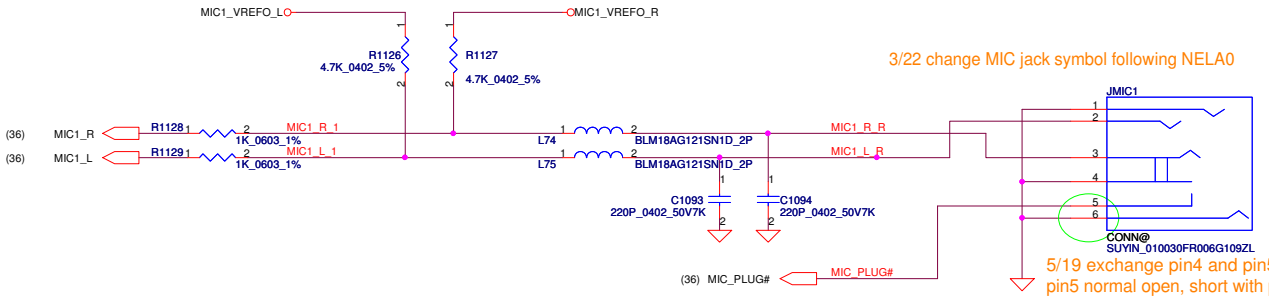
3/22 change headpone symbol following NELA0

Int. Speaker Conn.



MIC JACK

3/22 change MIC jack symbol following NELA0



5/19 exchange pin4 and pin5 connection,
pin5 normal open, short with pin4 when plugin

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

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Compal Electronics, Inc.

Title: ***Amplifier & Audio Jack***

Size: B | Document Number: ***PAU30 M/B LA-6392P Schematic*** | Rev: 0.2

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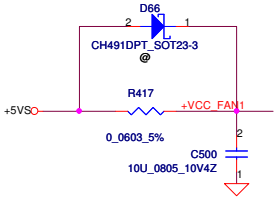
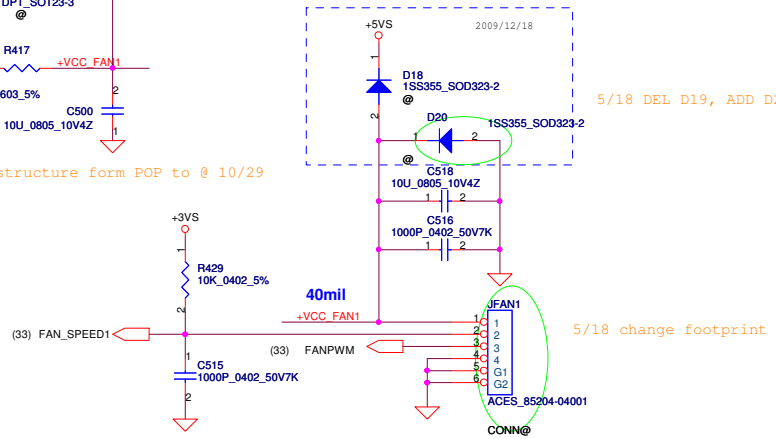
Change D66 BOM structure form @ to POP 10/29
reserve D66 10/26



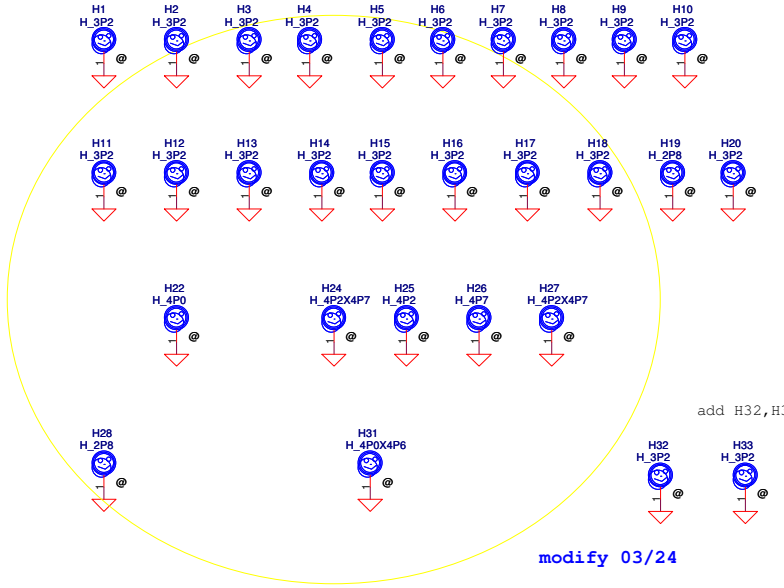
Change R417 BOM structure form POP to @ 10/29

FAN1 Conn



5/18 DEL D19, ADD D20

5/18 change footprint

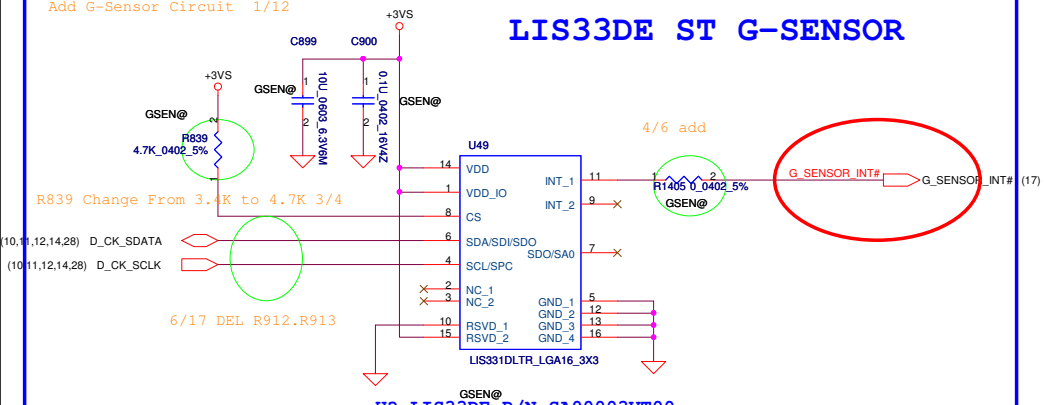


add H32,H33 7/12

modify 03/24

Add G-Sensor Circuit 1/12

LIS33DE ST G-SENSOR



4/6 add

R839 Change From 3.4K to 4.7K 3/4

6/17 DEL R912.R913

U? LIS33DE P/N SA00003VT00

Del Q63.R840.R841 1/13

Security Classification	Compal Secret Data		
Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

Title: ***FAN & G-Sensor & Screw Hole***

Size: B | Document Number: ***PAU30 M/B LA-6392P Schematic*** | Rev: 0.1

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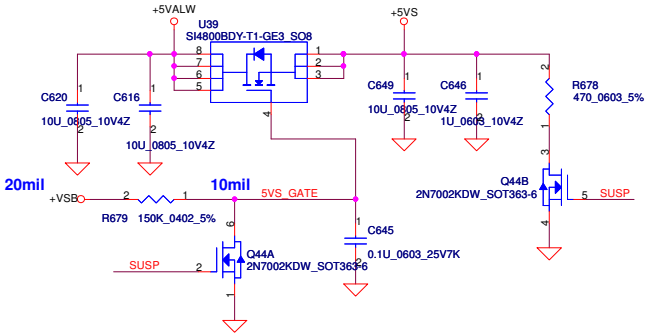
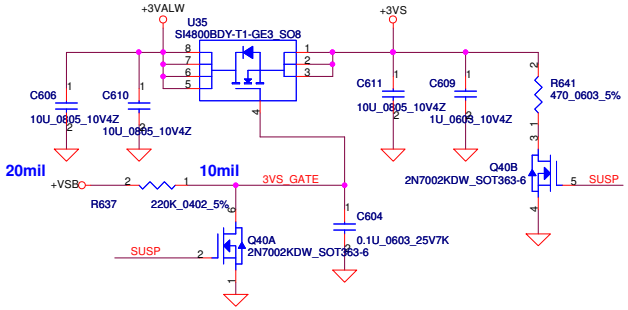
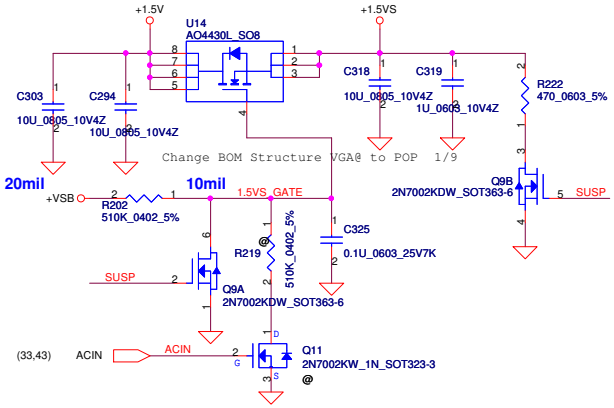
+5VALW TO +5VS

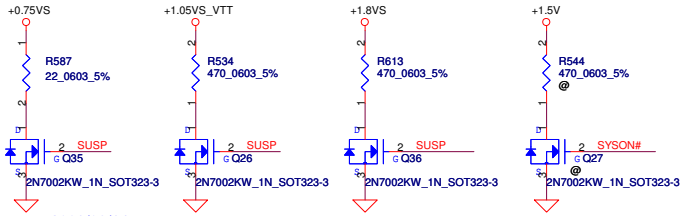


+3VALW TO +3VS



+1.5V to +1.5VS

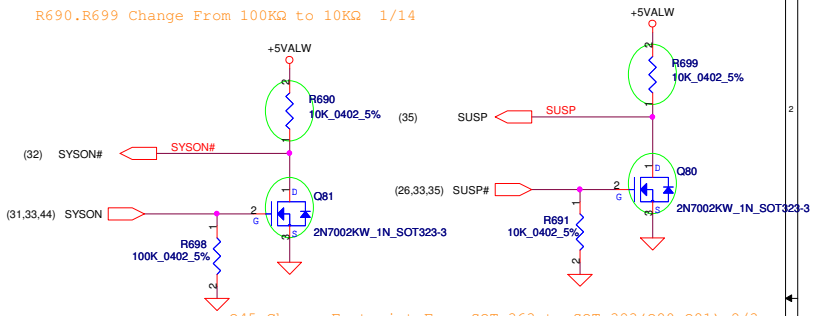




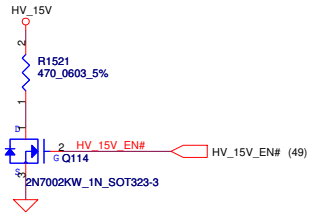
2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

Del +3VLAWS to +3V 1/8
Del +5VLAWS to +5V 1/8

R690.R699 Change From 100KΩ to 10KΩ 1/14



Q45 Change Footprint From SOT-363 to SOT-323(Q80,Q81) 2/3



4/6 remove

Security Classification	Compal Secret Data		
Issued Date	2009/11/23	Deciphered Date	2010/11/23

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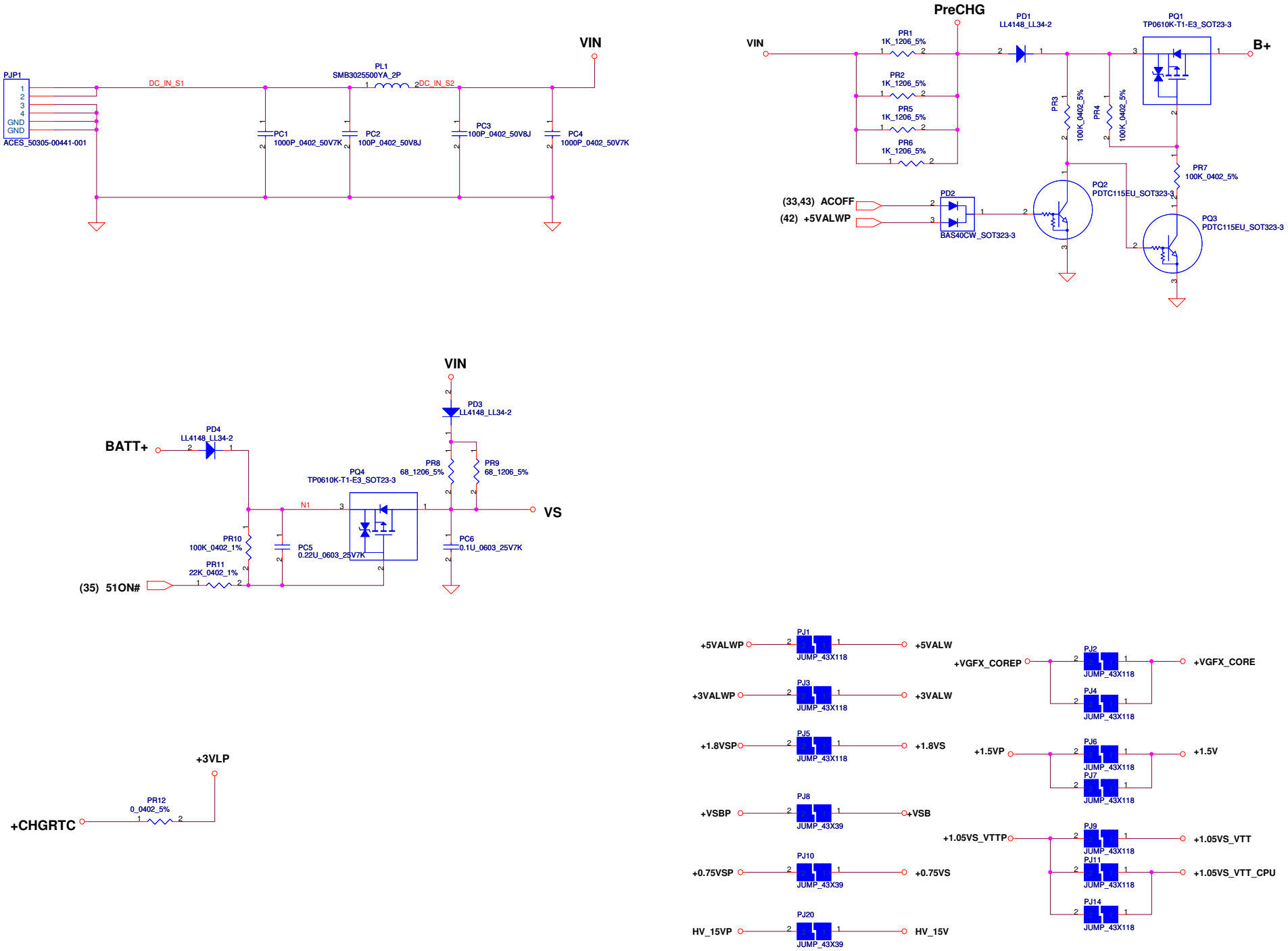
Compal Electronics, Inc.

Title: ***DC Interface***

Size: B | Document Number: ***PAU30 M/B LA-6392P Schematic*** | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 39 of 51



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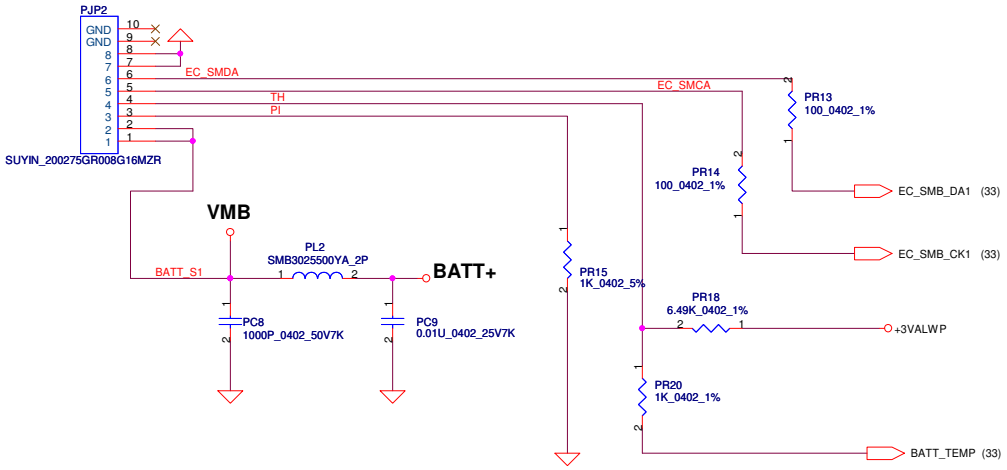
Compal Electronics, Inc.

Title: **DCIN & PRECHARGE**

Size: Custom | Document Number: SR40 Schematic | Rev: 0.1

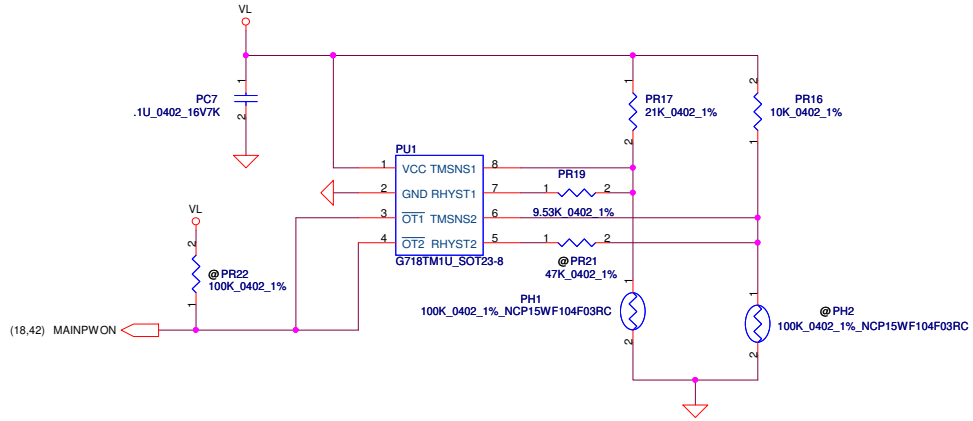
Date: Monday, November 22, 2010 | Sheet 40 of 51

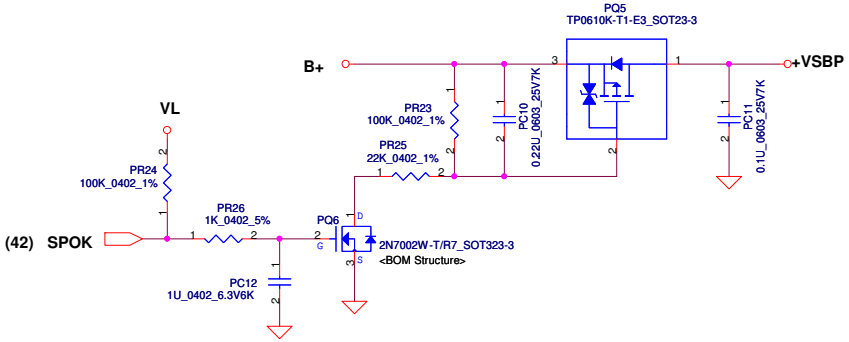


PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 56 degree C





Security Classification	Compal Secret Data		
Issued Date	2009/11/23	Deciphered Date	2010/11/23

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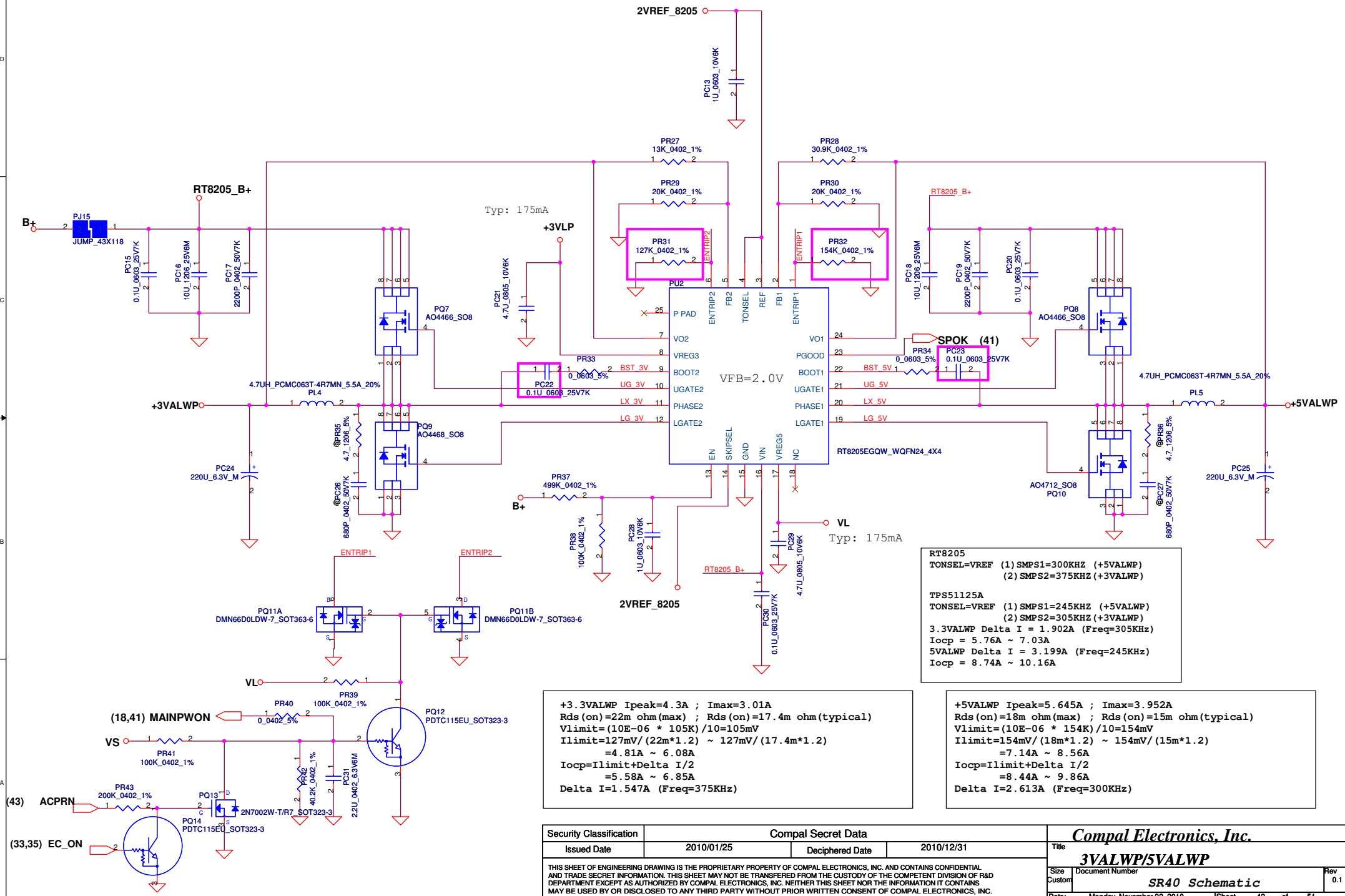
Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

Size: Custom | Document Number: *SR40 Schematic* | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 41 of 51

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO




```
RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
            (2)SMPS2=375KHZ(+3VALWP)

TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
            (2)SMPS2=305KHZ(+3VALWP)
3.3VALWP Delta I = 1.902A (Freq=305KHz)
Iocp = 5.76A ~ 7.03A
5VALWP Delta I = 3.199A (Freq=245KHz)
Iocp = 8.74A ~ 10.16A
```

```
+3.3VALWP Ipeak=4.3A ; Imax=3.01A
Rds(on)=22m ohm(max) ; Rds(on)=17.4m ohm(typical)
Vlimit=(10E-06 * 105K)/10=105mV
Ilimit=127mV/(22m*1.2) ~ 127mV/(17.4m*1.2)
       =4.81A ~ 6.08A
Iocp=Ilimit+Delta I/2
       =5.58A ~ 6.85A
Delta I=1.547A (Freq=375KHz)
```

```
+5VALWP Ipeak=5.645A ; Imax=3.952A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(10E-06 * 154K)/10=154mV
Ilimit=154mV/(18m*1.2) ~ 154mV/(15m*1.2)
       =7.14A ~ 8.56A
Iocp=Ilimit+Delta I/2
       =8.44A ~ 9.86A
Delta I=2.613A (Freq=300KHz)
```

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: SR40 Schematic | Rev: 0.1

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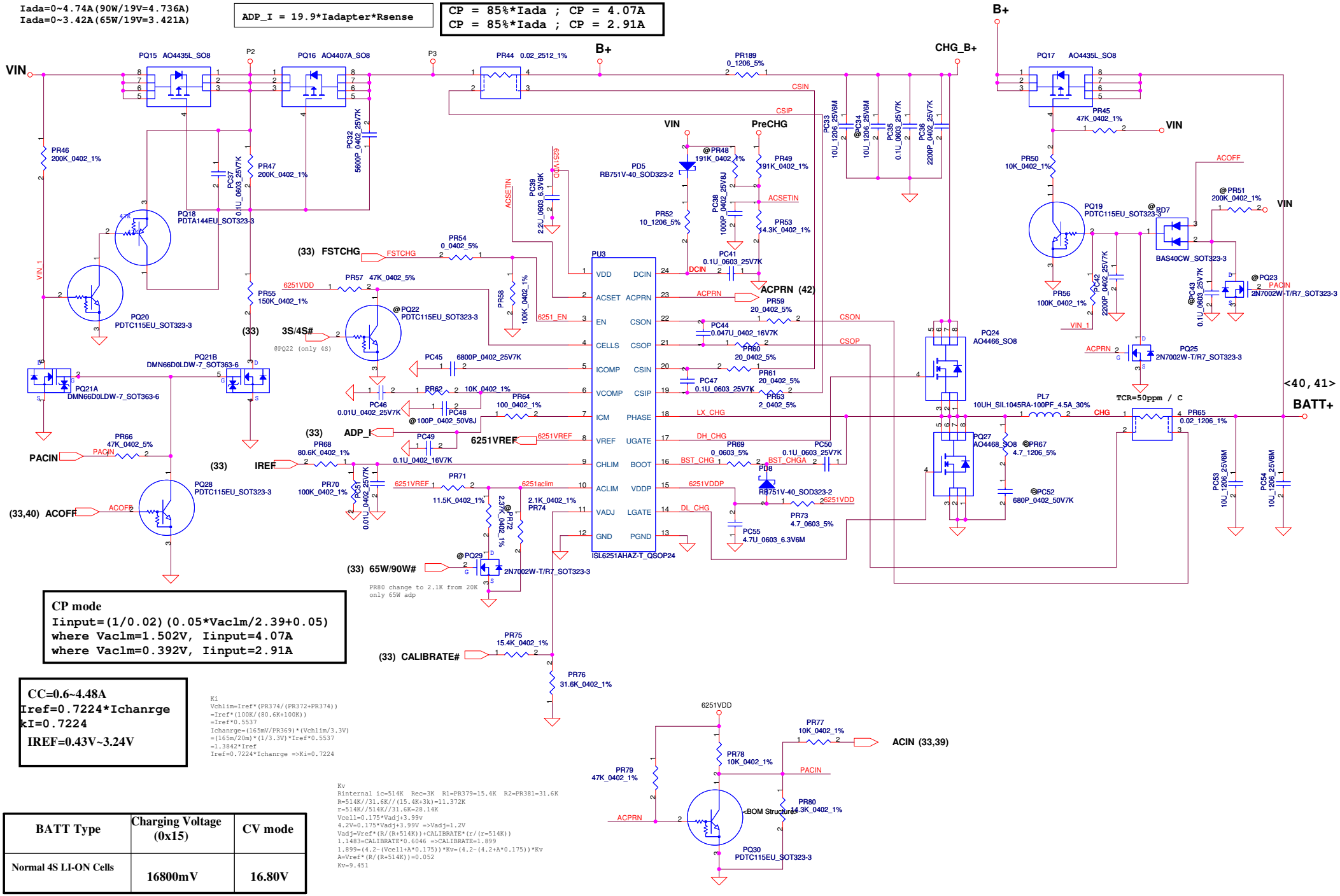
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(65W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A
where Vaclm=0.392V, Iinput=2.91A

CC=0.6~4.48A
Iref=0.7224*Ichanrge
kI=0.7224
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

BATT Type	Charging Voltage (0x15)	CV mode
Normal 4S LI-ON Cells	16800mV	16.80V

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

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Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: SR40 Schematic | Rev: 0.1

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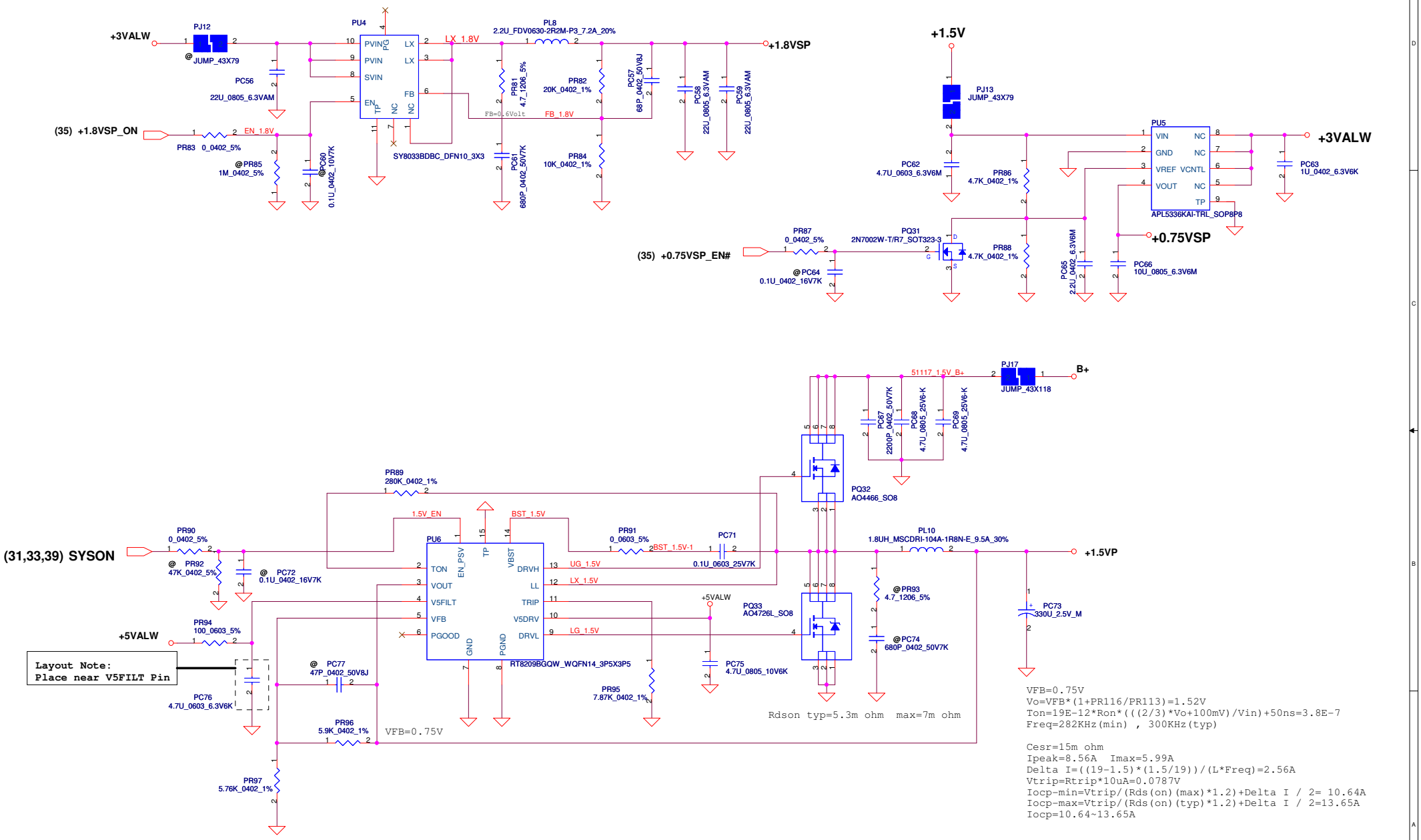
Note:Iload(max)=3.5A



VFB=0.75V
Vo=VFB*(1+PR116/PR113)=1.52V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/Vin)+50ns=3.8E-7
Freq=282KHz(min) , 300KHz(typ)

Cesr=15m ohm
Ipeak=8.56A Imax=5.99A
Delta I=((19-1.5)*(1.5/19))/(L*Freq)=2.56A
Vtrip=Rtrip*10uA=0.0787V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+Delta I / 2= 10.64A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+Delta I / 2=13.65A
Iocp=10.64~13.65A

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

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Compal Electronics, Inc.

Title: **+1.8VSP/+1.5VP/+0.75VSP**

Size	Document Number	Rev
Custom	SR40 Schematic	0.1

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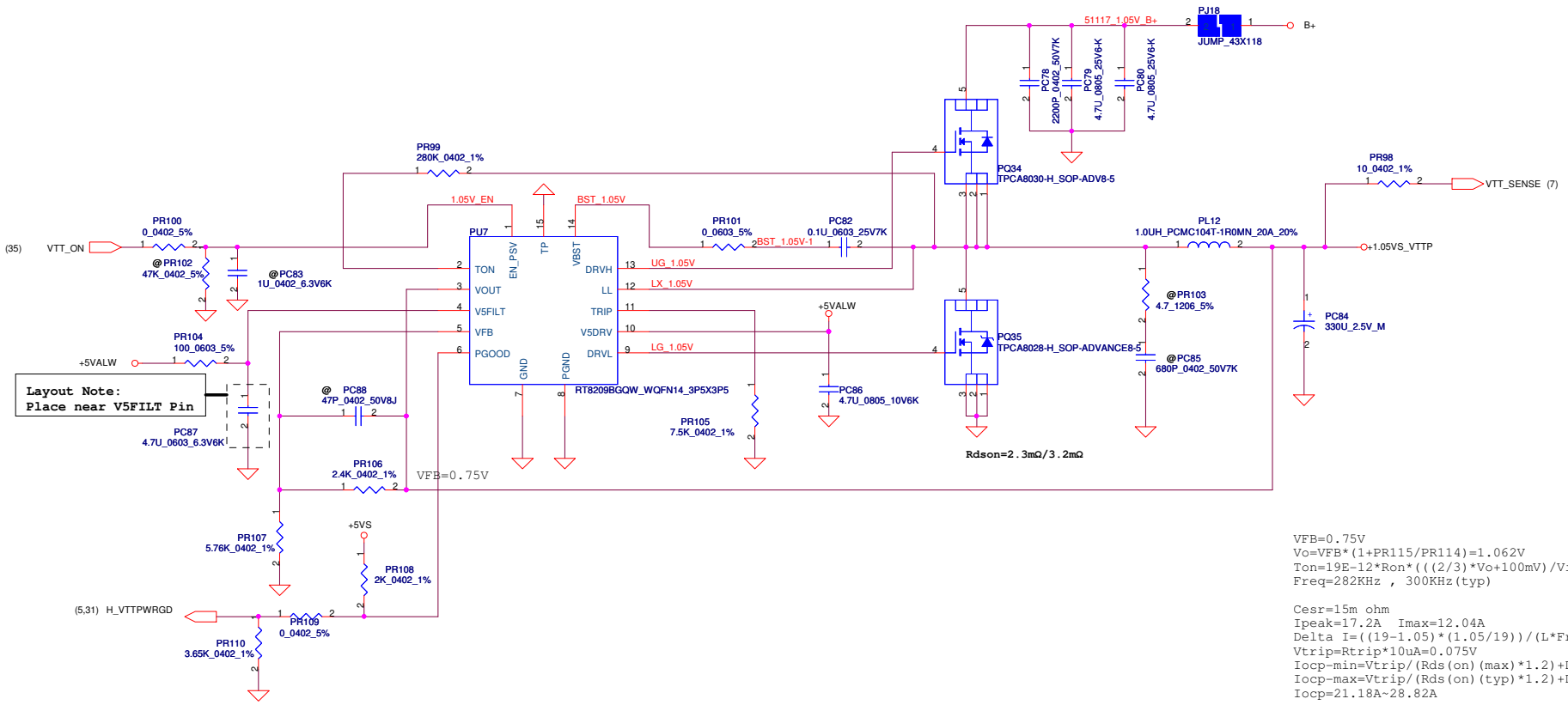

VFB=0.75V
Vo=VFB*(1+PR115/PR114)=1.062V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/Vin)+50ns=2.74E-07
Freq=282KHz , 300KHz(typ)

Cesr=15m ohm
Ipeak=17.2A Imax=12.04A
Delta I=((19-1.05)*(1.05/19))/(L*Freq)=3.306A
Vtrip=Rtrip*10uA=0.075V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+Delta I / 2= 21.18A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+Delta I / 2=28.82A
Iocp=21.18A~28.82A

Security Classification	Compal Secret Data		
Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

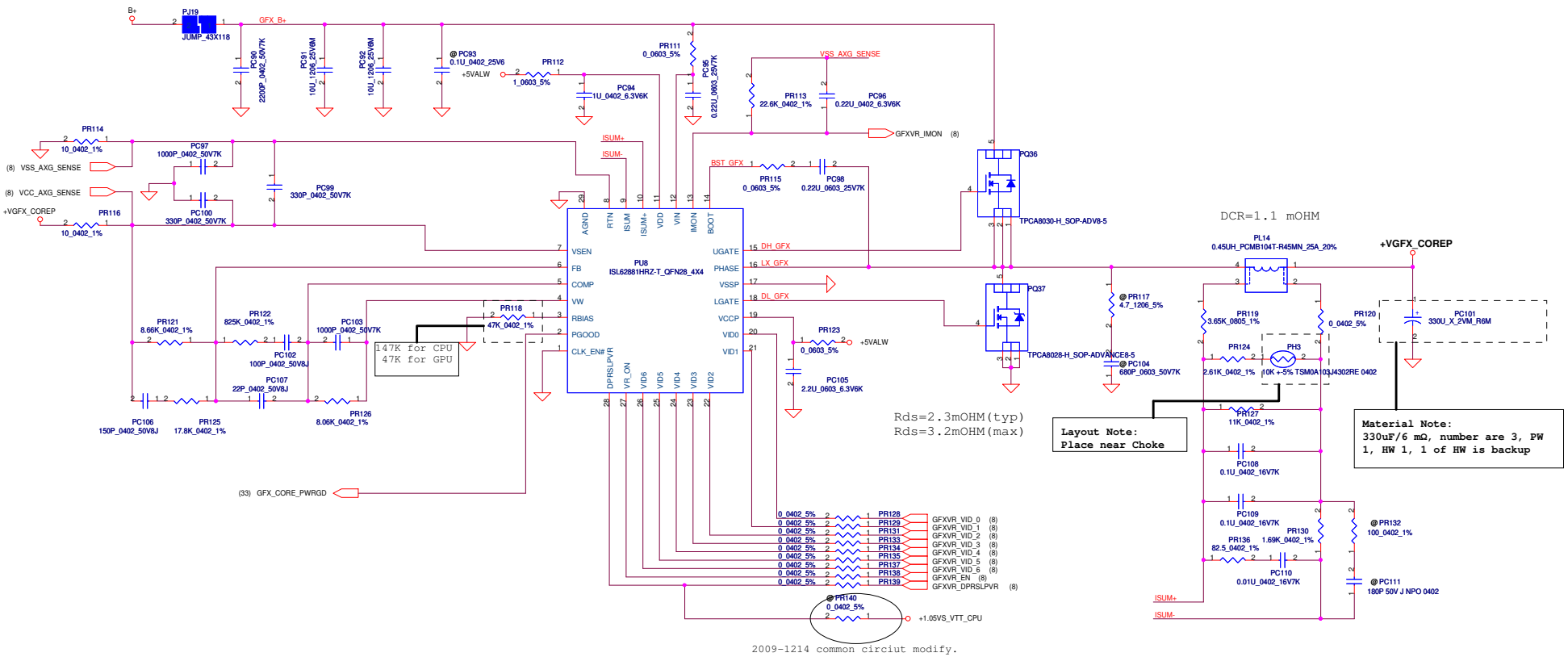
Title: **+1.05VS_VTTP**

Size: Custom | Document Number: *SR40 Schematic* | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 45 of 51

```
Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR127 // (PR124+PH3)=5.875k ohm
Rsum=PR119=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR121=2.87k ohm, Ri=PR130=562 ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A
```

```
Vvid = 1.25
LL = 7m ohm
Iccaxg = 22A
Icctdc_axg = 12 A
Iccaxg_dyn 19 A
```



2009-1214 common circiut modify.

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2009/4/15	Deciphered Date	2010/04/15	Title: GFX_COREP
				Size: C; Document Number: SR40 Schematic; Rev: 0.1
				Date: Monday, November 22, 2010; Sheet 46 of 51

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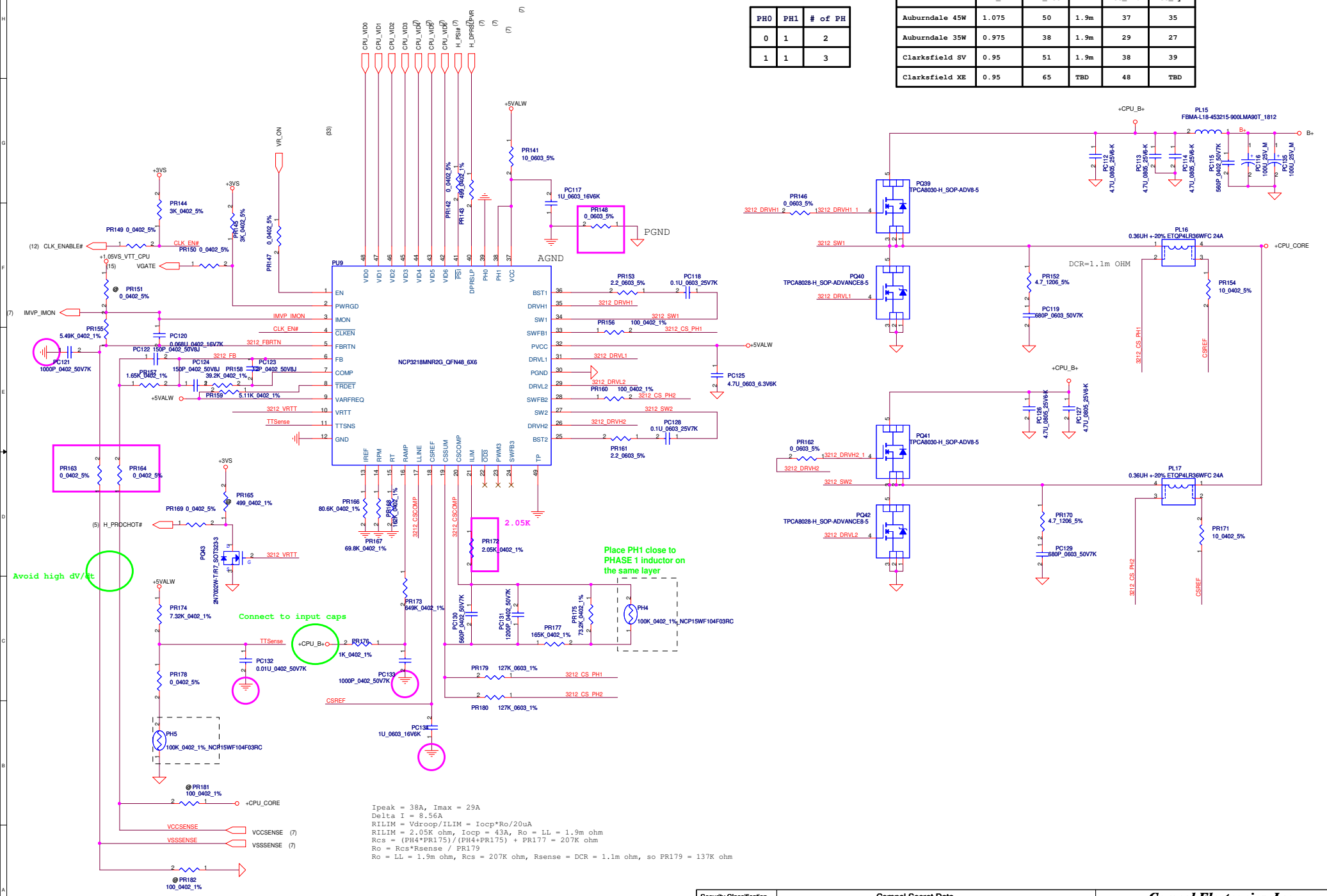
PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Ipeak = 38A, Imax = 29A
Delta I = 8.56A
RILIM = Vdroop/ILIM = Iocp*Ro/20uA
RILIM = 2.05K ohm, Iocp = 43A, Ro = LL = 1.9m ohm
Rcs = (PH4*PR175)/(PH4+PR175) + PR177 = 207K ohm
Ro = Rcs*Rsense / PR179
Ro = LL = 1.9m ohm, Rcs = 207K ohm, Rsense = DCR = 1.1m ohm, so PR179 = 137K ohm

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Issued Date	2009/02/04	Deciphered Date	2010/02/04

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Compal Electronics, Inc.

Title: CPU_CORE

Size: C | Document Number: SR40 Schematic | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 47 of 51

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	change bead to jamp	6 layers change to 8 layers, so change bead to jamp	0.1	50	1 del PC14 SE074681K80 (S CER CAP 680P 50V K X7R 0402) 2 del PL3 SM010016380 (FBMA-L11-322513-201LMA40T)	2010-0617	to DVT
2	change bead to jamp	6 layers change to 8 layers, so change bead to jamp	0.1	51	del PL6 SM010016380 (FBMA-L11-322513-201LMA40T)	2010-0617	to DVT
3	change bead to jamp	6 layers change to 8 layers, so change bead to jamp	0.1	52	1 del PC70 SE074561K80 (S CER CAP 560P 50V K X7R 0402) 2 del PL9 SM010016380 (FBMA-L11-322513-201LMA40T)	2010-0617	to DVT
4	change bead to jamp	6 layers change to 8 layers, so change bead to jamp	0.1	53	1 del PC81 SE074561K80 (S CER CAP 560P 50V K X7R 0402) 2 del PL11 SM010020720 (FBMA-L18-453215-900LMA90T)	2010-0617	to DVT
5	change bead to jamp	6 layers change to 8 layers, so change bead to jamp	0.1	54	1 del PC89 SE074561K80 (S CER CAP 560P 50V K X7R 0402) 2 del PL13 SM010016380 (FBMA-L11-322513-201LMA40T)	2010-0617	to DVT
6	change main souce	cost down	0.1	54	Chnage PQ36 from SB000008L80(S TR SI7686DP-T1-E3 1N POWERPAK SO8) to SB00000HL00(S TR TPCA8030-H 1N SOP-ADV) change PQ37 from SB000009F80(S TR AO4456 1N SO8) to SB00000GL00(S TR TPCA8028-H 1N SOP ADVANCE) Del PQ38 SB000009F80(S TR AO4456 1N SO8)	2010-0617	to DVT
7	reduce components quantity	cost down	0.1	53	Chnage PR104 from SD014100080(S RES 1/10W 100 +-5% 0603) to SD013100080 (S RES 1/10W 100 +-1% 0603)	2010-0624	to DVT
8	reduce components quantity	cost down	0.1	52	Chnage PR94 from SD014100080(S RES 1/10W 100 +-5% 0603) to SD013100080 (S RES 1/10W 100 +-1% 0603)	2010-0624	to DVT
9	change main souce	cost down	0.1	51	Chnage PQ15, PQ17 from SB00000DL00(S TR AO4407A 1P SO8) to SB00000DJ10 (S TR AO4435L 1P SO8)	2010-0624	to DVT
10	change main souce	cost down	0.1	51	Chnage PQ27 from SB00000CG00(S TR AO4466 1N SO8) to SB000009580 (S TR AO4468 1N SO8)	2010-0624	to DVT
11	change main souce	cost down	0.1	50	Chnage PQ9 from SB00000AJ00(S TR AO4712 1N SO8) to SB000009580 (S TR AO4468 1N SO8)	2010-0624	to DVT
12	adjust OCP setting	Because Rds(on) change to 22m(MAX) and 17.4m(TYP) ohm of low side MOS, so change OCP setting	0.1	50	Chnage PR31 from SD034105380(S RES 1/16W 105K +-1% 0402) to SD034127380 (S RES 1/16W 127K +-1% 0402)	2010-0624	to DVT
13	change main souce	ISL62881C has hang up issue, so change to ISL62881.	0.2	54	Chnage PU8 from SA000043N00(S IC ISL62881CHRZ-T QFN 28P PWM) to SA000030200 (S IC ISL62881HRZ-T QFN 28P PWM)	2010-0713	to DVT
14	adjust resistance value	adjust resistance value for ISL62881	0.2	54	Chnage PR113 from SD034750180(S RES 1/16W 7.5K +-1% 0402) to SD034226280 (S RES 1/16W 22.6K +-1% 0402)	2010-0713	to DVT
15	adjust resistance value	adjust resistance value for ISL62881	0.2	54	Chnage PR121 from SD034287180(S RES 1/16W 2.87K +-1% 0402) to SD034866180 (S RES 1/16W 8.66K +-1% 0402)	2010-0713	to DVT
16	adjust resistance value	adjust resistance value for ISL62881	0.2	54	Chnage PR130 from SD000009380(S RES 1/16W 562 +-1% 0402) to SD00000JB80 (S RES 1/16W 1.69K +-1% 0402)	2010-0713	to DVT
17	add resistance	pop resistance for ISL62881	0.2	54	add PR136 SD034825A80(S RES 1/16W 82.5 +-1% 0402)	2010-0713	to DVT
18	add cup.	pop Cup. for ISL62881	0.2	54	add PC110 SE076103K80(S CER CAP .01U 16V K X7R 0402)	2010-0713	to DVT
19	adjust capacitor	Because ME height limit, so change to 8 height capacitor.	0.2	55	Chnage PC116 from SF22004M210(S ELE CAP 220U 25V M 8X10.2 CE-AX) to SF000000S80 (S ELE CAP 100U 25V M 6.3X7.7 CE-LX)	2010-0713	to DVT
20	add cup.	Because ME height limit, so add an 8 height capacitor.	0.2	55	Add PC135 SF000000S80 (S ELE CAP 100U 25V M 6.3X7.7 CE-LX)	2010-0713	to DVT
21	adjust resistance value	adjust resistance value for CPU loadline	0.2	55	Chnage PR179 and PR180 from SD014137380(S RES 1/10W 137K +-1% 0603) to SD014127380(S RES 1/10W 127K +-1% 0603)	2010-0715	to DVT
22	adjust resistance value	adjust resistance value for +5Valwp to 5.1V	0.2	50	Chnage PR28 from SD034300280(S RES 1/16W 30K +-1% 0402) to SD034309280(S RES 1/16W 30.9K +-1% 0402)	2010-0723	to DVT

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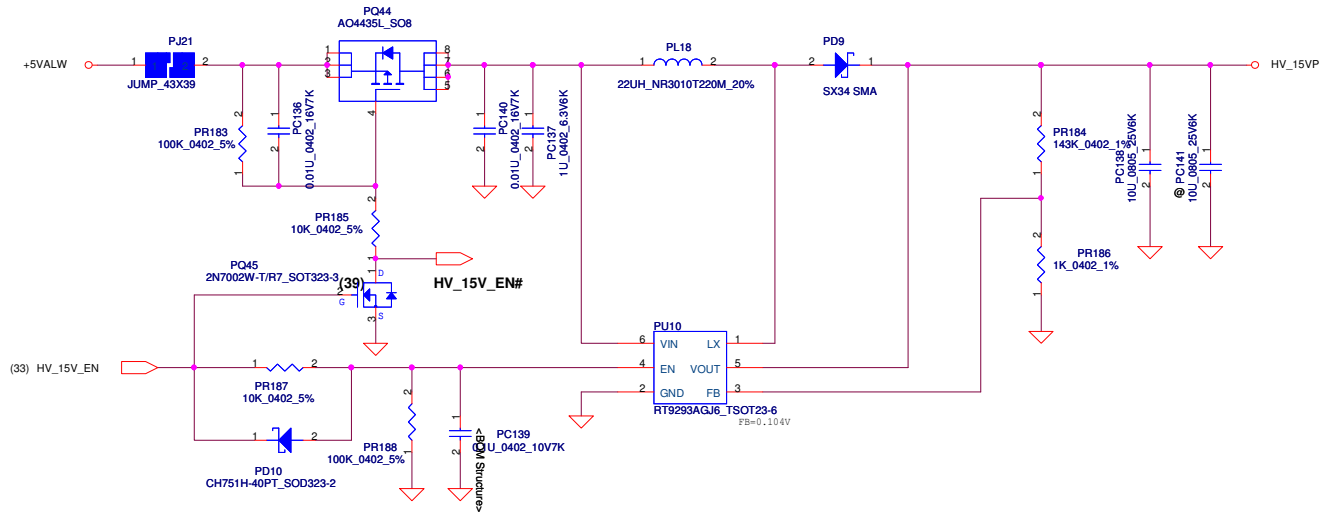

Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

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Compal Electronics, Inc.

Title: 12V

Size | Document Number | Rev 0.3

Date: Monday, November 22, 2010 | Sheet 49 of 51

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	EMI reguest reserve 0 ohm	EMI reguest reserve 0 ohm for EMI ISN test	0.3	43	change PJ16 to SD011000080(S RES 1/4W 0 +-5% 1206)	2010-0907	PVT
2	Add boost resister	EMI reguest add boost resister for EMI test	0.3	47	change PR153 and PR161 form SD013000080 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	2010-0907	PVT
3	Add snubber	EMI request add snubber for EMI test	0.3	47	Add PR152 and PR170 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC119 and PC129 SE025681K80(S CER CAP 680P 50V K X7R 0603)	2010-0907	PVT
4	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PU10 SA00004DD00(S IC RT9293AGJ6 TSOT-23 6P BOOST) Add PL18 SHI00005P00(S INDUC_ 22UH +-20% NR3010T220M)	2010-0907	PVT
5	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PD9 SCSSSM24A20(S DIO SSM24APT SMA-S) Add PQ44 SB00000DJ10(S TR AO4435L 1P SO8) Add PQ45 SB000006800(S TR 2N7002W T/R7 1N SOT-323)	2010-0907	PVT
6	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PD10 SC1H751H010(S DIO CH751H-40PT SOD323) Add PR183, PR188 SD028100380(S RES 1/16W 100K +-5% 0402) Add PR185, PR187 SD028100280(S RES 1/16W 10K +-5% 0402)	2010-0907	PVT
7	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PC136, PC140 SE076103K80(S CER CAP .01U 16V K X7R 0402) Add PC137 SE000000U00(S CER CAP 1U 16V K X5R 0402) Add PC139 SE102104K00(S CER CAP 0.1U 10V +-10% X7R 0402)	2010-0907	PVT
8	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PR184 SD034143380(S RES 1/16W 143K +-1% 0402) Add PR186 SD034100180(S RES 1/16W 1K +-1% 0402)	2010-0907	PVT
9	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PC138 SE00000QK00(S CER CAP 10U 25V K X5R 0805 H1.25)	2010-0907	PVT
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Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

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Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number | Rev 0.1

Date: Thursday, October 28, 2010 | Sheet 50 of 51

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1			0.1	48			
2			0.1	50			
3			0.1	51			
4			0.1	51			
5			0.1	52			
6			0.1	53			
7			0.1	46			
8			0.1	47			
9			0.1	52			
10			0.1	48			
11			0.1	52			
12			0.1	52			
13			0.2	46			
14			0.2	51			
15			0.2	52			
16			0.2	53			
17			0.2	52			
18			0.2	50			
19			0.2	55			
20			0.2	53			
21			0.2	55			
22			0.2	48			
23			0.2	52			

Security Classification	Compal Secret Data		
Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 0.1

Date: Tuesday, September 07, 2010 | Sheet 51 of 51