

Compal Confidential

JAQ10 M/B Schematics Document

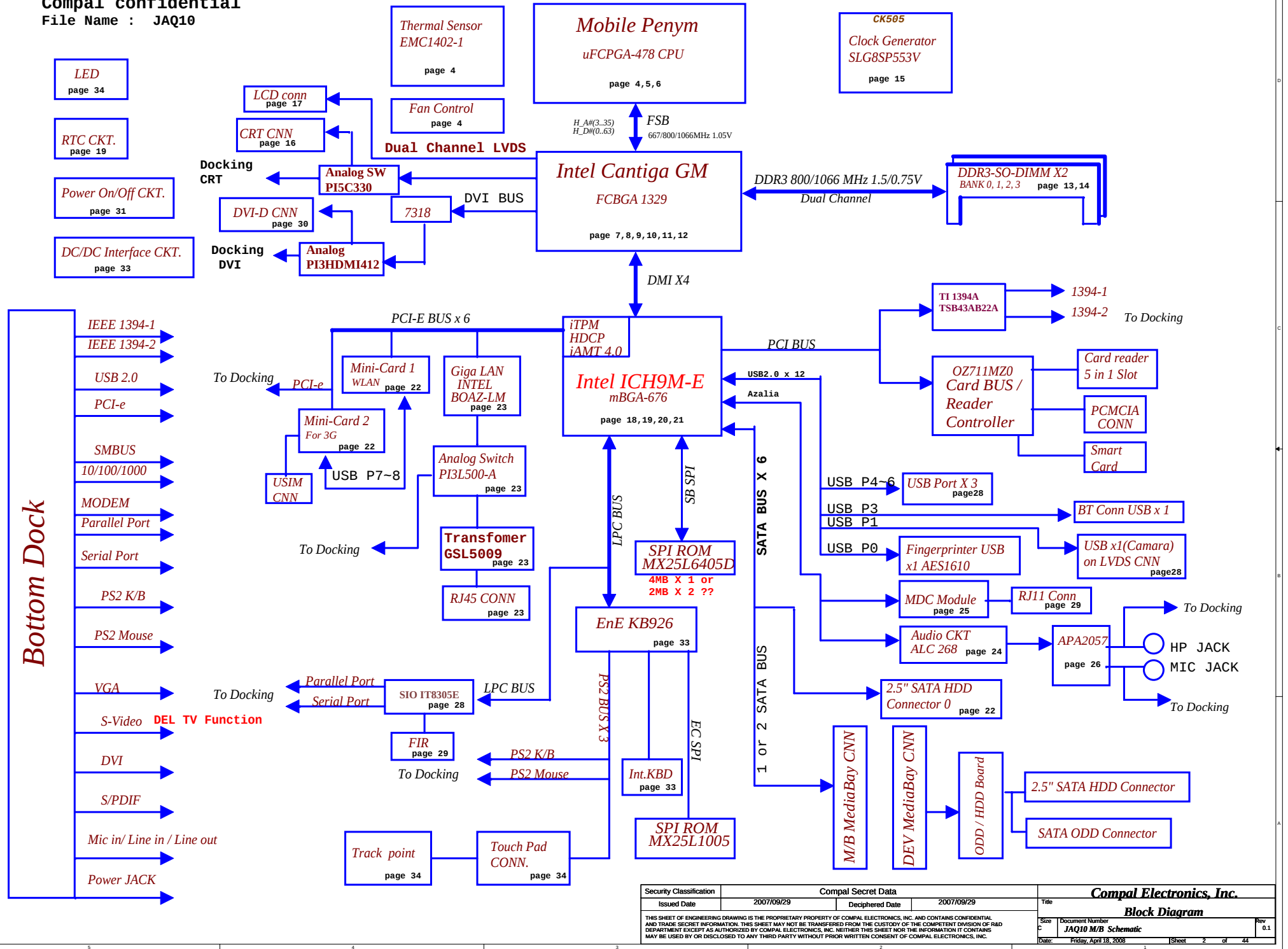
Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2008-04-21

REV: 0.4

Security Classification		Compal Secret Data		Title		
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Montevina Commercial UMA



Voltage Rails

Power Plane	Description	S1	S3/M1	S5/M1
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75VS power rail for DDR3 terminator	ON	OFF/ON	OFF/ON
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.05VM	1.05VM switched power rail	ON	OFF/ON	OFF/ON
+1.5V	1.5V power rail for HDA	ON	ON	OFF/ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	OFF/ON	OFF/ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394 TI	AD21	3	PIRQ-F
PCMCIA + Card Reader + Small Card	AD22	2	PIRQ-E

External PCI-e Devices

Device	PORT NO.	Interrupts
MINI CARD1 WLAN	P1	??
MINI CARD2 3G	P2	??
DOCKING PCI-E	P5	??
INTEL GIGA LAN	P6	??

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
		GMT G781-1	1001 101X b

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
HDMI Analog S/W	1100 000Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

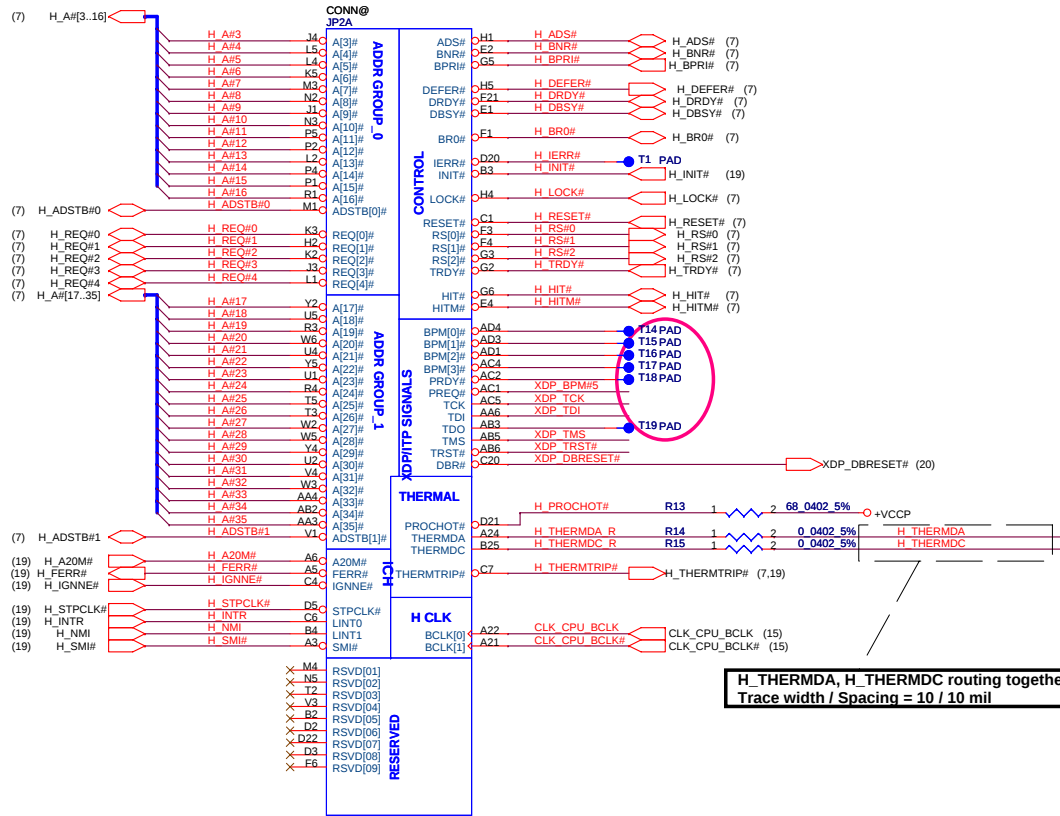
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

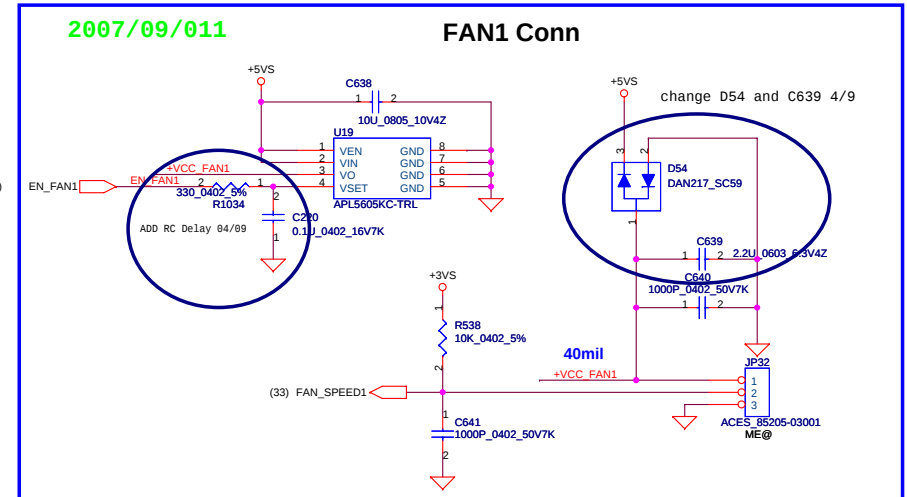
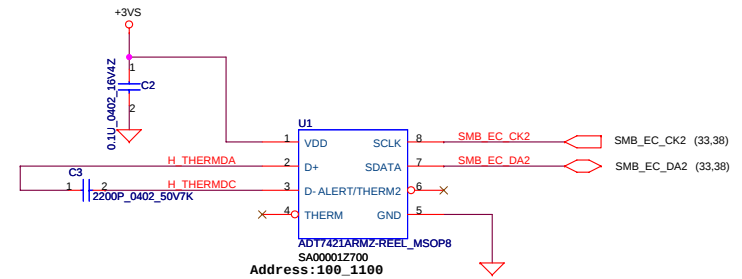
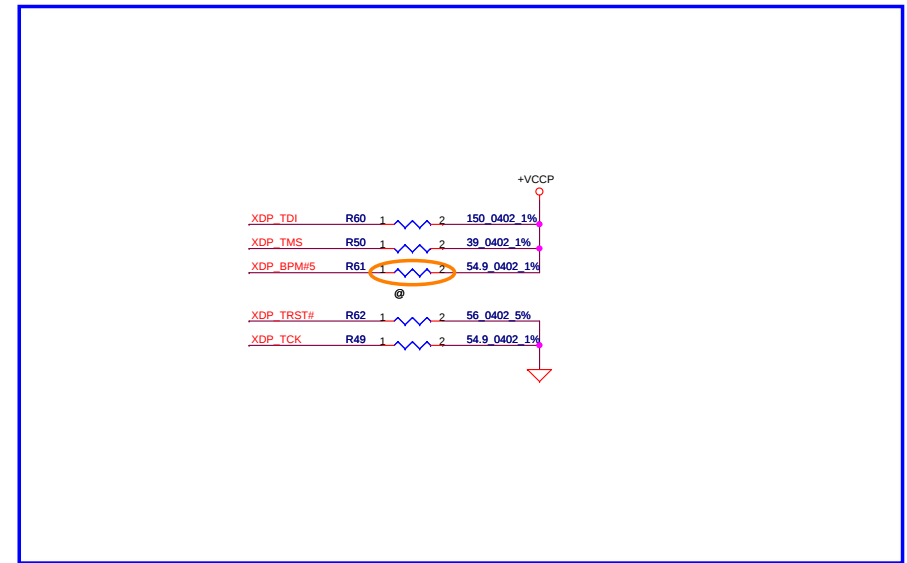
BTO Option Table

BTO Item	BOM Structure
Discrete	PM@
UMA	GM@
CIR	CIR@
8111C	8111C@
8102E	8102E@
ALC888VC	888VC@
ALC888VB	888VB@
ALC268	268@

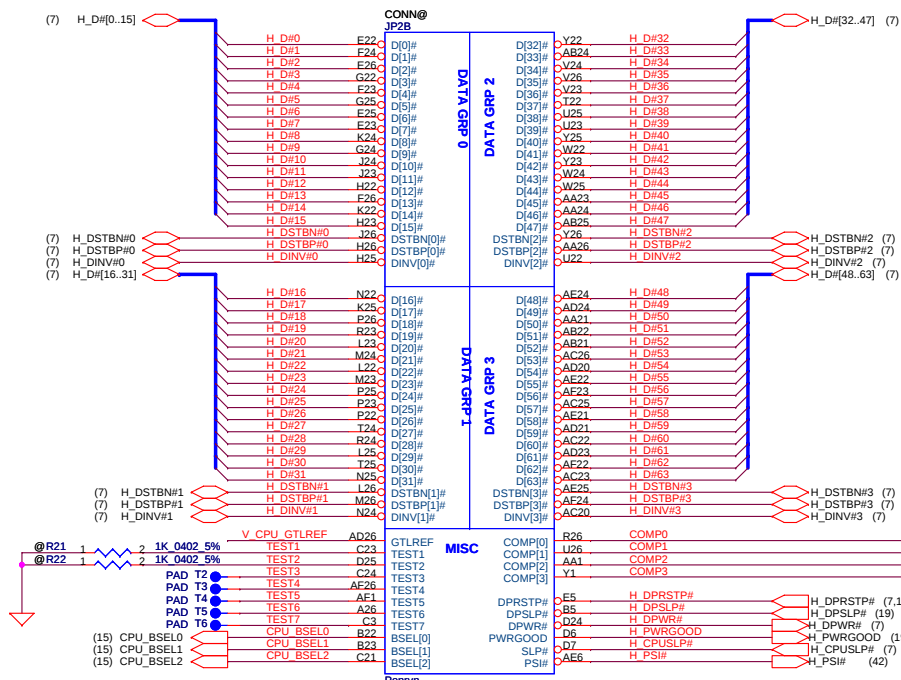
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Notes List		
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H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil



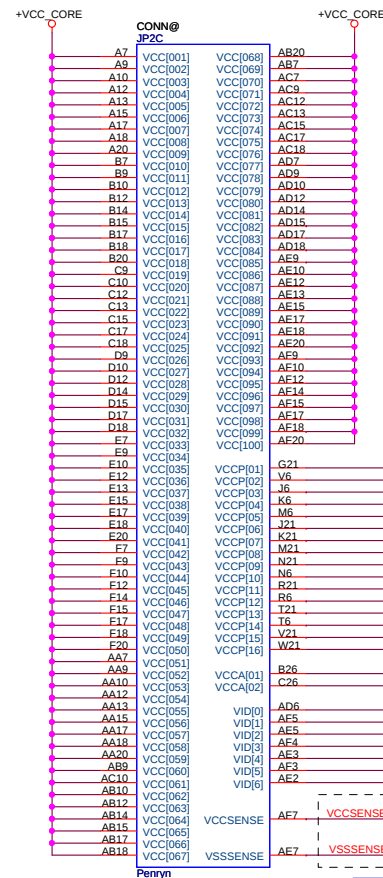
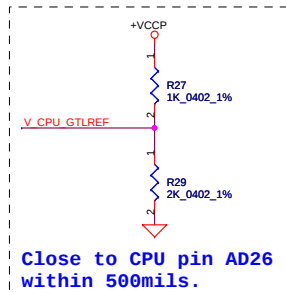
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				Deciphered Date				Title			
2007/09/29				2007/09/29				Penryn(1/3)-AGTL+/ITP-XDP			
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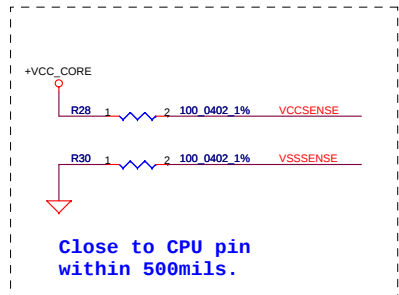
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

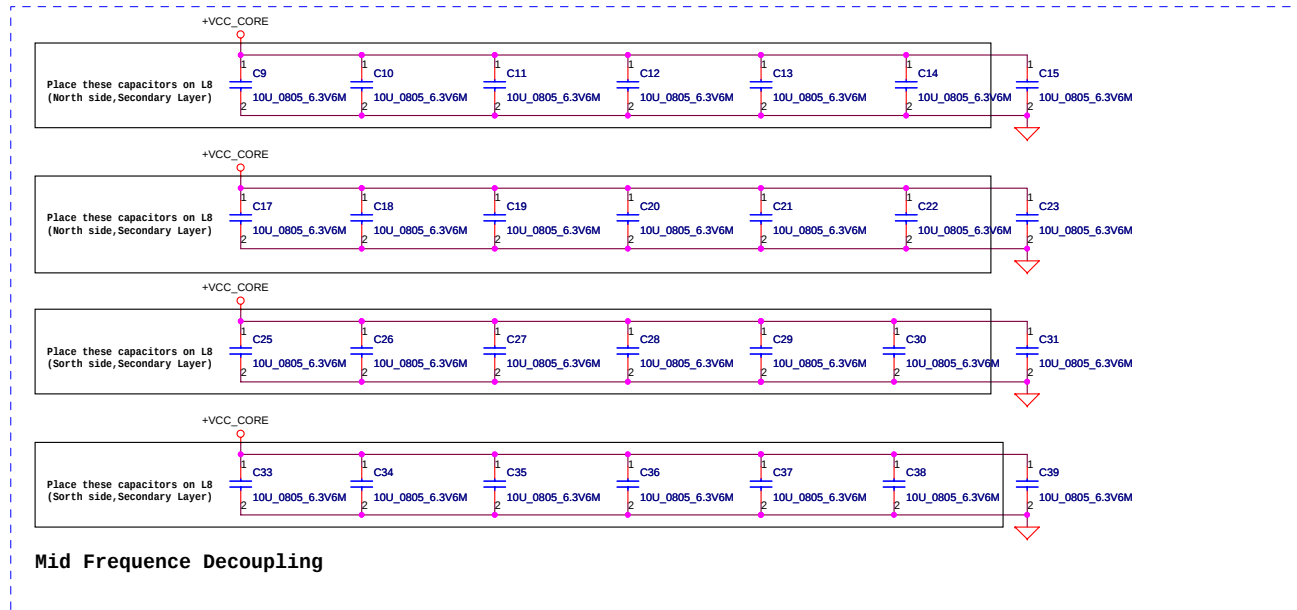
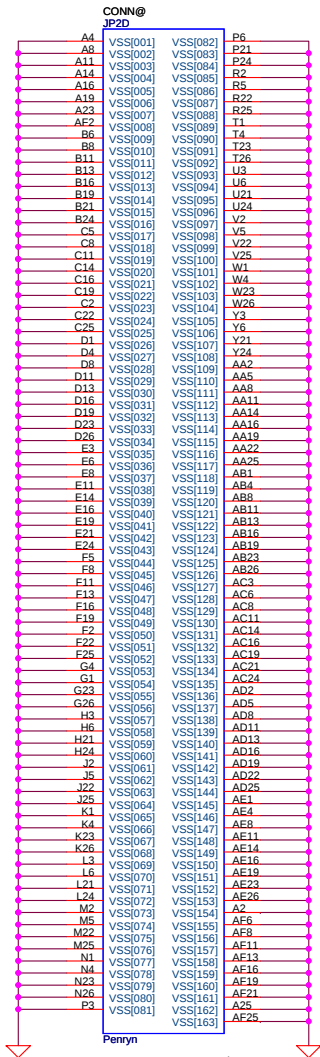
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



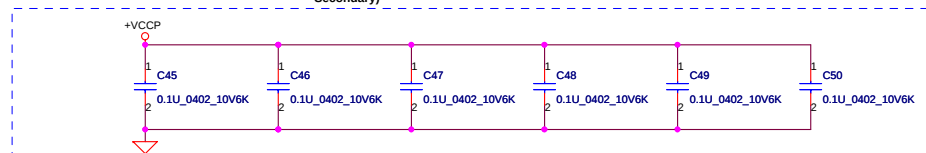
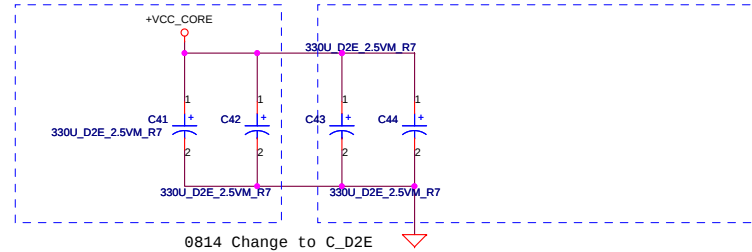
Length match within 25 mils. The trace width/space/other is 20/7/25.



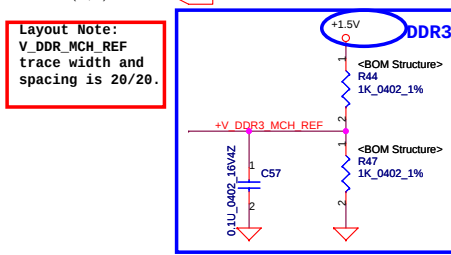
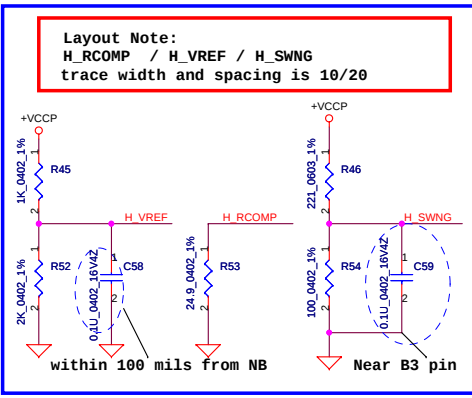
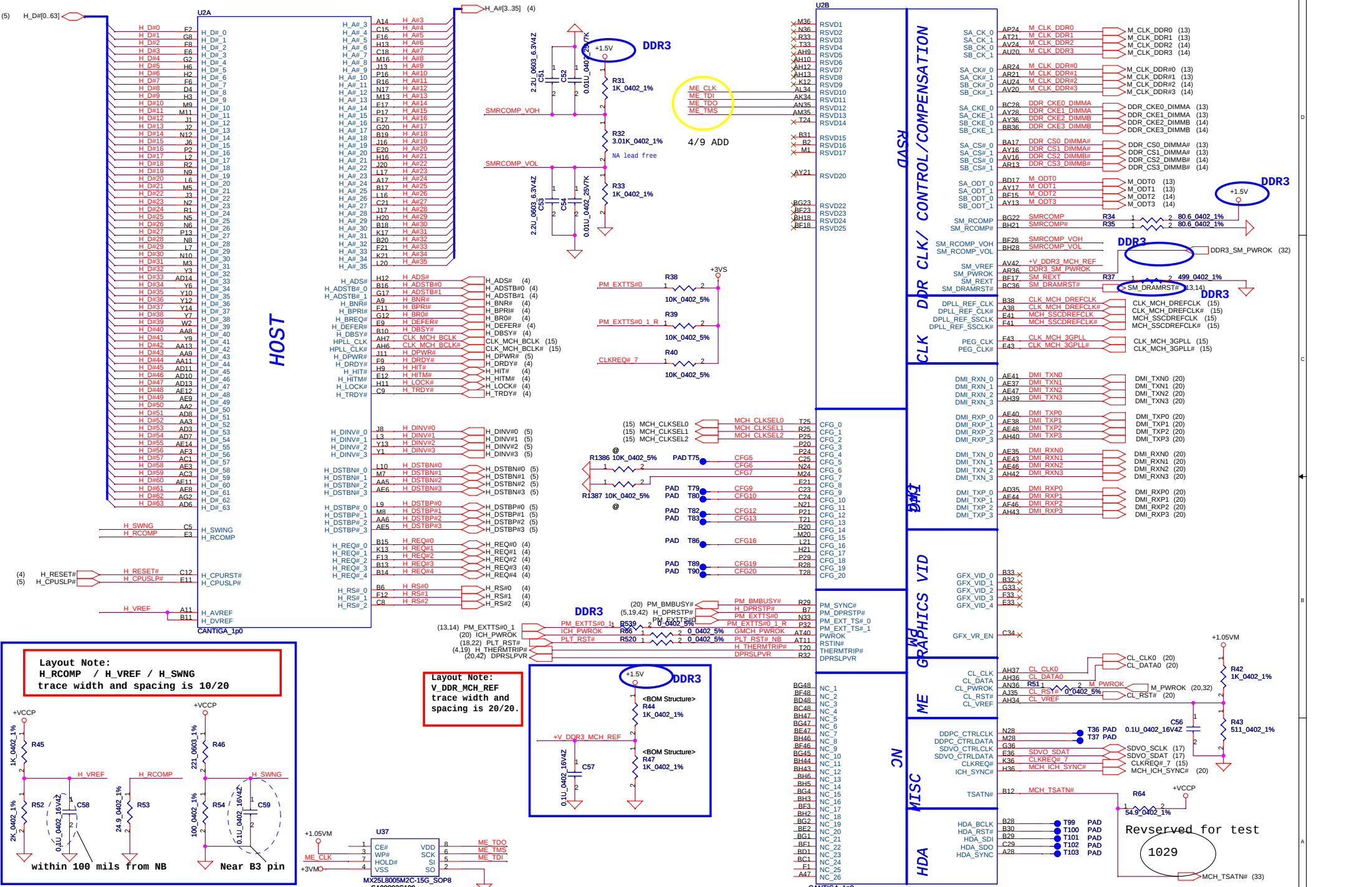


Near CPU CORE regulator

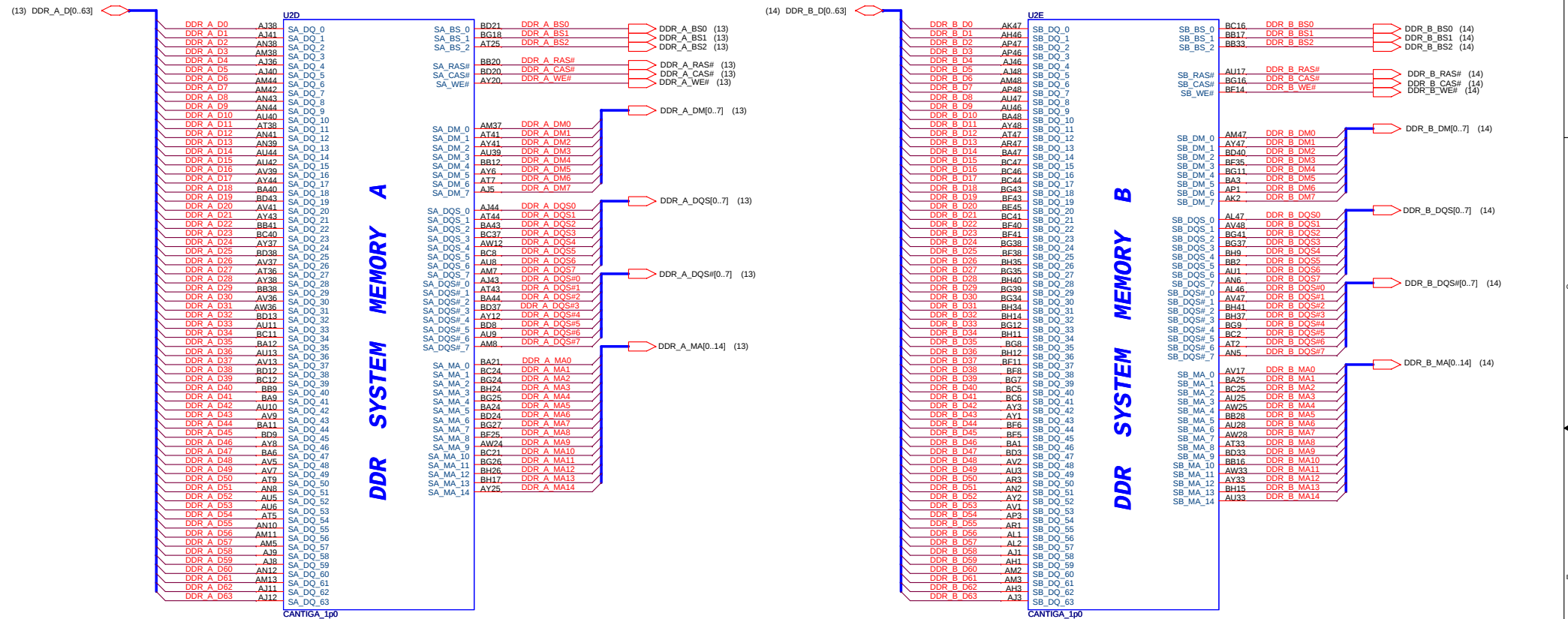
ESR <= 1.5m ohm
Capacitor > 1980uF



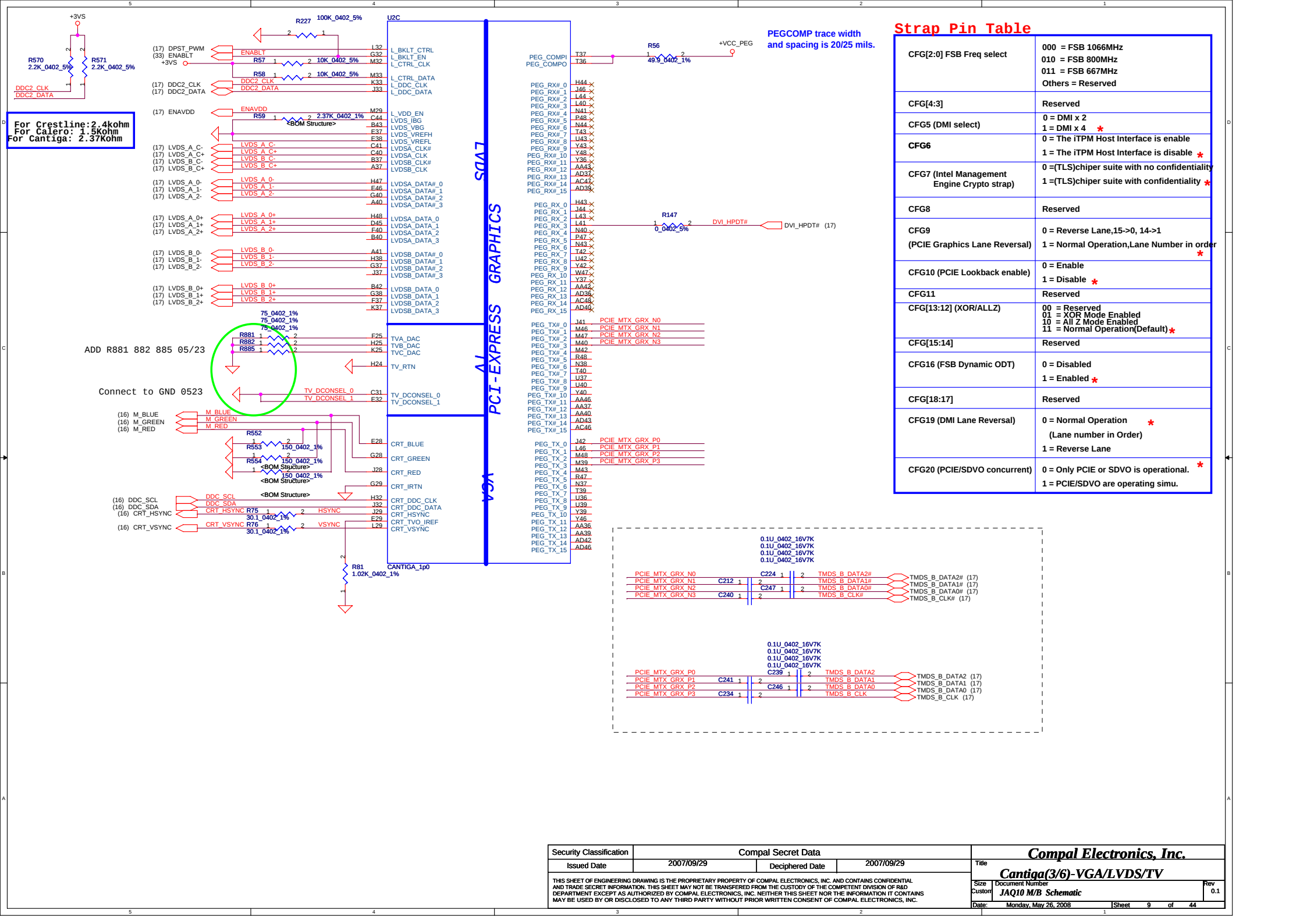
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Date: Monday, February 25, 2008		Sheet 6 of 44		Size	Rev
Cust: JAQ10 M/B Schematic				Document Number	0.1

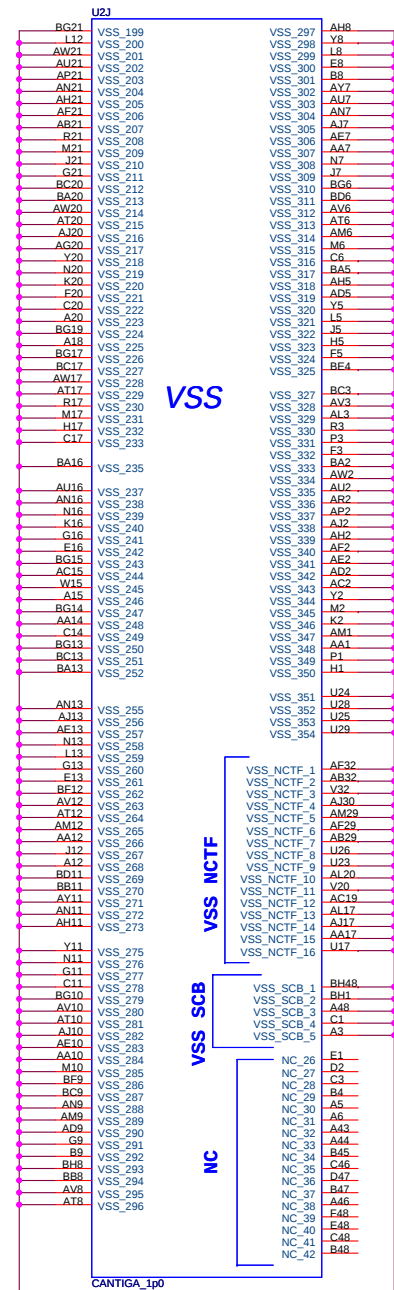
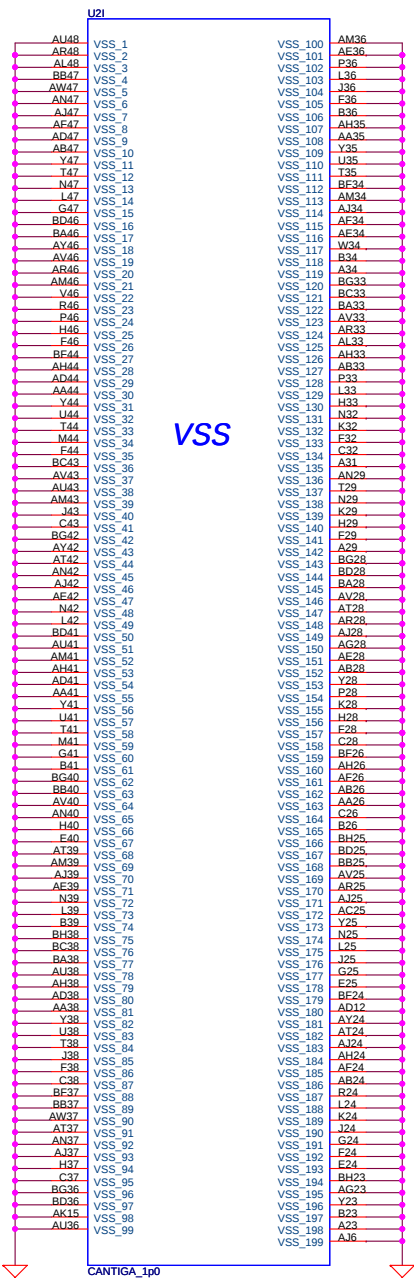


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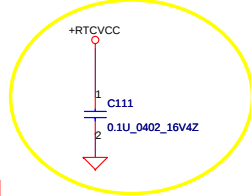
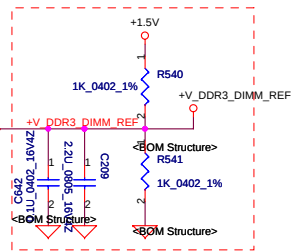




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Date: Tuesday, October 30, 2007				Sheet 12	Rev 0.1

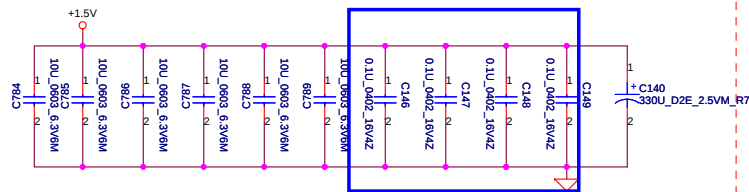
- (8) DDR_A_DQS#0[0..7]
- (8) DDR_A_D[0..63]
- (8) DDR_A_DM[0..7]
- (8) DDR_A_DQS#0[0..7]
- (8) DDR_A_MA[0..14]

(14) +V_DDR3_DIMM_REF

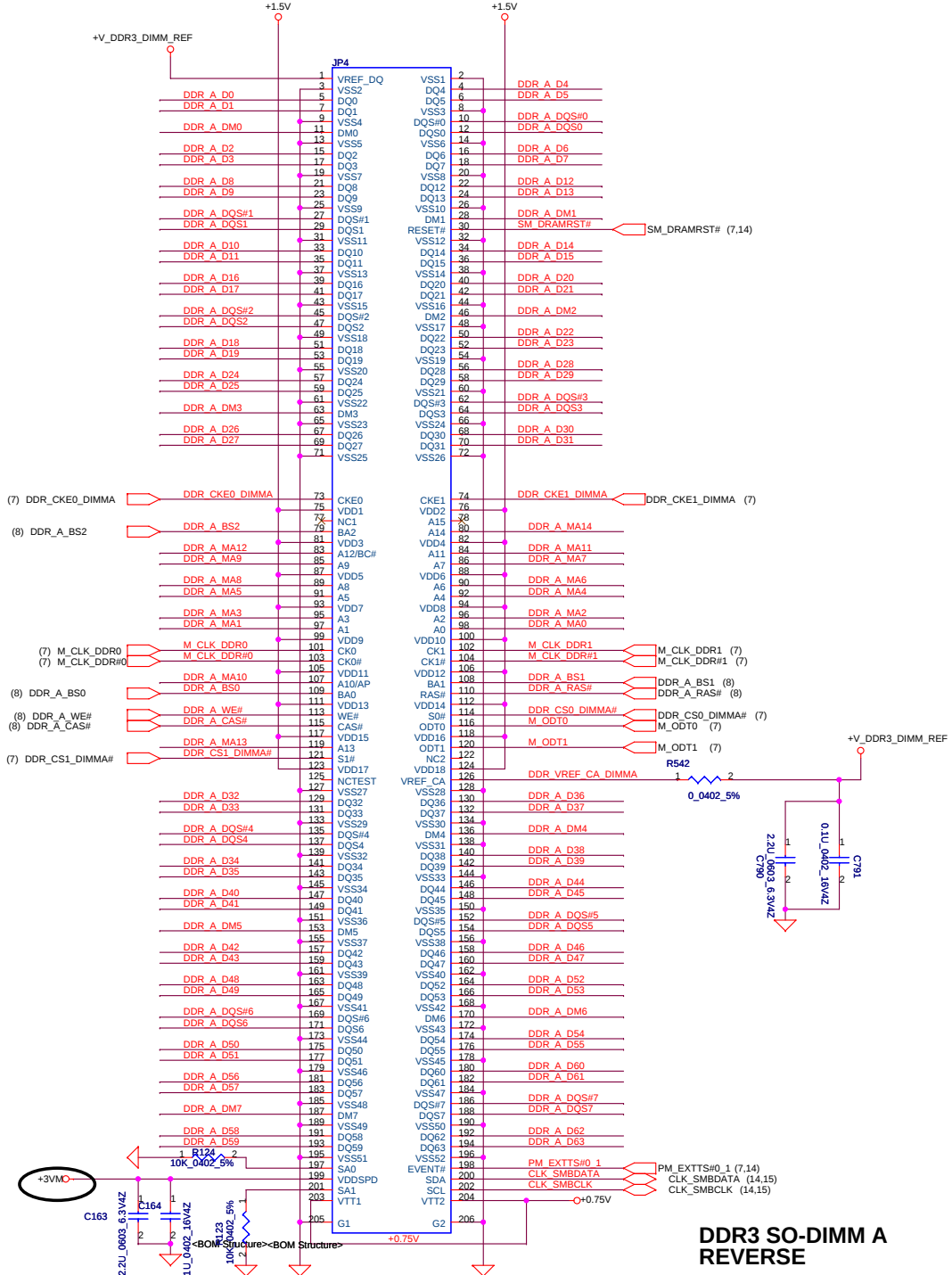
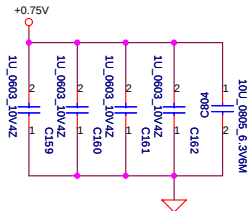


Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA



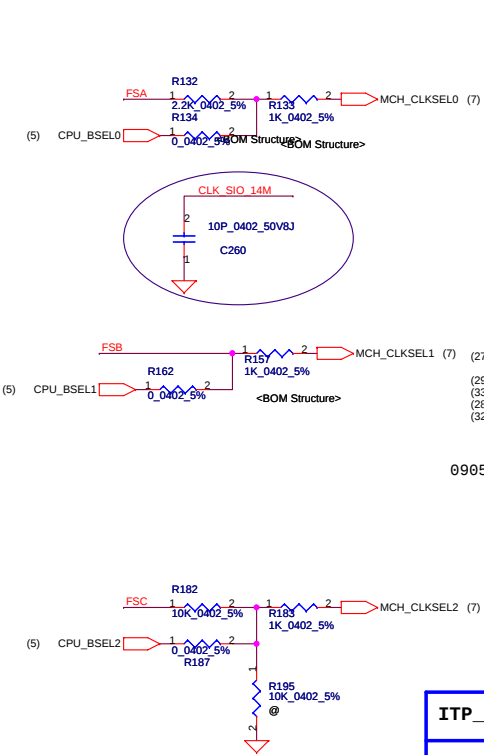
Layout Note:
Place near JP4.203 & JP4.204



DDR3 SO-DIMM A REVERSE

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Issued Date	2007/09/29	Deciphered Date	2007/09/29	DDR3 SODIMM SLOT1	
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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ	MHZ	MHZ	MHZ
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



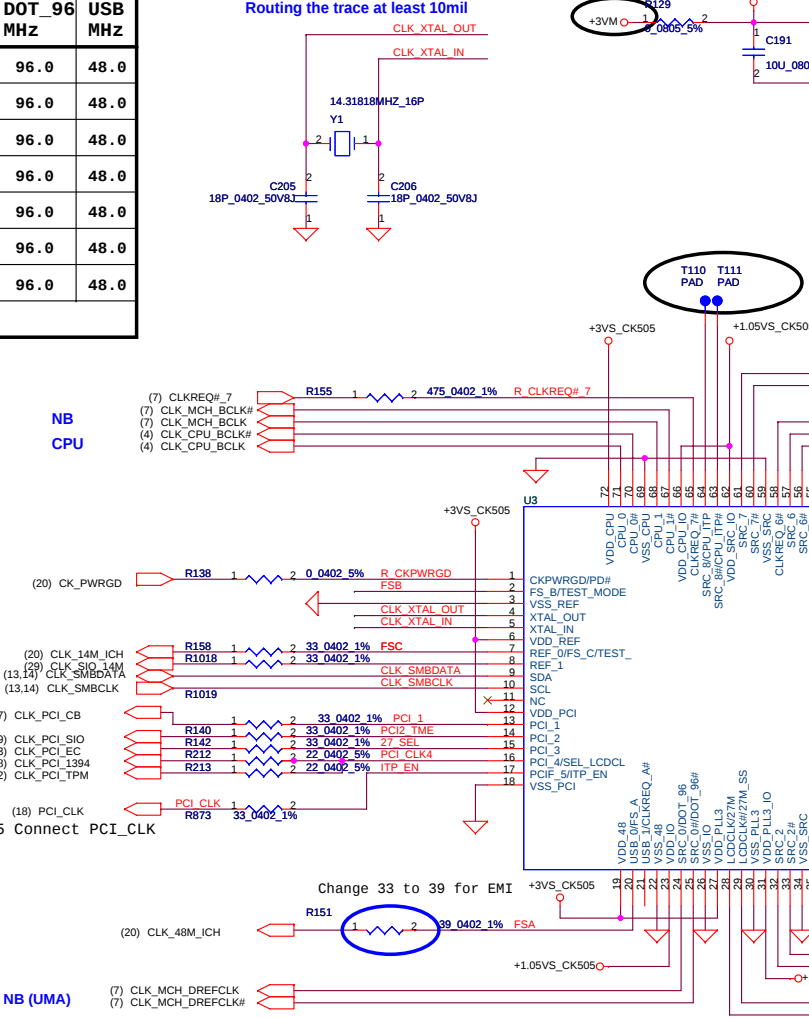
2007/09/26

for ICS Overclocking setting
0=overclocking of CPU and SRC allowed
1=overclocking of CPU and SRC NOT allowed

NB
CPU

NB (UMA)

ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)



M:ICS P/N:
S: Silego

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Place close to U3

3G_PLL

MiniCard

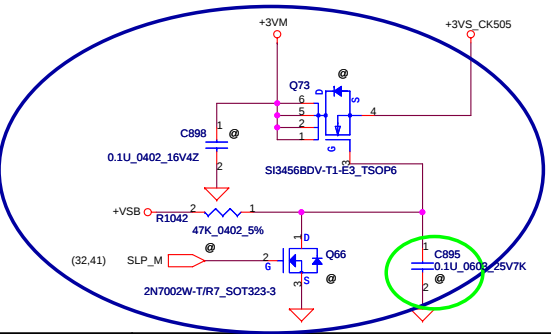
DOCKING

SATA

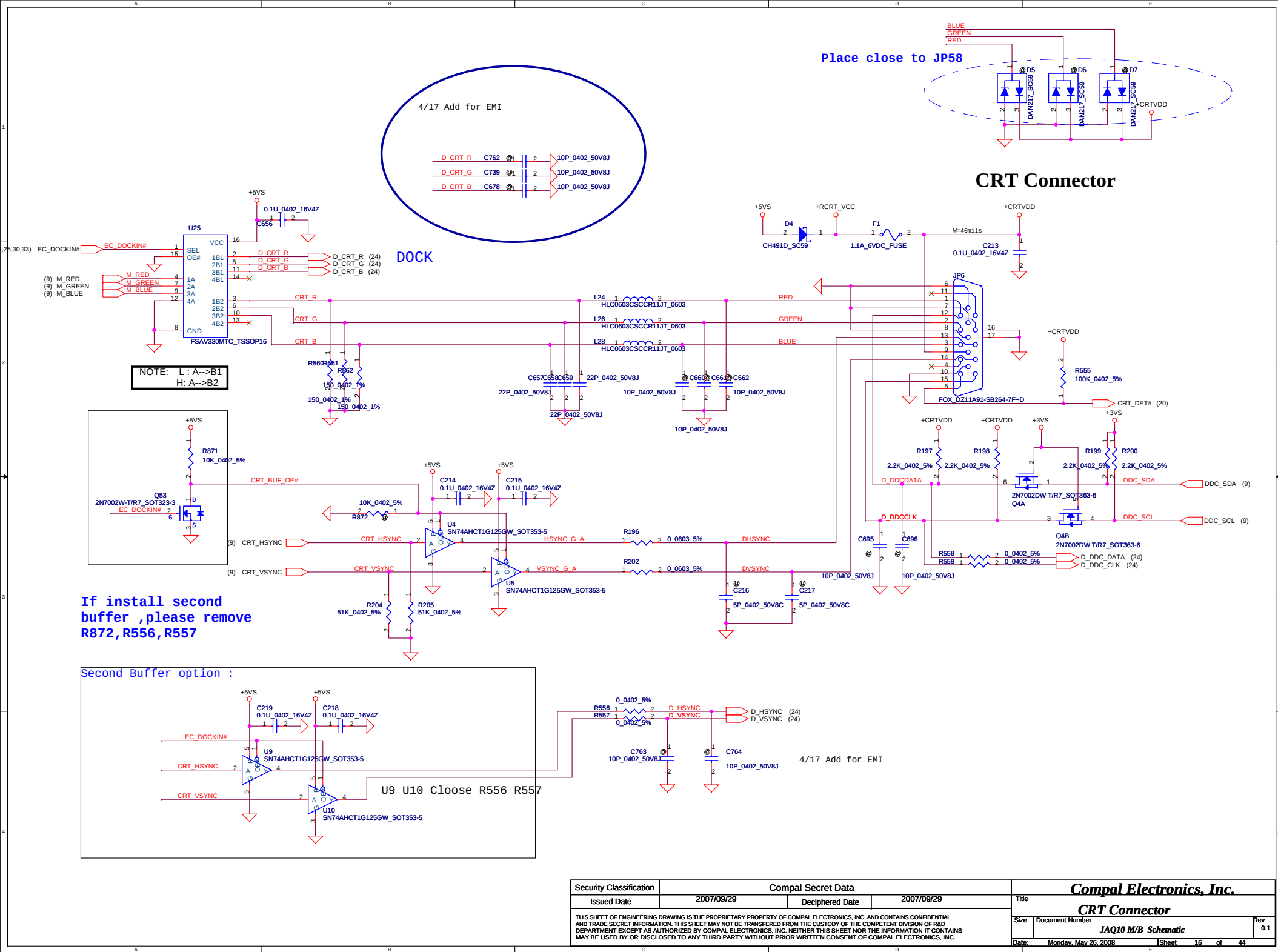
ICH

NB_SSC (UMA)

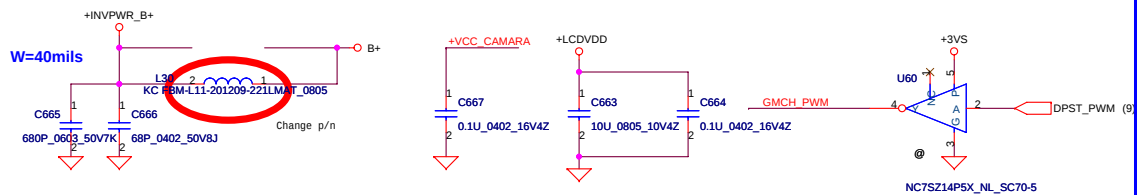
4/9 ADD MOS for CLK GEN



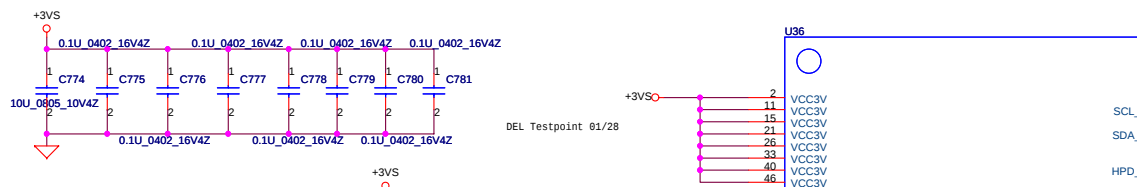
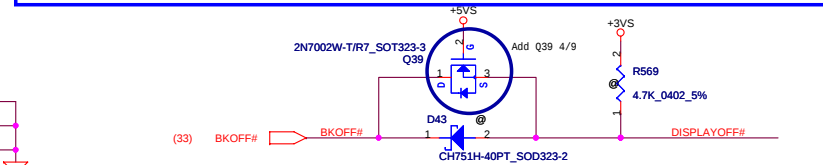
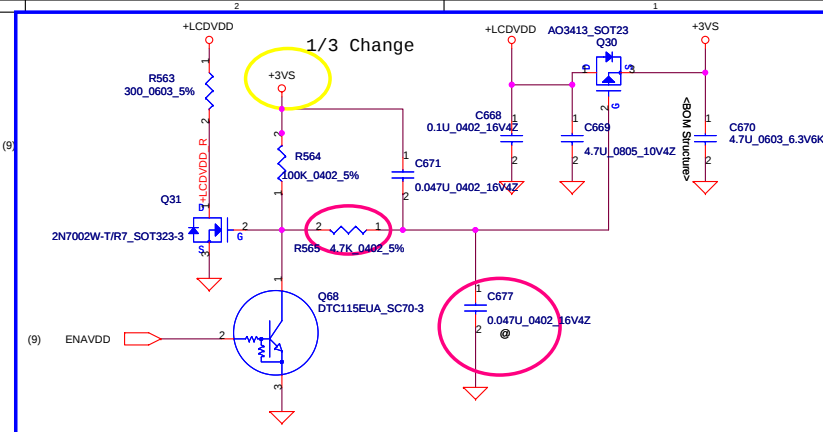
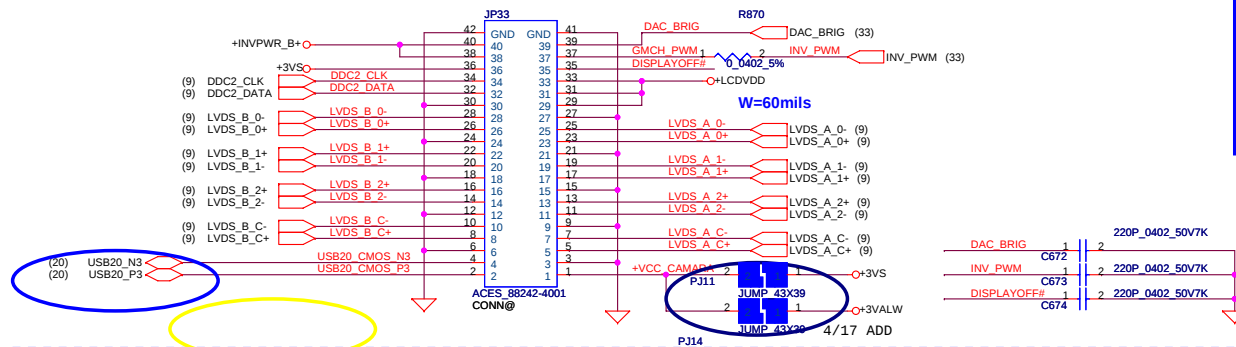
Compal Electronics, Inc.	
Clock Generator CK505	
Title	JAQ10 M/B Schematic
Size	Document Number
Date	Monday, June 23, 2008
Sheet	15 of 44
Rev	0.1



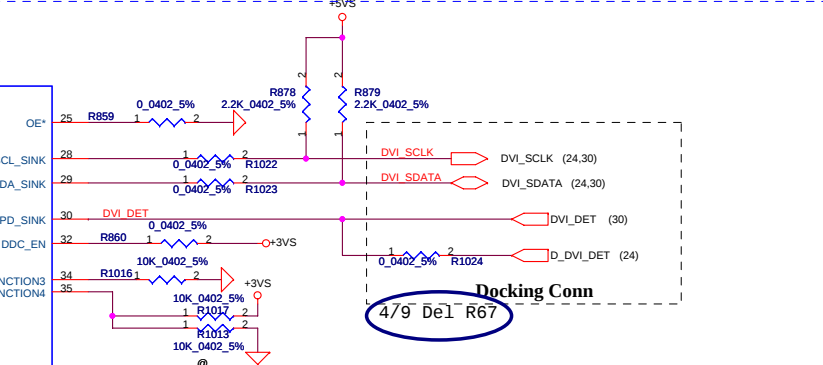
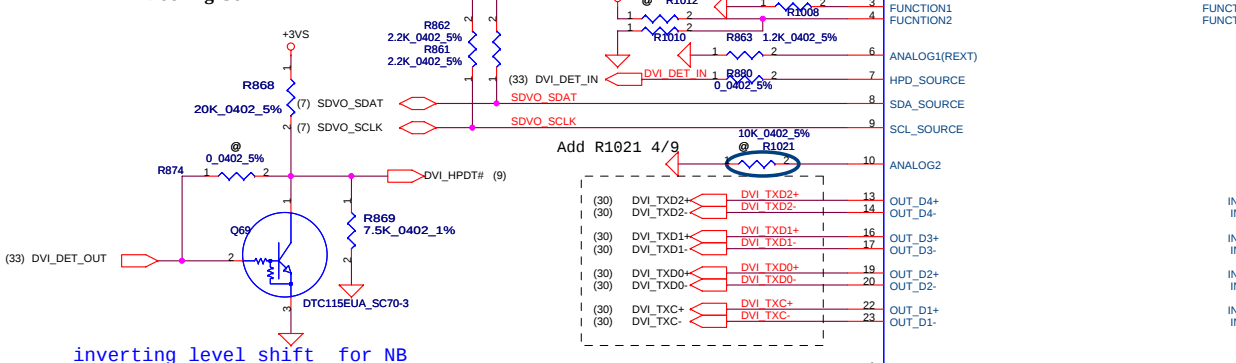
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2007/09/29	Deciphered Date	2007/09/29	CRT Connector			
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						JAQ10 M/B Schematic	0.1
				Date:		Monday, May 26, 2008	Sheet



LVDS and USB CAM connector



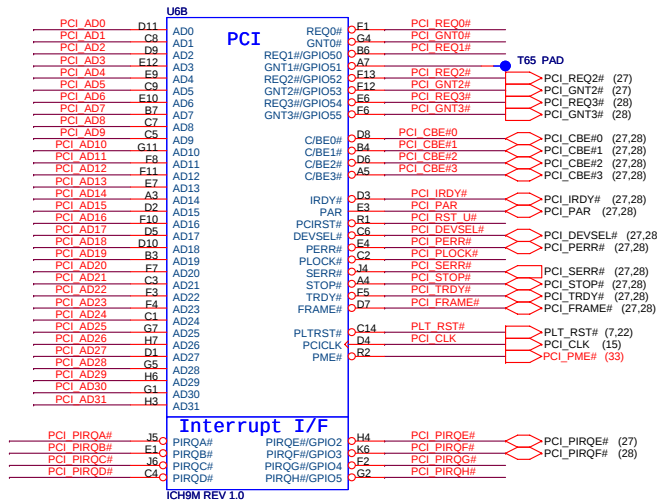
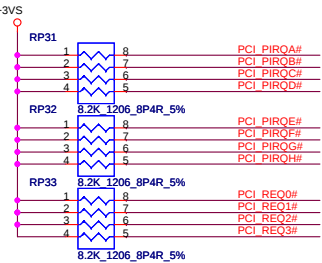
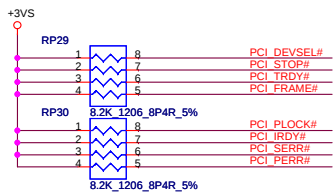
Docking Conn



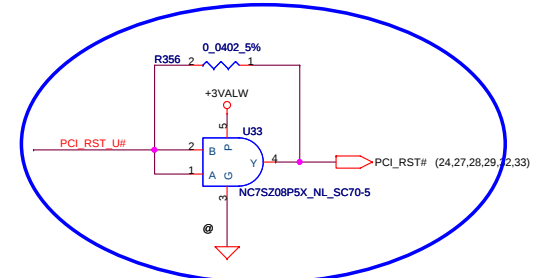
pin 4	0 = disable inverting output 1 = enable inverting output
pin 35	0 =Default value 1 = output driver current increased 10%

From GM

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Issued Date	2007/09/29	Deciphered Date	2007/09/29	LCD CONN & CH 7318	
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				JAQ10 M/B Schematic	
				Date:	Wednesday, June 11, 2008
				Sheet	17 of 44



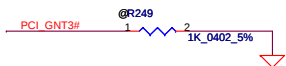
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(27,28) PCI_CBE#[0..3] < PCI_CBE#[0..3]



ADD Buffer for 4/9

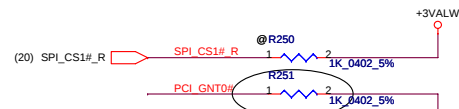
A16 swap override Strap

Low= A16 swap override Enble
High= Default *



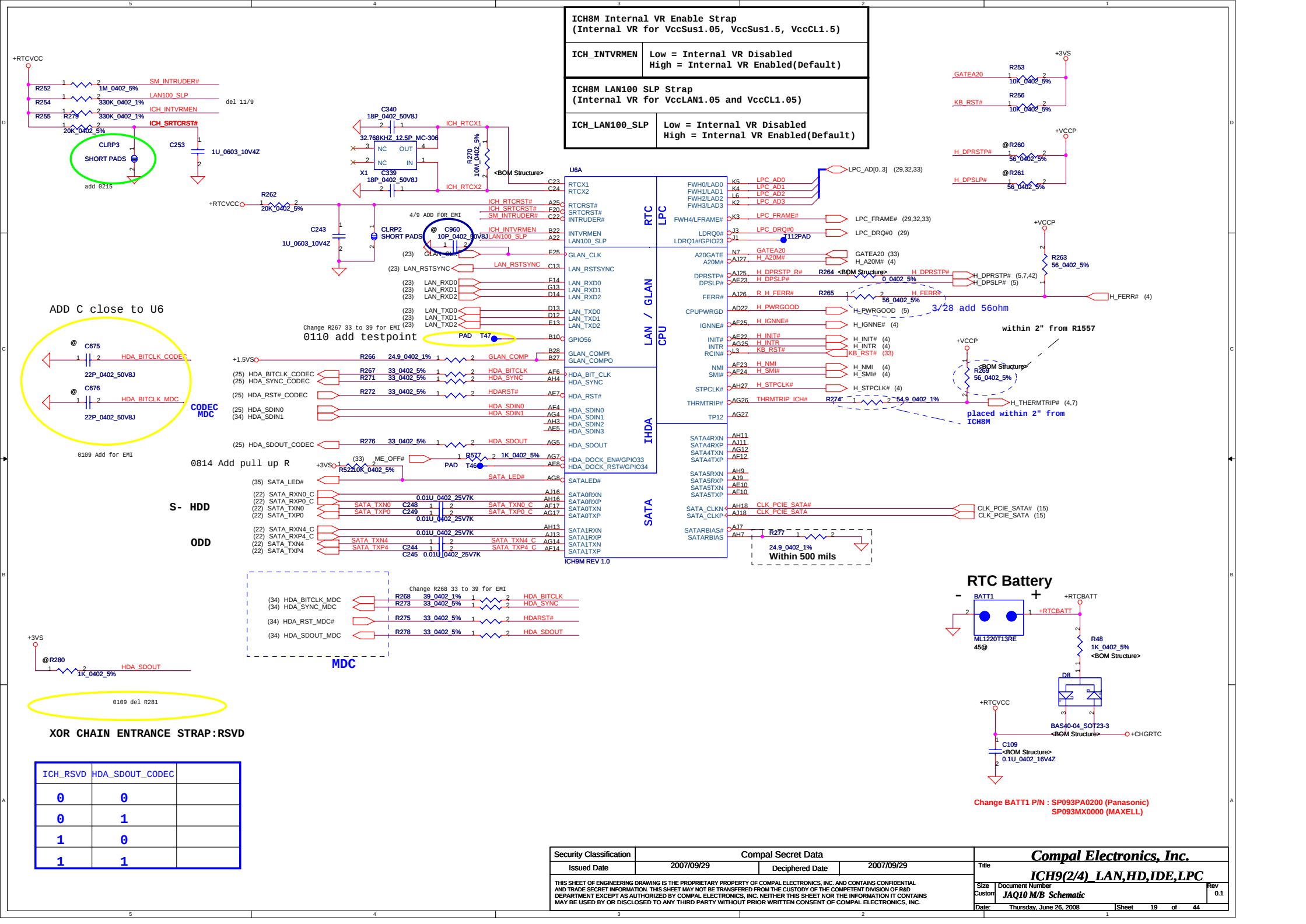
Boot BIOS Strap

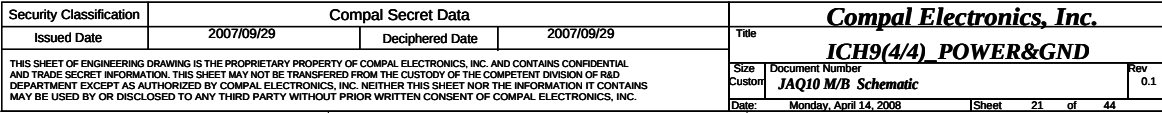
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1	0	PCI
1	1	LPC *



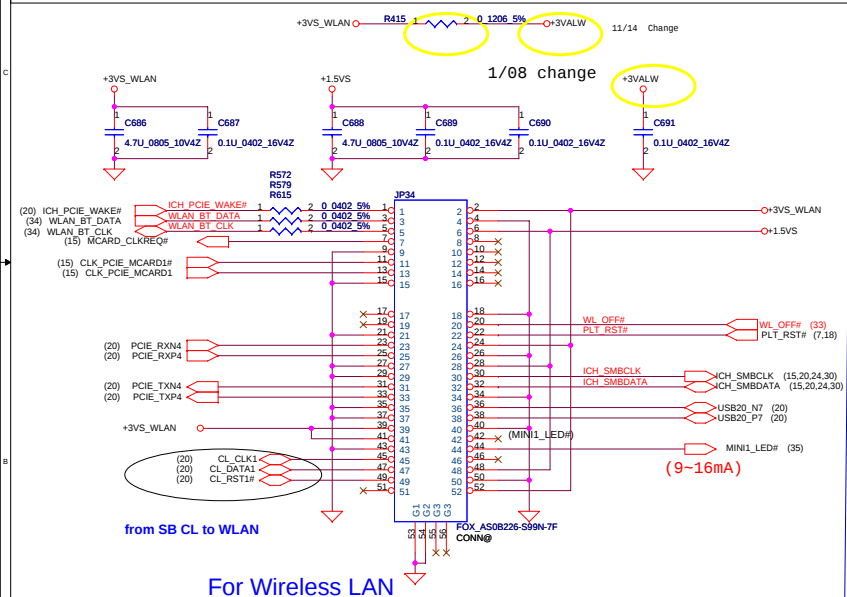
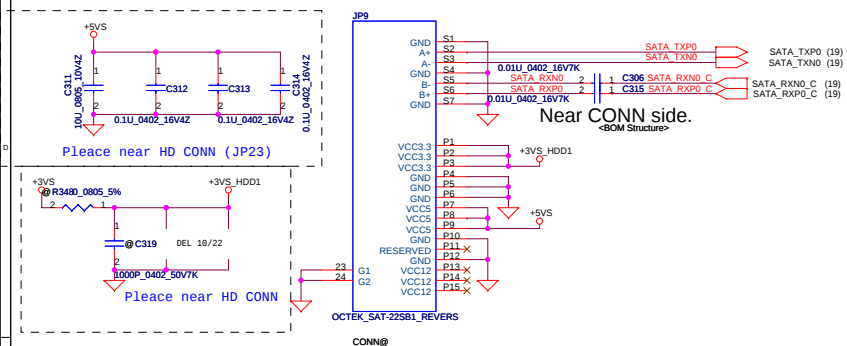
Change 11/15

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				Document Number		
				Rev		
Date: Monday, May 26, 2008				Sheet 18 of 44		

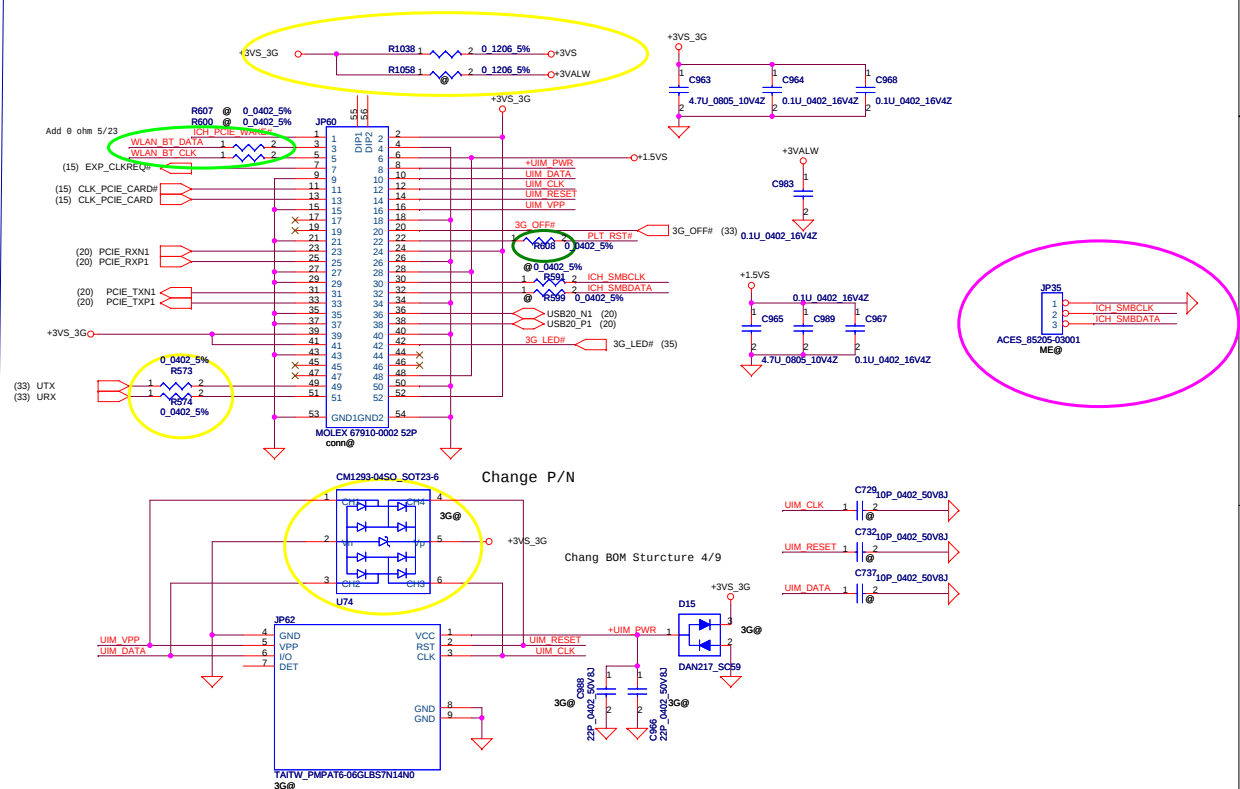
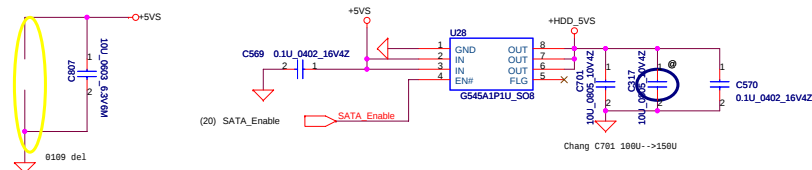
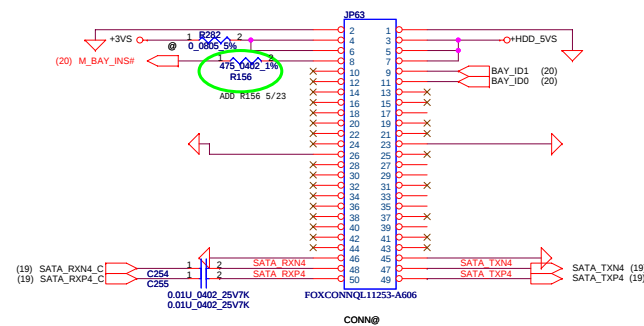




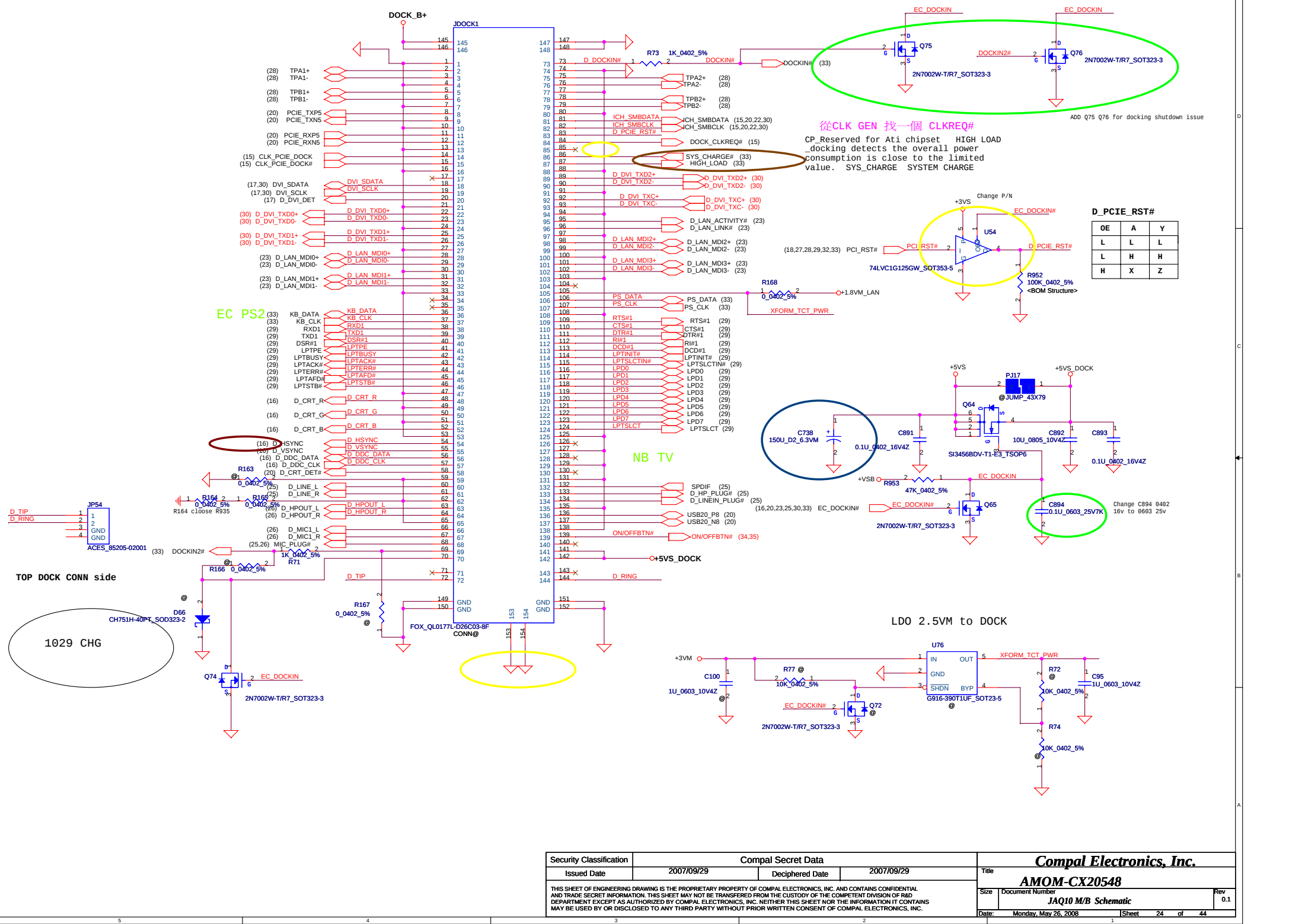
HDD Connector



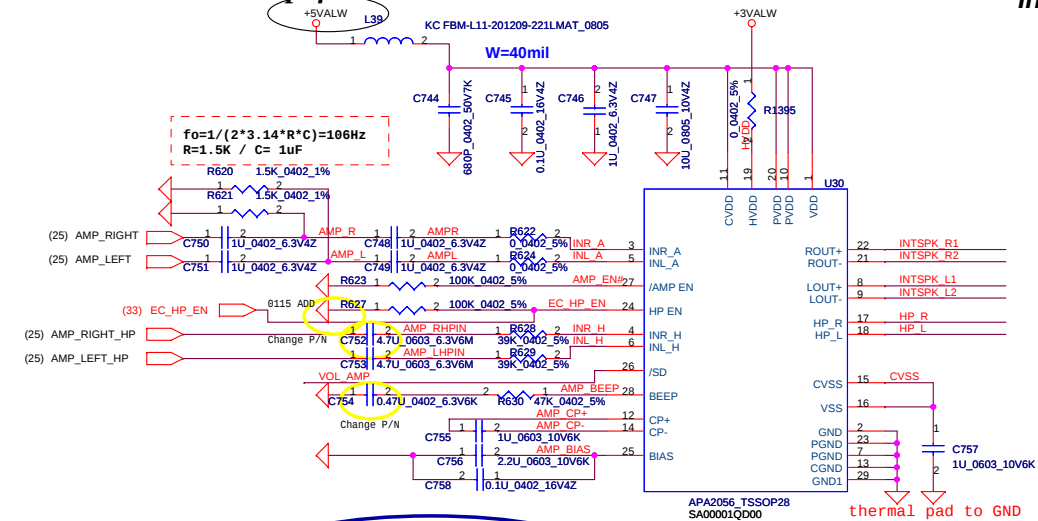
Media BAY for 2ND HDD BATT



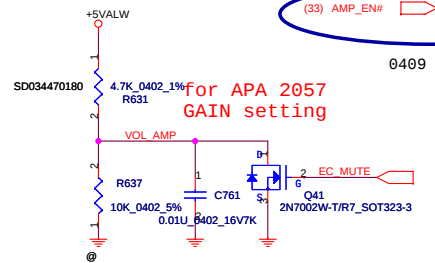
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Issued Date	2007/09/29	Deciphered Date	2007/09/29			
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				Size C	Document Number JAQ10 M/B Schematic	Rev 0.1
Date:				Friday, June 06, 2008	Sheet	22 of 44



APA2056 SPK/HP Amplifier



IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)

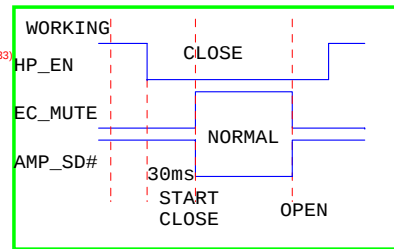


APA2057 gain setting table

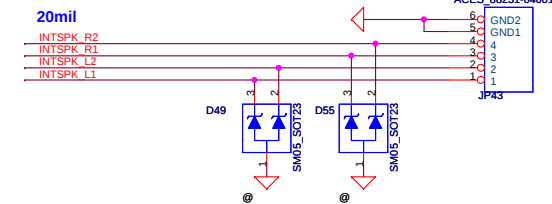
gain \ V	V(low)	V(high)
8	3.21	3.27
9	3.33	3.39
10	3.45	3.51

(dB)

```
current
setting(3.48V)
```

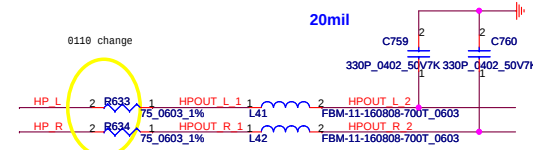


Int. Speaker Conn.

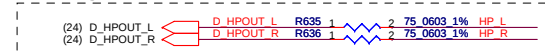


DEL SPDIF POWER 11/20

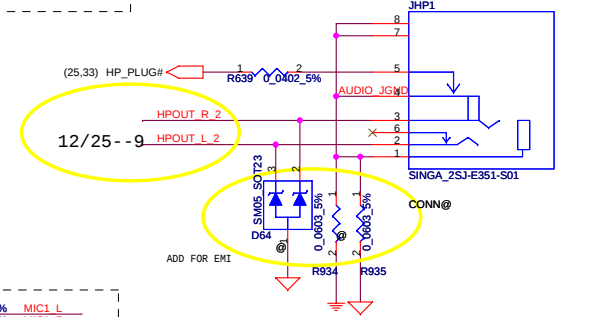
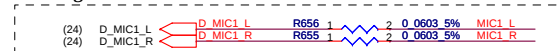
LINE Out/Headphone Out
S/PDIF Out JACK



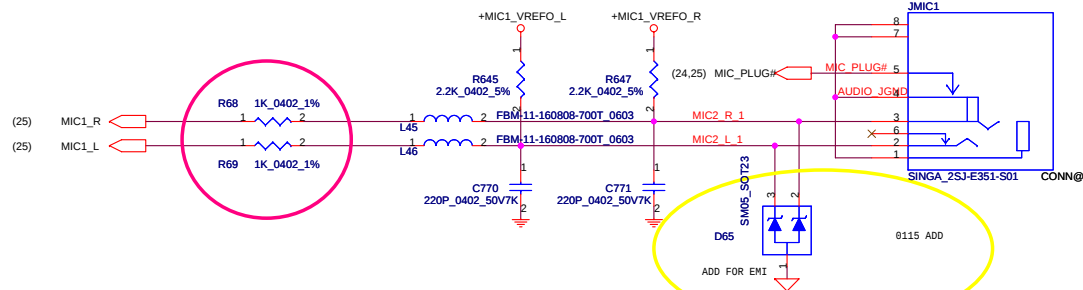
Docking Conn



Docking Conn

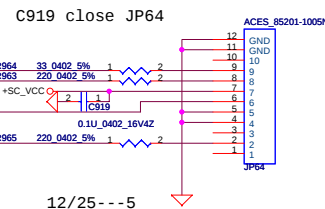
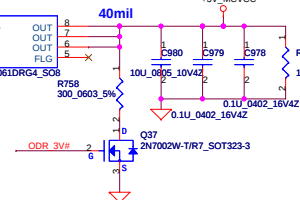
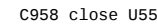
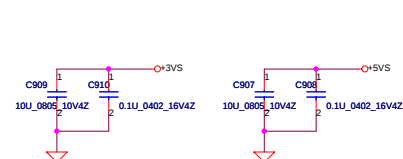


MIC JACK



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					JAQ10 M/B Schematic	0.1
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Change library U55/U56

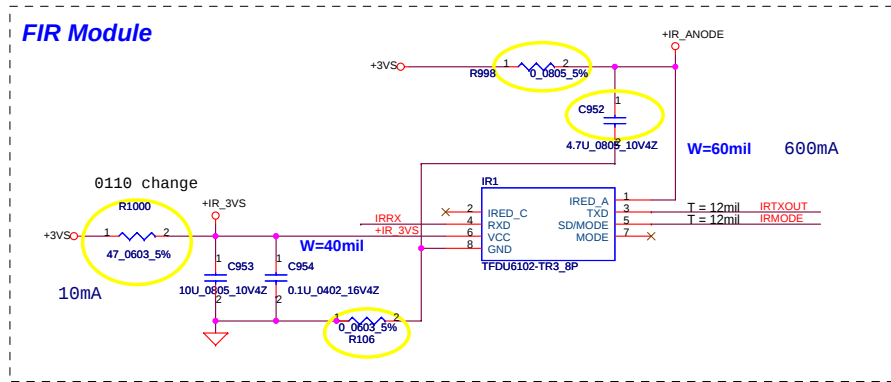
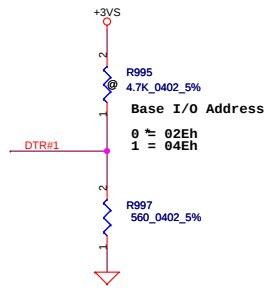
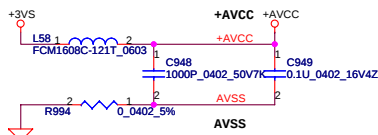
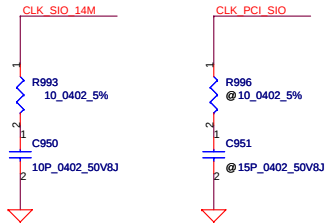
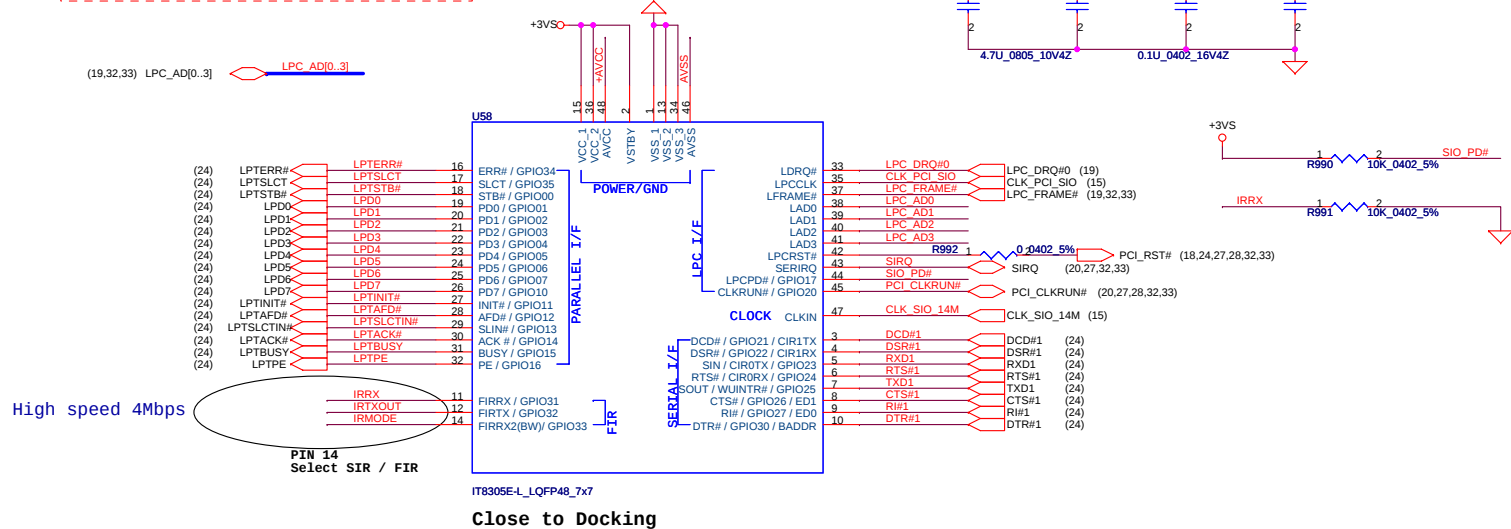


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				JAQ10 M/B Schematic	
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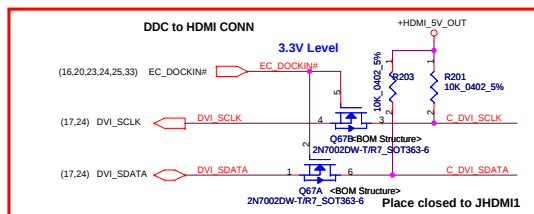
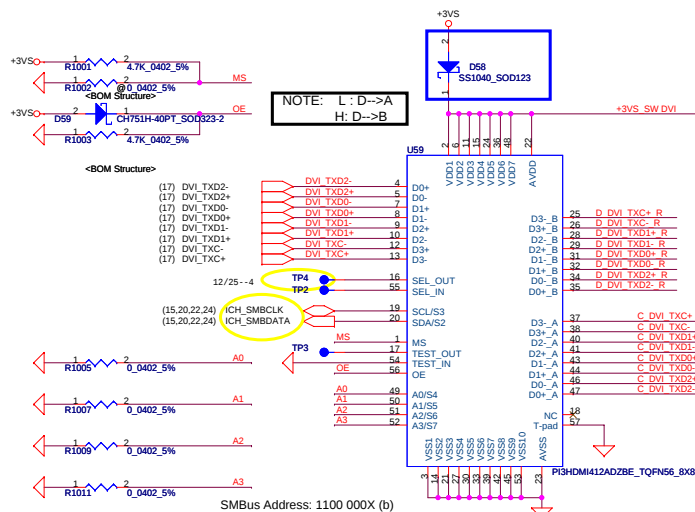
SUPER I/O ITE IT8305E

Note for pin 2:
If needs to support power on from IT8305 CIR, please connect pin2 for "VSTBY".
If don't need to support power on from IT8305 CIR, please connect pin2 for "V33".

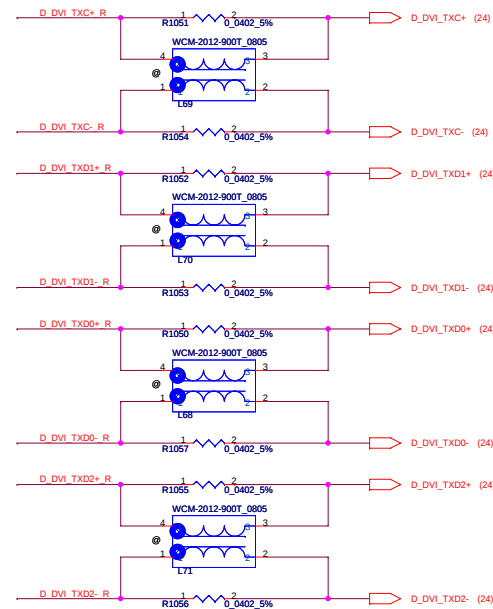
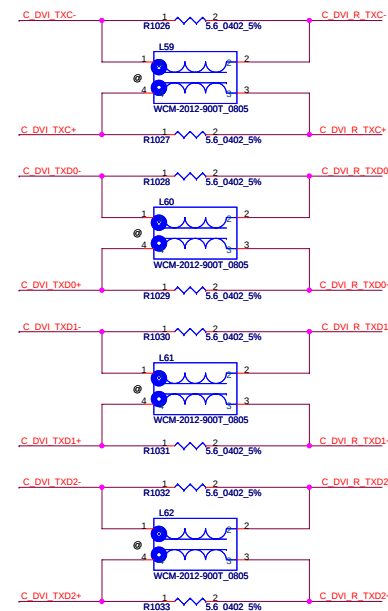
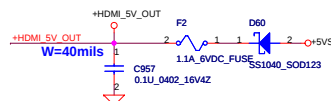
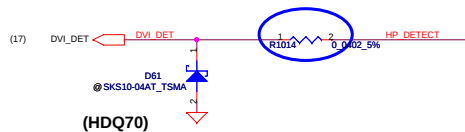
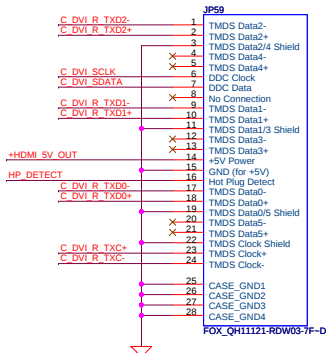
From External CLK for 14.318MHz(default) or 48MHz



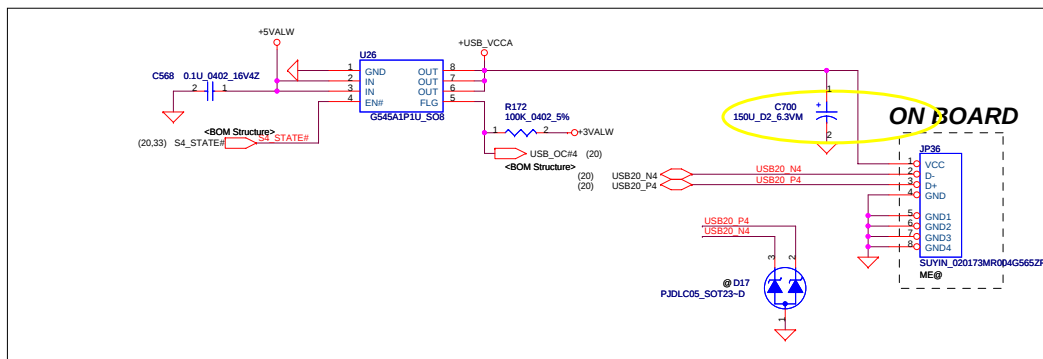
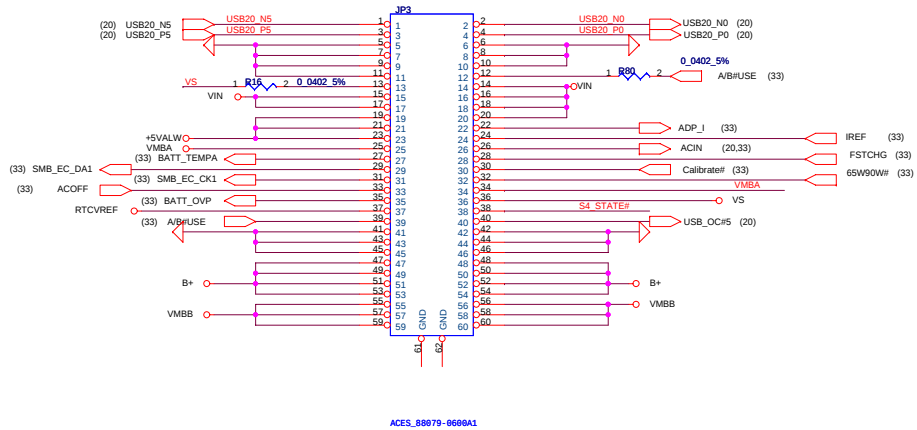
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				Size	Document Number
				Custort	JAQ10 M/B Schematic
Date: Wednesday, June 11, 2008				Rev	0.1
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DVI-D Connector

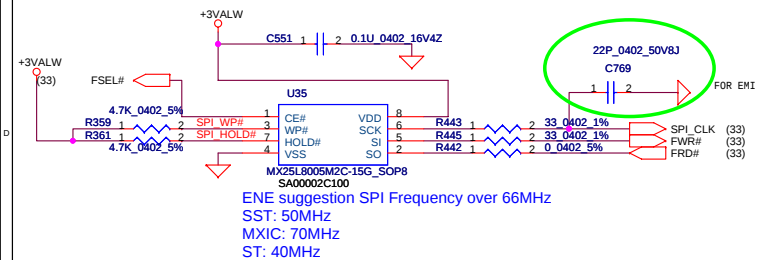


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					Size	
					Document Number	
					Rev	
					JAQ10 M/B Schematic	
Date					Monday, June 23, 2008	
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				Document Number	
				JAQ10 M/B Schematic	
				Rev	
				0.1	
				Date	
				Friday, June 06, 2008	
				Sheet	
				31 of 44	

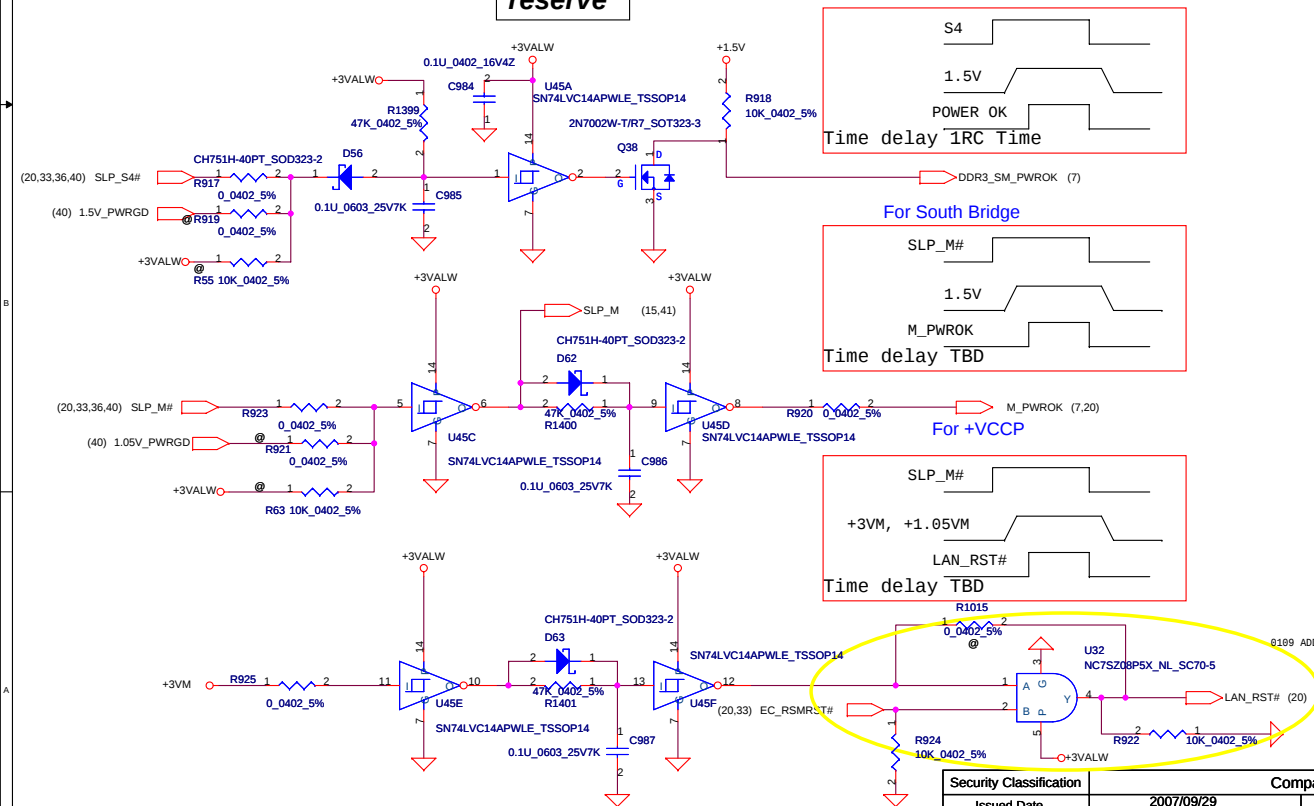
BIOS



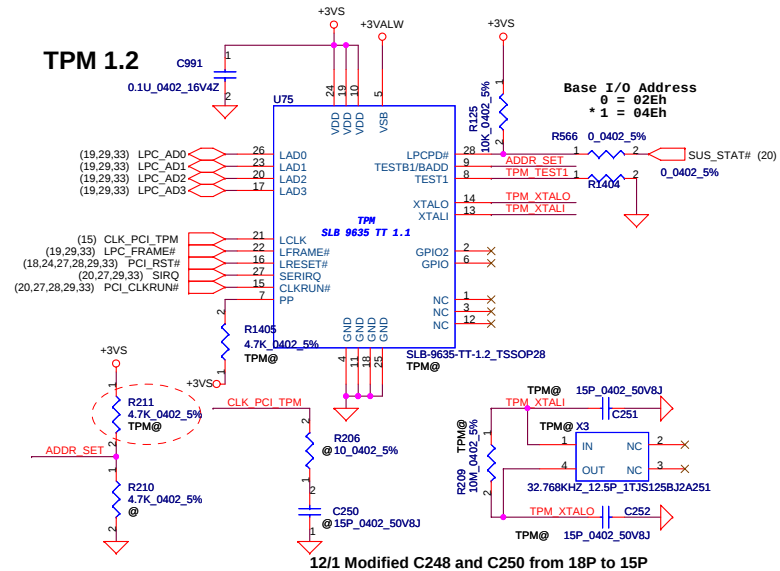
0115 DEL

Power ON Circuit

reserve



TPM 1.2



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Issued Date				2007/09/29				BIOS ROM			
Deciphered Date				2007/09/29				JAQ10 M/B Schematic			
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Date: Wednesday, June 11, 2008				Sheet 32 of 44							

Power Button

TOP Side

Bottom Side

ON/OFF switch

(24,35) ON/OFFBTN#

ON/OFFBTN#

R578

10K_0603_5%

+3VALW

R580

100K_0402_5%

D44

DAN202UT106_SC70-3

510N#

ON/OFF (33)

510N# (37)

C704

1000P_0402_50V7K

D45

RLZ20A_LL34

Q36

2N7002W-T/R7_SOT323-3

EC_ON

(33)

R501

10K_0402_5%

0409 change

+3VALW0

4.7u 0603 6.3V6M C707

0.1u 0402 10V6K C708

For EMI

D30 PSOT24C-LF-T7_SOT23-3

ACES_85201-0405N

(20) USB20_N6 USB20 N6

(20) USB20_P6 USB20 P6

JP44

G2

G1

4

3

2

1

[illegible]

The image shows two PCB layout sections. The top section is for the HDA MDC Conn. and the bottom section is for the BT connector.

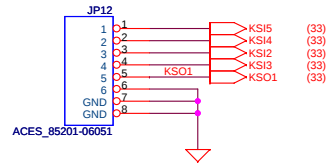
HDA MDC Conn.: This section shows a connector JP39 (12 pins) connected to various components. Pin 1 is connected to HDA_SDOUT_MDC. Pin 2 is connected to HDA_SYNC_MDC. Pin 3 is connected to HDA_SDIN1. Pin 4 is connected to HDA_RST_MDC#. Pin 5 is connected to HDA_BITCLK_MDC. Pin 6 is connected to HDA_SYNC_MDC. Pin 7 is connected to HDA_SYNC_MDC. Pin 8 is connected to HDA_SYNC_MDC. Pin 9 is connected to HDA_SYNC_MDC. Pin 10 is connected to HDA_SYNC_MDC. Pin 11 is connected to HDA_SYNC_MDC. Pin 12 is connected to HDA_SYNC_MDC. The components include a 20mil trace, a 33.0402 5% resistor (R583), a 0.0402 5% resistor (R582), a 10.0402 5% resistor (R584), a 22P_0402_50V8J capacitor (C706), and a 1u_0603_10V4Z capacitor (C705). The components are labeled with their values and tolerances. The components are labeled with their values and tolerances. The components are labeled with their values and tolerances.

BT: This section shows a connector JP37 (10 pins) connected to various components. Pin 1 is connected to USB20_P2. Pin 2 is connected to USB20_N2. Pin 3 is connected to WLAN_BT_DATA. Pin 4 is connected to WLAN_BT_CLK. Pin 5 is connected to WLAN_BT_DATA. Pin 6 is connected to WLAN_BT_CLK. Pin 7 is connected to WLAN_BT_DATA. Pin 8 is connected to WLAN_BT_CLK. Pin 9 is connected to WLAN_BT_DATA. Pin 10 is connected to WLAN_BT_CLK. The components include a PSOT24C-LF-T7_SOT23-3 component (D31), a 22P_0402_50V8J capacitor (C706), and a 1u_0603_10V4Z capacitor (C705). The components are labeled with their values and tolerances. The components are labeled with their values and tolerances. The components are labeled with their values and tolerances.

BT module power and control circuit schematic. The circuit includes a +3V3 supply connected to a network of resistors (R135, R136) and capacitors (C698, C699, C702, C703). A BT_ON# signal is connected to a network of resistors (R575, R576) and capacitors (C698, C699). A BT_LED# signal is connected to a network of resistors (R576) and capacitors (C702, C703). A BT_EC signal is connected to a network of resistors (R576) and capacitors (C702, C703). The circuit includes two MOSFETs, Q33 and Q34, which are used to switch the BT module's power and ground. The BT module is represented by a large oval labeled 'BT'.

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					JAQ10 M/B Schematic	0.1
				Date:	Wednesday, June 11, 2008	Sheet 34 of 44

TO S/W B

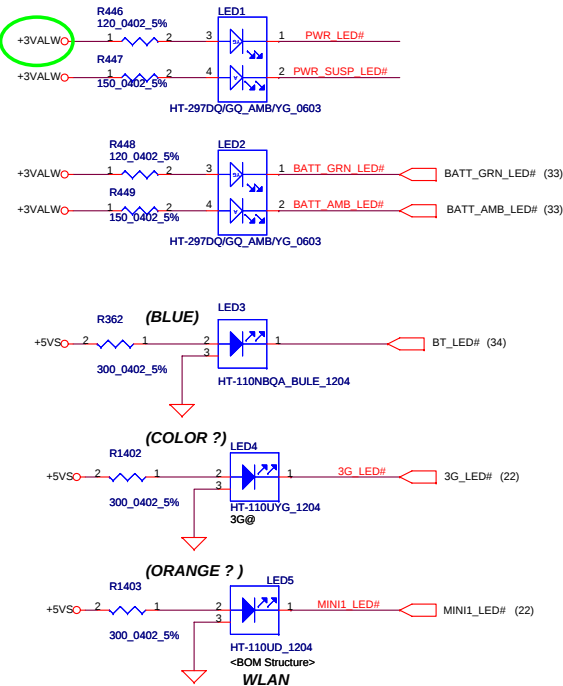


	KSO1	KSO2
KSI2	SYNC_BTN#	EMAIL_BTN#
KSI3	BRIEF_BTN#	PROGRAM_BTN#
KSI4	LOCK_BTN#	IE_BTN#
KSI5	E-KEY_BTN#	
KSI6		3G ON#
KSI7	WL ON#	BT ON#

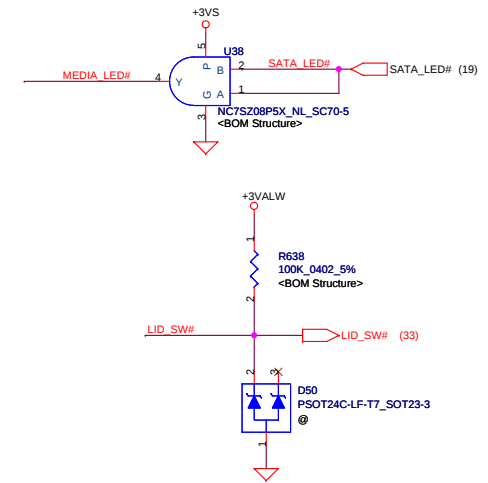
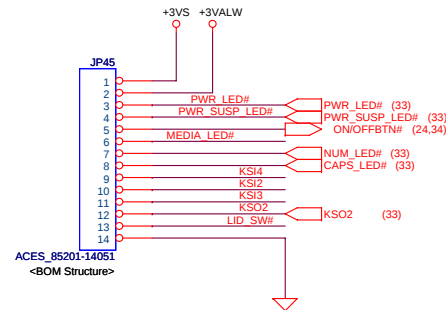
0103 Change1

Change +3vs to +3valw

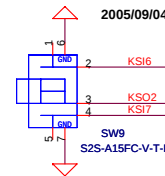
Compal Footprint



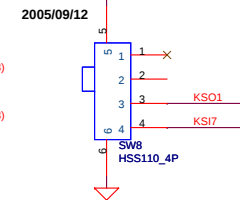
TO POWER BTN/B



BT_SW & 3G_SW



WL_SW

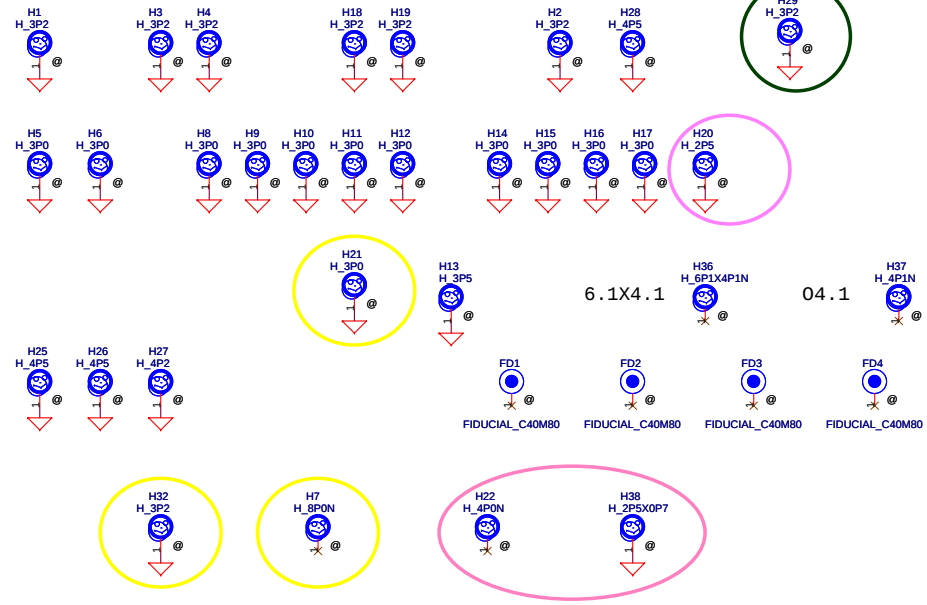


06 03.2

9 X 9 03

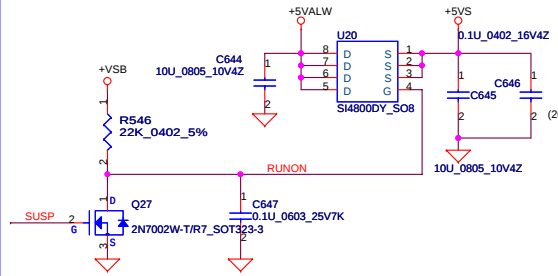
04.2

02.5

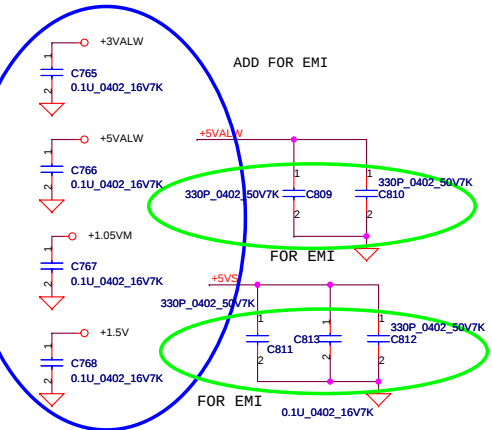
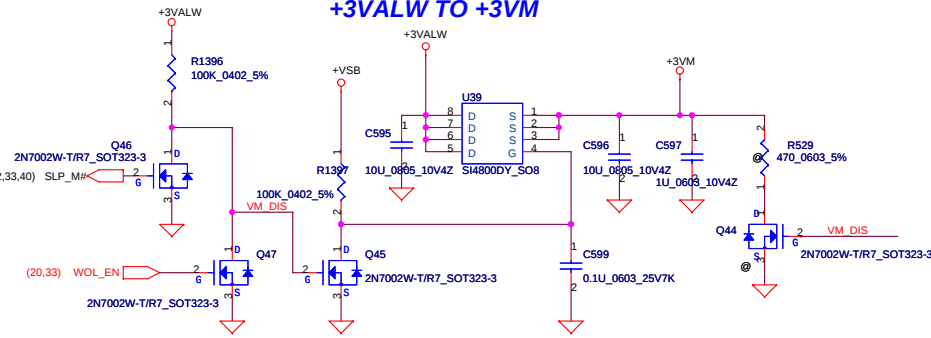


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Issued Date	2007/09/29	Deciphered Date	2007/09/29	Title	LED/SW
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				JAQ10 M/B Schematic	
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				Rev	0.1

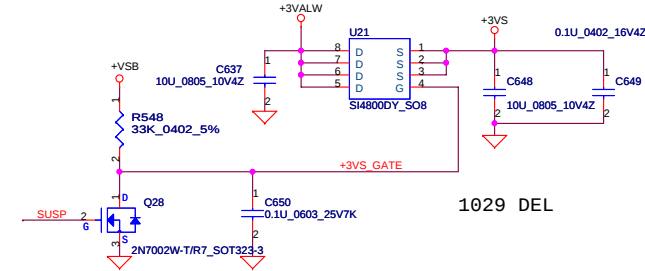
+5VALW to +5VS Transfer



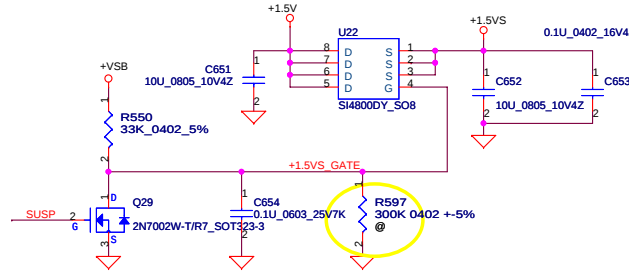
+3VALW TO +3VM



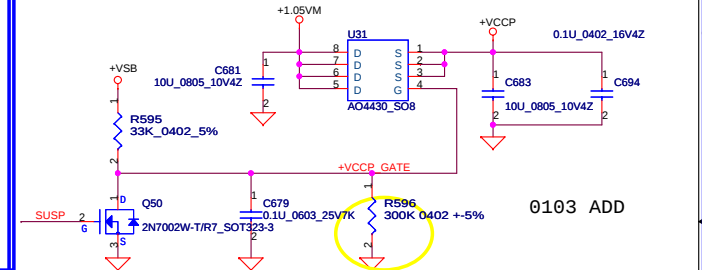
+3VALW to +3VS Transfer



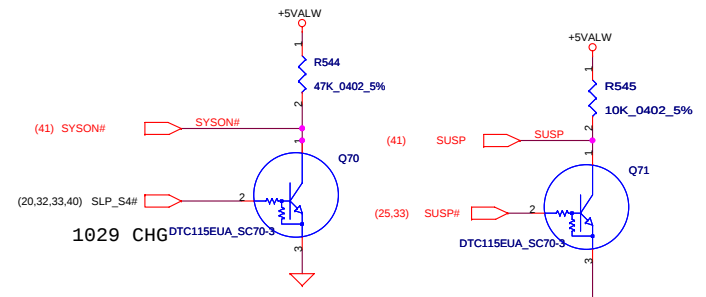
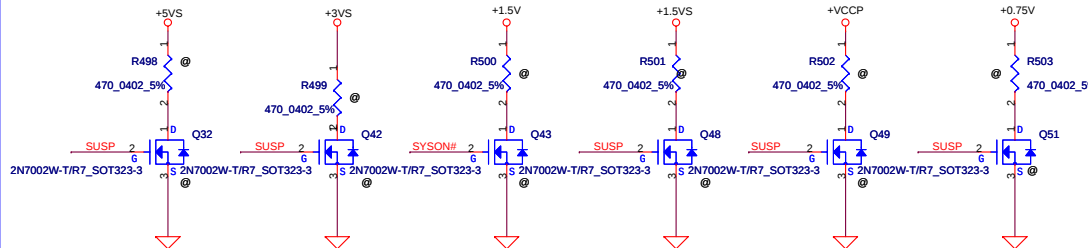
+1.5V to +1.5VS Transfer



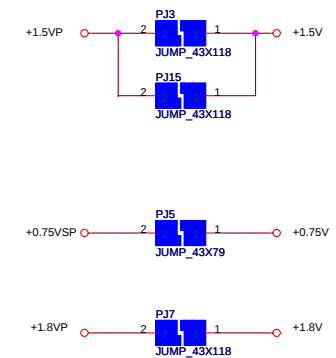
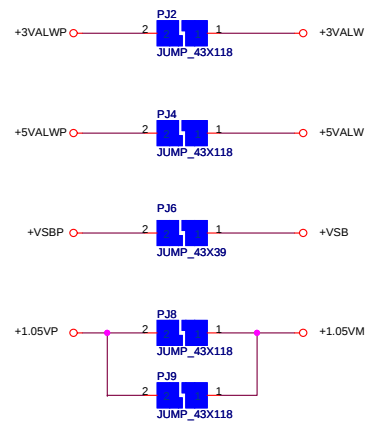
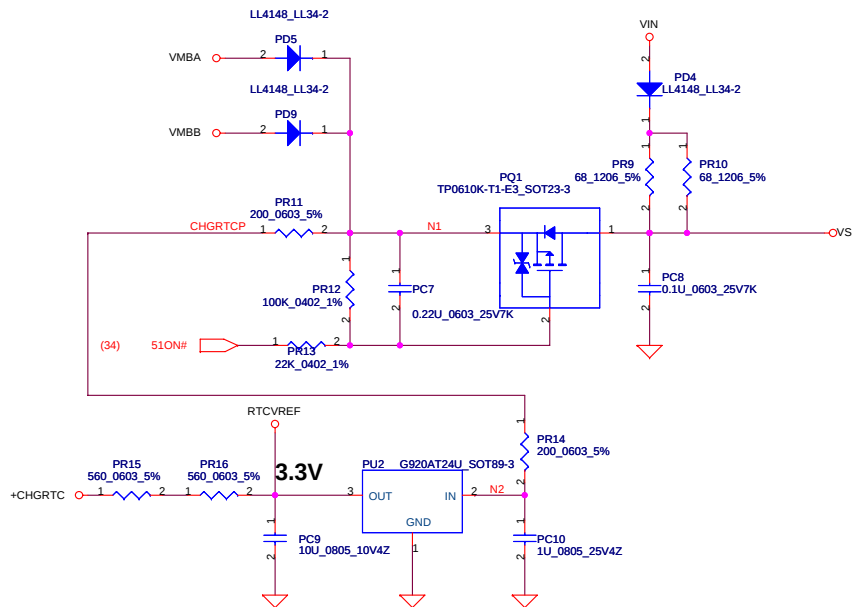
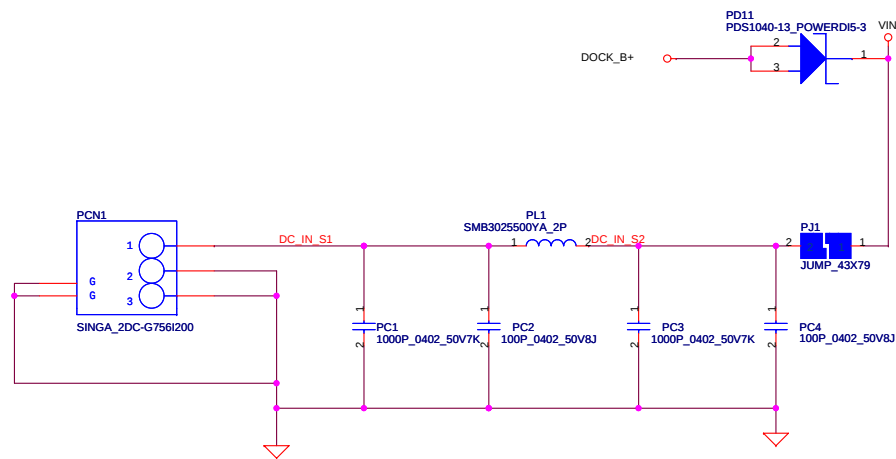
need power confirm +1.05VM to +VCCP Transfer



Discharge circuit

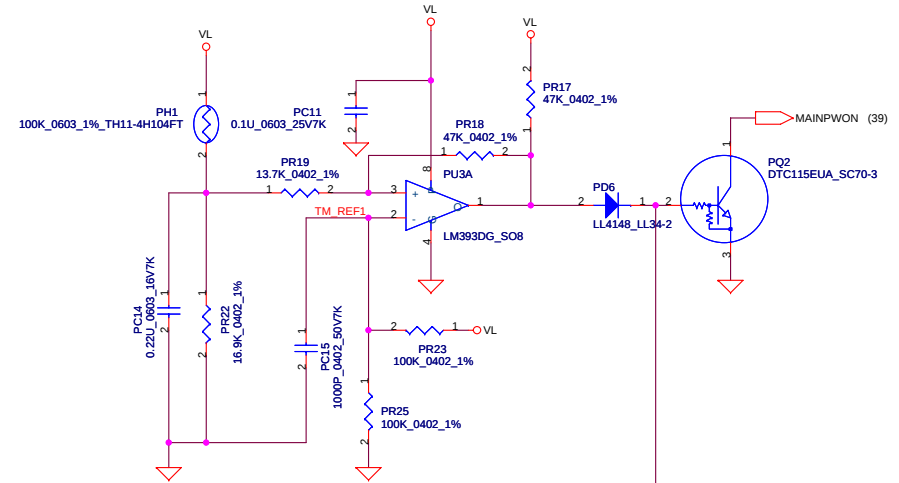
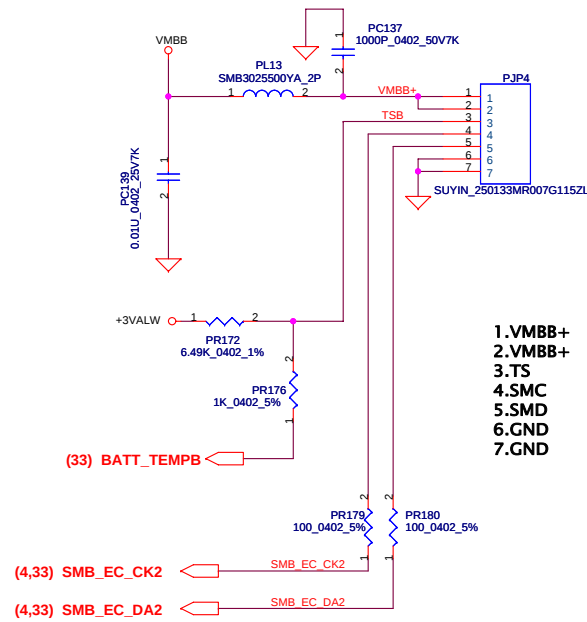


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Issued Date	2007/09/29	Deciphered Date	2007/09/29	DC/DC Interface	
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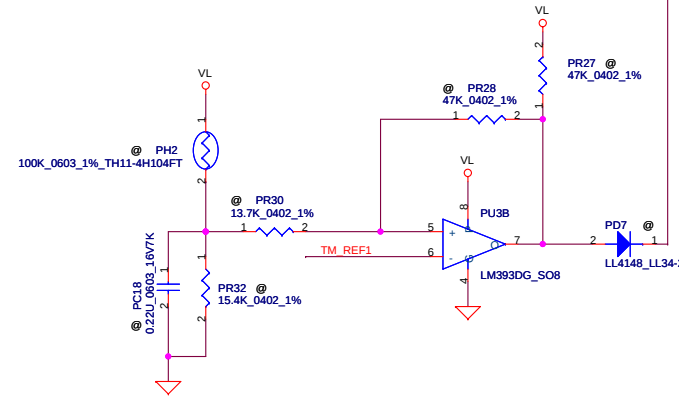
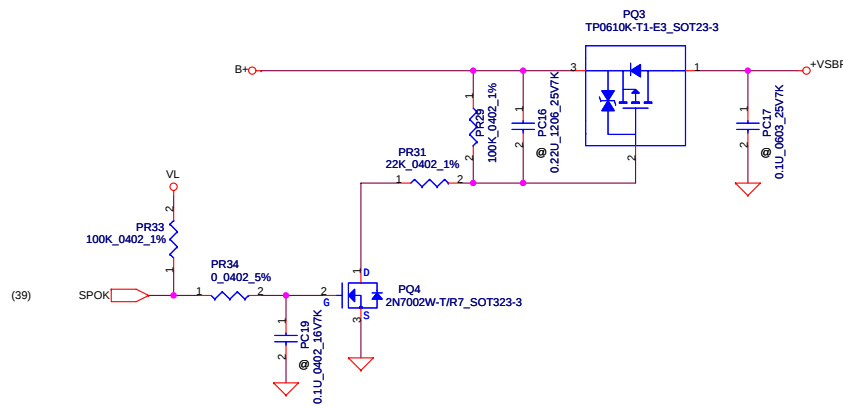


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					JAQ10	0.2
				Date:	Friday, June 06, 2008	Sheet 37 of 45

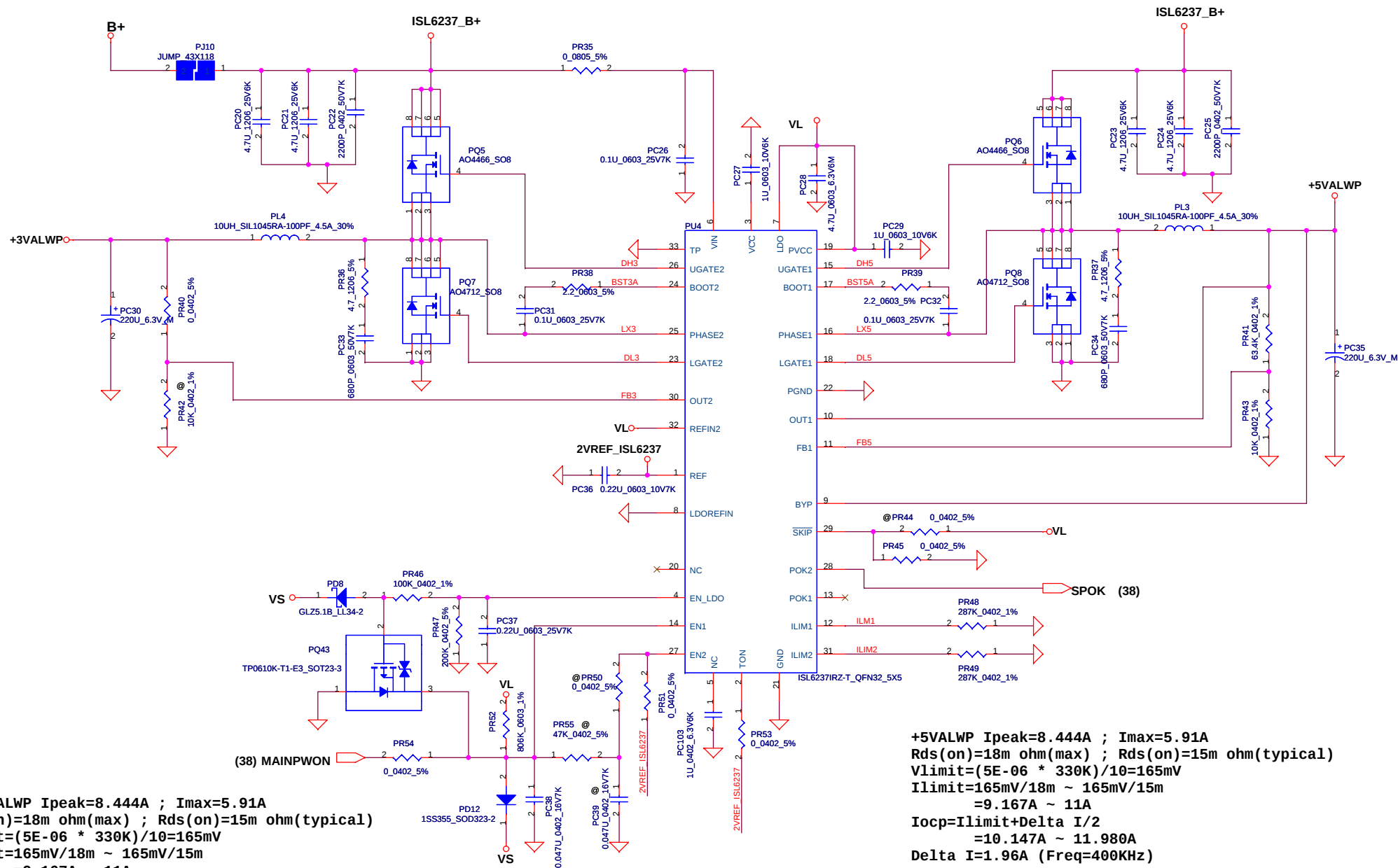
PH1 under CPU botten side :
CPU thermal protection at 86 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C



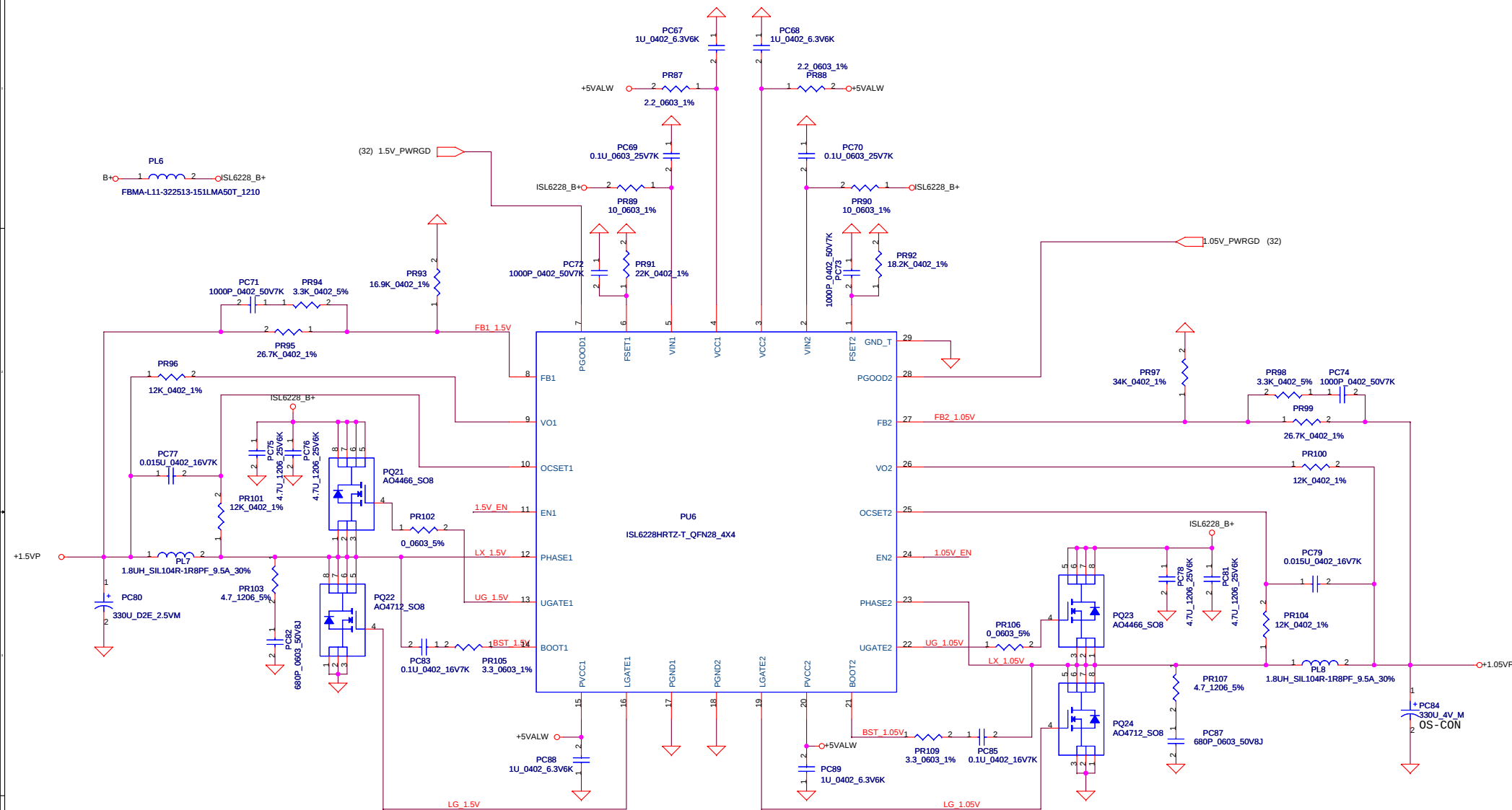
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/09/29	Deciphered Date	2007/09/29	Title	
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+3.3VALWP Ipeak=8.444A ; Imax=5.91A
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.134A ~ 11.967A
 Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.147A ~ 11.980A
 Delta I=1.96A (Freq=400KHz)

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Size		Document Number		Rev	
Custom		JAQ10		0.2	
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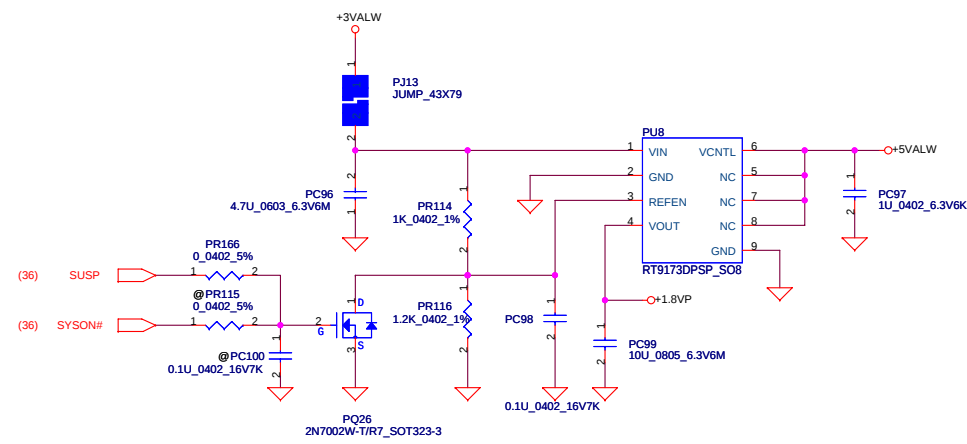
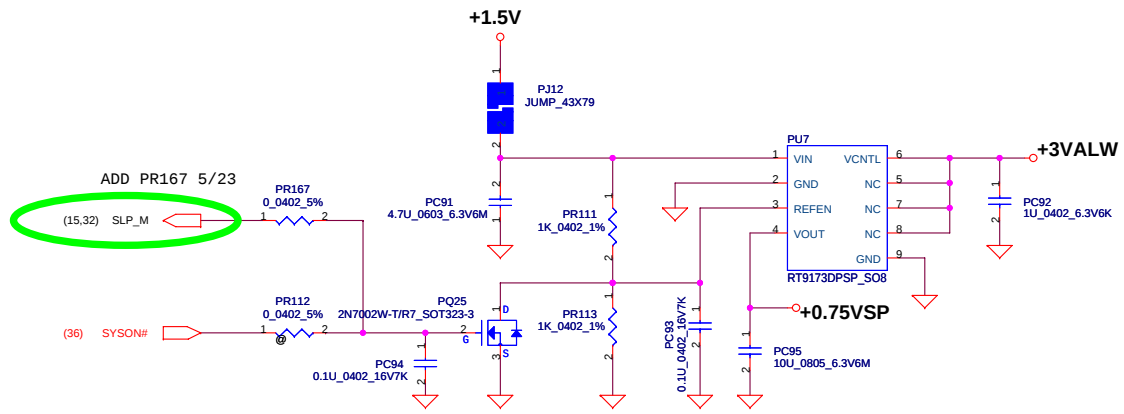
1.5VP Ipeak=9.45A ; Imax=6.615A
 DCR=10m ohm (max)
 $R_{ocset} = (I_{ocp} * DCR) / 10E-06 = 12K \text{ ohm}$
 $I_{ocp} = 12A$
 $C_{sen} = L / (R_{ocset} * DCR) = 0.015uF$

Freq=303KHz
 $R_{fset} = 1 / (1.5E-10 * Freq) = 22K$

1.05VP Ipeak=8.8A ; Imax=6.16A
 DCR=10m ohm (max)
 $R_{ocset} = (I_{ocp} * DCR) / 10E-06 = 12K \text{ ohm}$
 $I_{ocp} = 12A$
 $C_{sen} = L / (R_{ocset} * DCR) = 0.015uF$

Freq=366KHz
 $R_{fset} = 1 / (1.5E-10 * Freq) = 18.2K$

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				Rev	0.2
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For 2nd source of ISL6237		39	Add PC103 SE000000K80(S CER CAP 1U 6.3V K X5R 0402) on Pin5 of PU4 to GND	2007 12/26	EVT
2		For EN function of PU4		39	Add PD12 SC100001K00(S DIO 1SS355 SOD323 T/R-5K)on pin 3 of PQ43 to VS	2007 12/26	EVT
3		Down size		39	Change PC38 from 0603 to 0402(SE076473K80)	2007 12/26	EVT
4		Down size		39	Change PC28 from 0805 to 0603(SE107475M80)	2007 12/26	EVT
5		Down size		37	Change PC7 from 1206 to 0603(SE000005Z80)	2007 12/26	EVT
6		For more current		37	Change PD11 in SCS00002F00(S SCH DIO PDS1040-13 POWERDI5)	2007 12/26	EVT
7		For more current		37	Change PD1 in SCS00002F00(S SCH DIO PDS1040-13 POWERDI5)	2007 12/26	EVT
8		Down size		41	Change PC91 from 0805 to 0603(SE107475M80)	2007 12/26	EVT
9		Down size		41	Change PC96 from 0805 to 0603(SE107475M80)	2007 12/26	EVT
10		Down size		41	Change PC92 from 0603 to 0402(SE000000K80)	2007 12/26	EVT
11		Down size		41	Change PC97 from 0603 to 0402(SE000000K80)	2007 12/26	EVT
12		Down size		42	Change PC110 from 0603 to 0402(SE000000K80)	2007 12/26	EVT
13		Down size		42	Change PC112 from 0603 to 0402(SE074681K80)	2007 12/26	EVT
14		Down size		42	Change PC121 from 0603 to 0402(SE074681K80)	2007 12/26	EVT
15		Down size		42	Change PC128 from 0603 to 0402(SE000003W00)	2007 12/26	EVT
16		Down size		38	Change PC14 from 0805 to 0603(SE026224K80)	2007 12/26	EVT
17		Down size		38	Change PC18 from 0805 to 0603(SE026224K80)	2007 12/26	EVT
18		Sourcer request		40	Change PC71、PC74 from NP0 to X7R (SE074102K80)	2008 01/14	EVT
19		DFX		37	Delete PD1	2008 01/14	EVT
20		OCP adjust		39	Change PL3、PL4 from 4.7uH to 10uH (SH000002L80)	2008 01/14	EVT
21		OCP adjust		39	Change PR48、PR49 from 330K to 287K (SD000005D80)	2008 01/14	EVT
22	HW request	Set 1.5V==>1.54V, 1.05V==>1.07V		40	Change PR95、PR99 from 25.5K to 26.7K (SD034267280)	2008 01/14	EVT
23	HW request	Set 5V==>5.138V		39	Change PR41 from 61.9K to 63.4K (SD03463K280)	2008 04/17	DVT

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Title			
PIR (PWR)			
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Thermal request	Change protect point from 92 to 86 degree C		38	Change PR22 from 15.4K to 16.9K (SD034169280)	2008 04/17	DVT
25		3G EMI request			Delete PR36、PR37、PR103、PR107、PC33、PC34、PC82、PC87 "@" mark	2008 04/22	DVT
26					Change PR105、PR109、PR130、PR144 from 0 to 2.2		
27		3G EMI request		40	Change PR105、PR109 from 2.2 to 3.3	2008 05/21	PVT
28	EPA power	HW request		41	Add PR167, mark "@" PR112	2008 05/27	PVT
29		EMI request		37	Delete PJ4, add PL12 (SM010020720)	2008 05/27	PVT
30		3G EMI request		39	Change PR38、PR39 from 0 to 2.2	2008 05/29	PVT
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PIR (PWR)			
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