Compal Confidential

Model Name : P3MJ0
File Name : LA-7121P
BOM P/N:43XXXXXXL01(UMA)
43XXXXXXL02(DIS)

Compal Confidential

M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
Nvidia N12P-GS/GV

2010-11-16

REV:0.2

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/12/31

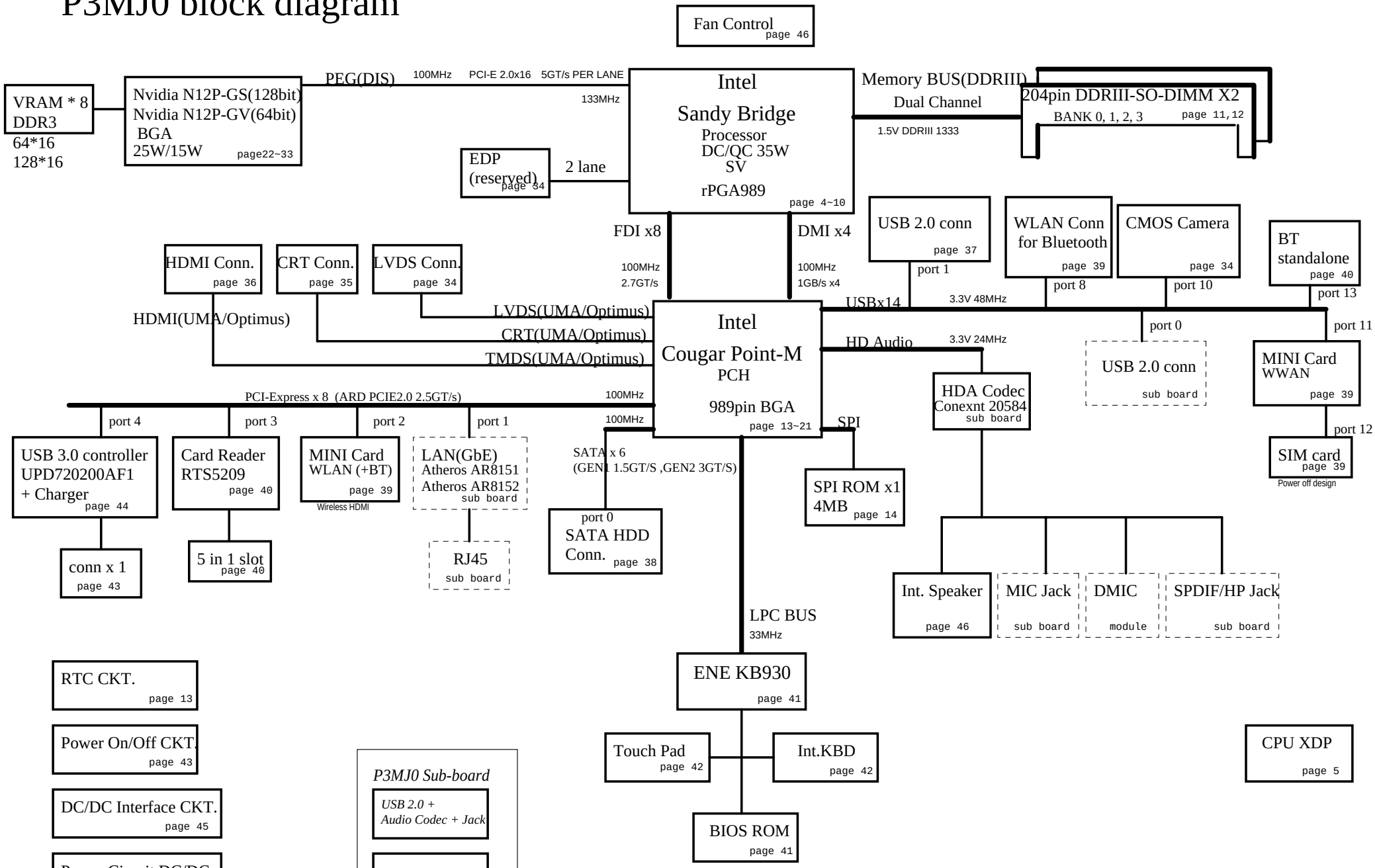
Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 1 of 57

P3MJ0 block diagram



Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 2 of 57

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

3G & BT Config
3G SKU: 3G@
BT SKU: BT@

BOM Config
UMA Only: UMA@ /BT@/3G@
N12P-GS OPTIMUS: OPT@/GS@/X76@/BT@/3G@
N12P-GV OPTIMUS: OPT@/GV@/X76@/BT@/3G@

VRAM BOM Config
add later

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMA@
Discrete(OPTIMUS)	OPT@
VRAM	X76@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
Unpop	@
N12P-GS	GS@
N12P-GV	GV@

Project ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_PID} min	V_{AD_PID} typ	V_{AD_PID} max
JM30	0	0 V	0 V	0 V
JM40	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
JM50	18K +/- 5%	0.436 V	0.503 V	0.538 V
SJM30	33K +/- 5%	0.712 V	0.819 V	0.875 V
SJM40	56K +/- 5%	1.036 V	1.185 V	1.264 V
SJM50	100K +/- 5%	1.453 V	1.650 V	1.759 V
NC	NC			
NC	NC			

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Left Side)
		1	USB/B (Left Side)
	UHCI1	2	
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	Mini Card(WWAN)
	UHCI5	10	Camera
		11	
	UHCI6	12	SIM Card
		13	Blue Tooth

Design Common

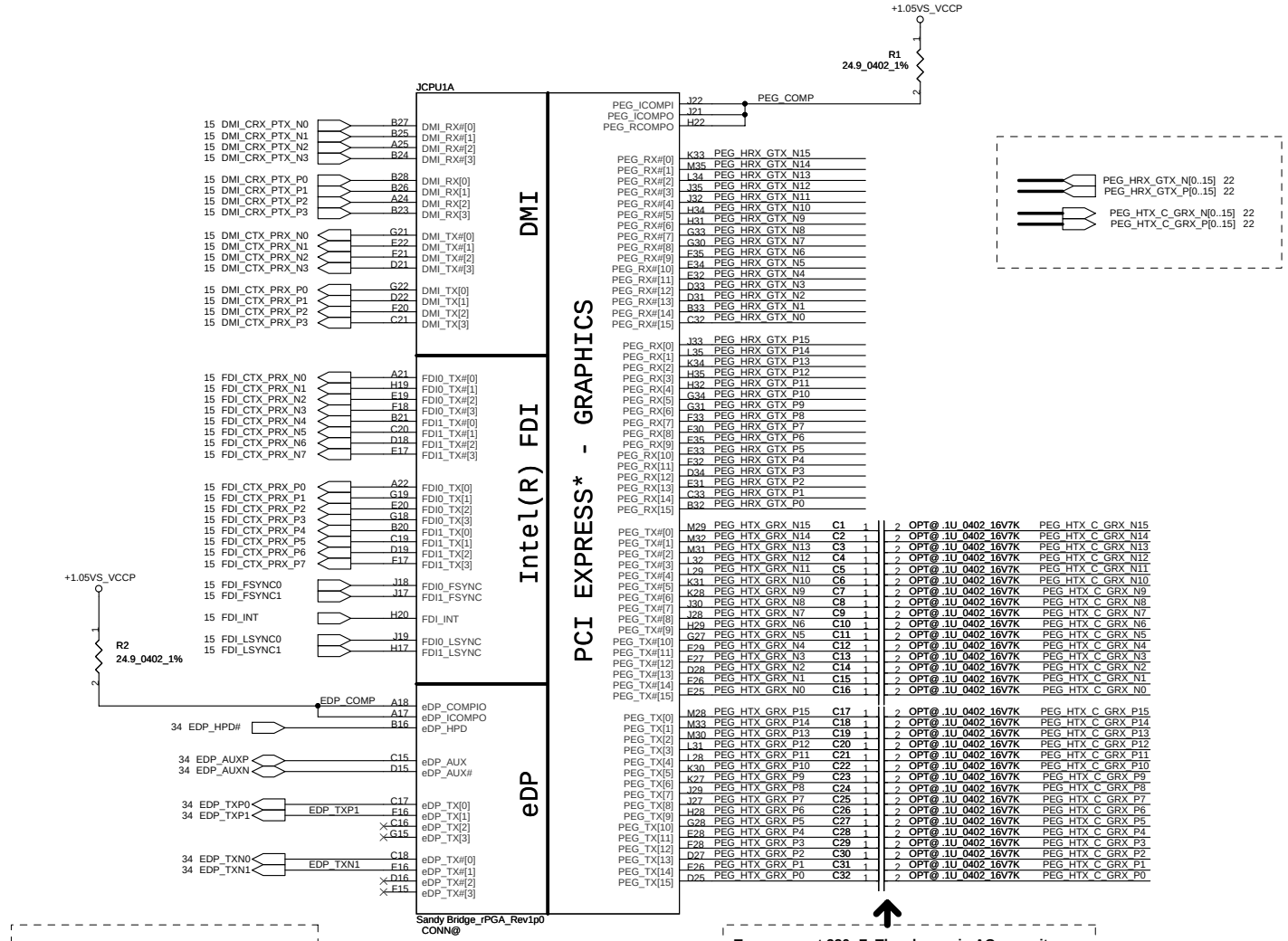
schematics pages sequence	Part count location define
CPU/PCH/CLK	1~1099
DIMM	2000~2099
dGPU	1400~1999
LVDS/CRT/HDMI/DP	2100~2199
Audio	1100~1199
LAN	1200~1299
Card Reader	1300~1399
Other IO (HDD/ODD/MINI/ USB/KBD/BIOS/ Button/LED)	2400~xxxx
KBC	2200~2299
POK CKT, DC/DC	2300~2399

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

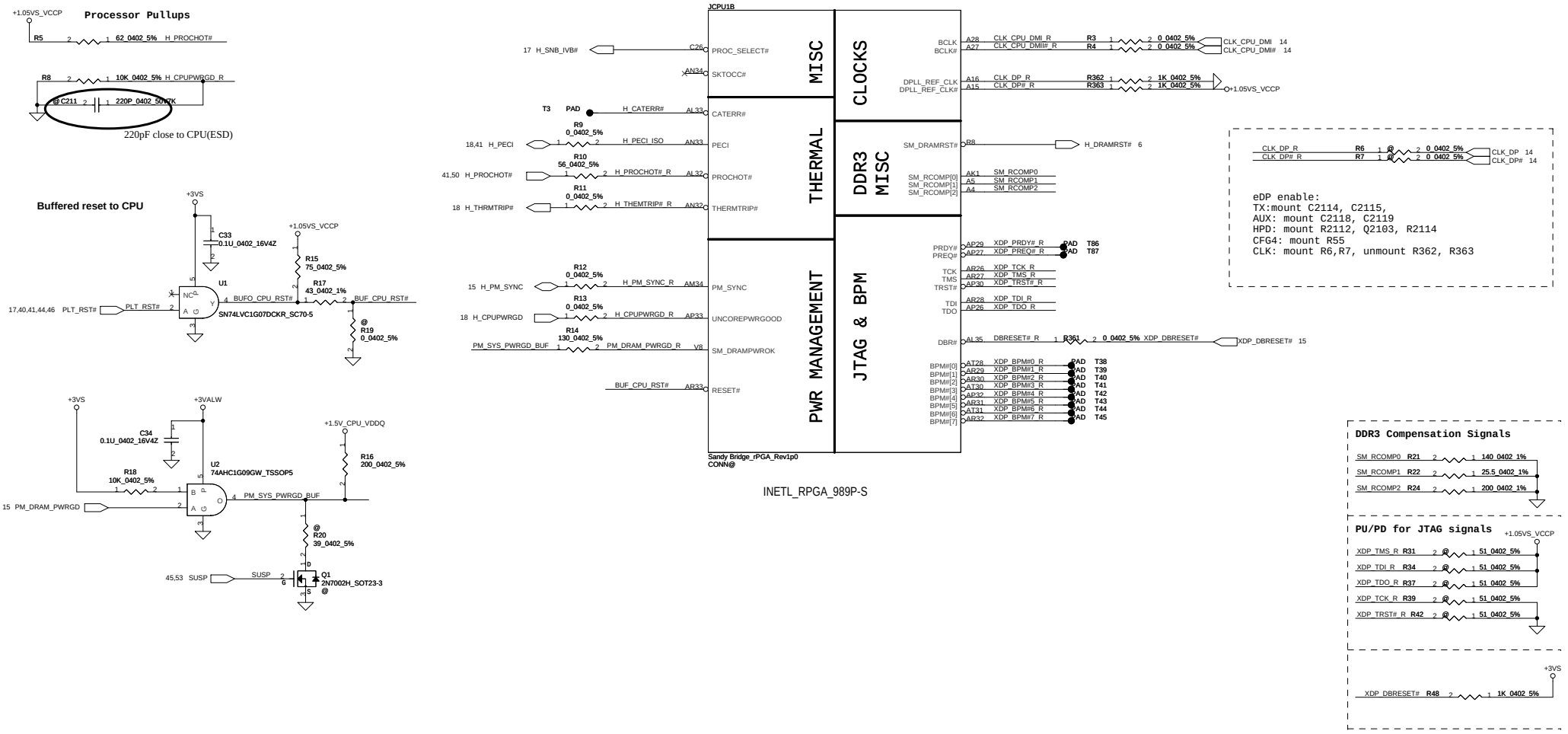
Size	Document Number	Rev
C	4019BI	A

Date: Tuesday, December 14, 2010 Sheet 3 of 57



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title	SCHEMATIC,MB LA-A7121		
Size: Custom	Document Number: 4019BI		Rev: A
Date: Tuesday, December 14, 2010	Sheet 4 of 57		



INETL_RPGA_989P-S

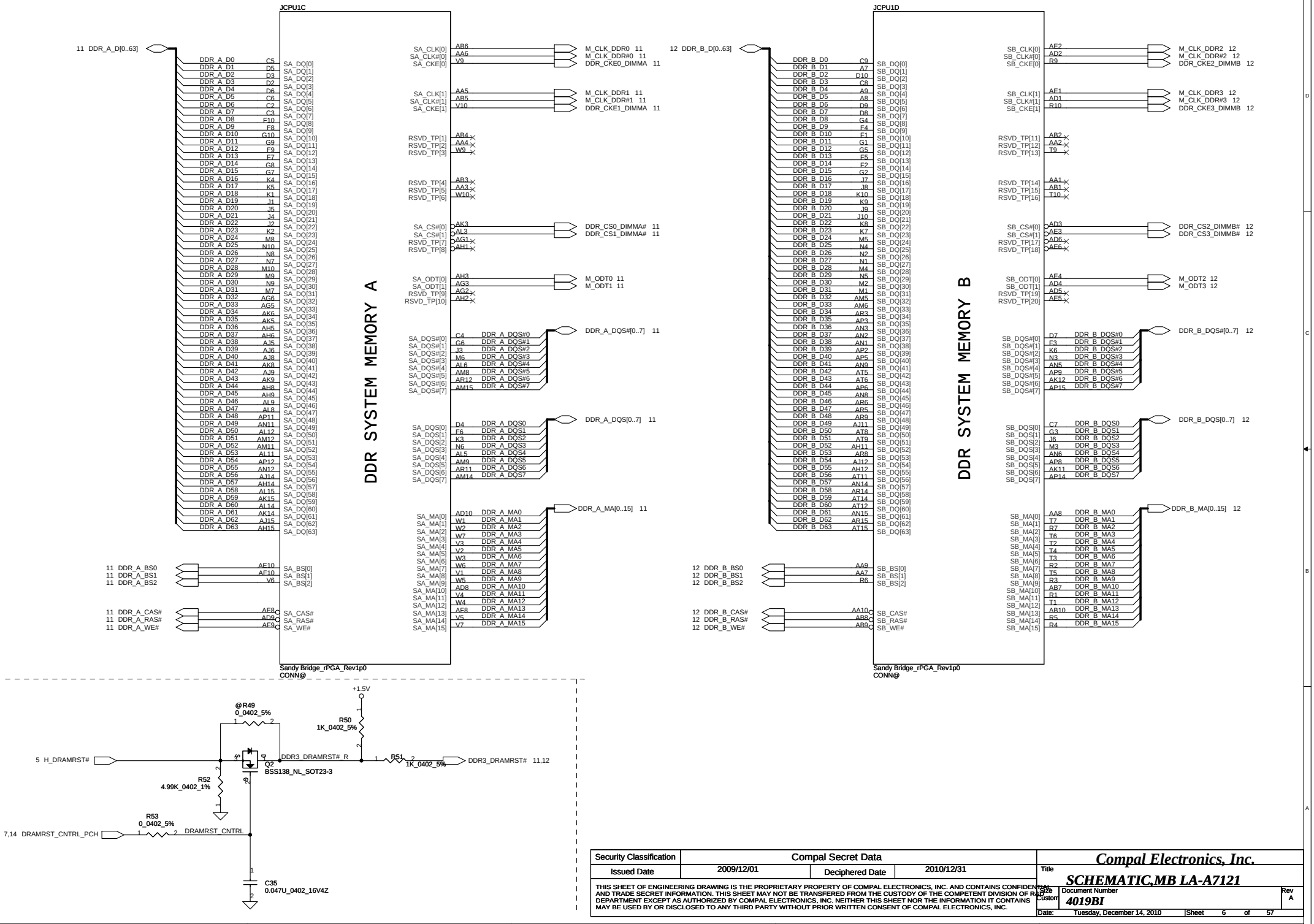
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size: C | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 5 of 57



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

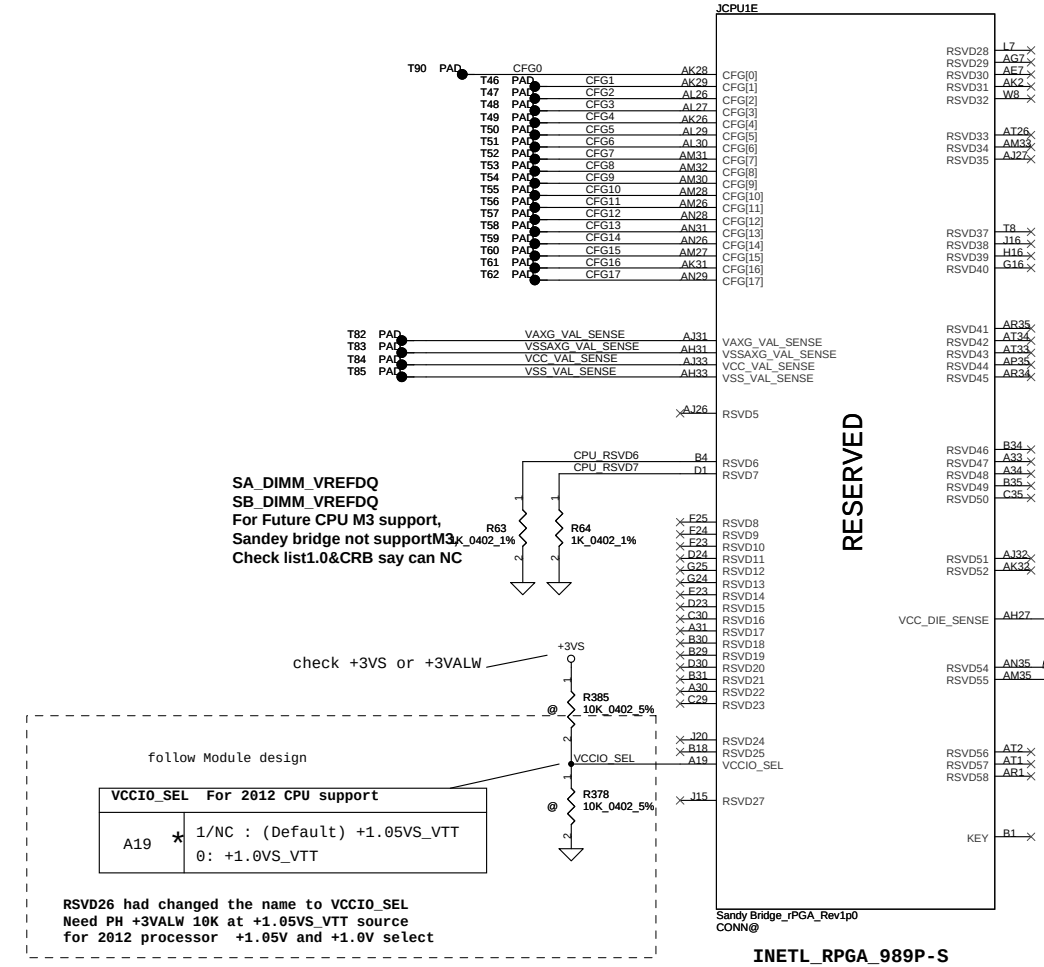
Compal Electronics, Inc.

Title: **SCHEMATIC,MB LA-A7121**

Size	Document Number	Rev
Custom	4019BI	A

Date: Tuesday, December 14, 2010 | Sheet 6 of 57

CFG Straps for Processor



INETL_RPGA_989P-S

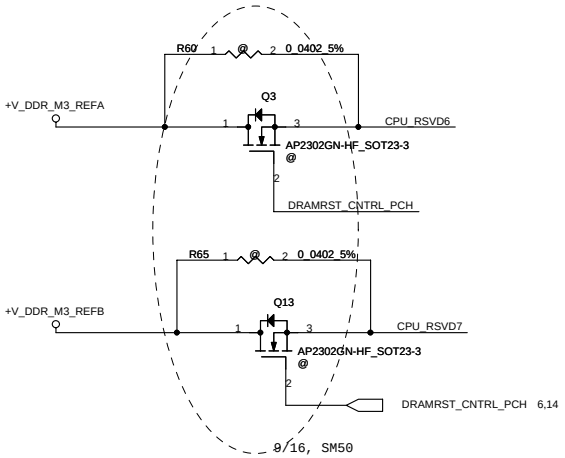
SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
For Future CPU M3 support,
Sandey bridge not supportM3
Check list1.0&CRB say can NC

check +3VS or +3VALW

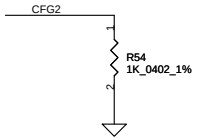
VCCIO_SEL For 2012 CPU support	
A19 *	1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

RSVD26 had changed the name to VCCIO_SEL
Need PH +3VALW 10K at +1.05VS_VTT source
for 2012 processor +1.05V and +1.0V select

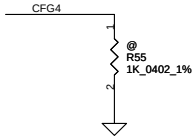
10/2, From JM50, delete,
10/19, From checklist 1.2, add the path



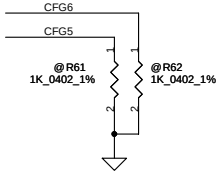
9/16, SM50



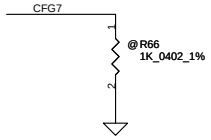
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



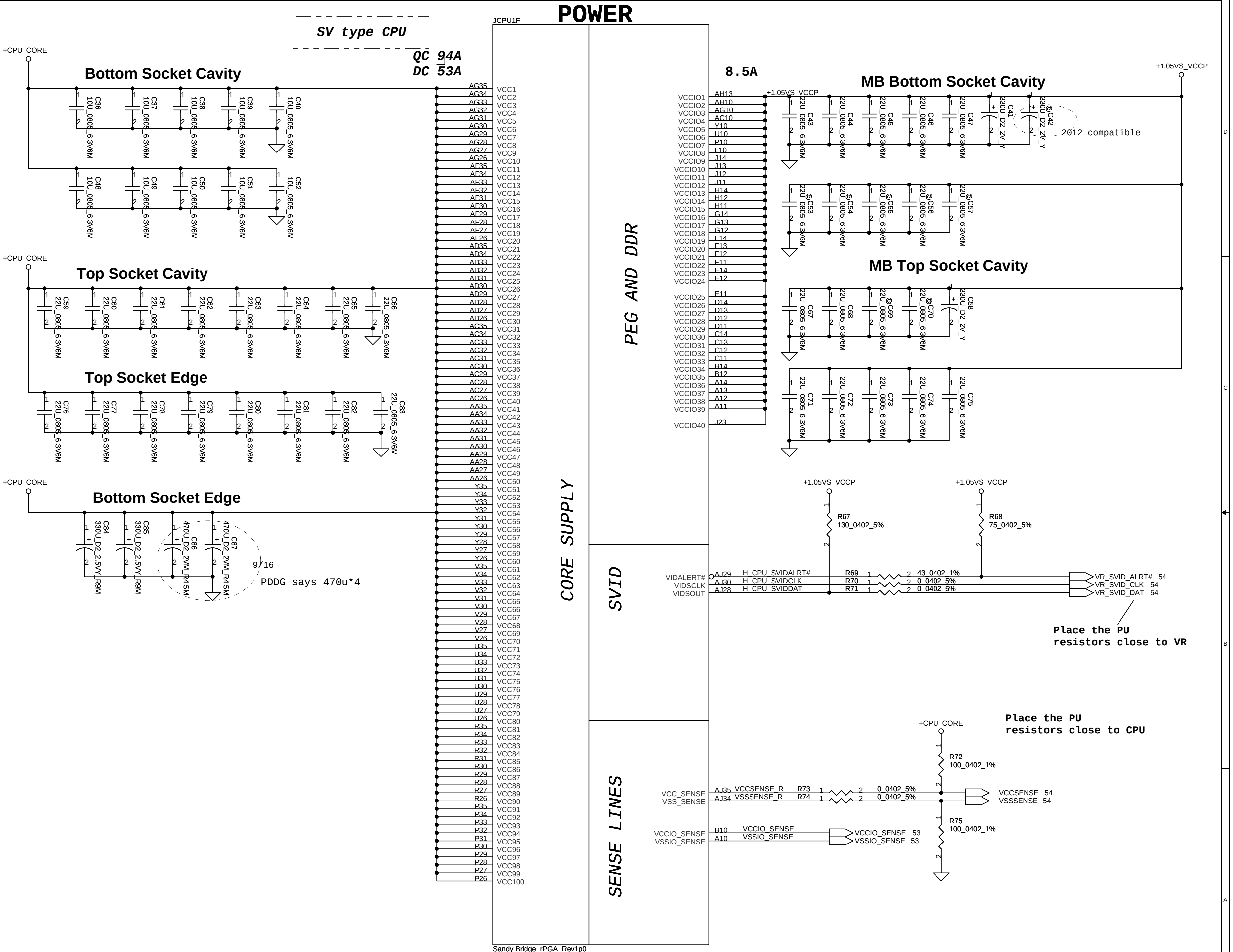
PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Title	Compal Electronics, Inc. SCHEMATIC,MB LA-A7121		
Size Custom	Document Number 4019BI		Rev A
Date: Tuesday, December 14, 2010	Sheet 7 of 57		



POWER
SV type CPU
QC 94A
DC 53A
JCPU1F
+CPU_CORE
Bottom Socket Cavity
C36 10U_0805_6.3V6M
C37 10U_0805_6.3V6M
C38 10U_0805_6.3V6M
C39 10U_0805_6.3V6M
C40 10U_0805_6.3V6M
C48 10U_0805_6.3V6M
C49 10U_0805_6.3V6M
C50 10U_0805_6.3V6M
C51 10U_0805_6.3V6M
C52 10U_0805_6.3V6M
Top Socket Cavity
C59 22U_0805_6.3V6M
C60 22U_0805_6.3V6M
C61 22U_0805_6.3V6M
C62 22U_0805_6.3V6M
C63 22U_0805_6.3V6M
C64 22U_0805_6.3V6M
C65 22U_0805_6.3V6M
C66 22U_0805_6.3V6M
Top Socket Edge
C76 22U_0805_6.3V6M
C77 22U_0805_6.3V6M
C78 22U_0805_6.3V6M
C79 22U_0805_6.3V6M
C80 22U_0805_6.3V6M
C81 22U_0805_6.3V6M
C82 22U_0805_6.3V6M
C83 22U_0805_6.3V6M
Bottom Socket Edge
C84 330U_D2_2.5VY_R9M
C85 330U_D2_2.5VY_R9M
C86 470U_D2_2VM_R4.5M
C87 470U_D2_2VM_R4.5M
9/16
PDDG says 470u*4
CORE SUPPLY
VCC1 … VCC100
AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26
PEG AND DDR
8.5A
VCCIO1 … VCCIO40
AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23
+1.05VS_VCCP
MB Bottom Socket Cavity
C43 22U_0805_6.3V6M
C44 22U_0805_6.3V6M
C45 22U_0805_6.3V6M
C46 22U_0805_6.3V6M
C47 22U_0805_6.3V6M
C41 330U_D2_2V_Y
@C42 330U_D2_2V_Y
2012 compatible
@C53 22U_0805_6.3V6M
@C54 22U_0805_6.3V6M
@C55 22U_0805_6.3V6M
@C56 22U_0805_6.3V6M
@C57 22U_0805_6.3V6M
MB Top Socket Cavity
C67 22U_0805_6.3V6M
C68 22U_0805_6.3V6M
@C69 22U_0805_6.3V6M
@C70 22U_0805_6.3V6M
C58 330U_D2_2V_Y
C71 22U_0805_6.3V6M
C72 22U_0805_6.3V6M
C73 22U_0805_6.3V6M
C74 22U_0805_6.3V6M
C75 22U_0805_6.3V6M
SVID
VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT
R67 130_0402_5%
R68 75_0402_5%
R69 43_0402_1%
R70 0_0402_5%
R71 0_0402_5%
VR_SVID_ALRT# 54
VR_SVID_CLK 54
VR_SVID_DAT 54
Place the PU resistors close to VR
SENSE LINES
VCC_SENSE AJ35 VCCSENSE_R
VSS_SENSE AJ34 VSSSENSE_R
R73 0_0402_5%
R74 0_0402_5%
R72 100_0402_1%
R75 100_0402_1%
VCCSENSE 54
VSSSENSE 54
Place the PU resistors close to CPU
VCCIO_SENSE B10 VCCIO_SENSE
VSSIO_SENSE A10 VSSIO_SENSE
VCCIO_SENSE 53
VSSIO_SENSE 53
Sandy Bridge_rPGA_Rev1p0
CONN@

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: **SCHEMATIC,MB LA-A7121**

Size: Custom | Document Number: **4019BI** | Rev: A

Date: Tuesday, December 14, 2010 |

DELETE

POWER

EDS1.3

QC DC 33A

JCPU1G

+VGFX_CORE

Top Socket Cavity

22U_0805_6.3V6M: C91, C92, C93, C94

Top Socket Edge

22U_0805_6.3V6M: C95, C96, C97, C98

Bottom Socket Cavity

22U_0805_6.3V6M: C100, C101, C102, C103

Bottom Socket Edge

22U_0805_6.3V6M: @ C111, @ C112, @ C113, @ C114

Bottom Socket Edge

330U_D2_2V_Y: C115

@ 330U_D2_2V_Y: C116

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

GRAPHICS

SENSE LINES

VAXG_SENSE AK35 → VCC_AXG_SENSE 54

VSSAXG_SENSE AK34 → VSS_AXG_SENSE 54

VREF

+V_SM_VREF should have 20 mil trace width

SM_VREF AL1 +V_SM_VREF_CNT

C99 0.1U_0402_16V4Z

R84 0_0402_5% +V_SM_VREF

10/2

+1.5V_CPU_VDDQ

R83 1K_0402_1%

R85 1K_0402_1%

DDR3 -1.5V RAILS

10A

VDDQ1 AF7, VDDQ2 AF4, VDDQ3 AF1, VDDQ4 AC7, VDDQ5 AC4, VDDQ6 AC1, VDDQ7 Y7, VDDQ8 Y4, VDDQ9 Y1, VDDQ10 U7, VDDQ11 U4, VDDQ12 U1, VDDQ13 P7, VDDQ14 P4, VDDQ15 P1

+1.5V_CPU_VDDQ, +1.5VS

JP1 @ PAD-OPEN 4x4m

10U_0805_6.3V6M: C105, C106, C107, C108, C109, C110

C104 330U_D2_2V_Y

SA RAIL

6A

VCCSA1 M27, VCCSA2 M26, VCCSA3 L26, VCCSA4 J26, VCCSA5 J25, VCCSA6 J24, VCCSA7 H26, VCCSA8 H25

+VCCSA

10U_0805_6.3V6M: C117, C118, C119

@ 10U_0603_6.3V6M: C120

C121 330U_D2_2V_Y

9/16, SM50

R86 100_0402_5% VCCSA_SENSE

R87 0_0402_5% VSSSA_SENSE 52

MISC

VCCSA_SENSE H23 → VCCSA_SENSE 52

FC_C22 C22, VCCSA_VID1 C24 H_FC_C22 → VCCSA_VID1 52

R89 10K_0402_5%

@ R90 0_0402_5%

1.8V RAIL

1.2A

+1.8VS R88 0_0805_5% +1.8VS_VCCPLL

VCCPLL1 B6, VCCPLL2 A6, VCCPLL3 A2

C122 330U_D2_2V_Y

C125 10U_0805_6.3V6M

C123 1U_0402_6.3V6K

C124 1U_0402_6.3V6K

Sandy Bridge_rPGA_Rev1p0

CONN@

Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

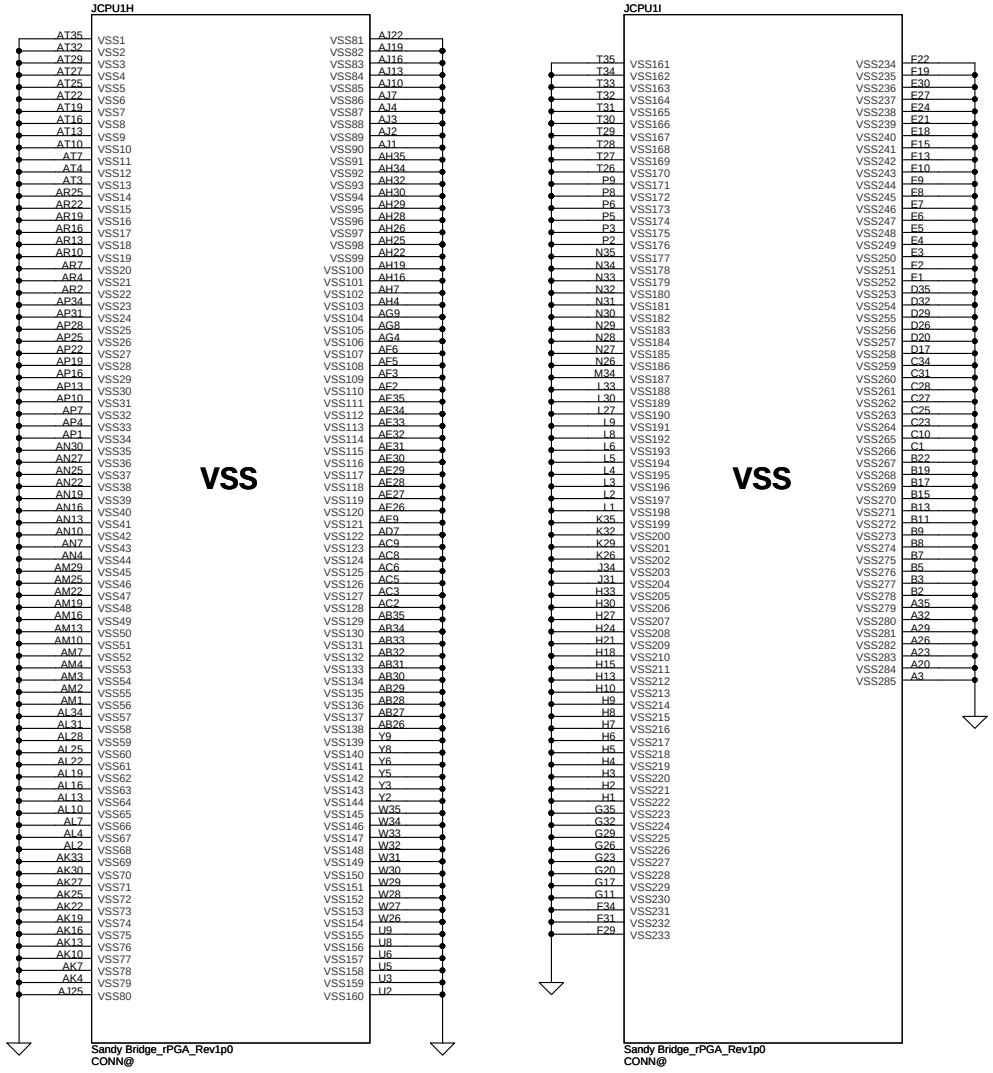
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 9 of 57



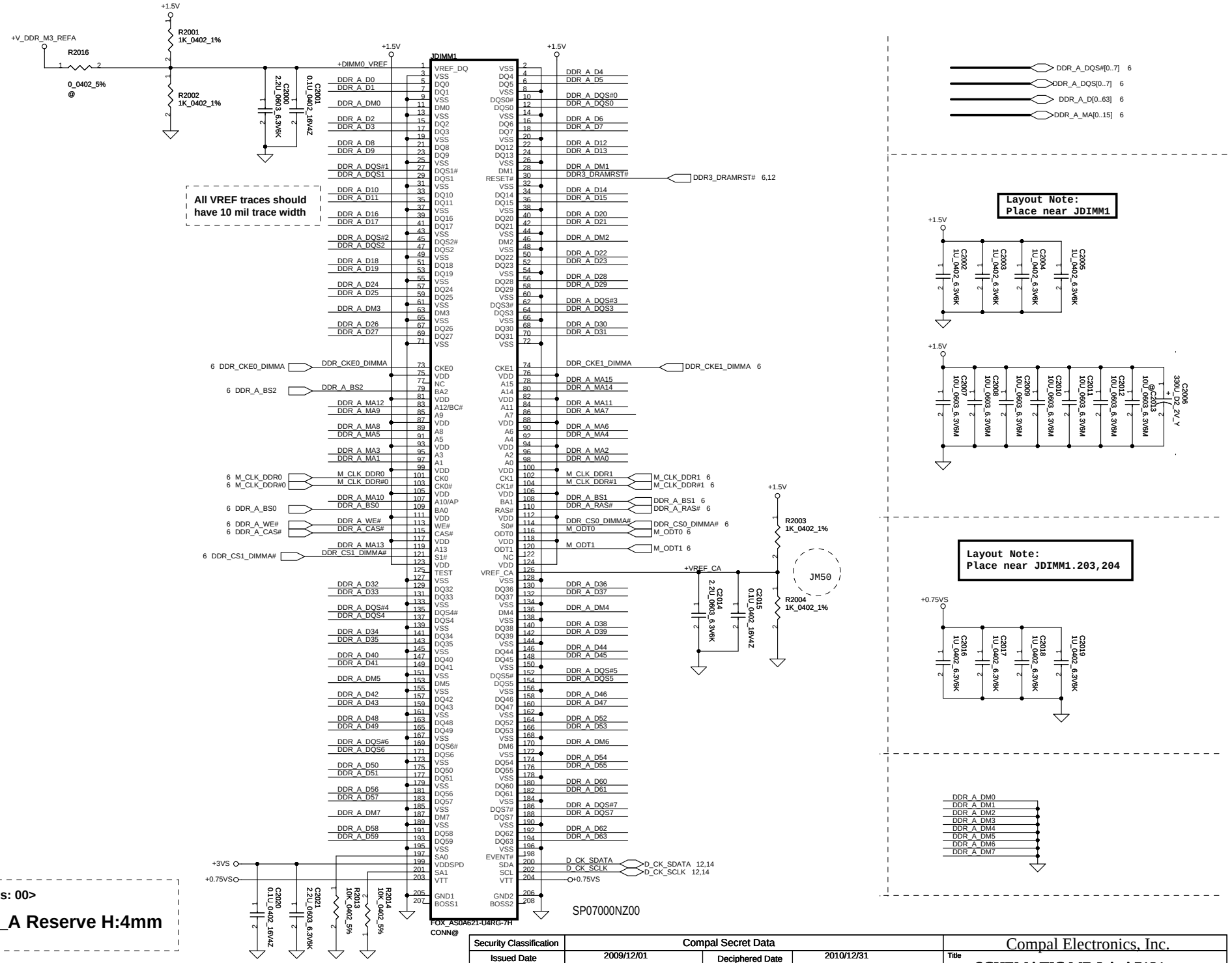
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size	Document Number	Rev
Custom	4019BI	A

Date: Tuesday, December 14, 2010 Sheet 10 of 57



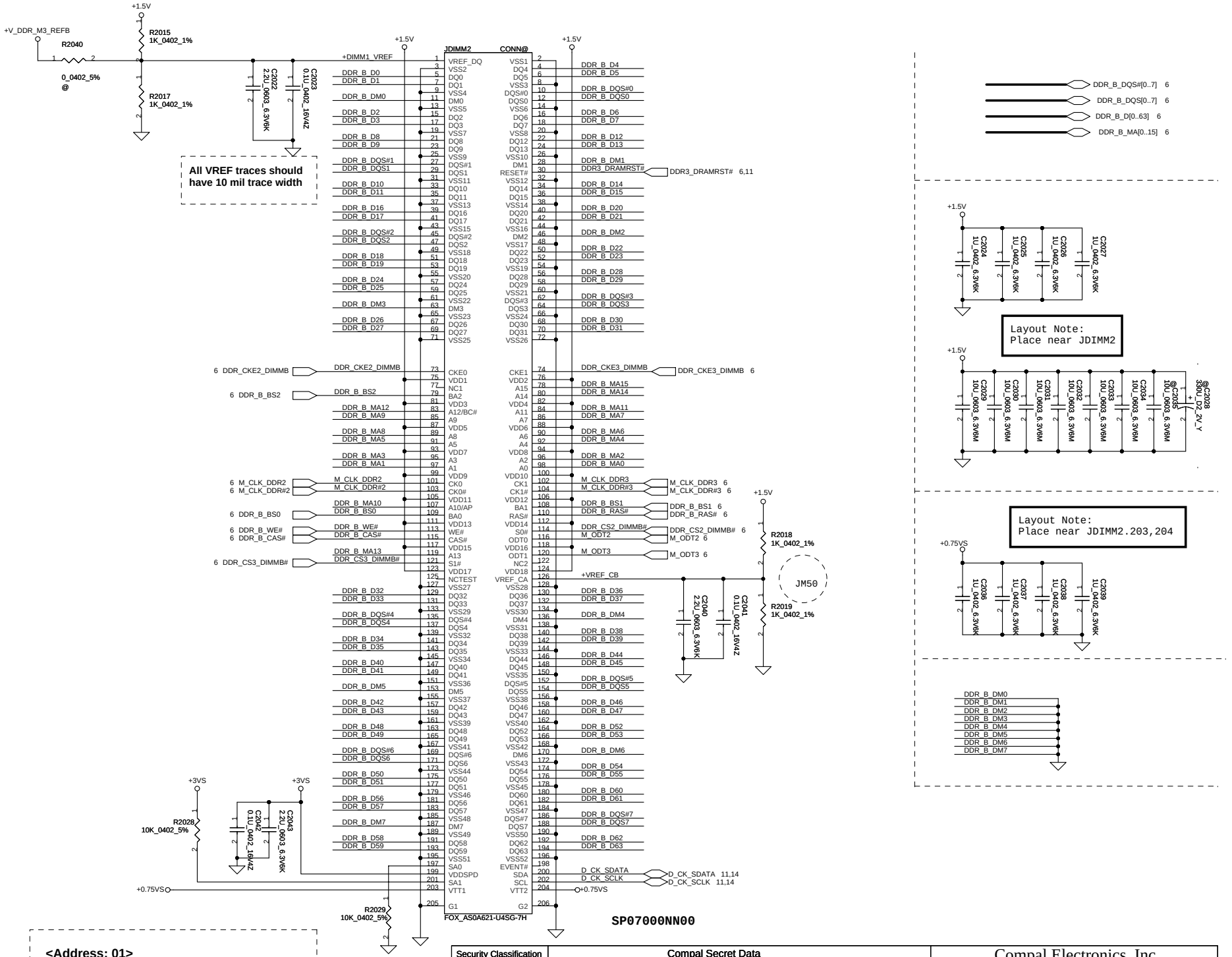
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size	Document Number	Rev
Custom	4019BI	A

Date: Tuesday, December 14, 2010 Sheet 11 of 57



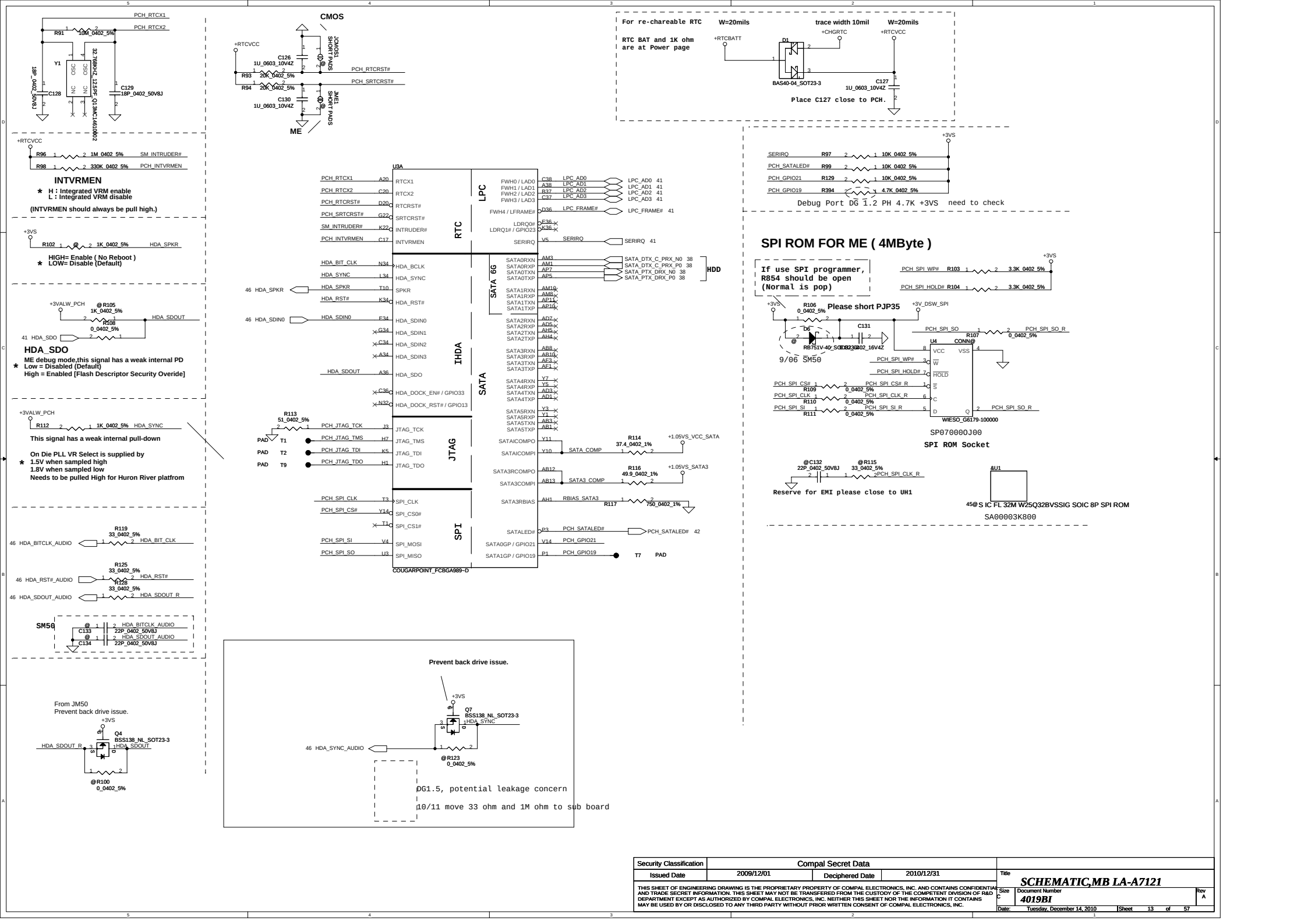
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

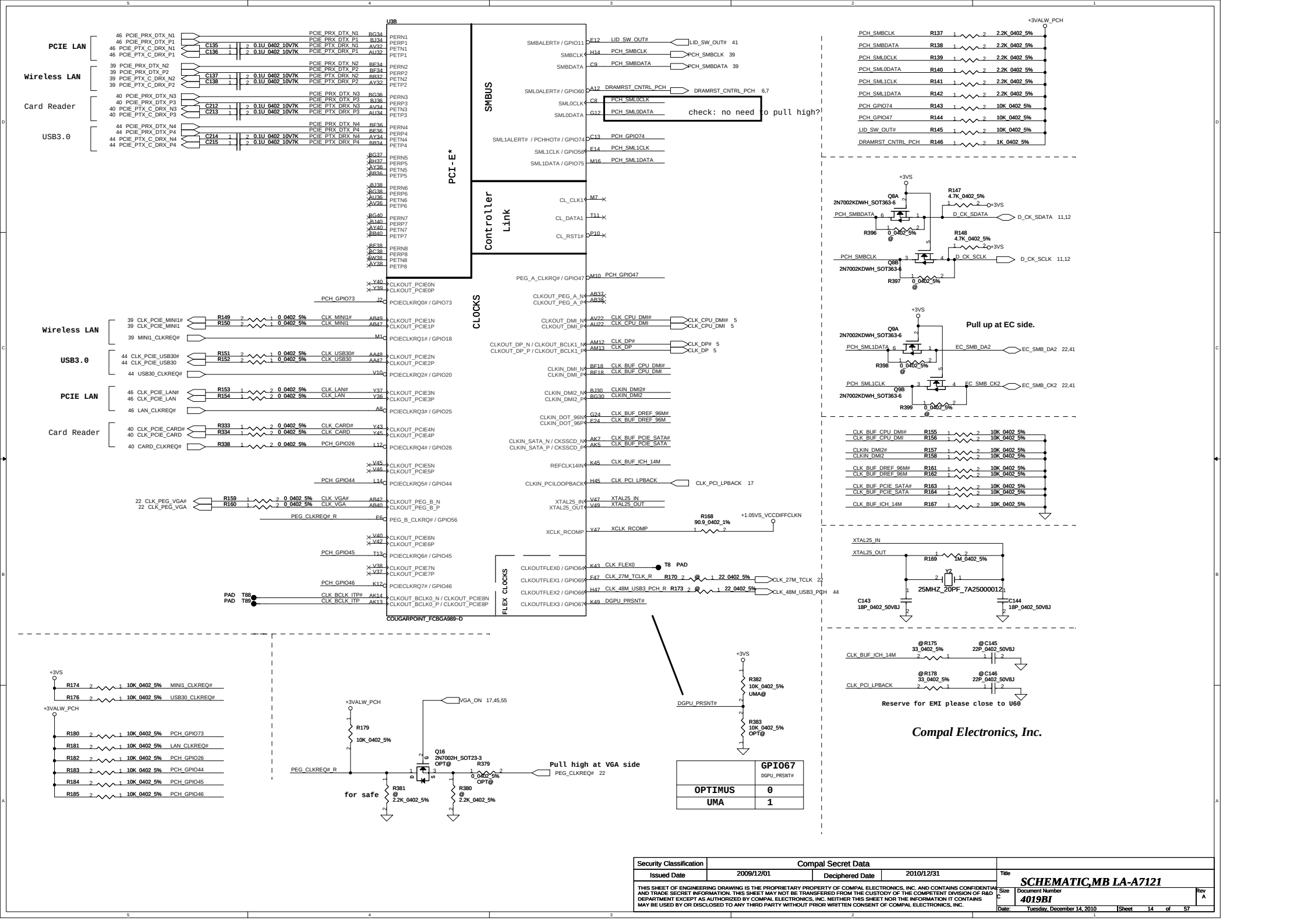
Size	Document Number	Rev
Custom	4019BI	A

Date: Tuesday, December 14, 2010 Sheet 12 of 57



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Title	SCHEMATIC,MB LA-A7121		
Size C	Document Number 4019BI		Rev A
Date: Tuesday, December 14, 2010	Sheet 13 of 57		



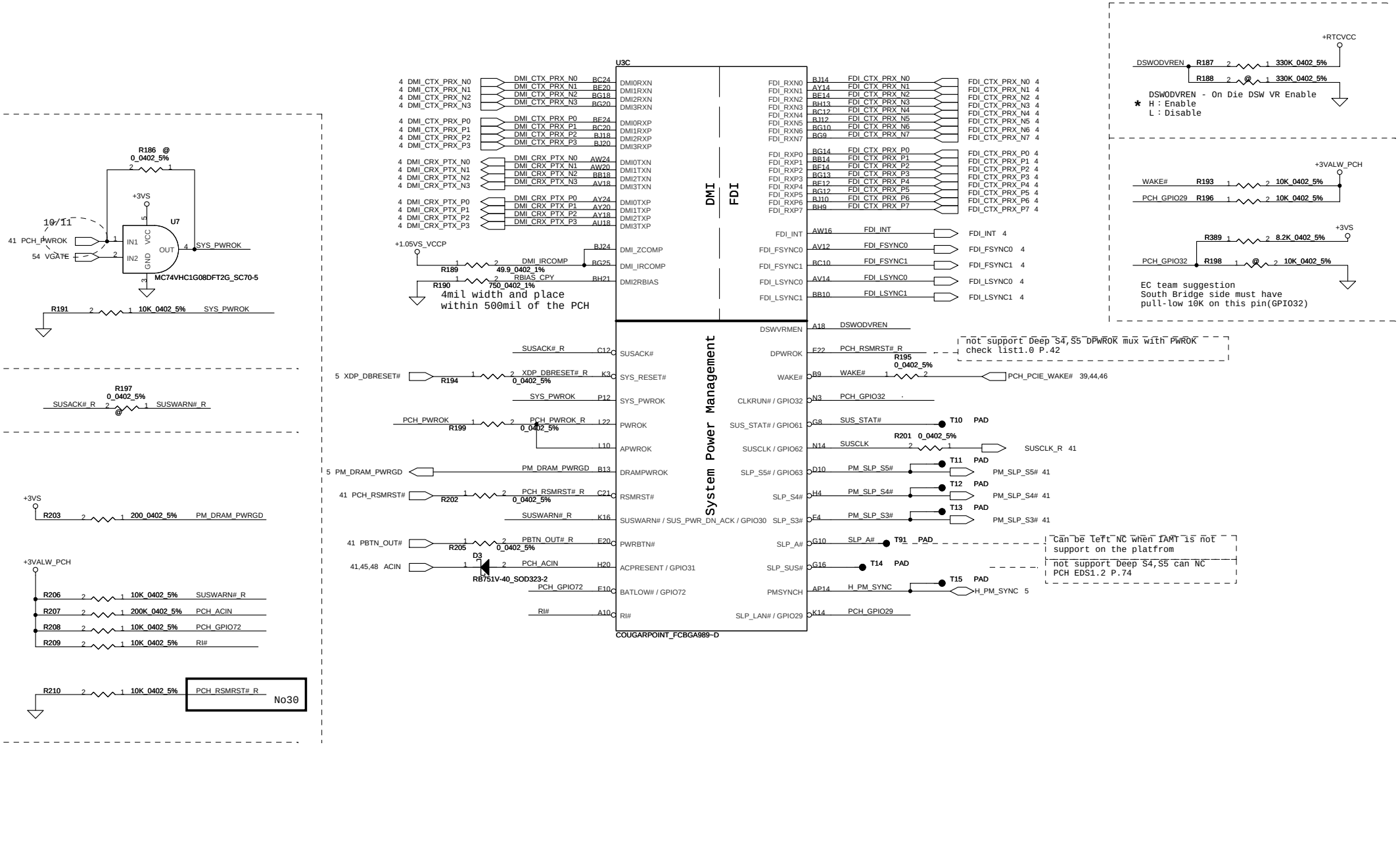
	GPIO67 DGPU_PRSNT#
OPTIMUS	0
UMA	1

Compal Electronics, Inc.

Security Classification	Compal Secret Data
Issued Date	2009/12/01
Deciphered Date	2010/12/31

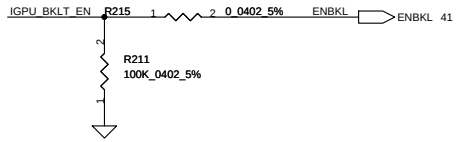
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

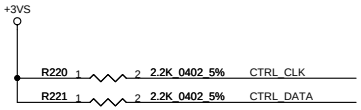
Title: SCHEMATIC,MB LA-A7121
Size: C | Document Number: 4019BI | Rev: A
Date: Tuesday, December 14, 2010 | Sheet 14 of 57

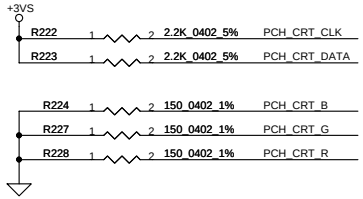


Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

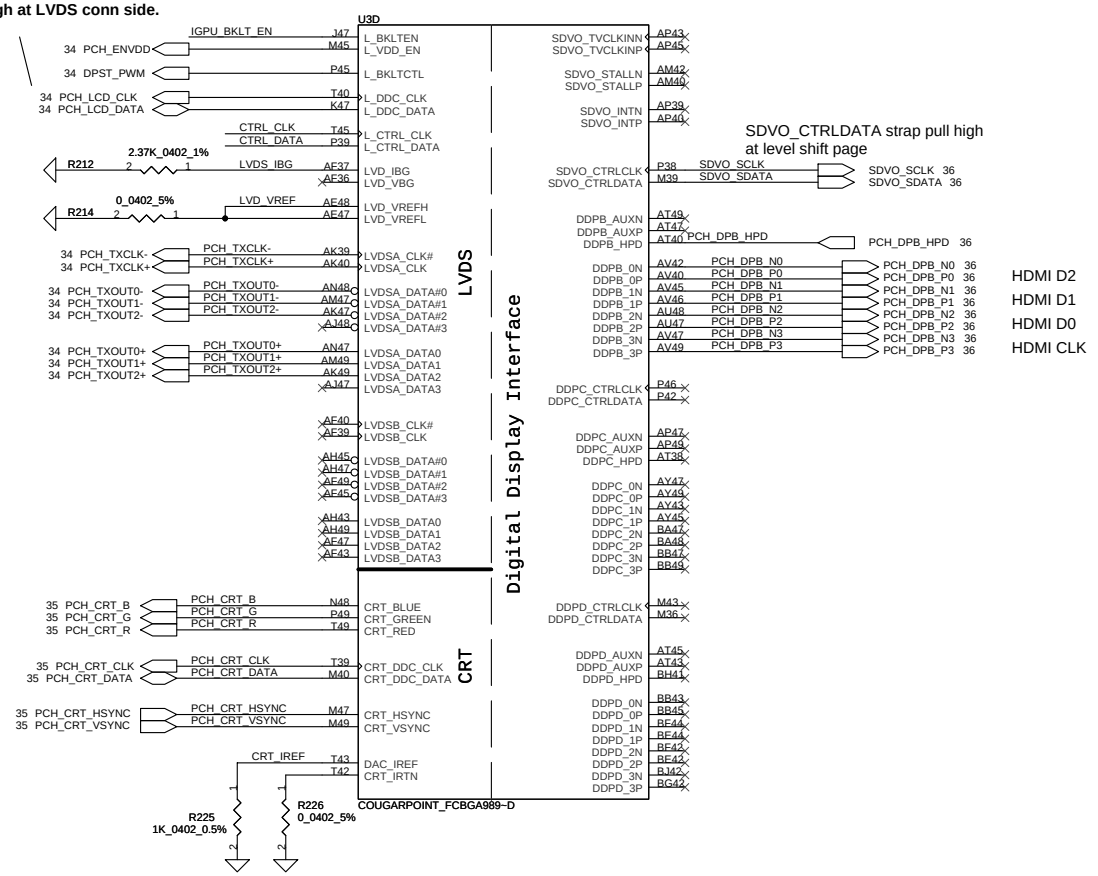
Compal Electronics, Inc.			
Title: SCHEMATIC,MB LA-A7121			
Size: Custom	Document Number: 4019BI		Rev: A
Date: Tuesday, December 14, 2010	Sheet 15 of 57		







Pull high at LVDS conn side.



Compal Electronics, Inc.	
Title	SCHEMATIC,MB LA-A7121
Size: Custom	Document Number: 4019BI
Rev: A	
Date: Tuesday, December 14, 2010	Sheet 16 of 57

footprint should change to RP_0804_8P4R
because RP_8P4R doesn't exist

+3VS

R229 8.2K_8P4R_5%: 8 PCI_PIRQA#, 7 PCI_PIRQD#, 6 PCI_PIRQC#, 5 PCI_PIRQB#

R230 8.2K_8P4R_5%: 8 PCH_GPIO55, 7 PCH_GPIO51, 6 PCH_GPIO5, 5 PCH_GPIO52

R231 8.2K_8P4R_5%: 8 PCH_GPIO2, 7 (No28), 6 PCH_GPIO4, 5 PCH_GPIO3

R233 8.2K_0402_5% PCH_GPIO53

10/2

R234 8.2K_0402_5% DGPU_HOLD_RST#

R388 100K_0402_5% PLT_RST#

Boot BIOS Strap bit1 BBS1

	Bit11	Bit10	Boot BIOS Destination
GNT1#/ GPIO51	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC

RF Boris Tsai suggests

CLK_PCI_LPBACK

CLK_PCI_LPC

C216 10P_0402_50V8J @

C217 10P_0402_50V8J @

U3E

RSVD: TP1 BG26, TP2 BJ26, TP3 BH25, TP4 BJ16, TP5 BG16, TP6 AH38, TP7 AH37, TP8 AK43, TP9 AK45, TP10 C18, TP11 N30, TP12 H3, TP13 AH12, TP14 AM4, TP15 AM5, TP16 Y13, TP17 K24, TP18 L24, TP19 AB46, TP20 AB45, TP21 B21, TP22 M20, TP23 AY16, TP24 BG46, TP25 BE28, TP26 BC30, TP27 BE32, TP28 BJ32, TP29 BC28, TP30 BE30, TP31 BF32, TP32 BG32, TP33 AV26, TP34 BB26, TP35 AU28, TP36 AY30, TP37 AU26, TP38 AY26, TP39 AV28, TP40 AW30

NVRAM: NV_CE#0 AY7, NV_CE#1 AV7, NV_CE#2 AU3, NV_CE#3 BG4, NV_DQS0 AT10, NV_DQS1 BC8, NV_DQ0 / NV_IO0 AU2, NV_DQ1 / NV_IO1 AT4, NV_DQ2 / NV_IO2 AT3, NV_DQ3 / NV_IO3 AT1, NV_DQ4 / NV_IO4 AV3, NV_DQ5 / NV_IO5 AT5, NV_DQ6 / NV_IO6 AV3, NV_DQ7 / NV_IO7 AV1, NV_DQ8 / NV_IO8 BB1, NV_DQ9 / NV_IO9 BA3, NV_DQ10 / NV_IO10 BB5, NV_DQ11 / NV_IO11 BB3, NV_DQ12 / NV_IO12 BB7, NV_DQ13 / NV_IO13 BE8, NV_DQ14 / NV_IO14 BD4, NV_DQ15 / NV_IO15 BF6

NV_ALE AV5, NV_CLE AY1 DF_TVS, NV_RCOMP AV10, NV_RB# AT8, NV_RE#_WRB0 AY5, NV_RE#_WRB1 BA2, NV_WE#_CK0 AT12, NV_WE#_CK1 BF3

PCI: PCI_PIRQA# K40 PIRQA#, PCI_PIRQB# K38 PIRQB#, PCI_PIRQC# H38 PIRQC#, PCI_PIRQD# G38 PIRQD#

R241 0_0402_5% DGPU_HOLD_RST# C46 REQ1# / GPIO50; PCH_GPIO52 C44 REQ2# / GPIO52; 14,45,55 VGA_ON — VGA_ON_R E40 REQ3# / GPIO54

PCH_GPIO51 D47 GNT1# / GPIO51; PCH_GPIO53 F42 GNT2# / GPIO53; PCH_GPIO55 F45 GNT3# / GPIO55

PCH_GPIO2 G42 PIRQE# / GPIO2; PCH_GPIO3 G40 PIRQF# / GPIO3; PCH_GPIO4 C42 PIRQG# / GPIO4; PCH_GPIO5 D44 PIRQH# / GPIO5

PAD T16 — PME# K10

5,40,41,44,46 PLT_RST# — PLT_RST# — PLTRST# C6

14 CLK_PCI_LPBACK, 41 CLK_PCI_LPC — CLK_PCI_LPC — R247 22_0402_5% — R248 22_0402_5%

CLKOUT_PCI0 H49 (CLK_PCI0), CLKOUT_PCI1 H43 (CLK_PCI1), CLKOUT_PCI2 J48 (CLK_PCI2), CLKOUT_PCI3 K42 (CLK_PCI3), CLKOUT_PCI4 H40 (CLK_PCI4)

PAD T17, PAD T18, PAD T19

No14

USB: USBP0N C24 USB20_N0 — USB20_N0 46; USBP0P A24 USB20_P0 — USB20_P0 46 — USB conn (left)

USBP1N C25 USB20_N1 — USB20_N1 37; USBP1P B25 USB20_P1 — USB20_P1 37 — USB conn (left)

USBP2N C26, USBP2P A26, USBP3N K28, USBP3P H28, USBP4N E28, USBP4P D28, USBP5N C28, USBP5P A28, USBP6N C29, USBP6P B29, USBP7N N28, USBP7P M28

PCH HM65 config not support USB port 6 & 7.

USBP8N L30 USB20_N8 — USB20_N8 39; USBP8P K30 USB20_P8 — USB20_P8 39 — Mini Card(WLAN)

USBP9N G30 USB20_N9 — USB20_N9 39; USBP9P E30 USB20_P9 — USB20_P9 39 — Mini Card(WWAN)

USBP10N C30 USB20_N10 — USB20_N10 34; USBP10P A30 USB20_P10 — USB20_P10 34 — CMOS Camera (LVDS)

USBP11N L32, USBP11P K32

USBP12N G32 USB20_N12 — USB20_N12 39; USBP12P E32 USB20_P12 — USB20_P12 39 — Mini Card(SIM reserved)

USBP13N C32 USB20_N13 — USB20_N13 40; USBP13P A32 USB20_P13 — USB20_P13 40 — Bluetooth

Within 500 mils

USBRBIAS# C33 USBRBIAS — R246 22.6_0402_1%

USBRBIAS B33

OC0# / GPIO59 A14 USB_OC0# — USB_OC0# 46; OC1# / GPIO40 K20 USB_OC1# — USB_OC1# 37 (For USB Port1)

OC2# / GPIO41 B17 USB_OC2#; OC3# / GPIO42 C16 USB_OC3#; OC4# / GPIO43 L16 USB_OC4#; OC5# / GPIO9 A16 USB_OC5#; OC6# / GPIO10 D14 USB_OC6#; OC7# / GPIO14 C14 USB_OC7#

(For USB Port0)

COUGARPOINT_FCBGA989~D

DMI Termination Voltage

DF_TVS	Set to Vcc when HIGH
	Set to Vss when LOW

+1.8VS

DG1.2

2.2K_0402_5% R235

DF_TVS — R236 1K_0402_5% — H_SNB_IVB# 5

CLOSE TO THE BRANCHING POINT

USB_OC0# R237 10K_0402_5%
USB_OC1# R238 10K_0402_5%
USB_OC2# R239 10K_0402_5%
USB_OC3# R240 10K_0402_5%
USB_OC4# R242 10K_0402_5%
USB_OC5# R243 10K_0402_5%
USB_OC6# R244 10K_0402_5%
USB_OC7# R245 10K_0402_5%
— +3VALW_PCH

OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2

No40

+3VS

U10 OPT@ (MC74VHC1G08DFT2G_SC70-5)

PLT_RST# 1 — IN1; DGPU_HOLD_RST# 2 — R232 0_0402_5% OPT@ — IN2

VCC 5, GND 3, OUT 4

R252 100_0402_5% OPT@ — PLTRST_VGA# 22

R253 100K_0402_5% OPT@

No40

R250 0_0402_5% @

+3VS

U11 (MC74VHC1G08DFT2G_SC70-5)

PLT_RST# 1 — IN1; IN2 2

VCC 5, GND 3, OUT 4 — PLT_RST_BUF# 39

R254 100K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 17 of 57

+3VS

R264 2 UMA@ 1 10K_0402_5% OPTIMUS_EN#

R393 1 OPT@ 2 10K_0402_5%

	GPIO38 OPTIMUS_EN#
* OPTIMUS	0
Non-OPTIMUS	1

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

+3VALW_PCH

R395 1 @ 2 4.7K_0402_5%

R260 1 @ 2 1K_0402_5% PCH_GPIO28

Debug Port DG 1.2 PH 4.7K +3VALW_PCH

Can be configured as wake input to allow wakes from Deep Sleep.
If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

R262 1 2 10K_0402_5% PCH_GPIO27

+3VS

R275 1 2 100K_0402_5% WWAN_OFF#

R391 1 @ 2 10K_0402_5%

R277 1 @ 2 200K_0402_5% PCH_GPIO36

R392 1 2 10K_0402_5%

GPIO36: CRB1.0 PH200K to +3VS, but CHK1.2 says pull down when not used

No26
No34

+3VALW

R273 10K_0402_5% OPT@

+3VS

R267 10K_0402_5%

VRAM_1.5VS

R130 OPT@ 10K_0402_5%

Q17 OPT@ 2N7002H_SOT23-3

Q5 OPT@ AP2302GN-HF_SOT23-3

C218 1U_0402_6.3V6K OPT@

+3VS

R255 2 1 10K_0402_5% PCH_GPIO0

R270 1 2 10K_0402_5% PCH_GPIO1

R271 1 2 10K_0402_5% PCH_GPIO6

R272 1 2 10K_0402_5% PCH_GPIO16

No20

R274 1 2 10K_0402_5% PCH_GPIO22

R276 1 2 10K_0402_5% PCH_GPIO39

R278 1 2 10K_0402_5% BT_ON#

R279 1 2 10K_0402_5% PCH_GPIO48

R280 1 2 10K_0402_5% WL_OFF#

+3VALW_PCH

R281 1 2 10K_0402_5% PCH_GPIO12

R282 1 2 1K_0402_5% SMIB

R283 1 2 10K_0402_5% PCH_GPIO57

R284 1 2 10K_0402_5% PCH_GPIO24

R285 1 2 10K_0402_5% PCH_GPIO35

10/2 JM50 install, SM50 uninstall

CRB1.0 PH10K to +3VALW
GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

U3F

PCH_GPIO0	T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40	PCH_GPIO68
PCH_GPIO1	A42	TACH1 / GPIO1	TACH5 / GPIO69	B41	PCH_GPIO69
PCH_GPIO6	H36	TACH2 / GPIO6	TACH6 / GPIO70	C41	PCH_GPIO70
41 EC_SCI#	E38	TACH3 / GPIO7	TACH7 / GPIO71	A40	PCH_GPIO71
41 EC_SMI#	C10	GPIO8			
PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12			
44 SMIB	G2	GPIO15	A20GATE	P4	GATEA20 41
PCH_GPIO16	U2	SATA4GP / GPIO16	PECI	AU16	PCH_PECI_R 0_0402_5% R265 H_PECI 5,41
DGPU_PWROK	D40	TACH0 / GPIO17	RCIN#	P5	EC_KBRST# EC_KBRST# 41
PCH_GPIO22	T5	SCLOCK / GPIO22	PROCPWRGD	AY11	H_CPUPWRGD 5
PCH_GPIO24	E8	GPIO24 / MEM_LED	THRMTRIP#	AY10	PCH_THRMTRIP# R 390_0402_5% R268 H_THRMTRIP# H_THRMTRIP# 5
PCH_GPIO27	E16	GPIO27	INIT3_3V#	T14	
PCH_GPIO28	P8	GPIO28	NC_1	AH8	
39,40 BT_ON#	K1	STP_PCI# / GPIO34	NC_2	AK11	
PCH_GPIO35	K4	GPIO35	NC_3	AH10	
PCH_GPIO36	V8	SATA2GP / GPIO36	NC_4	AK10	
39 WWAN_OFF#	M5	SATA3GP / GPIO37	NC_5	P37	
OPTIMUS_EN#	N2	SLOAD / GPIO38			
PCH_GPIO39	M3	SDATAOUT0 / GPIO39			
PCH_GPIO48	V13	SDATAOUT1 / GPIO48			
39 WL_OFF#	V3	SATA5GP / GPIO49			
PCH_GPIO57	D6	GPIO57			

GPIO

CPU/MISC

PAD T73	A4	VSS_NCTF_1	VSS_NCTF_15	BG2	T20 PAD
PAD T74	A44	VSS_NCTF_2	VSS_NCTF_16	BG48	T21 PAD
PAD T75	A45	VSS_NCTF_3	VSS_NCTF_17	BH3	T22 PAD
PAD T76	A46	VSS_NCTF_4	VSS_NCTF_18	BH47	T23 PAD
PAD T77	A5	VSS_NCTF_5	VSS_NCTF_19	BJ4	T63 PAD
PAD T78	A6	VSS_NCTF_6	VSS_NCTF_20	BJ44	T24 PAD
PAD T79	B3	VSS_NCTF_7	VSS_NCTF_21	BJ45	T25 PAD
PAD T80	B47	VSS_NCTF_8	VSS_NCTF_22	BJ46	T26 PAD
PAD T27	BD1	VSS_NCTF_9	VSS_NCTF_23	BJ5	T64 PAD
PAD T28	BD49	VSS_NCTF_10	VSS_NCTF_24	BJ6	T65 PAD
PAD T29	BE1	VSS_NCTF_11	VSS_NCTF_25	C2	T81 PAD
PAD T30	BE49	VSS_NCTF_12	VSS_NCTF_26	C48	T66 PAD
PAD T31	BE1	VSS_NCTF_13	VSS_NCTF_27	D1	T67 PAD
PAD T32	BF49	VSS_NCTF_14	VSS_NCTF_28	D49	T68 PAD
			VSS_NCTF_29	F1	T69 PAD
			VSS_NCTF_30	F49	T70 PAD
			VSS_NCTF_31	F1	T71 PAD
			VSS_NCTF_32	F49	T72 PAD

NCTF

COUGARPOINT_FCBGA989~D

check: pull high?

+3VS

R263 10K_0402_5%

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand.

+3VS

PCH_GPIO68 R256 1 2 10K_0402_5%

PCH_GPIO69 R257 1 2 10K_0402_5%

PCH_GPIO70 R258 1 2 10K_0402_5%

PCH_GPIO71 R259 1 2 10K_0402_5%

+3VS

EC_KBRST# R261 1 2 10K_0402_5%

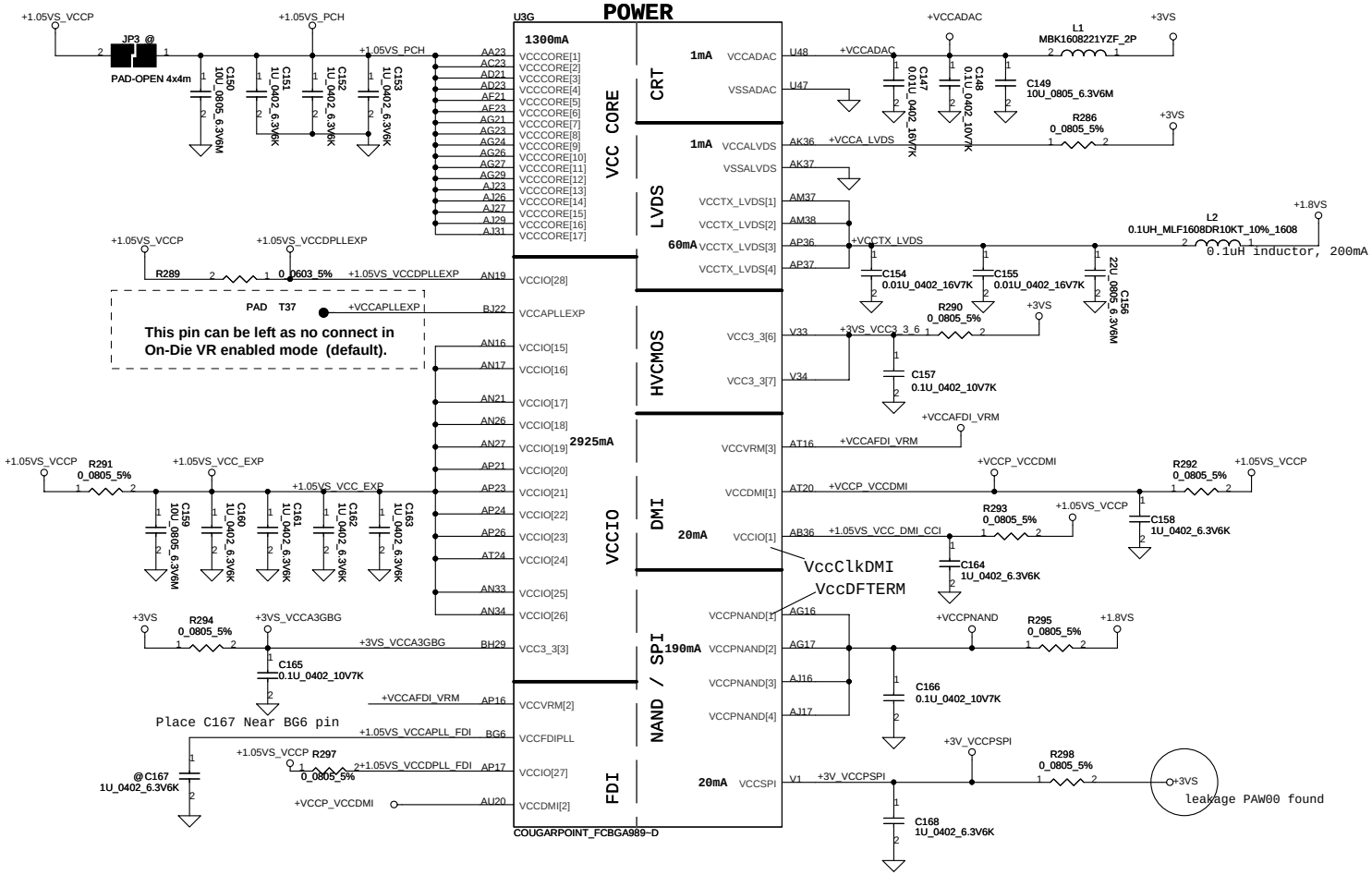
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

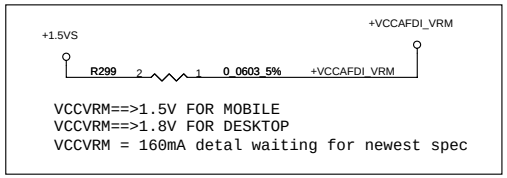
Title: SCHEMATIC,MB LA-A7121

Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 18 of 57



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



0 ohm for current test: delete when phase B

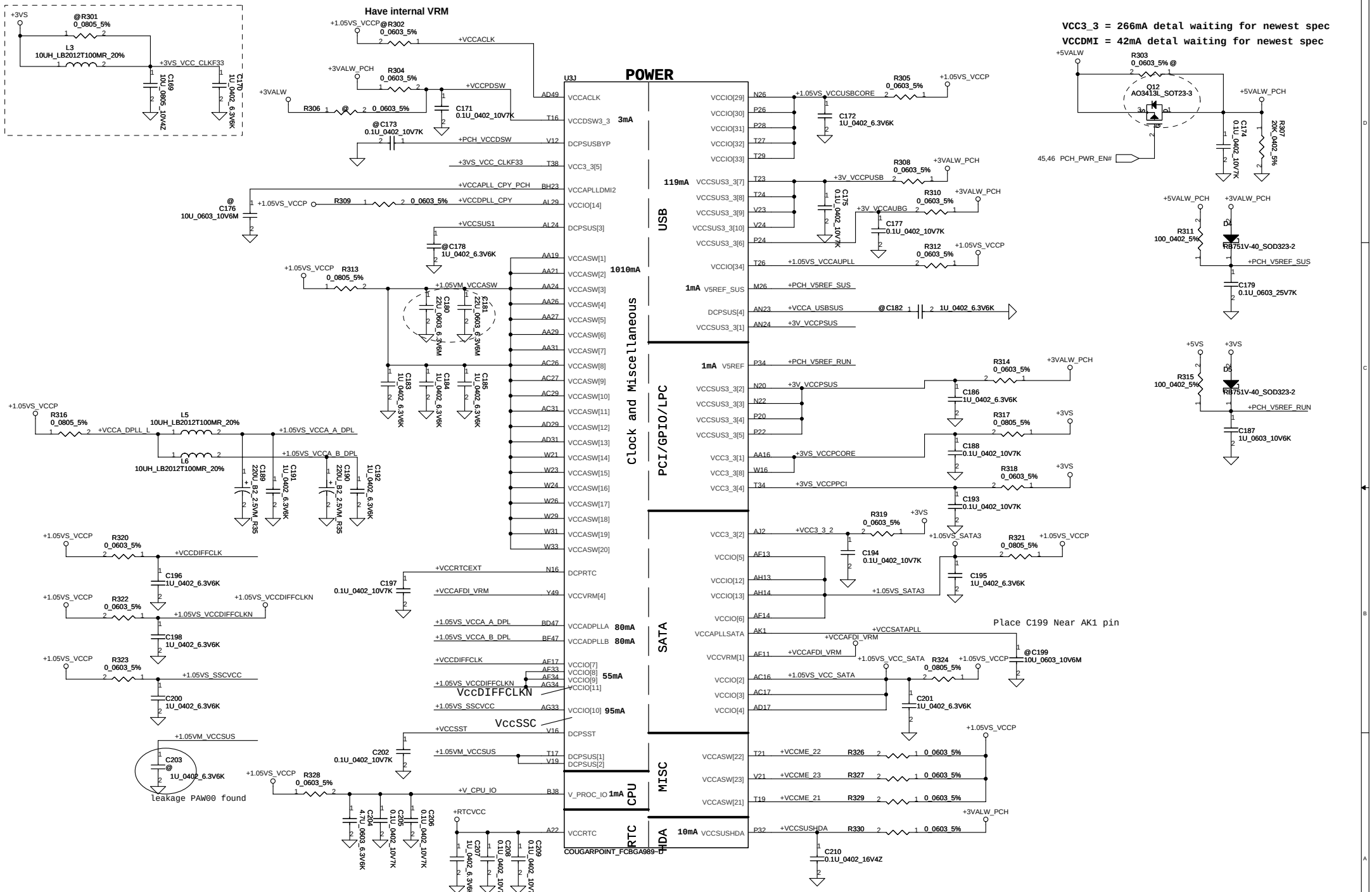
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

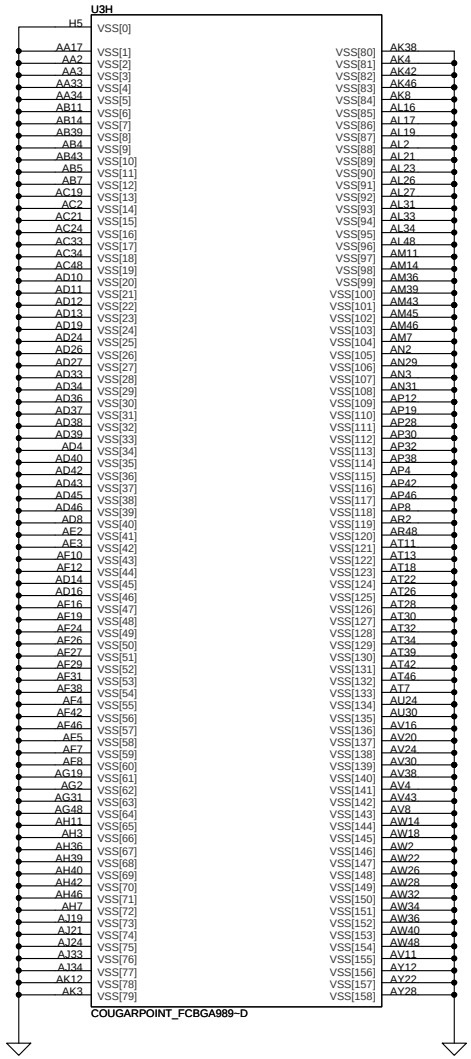
Size: Custom | Document Number: 4019BI | Rev: A

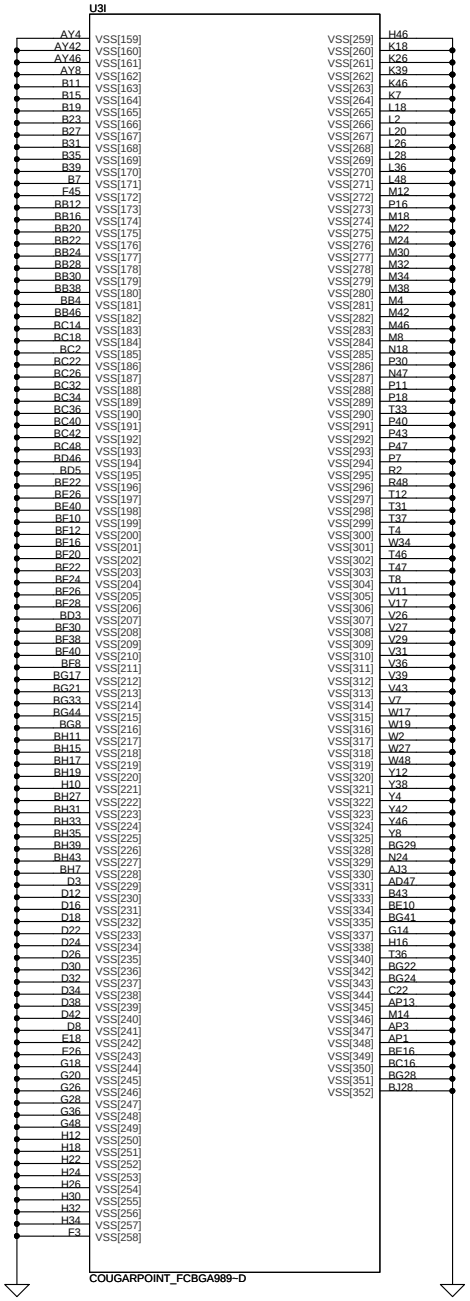
Date: Tuesday, December 14, 2010 | Sheet 19 of 57



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Title	*Compal Electronics, Inc.* **SCHEMATIC,MB LA-A7121**		
Size: Custom	Document Number: *4019BI*		Rev: A
Date: Tuesday, December 14, 2010	Sheet 20 of 57		





Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size	Document Number	Rev
Custom	4019BI	A

Date: Tuesday, December 14, 2010 Sheet 21 of 57

DG: 0.1u*4, 10u*1, bead 30 ohm

10/11 check ok

+1.05VS_DGPU → L1400 OPT@ BLM18PG330SN1D_2P → +PLLVDD

Layout note: Under GPU

150mA

0.1U_0402_16V4Z C1401 OPT@; 0.1U_0402_16V4Z C1402 OPT@; 0.1U_0402_16V4Z C1403 OPT@; 0.1U_0402_16V4Z C1404 OPT@; 0.1U_0402_16V4Z C1400 OPT@; 10U_0805_6.3V6M C1396 @; 4700P_0402_25V7K

10/5 JM50

4 PEG_HRX_GTX_N[0..15] — PEG_HRX_GTX_N[0..15]

4 PEG_HRX_GTX_P[0..15] — PEG_HRX_GTX_P[0..15]

4 PEG_HTX_C_GRX_N[0..15] — PEG_HTX_C_GRX_N[0..15]

4 PEG_HTX_C_GRX_P[0..15] — PEG_HTX_C_GRX_P[0..15]

PEG_HRX_GTX_P0	C1405	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P0	AL17
PEG_HRX_GTX_N0	C1406	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N0	AM17
PEG_HRX_GTX_P1	C1407	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P1	AM18
PEG_HRX_GTX_N1	C1408	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N1	AM19
PEG_HRX_GTX_P2	C1409	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P2	AL19
PEG_HRX_GTX_N2	C1410	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N2	AK19
PEG_HRX_GTX_P3	C1411	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P3	AL20
PEG_HRX_GTX_N3	C1412	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N3	AM20
PEG_HRX_GTX_P4	C1413	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P4	AM21
PEG_HRX_GTX_N4	C1414	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N4	AM22
PEG_HRX_GTX_P5	C1415	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P5	AL22
PEG_HRX_GTX_N5	C1416	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N5	AK22
PEG_HRX_GTX_P6	C1417	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P6	AL23
PEG_HRX_GTX_N6	C1418	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N6	AM23
PEG_HRX_GTX_P7	C1419	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P7	AM24
PEG_HRX_GTX_N7	C1420	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N7	AM25
PEG_HRX_GTX_P8	C1421	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P8	AL25
PEG_HRX_GTX_N8	C1422	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N8	AK25
PEG_HRX_GTX_P9	C1423	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P9	AL26
PEG_HRX_GTX_N9	C1424	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N9	AM26
PEG_HRX_GTX_P10	C1425	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P10	AM27
PEG_HRX_GTX_N10	C1426	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N10	AM28
PEG_HRX_GTX_P11	C1427	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P11	AL28
PEG_HRX_GTX_N11	C1428	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N11	AK28
PEG_HRX_GTX_P12	C1429	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P12	AK29
PEG_HRX_GTX_N12	C1430	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N12	AL29
PEG_HRX_GTX_P13	C1431	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P13	AM29
PEG_HRX_GTX_N13	C1432	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N13	AM30
PEG_HRX_GTX_P14	C1433	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P14	AM31
PEG_HRX_GTX_N14	C1434	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N14	AM32
PEG_HRX_GTX_P15	C1435	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_P15	AN32
PEG_HRX_GTX_N15	C1436	OPT@	.1U_0402_16V7K	PEG_HRX_C_GTX_N15	AP32

U1400A — Part 1 of 7

PCI EXPRESS DVO

PEG_HTX_C_GRX_P0	AP17	PEX_RX0	
PEG_HTX_C_GRX_N0	AN17	PEX_RX0_N	
PEG_HTX_C_GRX_P1	AN19	PEX_RX1	
PEG_HTX_C_GRX_N1	AP19	PEX_RX1_N	
PEG_HTX_C_GRX_P2	AR19	PEX_RX2	
PEG_HTX_C_GRX_N2	AR20	PEX_RX2_N	
PEG_HTX_C_GRX_P3	AP20	PEX_RX3	
PEG_HTX_C_GRX_N3	AN20	PEX_RX3_N	
PEG_HTX_C_GRX_P4	AN22	PEX_RX4	
PEG_HTX_C_GRX_N4	AP22	PEX_RX4_N	
PEG_HTX_C_GRX_P5	AR22	PEX_RX5	
PEG_HTX_C_GRX_N5	AR23	PEX_RX5_N	
PEG_HTX_C_GRX_P6	AP23	PEX_RX6	
PEG_HTX_C_GRX_N6	AN23	PEX_RX6_N	
PEG_HTX_C_GRX_P7	AN25	PEX_RX7	
PEG_HTX_C_GRX_N7	AP25	PEX_RX7_N	
PEG_HTX_C_GRX_P8	AR25	PEX_RX8	
PEG_HTX_C_GRX_N8	AR26	PEX_RX8_N	
PEG_HTX_C_GRX_P9	AP26	PEX_RX9	
PEG_HTX_C_GRX_N9	AN26	PEX_RX9_N	
PEG_HTX_C_GRX_P10	AN28	PEX_RX10	
PEG_HTX_C_GRX_N10	AP28	PEX_RX10_N	
PEG_HTX_C_GRX_P11	AR28	PEX_RX11	
PEG_HTX_C_GRX_N11	AR29	PEX_RX11_N	
PEG_HTX_C_GRX_P12	AP29	PEX_RX12	
PEG_HTX_C_GRX_N12	AN29	PEX_RX12_N	
PEG_HTX_C_GRX_P13	AN31	PEX_RX13	
PEG_HTX_C_GRX_N13	AP31	PEX_RX13_N	
PEG_HTX_C_GRX_P14	AR31	PEX_RX14	
PEG_HTX_C_GRX_N14	AR32	PEX_RX14_N	
PEG_HTX_C_GRX_P15	AR34	PEX_RX15	
PEG_HTX_C_GRX_N15	AP34	PEX_RX15_N	
		PEX_TX0	AL17
		PEX_TX0_N	AM17
		PEX_TX1	AM18
		PEX_TX1_N	AM19
		PEX_TX2	AL19
		PEX_TX2_N	AK19
		PEX_TX3	AL20
		PEX_TX3_N	AM20
		PEX_TX4	AM21
		PEX_TX4_N	AM22
		PEX_TX5	AL22
		PEX_TX5_N	AK22
		PEX_TX6	AL23
		PEX_TX6_N	AM23
		PEX_TX7	AM24
		PEX_TX7_N	AM25
		PEX_TX8	AL25
		PEX_TX8_N	AK25
		PEX_TX9	AL26
		PEX_TX9_N	AM26
		PEX_TX10	AM27
		PEX_TX10_N	AM28
		PEX_TX11	AL28
		PEX_TX11_N	AK28
		PEX_TX12	AK29
		PEX_TX12_N	AL29
		PEX_TX13	AM29
		PEX_TX13_N	AM30
		PEX_TX14	AM31
		PEX_TX14_N	AM32
		PEX_TX15	AN32
		PEX_TX15_N	AP32

GPIO

		GPIO0	K1
HPD_C		GPIO1	K2
		GPIO2	K3
		GPIO3	H3
		GPIO4	H2
GPU_VID0	→ GPU_VID0 55	GPIO5	H1
GPU_VID1	→ GPU_VID1 55	GPIO6	H4
	→ GPU_VID2 55	GPIO7	H5
OVERT# _VGA		GPIO8	H6
THERM# _VGA		GPIO9	J7
		GPIO10	K4
		GPIO11	K5
R1496 2 OPT@ 1 0_0402_5%		GPIO12	H7
		GPIO13	J4
		GPIO14	J6
		GPIO15	L1
		GPIO16	L2
		GPIO17	L4
R1497 2 @ 1 0_0402_5%		GPIO18	M4
		GPIO19	L7
		GPIO20	L5
		GPIO21	K6
		GPIO22	L6
		GPIO23	M6
		GPIO24	M7

Replace GPIO 12 with GPIO 18.
When : B stage platforms

No31

R1404 10K_0402_5% 2 OPT@ 1 — +3VSDGPU

Q1400 OPT@ 2N7002H_SOT23-3

NV_PERFORMANCE_R → NV_PERFORMANCE 41

HPD_C — R1401 OPT@ 100K_0402_5%

GPIO	I/O	FUNCTION
GPIO1	IN	HPD_C
GPIO5	OUT	GPU_VID0
GPIO6	OUT	GPU_VID1
GPIO7	OUT	GPU_VID2
GPIO8	IN	OVERT
GPIO9	IN	ALERT
GPIO12	IN	AC/DC detection
GPIO18	IN	Reserve for VPS

+3VSDGPU

VGA_EDID_CLK	R1405 OPT@	2.2K_0402_5%
VGA_EDID_DATA	R1406 OPT@	2.2K_0402_5%
SMB_CLK_GPU	R1407 OPT@	2.2K_0402_5%
SMB_DATA_GPU	R1408 OPT@	2.2K_0402_5%
THERM#_VGA	R1410 OPT@	100K_0402_5%
OVERT#_VGA	R1411 OPT@	10K_0402_5%
HDCP_SCL	R1412 OPT@	2.2K_0402_5%
HDCP_SDA	R1413 OPT@	2.2K_0402_5%
VGA_CRT_DATA	R1414 OPT@	2.2K_0402_5%
VGA_CRT_CLK	R1415 OPT@	2.2K_0402_5%
I2CB_SCL	R1416 OPT@	2.2K_0402_5%
I2CB_SDA	R1417 OPT@	2.2K_0402_5%

XTALIN — @R1419 22_0402_5% — @C1437 10P_0402_50V8J

Layout note: Reserve for EMI please close to UV1

14 CLK_PEG_VGA — CLK_PEG_VGA — AR16
14 CLK_PEG_VGA# — CLK_PEG_VGA# — AR17
PEG_CLKREQ# — AR13
PEX_REFCLK
PEX_REFCLK_N
PEX_CLKREQ_N

Layout note: Differential signal

R1421 200_0402_1% — PEX_TSTCLK_OUT — AJ17
PEX_TSTCLK_OUT#

PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N

17 PLTRST_VGA# — PLTRST_VGA# — AM16
AG21
PEX_RST_N
PEX_TERMP

R1400 OPT@ 2.49K_0402_1%

R1424 @ 10M_0402_5%

Y1400 OPT@ 27MHZ_16PF_X5H027000FG1H — XTALIN — XTAL_OUT

C1438 18P_0402_50V8J OPT@ — C1439 OPT@ 18P_0402_50V8J

+PLLVDD — *60mA* — AE9
45mA — AF9
45mA — AD9
PLLVDD
SP_PLLVDD
VID_PLLVDD

14 CLK_27M_TCLK — R1425 @ 22_0402_5% — XTALIN — B1
XTAL_OUT — B2
XTAL_IN
XTAL_OUT

R1426 OPT@ 10K_0402_5% — XTALOUT — D1
R1427 OPT@ 10K_0402_5% — XTALSSIN — D2
XTAL_OUTBUFF
XTAL_SSIN

CLK

MIOA_HSYNC_NC — N3
MIOA_VSYNC_NC — L3
MIOB_HSYNC_NC — W1
MIOB_VSYNC_NC — W2
MIOA_DE_NC — N2
MIOA_CTL3_NC — P5
MIOA_VREF_NC — N5
MIOB_DE_NC — Y5
MIOB_CTL3_NC — W3
MIOB_VREF_NC — AF1
MIOA_CLKIN_NC — N4
MIOA_CLKOUT_NC — R4
R1420 OPT@ 10K_0402_5%
MIOB_CLKIN_NC — AF1
MIOB_CLKOUT_NC — V4
R1422 OPT@ 10K_0402_5%
MIOA_CLKOUT_NC_N — T4
MIOB_CLKOUT_NC_N — W4
MIOACAL_PD_VDDQ_NC — U5
MIOACAL_PU_GND_NC — T5
MIOBCAL_PD_VDDQ_NC — AA7
MIOBCAL_PU_GND_NC — AA6

9/20

Diode at PCH

+3VSDGPU — R1428 OPT@ 10K_0402_5% — 14 PEG_CLKREQ# — PEG_CLKREQ#

DACA_RED — AM15
DACA_GREEN — AM14
DACA_BLUE — AL14
DACA_HSYNC — AM13
DACA_VSYNC — AL13
DACA_VDD — AJ12
DACA_VREF — AK12 — T1405
DACA_RSET — AK13 — T1406
R1516 10K_0402_5% OPT@
DACB_RED — AK4
DACB_GREEN — AL4
DACB_BLUE — AJ4
DACB_HSYNC — AM1
DACB_VSYNC — AM2
DACB_VDD — AG7
DACB_VREF — AK6 — T1408
DACB_RSET — AH7 — T1409
R1517 10K_0402_5% OPT@

10/11 NV: DACx-VDD 10K to GND, others NC

DACs

SMB_CLK_GPU — F2
SMB_DATA_GPU — F1
I2CS_SCL
I2CS_SDA
VGA_EDID_CLK — F3
VGA_EDID_DATA — F4
I2CC_SCL
I2CC_SDA
I2CB_SCL — G3
I2CB_SDA — G2
I2CB_SCL
I2CB_SDA
VGA_CRT_CLK — G1
VGA_CRT_DATA — G4
I2CA_SCL
I2CA_SDA
HDCP_SCL — F6
HDCP_SDA — G6
I2CH_SCL
I2CH_SDA

I2C

N12P-GS1-A1_BGA_973P — GS@

Note: Internal Thermal Sensor

+3VSDGPU — Q1401A 2N7002KDWH_SOT363-6 OPT@

SMB_CLK_GPU — EC_SMB_CK2 14,41

R1494 @ 0_0402_5%

check leakage

Q1401B 2N7002KDWH_SOT363-6 OPT@

SMB_DATA_GPU — EC_SMB_DA2 14,41

R1495 @ 0_0402_5%

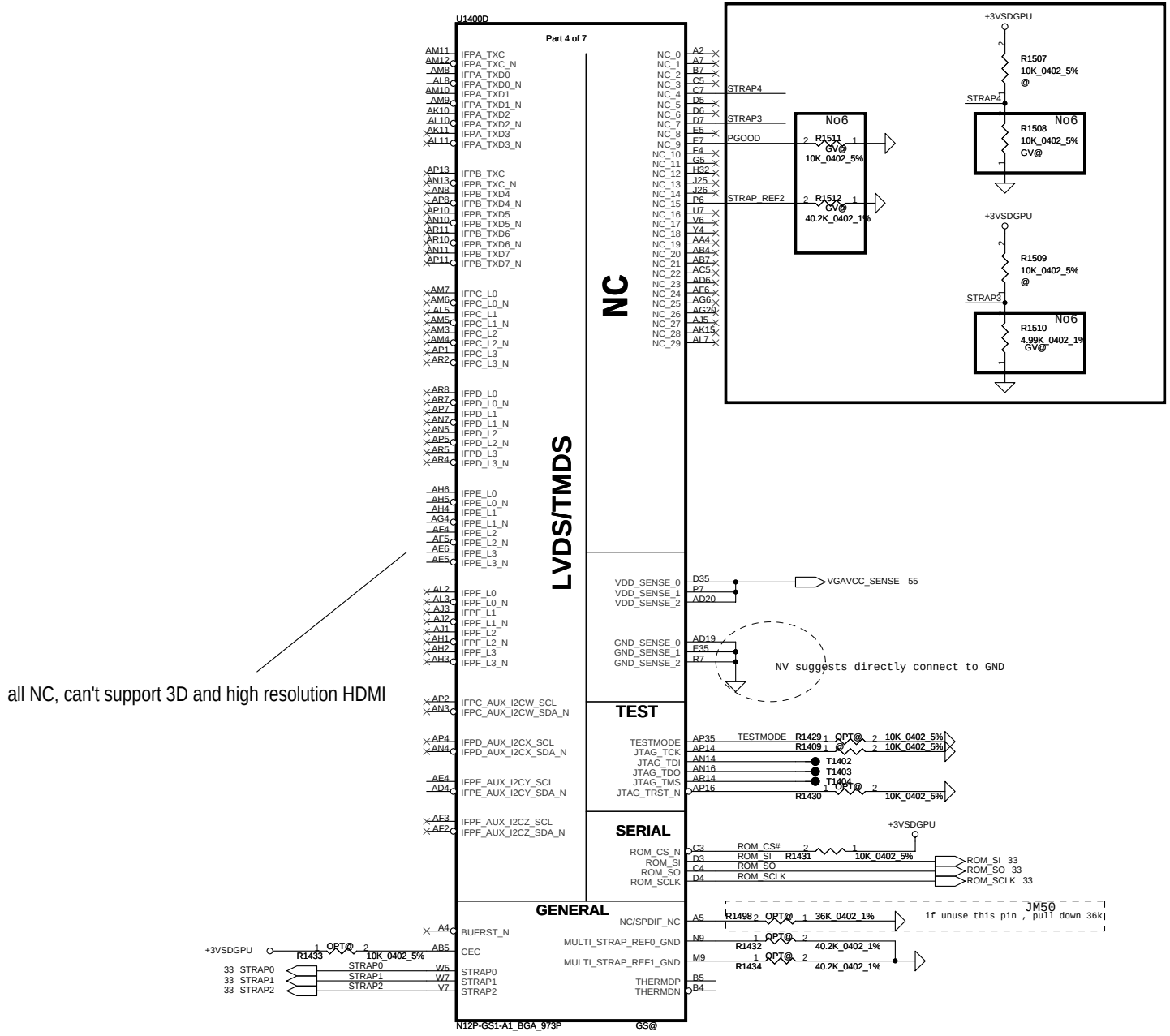
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size: — Document Number: 4019BI — Rev: A

Date: Tuesday, December 14, 2010 — Sheet 22 of 57



all NC, can't support 3D and high resolution HDMI

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 23 of 57

For PHQAA EVT Phase only

Mode	VID1	VID0	+VGA_CORE
P0(Cold)	1	1	0.95 V
P0	0	1	0.950V
P8/P12	0	0	0.825 V

N12M-GE Performance Mode

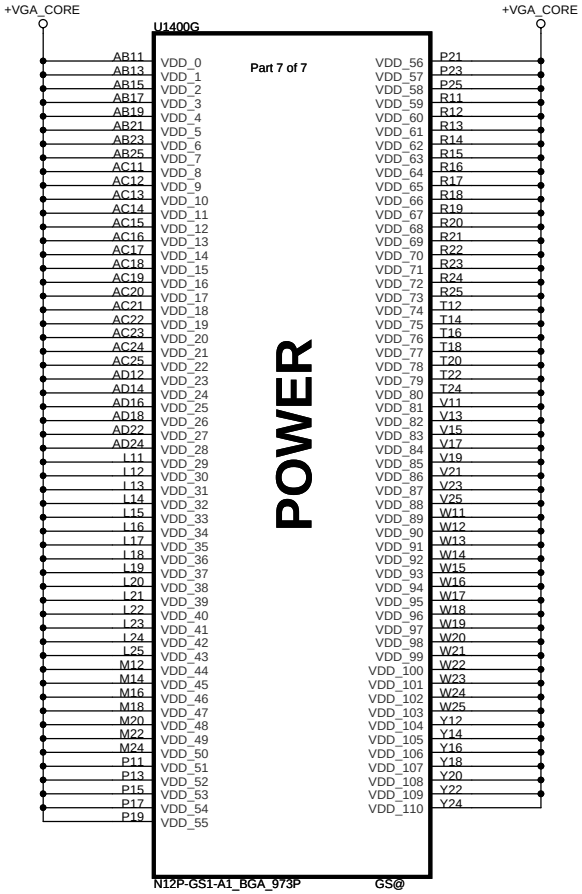
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	606	790	1.00 V
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

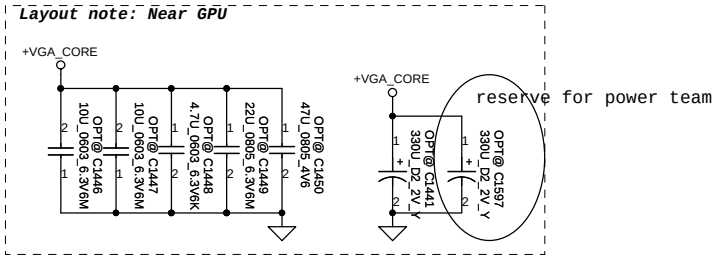
N12P-GS Performance Mode

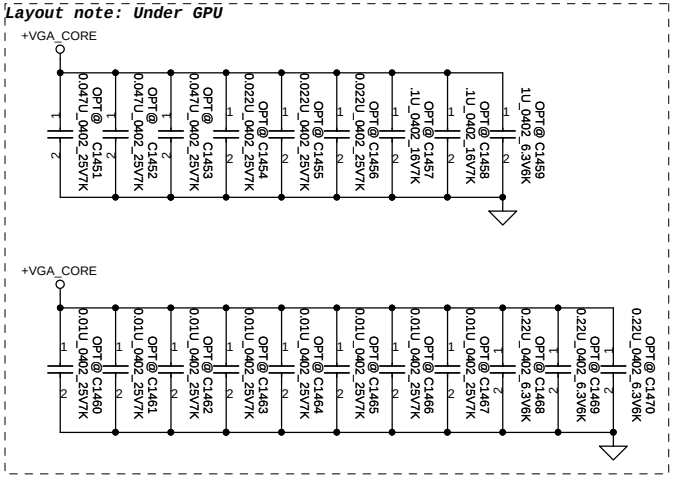
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

N12P-GE Performance Mode

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD







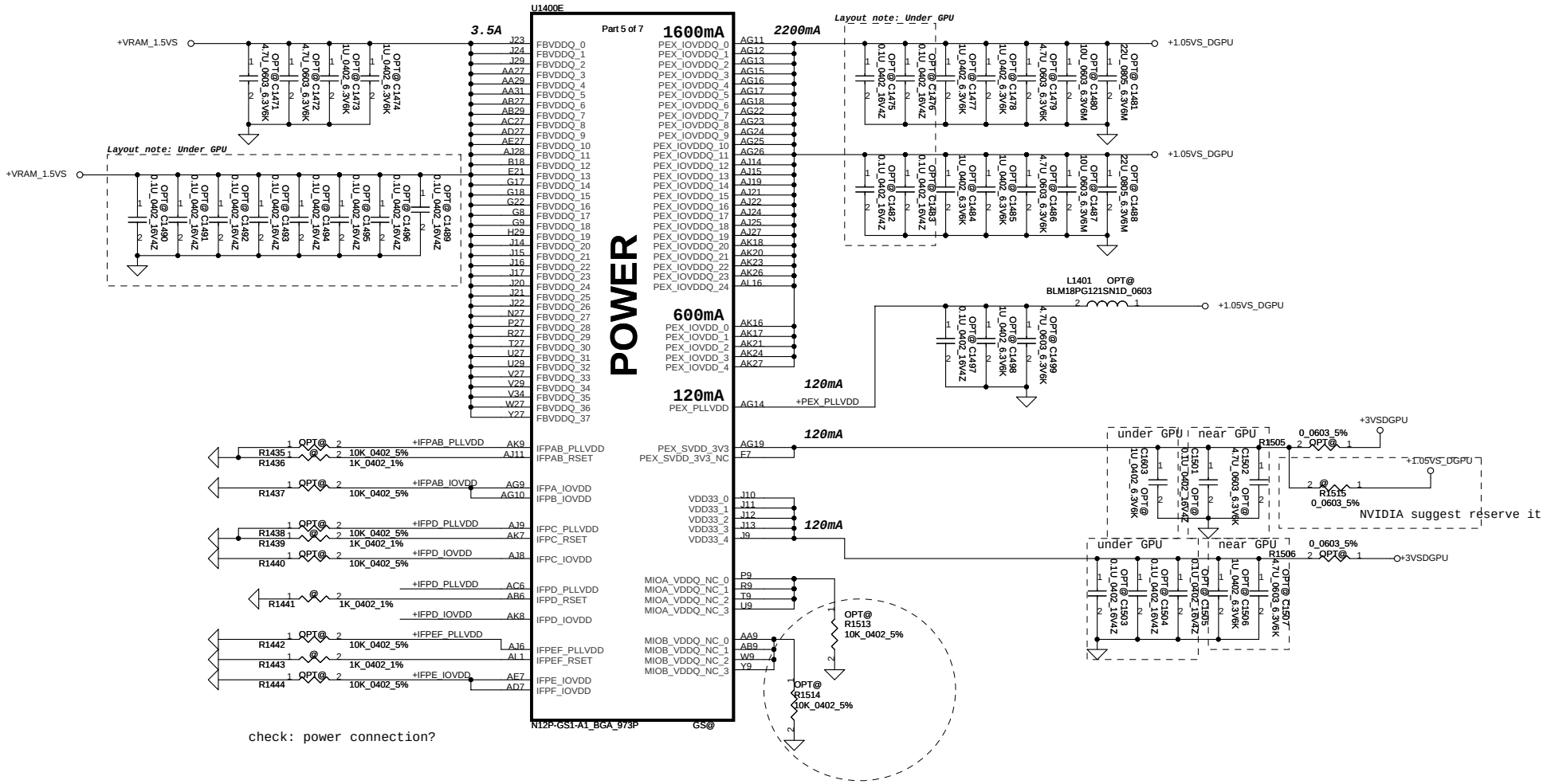
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 24 of 57



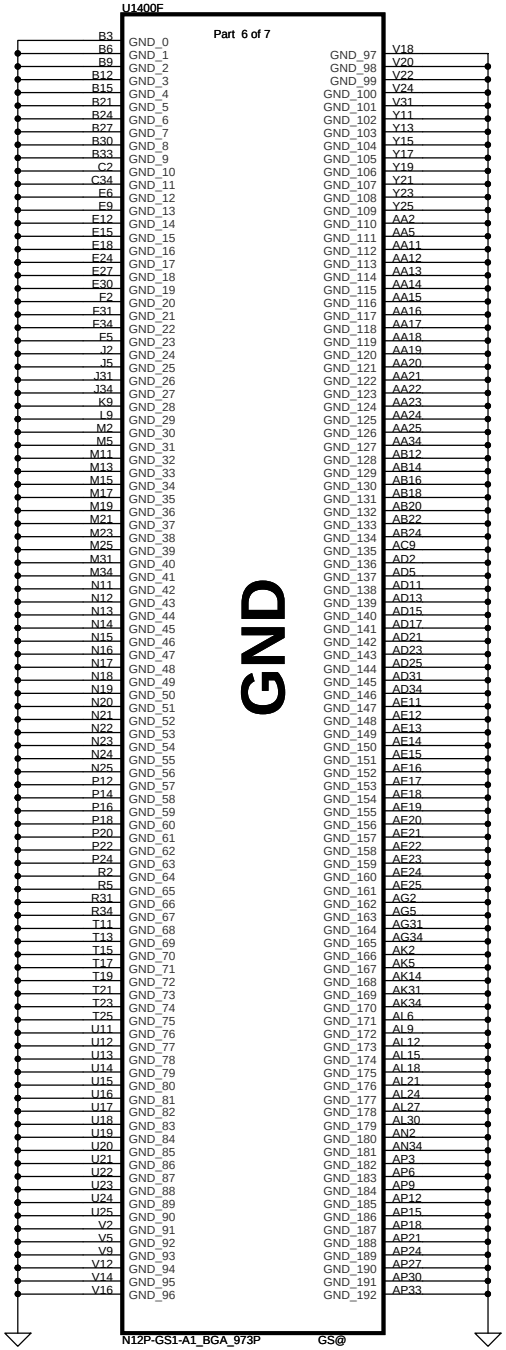
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size	Document Number	Rev
	4019BI	A

Date: Tuesday, December 14, 2010 Sheet 25 of 57



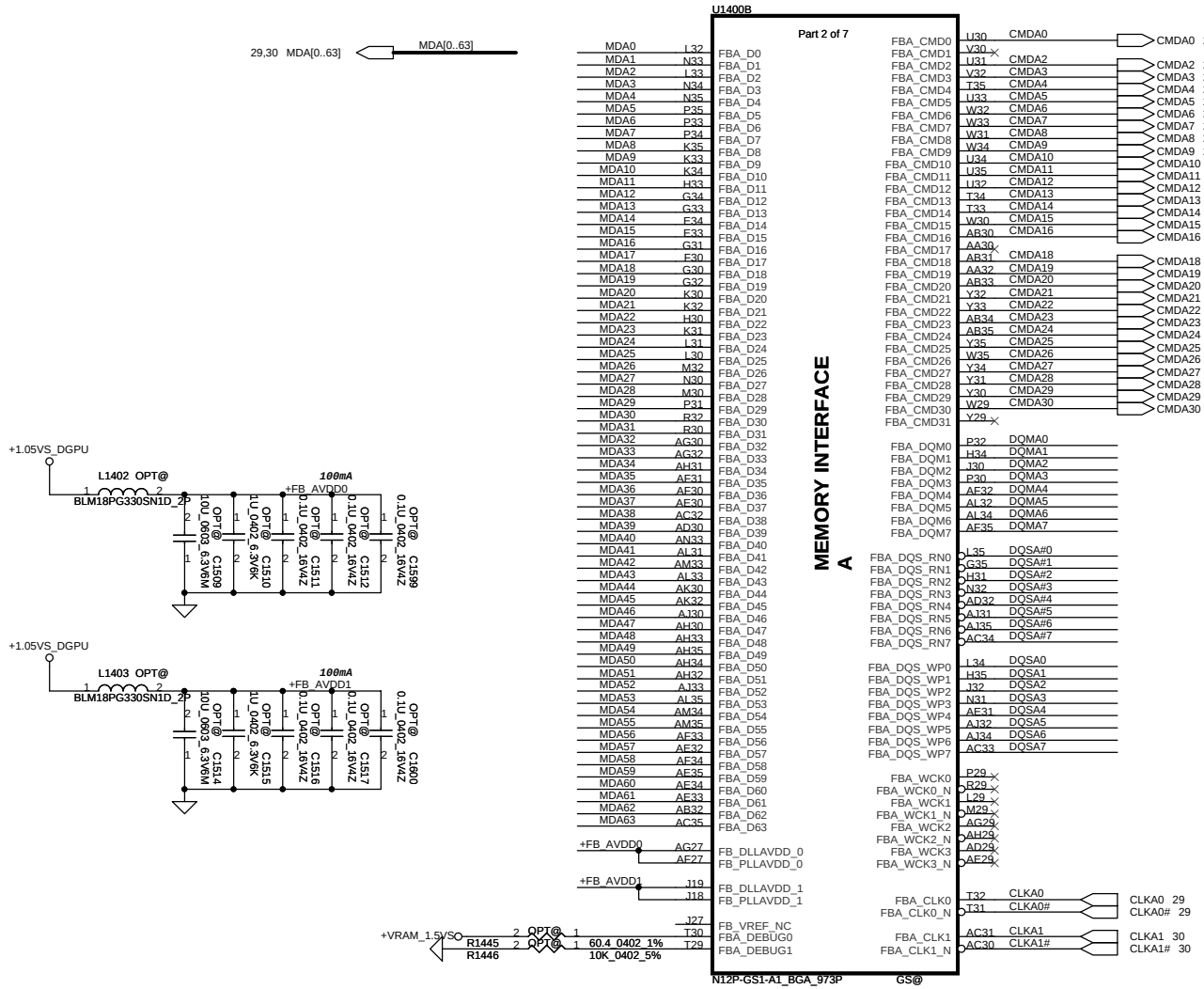
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **SCHEMATIC,MB LA-A7121**

Size	Document Number	Rev
	4019BI	A

Date: Tuesday, December 14, 2010 | Sheet 26 of 57



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

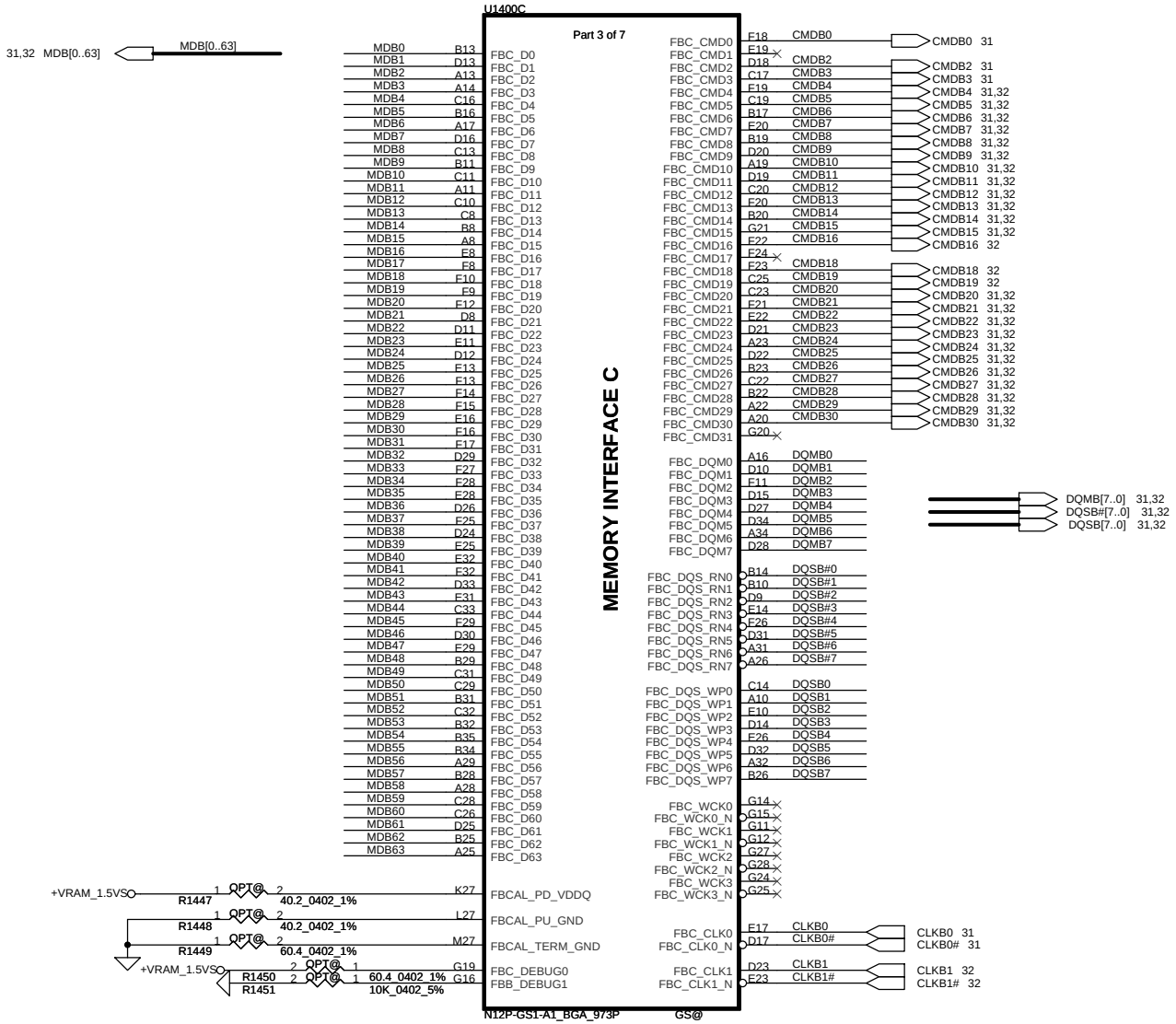
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **SCHEMATIC,MB LA-A7121**

Size | Document Number: **4019BI** | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 27 of 57



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

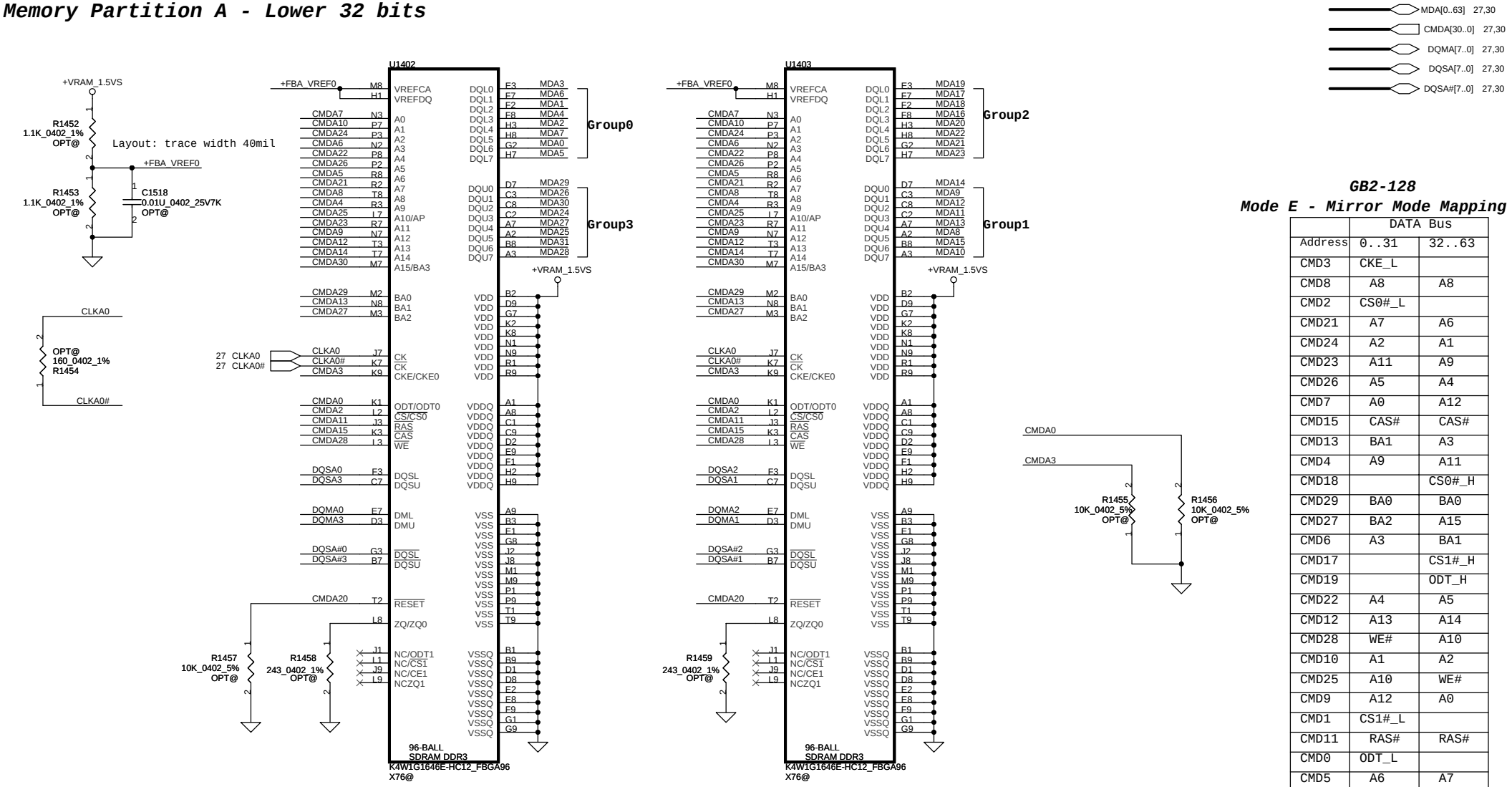
Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 28 of 57

Memory Partition A - Lower 32 bits



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

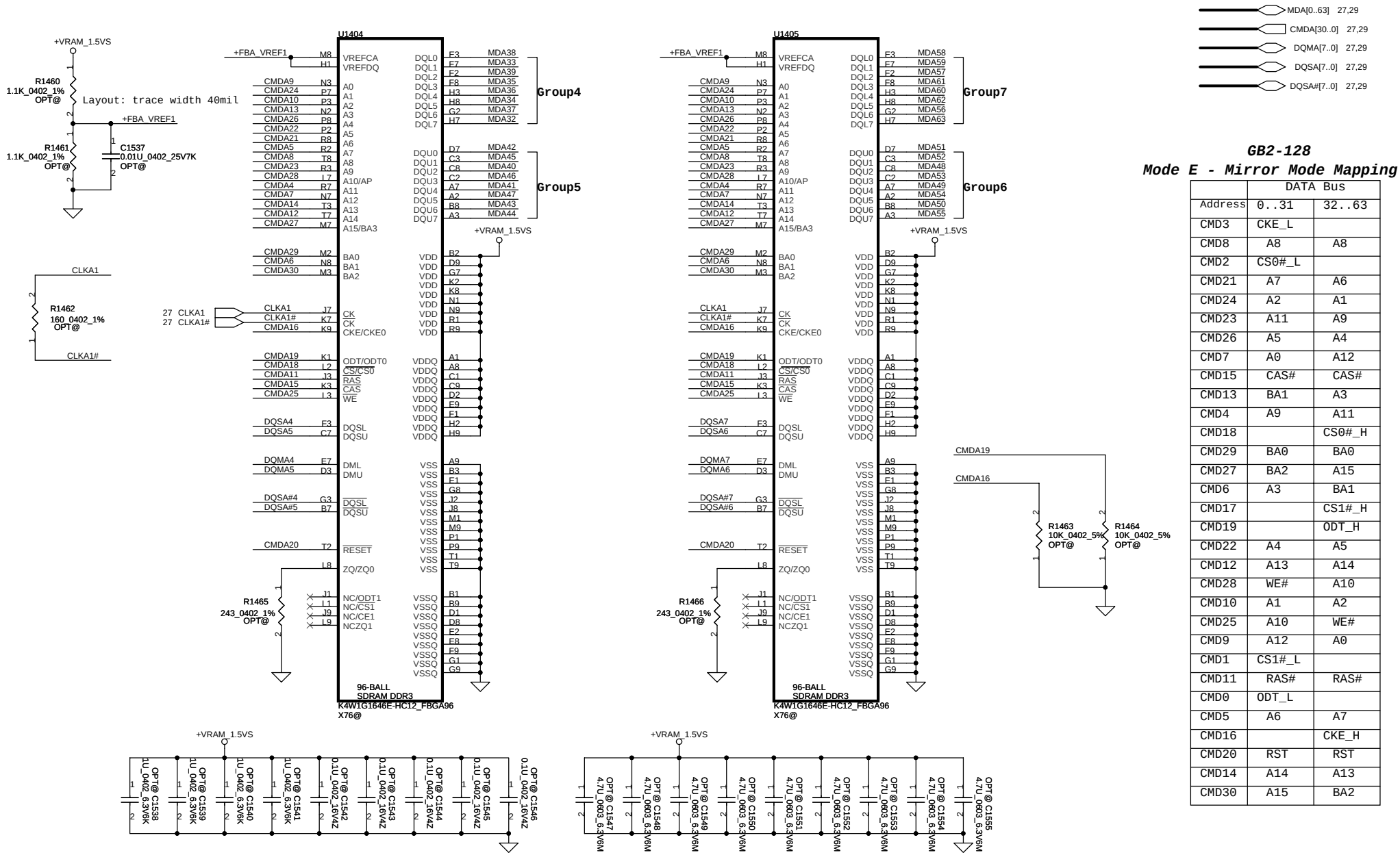
Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 29 of 57

Memory Partition A - Upper 32 bits



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

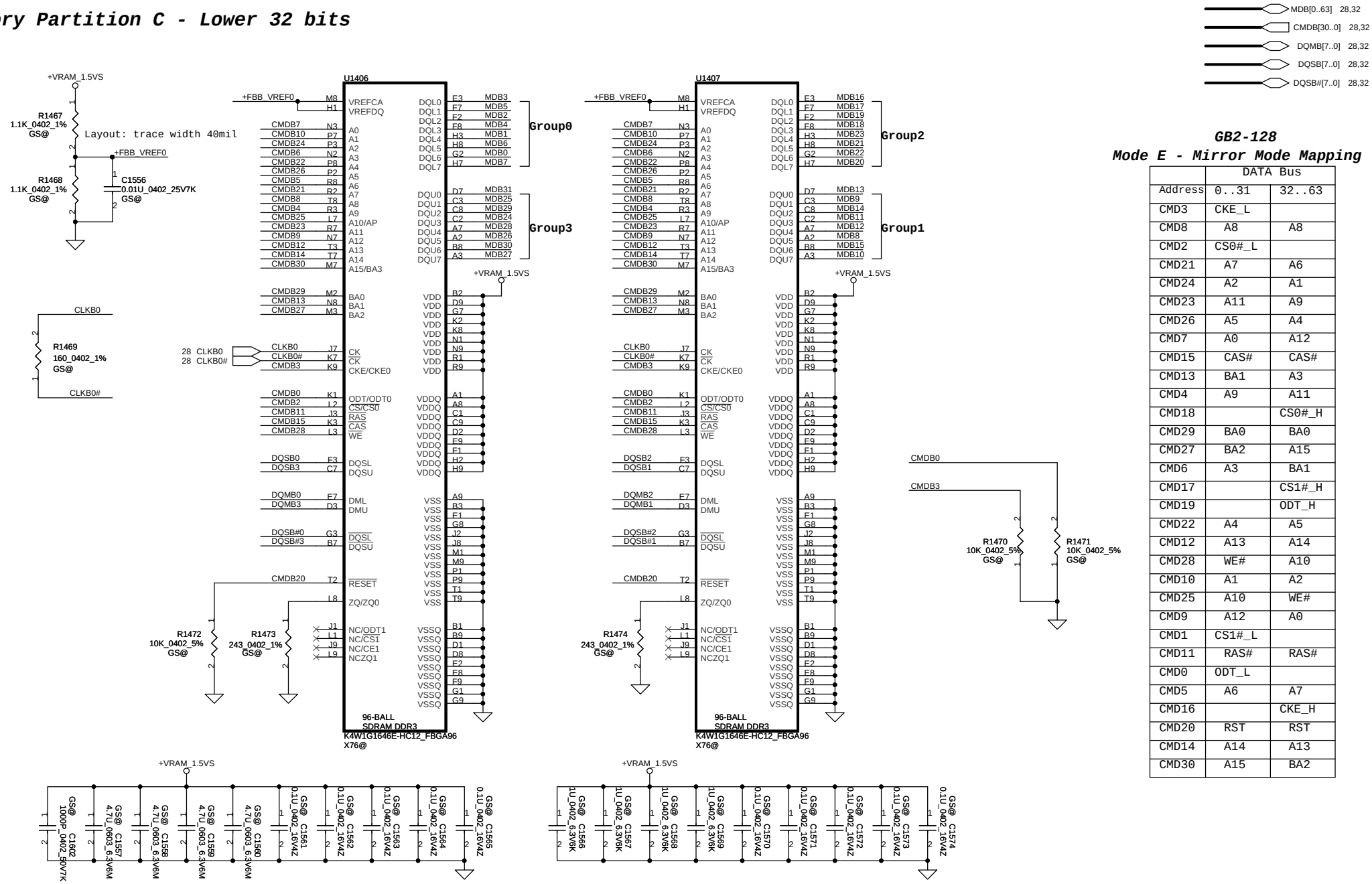
Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 30 of 57

Memory Partition C - Lower 32 bits



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

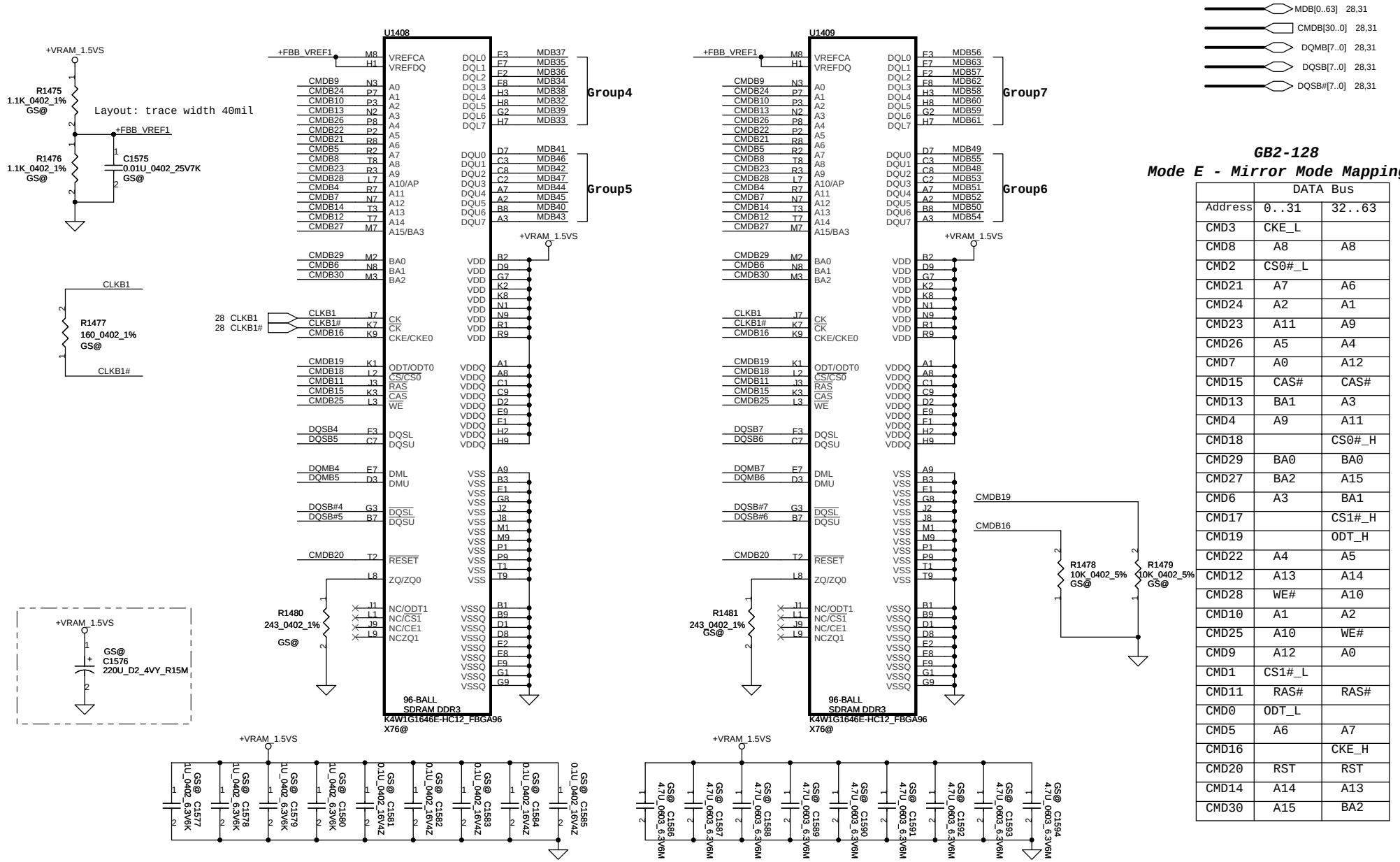
Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 31 of 57

Memory Partition C - Upper 32 bits



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

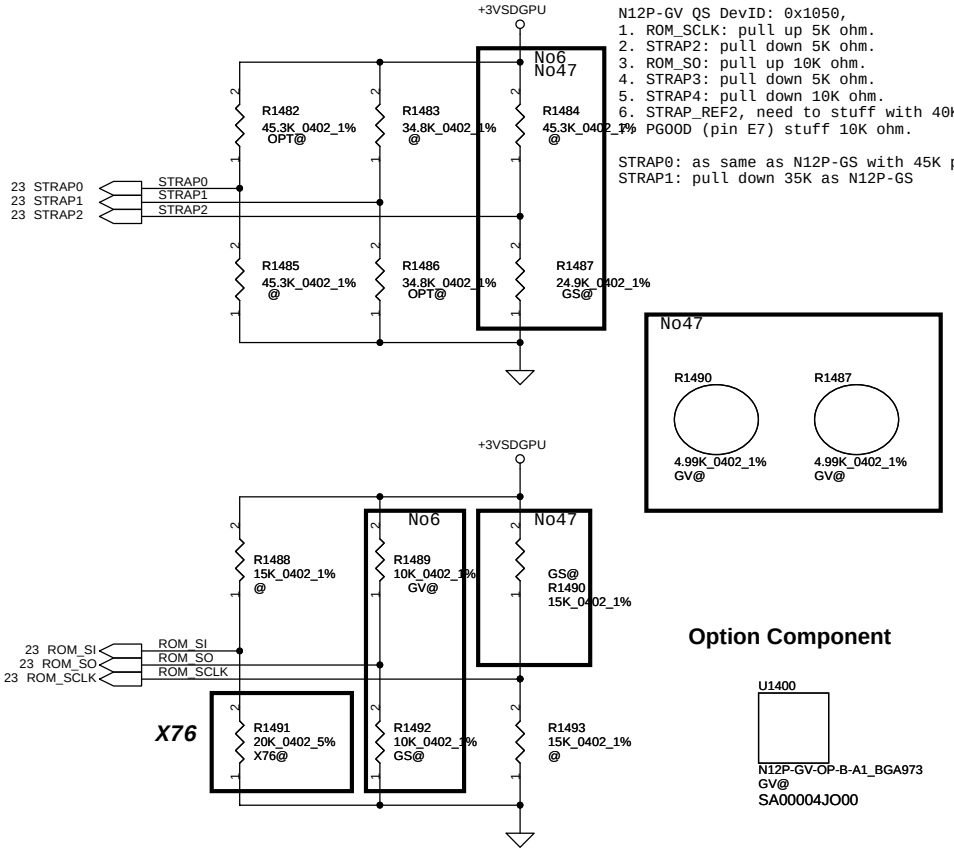
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 32 of 57



GS:

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

GV:
GB1b-64

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

N11P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	L 35K	L GV@ GS@ L	L 20K	L 10K	H 15K
64MX16 Hynix SA000032400	H 45K	L 35K	GV@ GS@	L 15K	L 10K	H 15K
128MX16 Samsung	H 45K	L 35K	L GS@	L 45K	L 10K	H 15K
128MX16 Hynix SA00003VS10	H 45K	L 35K	L GS@	L 35K	L 10K	H 15K

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K
N12P-GV	0x1050	Pull up 5K	pull down 5K

Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S40	512MB	0010	PD 15K (SD034150280)
	1GB	0010	PD 15K (SD034150280)
Hynix 2G No2 No44 128MX16 H5TQ2G63BFR-12C SA00003YO20	2GB	0110	PD 34.8k(SD034348280)
Samsung (900MHZ) 64MX16 K4W1G1646G-BC11 SA00004GS10	512MB	0011	PD 20K (SD034200280)
	1GB	0011	PD 20K (SD034200280)
Samsung 2G 128M16 K4W2G1646C-HC12 SA000047Q20	2GB	0111	PD 45.3K(SD034453280)

No1
No44

XCLK_417	
0	277MHz (Default)
1	Reserved

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

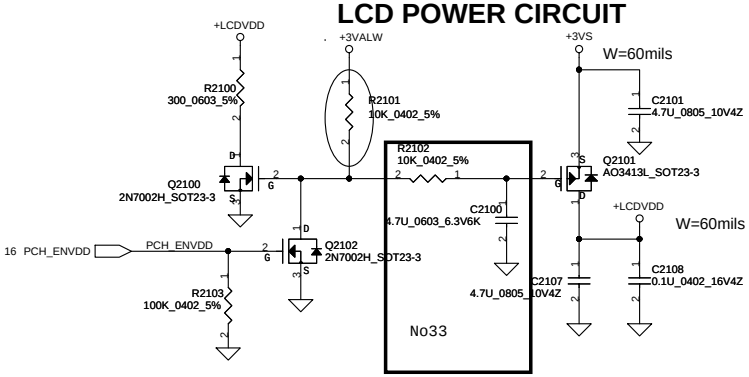
Compal Electronics, Inc.

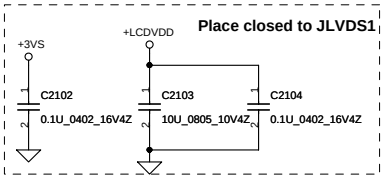
Title: SCHEMATIC,MB LA-A7121

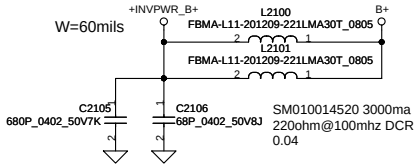
Size: Custom | Document Number: 4019BI | Rev: A

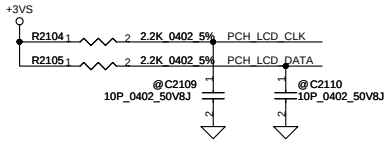
Date: Tuesday, December 14, 2010 | Sheet 33 of 57

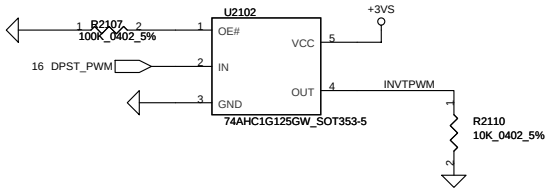
LCD POWER CIRCUIT

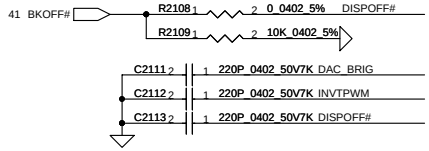






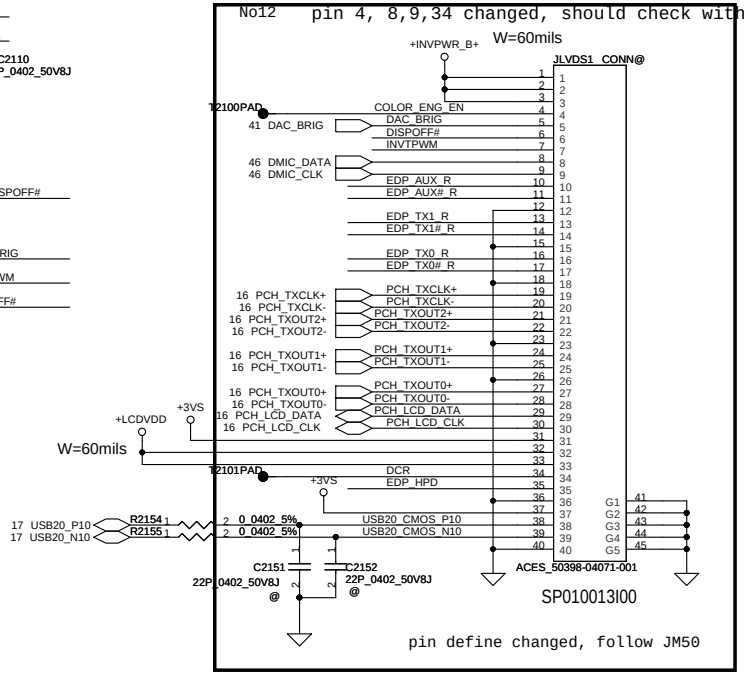


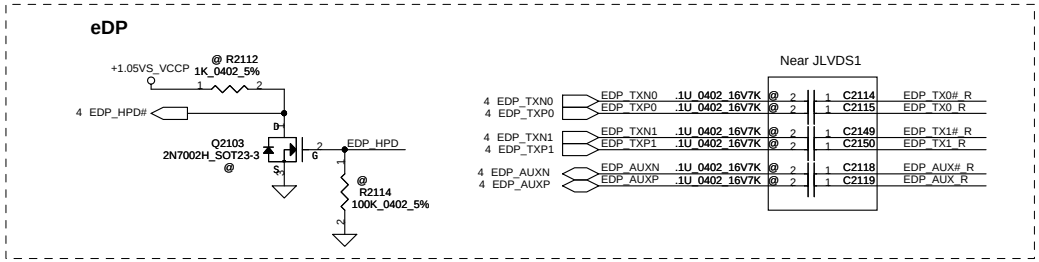


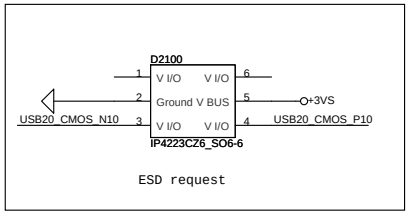


LCD/LED PANEL Conn.

No12 pin 4, 8,9,34 changed, should check with JM40/50







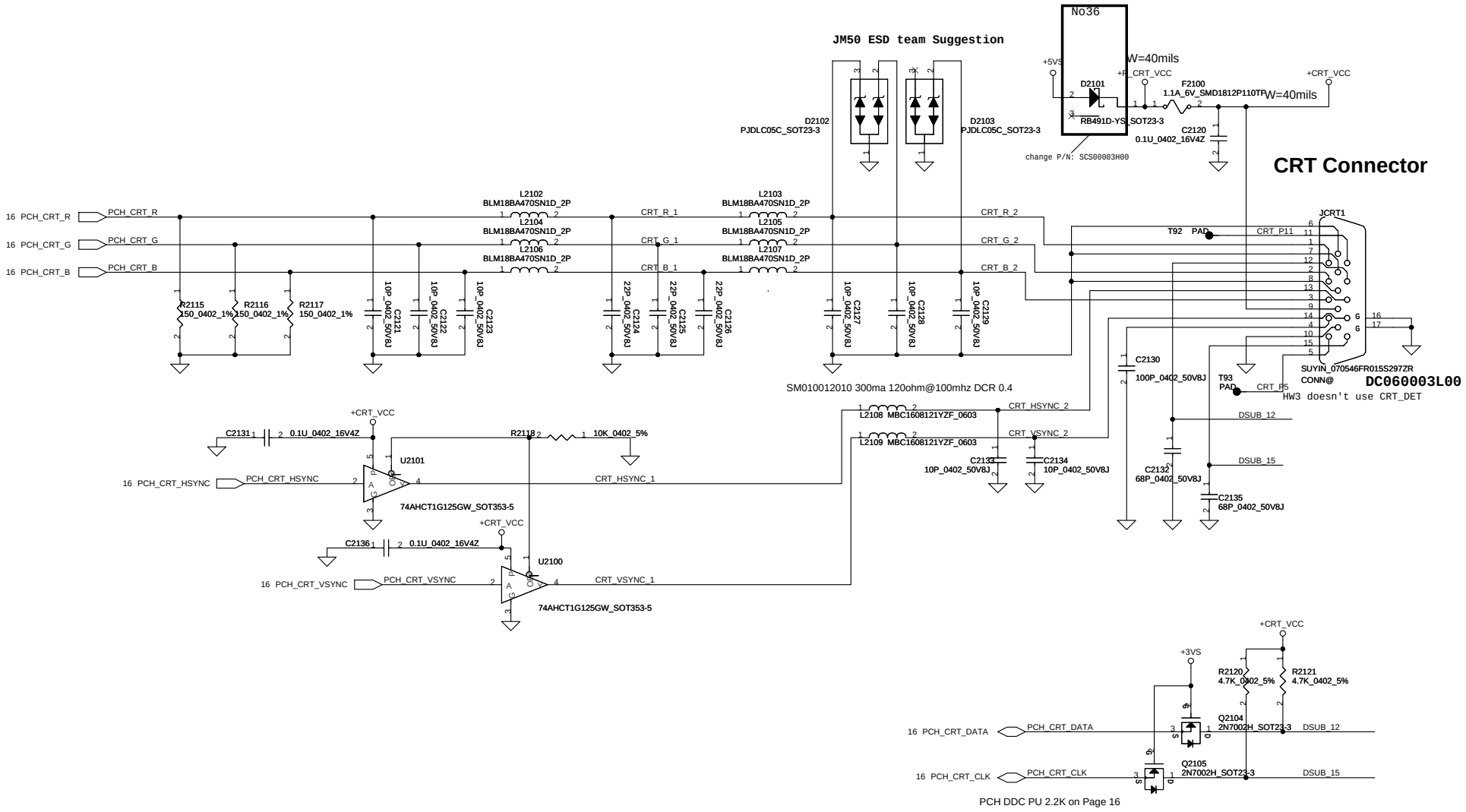
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

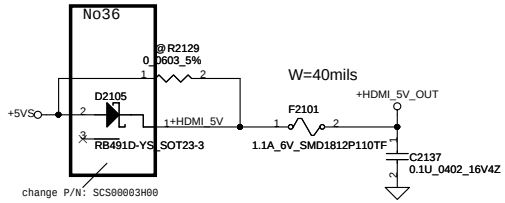
Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 34 of 57

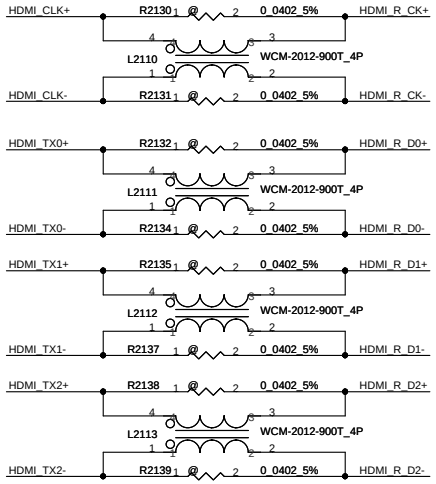


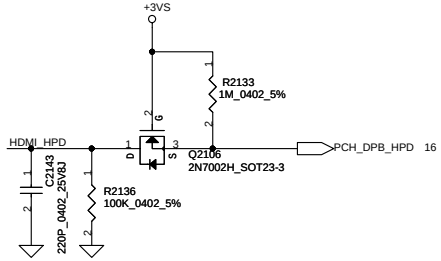
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.	
Title	SCHEMATIC,MB LA-A7121
Size: Custom	Document Number: 4019BI
Rev	A
Date: Tuesday, December 14, 2010	Sheet 35 of 57

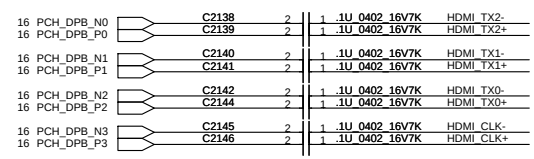


ESD request
Common mode choke 90ohm on these singals
Compal PN: SM070000K00
Vendor PN: WCM-2012-900T





UMA

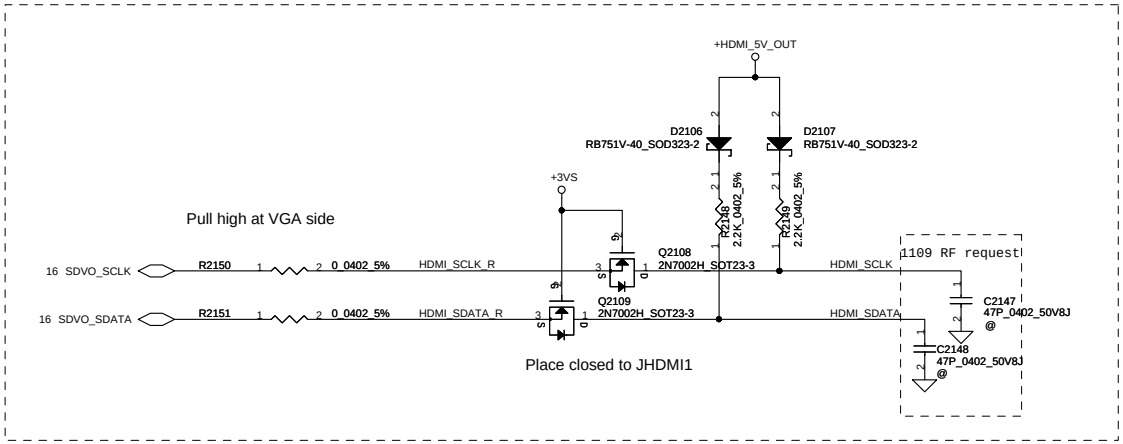


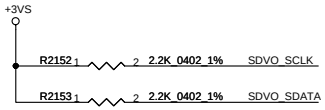
DIS

Not reserved

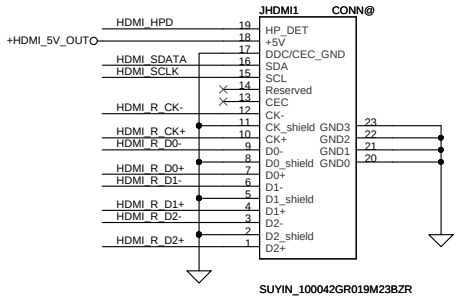
NVIDA Recommand 05/10

Not reserved



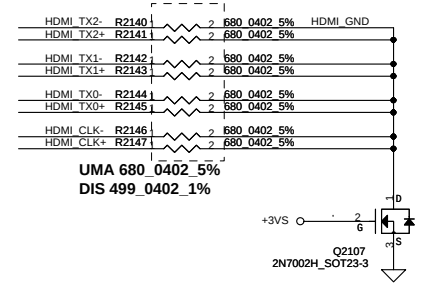


HDMI connector



SUYIN_100042GR019M23BZR
DC232001100

From layout request, change footprint
SUYIN_100042GR019M23BZR_19P-S



UMA 680_0402_5%
DIS 499_0402_1%

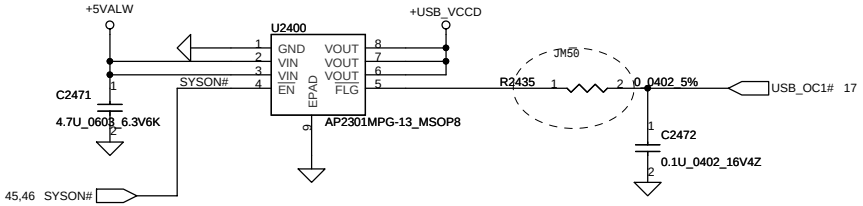
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/12/31

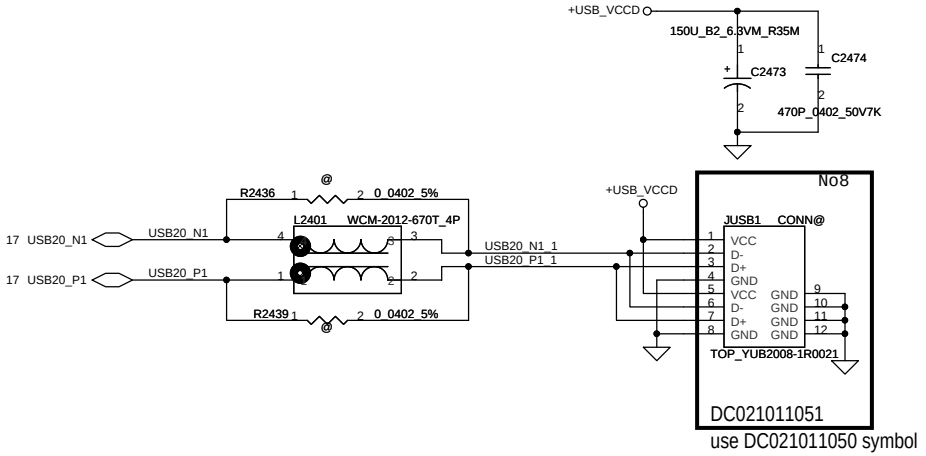
Compal Electronics, Inc.

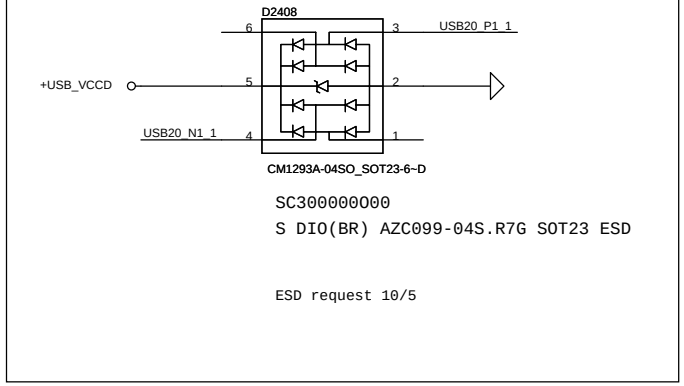
Title: SCHEMATIC,MB LA-A7121

Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 36 of 57







SC300000O00
S DIO(BR) AZC099-04S.R7G SOT23 ESD

ESD request 10/5

No15

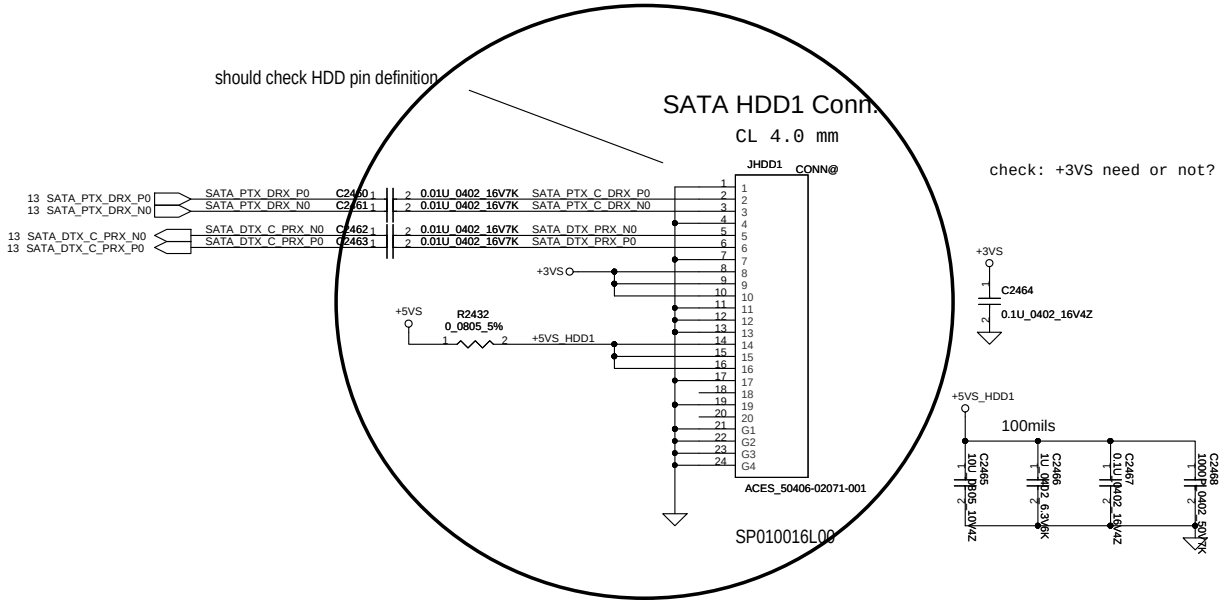
Security Classification	Compal Secret Data		
Issued Date	2009/12/4	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size	Document Number	Rev
Custom	4019BI	A

Date: Tuesday, December 14, 2010 Sheet 37 of 57



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/12/31

Compal Electronics, Inc.

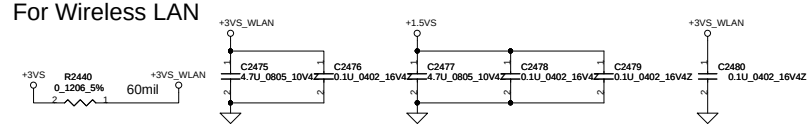
Title: SCHEMATIC,MB LA-A7121

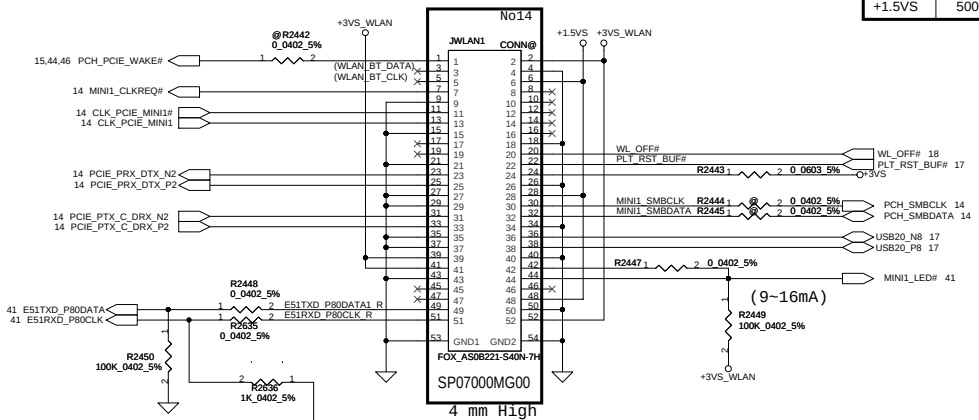
Size	Document Number	Rev
Custom	4019BI	A

Date: Tuesday, December 14, 2010 Sheet 38 of 57

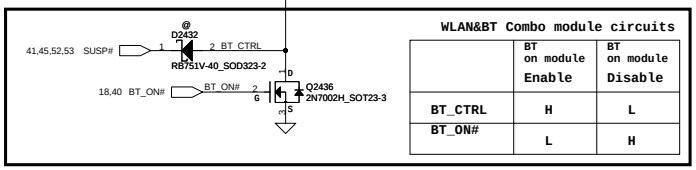
For Wireless LAN

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



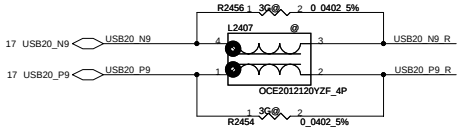


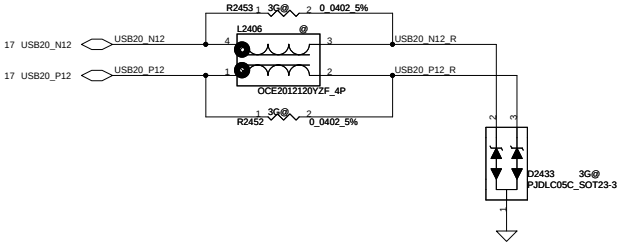
WLAN&BT Combo module circuits

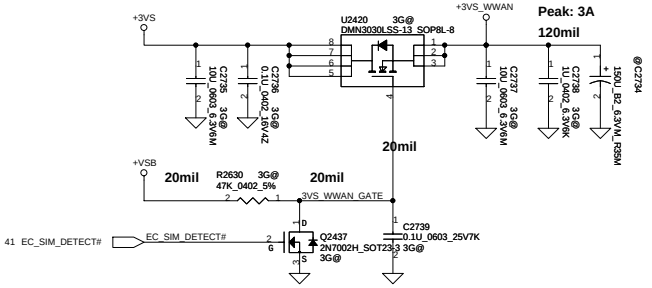


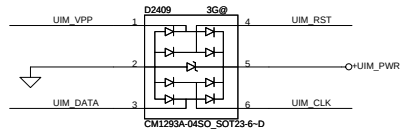
	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

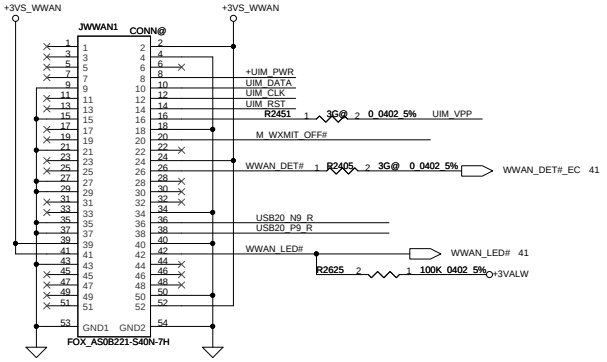
WWAN

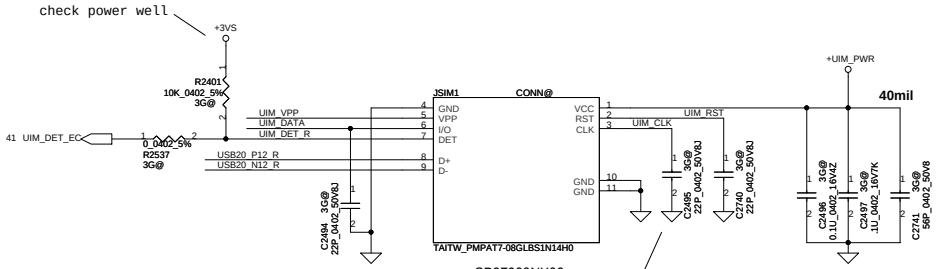












Place as close as JSIM1

DET signal, normal Close, connect to GND.

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/12/31

Compal Electronics, Inc.

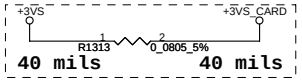
Title: SCHEMATIC,MB LA-A7121

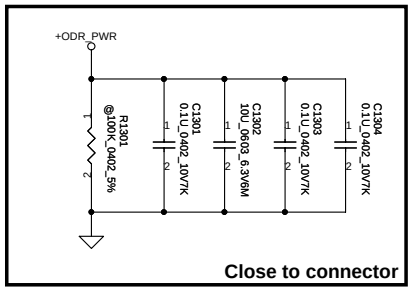
Size	Document Number	Rev
C	4019BI	A

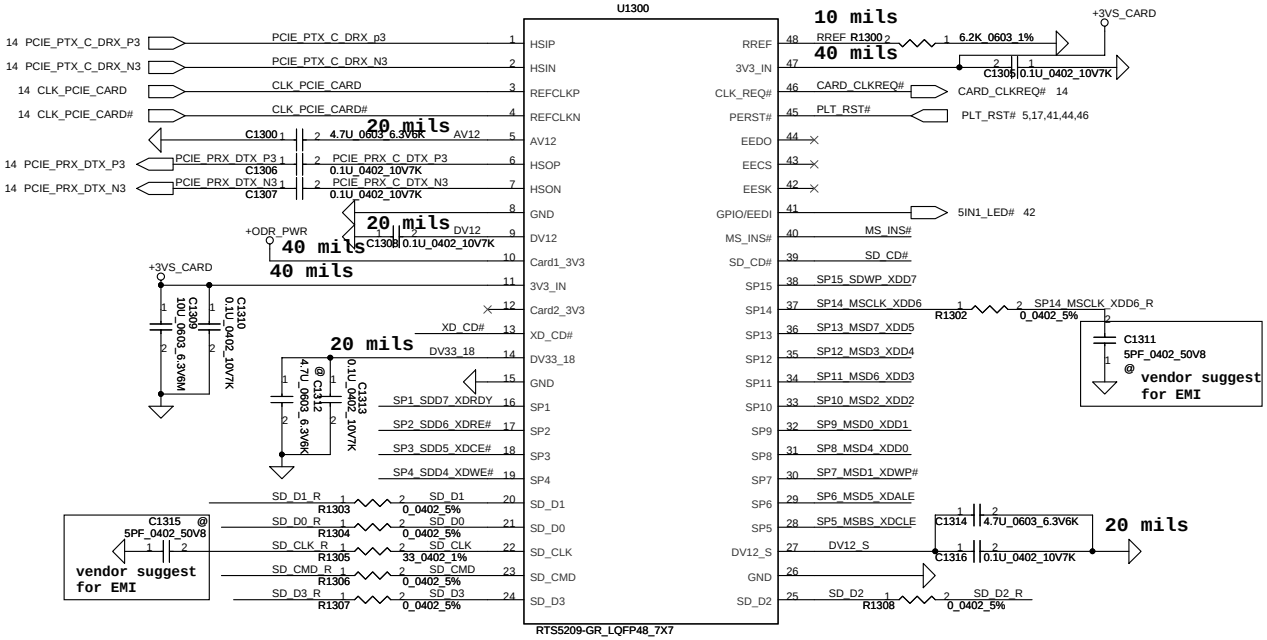
Date: Tuesday, December 14, 2010 | Sheet 39 of 57

Card Reader

No 41, for measurement

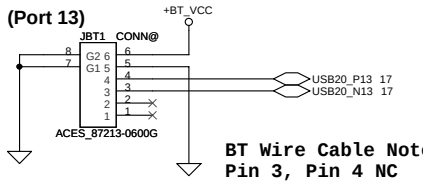




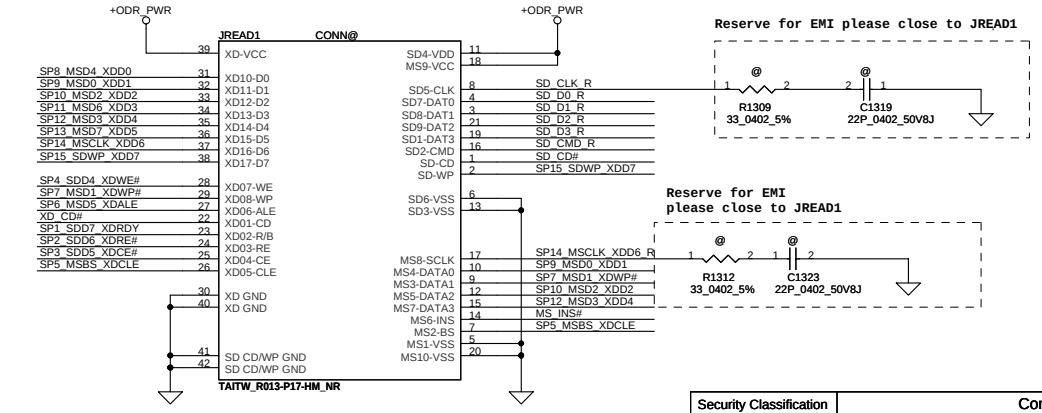


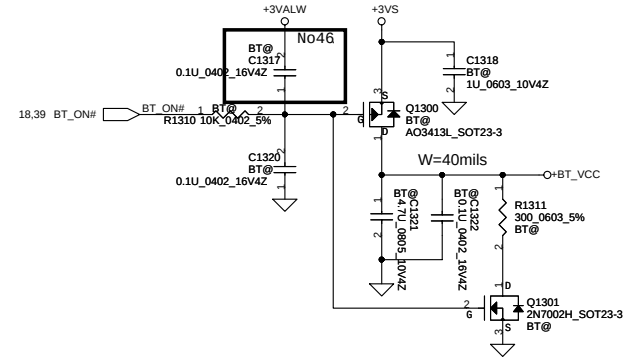
BT Conn.

(Port 13)



SP02000FR00





DC021010041 10/5

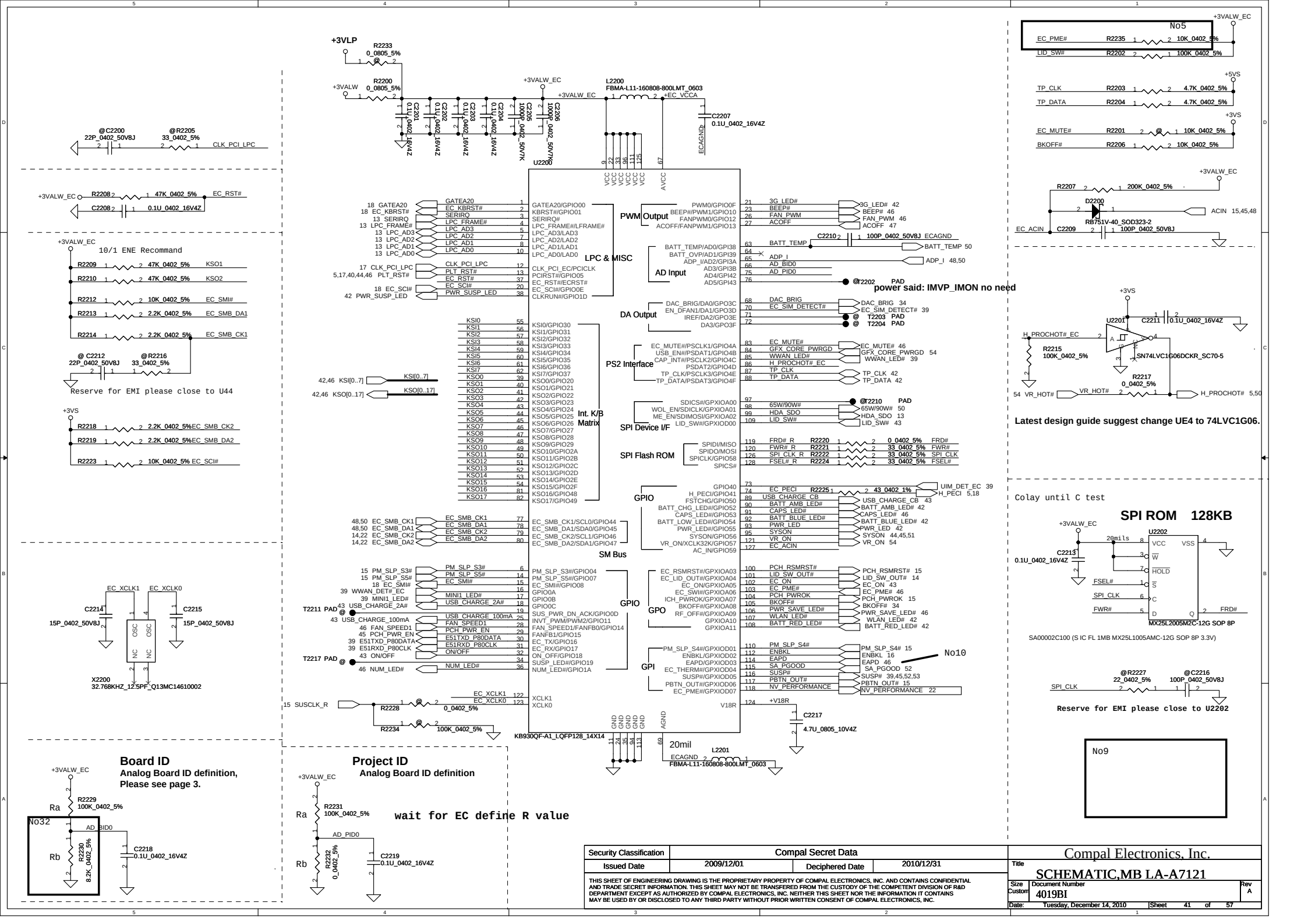
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 40 of 57



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size	Document Number	Rev
Custom	4019BI	A

Date: Tuesday, December 14, 2010 Sheet 41 of 57

Follow JM50

(Left) JKB1 CONN@

KSO0 1, KSO1 2, KSO2 3, KSO3 4, KSO4 5, KSO5 6, KSO6 7, KSO7 8, KSO8 9, KSO9 10, KSO10 11, KSO11 12, KSO12 13, KSO13 14, KSO14 15, KSO15 16, KSO16 17, KSO17 18, KSI0 19, KSI1 20, KSI2 21, KSI3 22, KSI4 23, KSI5 24, KSI6 25, KSI7 26

G1 27, G2 28

ACES_85201-26051

(Right)

10/04 Check footprint ok

SP01000GE00

KSI[0..7] KSI[0..7] 41,46

KSO[0..17] KSO[0..17] 41,46

KSO7	C2503	KSO6	C2505	KSO5	C2507	KSO4	C2509
KSO3	C2511	KSI4	C2513	KSO2	C2515	KSO1	C2517
KSO0	C2519	KSI5	C2521	KSI6	C2523	KSI7	C2525
KSO16	C2499	KSO17	C2502	KSO15	C2504	KSO14	C2506
KSO13	C2508	KSO12	C2510	KSI0	C2512	KSO11	C2514
KSO10	C2516	KSI1	C2518	KSI2	C2520	KSO9	C2522
KSI3	C2524	KSO8	C2526				

All: 100P_0402_50V8J

To TP/B Conn.

No11

+5VS, C2498 0.1U_0402_16V4Z

JTP1 CONN@

1 GND, 2 GND

ACES_85201-06051

TP_CLK 41, TP_DATA 41, LEFT_BTN#, RIGHT_BTN#

@C2500 100P_0402_50V8J, @C2501 100P_0402_50V8J

SP01000LB00

TP_CLK, TP_DATA, LEFT_BTN#, RIGHT_BTN#

D2410 PJSOT05C_SOT23-3, D2411 PJSOT05C_SOT23-3

ESD request

LEFT_BTN# SW2400 EVQPLHA15_4P

RIGHT_BTN# SW2401 EVQPLHA15_4P

Should Check LED, not the correct P/N

LED

3G/Wireless LED

+3VS

R2459 2.2K_0402_5%

R2460 3.9K_0402_5%

LED1

3G_LED# 3G_LED# 41

WLAN_LED# WLAN_LED# 41

HT-297UD5-CB5_AMBER-BLUE

Battery

Top View LED with Blue/Amber/Red Color

pin1,2 LED1 short wave length, BLU
pin3,4 LED2 long wave length, AMB

+3VALW

R2541 2.2K_0402_5%

R2542 3.9K_0402_5%

LED3

BATT_BLUE_LED# BATT_BLUE_LED# 41

BATT_AMB_LED# BATT_AMB_LED# 41

HT-297UD5-CB5_AMBER-BLUE

R2543 3.9K_0402_5%

LED4

BATT_RED_LED# BATT_RED_LED# 41

HT-191USD5_RED

Reserved

PWR_SUSP_LED#

41 PWR_SUSP_LED

Q2432A 2N7002KDWH_SOT363-6

R2546 100K_0402_5%

PWR_LED#

41 PWR_LED

Q2432B 2N7002KDWH_SOT363-6

R2547 100K_0402_5%

10/2

Power

46 PWR_LED#

+3VALW

R2462 2.2K_0402_5%

R2463 3.9K_0402_5%

LED2

PWR_LED#

PWR_SUSP_LED#

HT-297UD5-CB5_AMBER-BLUE

HDD

+3VS

R2540 100_0402_1%

LED5

MEDIA_LED#

HT-191NB5_BLUE

C2402 0.1U_0402_16V4Z @

+3VS

U2401

VCC, OUT, GND, IN1, IN2

5IN1_LED# 40

PCH_SATALED# 13

MC74VHC1G08DFT2G_SC70-5

+3VS

@ R2403 10K_0402_5%

LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/12/31

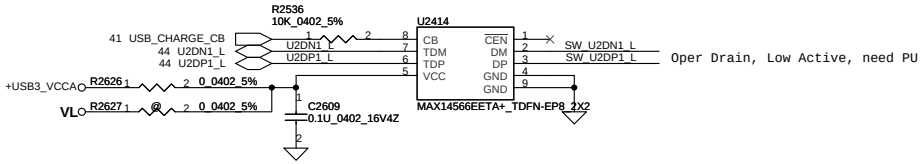
Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 42 of 57

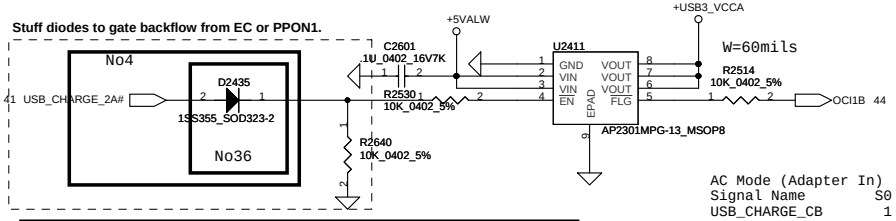
USB Host Charger

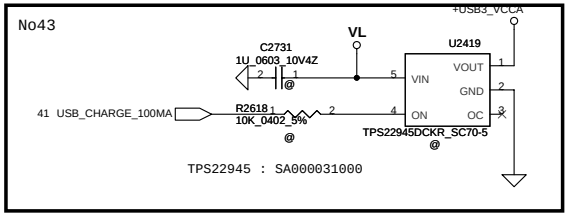


CB=0	Auto detection charger identification active
CB=1	Connect DP/DM to TDP/TDM

U37 EN# active at S0, S5(AC) and S5(DC)

	EN#	USB_CHARGE_2A#	PPON1
S0	ACTIVE	LOW	LOW
S5(AC)	ACTIVE	LOW	LOW
S5(DC)	OFF	HIGH	LOW





AC Mode (Adapter In)

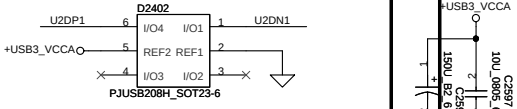
Signal Name	S0	S3	S5
USB_CHARGE_CB	1	0	0
USB_CHARGE_2A#	0	0	0

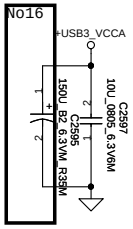
DC Mode (Battery >30%)

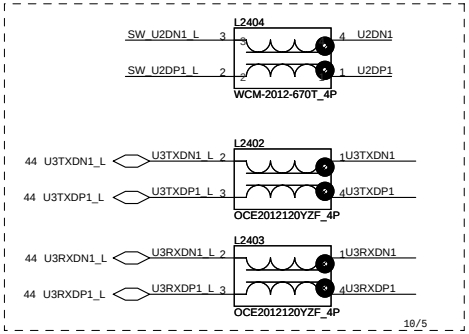
Signal Name	S0	S3	S5
USB_CHARGE_CB	1	0	0
USB_CHARGE_2A#	0	0	0

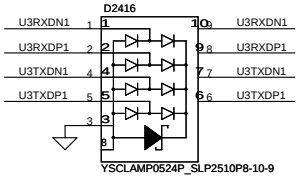
DC Mode (Battery <30%)

Signal Name	S0	S3	S5
USB_CHARGE_CB	1	0	0
USB_CHARGE_2A#	0	1	1

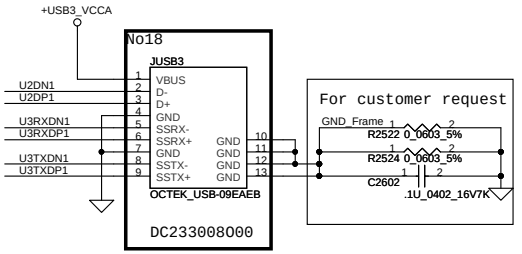






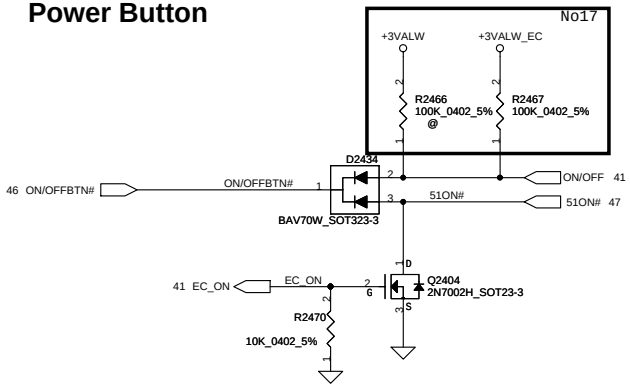


USB3.0 Connector



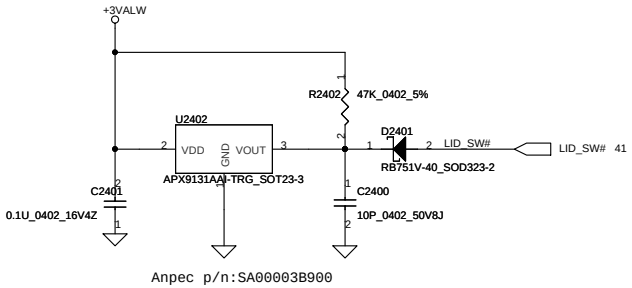
USB_CHARGE_CB Switch Control Bit, 0:Autio Detection, 1:Pass-through
USB_CHARGE_2A# Enable 2A USB Power Switch (Low active)

Power Button



Lid Switch

(Hall Effect Switch)



Anpec p/n:SA00003B900

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/12/31

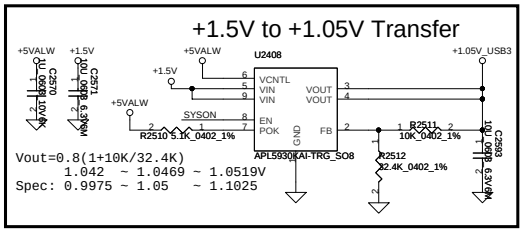
Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

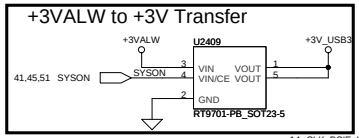
Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 43 of 57

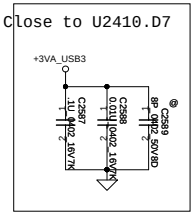
+1.5V to +1.05V Transfer



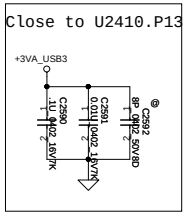
+3VALW to +3V Transfer

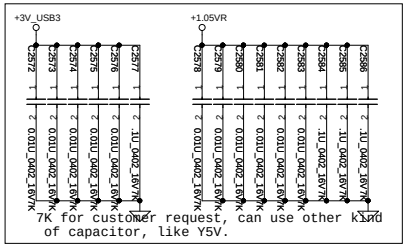


Close to U2410.D7

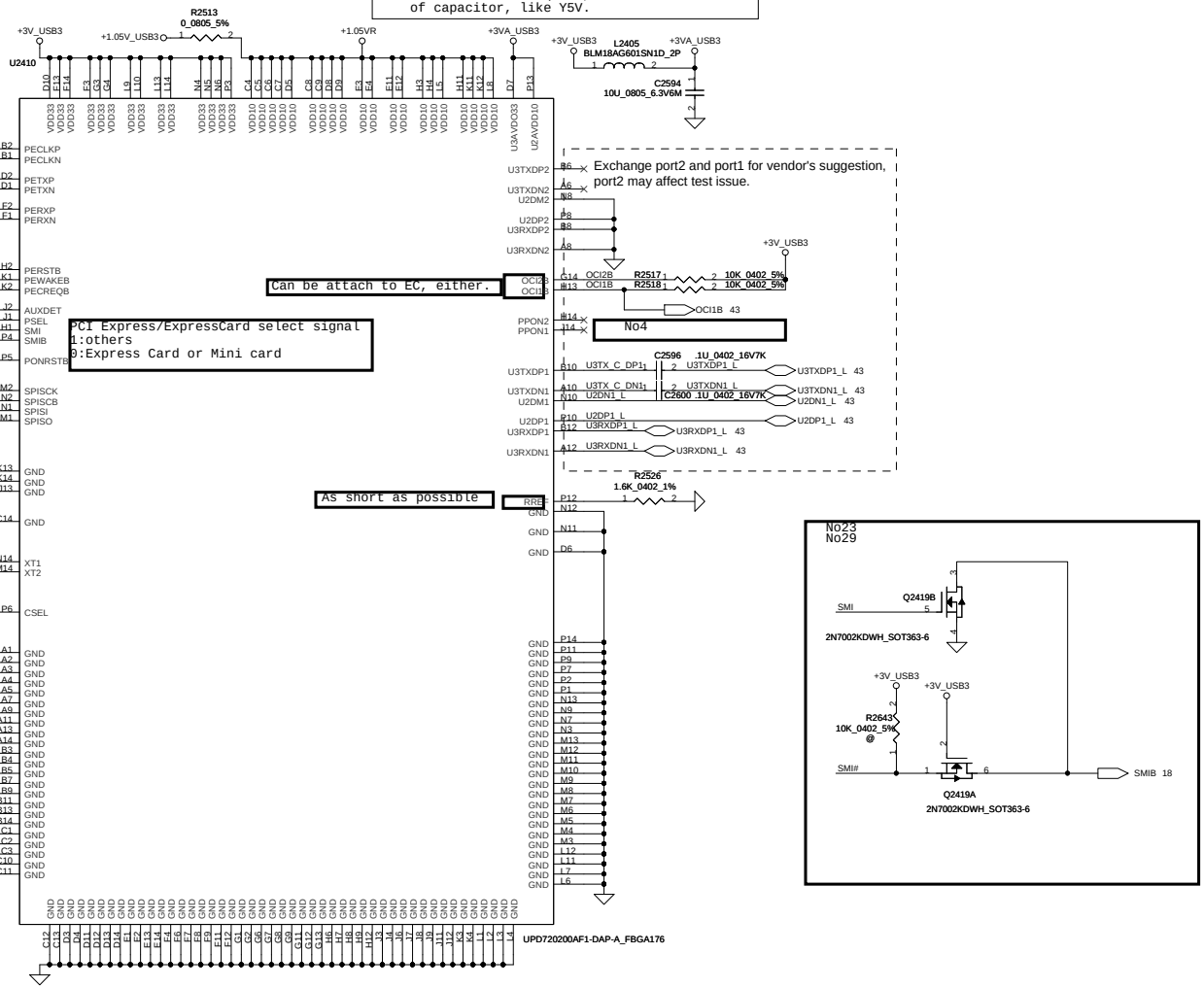


Close to U2410.P13





7K for customer request, can use other kind of capacitor, like Y5V.



PCB footprint change: UPD720200F1-XXX-A_FBGA_176P-NH

From JM50: P/N change to SA000048H10

10/29 From JM40: P/N change to SA000048H00

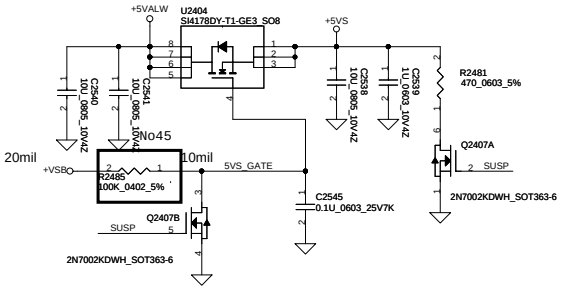
Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

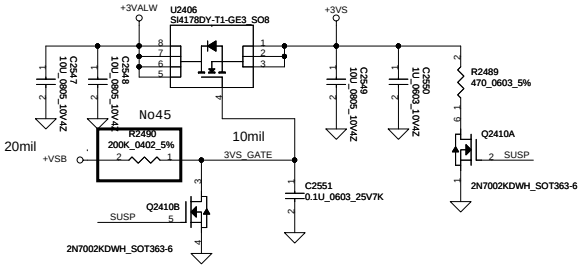
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Title	SCHEMATIC,MB LA-A712		
Size C	Document Number 4019BI		Rev A
Date: Tuesday, December 14, 2010	Sheet 44 of 57		

+5VALW TO +5VS

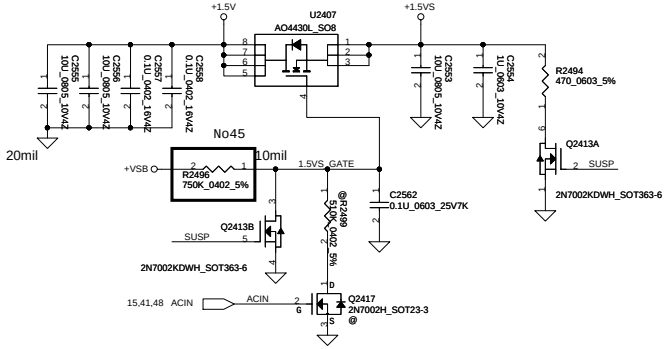


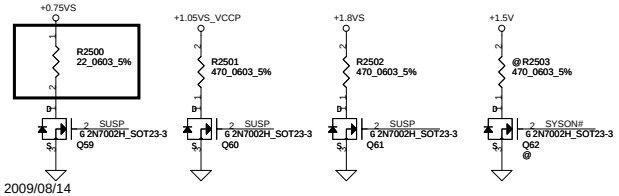
+3VALW TO +3VS



1211 EMI ADD 0.1U close PJ5

+1.5V to +1.5VS



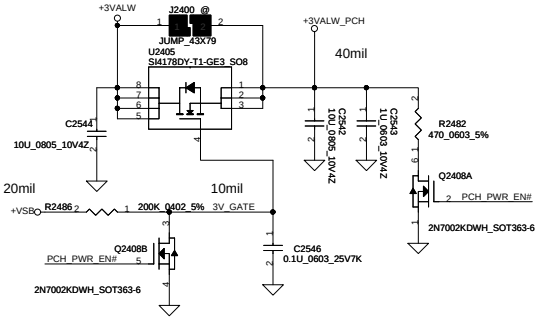


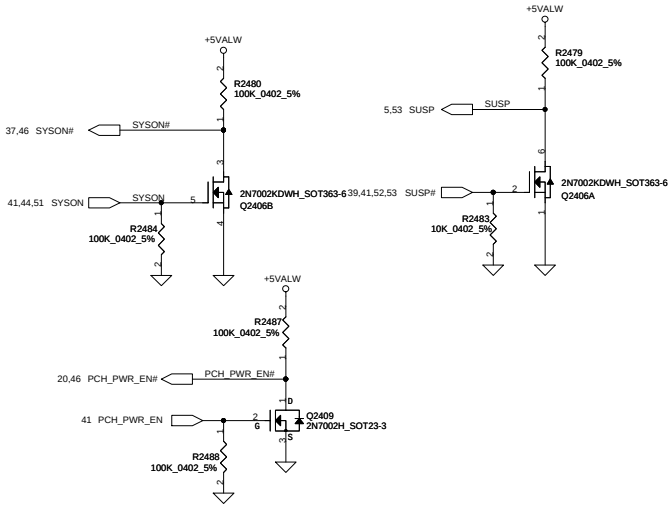
2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

MOS needed!

+3VALW TO +3VALW(PCH AUX Power)

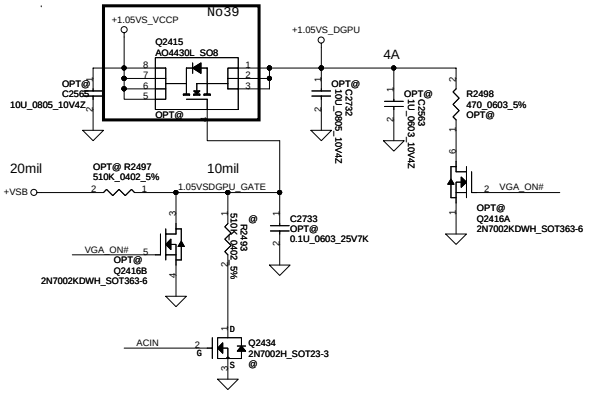
Short J5 for PCH VCCSUS3.3



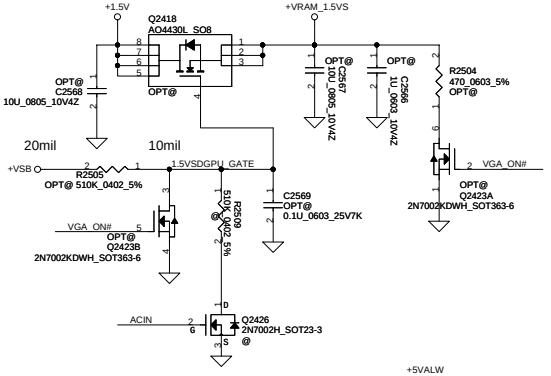


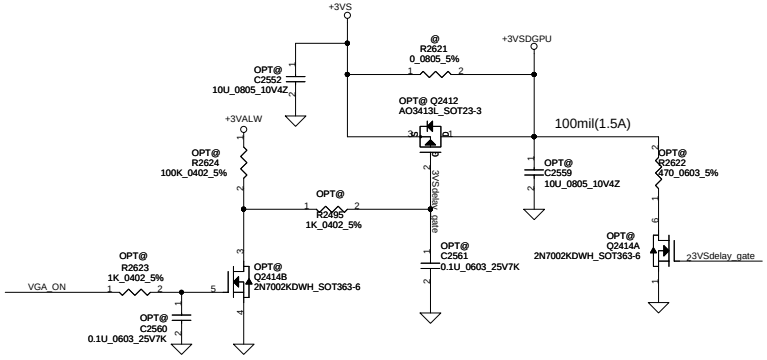
10/5, follow JM50

+1.05VS_VCCP to +1.05VSDGPU for GPU

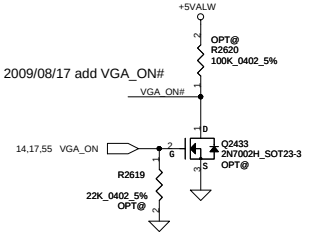


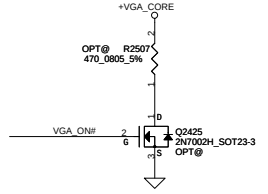
+1.5V to +1.5VSDGPU for GPU





2009/08/17 add VGA_ON#





Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/12/31

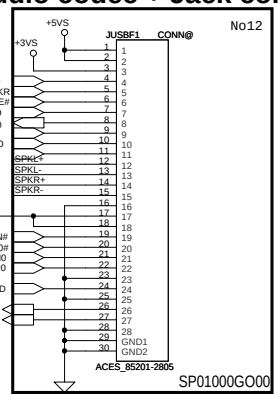
Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

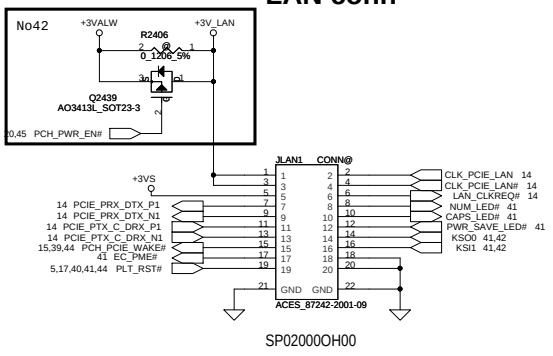
Size	Document Number	Rev
C	4019BI	A

Date: Tuesday, December 14, 2010 | Sheet 45 of 57

For USB 20 small board
USB2.0+Audio codec + Jack conn

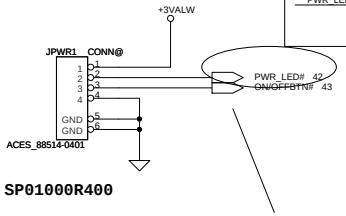


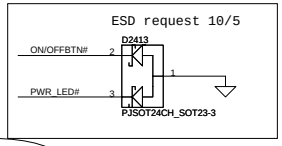
For LAN small board
LAN conn



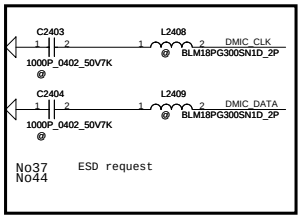
	KSO0
KSI1	PWR SAVE BTN#

PWR board

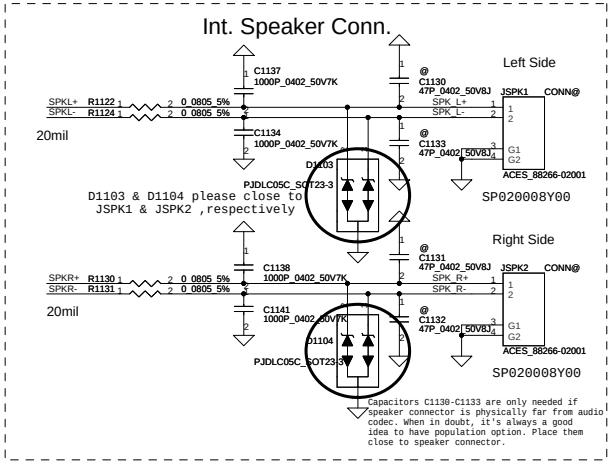


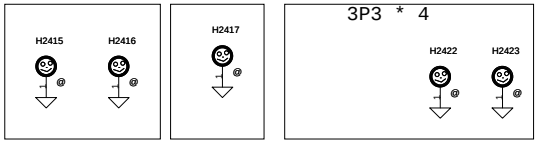


check:
PWR indicator is the same as PWR_LED?

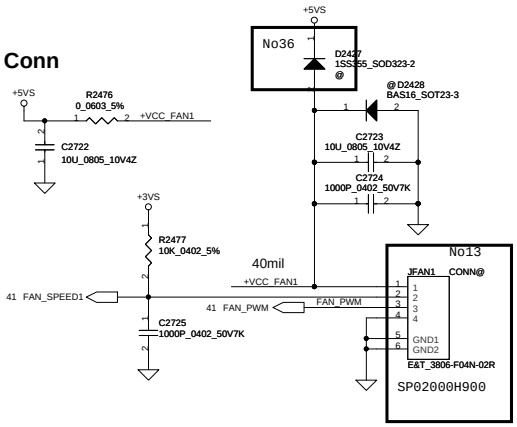


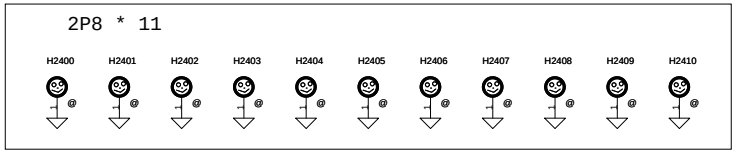
Int. Speaker Conn.

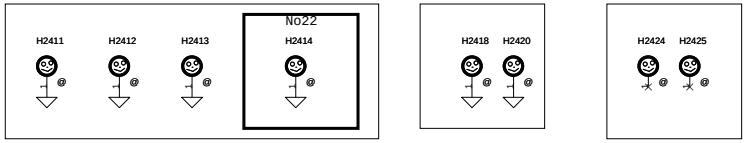




FAN1 Conn

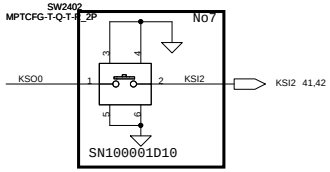






BUTTON

Battery Indicator BTN



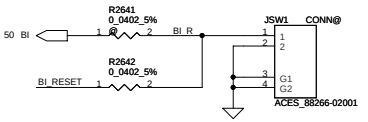
	KSO0
KSI1	PWR SAVE button
KSI2	Battery ID BTN#

check: PWR_SAVE# and BAT_STAT use keyboard matrix

Open Door shut down key

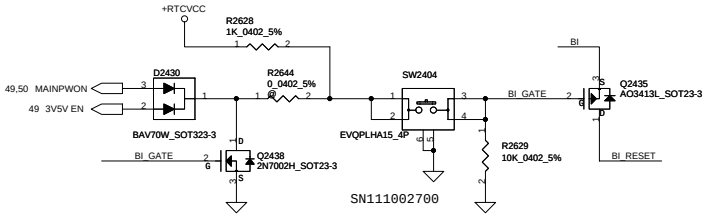
Normally door closed --> BI low --> battery power on
Open door --> BI high --> battery power off

No19
No27
No35
No38



Reset key (shut down)

press: low pulse --> shut down --> need user to press power button to turn on

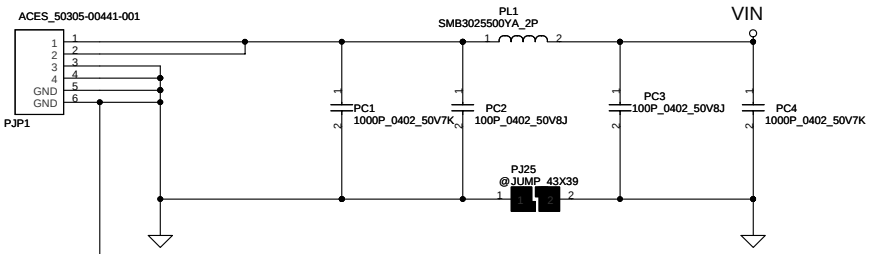


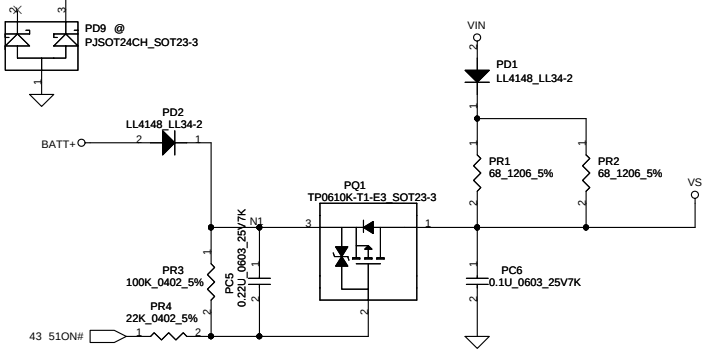
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2010/12/31

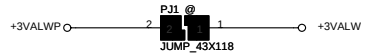
Title: SCHEMATIC,MB LA-A7121

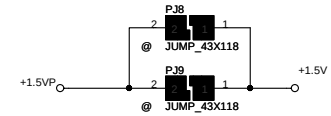
Size	Document Number	Rev
C	4019BI	A

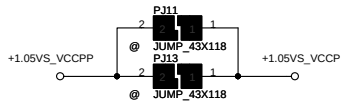
Date: Tuesday, December 14, 2010 | Sheet 46 of 57

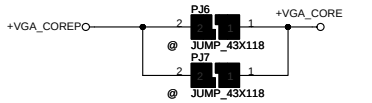


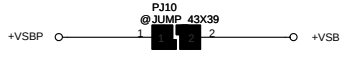


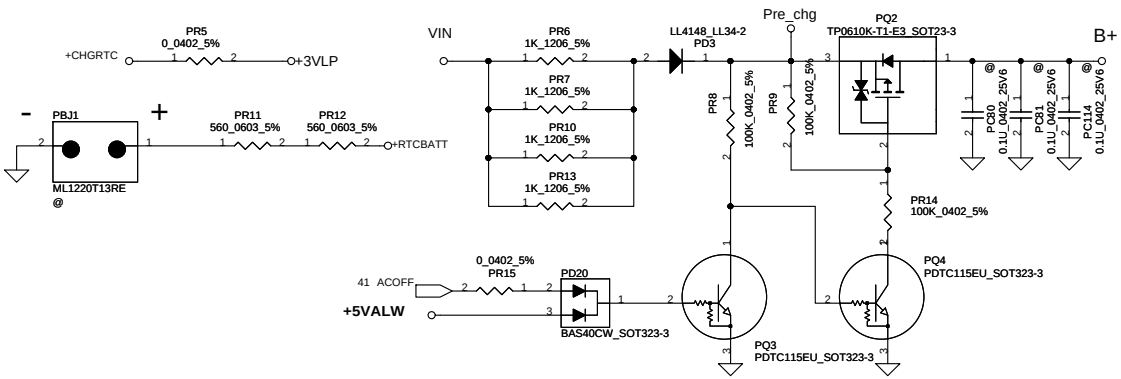












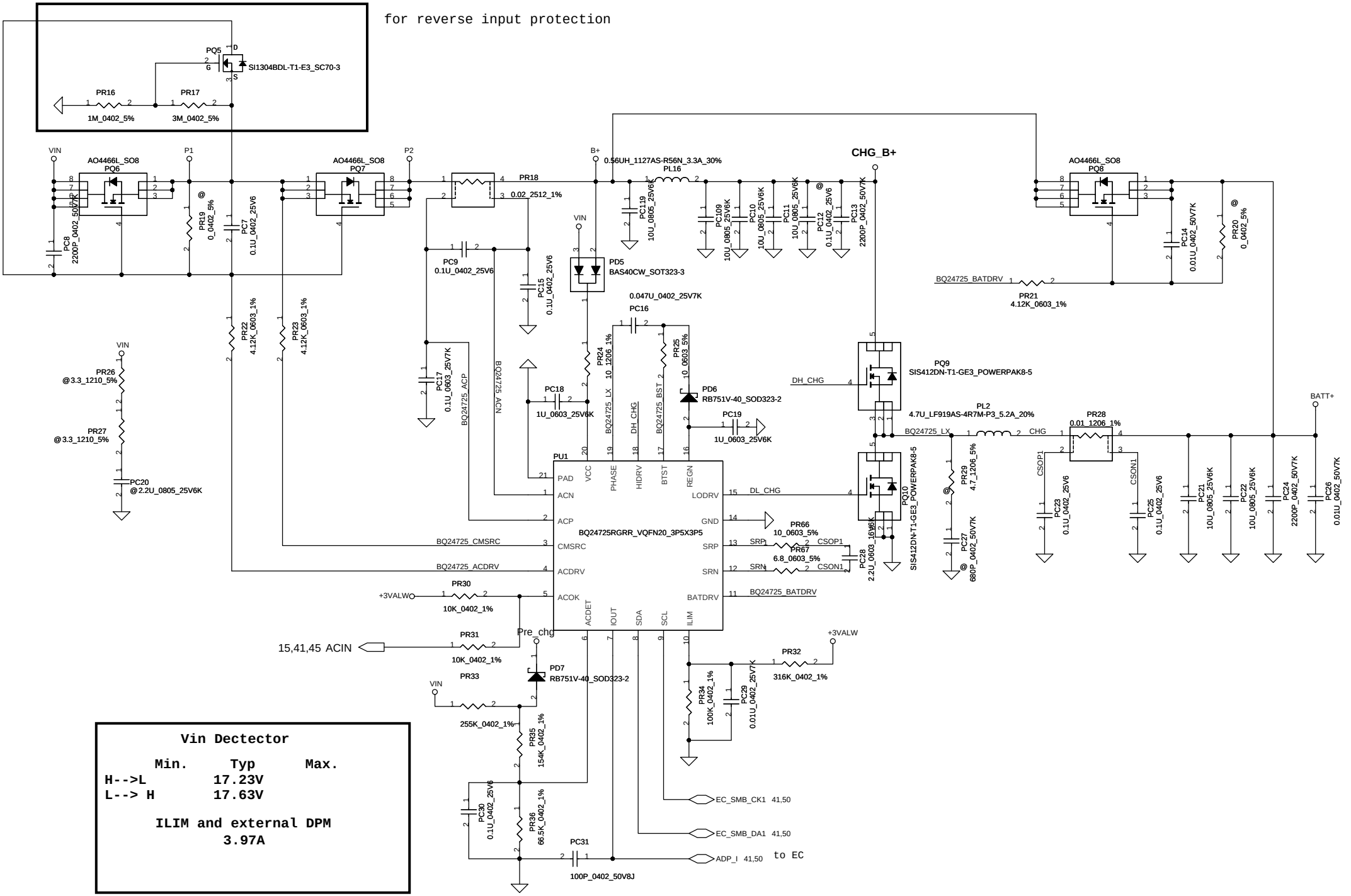
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size	Document Number	Rev
Custom	4019BI	A

Date: Tuesday, December 14, 2010 Sheet 47 of 55



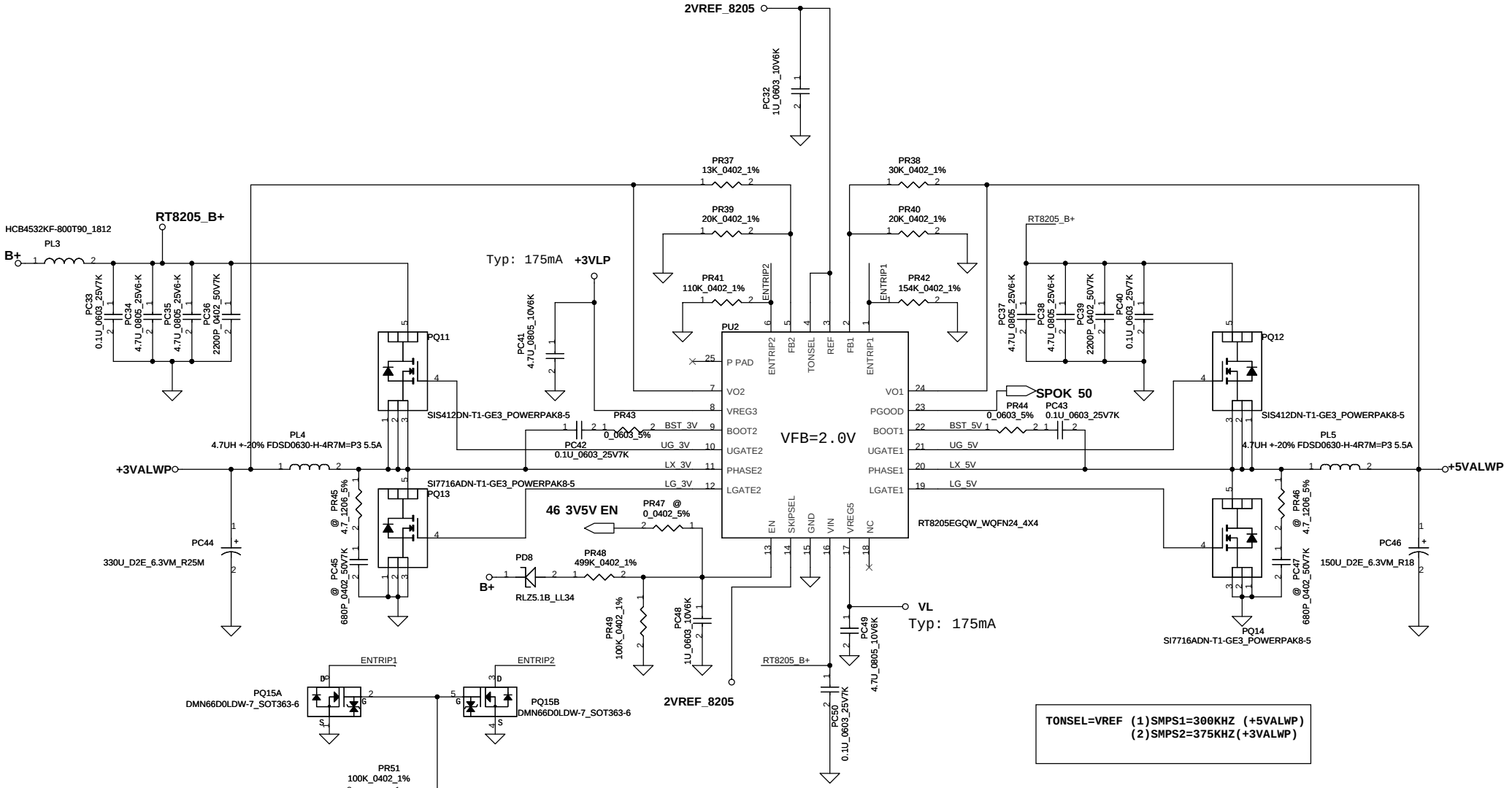
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

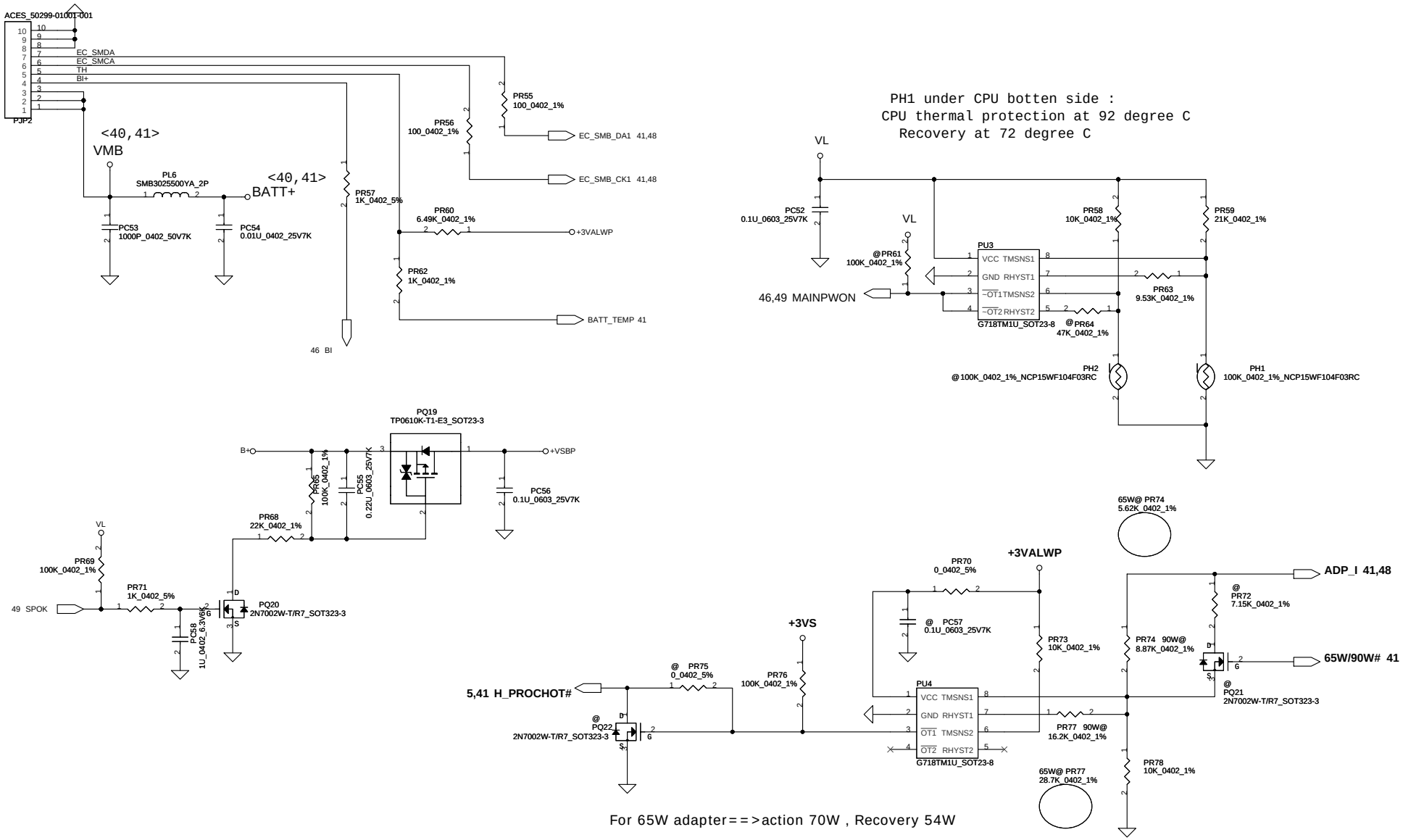
Size	Document Number	Rev
Custom	4019BI	A

Date: Tuesday, December 14, 2010 Sheet 48 of 55



Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.
Title: SCHEMATIC,MB LA-A7121
Size: Custom
Document Number: 4019BI
Rev: A
Date: Tuesday, December 14, 2010
Sheet 49 of 55



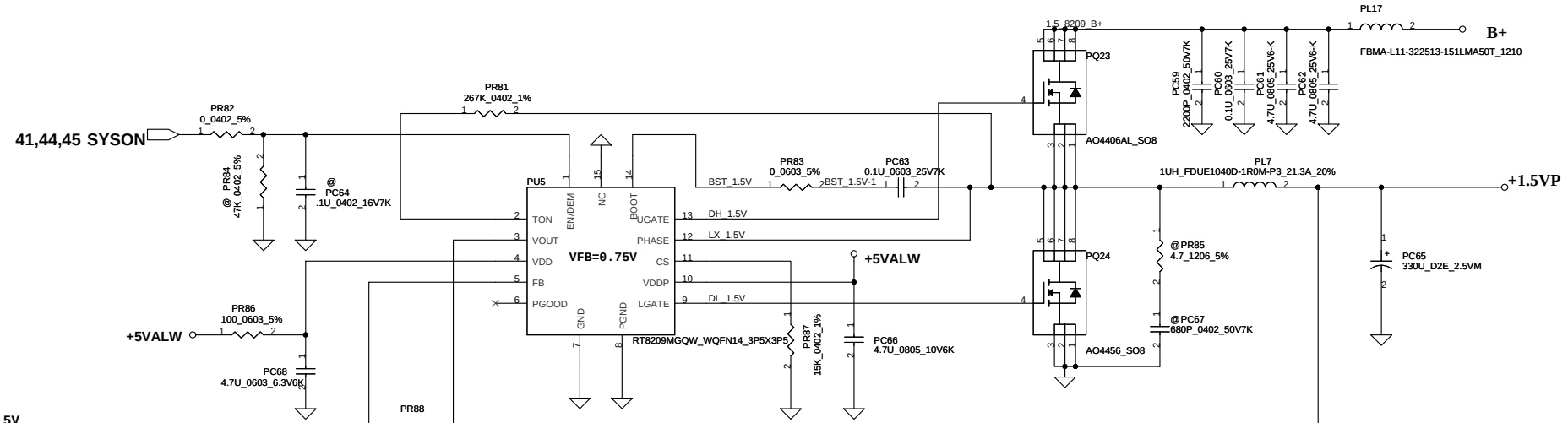
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size	Document Number	Rev
Custom	4019BI	A

Date: Tuesday, December 14, 2010 Sheet 50 of 55



<Vo=1.5V> VFB=0.75V
V=0.75*(1+10K/10K)=1.5V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=19.53A, Imax=23.44A, Iocp=13.67A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.63A
=>1/2Delta I=2.315A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+2.315A=35.65A
Iocpmin=((15K*9uA)/(0.0056*1.3))+2.315A=23.06A
Iocp=23.06A~35.65A

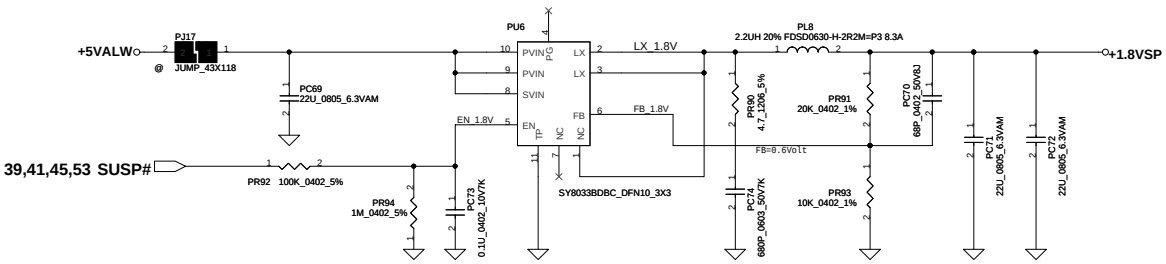
Compal Electronics, Inc.

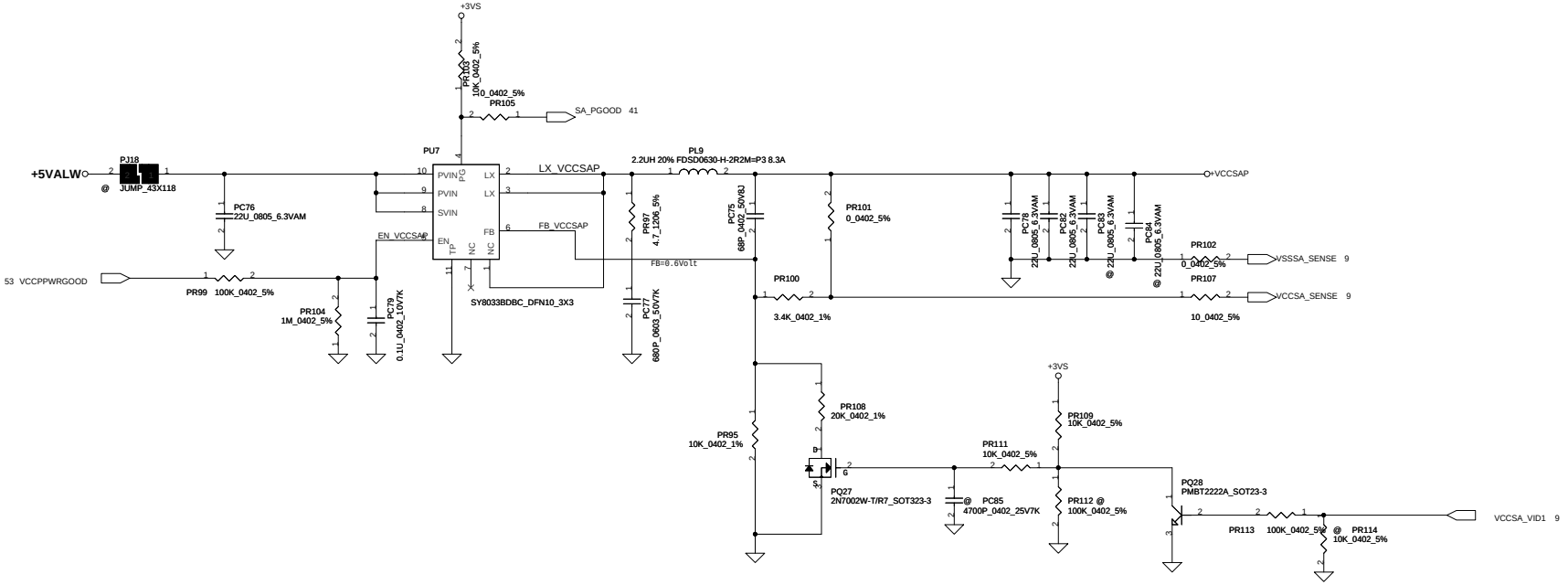
Title: SCHEMATIC,MB LA-A7121

Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 51 of 55

1.8VSP
Ipeak=3.35A ; 1.2Ipeak=4.02 ;Imax=2.345A
Vout=0.6*(1+(20K/10K))=1.8V





VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

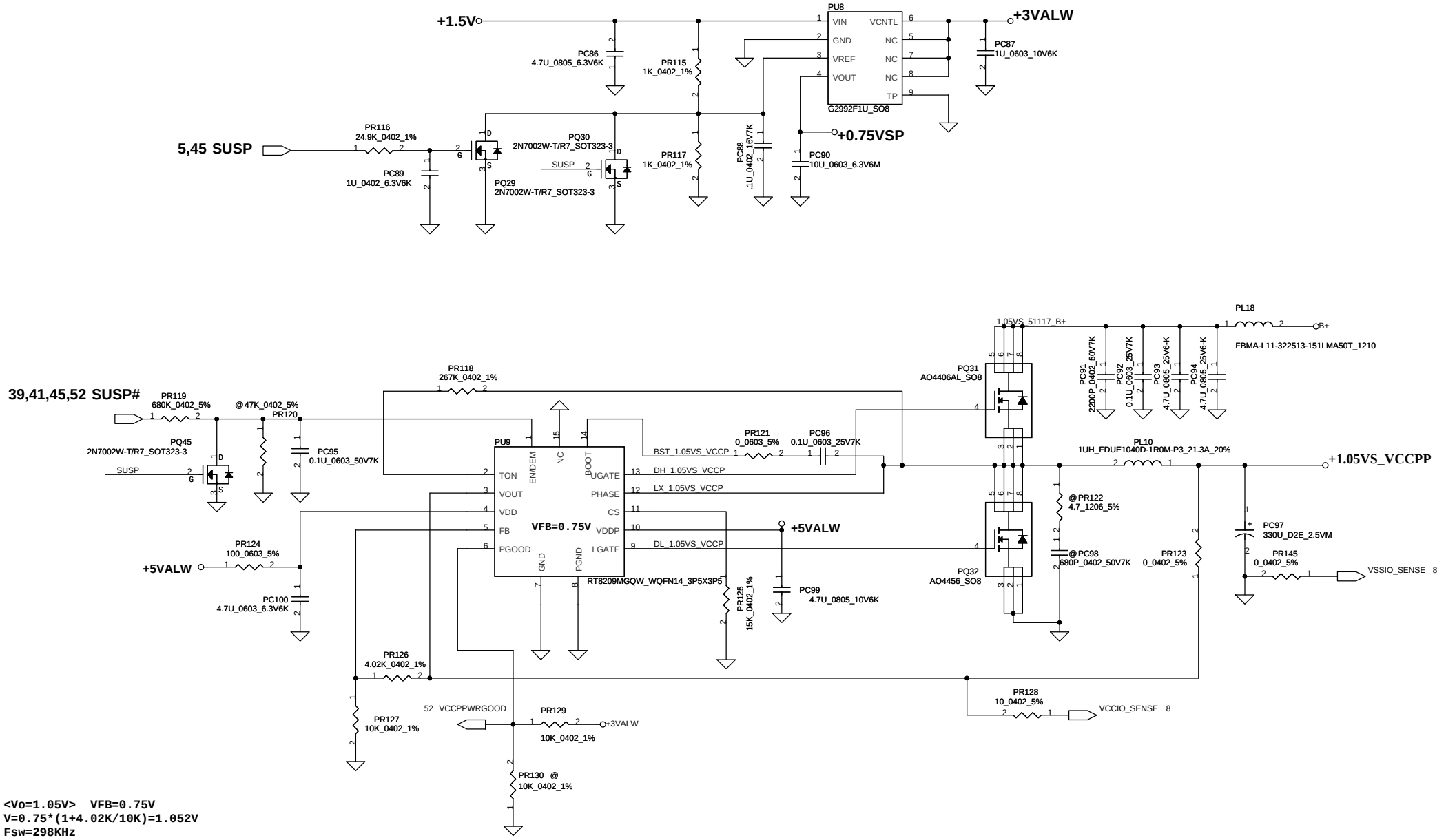
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size	Document Number	Rev
C	4019BI	A

Date: Tuesday, December 14, 2010 | Sheet 52 of 55



<Vo=1.05V> VFB=0.75V
V=0.75*(1+4.02K/10K)=1.052V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=12.866A, Imax=9A, Iocp=15.439A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=3.33A
=>1/2Delta I=1.665A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+1.665A=37.62A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=23.02A
Iocp=23.02A~37.62A

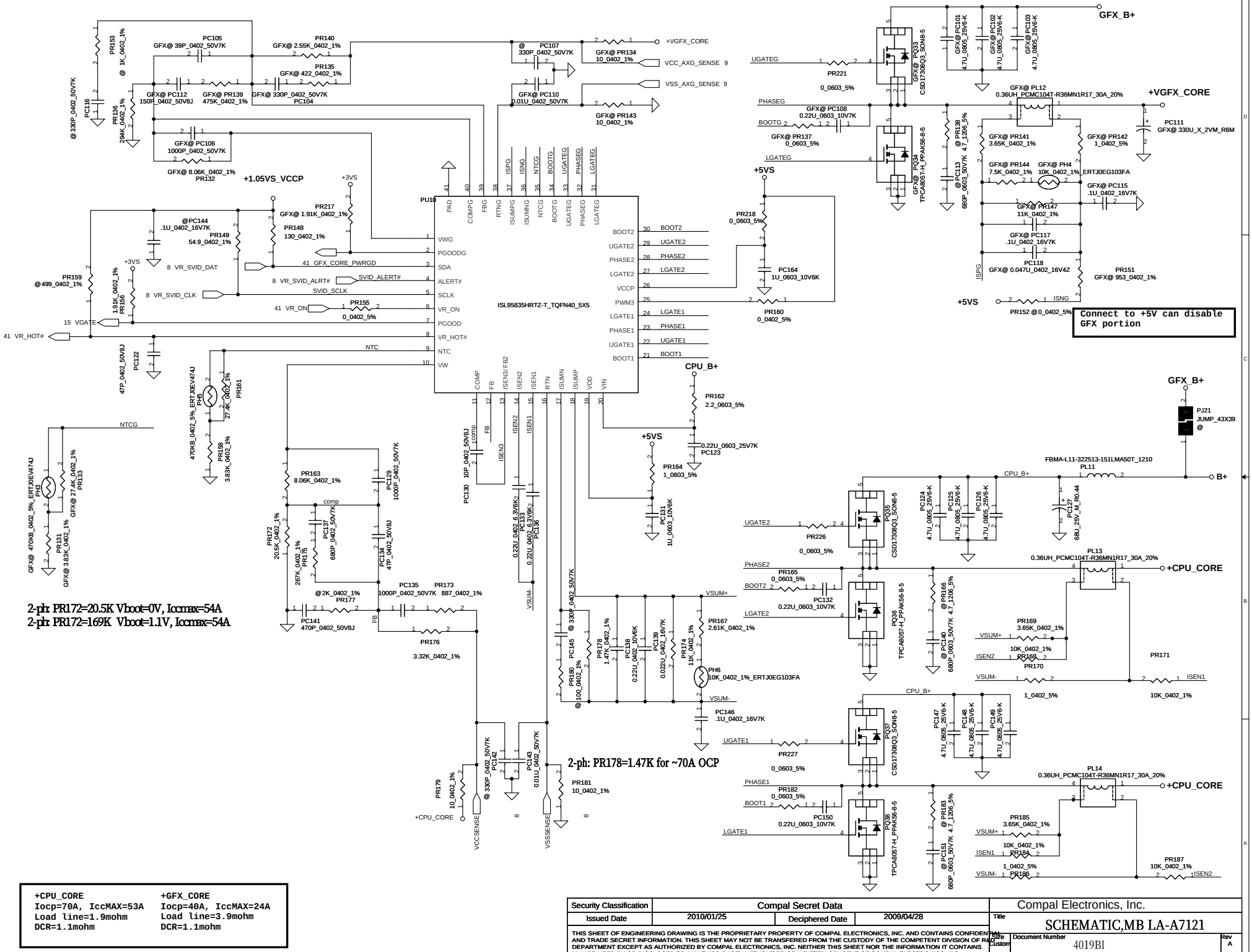
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 53 of 55



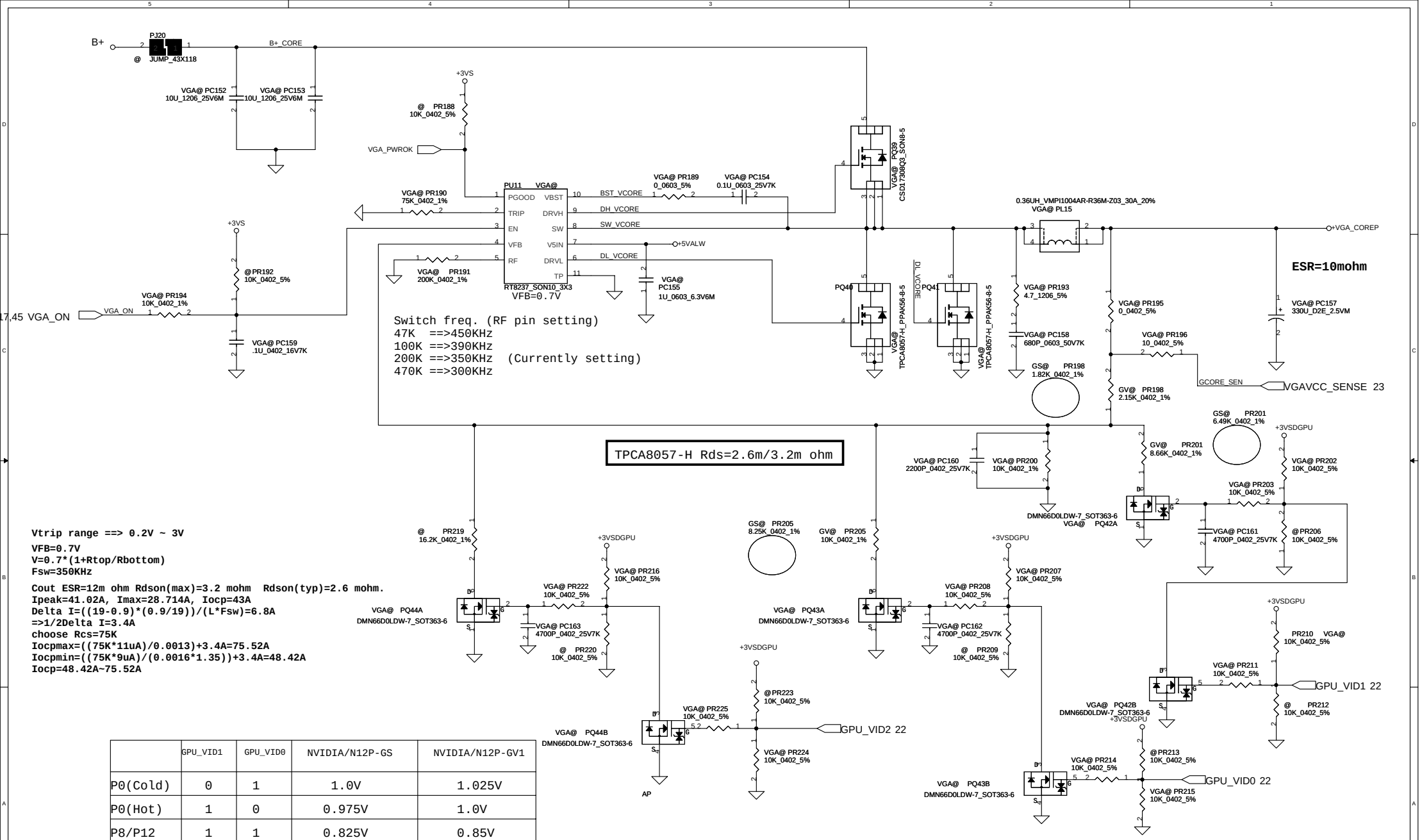
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size: Custom | Document Number: 4019BI | Rev: A

Date: Tuesday, December 14, 2010 | Sheet 54 of 55



Vtrip range ==> 0.2V ~ 3V

VFB=0.7V
V=0.7*(1+Rtop/Rbottom)
Fsw=350KHz

Cout ESR=12m ohm Rdson(max)=3.2 mohm Rdson(typ)=2.6 mohm.
Ipeak=41.02A, Imax=28.714A, Iocp=43A
Delta I=((19-0.9)*(0.9/19))/(L*Fsw)=6.8A
=>1/2Delta I=3.4A
choose Rcs=75K
Iocpmax=((75K*11uA)/0.0013)+3.4A=75.52A
Iocpmin=((75K*9uA)/(0.0016*1.35))+3.4A=48.42A
Iocp=48.42A~75.52A

	GPU_VID1	GPU_VID0	NVIDIA/N12P-GS	NVIDIA/N12P-GV1
P0(Cold)	0	1	1.0V	1.025V
P0(Hot)	1	0	0.975V	1.0V
P8/P12	1	1	0.825V	0.85V
ES	----	----	----	0.925V

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: SCHEMATIC,MB LA-A7121

Size	Document Number	Rev
Custom	4019BI	A

Date: Tuesday, December 14, 2010 Sheet 55 of 55

A pahse

09/23
No01: P45, chnge Q2407 and Q2408, change DC interface part number,
change Q2407,2408,2410,2413,2414,2416,2423,2424 to SB00000EO10

No02: P15, change PCH_GPIO32 to CLKRUN# and pull down
No03: P18, delete OptImus_EN# and change to GPIO38

09/24
No04: P05,P16,P17,18, delete JXDP2 and relative intersheet symbols.
No05: P46, add SP1 to 6
No06: D2100 swap from layout
No07: delete DCR and COLOR_ENG_EN function
No08: add LID_SW function and revise FAN circuits to following JM50 and NELA0
No09: add 3GP for WWAN
No10: add R385 for reserved VCCIO_SEL pull high
No11: change CPU 60pin XDP to 26pin, revise relative circuits

09/27
power circuits combined
No12: change WWAN circuits (EC_SIM_DETECT, UIM_DET, WWAN_DET#)

09/28
No13: P39, add pull high +3VS at UIM_DET
No14: P22, reserve SM bus 0 ohm
power circuits combined
No15: P07, From JM50, change VCCIO_SEL PU from +3VALW to +3VS, should check
No16: P49, from JM50, delete 6300 (11.8V5 path to +VCCAFDI_CRK)
No17: P39, only UMA path, delete 0 ohm at the path
No18: P37, from JM50, change D2416 symbol and add D2402, change R2536 symbol
No19: P43, from JM50, delete power delay circuits (DGPU_PWR_EN to VGA_ON, SUSP# to VS_ON)
No20: P46, change Power board conn 4 pin SP01000R400
No21: P42, from JM50, HDD_LED sources from PCH and CR
power circuits LA-7121P_R01_20100920A.dsn combined
No22: P41, Power, jackie: delete IMVP_IMON, no need
No23: P41, move PLT_RST# pull low from R2226 to R388
No24: P3, add part location define
No25: P18 and P35, from JM50, delete CRT_DET# (don't use this pin) and change CRT_DET to PCH_GPIO0
No26: P43, add P31, from JM50, change QC pin from USB_OC1# to USB_OC0#
No27: P14, from JM50, change R107 to 0 ohm
No28: P43, reserve 2x change R107 to 0 ohm
No29: P42, change JKB1 to SP01000R500, JTP1 to SP010014M00
No30: P37, change JUSB1 to DC233007T00
No31: P39, modify UIM_DET function, reserve WWAN_OFF# path

09/29
No32: P17 and 39, change WWAN from USB port 11 to port 9, and update page 3 table
No33: P14, change name: PEG_CLKREQ_R# to PEG_CLKREQ#_R
No34: P05, delete SM bus to XDP
No35: delete Net13
No36: P11, add R_HDA_SYNC_R for potential leakage concern, (DG1.5)
power circuits JM5JR-20100929.dsn combined
No37: P42, from JM50, delete Q2431, no need to reserve it
No38: P42, from JM50, modify BATT LED circuits (need to confirm P/N);
combine PWR_LED# and PWR_SUSP_LED# and change source from +3VS to +3VALW
No39: P42, from JM50 GPIO table,
pin 16: USB30_LED# and rename USB3_LED# to USB30_LED# for related circuits
pin 19: NC, and delete SUSWARN# from PCH.
pin 21: 3G_LED#
pin 25: NC
pin 70: EC_SIM_DETECT
pin 73: PWR_SAVE_LED#, and add this signal to LAN connector
pin 86: H_PROCHOT#_EC
pin 89: PWRSHARE_OE#
pin 97: NC
pin 103: EC_PME#
pin 106: CPU1.5V_S3_GATE
pin 108: SA_PGOOD
pin 118: NC

09/29
No40: P02, modify block diagram
No41: P04, P34, reserve eDP 2 lane
No42: P42, reverse KB conn pin define (pin1 different from the old one)
No43: P41 and P37, change USB3.0 and CODEC
No44: P46, change power conn name to JPWR1
No45: P39, correct name: +3V_WWAN to +3VS_WWAN;
delete PCIE IF;
add 4 x 0 ohm for WWAN_DET# and UIM_DET
No46: P41, change EC pin define (from EC Donate), add AD_PID0
No47: P09, From JM50, delete +1.5V_CPU_VDDQ and delete JP2 from +1.5V

09/30
No01: P41, EC pin define change
pin 106: PWR_SAVE_LED# (USB30_LED# delete y customer)
pin 118: NC

No2: P17, P37, delete JUSB1 (will on daughter board), delete R2434 (already PU at PCH)
No3: P14, From JM50, add PCH_GPIO44 back, delete R95
No4: P14, P44, for USB30 clock, install R173, R2538, uninstall R2535, Y2400, C2607, C2608
No5: P14, From JM50, due to no PCH_XDP, delete JTAG_TMS, TDO, TDI, add TP
No6: P15, From JM50, change CLKRUN# to PCH_GPIO32, Add pull high 8.2K
No7: P18, From JM50, add T83 to T88
No8: P20, From JM50, uninstall R3003, install Q12, C174, R307
No9: P46, From JM50, change PWRSHARE_OE# to USB_CHARGE_CB, Change PWRSHARE# to USB_CHARGE_EN#
No10: P46, install R2284 for phase A test
No11: P44, delete USB30_LED# circuits
No12: P43, From JM50, move USB3 conn and related power switch to P43
No13: P39, From ESD Jeremy, change HDMI ESD L2110~L2113 to SM070000K00 and install them;
No14: P37, P96, From ESD Jeremy, change USB ESD L2110~L2113 to SM070000K00 and install them;

10/2
No1: P7, From JM50, delete CPU AN35, AM35 signal
No2: P3, From JM50, delete 91S and change R83,R85 to 1k
No3: P14, From JM50, delete R2537, add T83 and T84 point
No4: P18, From JM50, delete R2537, pin1 to low, add T83 PD function
No5: P17, From JM50, delete R2477, change DGPU_PWR_EN to VGA_ON, DGPU_PWR_EN# to VGA_ON#
No6: P17, From JM50, delete R2478, change DGPU_HOLD_RST# pull high)
No7: P18, From JM50, install R285
No8: P18, From JM50, delete R584 PWR_SAVE#
No9: P39, delete not necessary part R1423
No10: P38, From JM50, reserved VDD 1.5V
No11: P41, From JM50, temporarily follow the name: active high: PWR_SUSP_LED, PWR_LED, wait for EC definition
No12: P42, From JM50, same as No1, add MOS to reverse the 2 signals
No13: P42, From JM50, change PWR_STAT key to KB matrix, and change LAN_connector pin define (PWR_SAVE# --> KSI1, KSO0)
No14: modify LAN board conn, now use 24 pin, will study 20 pin ok or not
No15: revise P01-06 small board
No16: P42, From JM50, change BATT_AMB_LED with BATT_GRN_LED#, change HDD LED and R, change Wireless LED part and to +3VS
No17: P46, From JM50, change PWRSHARE_OE# to PWR_LED#
No18: P22, From JM50, add R_PERFORMANCE to GPIO12, GPIO18
No19: P7,P11,P12, install M18 and change M30 to @.
No20: P43, From JM50, U2414.5 change power source to +USB3_VCCA, Delete R2619

10/4 Bryant Hou

Update JP4=>JUSBFPC1
C1576 390U=>220U
USB3.0 & HDMI Conn Footprint
U2419 footprint(need you chk)
Combine new pw circuit
Add original JUSB1 circuit
Del JUSB2 circuit
add Speaker

10/5
No1? P46, add USBFFC1 back and modify pin(add SPKR signal)
No2: P46, modify JLAN1, delete 1 +3VALW, add 1 GND
No3: P37, delete R2434 (double pull high)
No4: P43, From JM50, update U2413 symbol
No5: P13, From JM50, add Q4 and R100 for Audio Issue
No6: P43, Layout request, L2402, L2403, L2404 swap N-P
No7: P22~P30, From JM50, based on JM50 circuits and JM30 part reference,
(but delete VGA_HDMI_DET and HDMI output, IFPC power circuits, change PEG names)

No8: P45, From JM50, Due to the change of GPU pages, DC interface changes too

No9: page 34~46 change to page 31 to 43
power page 47 from P4 to P52
EE modify list : P09

No10: page12, From connector list,
change JDIMM2 to SP07000NN00,
change JLVDS1 to SP01001300,
change JCRT1 to DC680003L00
change JKB1 to SP01000GE00

No11: delete No7 and No8, change back original dGPU, add C1595~C1603, add R1498~R1506 , modify some R, C values

No12: From power_P46, change reset button connection to 3V5V_EN
No13: for JM30/40/50/power common name: change +3VS_DGPU to +3VSDGPU

No14: P37, From JM50, change R2435 from 10K to 0 ohm
No15: P43, From JM50, delete U36_1 net USB_Charge_EN#
No16: P41, From JM50, Add EC GPIO
Pin 118-->NV_PERFORMANCE
Pin 25-->USB_Charge_100mA
Pin 18-->USB_Charge_2A#

No17: From conn list, P40,update JREAD1 to DC021010041, update JUSB3 to DC231003030
No18: P37, From ESD Jeremy, change USB ESD to SC300000600
No19: P46, From ESD Jeremy,add PWR board conn ESD SCA00000E10

10/6
No1: P13, change BIOS conn SP07000F500
No2: P43, From ESD Jeremy, install D2416, D2402
No3: P5, From ME, change JXDP1 to SP01000N300
No4: P46, delete JUSBFPC1
No5: P3, From EC Donate, update PID table
No6: From ME conn list, change JHDMI1: DC232001100; JLAN1: SP02000H000
No7: Update schematic: SW2400,SW2401, C1405~1436, C1457, C1458, C1308, C1314, C1451~1453, R229~R231, R2619, Q2429
power circuits JM3JM_20101006.dsn combined:
1.Swap some component between NTC and NTCG.
2.Delete PC128
3.Add +0.75VSP on power IC side.
4.PQ41 on VGA low side.
5.Change PQ25 to SIS412DN.
6.Change PQ26 to SI7716.
7.Swap PH1 and PH2.
8.Delete PD4.
7.Add PL16 for EMI.

10/7

No1: Update footprint: R229, R230, R231 -- RP_0804_8P4R
No2: Update symbol: R51, R214, Q2406, Q2414, Q2416, Q2423, Q16, U2402, U2401

10/8
No1: P18, from checklist and CGS, pull down PCH_GPIO36 and 37
No2: P7 from JM50, delete R and add T82~85 on VAXG_VAL_SENSE ...
No3: P31,12, From JM50, delete R2539, R2041 R3 function
No4: P22, From JM50, add GPU_VID2
No5: P22, change part(reference) R755~R760 change to R1507~1512
No6: P38, From JM50,delete C1597, C1598 and add R1513, R1514 to GND
No7: P23, From JM50,install R1451
No8: P25, From NVIDIA, reserve one 0 ohm R1515 to connect to +1.05VSDGPU

10/11
No1: P46, change JUSBFFC1 pin definition: add 1 +5VS and delete 1 GND
No2: P15, From JM50, R186.2 connect to PCH_PWROK
No3: P17, for Layout request, shrink C180, C181 to 0603
No4: P13, From Layout request, move R172 and R52 to audio sub board
power circuits JM30_20101011C.dsn combined
change item-->Back the pull-up power to +3VSDGPU for GPUVID, add GPU_VID2
No5: P25, change R1515 connection to +1.05VS_DGPU
No6: P15, delete D2
No7: P22, delete C1440, add R1516, R1517
No8: P22, From Nv DG:
for PLL, delete C1595, for NVVDD, delete C1442(330u), C1443~C1445, for PEX_PLLVDD, delete C1500, for FBx_PLLAVDD, delete C1508, C1513
No9: P15, install R196
No10: P22, From NVCARE, GPIO12 pull high(R1404), and NV_PERFORMANCE(D1400) use diode to prevent leakage,
delete R1409, R1402, R1403, T1400, change C1~C32 X7R
No11: P23, From NVCARE, add reserved 10K pull down on JTAG_TCK
No12: P43, delete USB_100MA_OC# (wait the symbol ok)
No13: P39, change P39 +UIM_PWR_C to +UIM_PWR

10/12
No1, From JM50, P17, P18, Change WWAN_OFF# from GPIO51 to GPIO37; Change WL_OFF# from GPIO55 to GPIO49
No2, From JM40, P42, change TP switch: SN111002700, P46, change reset key:SN190003A00
No3, From JM40, P46, change JPWR1 pin definition
No4, From JM40, P41, change ESD solution connection from SPI_CLK_R to SPI_CLK
No5, From JM40, P38, add R2625 pull high for WWAN_LED#
No6, From JM40, P18, change back PCH_GPIO38 to OPTIMUS_EN# and modify PU/PD
No7, P17,P18, check PCH power, delete L4, R296, L7, R325 and change C170, C199 from 0805 to 0603
No8, From ME, P42, BAT_LED should be Top view, change LED2406 and LED2408 circuits
No9, From JM40, P41, reserve a path +3VLP to EC
No10, From ME, add C216, C217 for PCI CLK
No11, for BOM upload, change JUSBFFC1 to JUSBFC1, LED24xx to LED1,2,3,4,5; add ZZZ1
No12, for BOM upload,
change C1137, C1134, C1138, C1141 to SE07410ZK80,
change JP1 and JP3 "@",
change Q59~Q62, Q1301, Q2100, Q2102~Q2109, Q2404, Q2409, Q2417, Q2426, Q2433, Q2434 from SB5700201 20 to SB000008J10,
change JXDP1, JSPK1 and JSPK2 "CONN@",
update C2726, C1309, C1400, C1509, C1514, C1446, C1447, C1480, C1487, R1483, R1486, R170, R173,
R393, R1455, R1456, R1463, R1464, R1470, R1471, R1478, R1479, D2102, D2103, Q16
change T" to "@"

10/13
No1, From JM40, P39, change D2409 part for BOM
No2, for BOM upload,
change R1300 to SD00000BN80 (0603), change C2489, C2493, C2496, C2494, C2495, C2487, C2491, C2488, C2492, C2497, C2485
No3, From JM40, P43, modify USB30 charger function
No4, From JM40, P46, change SW2403 to SN4000001 00
No5, From Diode common, 2N7002 (SB00000EO10), 2 in1 2N7002 (SB00000EJ10), BSS138 (SB501380020)
No6, for BOM upload, update C1321, C2101, C2107, C2217, C2475, C2477
No7, for Layout request, update H2424 footprint, delete H2414
No8, follow nvidia, delete R1499~R1504, change C1~C32 to 0.1uF X7R

10/14
No1, P27, add GND_connection: +FB_AVDD0, +FB_AVDD1
No2, P13, change R126 connection to HDA_SDOUT to HDA_SDOUT_R
power circuits JM30_20101014.dsn combined:
No3, P46, From Layout request, delete H2421 H2419 (netlist 1B)
No4, P46, From Layout request, swap LC110~LC113, (netlist 1C)
No5, P46, From Layout request, change H2423, H2422 footprint, (netlist 1D)
power circuits JM30_20101014A.dsn combined:

10/15
No1, P37, add JUSB2 (standard type USB for study)
No2, P46, From Layout request, change reset key to SN111002700
No3, From JM50, update connector list, change JBT1 to Opin : SP02000FR00
No4, From Layout request, H5123, H2422, H2423, H2420, H2418 change to H_3P3, change JHDMI1 to SUYIN_100042GR019M23BZR_19P-S
No5, From JM50, change reset and D-door shut down solution
No6, From JM50, change BAT in bin from KSI0 to KSI3
No7, P39, change EC_SIM_DETECT to EC_SIM_DETECT# due to low active
No8, P18, P39, delete UIM_DET pin and WWAN_DET#_PCH path
No9, P39, change +3VS to +3VS_WWAN circuits

10/18
power circuits JM30_20101018.dsn combined:
No1, P43, From JM40, add R2631~R2634
No2, P41, From JM40, change +3VLAW to +3VALW_EC for 2 power sources
No3, P38, From JM40, change JHDD1 pin define
No4, P34, rename R478, R479 to R2154, R2155; change C492, C493 to C2151, C2152
No5, P39, From JM50, add WLAN1 components for BT: R2635, R2636, D2432, Q2436
No6, P43, P44, From JM50, change USB3 conn from port 2 to port 1
No7, P13, From JM50, add PCH_GPIO19 pull high R394
No8, P18, From JM50, add PCH_GPIO28 Pull high R395
No9, P44, From JM50, change U2412 to SA000045000
No10, P39, From JM50, change WWAN circuits
No11, (sourcer Amy requests, from Bryant mail 10/18 09:41PM)
change D2434 to SC600000B00,
change D3, D4, D5, D6, D1400, D2106, D2107, D2200, D2401, D2429 to SCS00000Z00,
change C1~C32, C1405~C1436, C1457, C1458 to SE076104K80

10/19
No1, P5, change JXDP1_13 from VGATE to SYS_PWROK
No2, P37, delete JUSB2
No3, P41, add R2234, T2217, T2218
No4, From JM50, P44, change 11 cap from 0.1u to 0.01uF (C2572~C2576, C2578~C2583)
No5, P46, reverse JFAN1 pin derintion
No6, P14, P7, add CLK_CPU_ITP / CLK_CPU_ITP# path
No7, P37, add JUSB2 back (colay)

10/20
No1, From ME, P13, change U4 from SP07000F500 to SP07000QJ00
No2, P33, From JM40, change VGA strap definition
No3, P14, P7, delete 10/19 No6, reserve test point
power circuits JM30_20101020.dsn combined:
No4, P37, From layout request, L2401 swap
No5, P24, add 1 more 330uF for power study
No6, P34, reseve JLVDS1 pin7,8 for COLOR_ENG_EN and DCR
No7, From JM40, P29, P30, change OPT@ to GS@
No8, From JM40, P22 to P33, modify some parts to GS@ and GV@
No9, From JM40, P14, P44, for USB3 wake up function, uninstall R173, R2538, install R2535, C2607, C2608, Y2400
power circuits JM30_20101021.dsn combined:
No10, From JM40, P15, install R197
No11, From JM40, P44, Change USB3.0 power name +3V to +3V_USB3, Change USB3.0 power name +1.05V to +1.05V_USB3
No12, From JM40, P37, P43, ,use ABO Common part, change U2400 and U2411 to AP2301MPG-13_MSOP8 (Follow HW3 Standard Part)

10/21
power circuits JM30_20101021.dsn combined (power revises)
No1, P22, From JM50, delete D1400 and add Q1400
power circuits JM30_20101021.dsn combined (revise +VGFX_CORE jumps)
No2, From JM40,
P33, add U2102 circuits for INVTPWM ESD
P44, add R2637, R2638, R2639, (Follow Vendor suggestion), change power name +3VA to +3VA_USB3
P43, add D2435, D2436, R2640, (Stuff diodes to gate backflow from EC or PPON1)
P39, change U2420.8 from +3VALW to +3VS

No3, P39, change D2431 to 2N7002
No4, P38, add J2 for GND_LVDS for GND noise solution
No5, P39, rename +3VS_GATE to +3VS_WWAN_GATE, and add BT_ON# intersheet
No6, From DRC check, delete some redundant nets
No7, P53, power changes +VGFX_CORE

10/22
No1, P43, From JM50, change D2435 from SCS00000Z00 to SC600000B00
No2, P33, delete 10/21 No 4 (add J2 for GND_LVDS for GND noise solution)
No3, P46, From ME request, add SPY5320200 for open door shut down function
No4, P46, change S1@ to install, S2@ to @
No5, P15, install R197 back
No6, P3, modify BOM config

10/24
No1: update schematics part and footprint: L2406, L2407, D2432, Q2436, D2427, C1130~C1133
No2: P46, change U2407 to AO4430L_SO8 for more power eating

10/25
No1: P41, P42, change netname from BATT_GRN_LED# to BATT_BLUE_LED#
power circuits JM30_20101025.dsn combined
No2: P05, delete XDP and related circuits
No3: P39, swap L2406, L2407
No4: P46, change P/N only: SW2405 _SN400000Z00 (ALPS P/N: SPVS410100)
power circuits JM30_20101025A.dsn combined
No5: From JM40, P13, change SPI ROM (&U1) to SA00003K800

10/27
No1: From JM40, update P/N: PCH SA00004EE10
power circuits JM30_20101027.dsn combined (for VID)

10/29
No1: From JM40, P44, change USB3.0 number to SA000048H00

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date: 2008/08/10	Deciphered Date: 2010/12/31		Title: SCHEMATIC,MB LA-A7121
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: D; Document Number: 4019BI; Rev: A
			Date: Tuesday, December 14, 2010; Sheet 56 of 57

11/10 A phase SMT MEMO and Rework instruction

11/3
No1: P33, change X76@ R1491 samsung 64*16 PD 20K (from 25K)

11/5 SMT MEMO
No2: P33, change VRAM P/N: from SA00003MQ60 to SA00004TQ20, from SA00003VS10 to SA00003YO00
No3: P44, uninstall R2637, R2639, install R2638 for BIOS setting from high active to low active

11/6 rework instruction
No4: P43,44, delete PPON1 signal and change D2435

11/8 rework instruction
No5: P41, add 10K pull high R2235 for EC_PME#

11/10 rework instruction
No6: follow nvidia Johnson Yeh, for N12P-GV strap pin:
below strap setting would need to be changed for N12P-GV-ES
1. ROM_SCLK: pull up 15K ohm.
2. ROM_SO: pull up 10K ohm.
3. STRAP2: pull up 45K ohm.
4. STRAP3: pull down 5K ohm.
5. STRAP4: pull down 10K ohm.
6. STRAP_REF2, need to stuff with 40K ohm 1%.
7. PGOOD (pin E7) stuff 10K ohm.

11/11
No7: From DFB request, P46, change SW2402 to SN100001D10 (P5LM0 design)
No8: From JM40, change JUSB1 to TopYang DC021011051

11/12
No9: P41, delete colay EC BIOS ROM U2203
No10: P41, P46, Follow JM40 design, add EAPD signal for MUTE function in EC common code
No11: P34, change reserved JUSB2 P/N
power circuits JM30_2010-11-12A-FOR DCIN CONNECTOR.dsn combined

11/15
No12: P46; P34, change JUSBF1 P/N to SP01000G000 (28 pin), and add DMIC_CLK, DMIC_DATA;
change JLVDS1 pin definition, but later should confirm with JM40/50
No13: P46, change JFAN1 P/N to SP02000H900 and swap pin definition
No8: JUSB1 footprint change because not sync up with ME

11/16
No14, P39,, change JWLAN1 pin definition: delete pin 17,19, 8, 10, 12, 14, 16;
P17, and delete R249 for no-use PCI CLK to WLAN
No8: change JUSB1 to TopYang DC021011051 and use DC021011050 footprint
No15, P37, delete JUSB6
No16, P43, change C2595 to SGA00002N80

11/19
No17, P43, add ON/OFF pull high R2467 to +3VALW_EC and unmount R2466
No18, From connector list v28, P43, JUSB3 to DC233000G00
No19, P46, (1) delete Open door shut down key (move to sub board), add 1 connector for this function;
(2) change reset key function, delete unmounted components
No20, P18, For VGA sequence logic, add circuits to DGPU_PWROK, and from pull high to pull low

11/24
No21, P44, To avoid leakage, delete R2638 0 ohm and add D2418
No22, P46, add H2414 7P0

11/25
No23, P44, To avoid SMIB leakage, Follow JM40 to do this circuit
No24, P14, reserve SMBUS 0 ohm: R396, R397, R398, R399

11/26
No25, P43, revise USB3.0 function table
power circuits JM30_20101125.dsn combined

11/29
No26, P18, modify No20, delete VGA_PWROK path and add PMOS
No27, P46, modify P19, add pack unpop parts, and reserve 0 ohm test resistor for open door function, use S1@ and S2@ to distinguish them
No28, P17, delete VGA_ON pull high
No29, P44, Modify No23, add pull low, change 2N7002
No30, P15, Follow JM40, change R210 to PCH_RSMRST#_R instead of PCH_RSMRST#
No31, P22, Follow JM40, change R1464_PU location from R1496.2 to Q1400.3
power circuits JM30_20101129.dsn combined
No32, P41, change Board ID:R2230 8.2K
No33, P34, From JM50, for LVDS rise sequence, change R2102 from 1K to 10K, change C2100 from 0.047u to 4.7U

11/30
No34, P18, modify VGA sequence - using 2 NMOS
No35, P46, modify reset and shut down function - delete S1@ and S2@ optional

12/1
No36, Follow JM40 2nd source,
D2101, D2105 change to SCS00003H00
D2417, D2427, D2435 change to SC100001K00
C186, C1459, C1473, C1474, C1477, C1478, C1484, C1485, C1498, C1506, C1510, C1515, C1538, C1539,
C1540, C1541, C1566, C1567, C1568, C1569, C1577, C1578, C1579, C1580, C1603, C2466 change to SE000000K80

No37, P34, 46, add EMI solution for DMIC_CLK, DMIC_DATA
power circuits JM30_20101201.dsn combined
No38, P46, From JM40, modify reset button
No39, P45, From JM40, change Q2415 to SB000007O10
No40, From JM40, due to common parts "AND", change U10, U11 to SA00000OH00
No41, add +3VS_CARD 0 ohm for power consumption measurement
new power circuits JM30_20101201.dsn combined again

12/3
No42, P46, Follow JM40add 3V_LAN MOS to separate 3VALW

date	Func.	No.	Page	
12/8	BOM change	No43		Change SB0000003J10 to SB0000QJ200
	description	No44	P33	VRAM hynix 128*16 --> SA00003Y020 VRAM samsung 64*16 --> value 0011
	design change	No45	P46	For DC power consumption and pwer sequence, change R2485 to 100K, R2490 to 200K, R2496 to 750K
	BOM change	No46	P17	change C1317 from @ to BT@
12/9	design change	No47	P33	N12P-GV QS DevID: 0x1050, 1. ROM_SCLK: pull up 5K ohm. 2. STRAP2: pull down 5K ohm. 3. ROM_SO: pull up 10K ohm. 4. STRAP3: pull down 5K ohm. 5. STRAP4: pull down 10K ohm. 6. STRAP_REF2, need to stuff with 40K ohm 1%. 7. PGOOD (pin E7) stuff 10K ohm. STRAP0: as same as N12P-GS with 45K pull up. STRAP1: pull down 35K as N12P-GS
should change later				
			P17	for VGA_ON pull high deleted, need to arrange RP instead R

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/08/10	Deciphered Date	2010/12/31

Title	SCHEMATIC,MB LA-A7121		
Size D	Document Number 4019BI		Rev A
Date: Tuesday, December 14, 2010		Sheet 57 of 57	