

Compal Confidential

Schematics Document

Intel Huron River

Sandy Bridge with Cougar Point core logic

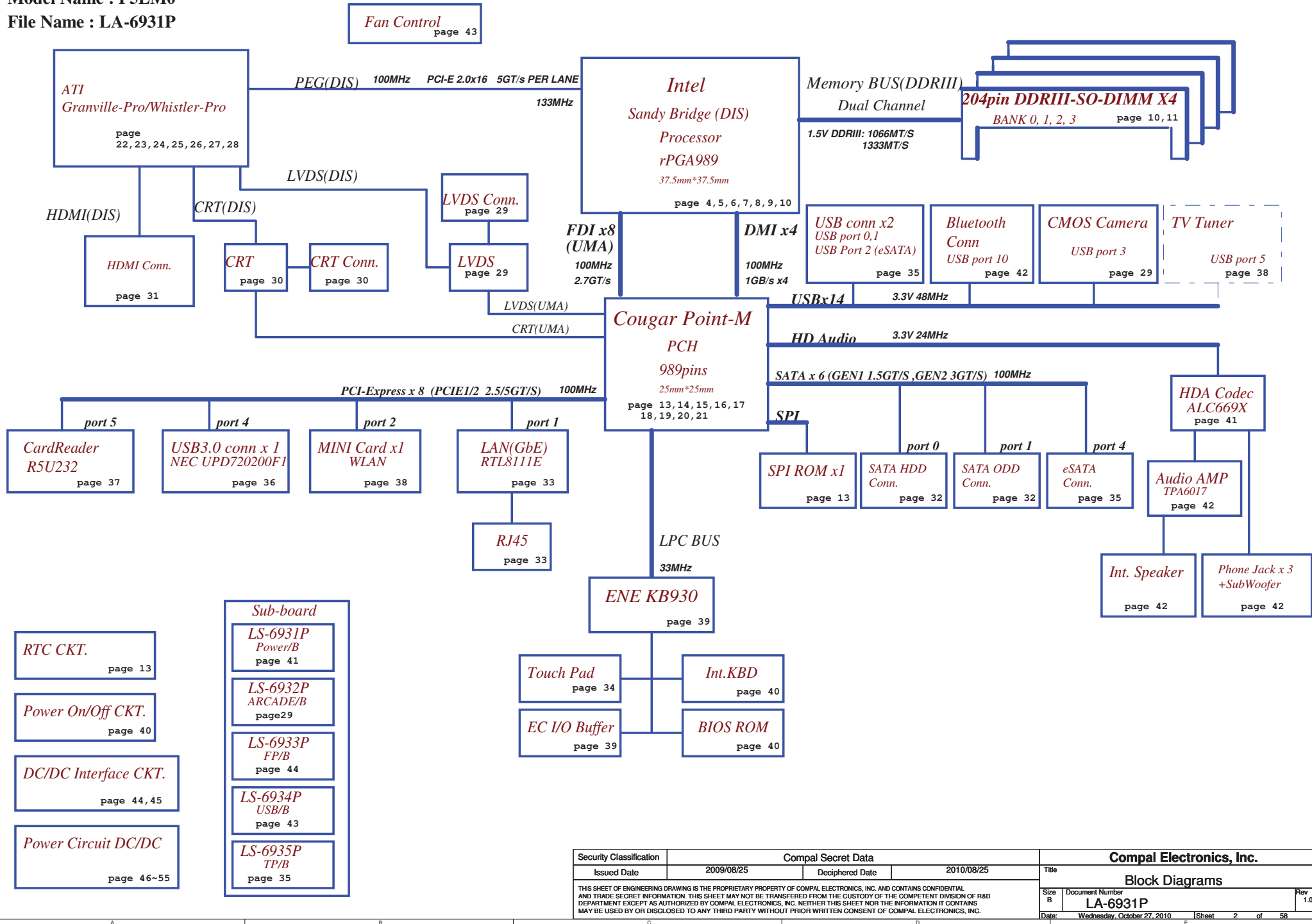
2010-10-27

REV:1.0

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Model Name : P5LM0
File Name : LA-6931P



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Voltage Rails

Power Plane	Description	S1	S3	S5	DGPU (DIS)	IGPU (SG)
VIN	Adapter power supply (19V)	N/A	N/A	N/A		
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A		
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A		
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF		
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF		
+1.05VS_VCCP	1.05V switched power rail for CPU (PCH)	ON	OFF	OFF		
+VGFX_CORE	Core voltage for IGPU	ON	OFF	OFF		
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF		
+1.5VS	1.5V switched power rail	ON	OFF	OFF		
+1.8VS	1.8V switched power rail	ON	OFF	OFF		
+3VALW	3.3V always on power rail	ON	ON	ON*		
+3VALW_PCH	3.3V power rail for PCH	ON	ON	ON*		
+LAN_JO	3.3V power rail for LAN	ON	ON	ON*		
+3VS	3.3V switched power rail	ON	OFF	OFF		
+5VALW	5V always on power rail	ON	ON	ON*		
+5VS	5V switched power rail	ON	OFF	OFF		
+VSB	VSB always on power rail	ON	ON	ON*		
+RTCVCC	RTC power	ON	ON	ON		
+VGA_CORE	5V power rail for GPU	ON	OFF	OFF	ON	OFF
+1.5VSDGPU	1.5V power rail for VRAM	ON	OFF	OFF	ON	OFF
+1.8VSDGPU	1.8V switched power rail for GPU	ON	OFF	OFF	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
--------	---------	--------	---------

Ibex SM Bus address

Device	Address
--------	---------

STATE	SIGNAL				SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON				
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW				
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF				
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF				
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF				

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
* 3	0.4
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
DIS Only	DIS@
Switchable Graphics	SG@
Granville	GRA@
Whistler	WHI@
For CIR	CIR@
USB2.0 bus	USB2@
DDR M1	M1@
DDR M3	M3@
For 45 level	45@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	USB/B
		1	USB Conn.
	UHCI1	2	
		3	
	UHCI2	4	Mini Card 1
		5	Mini Card 2
EHCI2	UHCI3	6	
		7	
	UHCI4	8	USB Conn.
		9	eSATA USB
	UHCI5	10	CMOS Camera
		11	Finger Print
	UHCI6	12	USB3.0 @
		13	Blue Tooth

43 Level BOM Config

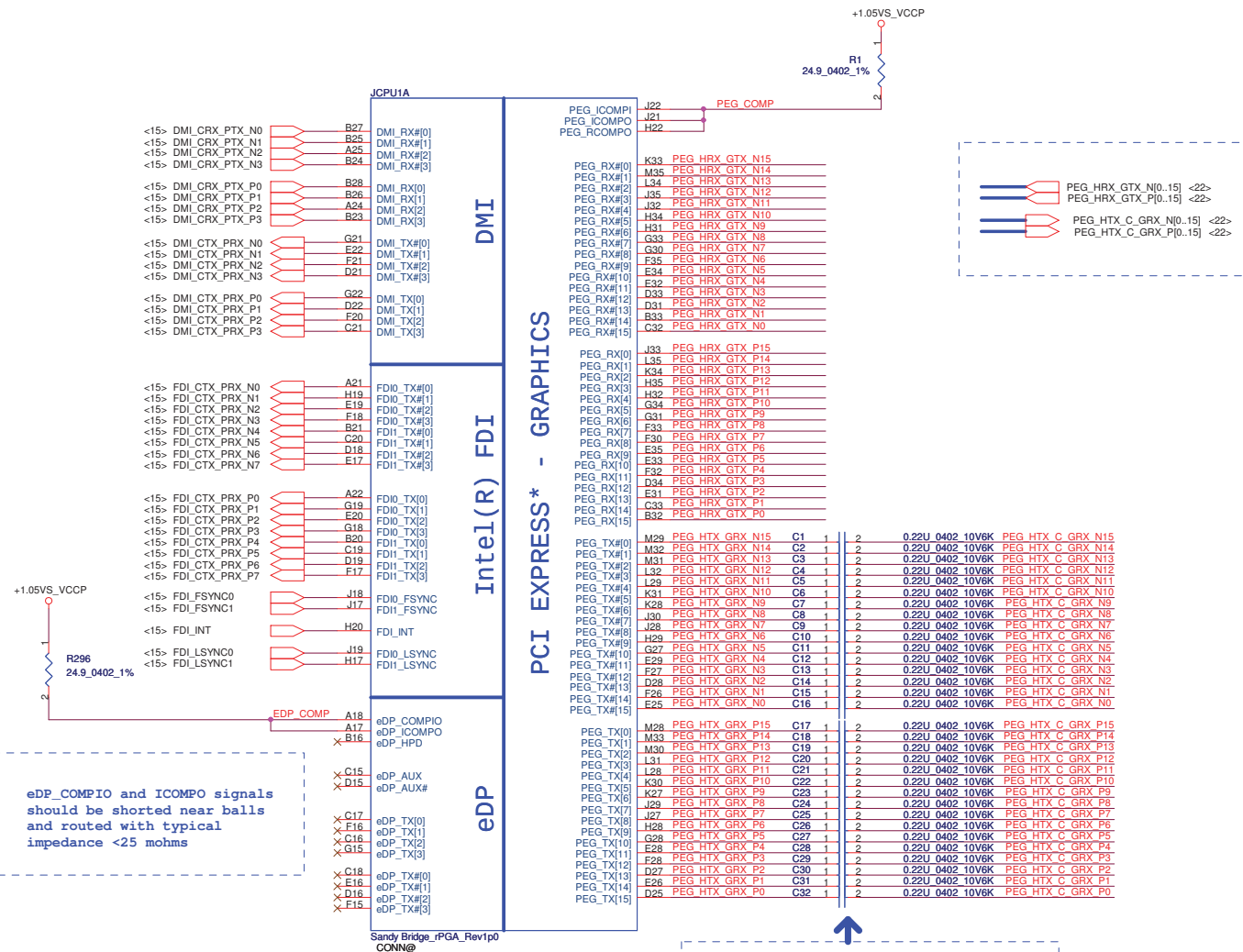
Granville DIS: GRA@ DIS@ CIR@ M1@
Whistler SG: WHI@ SG@ CIR@ M1@

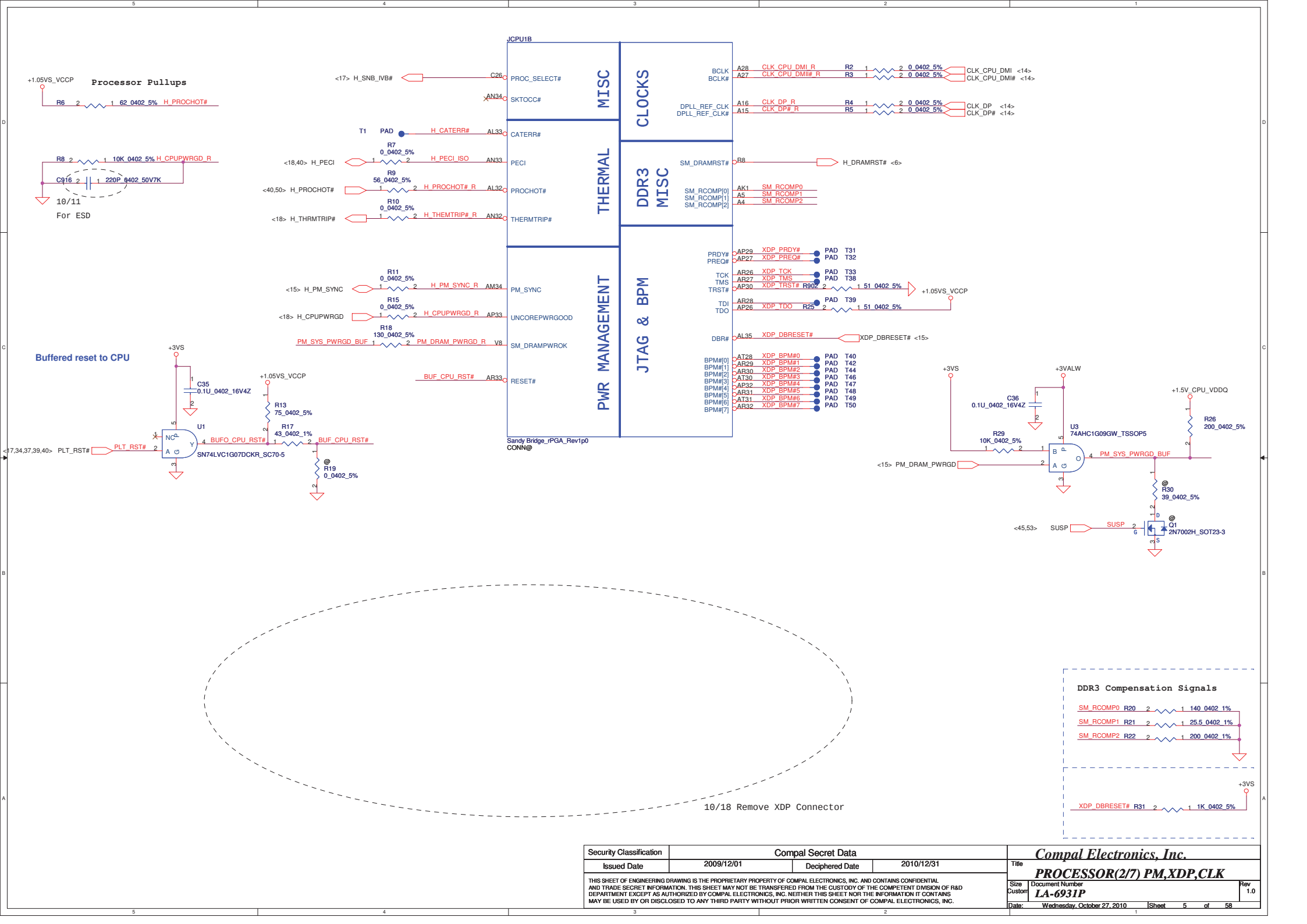
45 Level BOM Config

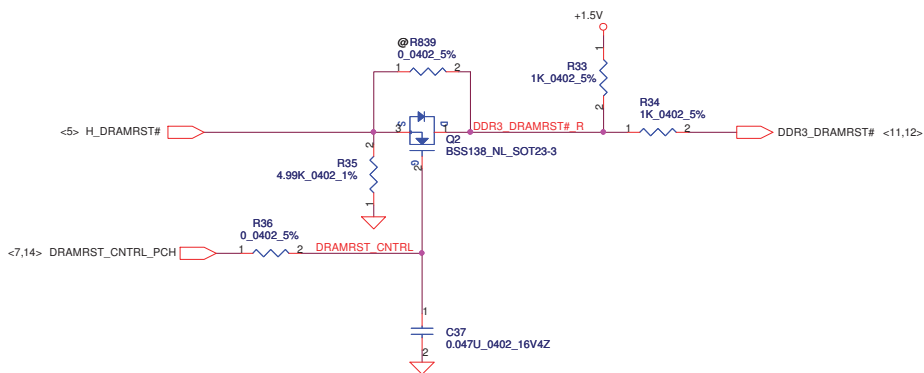
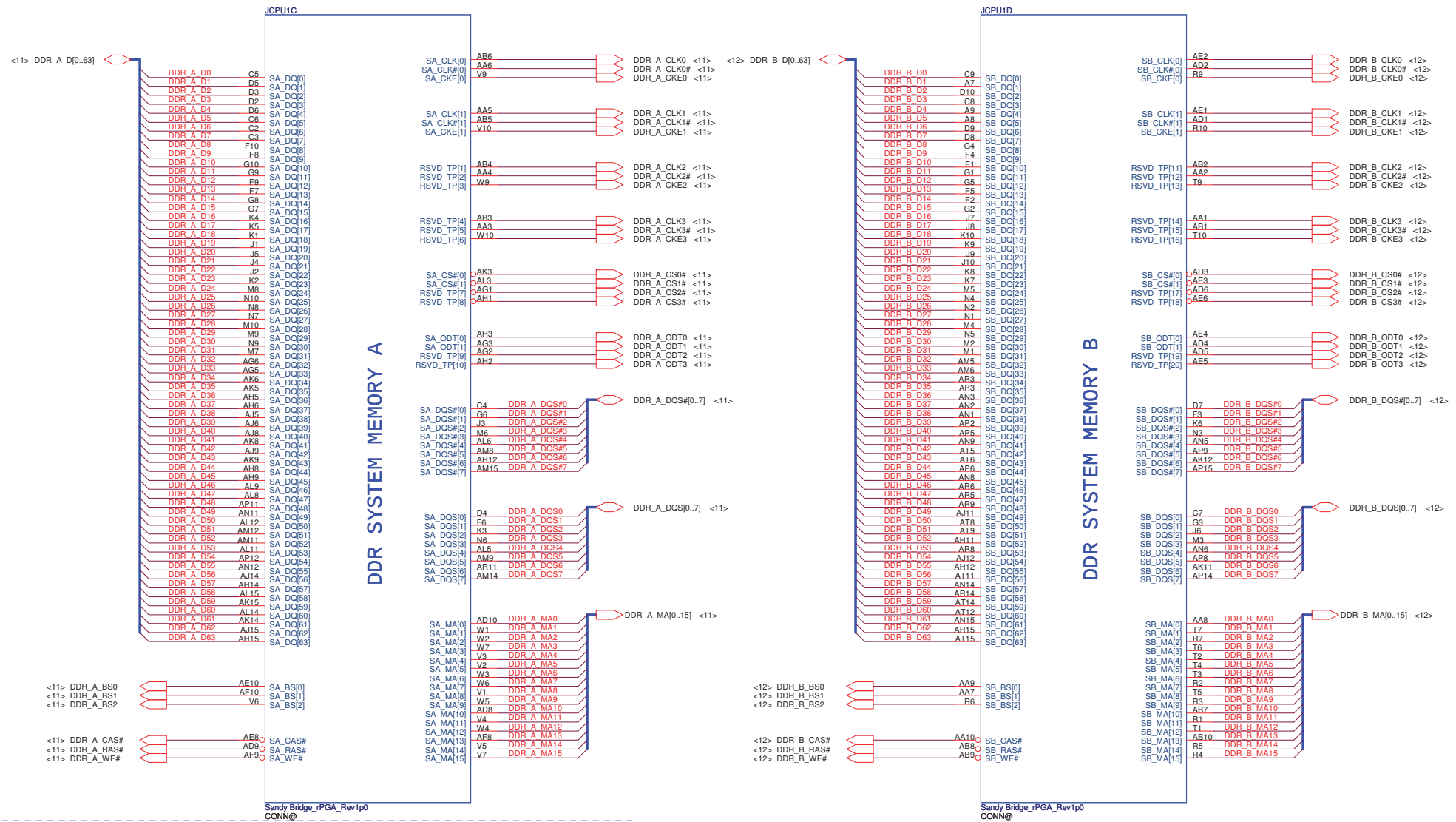
VRAM BOM Config

X76255BOL01: HYNIX 1G (old die)
X76255BOL02 HYNIX 1G (new die)
X76255BOL04 HYNIX 2G

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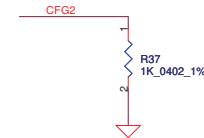




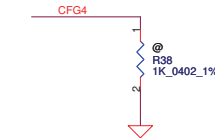


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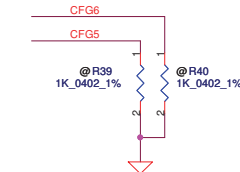
CFG Straps for Processor



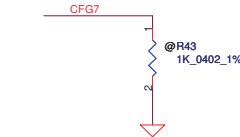
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



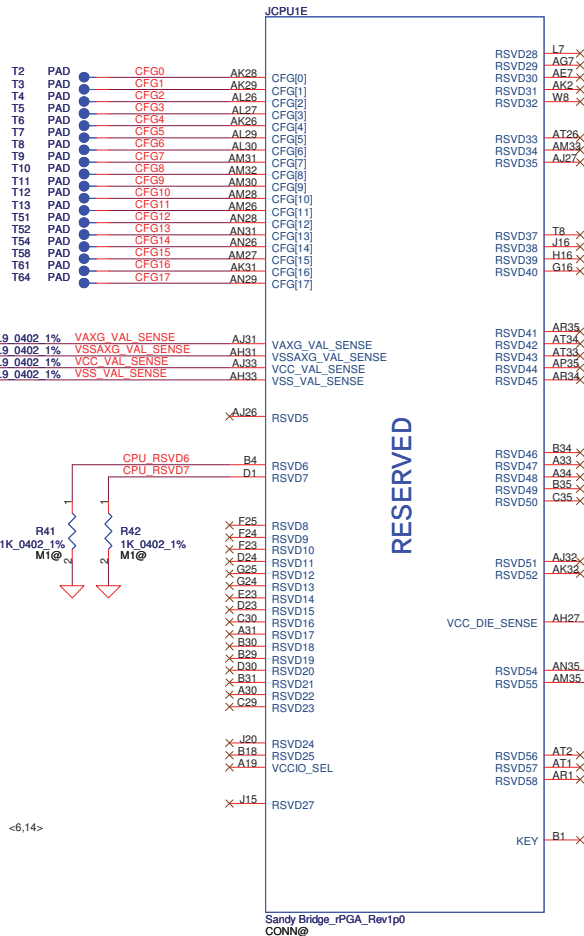
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



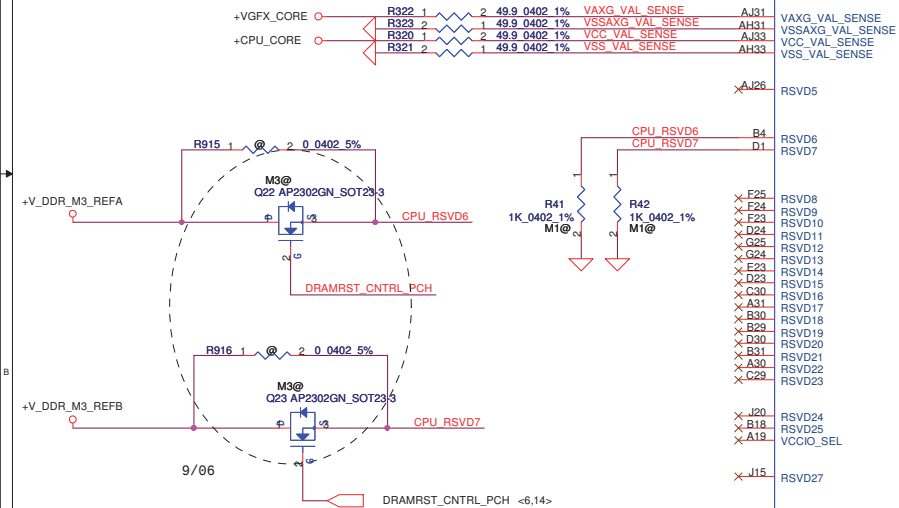
PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

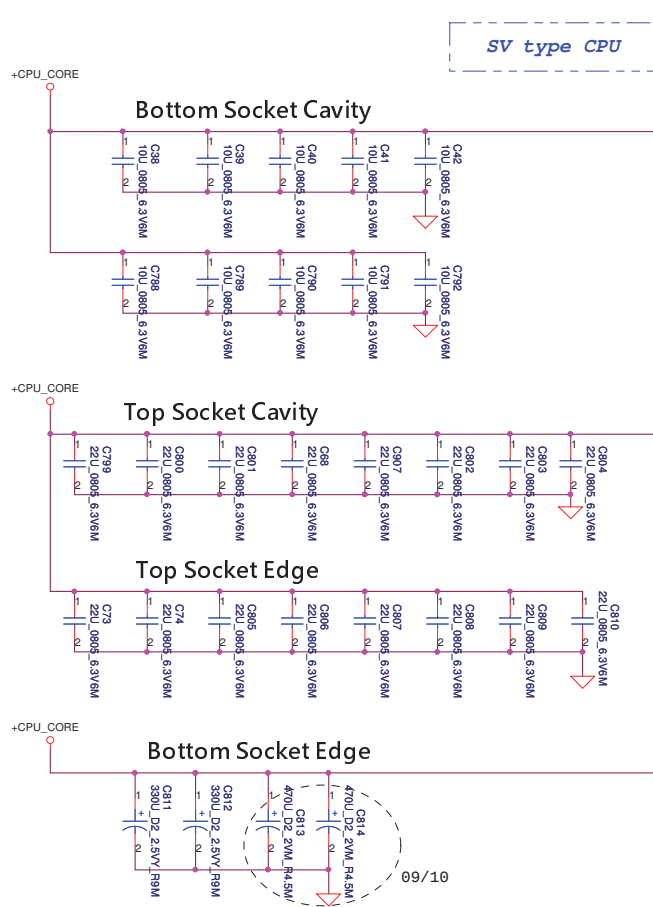


PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



Sandy Bridge_rPGA_Rev1p0
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CPU1F	
AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y34	VCC51
Y33	VCC52
Y32	VCC53
Y31	VCC54
Y30	VCC55
Y29	VCC56
Y28	VCC57
Y27	VCC58
Y26	VCC59
Y25	VCC60
Y24	VCC61
Y23	VCC62
Y22	VCC63
Y21	VCC64
Y20	VCC65
Y19	VCC66
Y18	VCC67
Y17	VCC68
Y16	VCC69
Y15	VCC70
Y14	VCC71
Y13	VCC72
Y12	VCC73
Y11	VCC74
Y10	VCC75
Y09	VCC76
Y08	VCC77
Y07	VCC78
Y06	VCC79
Y05	VCC80
Y04	VCC81
Y03	VCC82
Y02	VCC83
Y01	VCC84
Y00	VCC85
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Y00	VCC98
Y00	VCC99
Y00	VCC100

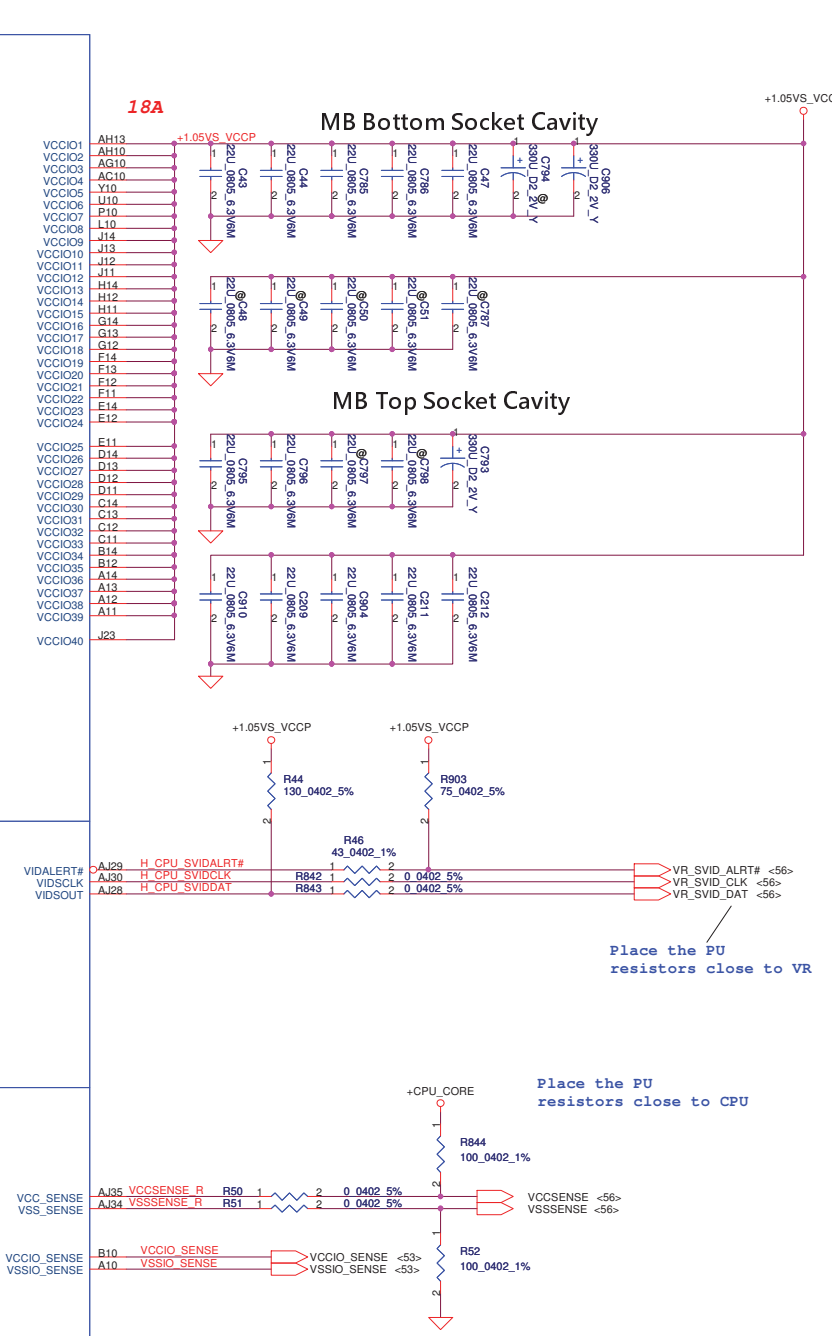
POWER

PEG AND DDR

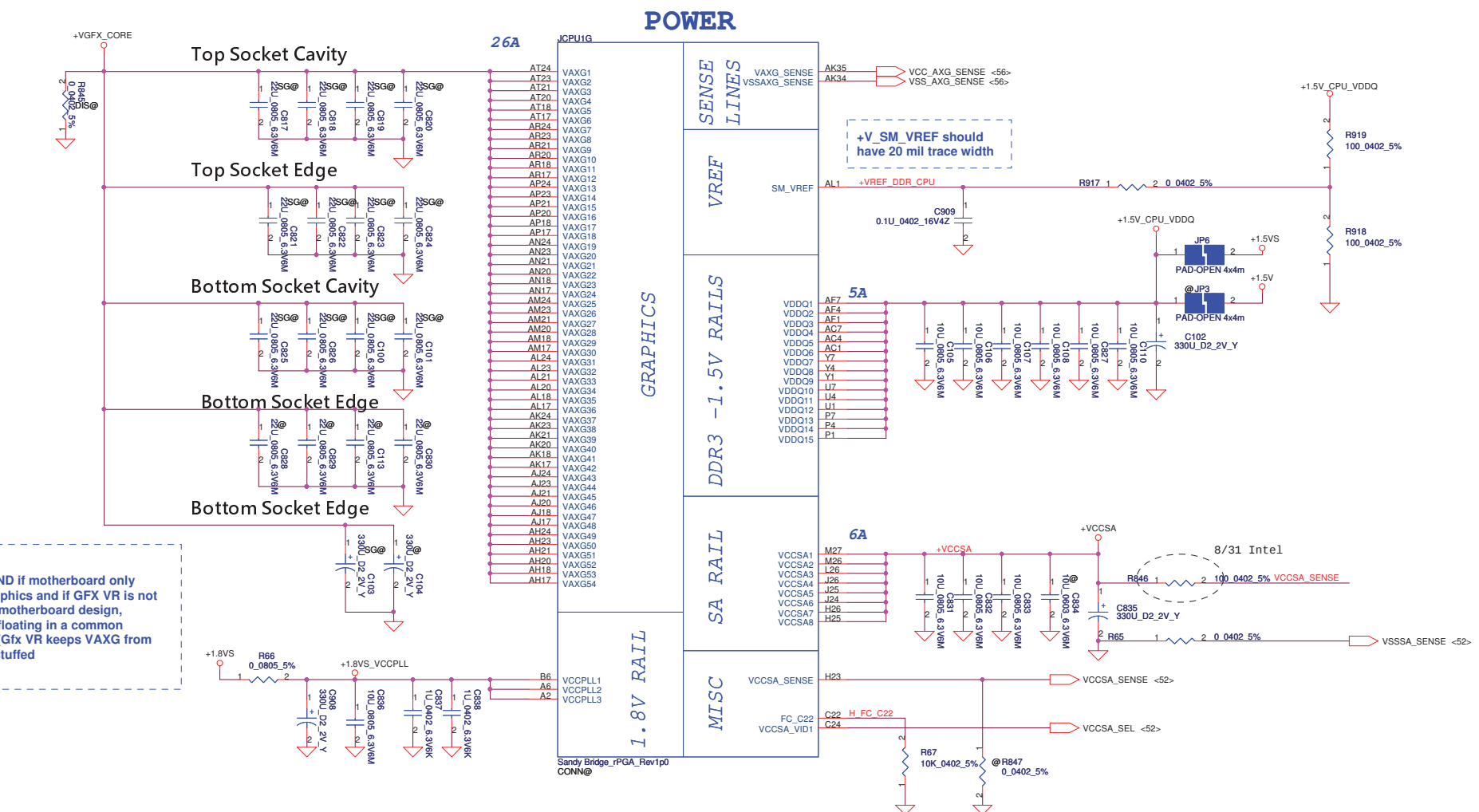
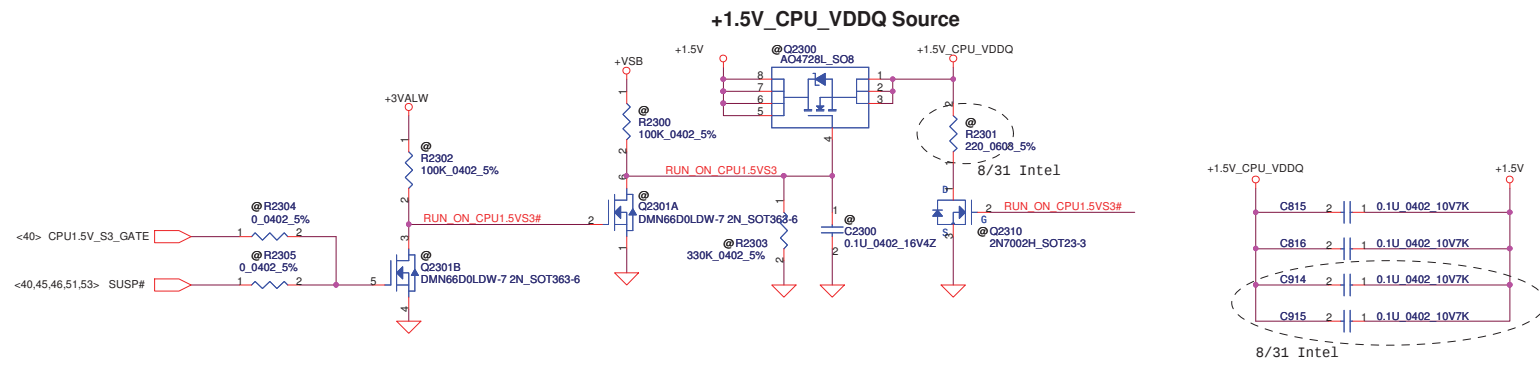
CORE SUPPLY

SVID

SENSE LINES

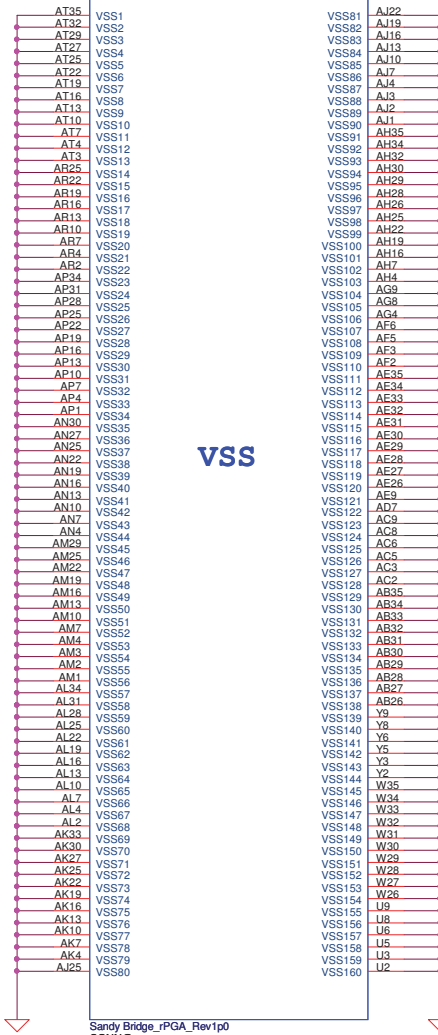


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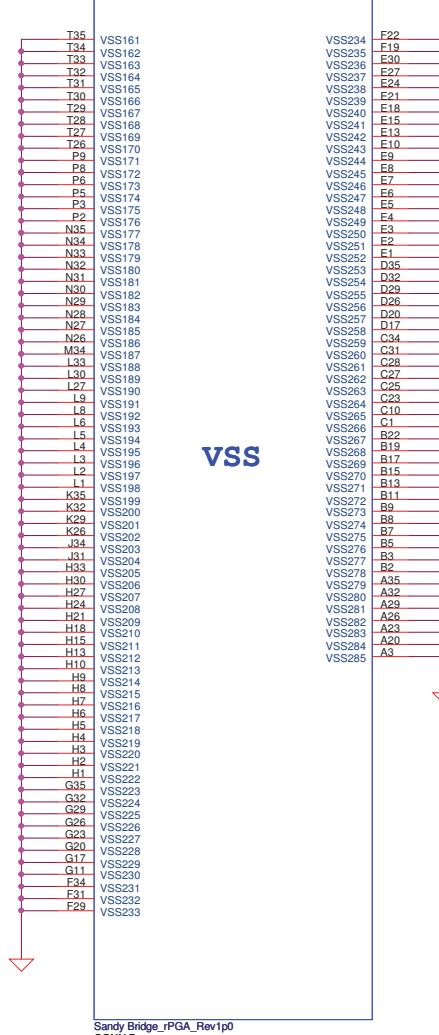
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JCPU1H

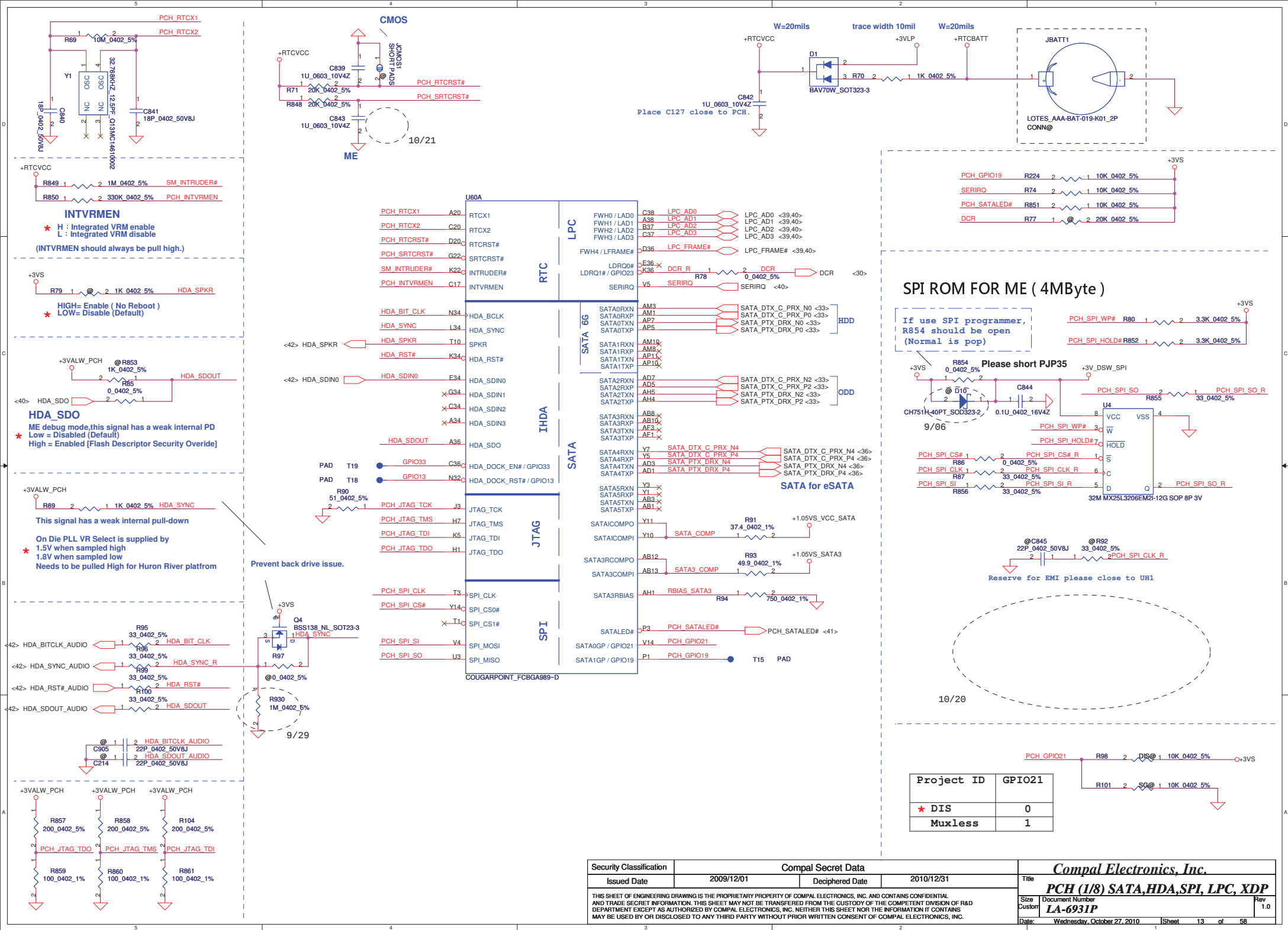


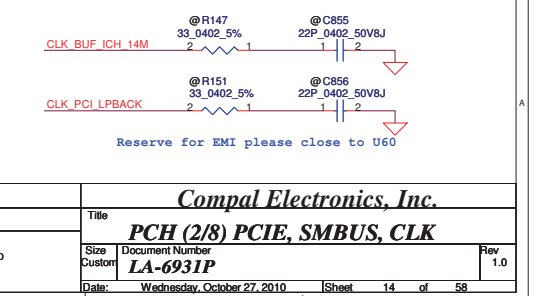
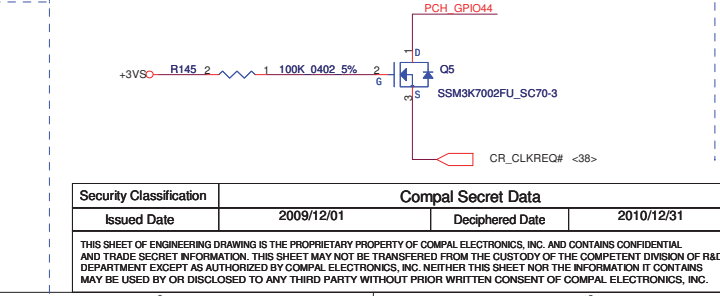
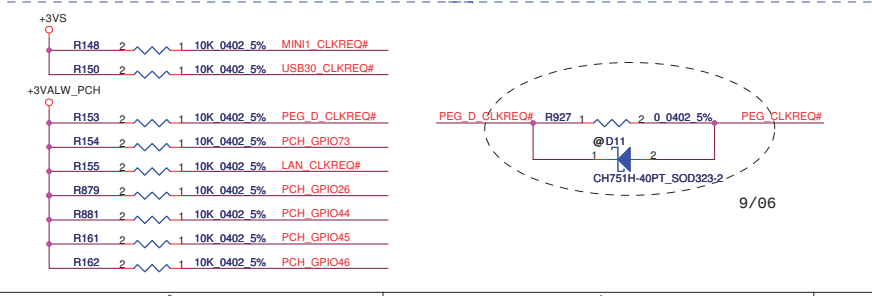
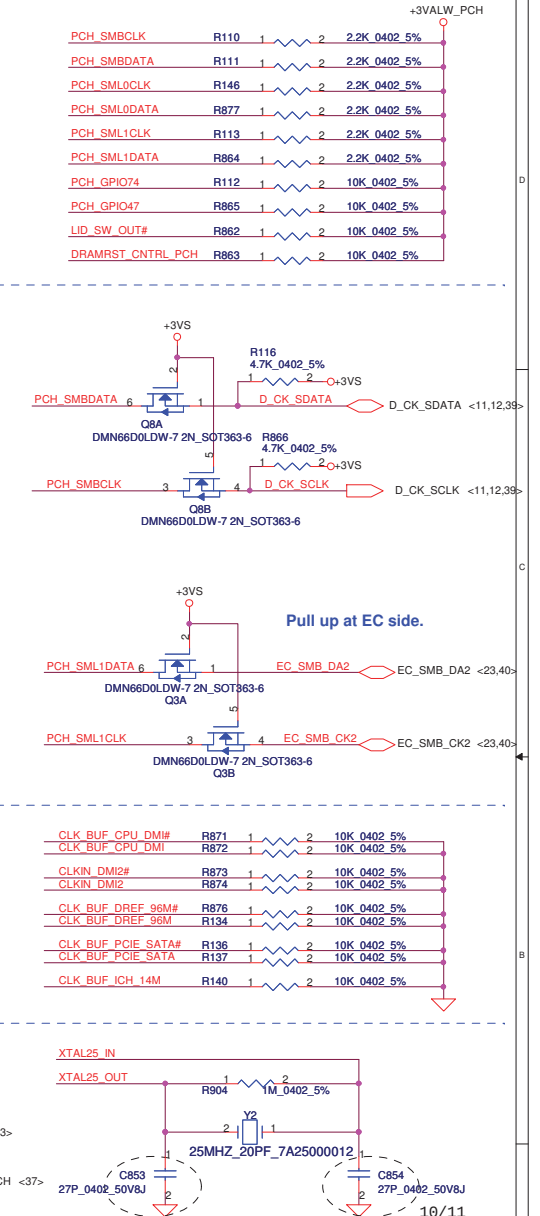
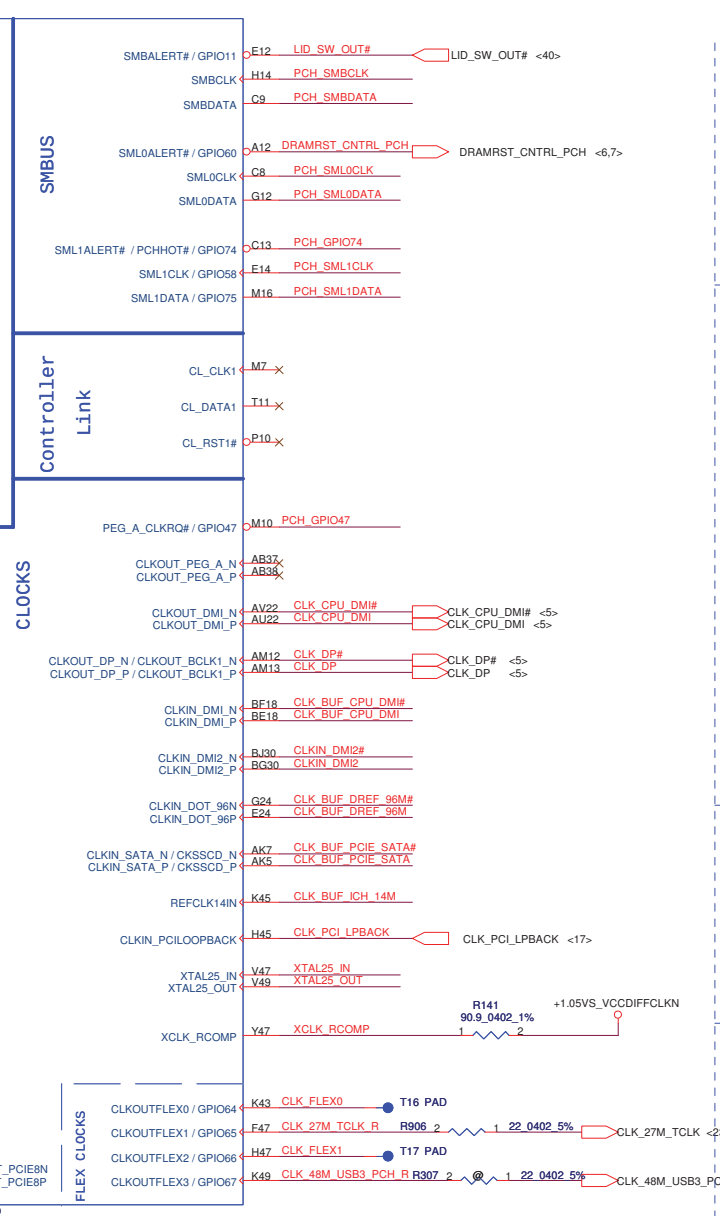
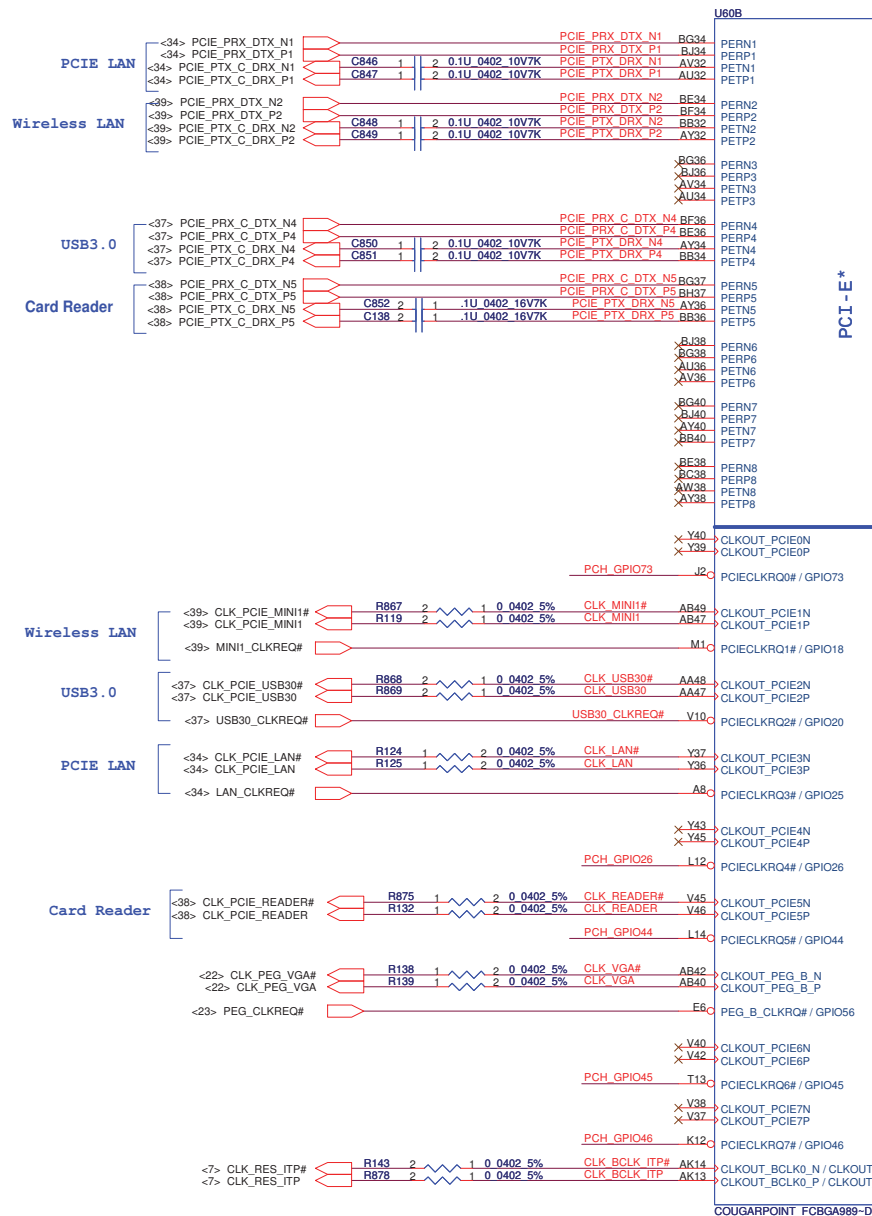
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CONN@

JCPU1I

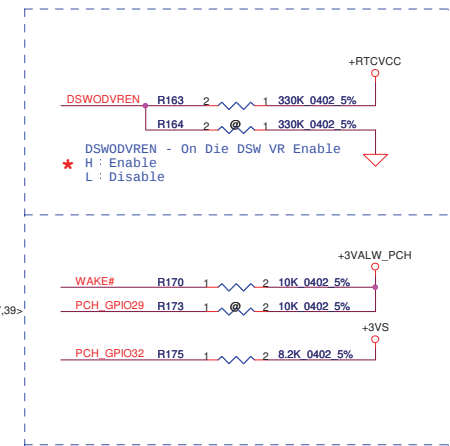
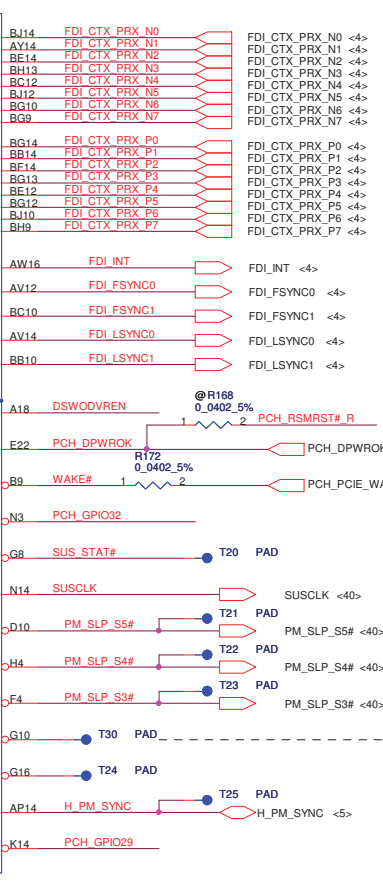
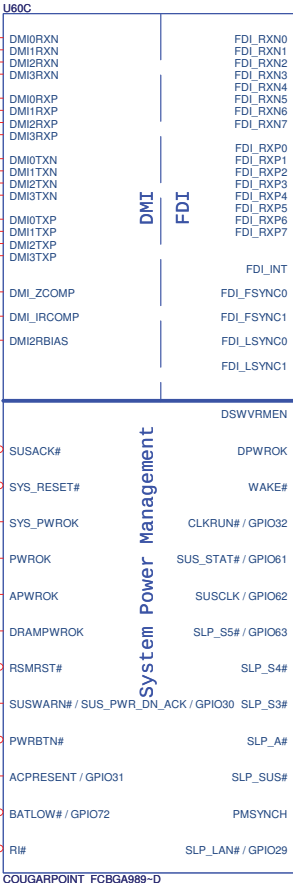
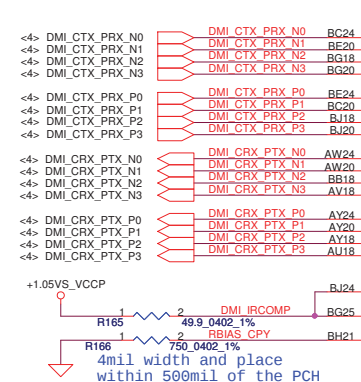
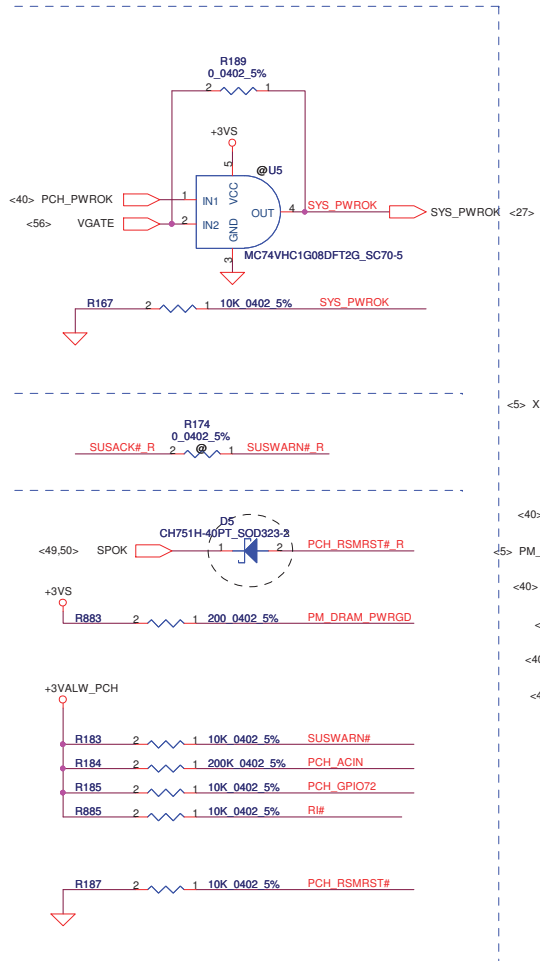


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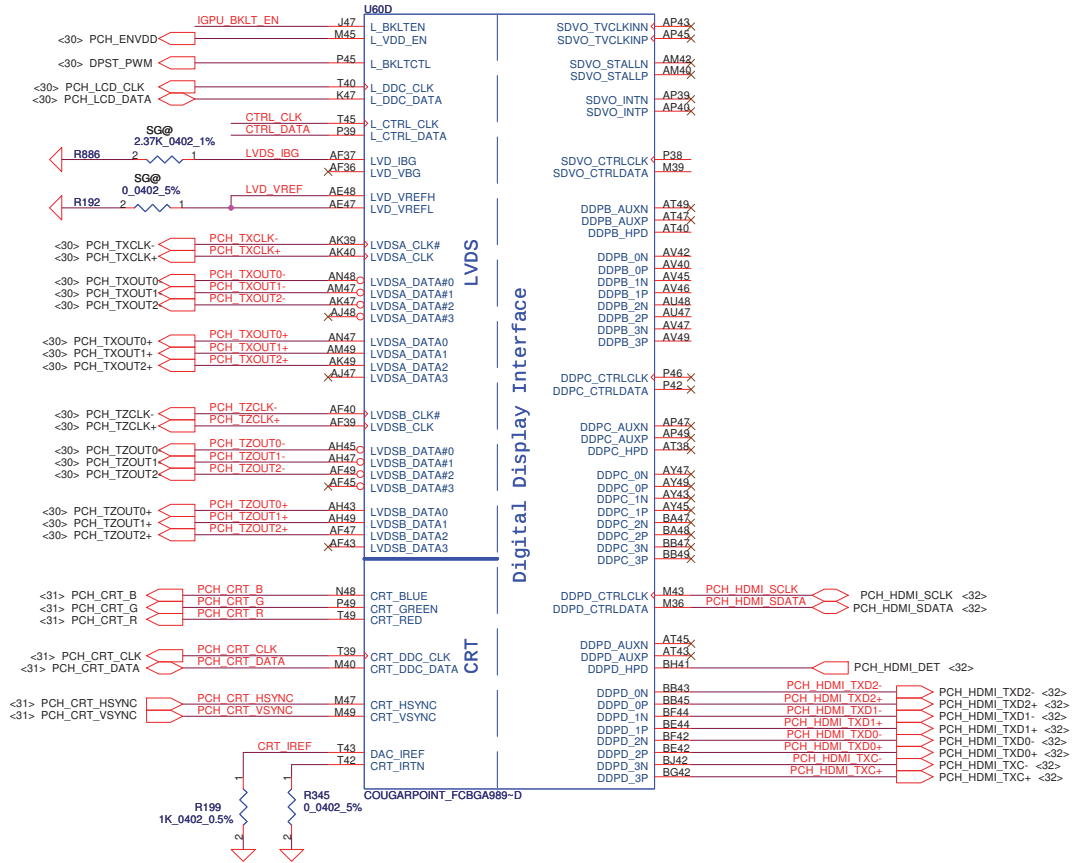
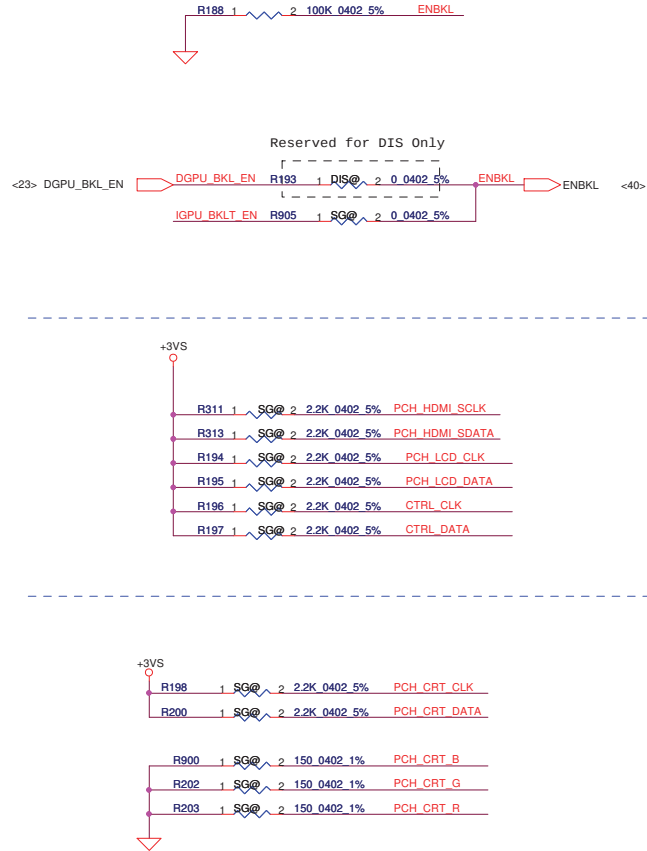




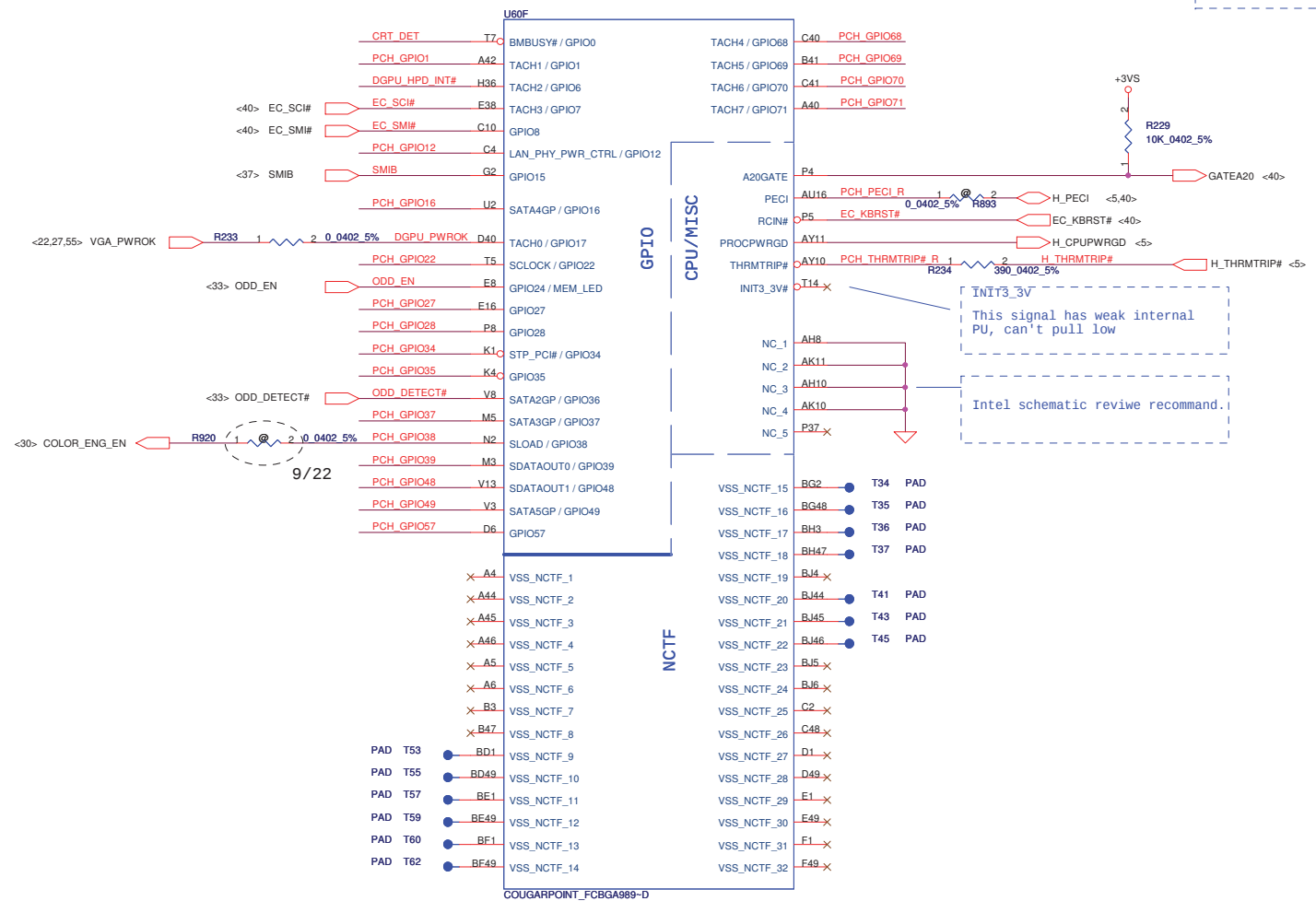
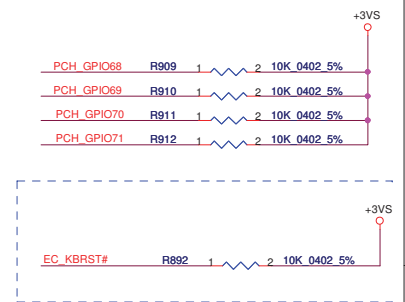
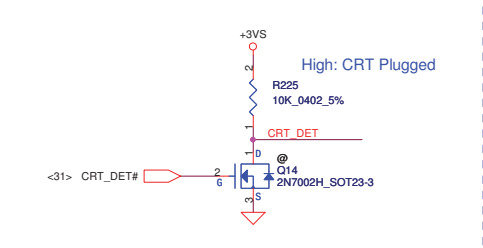
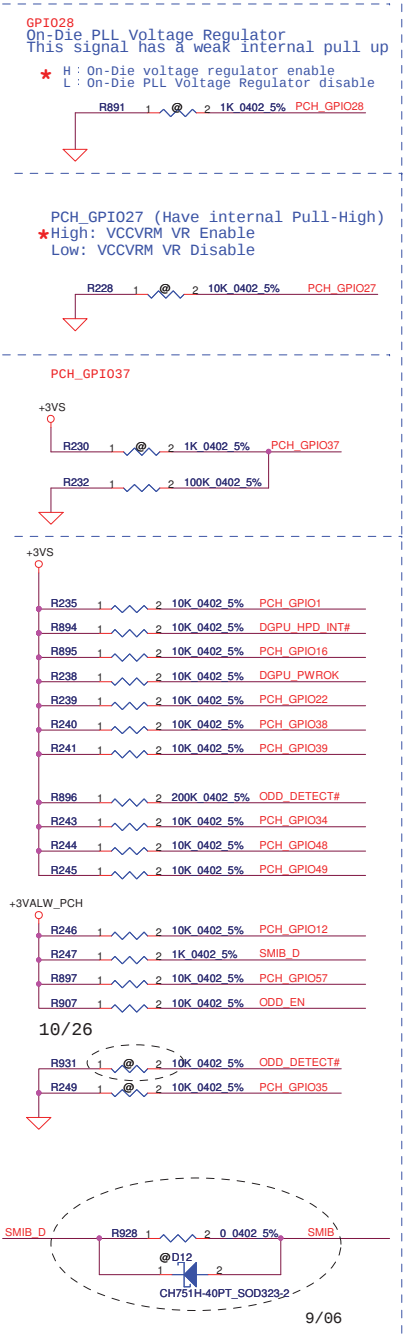
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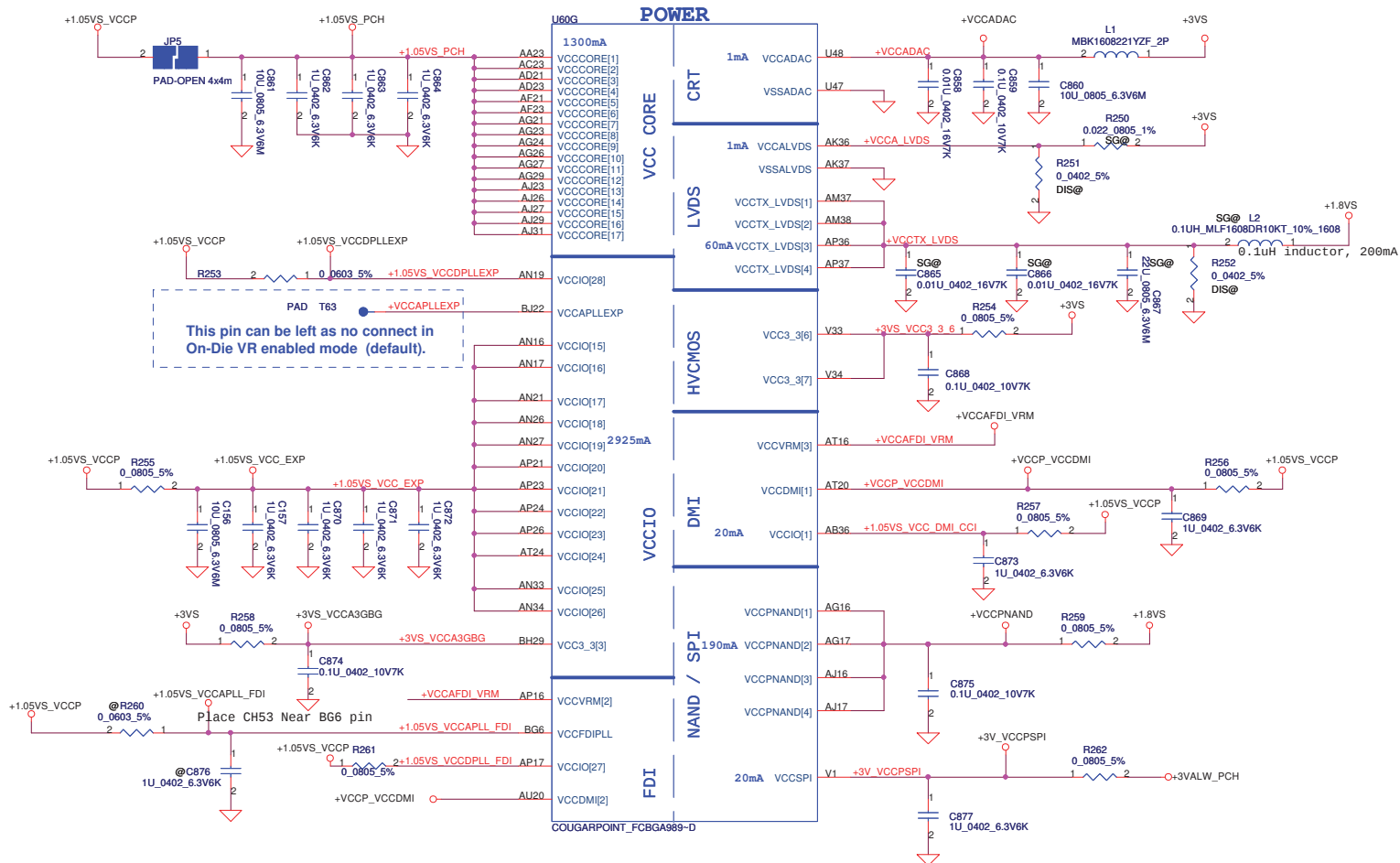
Can be left NC when IAMT is not support on the platform



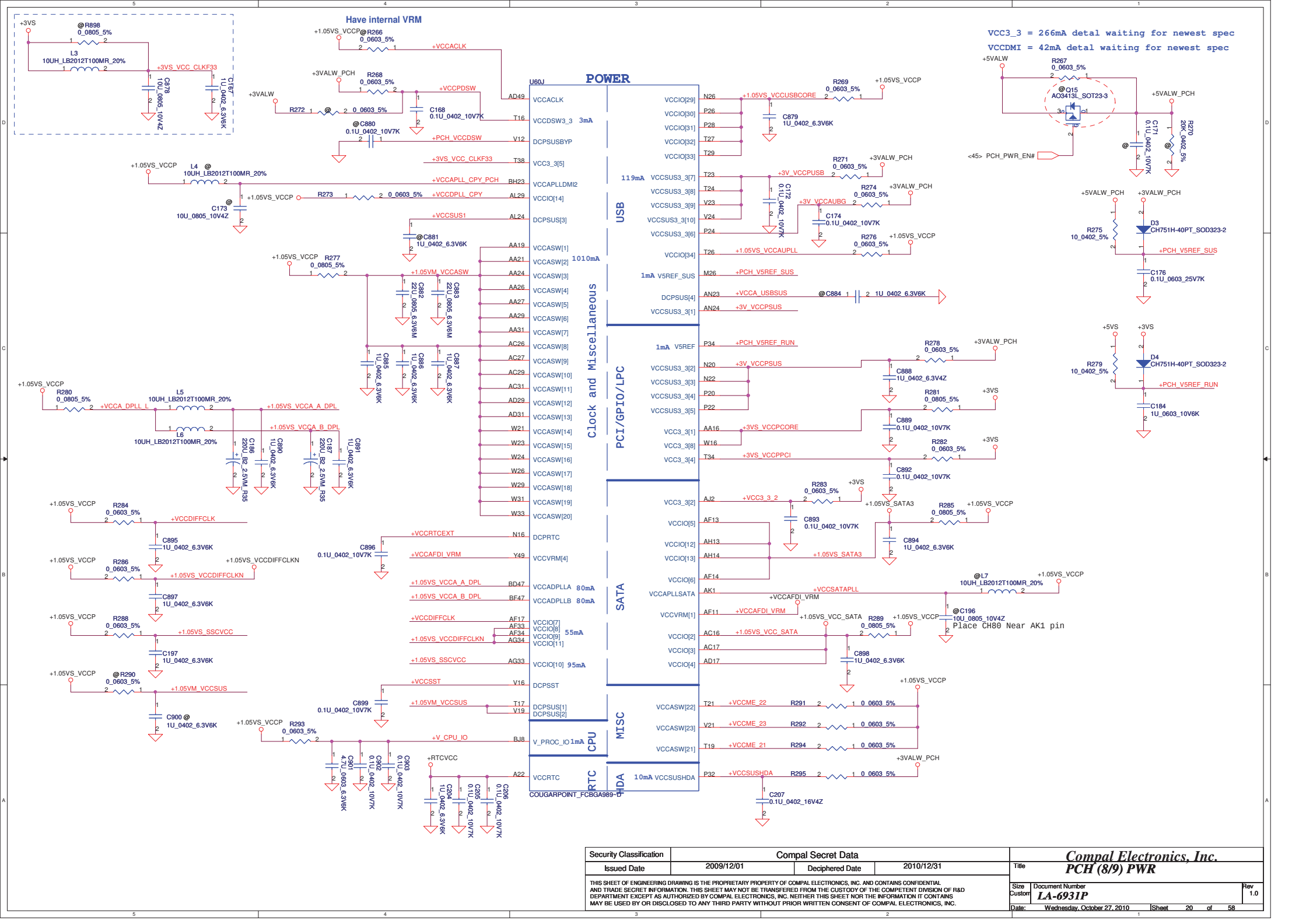
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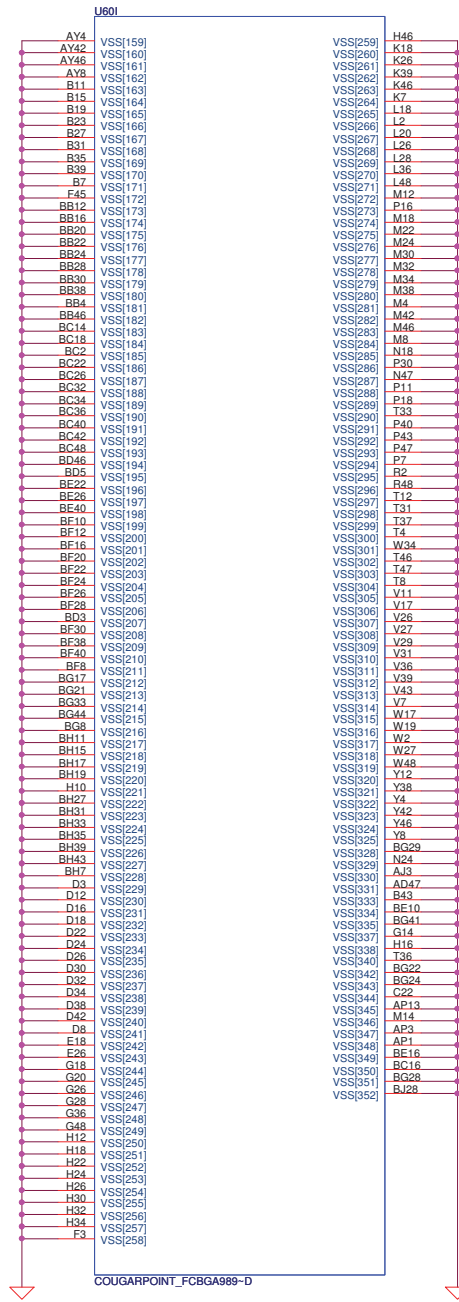
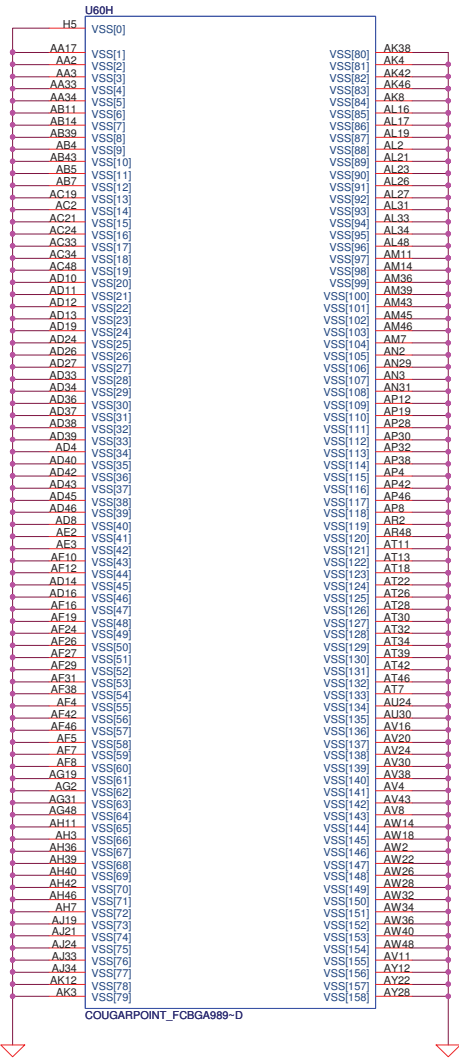


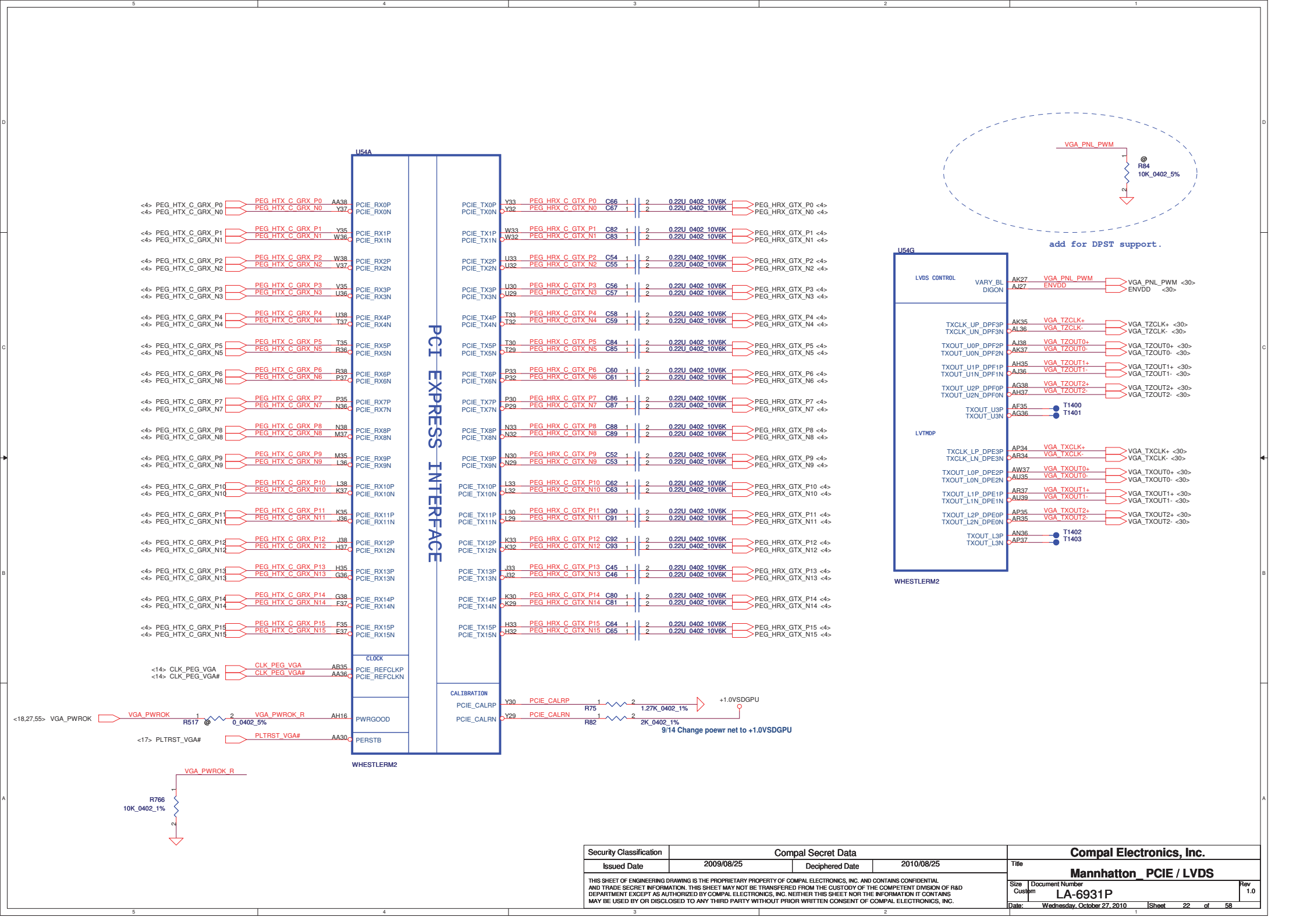
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Size	Custom	Document Number	LA-6931P	Rev	1.0
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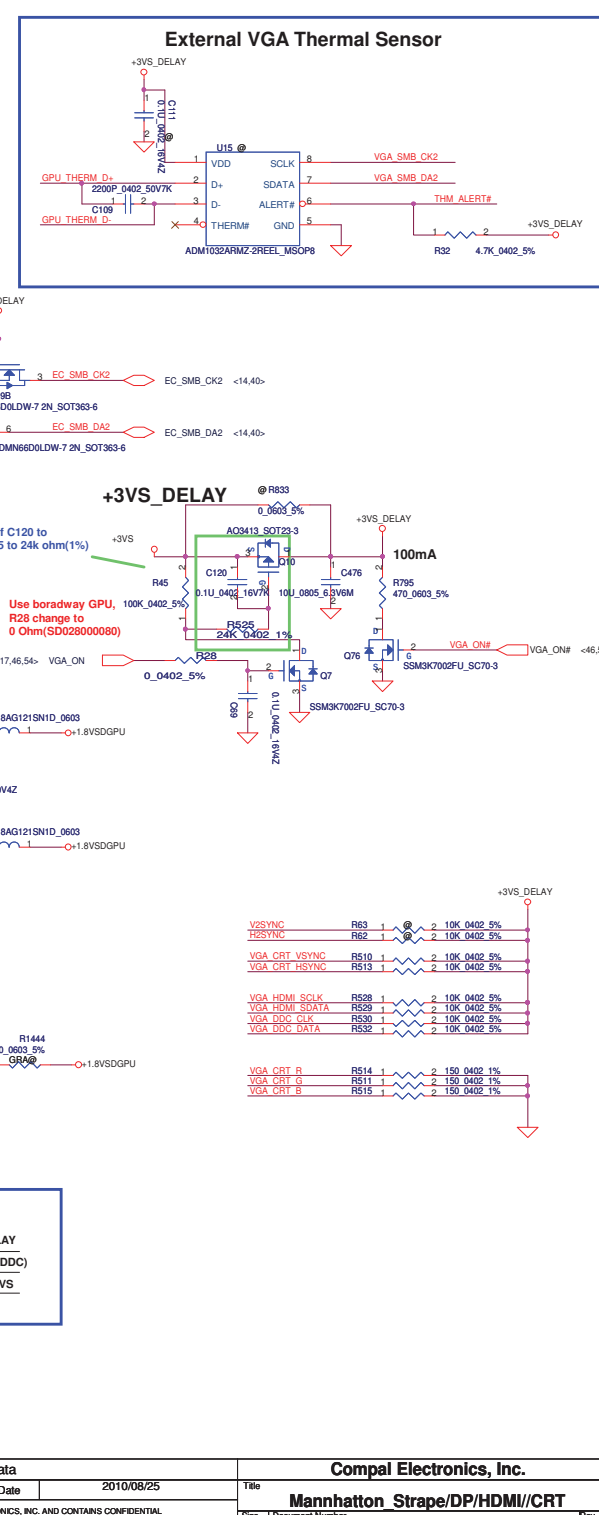
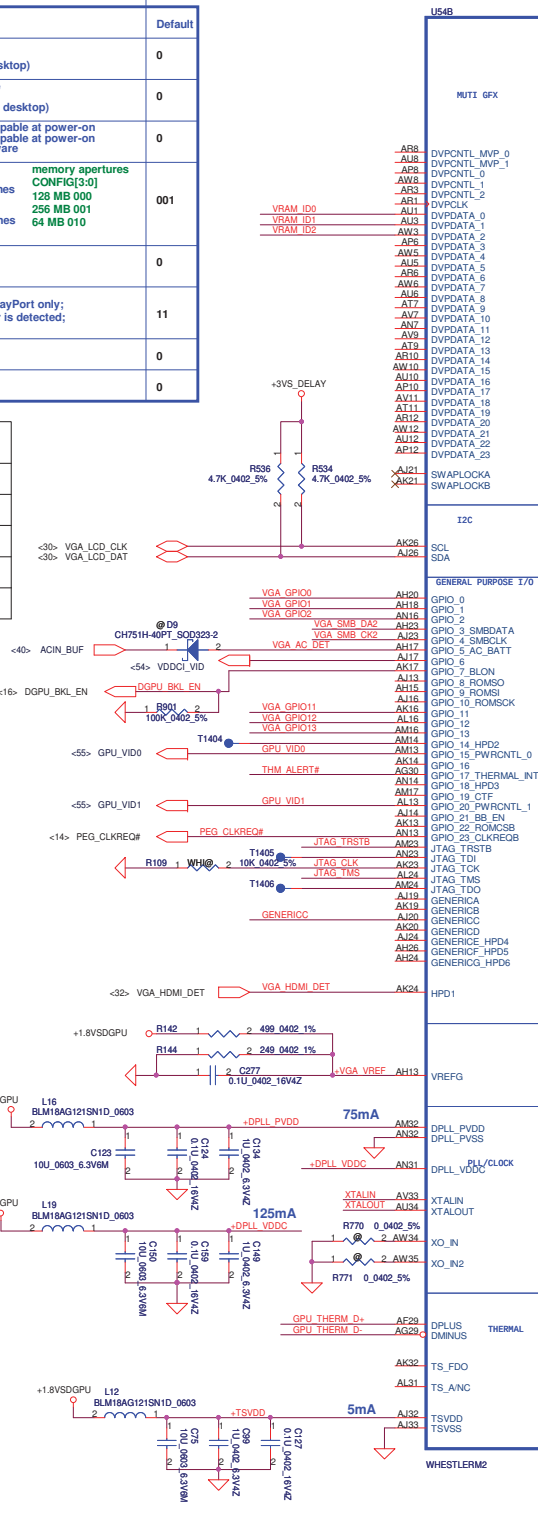
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccLVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



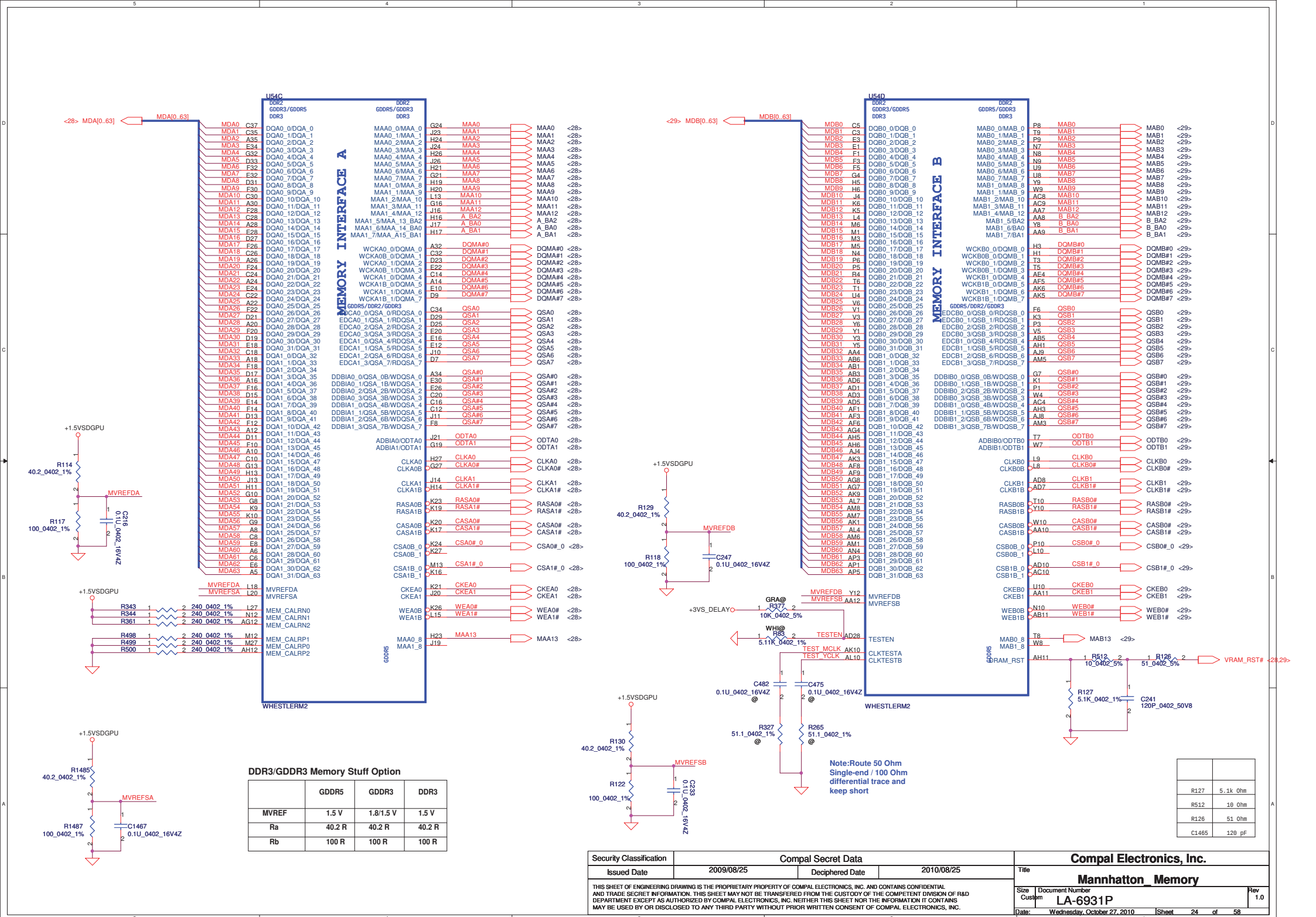


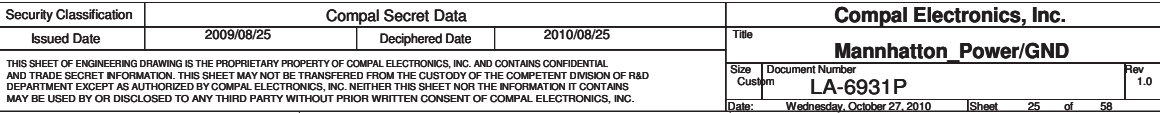


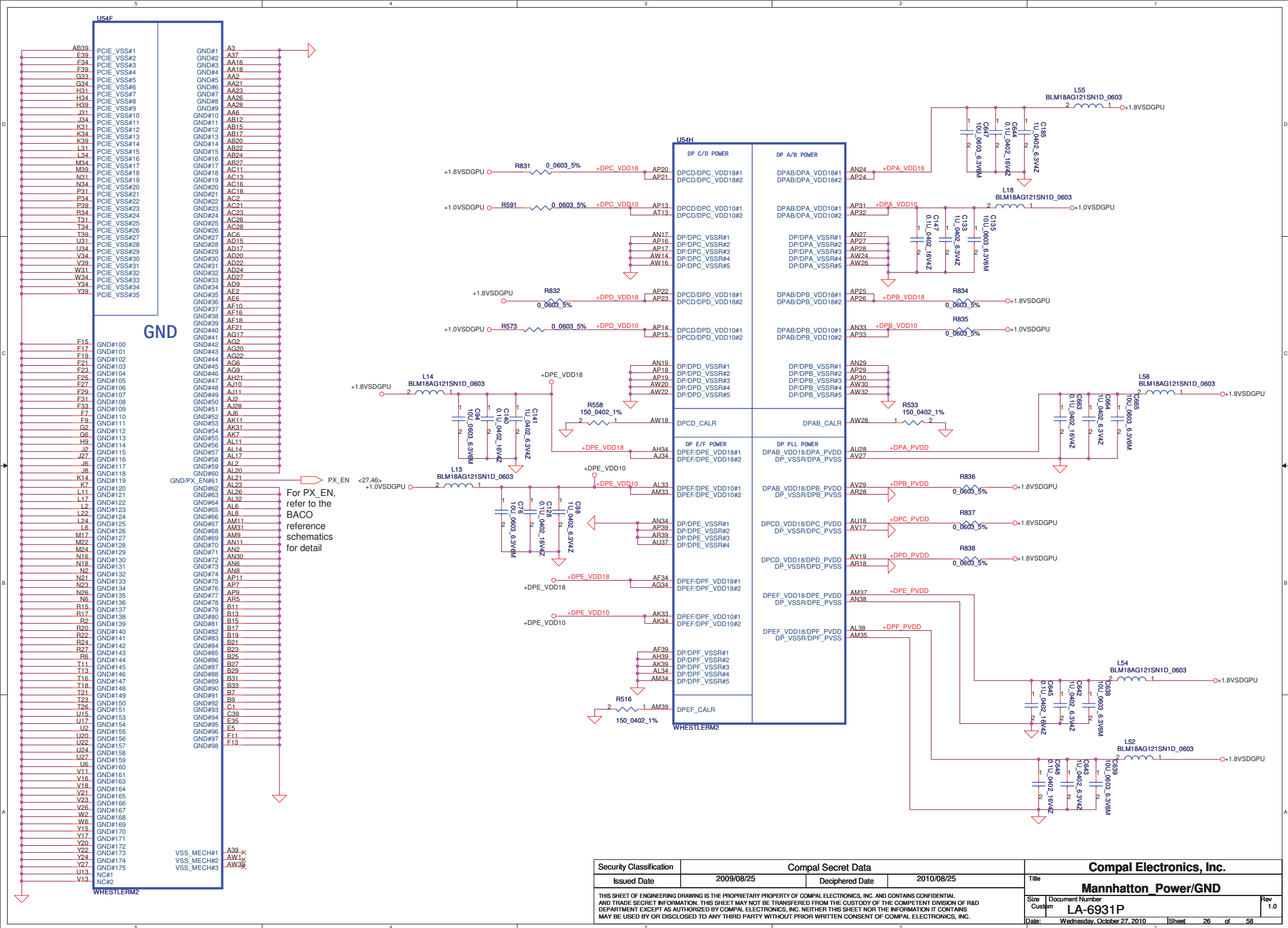
VRAM	Location	VRAM_ID2	VRAM_ID1	VRAM_ID0	
Hynix(8pcs) 1GB (old) H5TQ1G63BFR-12C		O	O	1	
Hynix(8pcs) 1GB (900MHz) H5TQ1G63DFR-11C		O	1	O	
Samsung(8pcs) 1GB (900MHz) K4W1G1646G-BC11 LF		O	1	1	
Hynix(8pcs) 2GB (800MHz) H5TQ2G63BFR-12C		1	O	O	
Samsung(8pcs) 2GB (800MHz) K4W2G1646C-HC12		1	O	1	

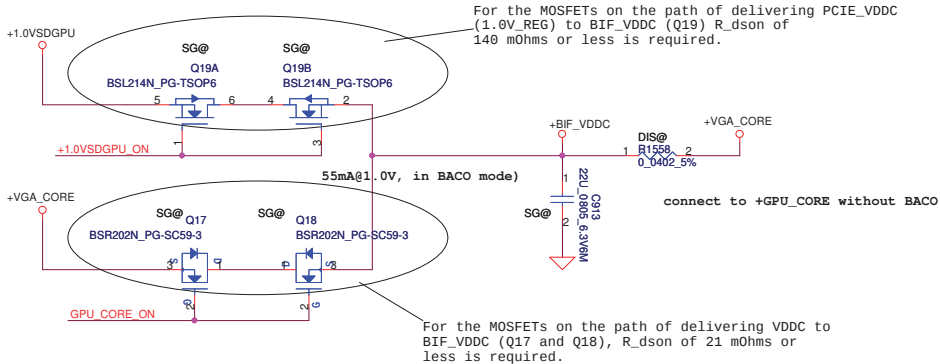
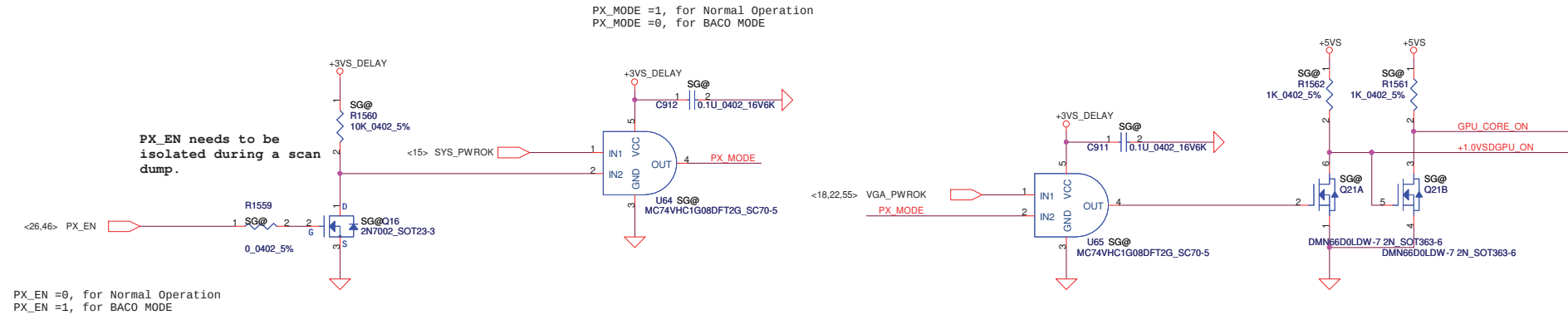


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				Mannhattan Strape/DP/HDMI/CRT			
				Size C Document Number LA-6931P			
Date: Wednesday, October 27, 2010				Sheet 23 of 58			

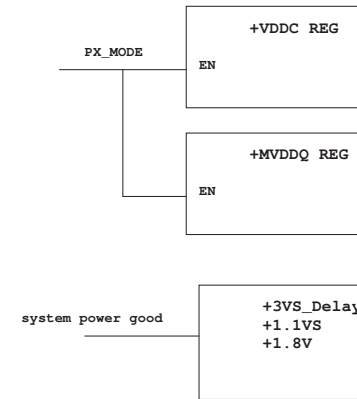






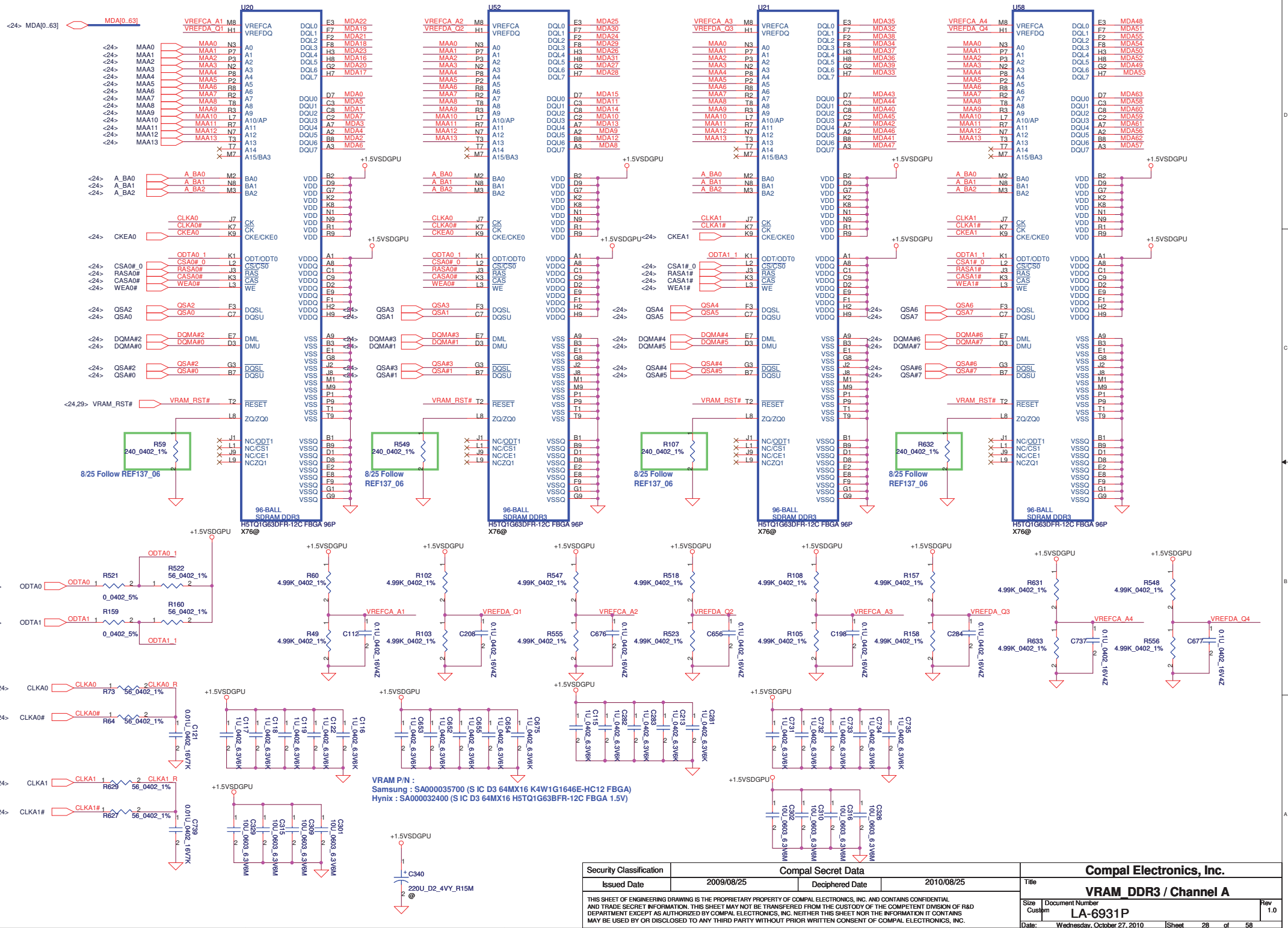


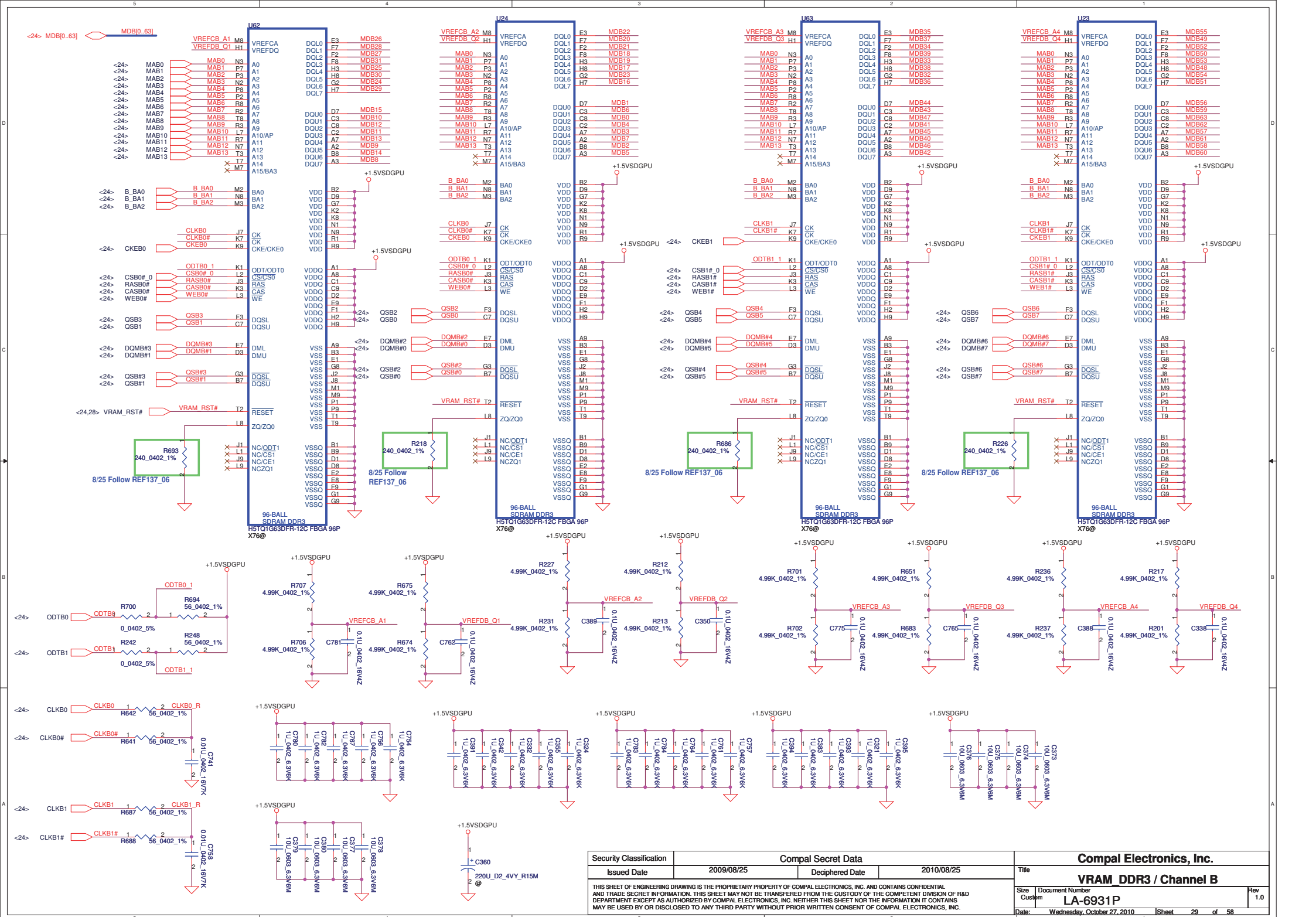
	Voltage	In BACO mode
VDDR1	1.5V	OFF
VDDC/VDDCI	0.85-1.15V	OFF
others		ON



power on sequence:
(1) +3VS_Delay ----> +VDDC ----> +1.8VS
(> 0ms) (reach 90%)
(2) +3VS_Delay ----> +1.8VS ----> +VDDC
(> 0ms) (reach 90%)

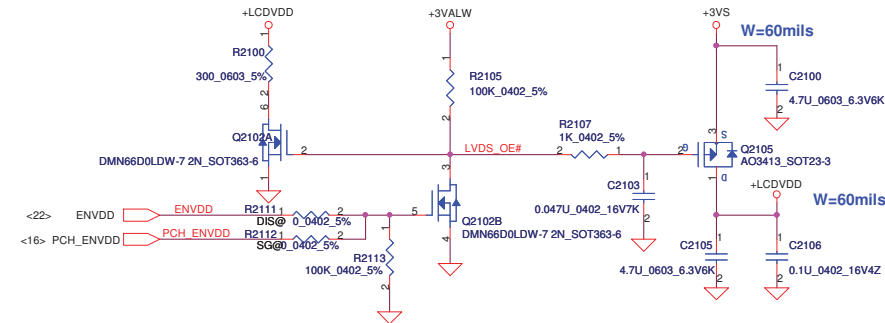
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				Document Number LA-6931P
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				Date: Wednesday, October 27, 2010
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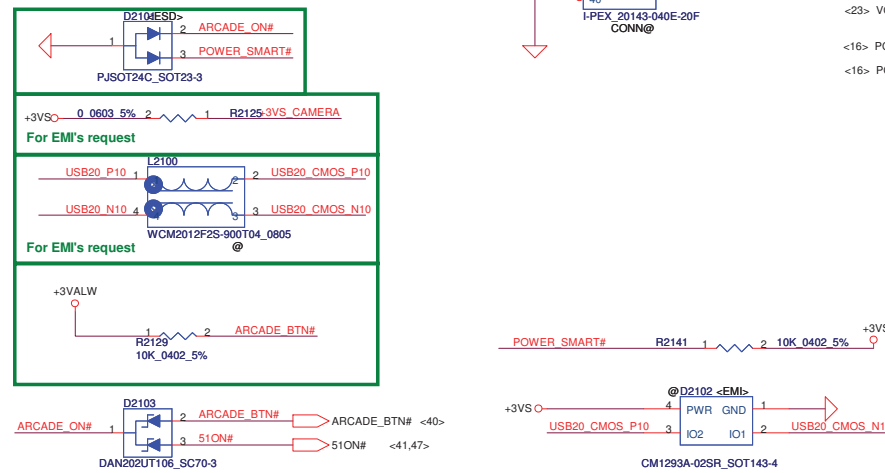
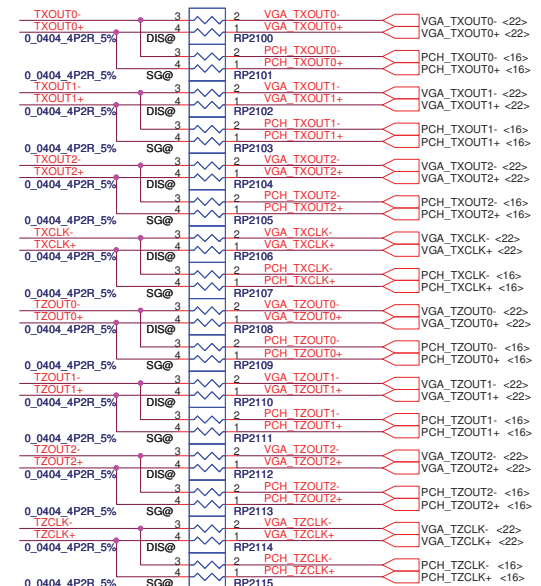
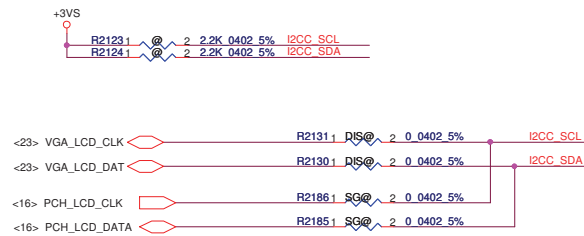
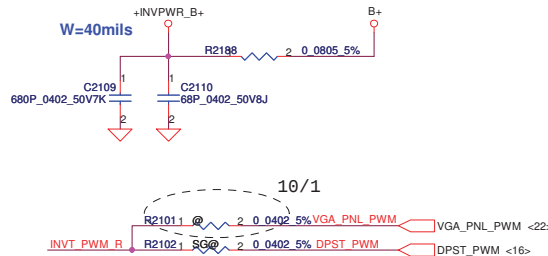
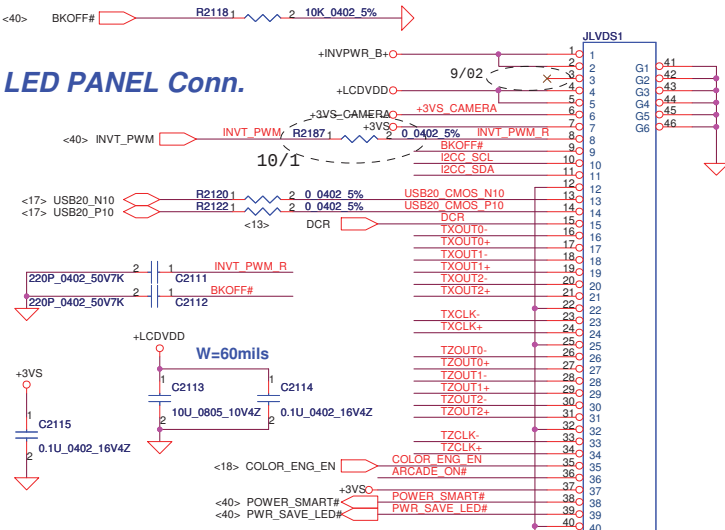


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						Size	Document Number		Rev
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LCD POWER CIRCUIT

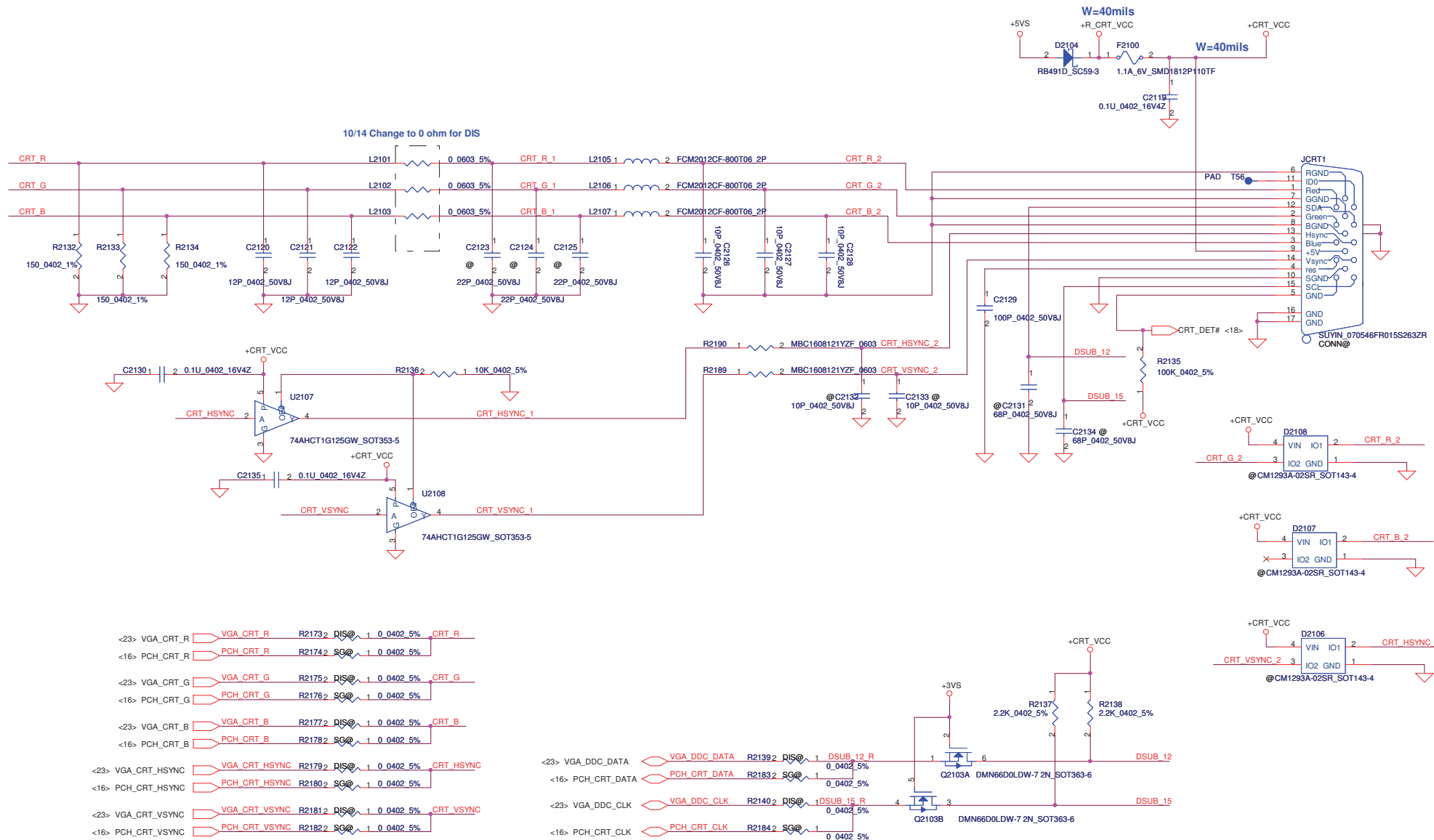


LED PANEL Conn.

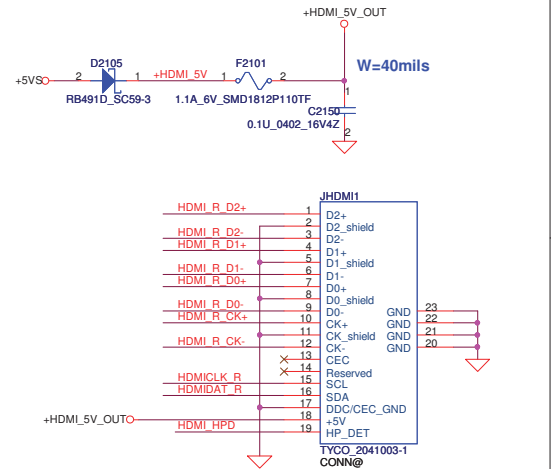
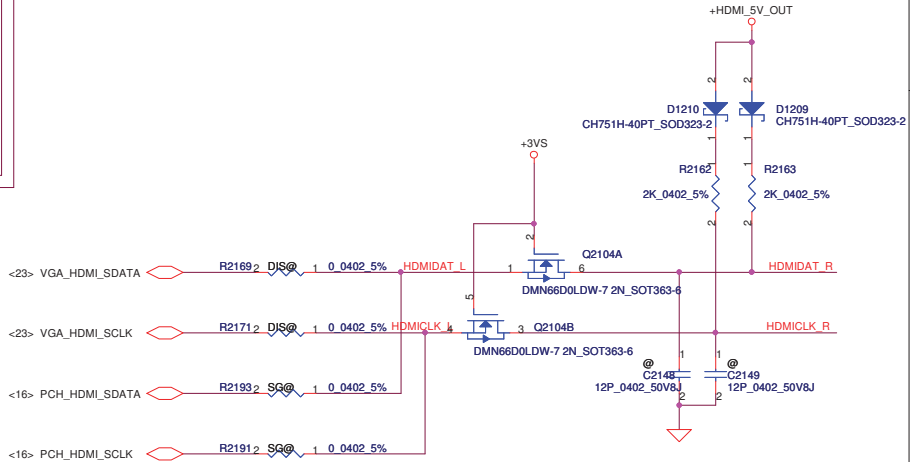
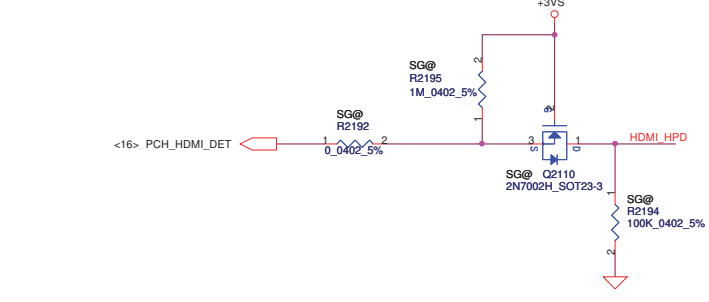
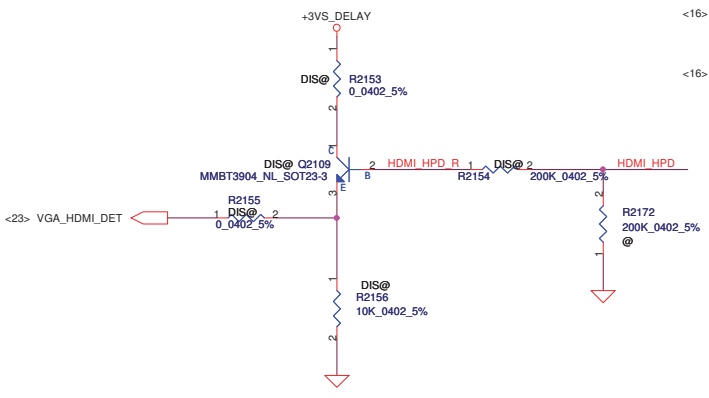
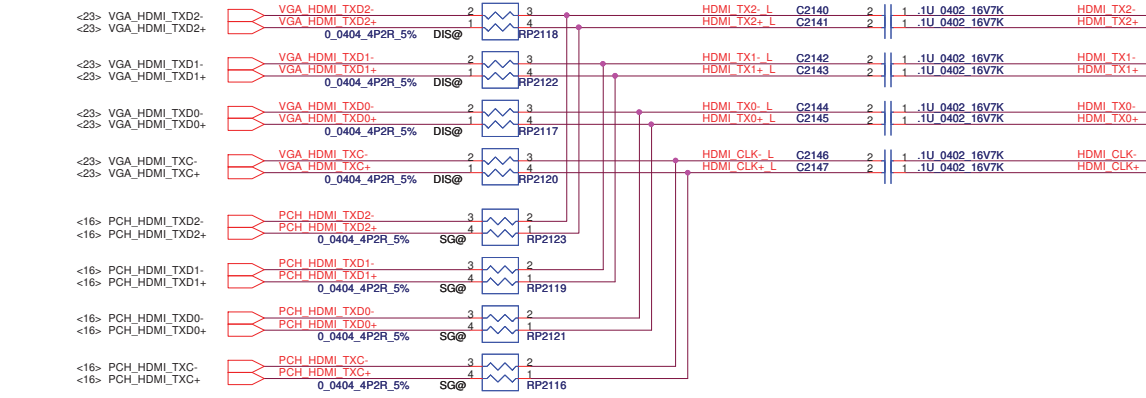
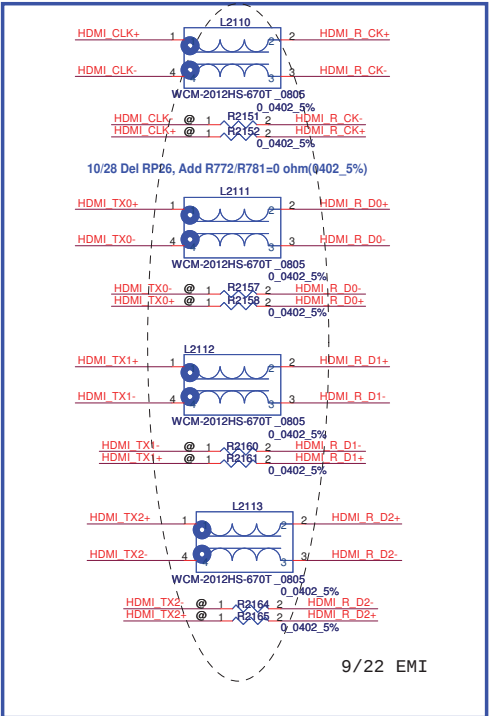
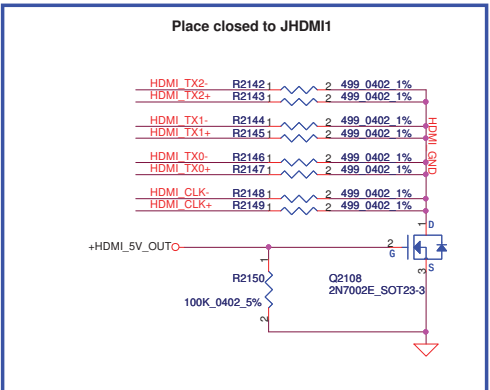


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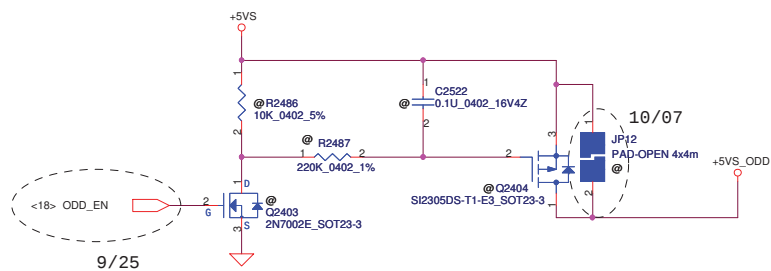
CRT Connector



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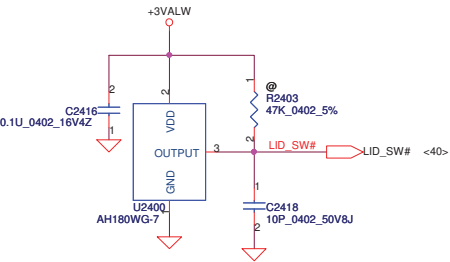


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Deciphered Date				2010/08/25				HDMI Level Shife & Conn			
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				58				Rev			
				1.0							

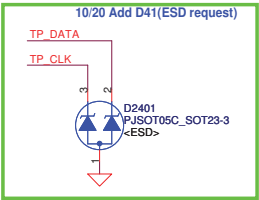
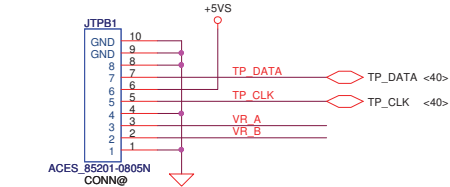
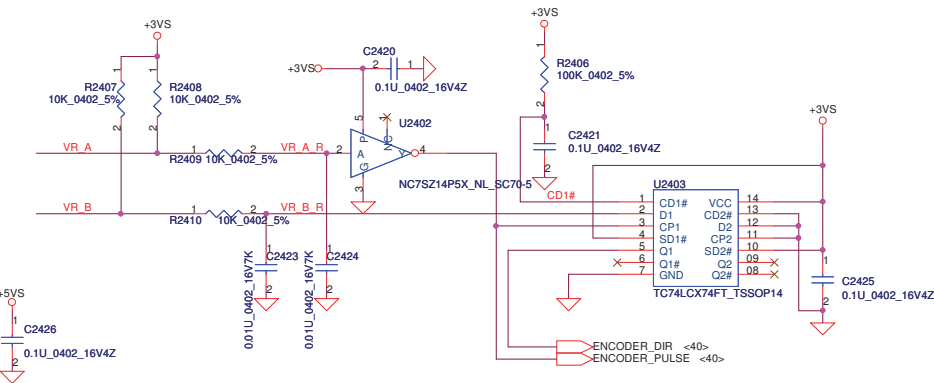


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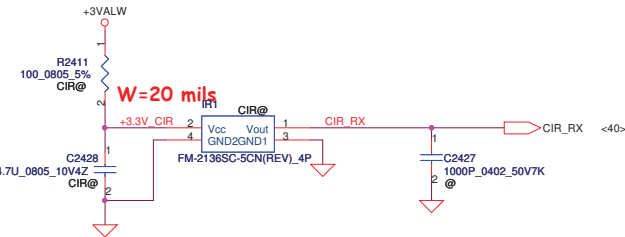
Lid Switch



Touch Pad

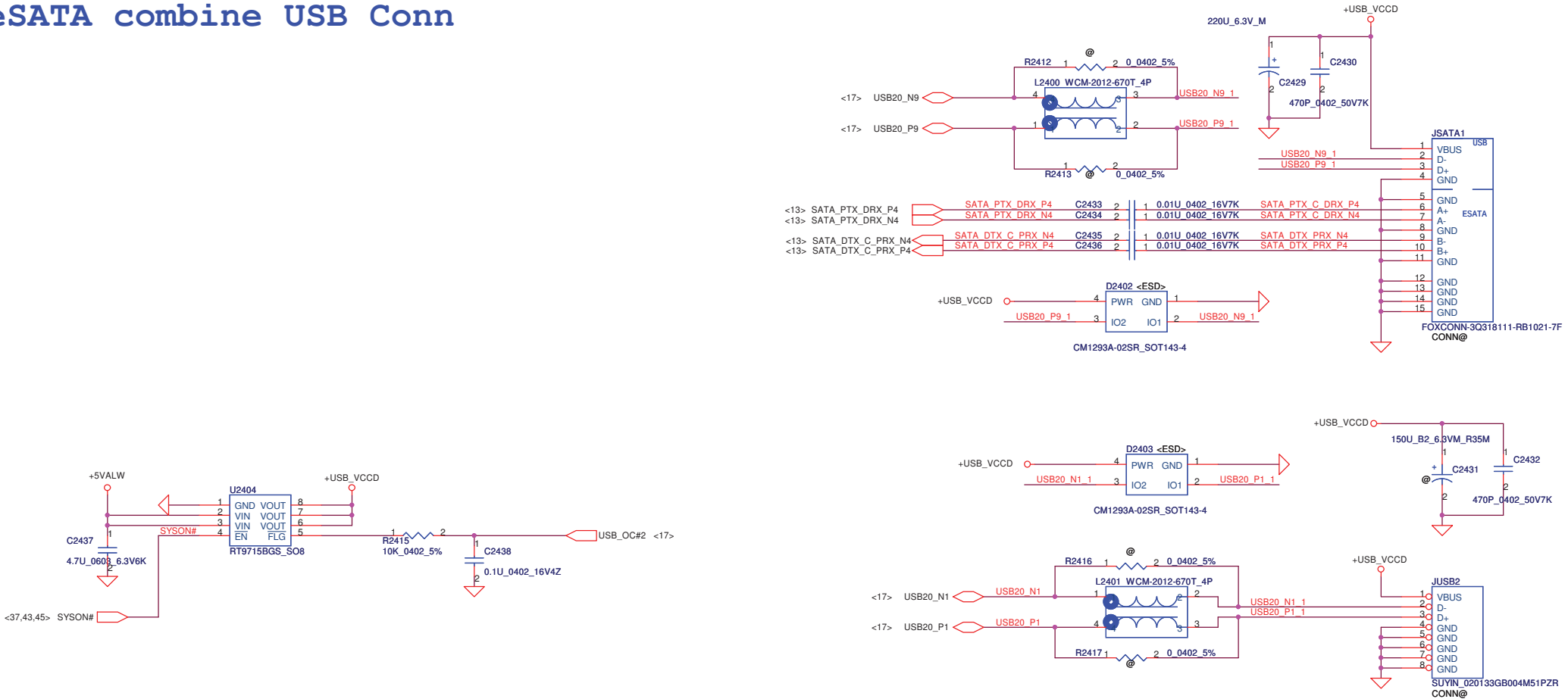


CIR

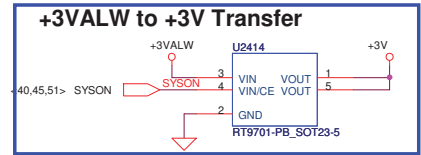
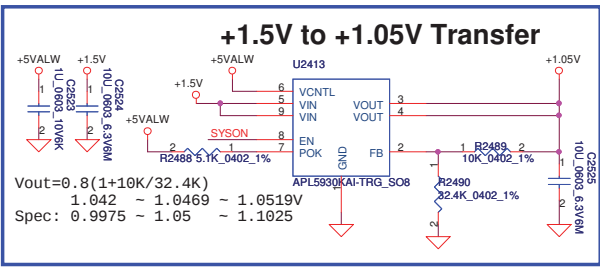


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eSATA combine USB Conn

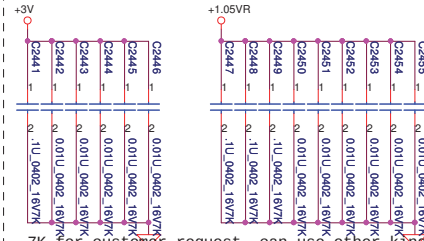
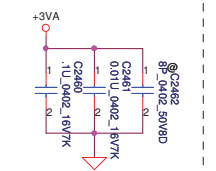
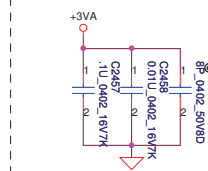


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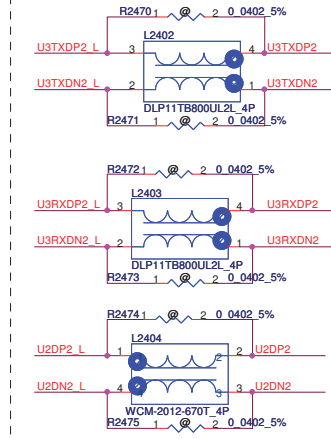


Close to U2407.D7

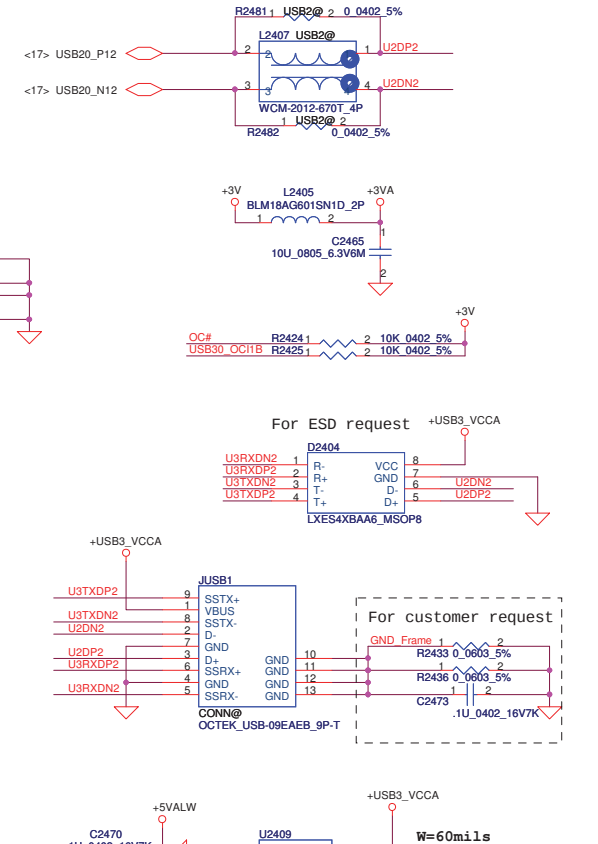
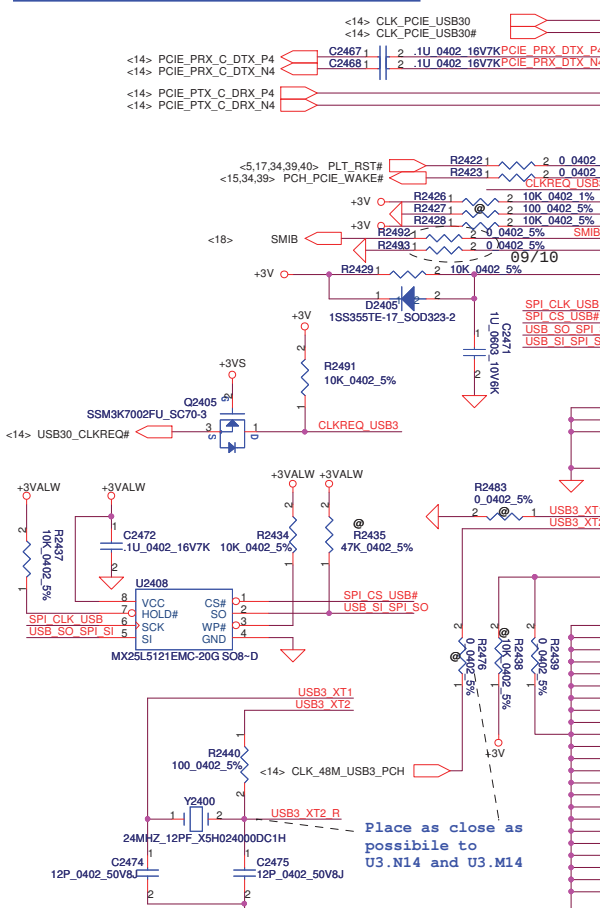
Close to U2407.P13



For EMI request (need confirm)



D-case for customer request can use B-case, either.



Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y2400,2440,C2474,C2475
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R2476,R2483

Security Classification

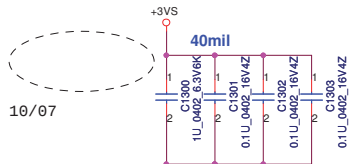
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Compal Secret Data			

USB3.0 PD720200

Size	Document Number	Rev
Customer		1.0

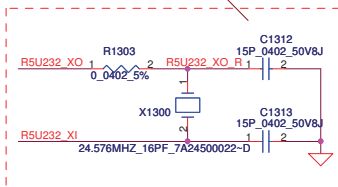
Date: Wednesday, October 27, 2010 Sheet 37 of 58

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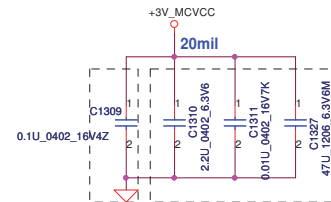


These caps close to U2 : Pin 12,37,48

Layout Note:
Place them close to U2

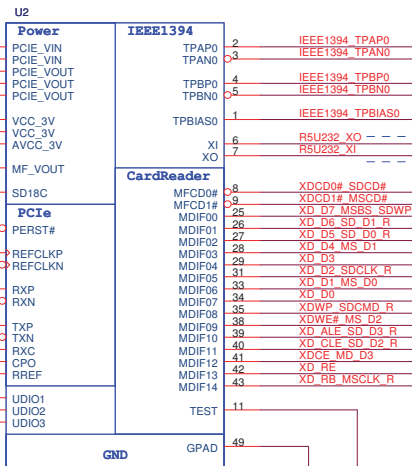
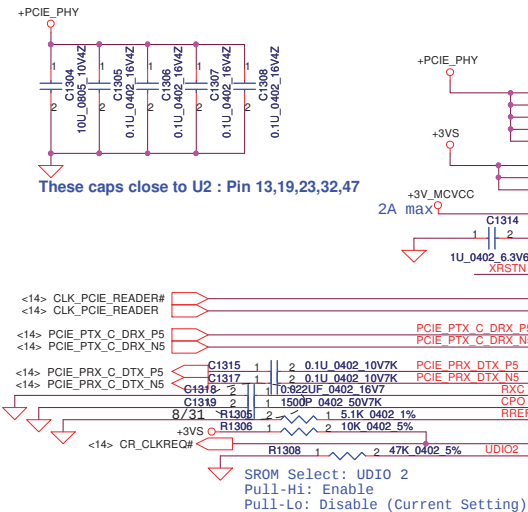


Memory Card Power



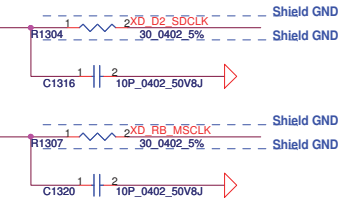
Layout Note:
Place them as close as possible to JREAD1
Place C1309 close to U2.36

These caps close to U2 : Pin 13,19,23,32,47

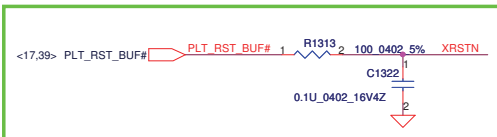
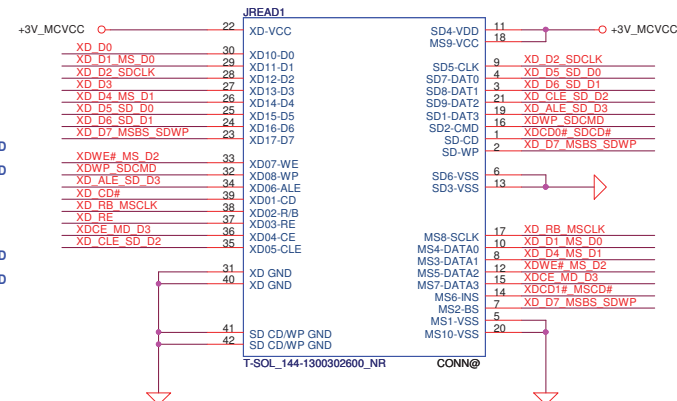


Layout Note:
Add GND shield for Xtal

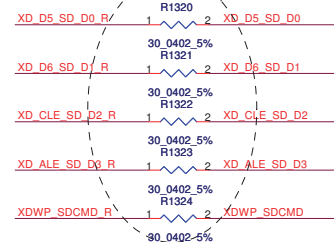
Impedance: 50 ohm (Microstrip)



5 IN 1 CardRead

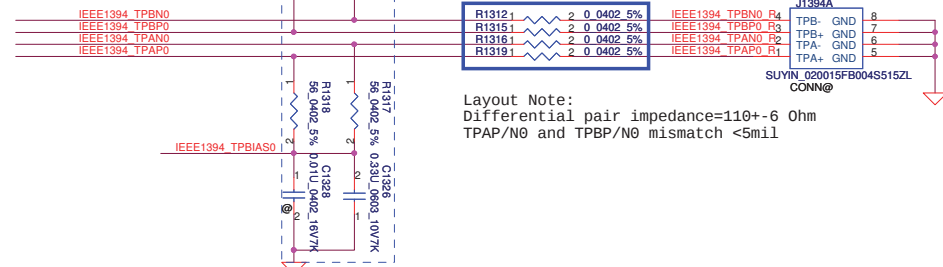


Layout Note:
Place them close to U2



Layout Note:
Add GND shield for 1394.

Layout Note:
Place them as close as possible to U2



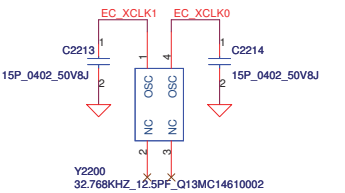
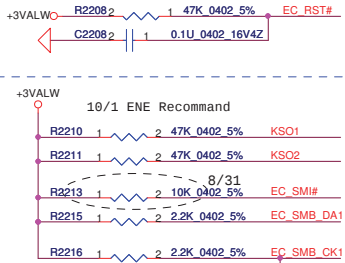
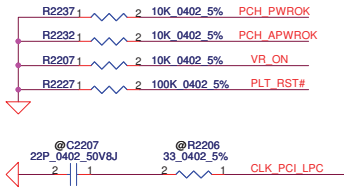
Layout Note:
Place them as close as possible to JP1394
Reserve them for test
if any EMI issue.

Layout Note:
Differential pair impedance=110+/-6 Ohm
TPAP/N0 and TPBP/N0 mismatch <5mil

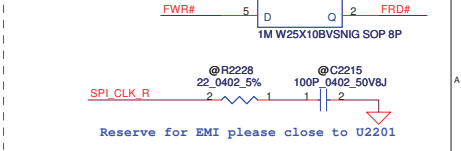
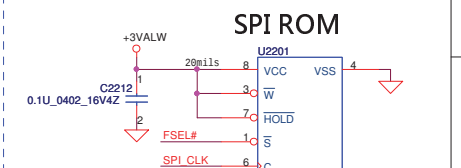
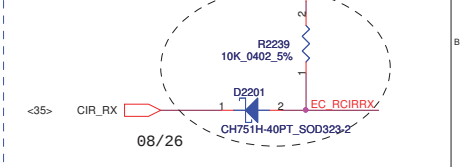
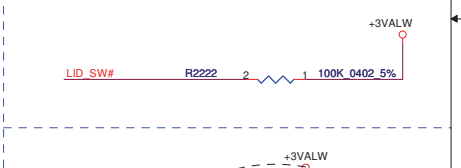
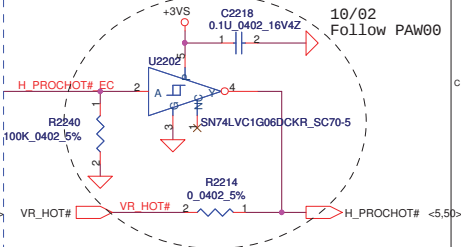
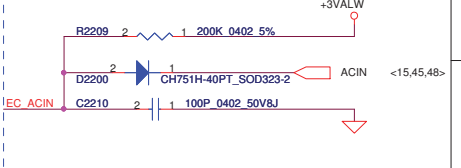
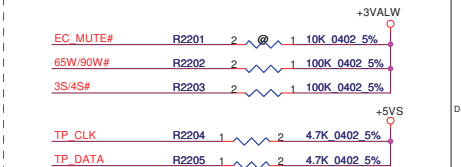
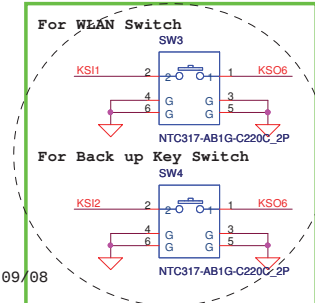
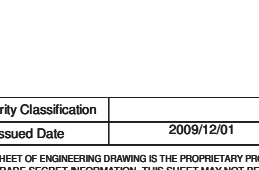
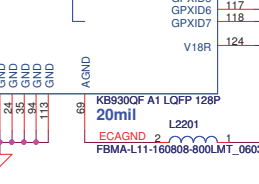
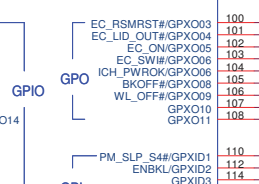
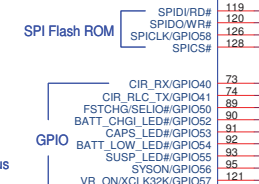
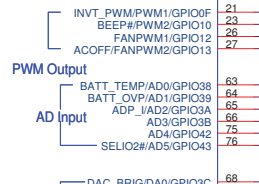
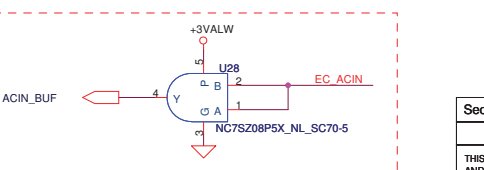
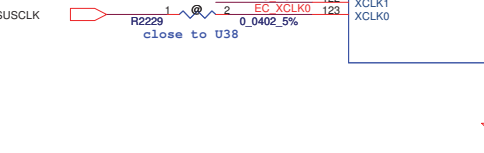
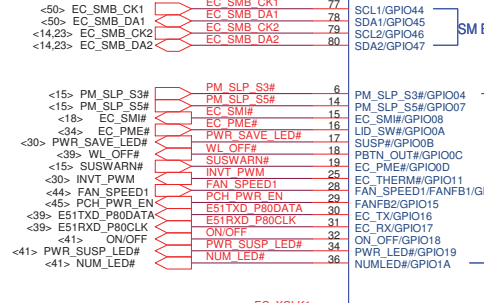
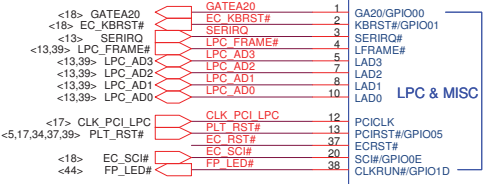
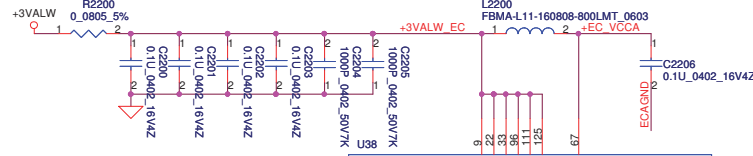
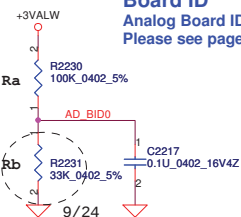
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01	D1	-	D6
02	D0	-	D5
03	D7	D1	D4
04	D6	D5	D3
05	CLK	-	D2
06	-	D0	D1
07	D5	D4	D0
08	CMD	-	WP#
09	D4	D2	WE#
10	D3	D6	ALE
11	D2	-	CLE
12	-	D3	CE#
13	-	D7	RE#
14	-	CLK	R/B#

When these pins are both set to Low, the xD Picture Card is detected.

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				Document Number	LA-6931P
				Date	Wednesday, October 27, 2010
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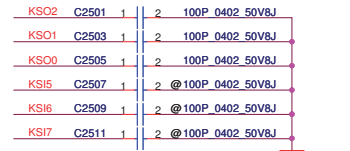
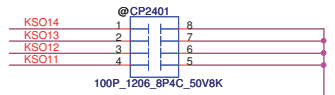
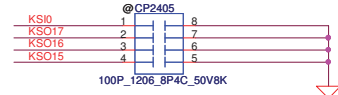
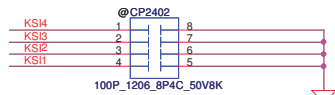
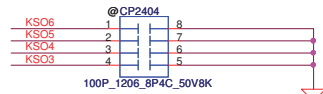
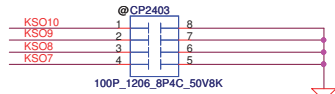
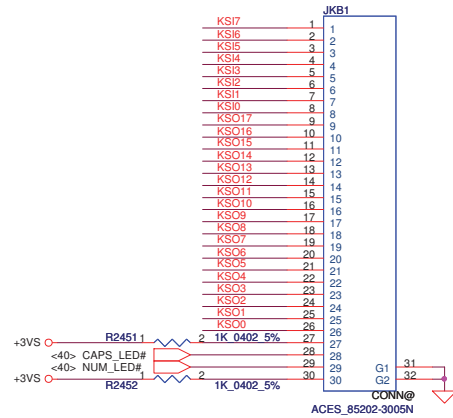
Board ID
Analog Board ID definition,
Please see page 3.



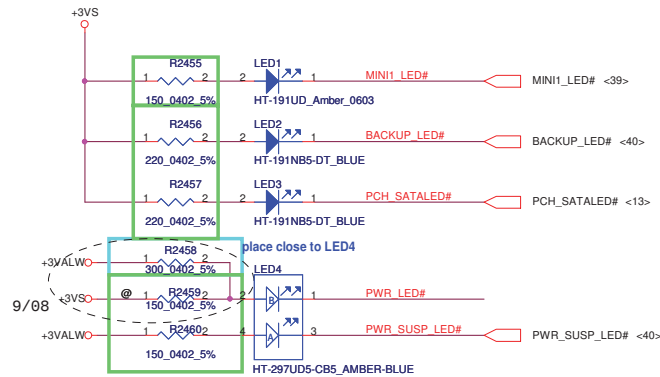
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Title		Compal Electronics, Inc.	
Size		Document Number	
Custom		LA-6931P	
Date		Wednesday, October 27, 2010	
Sheet		40 of 58	

INT_KBD Conn.

KS[0..7] <40>
KSQ[0..17] <40>

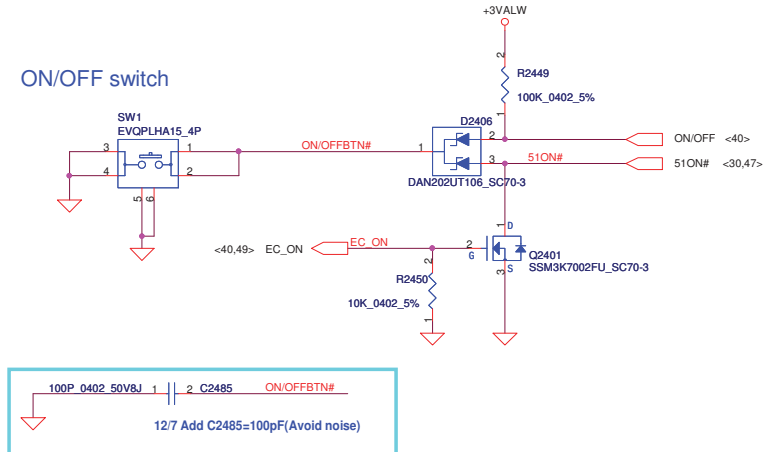


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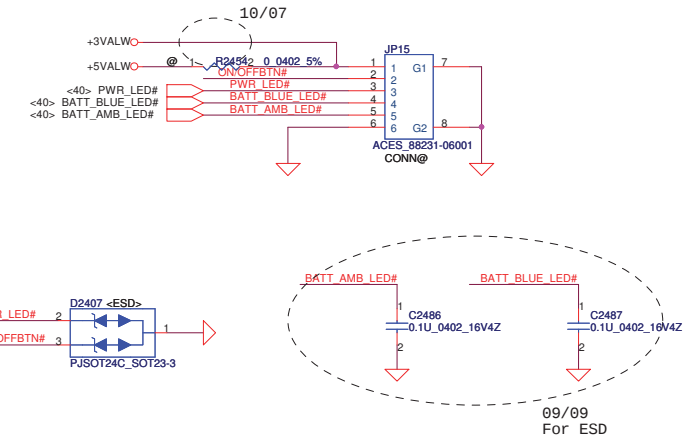


Power Button

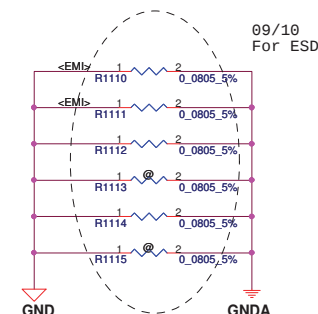
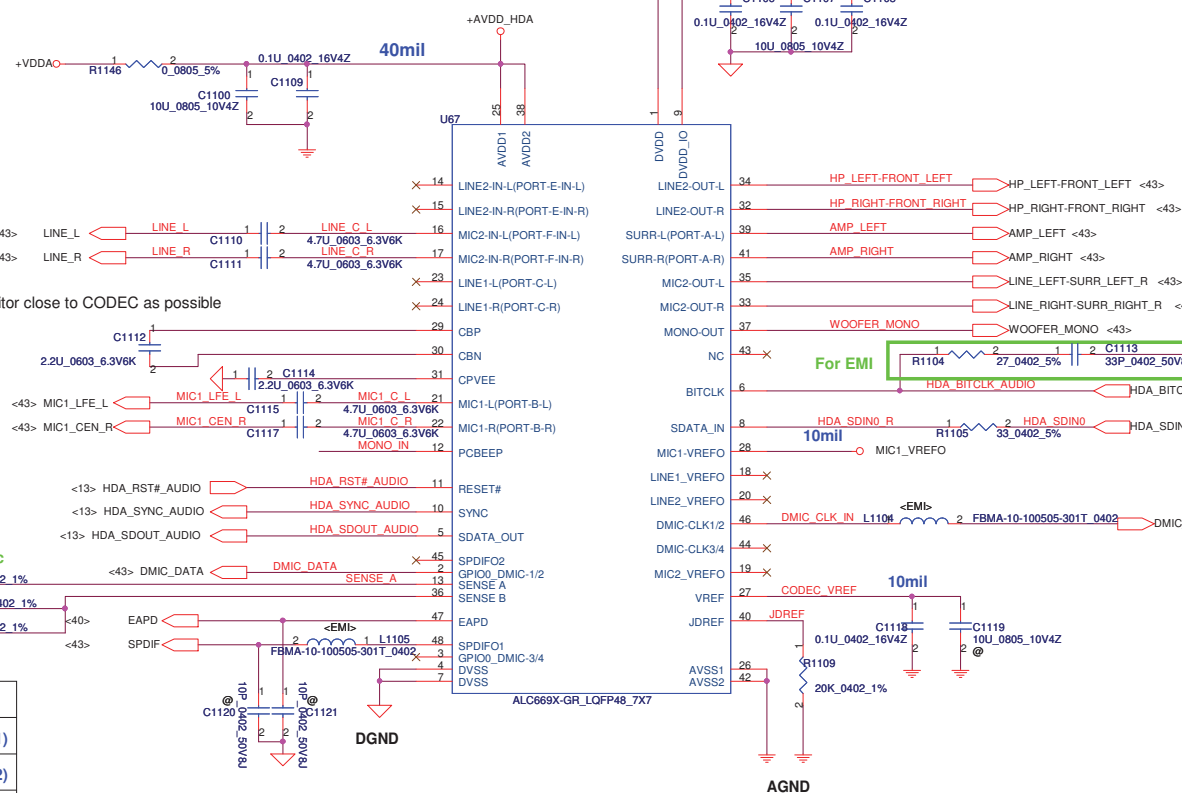
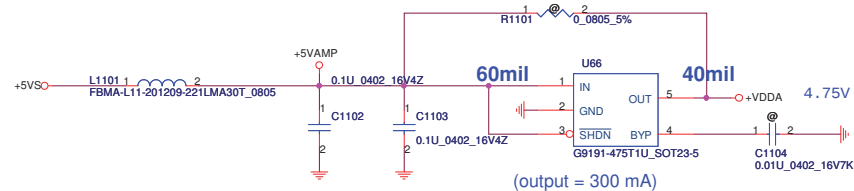
ON/OFF switch



Power Conn



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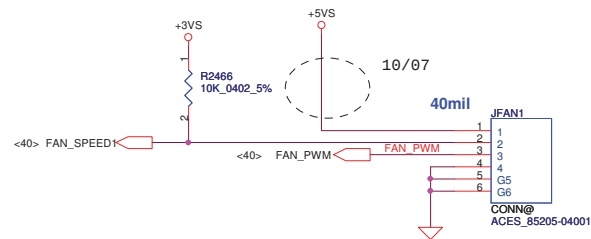


Sense Pin	Impedance	Codec Signals
SENSE A		PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
		PORT-C (PIN 23, 24)
SENSE B	39.2K	PORT-E (PIN 32, 34)
	20K	PORT-F (PIN 33, 35)
		PORT-H (PIN 37)

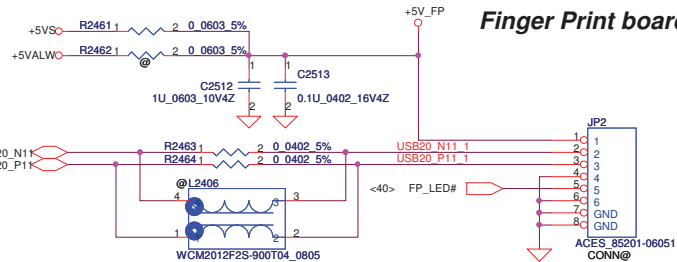
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Security Classification		Compal Secret Data		Compal Electronics, Inc. Amplifier & Audio Jack&USB	
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				Date:	Wednesday, October 27, 2010
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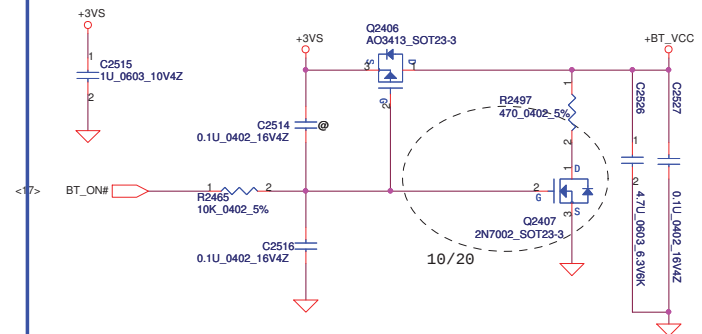
FAN1 Conn



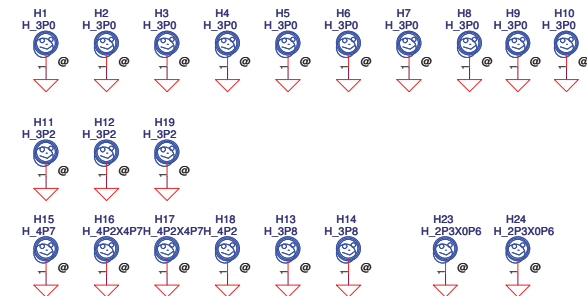
Finger Print board



BT



Screw



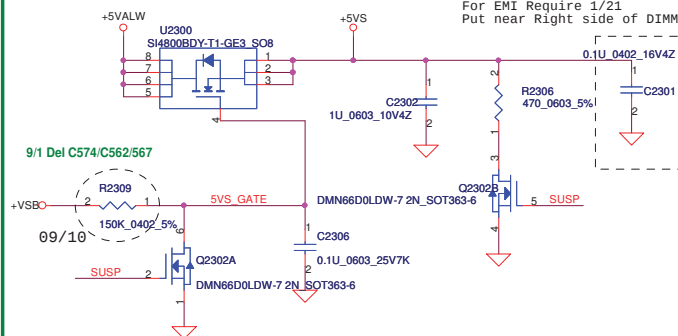
NON-PDH

2/25 Change footprint of H22

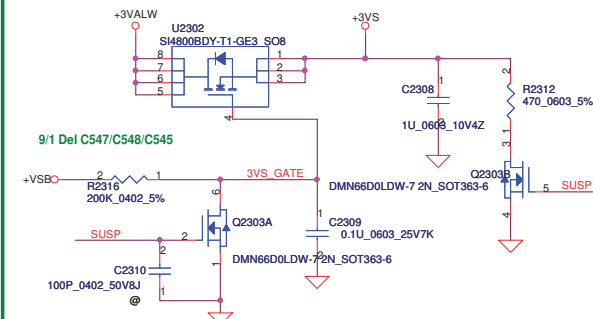


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+5VALW TO +5VS

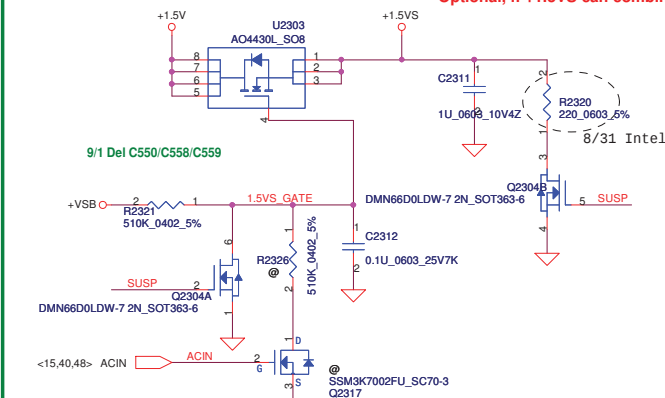


+3VALW TO +3VS



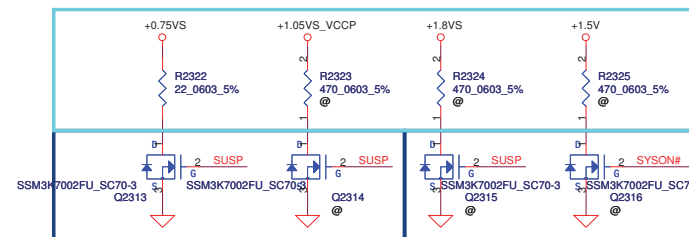
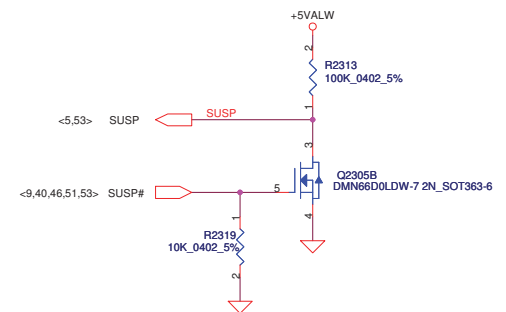
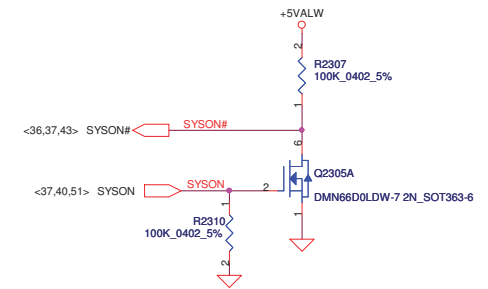
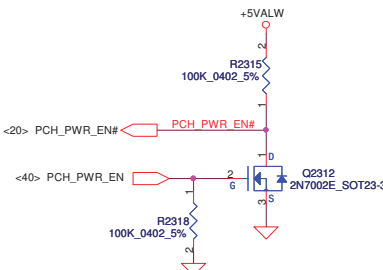
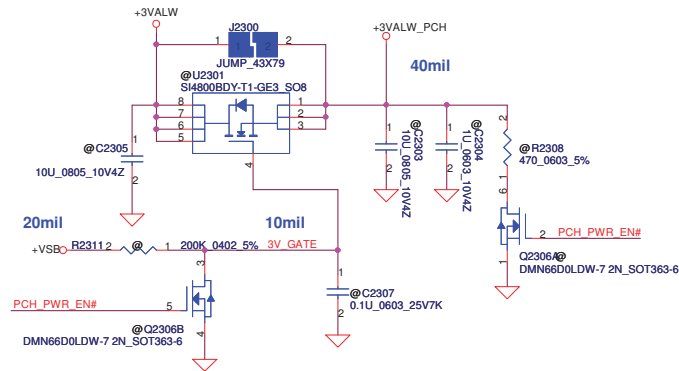
+1.5V to +1.5VS

Optional, if +1.5VS can combine with +1.5V_1

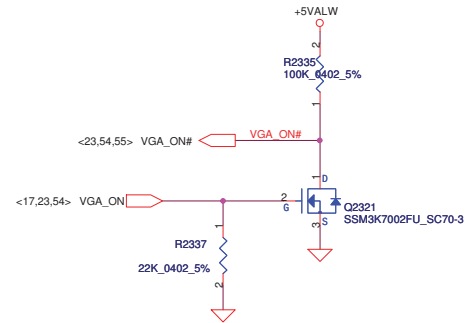
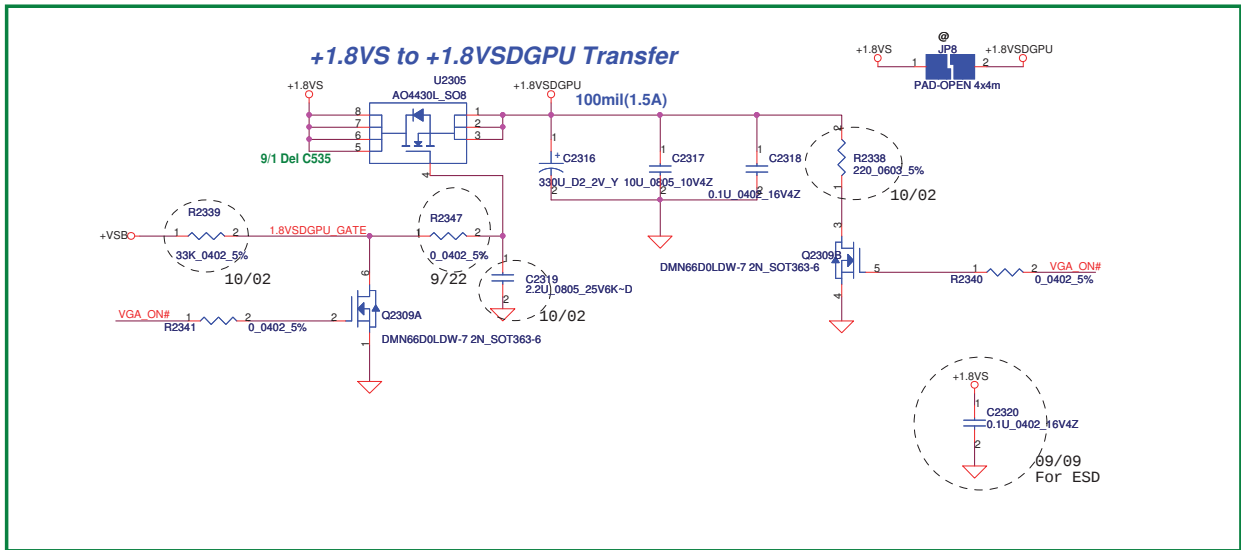
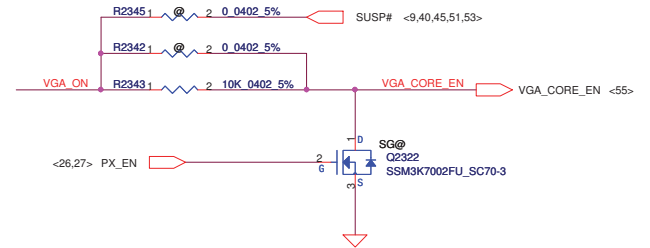
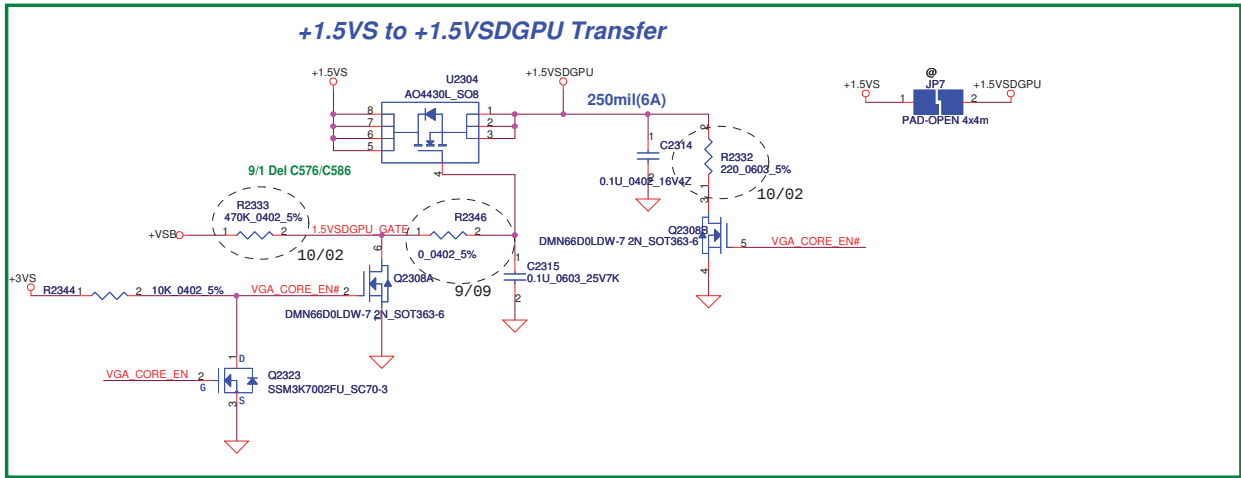


+3VALW TO +3VALW(PCH AUX Power)

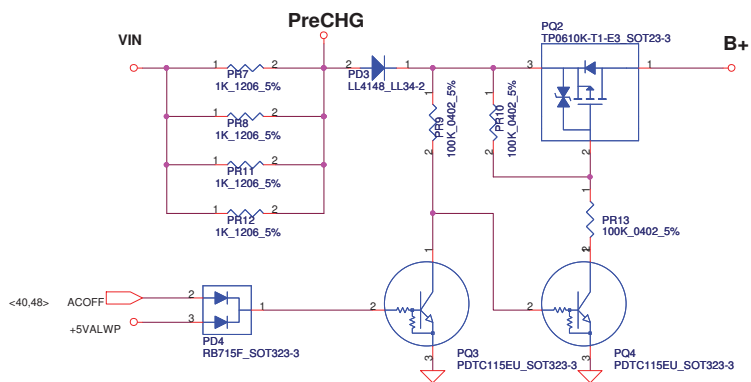
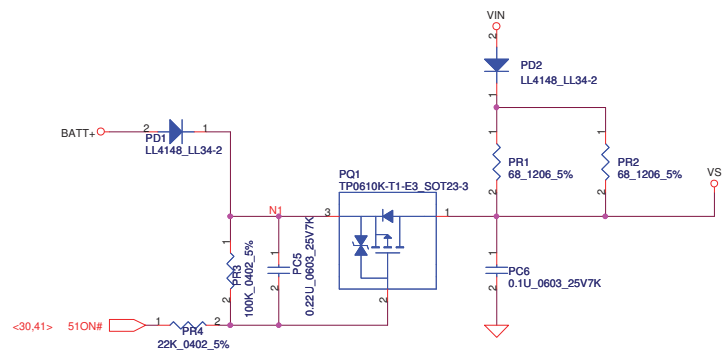
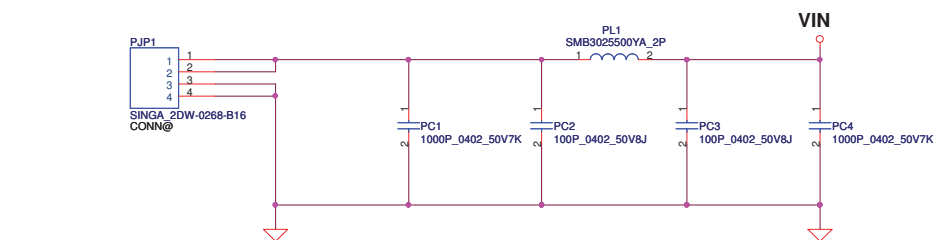
Short J5 for PCH VCCSUS3.3



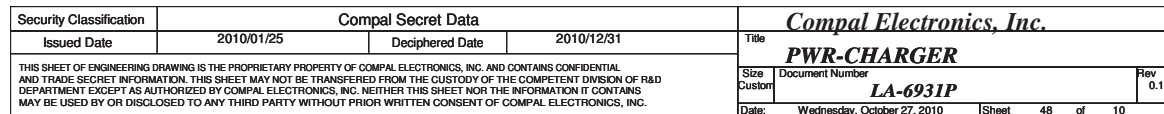
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								Size B	Document Number	Rev 1.0	
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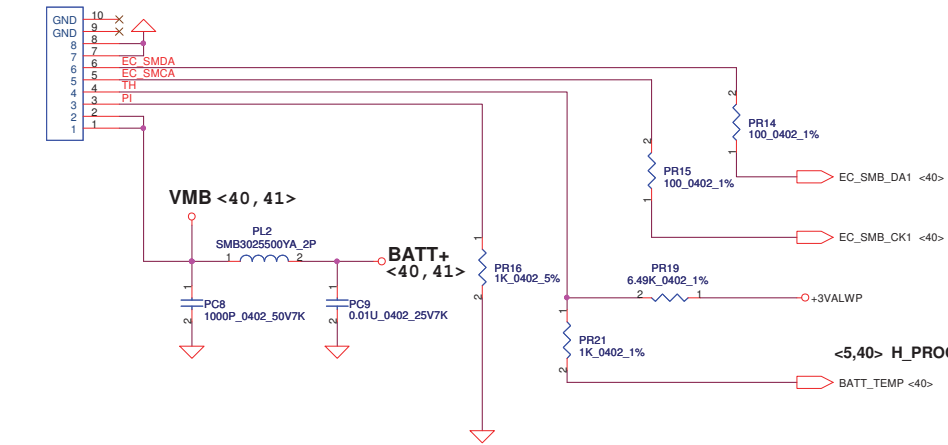
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Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title	VGA DC Interface	
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Date:				Wednesday, October 27, 2010	Sheet	46 of 58



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				Size	Rev
				Custom	0.1
				Date:	Wednesday, October 27, 2010
				Sheet	47 of 10

$$CP = 85\% \cdot I_{ada} ; CP = 4.07A$$


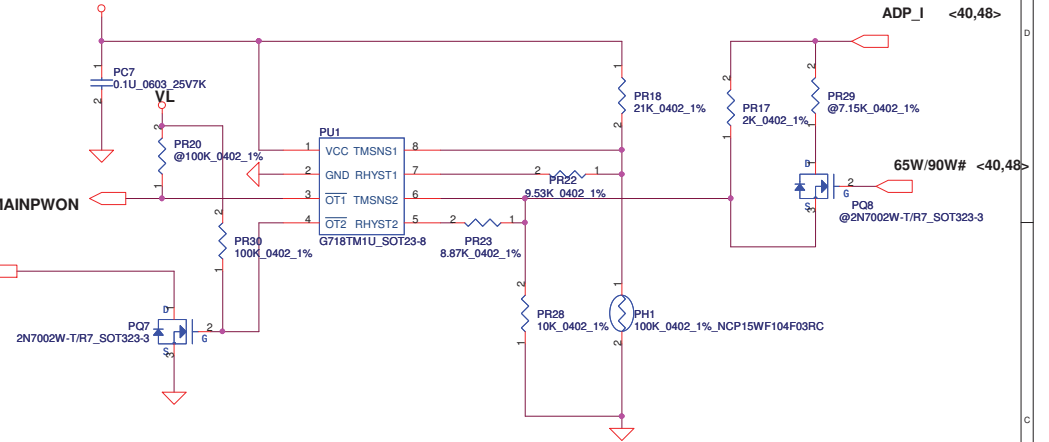
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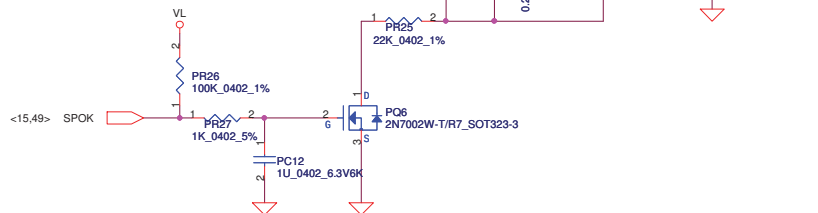
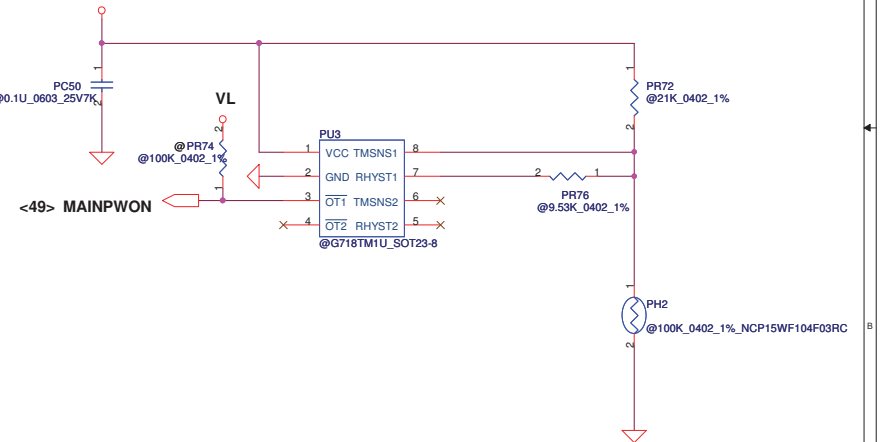
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VL

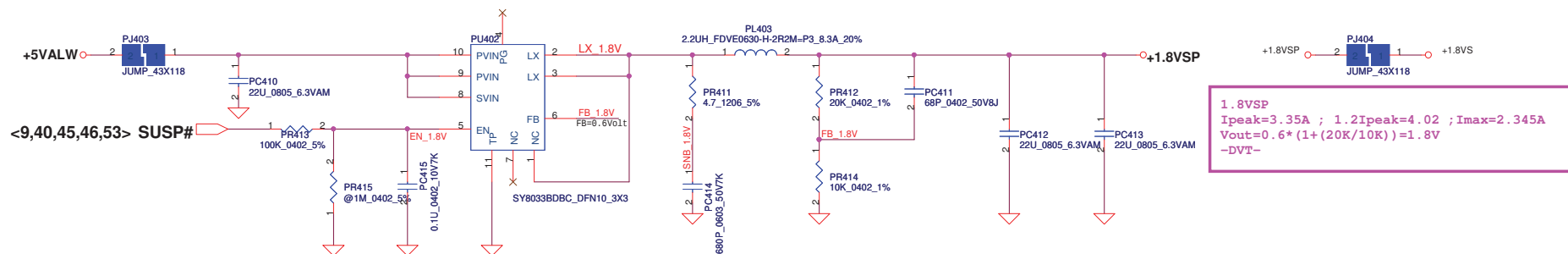
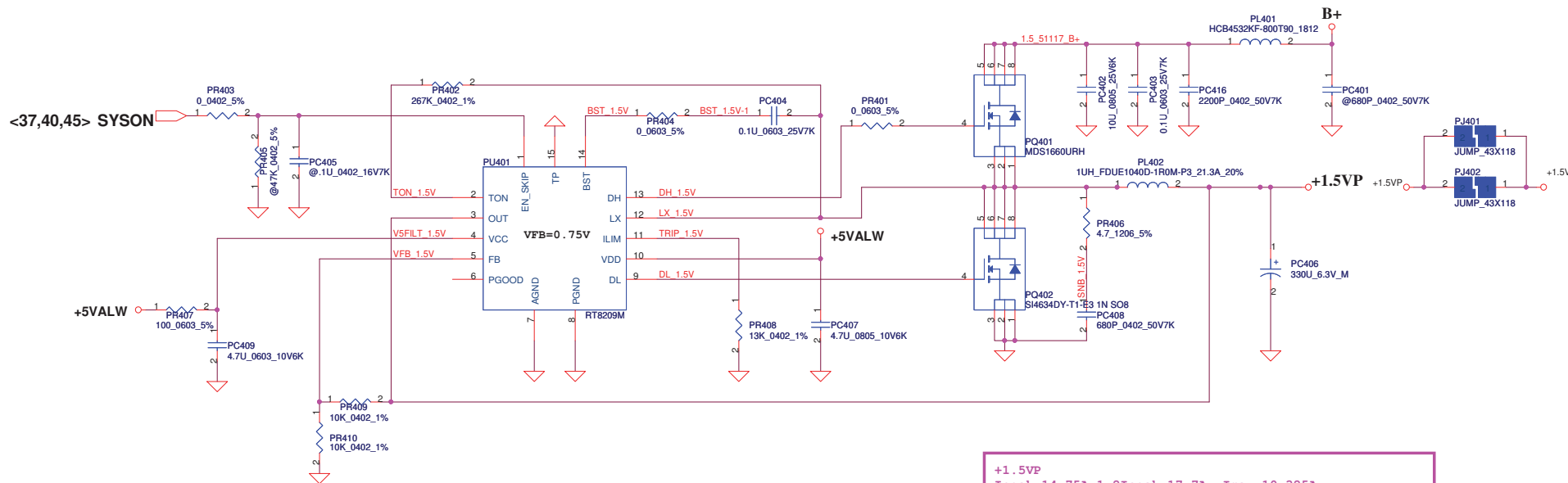


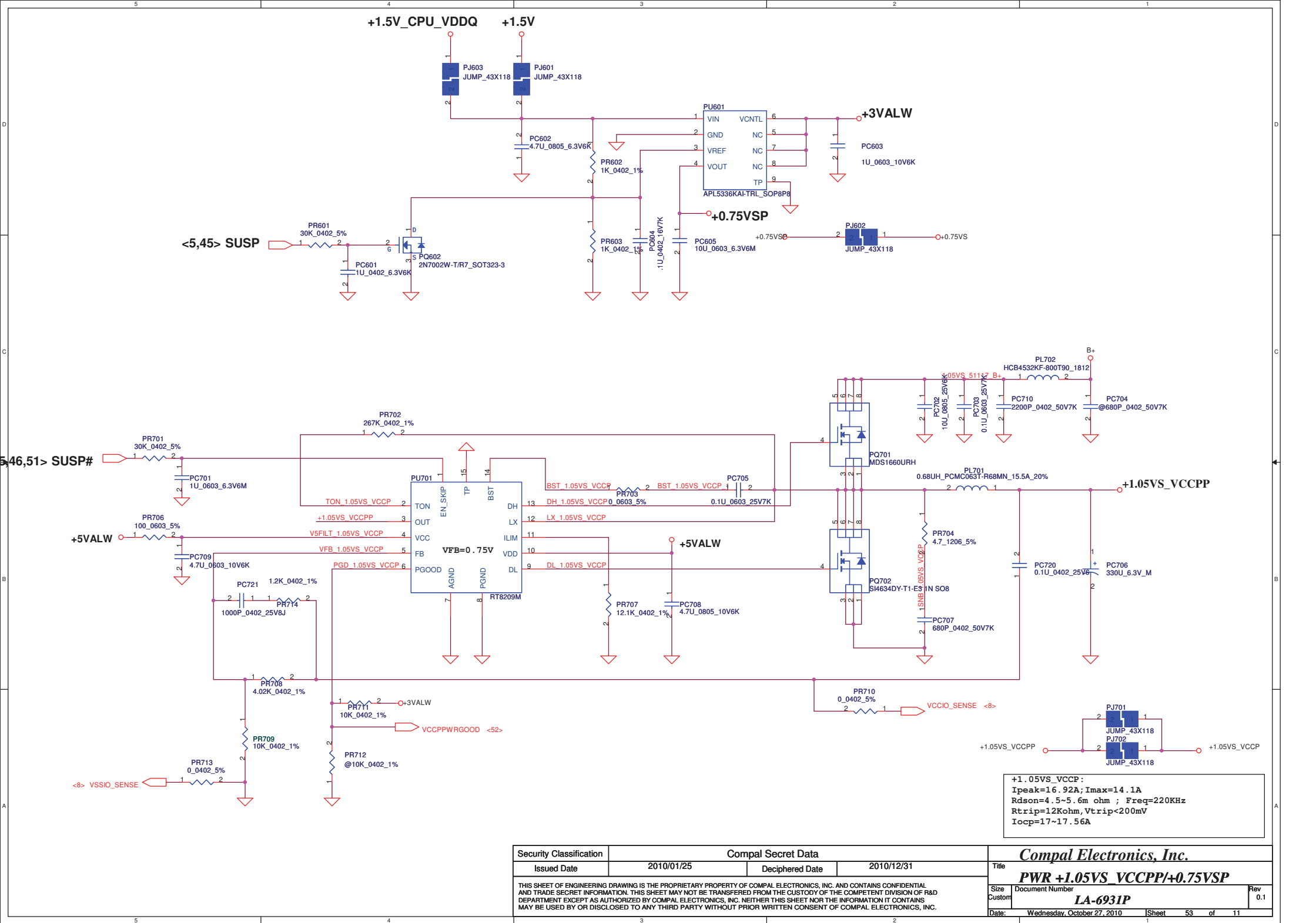
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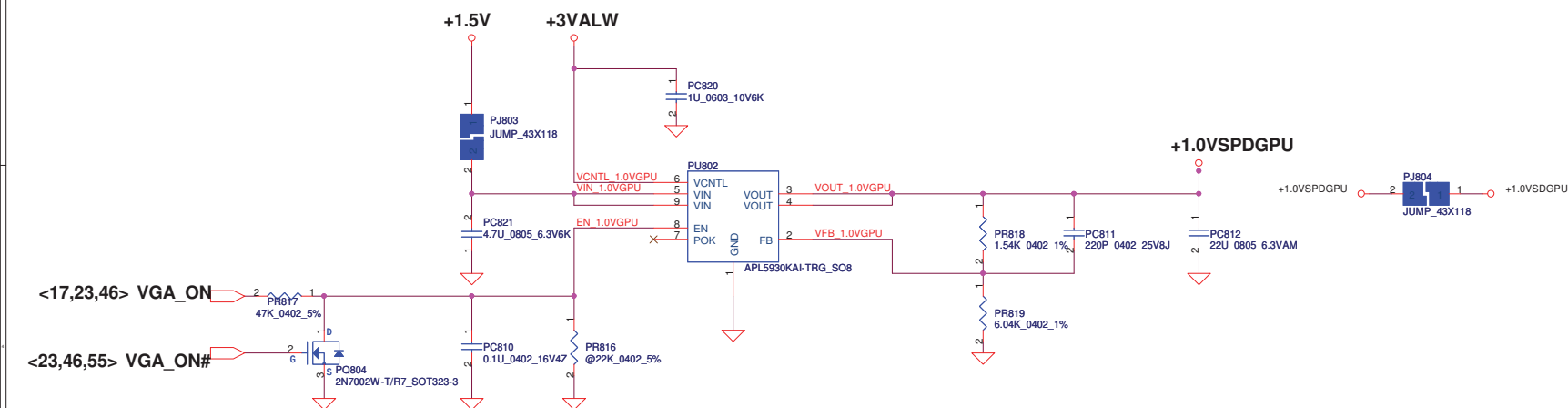
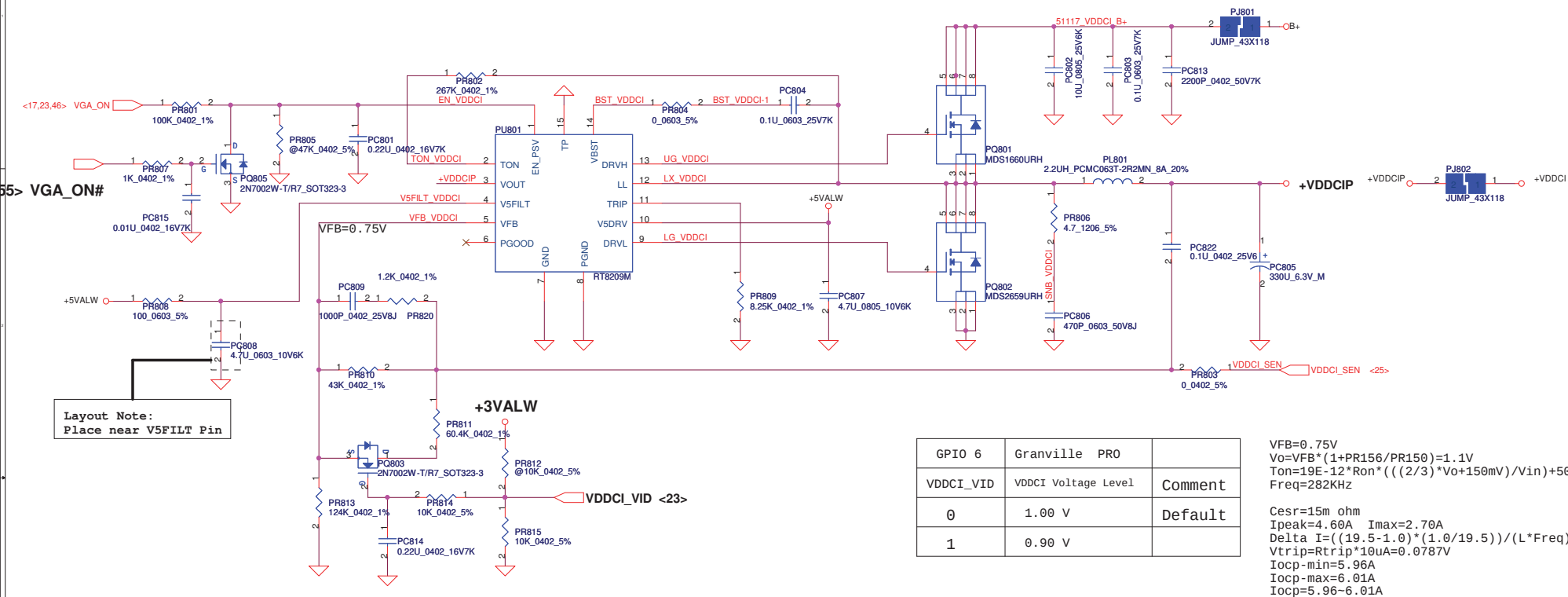


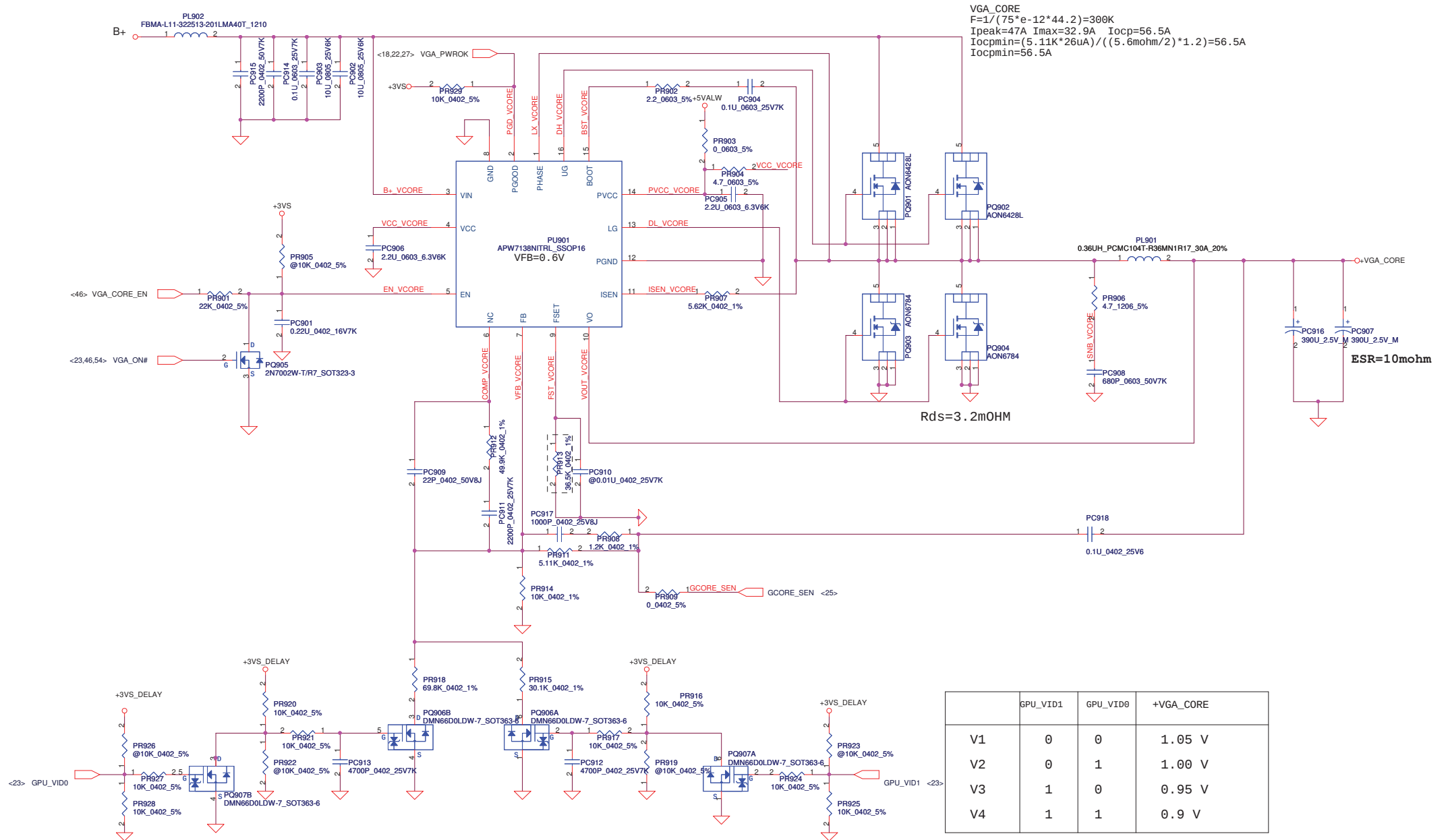
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										Wednesday, October 27, 2010
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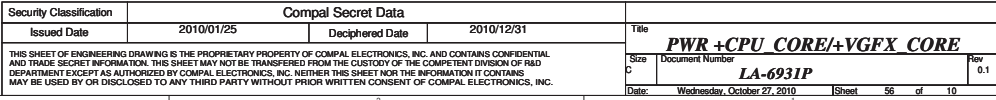




	GPU_VID1	GPU_VID0	+VGA_CORE
V1	0	0	1.05 V
V2	0	1	1.00 V
V3	1	0	0.95 V
V4	1	1	0.9 V

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								Size	Document Number						Rev
								Custom	LA-6931P						0.2
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Parallel and tune length



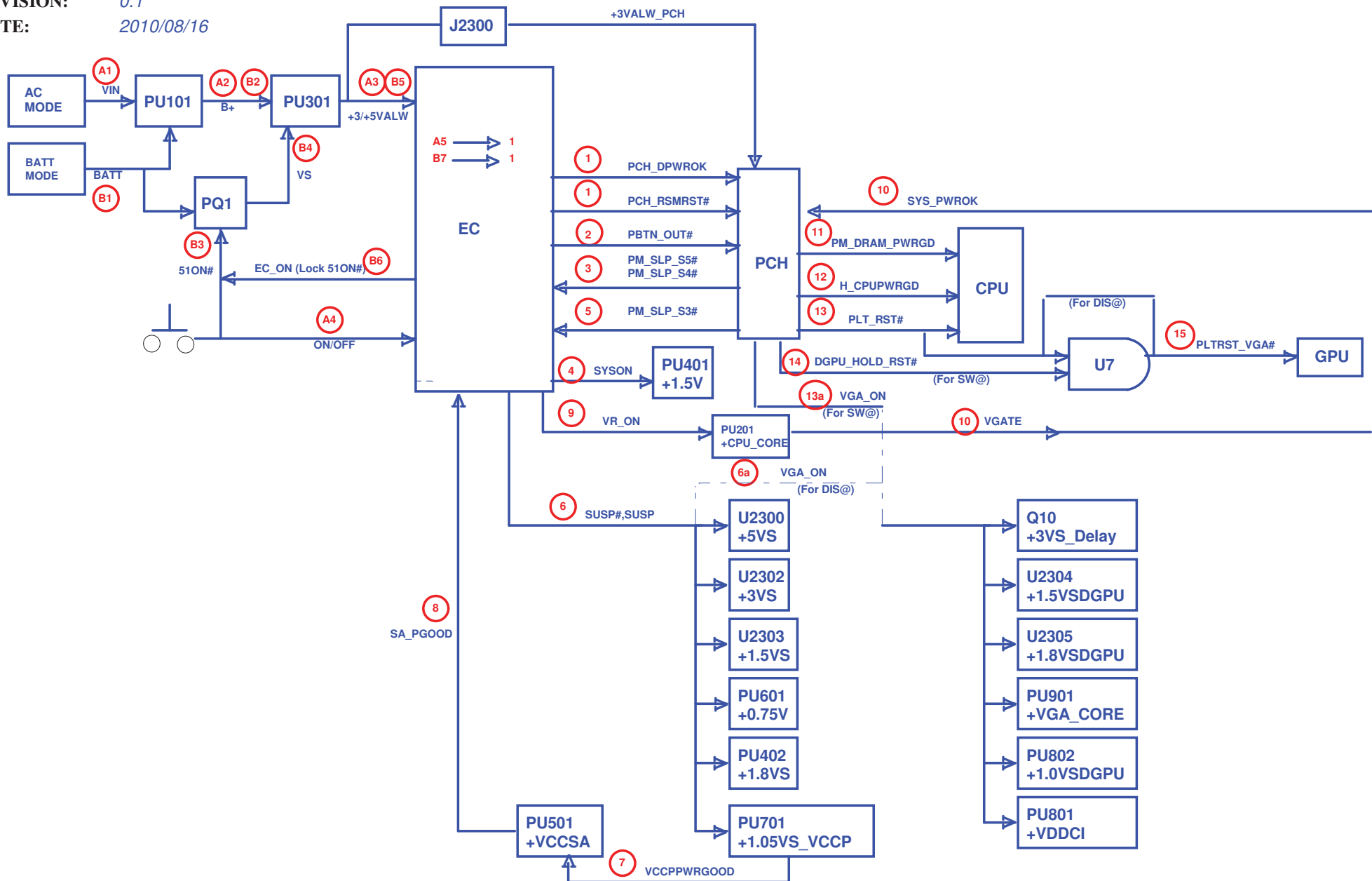
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MODEL NAME: P5LM0 Power Sequence Block Diagram

PCB NAME: LA-6931P

REVISION: 0.1

DATE: 2010/08/16



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Version Change List (P. I. R. List) for HW Circuit

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