ZZZ2

X76

Part Number = X76264BOL81

SEYSAM1G@

ZZZ

X76

Part Number = X76264BOL82

SEYHYN1G@

ZZZ3

X76

Part Number = X76264BOL55

WHISAM1G@

ZZZ5

X76

Part Number = X76264BOL60

WHIHYN1G@

ZZZ4

X76

Part Number = X76264BOL61

SAM2G@

ZZZ6

X76

Part Number = X76264BOL62

HYN2G@

Compal Confidential

P7YE5/S5 Schematics Document

AMD Sabine

APU Llano / Hudson M2 / Vancouver Whistler_Seymour

DIS only / UMA only / PX Muxless with BACO

ZZZ1

PCB

Part Number = DA80000NI00

2011-02-18

LA-6991P REV: 0.2

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Compal Confidential

Model Name : P5WS5

Sabine

VRAM 1G/2G
64M16/128M16 x 8
page 18, 19

DDR3

Thermal Sensor
ADM1032
page 14

ATI
Vancuver Whistler/ Seymour
uFCBGA-962
Page 13~17

GFX x 16 Gen2

GFX x 4 (Group 1~4)

APU HDMI
(UMA / Muxless)

DP x1 (DP0 TXP/N0)

VGA HDMI

VGA LVDS(eDP)

VGA CRT

AMD FS1 APU
Llano
uPGA-722 Package
Page 6~10

Memory BUS(DDR3)
Dual Channel
1.5V DDRIII 800~1600MHz

204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2, 3
Page 11,12

HDMI Conn.
page 23

LVDS Conn.
Reserve eDP
page 22

LVDS

UAM eDP

LVDS Translator
page 21

DP x2
(DP0 TXP/N 0~1)

P_GPP x 3
GEN2

DP x 4
(DP1 TXP/N 0~4)

UMI

CRT Conn.
page 24

FCH CRT (VGA DAC)

FCH
Hudson-M2/M3
uFCBGA-656
Page 25~29

USB20 M/B*1
page 34

USB20/B *2
page 35

USB30/B *1
page 35

CMOS Camera
page 22

Bluetooth Conn.
page 35

Mini Card 1
page 33

Mini Card 2
page 33

USB
3.3V 48MHz

Port 0

Port 1
Port 2

Port 3

Port5

FSD0

Port 8

Port 9

GPP3

GPP2

GPP1

GPP0

Card Reader
RT5138
page 33

MINI Card 2
Option
page 33

MINI Card 1
WLAN
page 33

LAN(GbE)
AR8151
page 31

RJ45
page 32

HD Audio 3.3V 24.576MHz/48Mhz

S-ATA Gen2

port 0

port 1

port 2

SATA HDD1
Conn.
page 30

SATA HDD1
Conn.
page 30

ODD
Conn.
page 30

HDA Codec
ALC271X
page 38

GPP x 2
GEN2

LPC BUS

ENE KB930/9012
page 36

LED
page 37

RTC CKT.
page 25

Power On/Off CKT.
page 37

Fan Control
page 30

DC/DC
Interface CKT.
page 39

Power Circuit
page 40~48

External board

GLAN - LAN/B
page 37

LID SW - Power/B
page 37

USB20/B
-USB20 x2
page 35

USB30/B
-USB20 x1+ USB30 x1
page 35

USB30
On SUB/B
page 35

USB30
On M/B
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Touch Pad
page 37

Int.KBD
page 37

EC I/O Buffer

BIOS ROM

SYS BIOS (2M)
page 27

EC BIOS (128K)
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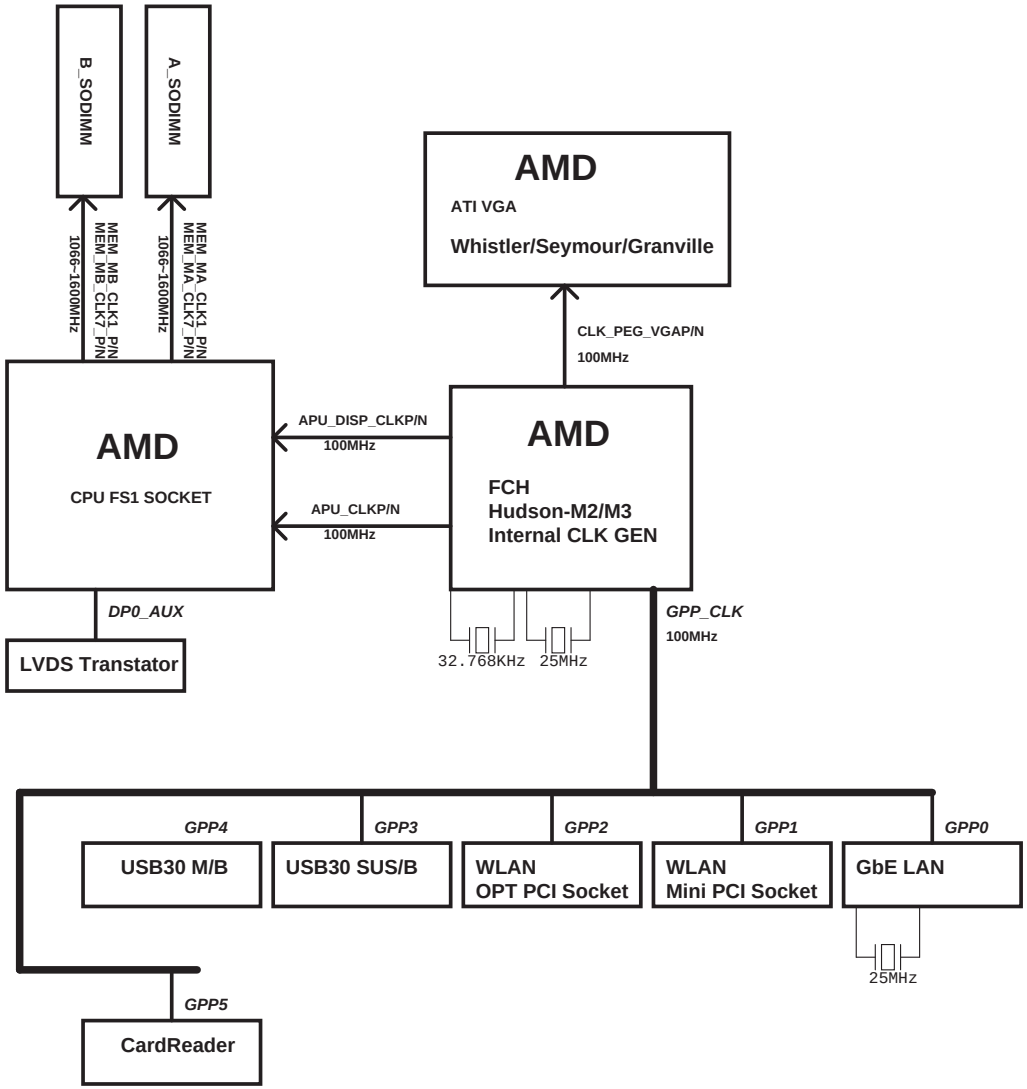
CLOCK DISTRIBUTION



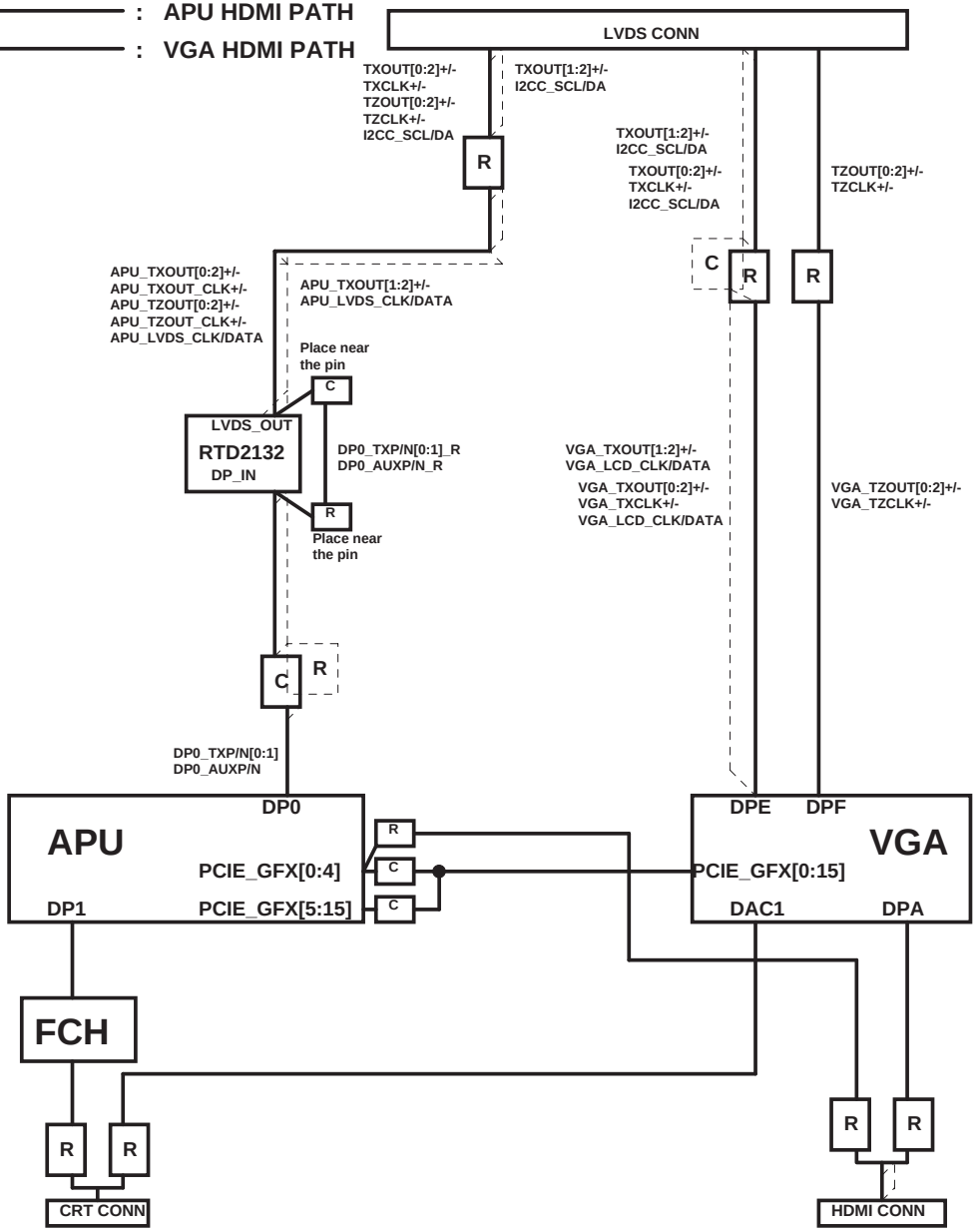
DISPLAY DISTRIBUTION

: LVDS PATH

: eDP PATH

: APU HDMI PATH

: VGA HDMI PATH



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PROJECT ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	0.1(EVT)
2	0.2(DVT)
3	
4	
5	
6	
7	

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
SB-TSI	1001 100X b	98H
GMT G781-1 (GPU)	1001 101X b	9AH
CAT24C64WI (RTD2136S)	1010 100X b	A8H
VGA-TSI	1000 001X b	82H

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1001 000Xb	90
DDR DIMM2	1001 010Xb	94

FCH SM Bus 1 address

Device	Address	HEX

BTO Option Table

BOM Structure	BTO Item
UMA@	Display from UMA (PX4.0 or UMA only)
VGA@	Have VGA chip (Discrete only or PX4.0)
DISO@	Display from VGA (Discrete only)
SEYM@	Use Seymour (Discrete only and PX4.0)
WHI@	Use Whistler (Discrete only and PX4.0)
GRAN@	Use Granville (Discrete only and PX4.0)
VAN@	Use Vancouver VGA (Discrete only and PX4.0)
RT@	Use translator RTD2136S
ANX@	Use translator ANX3110
M2@	Use Hudson-M2
M3@	Use Hudson-M3
930@	Use KB930
9012@	Use KB9012
128@	Use VRAM channel A
PX@	PX4.0
BACO@	Use BACO
NOBACO@	No use BACO
APULVDS@	UMA LVDS path
APUEDP@	UMA eDP path
VGALVDS@	VGA LVDS path
VGAEDP@	VGA eDP path
EDP@	eDP path
JE@	ACER
SJV@	PB and GW
NOGRAN@	No Use Granville

BOM Config

EVT

UMA only:

UMA@, RT@, ANX@, M3@, 930@, APULVDS@, JE@

DISO only:

VGA@, DISO@, VGALVDS@, SEYM@ or WHI@, VAN@, 128@(With WHI@), NOGRAN@, NOBACO@, M3@, 930@, JE@

PX

UMA@, VGA@, PX@, SEYM@ or WHI@, VAN@, 128@(With WHI@), NOGRAN@, RT@, ANX@, APULVDS@, BACO@, M3@, 930@, JE@

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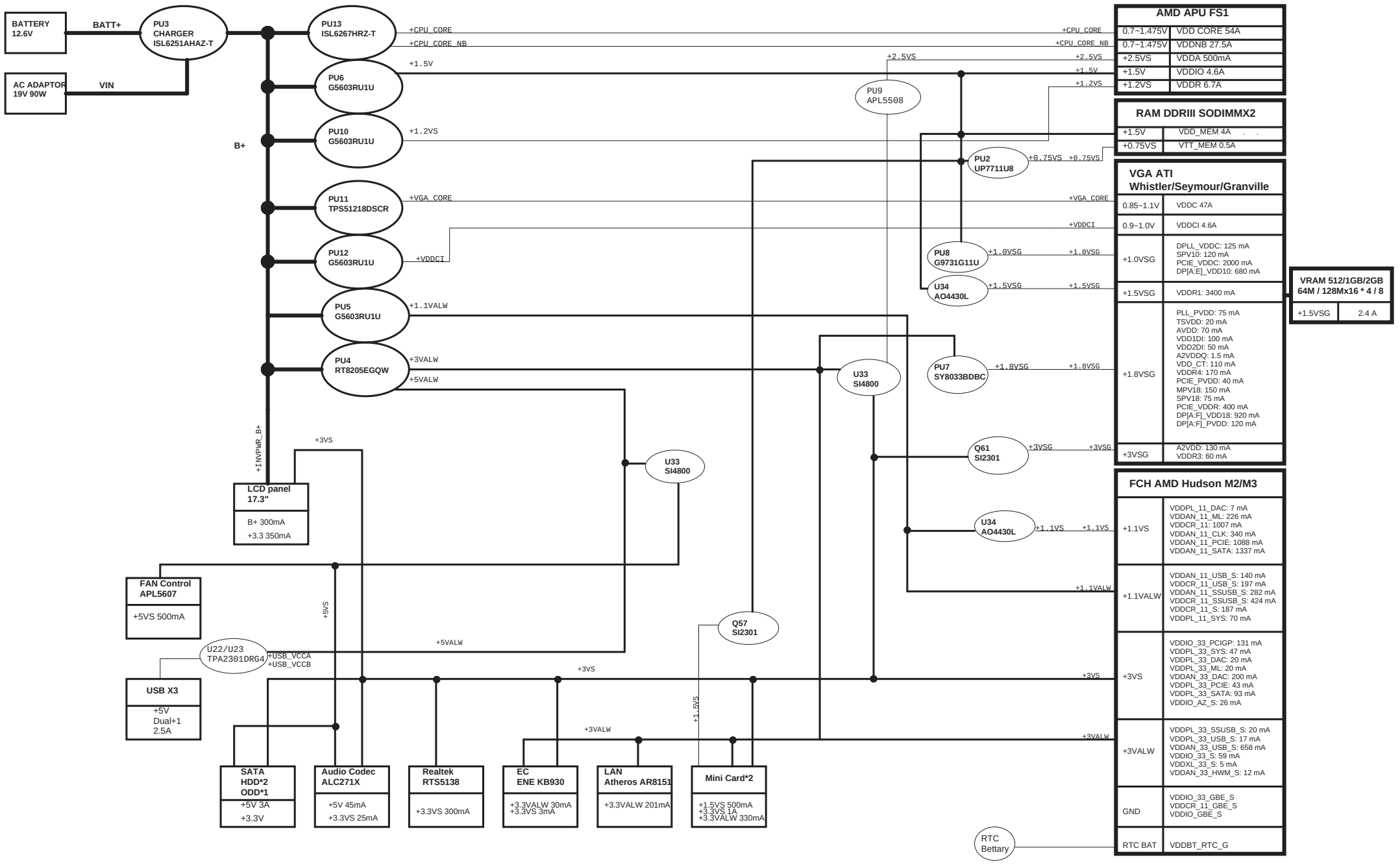

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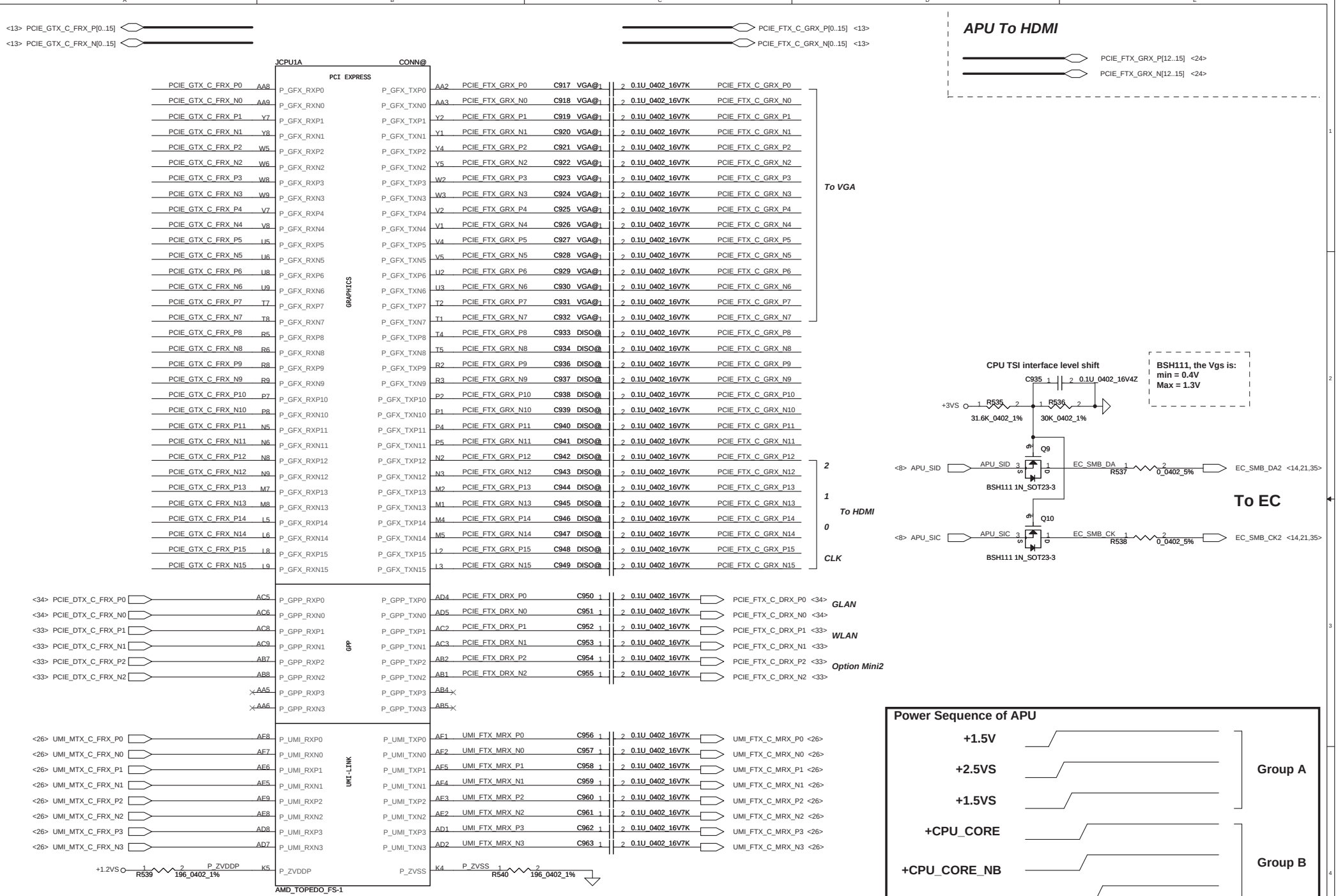

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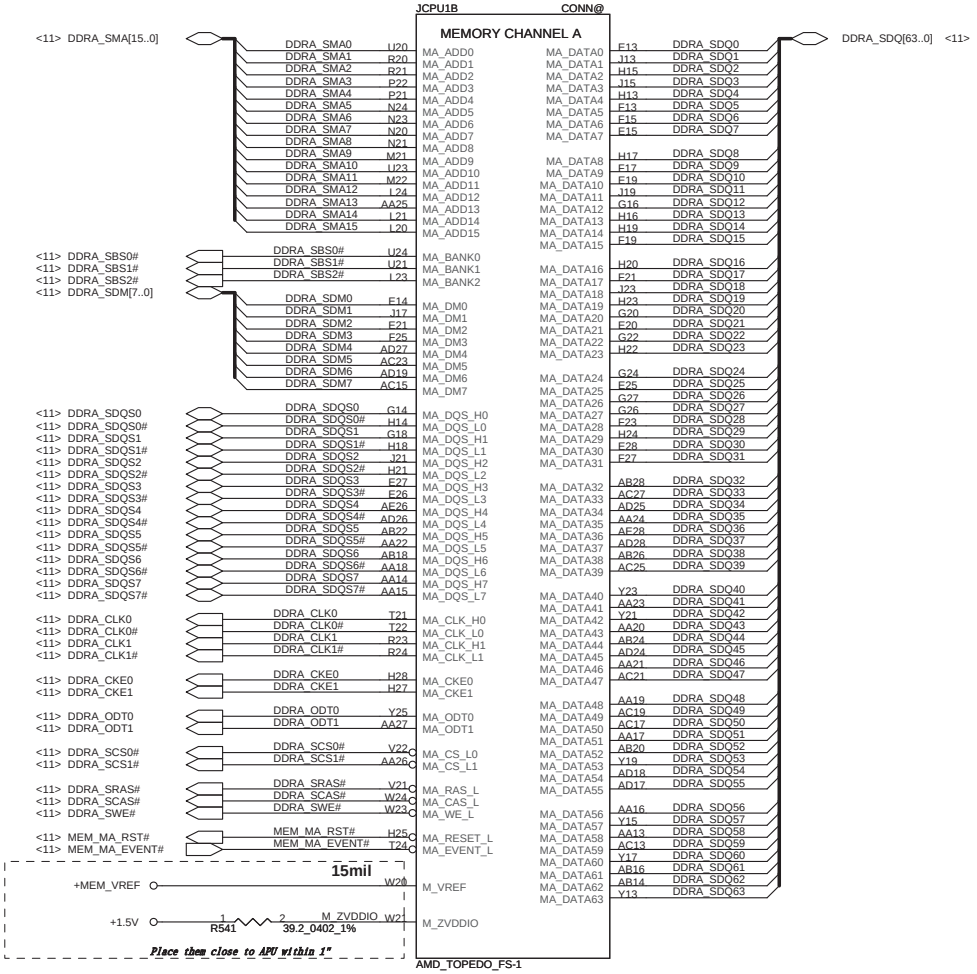
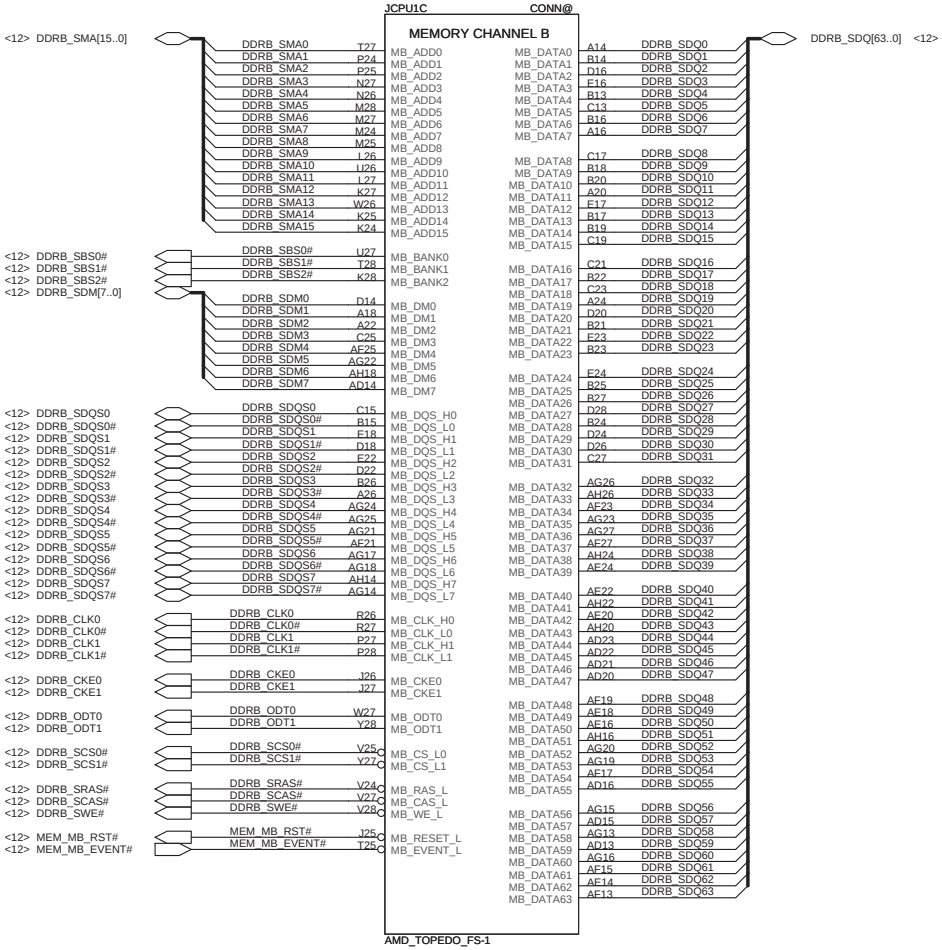
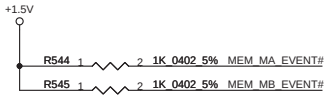
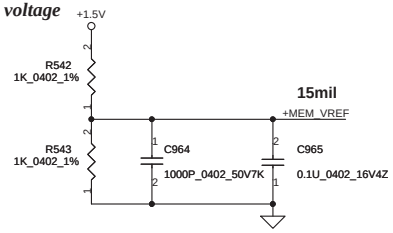




EVENT# pull high



0.75V reference voltage



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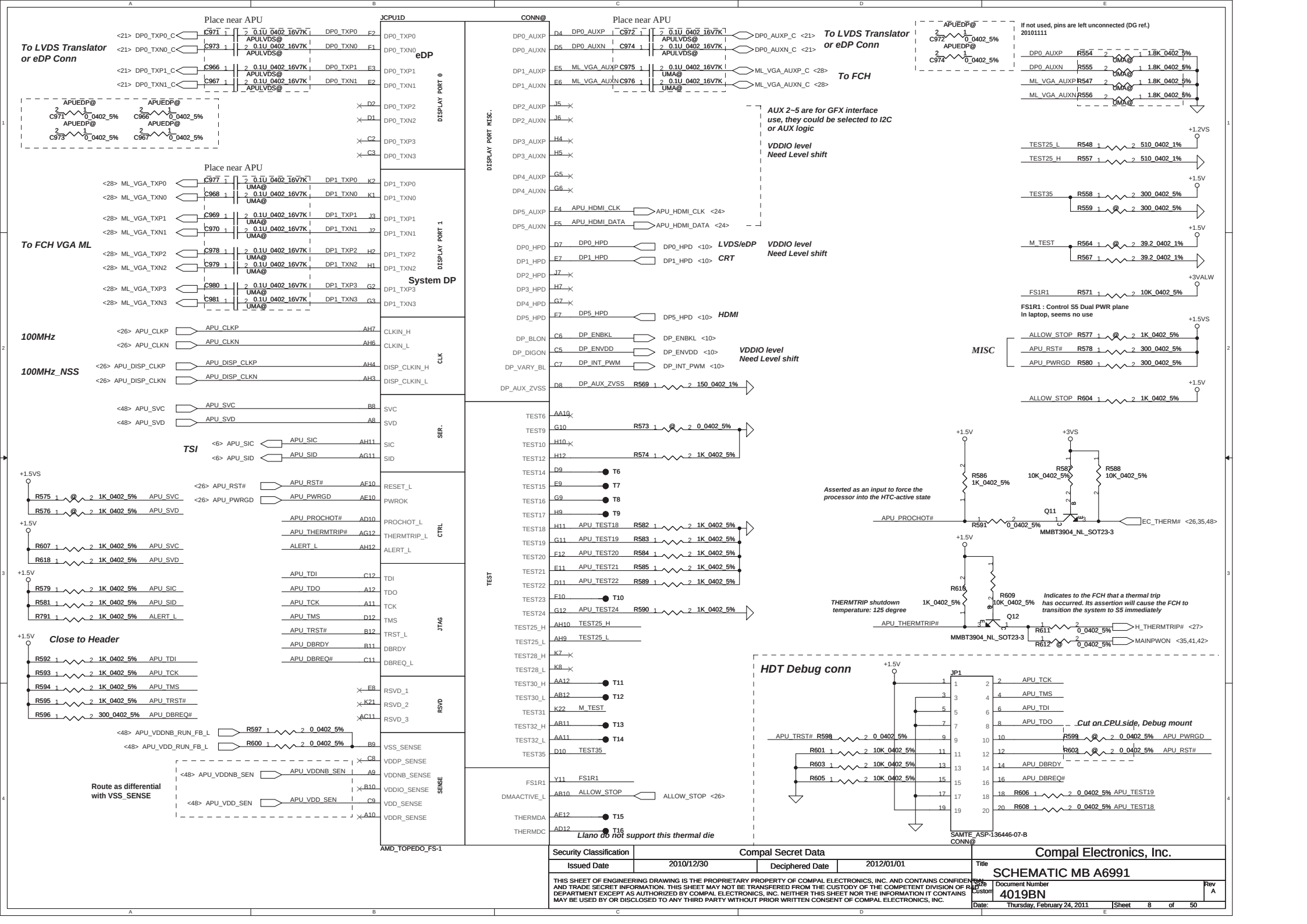

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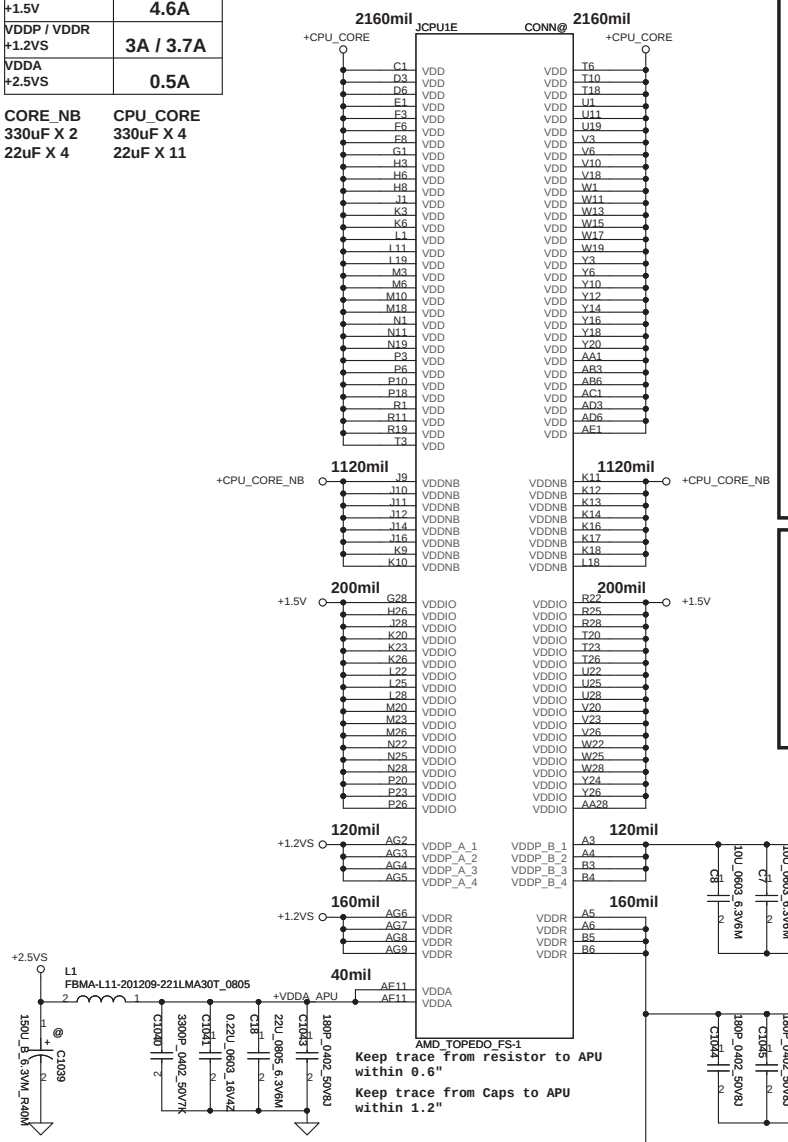
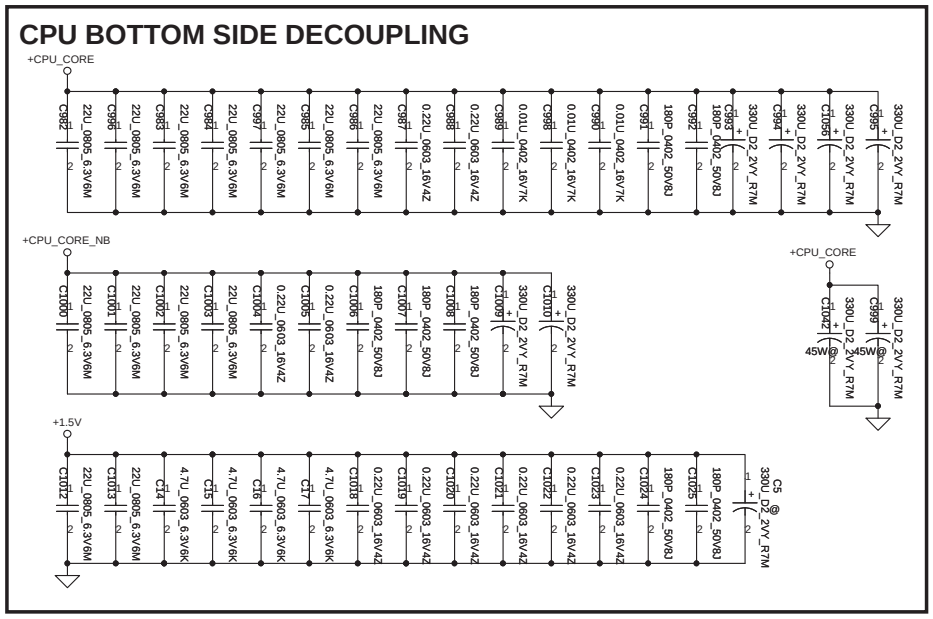
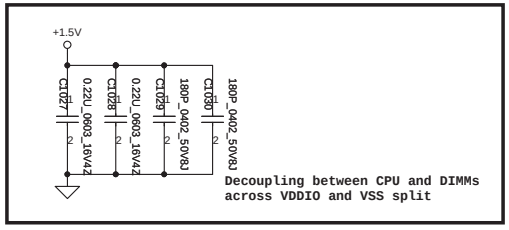
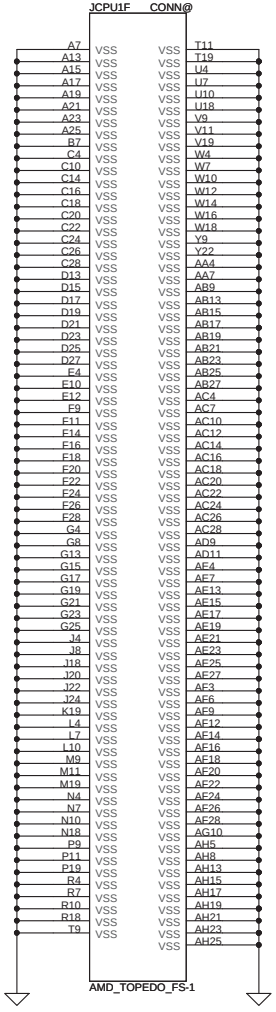
Power Name	Consumption
VDD +CPU_CORE	54A
VDDNB +CPU_CORE_NB	27.5A
VDDIO +1.5V	4.6A
VDDP / VDDR +1.2VS	3A / 3.7A
VDDA +2.5VS	0.5A

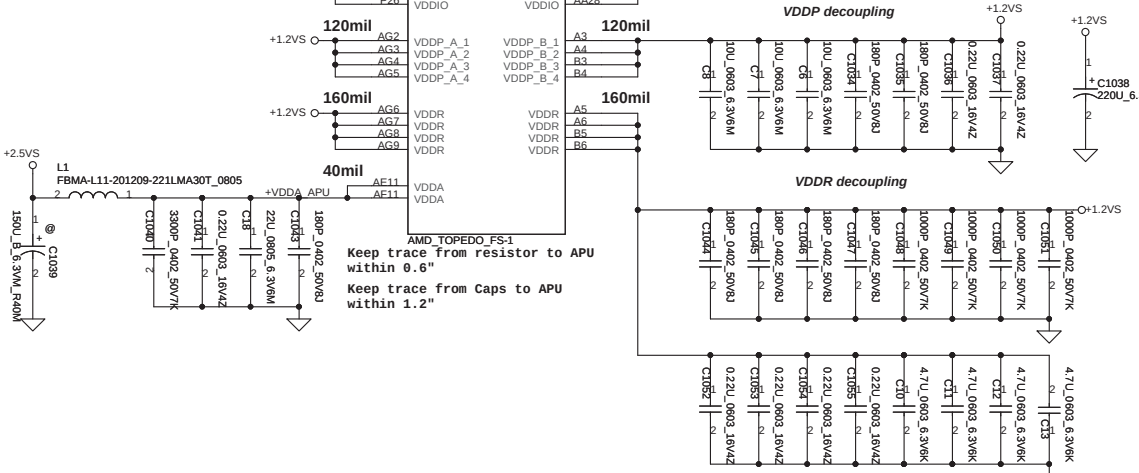
CORE_NB	CPU_CORE
330uF X 2	330uF X 4
22uF X 4	22uF X 11











Demo Board Capacitor (include PWM side)

CPU_CORE	CORE_NB	VDDIO_SUS (CPU side)	VDDIO_SUS (DIMM x2)	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	680uF x 1	100uF x 4	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	330uF x 1	0.1uF	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	22uF x 3			180pF x 2	1nF x 4
180uF x 2	180uF x 3	4.7uF x 4				180pF x 4
10nF x 3		0.22uF x 6				
		180pF x 4				

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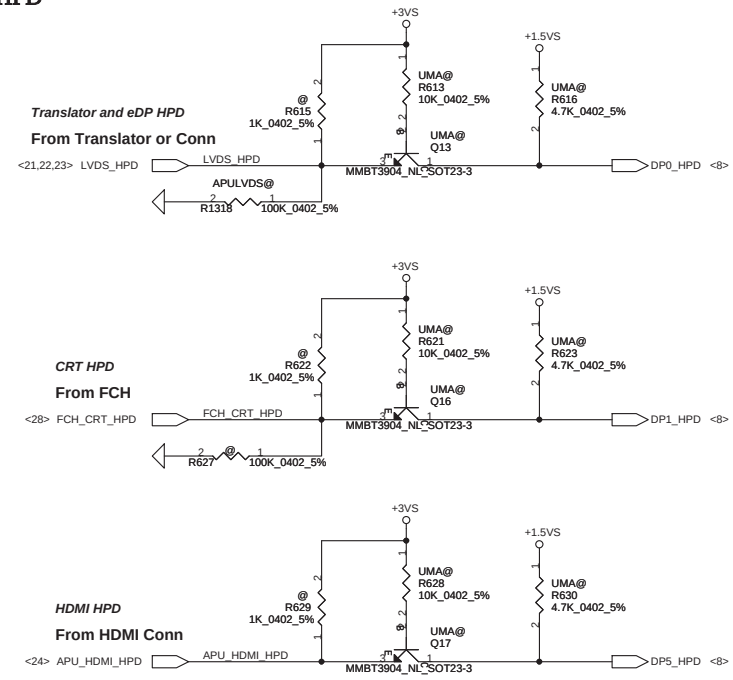
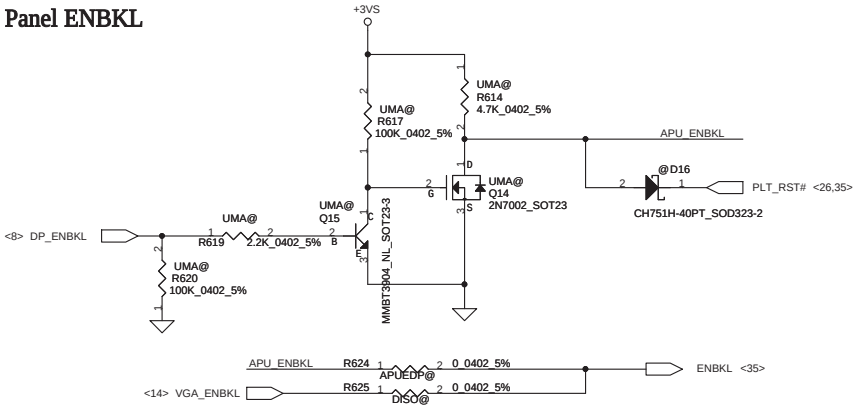
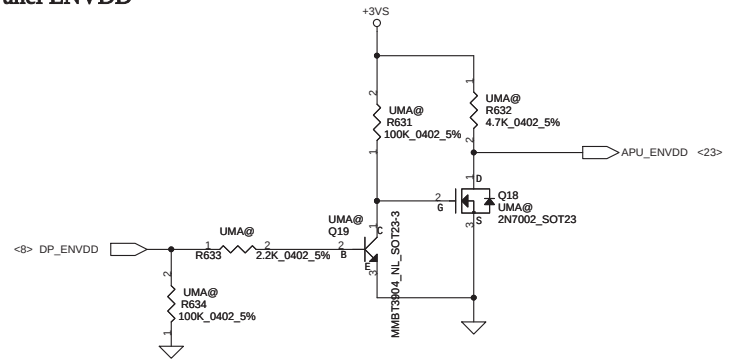
HPD



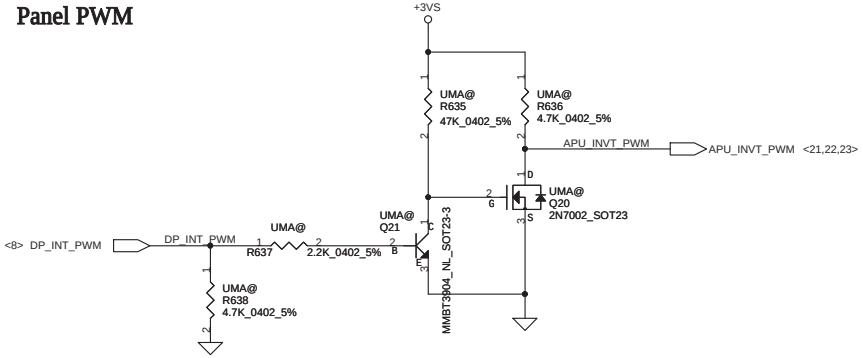
Panel ENBKL



Panel ENVDD



Panel PWM



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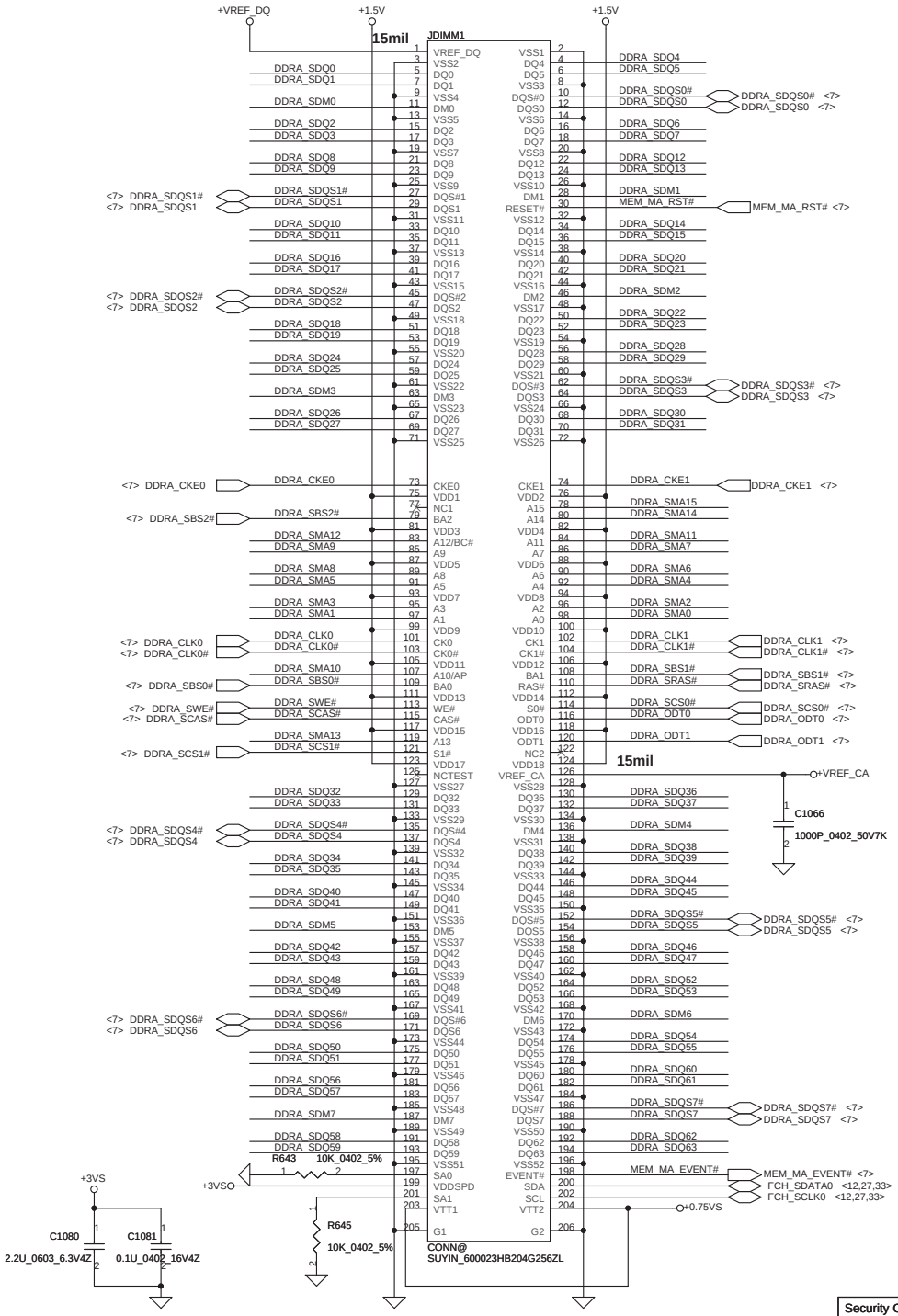
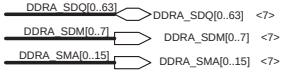
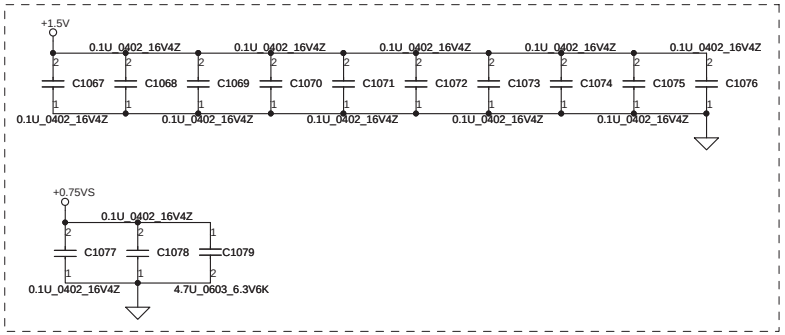
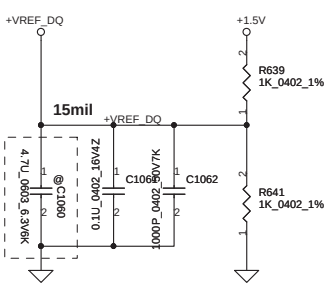
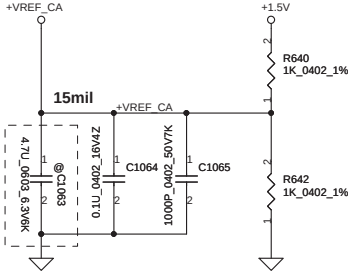




Place near DIMM1







DIMM_A STD H:8mm Change to SUYIN SP07000N500

<Address: 00>

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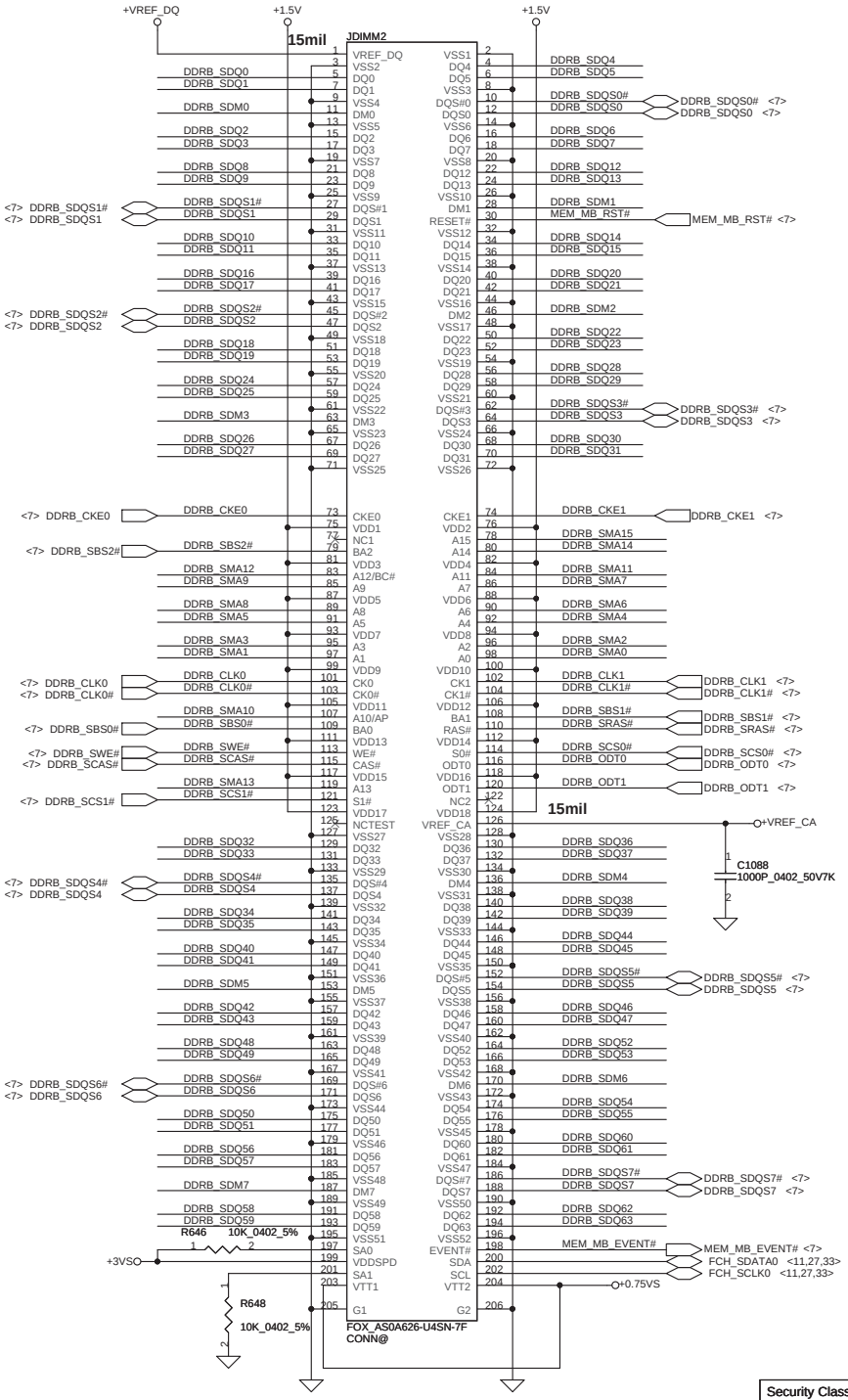
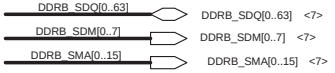
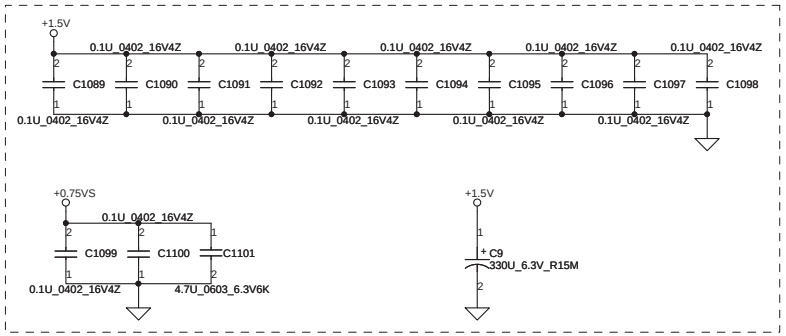
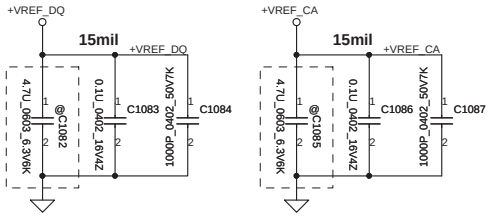




Place near DIMM2





DIMM_B STD H:4mm

<Address: 01>

P/N: SP07000H800

F/P: FOX_AS0A626-U4SN-7F_204P

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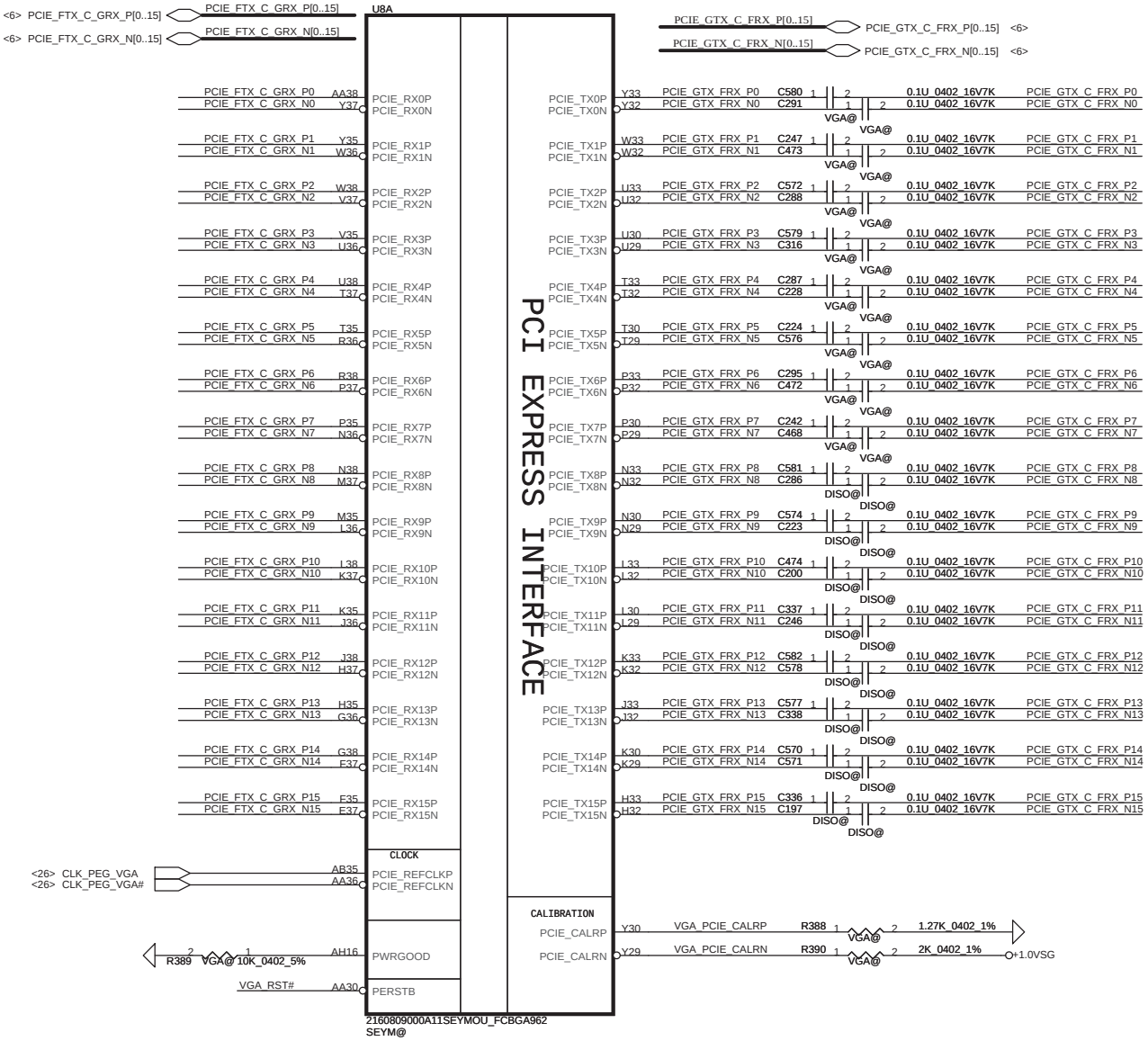
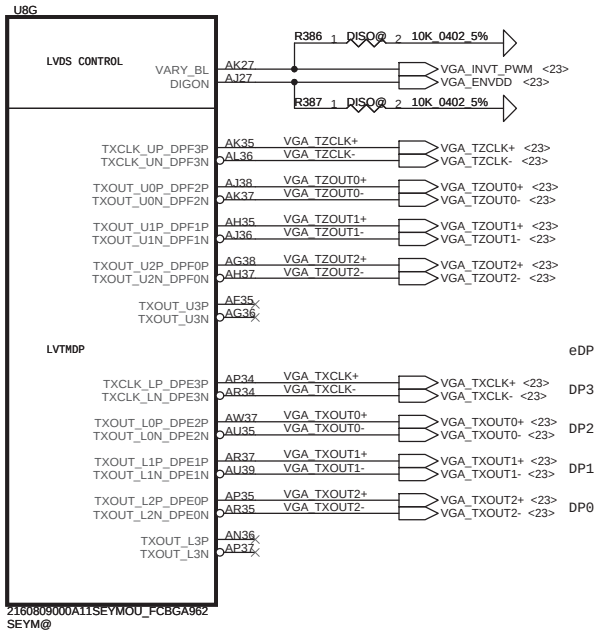
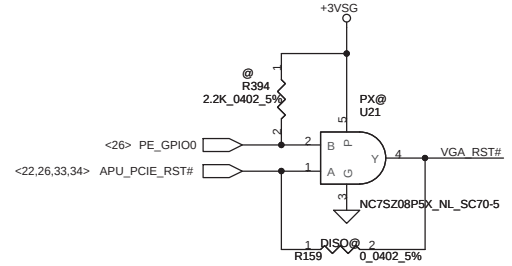
GFX PCIE LANE REVERSAL







U8 WHI@

216-0810005 A11

WHISTLER PRO M2 A11:
SA00004C720(S IC 216-0810005 A11 WHISTLER PRO FCBGA 962P ABO !)

Security Classification	Compal Secret Data		
Issued Date	2010/12/30	Deciphered Date	2012/01/01

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Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0] 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines 256 MB 001 * the primary memory aperture size. 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

SEYMOUR-XT

	ID3-0	Vendor	Size	Freq	P/N	Description	Qualify
	0000						
	0001						
*	0010	SAM	C-die 128*16	933MHz	SA0000047Q20	K4W2G1646C-HC11	
	0011	SAM	G-die 64*16	933MHz	SA00000GS10	K4W1G1646G-BC11	
	0100	SAM	E-die 64*16	800MHz	SA000035720	K4W1G1646E-HC12	V
	0101	SAM	C-die 128*16	800MHz	SA00003MQ60	K4W2G1646C-HC12	V
	0110						
	0111						
	1000						
	1001						
	1010						
	1011	HYN	Vega-die 64*16	800MHz	SA0000324G0	H5TQ1G63DFR-12C	
	1100	HYN	Orion-die 64*16	800MHz	SA0000324Z0	H5TQ1G63BFR-12C	
	1101	HYN	Vega-die 128*16	800MHz	SA00003VS10	H5TQ2G63BFR-12C	V
	1110	HYN	Vega-die 64*16	900MHz	SA000041S40	H5TQ1G63DFR-11C	V
*	1111	HYN	Vega-die 128*16	900MHz	SA00003YO20	H5TQ2G63BFR-11C	

WHISTLER-PRO

	ID3-0	Vendor	Size	Freq	P/N	Description	Qualify
	0000	SAM	E-die 64*16	800MHz	SA000035720	K4W1G1646E-HC12	V
	0001	SAM	C-die 128*16	800MHz	SA00003MQ60	K4W2G1646C-HC12	V
	0010	SAM	G-die 64*16	933MHz	SA00000GS10	K4W1G1646G-BC11	
*	0011	SAM	C-die 128*16	933MHz	SA000047Q20	K4W2G1646C-HC11	
	0100						
	0101						
	0110						
	0111						
	1000	HYN	Orion-die 64*16	800MHz	SA0000324Z0	H5TQ1G63BFR-12C	
	1001	HYN	Vega-die 128*16	800MHz	SA00003VS10	H5TQ2G63BFR-12C	V
	1010	HYN	Vega-die 64*16	900MHz	SA000041S40	H5TQ1G63DFR-11C	V
	1011	HYN	Vega-die 64*16	800MHz	SA0000324G0	H5TQ1G63DFR-12C	
*	1100	HYN	Vega-die 128*16	900MHz	SA00003YO20	H5TQ2G63BFR-11C	
	1101						
	1110						
	1111						

VRAM ID

External 27MHZ 3.3V CLK

External VGA Thermal Sensor

ADM1032ARMZ-2REEL_MSOP8

Q8A DMN66D0LDW-7_SOT363-6

Q8B DMN66D0LDW-7_SOT363-6

NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs

NC on Park, Robson and Seymour

Not share via for other GND

NC on Whistler and Seymour

SM010030010
200ma 120ohm@100mhz DCR 0.2

Park NC pins

Back compatibility(Manhattan)

Whistler and Seymour
Except A2VSSQ change to TSVSSQ, others are NC

HDMI

LVDS

NC on Park, Robson and Seymour

CRT

NC on Park, Robson and Seymour

Future ASIC call MLPS.
OLD ASIC is Fan PWM

2160809000A11SEYMOU_FCBGA962
SEYM@

HSYNC:VSYNC
11: Audio for both DisplayPort and HDMI

AUD Strap

CRT,HDMI DDC

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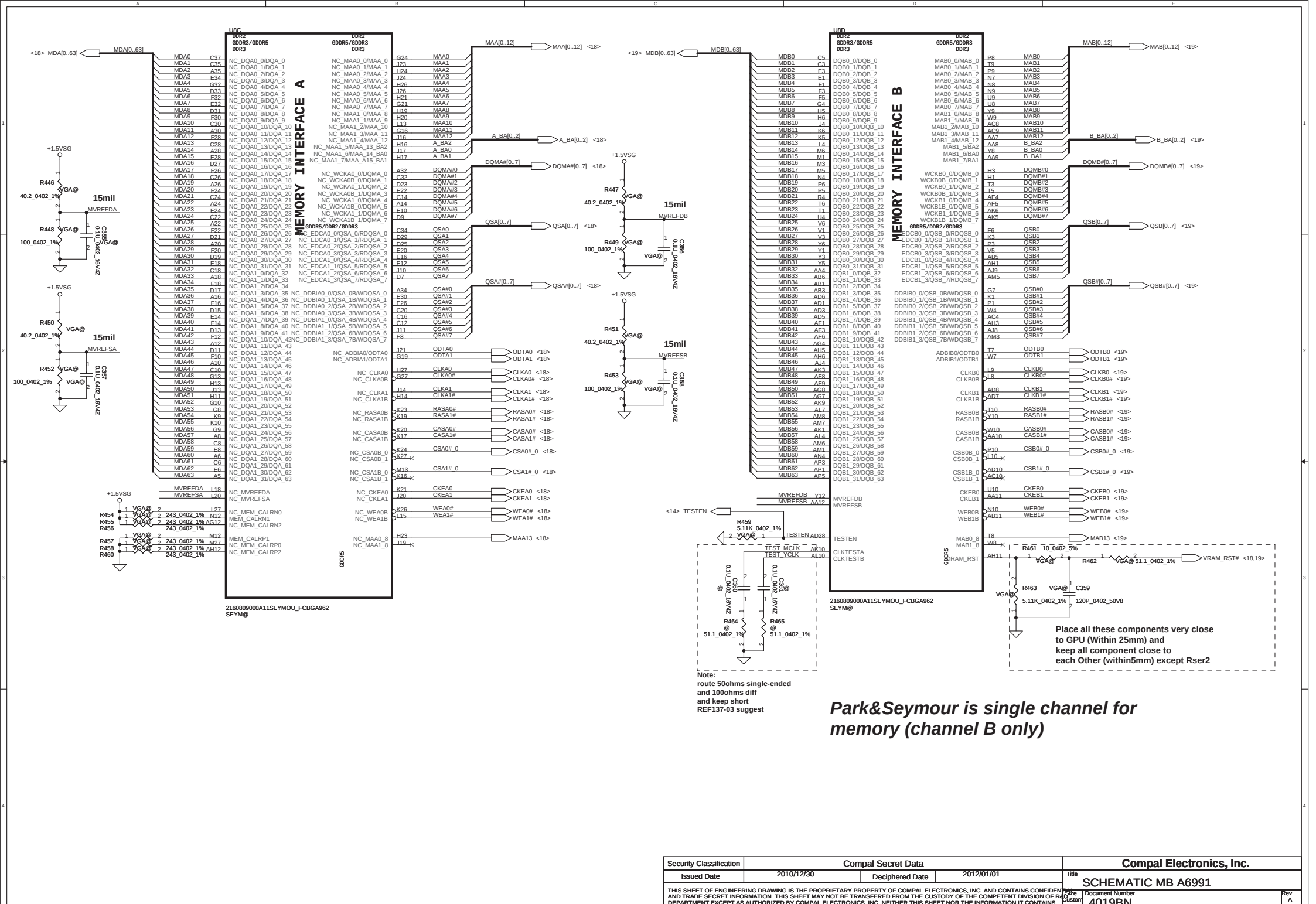

Park&Seymour is single channel for memory (channel B only)

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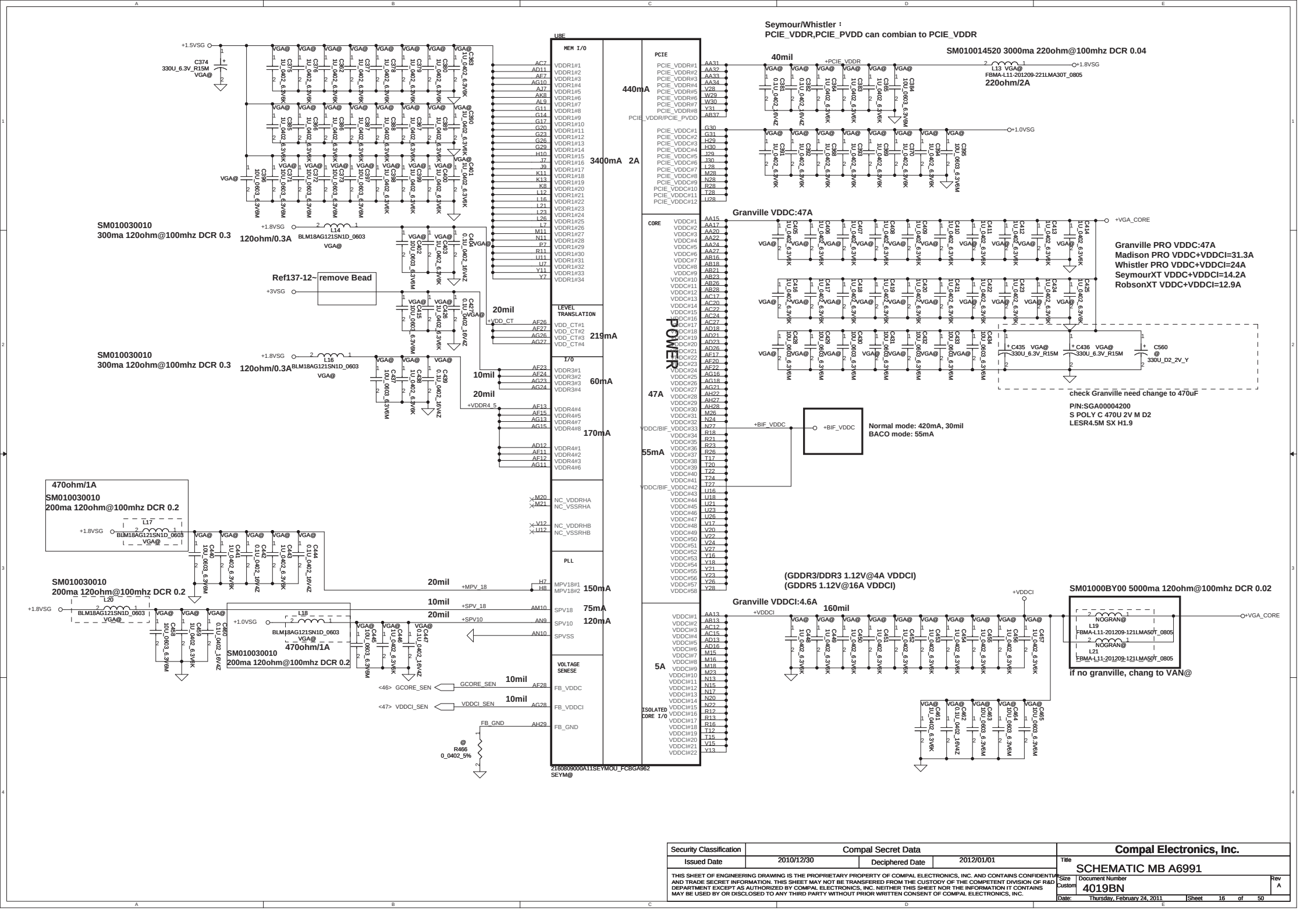

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DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

Seymour/Whistler：
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

U8F

GND

2160809000A11SEYMOU_FCBGA962
SEYM@

REF137-13 update

U8H

DP C/D POWER

DP A/B POWER

DP E/F POWER

DP PLL POWER

2160809000A11SEYMOU_FCBGA962
SEYM@

Manhatann:300mA
Seymour:150mA

Manhatann:220mA
Seymour:110mA

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L26
MCK1608471YZF_2P

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L27
MCK1608471YZF_2P

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L23
MCK1608471YZF_2P

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L25
MCK1608471YZF_2P

DP mode:300mA
LVDS mode:440mA

DP mode:220mA
LVDS mode:240mA

PX_EN

PX_EN <20>

PX_EN:
SBIOS will control VGA power on/off.
High :BACO mode enable
LOWLBACO disable

Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

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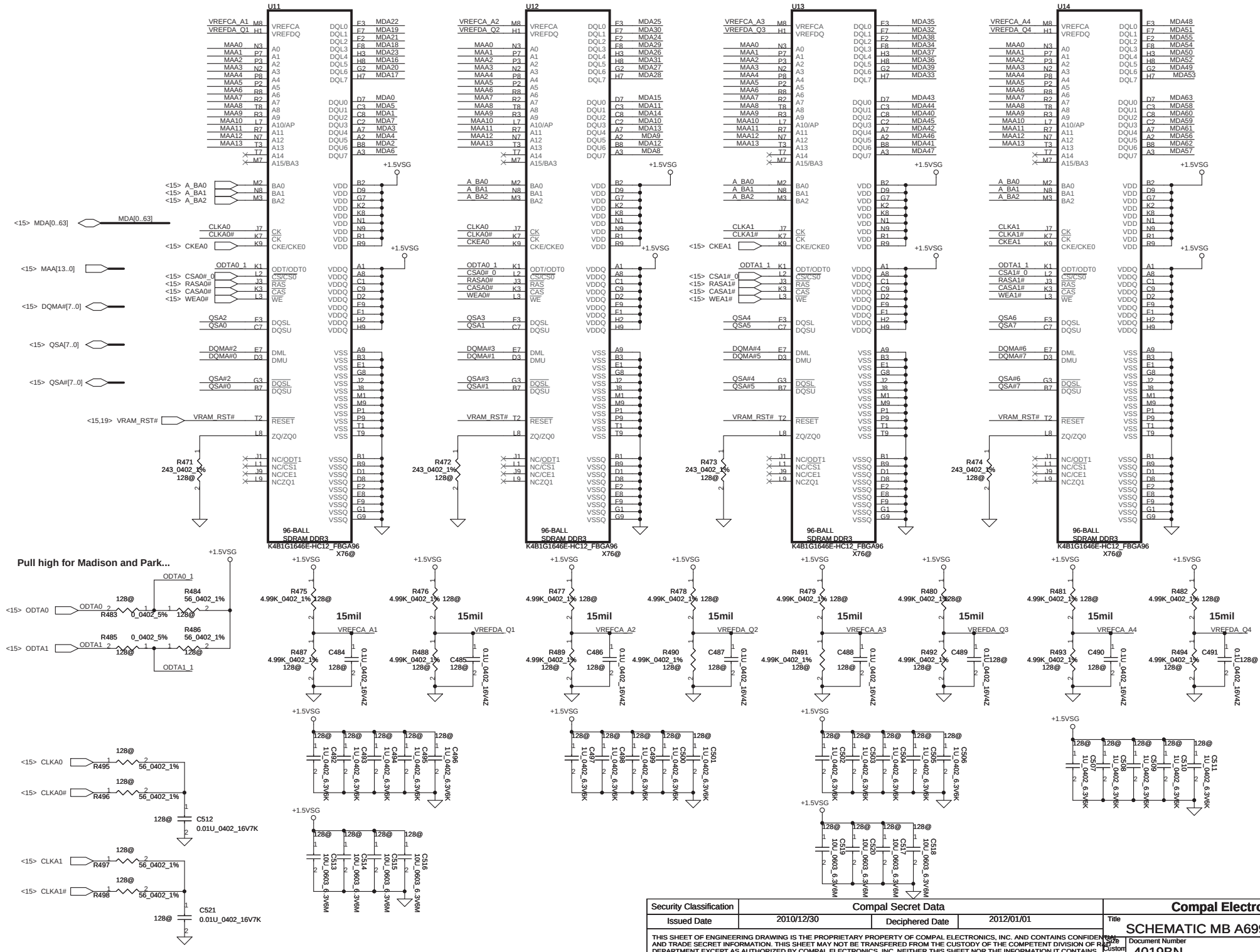

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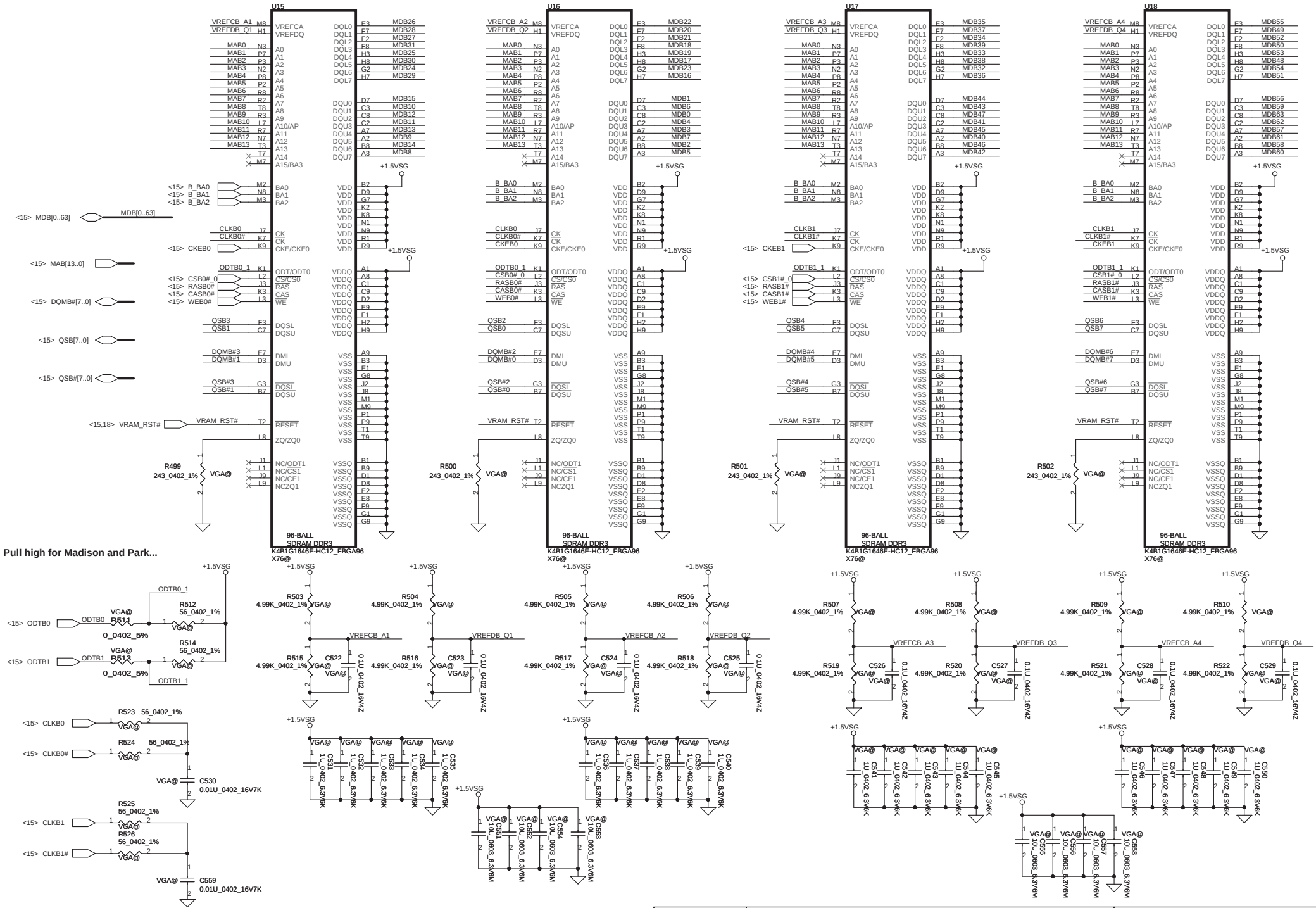

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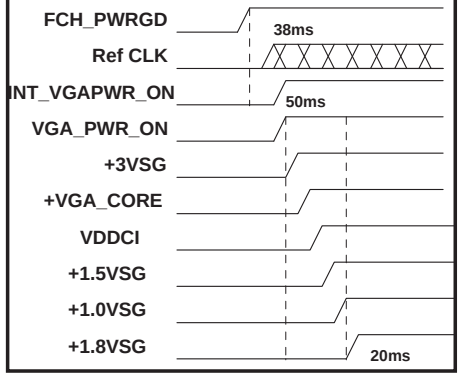
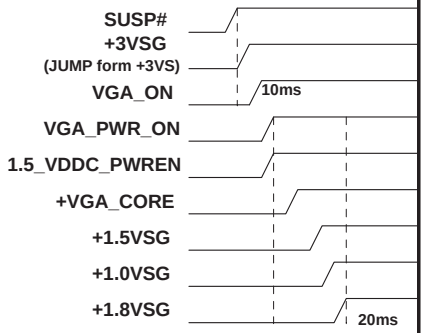
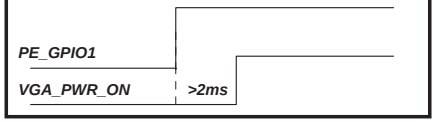
Power Sequence of Granville



Power Sequence of Whistler and Seymour



For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON



VGA Muxless and Dis only Status Mapping table			
	Dis only	Muxless High performance GPU	Muxless Power-saving GPU
VGA_PWR_ON	1	1	0
1.5_VDDC_PWREN	1	1	0
+3.3VSG	ON	ON	OFF
+1.8VSG	ON	ON	OFF
+1.0VSG	ON	ON	OFF
+VGA_CORE	ON	ON	OFF
+1.5VSG	ON	ON	OFF
+BIF_VDDC	+VGA_CORE	+VGA_CORE	OFF

VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
VGA_PWR_ON source signal	INT_VGAPWR_ON	VGA_ON
+3.3VSG	VGA_PWR_ON	SUSP#
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN

VGA Power ON Circuit

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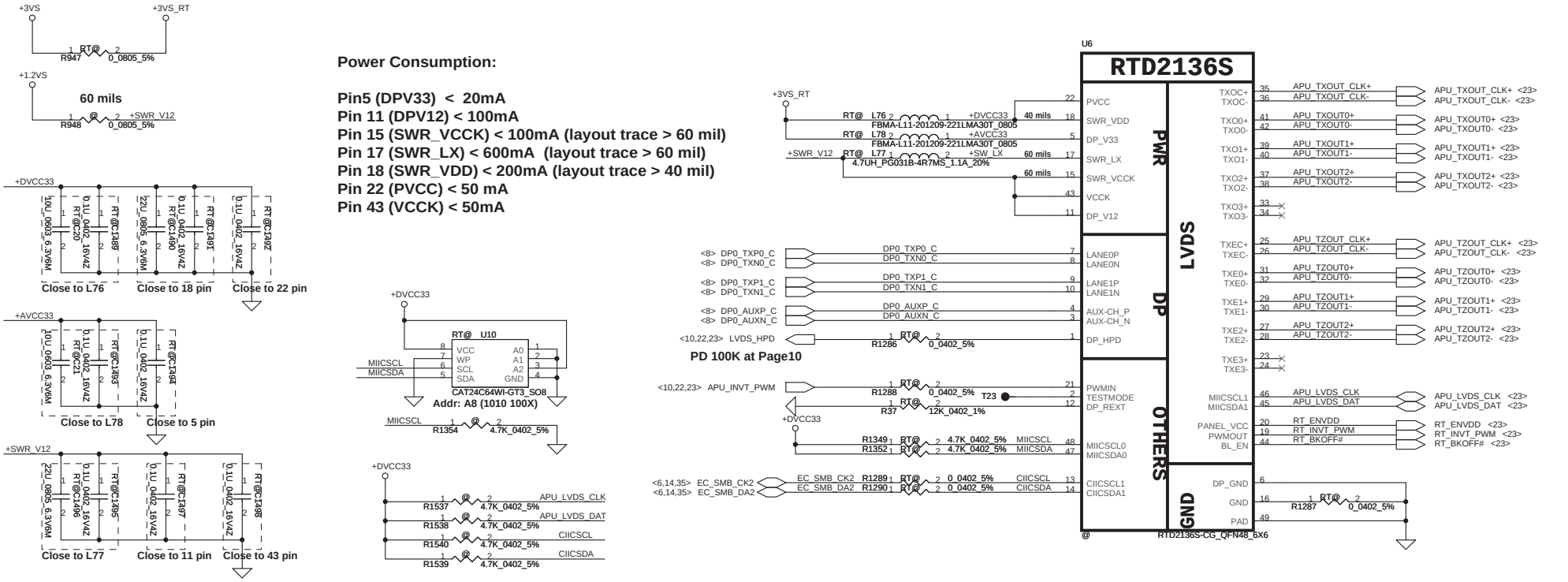

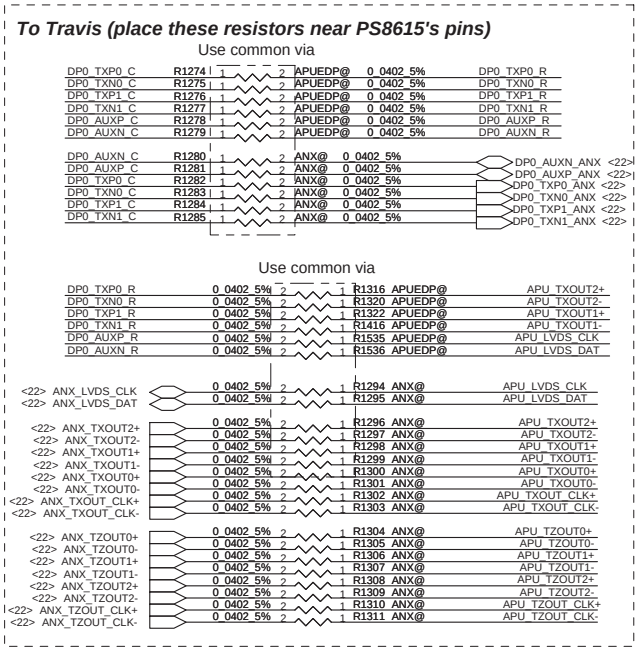

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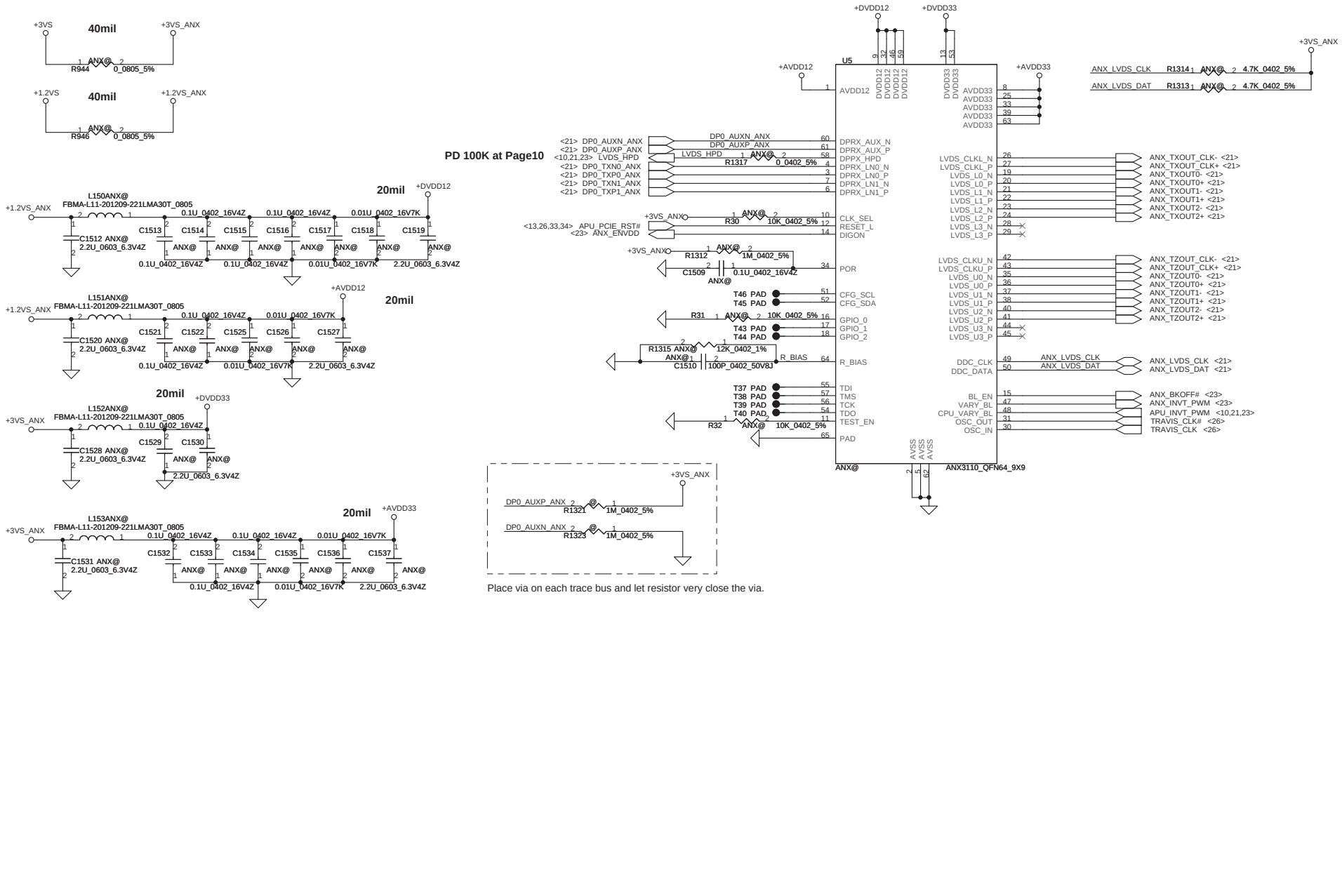

Place via on each trace bus and let resistor very close the via.

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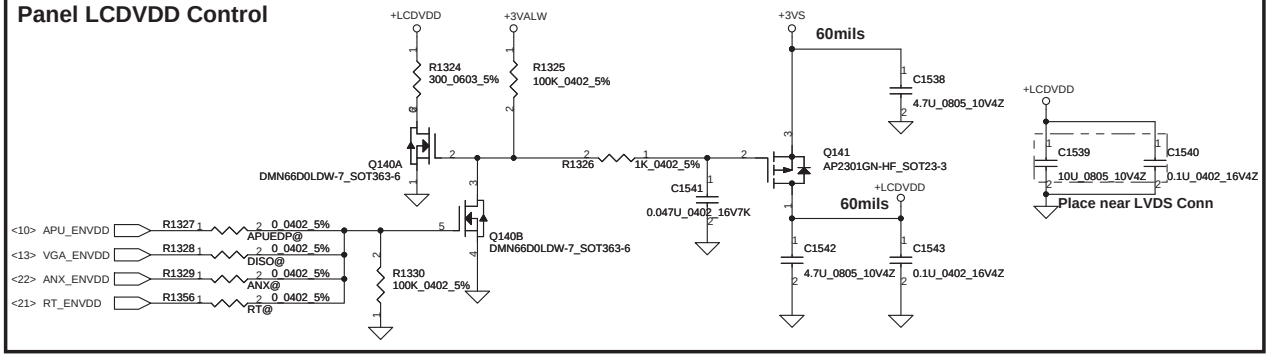
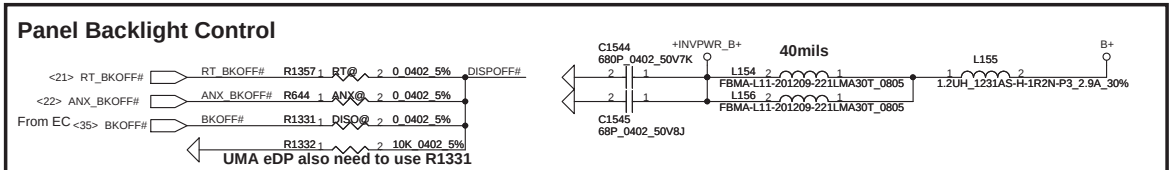
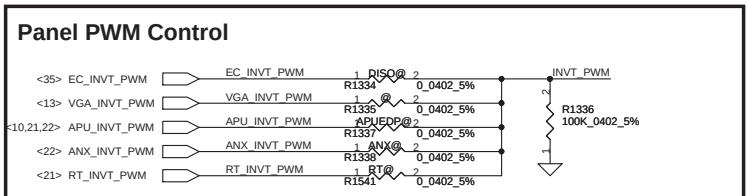
Panel LCDVDD Control



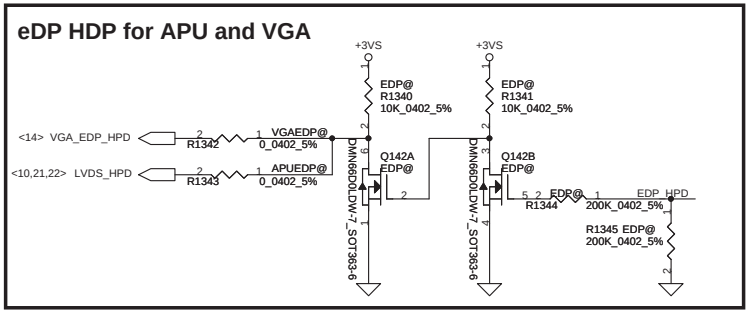
Panel Backlight Control



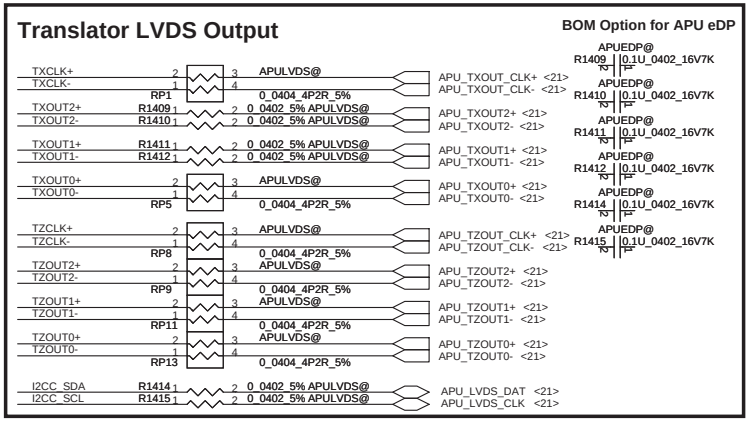
Panel PWM Control



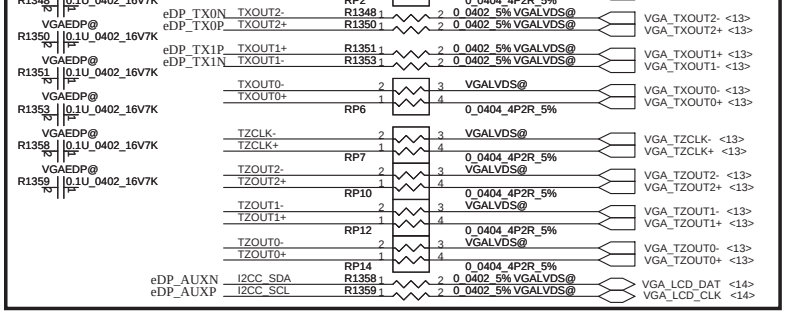
eDP HDP for APU and VGA



Translator LVDS Output



VGA LVDS Output (Reserve eDP)

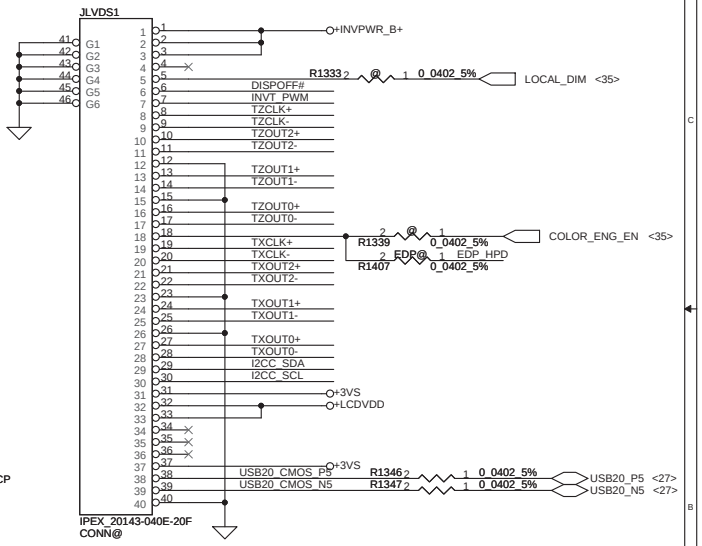


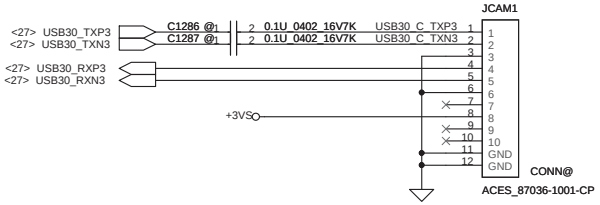
UMA/DIS LVDS/eDP Mapping table

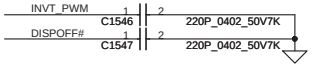
UMA		DIS		Panel
LVDS	eDP	LVDS	eDP	Conn.
APU_TXOUT0+ APU_TXOUT0-		VGA_TXOUT0+ VGA_TXOUT0-		TXOUT0+ TXOUT0-
APU_TXOUT1+ APU_TXOUT1-	DP0_TXP1_R DP0_TXN1_R	VGA_TXOUT1+ VGA_TXOUT1-	eDP_TX1P eDP_TX1N	TXOUT1+ TXOUT1-
APU_TXOUT2+ APU_TXOUT2-	DP0_TXP0_R DP0_TXN0_R	VGA_TXOUT2+ VGA_TXOUT2-	eDP_TX0P eDP_TX0N	TXOUT2+ TXOUT2-
APU_TXOUT_CLK+ APU_TXOUT_CLK-		VGA_TXCLK+ VGA_TXCLK-		TXCLK+ TXCLK-
APU_TZOUT0+ APU_TZOUT0-		VGA_TZOUT0+ VGA_TZOUT0-		TZOUT0+ TZOUT0-
APU_TZOUT1+ APU_TZOUT1-		VGA_TZOUT1+ VGA_TZOUT1-		TZOUT1+ TZOUT1-
APU_TZOUT2+ APU_TZOUT2-		VGA_TZOUT2+ VGA_TZOUT2-		TZOUT2+ TZOUT2-
APU_TZOUT_CLK+ APU_TZOUT_CLK-		VGA_TZCLK+ VGA_TZCLK-		TZCLK+ TZCLK-
APU_LVDS_CLK APU_LVDS_DAT	DP0_AUXP_R DP0_AUXN_R	VGA_LCD_CLK VGA_LCD_DATA	eDP_AUXP eDP_AUXN	I2CC_SCL I2CC_SDA

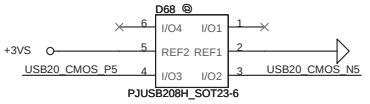
LCD/LED PANEL Conn.

P/N: SP010016810
F/P: IPEX_20143-040E-20F_40P









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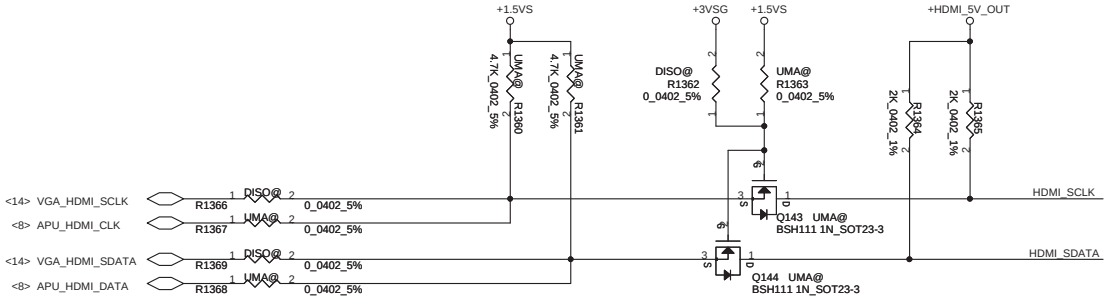
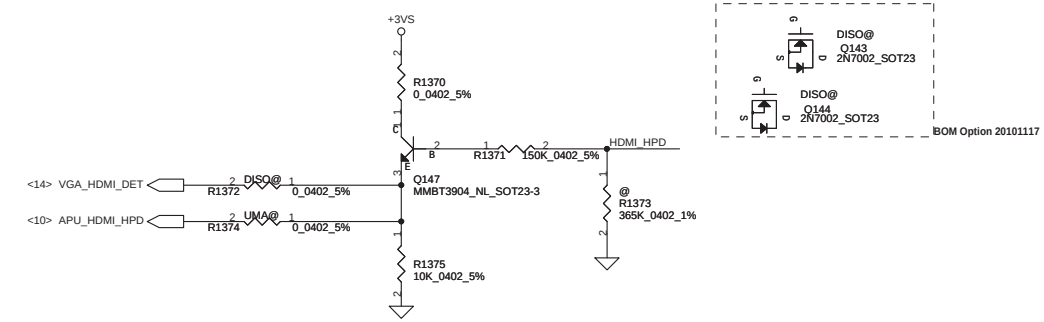
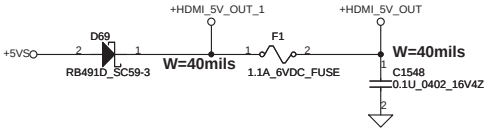
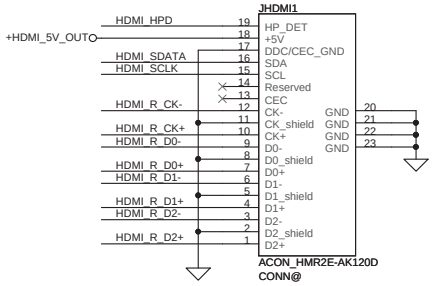








<P7YE0 use>

P/N: DC232000Y00
F/P: ACON_HMR2E-AK120D_19P

Place near C917~C924 and use common via

From VGA

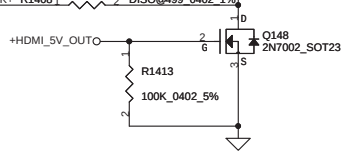
<14> VGA_HDMI_TXD2-	DISO@	R1378	0_0402_5%	HDMI_C_TX2- R
<14> VGA_HDMI_TXD2+	DISO@	R1379	0_0402_5%	HDMI_C_TX2+ R
<14> VGA_HDMI_TXD1-	DISO@	R1380	0_0402_5%	HDMI_C_TX1- R
<14> VGA_HDMI_TXD1+	DISO@	R1382	0_0402_5%	HDMI_C_TX1+ R
<14> VGA_HDMI_TXD0-	DISO@	R1383	0_0402_5%	HDMI_C_TX0- R
<14> VGA_HDMI_TXD0+	DISO@	R1384	0_0402_5%	HDMI_C_TX0+ R
<14> VGA_HDMI_TXC-	DISO@	R1385	0_0402_5%	HDMI_C_CLK- R
<14> VGA_HDMI_TXC+	DISO@	R1386	0_0402_5%	HDMI_C_CLK+ R

From APU

<6> PCIE_FTX_GRX_N12	UMA@	R1388	0_0402_5%	HDMI_C_TX2- R
<6> PCIE_FTX_GRX_P12	UMA@	R1389	0_0402_5%	HDMI_C_TX2+ R
<6> PCIE_FTX_GRX_N13	UMA@	R1390	0_0402_5%	HDMI_C_TX1- R
<6> PCIE_FTX_GRX_P13	UMA@	R1392	0_0402_5%	HDMI_C_TX1+ R
<6> PCIE_FTX_GRX_N14	UMA@	R1393	0_0402_5%	HDMI_C_TX0- R
<6> PCIE_FTX_GRX_P14	UMA@	R1394	0_0402_5%	HDMI_C_TX0+ R
<6> PCIE_FTX_GRX_N15	UMA@	R1395	0_0402_5%	HDMI_C_CLK- R
<6> PCIE_FTX_GRX_P15	UMA@	R1396	0_0402_5%	HDMI_C_CLK+ R

Near the connector

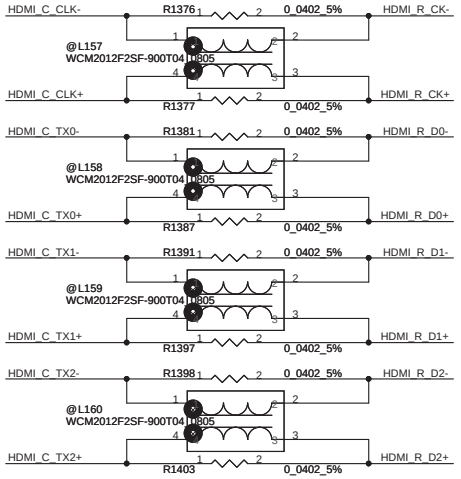
HDMI_C_TX2- R	C1549	0.1U_0402_16V7K	HDMI_C_TX2-	R1399 DISO@499_0402_1%
HDMI_C_TX2+ R	C1550	0.1U_0402_16V7K	HDMI_C_TX2+	R1400 DISO@499_0402_1%
HDMI_C_TX1- R	C1551	0.1U_0402_16V7K	HDMI_C_TX1-	R1401 DISO@499_0402_1%
HDMI_C_TX1+ R	C1552	0.1U_0402_16V7K	HDMI_C_TX1+	R1402 DISO@499_0402_1%
HDMI_C_TX0- R	C1553	0.1U_0402_16V7K	HDMI_C_TX0-	R1404 DISO@499_0402_1%
HDMI_C_TX0+ R	C1554	0.1U_0402_16V7K	HDMI_C_TX0+	R1405 DISO@499_0402_1%
HDMI_C_CLK- R	C1555	0.1U_0402_16V7K	HDMI_C_CLK-	R1406 DISO@499_0402_1%
HDMI_C_CLK+ R	C1556	0.1U_0402_16V7K	HDMI_C_CLK+	R1408 DISO@499_0402_1%



UMA use 604 ohm
VGA use 499 ohm

For UMA HDMI termination BOM option

R1399 2 UMA@1_604_0402_1%
R1400 2 UMA@1_604_0402_1%
R1401 2 UMA@1_604_0402_1%
R1402 2 UMA@1_604_0402_1%
R1404 2 UMA@1_604_0402_1%
R1405 2 UMA@1_604_0402_1%
R1406 2 UMA@1_604_0402_1%
R1408 2 UMA@1_604_0402_1%



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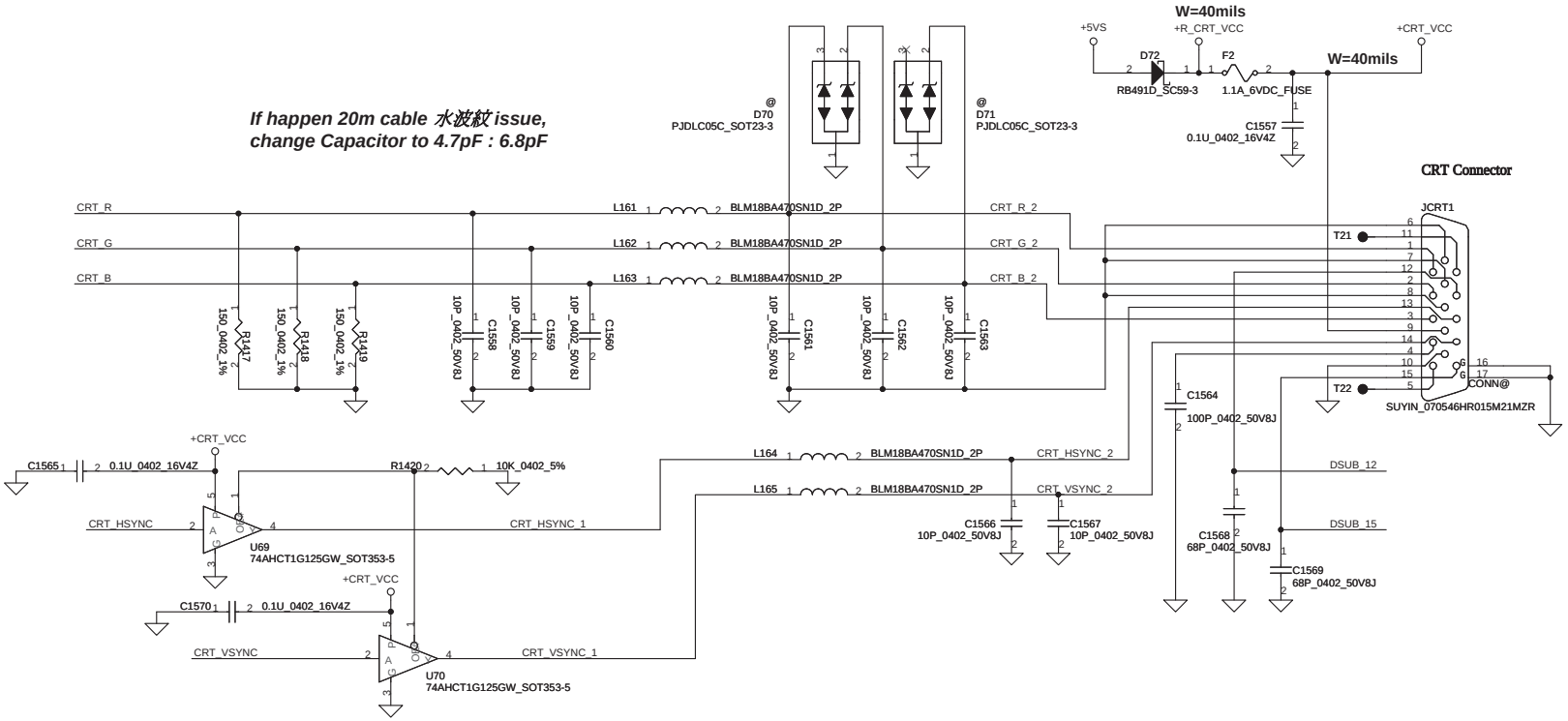


Use common via

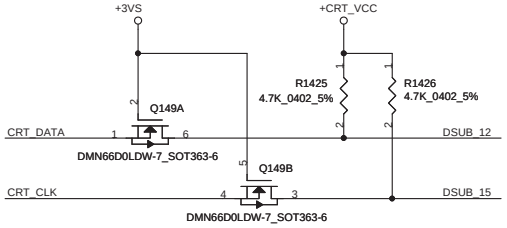
From FCH

<28> FCH_CRT_R	FCH_CRT_R	R1421	UMA@	0_0402_5%	CRT_R
<28> FCH_CRT_G	FCH_CRT_G	R1422	UMA@	0_0402_5%	CRT_G
<28> FCH_CRT_B	FCH_CRT_B	R1423	UMA@	0_0402_5%	CRT_B
<28> FCH_CRT_HSYNC	FCH_CRT_HSYNC	R1424	UMA@	0_0402_5%	CRT_HSYNC
<28> FCH_CRT_VSYNC	FCH_CRT_VSYNC	R1427	UMA@	0_0402_5%	CRT_VSYNC
<28> FCH_CRT_DDC_SDA	FCH_CRT_DDC_SDA	R1428	UMA@	0_0402_5%	CRT_DATA
<28> FCH_CRT_DDC_SCL	FCH_CRT_DDC_SCL	R1429	UMA@	0_0402_5%	CRT_CLK

From VGA

<14> VGA_CRT_R	VGA_CRT_R	R1430	DISC@	0_0402_5%	CRT_R
<14> VGA_CRT_G	VGA_CRT_G	R1431	DISC@	0_0402_5%	CRT_G
<14> VGA_CRT_B	VGA_CRT_B	R1432	DISC@	0_0402_5%	CRT_B
<14> VGA_CRT_HSYNC	VGA_CRT_HSYNC	R1433	DISC@	0_0402_5%	CRT_HSYNC
<14> VGA_CRT_VSYNC	VGA_CRT_VSYNC	R1434	DISC@	0_0402_5%	CRT_VSYNC
<14> VGA_CRT_DATA	VGA_CRT_DATA	R1435	DISC@	0_0402_5%	CRT_DATA
<14> VGA_CRT_CLK	VGA_CRT_CLK	R1436	DISC@	0_0402_5%	CRT_CLK

Close to Conn side



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U25A

HUDSON-2

PCI Host Bus Reset (To EC)

C1188 150P_0402_50V8J

<10,35> PLT_RST# R825 33_0402_5% APU_PCIE_RST#_C AE2 PCIE_RST#

AD5 A_RST#

PCI CLKS

PCICLK0 AE3
PCICLK1/GPO36 AF1 → PCI_CLK1 <29>
PCICLK2/GPO37 AF5
PCICLK3/GPO38 AG2 → PCI_CLK3 <29>
PCICLK4/14M_OSC/GPO39 AF6 → PCI_CLK4 <29>

PCIRST# AB5

PCI EXPRESS INTERFACES

<6> UMI_MTX_C_FRX_P0	C1189 0.1U_0402_16V7K	UMI_MTX_FRX_P0	AE30 UMI_TX0P
<6> UMI_MTX_C_FRX_N0	C1190 0.1U_0402_16V7K	UMI_MTX_FRX_N0	AE32 UMI_TX0N
<6> UMI_MTX_C_FRX_P1	C1191 0.1U_0402_16V7K	UMI_MTX_FRX_P1	AD33 UMI_TX1P
<6> UMI_MTX_C_FRX_N1	C1192 0.1U_0402_16V7K	UMI_MTX_FRX_N1	AD31 UMI_TX1N
<6> UMI_MTX_C_FRX_P2	C1196 0.1U_0402_16V7K	UMI_MTX_FRX_P2	AD28 UMI_TX2P
<6> UMI_MTX_C_FRX_N2	C1197 0.1U_0402_16V7K	UMI_MTX_FRX_N2	AD29 UMI_TX2N
<6> UMI_MTX_C_FRX_P3	C1198 0.1U_0402_16V7K	UMI_MTX_FRX_P3	AC30 UMI_TX3P
<6> UMI_MTX_C_FRX_N3	C1194 0.1U_0402_16V7K	UMI_MTX_FRX_N3	AC32 UMI_TX3N

<6> UMI_FTX_C_MRX_P0	UMI_FTX_C_MRX_P0	AB33 UMI_RX0P
<6> UMI_FTX_C_MRX_N0	UMI_FTX_C_MRX_N0	AB31 UMI_RX0N
<6> UMI_FTX_C_MRX_P1	UMI_FTX_C_MRX_P1	AB28 UMI_RX1P
<6> UMI_FTX_C_MRX_N1	UMI_FTX_C_MRX_N1	AB29 UMI_RX1N
<6> UMI_FTX_C_MRX_P2	UMI_FTX_C_MRX_P2	Y33 UMI_RX2P
<6> UMI_FTX_C_MRX_N2	UMI_FTX_C_MRX_N2	Y31 UMI_RX2N
<6> UMI_FTX_C_MRX_P3	UMI_FTX_C_MRX_P3	Y28 UMI_RX3P
<6> UMI_FTX_C_MRX_N3	UMI_FTX_C_MRX_N3	Y29 UMI_RX3N

+PCIE_VDDR_FCH R827 590_0402_1% PCIE_CALRP AE29 PCIE_CALRP
R828 2K_0402_1% PCIE_CALRN AE31 PCIE_CALRN

V33	GPP_TX0P
V31	GPP_TX0N
W30	GPP_TX1P
W32	GPP_TX1N
AB26	GPP_TX2P
AB27	GPP_TX2N
AA24	GPP_TX3P
AA23	GPP_TX3N
AA27	GPP_RX0P
AA26	GPP_RX0N
W27	GPP_RX1P
V27	GPP_RX1N
V26	GPP_RX2P
W26	GPP_RX2N
W24	GPP_RX3P
W23	GPP_RX3N

PCI INTERFACE

AJ3	GPIO0	
AL5	GPIO1	
AG4	GPIO2	
AL6	GPIO3	
AH3	GPIO4	
AJ5	GPIO5	
AL1	GPIO6	
AN5	GPIO7	
AN6	GPIO8	
AJ1	GPIO9	
AL8	GPIO10	
AL3	GPIO11	
AM7	GPIO12	
AJ6	GPIO13	
AK7	GPIO14	
AN8	GPIO15	
AG9	GPIO16	
AM11	GPIO17	
AJ10	GPIO18	
AL12	GPIO19	
AK11	GPIO20	
AN12	GPIO21	
AG12	GPIO22	
AE12	GPIO23	→ PCI_AD23 <29>
AC12	GPIO24	→ PCI_AD24 <29>
AE13	GPIO25	→ PCI_AD25 <29>
AF13	GPIO26	→ PCI_AD26 <29>
AH13	GPIO27	→ PCI_AD27 <29>
AH14	GPIO28	VGA_PWRGD_R
AD15	GPIO29	
AC15	GPIO30	
AE16	GPIO31	
AN3	CBE0#	
AJ8	CBE1#	
AN10	CBE2#	
AD12	CBE3#	
AG10	FRAME#	
AK9	DEVSEL#	
AL10	IRDY#	
AE10	TRDY#	
AE10	PAR	
AH1	STOP#	
AM9	PERR#	
AH8	SERR#	
AG15	REQ0#	
AG13	REQ1#/GPIO40	
AF15	REQ2#/CLK_REQ8#/GPIO41	
AM17	REQ3#/CLK_REQ5#/GPIO42	
AD16	GNT0#	
AD13	GNT1#/GPO44	R842 PX@ 0_0402_5% / R843 PX@ 0_0402_5% → PE_GPIO0 <13>, PE_GPIO1 <20>
AD21	GNT2#/SD_LED/GPO45	
AK17	GNT3#/CLK_REQ7#/GPIO46	
AD19	CLKRUN#	
AH9	LOCK#	
AF18	INTE#/GPIO32	
AE18	INTF#/GPIO33	
AC16	INTG#/GPIO34	
AD18	INTH#/GPIO35	

For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)

+3VALW C1193 0.1U_0402_16V4Z

APU_PCIE_RST#_C R829 33_0402_5% → U26 NC7SZ08P5X_NL_SC70-5 → APU_PCIE_RST# <13,22,33,34>

C1195 @ 150P_0402_50V8J
R826 @ 8.2K_0402_5%

+3VALW @C1199 0.1U_0402_16V4Z

PU to +3VS on PWR side

<20,46> VGA_PWRGD → @U27 NC7SZ08P5X_NL_SC70-5 → VGA_PWRGD_R

R830 @ 0_0402_5%
R831 @ 100K_0402_5%
R832 0_0402_5%

Level shift to ISL6267

+1.5VS R834 10K_0402_5%
+3VS R836 4.7K_0402_5%
APU_PWRGD → Q38 MMBT3904_NL_SOT23-3 → APU_PWRGD_L <48>

RTC BATT Conn.

+RTCBATT CONN@ JBATT1
P/N: SP07000OU00
F/P: SUYIN_060003HA002G202ZL_2P
SUYIN_060003HA002G202ZL

CLOCK GENERATOR

+1.1VS_CKVDD R833 2K_0402_1% CLK_CALRN F27 CLK_CALRN

SS For "EXT" CLK Gen

G30 PCIE_RCLKP
G28 PCIE_RCLKN

NSS

APU DISP	<8> APU_DISP_CLKP	APU_DISP_CLKP	R26 DISP_CLKP
	<8> APU_DISP_CLKN	APU_DISP_CLKN	T26 DISP_CLKN
LVDS IC	<22> TRAVIS_CLK	TRAVIS_CLK	H33 DISP2_CLKP
	<22> TRAVIS_CLK#	TRAVIS_CLK#	H31 DISP2_CLKN
APU	<8> APU_CLKP	APU_CLKP	T24 APU_CLKP
	<8> APU_CLKN	APU_CLKN	T23 APU_CLKN
VGA	<13> CLK_PEG_VGA	CLK_PEG_VGA	J30 SLT_GFX_CLKP
	<13> CLK_PEG_VGA#	CLK_PEG_VGA#	K29 SLT_GFX_CLKN

H27	GPP_CLK0P
H28	GPP_CLK0N
J27	GPP_CLK1P
K26	GPP_CLK1N

SS

WLAN	<33> CLK_PCIE_MINI1	CLK_PCIE_MINI1	F33 GPP_CLK2P
	<33> CLK_PCIE_MINI1#	CLK_PCIE_MINI1#	E31 GPP_CLK2N
GLAN	<34> CLK_PCIE_LAN	CLK_PCIE_LAN	E33 GPP_CLK3P
	<34> CLK_PCIE_LAN#	CLK_PCIE_LAN#	E31 GPP_CLK3N
OPT MINI2	<33> CLK_PCIE_MINI2	CLK_PCIE_MINI2	M23 GPP_CLK4P
	<33> CLK_PCIE_MINI2#	CLK_PCIE_MINI2#	M24 GPP_CLK4N

M27	GPP_CLK5P
M26	GPP_CLK5N
N25	GPP_CLK6P
N26	GPP_CLK6N
R23	GPP_CLK7P
R24	GPP_CLK7N
N27	GPP_CLK8P
R27	GPP_CLK8N

<32> CLK_SD_48M → CLK_SD_48M J26 14M_25M_48M_OSC

LPC

LPCCLK0 B25	LPC_CLK0	R852 22_0402_5% → LPC_CLK0_EC <29,35>
LPCCLK1 D25	LPC_CLK1	→ LPC_CLK1 <29>
LAD0 D27	LPC_AD0	→ LPC_AD0 <35>
LAD1 C28	LPC_AD1	→ LPC_AD1 <35>
LAD2 A26	LPC_AD2	→ LPC_AD2 <35>
LAD3 A29	LPC_AD3	→ LPC_AD3 <35>
LFRAME# A31		→ LPC_FRAME# <35>
LDRQ0# B27		
LDRQ1#/CLK_REQ6#/GPIO49 AE27		
SERIRQ/GPIO48 AF19		→ SERIRQ <35>

APU

DMA_ACTIVE# G25		→ ALLOW_STOP <8>
PROCHOT# E28		R853 @ 0_0402_5% → EC_THERM# <8,35,48>
APU_PG E26	APU_PWRGD	→ APU_PWRGD <8>
LDT_STP# G26		
APU_RST# E26		→ APU_RST# <8>

APU_PG/APU_RST#/LDT_STP# : OD pin
DMA_ACTIVE# : IN/OD, 0.8V threshold
PROCHOT# : IN, 0.8V threshold
LDT_STP : No use, NC

DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

SS PLUS

S5_CORE_EN H7		
RTCCLK F1		R855 22_0402_5% → RTC_CLK <29,35>
INTRUDER_ALERT# F3		
VDDBT_RTC_G E6		

M3@ U25
FCH M3 A13
Part Number = SA000043IB0

C1200 27P_0402_50V8J
X1 25MHZ_20PF_7A25000012
C1201 27P_0402_50V8J
R856 0_0402_5% 25M_X1 C31 25M_X1
R858 1M_0402_5% 25M_X2 C33 25M_X2

32K_X1 G2 32K_X1
32K_X2 G4 32K_X2

C1205 22P_0402_50V8J
Y4 32.768KHZ_12.5PF_Q13MC14610002
R861 20M_0402_5%
C1206 22P_0402_50V8J
Close to HUDSON-M2

RTCVCC_R R859 510_0402_5% W=20mils
C1202 0.1U_0402_16V4Z
C1203 1U_0402_6.3V4Z
for Clear CMOS
R860 @ 0_0603_5%
+RTCVCC C1204 0.1U_0402_16V4Z
D23 DAN202UT106_SC70-3 → +CHGRTC
+RTCBATT R857 1K_0402_5%

HUDSON-M2_FCBGA656 M2@

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PCIE_RST2 : Reset PCIE device on Hudson2

U25D

HUDSON-2

T35

<35> EC_LID_OUT#
<35> SLP_S3#
<35> SLP_S5#
<35> PBTN_OUT#
<35> FCH_PWRGD
TEST0
TEST1
TEST2
<35> EC_GA20
<35> EC_KBRST#
<35> EC_SCI#
<35> EC_SMI#
+3VALW R18 10K_0402_5% SYS_RESET#
<33,34> FCH_PCIE_WAKE#
THERMTRIP:
Need level shift from +3VALW to +1.5V
<8> H_THERMTRIP#
+3VS R862 10K_0402_5% H_THERMTRIP#
<35> EC_RSMRST#
<33> MINI2_CLKREQ#
<34> LAN_CLKREQ#
R81 0_0402_5%
@D17 CH751H-40PT_SOD323-2
MINI2_CLKREQ#
LAN_CLKREQ#_1
<37> FCH_SPKR
<11,12,33> FCH_SCLK0
<11,12,33> FCH_SDATA0
FCH_SCLK1
FCH_SDATA1
<33> MINI1_CLKREQ#
SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain
VGA_PD: Support MLDAC power save if connect
0: MLDAC power on
1: MLDAC power off
<29> VGA_PD
Check with SW for CARD_DET
<31> ODD_PLUG#
<31> ODD_DA#_1
T34
<34> USB_OC1# R82 0_0402_5%
<34> USB_OC0#
<37> HDA_BITCLK_AUDIO R866 33_0402_5%
<37> HDA_SDOUT_AUDIO R867 33_0402_5%
<37> HDA_SDIN0
<37> HDA_SYNC_AUDIO R868 33_0402_5%
<37> HDA_RST_AUDIO# R869 33_0402_5%
T27

PCIE_RST2#/PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226

USB MISC
USB 1.1
ACPI / WAKE UP EVENTS
USB 2.0
GPIO
USB OC
USB 3.0
HD AUDIO
EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC
USB_RCOMP R863 11.8K_0402_1%
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USBFS_P0 <34>
USBFS_N0 <34>
BT
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB30_P12 <34>
USB30_N12 <34>
30 Pin Sub board USB3.0 Conn
USB30_P11 <34>
USB30_N11 <34>
USB30_P10 <34>
USB30_N10 <34>
On board USB Conn
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB20_P8 <33>
USB20_N8 <33>
Mini1-WLAN
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB20_P6 <32>
USB20_N6 <32>
Card Reader RTS5138
USB_HSD5P
USB_HSD5N
USB20_P5 <23>
USB20_N5 <23>
Camera
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
T24
T29
USB_HSD0P
USB_HSD0N
USB20_P0 <33>
USB20_N0 <33>
Option Mini2
USBSS_CALRP R864 3K@ 1K_0402_1%
USBSS_CALRN R865 3K@ 1K_0402_1%
+FCH_VDD_11_SSUSB_S
USB_SS_TX3P
USB_SS_TX3N
USB30_TXP3 <23>
USB30_TXN3 <23>
USB_SS_RX3P
USB_SS_RX3N
USB30_RXP3 <23>
USB30_RXN3 <23>
HD Camera
USB_SS_TX2P
USB_SS_TX2N
USB30_TXP2 <34>
USB30_TXN2 <34>
USB_SS_RX2P
USB_SS_RX2N
USB30_RXP2 <34>
USB30_RXN2 <34>
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USB_SS_TX1N
USB30_TXP1 <34>
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USB_SS_RX1N
USB30_RXP1 <34>
USB30_RXN1 <34>
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USB_SS_TX0N
USB30_TXP0 <34>
USB30_TXN0 <34>
USB_SS_RX0P
USB_SS_RX0N
USB30_RXP0 <34>
USB30_RXN0 <34>
SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
R870 10K_0402_5%
R872 10K_0402_5%
R873 10K_0402_5%
R875 10K_0402_5%
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
EC_PWM2
T28
EC_PWM2 <29>
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)

Hudson-M2/M3
OHCI CTL
DEV 20, Fn 5
<Disable CTL>

Hudson-M2
EHCI CTL
DEV 22, Fn 2
Hudson-M3
xHCI CTL
DEV 16, Fn 1
<Support Wakeup>

Hudson-M3
xHCI CTL
DEV 16, Fn 0
<Support Wakeup>

Hudson-M2/M3
EHCI CTL
DEV 19, Fn 2

Hudson-M2/M3
EHCI CTL
DEV 18, Fn 2
<Disable CTL>

Hudson-M3
xHCI CTL
DEV 16, Fn 1

Hudson-M3
xHCI CTL
DEV 16, Fn 0

HUDSON-M2_FCBGA656 M2@

+3VALW
R871 10K_0402_5% H_THERMTRIP#
R874 2.2K_0402_5% FCH_SCLK1
R876 2.2K_0402_5% FCH_SDATA1
R877 @ 100K_0402_5% EC_LID_OUT#
R878 10K_0402_5% FCH_PCIE_WAKE#
R88 100K_0402_5% USB_OC1#

+3VS
R880 2.2K_0402_5% FCH_SCLK0
R881 2.2K_0402_5% FCH_SDATA0
R882 8.2K_0402_5% MINI1_CLKREQ#
R883 8.2K_0402_5% MINI2_CLKREQ#
R940 @ 8.2K_0402_5% LAN_CLKREQ#_1

+3VALW
R50 8.2K_0402_5%
R47 8.2K_0402_5%
R46 PX@ 2.2K_0402_5%
R43 VGA@ 2.2K_0402_5%
FCH_GPIO189
FCH_GPIO190
FCH_GPIO191
FCH_GPIO192
R49 8.2K_0402_5%
R48 @ 8.2K_0402_5%
R46 100K_0402_5%
R44 UMA@ 100K_0402_5%

Project SKU ID	HIGH	LOW
GPIO189	VGA *	UMA
GPIO190	PX *	NO PX
GPIO191	17" *	15"
GPIO192	Reserve	Reserve

R884 2.2K_0402_5% EC_RSMRST#
R885 @ 10K_0402_5% HDA_BITCLK
R886 @ 10K_0402_5% HDA_SDIN0
R888 @ 10K_0402_5% HDA_SDIN1

+3VALW *For FCH internal debug use*
R887 @ 2.2K_0402_5% TEST0
R889 @ 2.2K_0402_5% TEST1
R890 @ 2.2K_0402_5% TEST2

Security Classification	Compal Secret Data		
Issued Date	2010/12/30	Deciphered Date	2012/01/01

Compal Electronics, Inc.

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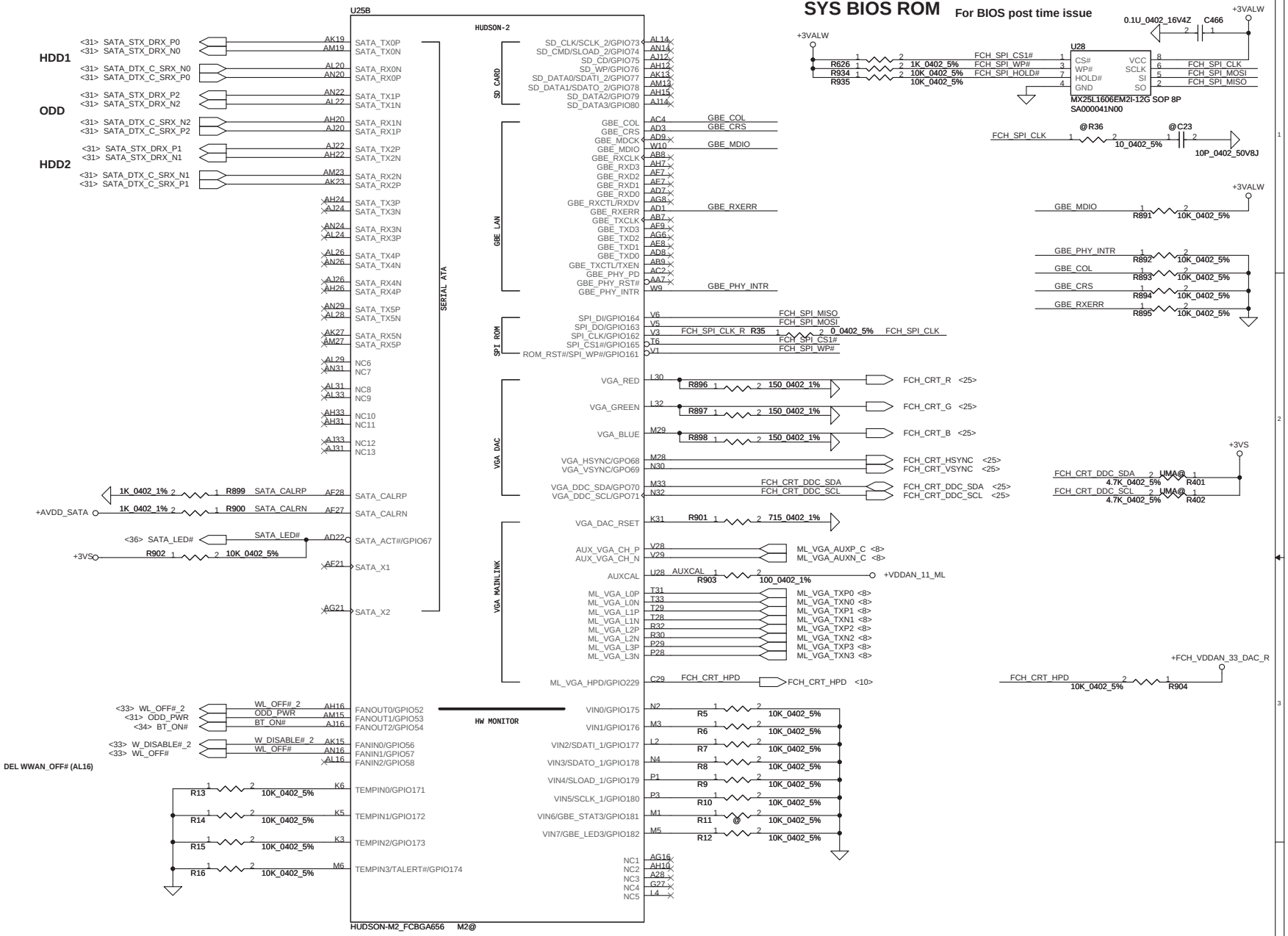

Security Classification	Compal Secret Data		
Issued Date	2010/12/30	Deciphered Date	2012/01/01

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Title: SCHEMATIC MB A6991

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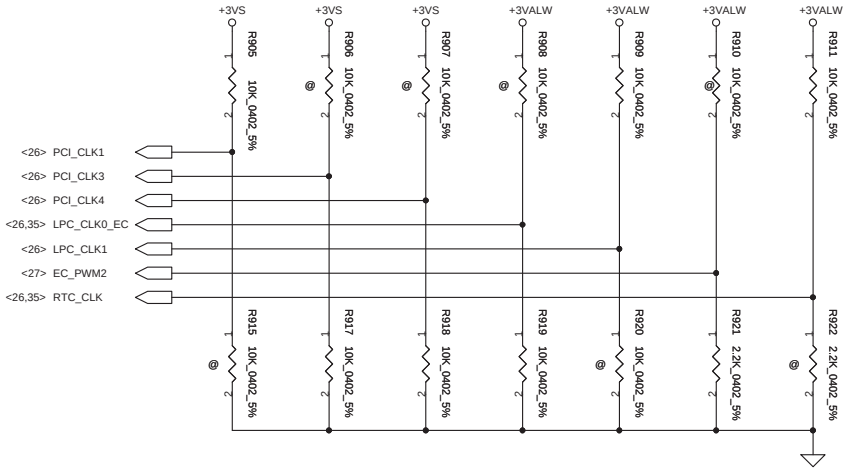
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

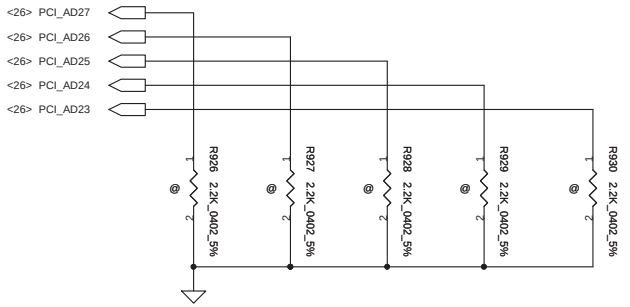


DEBUG STRAPS

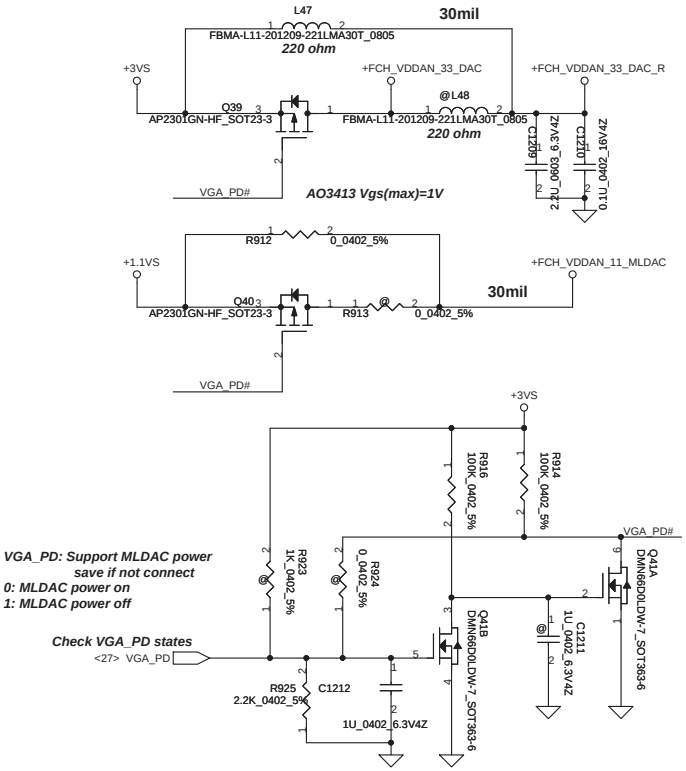
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26

	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



If support ML DAC power down when no VGA plug



Compal Electronics, Inc.

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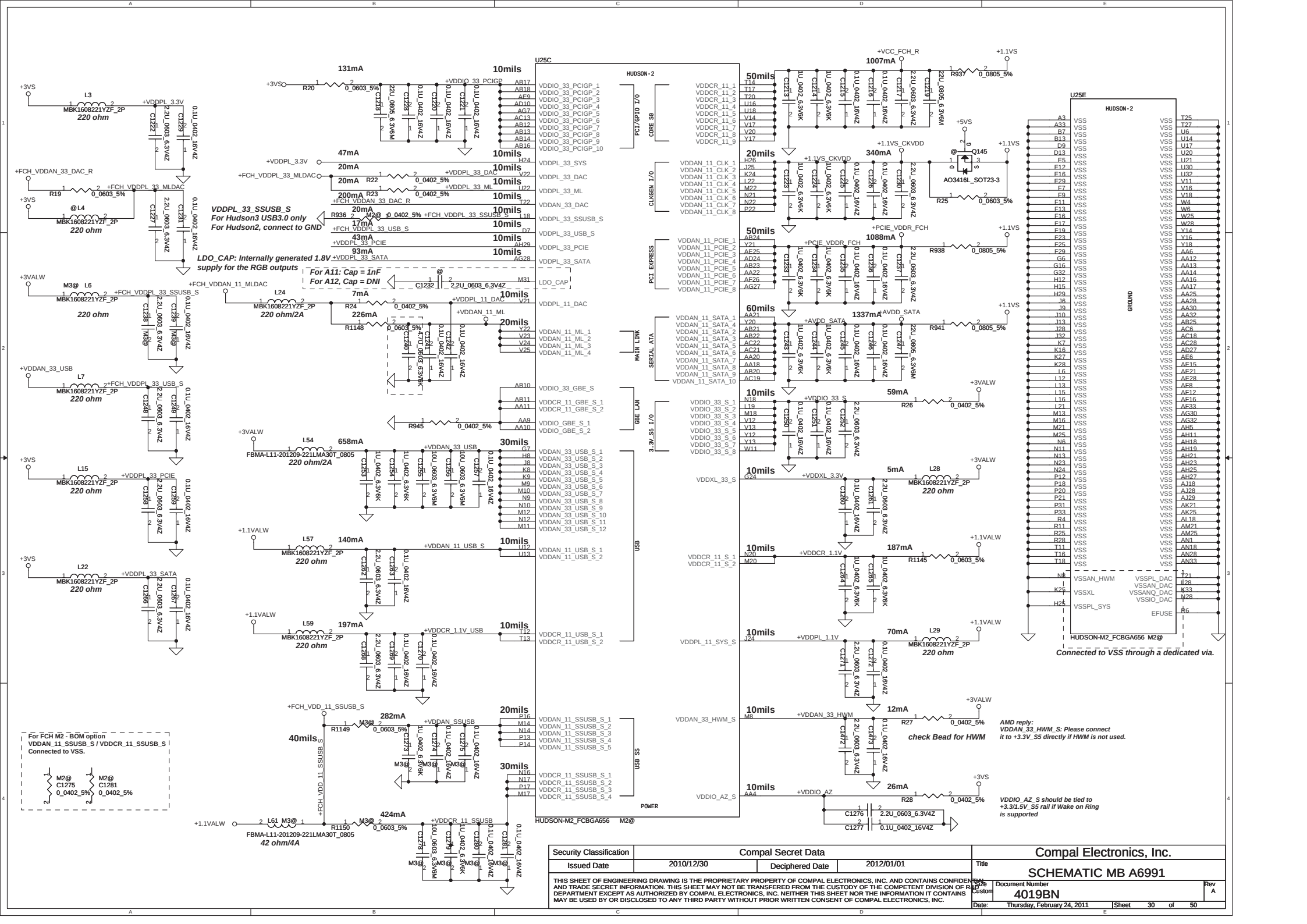

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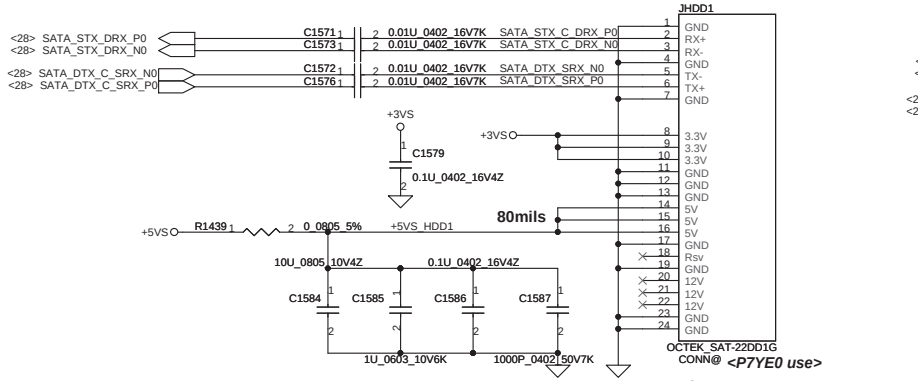
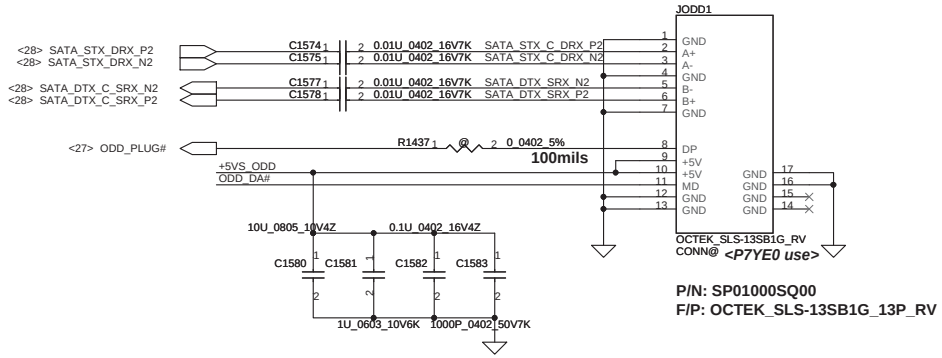
SATA HDD1 Conn.



P/N: DC010002Q00
F/P: OCTEK_SAT-22DD1G_22P

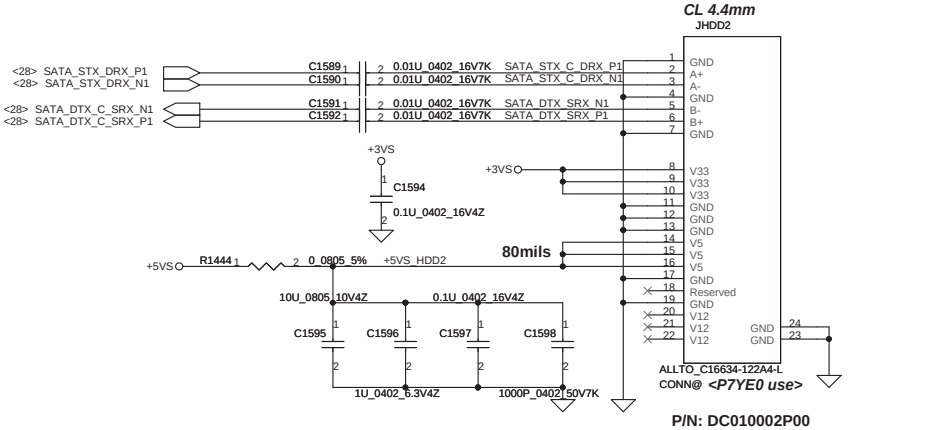
SATA ODD Conn.



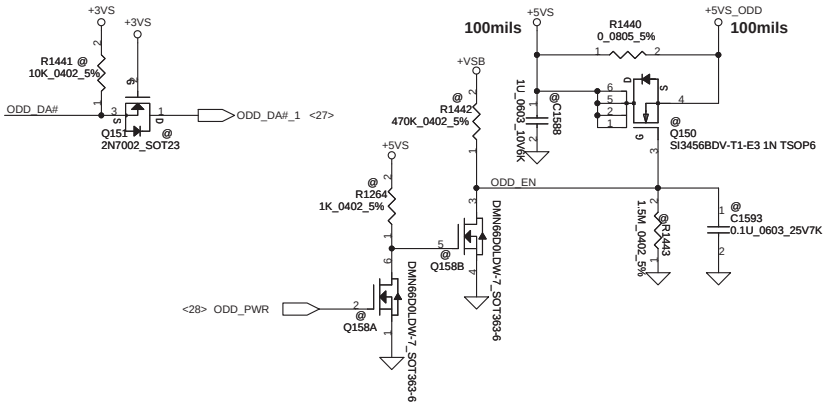
P/N: SP01000SQ00
F/P: OCTEK_SLS-13SB1G_13P_RV

SATA HDD2 Conn.

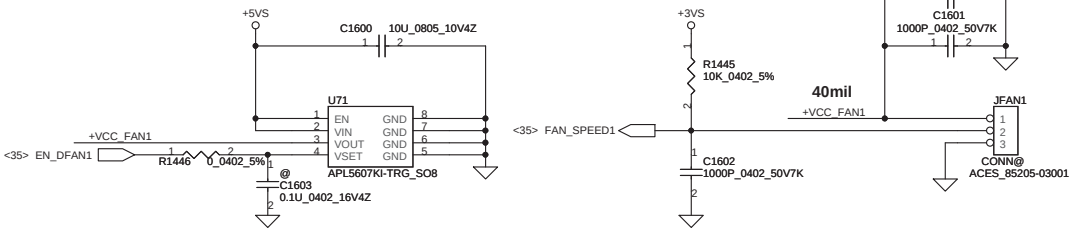
CL 4.4mm

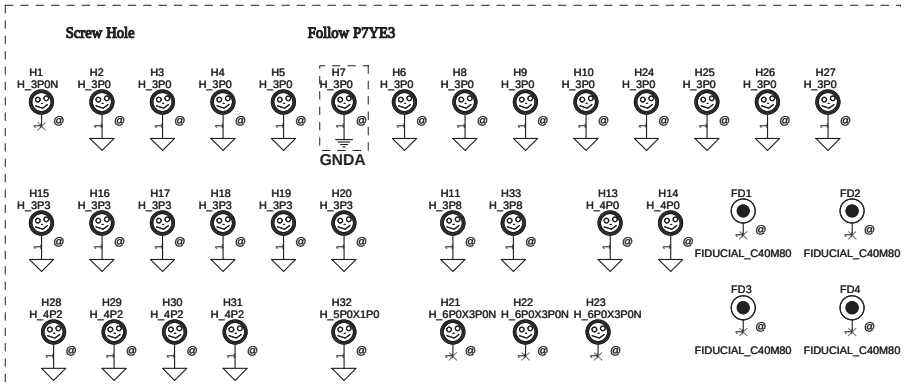


P/N: DC010002P00
F/P: ALLTO_C16634-122A4-L_22P



FAN





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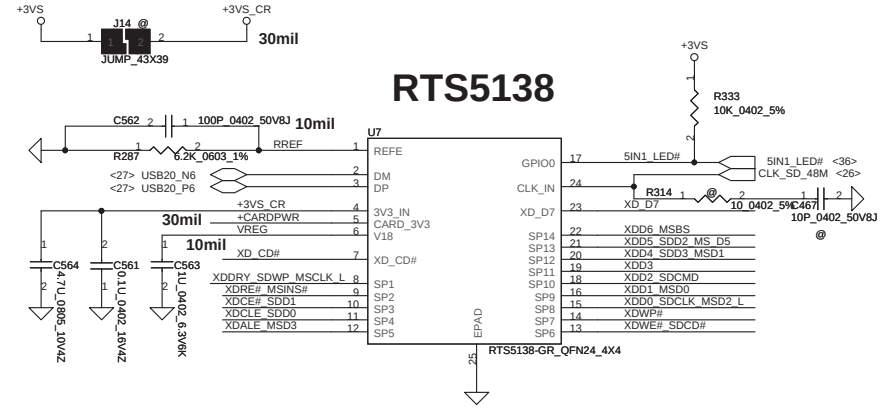
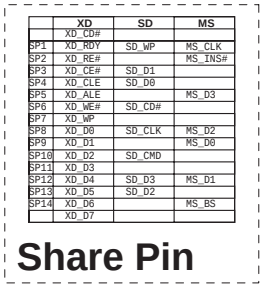
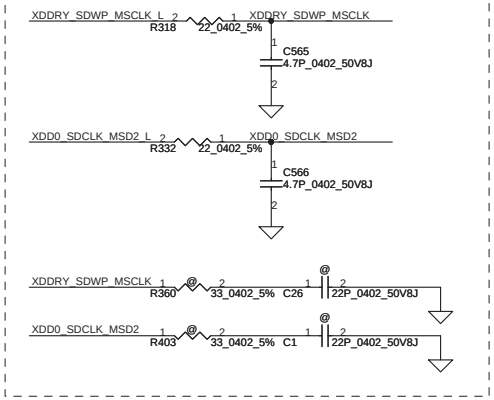
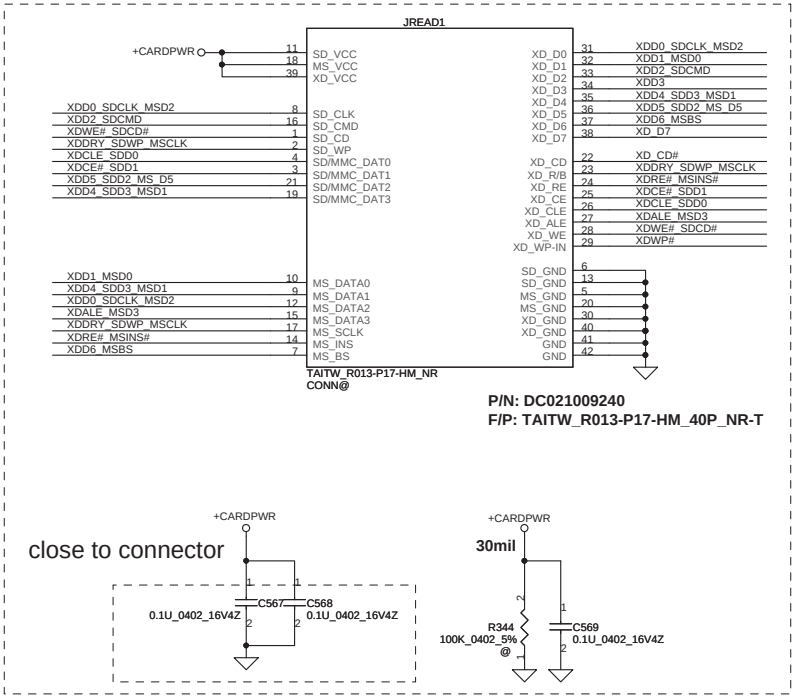




	XD	SD	MS
	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE		MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP		
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1		MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3		
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS
	XD_D7		

Share Pin





Security Classification	Compal Secret Data		
Issued Date	2010/12/30	Deciphered Date	2010/08/04

Compal Electronics, Inc.

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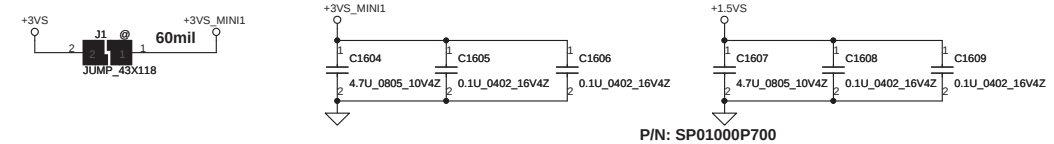
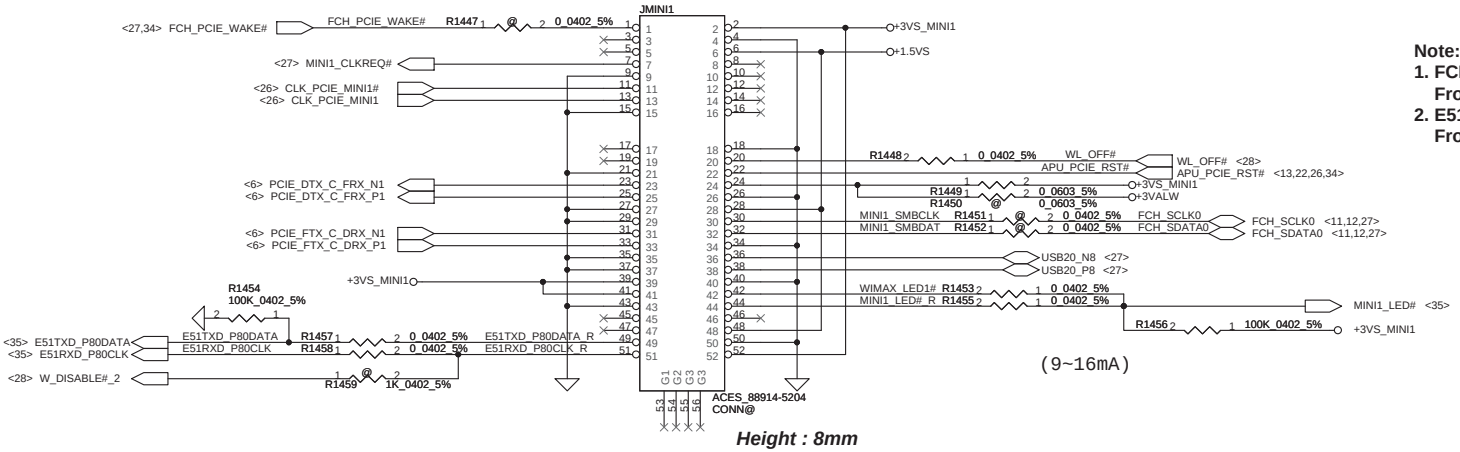
Mini-Express Card for WLAN

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



P/N: SP01000P700
F/P: ACES_88914-5204_52P

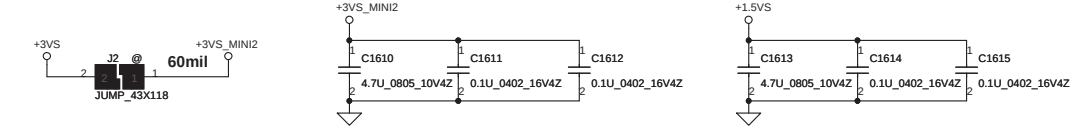


Note:
1. **FCH_SCLK0 and FCH_SDATA0 route as daisy chain. From FCH->JMINI2->DDR SOCKET->JMINI1**
2. **E51RXD_P80CLK and E51TXD_P80DATA route as daisy chain. From EC->JMINI1->JMINI1**

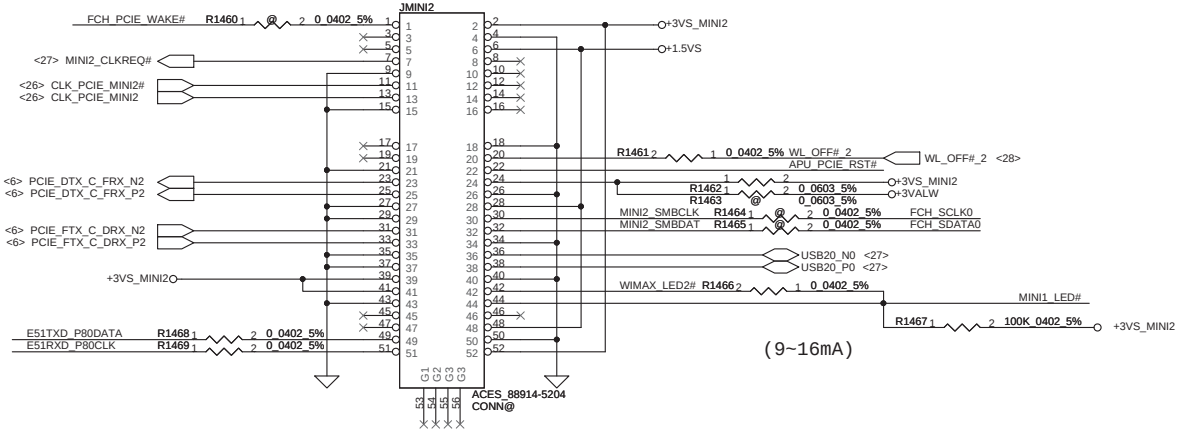
(9~16mA)

Height : 8mm

<P7WE0 use>



P/N: SP01000P700
F/P: ACES_88914-5204_52P



(9~16mA)

Height : 8mm

<P7WE0 use>

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Issued Date	2010/12/30	Deciphered Date	2012/01/01

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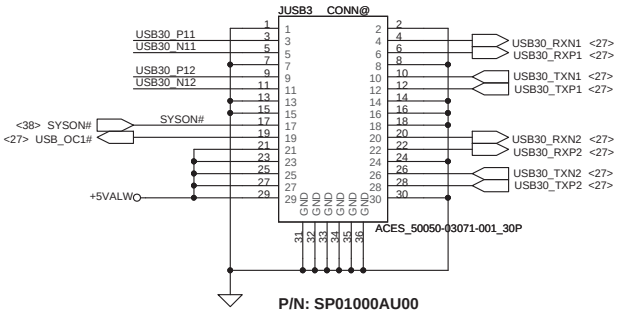
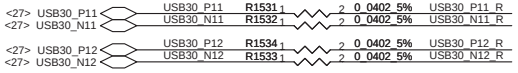
30 Pin USB/B Conn.

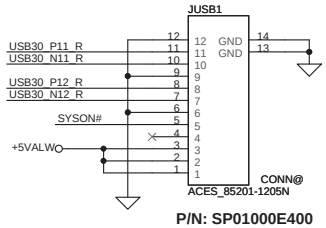


P/N: SP01000AU00
F/P: ACES_50050-03071-001_30P-T



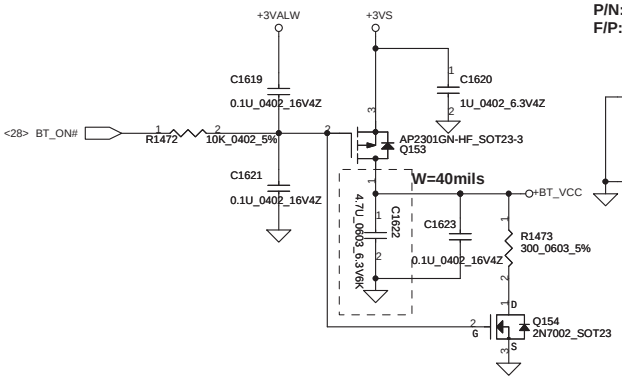
When use FPC, these four resistors not pop.

12 Pin USB/B Conn.

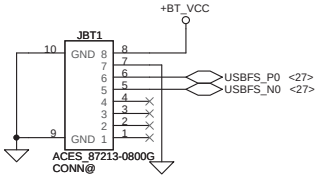


P/N: SP01000E400
F/P: ACES_85201-1205N_12P

Bluetooth Conn.

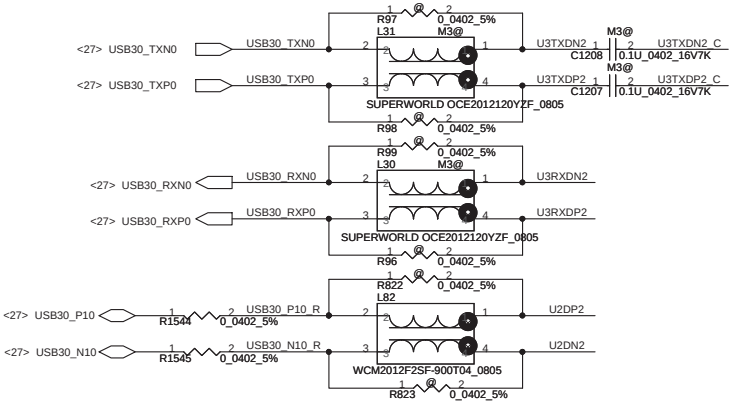


P/N: SP02000CZ00
F/P: ACES_87213-0800G_8P

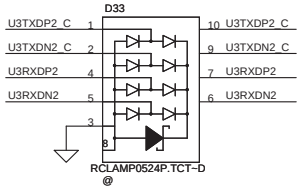


<NAL00 use>

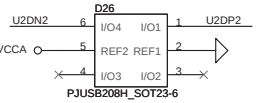
On Board USB3.0 Conn.

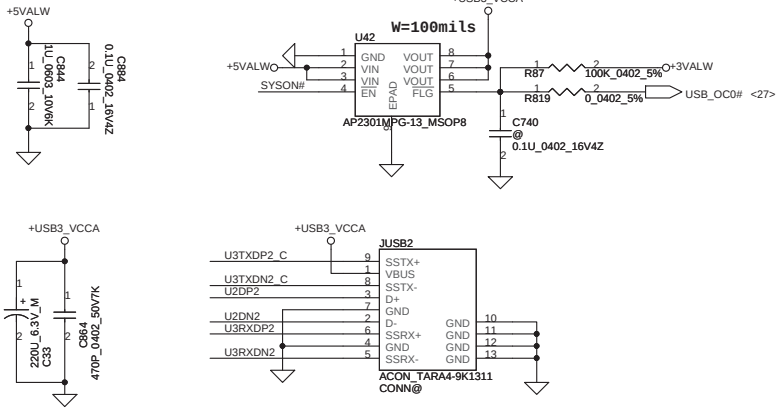


For USB3.0 ESD diode



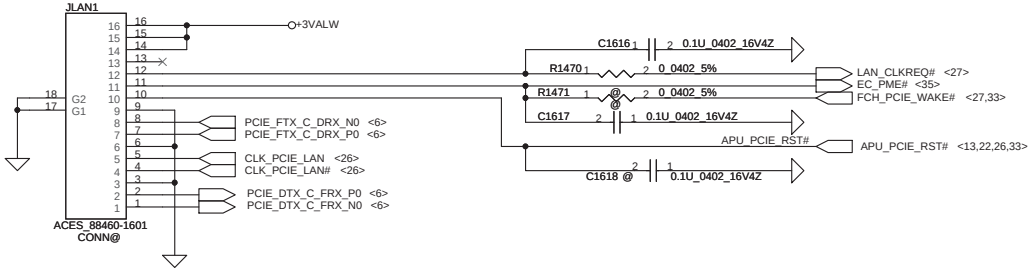
For USB2.0 ESD diode





LAN/B Conn.

P/N: DC020911300
F/P: ACES_88460-1601_16P-T



Security Classification	Compal Secret Data		
Issued Date	2010/12/30	Deciphered Date	2012/01/01

Compal Electronics, Inc.

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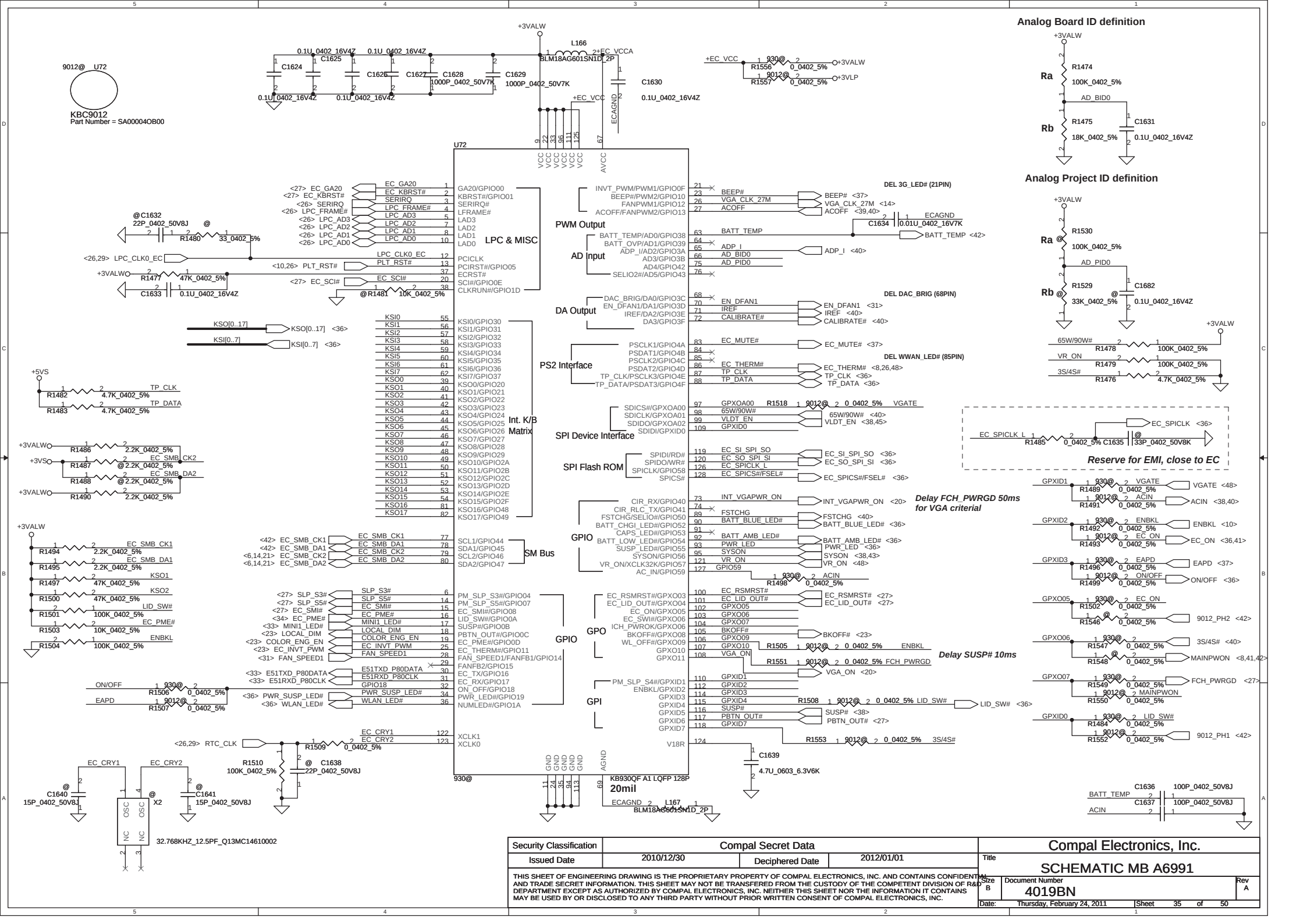
KBC9012
Part Number = SA00004OB00
U72
930@
KB930QF A1 LQFP 128P
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
Int. K/B Matrix
SM Bus
GPIO
GPO
GPI
Analog Board ID definition
Analog Project ID definition
Reserve for EMI, close to EC
Delay FCH_PWRGD 50ms for VGA criterial
Delay SUSP# 10ms
DEL 3G_LED# (21PIN)
DEL DAC_BRIG (68PIN)
DEL WWAN_LED# (85PIN)
32.768KHZ_12.5PF_Q13MC14610002
Security Classification
Compal Secret Data
Issued Date
2010/12/30
Deciphered Date
2012/01/01
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Rev A
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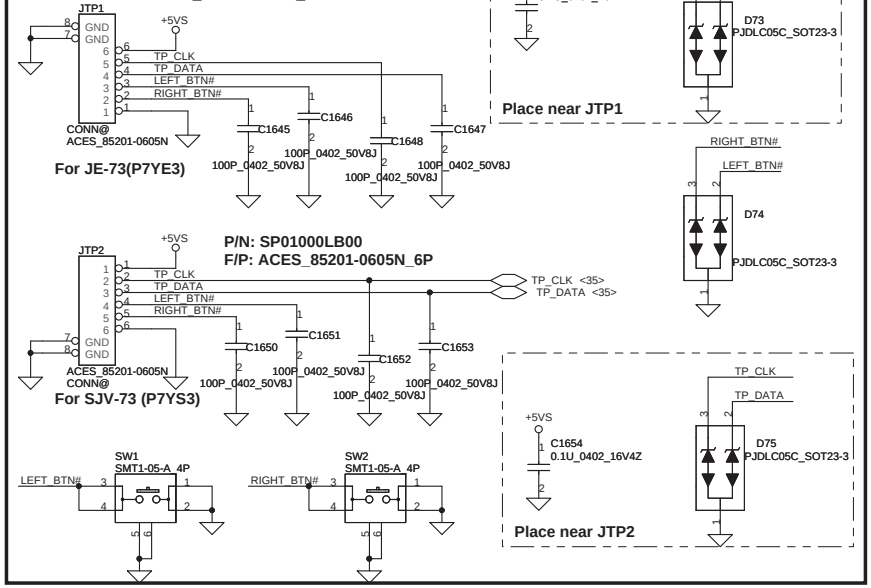
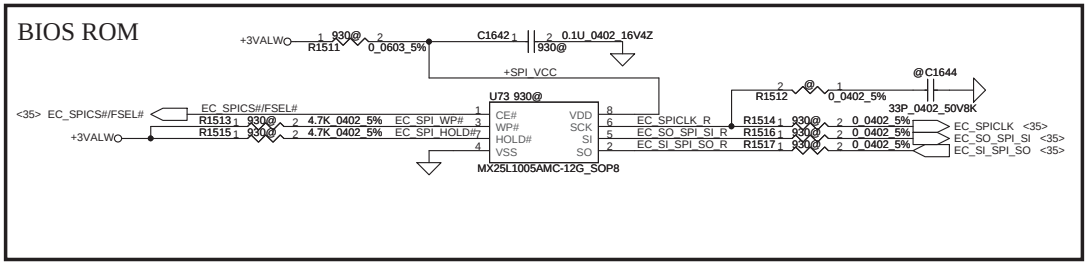
TP Conn.

P/N: SP01000LB00
F/P: ACES_85201-0605N_6P

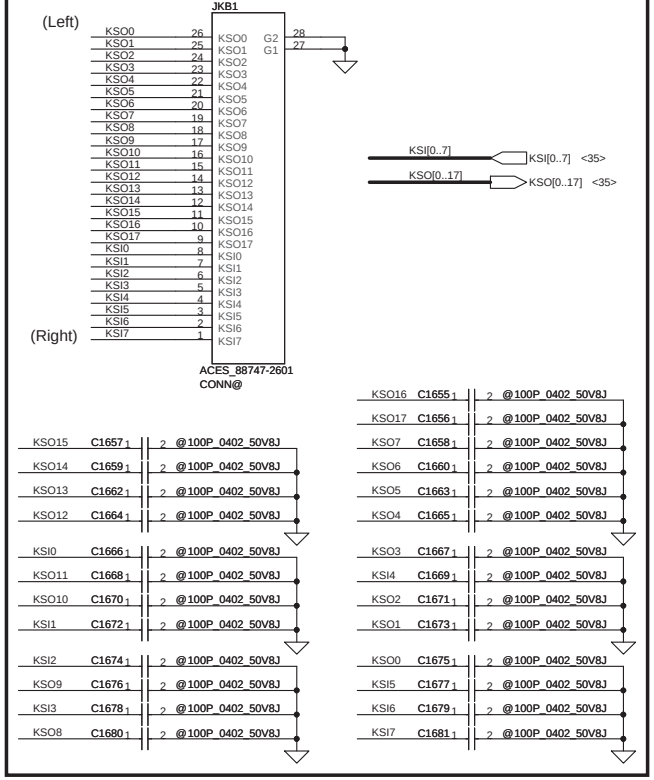


BIOS ROM



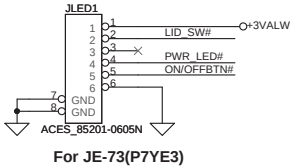
KB Conn.

P/N: SP01000PC00
F/P: ACES_88747-2601_26P



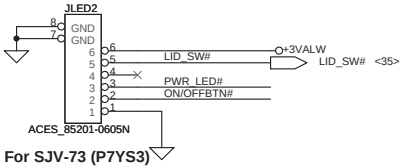
LS-6913P

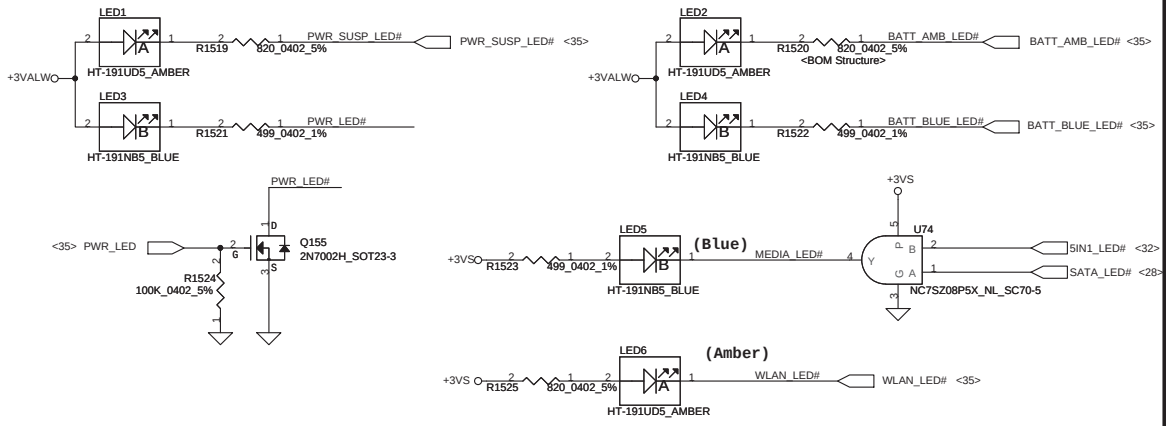
P/N: SP01000LB00
F/P: ACES_85201-0605N_6P



LS-6913P

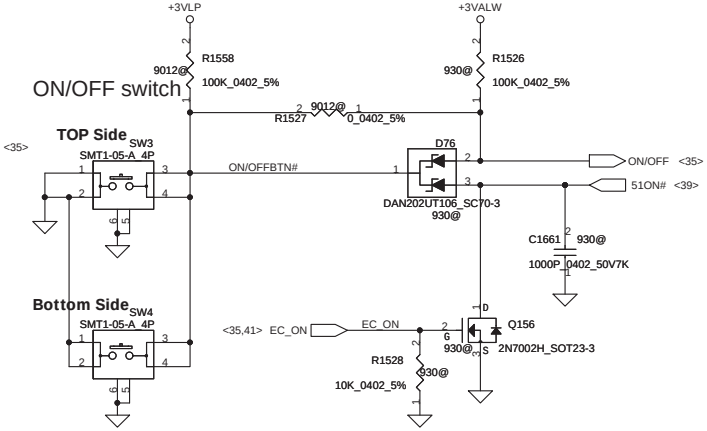
P/N: SP01000LB00
F/P: ACES_85201-0605N_6P





LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
P7YE/S3	Blue	Amber	Blue	Amber	Blue	Amber		

Power Button



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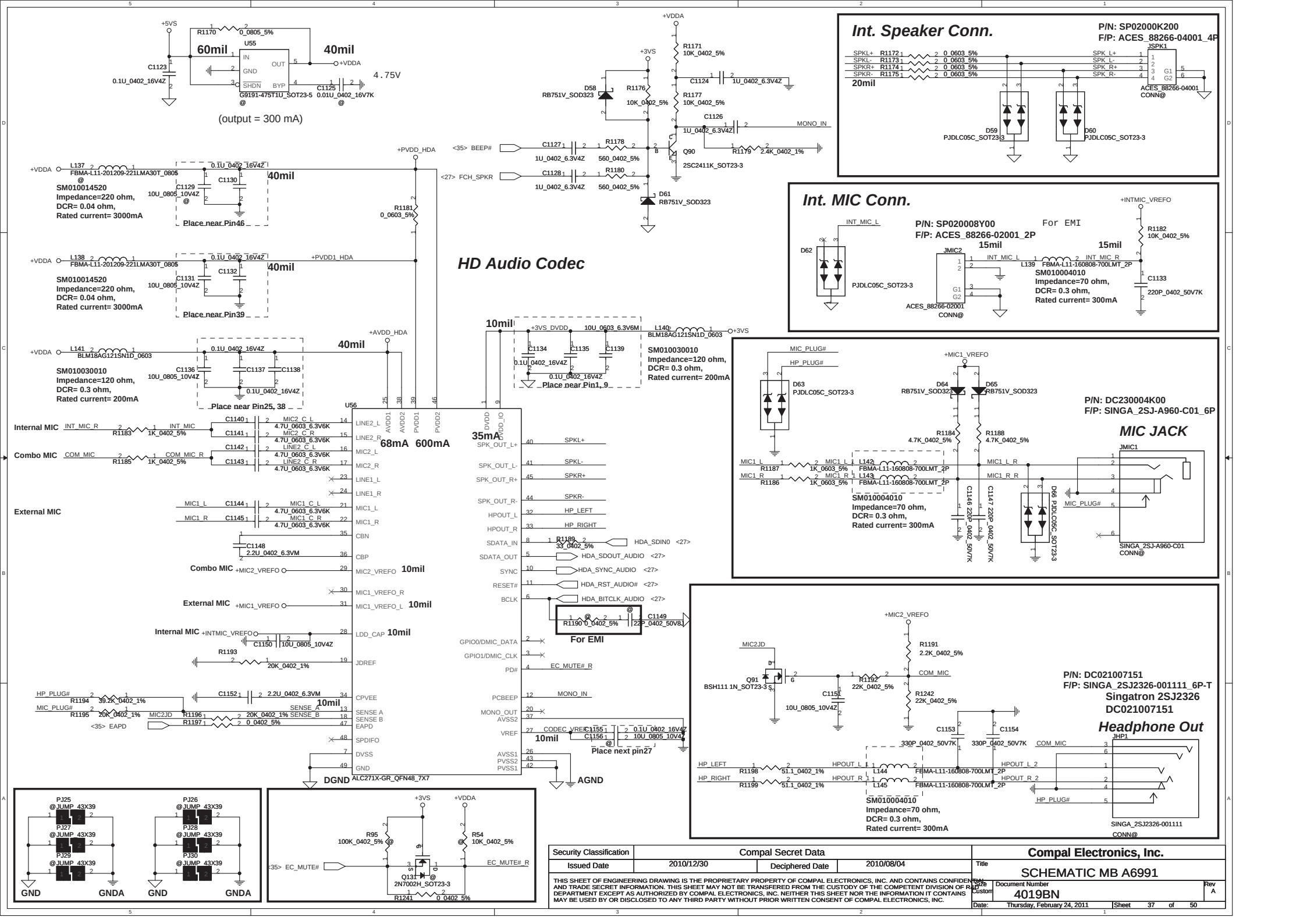
HD Audio Codec
Int. Speaker Conn.
P/N: SP02000K200
F/P: ACES_88266-04001_4P
Int. MIC Conn.
P/N: SP020008Y00
F/P: ACES_88266-02001_2P
For EMI
MIC JACK
P/N: DC230004K00
F/P: SINGA_2SJ-A960-C01_6P
Headphone Out
P/N: DC021007151
F/P: SINGA_2SJ2326-001111_6P-T
Singatron 2SJ2326
DC021007151
U56
ALC271X-GR_QFN48_7X7
SM010014520
SM010030010
SM010004010
Internal MIC
Combo MIC
External MIC
DGND
AGND
GND
GNDA
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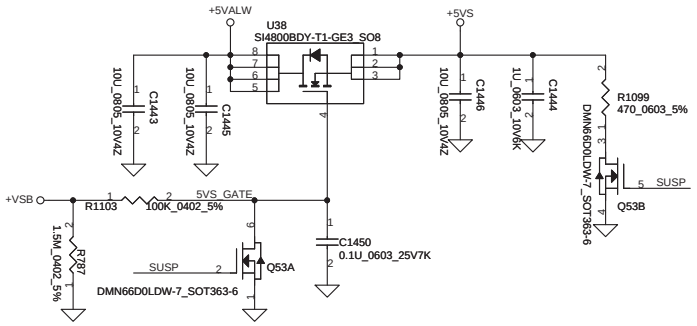
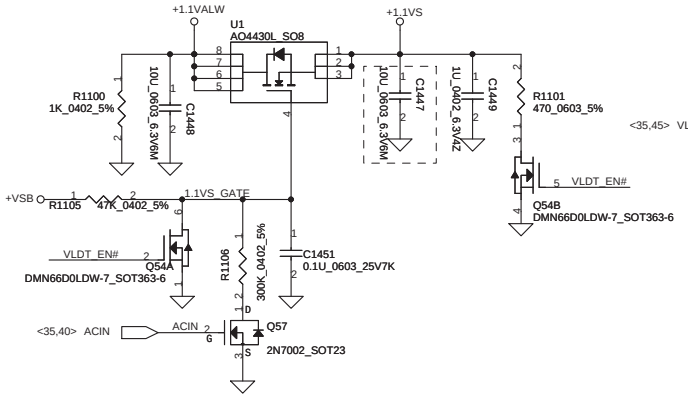
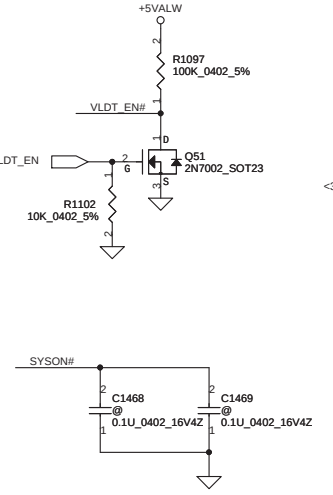
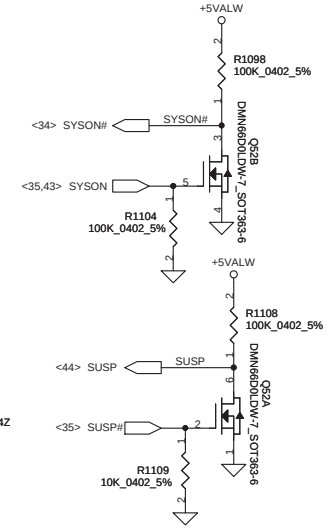
+5VALW TO +5VS



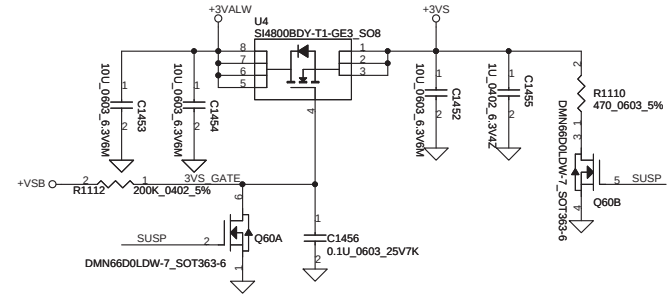
+1.1VALW TO +1.1VS



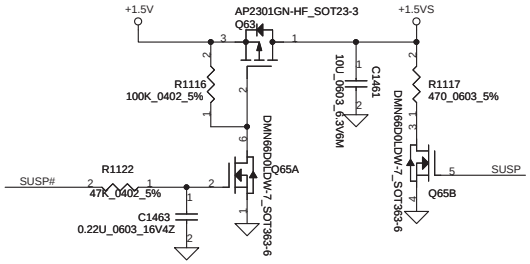




+3VALW TO +3VS

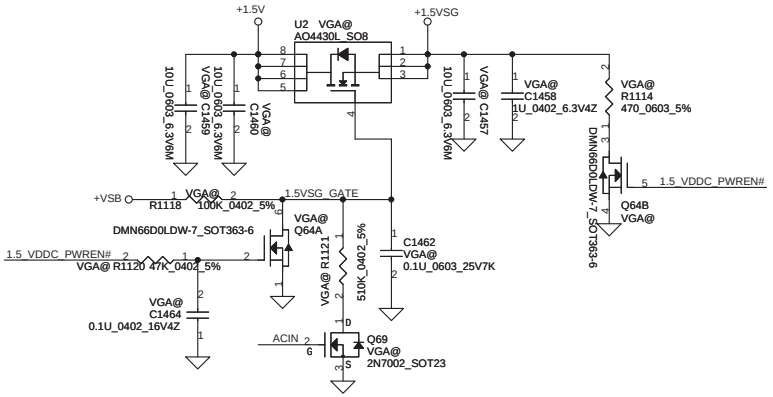


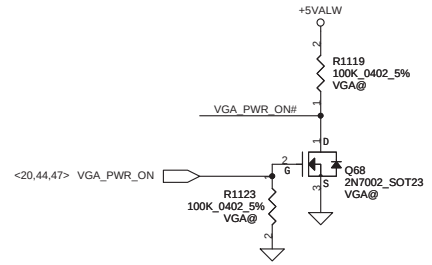
+1.5V TO +1.5VS



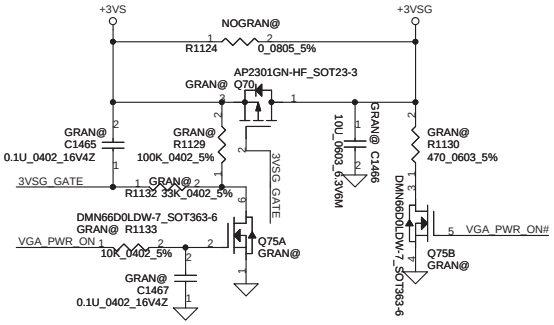
VGA Power

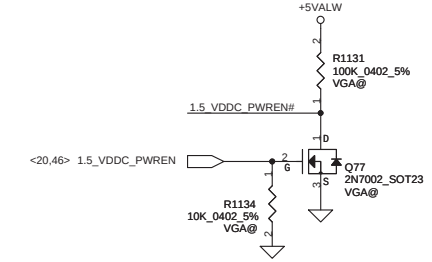
+1.5V to +1.5VSG

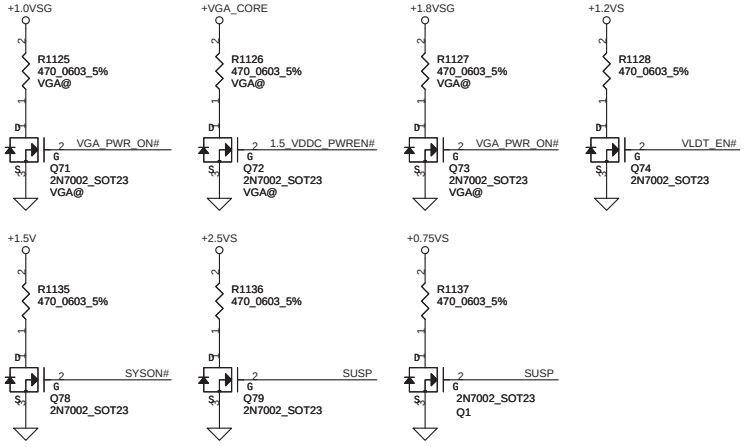




+3VS to +3VSG







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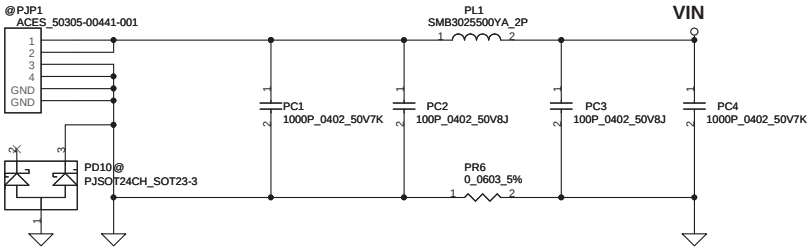

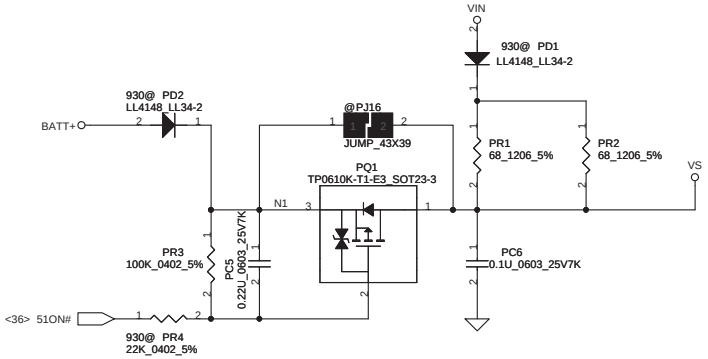

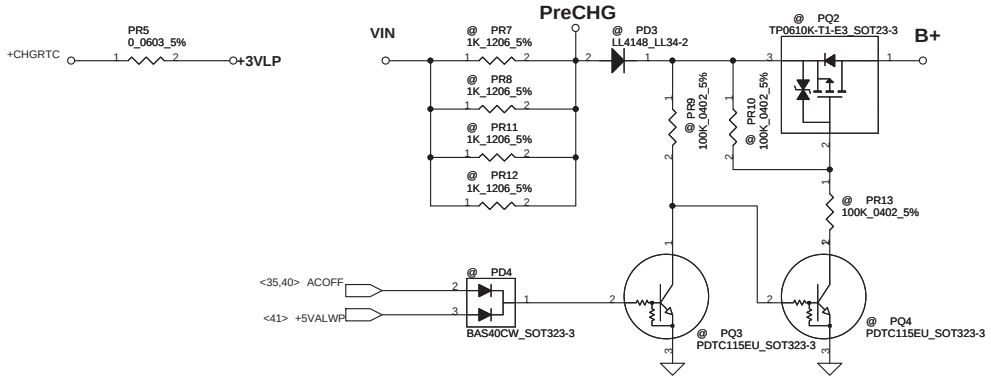

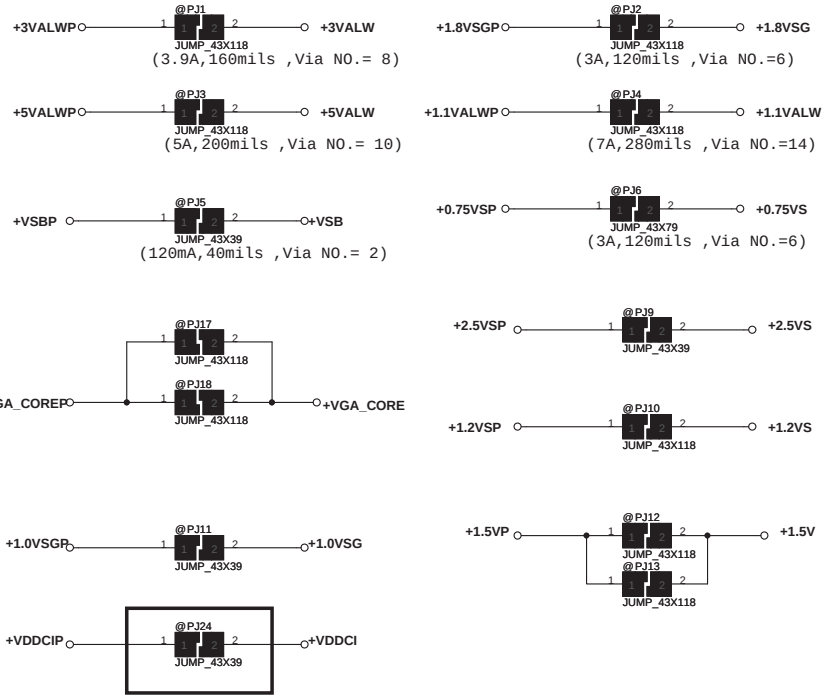

When use Granville, short PJ24

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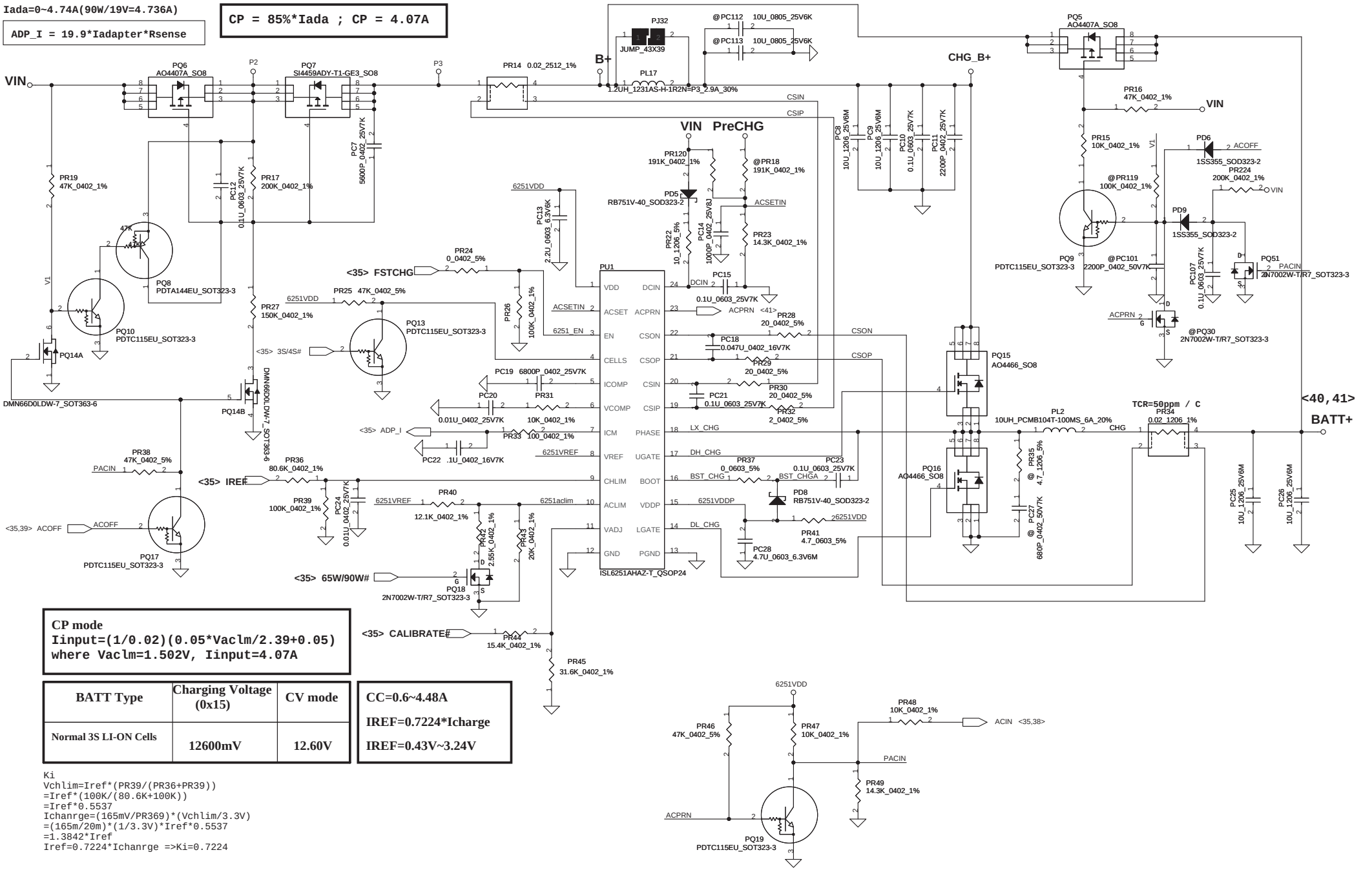
Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR39/(PR36+PR39))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR44=15.4K R2=PR45=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

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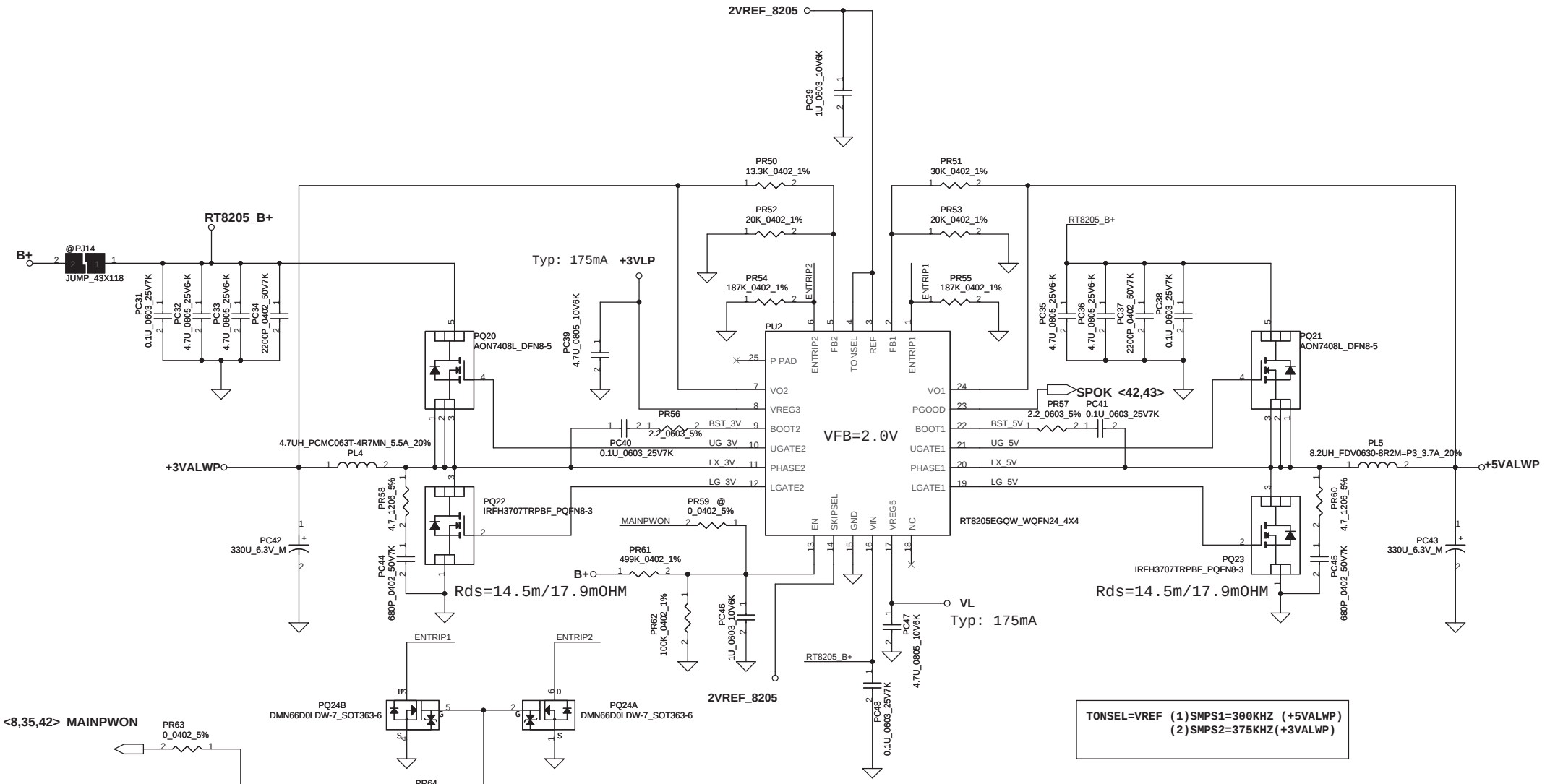

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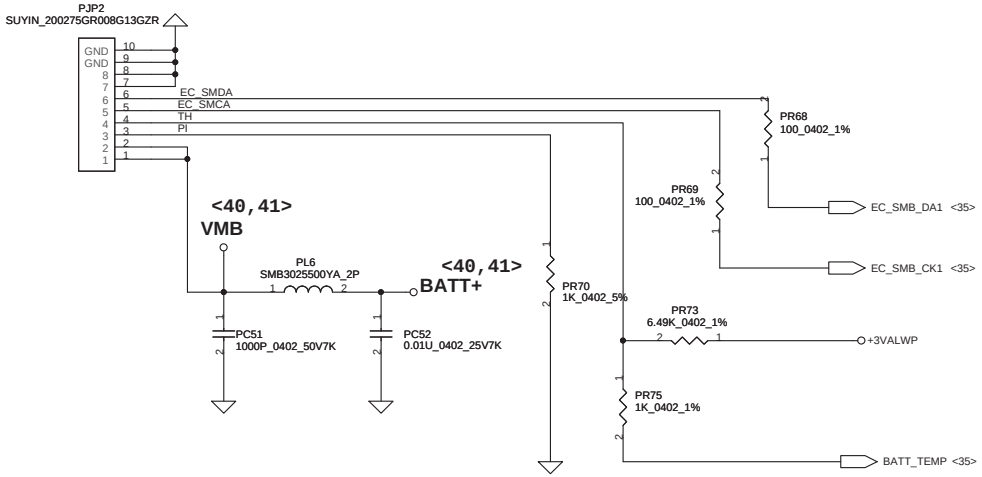
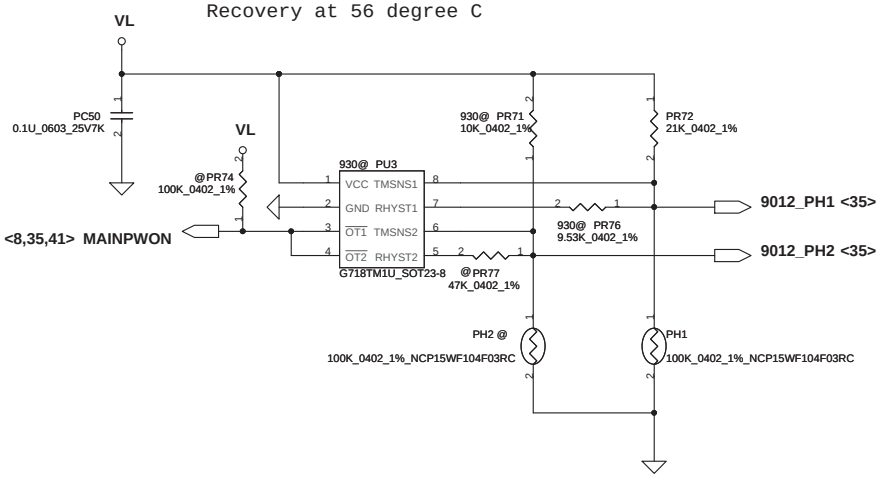
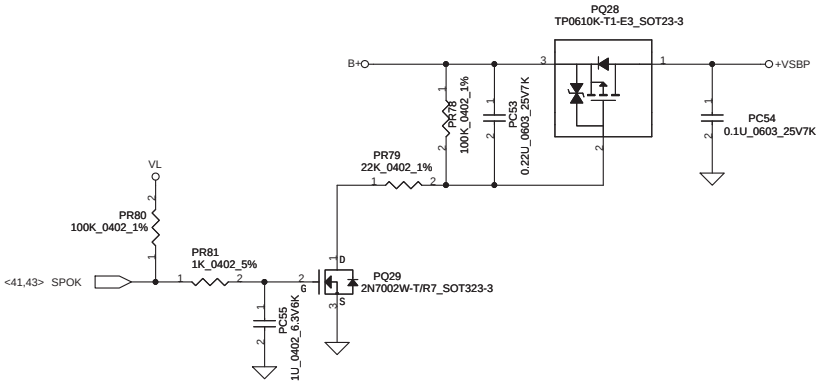


PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





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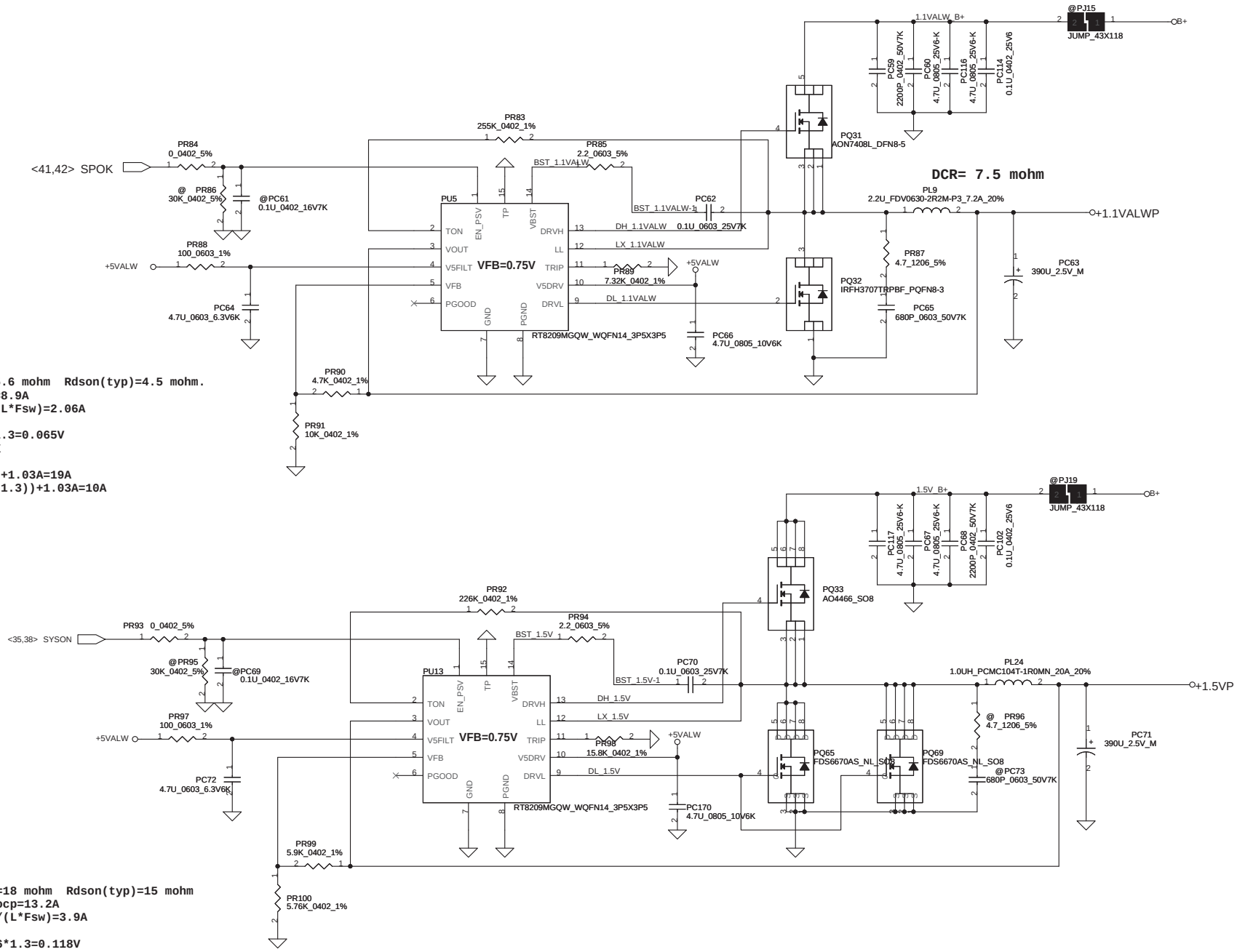

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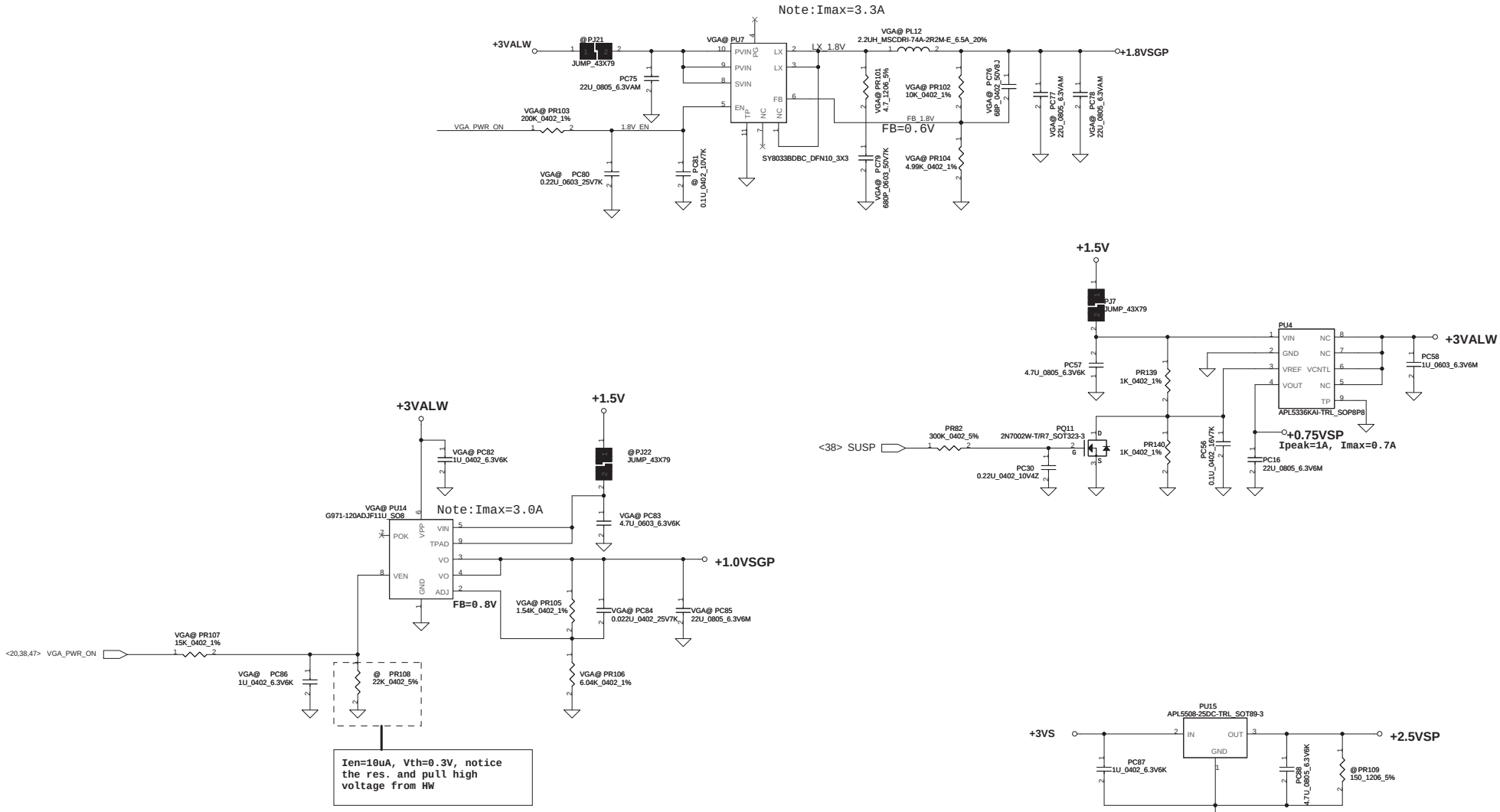

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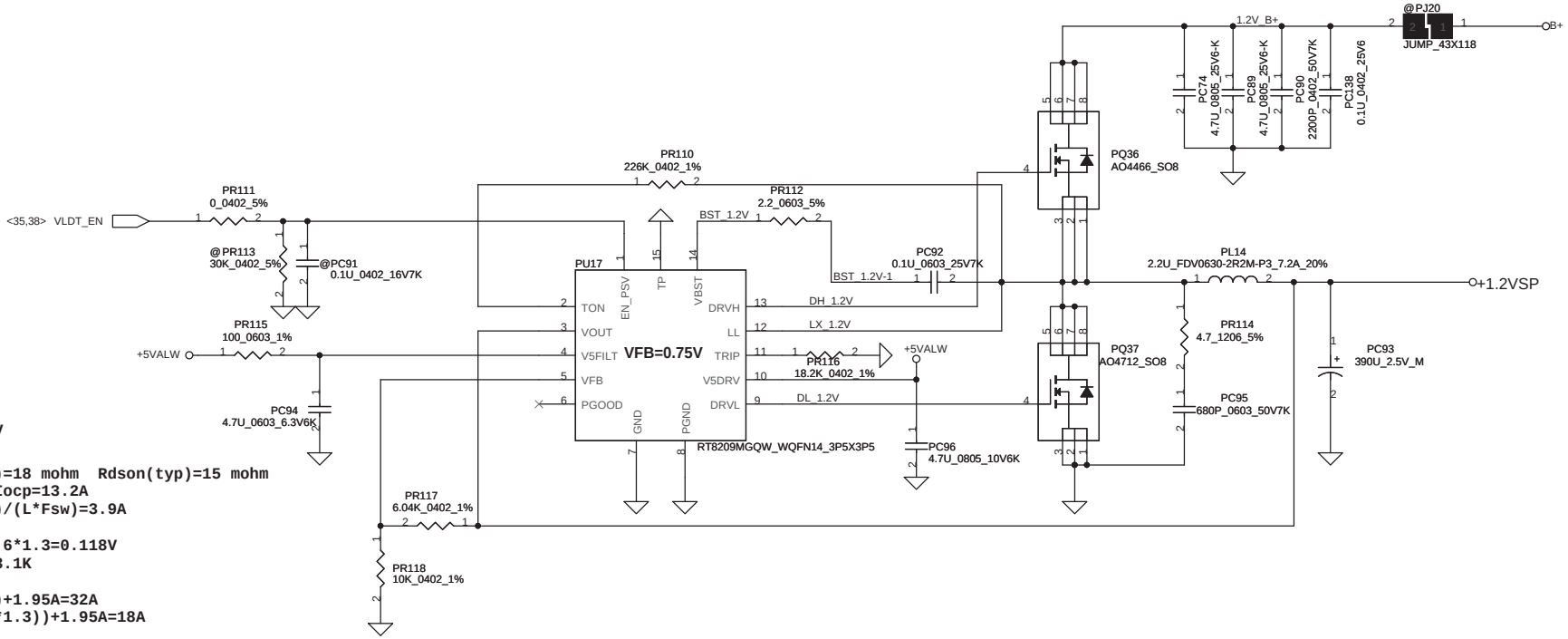

<Vo=1.5V> VFB=0.75V
Vo=0.75*(1+5.9K/5.76K)=1.5V
Fsw=335KHz

Cout ESR=17 mohm Rdson(max)=18 mohm Rdson(typ)=15 mohm
Ipeak=27.7A, Imax=19.39A, Iocp=13.2A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=3.9A
=>1/2Delta I=1.95A
Vtripmax=Iocp*Rdson=16.2*5.6*1.3=0.118V
Rcs=Vtrip/9uA=0.118V/9uA=13.1K
choose Rcs=13K
Iocpmax=((13K*11uA)/0.0045)+1.95A=32A
Iocpmin=((13K*9uA)/(0.0056*1.3))+1.95A=18A
Iocp=9.94A~13.2A

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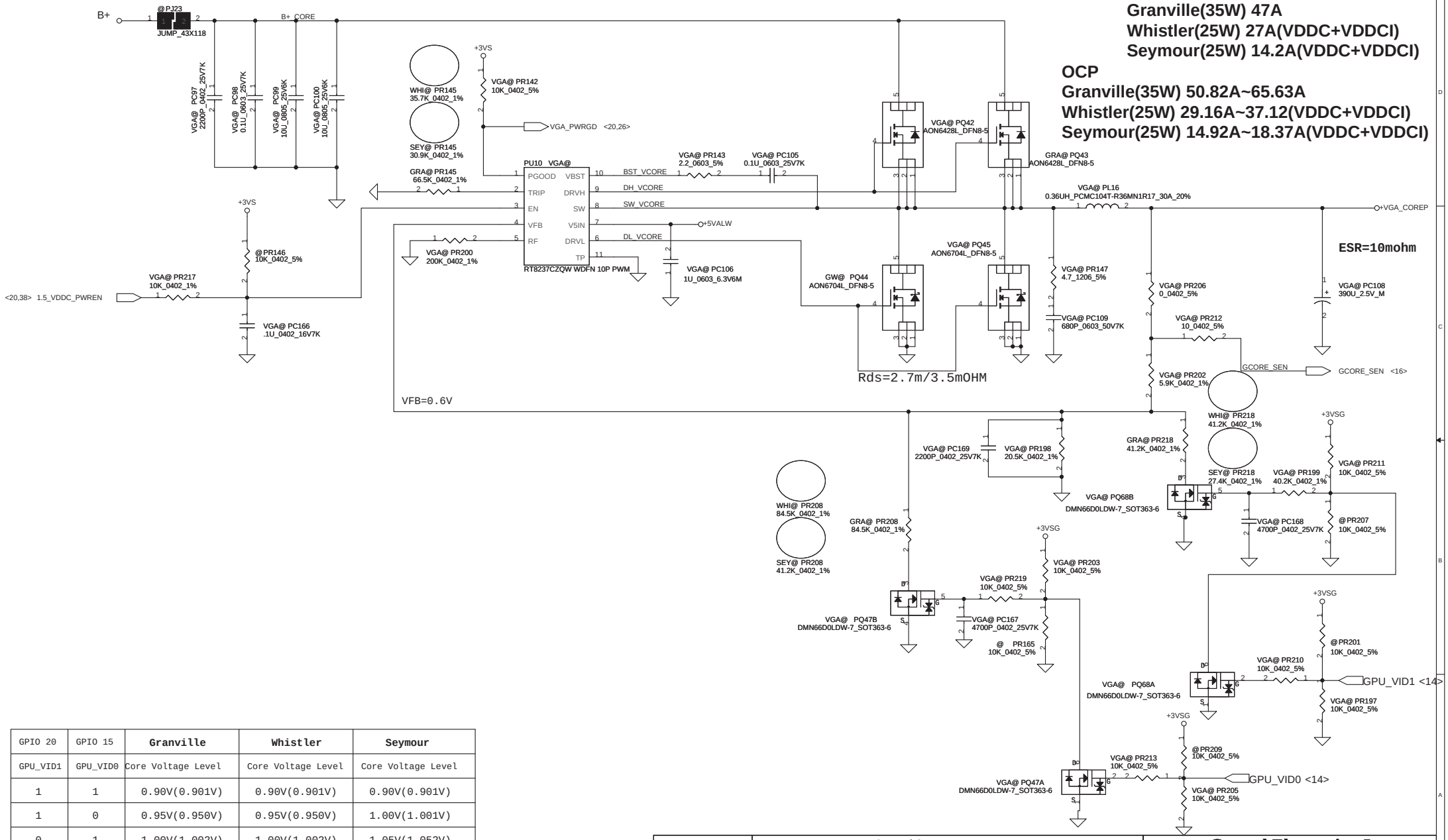
Ipeak
Granville(35W) 47A
Whistler(25W) 27A(VDDC+VDDCI)
Seymour(25W) 14.2A(VDDC+VDDCI)

OCP
Granville(35W) 50.82A~65.63A
Whistler(25W) 29.16A~37.12(VDDC+VDDCI)
Seymour(25W) 14.92A~18.37A(VDDC+VDDCI)



GPIO 20	GPIO 15	Granville	Whistler	Seymour
GPU_VID1	GPU_VID0	Core Voltage Level	Core Voltage Level	Core Voltage Level
1	1	0.90V(0.901V)	0.90V(0.901V)	0.90V(0.901V)
1	0	0.95V(0.950V)	0.95V(0.950V)	1.00V(1.001V)
0	1	1.00V(1.002V)	1.00V(1.002V)	1.05V(1.052V)
0	0	1.05V(1.051V) **Default**	1.05V(1.051V) **Default**	1.15V(1.152V) **Default**

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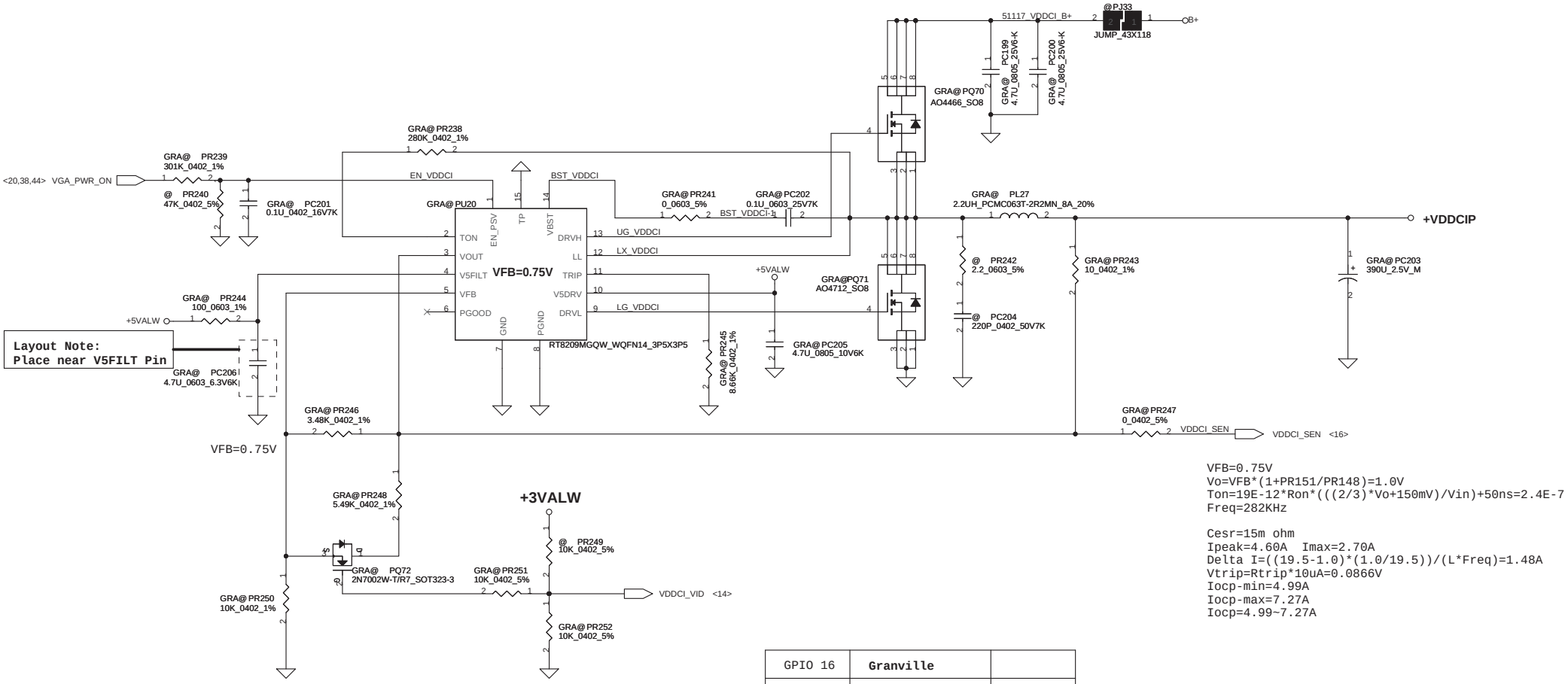

VFB=0.75V
Vo=VFB*(1+PR151/PR148)=1.0V
Ton=19E-12*Ron*(((2/3)*Vo+150mV)/Vin)+50ns=2.4E-7
Freq=282KHz

Cesr=15m ohm
Ipeak=4.60A Imax=2.70A
Delta I=((19.5-1.0)*(1.0/19.5))/(L*Freq)=1.48A
Vtrip=Rtrip*10uA=0.0866V
Iocp-min=4.99A
Iocp-max=7.27A
Iocp=4.99~7.27A

GPIO 16	**Granville**	
VDDCI_VID	VDDCI Voltage Level	Comment
0	1.00 V	Default
1	0.90 V	

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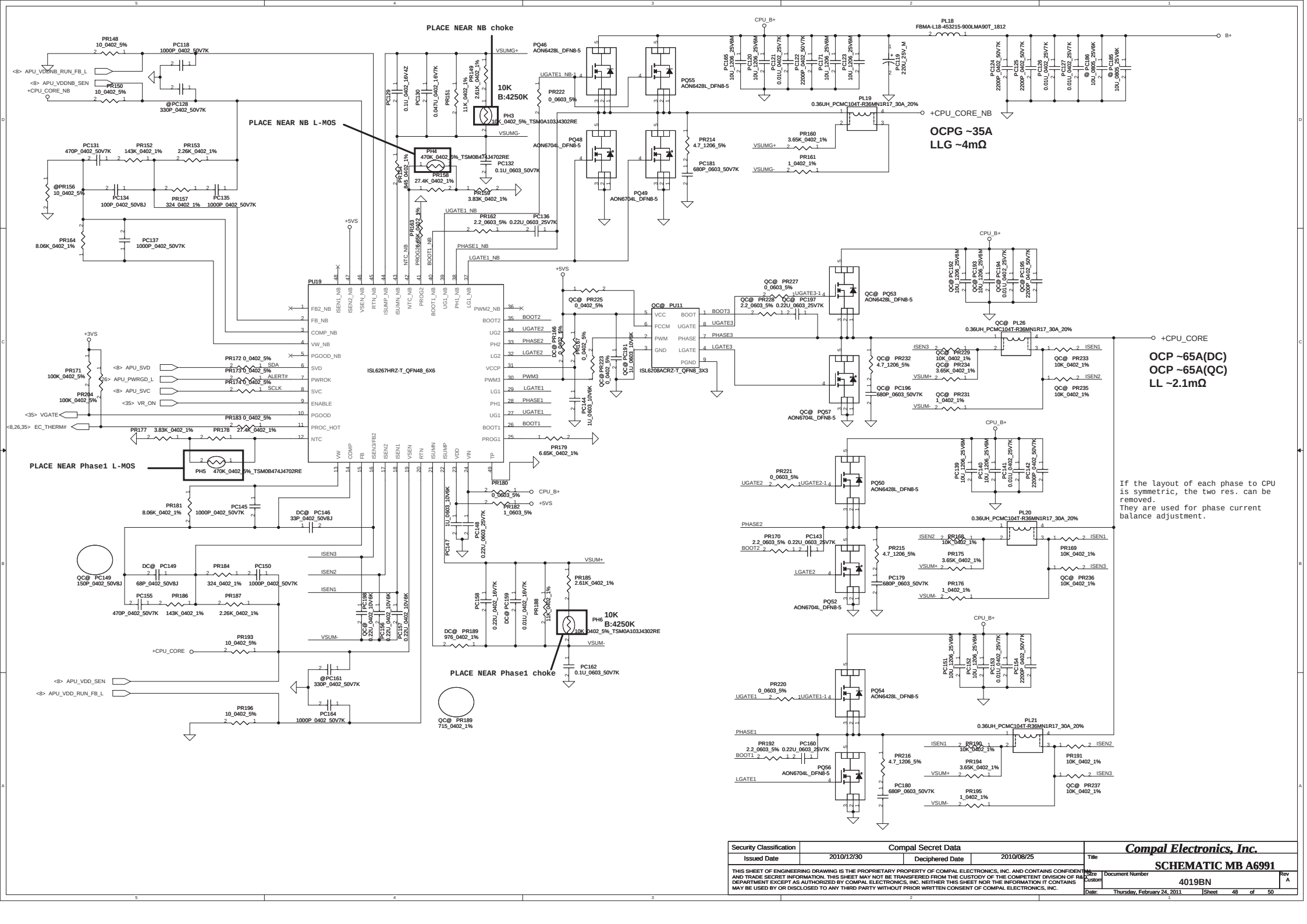

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Prevent ESD			Change SB000006800 to SB000009Q80	2011 02/09	DVT
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							

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Version change list (P.I.R. List)

0.1->0.2

1. R1244 change to BACO@; Q136, Q139, R1262, R1259, R1260, R1261 change to @.
2. Change TEST35 to PU (pop R558; unpopR559).
3. EC_PME# PU (Pop R1503).
4. Change U56 pin 42,43 to DGND.
5. Change U6, R1537, R1538, R1539, R1540 to @.
6. ALLOW_STOP, APU_SVC, APU_SVD PU to +1.5V (add R604, R607, R618).
7. Reserve +1.2VS to replace U6 SW power (add R948 pad).
8. Unpop R25, add Q145.
9. Add component for KBC930 and KBC9012 colay:
   R1518 (9012@), R1546 (@), R1547 (930@), R1548 (@), R1549 (930@), R1550 (9012@), R1551 (@), R1552 (9012@), R1553 (9012@), R1556 (930@), R1557 (9012@), R1558 (9012@).
10. Add Net for KBC930 and KBC9012 colay:
    9012_PH2, GPXO06, GPXO07, GPXO10, 9012_PH1, GPXID7, +EC_VCC.
11. Reserve R1554, R1555 for FFC USB/B.
12. Delete RTS5209 PCIE port (del C1376, C1377, C158, C248); delete CLK req (del R55); delete Card det (del R144).
13. For RTS5138, add USB port 6 and one 48MHz clock from FCH.
14. Add R88 for USB/B oc pin.
15. Change D33 to @.
16. Change R1529, R1530, C1682 to @.
17. For DVT board ID, change R1475 to 18K.
18. Change R1526 to 930@.
19. Change C1486 to PX@.
20. Reserve R360, R403, C1 and C26 for EMI.
21. Del R1554, R1555 for FFC USB/B.
22. Change mini2 USB port from port 9 to port 0 (del R1542, R1543).
23. Change R1289, R1290 to RT@.
24. Add C1468, C1469 on SYSON# for ESD reserve.
25. Change R417, R148 to DISO@.
26. Add TP on JCRT1.5, JCRT1.11, USB port2.
27. Add all EMI solution on TP Conn(include JE and SJV).
28. Change U25 from A12 to A13 (unpop Q145, pop R25).
29. Change U73, R1513, R1515, R1514, R1516, R1517, R1511, C1642 to 930@.

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