

Model Name : Z5WE3/Z5WT3
File Name : LA-A621P

Compal Confidential

EA50_BM UMA M/B Schematics Document

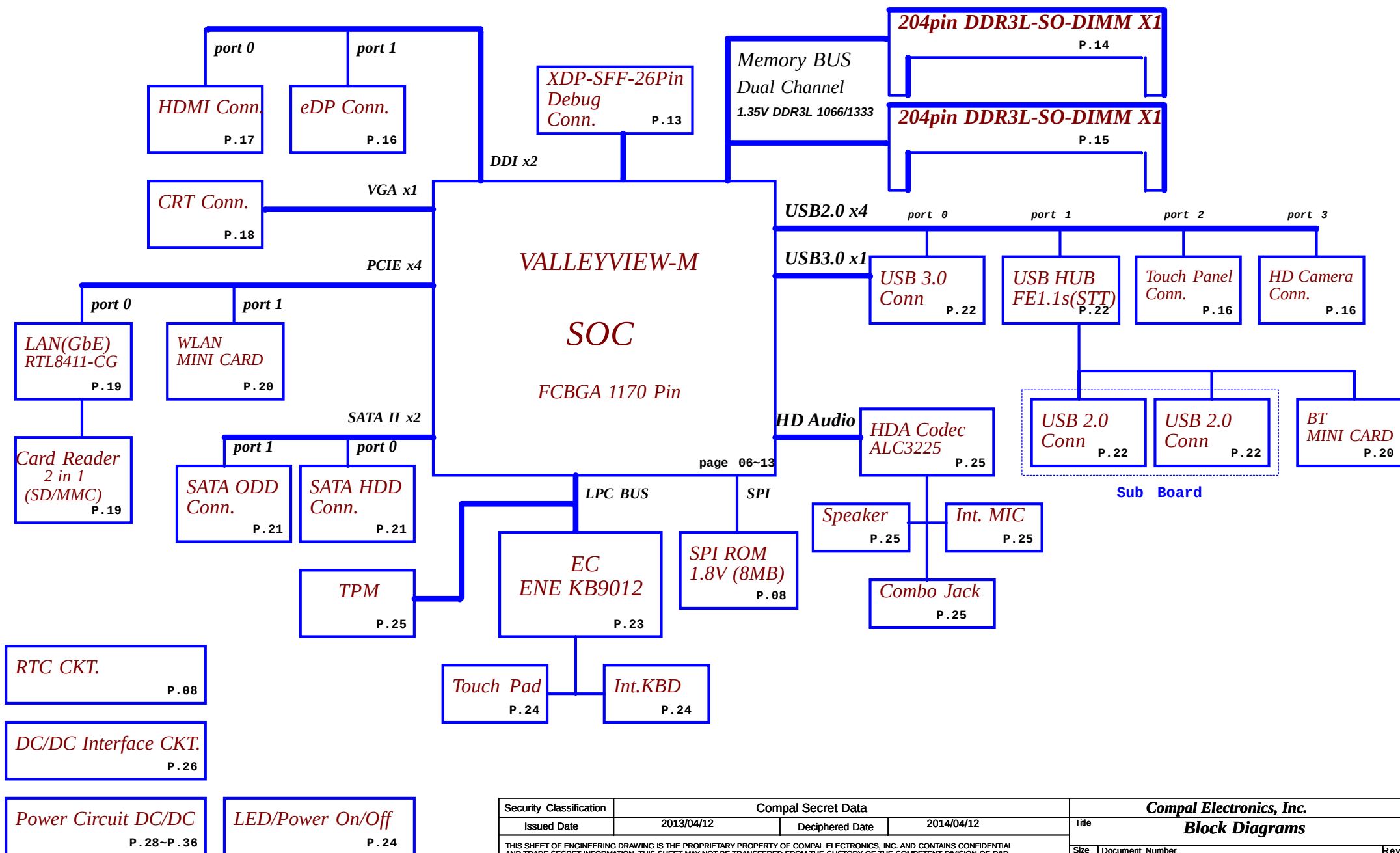
Intel Bay Trail M

2013-09-03

REV: 0.3

PCB@ ZZZ PCB 12R LA-A621P REV0 M/B	
Part Number	Description
DA60012W000	PCB 12R LA-A621P REV0 M/B

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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
TPM	TPM@
Touch Screen	TS@
R short	RS@
Test Point	TEST@

EC SM Bus1 address

EC SM Bus2 address

Device	Address
Smart Battery	0001 011X b

SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1)	A0h
SO-DIMM B (JDIMM2)	A2h

43 level BOM table

43 Level	Description	BOM Structure
4319QPB0L01	SMT MB AA621 Z5WE3 BTM 1.67G HDM1	DBG@/EMC@/TS@/XDP@/B0@
4319QPB0L02	SMT MB AA621 Z5WE3 N2910 1.67G HDM1	DBG@/EMC@/TS@/XDP@/N2910@
4319QPB0L03	SMT MB AA621 Z5WE3 N3510 2.16G HDM1	DBG@/EMC@/TS@/XDP@/N3510@
4319QPB0L04	SMT MB AA621 Z5WE3 N2910 B2 1.67G HDM1	DBG@/EMC@/TS@/XDP@/N2910B2@



S IC FH8065301546401 QF9D B1 1.67G ABO!
Part Number = SA000072B20



S IC FH8065301546300 QF9E B1 2.16G ABO!
Part Number = SA000075O10



S IC FH8065301546402 QFH0 B2 1.6G ABO!
Part Number = SA000072B60

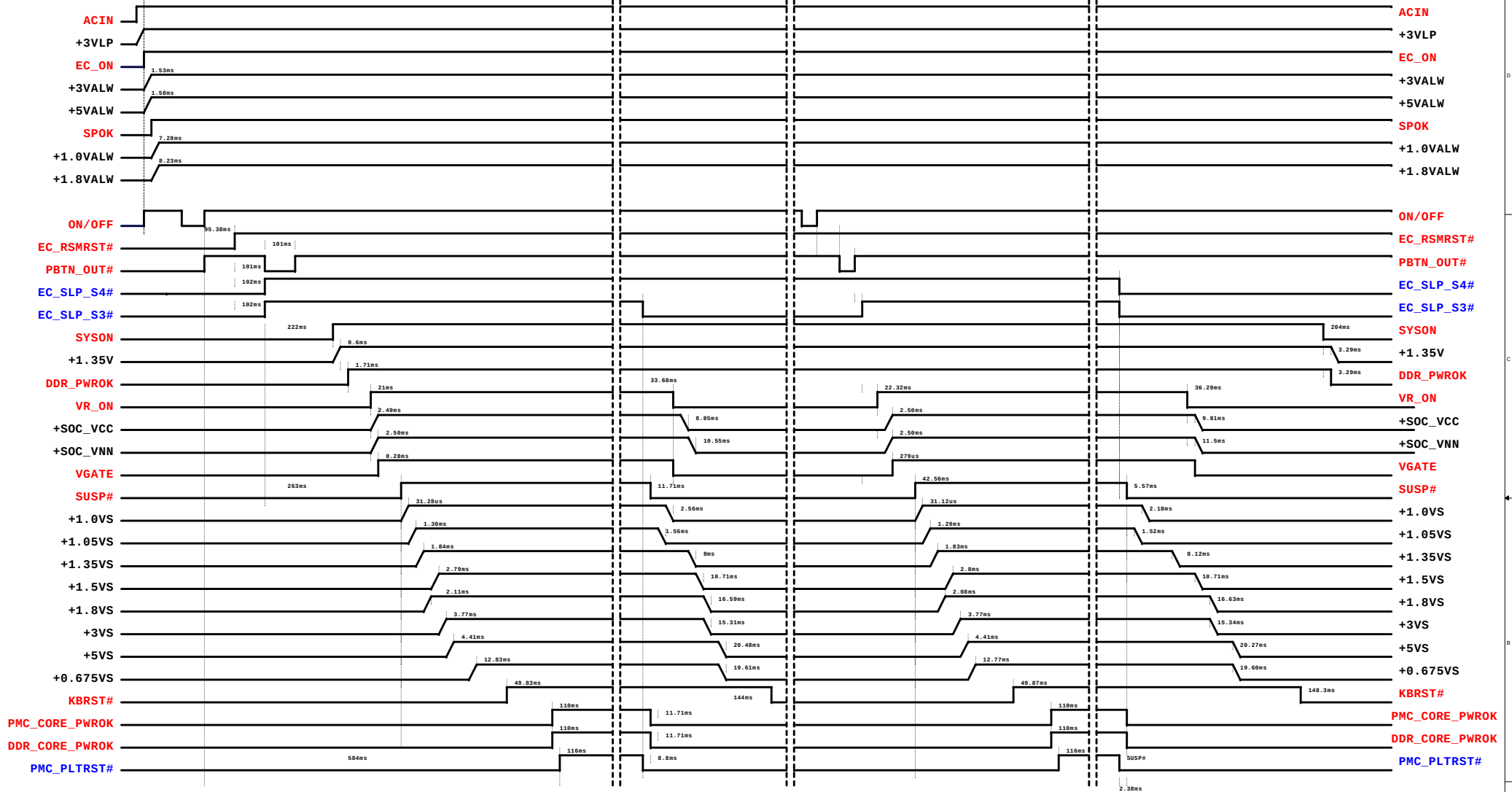
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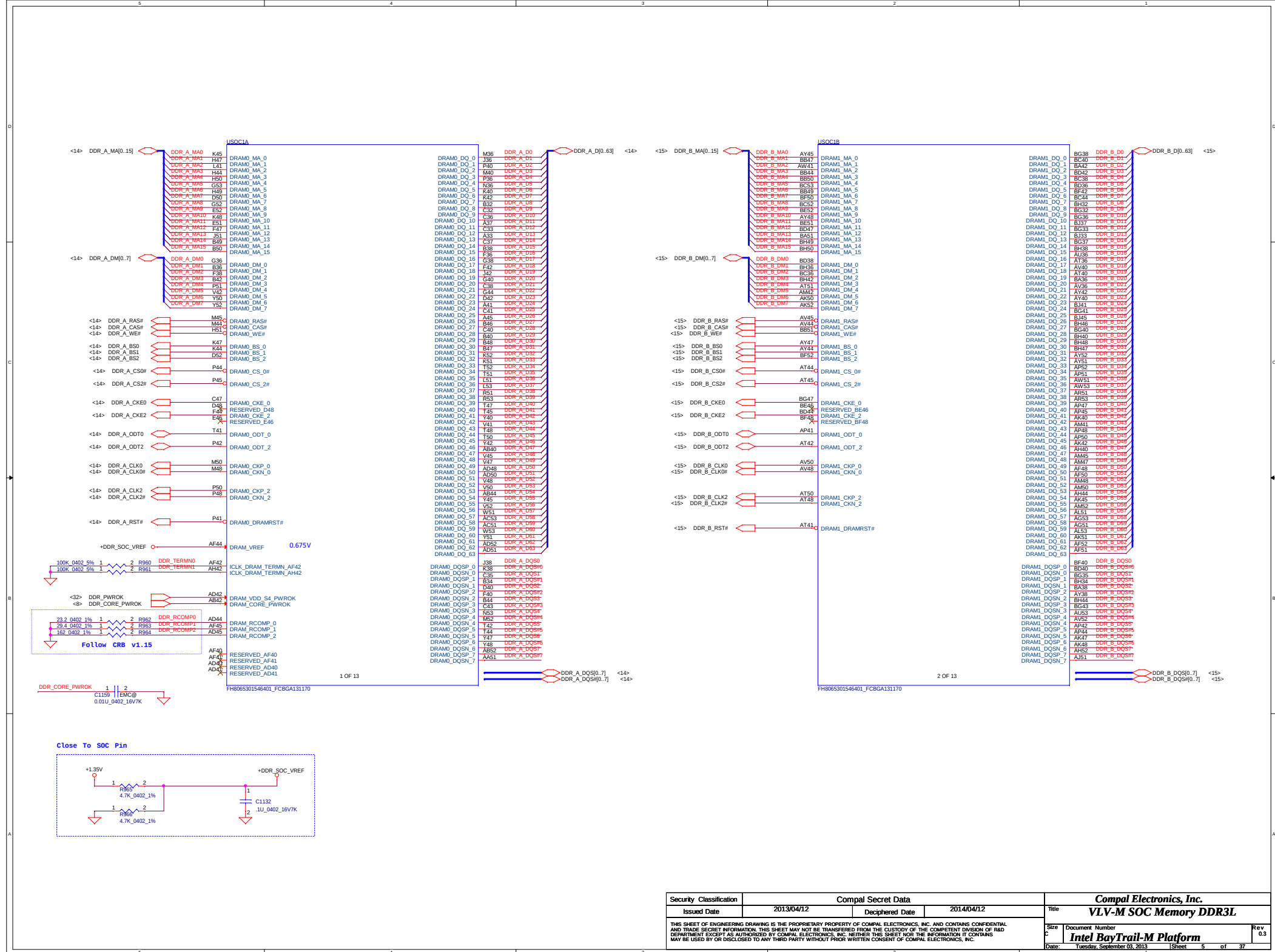
G3->S0

S0->S3

S3->S0

S0->S5

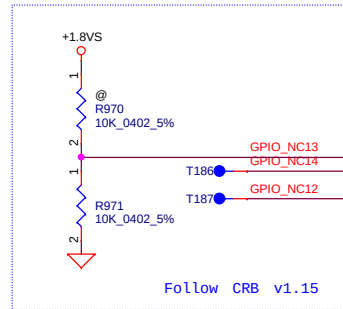




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HDMI

Follow CRB v1.15 0ohm till to GND



GPIO_S0_NC[13]:
Multiplexed with Hardware Straps Pin:MDSI_DDCDATA

USOC1C

DDIO_TXP_0 1.0V
DDIO_TXN_0
DDIO_TXP_1
DDIO_TXN_1
DDIO_TXP_2
DDIO_TXN_2
DDIO_TXP_3
DDIO_TXN_3
DDIO_AUXP
DDIO_AUXN
DDIO_HPD 1.8V
DDIO_DDCDATA 1.8V
DDIO_DDCCLK 1.8V
DDIO_VDDEN
DDIO_BKLTEN
DDIO_BKLTCTL

T2
T3
AB3
AB2
Y3
Y2
Y1
W3
W2
W1
V3
V2
V1
R3
R1
AD6
AD4
AB9
AB7
Y6
Y4
V6
V4
V2
A29
C29
AB14
B30
C30

FH8065301546401_FCBGA131170

3 OF 10

DDI1_TXP_0 1.0V
DDI1_TXN_0
DDI1_TXP_1
DDI1_TXN_1
DDI1_TXP_2
DDI1_TXN_2
DDI1_TXP_3
DDI1_TXN_3
DDI1_AUXP
DDI1_AUXN
DDI1_HPD 1.8V
DDI1_DDCDATA 1.8V
DDI1_DDCCLK 1.8V
DDI1_VDDEN
DDI1_BKLTEN
DDI1_BKLTCTL

VSS_AH3
VSS_AH2
RESERVED_AH14
RESERVED_AH13
RESERVED_AH14
RESERVED_AH13
RESERVED_AH13

VGA_RED
VGA_BLUE
VGA_GREEN
VGA_IREF
VGA_IRTN
VGA_HSYNC 3.3V
VGA_VSYNC 3.3V
VGA_DDCCLK 3.3V
VGA_DDCDATA 3.3V

RESERVED_T7
RESERVED_T9
RESERVED_AB13
RESERVED_AB12
RESERVED_Y12
RESERVED_Y13
RESERVED_Y10
RESERVED_Y9
RESERVED_Y12
RESERVED_Y10
RESERVED_T10
RESERVED_V13
RESERVED_T14
RESERVED_T13
RESERVED_T6
RESERVED_T4
RESERVED_P14

GPIO_S0_NC_15
GPIO_S0_NC_16
GPIO_S0_NC_17
GPIO_S0_NC_18
GPIO_S0_NC_19
GPIO_S0_NC_20
GPIO_S0_NC_21
GPIO_S0_NC_22
GPIO_S0_NC_23
GPIO_S0_NC_24
GPIO_S0_NC_25
GPIO_S0_NC_26

AG3
AF3
AF2
AD3
AD2
AC3
AC1
AK3
AK2
K30
P30
G30
N30
J30
M30

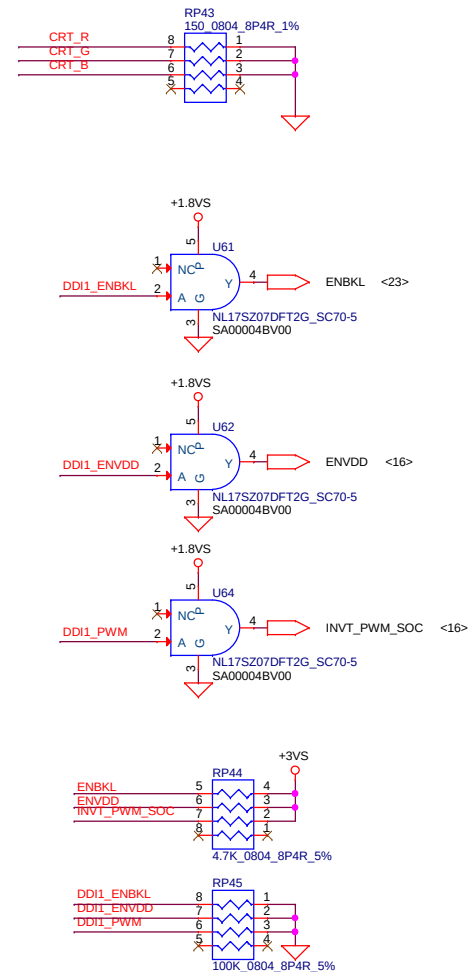
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EDP_TXP1 <16>
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EDP_HPD# <16>
DDI1_ENABLE R967 1 2 2.2K_0402 5%
DDI1_ENVDD
DDI1_ENBKLL
DDI1_PWM

Follow CRB v1.15 0ohm till to GND

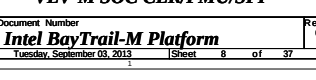
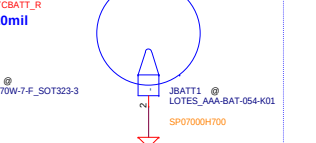
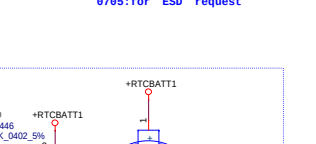
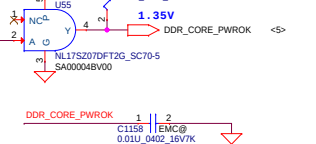
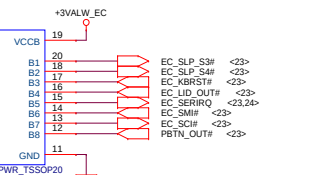
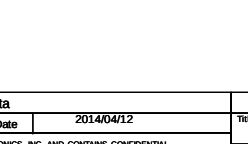
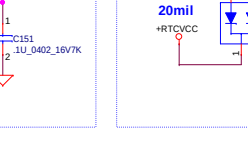
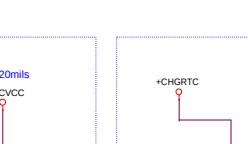
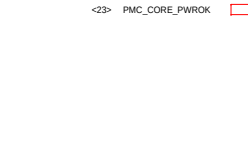
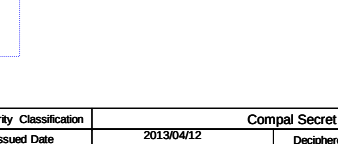
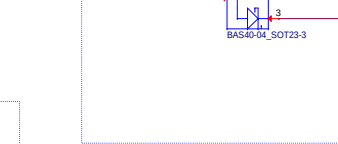
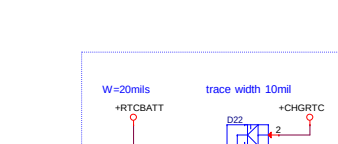
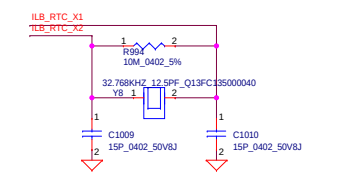
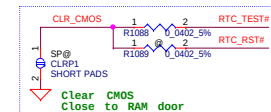
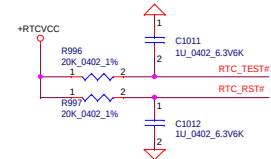
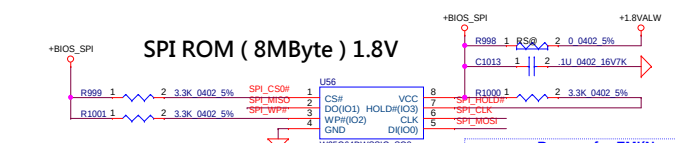
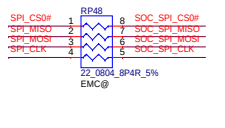
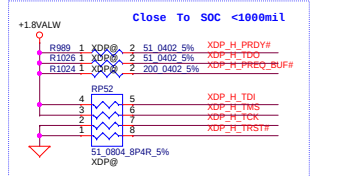
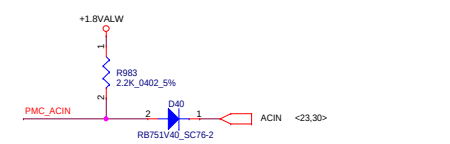
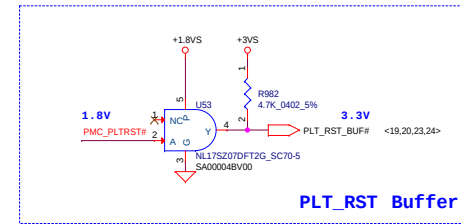
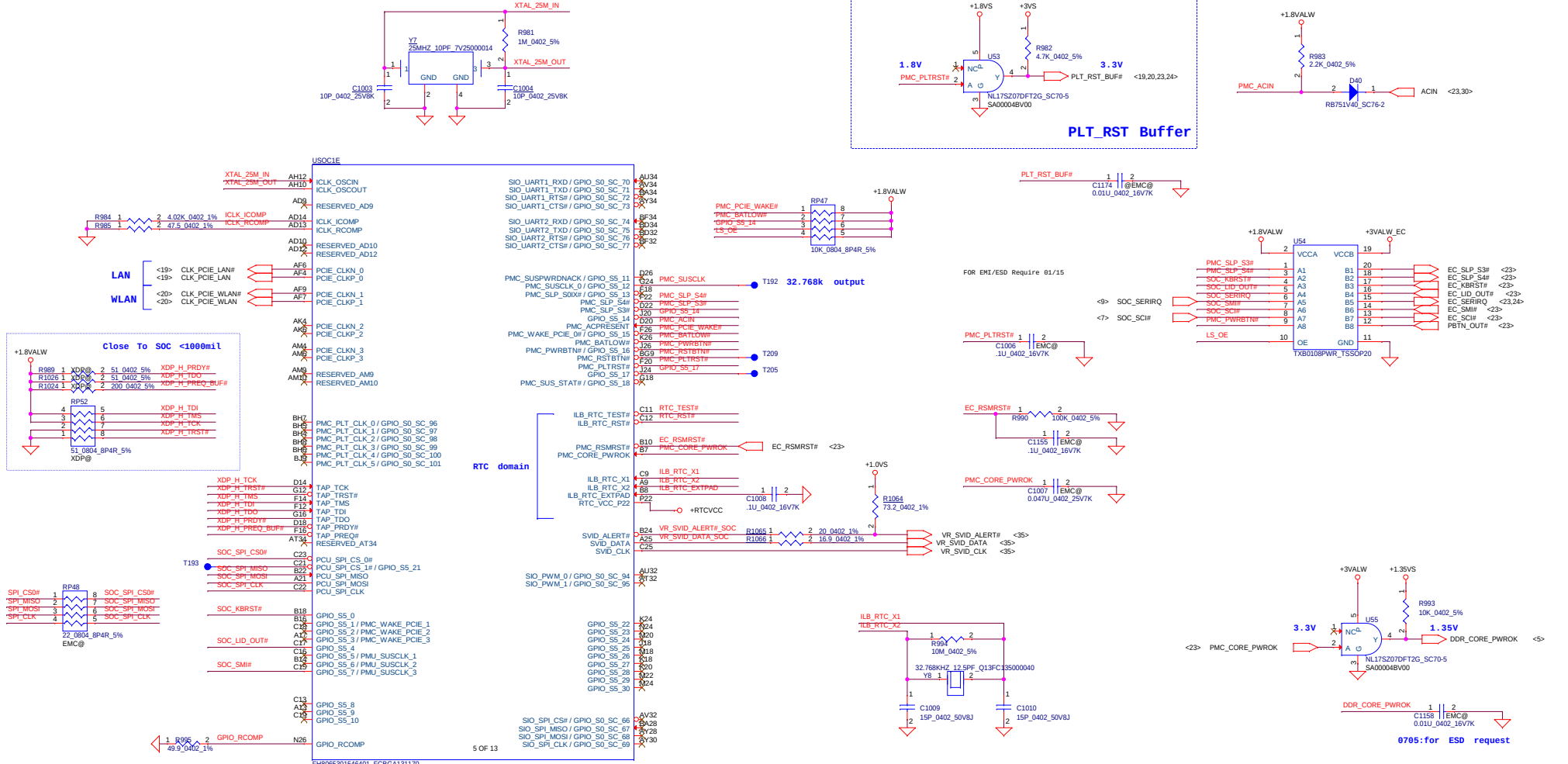
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BA1 CRT_G <18>
AW1 CRT_IREF
AY3
BD2 CRT_HSYNC <18>
BF2 CRT_VSYNC <18>
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BC2 CRT_DDC_DATA <18>

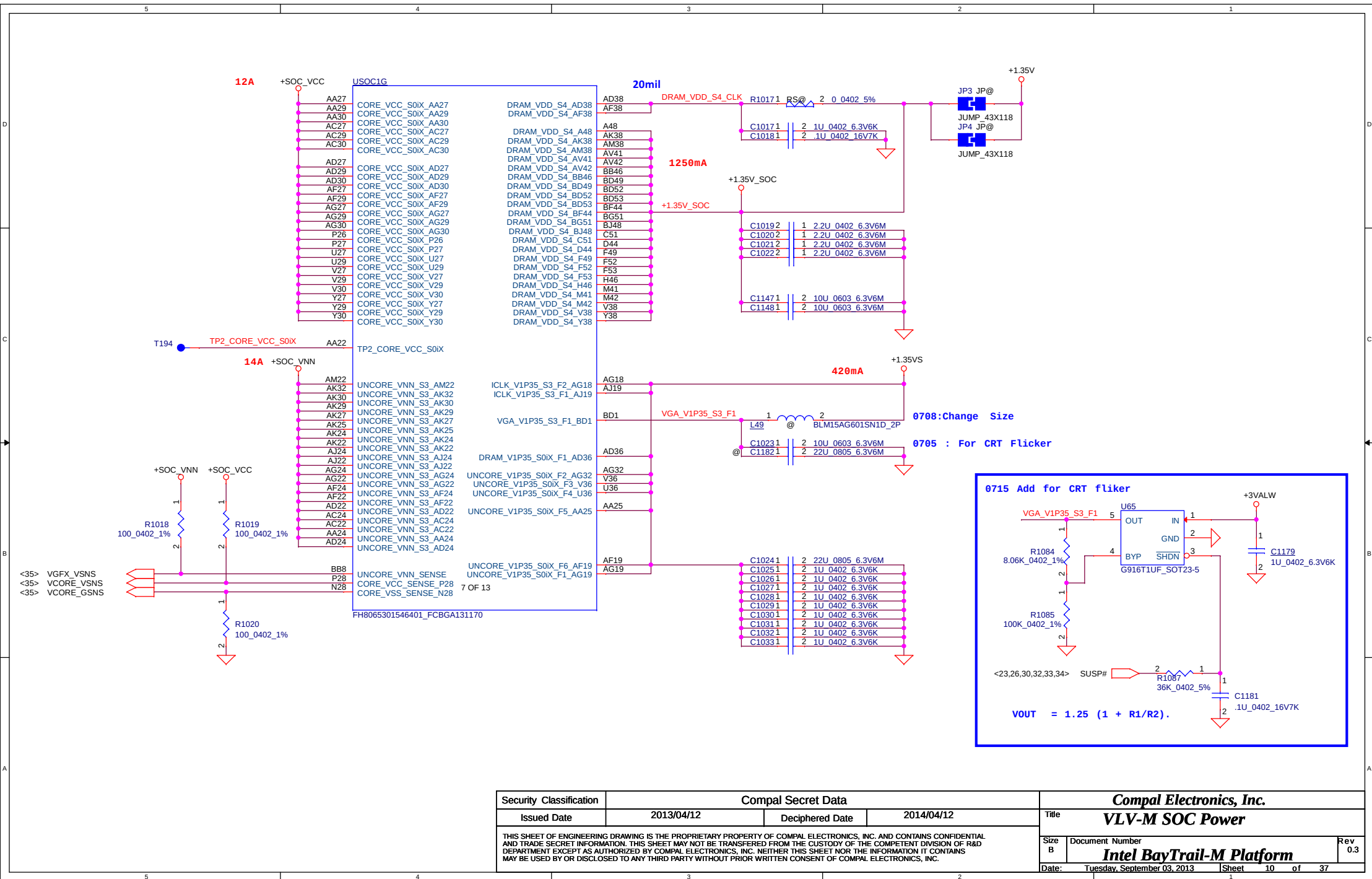
eDP Panel

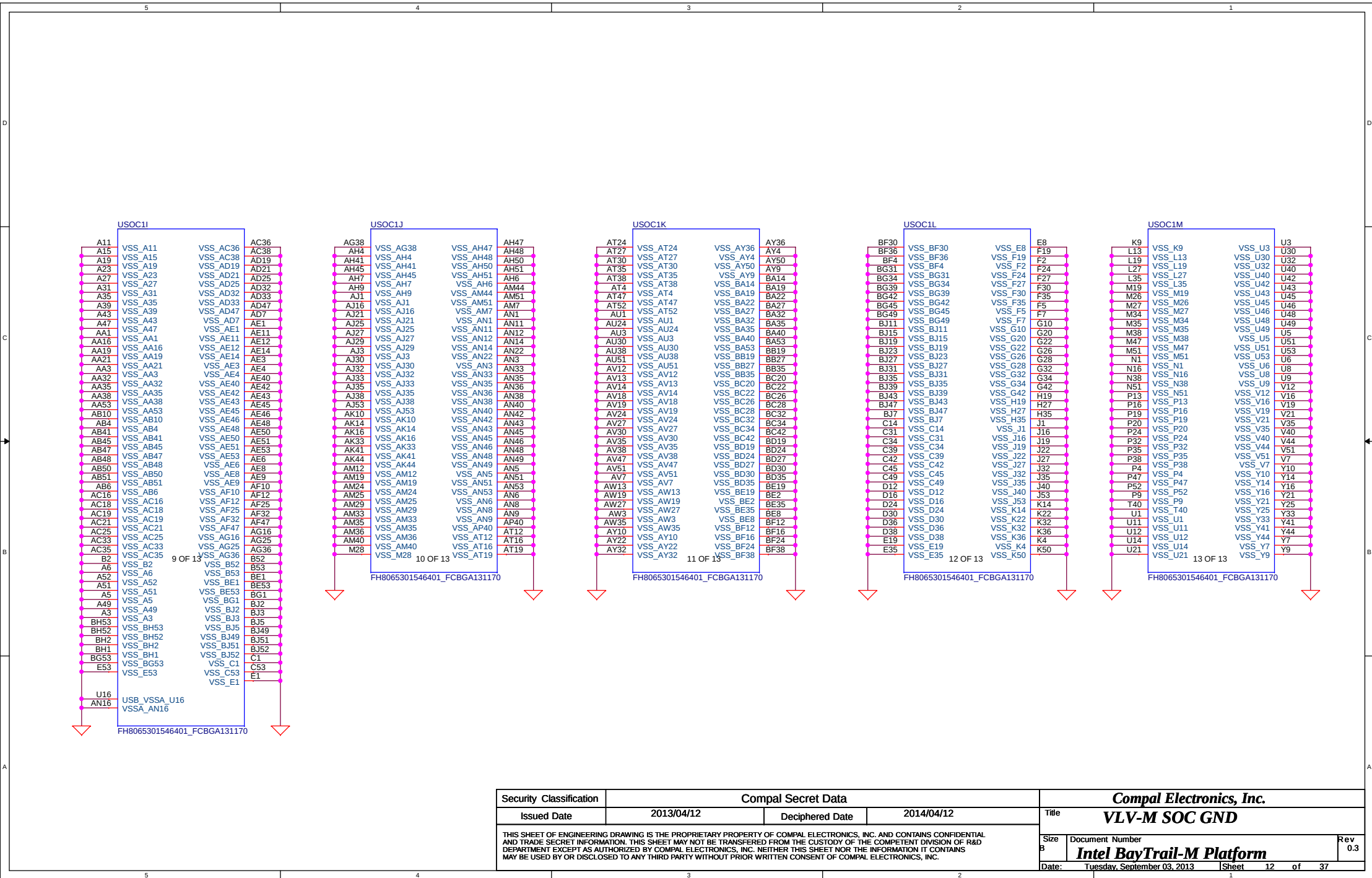
CRT



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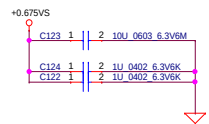






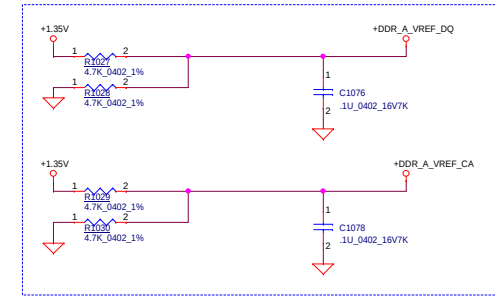
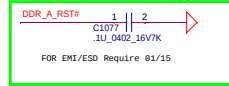
PVT 0827: Remove Debug Connector for ESD request.

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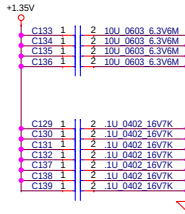
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DIMM_1 STD H:4mm

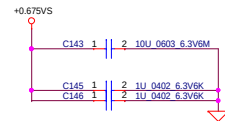


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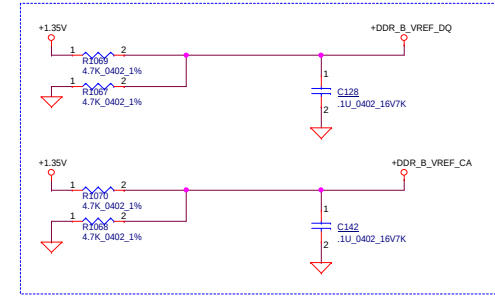
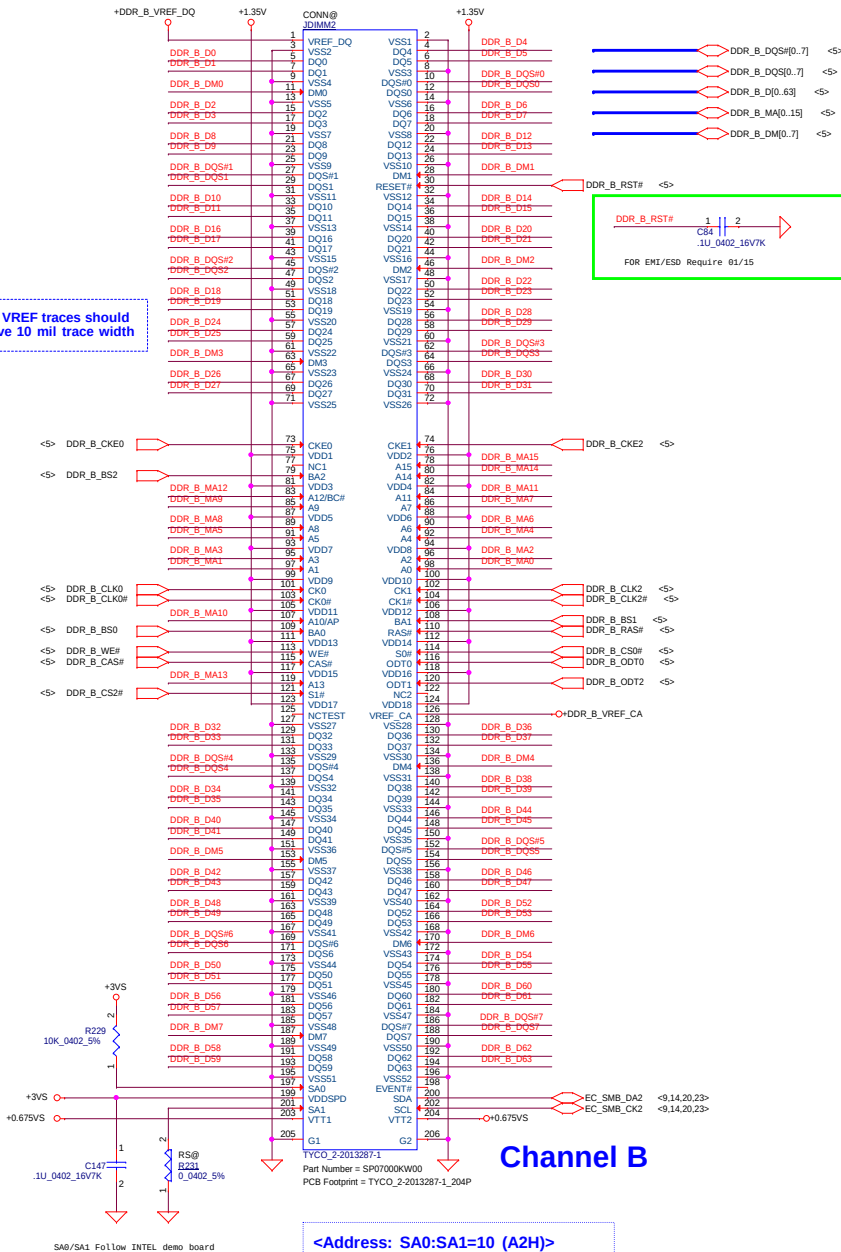
Layout Note:
Place near JDIMM2



All VREF traces should
have 10 mil trace width

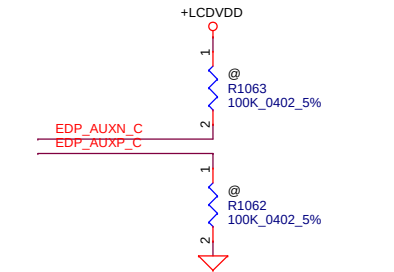
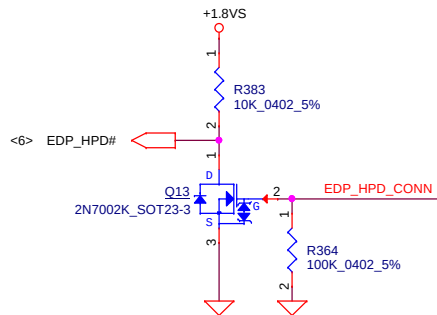
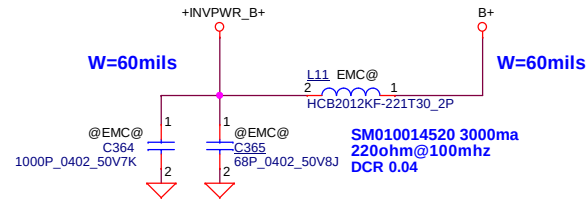
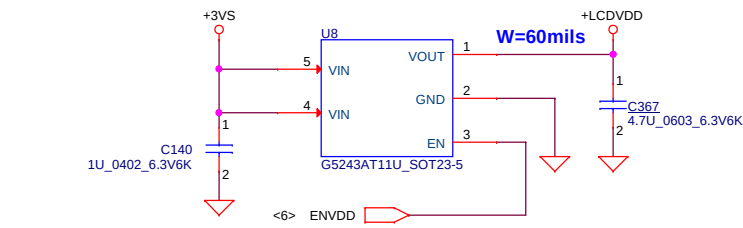


Layout Note:
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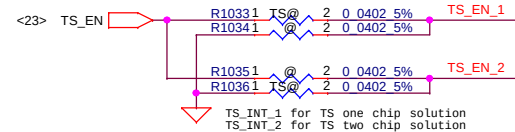
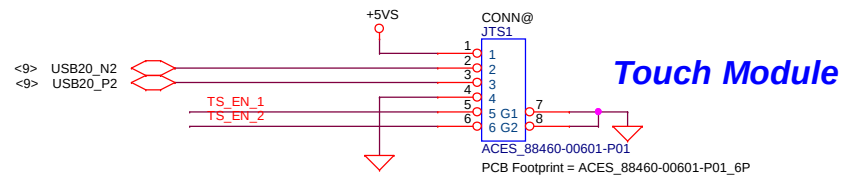
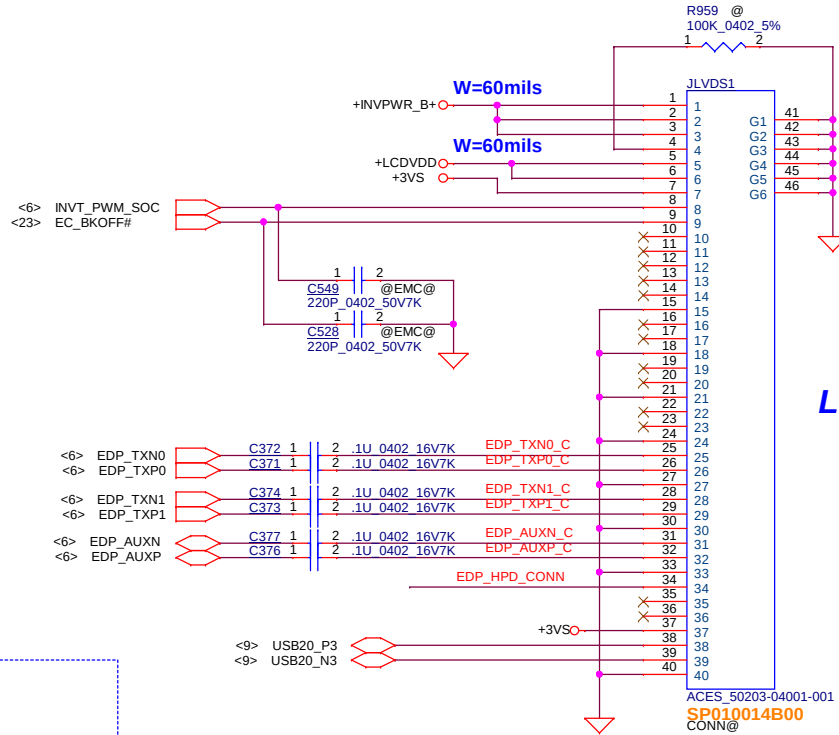


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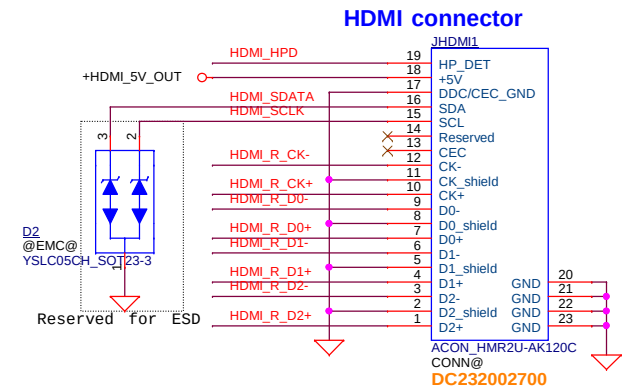
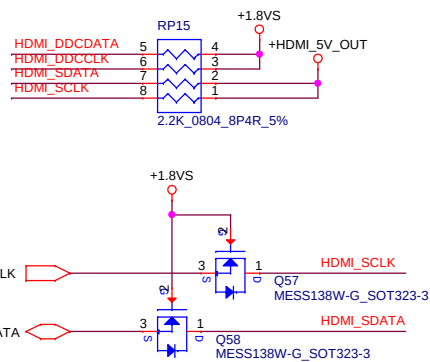
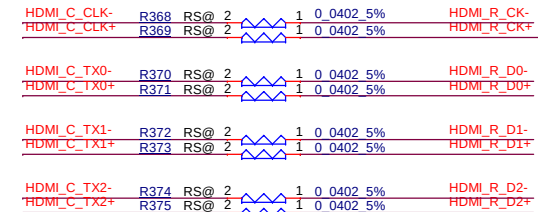
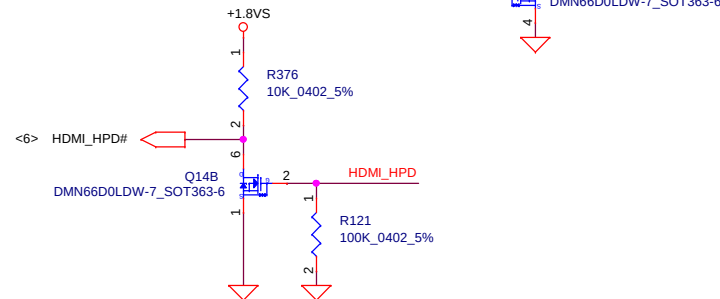
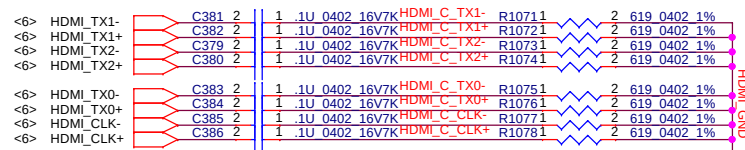
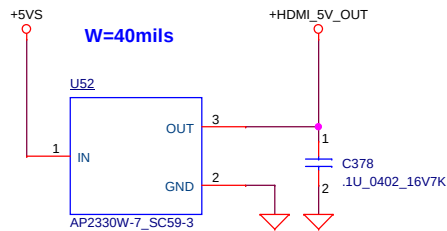
LCD POWER CIRCUIT



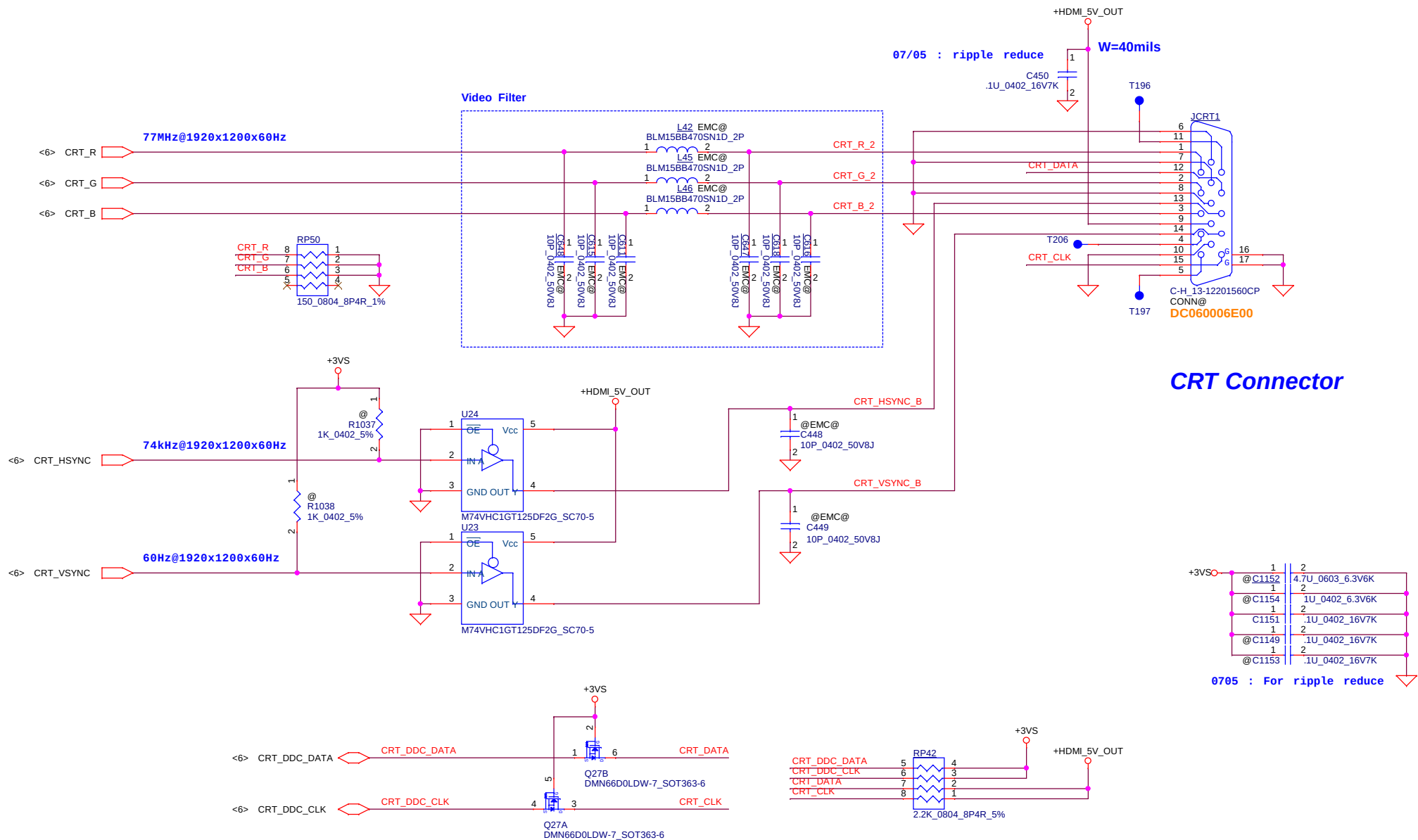
Intel recommends having a pull-up resistor of 100 k Ω for AUXN and a pull-down resistor of 100 k Ω for AUXP between the AC capacitor and the connector, to assist source detection by the sink device.



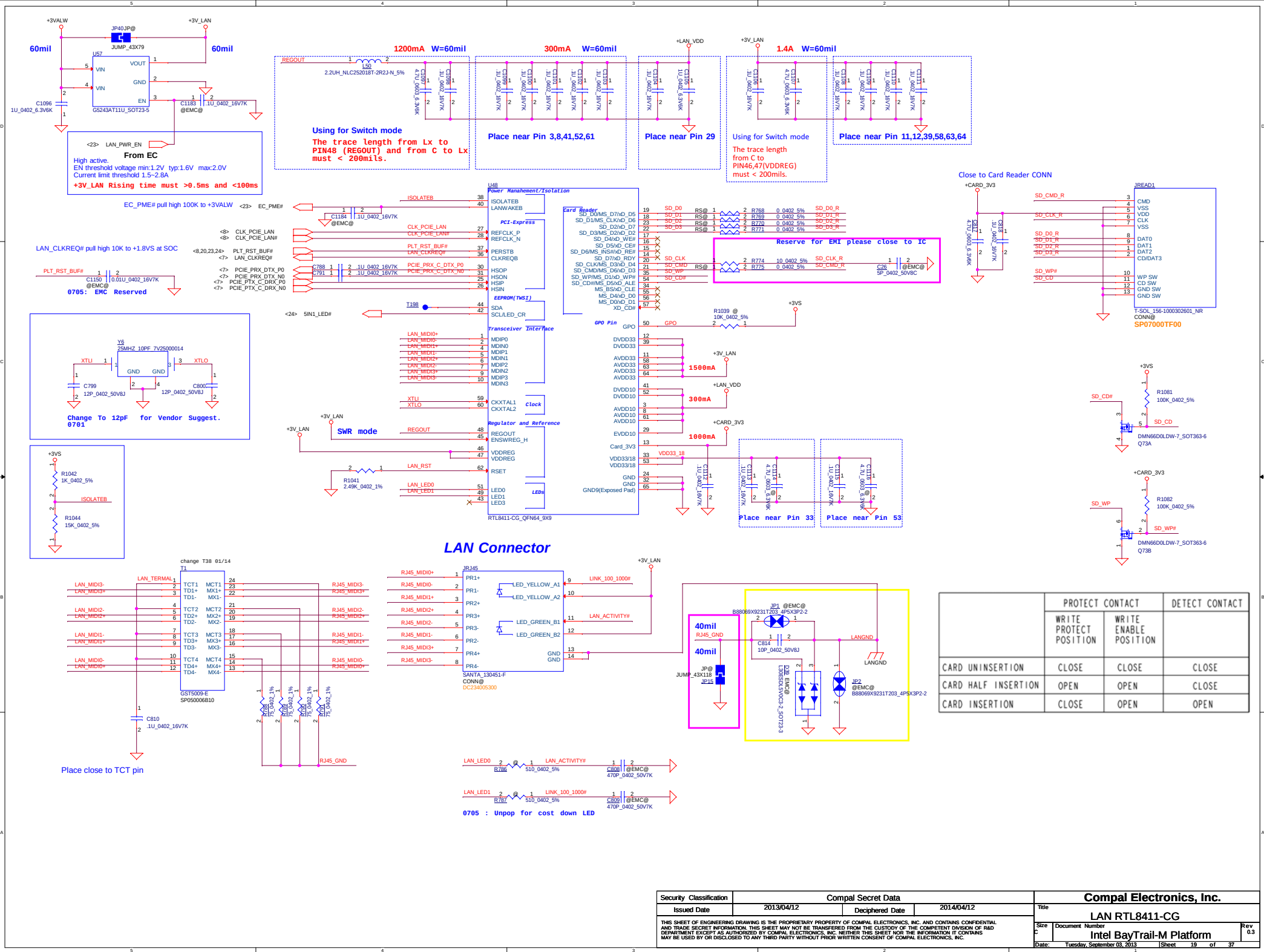
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title	
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				Size B	Document Number
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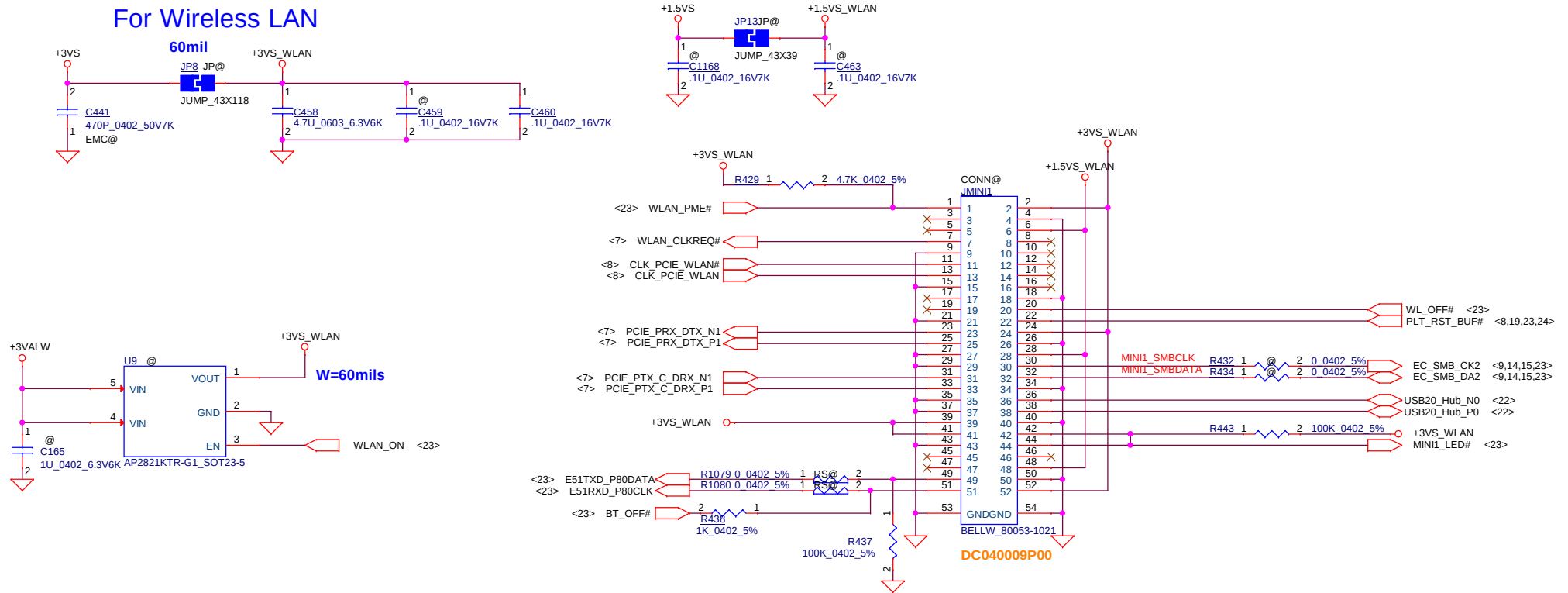
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Issued Date		2013/04/12		Deciphered Date		2014/04/12		Title	
								HDMI CONN.	
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						Size B	Document Number				Rev 0.3
						Intel BayTrail-M Platform					
Date:		Tuesday, September 03, 2013		Sheet 18	of 37						

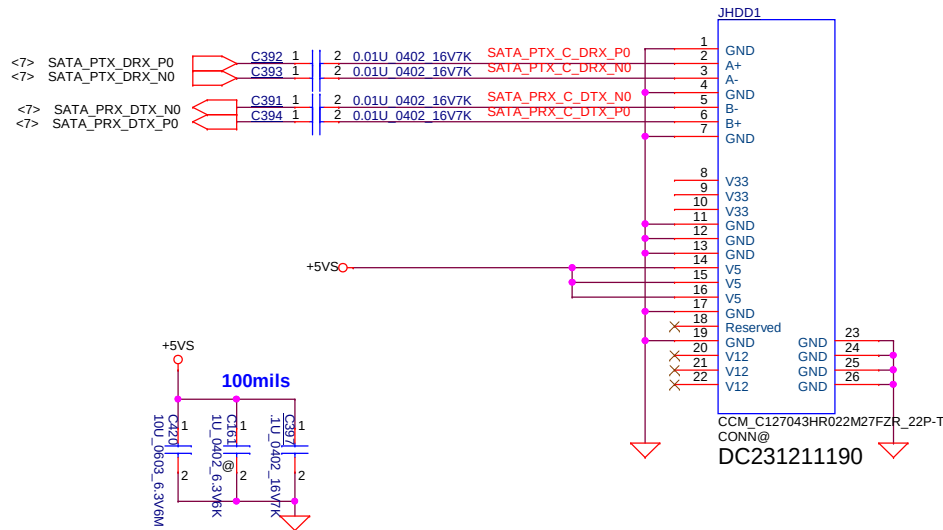


For Wireless LAN

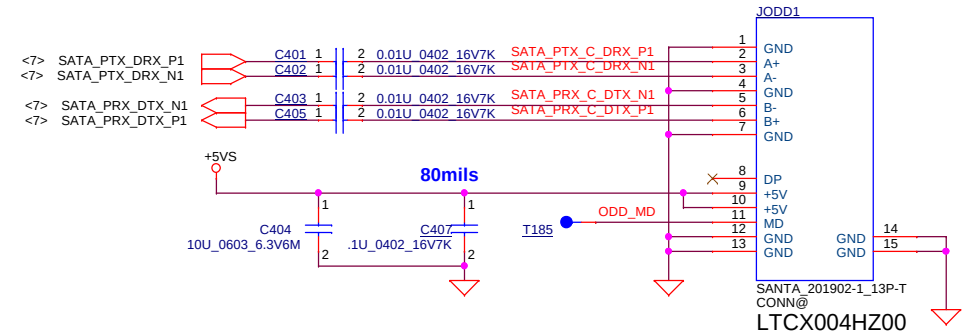


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Size B		Document Number		Rev 0.3	
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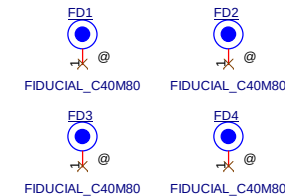
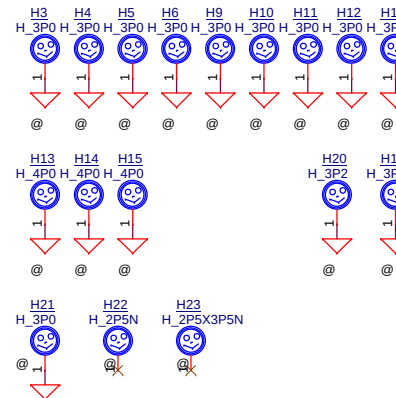
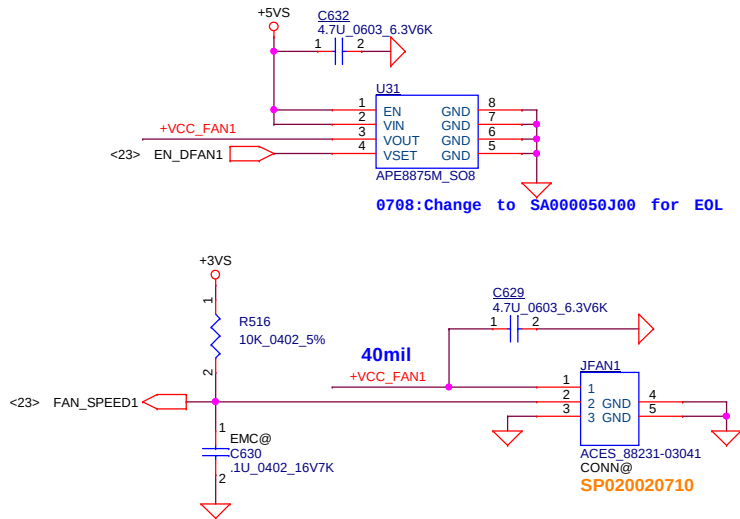
SATA HDD1 Conn.



SATA ODD Conn.

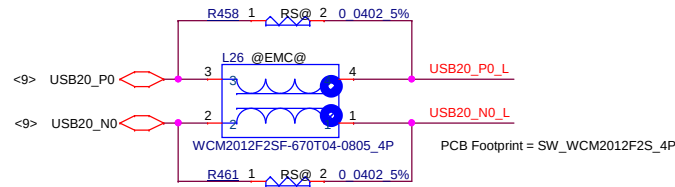
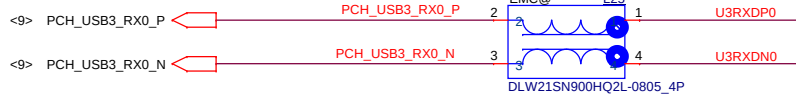
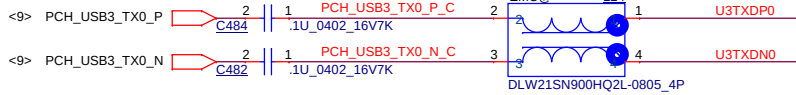


FAN1 Conn

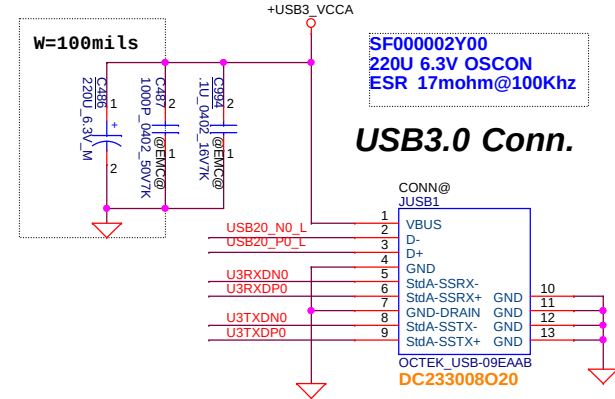
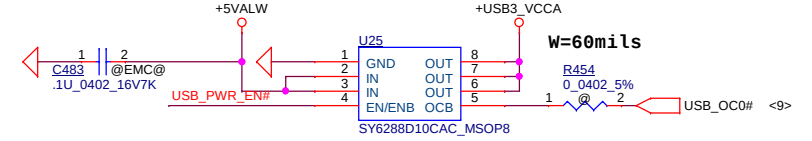
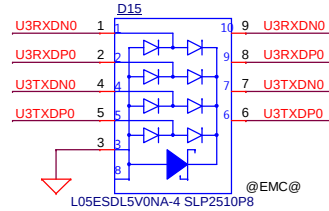


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				Size	Document Number
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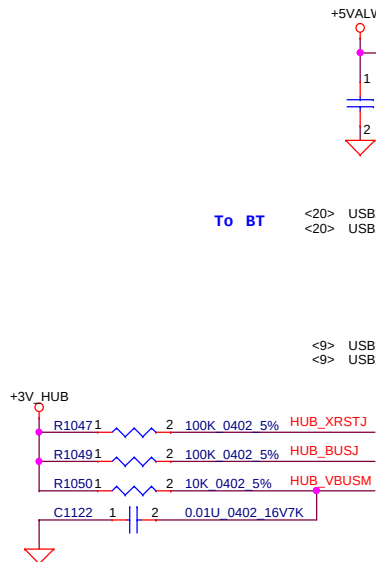
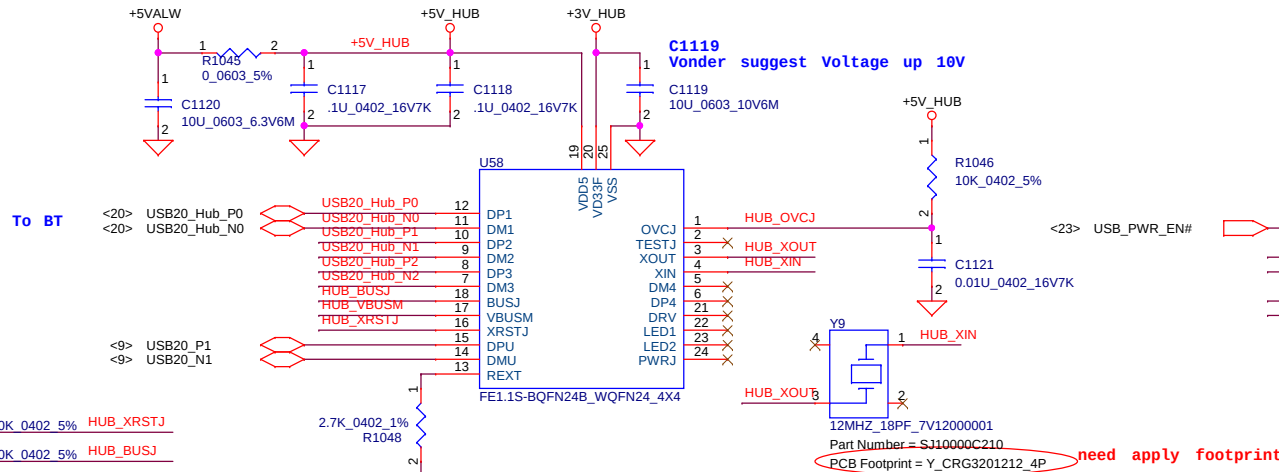
SM070000S80 WCM2012F2SF-670T04 67ohm



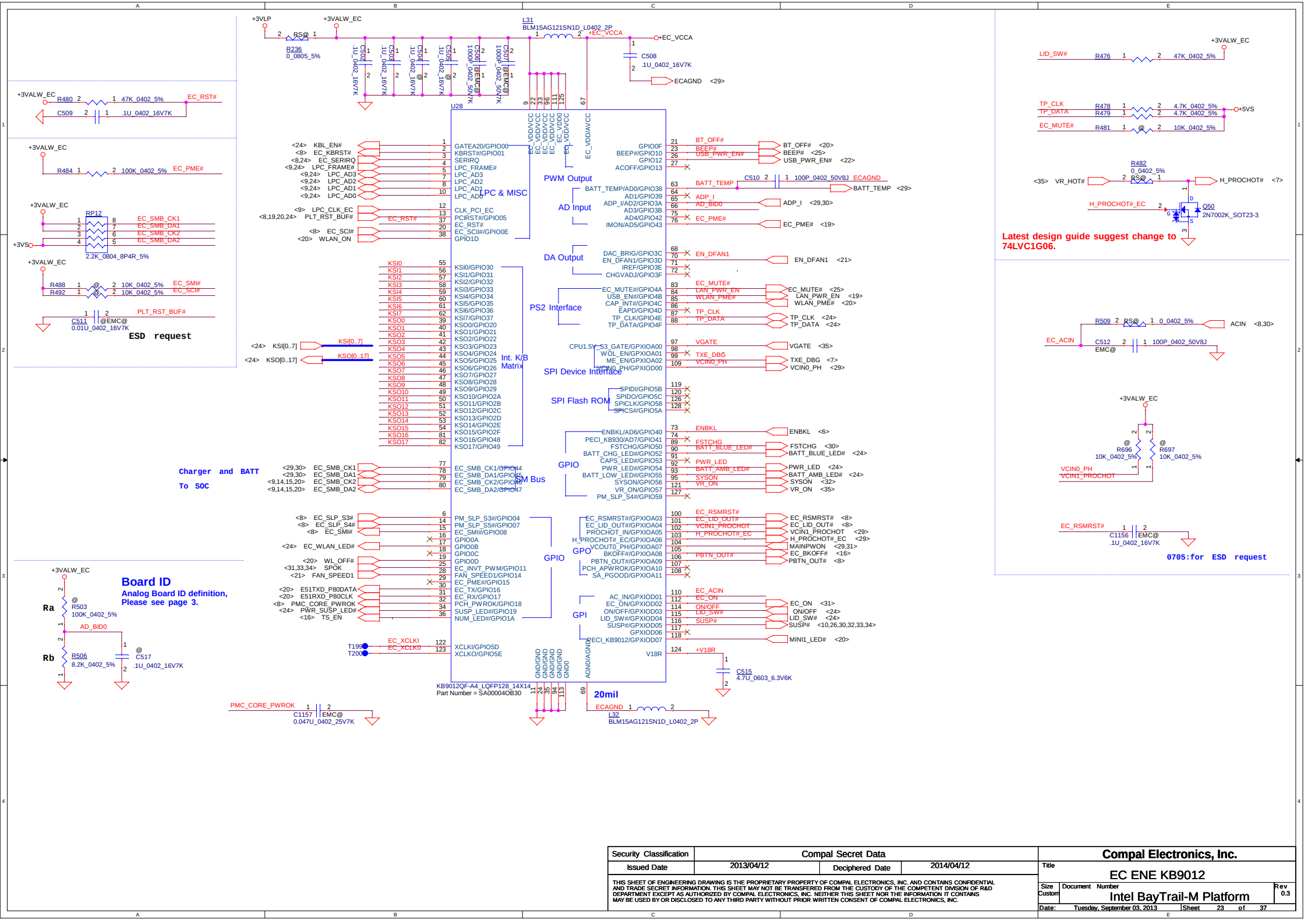
For ESD request



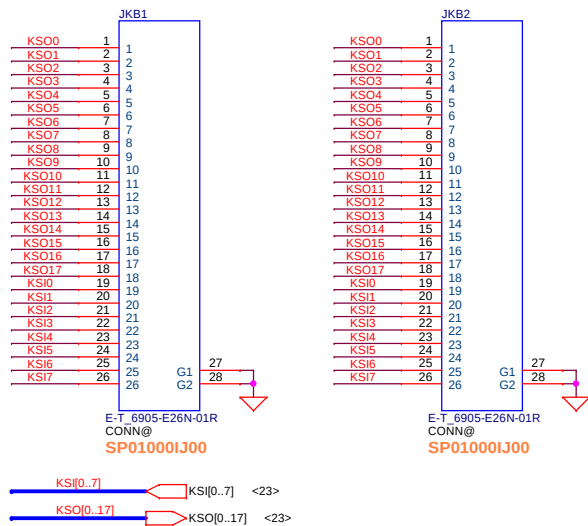
USB/B (USB Port 1, Port2)



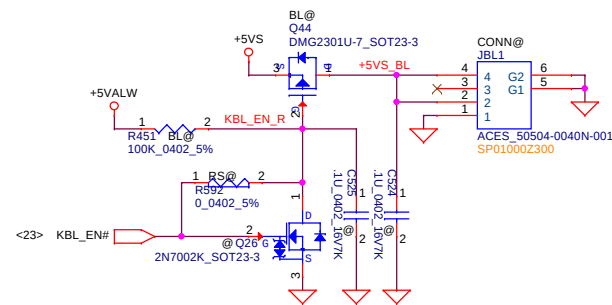
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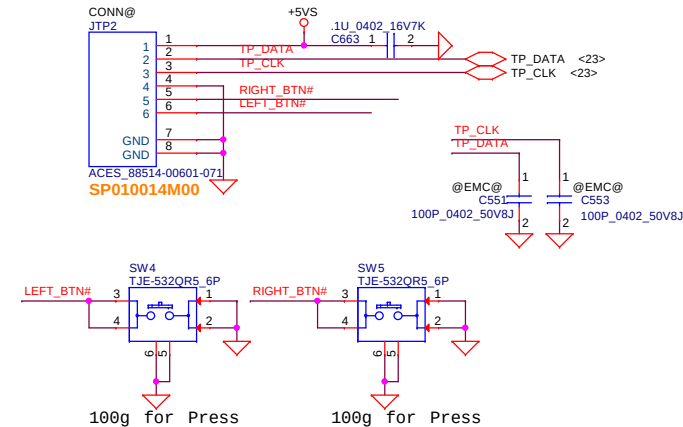
KB Conn.



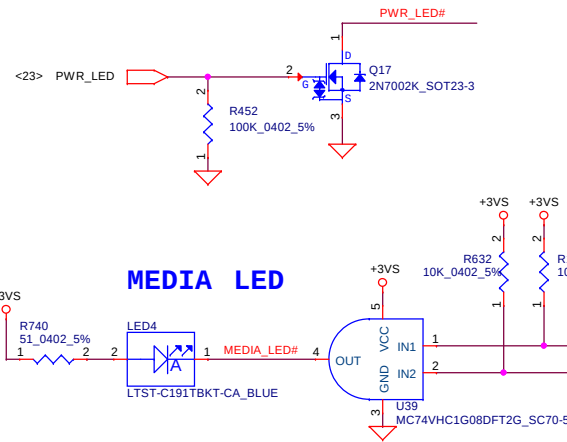
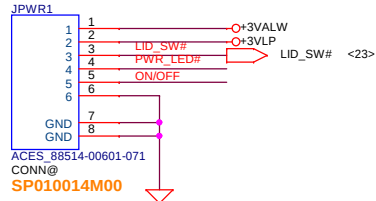
KB BackLight Conn.



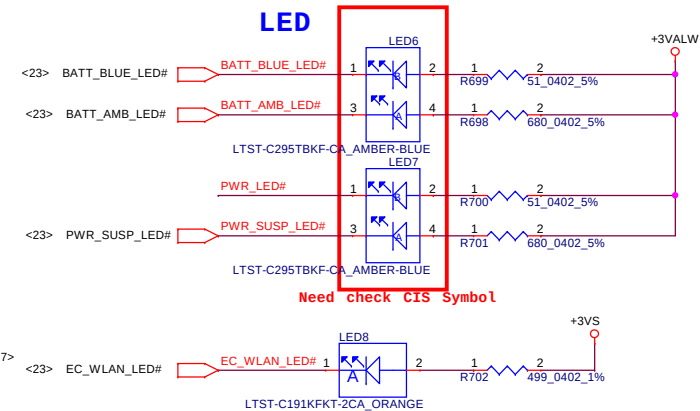
To TP/B Conn.



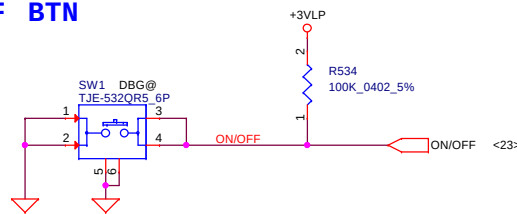
PWR/B



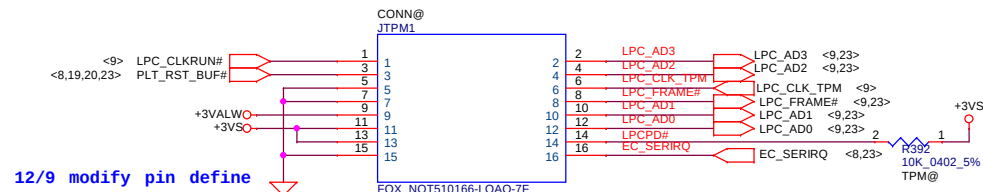
LED



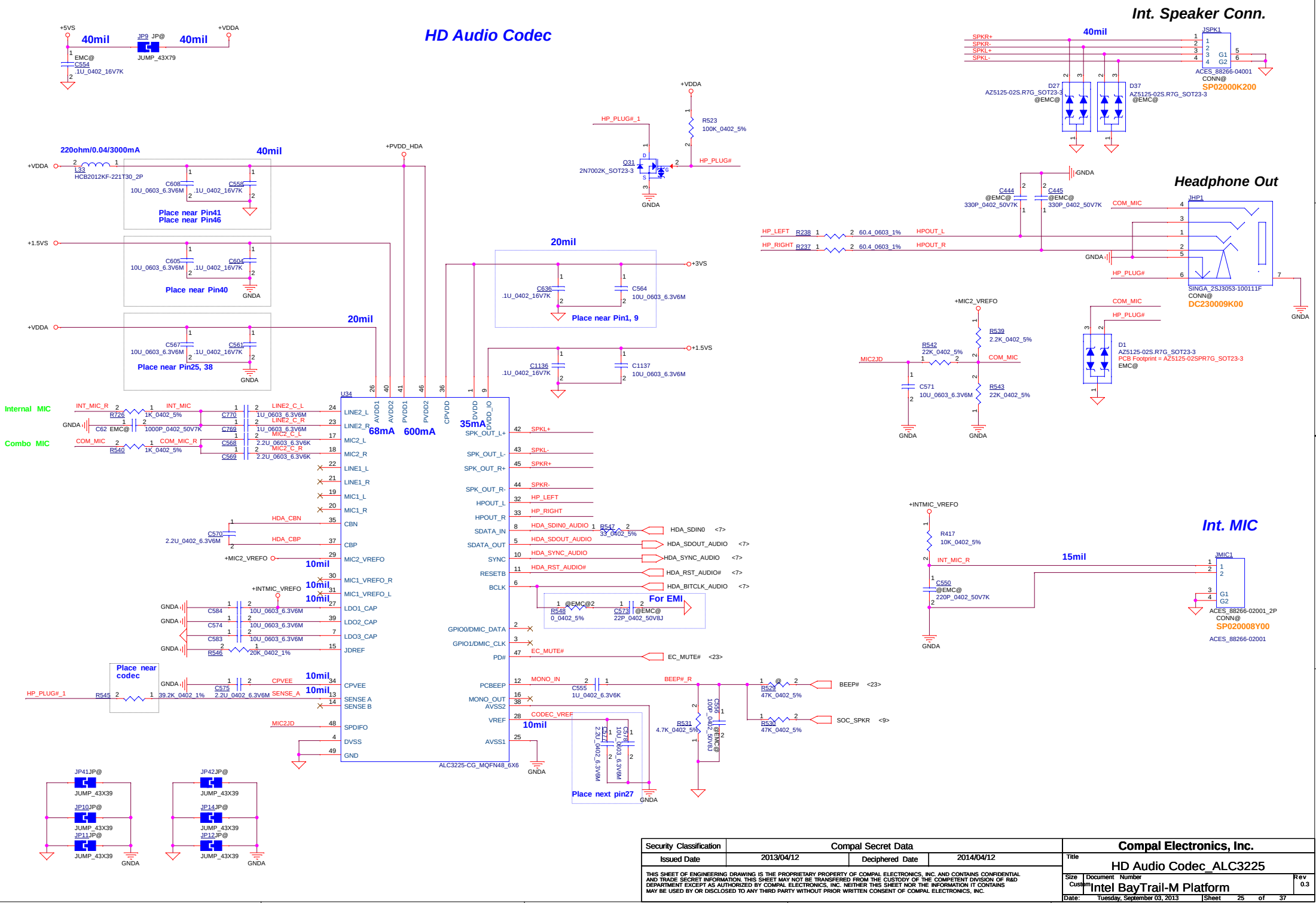
ON/OFF BTN



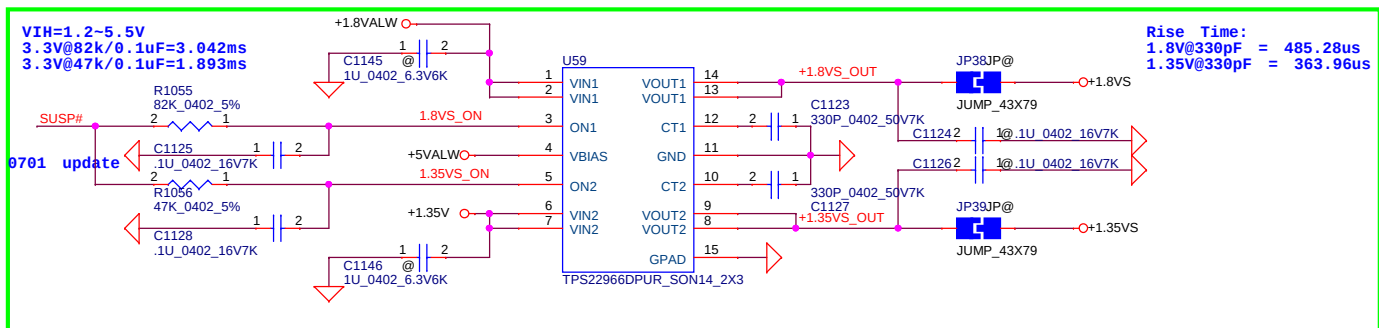
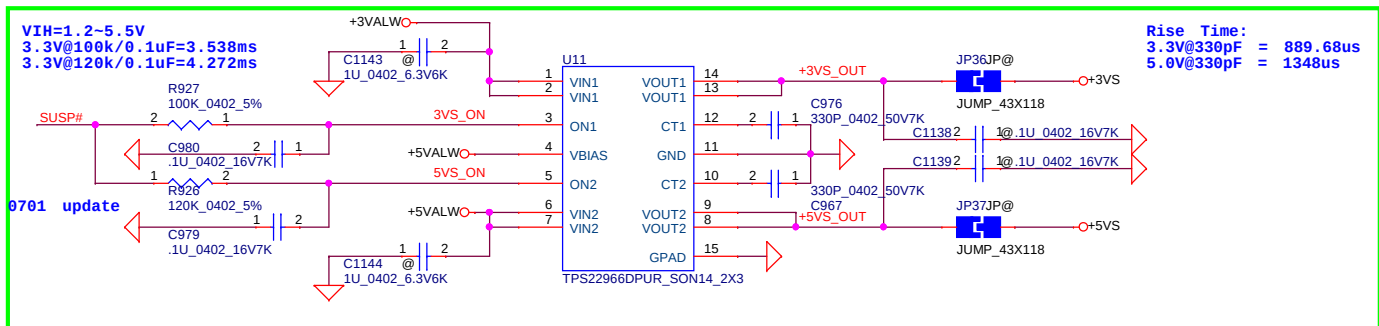
TPM Board



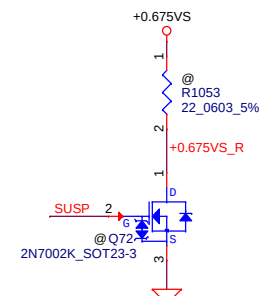
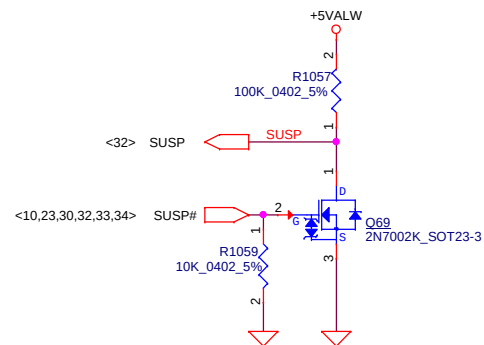
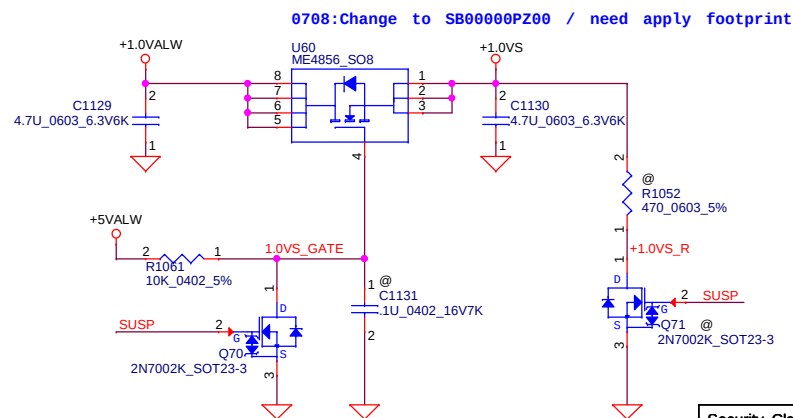
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								KB/TP/LED/TPM	
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						Date:		Tuesday, September 03, 2013	
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						Intel BayTrail-M Platform			



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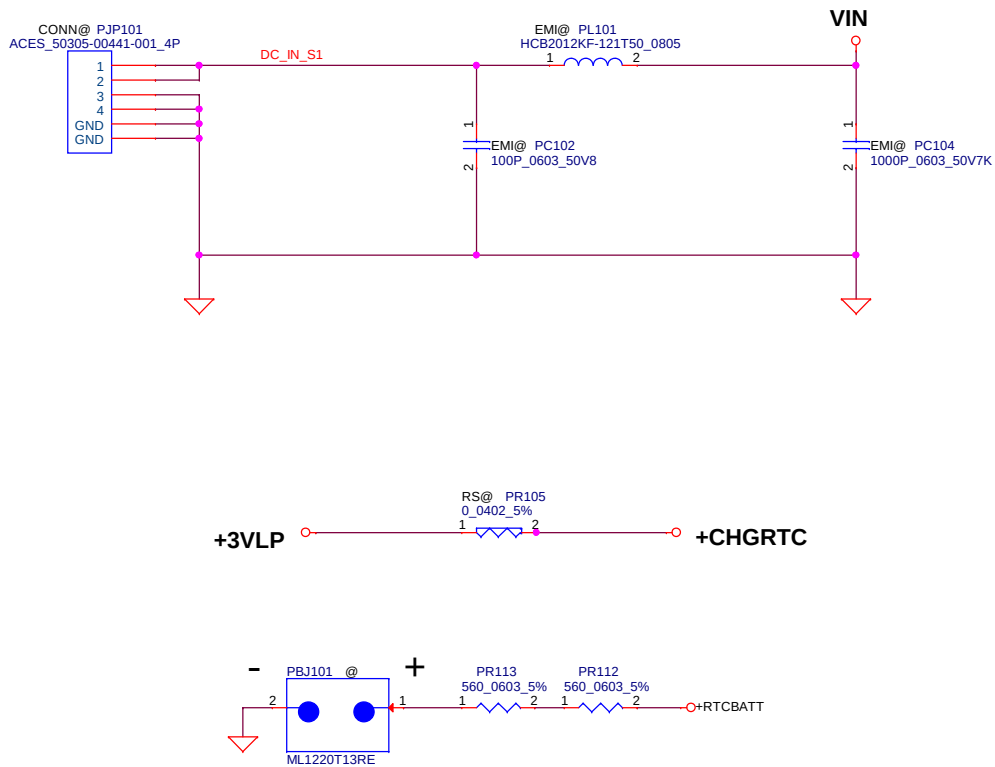
+1.0VALW TO +1.0VS



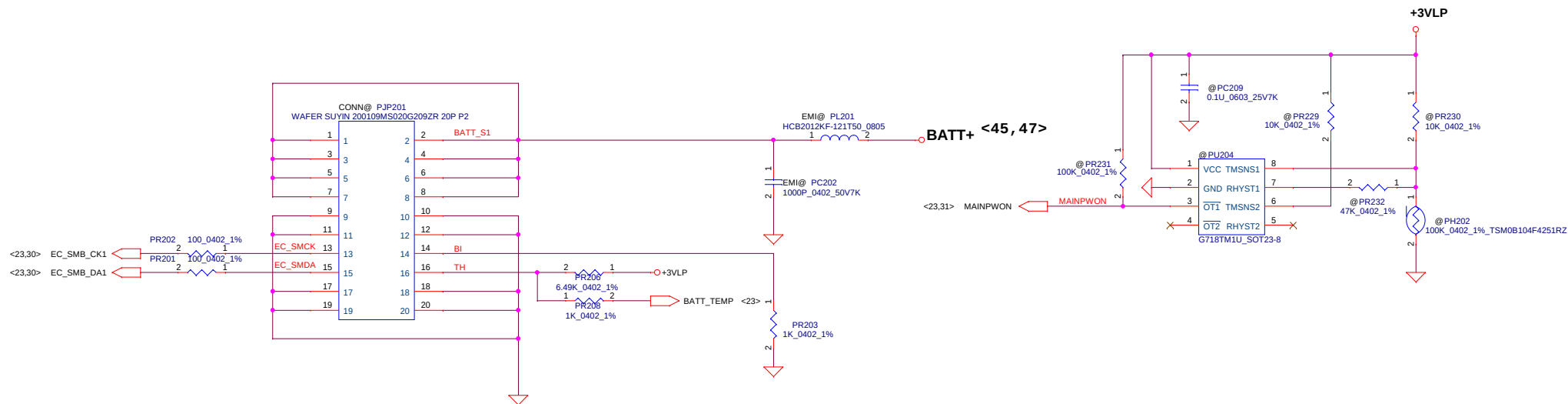
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				Intel BayTrail-M Platform		
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1. Change U8,U57 (SA000028Y10) to SA00006EE00 (S IC AP2821KTR-G1 SOT-23 5P PWR SW)
2. Change U28 to SA000040B30(S IC KB9012QF A4 LQFP 128P KB CONTROLLER)
3. Change U31 to SA000050J00 (S IC APE8875M SO 8P FAN CONTROL)
4. Change Q57,Q58,Q62,Q63,Q64,Q65 to SB00000S700(S TR MESS138W-G 1N SOT323-3)
5. Change D40 to SCS00003500 (S SCH DIO RB751V-40 SOD-323 YEASHIN)
6. Unpop R1025 for +1.8VS leakage
7. Pop R1061 for +1.0VS leakage
8. Change RP53 to R1081,R1082 and change SD_CD PU to +3VS for Card Reader un-plug issue
9. Change R927 to 100k for +3VS power sequence
10. Change R926 to 120k for +5VS power sequence
11. Change R1055 to 82k for +1.8VS power sequence
12. Change R1056 to 47k for +1.35VS power sequence
13. Unpop R786,R787 for cost down RJ45 Conn.
14. Pop C449,C450 for CRT_VSYNC_B reduce noise
15. Change C1003,C1004 to 10P for System 25MHz Crystal fine tune
16. Change C799,C800 to 12P for LAN 25MHz Crystal fine tune
17. Change C1009,C1010 to 15P for System 32.768kHz Crystal fine tune
18. Change C1006 from 0.01U to 0.1U for ESD request
19. ADD C1151,C1152 for CRT flicker
20. Change L31,L32,L49 to 0402 Size
21. Add C1169 0.1uF for ESD request
22. Pop C1007 0.047uF for ESD request
23. 0708:Changg U60 to ME4856_S08(SB00000PZ00)
24. Unpop L49 and Add U65,R1084,R1085,R1087,C1179,C1181 for +1.35VS LDO for CRT
25. Unpop Q71,Q72,R1052,R1053 for power discharge
26. Add C1155,C1156,C1157,C1158,C1159 for ESD request
26. Add C1160~C1167,C1167~C1173 for Debug Port for ESD

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				Size	Document Number	Rev
				B	Bay Trail M LA-A621P	0.3
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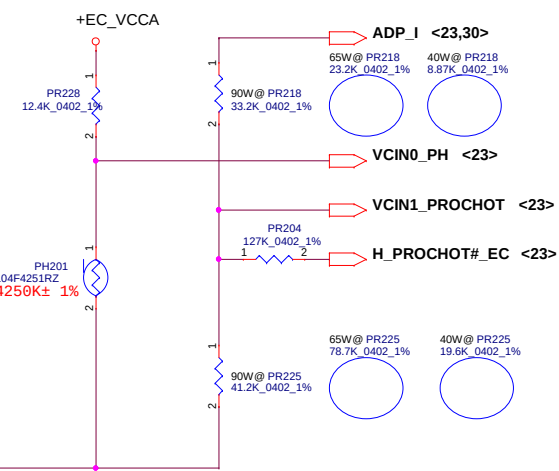
For KB9012 OTP	
92 °C	1.2V, Active
56 °C	2.255V, Recovery

For KB9012 sense 20mΩ	Active	Recovery
40W	50W, 0.7V	40W, 0.7V
65W	84W, 1.2V	56W, 1.2V
90W	117W, 1.2V	77W, 1.2V

PH201 under CPU bottom side :
 CPU thermal protection at 92 degree C (shutdown)
 Recovery at 56 degree C

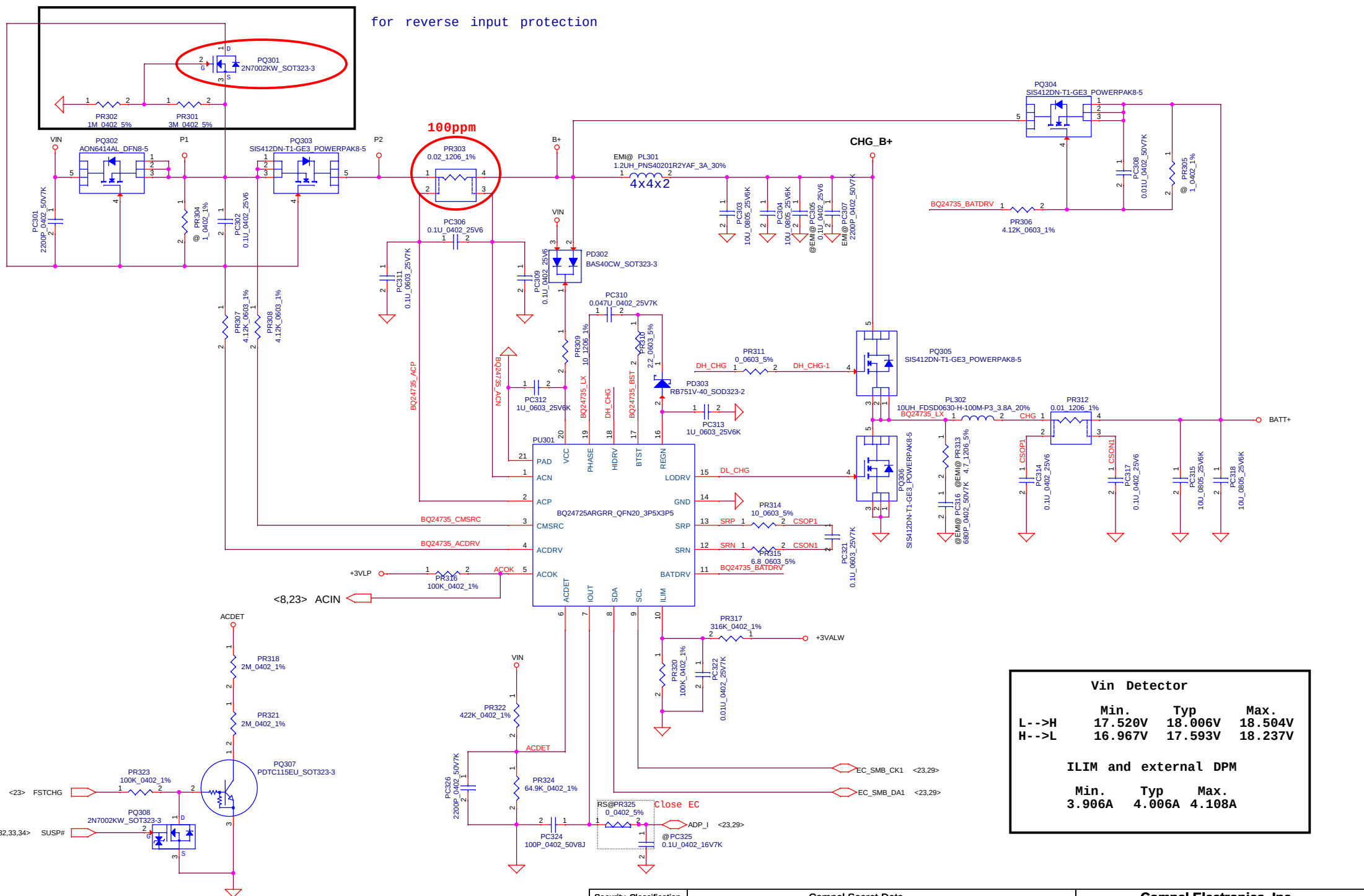
For 65W adapter==>action 70W , Recovery 54W
 For 90W adapter==>action 97W , Recovery 75W

<23> ECAGND



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				Size	Document Number	Rev
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for reverse input protection

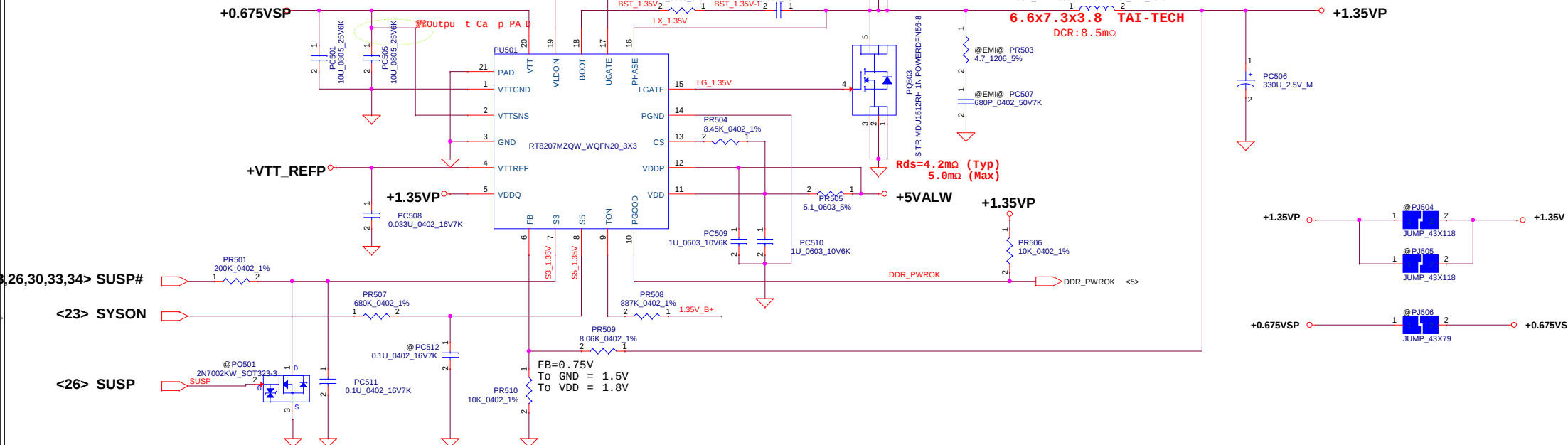


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$+1.35VP$
 $I_{peak} = \max\{0.7 \cdot I_{budget}, 1st + 2nd \text{ max loading}\}$
 $I_{peak} = \max\{12.34 \cdot 0.7, 4.2 + 8.14\}$
 $I_{peak} = 12.34A$; $1.2I_{peak} = 14.808A$; $I_{max} = 8.638A$
 $1/2\Delta I = 0.7353A$ (F=300K Hz)
 $PR504 = (1.2I_{peak} - 1/2\Delta I) \cdot R_{ds(on)}(max) \cdot 1.2/9uA = 8.45Kohm$
 choose $PR504 = 8.45Kohm$ (for safety $> 1.2I_{peak}$)
 $R_{ds(on)} = 5.0m \text{ ohm}(max)$; $R_{ds(on)} = 4.2m \text{ ohm}(typical)$
 $I_{limit_min} = (8.366K \cdot 9uA) / (5.0m \cdot 1.2) = 15.058A$
 $I_{limit_max} = (8.535K \cdot 11uA) / (4.2m \cdot 1.2) = 22.352A$
 $I_{ocp} = I_{limit} + 1/2\Delta I$; $I = 15.79A - 23.09A$
 $I_{ocp}(min) > 1.2I_{peak}$

2011/9/19

OVP=110% 115% 120%

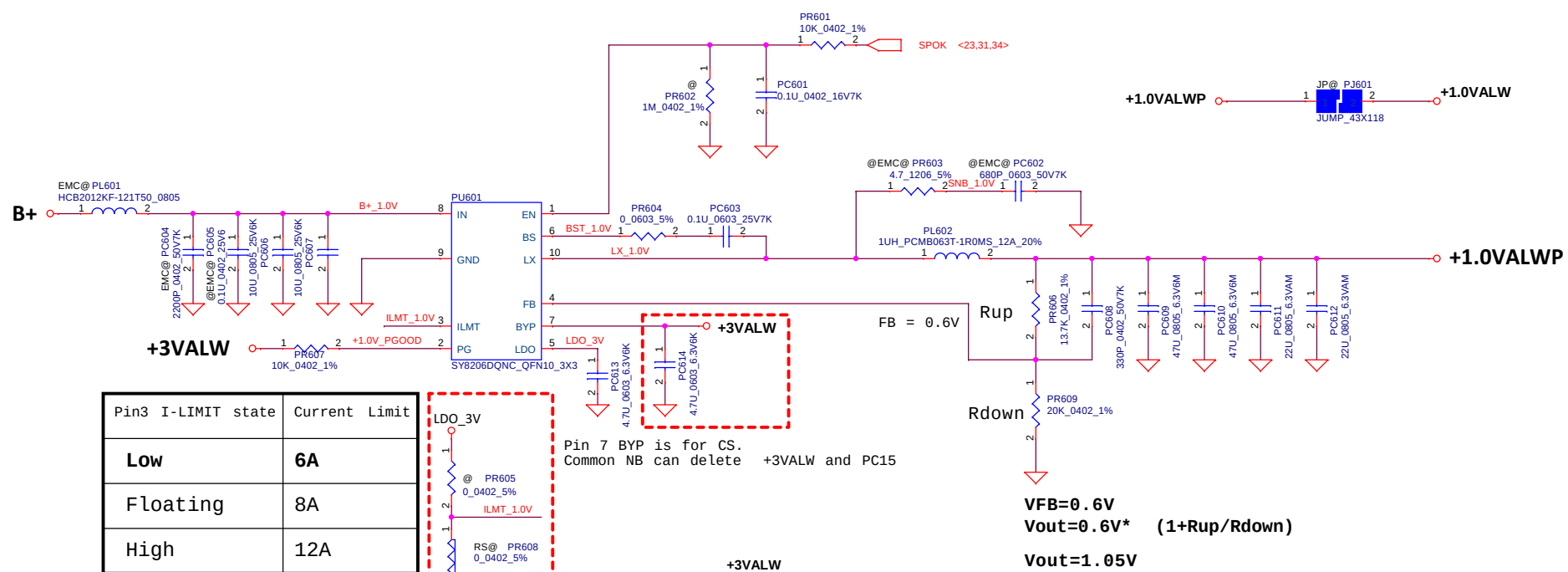


STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

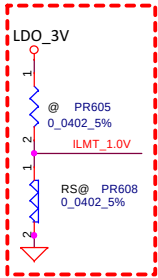
Note: S3 - sleep ; S5 - power off

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								Size	Document	Number	Rev 0.
								Bay Trail M LA-A621P			
								Date: Tuesday, September 03, 2013			
								Sheet	32	of	37

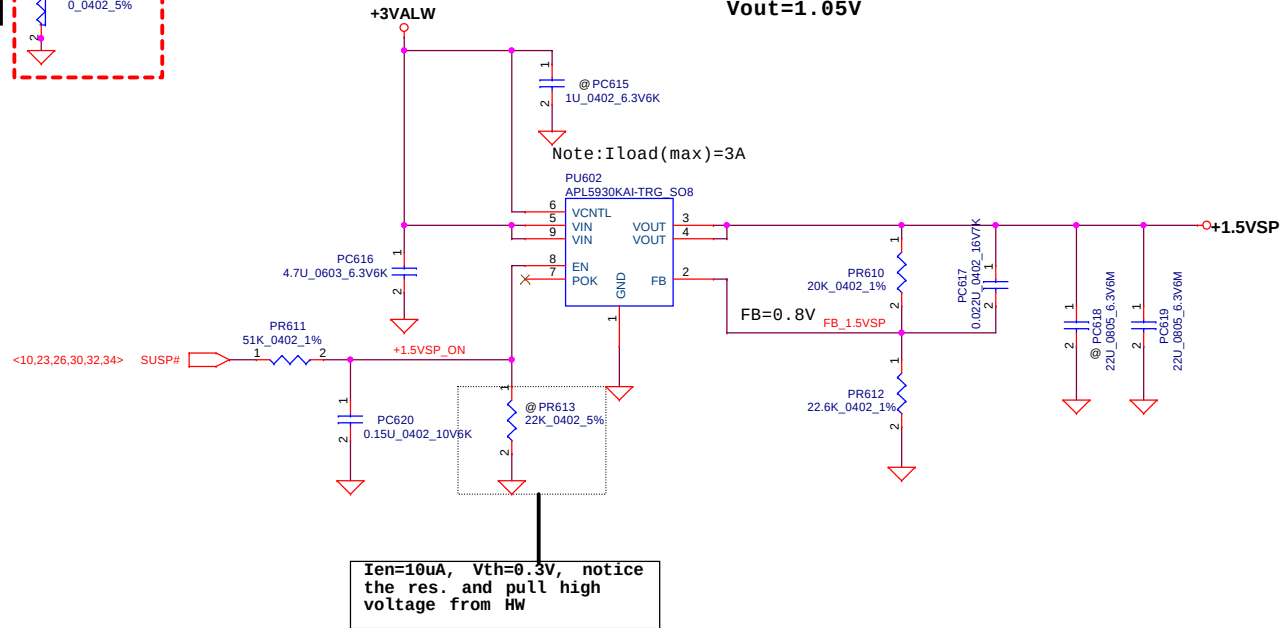
Notes: Use VCCSA_SEL to switch High & Low Level for VDD[1]



Pin3 I-LIMIT state	Current Limit
Low	6A
Floating	8A
High	12A

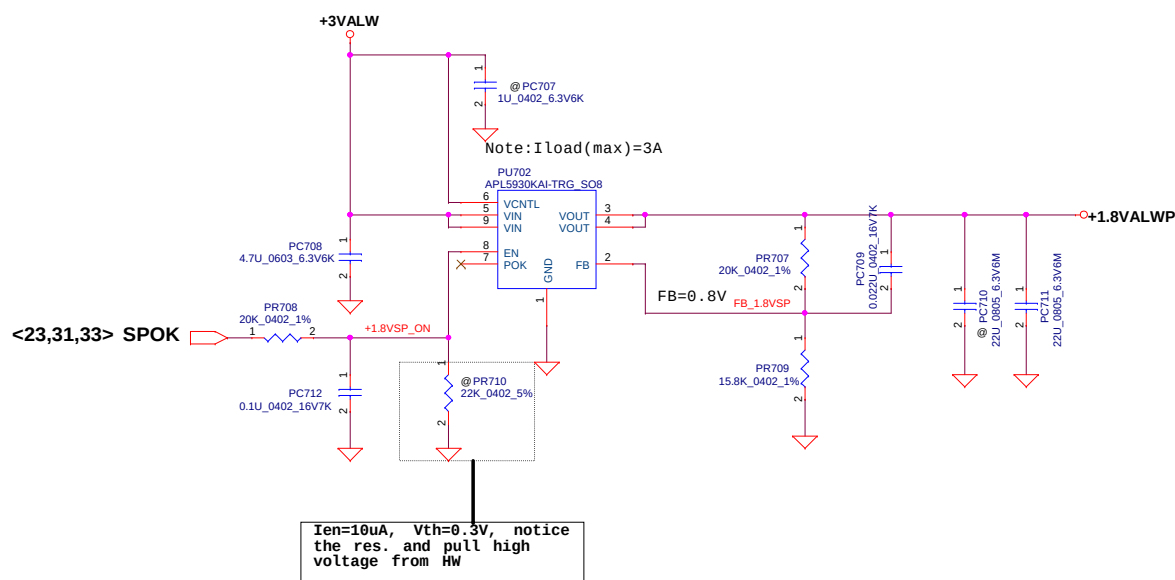
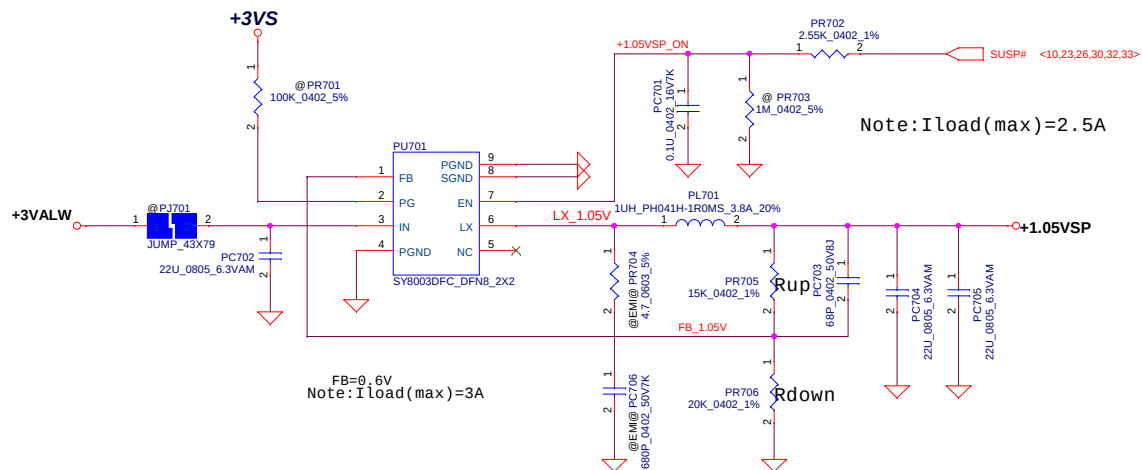


Pin 7 BYP is for CS.
 Common NB can delete +3VALW and PC15



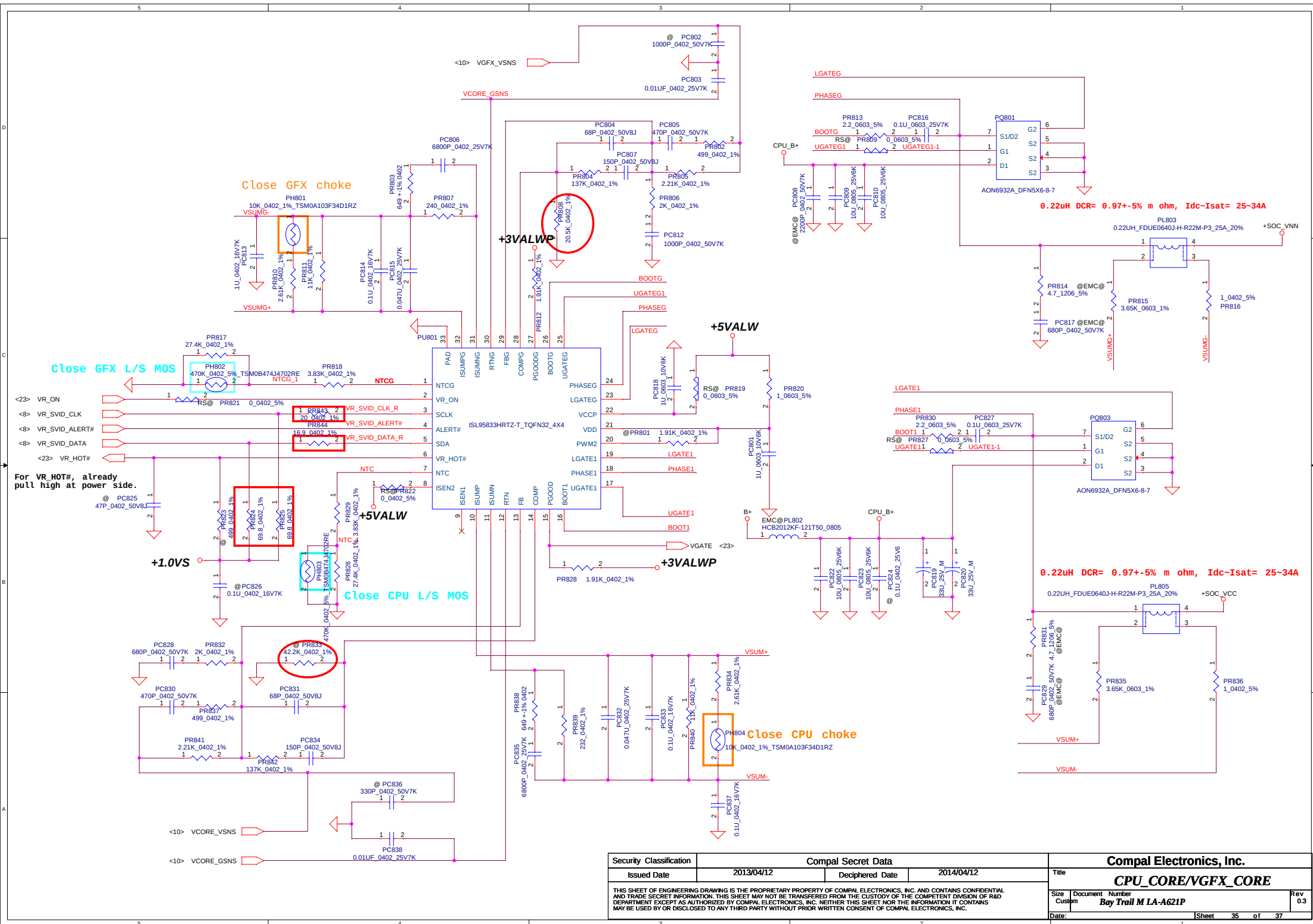
Ien=10uA, Vth=0.3V, notice the res. and pull high voltage from HW

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										Size Document Number	
										Customer	
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Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

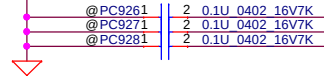
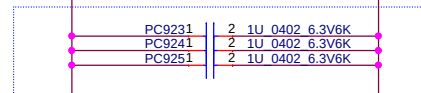
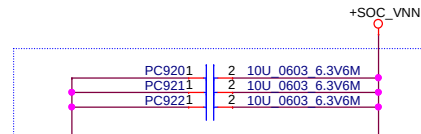
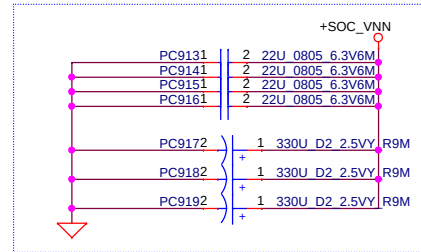
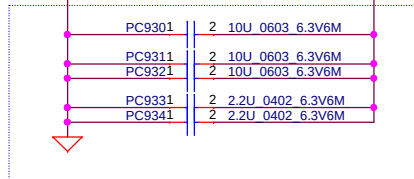
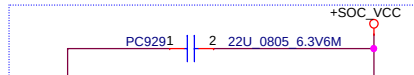
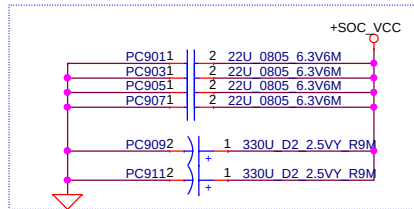
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Output Cap

Package Edge Cap

Back Side Cap



Output Cap

Package Edge Cap

Back Side Cap

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Tune Power sequence by HW request	1.05VS & 1.5VS sequence meet SPEC			Change PR702 to 2.5K, PR611 to 51K, PC620 to 150nF	07/05	DVT
2		Change 1.35V voltage close to 1.35		32	Change PR509 to 7.68K	07/05	DVT
3	EMI request	Cut-in EMI solution		30	Change PR310 to 2.2	07/05	DVT
4		Approve CPU transient		CPU	Change PC931, PC932 from 4.7uF to 10uF Change PR839 from 240 to 232 Add PR808 to 20.5K Change PC812 from 330pF to 1000pF Change PC828 from 470pF to 680pF	07/24	DVT
5							
6					Add PR411, PR413	12/22	DVT2
7					Add PC609 into 4700P		
8	+1.05V ripple close upper and mean too low	Adjust output voltage and add Cff			Change PR608 from 133K to 127K	12/22	DVT2
9		Improve CPU transient character		40	Unpop PC926	01/09	DVT2
10		Tune sequence		35	Change PC428 from 4700p to 10n, PC427 from 0.047u to 6.8n	02/04	PVT
11		0 ohm reduce			Change PR507,PR513,PR523 to R-pad	02/22	PVT
12		Provide 3/5V PG signal to EC		35	Add PR416	02/22	PVT
13	ESD request			32	Add PC101 into 0.1uF	02/26	PVT
14	ESD request			36	Add PC521, PR503, PC507	02/26	PVT
15		Use HW to control VCIN1 function		33	Add PR204	03/05	PVT
12							
13							
14							
15							
16							
17							

Delete
08/14

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