

Compal Confidential

Model Name : V5WE2/T2/C2 (EA/EG/BA50_HW)

File Name : LA-9531P

Compal Confidential

EA50_HW M/B Schematics Document

Intel Shark Bay ULT (Hasswell + Lynx Point-LP)

AMD MARS / SUN

2012-12-03

REV : 0 . 2

Part Number	Description
DA60000XL00	PCB 0VR LA-9531P REV0 M/B

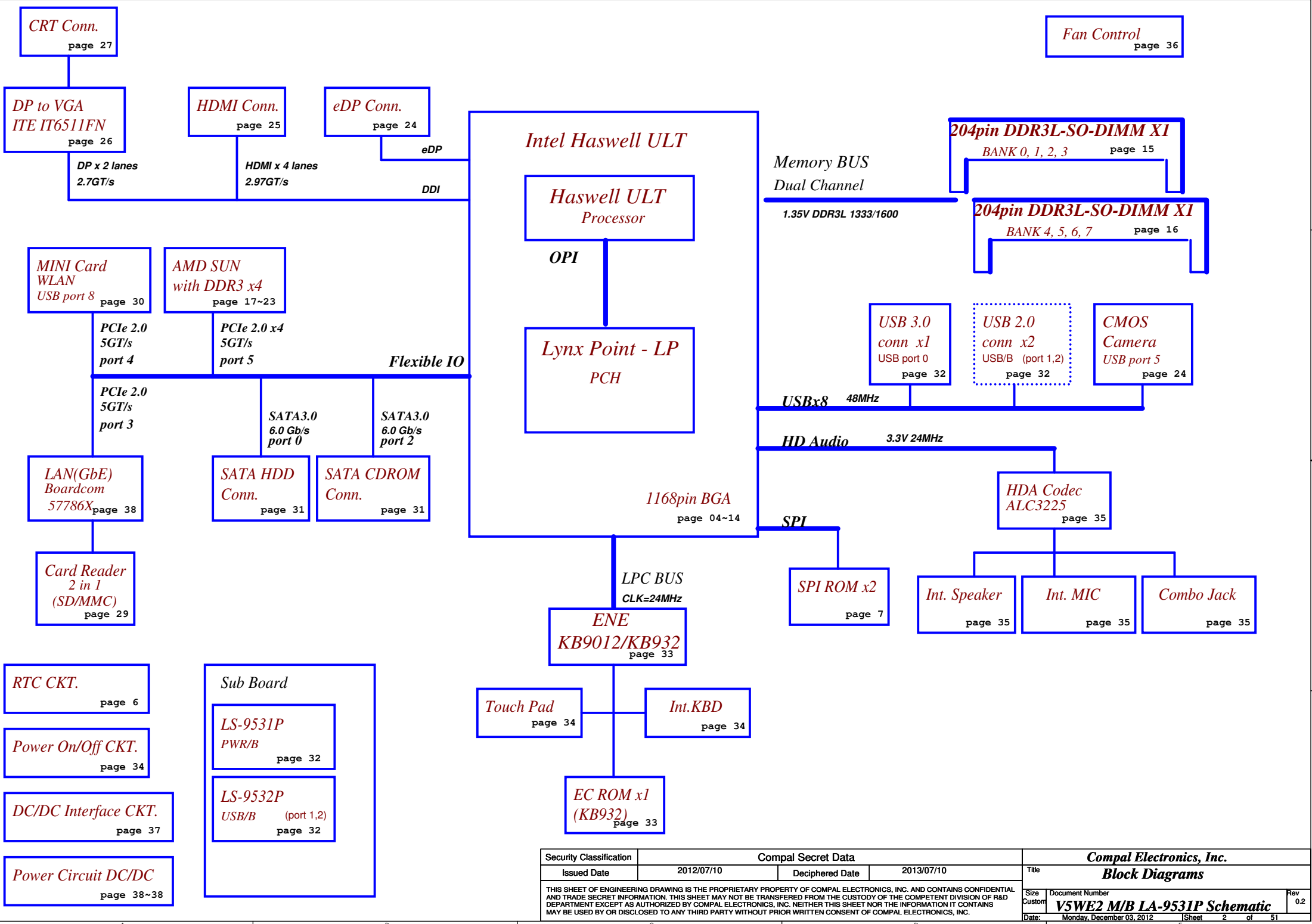
V5WE2_PCB

PWZZZ 45PWR@

Part Number	Description
DC30100NK00	CONN SET 0VR DC-MB 2DW2024-015121F DIS

V5WE2_DCIN_Cable

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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title Cover Page	
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								Block Diagrams			
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSDGPUP switched power rail for GPU	ON	OFF	OFF
+0.95VSDGPU	+0.95VSDGPUP to +0.95VSDGPU switched power rail for CPU	ON	OFF	OFF
+1.35V	+1.35VP to +1.35V power rail for DDRIIIIL	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VSDGPUP to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	+3VS to 1.8V switched power rail to CPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU switched power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X

EC SM Bus2 address

Device	Address
On Board Thermal Sensor	0100 110x
VGA Internal Thermal Sensor	0100 000x
G Sensor	0011 000x

PCH SM Bus address

Device		Address	
ChannelA	DIMM0	1001 000x	JDIMM1
ChannelB	DIMM1	1001 010x	JDIMM2

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

USB Port Table

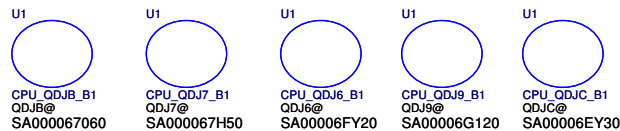
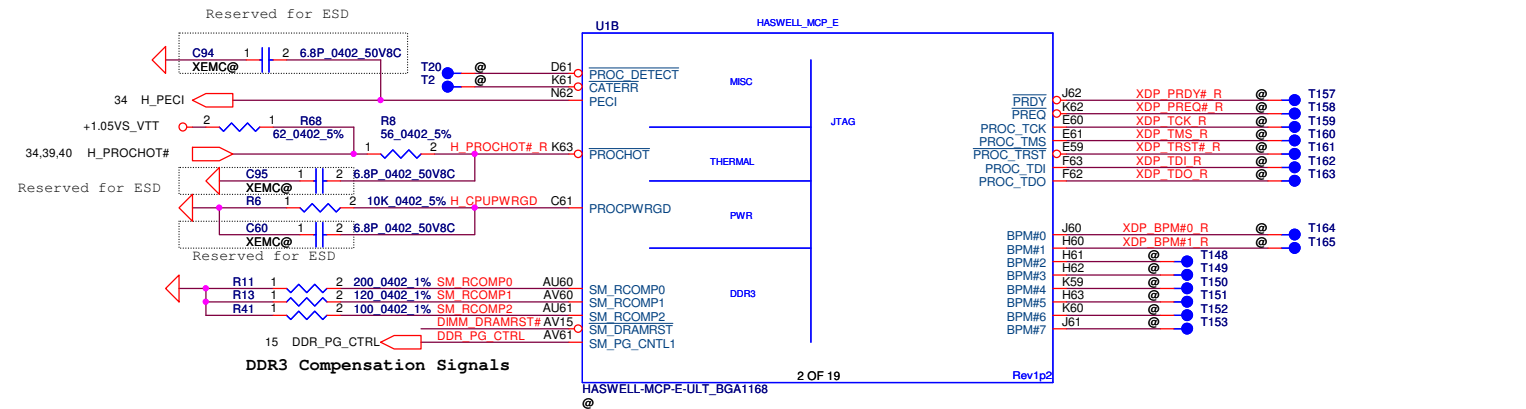
USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port(Left 3.0)
	1	USB Port(Right 2.0)
	2	USB Port(Right 2.0)
	3	
	4	Mini Card (WLAN+BT)
	5	
	6	
	7	Camera

USB 3.0	Port	
XHCI	0	USB Port(Left 3.0)
	1	
	2	
	3	

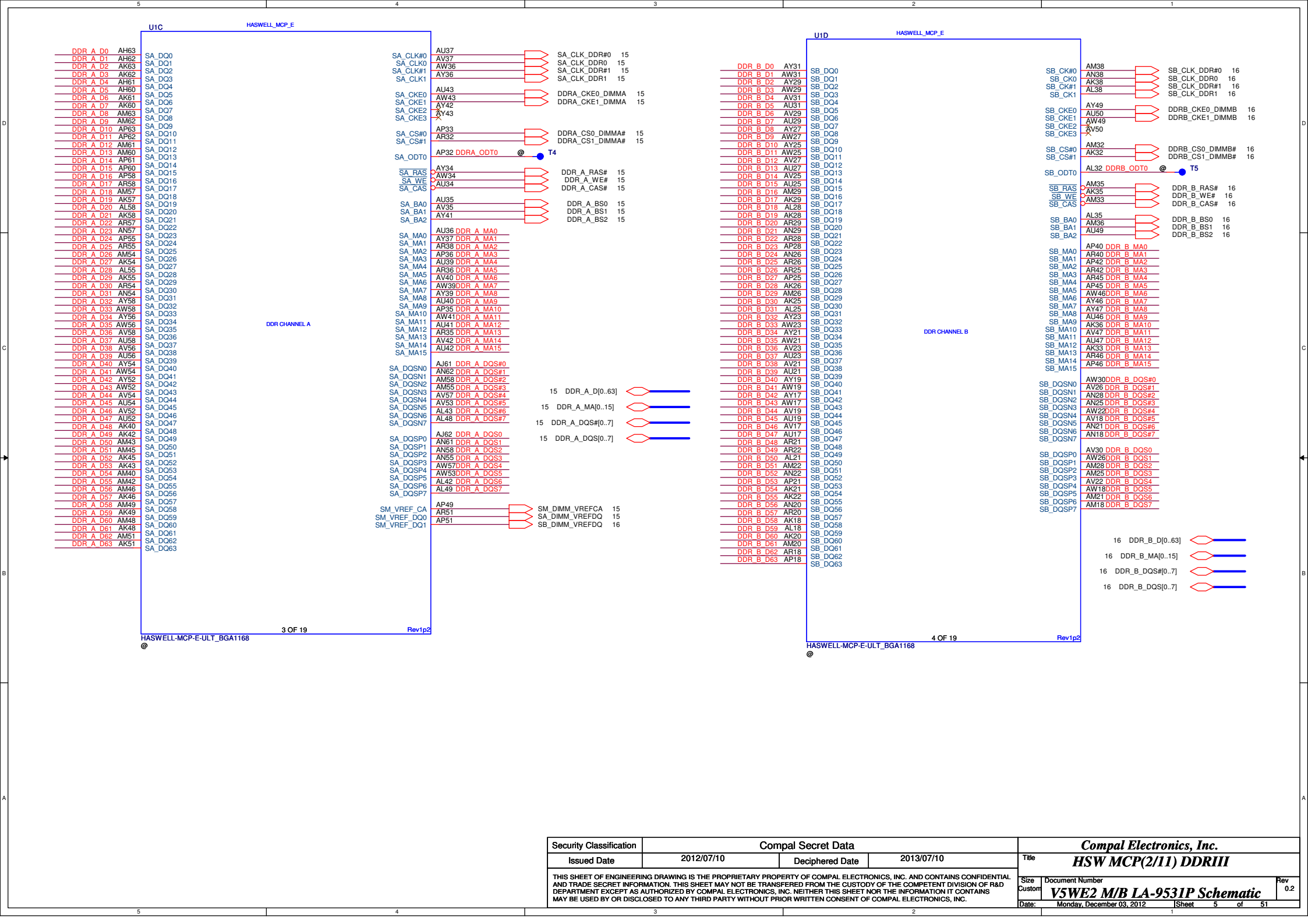
BTO Option Table

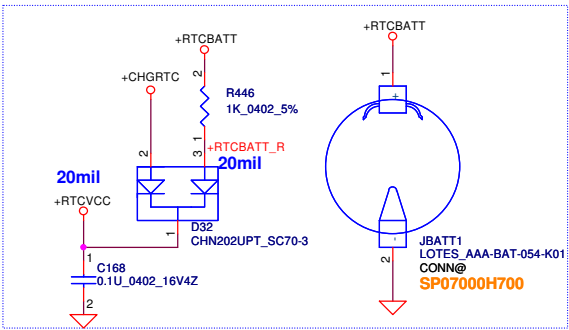
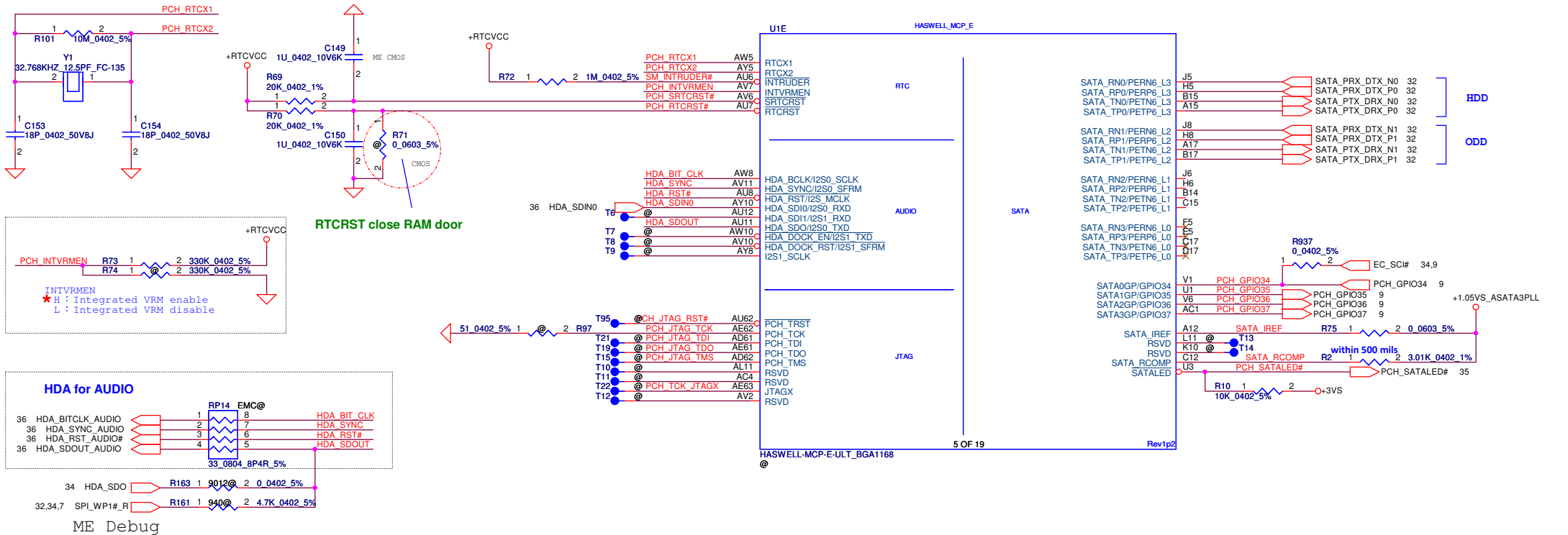
[illegible]

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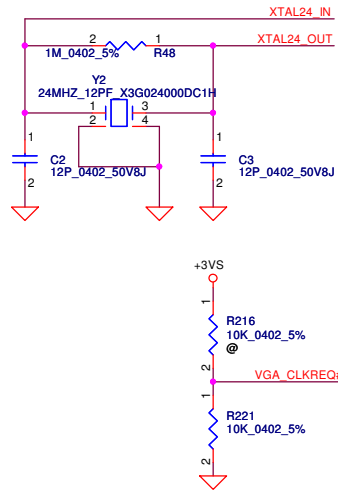


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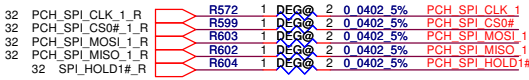
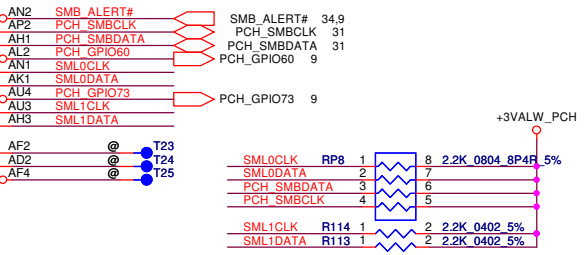
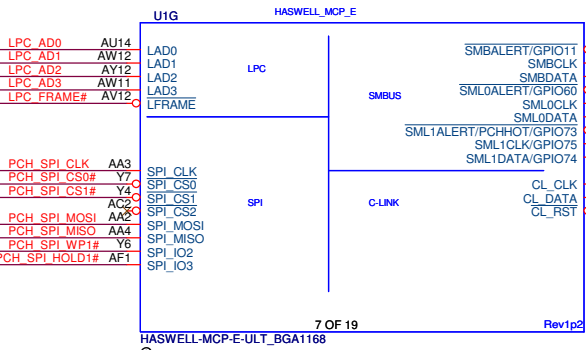
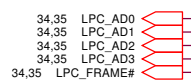
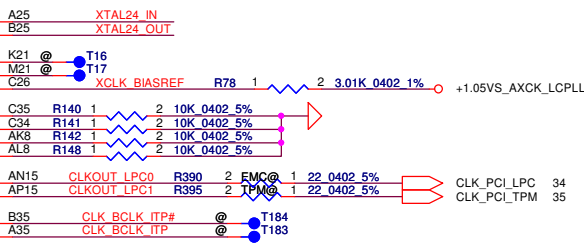
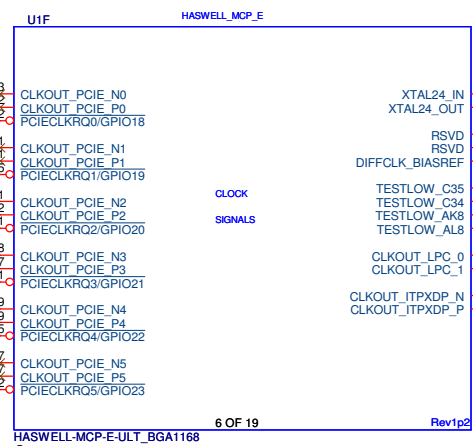
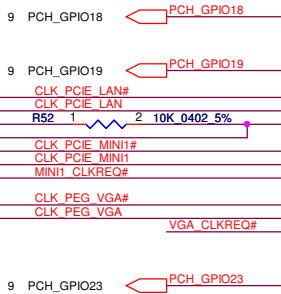




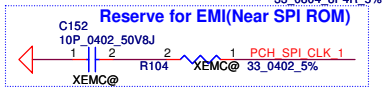
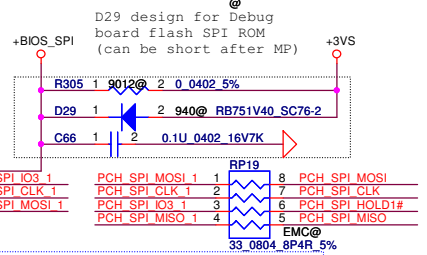
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2013/07/10		Title		H5WE2 M/B LA-9531P Schematic	
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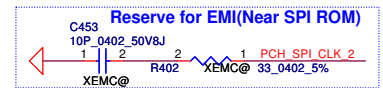
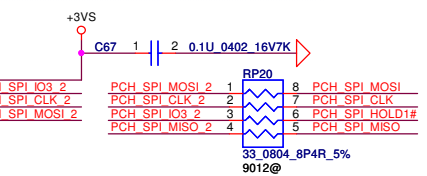
PCIE LAN
WLAN



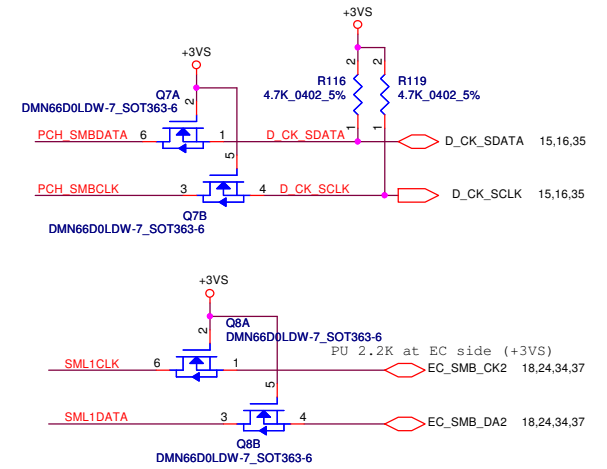
SPI ROM (2MByte)



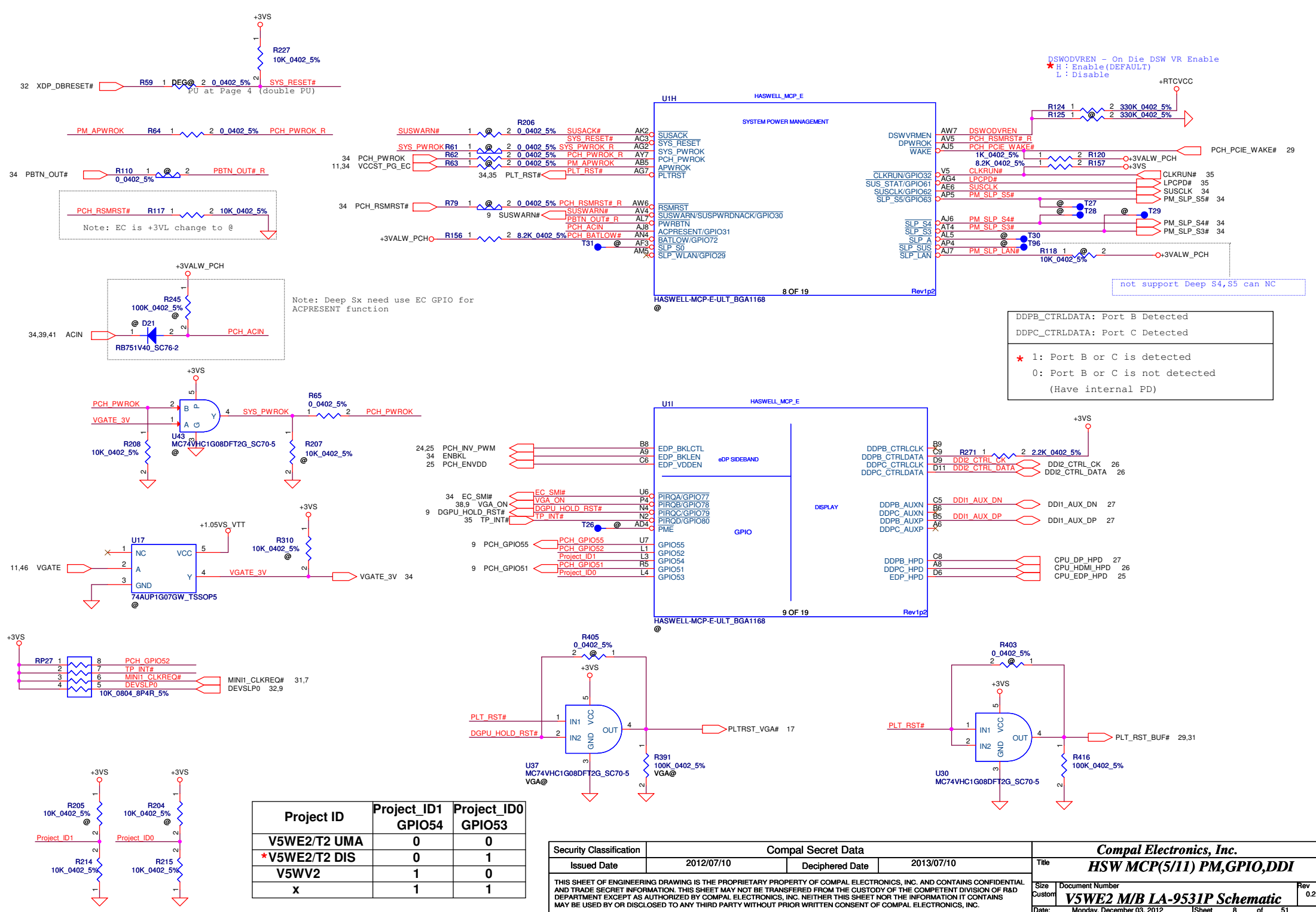
SPI ROM (4MByte)



SPI ROM (8MByte for Chrome)



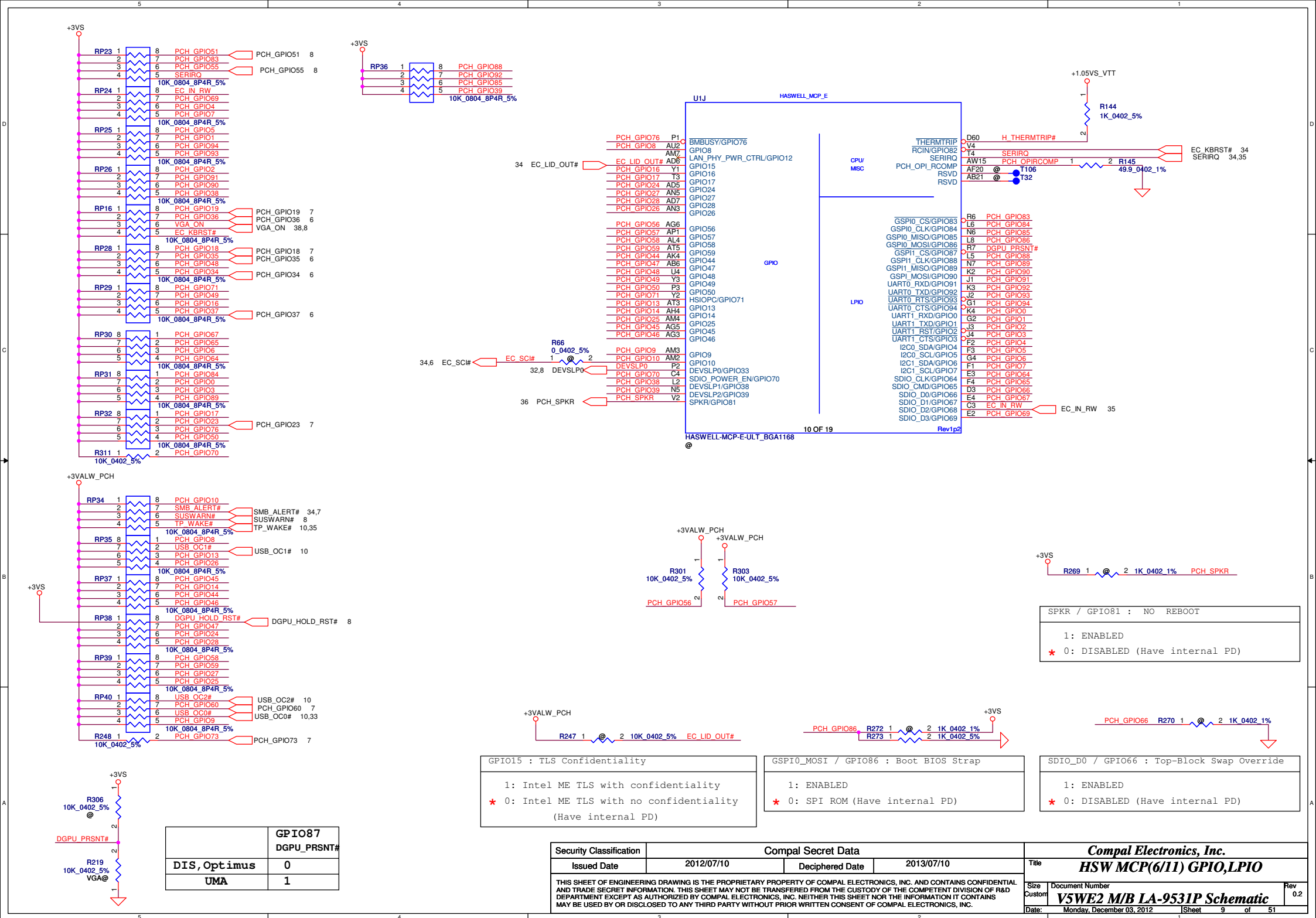
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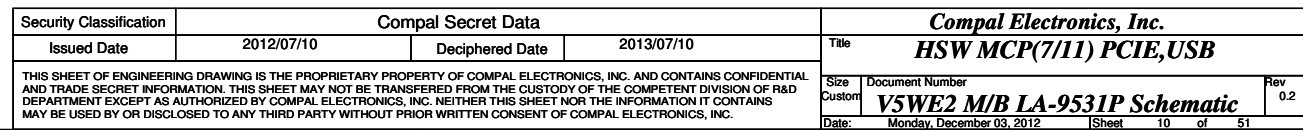


Project ID	Project_ID1 GPIO54	Project_ID0 GPIO53
V5WE2/T2 UMA	0	0
*V5WE2/T2 DIS	0	1
V5WV2	1	0
X	1	1

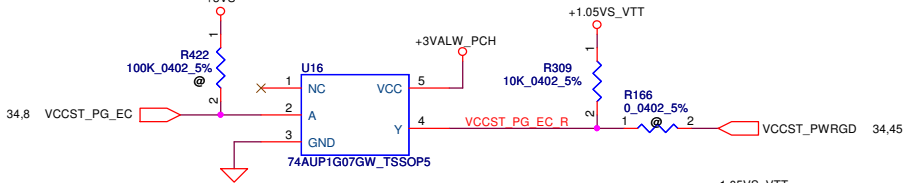
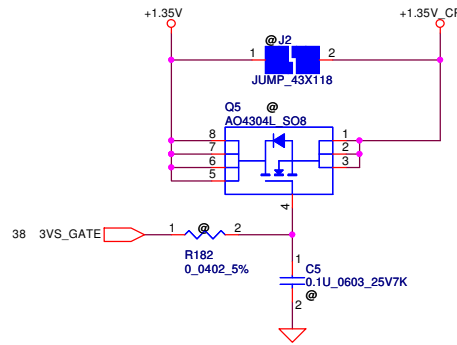
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Compal Electronics, Inc.			
HSW MCP(5/11) PM,GPIO,DDI			
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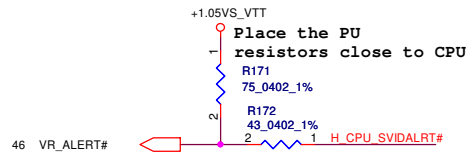




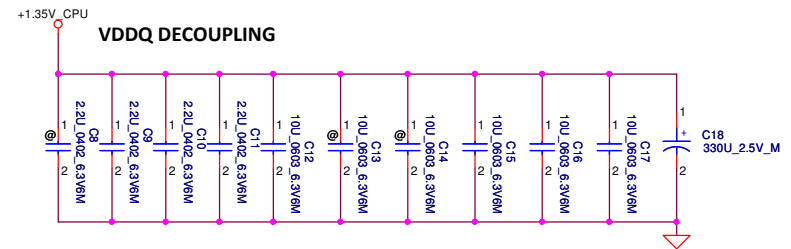
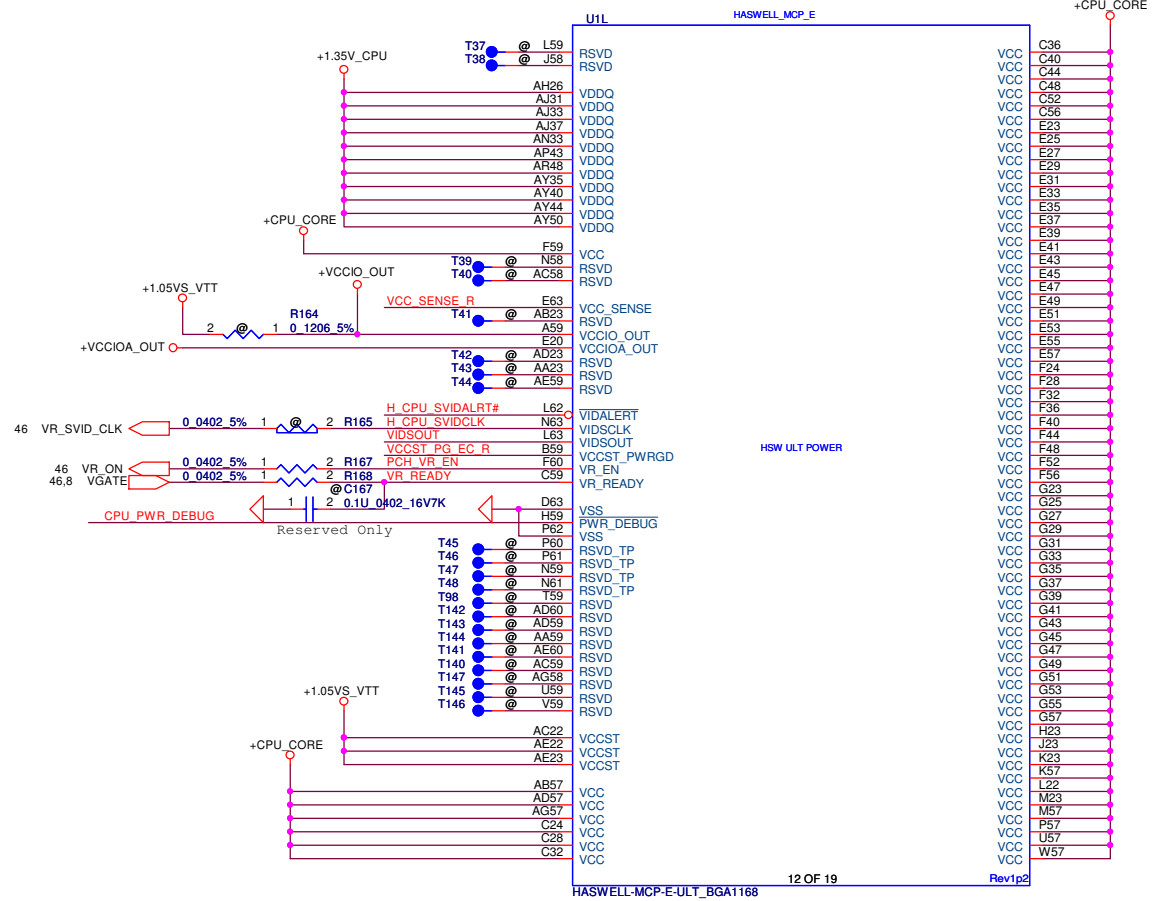
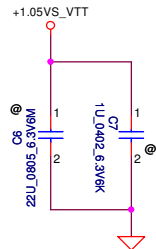
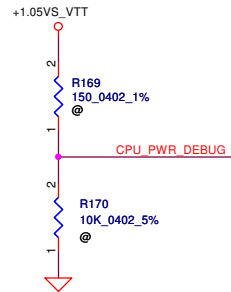
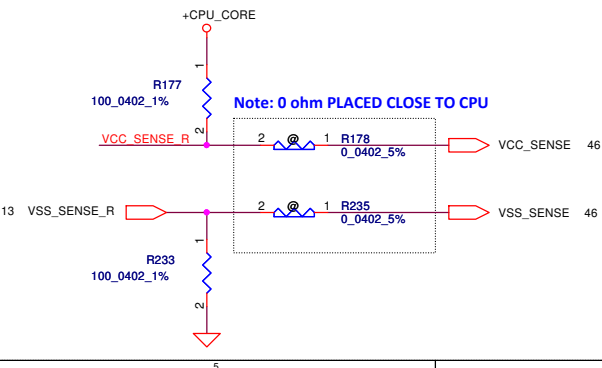
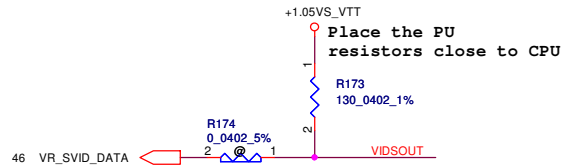
Shark Bay ULT have internal gate for VDDQ



SVID ALERT

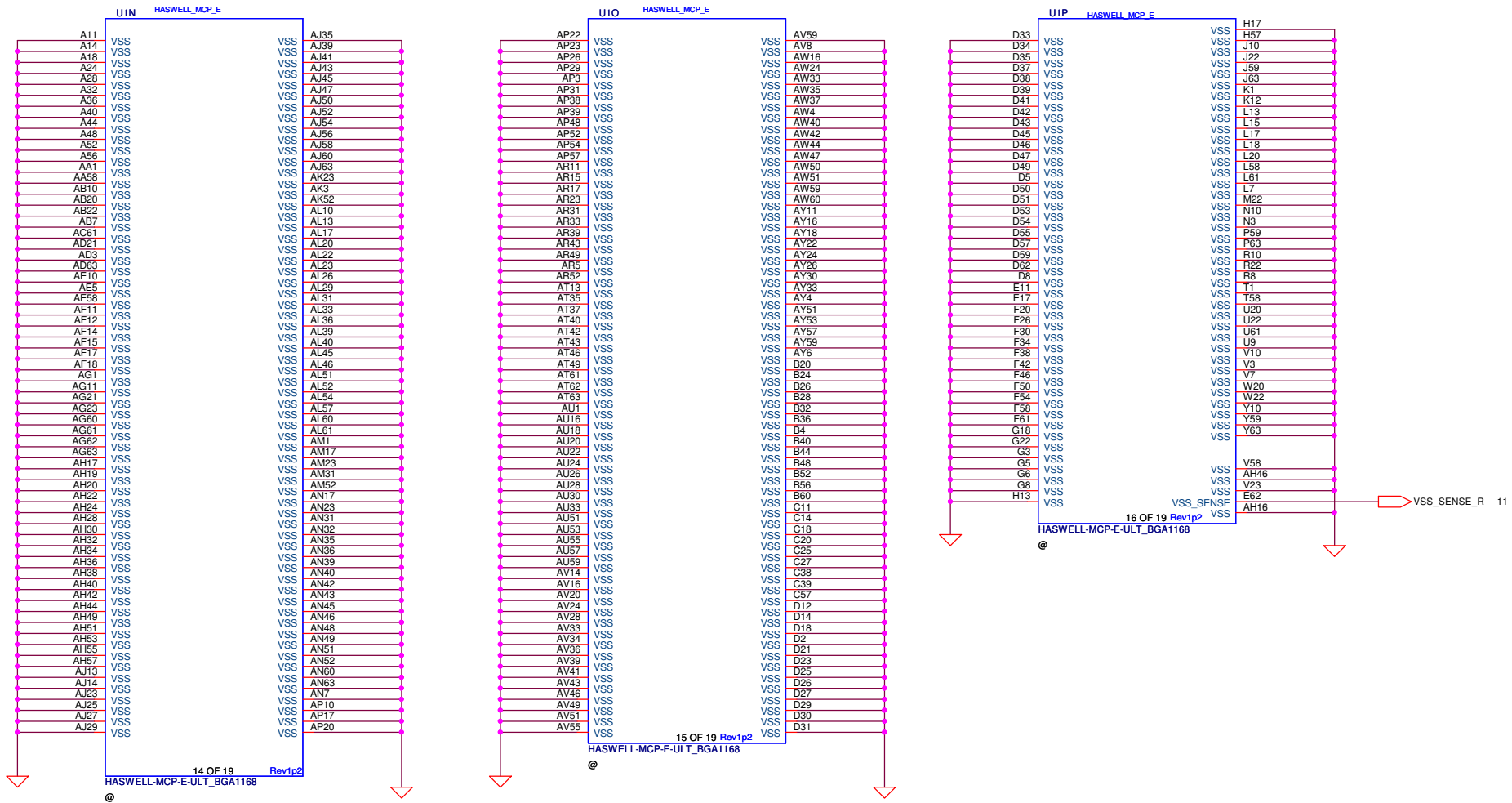


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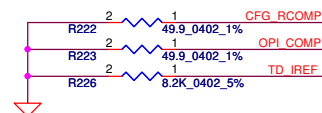
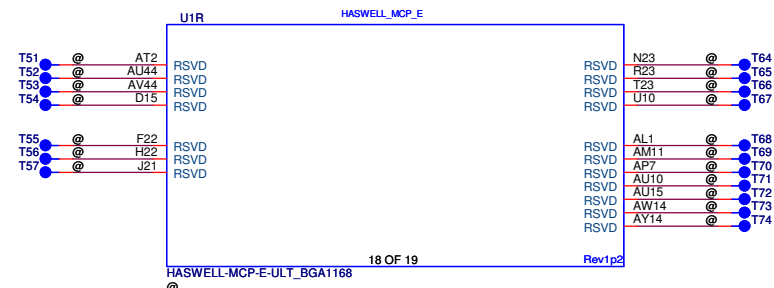


+1.35V : 470UF/2V/7343 * 2
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

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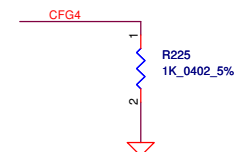


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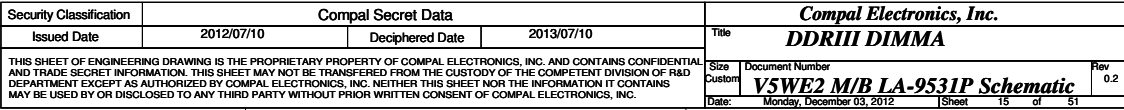


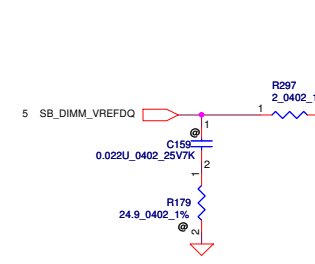
A circuit diagram showing a resistor R224 (1K_0402_1%) connected between the CFG3 pin and ground. The resistor is represented by a blue zigzag line with terminals 1 and 2. Terminal 1 is connected to the CFG3 pin, and terminal 2 is connected to a ground symbol (a triangle with a circle inside). The text "R224 1K_0402_1%" and a circled "a" are placed next to the resistor.

Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR

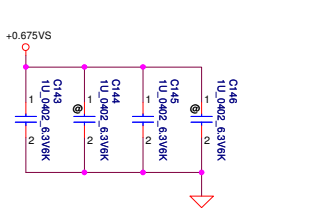
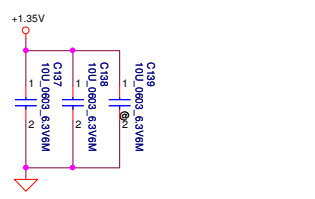
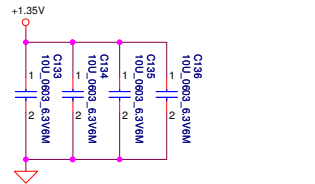
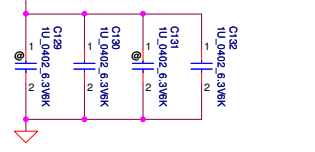


Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



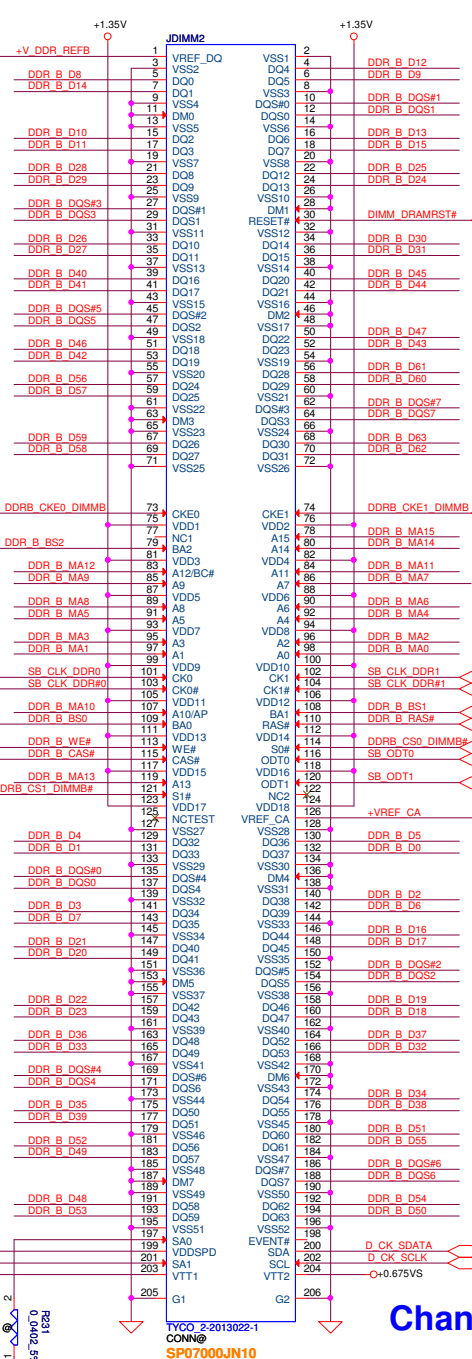
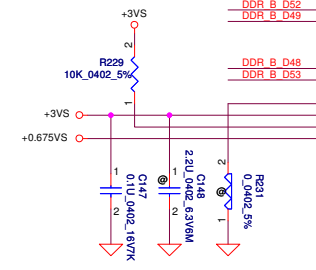


Layout Note:
Place near JDIMM1

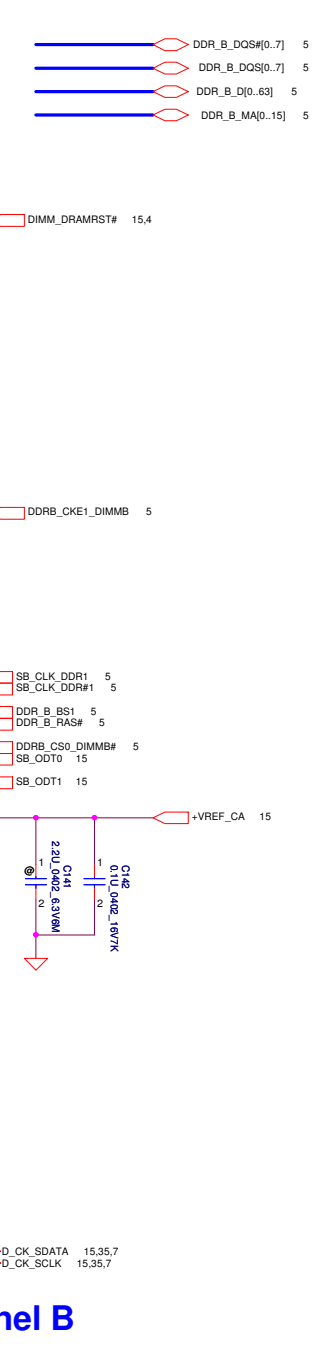


Layout Note:
Place near JDIMM1.203,204

All VREF traces should have 10 mil trace width



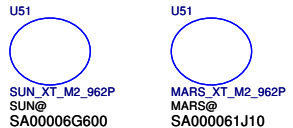
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DIMM_2 STD H:4mm



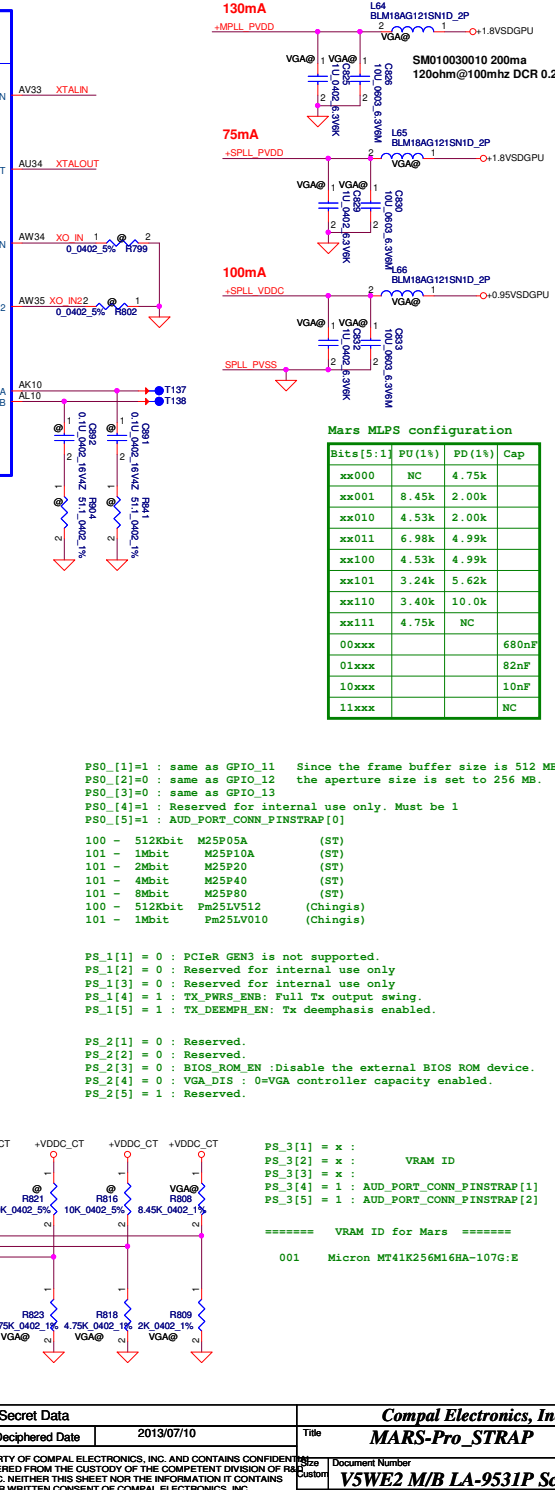
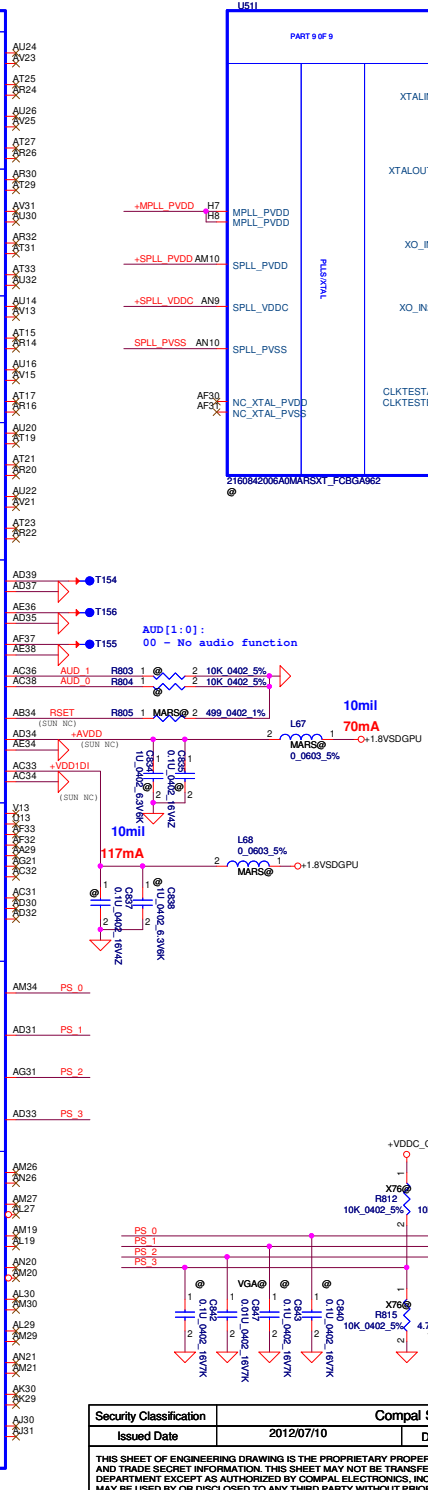
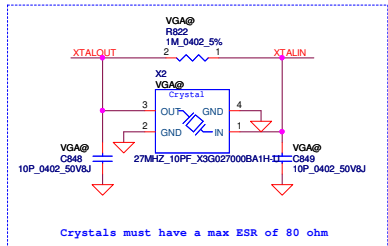
Channel B



A	B	C	D	E
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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	MARS-Pro_PCIE	
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				Date:	Monday, December 03, 2012	Sheet 17 of 51



Bits[5:1]	PU(1%)	PD(1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.98k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC

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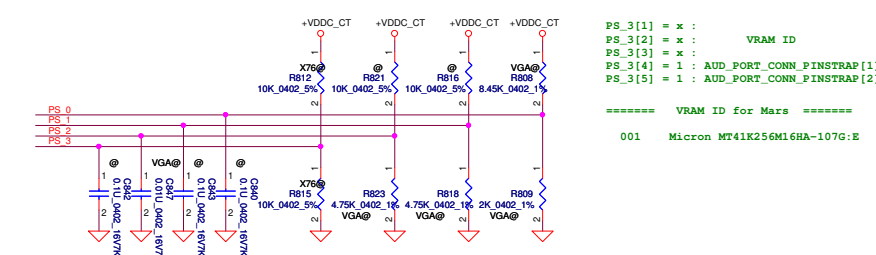
PS0_1[1]=0 : same as GPIO_11      Since the frame buffer size is 512 MB
PS0_2[2]=0 : same as GPIO_12      the aperture size is set to 256 MB.
PS0_3[3]=0 : same as GPIO_13
PS0_4[4]=1 : Reserved for internal use only. Must be 1
PS0_5[5]=1 : AUD_F0RN_CONN_F1NSTRAP[0]

100 - 512Kbit M25P05A      (ST)
101 - 1Mbit M25P10A      (ST)
101 - 2Mbit M25P20      (ST)
101 - 4Mbit M25P40      (ST)
101 - 8Mbit M25P80      (ST)
100 - 512Kbit Pm25LV512  (Chingis)
101 - 1Mbit Pm25LV010    (Chingis)

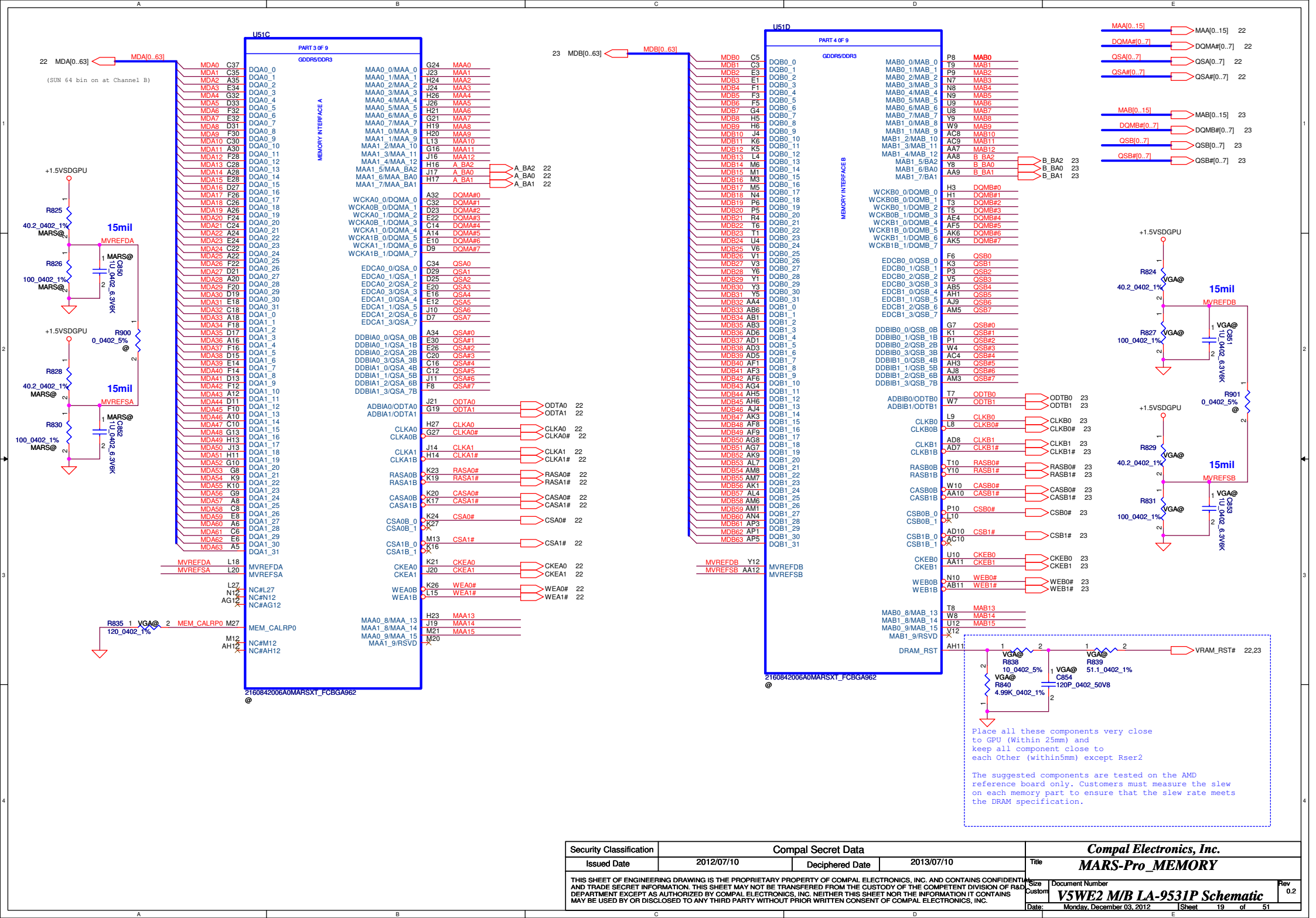
PS_1[1] = 0 : PCIe GEN3 is not supported.
PS_1[2] = 0 : Reserved for internal use only
PS_1[3] = 0 : Reserved for internal use only
PS_1[4] = 1 : TX_PRRS_ENB: Full Tx output swing
PS_1[5] = 1 : TX_DEEMPH_EN: Tx deemphasis enabled.

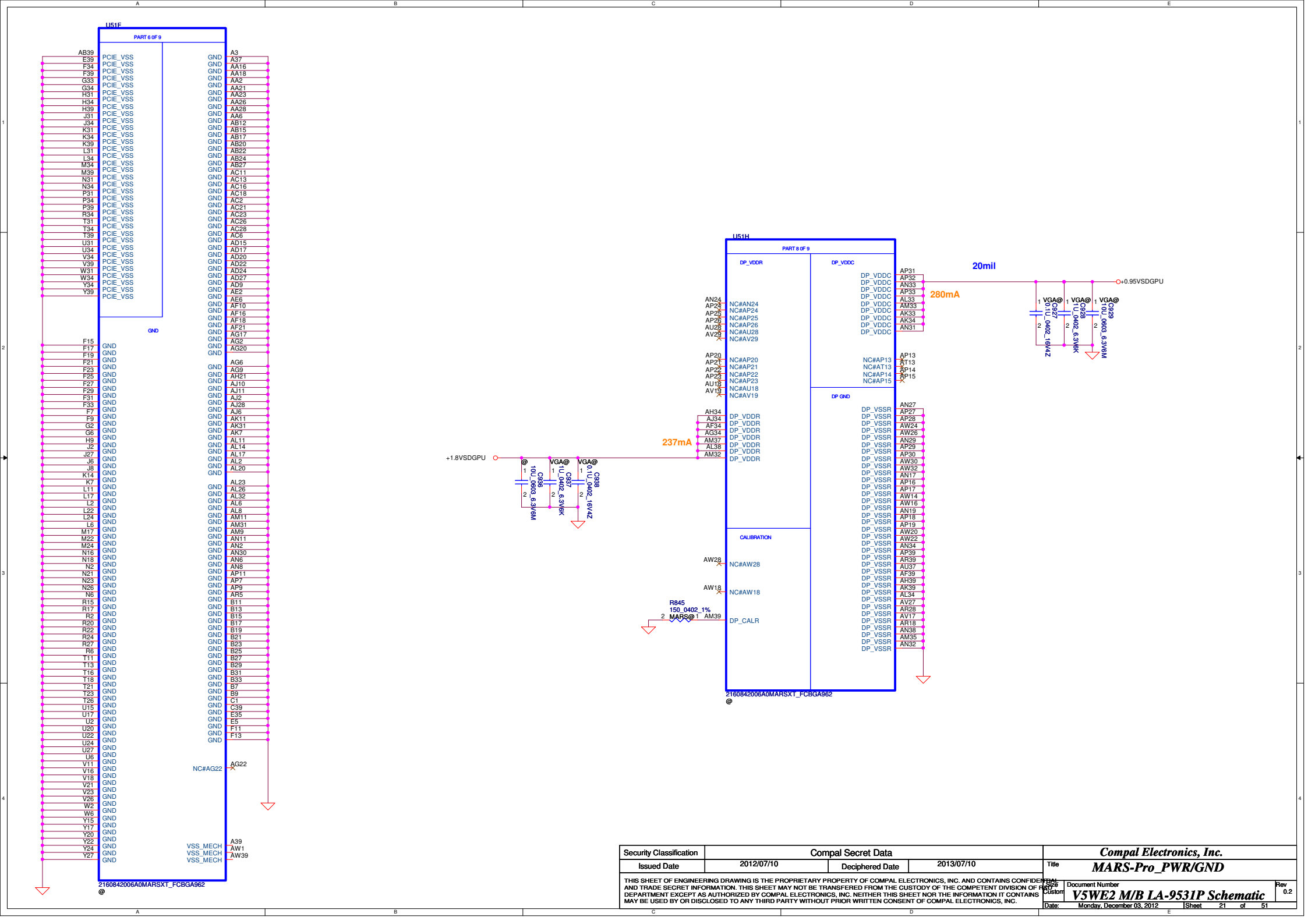
PS_2[1] = 0 : Reserved.
PS_2[2] = 0 : Reserved.
PS_2[3] = 0 : BIOS_ROM_EN :Disable the external BIOS ROM device.
PS_2[4] = 0 : VGA_DIS = 0:VGA controller capacity enabled.
PS_2[5] = 1 : Reserved.

```



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				V5WE2 M/B LA-9531P Schematic Date: Monday, December 03, 2012 Sheet 18 of 51		0.2

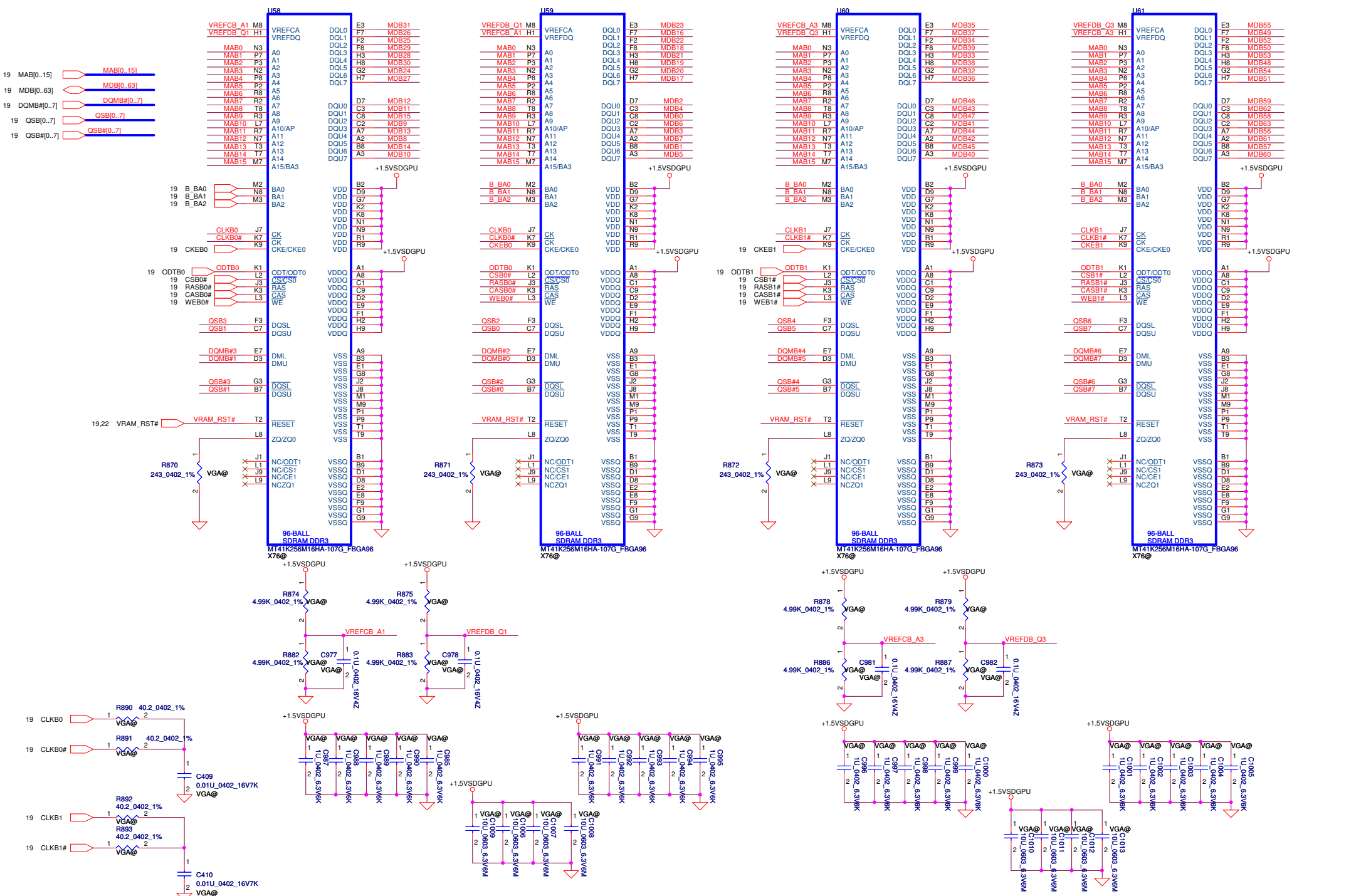


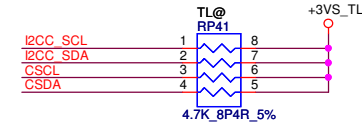
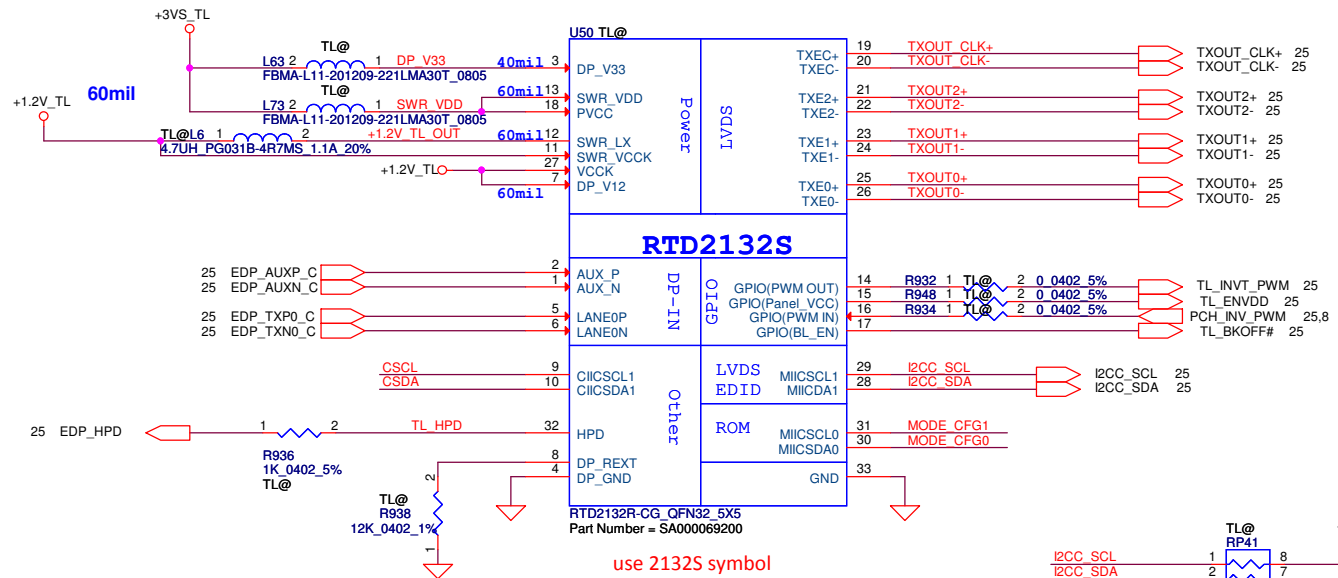
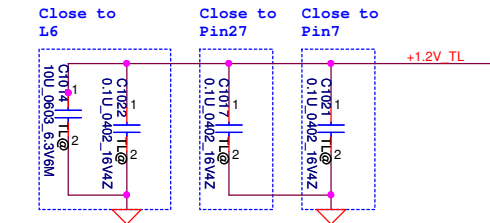
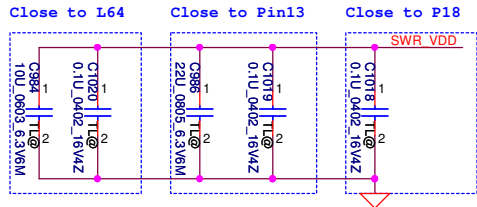
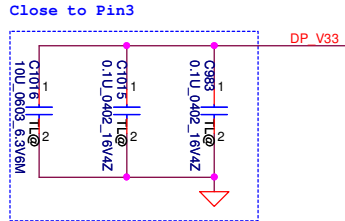
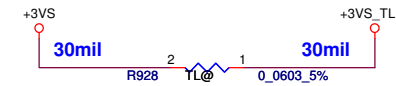


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				Customer		
				Date:	Monday, December 03, 2012	Sheet 22 of 51
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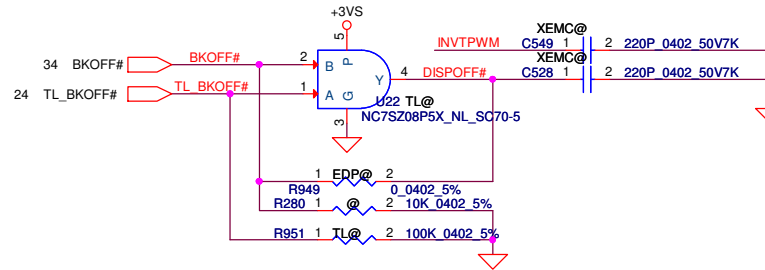
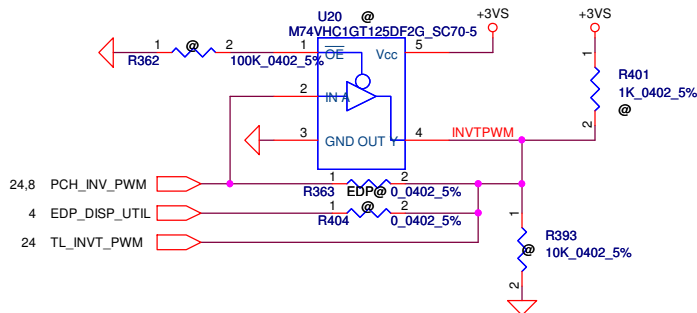
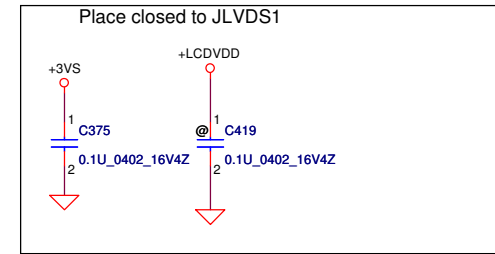
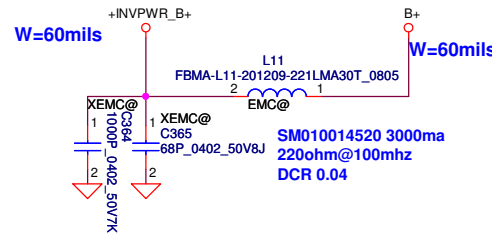
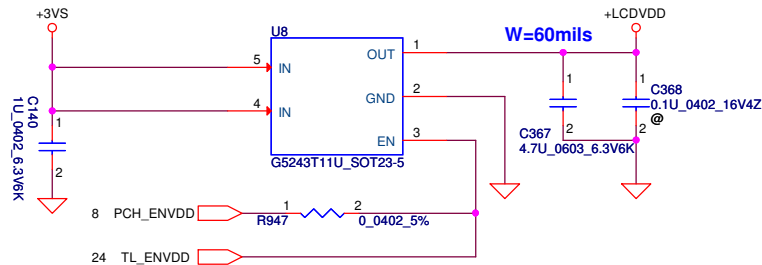




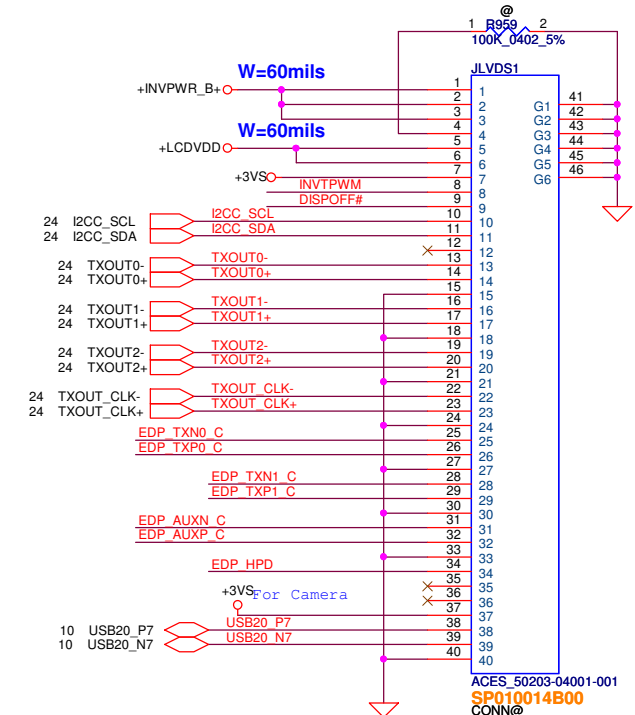
MODE_CFG0(PIN30)		
	0	1
MODE_CFG1(PIN31)	0	EP MODE
	1	ROM ONLY MODE*
		EEPROM MODE

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						B	V5WE2 M/B LA-9532P Schematic	
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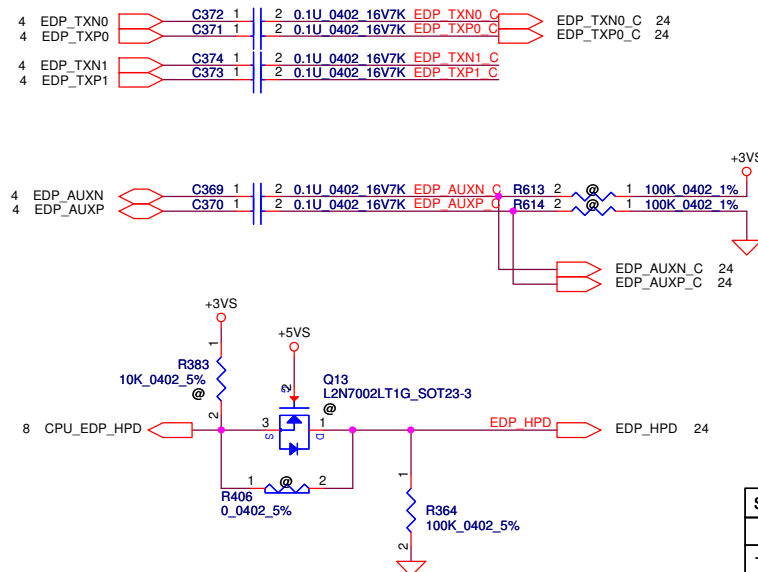
LCD POWER CIRCUIT



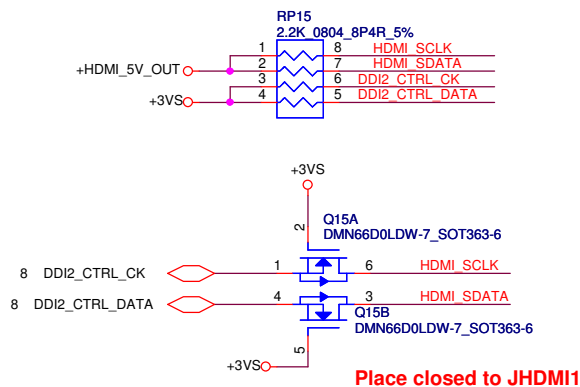
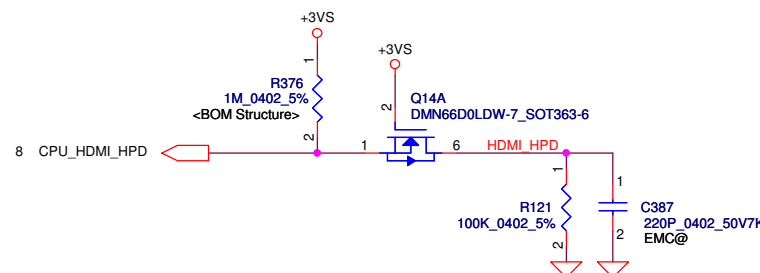
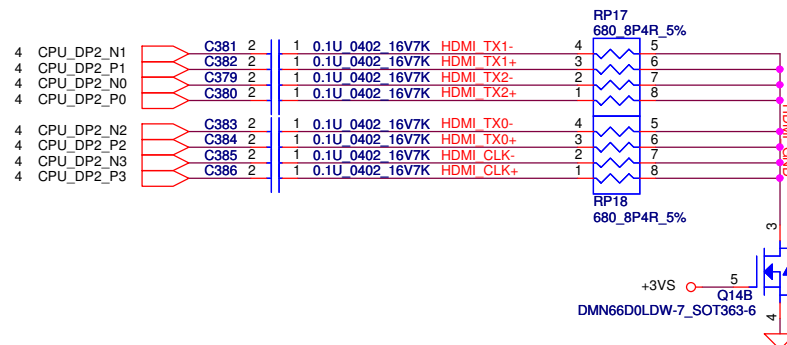
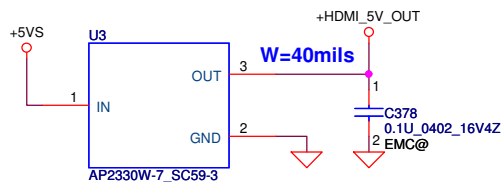
LCD/ LED PANEL Conn.



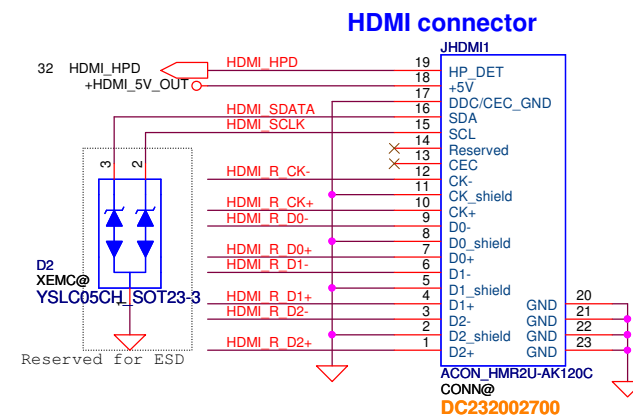
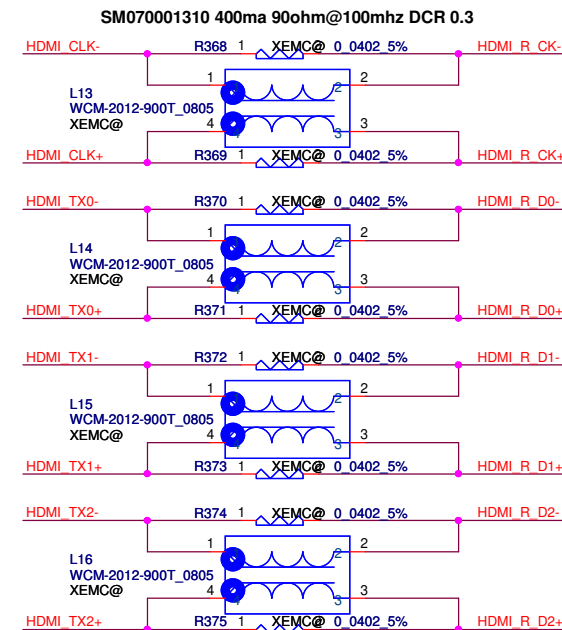
eDP



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								eDP Connector	
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						Custom	V5WE2 M/B LA-9531P Schematic		
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Place closed to JHDMI1

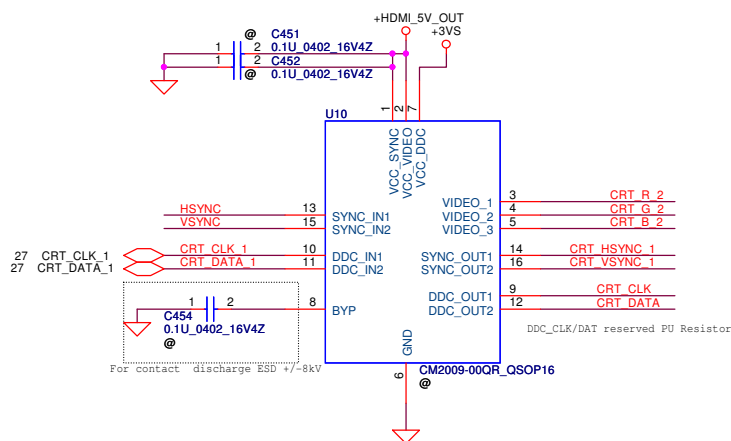
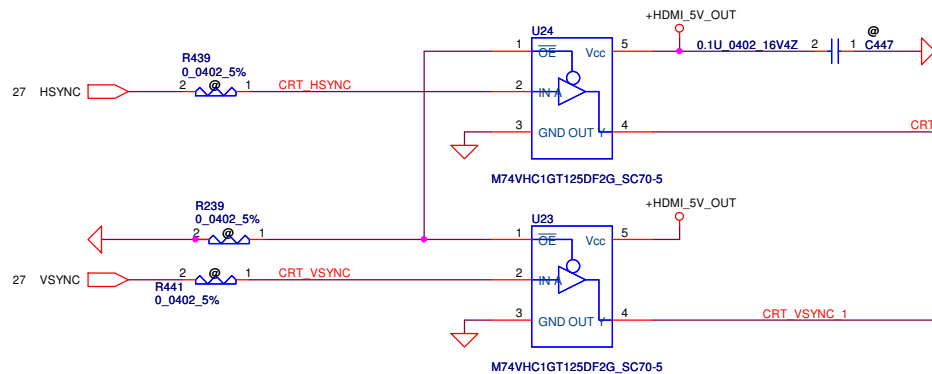
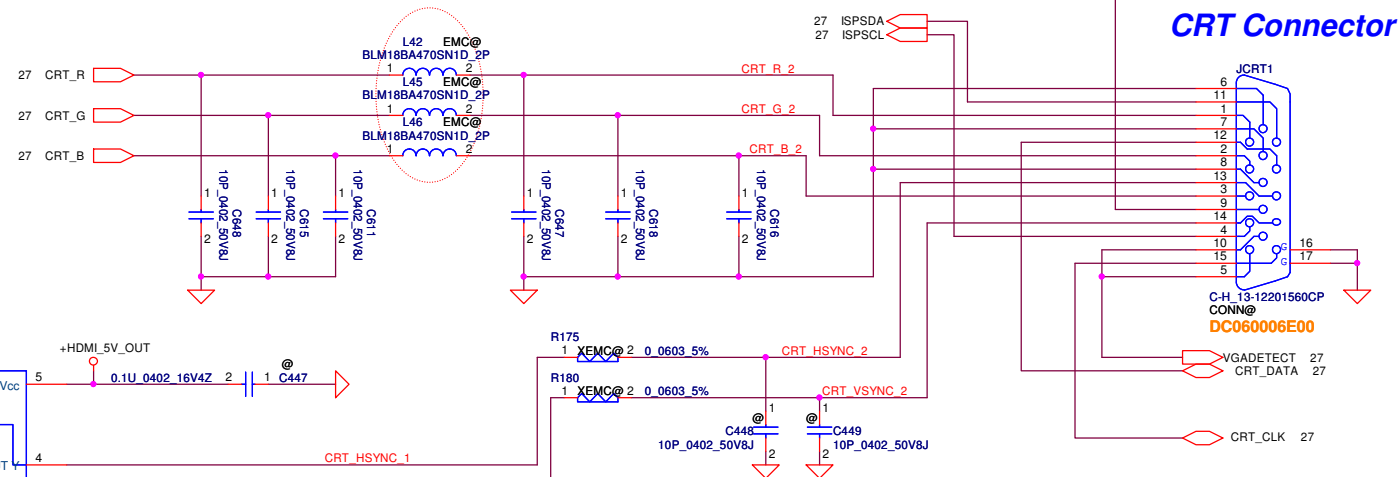


HDML ROYALTY
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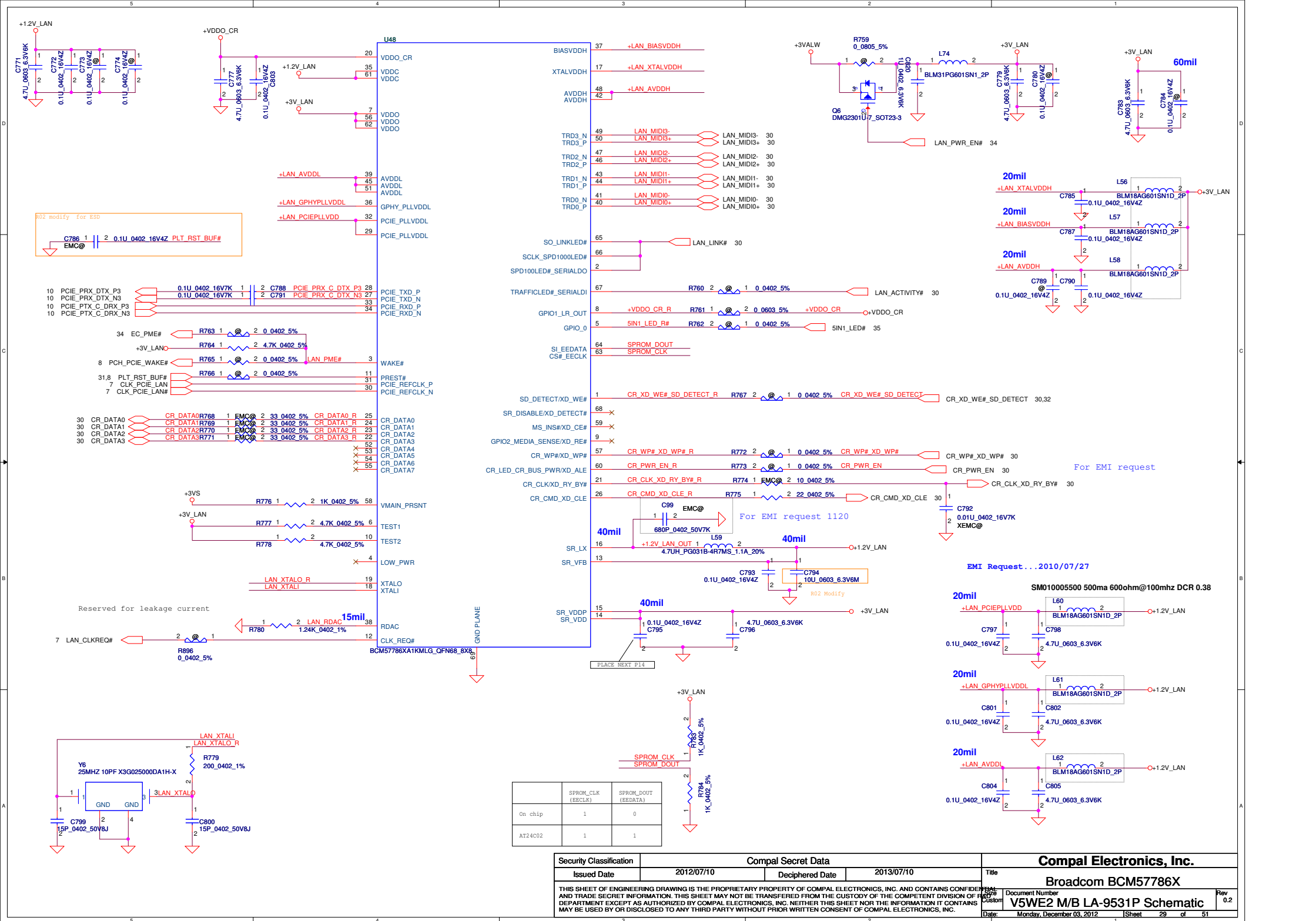
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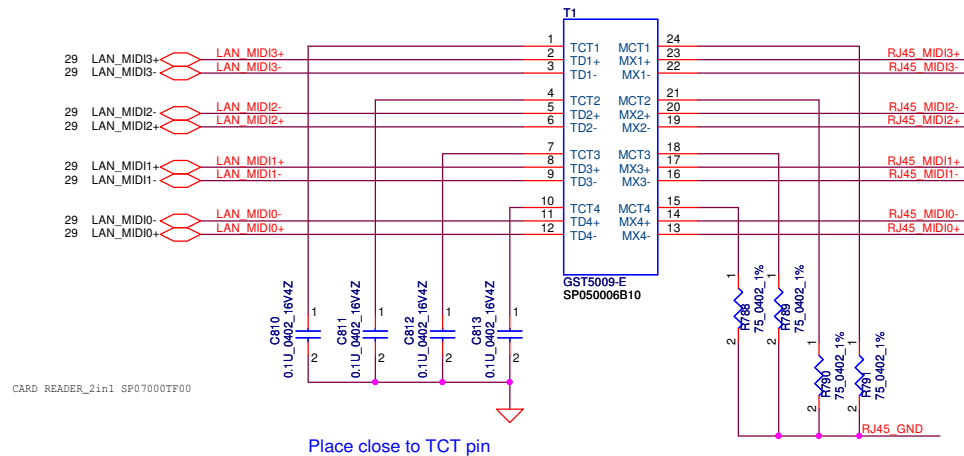
W=40mils

CRB1.0 use 47ohm@100Mhz Bead



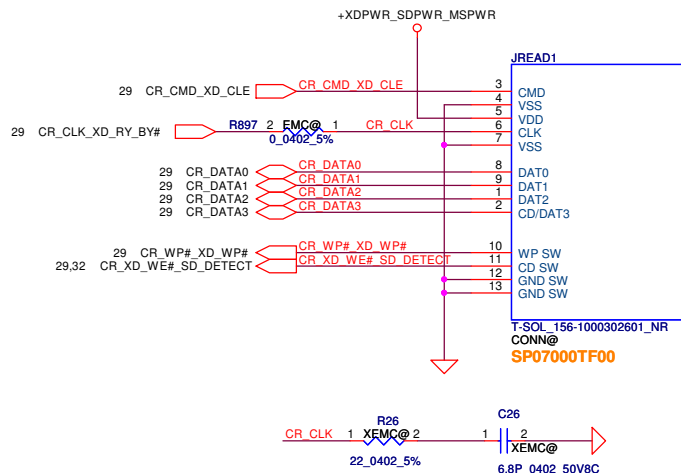
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	Document Number	Rev			0.2
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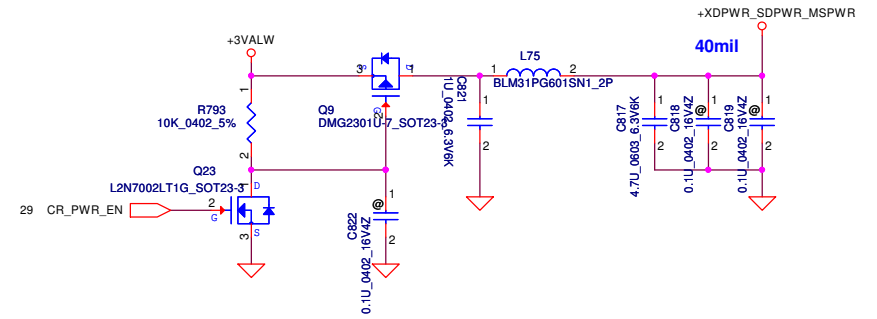
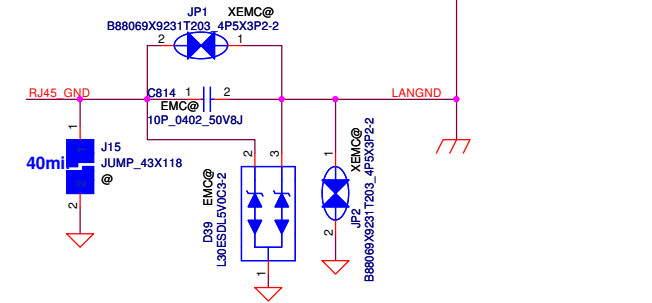
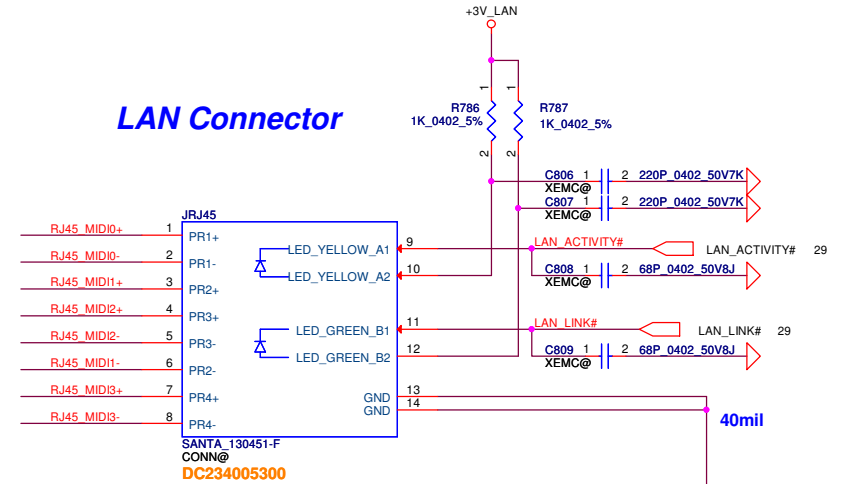


BOTH HAND: S X'FORM_GST5009-E LF LAN, SP050006B10
 TIMAG: S X'FORM_IH-160 LAN, SP050006F00
 FCE: S X'FORM_NS892407 1G, SP050006800

Card Reader Connector

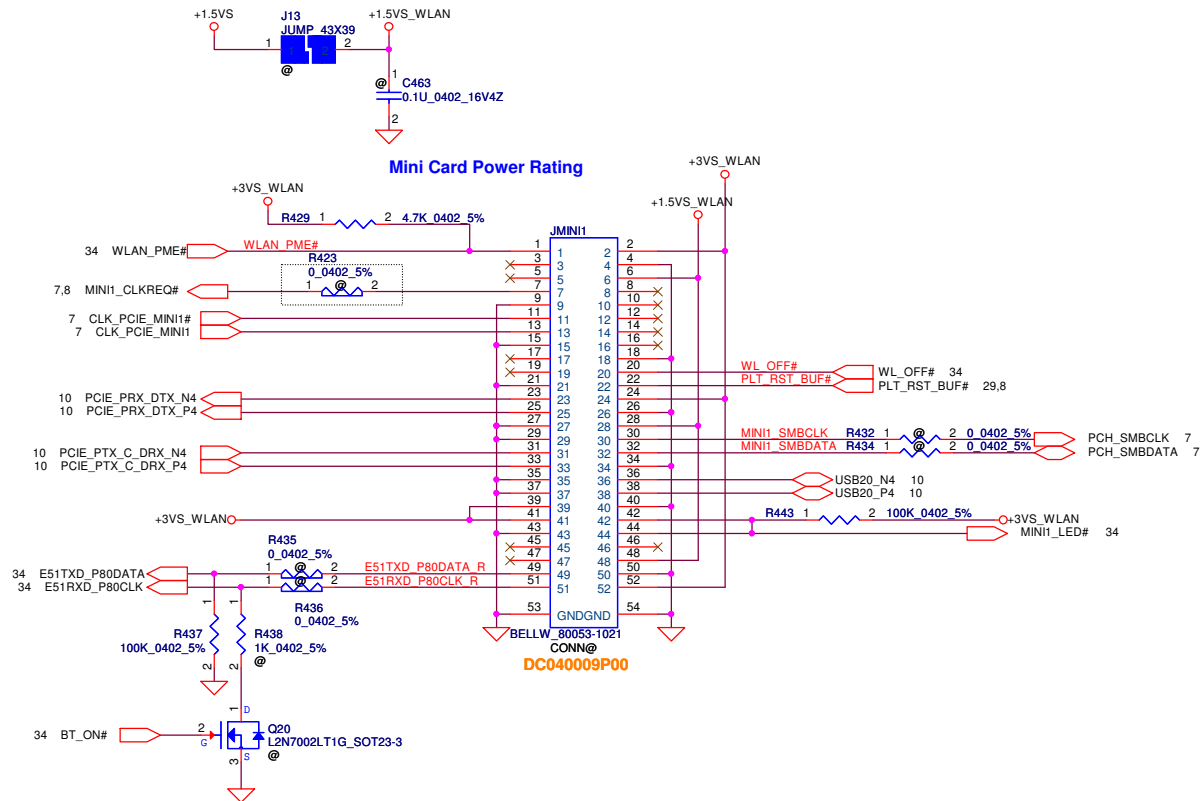
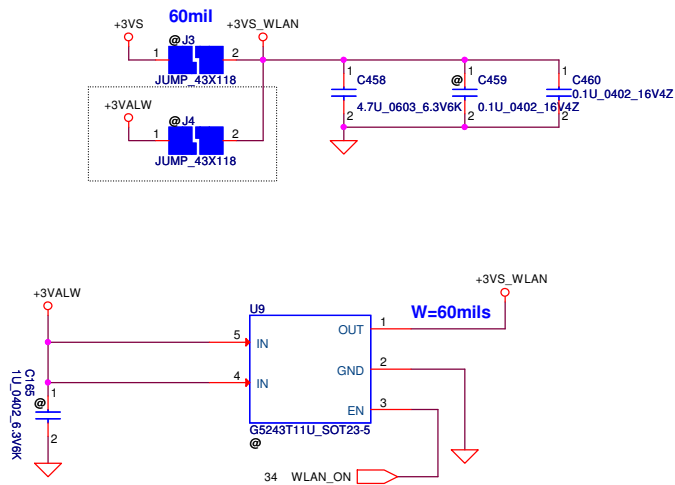


LAN Connector



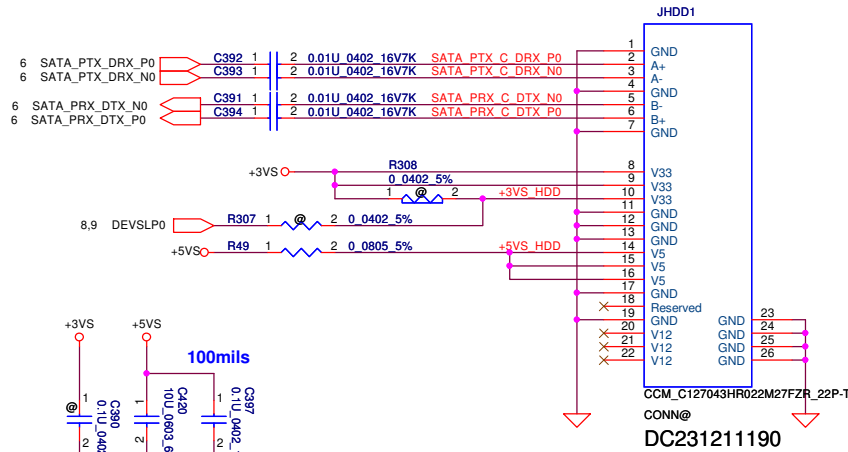
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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	
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For Wireless LAN

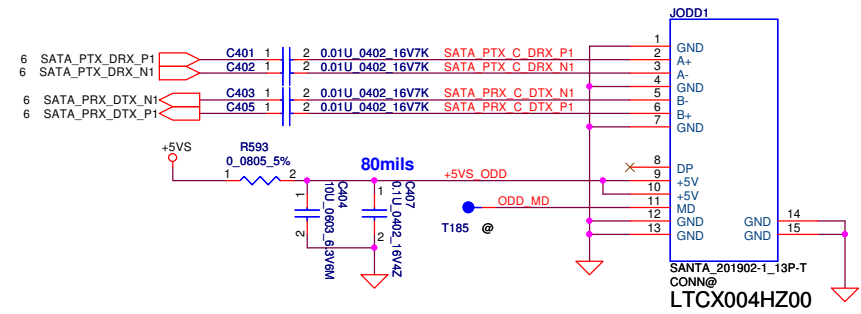


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2012/07/10		2013/07/10		Title	
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				Document Number	
				V5WE2 M/B LA-9531P Schematic	
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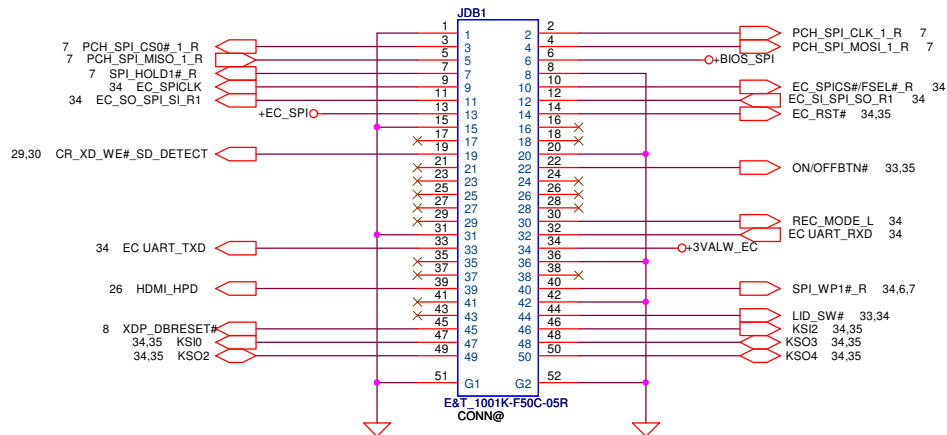
SATA HDD1 Conn.



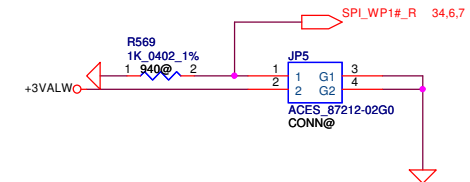
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Debug Board

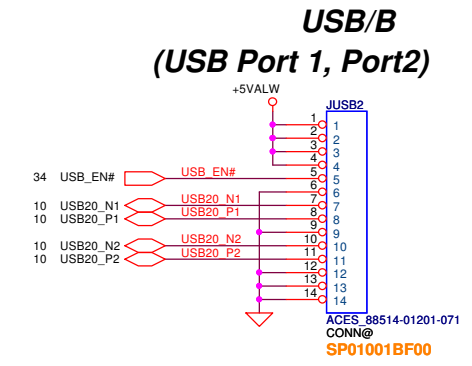
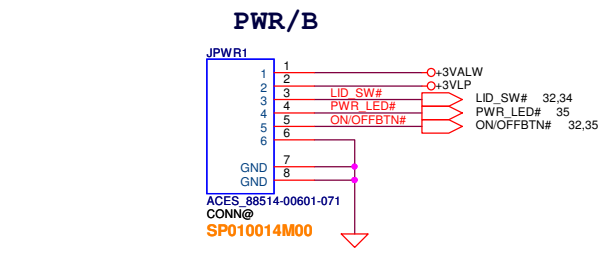
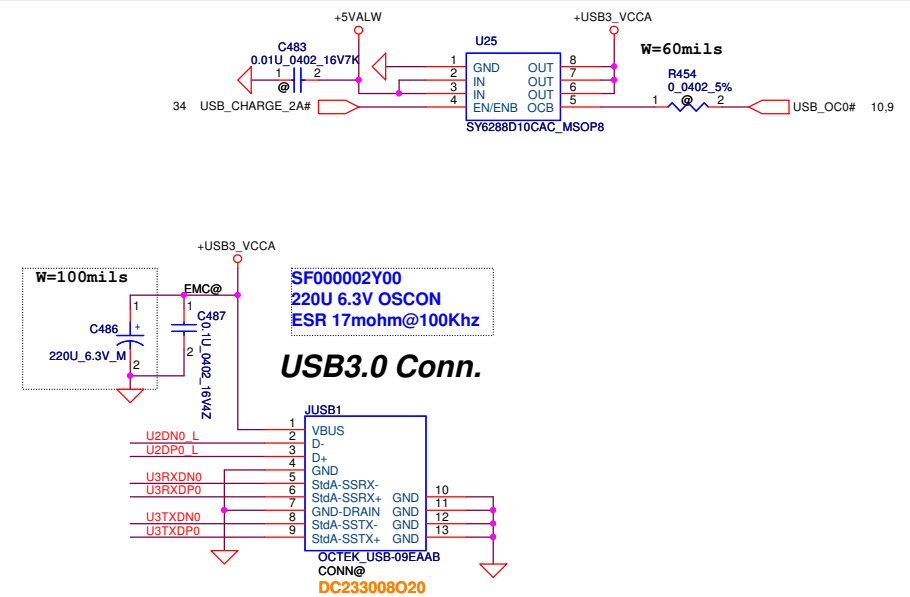
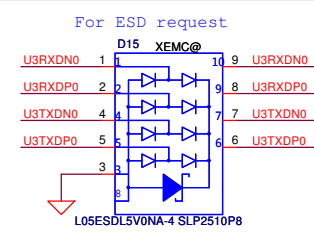
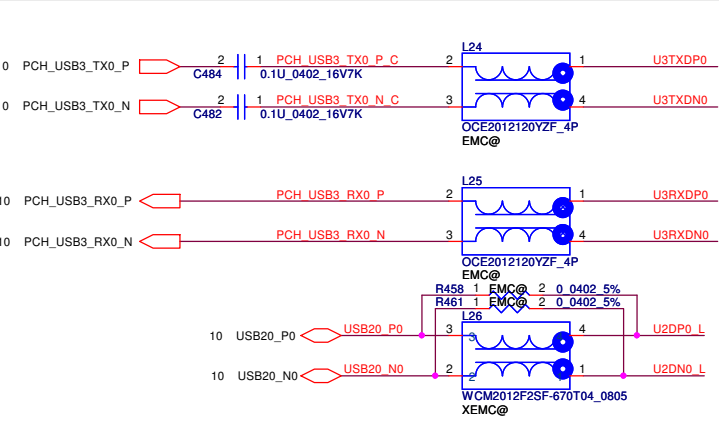


Kill SW

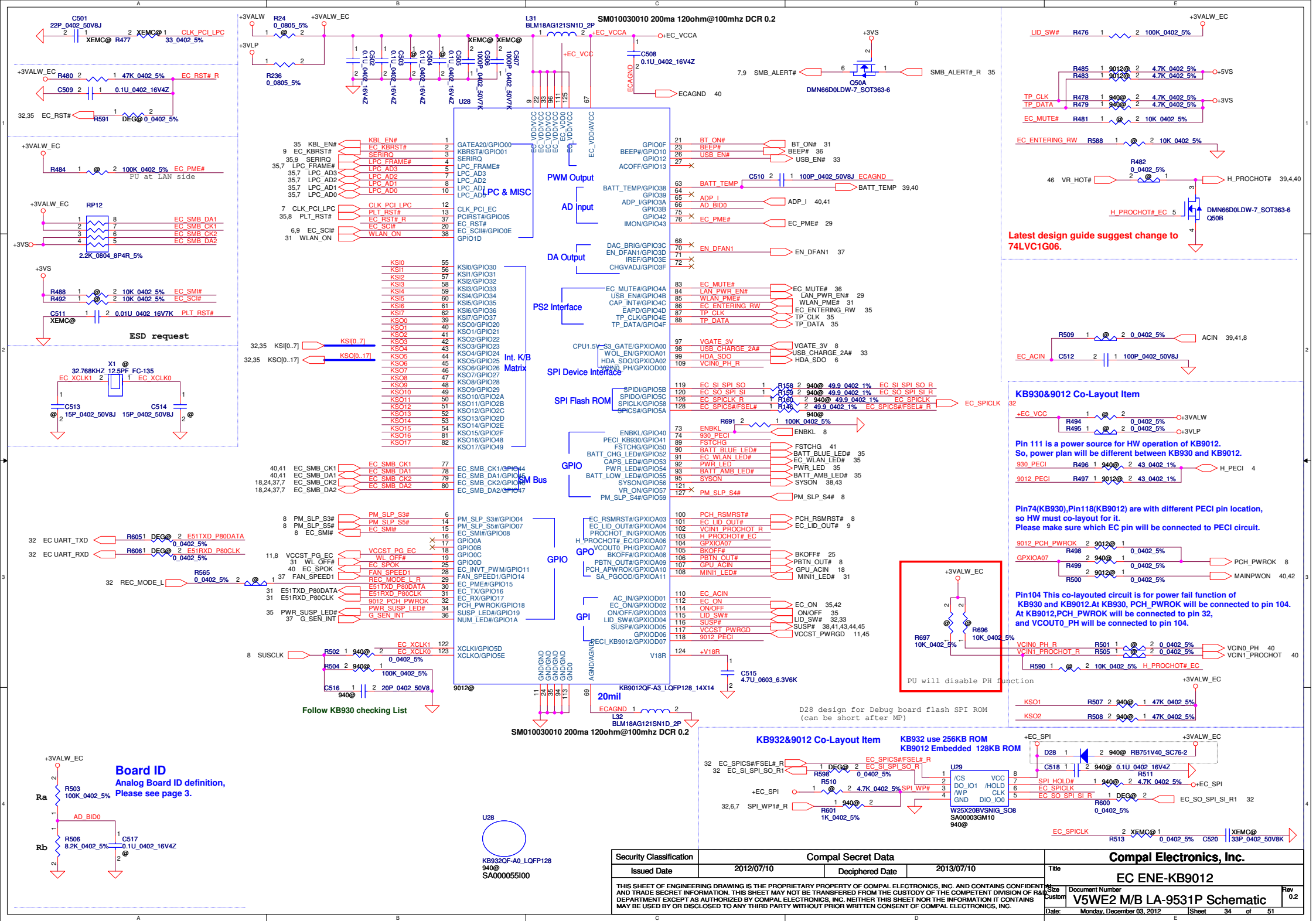


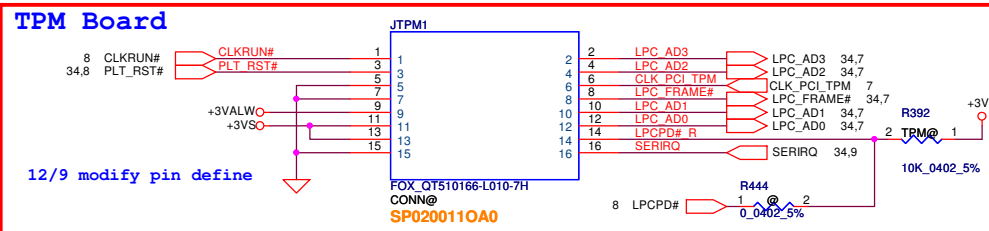
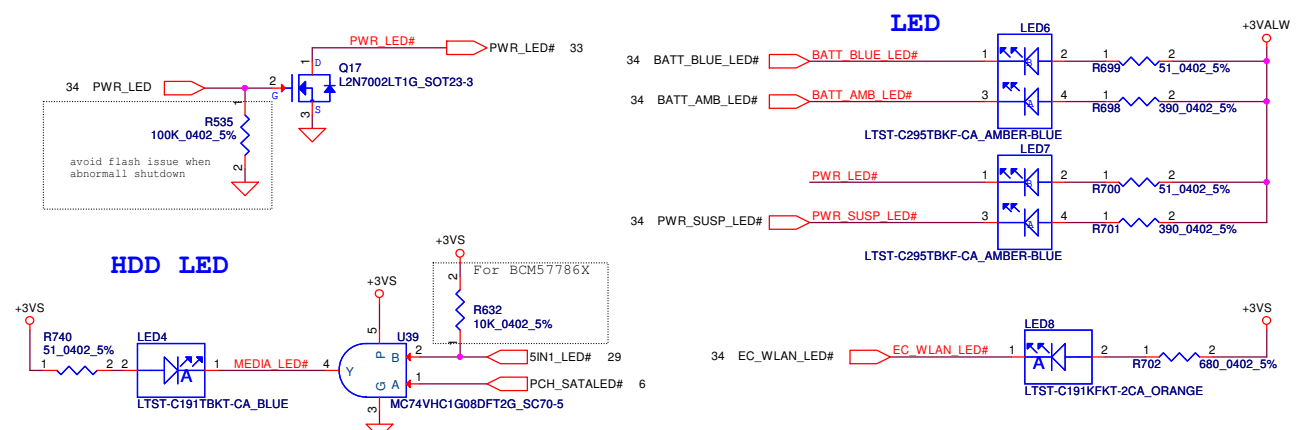
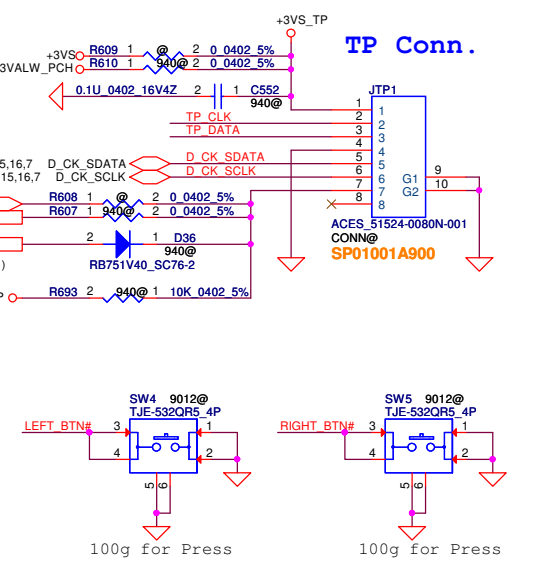
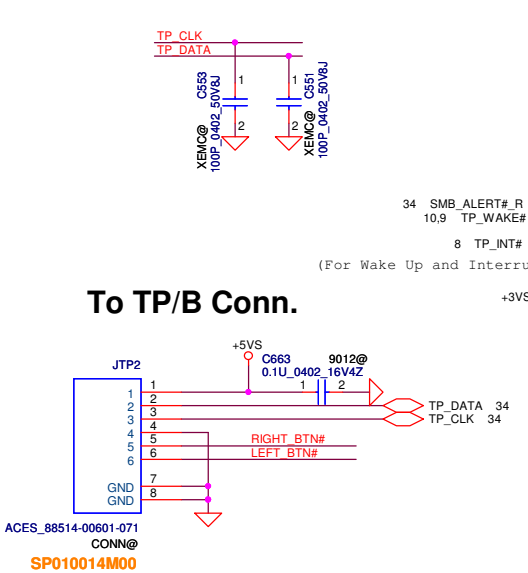
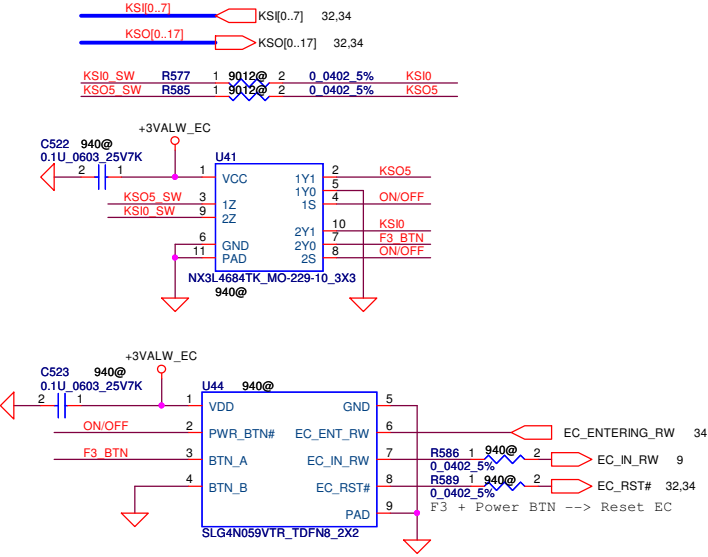
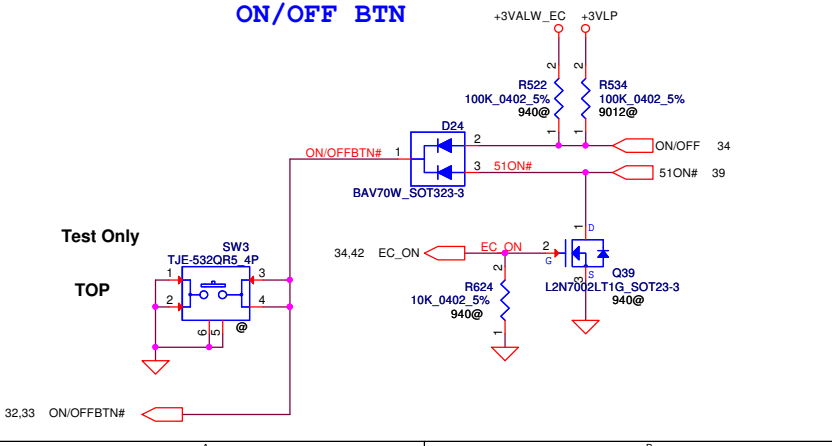
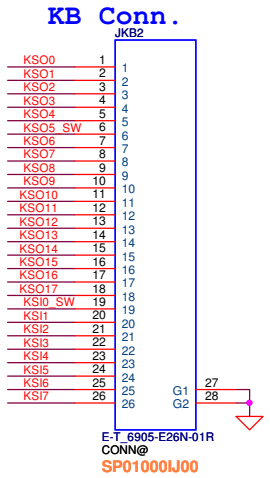
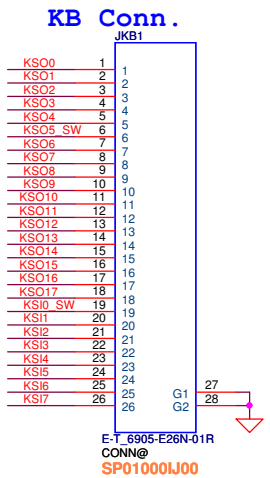
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Ctrl (R, 64)	C01, R04 (KSI0, KSO3)
D (33)	C01, R03 (KSI0, KSO2)
F3 (114)	C03, R03 (KSI2, KSO2)
Enter (43)	C01, R05 (KSI0, KSO4)
Space (61)	C03, R05 (KSI2, KSO4)

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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	
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Size	Custom	Document Number	V5WE2 M/B LA-9531P Schematic		Rev
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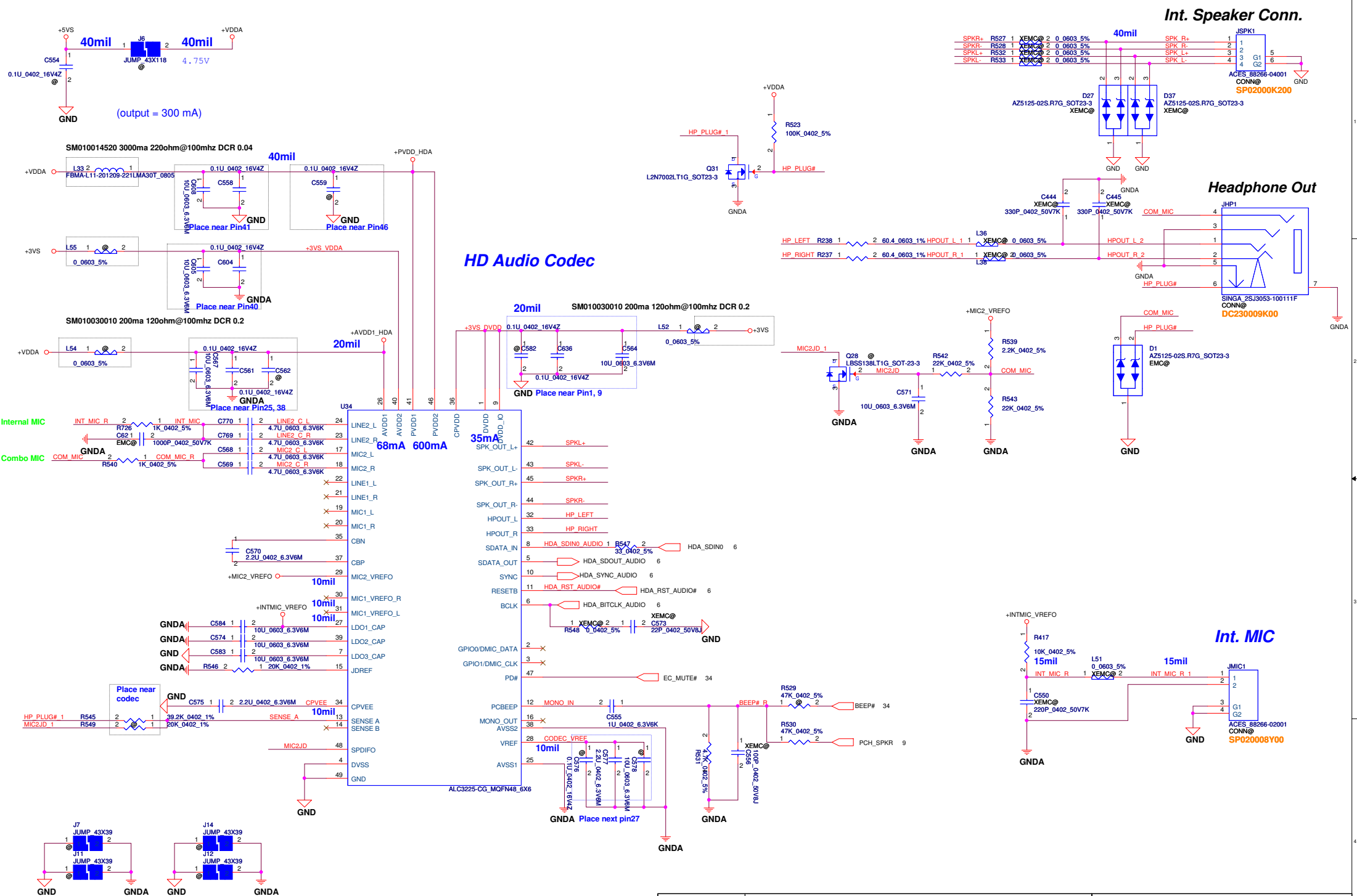


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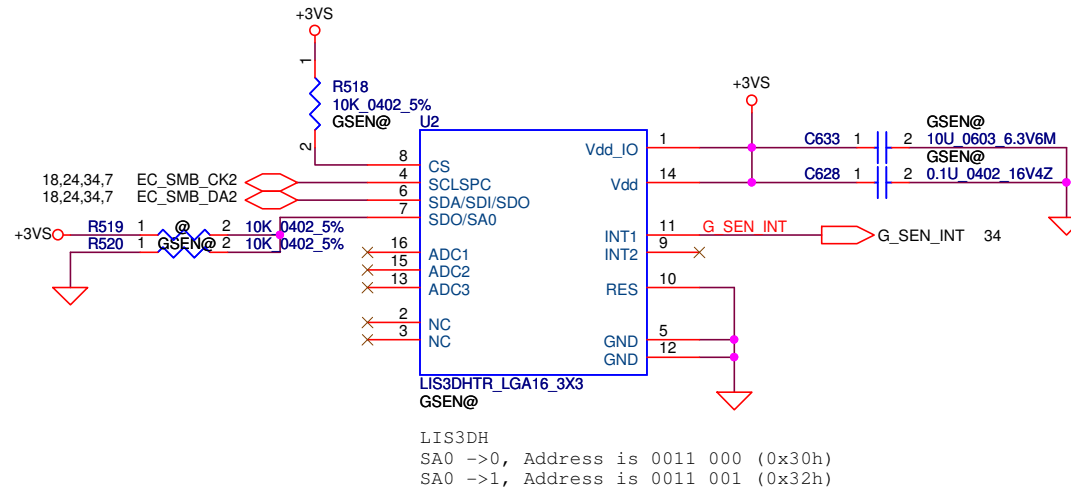
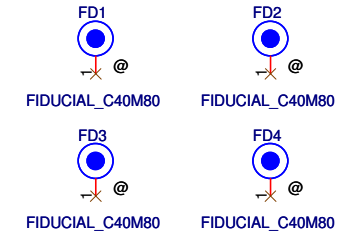
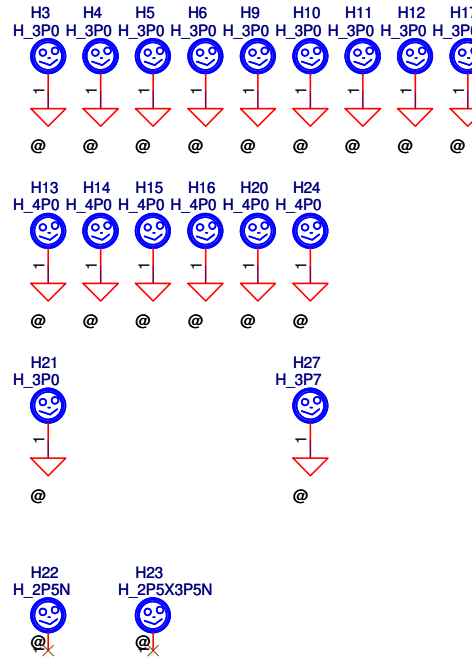
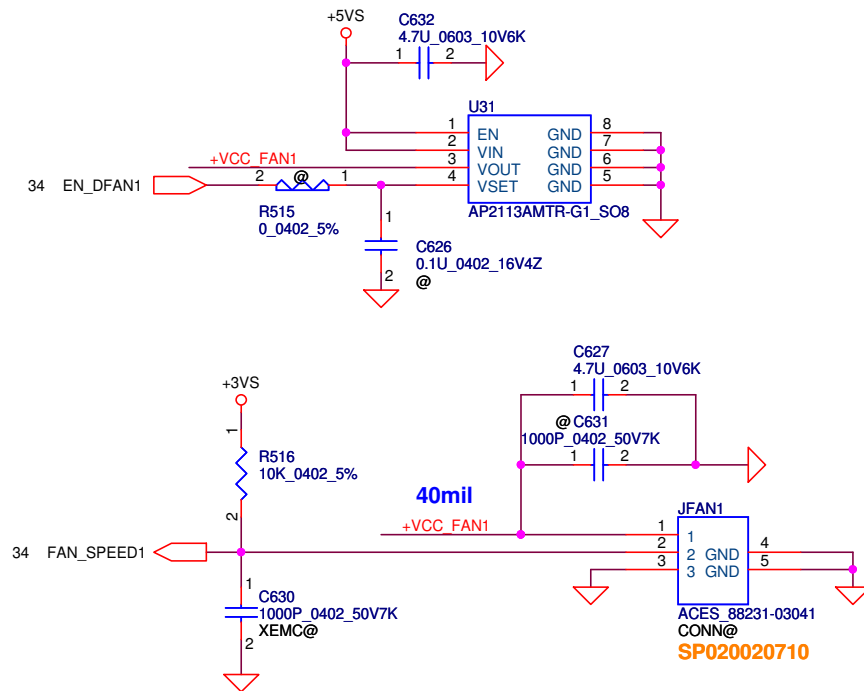


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				Size	Document Number	Rev	
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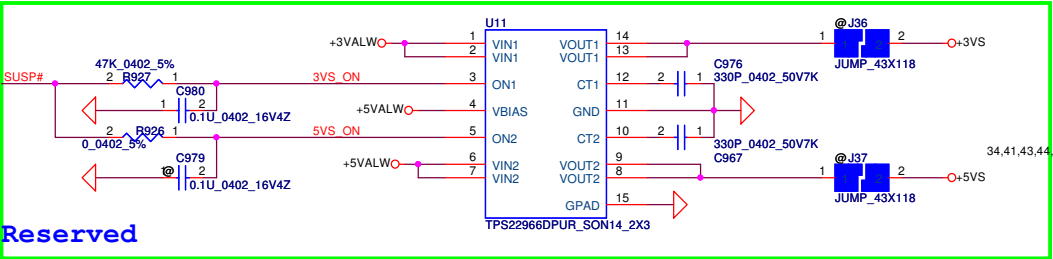
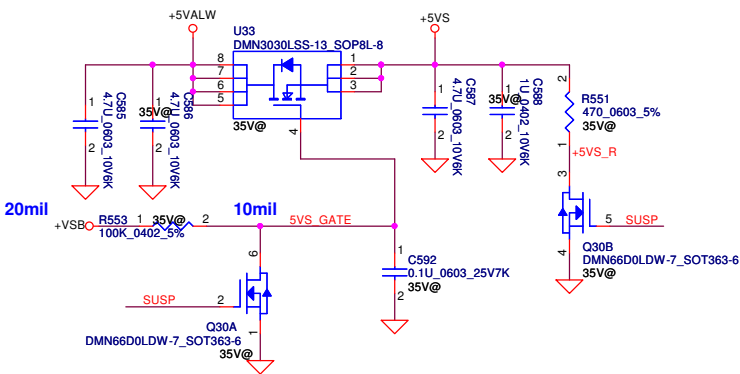
FAN1 Conn



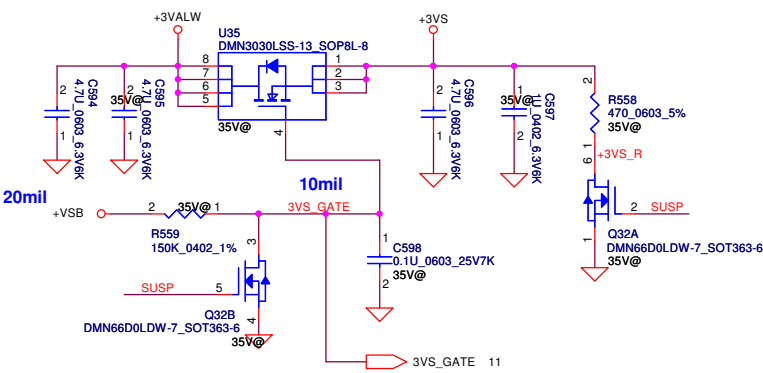
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Normal Platform (Not support M-STATE and Deep Sleep)

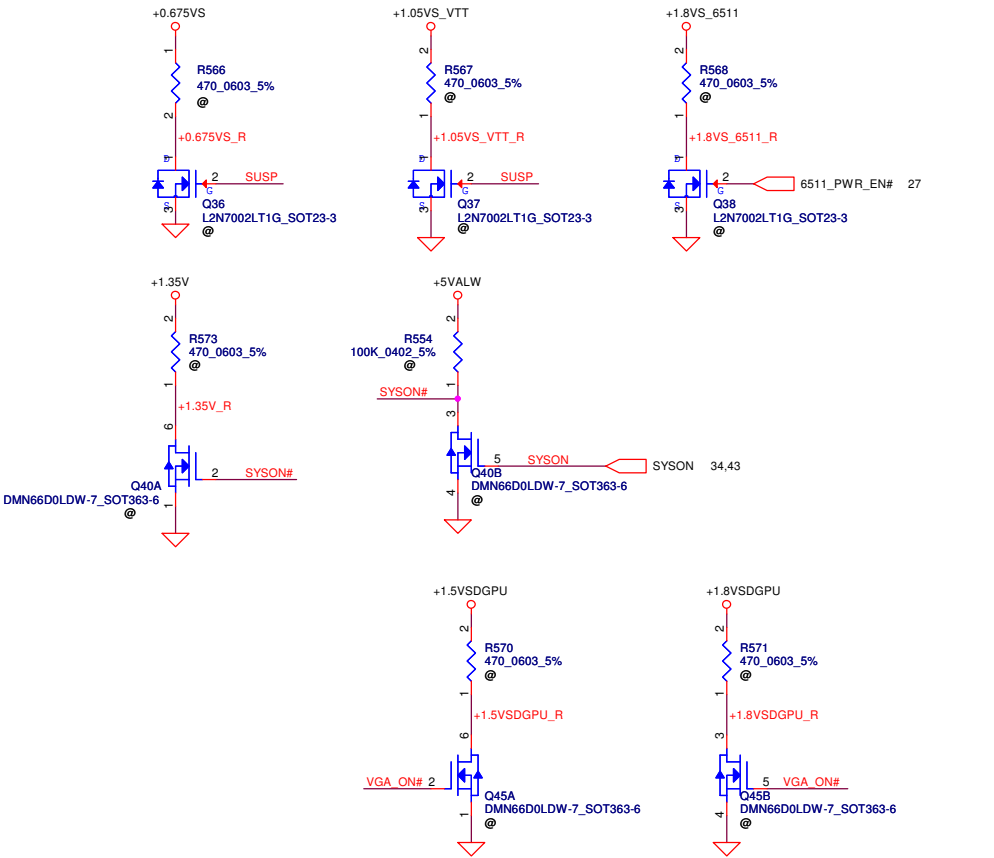
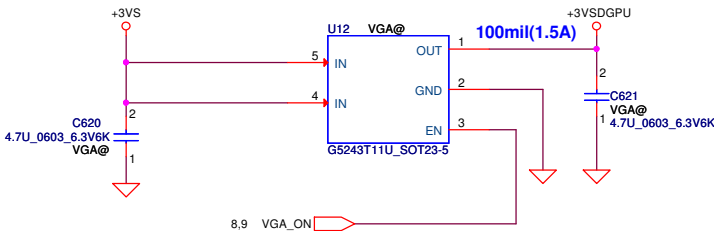
+5VALW TO +5VS



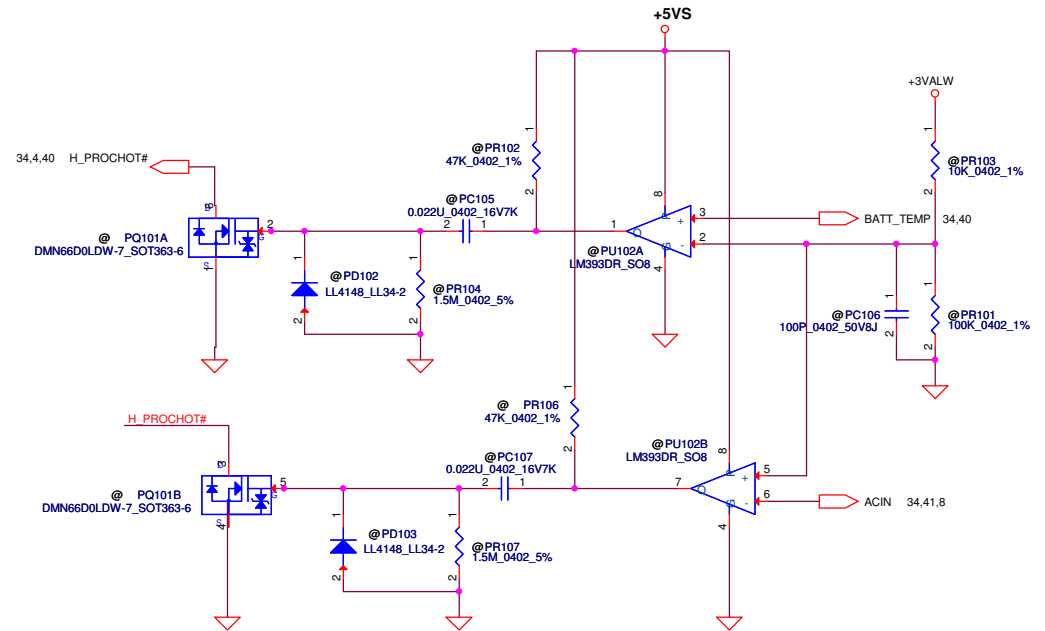
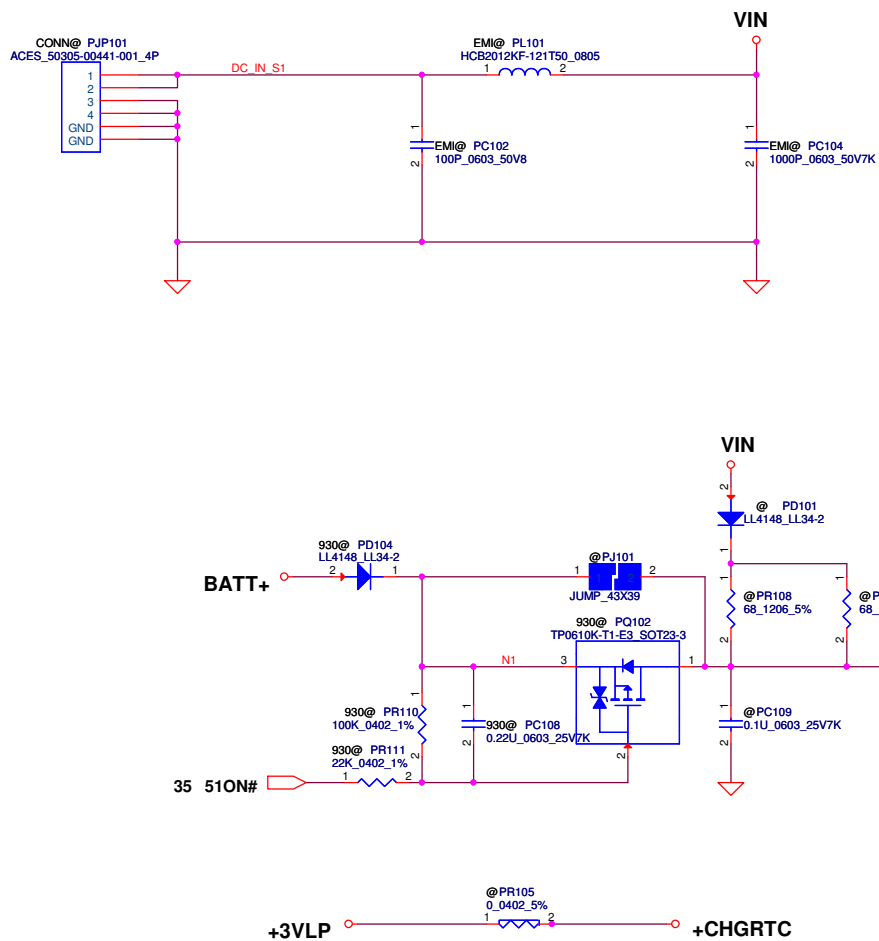
+3VALW TO +3VS



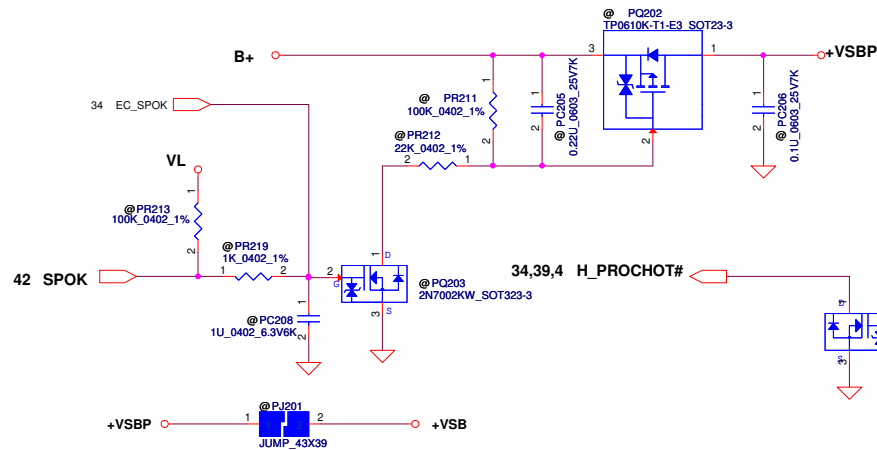
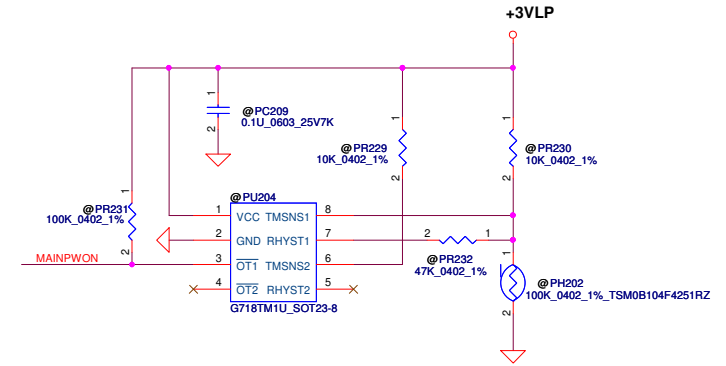
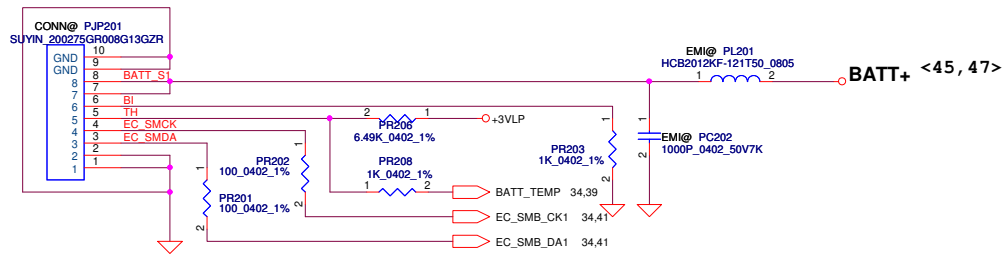
+3VS to +3VSDGPU for GPU



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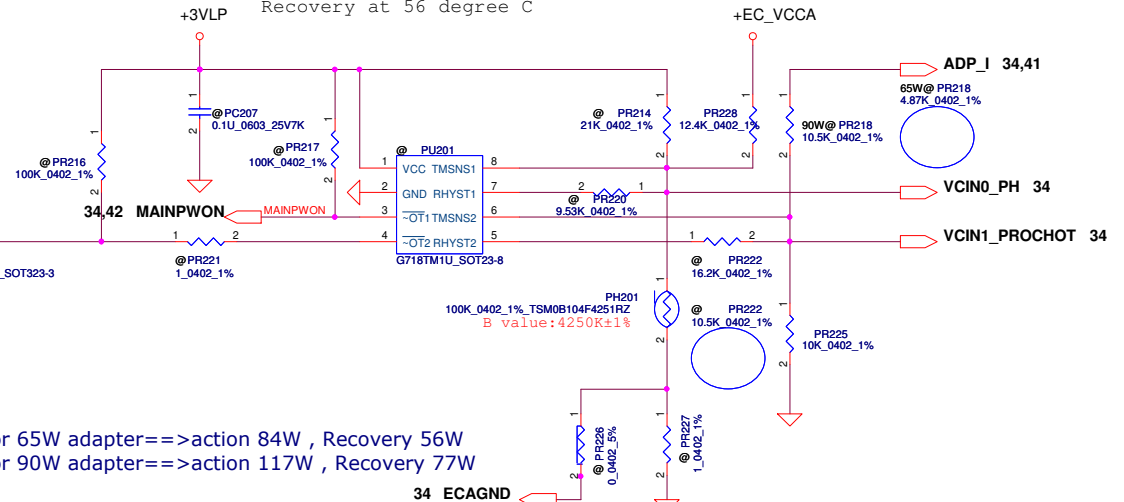
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PH201 under CPU bottom side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C

For KB9012 OTP	
92°C	1.2V, Active
56°C	2.255V, Recovery

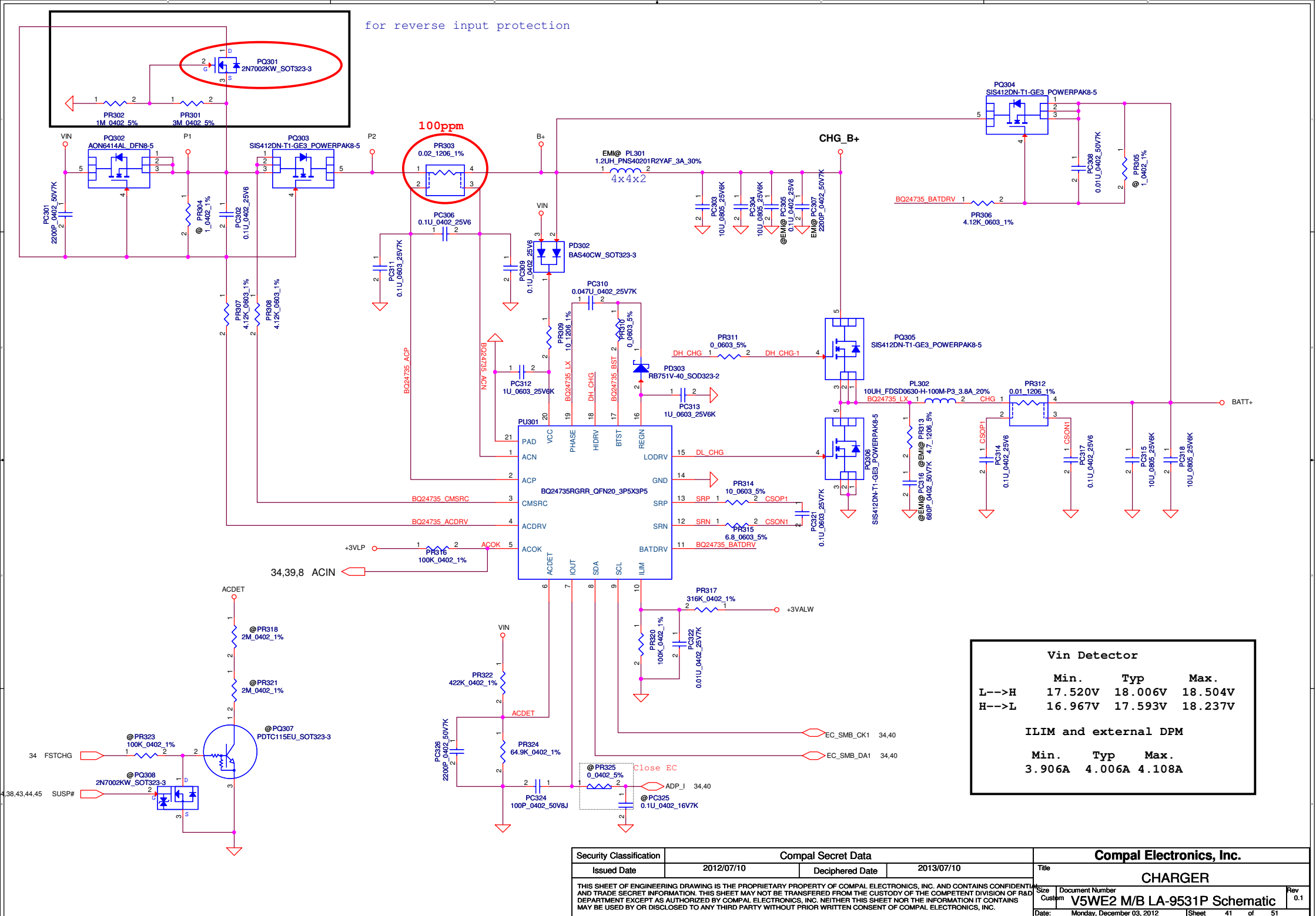
For KB9012 sense 20mΩ	Active	Recovery
65W	84W, 1.2V	56W, 0.793V
90W	117W, 1.2V	77W, 0.791V
120W		



For 65W adapter==>action 84W , Recovery 56W
For 90W adapter==>action 117W , Recovery 77W

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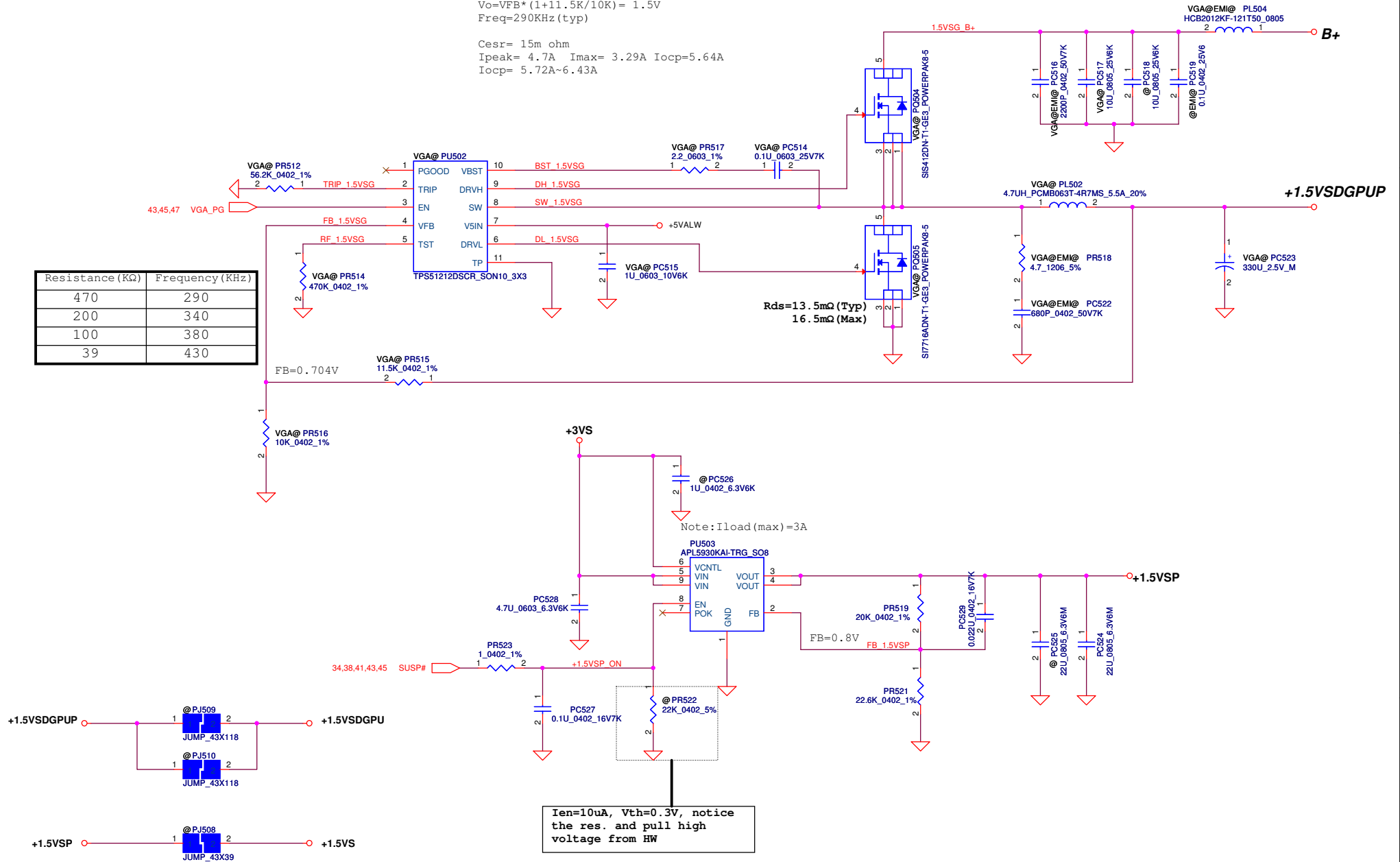
for reverse input protection



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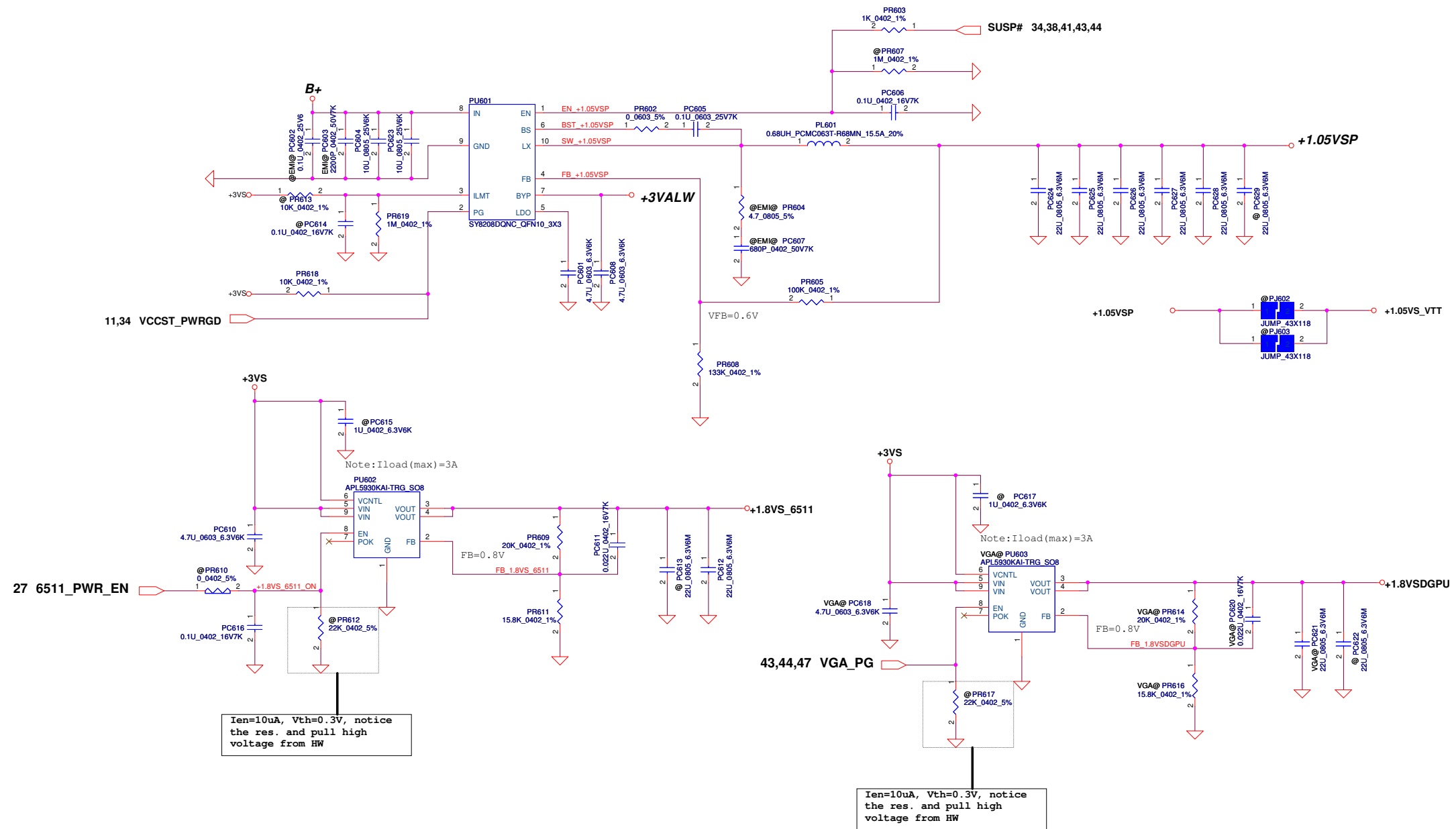
$V_{FB} = 0.704V$
 $V_o = V_{FB} * (1 + 11.5K/10K) = 1.5V$
 $Freq = 290KHz (typ)$
 $C_{esr} = 15m\ ohm$
 $I_{peak} = 4.7A$ $I_{max} = 3.29A$ $I_{ocp} = 5.64A$
 $I_{ocp} = 5.72A \sim 6.43A$

Resistance (KΩ)	Frequency (KHz)
470	290
200	340
100	380
39	430

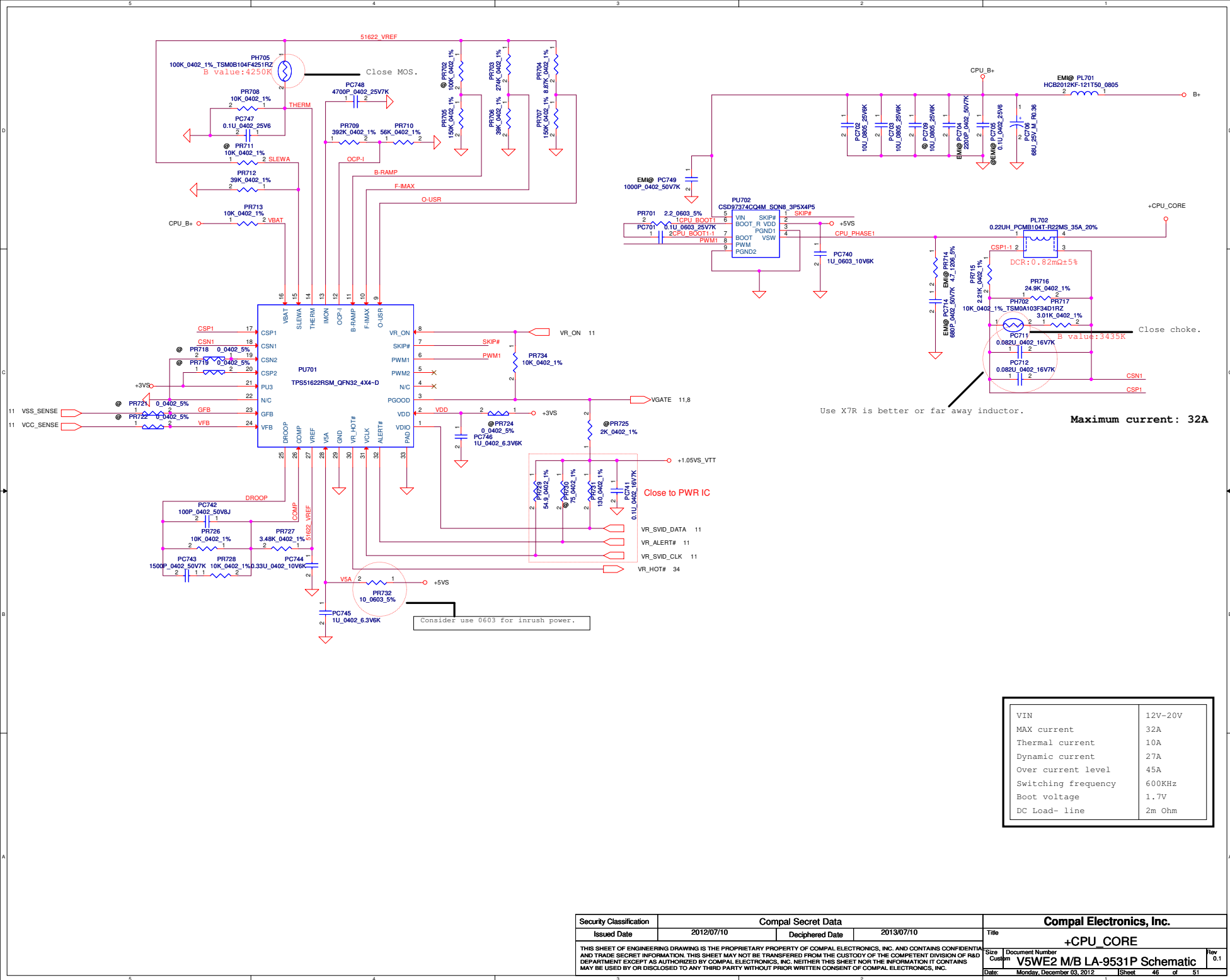


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+1.05VSP Ipeak=5.36A ; I_{max}=3.752A ; 1.2I_{peak}=6.432
Delta I=0.xxxxΔ=>1/2ΔI I=0.xxxxΔ, F= 800K Hz (typ)

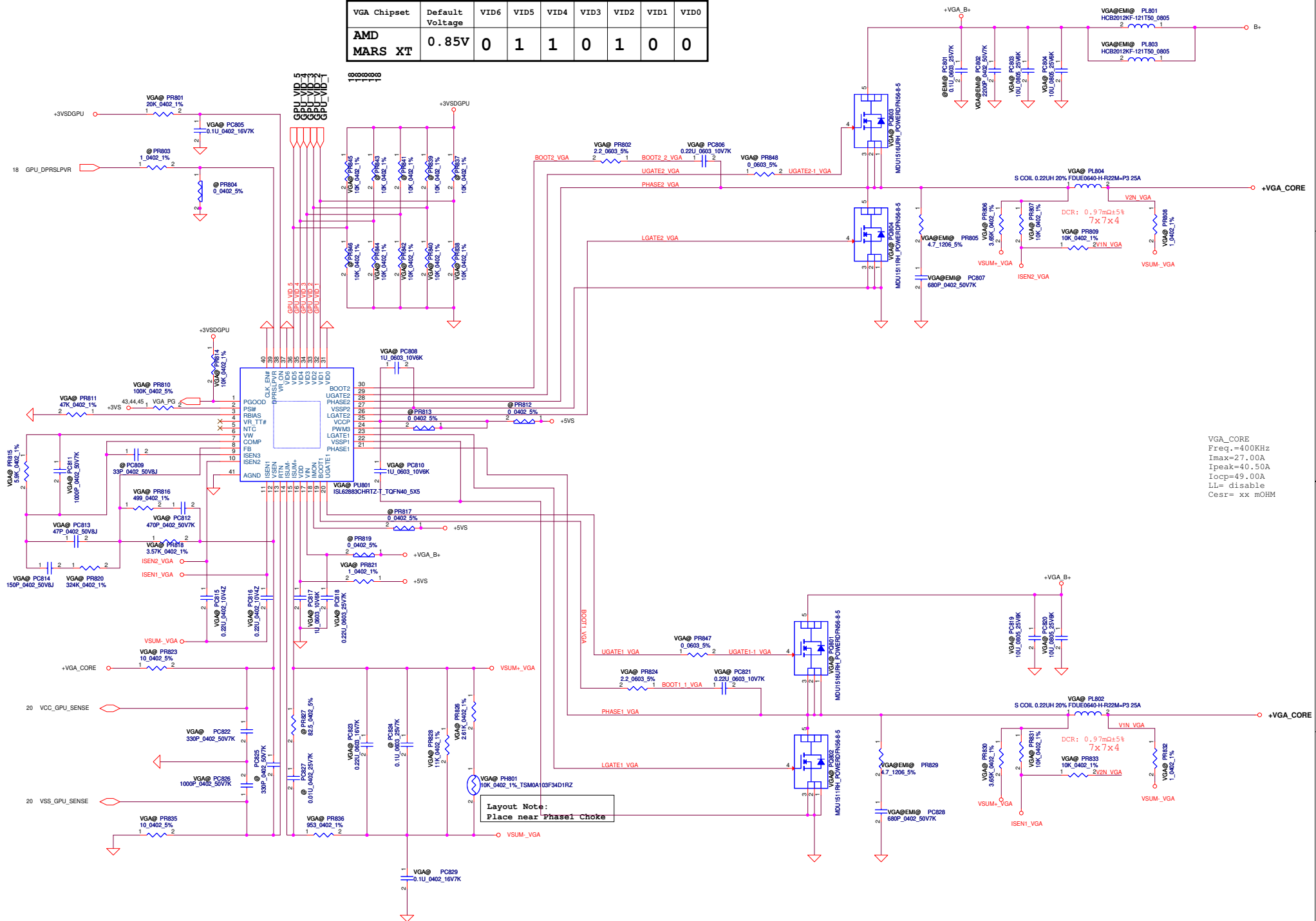


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				Deciphered Date				+CPU CORE			
				2013/07/10				Size			
								Customer			
								V5WE2 M/B LA-9531P Schematic			
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								0.1			
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VGA Chipset	Default Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0
AMD MARS XT	0.85V	0	1	1	0	1	0	0

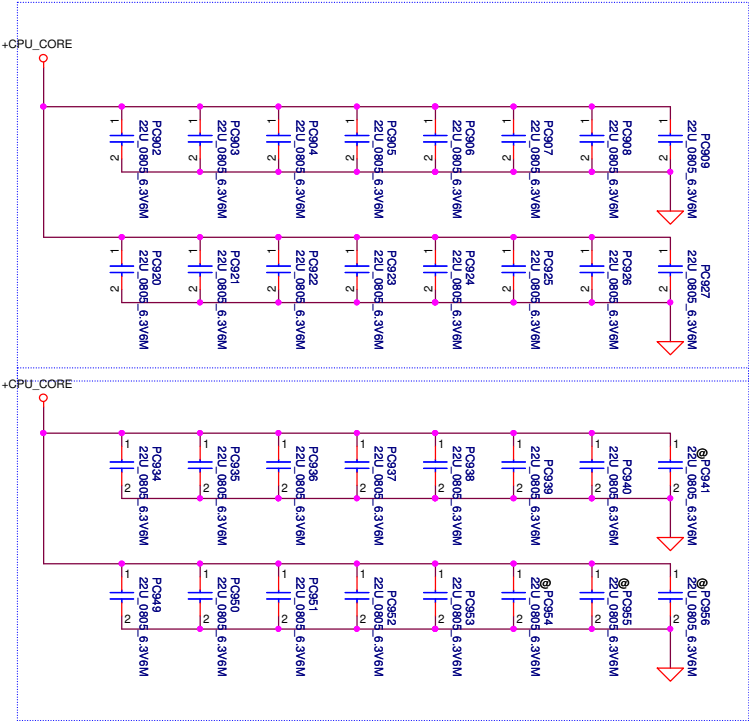


```
VGA_CORE
Freq.=400KHz
Imax=27.00A
Ipeak=40.50A
Iocp=49.00A
LL= disable
Cesr= xx mOHM
```

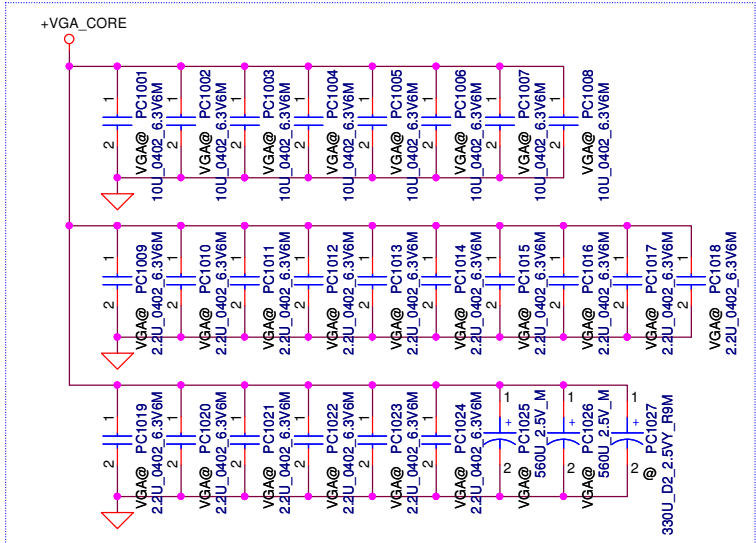
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								+GPU COREP					
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PWR Rule
CPU DCLL=1.5m ohm dedign 330uF/9m *0, 22uF *30

22u *28, @*4



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AMD MARS
GPU_CORE
560uF*2+330uF*2
10uF*8+2.2uF*16



AMD MARS
VDDCI
330uF*1+2.2uF*1

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A --> B Change List

1203A-----
1. Page11, R169 change to @
2. Page36, Mound R417 (Cancel AMIC@)
3. Page18, R898, R899, R409, D22 change BOM Structure to VGA@
4. Page34, R485, R483 change to 9012@
R479, R478 change to 940@
5. Page35, C663, SW4, SW5 change to 9012@
1129A-----
1. Page32, JODD1.11 Reserve a TestPoint for DFT
2. Page29, Pop C779, C783
3. Page17, Update U51 BOM Structure for BOM Select
4. Page04, Add QDJC@ BOM Structure for U1
1128A-----
1. Page18, Add D22 to prevent GPU_ACIN leakage
2. Broadcom recommend modify(Add Component Function Field is 45.1)
 Page29, Add C803 0.1uF to U48.20 (VDDO_CR),
 Page29, Add L74(BLM31PG601SN1) between Q6.1 and +3V_LAN
 Add C820 (1uF) to Q6.1
 Page30, Add L75(BLM31PG601SN1) between Q9.1 and
 +XDPWR_SDPWR MSPWR
 Add C820 (1uF) to Q9.1
3. Page18, Change L69 to R_Short
4. Page20, Change L72 to BLM18AG121SN1D (the same to L71)
5. SW confirmed function
 Page08, unpop R245,d21 (ACPRESENT tp PCH no need)
 Page36, unpop R529 (EC_BEEP no need)
6. Default EC_SCI# to GPIO34
 Page06, Pop R937
 Page09, Unpop R66
7. Reserve DGPU_HOLD_RST# direct to PLTRST_VGA# path
 Page08, Add R405 0ohm connect DGPU_HOLD_RST# and PLTRST_VGA#
8. Page35, Chagne R702 to 680ohm (ME confirm)
9. Page35, Delete SW1 (debug) for Layout convenience
10. Page24, Change L6 to (4.7uH_SH00000GS00) same as Q5WV8
11. Page29, Change RP22 to R768, R769, R770, R771 for SD 3.0 EMI
1127A-----
1. Page24, Change U50.11 connect from L6.2 to L6.1
2. Page34, Change R502 from R_short to 940@ 0ohm
3. Page36, Change R237, R238 to 60 Ohm(Codec vendor recommend)
4. Page09, Add R67 for EC_SCI# -> GPIO 10 option
1126A-----
1. Page36, Delete D26 (ESD Confirm)
2. EMI part Schematics modify(EMI confirm123)
 Page26, Change R368, R369, R370, R371, R372, R373, R374, R375 to 0403
R_short
 Page28, Change R175, R180 to 0603 R_short
 Page36, Change L36, L38, L51, R527, R528, R532, R533 to 0603 R_short
 Page32, Delete C408, C398
 Page33, Delete R453, R455, R456, R457
3. Page38, Change 3/5 VS circuit BOM Structer to 35V@
4. Page32, Modfiy JHDD1 to LTCX004LGA0 (S H-CONN CCM
C127043HR022M27FZR 22P H3.05 HDD)
 Modfiy JODD1 to LTCX004HZ00 (S H-CONN SANTA 20190X-X
13P H3.6 ODD)
1123A-----
1. Delete +3VALW to +3VALW_PCH MOS Circuit:
 Page12, Delete C589, C414, R77, Q10, C590, C591
 Page34, Delete U28.16 PCH_PWR_EN# off page
2. Page12, Unpop R210 , Pop L3 and C22 for +1.05VS_VTT high ripple
3. Unpop and Component reduce-----
 Page16, Delete C824, C828, C831, C836, C839 for unpop reduce.
 Page20, Delete C870, C871, C923, C922, C921, C920 for unpop reduce.
 Page27, Change R399, L30, L47 TO R_Short
 Delete C456, C637, C474, C497, C580, C581
 Pop R80 and unpop R396, Q25, C411, R584, Q52
 Page28, Delete C606, C646, C607
 Change R239 to R_short
 Page29, Delete C775, C776, C778, C781, C782
 Page31, Delete C461, C462
 Change R423 to R_short
 Page32, Delete C161
 Change R308 to R_short
 Page34, Change R495 to R_short
 Page36, Chagne L55, L54, L52 to R_short
4. Page24, SWAP RP41.1, RP41.2
5. Page27, Change R123, R127 Pull high to +HDMI_5V_OUT

1122A-----
1. Page22, Add X7603@ for VRAM 2Gb*4 HYN 128M16
 Add X7604@ for VRAM 2Gb*8 HYN 128M16
1121A-----
1. Page06, Add R937 for EC_SCI# Path to GPIO34
2. Page09, RP28.5 connect to GPIO34
1120A-----
1. Page06, Delete chargeable RTC circuit
 Change ODD to SATA port1
 Page32, Modify ODD SATA netname to SATA port 1 .
2. Page29, +1.2V_LAN_OUT add 680P for EMI
3. Page37, Modify H21 from 2P5 to 3P0
4. Page38, Add 2 jump for power cousumption measure
 J36(+3VS), J37(+5VS)
5. Delete XDP port and related circuit
 Page04, Delete C63, C64, C96, C97, C98, R20, R21, R22, R23, R27-R31
 Delete R3, R86, R87, R88, R89, R90, R91, R4, C92, C93
 Delete R5, R14, R15, R16, R7, R19, R25, C35, JXDP1
 Page07, Delete R66, R67
6. ESD DVT Modify:
 Page08, Delete C39
 Page24, Delete D6
 Page28, Delete D7, D18
 Page30, Delete D38
 Page33, Delete D16
 Page35, Delete D25, D30, D34
 Page36, Delete D26, R544, C572
 Page37, Delete ESD TP JUMPS:
 J10, J20, J17, J21, J16, J19, J18
 J22, J24, J28, J25, J29, J23, J27
 J26, J30, J31, J33, J32, J34, J35
 Page29, C786 change to EMC@
 Page04, Add C96 to DIMM_DRAMRST#
 Page33, C487 change to EMC@ and 0.1uf
 Delete D4
 Page26, C378 change to EMC@
 C387 change to EMC@
1119A-----
1. Page06, Add a nochargeable RTC battery.
2. Page15, Add R191 for DDR_VTT_PG_CTRL pull high +5VS option.
3. Add page24, Reserve eDP to LVDS translator (RTD2132R)
 Add bom structure TL@ (translate) and EDP@ (eDP mode)
4. Page25, Add R947 for ENVIDD option.
 Add connect TL_INVIT_PW to INVITPDM
 Add connect RTD2132R TL_HPD to EDP_HPD
 Modify JLVDS1 pin net name fo Co-Lay eDP & LVDS

1107A-----
1. Page04, Move R25 to JXDP1.60
 Update U1 option component for CPU
2. Page6,8, Change EC_SMI from GPIO77 to GPIO34
 Delete R445
3. Page07, Change Y2 to X3G024000DC1H(SJ10000CS00)
4. Page08, U17, U43, R310 change to @
 Mount R65
 R310.1 change to +3VS
5. Change all 932@ to 940@
 R161, D29, R564, U6, R569, C522, C523, C552, D36, Q39, R522, R586, R589, R607,
 R610, R624, R693, U41, U44, C516, C518, D28, R146, R158, R159, R160, R496, R499,
 R504, R507, R508, R511, R601, U28, U29
6. Page11, R169 change to XDP@
7. Page12, add C414 and change PCH_PWR_EN to PCH_PWR_EN#
 delete Q33, R561, R563
8. Page16, delete R58, R298, R300, C163, R299, R302
9. Page17, Add option component (U51) for SUN_XT
10. Page19, Add R900, R901 with BOM structure @
11. Page24, delete R405, U20, R362, R401, C164
 Change U8 to G5243AT11U(SA000028Y10)
12. Page25, delete R367, D7, F1, D8, D19
13. Page26, change L47, L48 to BLM18AG121SN1D(SM010030010)
14. Page27, Delete D31, F2, C450
15. Page28, Delete R781, D23, R782, R785, U49, C803
16. Page29, Delete R792
 change T1 to GST5009-E (SP050006B10)
17. Page30, delete R414, C166
 R438, Q20 change to @
 Change U9 to G5243AT11U(SA000028Y10) with BOM@
18. Page31, delete R595, R587, Q34, R597, R596, R562
19. Page32, Change U25 to SY6288D10CAC_MSOP8(SA00004KB10)
 Change JUSB1 to OCTEK_USB-09EAAB(DC233008020)
 Delete R472, R469, R460, R462, C635, U46, R459, R463, R464
20. Page33, Mount R503
 Change R506 to 8.2K
 Change R509 to R_Short with BOM @
 Delete R491, R493, D20
21. Page34, add R535 (100K_0402)
 Mount R632
21. Page35, L51 change to BLM18AG121SN1D(SM010030010)
 Change JM1C1 to ACES_88266-02001(SP020008Y00)
 Delete R143, R668, R162, R181, C719, R671
23. Page37, delete R424, C169
 Change U12 to G5243AT11U(SA000028Y10)
24. Page43, SW1 change BOM Structure to @
1015A-----
1. Modify BOM Structure/Function Field for EMC@(45.1)
 Page06, RP14
 Page07, RP19, R390
 Page24, L11
 Page25, R368, R369, R370, R371, R372, R373, R374, R375
 Page27, L42, L45, L46, R175, R180
 Page28, R774
 Page29, R897, C814, D39
 Page32, L24, L25, R458, R461
 Page35, R527, R528, R532, R533, L36, L38, D1, C62
2. Modify BOM Structure/Function Field for XEMC@(45.1)
 Page04, C63, C64, C96, C97, C98, C94, C95, C60, C92, C93, C35
 Page07, R104, C152, R402, C453
 Page08, C39
 Page24, C528, C549, C364, C365, D6
 Page25, D2, L13, L14, L15, L16
 Page28, C792, C786
 Page29, R26, C26, C806, C807, C808, C809, JP1, JP2, D38
 Page31, C408, C398
 Page32, D15, D16, D4, C487, R453, R455, R456, R457, L26
 Page33, R477, C501, R513, C520, C506, C507, C511
 Page34, C551, C553, D25, D30, D34
 Page35, R548, C573, R671, C719, C556, C550, C444, C445, D27, D37, D26, R544, C572
 Page36, C630
3. Modify Function Field to 45.1 only (BOM Structure is same as before)
 Page04, R27, R28, R29, R30, R31
 Page07, RP20
 Page33, R160
 Page35, R143, L51
4. Display BOM structure and Value of U1 (CPU)
5. Display BOM structure of R0402_0OHH-NEW and R0603_0OHH-NEW (R Short Pad show BOM Structure @)
6. Page08, Update note of GPIO66

Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Tune VGA sequence	Tune VGA sequence		VGA	PR801 change to 20K Add PC805, PR814 Delete PR615, PC619, PR511, PC513, PR530, PR531, PC530	11/06	DVT
2	Module Design	Module Design change 3/5V solution		3/5V		11/13	DVT
3		Change RTC type to non-charge		39	Un-pop PR112, PR113	11/13	DVT
4		Check no need keep with HW		39	Delete PR112, PR113, PBJ101	11/20	DVT
5	EMI request			EMI	Add PR518, PC522, PR714, PC714, PR829, PC828, PR806, PC807, PC749 Change PR701 to 2.2	11/20	DVT
6	EMI request	EMI confirm remove		EMI	Delete PL102, PC103, PC101, PL202, PC201 and PL703	11/26	DVT
7							
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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	PIR (PWR)	
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