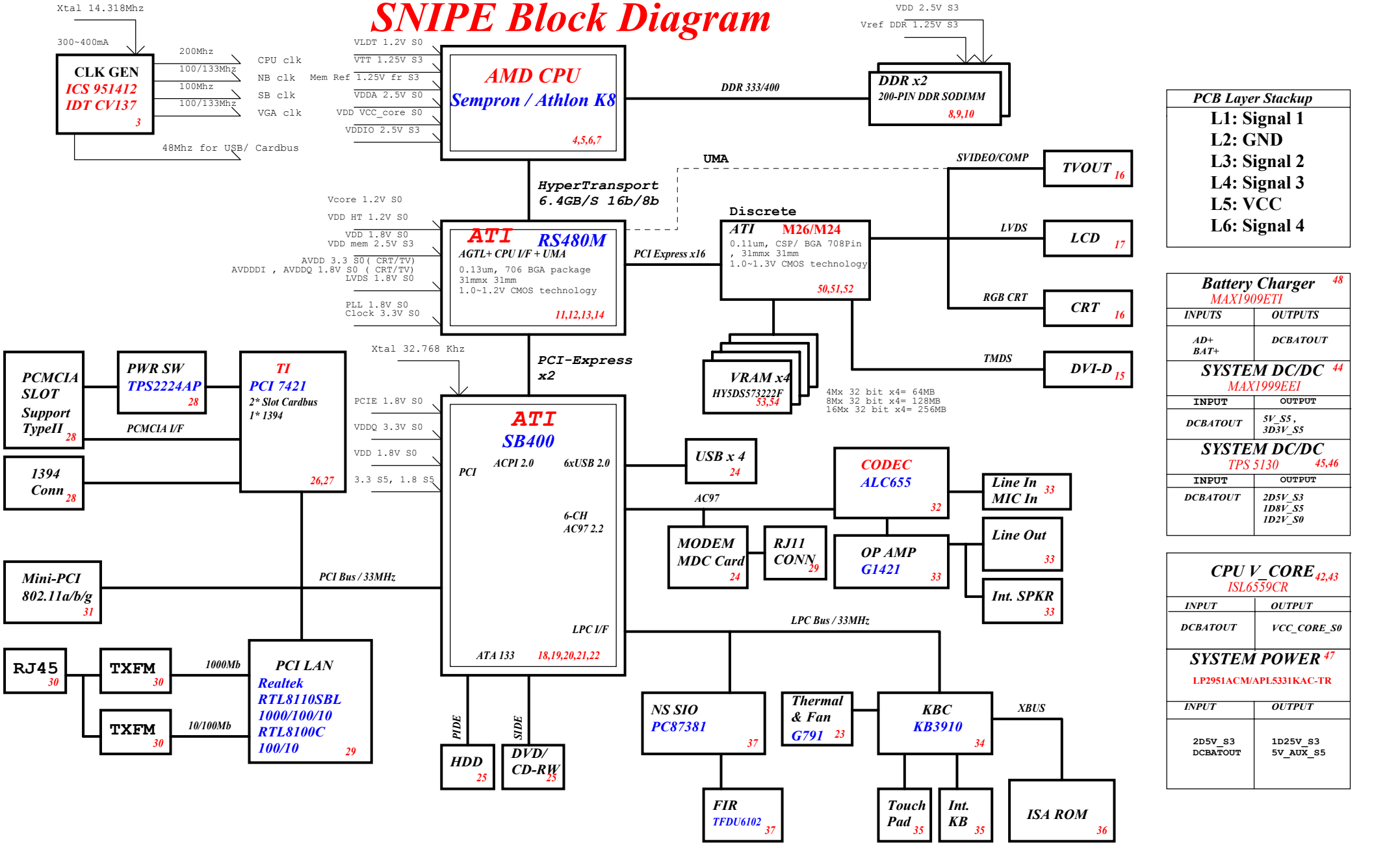
SNIPE Block Diagram



PCB Layer Stackup
L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

Battery Charger 48
MAX1909ETI

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SYSTEM DC/DC 44
MAX1999EEI

INPUT	OUTPUT
DCBATOUT	5V_S5 , 3D3V_S5

SYSTEM DC/DC
TPS 5130 45,46

INPUT	OUTPUT
DCBATOUT	2D5V_S3 1D8V_S5 1D2V_S0

CPU V_CORE 42,43
ISL6559CR

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM POWER 47
LP2951ACM/APL5331KAC-TR

INPUT	OUTPUT
2D5V_S3 DCBATOUT	1D25V_S3 5V_AUX_S5

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLOCK DIAGRAM**

Size	Document Number	Rev
A3	SNIPE	SA

Date: Monday, November 22, 2004 Sheet 1 of 56

SA to SB need to check
1. connect G781 Thermal Alert pin to VGA_GPIO14
2. ene KBC P165 LPCRST# , we suggest pull low avoid leakage
3. Clk to NB need to add Cap. when the trace change layer.
4. check page 9. what is the value of R481,R486, R498 and R499 is 100 ohm or 12 ohm.
5. check page 15, if on discrete mode does the 1D8V_S0 power for lvds should dummy or still contect on power plan.
6. check page 19, can the 0 ohm resistance be dummied on P.19 right hand side?
7. check page 20, R203's voltage on pin 2.
8. page 21. check when the unused USB pin should be pull down or floating.
9. Can R471 change to common value?
10. check giga lan and 10/100 connect. Does them the same or can chose a cheaper one?
11. page 38. 12VGATE_S0 can decreased resistance.
12. Does the 1D5V_VGA_S0 can come from TPS5130?

Schematic change:
R659, change from 0R2 to 10Kr2

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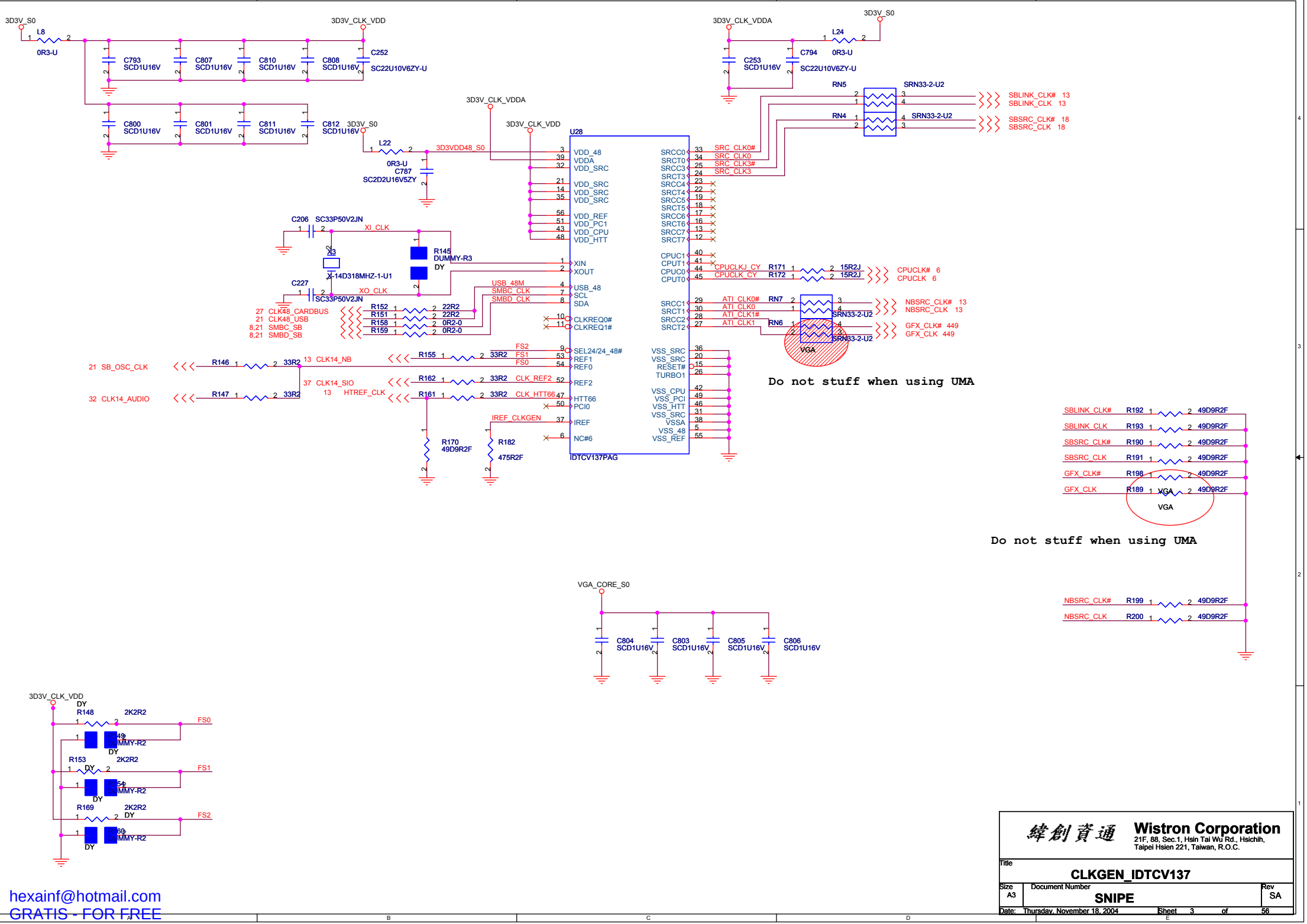
Title	CHANGE HISTORY	
Size A3	Document Number SNIPE	Rev SA
Date: Thursday, November 18, 2004	Sheet 2 of 56	



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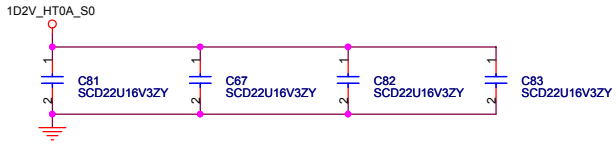
Title: **CLKGEN_IDTCV137**

Size	Document Number	Rev
A3	SNIPE	SA

Date: Thursday, November 18, 2004 Sheet 3 of 56



HTT for CPU sideA Transmit power and NB sideA Receive power

HTT for CPU sideB Receive power and NB sideA Transmit power

LAYOUT: Place bypass cap on topside of board near HTT power pins that are not connected directly to downstream HTT device, but connected internally to other HTT power pins.

By ME requset U11 P/N:
Main 62.10030.041
Second 62.10053.191
Third 62.10053.201

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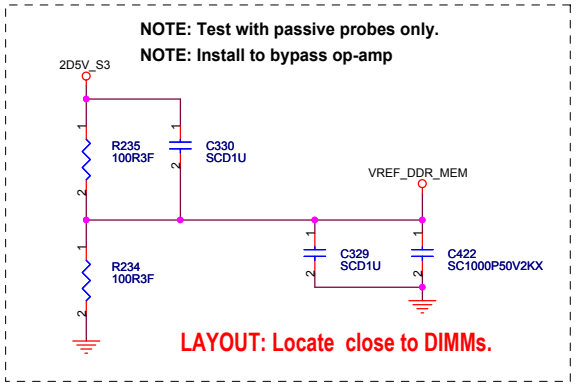
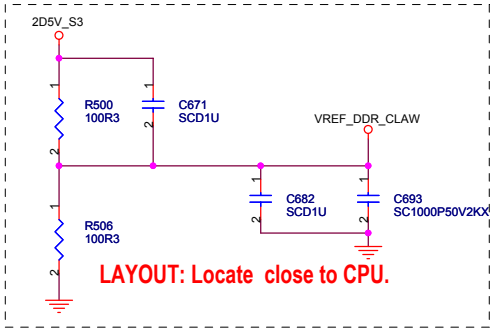
Title	CPU(1/4)_HyperTransport I/F
Size A3 / Document Number	SNIPE
Rev	SA
Date: Thursday, November 18, 2004	Sheet 4 of 56

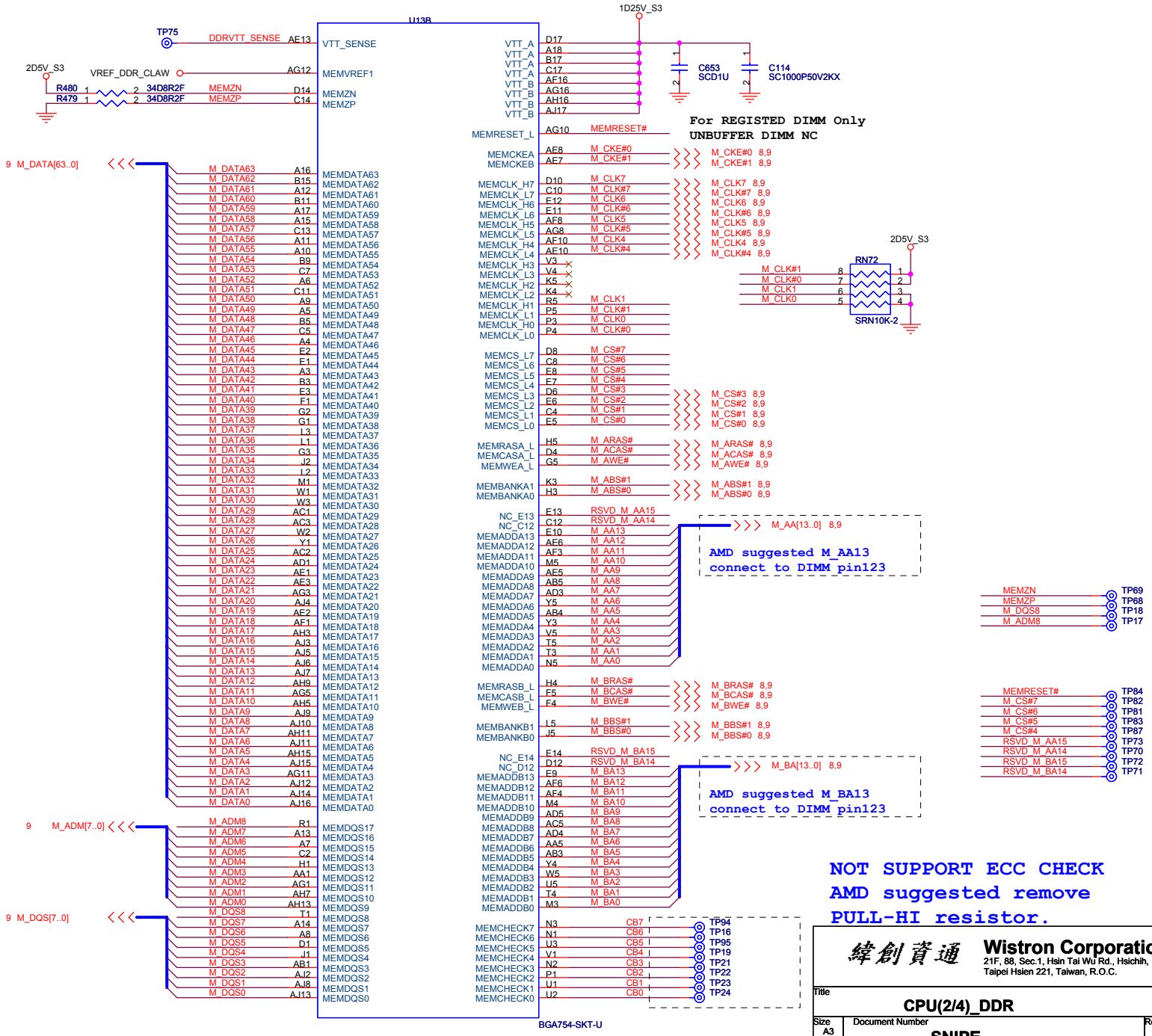
VREF_DDR_MEM



NOTE: Remove to bypass op-amp

VREF_DDR_CLAW





NOT SUPPORT ECC CHECK
AMD suggested remove
PULL-HI resistor.

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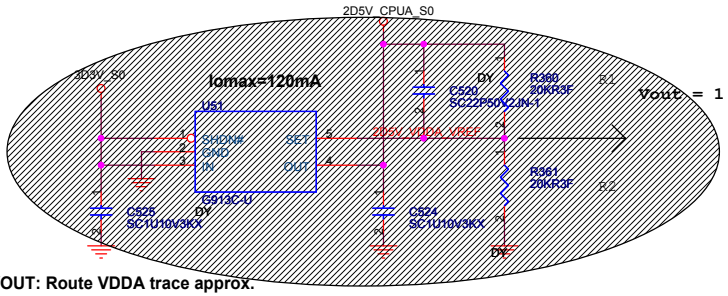
Title: CPU(2/4)_DDR

Size: A3 | Document Number: SNIPE | Rev: SA

Date: Thursday, November 18, 2004 | Sheet 5 of 56

2D5V_VDDA_S0



2D5V_S0 — R385 0R3-U — 2D5V_CPUR_S0 — C544 SC10U10V5ZY

AMD SUGGEST TO USE 100 ~ 300UH

Change L270H

2D5V_VDDA_S0

2D5V_CPUA_S0 — R362 0R3-U — L19 0R5J — DY 63.R0004.151 — TC9 ST100U4VBM-1

C543 SC4D7U10V5ZY 78.47593.411

LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.

LAYOUT: Route VDDA trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.

C556 SC3300P50V2KX — C571 SCD22U16V3ZY

1D2V_HT0A_S0 — R389 44D2R3F — R388 44D2R3F — 64.44R25.551

C535 SC1000P50V2KX — C534 SC1000P50V2KX

AMD SUGGEST TO USE 2D5V_CPUA_S0

KEMET,NT:5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A,ESR=70mohm

SANYO, NT$:6.1
Iripple=1.1A,ESR=70mohm
3.5/2.8/2.0
77.21071.031

AMD suggest voltege from 2D5V_S0 to 2D5V_S3 differentially impedance 100

2D5V_S3 — R428 820R3 — R415 820R3

CPUCLK — C584 SC3900P50V3KX — CPUCLK# — C581 SC3900P50V3KX

R431 169R3F

1D25V_S3

2D5V_S0 — LDT_RST# — SB_CPUPWRGD — LDT_STP# — R441 680R3 — R440 680R3 — R408 680R3

2D5V_S0 — R89 680R3 — R88 680R3

U13C

VDDA1 VDDA2 — RESET_L PWROK LDTSTOP_L — L0_REF1 L0_REF0 — COREFB_H COREFB_L CORE_SENSE — VDDIOFB_H VDDIOFB_L VDDIO_SENSE — CLKIN_H CLKIN_L — NC_AJ23 NC_AH23 NC_AE24 NC_AF24 — VTT_A VTT_B — DBRDY — NC_C15 — TMS TCK TRST_L TDI — NC_C18 NC_A19 — KEY1 KEY0 — NC_AE23 NC_AF23 NC_AF22 NC_AF21 — NC_C1 NC_J3 NC_R3 NC_AA2 NC_AA2 NC_D3 NC_AG2 NC_B18 NC_AH1 NC_AE21 NC_C20 NC_AG4 NC_C6 NC_AG6 NC_AE9 NC_AG9

THERMTRIP_L — THERMTRIP# — THERMDA THERMDC — THERMDP 23 THERMDN 23 — VID[4..0] 41 — NC_AG18 NC_AH18 NC_AG17 NC_AJ18 — TP62 TP63

FBCLKOUT_H FBCLKOUT_L — FBCLKOUT FBCLKOUTJ — R452 80D6R3F-U

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

DBREQ_L — DBREQJ — DY — 51Ω MMY-R3

NC_D20 NC_C21 NC_D18 NC_C19 NC_B19 — TDO — NC_AF18 — 2D5V_S3

Connect to VDDIO for AMD suggest.

NC_D22 NC_C22 — NC_B13 NC_B7 NC_C3 NC_K1 NC_R2 NC_AA3 NC_F3 NC_C23 NC_AG7 NC_AE22 NC_C24 NC_A25 NC_C9

BGA754-SKT-U

HDT Connectors

2D5V_S0 — C518 SCD1U — RN66 SRN680-U — R356 680R3 — R357 680R3

DBRDY TMS TDI TRST_L TDO — DY

2D5V_S3 — R359 680R3 — DY

Add HDT connector for AMD suggested

2D5V_S0 — C519 SCD1U — CN5 — SMC-CONN26A-FP 20.F0357.025 — DY

RN67 SRN680-U — DY

CHANGE FROM 1KR3 TO 680R2 FOR AMD CHECK LIST

RN70 SRN680-U — NC_AG17 NC_AJ18 NC_D18

RN3 SRN680-U — NC_B19 NC_C19 NC_D20 NC_C21

2D5V_S0 — R427 680R3 — 3D3V_S5 — R392 10KR2 — THERMTRIP# — Q26 MMBT3904-U1 — CPU_THERMTRIP# 21,23

2D5V_S0 — NS3 — R414 1KR3

THERMTRIP#Level shift to SB400

Validation Test Points

LAYOUT: Place close to the CPU.

NC_C15 NC_AE23 NC_AF23 NC_AF22 NC_AF21 — TP66 TP51 TP52 TP53 TP54

LDT_RST# CLKIN CLKIN# CORE_SENSE VDDIOFB VDDIOFBJ VDDIOSENSE NC_AE24 NC_AF24 — TP60 TP58 TP59 TP56 TP76 TP77 TP74 TP55 TP57

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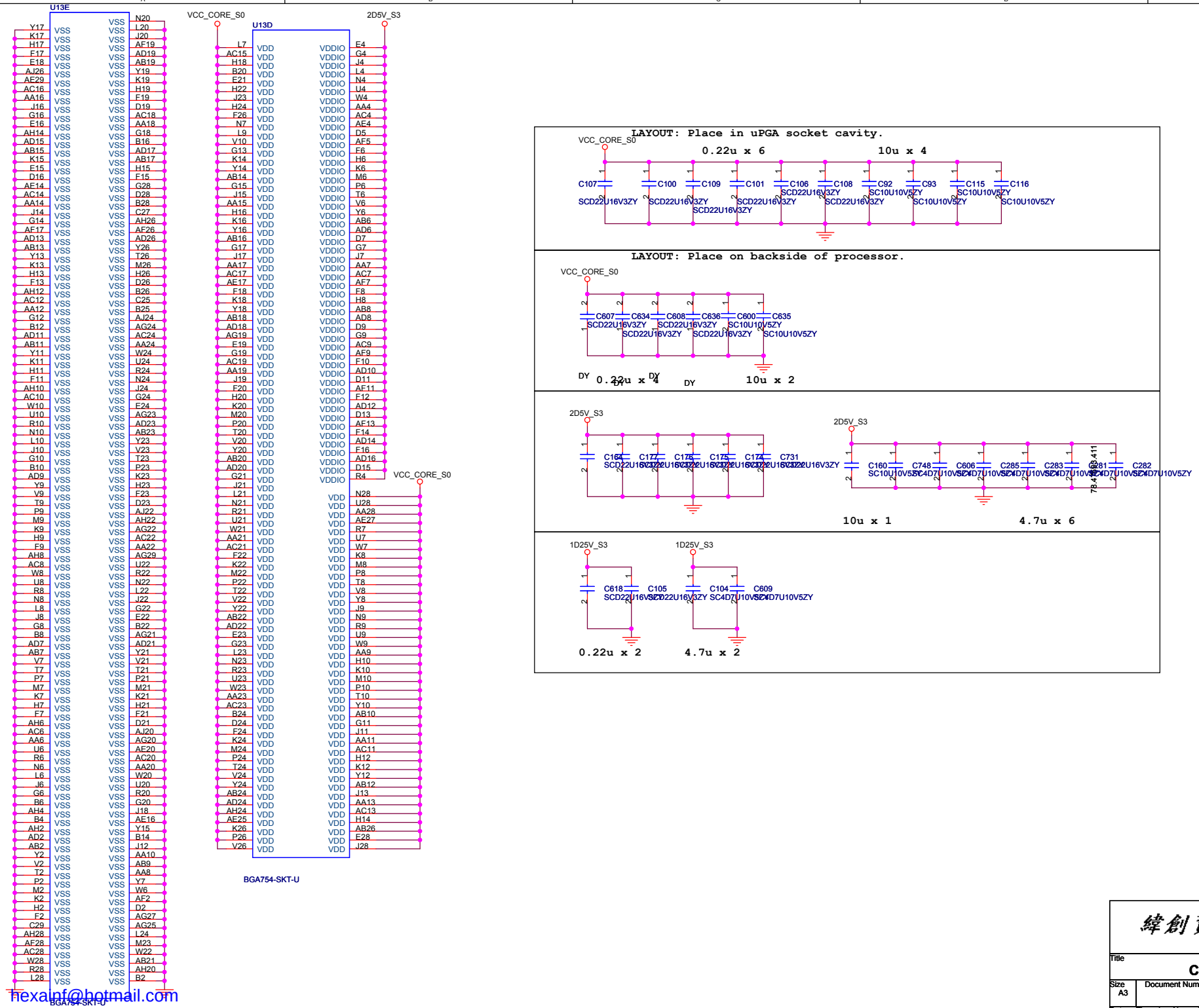
Title: CPU(3/4)_Control & Debug

Size: A3 | Document Number: SNIPE | Rev: SA

Date: Thursday, November 18, 2004 | Sheet 6 of 56



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Title	CPU(4/4)_Power	
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 7 of 56	

DM1

NORMAL TYPE

DDR-SODIMM-N-U1

NOT SUPPORT ECC CHECK
AMD suggested pull-low

Layout trace 20 mil

DM2

REVERSE TYPE

DDR-SODIMM-R-U2

Layout trace 20 mil

By ME requset DM1 P/N:
Main 62.10017.191
Second 62.10017.381

By ME requset DM2 P/N:
Main 62.10017.201
Second 62.10017.371
Third 62.10017.701

DY

AMD K8
ClawHummar

MD63 SMA11 SMA10 SMA0 SMA14 SMA12 MD0

DDR SOCKET PLACEMENT

TOP VIEW PERSPECTIVE DRAWING

DM1

Pin 200 Pin 2 Pin 199 Pin 1

DM2(Reverse)

Pin 200 Pin 2 Pin 199 Pin 1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR SO-DIMM SKT

Size	Document Number	Rev
A3	SNIPE	SA

Date: Thursday, November 18, 2004 Sheet 8 of 56

SERIES DAMPING

PLACE RNs CLOSE TO FIRST DM (DM1), < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS,
CB PINS

RN21
M_DATA4 1 16 M_DATA_R_4
M_DATA5 2 15 M_DATA_R_5
M_ADM0 3 14 M_ADM_R0
M_DATA6 4 13 M_DATA_R_6
M_DATA7 5 12 M_DATA_R_7
M_DATA13 6 11 M_DATA_R_13
M_DATA12 7 10 M_DATA_R_12
M_ADM1 8 9 M_ADM_R1
SRN10J-3

RN18
M_DATA34 1 16 M_DATA_R_34
M_DATA32 2 15 M_DATA_R_32
M_DQS4 3 14 M_DQS_R4
M_DATA33 4 13 M_DATA_R_33
M_DATA36 5 12 M_DATA_R_36
M_DATA37 6 11 M_DATA_R_37
M_ADM4 7 10 M_ADM_R4
M_DATA39 8 9 M_DATA_R_39
SRN10J-3

RN34
M_DATA1 1 16 M_DATA_R_1
M_DATA0 2 15 M_DATA_R_0
M_DQS0 3 14 M_DQS_R0
M_DATA2 4 13 M_DATA_R_2
M_DATA3 5 12 M_DATA_R_3
M_DATA8 6 11 M_DATA_R_8
M_DATA9 7 10 M_DATA_R_9
M_DQS1 8 9 M_DQS_R1
SRN10J-3

RN28
M_DATA35 1 16 M_DATA_R_35
M_DATA41 2 15 M_DATA_R_41
M_DATA40 3 14 M_DATA_R_40
M_DQS5 4 13 M_DQS_R5
M_DATA42 5 12 M_DATA_R_42
M_DATA43 6 11 M_DATA_R_43
M_DATA49 7 10 M_DATA_R_49
M_DATA48 8 9 M_DATA_R_48
SRN10J-3

RN20
M_DATA14 1 16 M_DATA_R_14
M_DATA15 2 15 M_DATA_R_15
M_DATA21 3 14 M_DATA_R_21
M_DATA20 4 13 M_DATA_R_20
M_ADM2 5 12 M_ADM_R2
M_DATA23 6 11 M_DATA_R_23
M_DATA22 7 10 M_DATA_R_22
M_DATA25 8 9 M_DATA_R_25
SRN10J-3

RN17
M_DATA38 1 16 M_DATA_R_38
M_DATA45 2 15 M_DATA_R_45
M_DATA44 3 14 M_DATA_R_44
M_ADM5 4 13 M_ADM_R5
M_DATA47 5 12 M_DATA_R_47
M_DATA46 6 11 M_DATA_R_46
M_DATA53 7 10 M_DATA_R_53
M_DATA52 8 9 M_DATA_R_52
SRN10J-3

RN33
M_DATA11 1 16 M_DATA_R_11
M_DATA10 2 15 M_DATA_R_10
M_DATA17 3 14 M_DATA_R_17
M_DATA16 4 13 M_DATA_R_16
M_DQS2 5 12 M_DQS_R2
M_DATA19 6 11 M_DATA_R_19
M_DATA18 7 10 M_DATA_R_18
M_DATA24 8 9 M_DATA_R_24
SRN10J-3

RN27
M_DQS6 1 16 M_DQS_R6
M_DATA50 2 15 M_DATA_R_50
M_DATA51 3 14 M_DATA_R_51
M_DATA56 4 13 M_DATA_R_56
M_DATA57 5 12 M_DATA_R_57
M_DQS7 6 11 M_DQS_R7
M_DATA58 7 10 M_DATA_R_58
M_DATA59 8 9 M_DATA_R_59
SRN10J-3

RN19
M_DATA29 1 16 M_DATA_R_29
M_DATA28 2 15 M_DATA_R_28
M_DQS3 3 14 M_DQS_R3
M_ADM3 4 13 M_ADM_R3
M_DATA26 5 12 M_DATA_R_26
M_DATA27 6 11 M_DATA_R_27
M_DATA30 7 10 M_DATA_R_30
M_DATA31 8 9 M_DATA_R_31
SRN10J-3

RN16
M_ADM6 1 16 M_ADM_R6
M_DATA54 2 15 M_DATA_R_54
M_DATA55 3 14 M_DATA_R_55
M_DATA61 4 13 M_DATA_R_61
M_DATA60 5 12 M_DATA_R_60
M_ADM7 6 11 M_ADM_R7
M_DATA62 7 10 M_DATA_R_62
M_DATA63 8 9 M_DATA_R_63
SRN10J-3

5,8 M_CKE#0 M_CKE#0
5,8 M_CKE#1 M_CKE#1

05/10
Remove the damping resistor for AMD suggest.

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)
NO EQUAL LENGTH LIMITATION

1D25V_S3

RN44
M_ADM_R1 1 16 M_DATA_R_36
M_DATA_R_13 2 15 M_DATA_R_32
M_DATA_R_12 3 14 M_DATA_R_37
M_DATA_R_6 4 13 M_DATA_R_33
M_DATA_R_7 5 12 M_ADM_R4
M_ADM_R0 6 11 M_DQS_R4
M_DATA_R_5 7 10 M_DATA_R_38
M_DATA_R_4 8 9 M_DATA_R_39
SRN68J-1

RN38
1 16 M_DATA_R_36
2 15 M_DATA_R_32
3 14 M_DATA_R_37
4 13 M_DATA_R_33
5 12 M_ADM_R4
6 11 M_DQS_R4
7 10 M_DATA_R_38
8 9 M_DATA_R_39
SRN68J-1

RN52
M_DATA_R_1 1 16 M_DATA_R_48
M_DATA_R_0 2 15 M_DATA_R_49
M_DQS_R0 3 14 M_DATA_R_43
M_DATA_R_2 4 13 M_DATA_R_42
M_DATA_R_3 5 12 M_DQS_R5
M_DATA_R_8 6 11 M_DATA_R_41
M_DATA_R_9 7 10 M_DATA_R_40
M_DQS_R1 8 9 M_DATA_R_34
SRN68J-1

RN48
1 16 M_DATA_R_48
2 15 M_DATA_R_49
3 14 M_DATA_R_43
4 13 M_DATA_R_42
5 12 M_DQS_R5
6 11 M_DATA_R_41
7 10 M_DATA_R_40
8 9 M_DATA_R_34
SRN68J-1

RN43
M_DATA_R_25 1 16 M_DATA_R_35
M_DATA_R_22 2 15 M_DATA_R_46
M_DATA_R_23 3 14 M_DATA_R_47
M_ADM_R2 4 13 M_ADM_R5
M_DATA_R_20 5 12 M_DATA_R_44
M_DATA_R_21 6 11 M_DATA_R_45
M_DATA_R_14 7 10 M_DATA_R_53
M_DATA_R_15 8 9 M_DATA_R_52
SRN68J-1

RN37
1 16 M_DATA_R_35
2 15 M_DATA_R_46
3 14 M_DATA_R_47
4 13 M_ADM_R5
5 12 M_DATA_R_44
6 11 M_DATA_R_45
7 10 M_DATA_R_53
8 9 M_DATA_R_52
SRN68J-1

RN51
M_DATA_R_11 1 16 M_DATA_R_59
M_DATA_R_10 2 15 M_DATA_R_58
M_DATA_R_16 3 14 M_DQS_R7
M_DATA_R_17 4 13 M_DATA_R_57
M_DQS_R2 5 12 M_DATA_R_56
M_DATA_R_19 6 11 M_DATA_R_51
M_DATA_R_18 7 10 M_DATA_R_50
M_DATA_R_24 8 9 M_DQS_R6
SRN68J-1

RN47
1 16 M_DATA_R_59
2 15 M_DATA_R_58
3 14 M_DQS_R7
4 13 M_DATA_R_57
5 12 M_DATA_R_56
6 11 M_DATA_R_51
7 10 M_DATA_R_50
8 9 M_DQS_R6
SRN68J-1

RN42
M_DATA_R_30 1 16 M_DATA_R_55
M_DATA_R_31 2 15 M_DATA_R_54
M_DATA_R_26 3 14 M_ADM_R6
M_DATA_R_27 4 13 M_DATA_R_60
M_ADM_R3 5 12 M_DATA_R_61
M_DQS_R3 6 11 M_ADM_R7
M_DATA_R_29 7 10 M_DATA_R_63
M_DATA_R_28 8 9 M_DATA_R_62
SRN68J-1

RN36
1 16 M_DATA_R_55
2 15 M_DATA_R_54
3 14 M_ADM_R6
4 13 M_DATA_R_60
5 12 M_DATA_R_61
6 11 M_ADM_R7
7 10 M_DATA_R_63
8 9 M_DATA_R_62
SRN68J-1

1D25V_S3

RN50
M_CKE#1 2 3
M_BA12 1 4
SRN47J

RN32
M_CKE#0 2 3
M_AA12 1 4
SRN47J

RN31
M_AA11 1 16
M_AA9 2 15
M_AA7 3 14
M_AA5 4 13
M_AA4 5 12
M_AA8 6 11
M_AA6 7 10
M_AA3 8 9
SRN47J-1-U

RN39
M_CS#3 1 16
M_BA13 2 15
M_CS#2 3 14
M_BRAS# 4 13
M_BBS#1 5 12
M_BCAS# 6 11
M_BA0 7 10
M_BA2 8 9
SRN47J-1-U

RN30
M_AA1 1 16
M_AA10 2 15
M_AA2 3 14
M_AA0 4 13
M_ABS#1 5 12
M_ARAS# 6 11
M_AWE# 7 10
M_ABS#0 8 9
SRN47J-1-U

RN49
M_BA7 1 16
M_BA3 2 15
M_BA6 3 14
M_BA9 4 13
M_BA10 5 12
M_BA1 6 11
M_BBS#0 7 10
M_BWE# 8 9
SRN47J-1-U

RN40
M_BA5 1 8
M_BA8 2 7
M_BA11 3 6
M_BA4 4 5
SRN47-1

RN29
M_AA13 1 8
M_CS#0 2 7
M_CS#1 3 6
M_ACAS# 4 5
SRN47-1

M_ADM_R[7..0] 8
M_ADM[7..0] 5
M_DATA[63..0] 5
M_DATA_R_[63..0] 8
M_DQS[7..0] 5
M_DQS_R[7..0] 8
M_AA[13..0] 5,8
M_ABS#[1..0] 5,8
M_BA[13..0] 5,8
M_BBS#[1..0] 5,8
M_AWE# 5,8
M_ACAS# 5,8
M_ARAS# 5,8
M_BWE# 5,8
M_BCAS# 5,8
M_BRAS# 5,8
M_CS#0 5,8
M_CS#1 5,8
M_CS#2 5,8
M_CS#3 5,8

Place it near CPU

1 R498 121R3F M_CLK7 M_CLK#7 M_CLK7 5,8 M_CLK#7 5,8
1 R481 121R3F M_CLK6 M_CLK#6 M_CLK6 5,8 M_CLK#6 5,8
1 R499 121R3F M_CLK5 M_CLK#5 M_CLK5 5,8 M_CLK#5 5,8
1 R486 121R3F M_CLK4 M_CLK#4 M_CLK4 5,8 M_CLK#4 5,8

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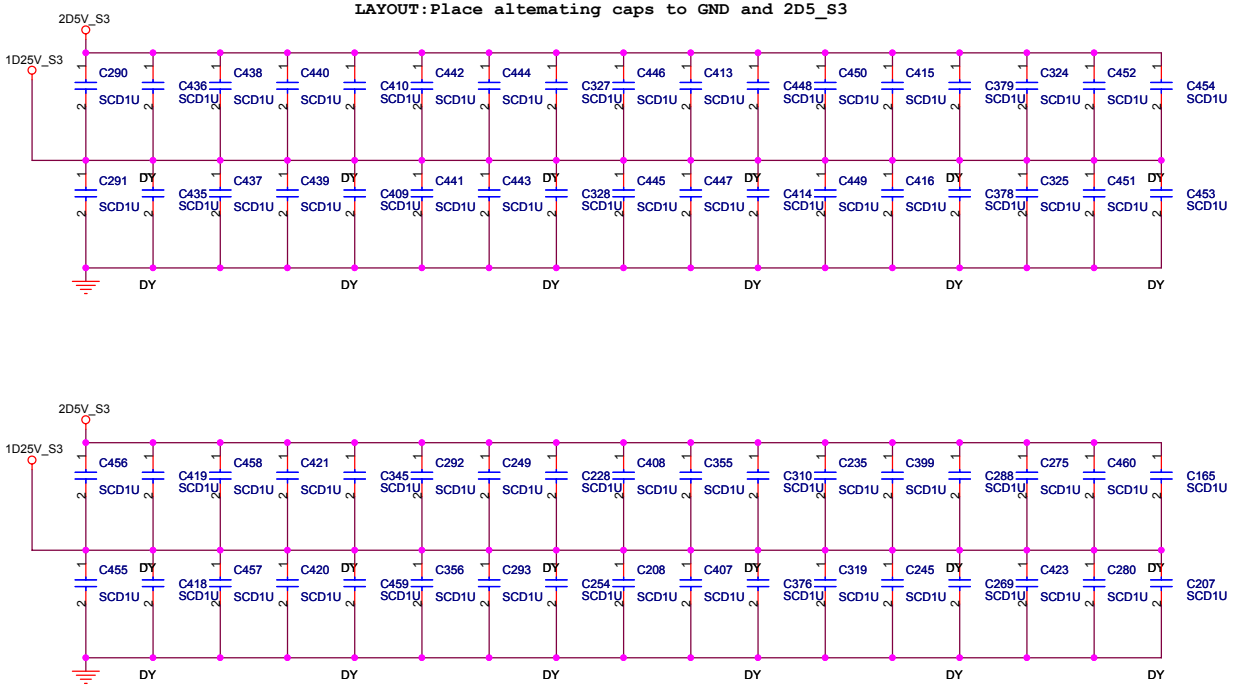
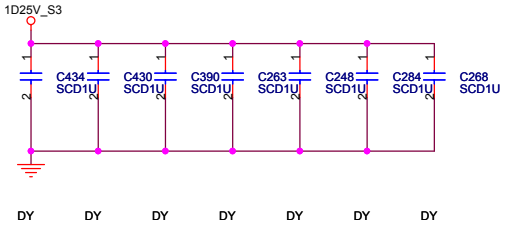
Taipei Hsien 221, Taiwan, R.O.C.

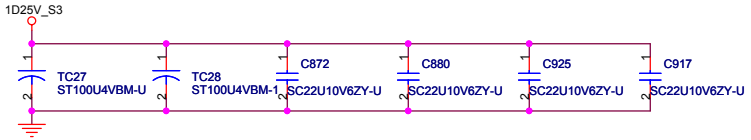
Title: DDR DAMPING & TERMINATION
Size: A3 | Document Number: SNIPE | Rev: SA
Date: Thursday, November 18, 2004 | Sheet 9 of 56

LAYOUT:Place altemating caps to GND and 2D5_S3

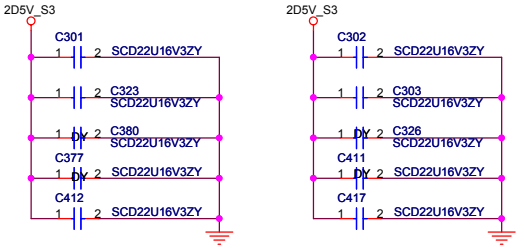




LAYOUT:Place at end of the DIMMs



LAYOUT:Place close to Power Pin of DDR socket.



0.22u x 10

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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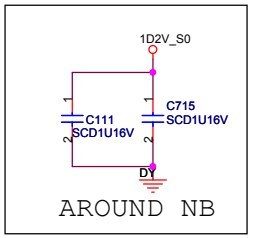
Title: **DDR DECOUPLING**

Size	Document Number	Rev
A3	SNIPE	SA

Date: Thursday, November 18, 2004 Sheet 10 of 56

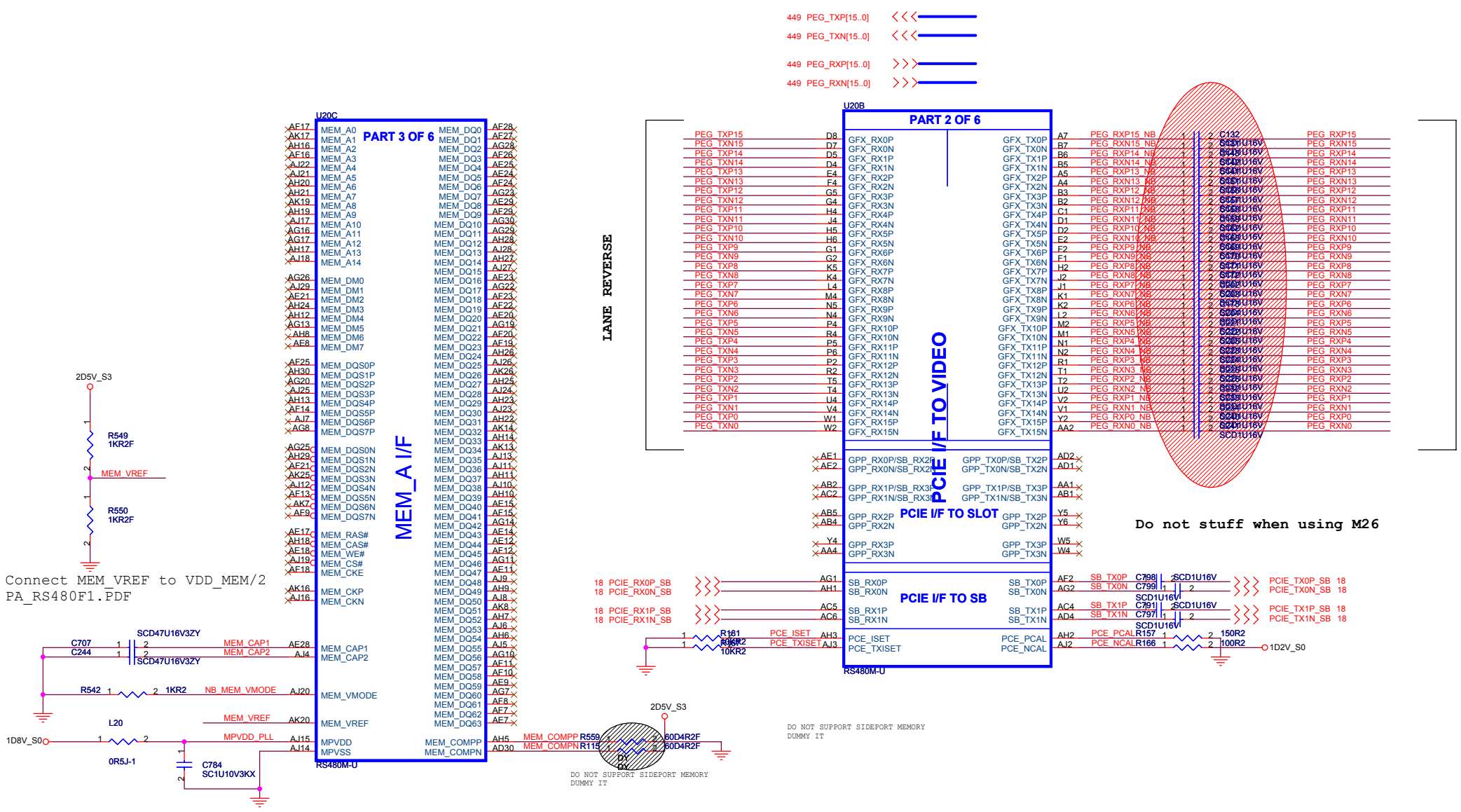
CLAW HAMMER TO NB

NB TO CLAW HAMMER



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	NB-RS480M_HT	
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 11 of 56	



When disable local frame buffer,
VDD_MEM connect to 2D5V_S3, MEM_VMODE
connect to GND, MEM_VREF connect to
2D5V_S3, MPVDD connected to 1D8V
DSG-215-RS480-04.PDF

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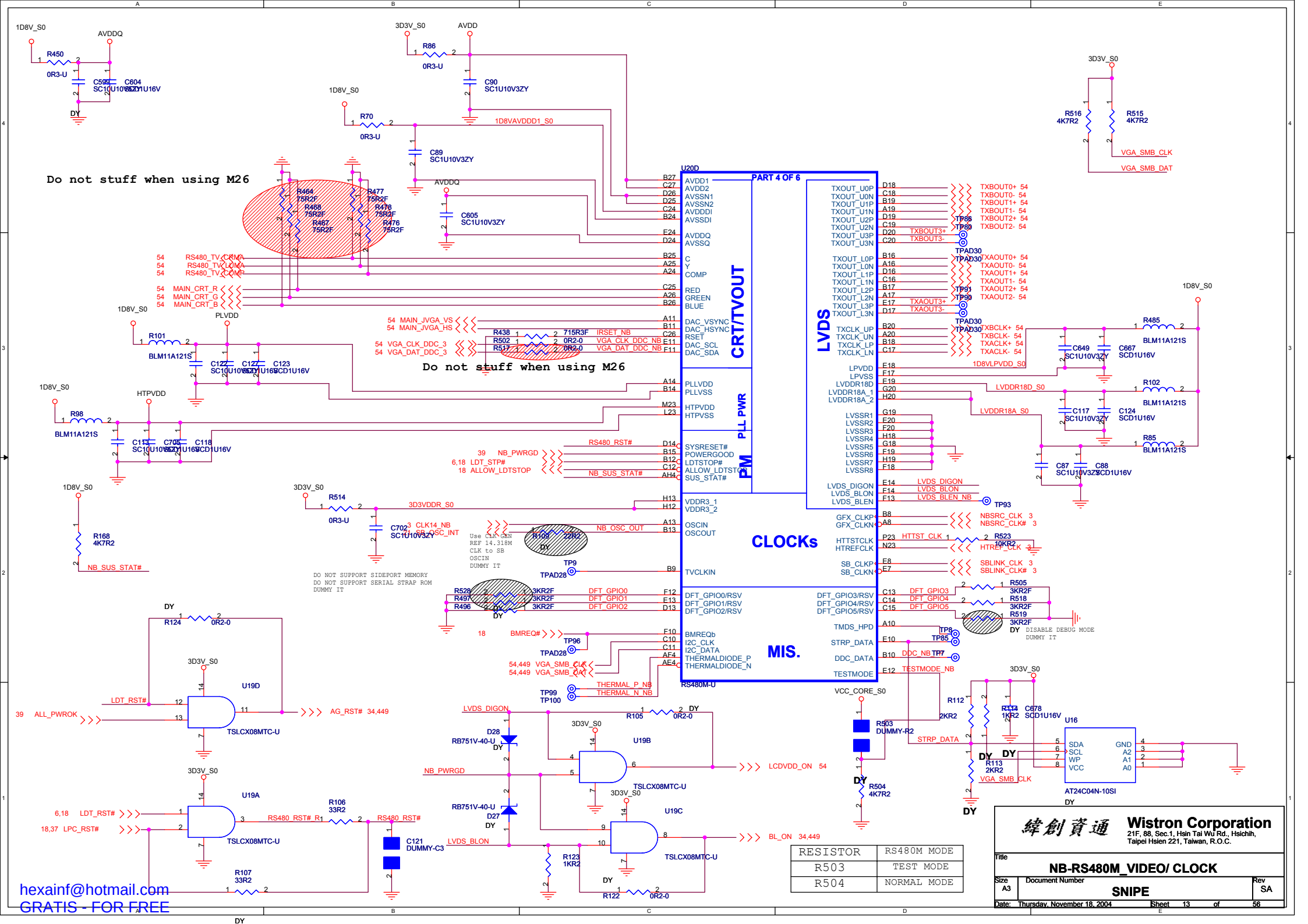
Title	NB-RS480M_MEM/PCIE_LINK I/F	
Size A3	Document Number SNIPE	Rev SA
Date: Thursday, November 18, 2004	Sheet 12 of 56	


Do not stuff when using M26
Do not stuff when using M26
U20D
PART 4 OF 6
CRT/TVOUT
PLL PWR
PM
CLOCKs
MIS.
LVDS
RS480M-U
AVDD1
AVDD2
AVSSN1
AVSSN2
AVDDDI
AVSSDI
AVDDQ
AVSSQ
C
Y
COMP
RED
GREEN
BLUE
DAC_VSYNC
DAC_HSYNC
RSET
DAC_SCL
DAC_SDA
PLLVDD
PLLVSS
HTPVDD
HTPVSS
SYSRESET#
POWERGOOD
LDTSTOP#
ALLOW_LDTSTOP
SUS_STAT#
VDDR3_1
VDDR3_2
OSCIN
OSCOUT
TVCLKIN
DFT_GPIO0/RSV
DFT_GPIO1/RSV
DFT_GPIO2/RSV
DFT_GPIO3/RSV
DFT_GPIO4/RSV
DFT_GPIO5/RSV
BMREQb
I2C_CLK
I2C_DATA
THERMALDIODE_P
THERMALDIODE_N
TMDS_HPD
STRP_DATA
DDC_DATA
TESTMODE
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
TXCLK_UP
TXCLK_UN
TXCLK_LP
TXCLK_LN
LVDS_DIGON
LVDS_BLON
LVDS_BLEN
GFX_CLKP
GFX_CLKN
HTTSTCLK
HTREFCLK
SB_CLKP
SB_CLKN
LVDDR18D
LVDDR18A_1
LVDDR18A_2
LVSSR1
LVSSR2
LVSSR3
LVSSR4
LVSSR5
LVSSR6
LVSSR7
LVSSR8
LPVDD
LPVSS
1D8V_S0
3D3V_S0
AVDDQ
AVDD
1D8VAVDDD1_S0
PLVDD
HTPVDD
3D3VDDR_S0
VCC_CORE_S0
LVDDR18D_S0
LVDDR18A_S0
1D8VLPVDD_S0
R450
0R3-U
C590
SC1U10V3ZY
C604
SCD1U16V
DY
R86
C90
R70
C89
C605
R464
75R2F
R468
75R2F
R467
75R2F
R477
75R2F
R478
75R2F
R476
75R2F
R101
BLM11A121S
C122
C127
C123
R98
C113
C705
C118
R168
4K7R2
NB_SUS_STAT#
R514
C702
R438
715R3F
IRSET_NB
R502
0R2-0
VGA_CLK_DDC_NB
R517
0R2-0
VGA_DAT_DDC_NB
R516
4K7R2
R515
4K7R2
VGA_SMB_CLK
VGA_SMB_DAT
R485
BLM11A121S
C649
SC1U10V3ZY
C667
SCD1U16V
R102
BLM11A121S
C117
SC1U10V3ZY
C124
SCD1U16V
R85
BLM11A121S
C87
SC1U10V3ZY
C88
SCD1U16V
R523
10KR2
HTREF_CLK
R505
3KR2F
R518
3KR2F
R519
3KR2F
DISABLE DEBUG MODE
DUMMY IT
R124
0R2-0
R528
3KR2F
R497
3KR2F
R496
3KR2F
R105
0R2-0
R106
33R2
R107
33R2
C121
DUMMY-C3
R123
1KR2
R122
0R2-0
R503
DUMMY-R2
R504
4K7R2
R112
2KR2
R114
1KR2
C678
SCD1U16V
R113
2KR2
U16
AT24C04N-10SI
SDA
SCL
WP
VCC
GND
A2
A1
A0
U19A
U19B
U19C
U19D
TSLCX08MTC-U
D28
RB751V-40-U
D27
RB751V-40-U
TP96
TP99
TP100
TP9
TP8
TP85
TP7
TP93
TPAD28
TPAD30
TXBOUT0+ 54
TXBOUT0- 54
TXBOUT1+ 54
TXBOUT1- 54
TXBOUT2+ 54
TXBOUT2- 54
TXBOUT3+
TXBOUT3-
TXAOUT0+ 54
TXAOUT0- 54
TXAOUT1+ 54
TXAOUT1- 54
TXAOUT2+ 54
TXAOUT2- 54
TXAOUT3+
TXAOUT3-
TXBCLK+ 54
TXBCLK- 54
TXACLK+ 54
TXACLK- 54
LVDS_DIGON
LVDS_BLON
LVDS_BLEN_NB
NBSRC_CLK 3
NBSRC_CLK# 3
HTTST_CLK 1
SBLINK_CLK 3
SBLINK_CLK# 3
DFT_GPIO3
DFT_GPIO4
DFT_GPIO5
DDC_NB
TESTMODE_NB
STRP_DATA
VGA_SMB_CLK
RS480_TV_CRMA 54
RS480_TV_LUMA 54
RS480_TV_COMP 54
MAIN_CRT_R 54
MAIN_CRT_G 54
MAIN_CRT_B 54
MAIN_JVGA_VS 54
MAIN_JVGA_HS 54
VGA_CLK_DDC_3 54
VGA_DAT_DDC_3 54
NB_PWRGD 39
LDT_STP# 6,18
ALLOW_LDTSTOP 18
RS480_RST#
NB_SUS_STAT#
CLK14_NB
SB_OSC_INT
NB_OSC_OUT
Use CLK GEN
REF 14.318M
CLK to SB
OSCIN
DUMMY IT
DO NOT SUPPORT SIDEPORT MEMORY
DO NOT SUPPORT SERIAL STRAP ROM
DUMMY IT
BMREQ# 18
VGA_SMB_CLK 54,449
VGA_SMB_DAT 54,449
THERMAL_P_NB
THERMAL_N_NB
LDT_RST#
ALL_PWROK 39
AG_RST# 34,449
LCDVDD_ON 54
BL_ON 34,449
LVDS_DIGON
LVDS_BLON
NB_PWRGD
RS480_RST#_R
6,18 LDT_RST#
18,37 LPC_RST#
RESISTOR
RS480M MODE
R503
TEST MODE
R504
NORMAL MODE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
NB-RS480M_VIDEO/ CLOCK
Size
A3
Document Number
SNIPE
Rev
SA
Date: Thursday, November 18, 2004
Sheet 13 of 56
hexainf@hotmail.com
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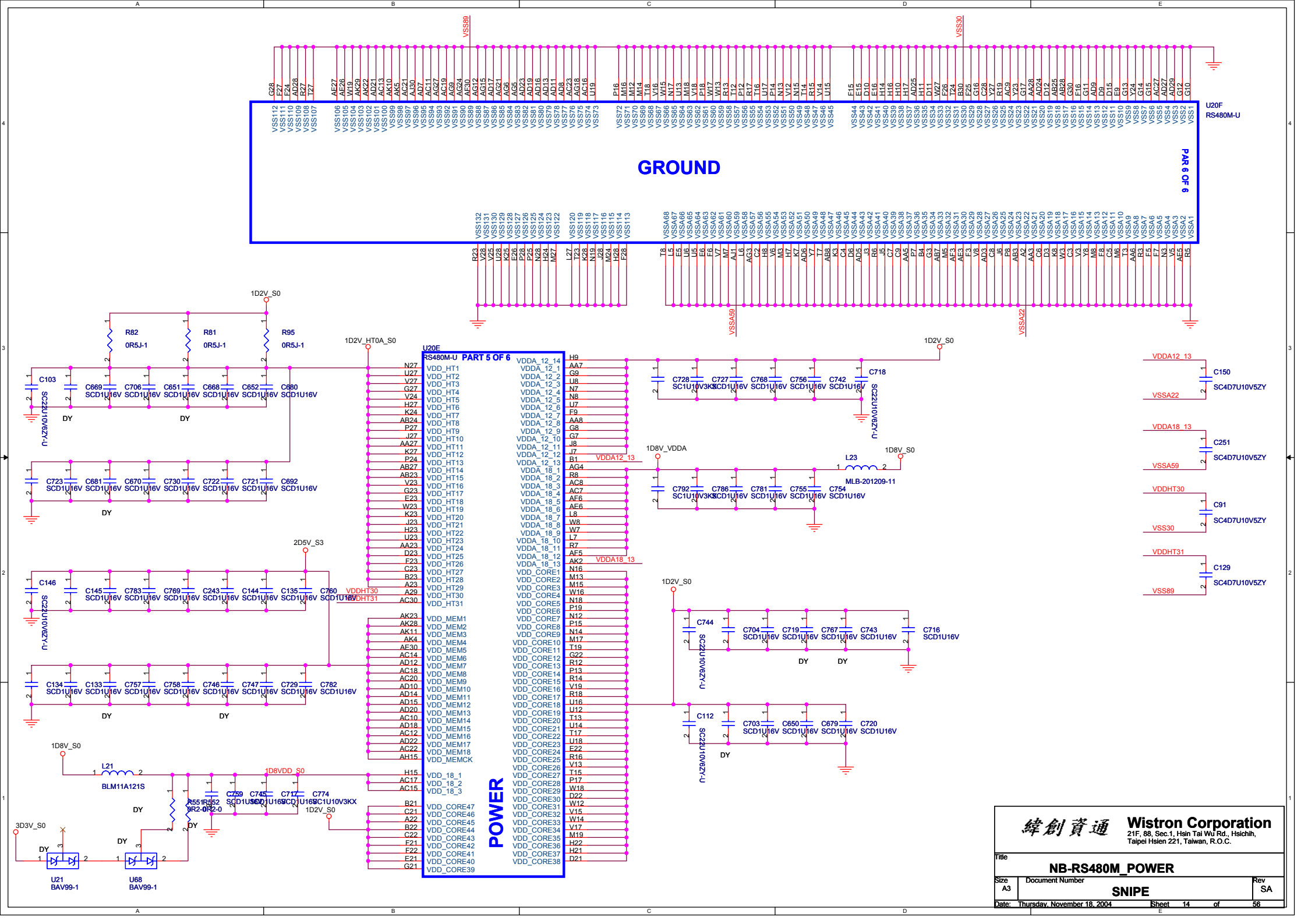
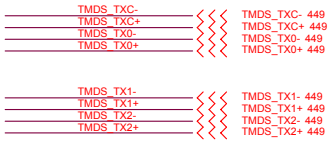
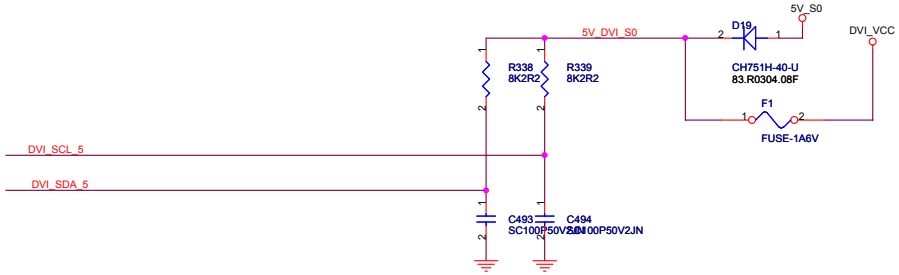
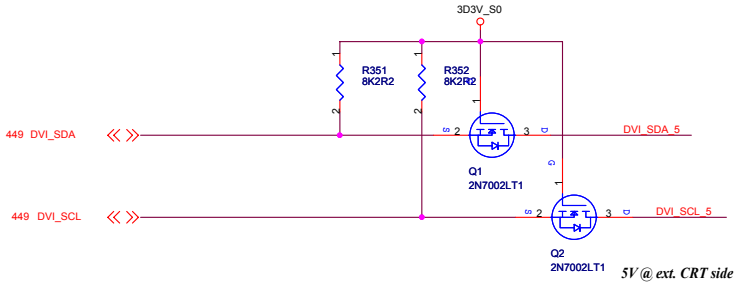
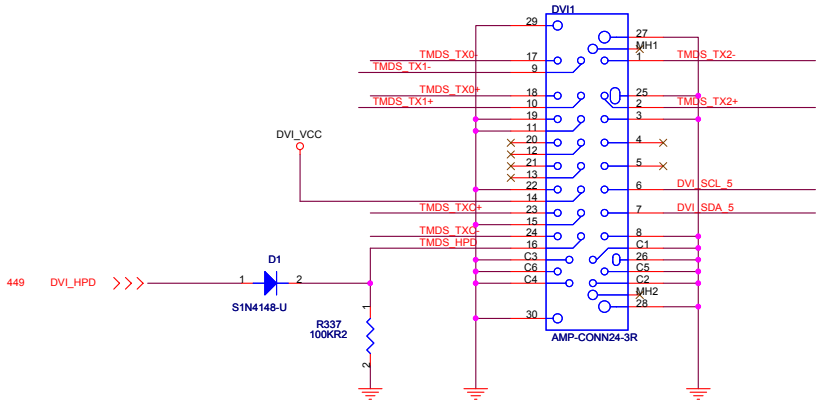

GROUND
U20F
RS480M-U
PART 6 OF 6
U20E
RS480M-U
PART 5 OF 6
POWER
1D2V_S0
1D8V_S0
1D8V_VDDA
2D5V_S3
3D3V_S0
1D2V_HT0A_S0
1D8VDD_S0
VDDA12_13
VDDA18_13
VDDHT30
VDDHT31
R82 0R5J-1
R81 0R5J-1
R95 0R5J-1
L21 BLM11A121S
L23 MLB-201209-11
U21 BAV99-1
U68 BAV99-1
R551 9R2-0
R552 9R2-0
C103 SC22U10V6ZY-U
C669 SCD1U16V
C706 SCD1U16V
C651 SCD1U16V
C668 SCD1U16V
C652 SCD1U16V
C680 SCD1U16V
C723 SCD1U16V
C681 SCD1U16V
C670 SCD1U16V
C730 SCD1U16V
C722 SCD1U16V
C721 SCD1U16V
C692 SCD1U16V
C146 SC22U10V6ZY-U
C145 SCD1U16V
C783 SCD1U16V
C769 SCD1U16V
C243 SCD1U16V
C144 SCD1U16V
C135 SCD1U16V
C760 SCD1U16V
C134 SCD1U16V
C133 SCD1U16V
C757 SCD1U16V
C758 SCD1U16V
C746 SCD1U16V
C747 SCD1U16V
C729 SCD1U16V
C782 SCD1U16V
C759 SCD1U16V
C745 SCD1U16V
C717 SCD1U16V
C774 SC1U10V3KX
C728 SC1U10V3KX
C727 SCD1U16V
C768 SCD1U16V
C756 SCD1U16V
C742 SCD1U16V
C718 SC22U10V6ZY-U
C792 SC1U10V3KX
C786 SCD1U16V
C781 SCD1U16V
C755 SCD1U16V
C754 SCD1U16V
C744 SC22U10V6ZY-U
C704 SCD1U16V
C719 SCD1U16V
C767 SCD1U16V
C743 SCD1U16V
C716 SCD1U16V
C112 SC22U10V6ZY-U
C703 SCD1U16V
C650 SCD1U16V
C679 SCD1U16V
C720 SCD1U16V
C150 SC4D7U10V5ZY
C251 SC4D7U10V5ZY
C91 SC4D7U10V5ZY
C129 SC4D7U10V5ZY
VDDA12_13
VDDA18_13
VDDHT30
VDDHT31
VSS89
VSS30
VSSA59
VSSA22
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS480M_POWER
Size A3
Document Number
SNIPE
Rev SA
Date: Thursday, November 18, 2004
Sheet 14 of 56





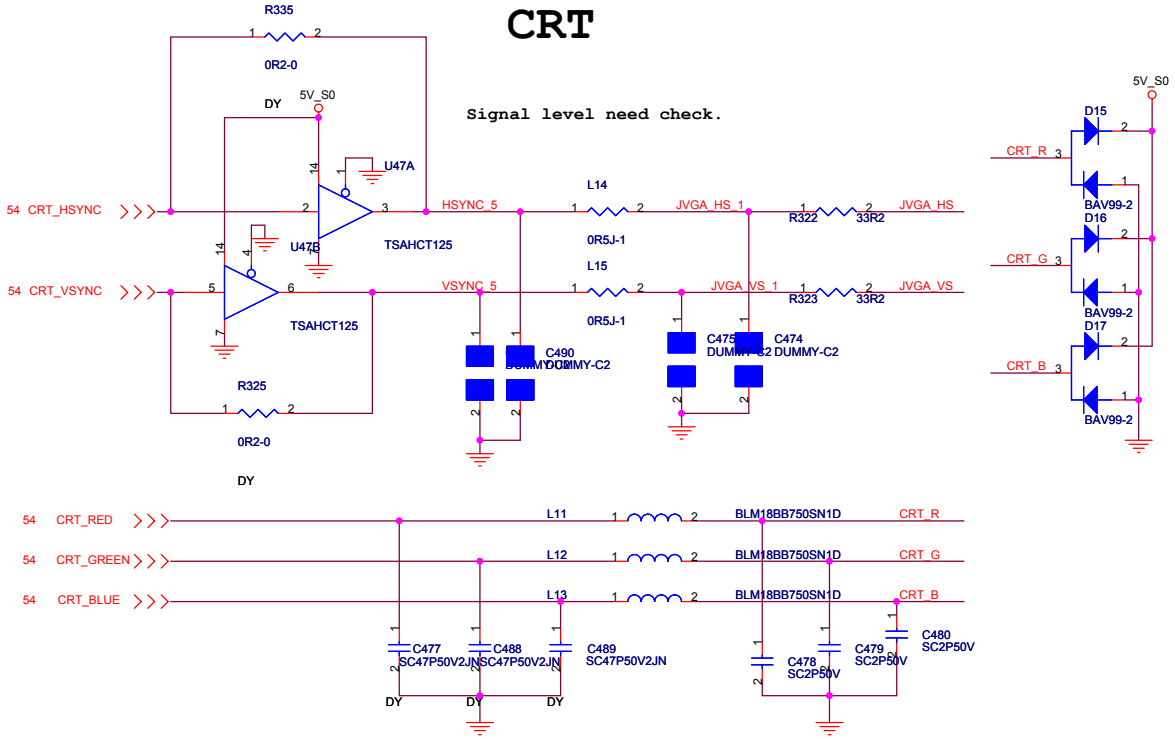
Do not stuff when using UMA





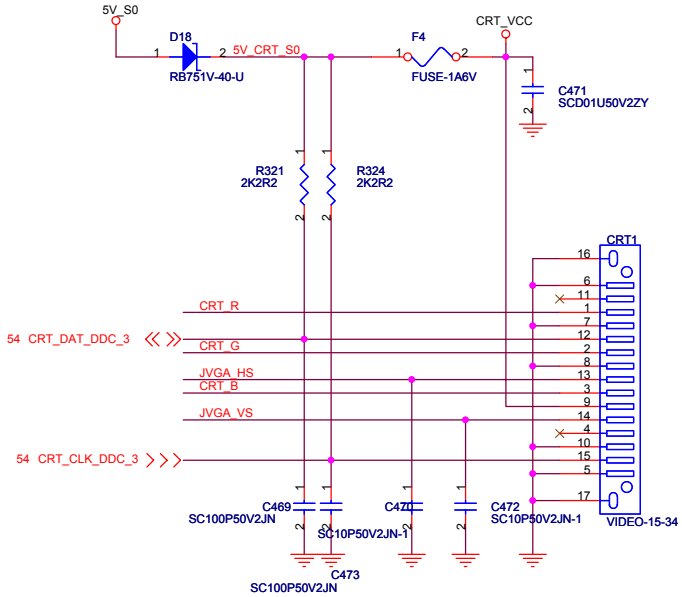
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: DVI CONNECTOR			
Size: Custom	Document Number: SNIPE		Rev: SA
Date: Thursday, November 18, 2004	Sheet 15 of 56		

CRT



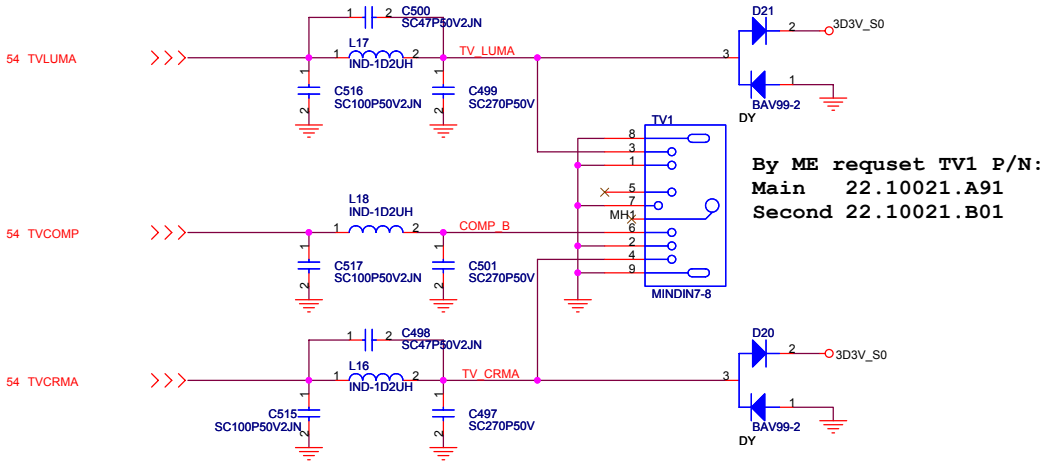
CRT CONN

200mA Rating/Spec 500mA

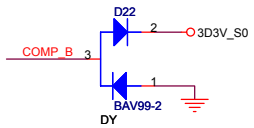


By ME requset CRT1 P/N:
Main 20.B0026.A15
Second 20.B0034.015

TV CONN



By ME requset TV1 P/N:
Main 22.10021.A91
Second 22.10021.B01



緯創資通 Wistron Corporation
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Title	CRT / TV	
Size A3	Document Number SNIPE	Rev SA
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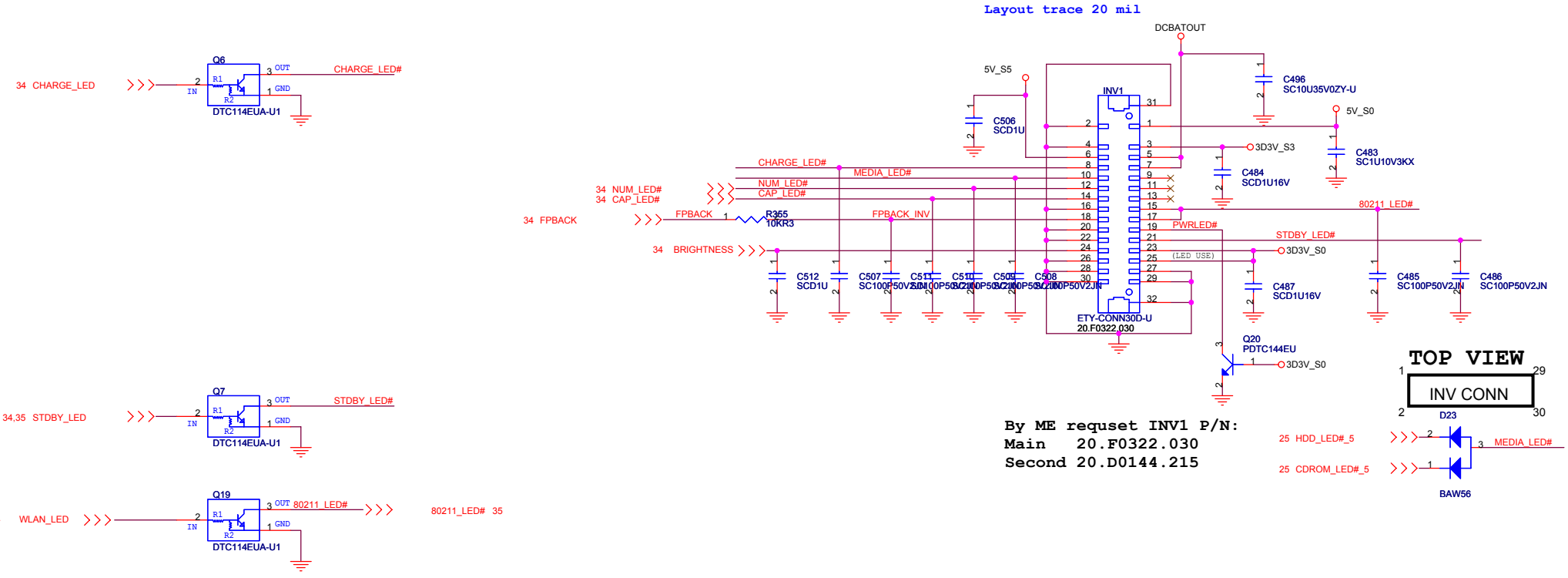
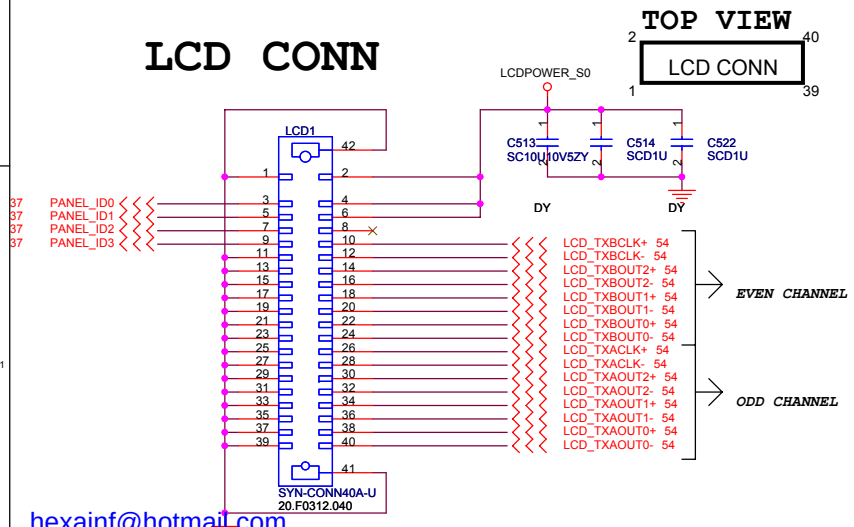
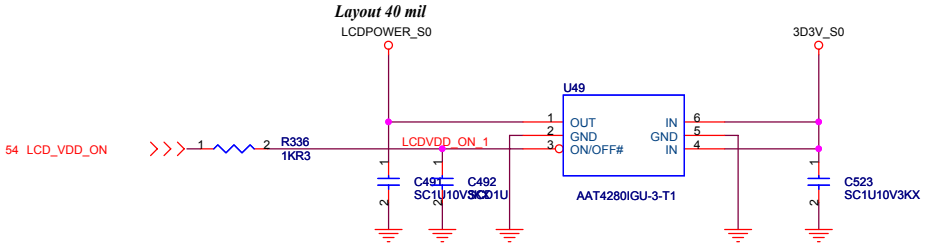
INVERTER/LED



LCD CONN



LCD POWER



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	INV / LCD	
Size A3	Document Number SNIPE	Rev SA
Date: Thursday, November 18, 2004	Sheet 17 of 56	

32K suspend clock output

MAIN SOURCE: 82.30001.031 EPSON
2ND SOURCE: 82.30001.341 KDS

SB400 SB
Part 1 of 4

U84A

CHS-215SB400

PCIRST# 3V to 5V level shift for HDD & CDROM

SB400 asserts PLTRST# to reset devices on the platform.

Secondary PCI Bus reset signal.

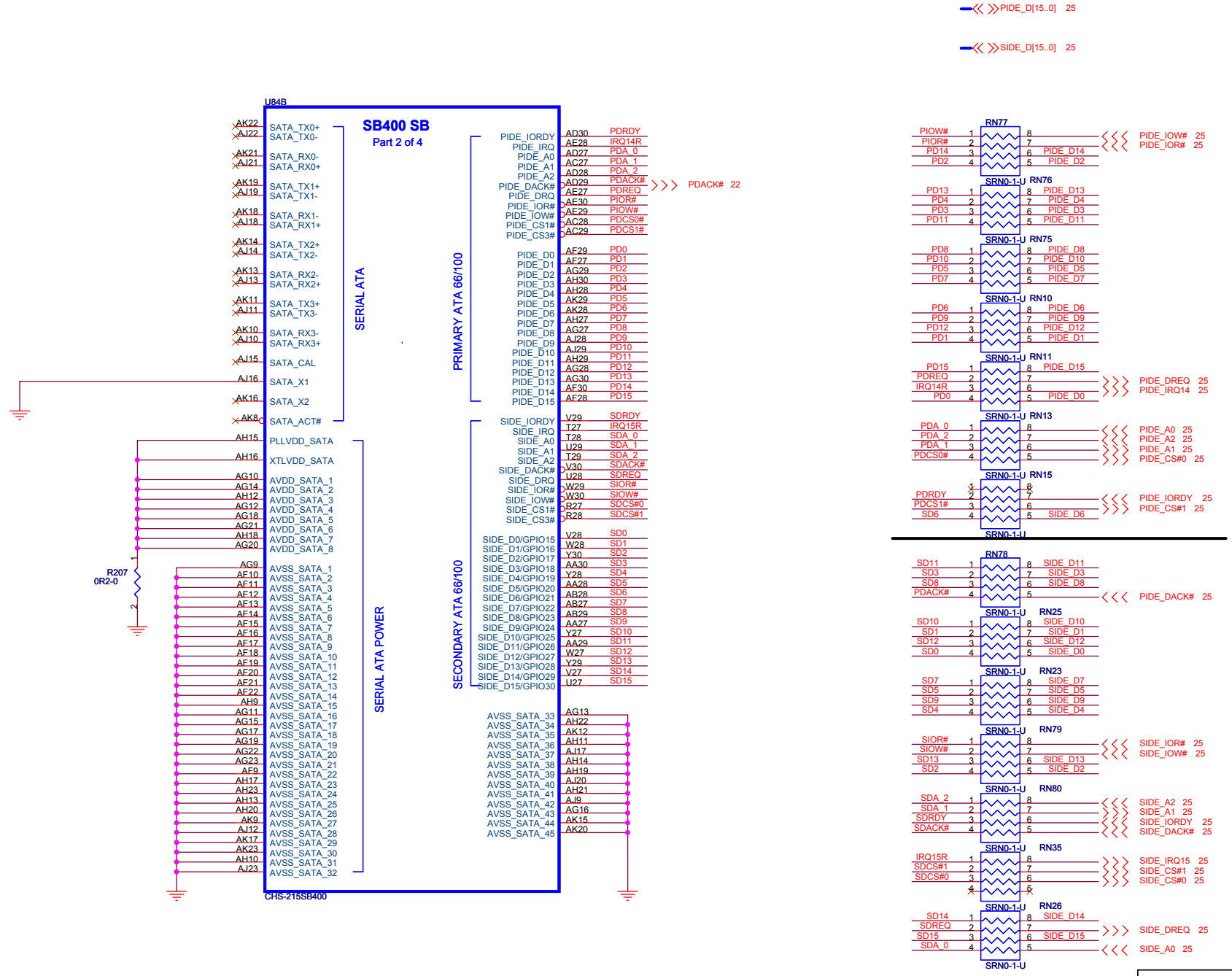
Pull up 100k to 3D3V_S0

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB400 PCI/CPU/LPC/RTC (1 of 5)

Size: A3 | Document Number: SNIPE | Rev: SA

Date: Thursday, November 18, 2004 | Sheet 18 of 56

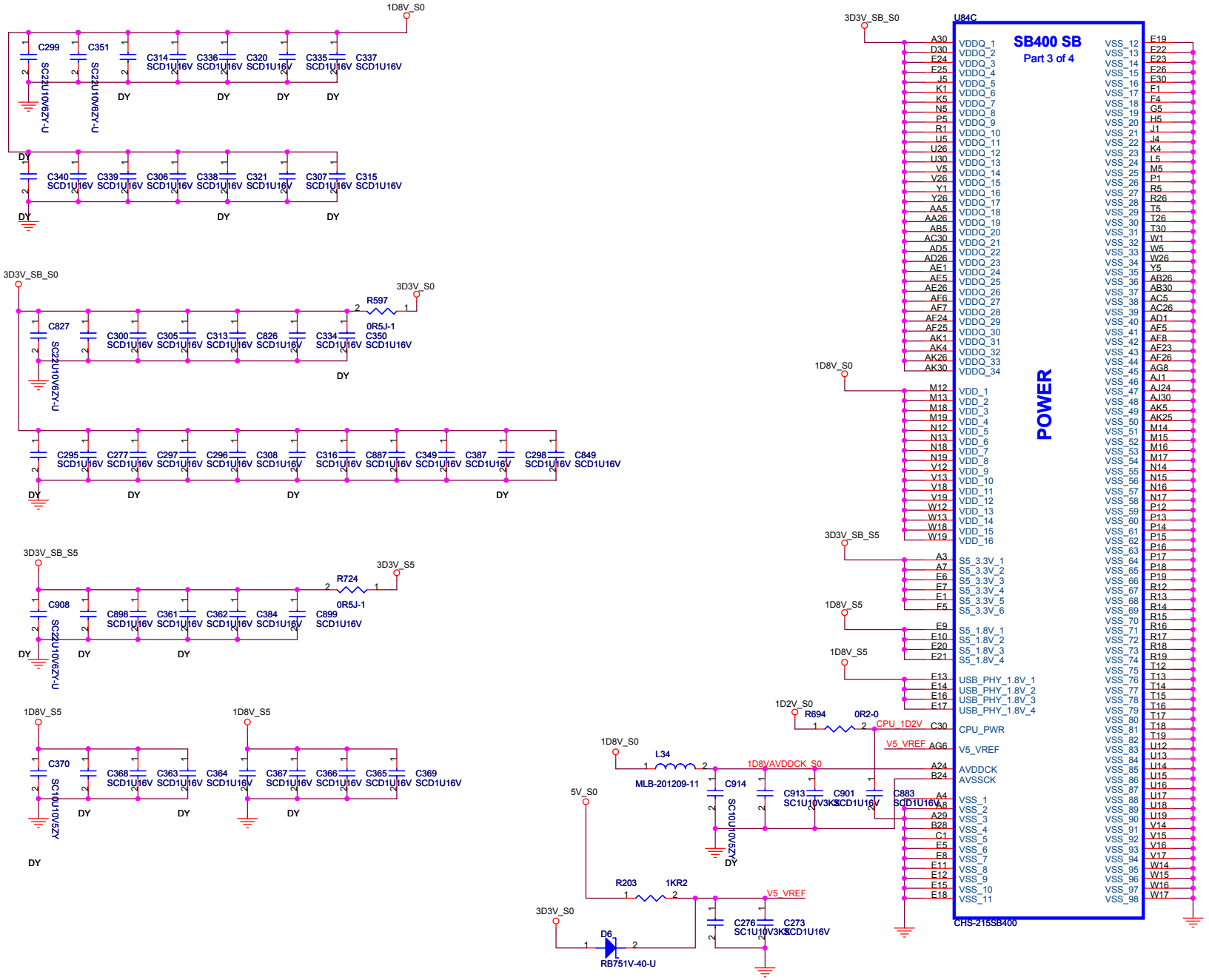


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB400 ACPI/GPIO/SATA/IDE (2 of 5)**

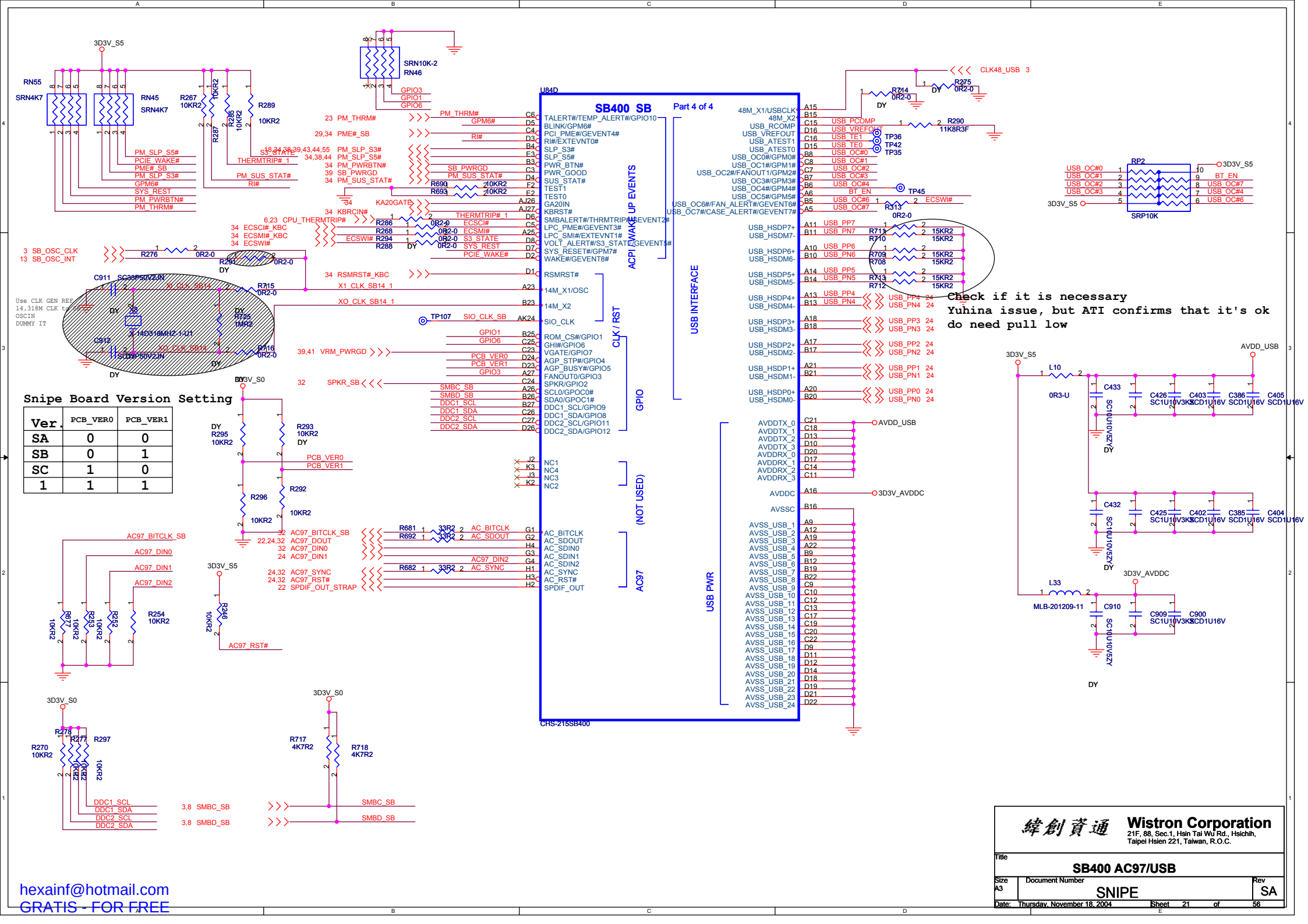
Size	Document Number	Rev
A3	SNIPE	SA

Date: Thursday, November 18, 2004 Sheet 19 of 56



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB400 POWER/DECOUPLING		
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 20 of 56	


SB400 SB
Part 4 of 4
U84D
CHS-215SB400
ACPI / WAKE UP EVENTS
CLK / RST
GPIO
(NOT USED)
AC97
USB INTERFACE
USB PWR
Snipe Board Version Setting
Ver. PCB_VER0 PCB_VER1
SA 0 0
SB 0 1
SC 1 0
1 1 1
Check if it is necessary
Yuhina issue, but ATI confirms that it's ok
do need pull low
Use CLK GEN REF 14.318M CLK to SB OSCIN
DUMMY IT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB400 AC97/USB
Size A3
Document Number SNIPE
Rev SA
Date: Thursday, November 18, 2004
Sheet 21 of 56
hexainf@hotmail.com
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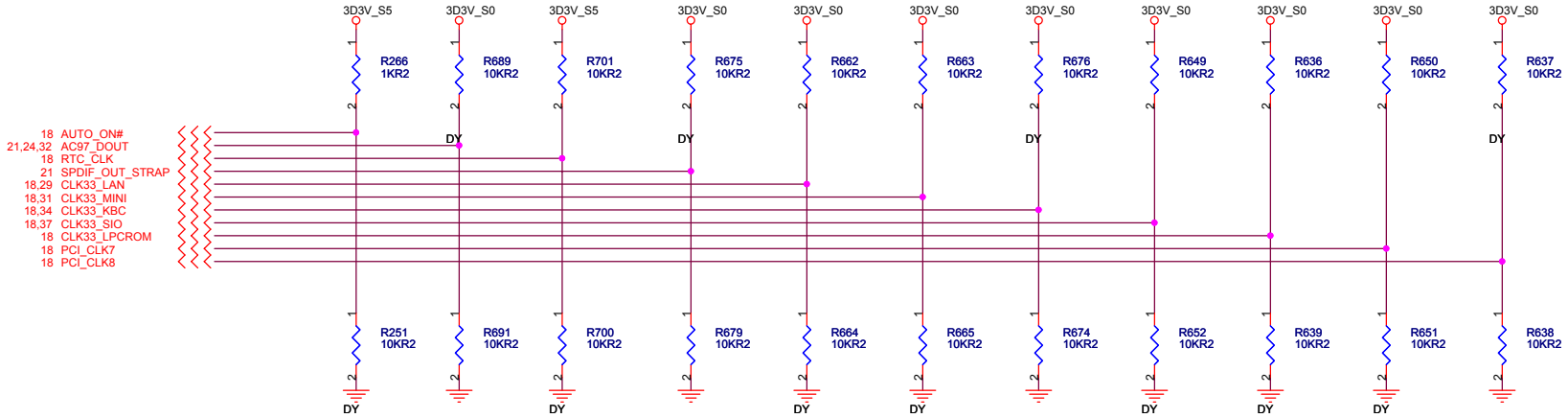
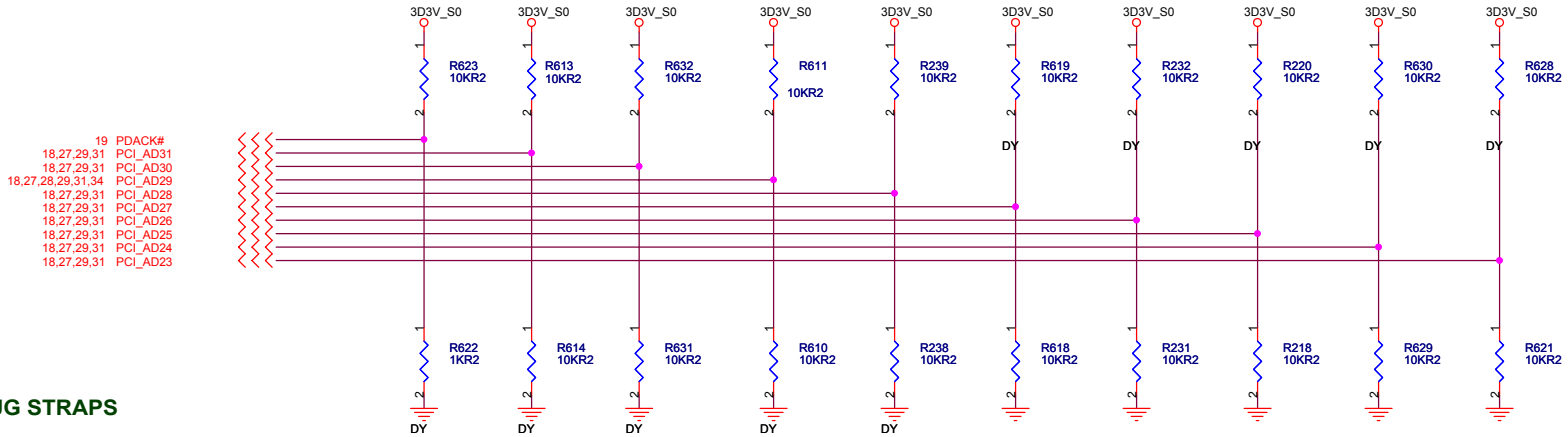


REQUIRED SYSTEM STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7 PCI_CLK8
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHZ-Clock Input Buffer DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	USB INT PLL48 DEFAULT	14MHZ OSC MODE DEFAULT	CPU I/F=K8 DEFAULT	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTENNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz DEFAULT	48MHZ -Crytsal Pad	USB PHY PWRDOWN ENABLE	USB EXT. 48MHZ	14MHZ XTAL MODE	CPU I/F=P4	L,H=LPC ROM II L,L=Firmware Hub ROM



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

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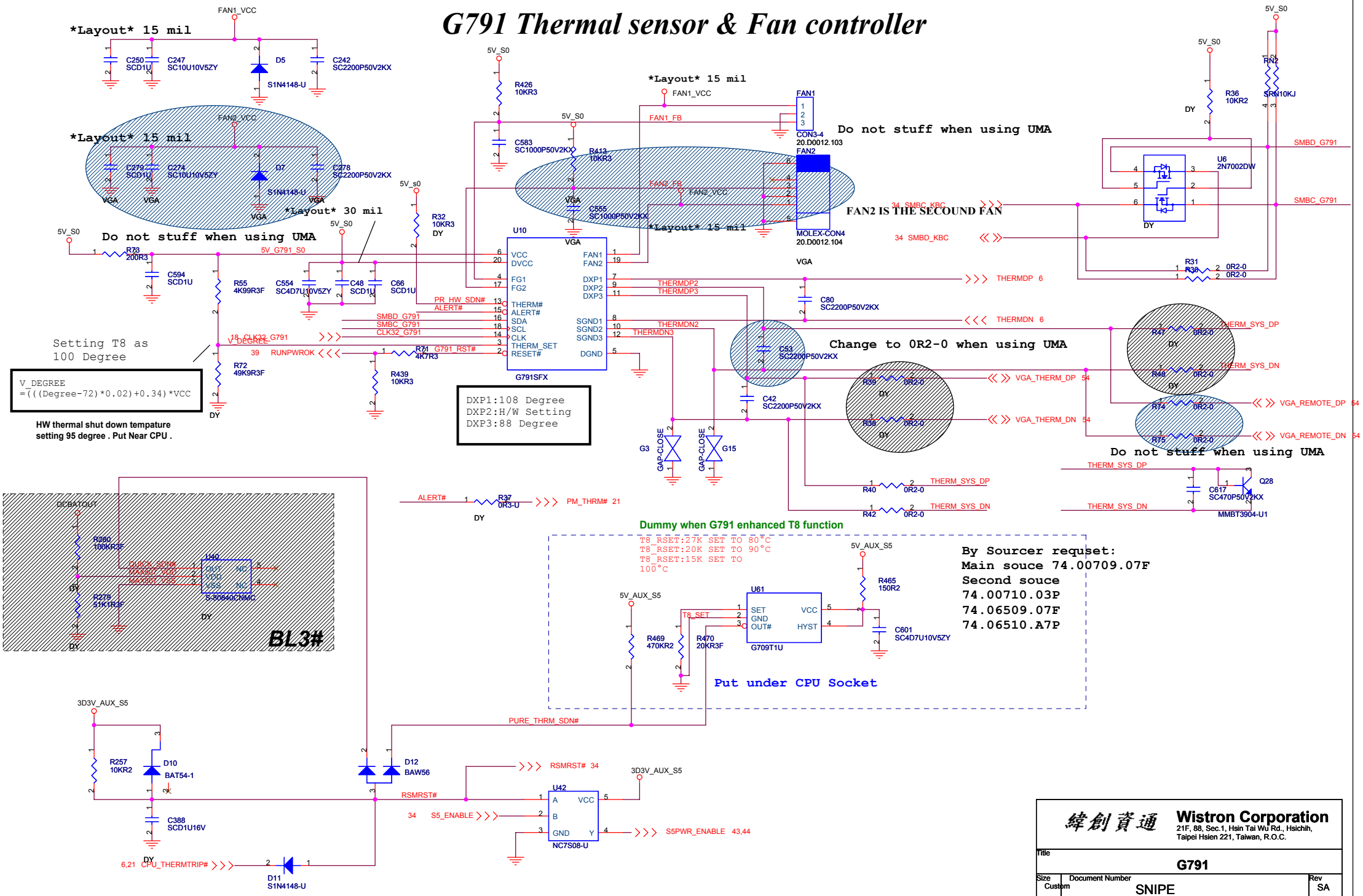
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB400 STRAPPING PIN

Size: A3 | Document Number: SNIPE | Rev: SA

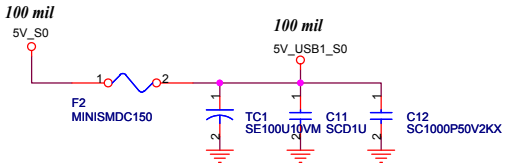
Date: Thursday, November 18, 2004 | Sheet 22 of 56

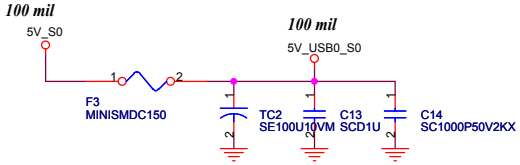
G791 Thermal sensor & Fan controller



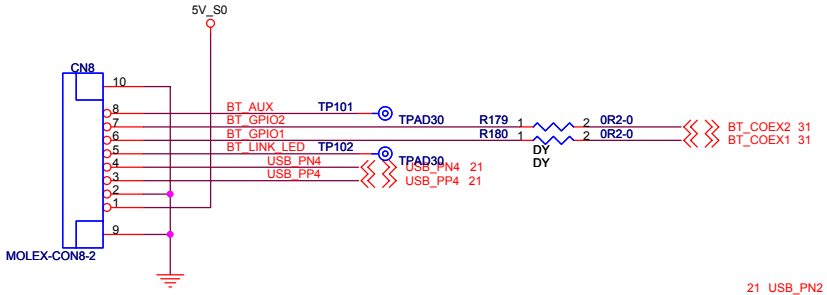
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	G791	
Size: Custom	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 23 of 56	

USB PORT

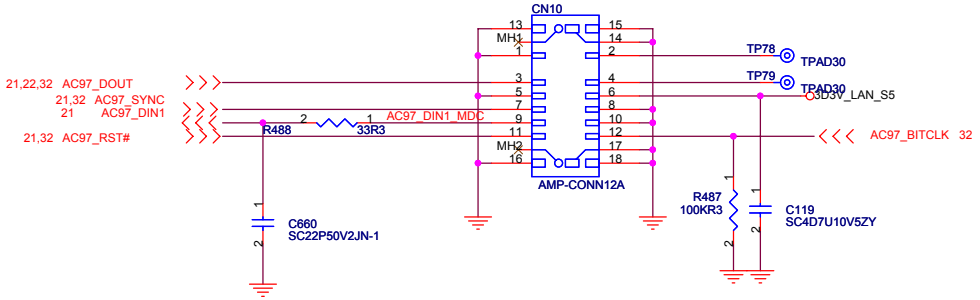


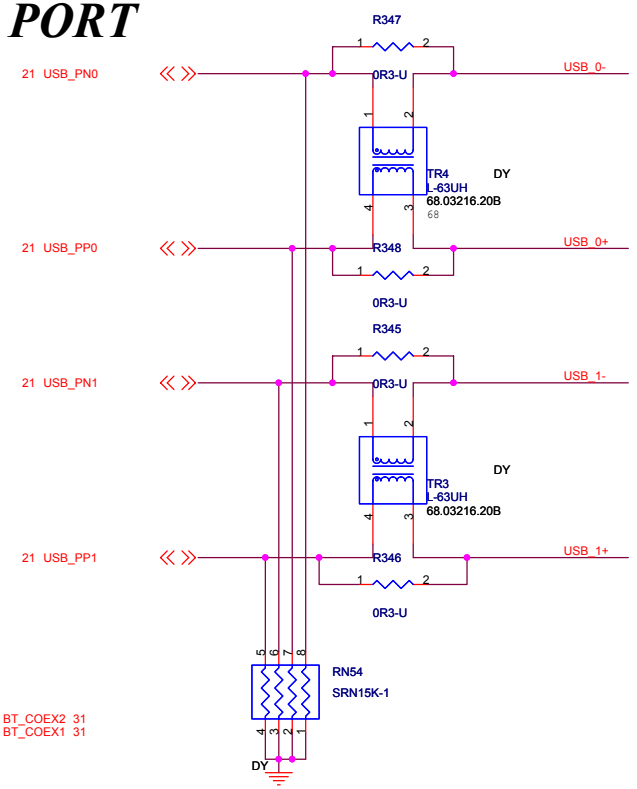


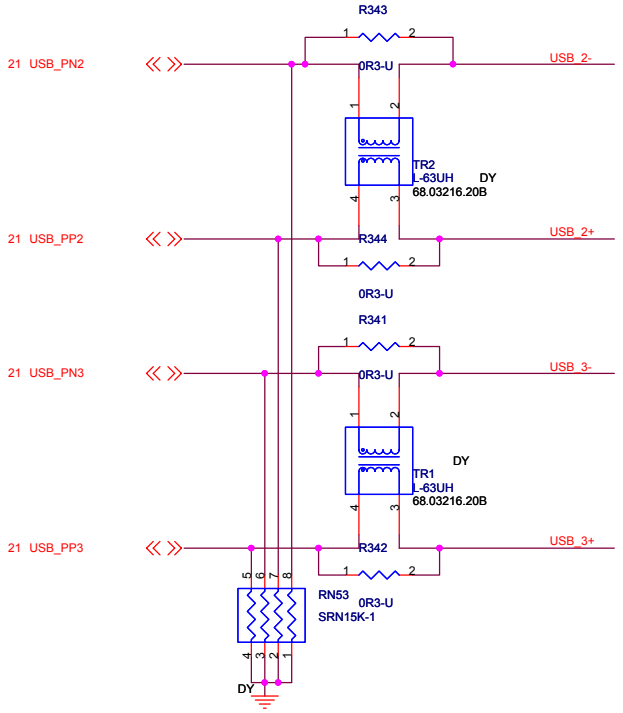
BLUETOOTH MODULE CONNECTOR

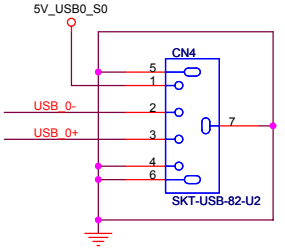


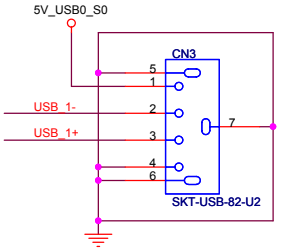
MDC 1.5 CONNECTOR

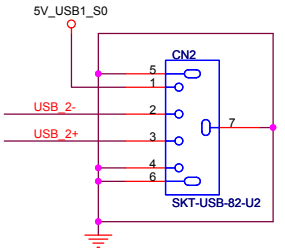


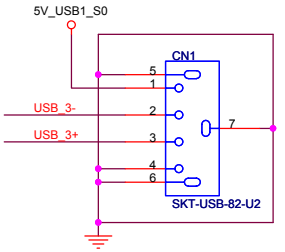












By Sourcer requset change P/N:
From 22.10218.701
To 22.10218.F51

By ME requset P/N:
Main 22.10218.F51
Second 22.10218.F41

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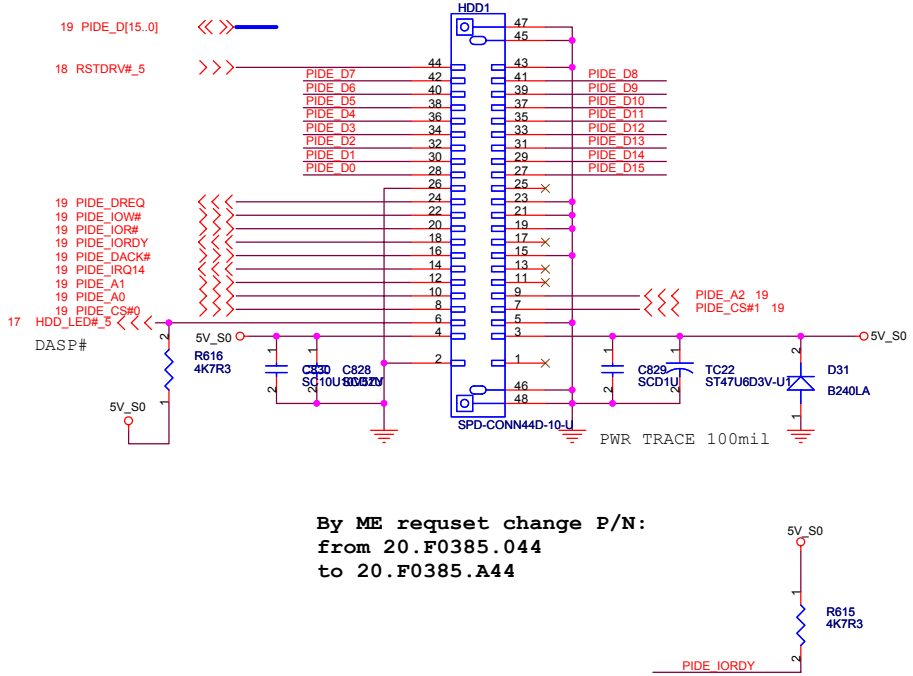
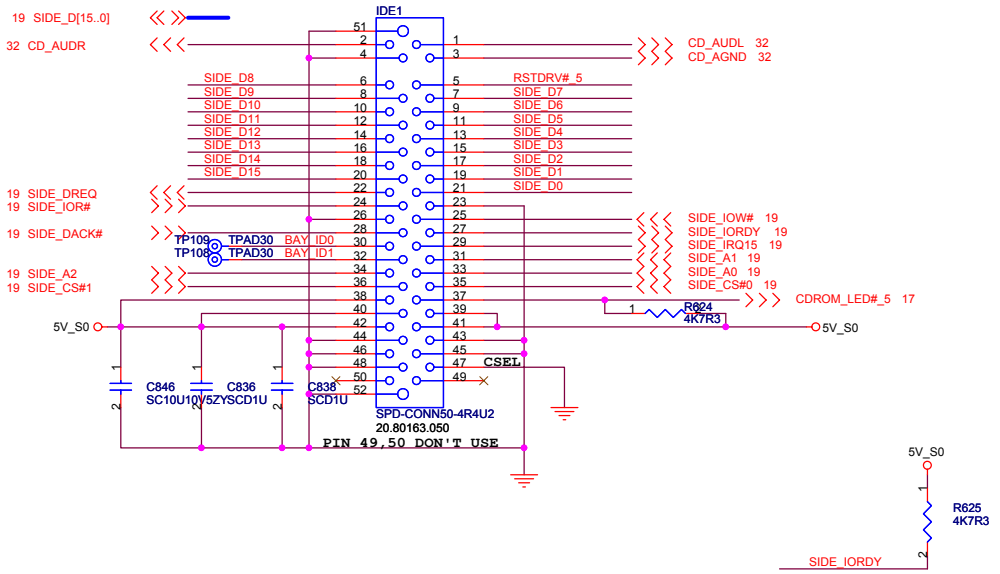
Title: USB and MDC		
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 24 of 56	

HDD



By ME requset change P/N:
from 20.F0385.044
to 20.F0385.A44

CDROM



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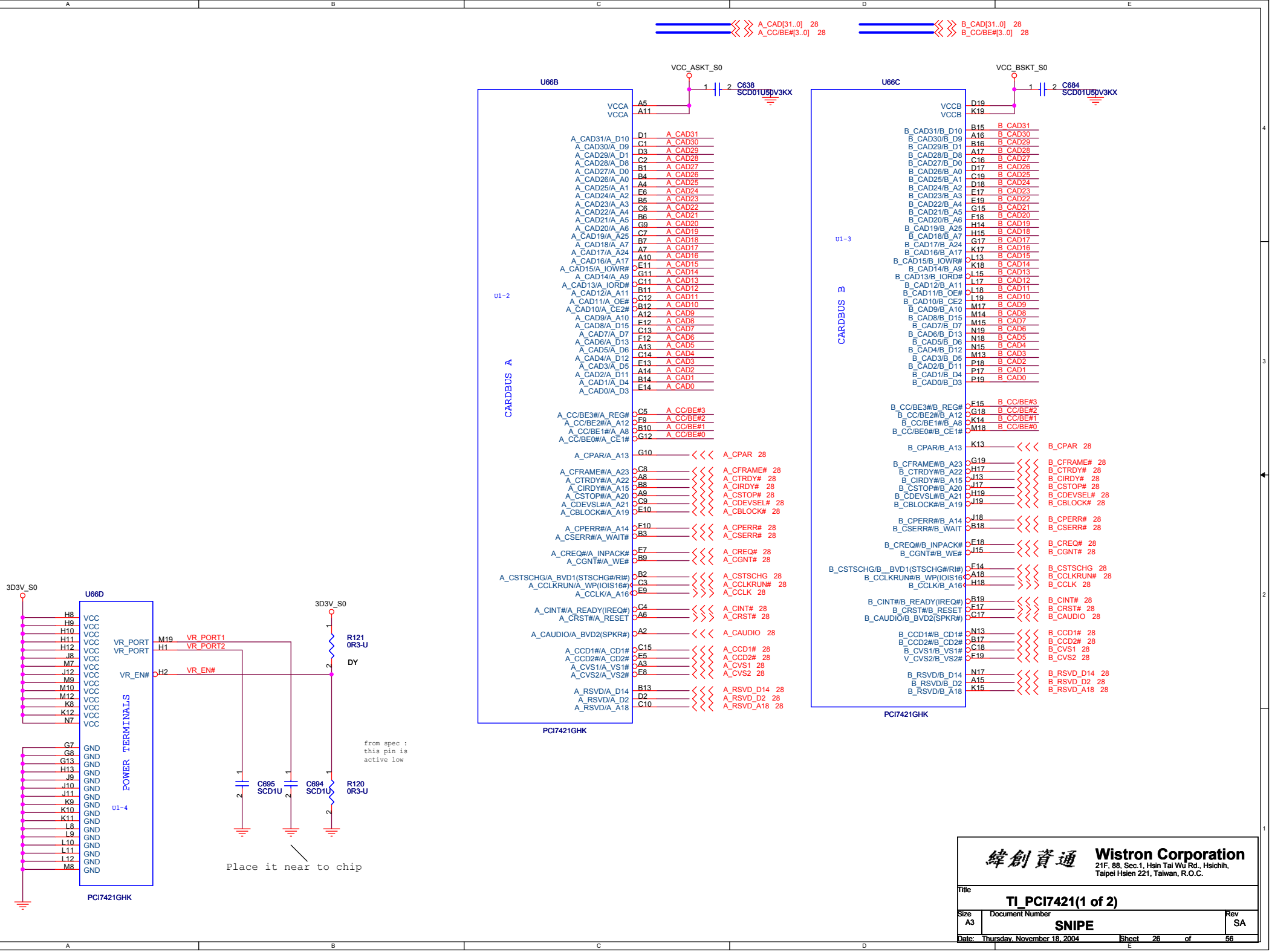
Title	HDD / CDROM	
Size A3	Document Number SNIPE	Rev SA
Date: Thursday, November 18, 2004	Sheet 25 of 56	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A_CC/BE#[3..0] 28
B_CAD[31..0] 28
B_CC/BE#[3..0] 28
VCC_ASKT_S0
U66B
C638
SCD01U50V3KX
VCCA
VCCA
CARDBUS A
U1-2
A_CAD31/A_D10
A_CAD30/A_D9
A_CAD29/A_D1
A_CAD28/A_D8
A_CAD27/A_D0
A_CAD26/A_A0
A_CAD25/A_A1
A_CAD24/A_A2
A_CAD23/A_A3
A_CAD22/A_A4
A_CAD21/A_A5
A_CAD20/A_A6
A_CAD19/A_A25
A_CAD18/A_A7
A_CAD17/A_A24
A_CAD16/A_A17
A_CAD15/A_IOWR#
A_CAD14/A_A9
A_CAD13/A_IORD#
A_CAD12/A_A11
A_CAD11/A_OE#
A_CAD10/A_CE2#
A_CAD9/A_A10
A_CAD8/A_D15
A_CAD7/A_D7
A_CAD6/A_D13
A_CAD5/A_D6
A_CAD4/A_D12
A_CAD3/A_D5
A_CAD2/A_D11
A_CAD1/A_D4
A_CAD0/A_D3
A_CC/BE3#/A_REG#
A_CC/BE2#/A_A12
A_CC/BE1#/A_A8
A_CC/BE0#/A_CE1#
A_CPAR/A_A13
A_CFRAME#/A_A23
A_CTRDY#/A_A22
A_CIRDY#/A_A15
A_CSTOP#/A_A20
A_CDEVSL#/A_A21
A_CBLOCK#/A_A19
A_CPERR#/A_A14
A_CSERR#/A_WAIT#
A_CREQ#/A_INPACK#
A_CGNT#/A_WE#
A_CSTSCHG/A_BVD1(STSCHG#/RI#)
A_CCLKRUN/A_WP(IOIS16#)
A_CCLK/A_A16
A_CINT#/A_READY(IREQ#)
A_CRST#/A_RESET
A_CAUDIO/A_BVD2(SPKR#)
A_CCD1#/A_CD1#
A_CCD2#/A_CD2#
A_CVS1/A_VS1#
A_CVS2/A_VS2#
A_RSVD/A_D14
A_RSVD/A_D2
A_RSVD/A_A18
PCI7421GHK
VCC_BSKT_S0
U66C
C684
SCD01U50V3KX
VCCB
VCCB
U1-3
CARDBUS B
B_CAD31/B_D10
B_CAD30/B_D9
B_CAD29/B_D1
B_CAD28/B_D8
B_CAD27/B_D0
B_CAD26/B_A0
B_CAD25/B_A1
B_CAD24/B_A2
B_CAD23/B_A3
B_CAD22/B_A4
B_CAD21/B_A5
B_CAD20/B_A6
B_CAD19/B_A25
B_CAD18/B_A7
B_CAD17/B_A24
B_CAD16/B_A17
B_CAD15/B_IOWR#
B_CAD14/B_A9
B_CAD13/B_IORD#
B_CAD12/B_A11
B_CAD11/B_OE#
B_CAD10/B_CE2
B_CAD9/B_A10
B_CAD8/B_D15
B_CAD7/B_D7
B_CAD6/B_D13
B_CAD5/B_D6
B_CAD4/B_D12
B_CAD3/B_D5
B_CAD2/B_D11
B_CAD1/B_D4
B_CAD0/B_D3
B_CC/BE3#/B_REG#
B_CC/BE2#/B_A12
B_CC/BE1#/B_A8
B_CC/BE0#/B_CE1#
B_CPAR/B_A13
B_CFRAME#/B_A23
B_CTRDY#/B_A22
B_CIRDY#/B_A15
B_CSTOP#/B_A20
B_CDEVSL#/B_A21
B_CBLOCK#/B_A19
B_CPERR#/B_A14
B_CSERR#/B_WAIT
B_CREQ#/B_INPACK#
B_CGNT#/B_WE#
B_CSTSCHG/B_BVD1(STSCHG#/RI#)
B_CCLKRUN#/B_WP(IOIS16)
B_CCLK/B_A16
B_CINT#/B_READY(IREQ#)
B_CRST#/B_RESET
B_CAUDIO/B_BVD2(SPKR#)
B_CCD1#/B_CD1#
B_CCD2#/B_CD2#
B_CVS1/B_VS1#
V_CVS2/B_VS2#
B_RSVD/B_D14
B_RSVD/B_D2
B_RSVD/B_A18
PCI7421GHK
3D3V_S0
U66D
POWER TERMINALS
U1-4
VR_PORT
VR_PORT
VR_EN#
M19 VR_PORT1
H1 VR_PORT2
H2 VR_EN#
R121
0R3-U
DY
C695
SCD1U
C694
SCD1U
R120
0R3-U
from spec :
this pin is
active low
Place it near to chip
PCI7421GHK
緯創資通
Wistron Corporation
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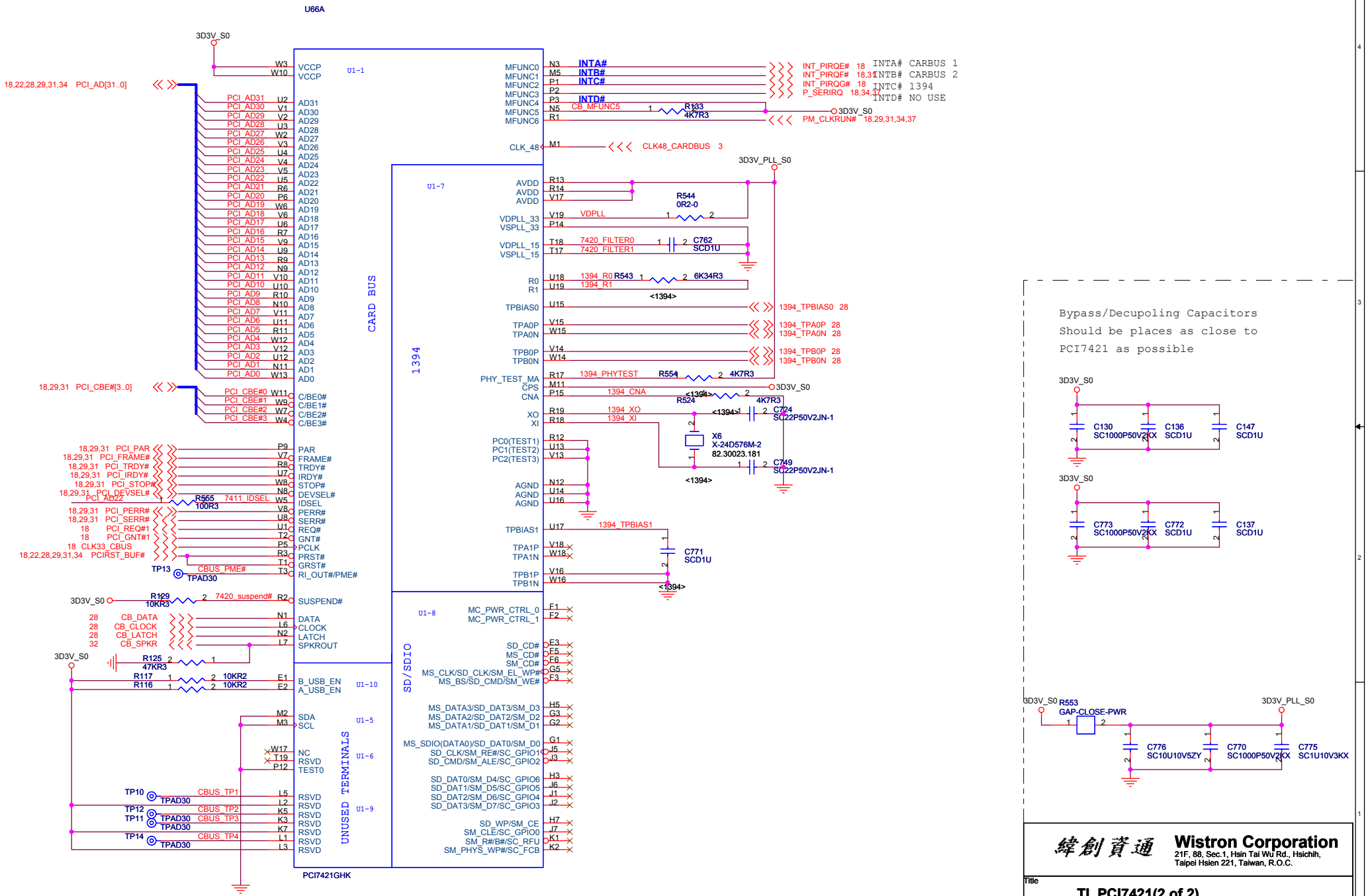
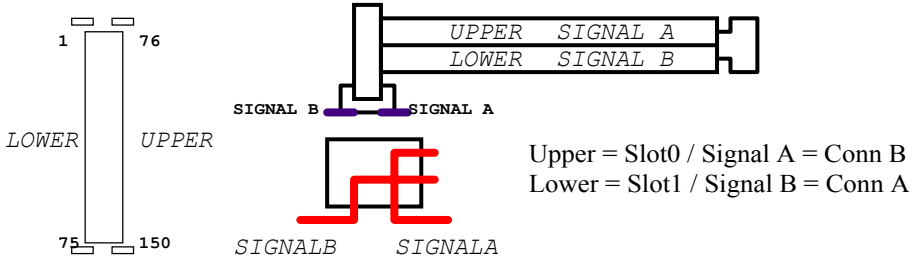
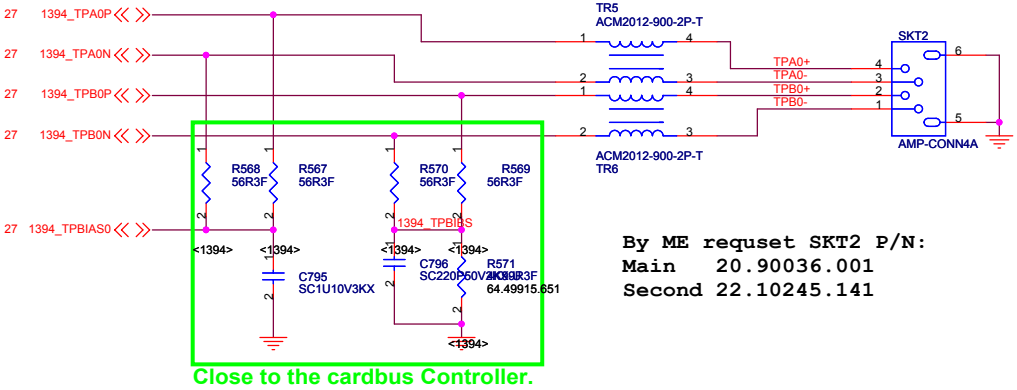
Taipei Hsien 221, Taiwan, R.O.C.
Title
TI_PCI7421(1 of 2)
Size
A3
Document Number
SNIPE
Rev
SA
Date: Thursday, November 18, 2004
Sheet 26 of 56



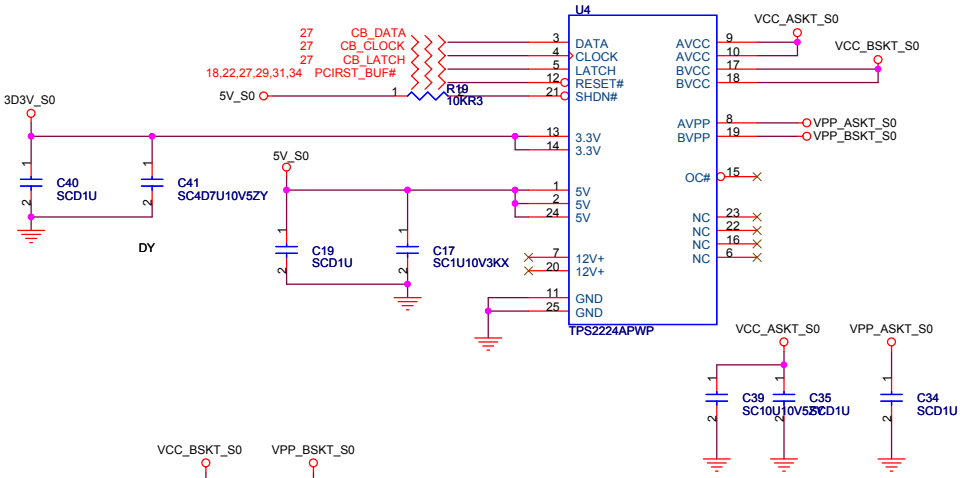


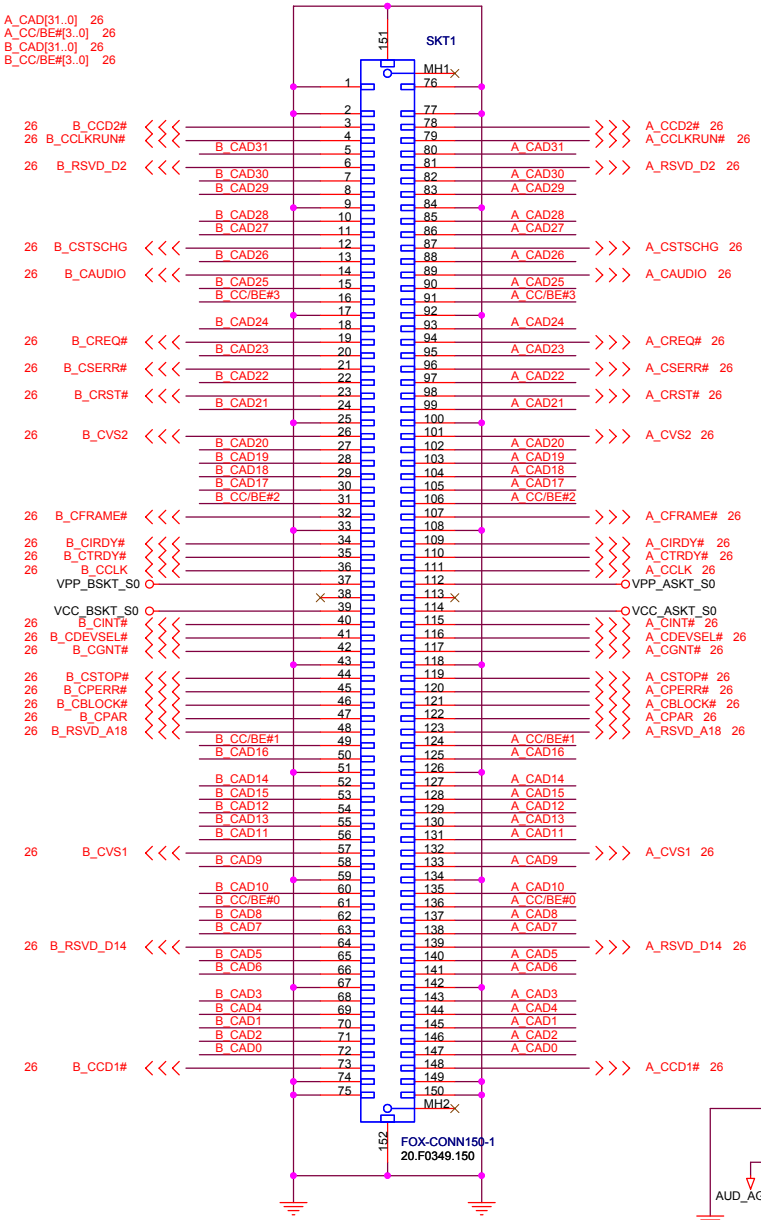
Upper = Slot0 / Signal A = Conn B
Lower = Slot1 / Signal B = Conn A

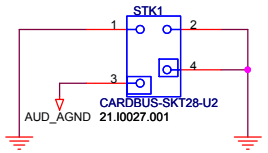
1394 Connector



Power switch







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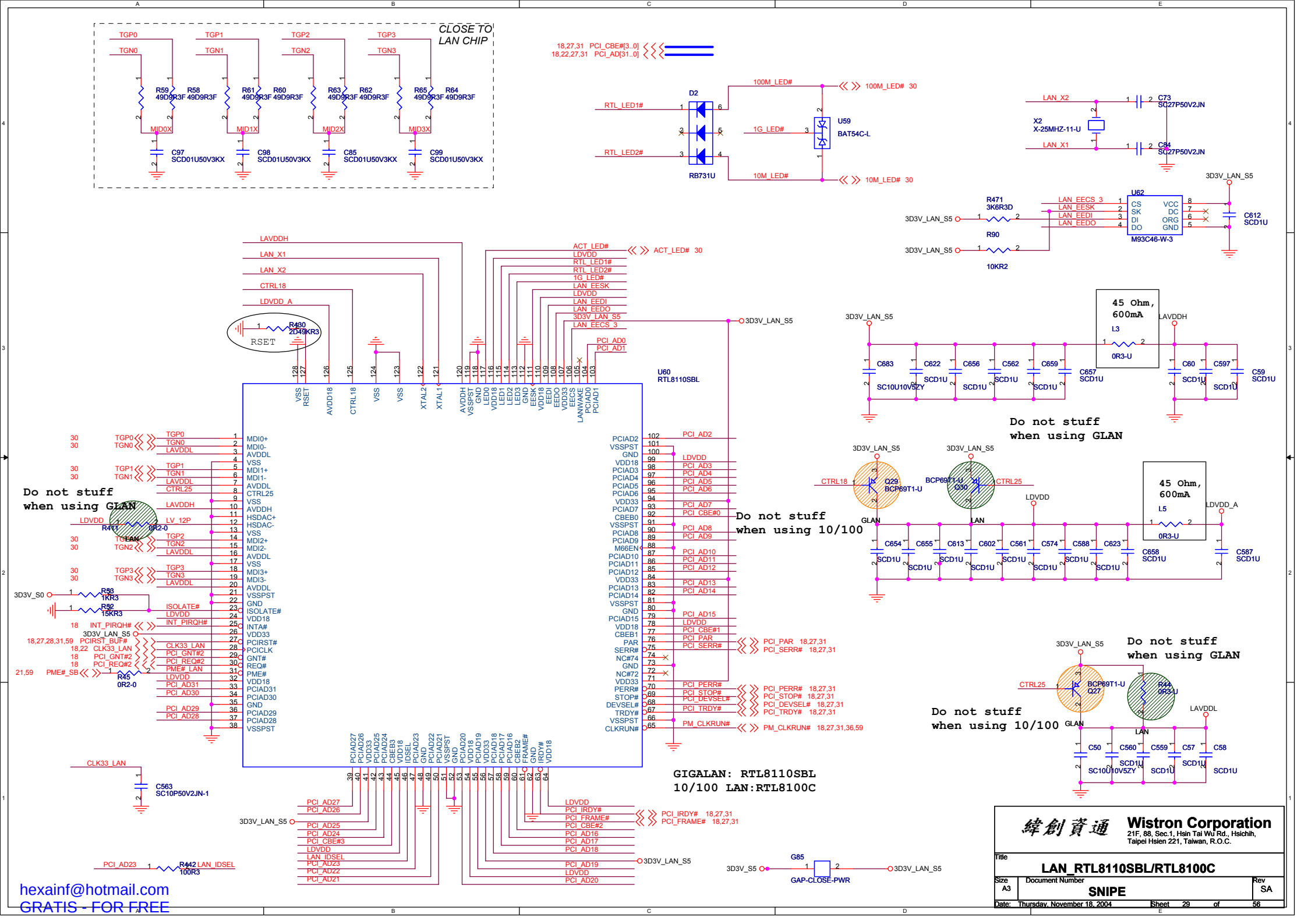
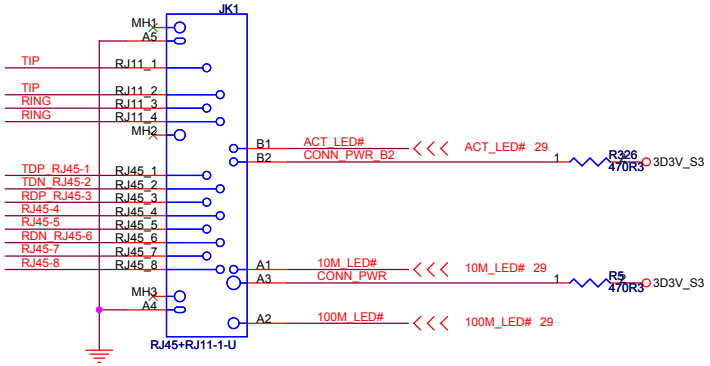
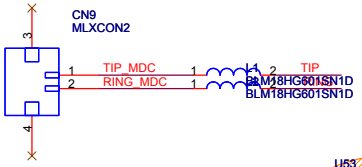
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCMCA SLOT_1394 CONN		
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 28 of 56	


CLOSE TO LAN CHIP
TGP0
TGN0
TGP1
TGN1
TGP2
TGN2
TGP3
TGN3
R59 49D9R3F
R58 49D9R3F
R61 49D9R3F
R60 49D9R3F
R63 49D9R3F
R62 49D9R3F
R65 49D9R3F
R64 49D9R3F
MID0X
MID1X
MID2X
MID3X
C97 SCD01U50V3KX
C98 SCD01U50V3KX
C85 SCD01U50V3KX
C99 SCD01U50V3KX
18,27,31 PCI_CBE#[3..0]
18,22,27,31 PCI_AD[31..0]
D2
RB731U
RTL_LED1#
RTL_LED2#
100M_LED#
1G_LED#
10M_LED#
U59
BAT54C-L
100M_LED# 30
10M_LED# 30
LAN_X2
LAN_X1
X2
X-25MHZ-11-U
C73 SC27P50V2JN
C84 SC27P50V2JN
3D3V_LAN_S5
R471 3K6R3D
R90
10KR2
LAN_EECS_3
LAN_EESK
LAN_EEDI
LAN_EEDO
U62
M93C46-W-3
C612 SCD1U
LAVDDH
LAN_X1
LAN_X2
CTRL18
LDVDD_A
R430 2D49KR3
RSET
ACT_LED#
LDVDD
RTL_LED1#
RTL_LED2#
1G_LED#
LAN_EESK
LAN_EEDI
LAN_EEDO
3D3V_LAN_S5
LAN_EECS_3
PCI_AD0
PCI_AD1
ACT_LED# 30
U60
RTL8110SBL
VSS
RSET
AVDD18
CTRL18
XTAL2
XTAL1
AVDDH
VSSPST
LED0
VDD18
LED1
LED2
LED3
EESK
EEDI
EEDO
VDD33
EECS
LANWAKE
PCIAD0
PCIAD1
MDI0+
MDI0-
MDI1+
MDI1-
CTRL25
HSDAC+
HSDAC-
MDI2+
MDI2-
MDI3+
MDI3-
VDD33
ISOLATE#
INTA#
PCIRST#
PCICLK
GNT#
REQ#
PME#
PCIAD31
PCIAD30
PCIAD29
PCIAD28
PCIAD2
PCIAD3
PCIAD4
PCIAD5
PCIAD6
PCIAD7
CBEB0
M66EN
PCIAD10
PCIAD11
PCIAD12
PCIAD13
PCIAD14
PCIAD15
CBEB1
PAR
SERR#
NC#74
NC#72
PERR#
STOP#
DEVSEL#
TRDY#
CLKRUN#
PCI_AD2
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_CBE#0
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
PCI_CBE#1
PCI_PAR
PCI_SERR#
PCI_PERR#
PCI_STOP#
PCI_DEVSEL#
PCI_TRDY#
PM_CLKRUN#
PCI_PAR 18,27,31
PCI_SERR# 18,27,31
PCI_PERR# 18,27,31
PCI_STOP# 18,27,31
PCI_DEVSEL# 18,27,31
PCI_TRDY# 18,27,31
PM_CLKRUN# 18,27,31,36,59
Do not stuff when using 10/100
Do not stuff when using GLAN
LV_12P
R411 0R2-0
LAN
TGP0
TGN0
TGP1
TGN1
TGP2
TGN2
TGP3
TGN3
LAVDDL
CTRL25
LAVDDH
3D3V_S0
R53 1KR3
R52 15KR3
ISOLATE#
LDVDD
INT_PIRQH#
18,27,28,31,59 PCIRST_BUF#
18,22 CLK33_LAN
18 PCI_GNT#2
18 PCI_REQ#2
21,59 PME#_SB
R45 0R2-0
PME#_LAN
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
CLK33_LAN
C563 SC10P50V2JN-1
PCI_AD23
R442 100R3
LAN_IDSEL
PCIAD27
PCIAD26
PCIAD25
PCIAD24
CBEB3
IDSEL
PCIAD23
PCIAD22
PCIAD21
PCIAD20
PCIAD19
PCIAD18
PCIAD17
PCIAD16
CBEB2
FRAME#
IRDY#
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_CBE#3
PCI_AD23
PCI_AD22
PCI_AD21
PCI_IRDY#
PCI_FRAME#
PCI_CBE#2
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_IRDY# 18,27,31
PCI_FRAME# 18,27,31
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
G85
GAP-CLOSE-PWR
3D3V_S5
45 Ohm, 600mA
L3
0R3-U
C683 SC10U10V5ZY
C622 SCD1U
C656 SCD1U
C562 SCD1U
C659 SCD1U
C657 SCD1U
C60 SCD1U
C597 SCD1U
C59 SCD1U
Do not stuff when using GLAN
CTRL18
CTRL25
Q29 BCP69T1-U
Q30 BCP69T1-U
GLAN
LAN
LDVDD
LDVDD_A
45 Ohm, 600mA
L5
0R3-U
C654 SCD1U
C655 SCD1U
C613 SCD1U
C602 SCD1U
C561 SCD1U
C574 SCD1U
C588 SCD1U
C623 SCD1U
C658 SCD1U
C587 SCD1U
Do not stuff when using 10/100
Do not stuff when using GLAN
Q27 BCP69T1-U
R44 0R3-U
C50 SC10U10V5ZY
C560 SCD1U
C559 SCD1U
C57 SCD1U
C58 SCD1U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN_RTL8110SBL/RTL8100C
Size A3
Document Number SNIPE
Rev SA
Date: Thursday, November 18, 2004
Sheet 29 of 56
hexainf@hotmail.com
GRATIS - FOR FREE

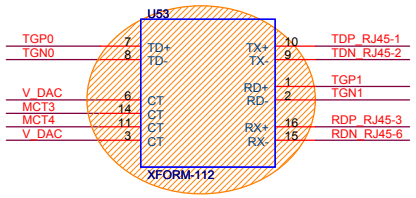
Link: Green - 10Mbps/802.11b Activity: Yellow
Orange - 100Mbps/802.11a
Yellow - 1Gbps



By ME requset for
10/100 LAN change P/N:
From 22.10177.621
To 22.10177.731
By ME requset for
GigaLAN JK1 P/N:
Main 22.10177.601
Second 22.10245.771
By ME requset change P/N:
From 20.D0121.102
To 21.D0010.102



Do not stuff
when using GLAN



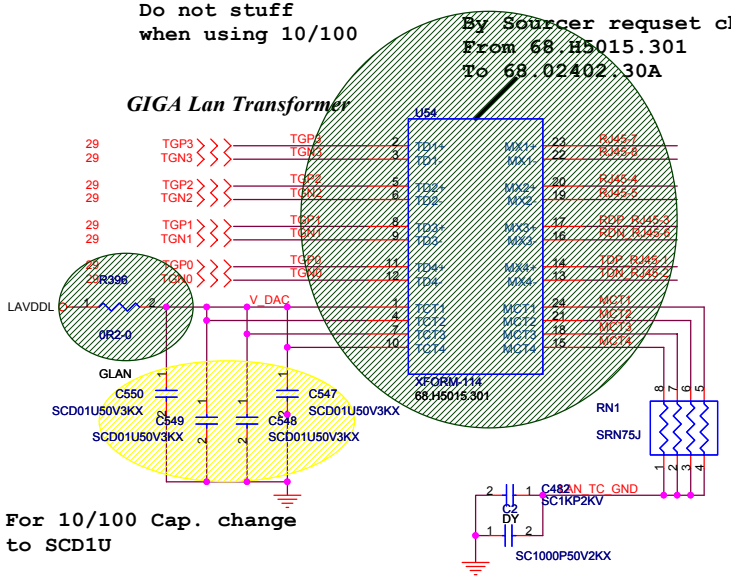
10/100M Lan Transformer

By Sourcer requset change P/N:
From 68.H0013.301
To 68.0H80P.301

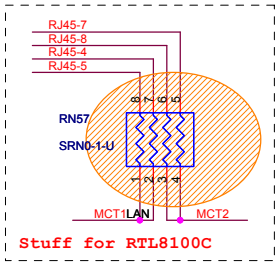
Do not stuff
when using 10/100

By Sourcer requset change P/N:
From 68.H5015.301
To 68.02402.30A

GIGA Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



Do not stuff
when using GLAN

For 10/100 Cap. change
to SCD1U

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Title: LAN_CONN 10/100/1000
Size: A3 | Document Number: SNIPE | Rev: SA
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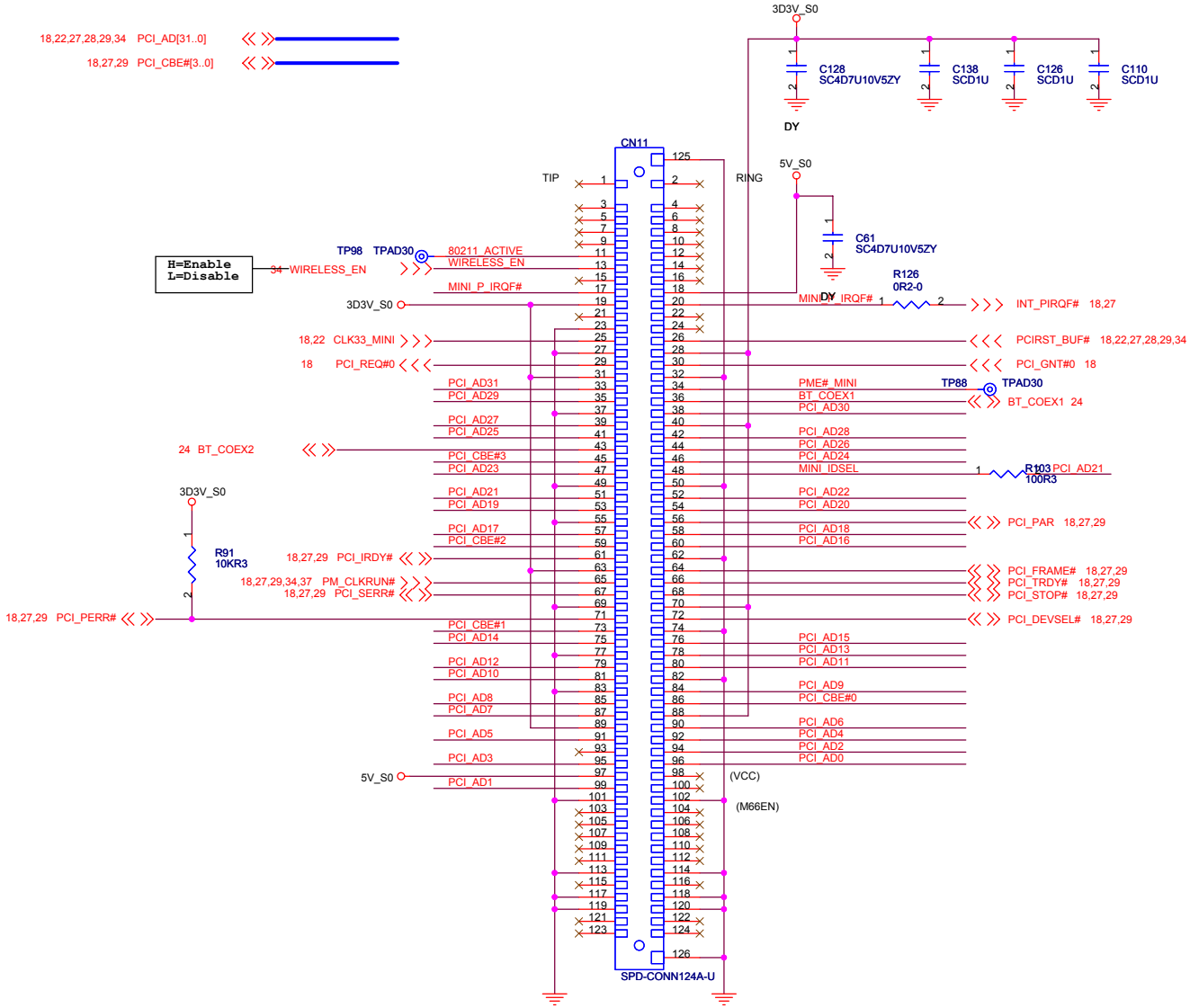
MINI-PCI



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Title	MINI-PCI	
Size A3	Document Number SNIPE	Rev SA
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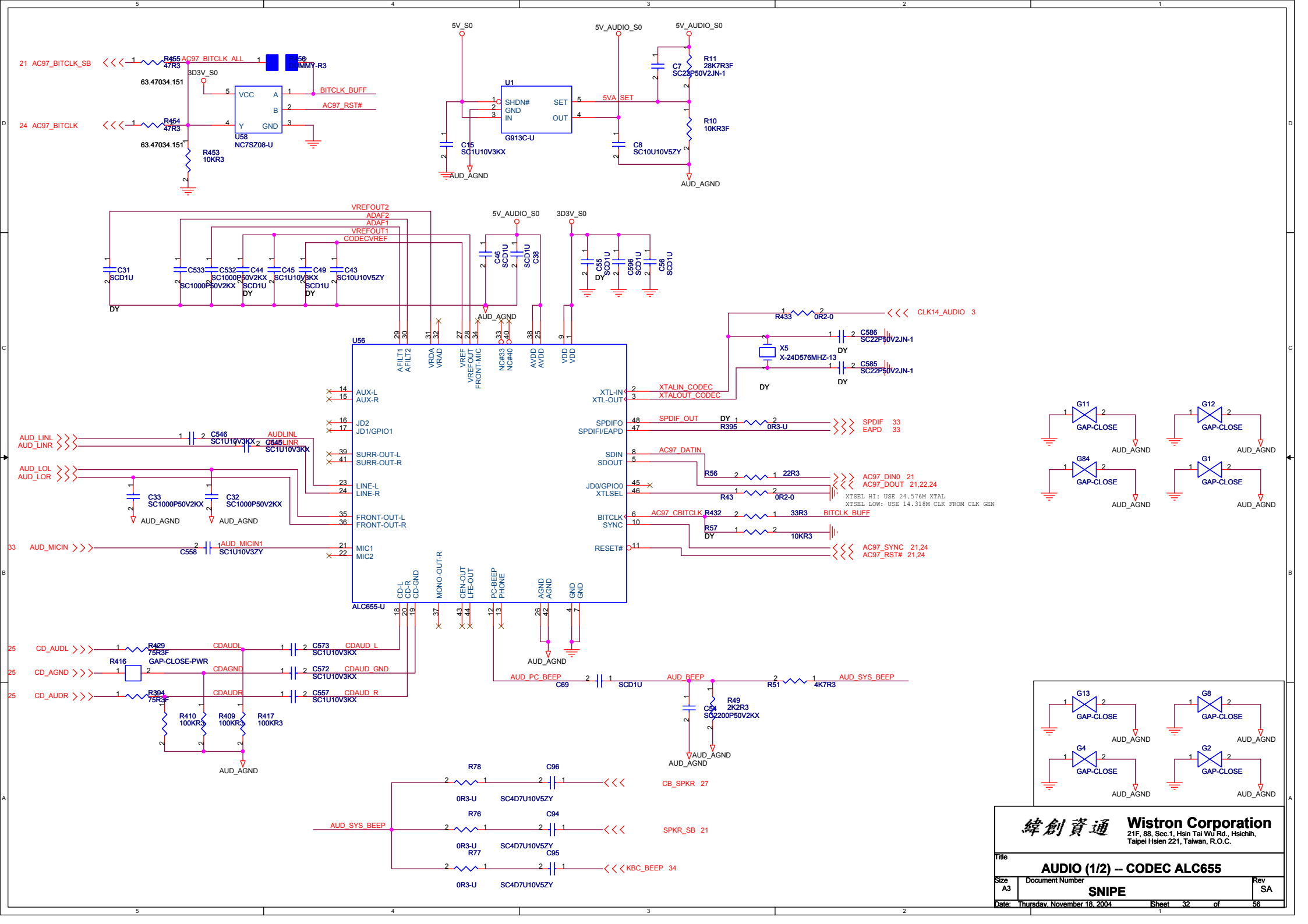

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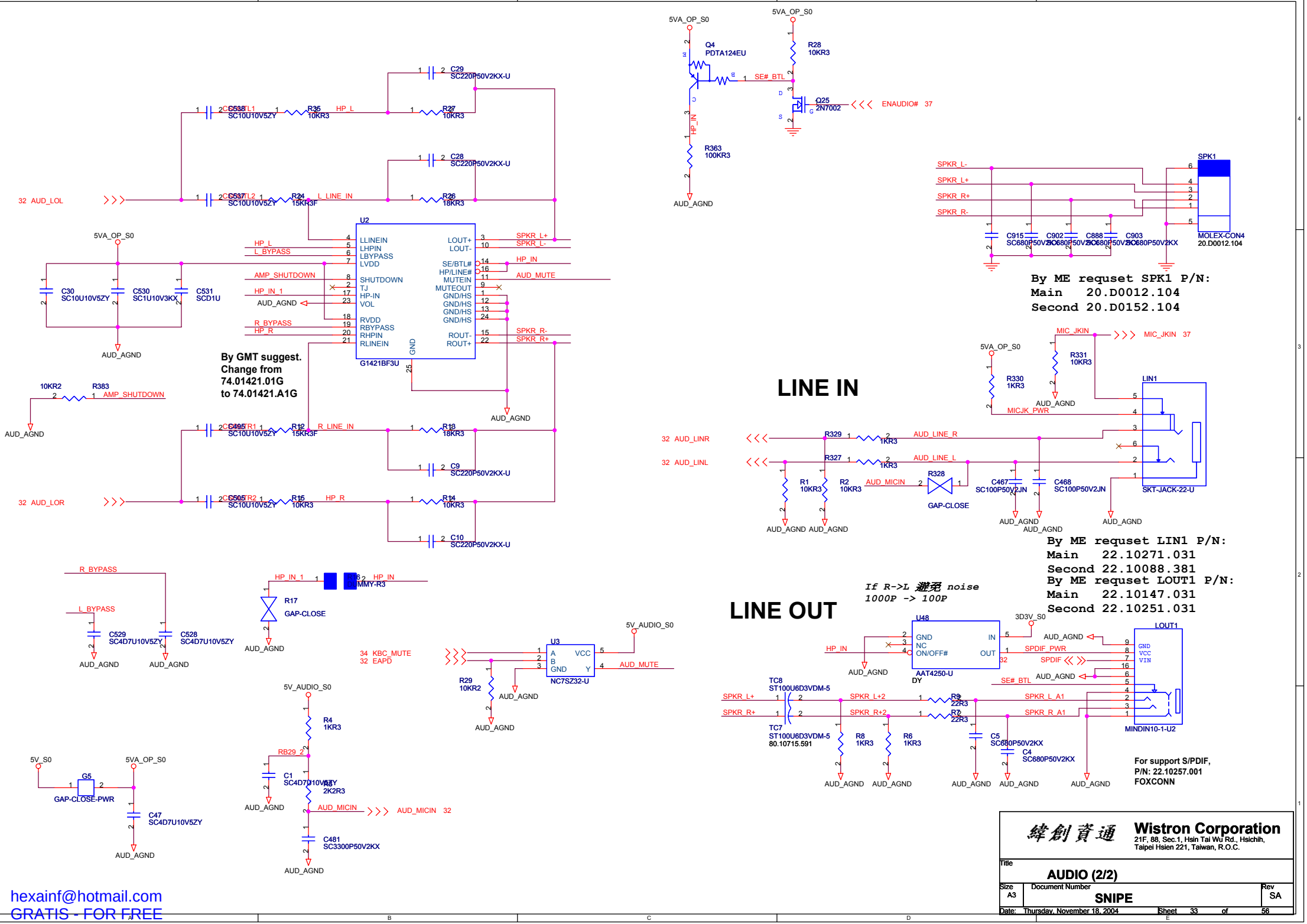
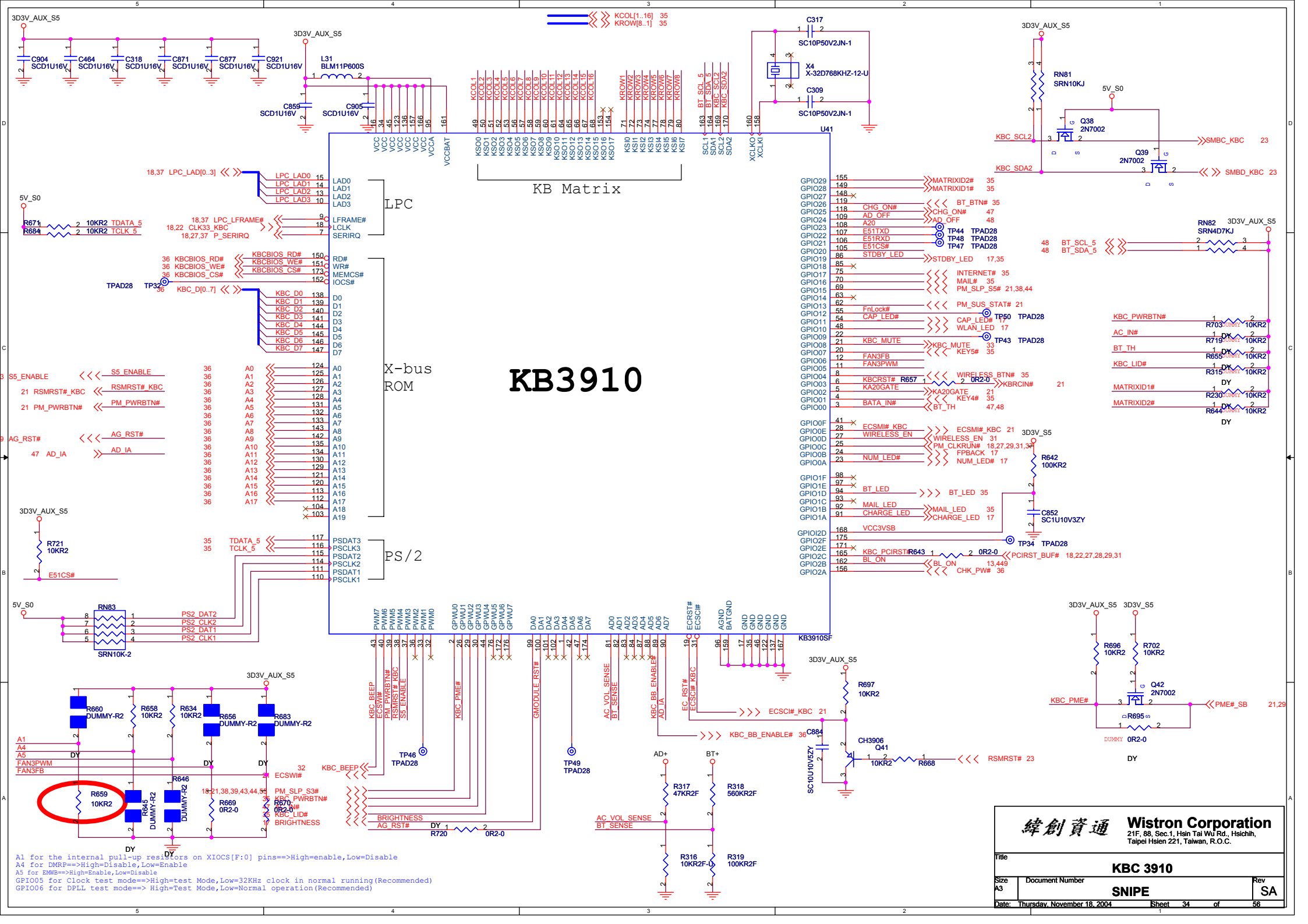
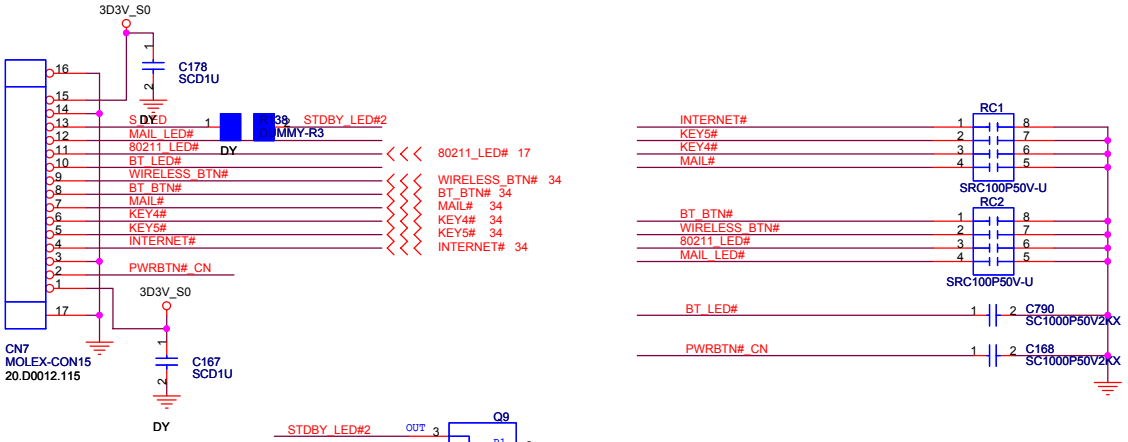
Title: **AUDIO (1/2) -- CODEC ALC655**

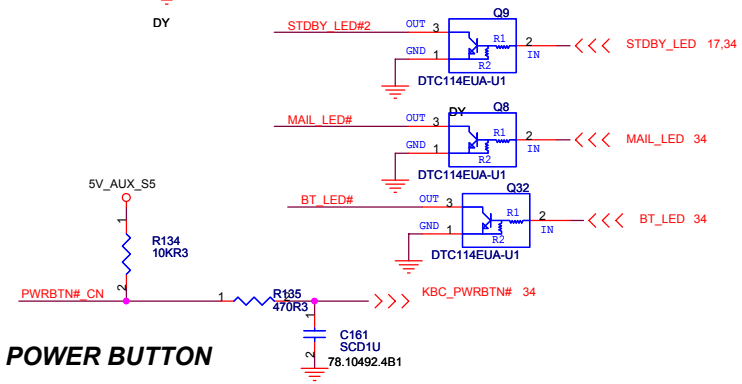
Size	Document Number	Rev
A3	SNIPE	SA

Date: Thursday, November 18, 2004 Sheet 32 of 56

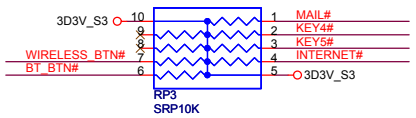



KB3910
KB Matrix
LPC
X-bus ROM
PS/2
KB3910SF
U41
3D3V_AUX_S5
5V_S0
KCOL[1..16] 35
KROW[8..1] 35
C317 SC10P50V2JN-1
X4 X-32D768KHZ-12-U
C309 SC10P50V2JN-1
RN81 SRN10KJ
Q38 2N7002
Q39 2N7002
KBC_SCL2
KBC_SDA2
SMBC_KBC 23
SMBD_KBC 23
RN82 SRN4D7KJ
BT_SCL_5 48
BT_SDA_5 48
KBC_PWRBTN#
AC_IN#
BT_TH
KBC_LID#
MATRIXID1#
MATRIXID2#
R703 10KR2
R719 10KR2
R655 10KR2
R315 10KR2
R230 10KR2
R644 10KR2
LPC_LAD[0..3] 18,37
LPC_LFRAME# 18,37
CLK33_KBC 18,22
P_SERIRQ 18,27,37
KBCBIOS_RD# 36
KBCBIOS_WE# 36
KBCBIOS_CS# 36
KBC_D[0..7] 36
A0 36
A1 36
A2 36
A3 36
A4 36
A5 36
A6 36
A7 36
A8 36
A9 36
A10 36
A11 36
A12 36
A13 36
A14 36
A15 36
A16 36
A17 36
TDATA_5 35
TCLK_5 35
S5_ENABLE
RSMRST#_KBC 21
PM_PWRBTN# 21
AG_RST#
AD_IA 47
E51CS#
R671 10KR2 TDATA_5
R684 10KR2 TCLK_5
R721 10KR2
RN83 SRN10K-2
PS2_DAT2
PS2_CLK2
PS2_DAT1
PS2_CLK1
GPIO29 MATRIXID2# 35
GPIO28 MATRIXID1# 35
GPIO26 BT_BTN# 35
GPIO25 CHG_ON# 47
GPIO24 AD_OFF 48
GPIO23 E51TXD TP44 TPAD28
GPIO22 E51RXD TP48 TPAD28
GPIO21 E51CS# TP47 TPAD28
GPIO20 STDBY_LED 17,35
GPIO17 INTERNET# 35
GPIO16 MAIL# 35
GPIO15 PM_SLP_S5# 21,38,44
GPIO13 PM_SUS_STAT# 21
GPIO12 FnLock# TP50 TPAD28
GPIO11 CAP_LED# 17
GPIO10 WLAN_LED 17
GPIO09 TP43 TPAD28
GPIO08 KBC_MUTE 33
GPIO07 KEY5# 35
GPIO06 FAN3FB
GPIO05 FAN3PWM
GPIO04 WIRELESS_BTN# 35
GPIO03 KBCRST# R657 0R2-0 KBRCIN# 21
GPIO02 KA20GATE 21
GPIO01 KEY4# 35
GPIO00 BATA_IN# BT_TH 47,48
GPIO0F ECSMI# KBC ECSMI#_KBC 21
GPIO0E WIRELESS_EN WIRELESS_EN 31
GPIO0D PM_CLKRUN# 18,27,29,31,34
GPIO0C FPBACK 17
GPIO0B NUM_LED# 17
GPIO0A
GPIO1F
GPIO1E
GPIO1D BT_LED BT_LED 35
GPIO1C
GPIO1B MAIL_LED MAIL_LED 35
GPIO1A CHARGE_LED CHARGE_LED 17
GPIOI2D VCC3VSB
GPIO2F TP34 TPAD28
GPIO2E
GPIO2C KBC_PCIRST# R643 0R2-0 PCIRST_BUF# 18,22,27,28,29,31
GPIO2B BL_ON BL_ON 13,449
GPIO2A CHK_PW# 36
R642 100KR2
C852 SC1U10V3ZY
R660 DUMMY-R2
R658 10KR2
R634 10KR2
R656 DUMMY-R2
R683 DUMMY-R2
R659 10KR2
R645 DUMMY-R2
R646
R669 0R2-0
R670 0R2-0
KBC_BEEP 32
ECSWI# 24
PM_SLP_S3# 18,21,38,39,43,44,55
KBC_PWRBTN# 36
KBC_LID# 36
BRIGHTNESS 37
AG_RST# 9
R720 DY 0R2-0
TP46 TPAD28
TP49 TPAD28
KBC_PME#
GMODULE_RST#
AC_VOL_SENSE
BT_SENSE
KBC_BB_ENABLE# 36
ECSCI#_KBC 21
R697 10KR2
C884
CH3906 Q41
R668 10KR2
RSMRST# 23
R696 10KR2
R702 10KR2
Q42 2N7002
R695 DUMMY 0R2-0
PME#_SB 21,29
R317 47KR2F
R318 560KR2F
R316 10KR2F-L
R319 100KR2F
AD+
BT+
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==> High=Test Mode,Low=Normal operation(Recommended)
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC 3910
Size A3
Document Number
SNIPE
Rev SA
Date: Thursday, November 18, 2004
Sheet 34 of 56

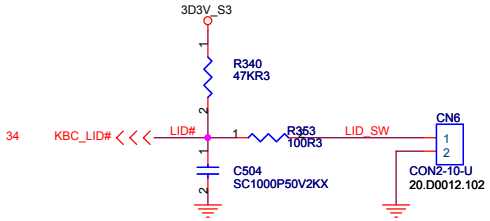




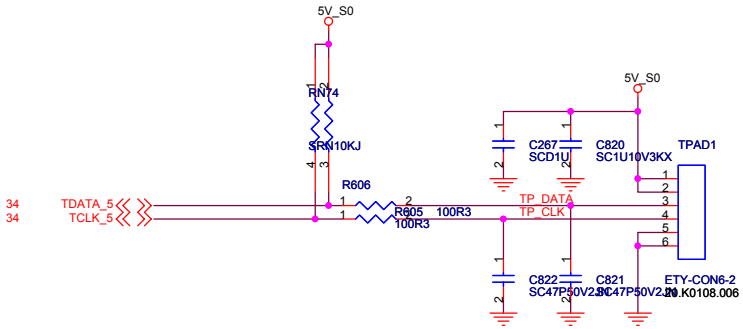
POWER BUTTON



Launch Board CONN

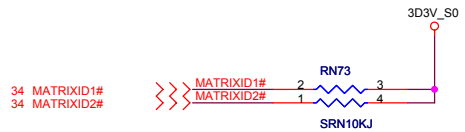


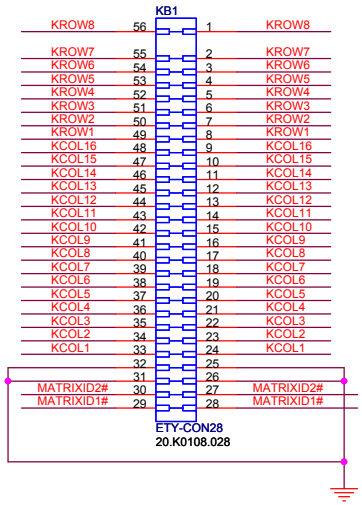
Cover Up Switch



TOUCH PAD

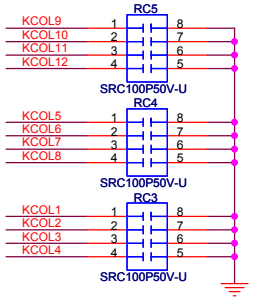
Internal KeyBoard CONN

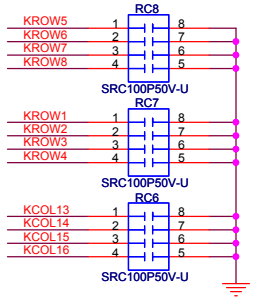




Keyboard matrix	(from vendor)			
	US	Jap	Eur	Other
Low Bit MATRIXID1#	1	1	0	0
High Bit MATRIXID2#	1	0	1	0

EMI Bypass cap.





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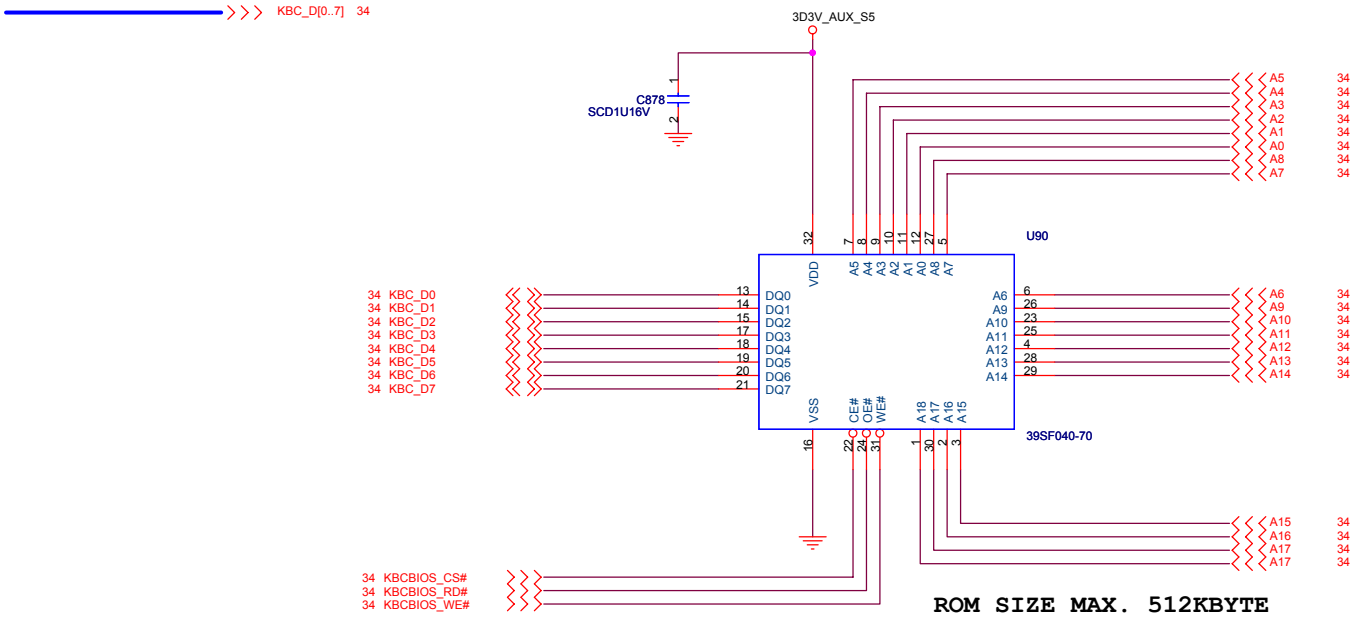
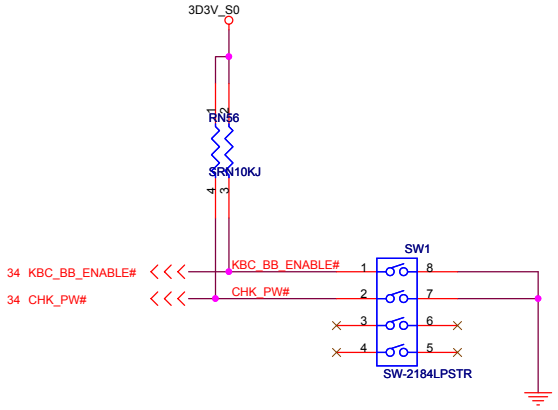
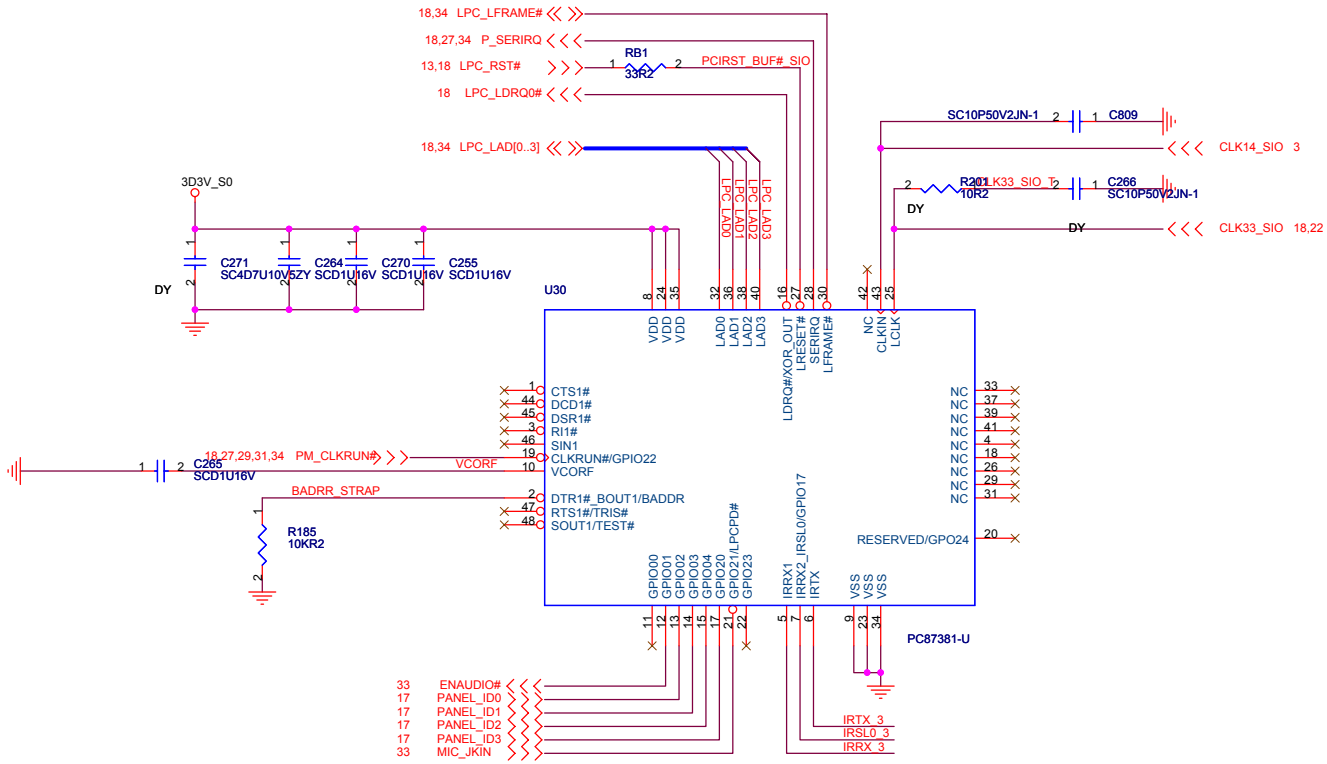
Title	LAUNCH / TOUCHPAD / KB CONN	
Size A3	Document Number SNIPE	Rev SA
Date: Thursday, November 18, 2004	Sheet 35 of 56	



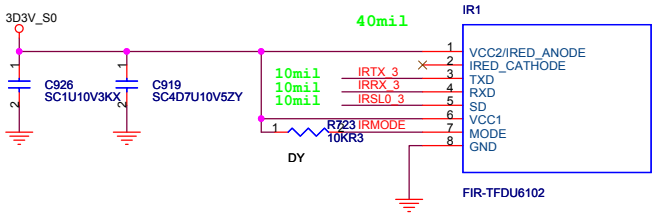
PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **BIOS ROM**		
Size: A3	Document Number: **SNIPE**	Rev: SA
Date: Thursday, November 18, 2004	Sheet 36 of 56	



Infineon FIR Module



PANEL ID DEFINE				
PANEL_ID3	PANEL_ID2	PANEL_ID1	PANEL_ID0	VENDORS
0	0	0	0	15" SXGA+
0	0	0	1	Hydis (14")SPWG
0	0	1	0	15" WIDE
0	0	1	1	Hitachi (15")
0	0	1	1	AU (15")
0	0	1	1	CMO(15")
0	1	0	0	CMO(14")
0	1	0	1	AU (14")
0	1	1	0	AU (14")**
0	1	1	1	No Panel
Note : AU (友達),CMO(奇美),** : With Digitizer				

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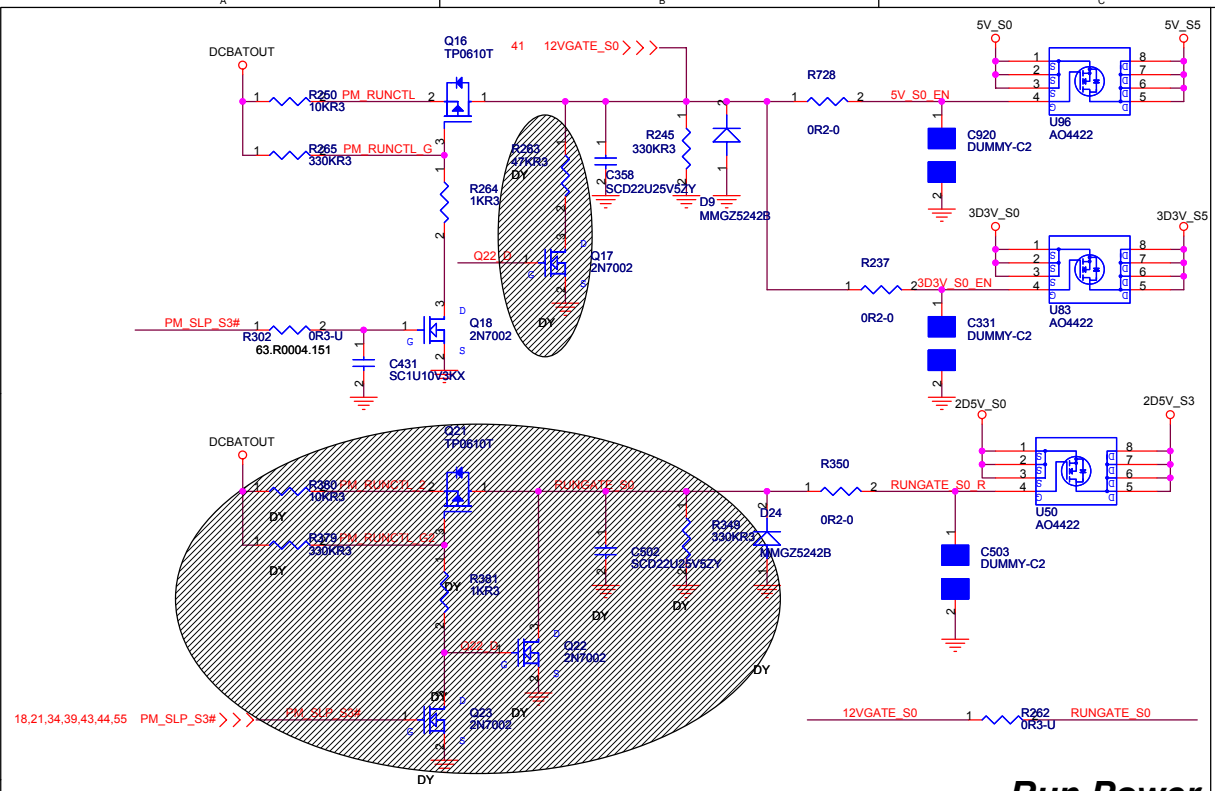
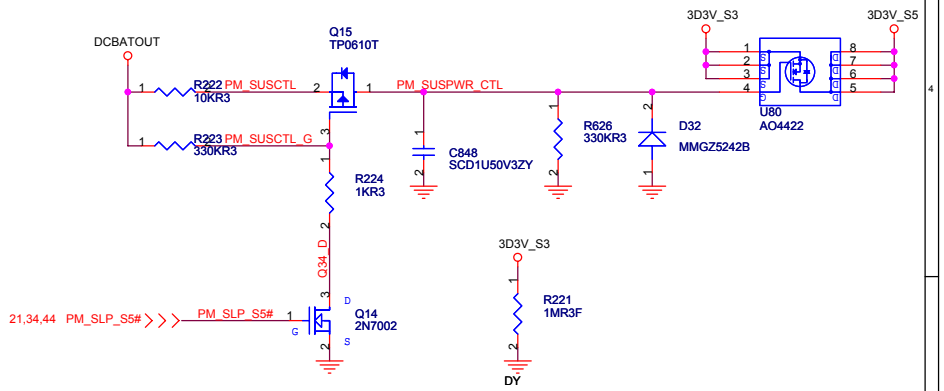
Title: **SUPER IO NC87381**

Size	Document Number	Rev
A3	SNIPE	SA

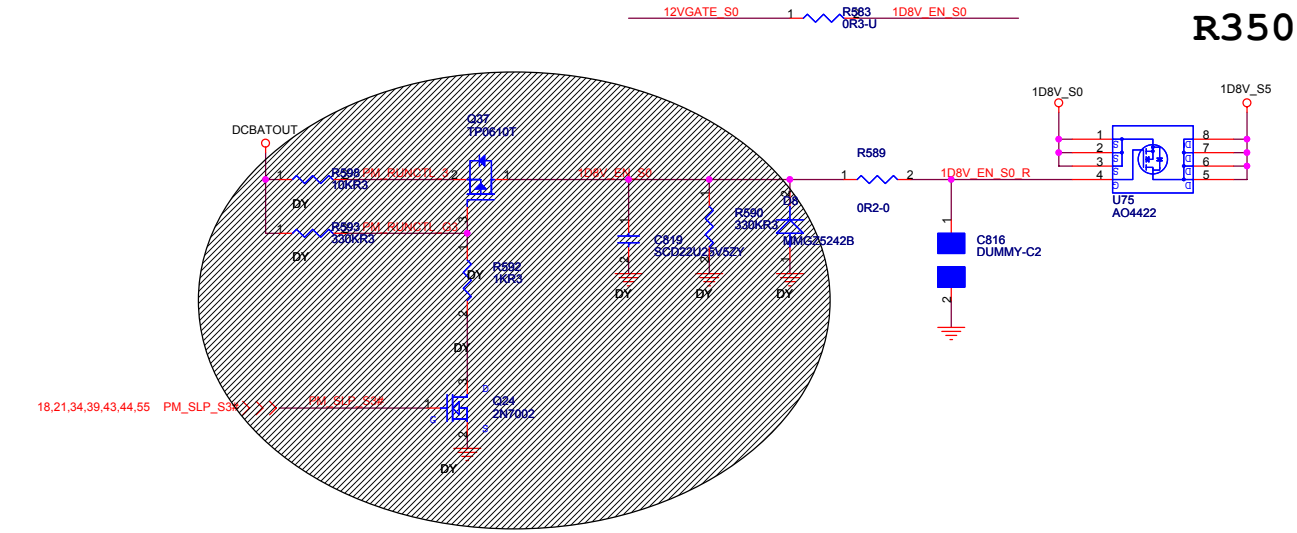
Date: Thursday, November 18, 2004 Sheet 37 of 56



Run Power



Suspend Power



R350 & R589 WILL BE REMOVED ON VER SB

Power On Logic

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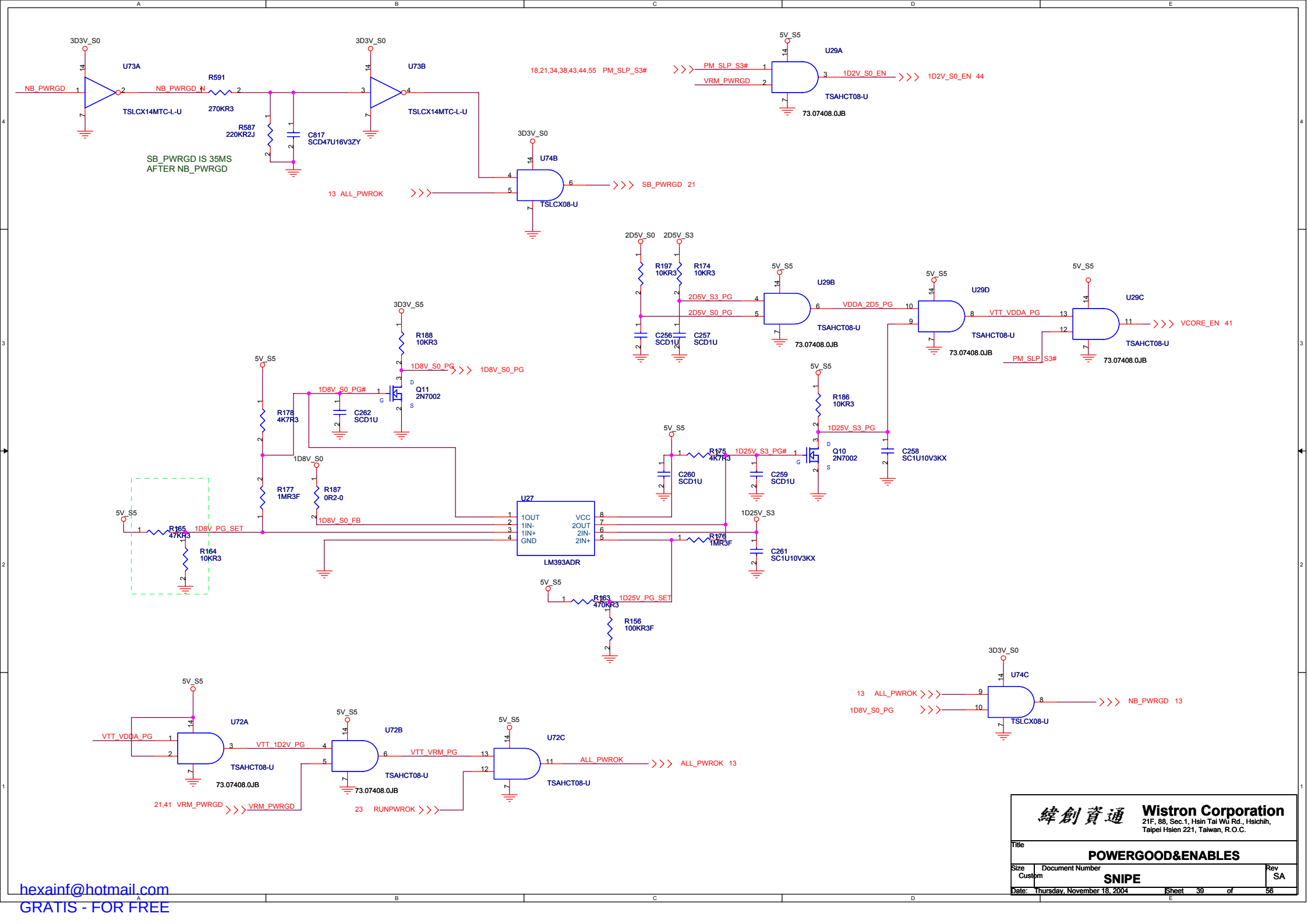
Title	PWR CTL LOGIC / PWR PLANE	
Size A3	Document Number SNIPE	Rev SA
Date: Thursday, November 18, 2004	Sheet 38 of 56	



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Title: **POWERGOOD&ENABLES**

Size	Document Number	Rev
Custom	SNIPE	SA

Date: Thursday, November 18, 2004 Sheet 39 of 56

CPU_CORE
Intersil 6559CR + ISL6207CB*3 (Dummy *1)

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Output Signal
PGOOD(OD / 3.3V) → VRM_PG

Output Power
VCC_CORE_PWR(O) → VCC_CORE_S0(Imax=53A)

VCORE_EN

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore) ← COREFB
RGND(I / Vcore) ← COREFB#

Input Power
VCC(I) ← DCBATOUT
VCC(I) ← 5V_S0
VCC(I) ← 3D3V_S0

TI TPS5130
2D5V/1D2V/1D8V

PM_SLP_S5#
1D2V_S0_EN
S5PWR_ENABLE
GND

Input Signal
SS_STBY1(I / 5V) FOR 2.5V
SS_STBY2(I / 5V) FOR 1.2V
SS_STBY3(I / 5V) FOR 1.8V
STBY_LDO(I / 5V)

DCBATOUT_5130
DCBATOUT_5130

STBY_VREF5(I / 28V)
STBY_VREF3.3(I / 28V)

Input Power
VIN (I / 28V) ← DCBATOUT
REG5V_IN(I / 5V) ← 5V_S5
5V_AUX_S5 ← 5V_AUX_S5
For PGOUT ← 5V_S0

Output Signal
PGOUT(OD / 5V) → Pull High (5V)

Output Power
2D5(O) → 2D5V (9A)
1D2V(O) → 1D2V (5A)
1D8V(O) → 1D8V (5A)
LDO(O)

5V_AUX_S5

DCBATOUT
AUX_SD
INPUT
SD
OUT → 5V_AUX_S5

LP2951ACM

1D25V_S3

2D5V_S3
5V_S5
APL5331_1D25V_VREF
VIN
VCNTL
VREF
VOUT → 1D25V_S0

APL5331KAC

FAN5234_VGA_Core
1D15V or 1D20V

5V_S0
DCBATOUT
PM_SLP_S3#

Input Power
VCC
VIN

Input Signal
EN

Output Signal
PG

Output Power
1D15V (O) or 1D20V (O) → 1D15V (5.2A) or 1D20V (9A)

Adapter

AD_OFF

Input Signal (I)
Output Signal (O) → AD_IN

AD_JK
5V_AUX_S5

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O) → AD+

Max1999
5V/3D3V

SHUTDOWN_S5
SHUTDOWN_S5
DCBATOUT
PM_SLP_S3#

Input Signal
ON3
ON5
SHDN#
SKIP#

Output Signal
PGOOD(OD / 5V) → MAX1999_PGD

Input Power
V+ ← DCBATOUT

Output Power
5V(O) → 5V_S5 (6A)
3D3V(O) → 3D3V_S5 (4A)
LDO5(O) → MAX1999_LDO5 (30mA)
LDO3 (O) → MAX1999_LDO3 (30mA)

Charger_Max1909

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V) → AD_IN
XTAL2/PB4 (O/5V) → CHARGE_LED#
XTAL1/PB3 (O/5V) → BL2#

Input Power
DCIN (I) ← AD+

Output Power
VCC (O) → DCBATOUT
VCC (O) → BT+

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**
Size: A3 | Document Number: SNIPE | Rev: SA
Date: Thursday, November 18, 2004 | Sheet 40 of 56

Vcore_CPU=1.500V
Iomax=52.9A
Vcore_CPU=1.400V
Iomax=42.7A

Vdrop is over spec under max loading

R value large, then offset small.
=> 3K or 4.99K?
Now=>Offset value is over 0.05V
If without offset =>R158=0ohm

Gain value large, then bandwidth large!
=> 2.74K or 3.65K

PLACE IN THE BACK OF CPU

Remote Sense Tie to CPU

SB

53A*1.5=79.5A (OCP),=>79.5A/2Phase=39.75A/Phase
90uA*Rsense=39.75A*(6.5m/2)*1.4
=>Rsense=2.0K

C216/C201/C140 Can not stuff!

Rt=10^[11.09-1.13log(fs)]
Rt=107K,=>fs=230KHz
But real freq.=270KHz

Follow MOSFET rise time spec.

DCR=1.3mohm+-10% / Imax=40A /
Panasonic /
ETQP2H0R7BF / 0.48uH /
13.4*13.3*4.9

Power-PAK
Id=7A
Qg=10~15nC
Rdson=13~16.5mohm

Power-PAK
Id=13A
Qg=32~50nC
Rdson=4~4.8mohm

BSC059N03S-U (84.59N03.037)
BSC042N03S-U (84.42N03.037)
2'nd Source:
H/S:SI7392DP (84.07392.037)
L/S:SI7636DP (84.07636.037)

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

Main Source:
KEMET 2D5V/ 330uF / ESR=9mohm / Iripple=3.7A / ST330U2D5VDM-3
80.3371V.191/ 7.3*4.3*1.9 / NT$:9.5
2'nd Source:
Panasonic 2V/ 330uF / ESR=9mohm / Iripple=3.0A/ SE330U2VDM-2
79.33719.20A/ 7.3*4.3*1.9 / NT$:10.0

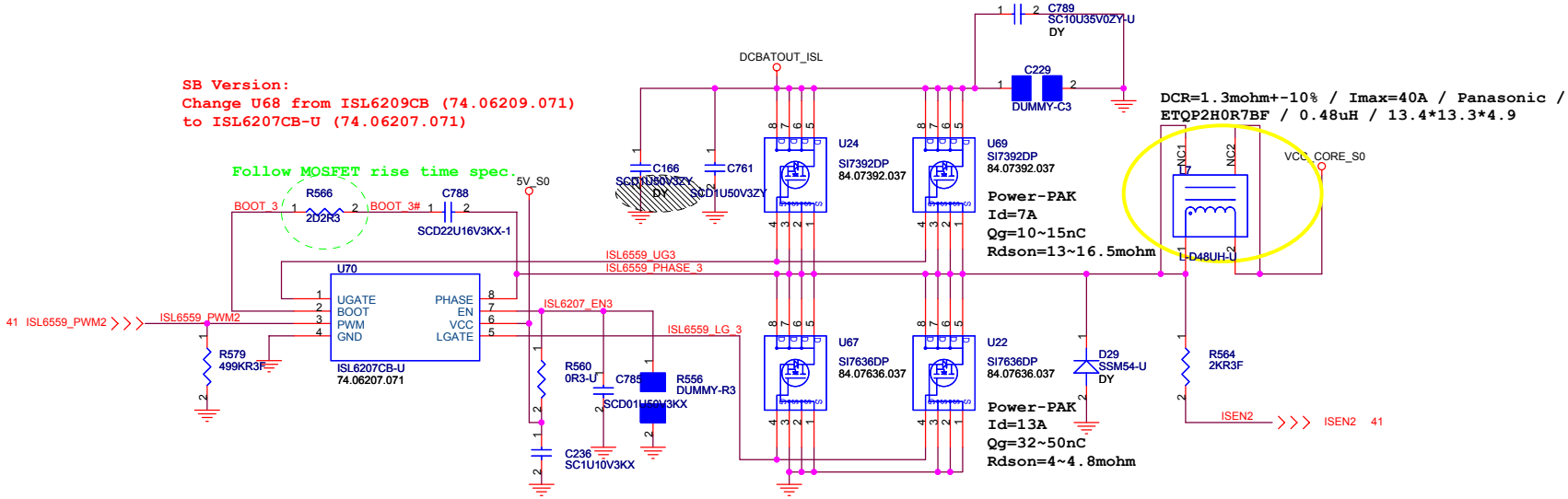
Panasonic 25V / E1 Cap.
8.5*6.5mm / SMD
ESR=0.26ohm, Iripple=0.3A
FX Serial

Follow MOSFET rise time spec.
=> Mount 0ohm first.

SB Version:
Change U4 from ISL6209CB (74.06209.071)
to ISL6207CB-U (74.06207.071)

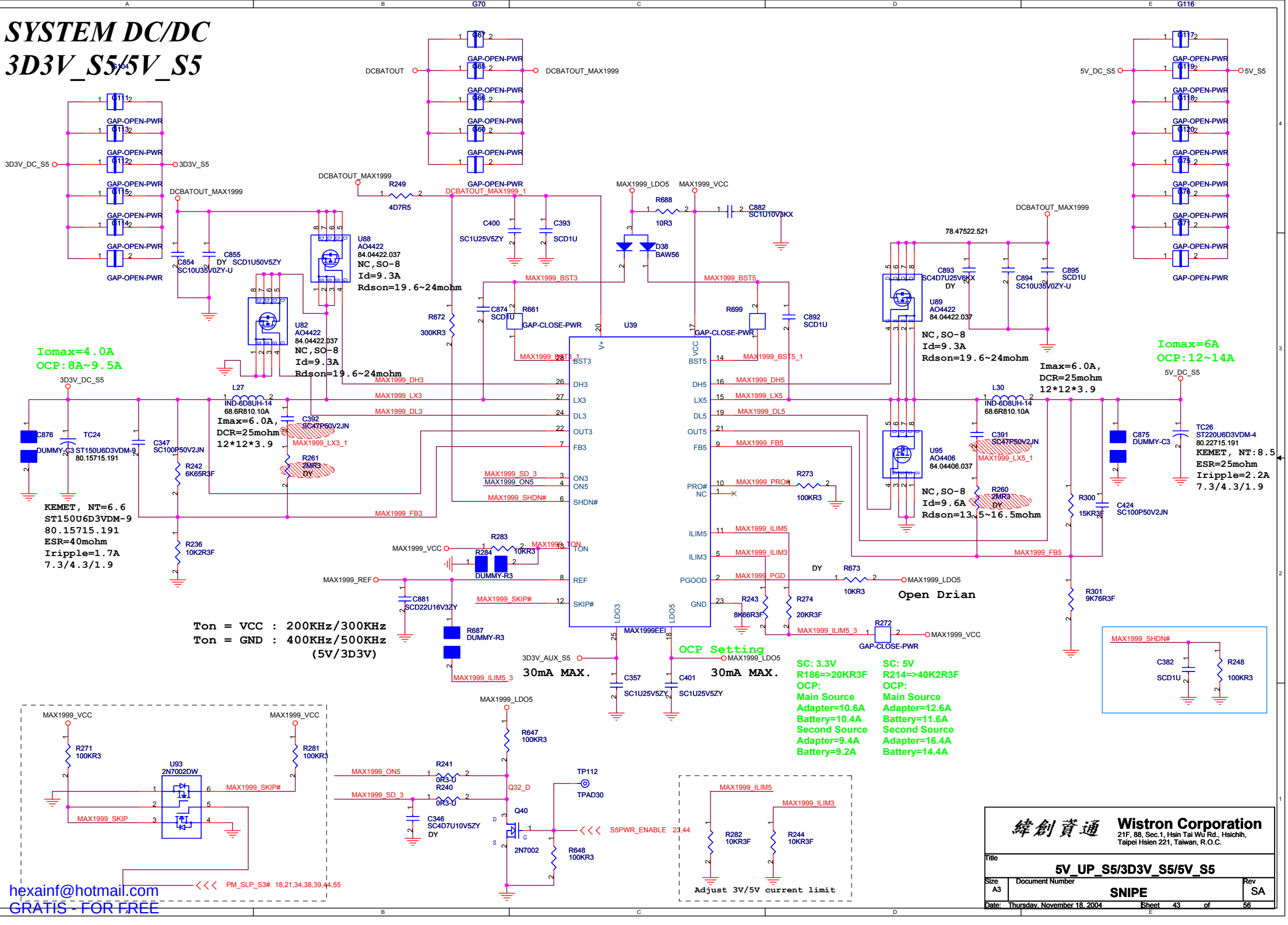
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_1
Size: A2 | Document Number: SNIPE | Rev: SA
Date: Thursday, November 18, 2004 | Sheet 41 of 58



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU Vcore Power_2**	
Size: A3	Document Number: **SNIPE**	Rev: SA
Date: Thursday, November 18, 2004	Sheet 42 of 56	

SYSTEM DC/DC
3D3V_S5/5V_S5



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	5V_UP_S5/3D3V_S5/5V_S5	
Size A3	Document Number SNIPE	Rev SA
Date: Thursday, November 18, 2004	Sheet 43 of 56	

TI TPS5130 for 2.5V, 1.2V, 1.8V

Vo=(R1*0.85)/R2+0.85

(2D5V=>CH1 , 1D2V=>CH2 , 1D8V =>CH3)

For 1.8V
SETTING=1.8275V

For 1.2V
SETTING=1.2172V

For 2.5V
SETTING=2.516V

close to IC

T(soft)=1.736ms

TPS5130

TPS5130PT-U

LDO SETTING

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

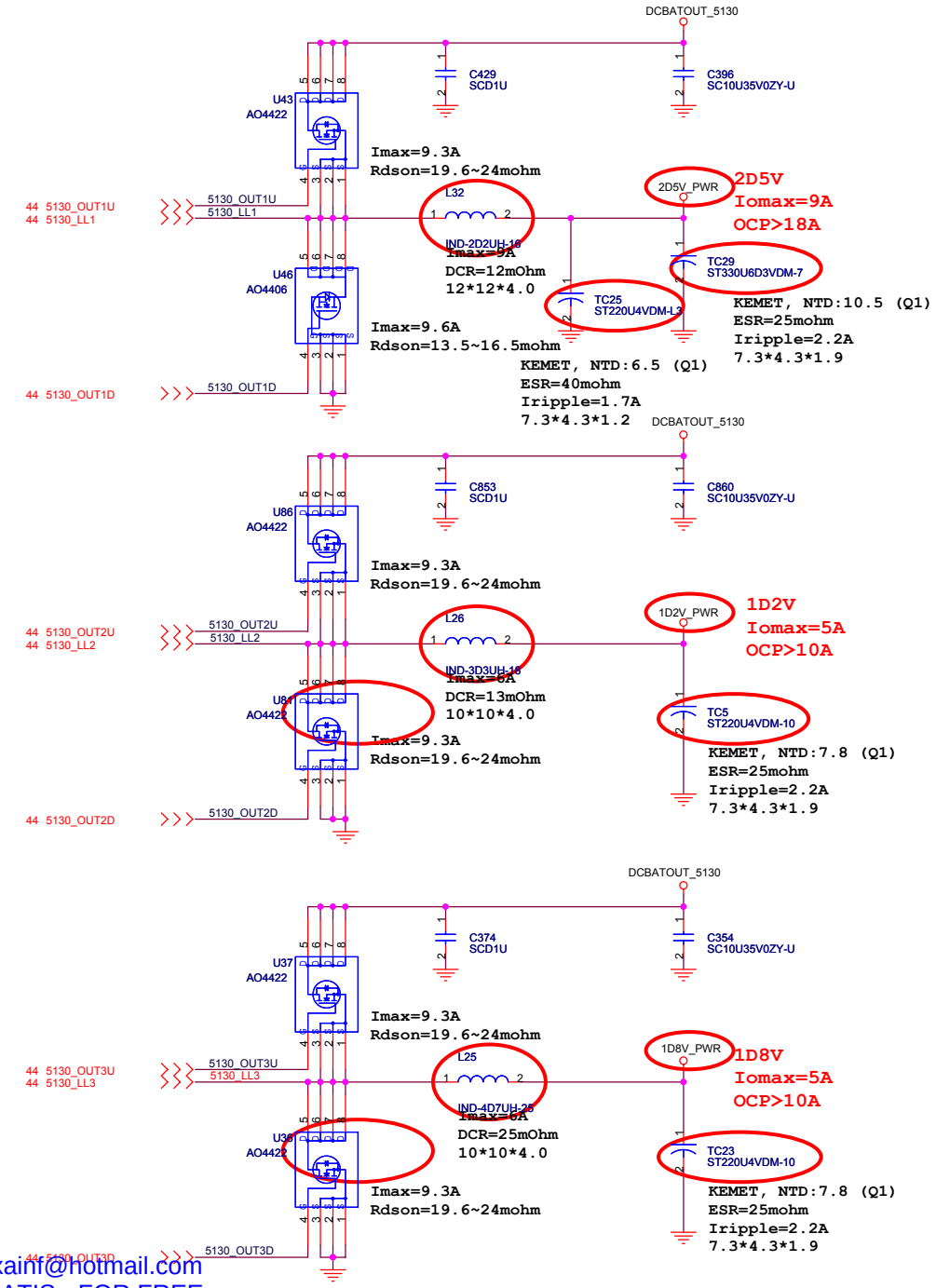
Title: TI TPS5130 2D5V/1D2V/1D8V (1/2)

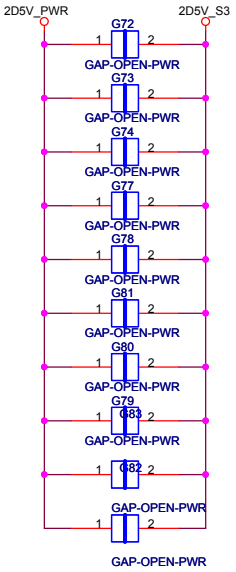
Size: A3 | Document Number: SNIPE | Rev: SA

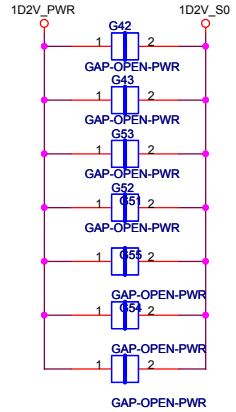
Date: Thursday, November 18, 2004 | Sheet 44 of 56

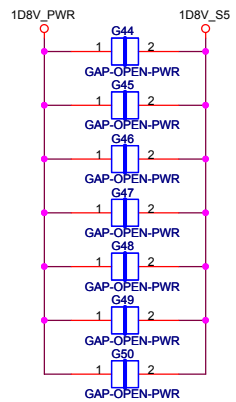
TI TPS5130 for 2D5V, 1D2V, 1D8V

(2D5V=>CH1 , 1D2V=>CH2 , 1D8V =>CH3)









緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TI TPS5130 2D5V/1D2V/1D8V (2/2)**

Size	Document Number	Rev
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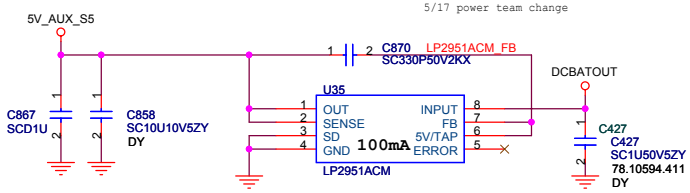
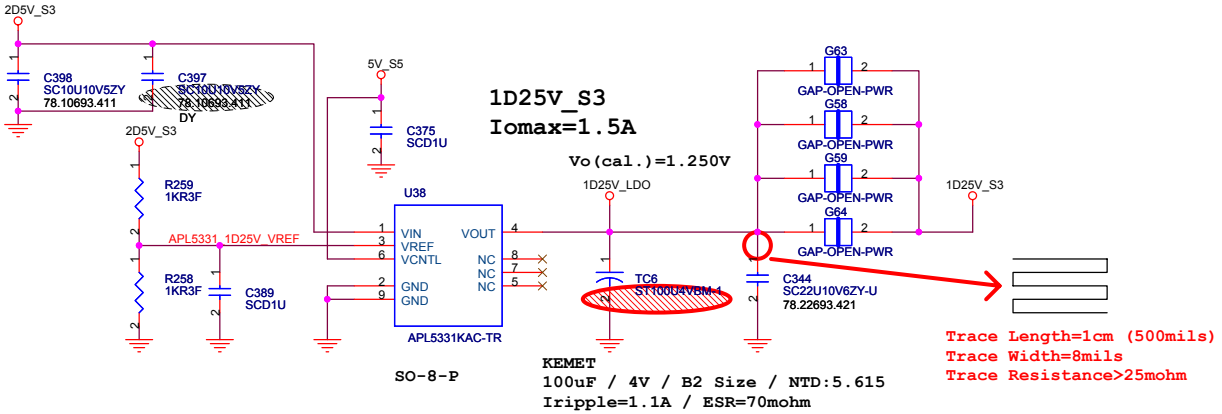
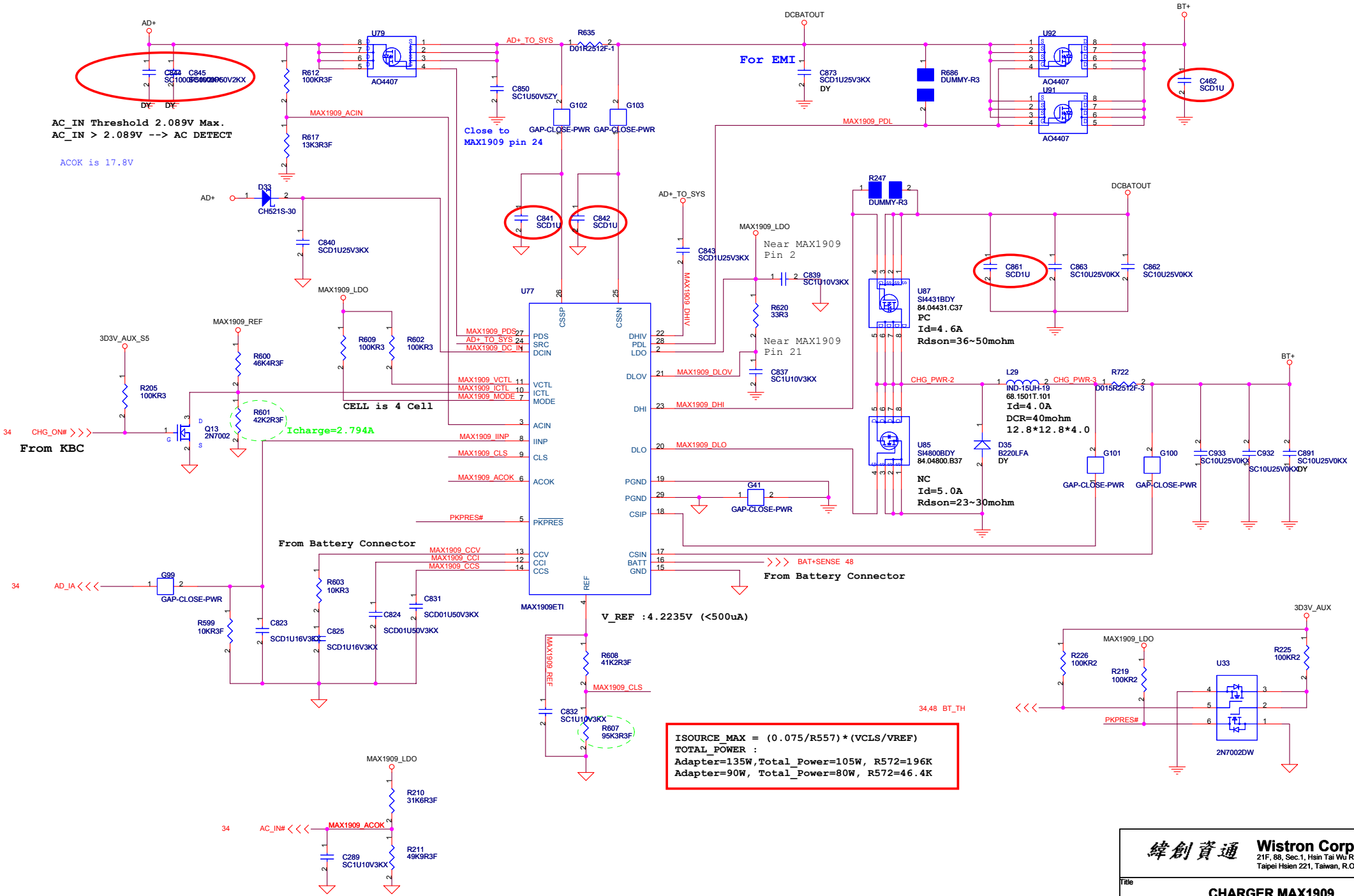
5V_AUX_S5

5/17 power team change





緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D2V_LDO/5V_AUX		
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 46 of 56	



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER MAX1909

Size: Custom | Document Number: SNIPE | Rev: SA

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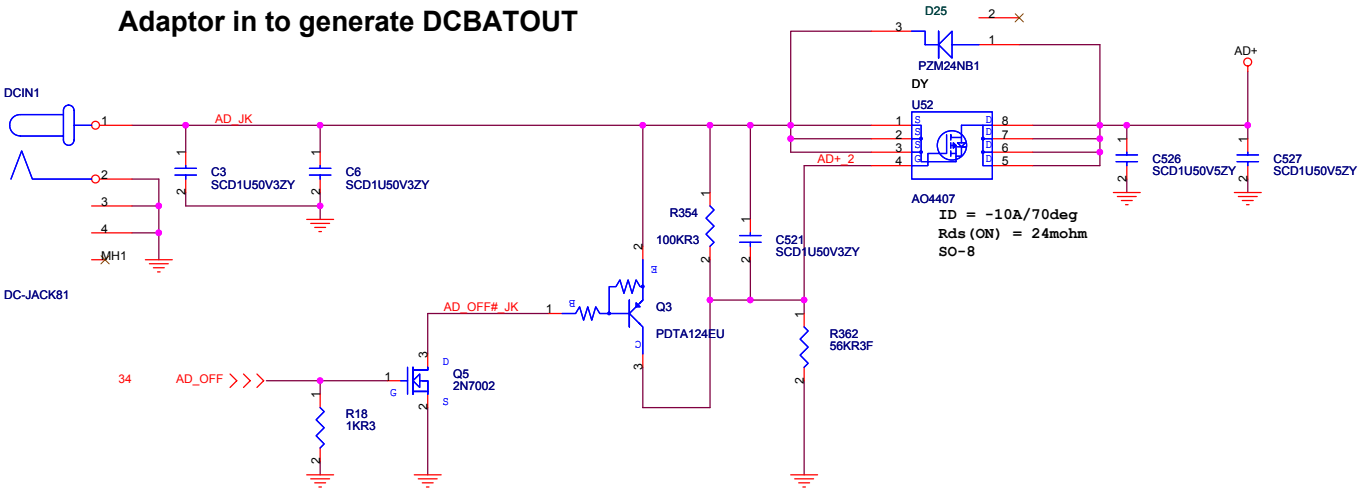
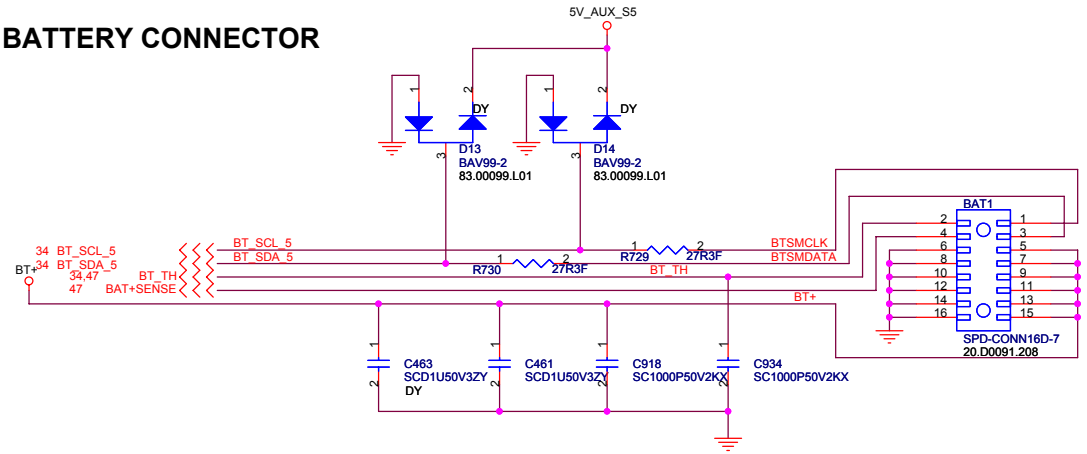
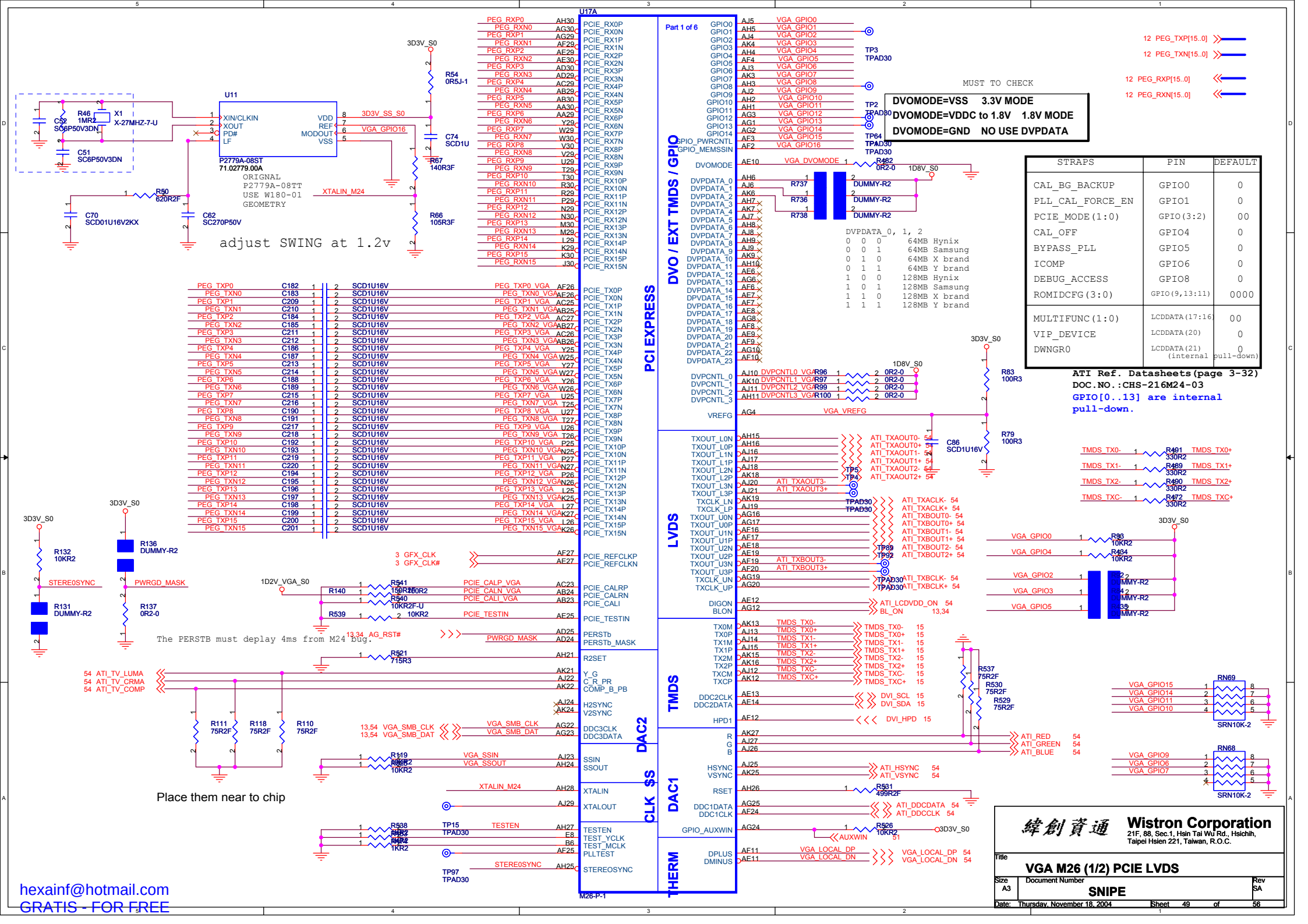
Adaptor in to generate DCBATOUT

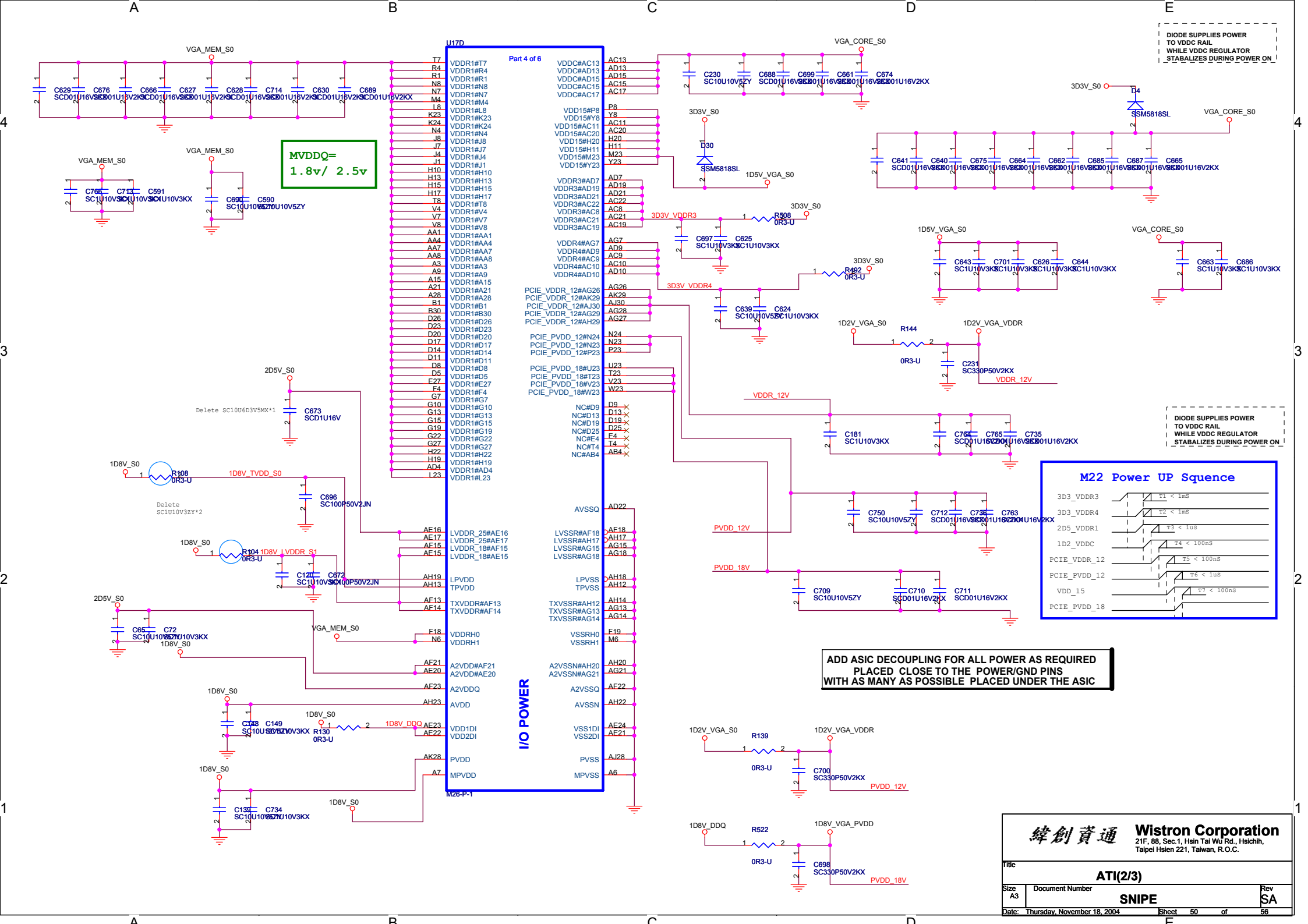


BATTERY CONNECTOR



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DC/DC (1/2) -- 5V / 3.3V / 2.5V		
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 48 of 56	


U17A
Part 1 of 6
PCI EXPRESS
DVO / EXT TMDS / GPIO
LVDS
TMDS
DAC2
DAC1
CLK $S
THERM
M26-P-1
U11
P2779A-08ST
71.02779.00A
ORIGNAL
P2779A-08TT
USE W180-01
GEOMETRY
adjust SWING at 1.2v
The PERSTB must deplay 4ms from M24 bug.
Place them near to chip
MUST TO CHECK
DVOMODE=VSS 3.3V MODE
DVOMODE=VDDC to 1.8V 1.8V MODE
DVOMODE=GND NO USE DVPDATA
STRAPS | PIN | DEFAULT
CAL_BG_BACKUP | GPIO0 | 0
PLL_CAL_FORCE_EN | GPIO1 | 0
PCIE_MODE(1:0) | GPIO(3:2) | 00
CAL_OFF | GPIO4 | 0
BYPASS_PLL | GPIO5 | 0
ICOMP | GPIO6 | 0
DEBUG_ACCESS | GPIO8 | 0
ROMIDCFG(3:0) | GPIO(9,13:11) | 0000
MULTIFUNC(1:0) | LCDDATA(17:16) | 00
VIP_DEVICE | LCDDATA(20) | 0
DWNGR0 | LCDDATA(21) | 0 (internal pull-down)
ATI Ref. Datasheets(page 3-32)
DOC.NO.:CHS-216M24-03
GPIO[0..13] are internal pull-down.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA M26 (1/2) PCIE LVDS
Size A3
Document Number SNIPE
Rev SA
Date: Thursday, November 18, 2004
Sheet 49 of 56
hexainf@hotmail.com
GRATIS - FOR FREE


U17D
Part 4 of 6
I/O POWER
M26-P-1
MVDDQ=
1.8v/ 2.5v
DIODE SUPPLIES POWER
TO VDDC RAIL
WHILE VDDC REGULATOR
STABALIZES DURING POWER ON
M22 Power UP Squence
3D3_VDDR3
3D3_VDDR4
2D5_VDDR1
1D2_VDDC
PCIE_VDDR_12
PCIE_PVDD_12
VDD_15
PCIE_PVDD_18
T1 < 1mS
T2 < 1mS
T3 < 1uS
T4 < 100nS
T5 < 100nS
T6 < 1uS
T7 < 100nS
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED
PLACED CLOSE TO THE POWER/GND PINS
WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
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Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI(2/3)
Size A3
Document Number
SNIPE
Rev SA
Date: Thursday, November 18, 2004
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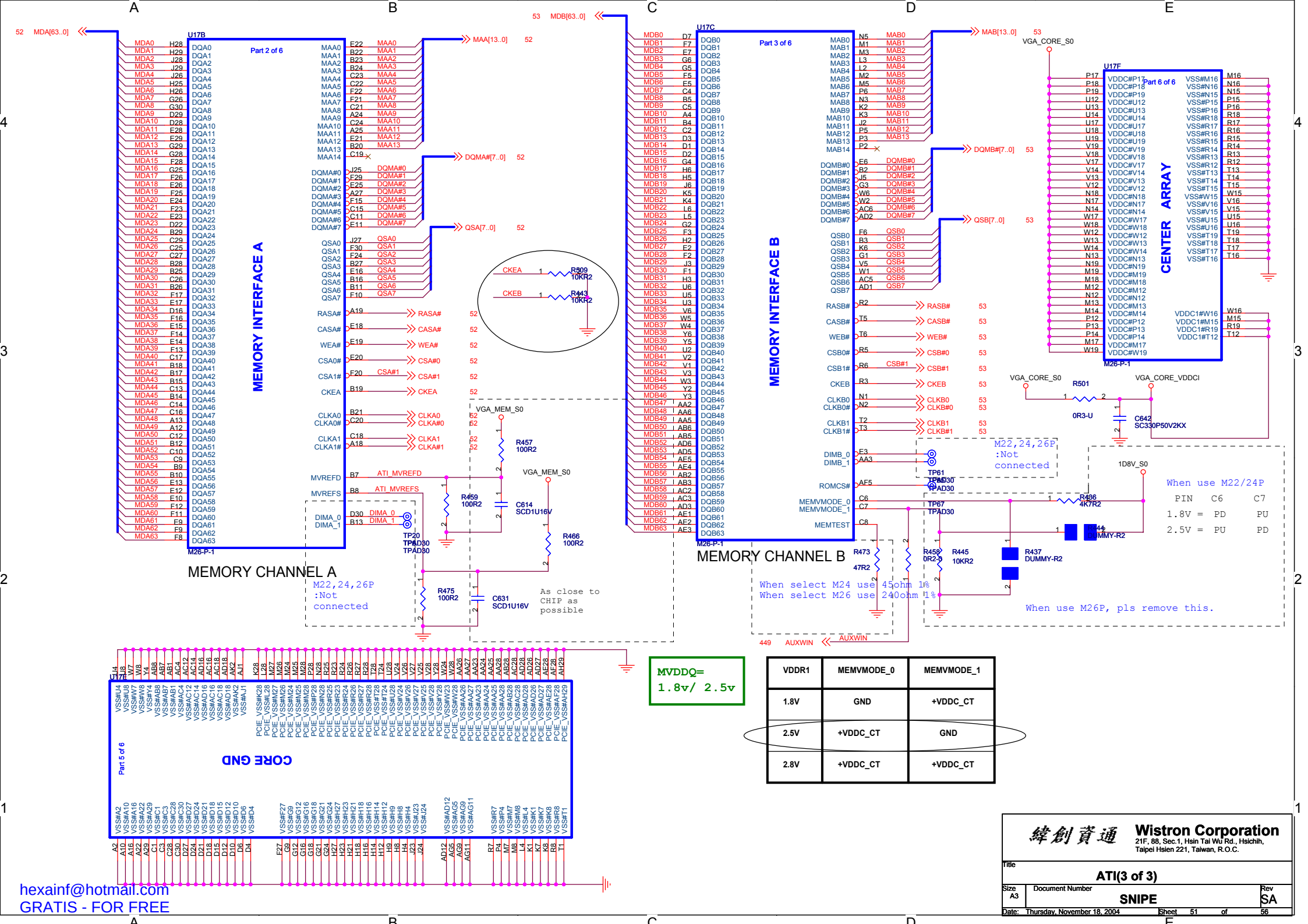
MEMORY INTERFACE A
MEMORY CHANNEL A
MEMORY INTERFACE B
MEMORY CHANNEL B
CENTER ARRAY
CORE GND
M22,24,26P :Not connected
When use M22/24P
PIN C6 C7
1.8V = PD PU
2.5V = PU PD
When use M26P, pls remove this.
When select M24 use 45ohm 1%
When select M26 use 240ohm 1%
As close to CHIP as possible
MVDDQ= 1.8v/ 2.5v
VDDR1 MEMVMODE_0 MEMVMODE_1
1.8V GND +VDDC_CT
2.5V +VDDC_CT GND
2.8V +VDDC_CT +VDDC_CT
Wistron Corporation
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ATI(3 of 3)
SNIPE
Thursday, November 18, 2004
hexainf@hotmail.com
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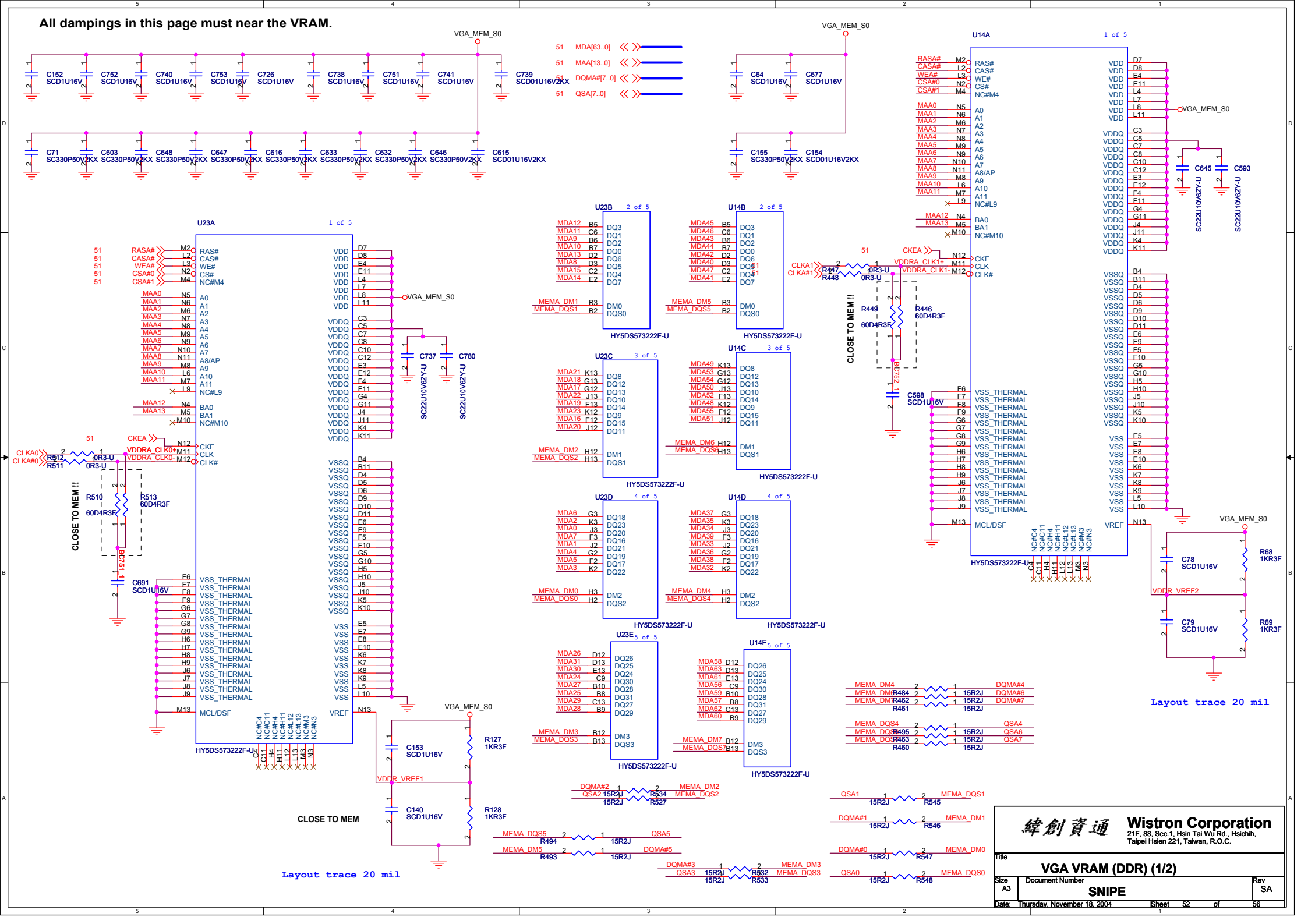
All dampings in this page must near the VRAM.



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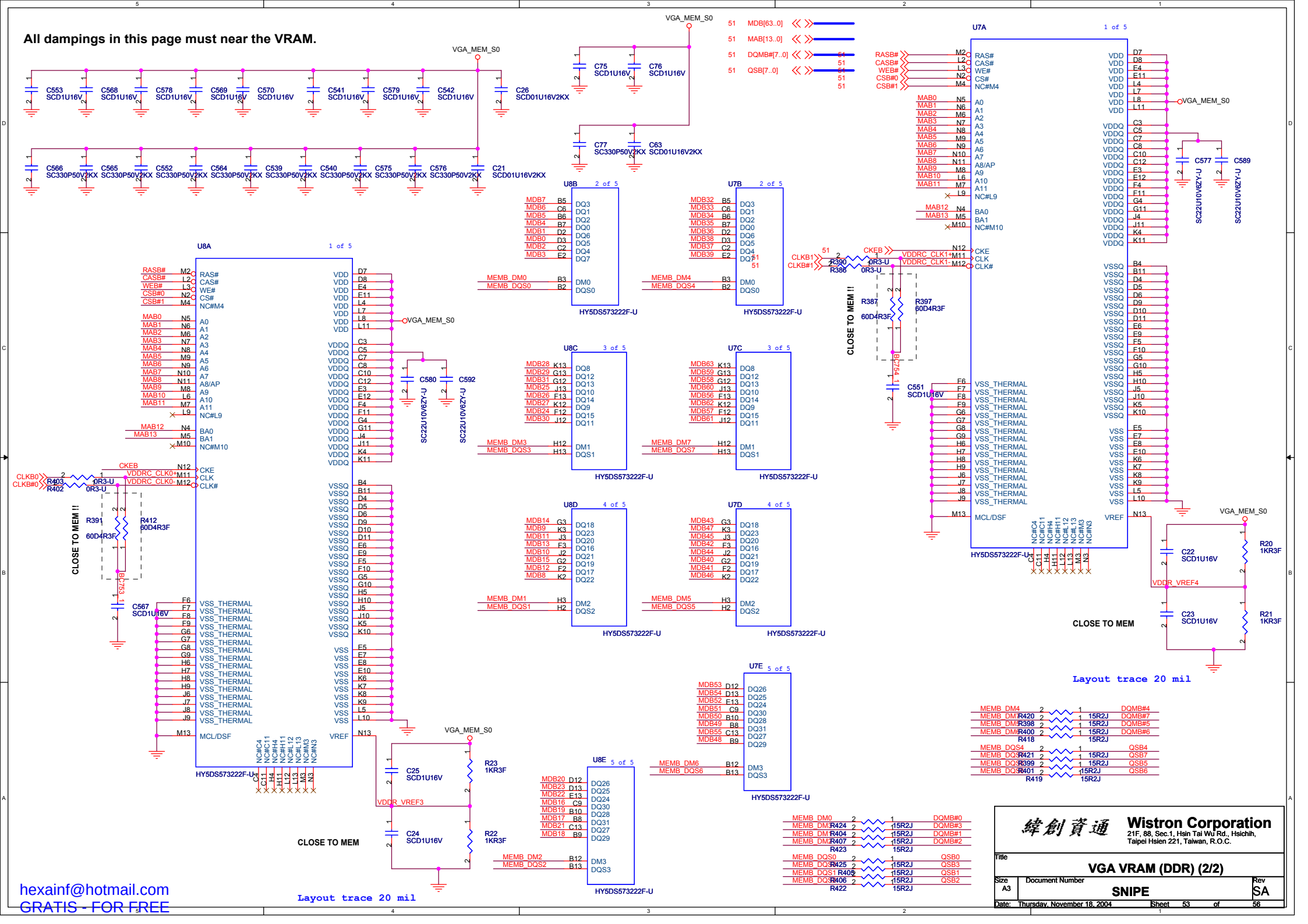
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VGA VRAM (DDR) (1/2)**

Size	Document Number	Rev
A3	SNIPE	SA

Date: Thursday, November 18, 2004 Sheet 52 of 56

All dampings in this page must near the VRAM.



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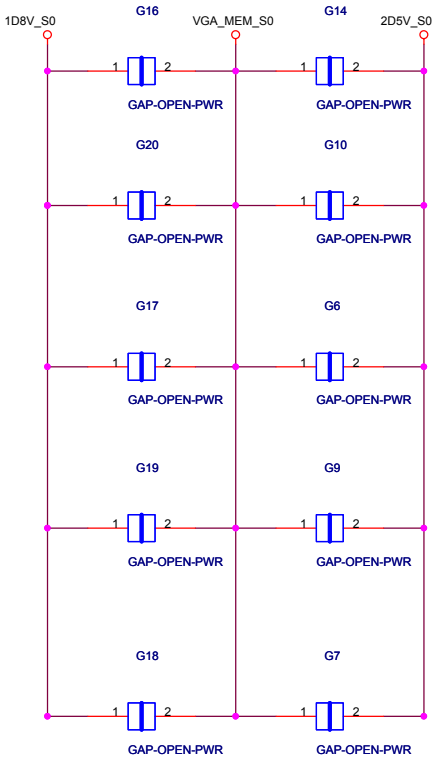
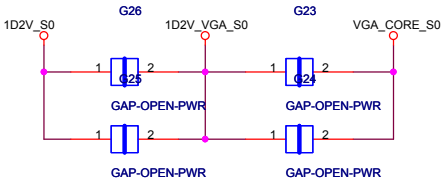
Taipei Hsien 221, Taiwan, R.O.C.

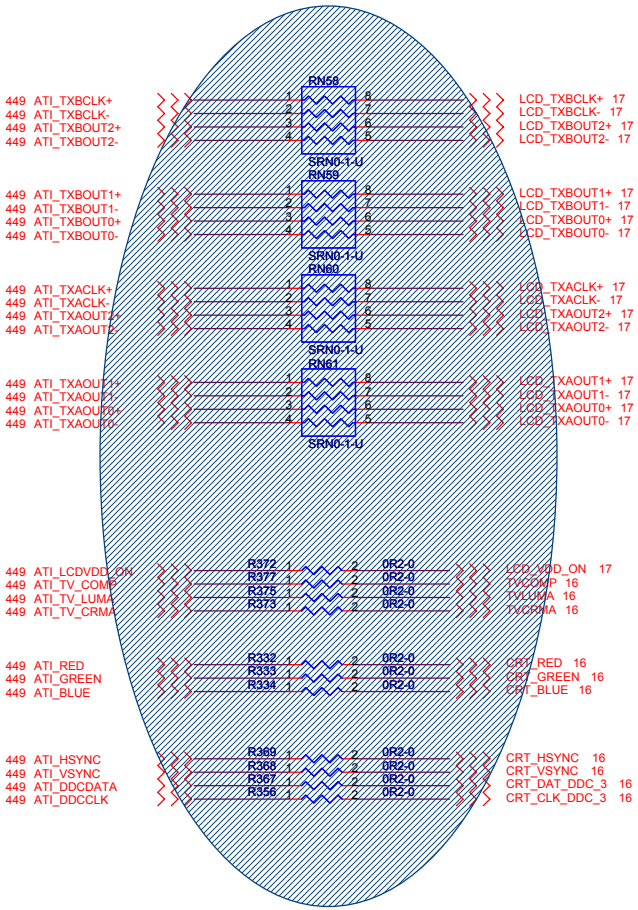
Title: VGA VRAM (DDR) (2/2)

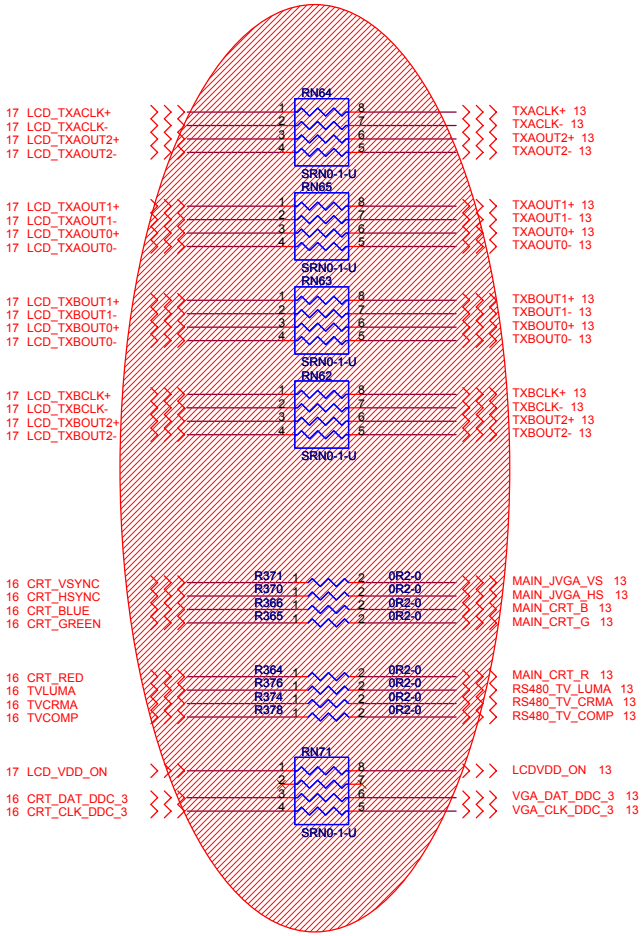
Size: A3 | Document Number: SNIPE | Rev: SA

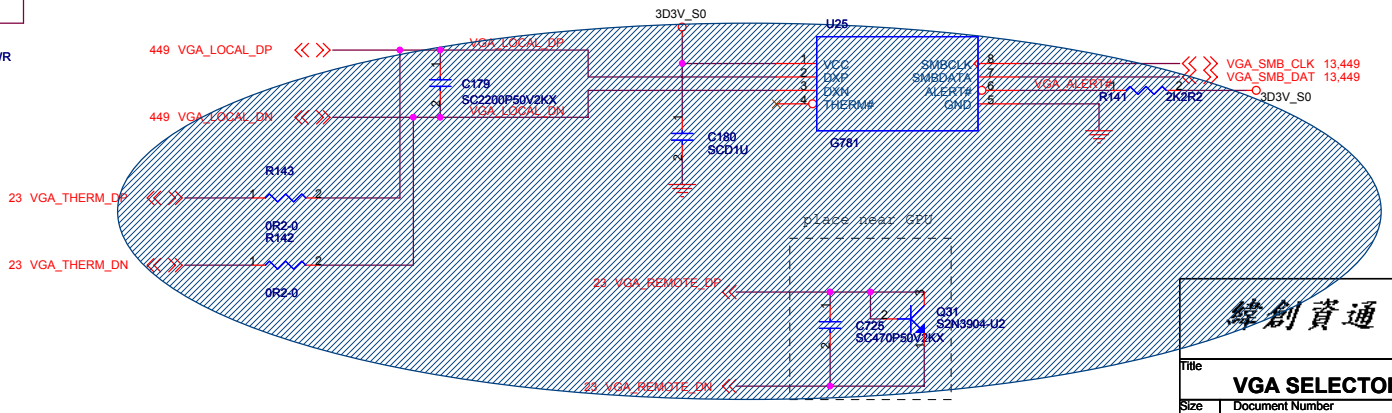
Date: Thursday, November 18, 2004 | Sheet 53 of 56











緯創資通
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **VGA SELECTOR**

Size	Document Number	Rev
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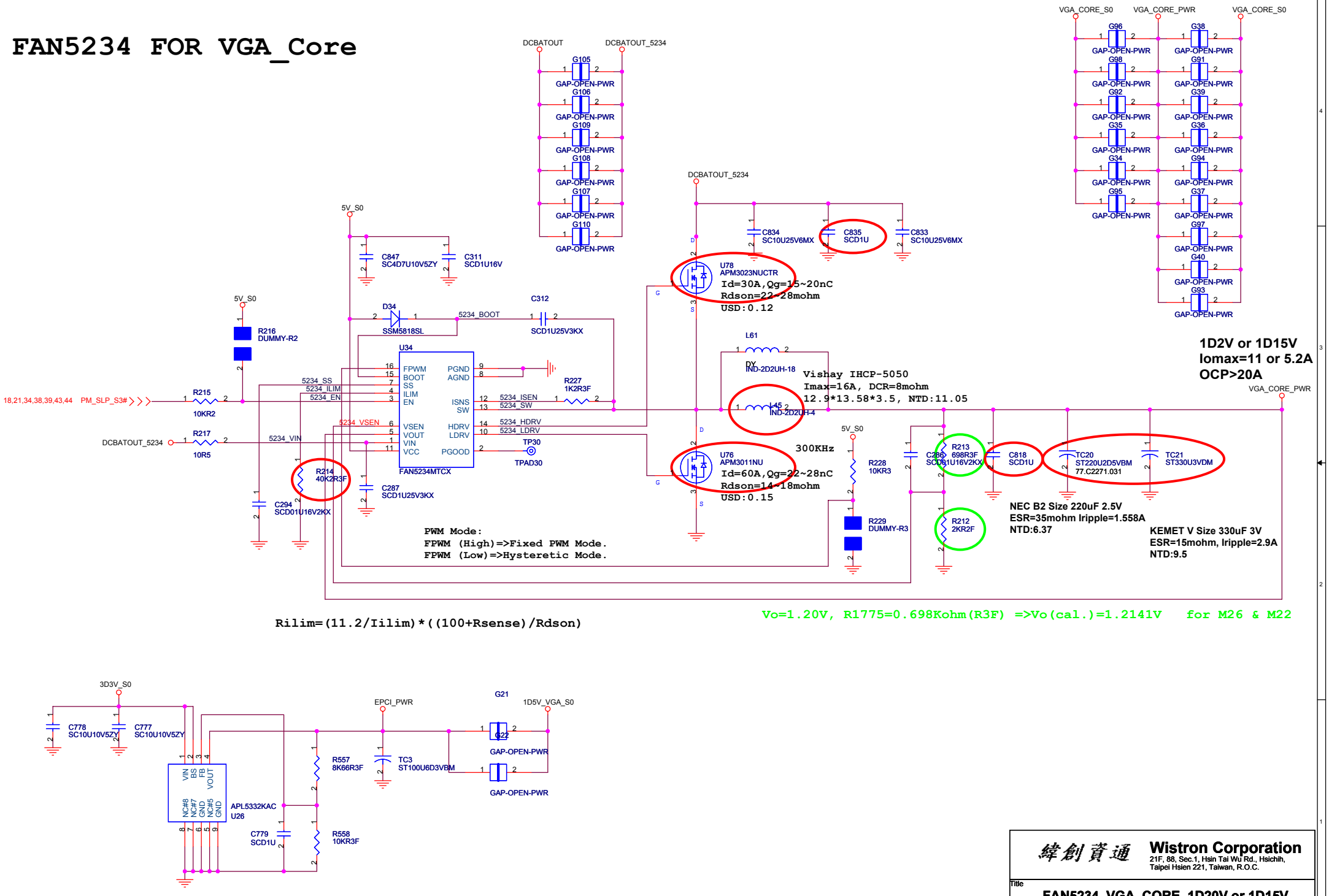
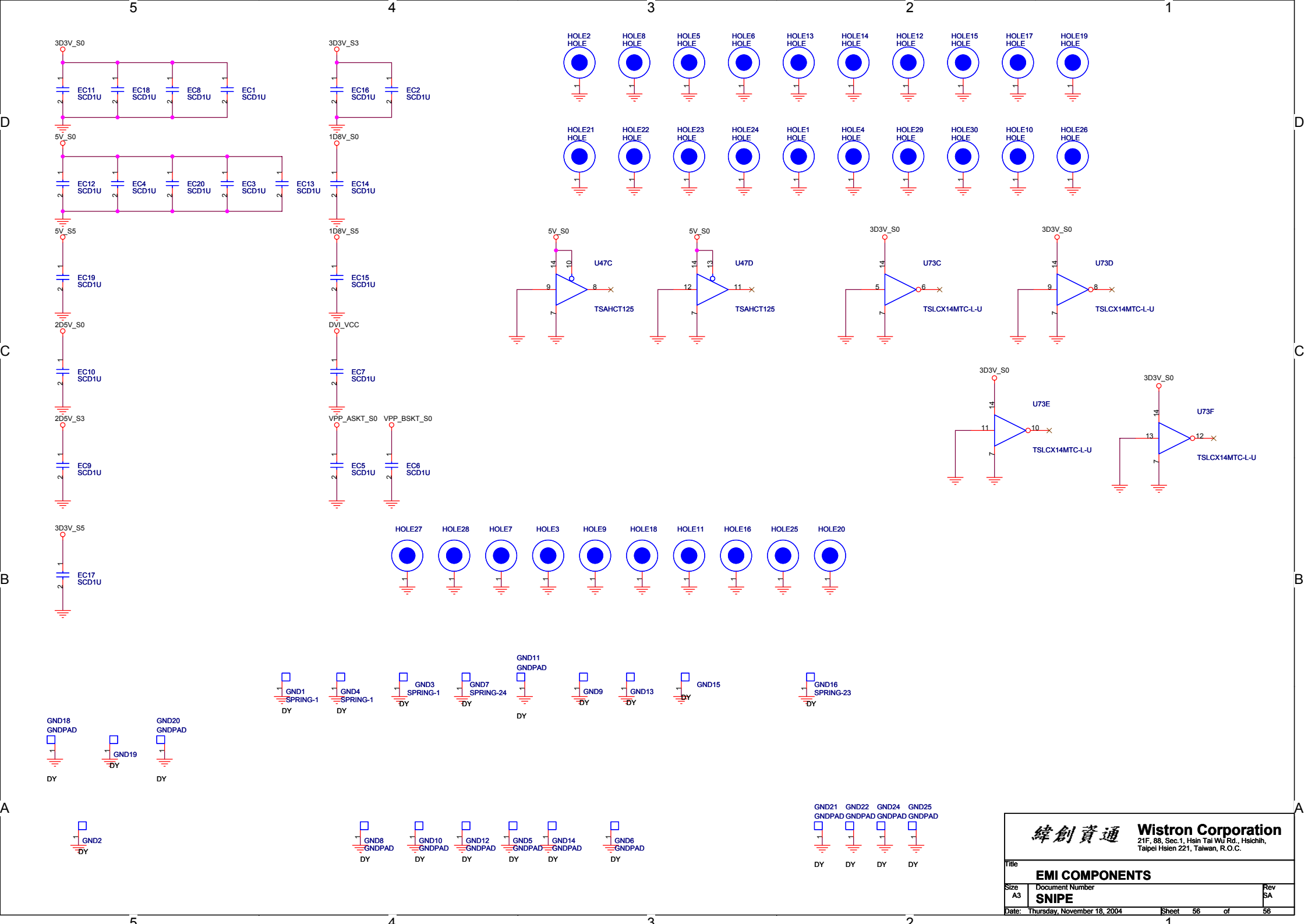
FAN5234 FOR VGA_Core



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	FAN5234_VGA_CORE_1D20V or 1D15V	
Size A3	Document Number SNIPE	Rev SA
Date: Thursday, November 18, 2004	Sheet 55 of 56	



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI COMPONENTS**

Size	Document Number	Rev
A3	SNIPE	SA

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