ACER_BAP31

MAIN BOARD

2008.12.29

Tuesday, March 10, 2009		X01
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:

FILE NAME: XXXX-XXXXXX-XX

P/N XXXXXXXXXXX

INVENTEC

TITLE: ACER_JM31

SIZE	CODE	DOC.NUMBER	REV
C	X01	D-CS-1310A2264501-ALG	X01

SHEET 1 of 36

1. Schematic Page Description :

Montevina Schematic Ver : X01

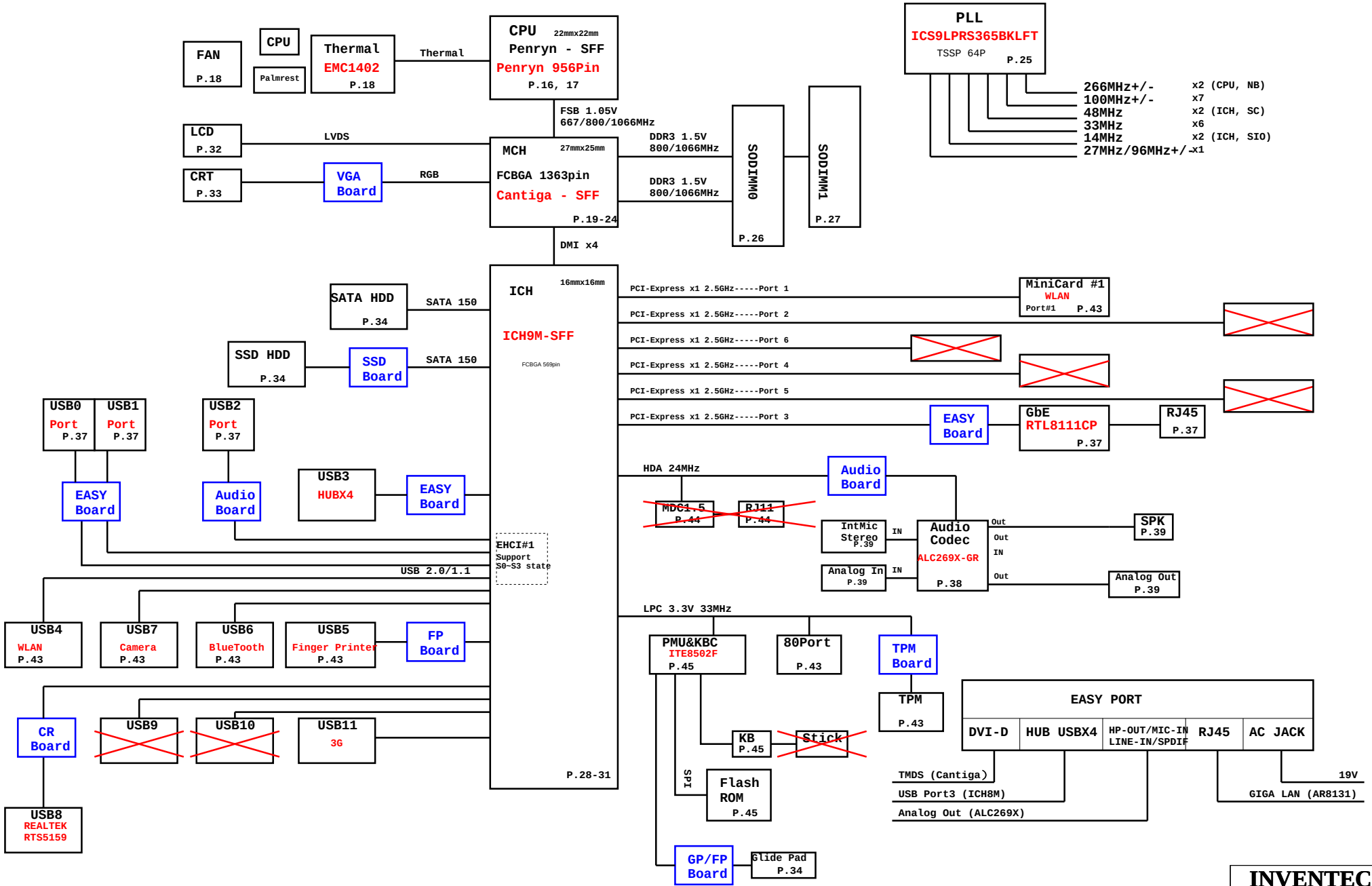
1. Title
2. Schematic Page DESCR
3. Block Diagram
4. Annotations
5. Schematic Modify
6. Timing Diagram
7. Power Block Diagram
8. Adaptor in/Charge
9. 5VLA/5VA/3VA
10. 3VS/5VS/1.5V (DDR3)
11. 1.05VS/1.5S/1.8V/1.5VA
12. Power Latch/1.5VS/SCREW HOLE
13. CPU Core Power
14. GPU Core Power
15. Penryn Processor(1/2)
16. Penryn Processor(2/2)
17. CPU Thermal
18. Cantiga Host(1/6)
19. Cantiga DMI/Graph(2/6)
20. Cantiga DDRII(3/6)
21. Cantiga Power(4/6)
22. Cantiga Power(5/6)
23. Cantiga Ground(6/6)
24. Clock Generator
25. DDR3 SDRAM SO-DIMM0
26. DDR3 SDRAM SO-DIMM1
27. ICH9M CPU/IDE/SATA(1/4)
28. ICH9M PCI/PCIE/DMI/USB(2/4)
29. ICH9M GPIO(3/4)
30. ICH9M Power/GND(4/4)
31. LCD CNN/SATA/3G/WLAN
32. KBC ITE8512F
33. IO CN

CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF Schematic Page			
SIZE: Custom	CODE: X01	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: X01
SHEET: 2 of 36			

3. Block Diagram :



INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF Block Diagram			
SIZE: Custom	CODE: X01	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: X01
CHANGE by: Miles Liu	DATE: Tuesday, March 10, 2009	SHEET	

4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer
Layer 4	Power Plane
Layer 5	Stripline Layer
Layer 6	Stripline Layer
Layer 7	Ground Plane
Layer 8	Solder Side,Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM:	1.3319V~1.4375V~1.4591V	18A
	LFM:	0.9221V~0.9625V~0.9739V	
1.05VS	Penryn SFF : AGTL+ termination	1V~1.05V~1.10V	4.5A
	Cantiga GS: Core	0.997V~1.05V~1.102V	8.7A
	Cantiga GS: PCIE	0.9975V~1.05V~1.1025V	1.78A
	Cantiga GS:Core+IMEL+HSIO	0.9975V~1.05V~1.1025V	2.898A
	Cantiga GS:VCC_GMCH	0.997V~1.05V~1.102V	10.154A
	Cantiga GS:VCCA_SM_CK and NCTF	0.997V~1.05V~1.102V	37.95mA
	Cantiga GS:VCC_DMI	0.997V~1.05V~1.102V	456mA
	Cantiga GS:VCCA_SM	0.997V~1.05V~1.102V	747.5mA
	Cantiga GS:VTT	0.997V~1.05V~1.102V	852mA
	ICH9M:VCC1_05	0.997V~1.05V~1.102V	1.634A
	ICH9M:DMI	0.997V~1.05V~1.102V	48mA
	ICH9M:CPU_IO	0.997V~1.05V~1.102V	2mA
1.5VS	Penryn SFF PLL	1.425V~1.5V~1.575V	130mA
	Cantiga GS: QDAC	1.425V~1.5V~1.575V	0.5mA
	Cantiga GS: LVDS	1.71V~1.8V~1.89V	60.31mA
	Cantiga GS: TVDAC	1.425V~1.5V~1.575V	35mA
	Cantiga GS: Various PLLS analog supply	1.425V~1.5V~1.575V	485mA
	Cantiga GS: VCC_SM_CK	1.425V~1.5V~1.575V	149.5mA
	Cantiga GS: VCC_SM	1.425V~1.5V~1.575V	3.1625A
	ICH9M:PCIE_ICH	1.425V~1.5V~1.575V	646mA
	ICH9M:SATA_ICH	1.425V~1.5V~1.575V	1.342A
	ICH9M:VCC_GLAN	1.425V~1.5V~1.575V	80mA
	Mini Card:		
	Express Card:	1.425V~1.5V~1.575V	650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V~1.5V~1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V~0.75V~0.7875V	1.0A
3VS	Cantiga GS: HV CMOS	3.135V~3.3V~3.465V	105.3mA
	Cantiga GS: VCCS_TVDAC	3.135V~3.3V~3.465V	78mA
	ICH9M:VCC3_3	3.135V~3.3V~3.465V	308mA
	ICH9M:VCCGLAN3_3	3.135V~3.3V~3.465V	1mA
	Thermal Sensor:	3.0V~3.3V~3.6V	5mA
	Mini Card: UMTS		
	Express Card:	3.135V~3.3V~3.465V	1.3A
	CLK Generator: ICS9LPRS365BKLFT	3.135V~3.3V~3.465V	500mA
	Mini Card: WirelessLan		
	Bluetooth:		
	Super I/O: IT8305E	3.0V~3.3V~3.6V	
	Azalia Codec: ALC262		
	Azalia MDC:		
1.8VS	DVI	3.0V~3.3V~3.6V	120mA
3VA	ICH9M: RTC	2V~3.3V~3.465V	6uA
	ICH9M:VCCSUS3_3	3.135V~3.3V~3.465V	212mA
	ICH9M:VCCCL3_3	3.135V~3.3V~3.465V	73mA
	ICH9M:VCCLAN3_3	3.135V~3.3V~3.465V	78mA
	LCD:	3.0V~3.3V~3.6V	2A
	Lan:AR8131	3.0V~3.3V~3.6V	1A
	Azalia MDC:		
	Flash ROM: BIOS	3.0V~3.3V~3.6V	
5VS	Cardreader: RTS5159	3.0V~3.3V~3.6V	
	Azalia Codec: ALC269	3.0V~3.3V~3.6V	
	HDD: SATA	4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA
	~~ODD: SATA~~	~~4.75V~5.0V~5.25V~~	~~Max: 1.5A ; R/W: 900mA ; STDBY: 45mA~~
	~~Audio AMP: G1432~~		
	Inverter:		
	WebCam	4.75V~5.0V~5.25V	1A
5VA	USB: x 2 ports	5VA	2A
	USB	5VA	1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V~3.3V~3.6V	300mA

INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
ANNOTATIONS

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by: Miles Liu | DATE: Tuesday, March 10, 2009 | SHEET 4 of 36

6.Schematic modify Item and History :

2009.0108

1. ADD USB P3 for Docking, USB P5 for Finger printer,
   Modify CN5 -----P28
2. Modify CN20 to 50pin-------P33
3. Move PWR_SWIN# from CN14 to CN20
4. ADD TPM module------P34

2009.0109

1. ADD DOCK_USB_EN, DOCK_CRT_IN#-----P32,33

2009.0112

1. Change power item: R490,R291,BAT CNN TH PIN

INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
Schematic Modify

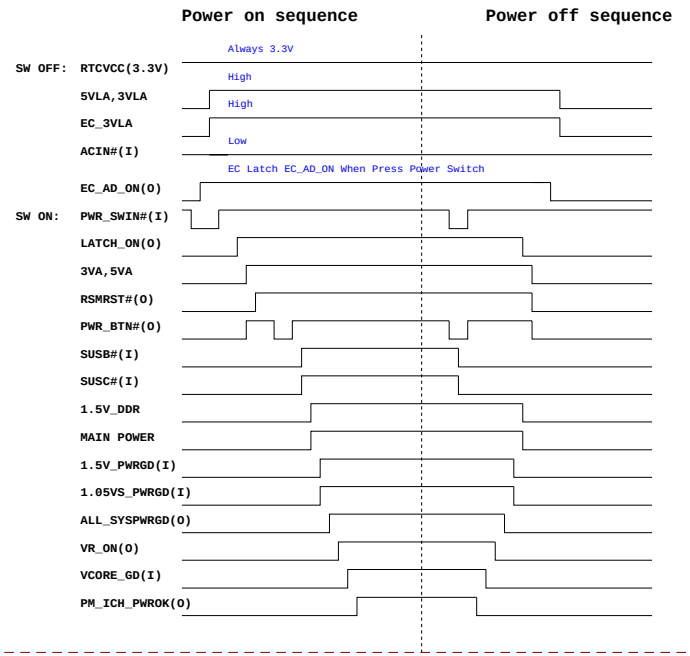
SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by: Miles Liu | DATE: Tuesday, March 10, 2009 | SHEET

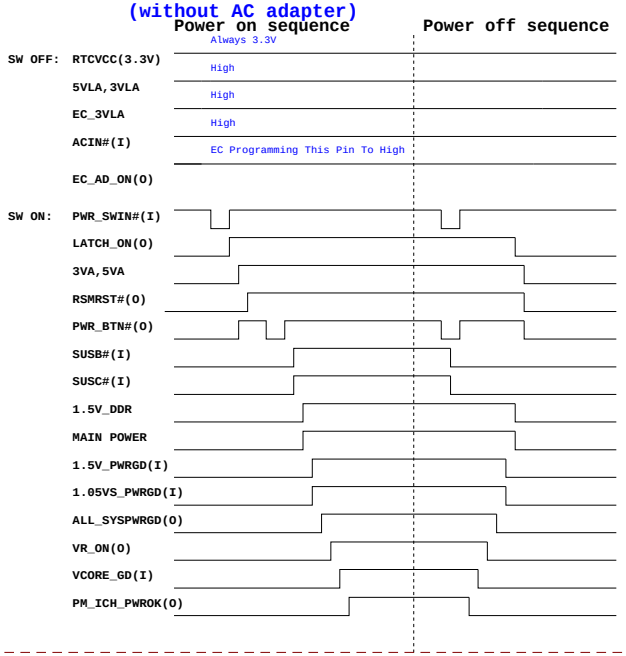
SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

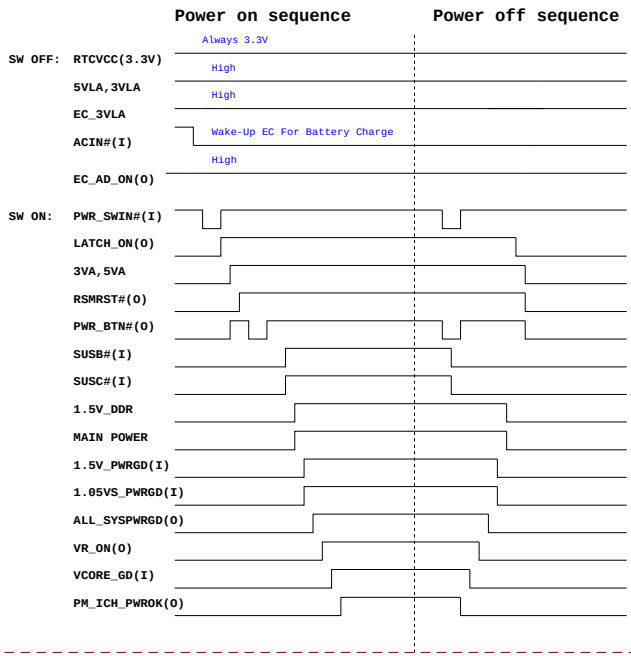
Power on/off sequence AC insert (without Battery Pack)



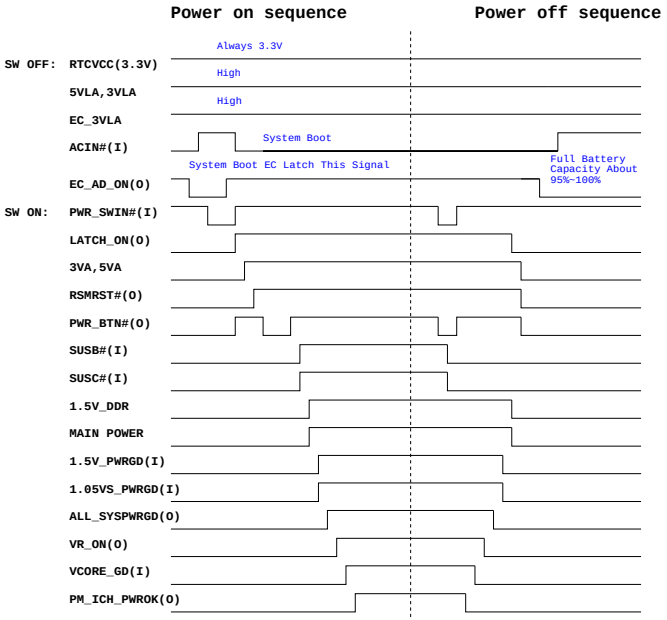
Power on/off sequence Battery insert (without AC adapter)



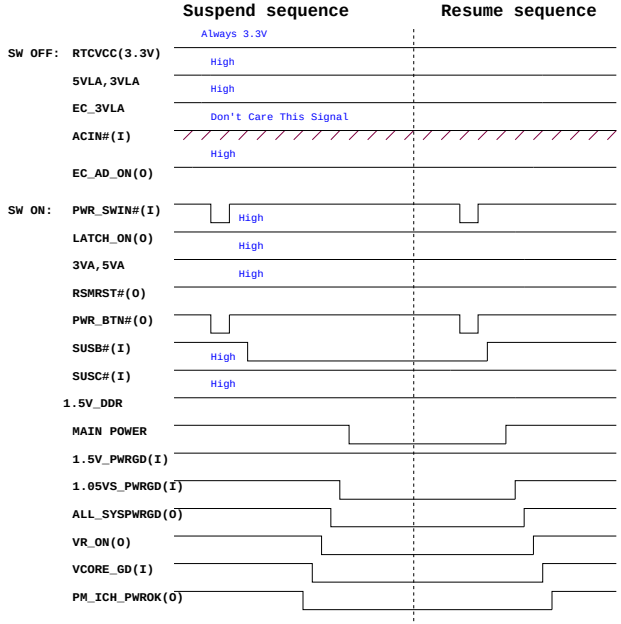
Power on/off sequence AC insert(with charge over 95%)



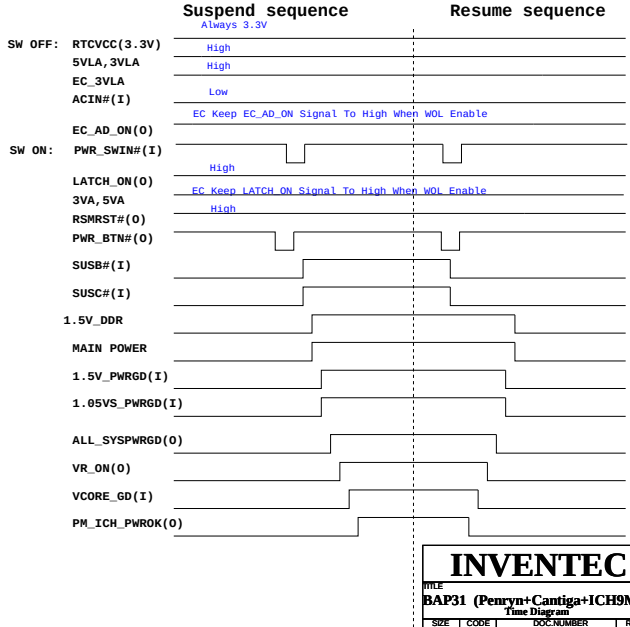
Power on/off sequence AC insert(without charge over 95%)



Suspend And Resume Sequence (S3)



Power on/off sequence after windows shoutdown (WOL enable)



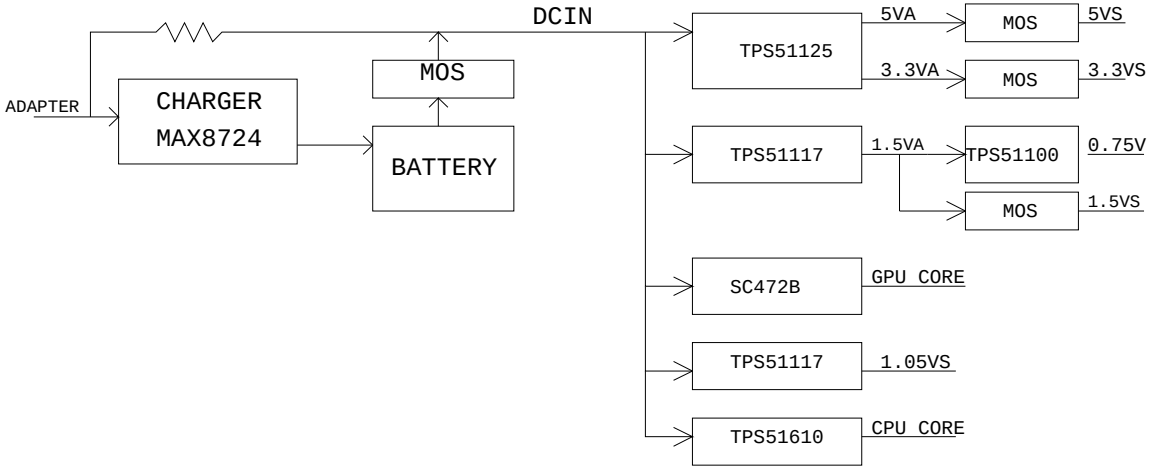
INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
Time Diagram

SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by: Milles Liu | DATE: Tuesday, March 10, 2009 | SHEET 6 of 36

Power Block Diagram :



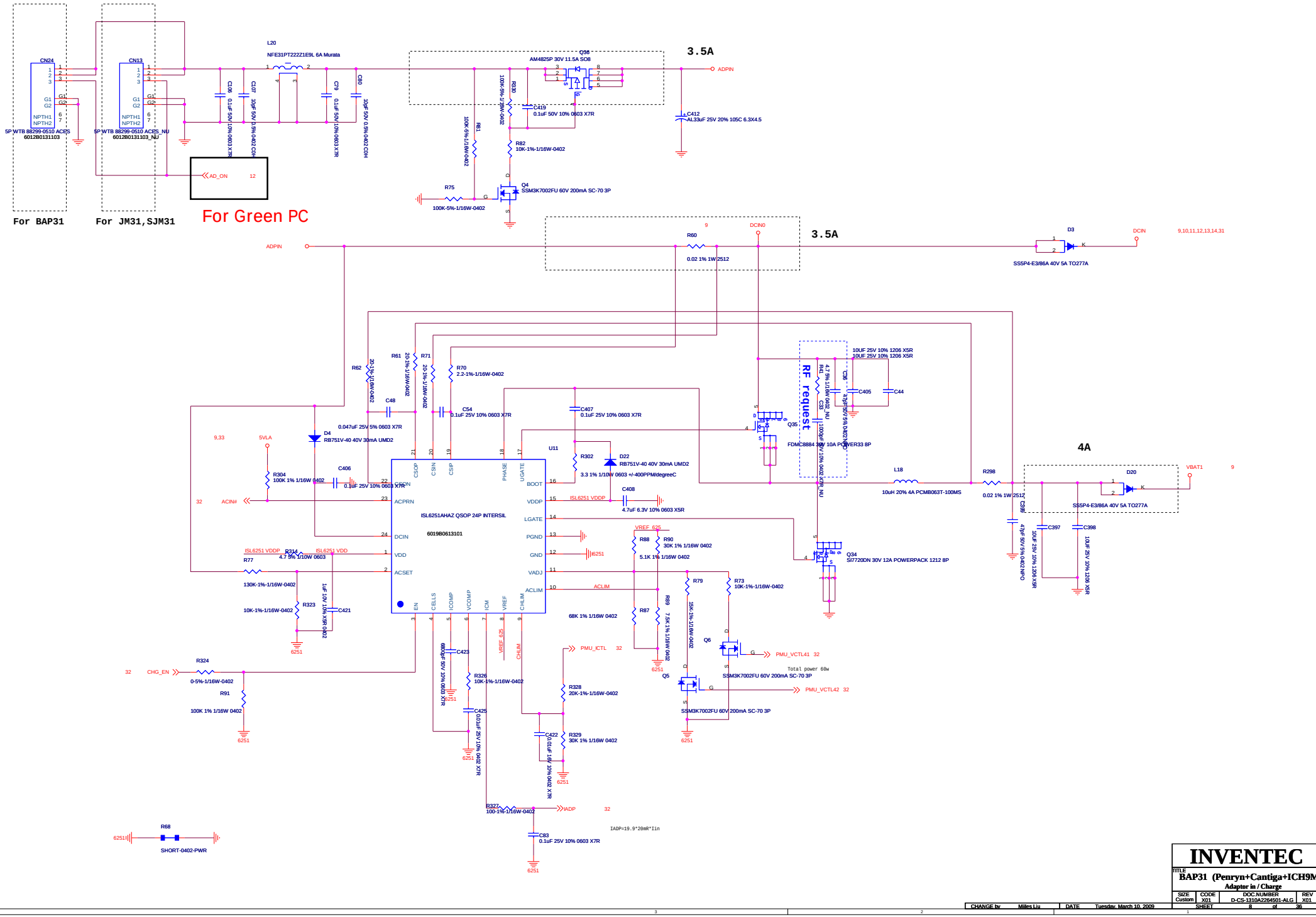
INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
Power Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	X01	D-CS-1310A2264501-ALG	X01

SHEET

CHANGE by: Miles Liu | DATE: Tuesday, March 10, 2009


For BAP31
For JM31,SJM31
For Green PC
3.5A
4A
RF request
ISL6251AHAZ QSOP 24P INTERSIL
6019B0613101
FDMC8884 30V 10A POWER33 8P
SSM3K7002FU 60V 200mA SC-70 3P
SS5P4-E3/86A 40V 5A TO277A
AM4825P 30V 11.5A SO8
SI7720DN 30V 12A POWERPACK 1212 8P
SHORT-0402-PWR
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
Adaptor in / Charge
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009
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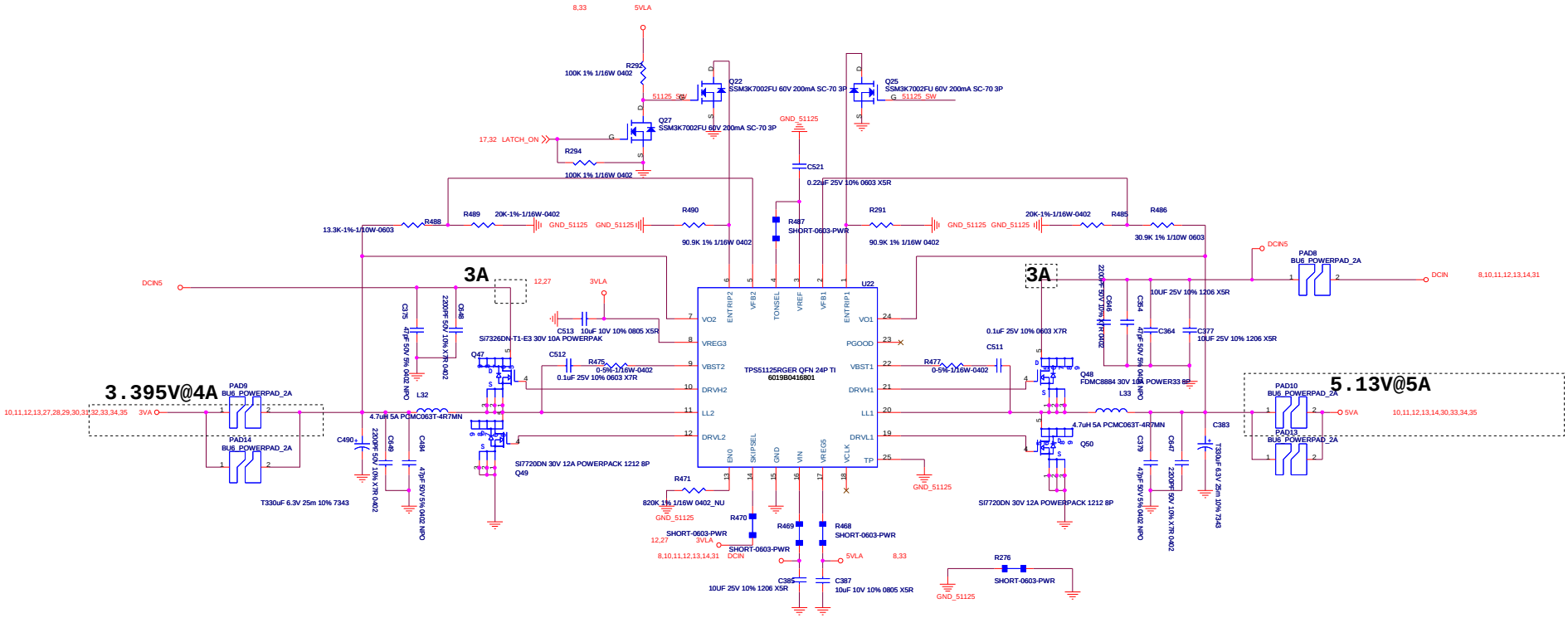
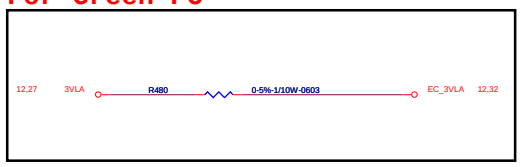
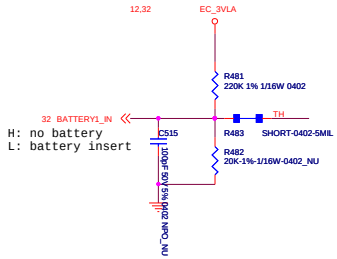
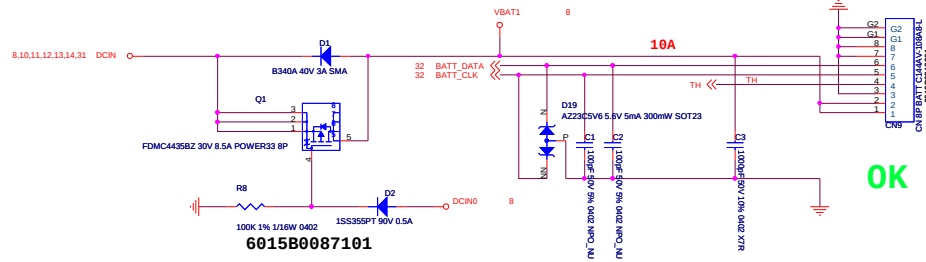


For Green PC





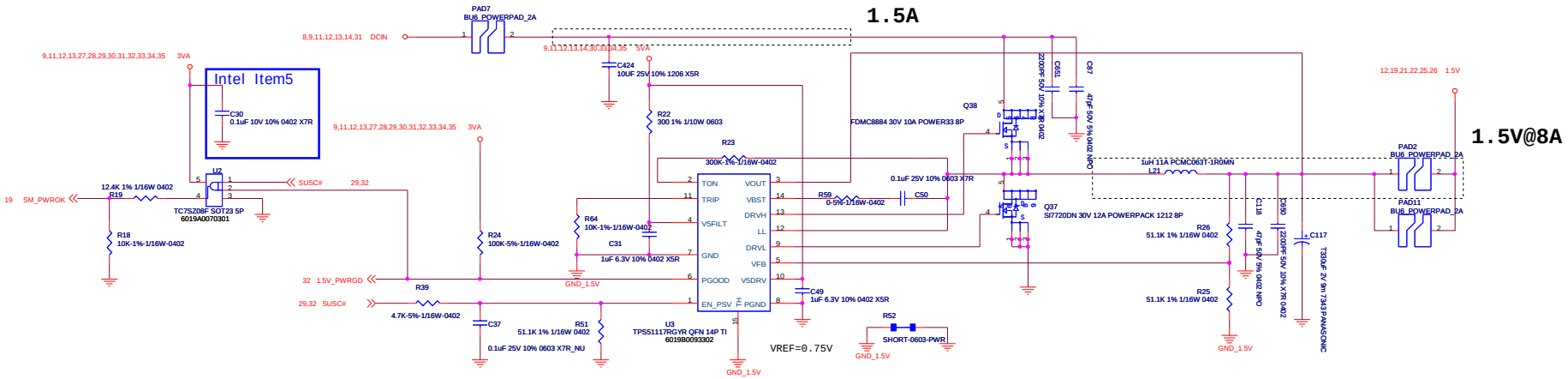


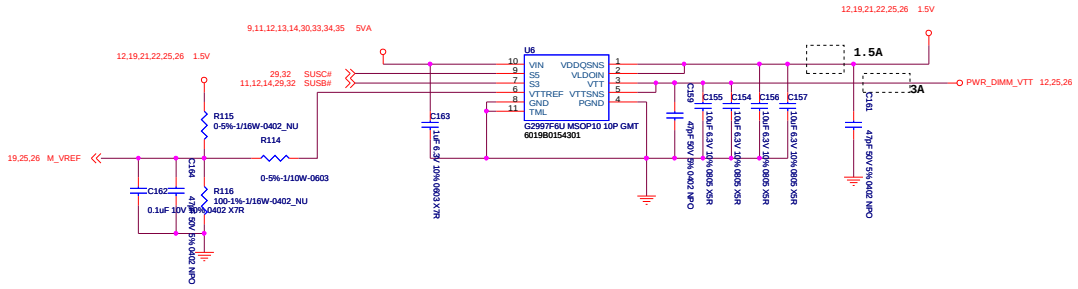
INVENTEC

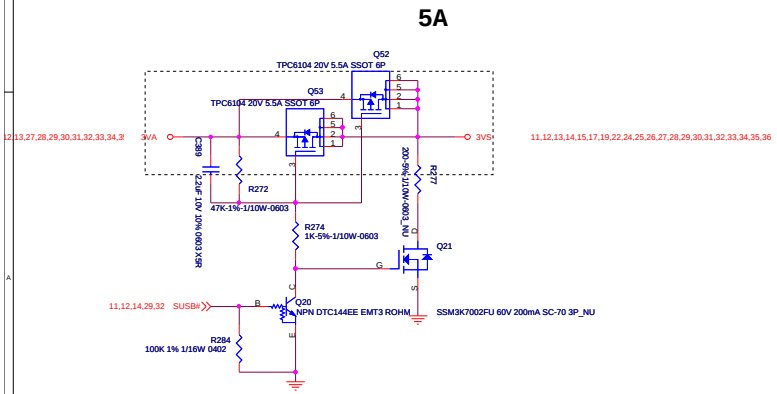
TITLE: BAP31 (Penryn+Cantiga+ICH9M)SF
5VLA/5VA/3VLA/3VA

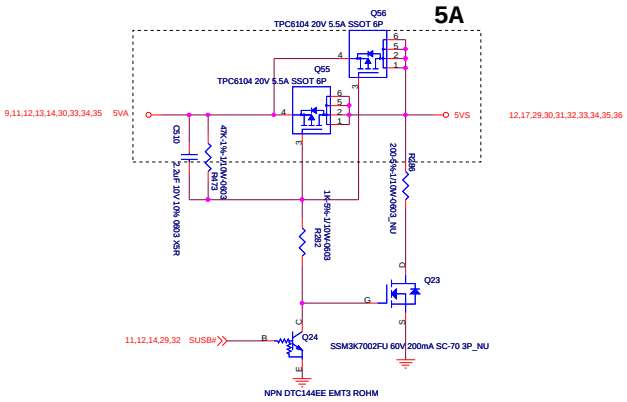
SIZE: Custom

CHANGE by: Miles Liu | DATE: Tuesday, March 10, 2009









CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009		

INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SF
3VS/5VS/1.5V (DDR3)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01
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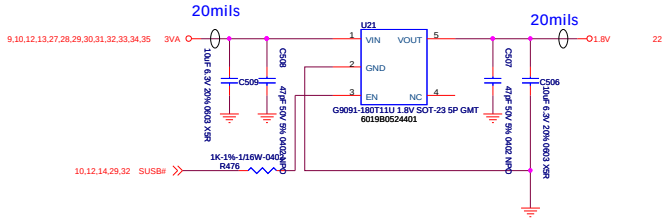
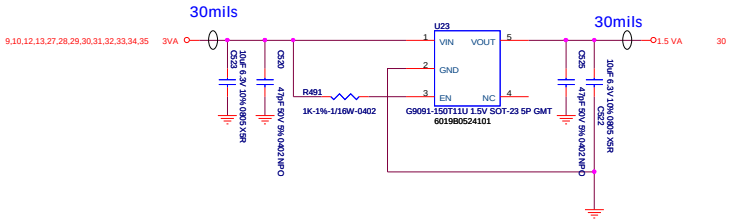
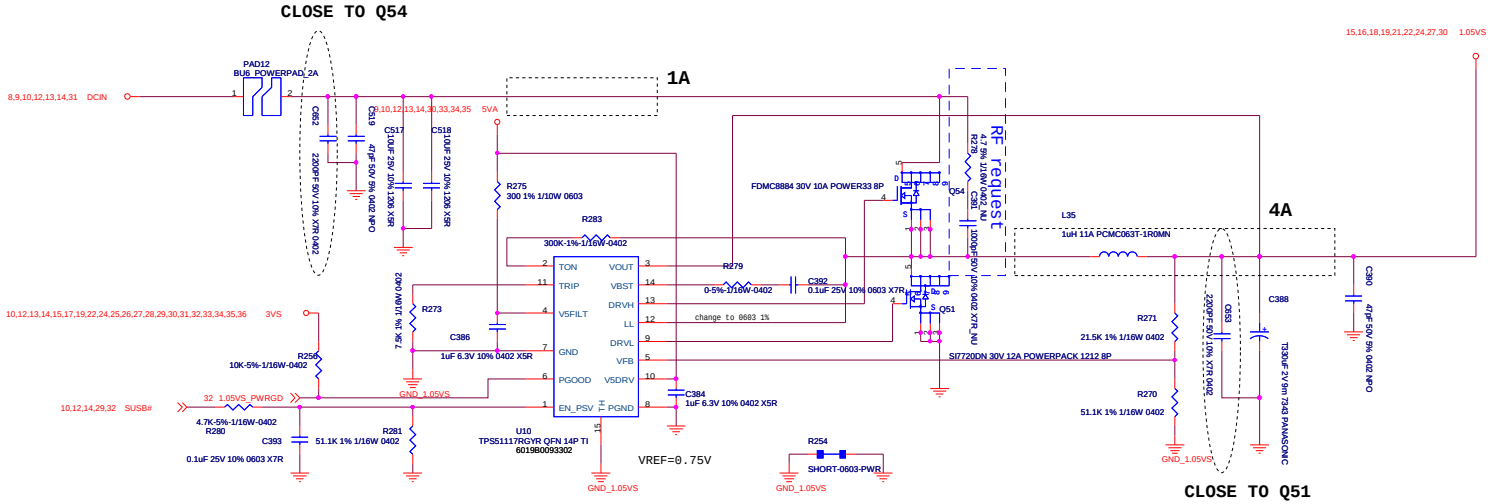






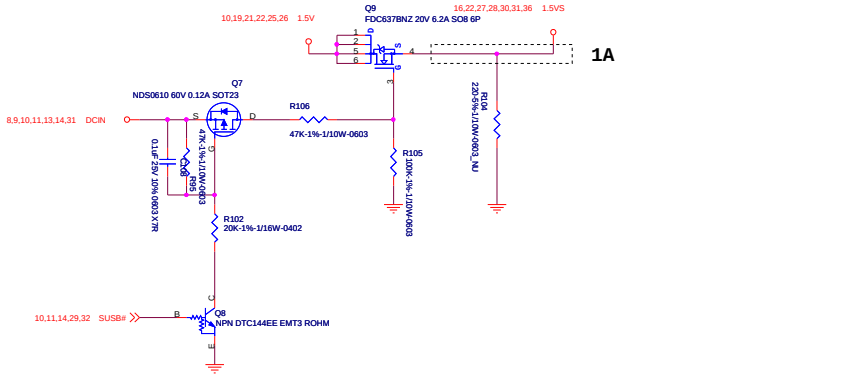
INVENTEC

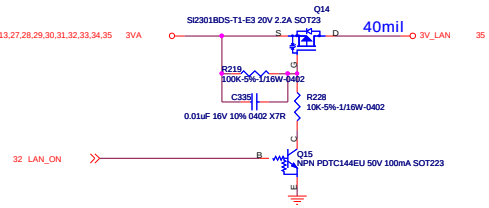
TITLE: BAP31 (Penryn+Cantiga+ICH9M)SF
1.05VS/1.5S/1.8V/1.5VA

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

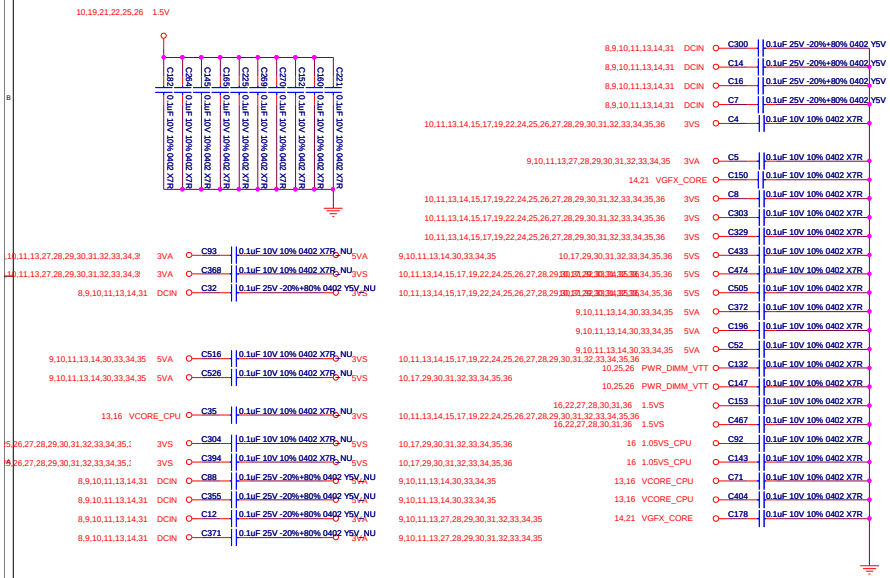
CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

1.5VS

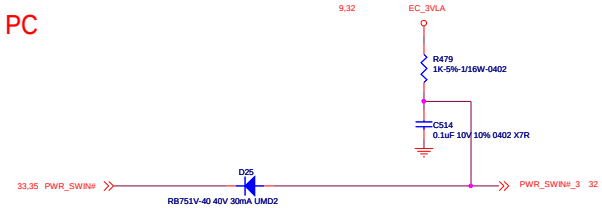




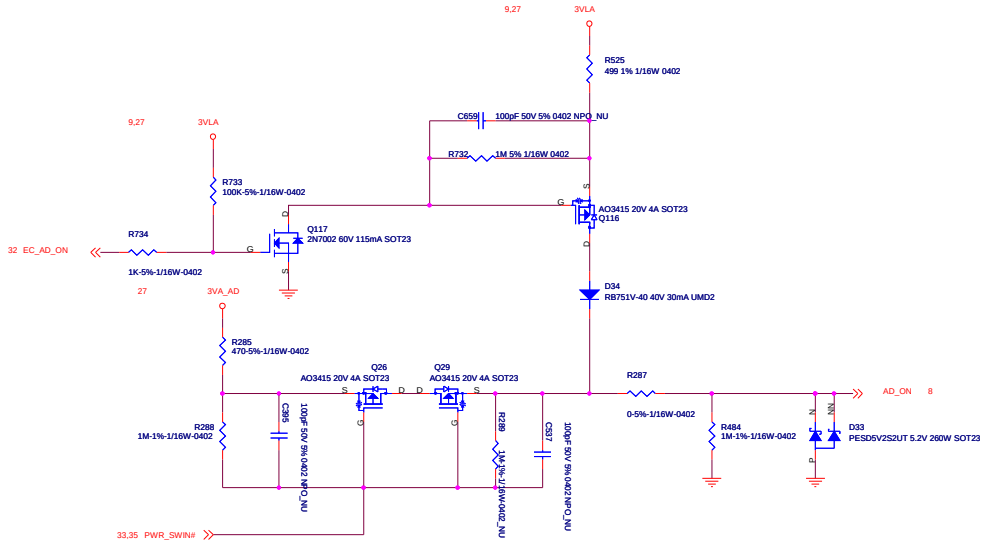
EMI Cap

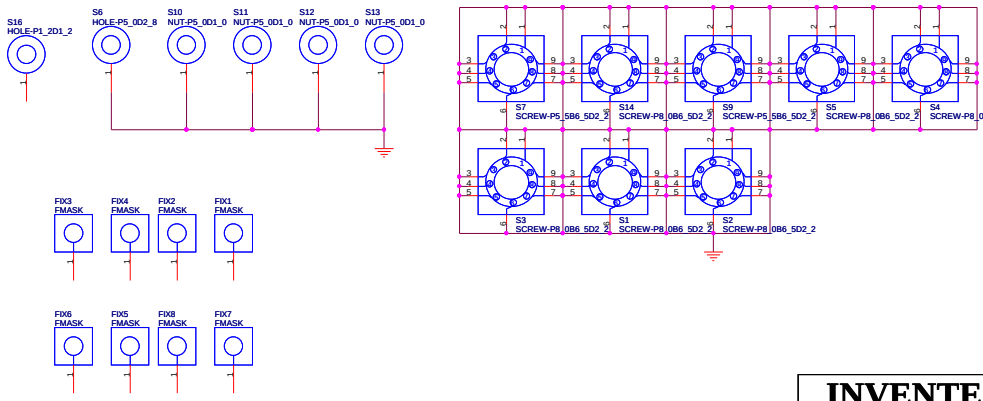


For Green PC



None Green PC ---- NU



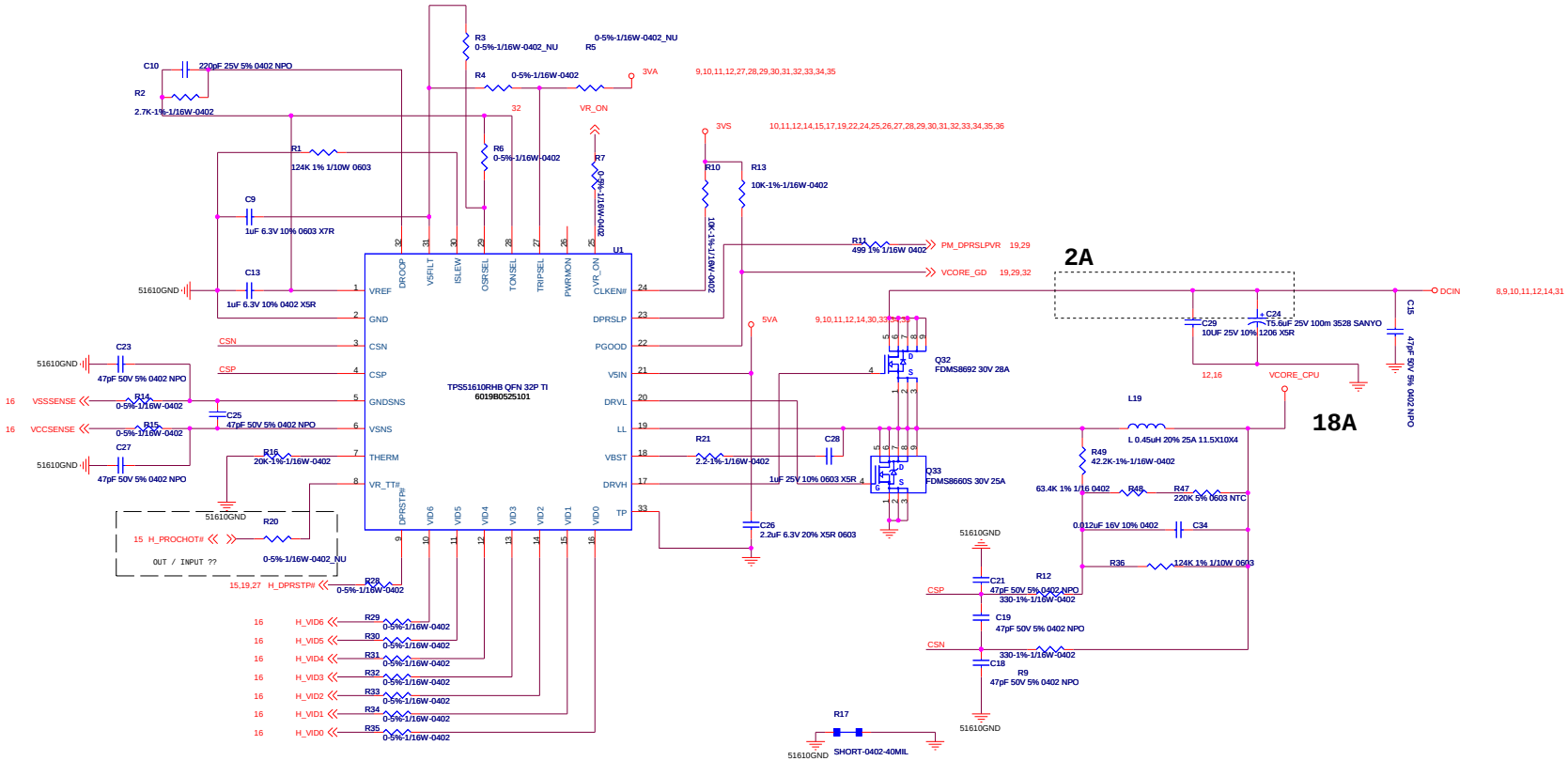


INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SF
Power on latch

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by: Miles Liu | DATE: Tuesday, March 10, 2009 | SHEET: 12 of 36

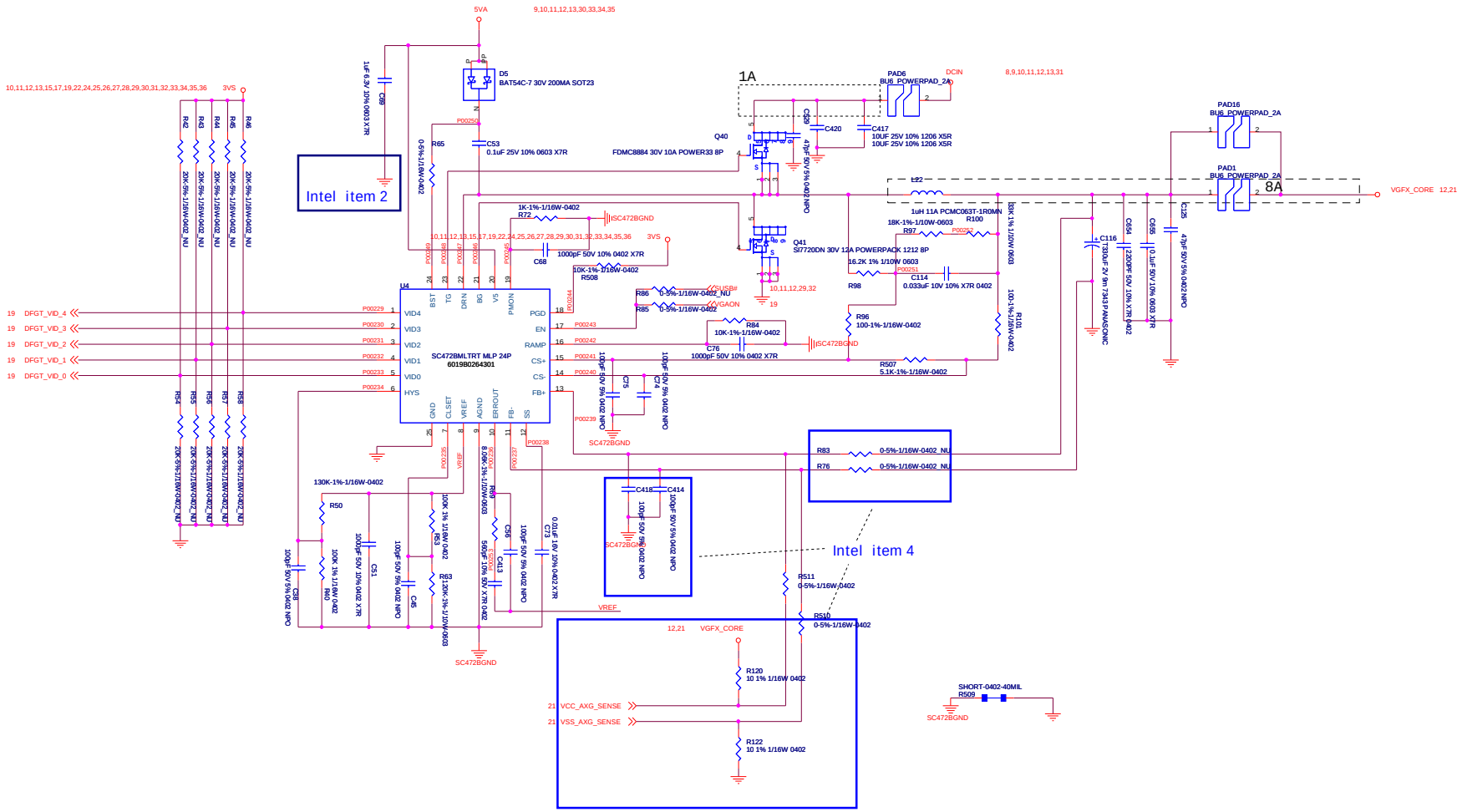


INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
CPU Core Power

SIZE	CODE	DOC.NUMBER
C	X01	D-CS-1310A2264501-ALG

CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009	SHEET	13	of



CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

INVENTEC

TITLE: **BAP31 (Penryn+Cantiga+ICH9M)SFF**
GPU CORE

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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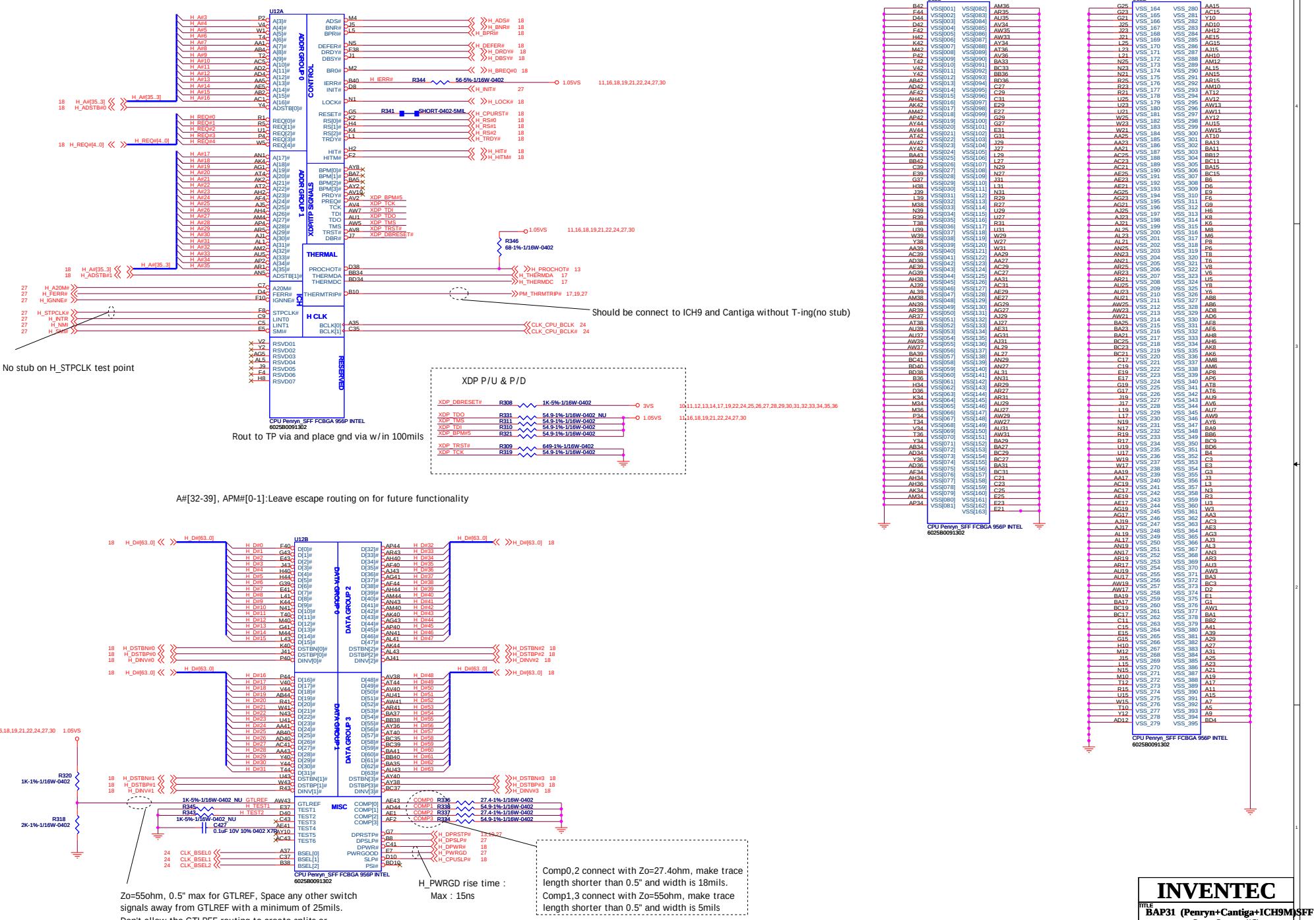
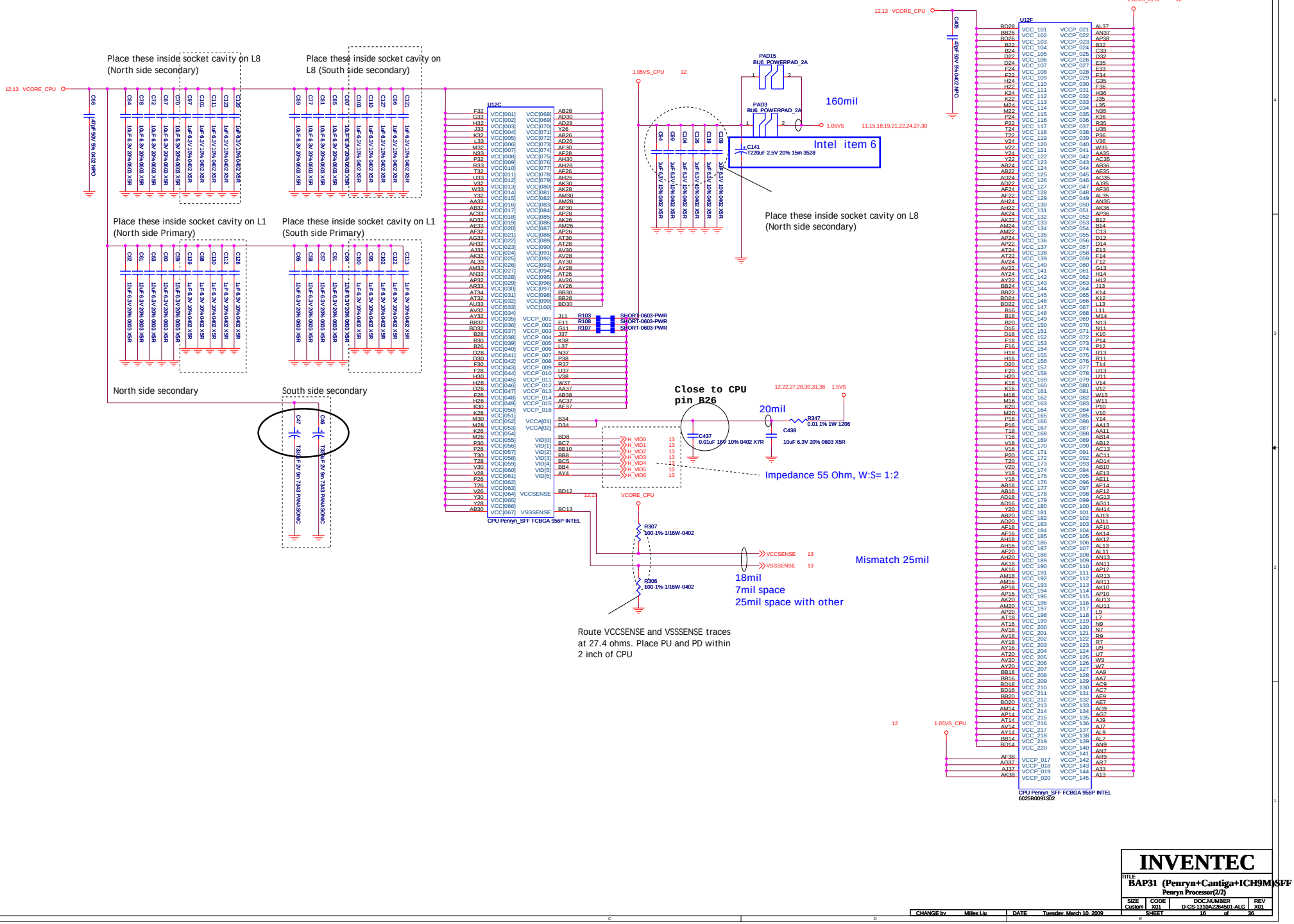

U12A
ADDR GROUP 0
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
CPU Penryn_SFF FCBGA 956P INTEL
6025B0091302
No stub on H_STPCLK test point
Rout to TP via and place gnd via w/in 100mils
Should be connect to ICH9 and Cantiga without T-ing(no stub)
XDP P/U & P/D
A#[32-39], APM#[0-1]:Leave escape routing on for future functionality
U12B
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
MISC
Zo=55ohm, 0.5" max for GTLREF, Space any other switch signals away from GTLREF with a minimum of 25mils.
Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals
H_PWRGD rise time : Max : 15ns
Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5" and width is 18mils.
Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5" and width is 5mils
U12D
U12E
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
Penryn Processor(1/2)
SIZE Custom
CODE X01
DOC.NUMBER D-CS-1310A2264501-ALG
REV X01
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009
SHEET


Place these inside socket cavity on L8 (North side secondary)
Place these inside socket cavity on L8 (South side secondary)
Place these inside socket cavity on L1 (North side Primary)
Place these inside socket cavity on L1 (South side Primary)
North side secondary
South side secondary
12,13 VCORE_CPU
1.05VS_CPU 12
U12C
CPU Penryn_SFF FCBGA 956P INTEL
U12F
CPU Penryn_SFF FCBGA 956P INTEL
6025B0091302
PAD15 BU6_POWERPAD_2A
PAD3 BU6_POWERPAD_2A
160mil
Intel item 6
C141 T220uF 2.5V 20% 15m 3528
1.05VS
11,15,18,19,21,22,24,27,30
Place these inside socket cavity on L8 (North side secondary)
SHORT-0603-PWR
Close to CPU pin B26
20mil
R347 0.01 1% 1W 1206
C437 0.01uF 16V 10% 0402 X7R
C438 10uF 6.3V 20% 0603 X5R
12,22,27,28,30,31,36 1.5VS
Impedance 55 Ohm, W:S= 1:2
VCORE_CPU
R307 100-1%-1/16W-0402
R306 100-1%-1/16W-0402
VCCSENSE 13
VSSSENSE 13
Mismatch 25mil
18mil
7mil space
25mil space with other
Route VCCSENSE and VSSSENSE traces at 27.4 ohms. Place PU and PD within 2 inch of CPU
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
Penryn Processor(2/2)
SIZE Custom
CODE X01
DOC.NUMBER D-CS-1310A2264501-ALG
REV X01
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009
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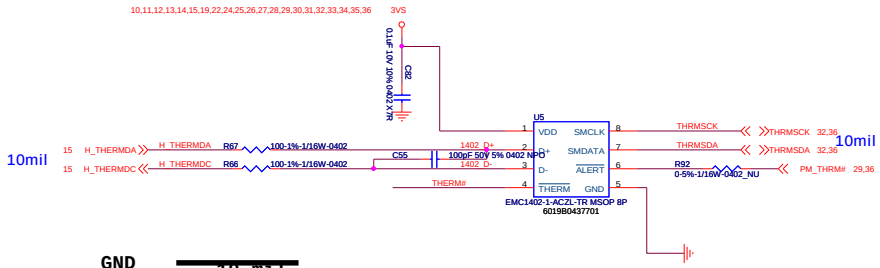
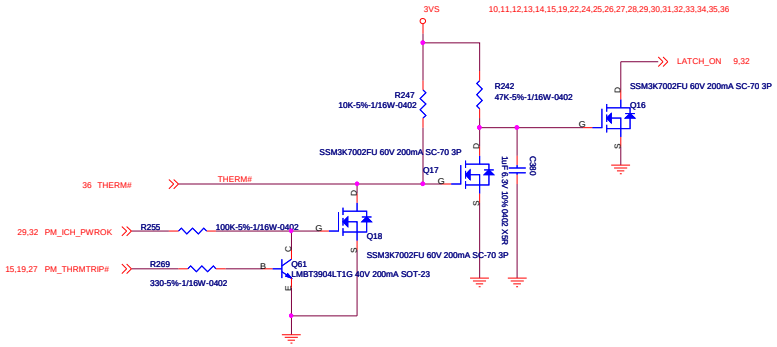
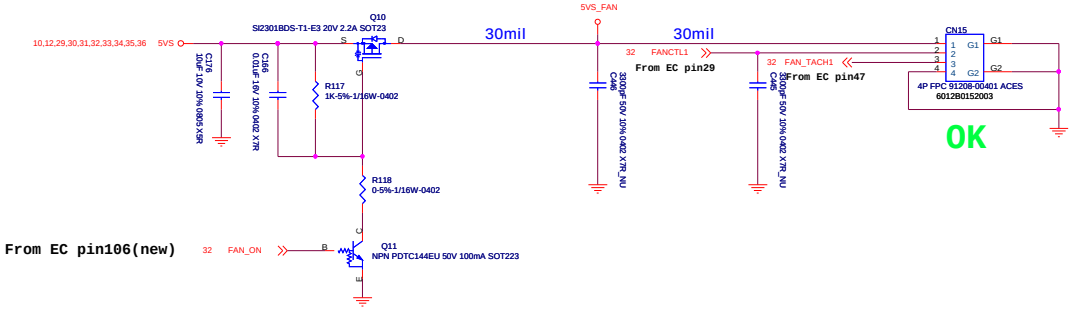
THERMAL SENSOR

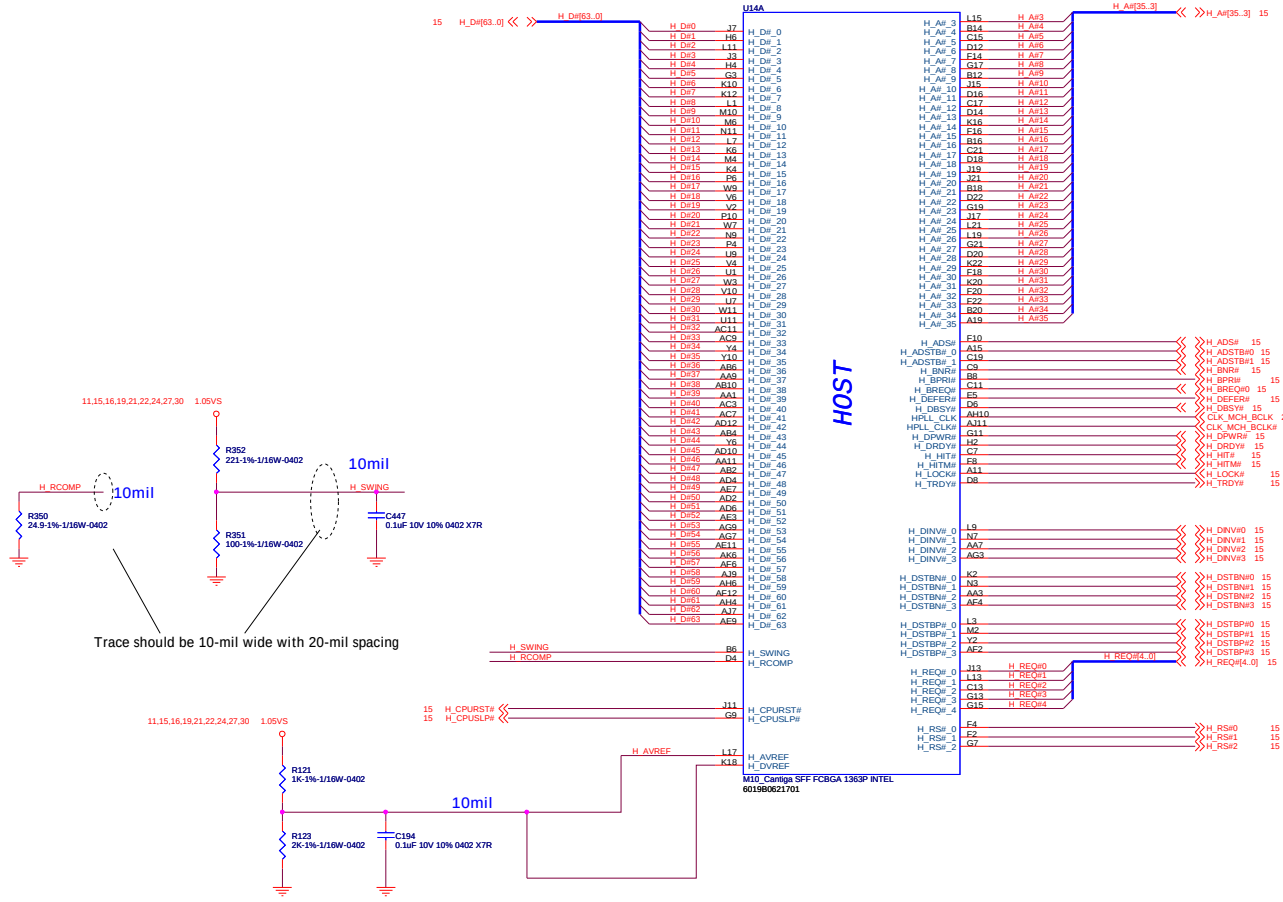




Fan control



INVENTEC			
TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF CPU Thermal			
SIZE: Custom	CODE: X01	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: X01
CHANGE by: Miles Liu	DATE: Tuesday, March 10, 2009	SHEET	



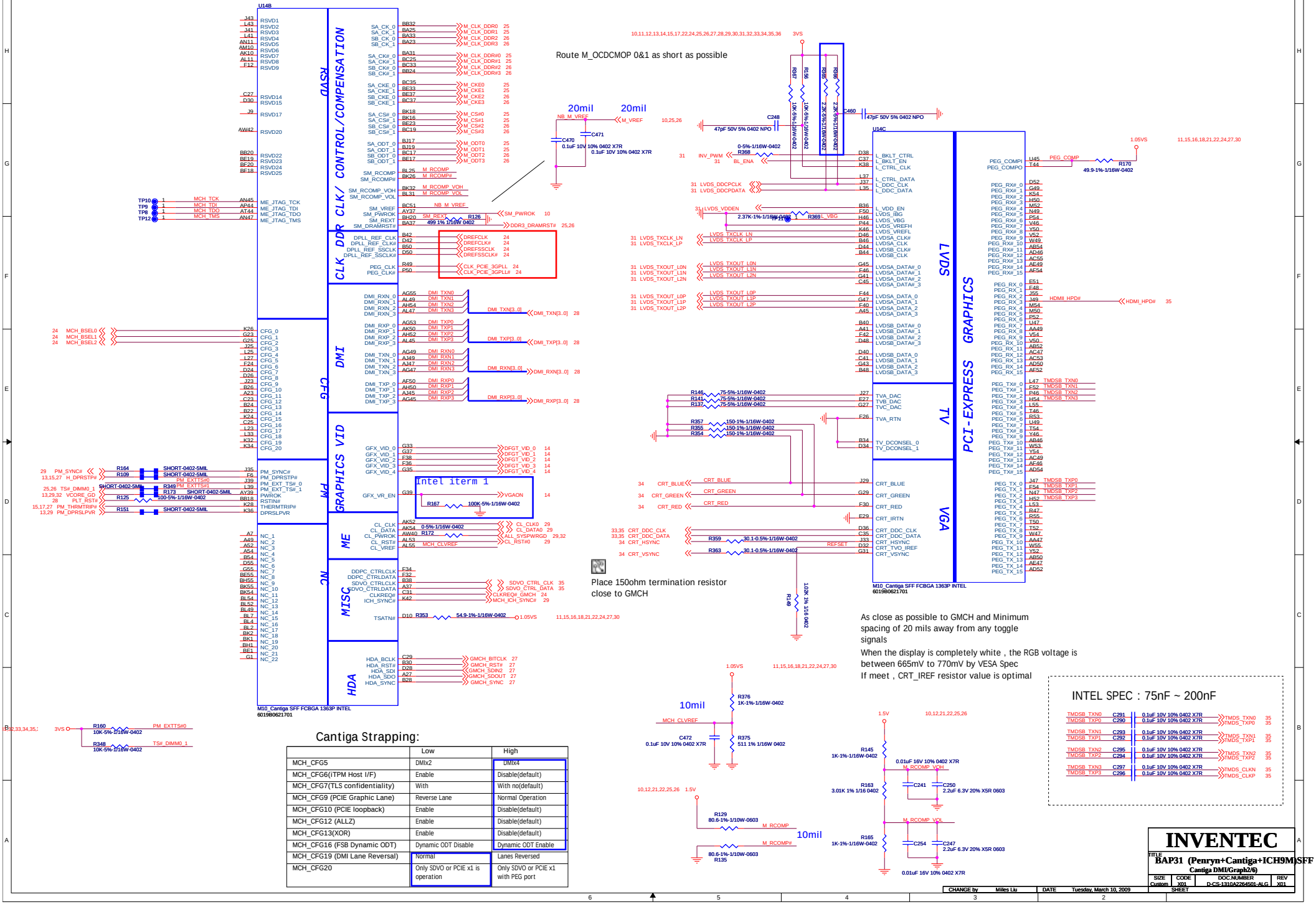
CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga Host(1/6)

SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

SHEET 18 of 36



Cantiga Strapping:

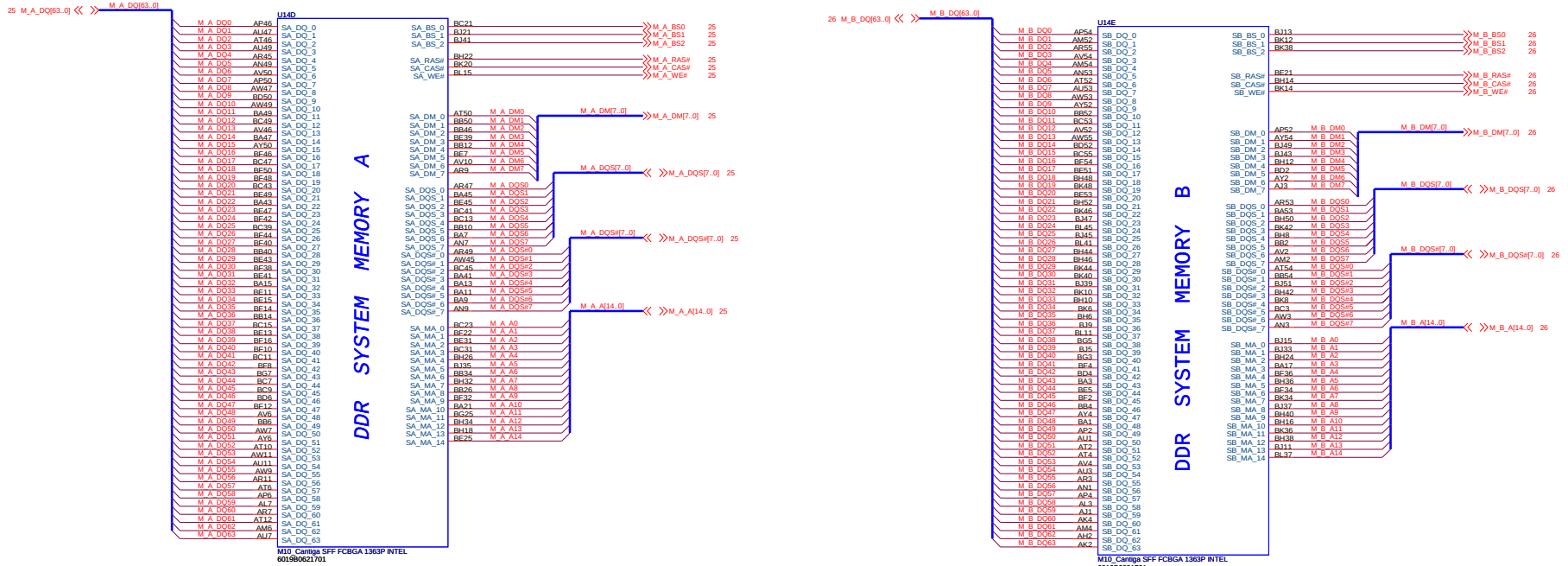
	Low	High
MCH_CFG5	DMIx2	DMIx4
MCH_CFG6(iTPM Host I/F)	Enable	Disable(default)
MCH_CFG7(TLS confidentiality)	With	With no(default)
MCH_CFG9 (PCIE Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIE loopback)	Enable	Disable(default)
MCH_CFG12 (ALLZ)	Enable	Disable(default)
MCH_CFG13(XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only SDVO or PCIE x1 is operation	Only SDVO or PCIE x1 with PEG port

CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

INVENTEC

TITLE: **BAP31 (Penryn+Cantiga+ICH9M)SFF**
Cantiga DMI/Graph2/6)

SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01
		SHEET	

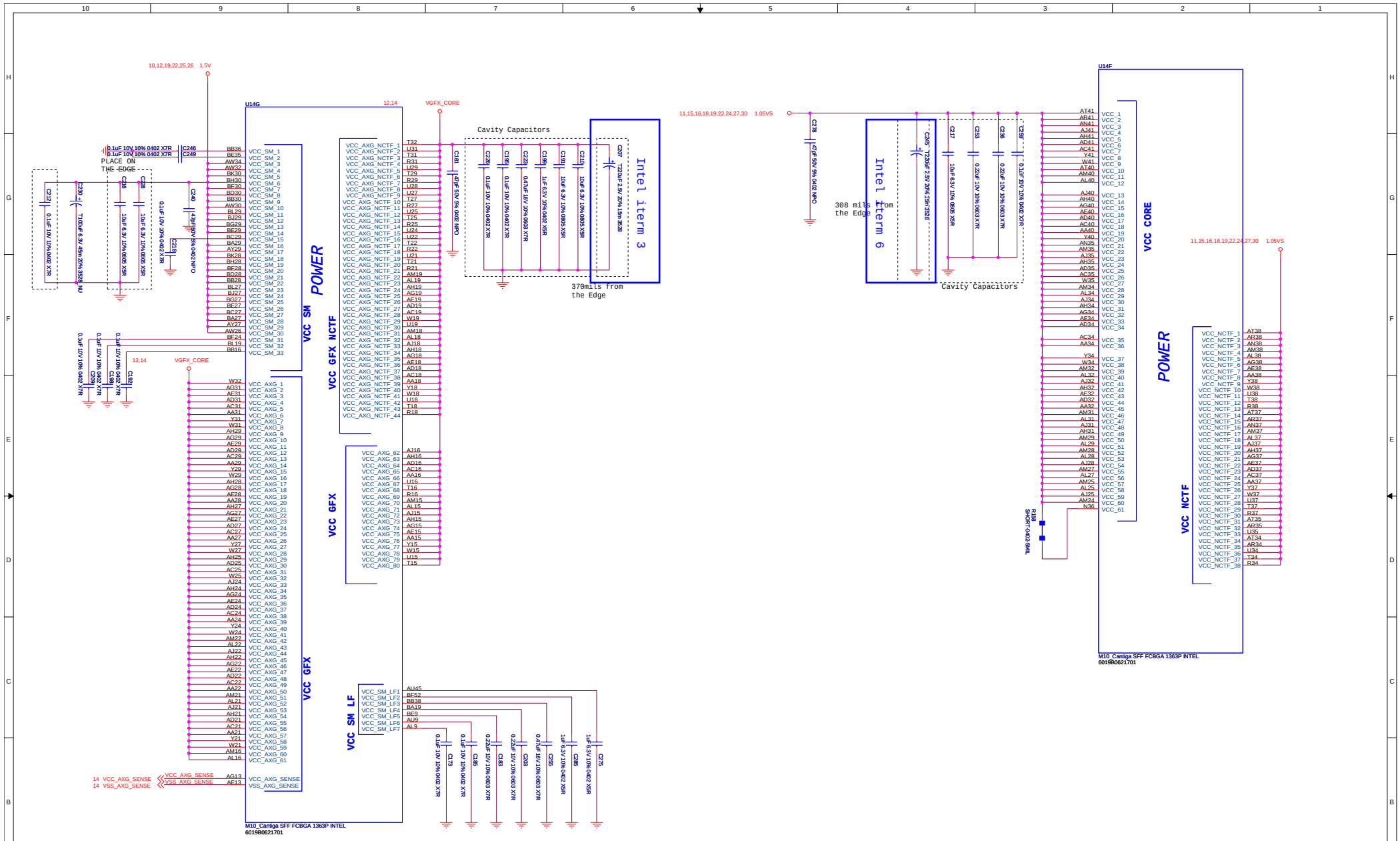


INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga DDR3(3/6)

SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A226450L-ALG	X01

CHANGE by: Miles Liu | DATE: Tuesday, March 10, 2009 | SHEET 20 of 36


VCC SM POWER
VCC GFX NCTF
VCC GFX
VCC SM LF
VCC CORE POWER
VCC NCTF
Cavity Capacitors
370mils from the Edge
308 mils from the Edge
Intel iterm 3
Intel iterm 6
PLACE ON THE EDGE
U14G
U14F
M10_Cantiga SFF FCBGA 1363P INTEL
6019B0621701
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga Power(4/6)
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009
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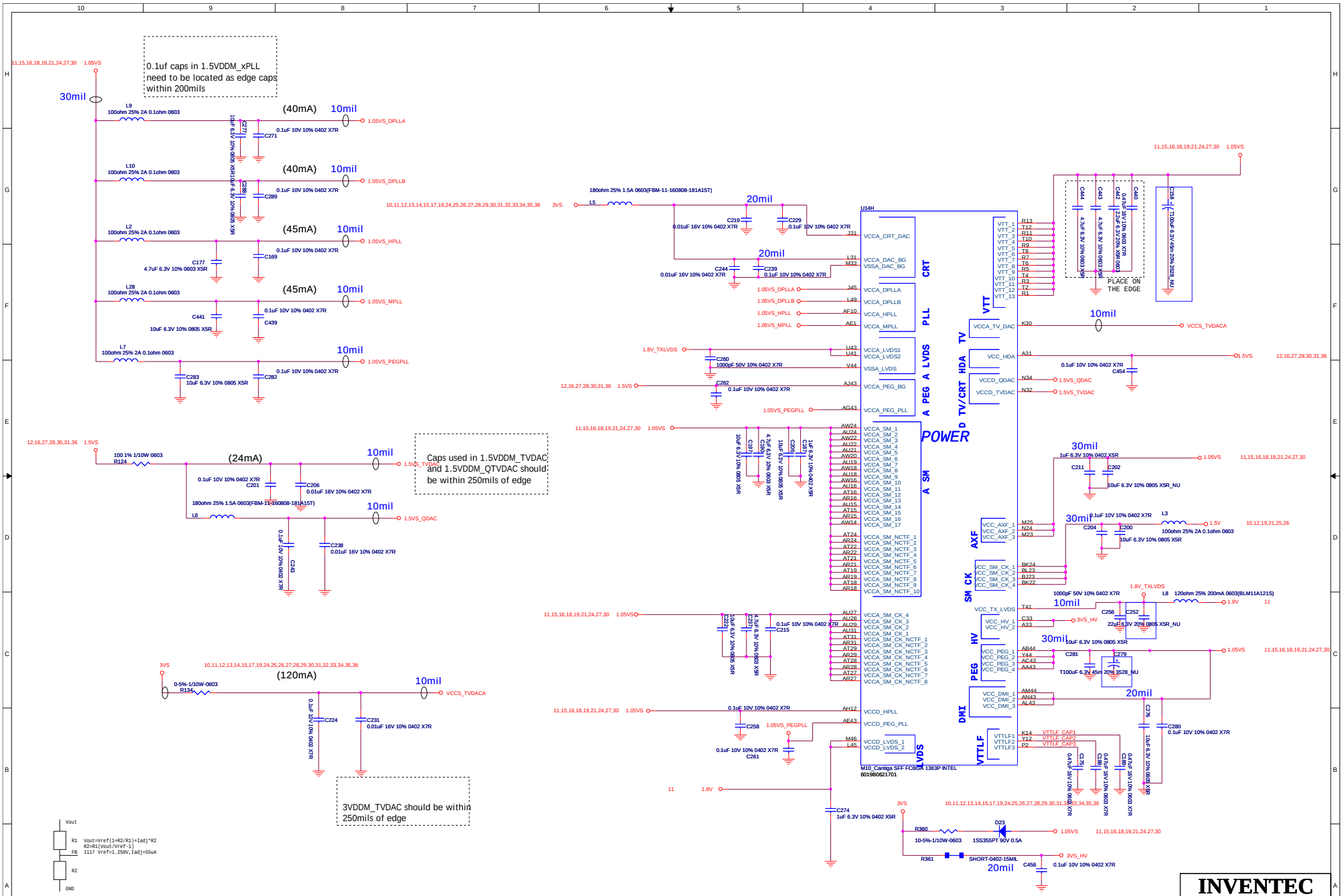
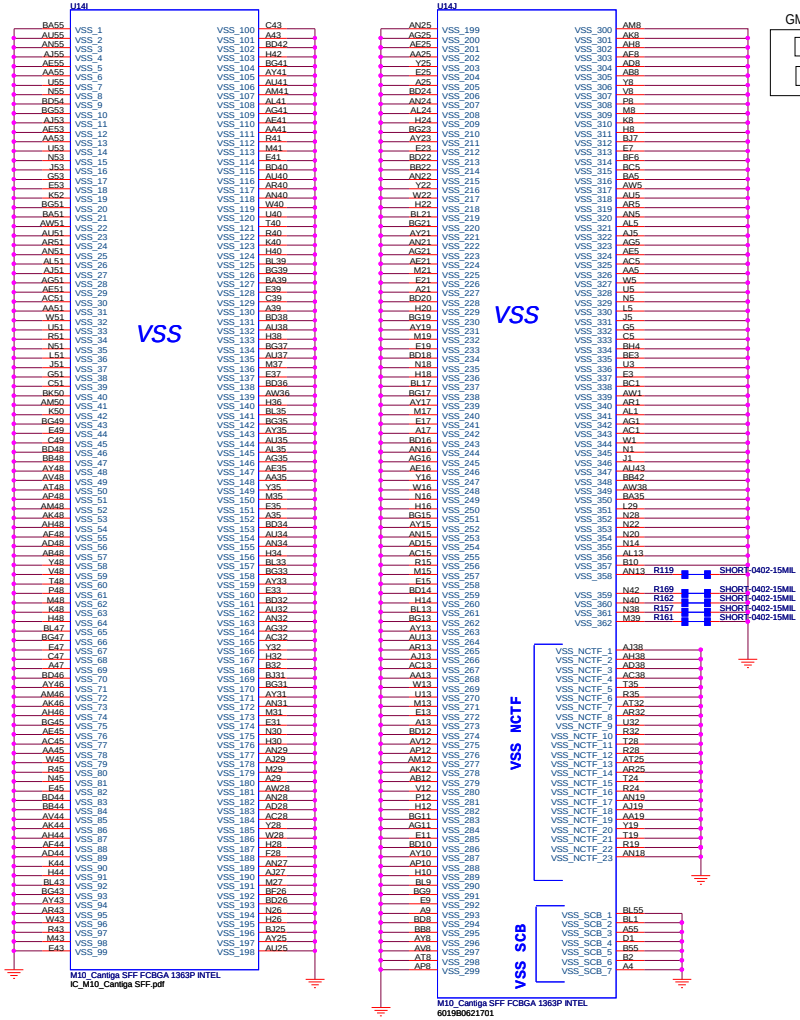
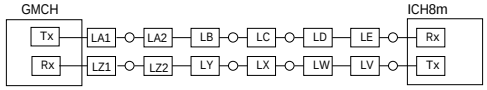

0.1uf caps in 1.5VDDM_xPLL need to be located as edge caps within 200mils
Caps used in 1.5VDDM_TVDAC and 1.5VDDM_QTVDAC should be within 250mils of edge
3VDDM_TVDAC should be within 250mils of edge
PLACE ON THE EDGE
POWER
CRT
PLL
LVDS
PEG
TV/CRT
HDA
TV
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
VDS
M10_Cantiga SFF FCBGA 1363P INTEL
6019B0621701
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga Power(5/6)
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009

DMI Routing Guideline

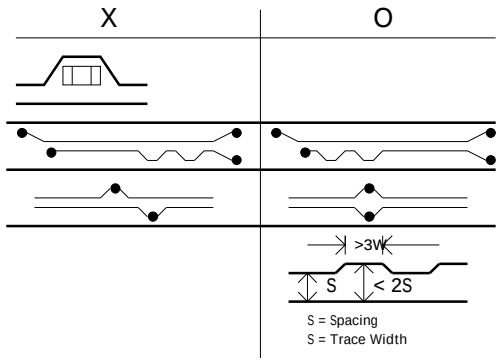




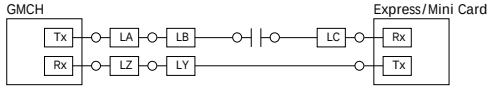
Breakout/in LA/LZ	Main Route LB/LY		Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Didderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



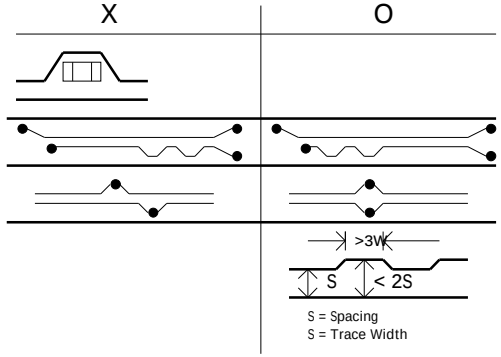
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga Ground(6/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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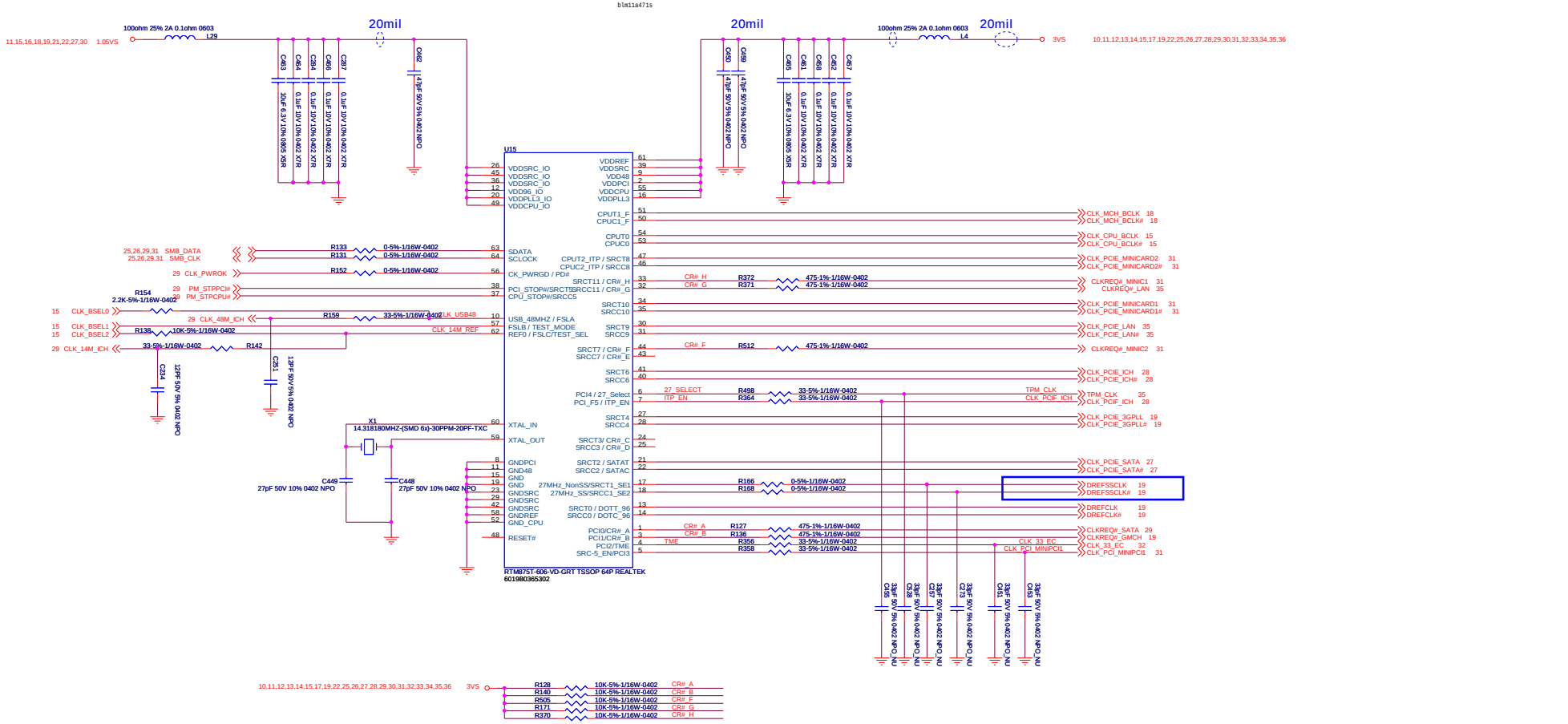
CHANGE by: Miles Liu | DATE: Tuesday, March 10, 2009



FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY	
1	1	0	667	166	
0	1	0	800	200	
0	0	0	1067	266	*

CR#_A:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2=0--->SRC0 bit 2=1--->SRC2	BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

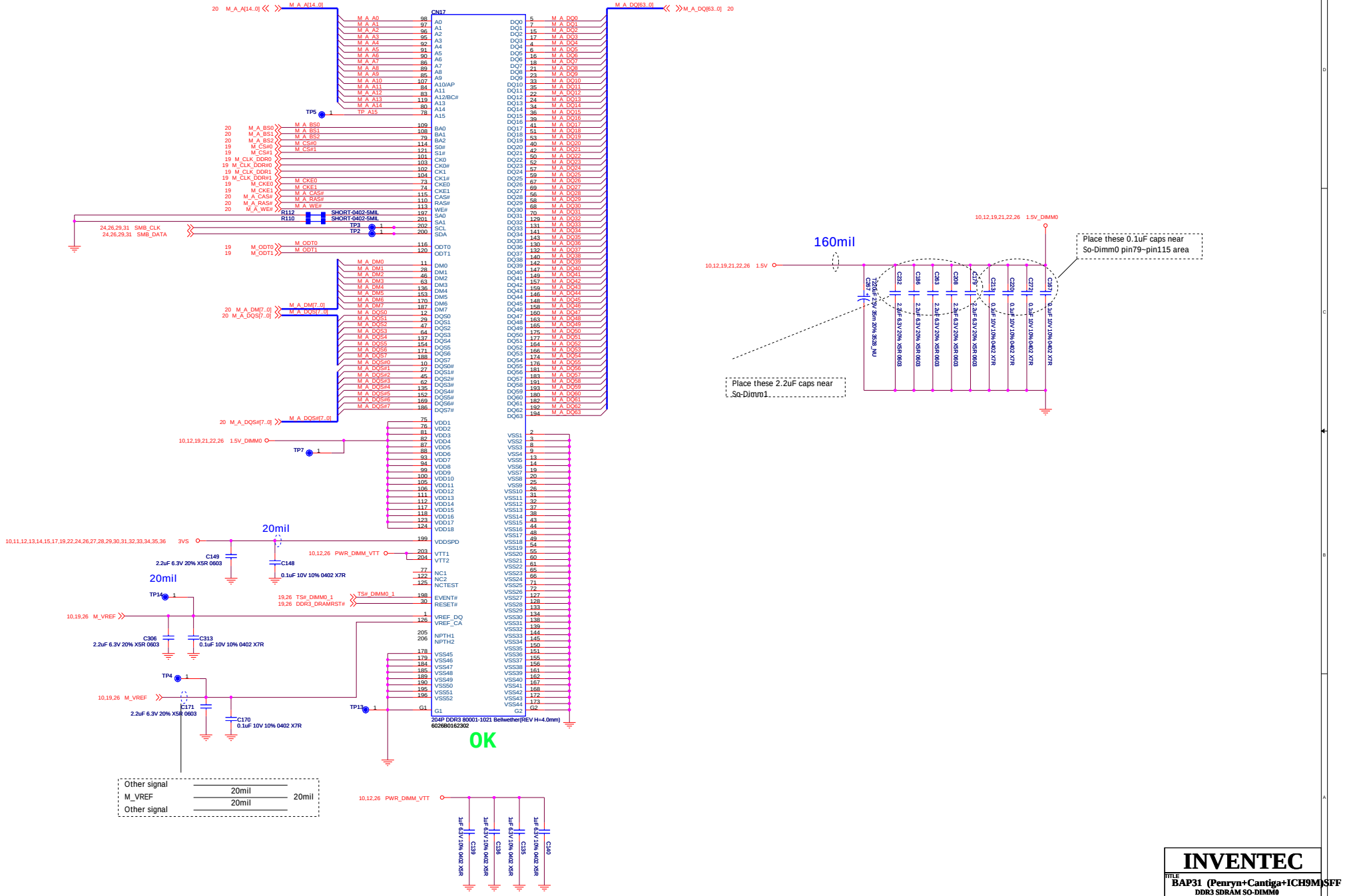
INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
Clock Generator

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by: Miles Liu | DATE: Tuesday, March 10, 2009 | SHEET: 24 of 36

SO-DIMM0



CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

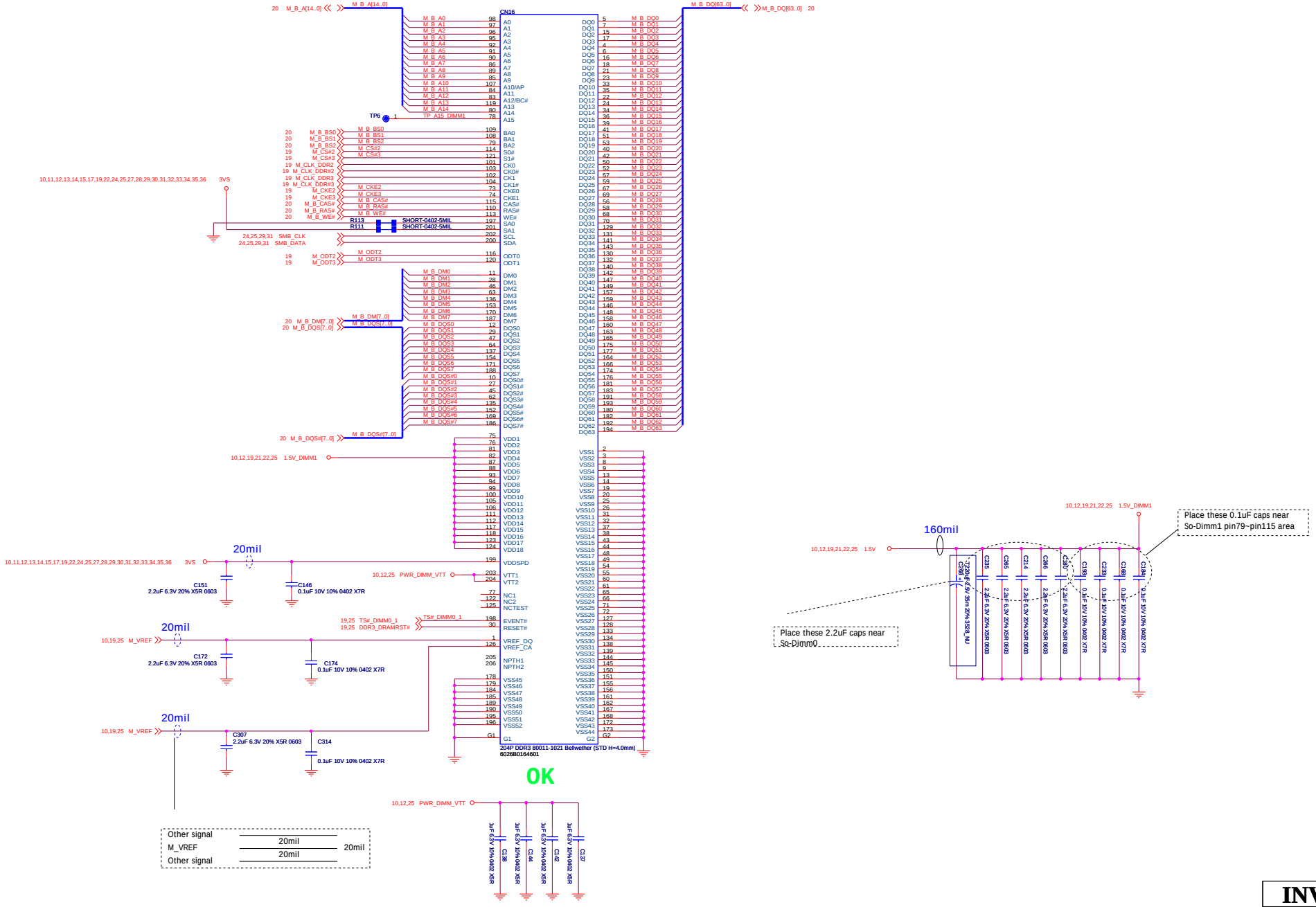
INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
DDR3 SDRAM SO-DIMM0

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

SHEET

SO-DIMM1



CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

INVENTEC

TITLE: **BAP31 (Penryn+Cantiga+ICH9M)SFF**
DDR3 SDRAM SO-DIMM1

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

SHEET 26 of 36

RTC Circuit

1. RC delay time should be in the range of 18~25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended

D12 RB751V-40 40V 30mA UMD2

R231 0-5%-1/10W-0603

R226 665-1%-1/10W-0603

R217 200-1%-1/16W-0402

20mil

CN25 2P WTB 85204-0200N ACES_NU 6012B0030108_NU

CN18 CN 2P WTB 85482-0271 ACES 6012B0130701

For JM31,SJM31 For BAP31

For Green PC

BATT1

123

CABLE,ROUND,3POS,75mm,I,RTC_NU

6027B0066801

RTC Battery Life :

220mAh(220000uAh) / 6uA = 4.2 year

R221 20K-5%-1/16W-0402

C339 1uF 6.3V 10% 0402 X5R

C336 1uF 6.3V 10% 0402 X5R

R220 20K-5%-1/16W-0402

C338 1uF 6.3V 10% 0402 X5R

R198 1M-5%-1/16W-0402

INTRUDER#

R382 10M-5%-1/16W-0402

X2

C478 15pF 5% 50V 0402

C477 15pF 5% 50V 0402

32.768KHZ 10ppm 12.5pF(8.4X3.7X2.5)

Place all series resistors 0.6 to 2.6 inches from the ICH9

Distance between the ICH9-M and cap on the "P" signal should be identical distance between the ICH9-M and cap on the "N" signal for same pair.

Needs to be placed within 2" of ICH9m

Must be placed within 2" of 24.9 ohm w/o stub

Placed within 500mils of ICH9m ball

R418 24.9-1%-1/16W-0402

Short pins AG1 and AG2 at the package

ICH8m internal VR enable strap

	Enable	Disable
INTVRMEN	1(Default)	0

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05

R176 332K-1%-1/10W-0603

ACZ_SDATAOUT strap functionality base on RSVD9 strap

XOR chain entrance (RSVD9 pulled low)

PCIE port config bit 1(RSVD9 not pulled low)

R240 1K-5%-1/16W-0402_NU

R401 1K-5%-1/16W-0402_NU

Stuff for XOR chain testing

XOR Chain Entrance Strap - to be updated		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

C495 5pF 50V 0.25% 0402 C0G_NU

By Tony

R454 8.2K-5%-1/16W-0402

R453 10K-5%-1/16W-0402

R451 10K-5%-1/16W-0402

R452 10K-5%-1/16W-0402

INVENTEC

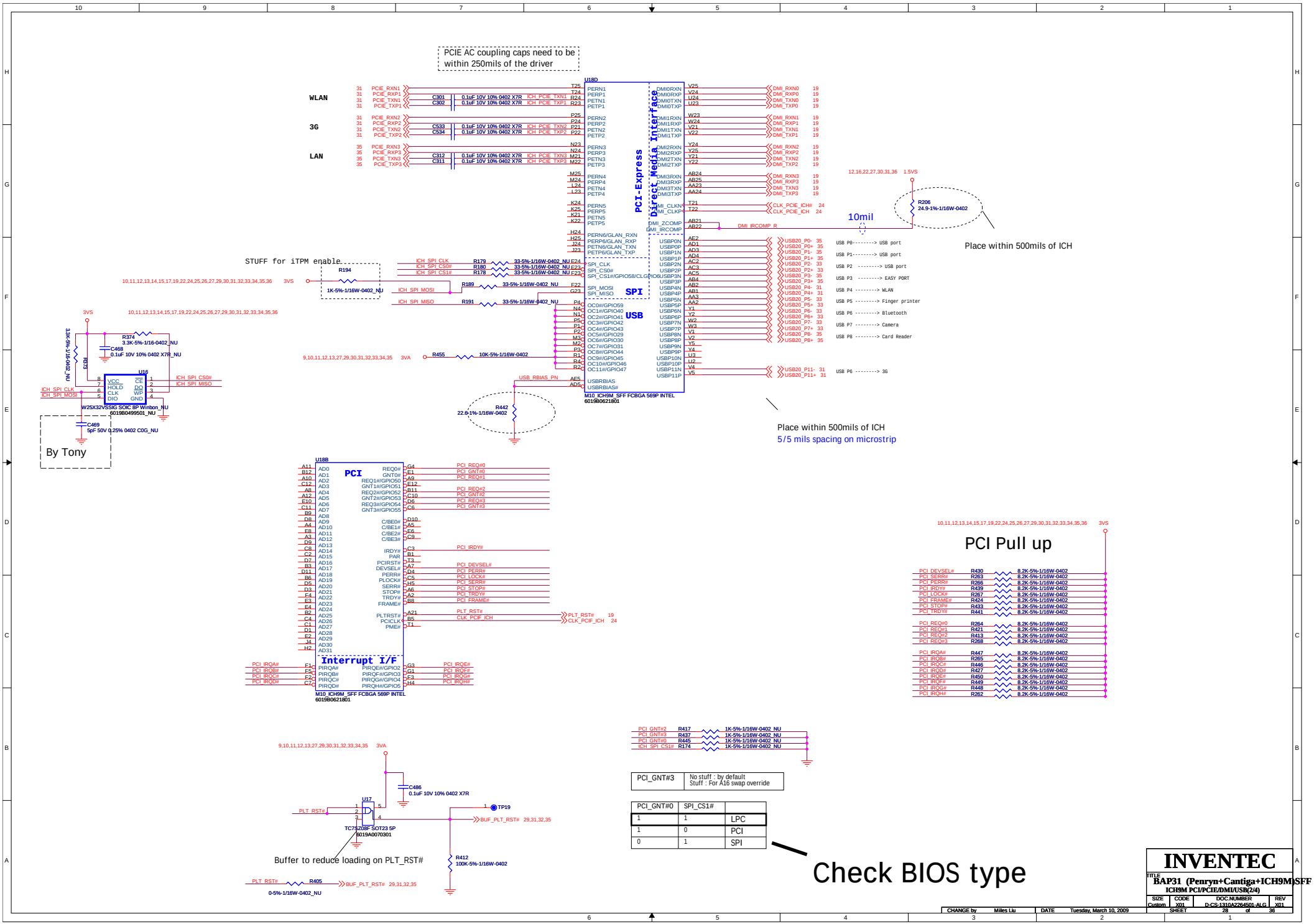
TITLE: BAP31 (Penryn+Cantiga+ICH9M SFF)

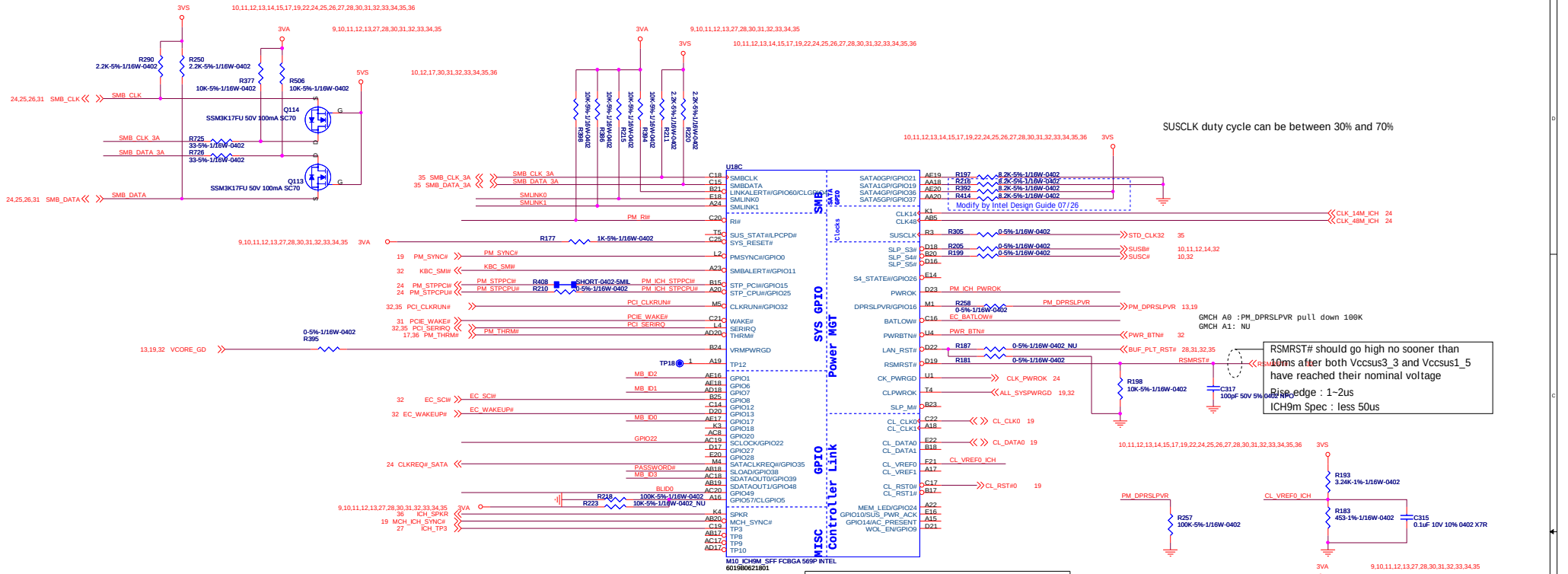
ICH9M CPU/IDE/SATA(1/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

SHEET

CHANGE by: Miles Liu DATE: Tuesday, March 10, 2009


PCIE AC coupling caps need to be within 250mils of the driver
WLAN
3G
LAN
PCIE_RXN1
PCIE_RXP1
PCIE_TXN1
PCIE_TXP1
PCIE_RXN2
PCIE_RXP2
PCIE_TXN2
PCIE_TXP2
PCIE_RXN3
PCIE_RXP3
PCIE_TXN3
PCIE_TXP3
C301 0.1uF 10V 10% 0402 X7R ICH_PCIE_TXN1
C302 0.1uF 10V 10% 0402 X7R ICH_PCIE_TXP1
C533 0.1uF 10V 10% 0402 X7R ICH_PCIE_TXN2
C534 0.1uF 10V 10% 0402 X7R ICH_PCIE_TXP2
C312 0.1uF 10V 10% 0402 X7R ICH_PCIE_TXN3
C311 0.1uF 10V 10% 0402 X7R ICH_PCIE_TXP3
U18D
PCI-Express
Direct Media Interface
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
DMI_IRCOMP_R
R206 24.9-1%-1/16W-0402
10mil
Place within 500mils of ICH
STUFF for iTPM enable
R194 1K-5%-1/16W-0402_NU
ICH_SPI_CLK R179 33-5%-1/16W-0402_NU
ICH_SPI_CS0# R180 33-5%-1/16W-0402_NU
ICH_SPI_CS1# R178 33-5%-1/16W-0402_NU
ICH_SPI_MOSI R189 33-5%-1/16W-0402_NU
ICH_SPI_MISO R191 33-5%-1/16W-0402_NU
SPI_CLK
SPI_CS0#
SPI_CS1#/GPIO58/CLGPIO6
SPI_MOSI
SPI_MISO
SPI
USB
R455 10K-5%-1/16W-0402
USB_RBIAS_PN
USB_RBIAS_PN
R442 22.6-1%-1/16W-0402
USBRBIAS
USBRBIAS#
USB P0--------> USB port
USB P1--------> USB port
USB P2 --------> USB port
USB P3 --------> EASY PORT
USB P4 --------> WLAN
USB P5 --------> Finger printer
USB P6 --------> Bluetooth
USB P7 --------> Camera
USB P8 --------> Card Reader
USB P6 --------> 3G
M10_ICH9M_SFF FCBGA 569P INTEL
6019B0621801
3VS
3VA
R374 3.3K-5%-1/16W-0402_NU
C468 0.1uF 10V 10% 0402 X7R_NU
R373 3.3K-5%-1/16W-0402_NU
U16
W25X32VSSIG SOIC 8P Winbon_NU
6019B0499501_NU
C469 5pF 50V 0.25% 0402 C0G_NU
By Tony
U18B
PCI
Interrupt I/F
PCI_REQ#0
PCI_GNT#0
PCI_REQ#1
PCI_REQ#2
PCI_GNT#2
PCI_REQ#3
PCI_GNT#3
PCI_IRDY#
PCI_DEVSEL#
PCI_PERR#
PCI_LOCK#
PCI_SERR#
PCI_STOP#
PCI_TRDY#
PCI_FRAME#
PLT_RST#
CLK_PCIF_ICH
PCI_IRQA#
PCI_IRQB#
PCI_IRQC#
PCI_IRQD#
PCI_IRQE#
PCI_IRQF#
PCI_IRQG#
PCI_IRQH#
M10_ICH9M_SFF FCBGA 569P INTEL
6019B0621801
PCI Pull up
R430 8.2K-5%-1/16W-0402
R263 8.2K-5%-1/16W-0402
R266 8.2K-5%-1/16W-0402
R439 8.2K-5%-1/16W-0402
R267 8.2K-5%-1/16W-0402
R424 8.2K-5%-1/16W-0402
R433 8.2K-5%-1/16W-0402
R441 8.2K-5%-1/16W-0402
R264 8.2K-5%-1/16W-0402
R421 8.2K-5%-1/16W-0402
R413 8.2K-5%-1/16W-0402
R268 8.2K-5%-1/16W-0402
R447 8.2K-5%-1/16W-0402
R265 8.2K-5%-1/16W-0402
R446 8.2K-5%-1/16W-0402
R427 8.2K-5%-1/16W-0402
R450 8.2K-5%-1/16W-0402
R449 8.2K-5%-1/16W-0402
R448 8.2K-5%-1/16W-0402
R262 8.2K-5%-1/16W-0402
PCI_GNT#2 R417 1K-5%-1/16W-0402_NU
PCI_GNT#3 R437 1K-5%-1/16W-0402_NU
PCI_GNT#0 R445 1K-5%-1/16W-0402_NU
ICH_SPI_CS1# R174 1K-5%-1/16W-0402_NU
PCI_GNT#3
No stuff : by default
Stuff : For A16 swap override
PCI_GNT#0
SPI_CS1#
1 1 LPC
1 0 PCI
0 1 SPI
Check BIOS type
C486 0.1uF 10V 10% 0402 X7R
U17
TC7SZ08F SOT23 5P
6019A0070301
TP19
BUF_PLT_RST# 29,31,32,35
Buffer to reduce loading on PLT_RST#
R412 100K-5%-1/16W-0402
R405 0-5%-1/16W-0402_NU
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
ICH9M PCI/PCIE/DMI/USB(2/4)
SIZE Custom
CODE X01
DOC NUMBER D-CS-1310A226450L-ALG
REV X01
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009
SHEET 28 of 36



BIOS ID setting

Project	MB_ID3	MB_ID2	MB_ID1	MB_ID0
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
	1	1	0	0
	1	0	1	1
	1	0	1	0
	1	0	0	1
	1	0	0	0
	0	1	1	1
	0	1	1	0
	0	1	0	1
	0	1	0	0
	0	0	1	1
	0	0	1	0
	0	0	0	1
	0	0	0	0

ICH9m strap

ACZ_SPKR	No stuff : by default Stuff : For NO reboot

Default is OPEN
Add 0ohm for BIOS Recovery

PMU P/U

EC_WAKEUP#	R208	10K-5%-1/16W-0402
EC_SCI#	R175	10K-5%-1/16W-0402
EC_BATLOW#	R406	8.2K-5%-1/16W-0402
PCIE_WAKE#	R201	1K-5%-1/16W-0402
KBC_SMI#	R389	10K-5%-1/16W-0402
PCI_SERIRQ	R259	8.2K-5%-1/16W-0402
PM_THRM#	R190	8.2K-5%-1/16W-0402
PCI_CLKRUN#	R260	8.2K-5%-1/16W-0402
MB_ID0	R407	10K-5%-1/16W-0402
MB_ID3	R403	10K-5%-1/16W-0402
MB_ID2	R400	10K-5%-1/16W-0402
MB_ID1	R399	10K-5%-1/16W-0402_NU
BLID0	R396	10K-5%-1/16W-0402_NU
MB_ID3	R504	10K-5%-1/16W-0402_NU
MB_ID2	R503	10K-5%-1/16W-0402_NU
MB_ID0	R409	10K-5%-1/16W-0402_NU
MB_ID1	R402	10K-5%-1/16W-0402
PM_STPPCI#	R380	10K-5%-1/16W-0402_NU
PM_STPCPU#	R381	10K-5%-1/16W-0402_NU

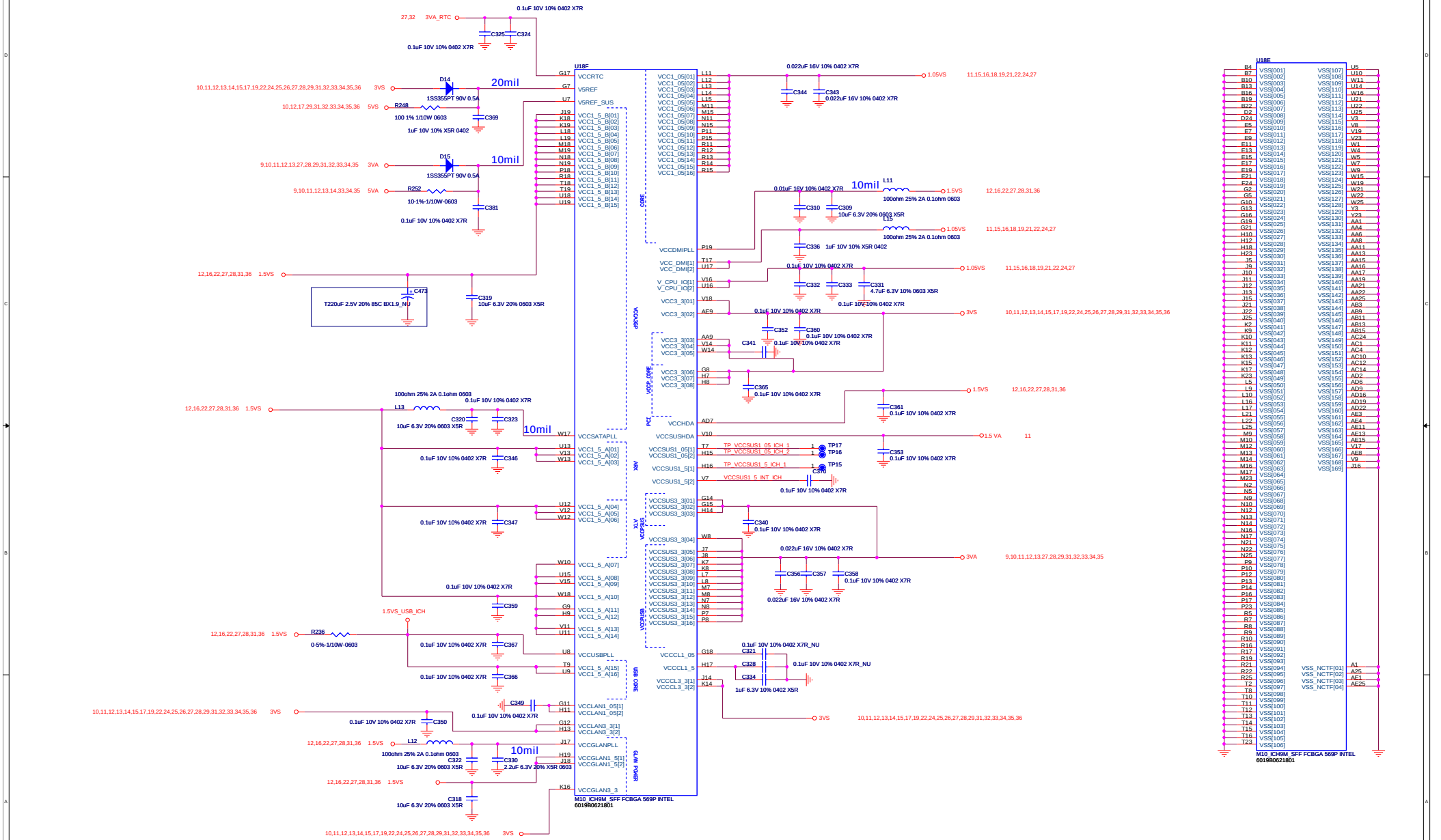
CHANGE by	Miles Liu
DATE	Tuesday, March 10, 2009

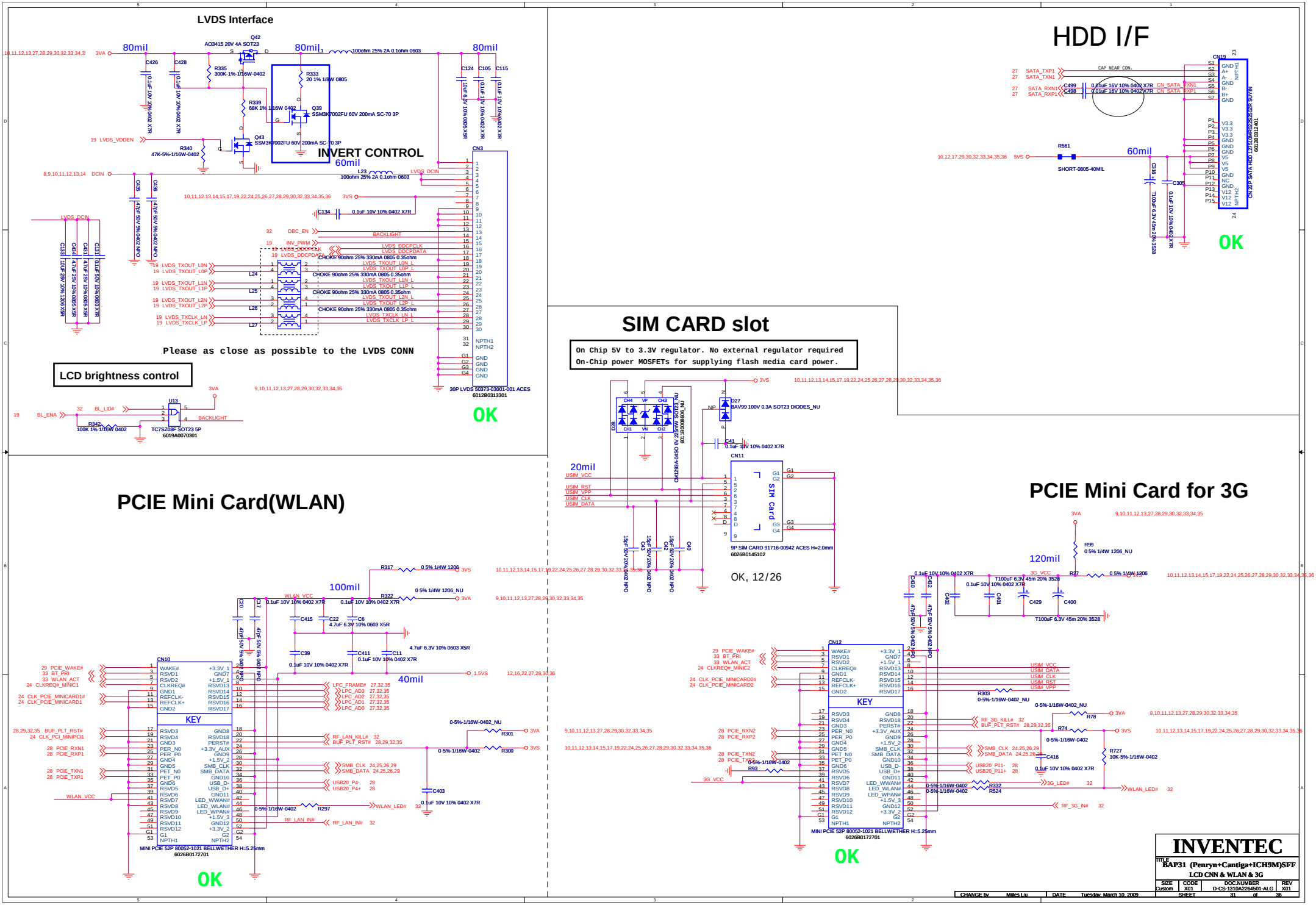
INVENTEC

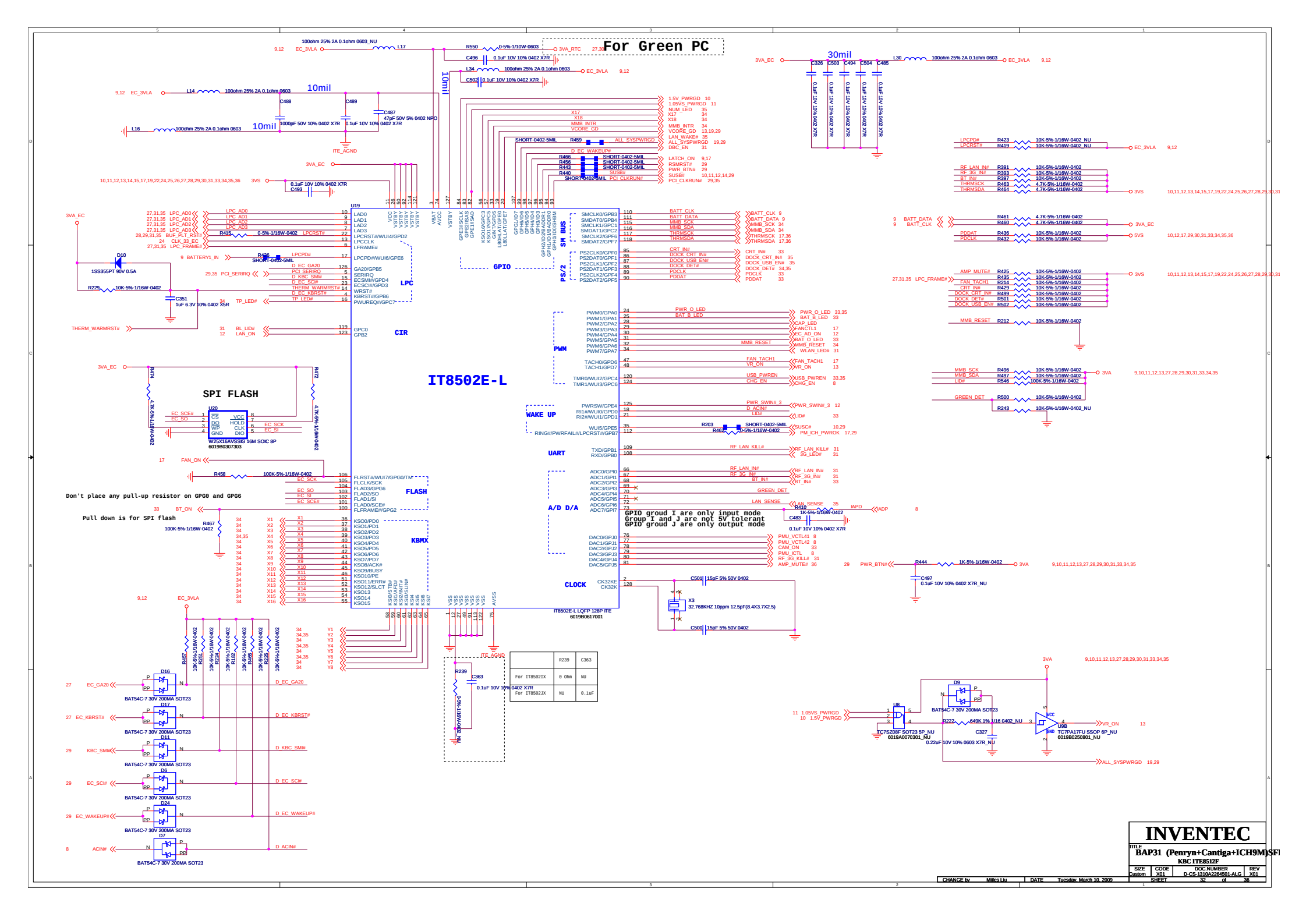
TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
ICH9M GPIO(3/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

SHEET

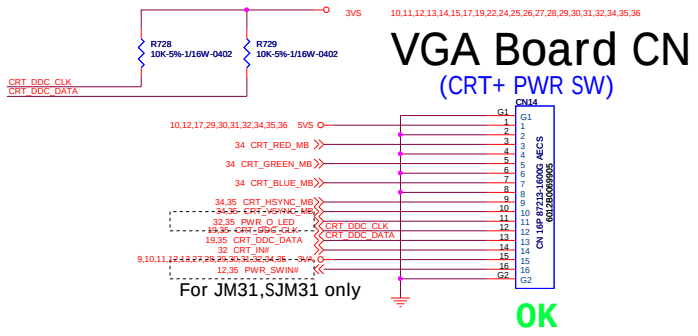

U18F
M10_ICH9M_SFF FCBGA 569P INTEL
6019B0621801
U18E
M10_ICH9M_SFF FCBGA 569P INTEL
6019B0621801
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
ICH9M Power/GND(4/4)
SIZE Custom
CODE X01
DOC.NUMBER D-CS-1310A2264501-ALG
REV X01
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009
SHEET 30 of 36


LVDS Interface
INVERT CONTROL
Please as close as possible to the LVDS CONN
LCD brightness control
OK
HDD I/F
OK
SIM CARD slot
On Chip 5V to 3.3V regulator. No external regulator required
On-Chip power MOSFETs for supplying flash media card power.
OK, 12/26
PCIE Mini Card(WLAN)
OK
PCIE Mini Card for 3G
OK
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
LCD CNN & WLAN & 3G


For Green PC
IT8502E-L
SPI FLASH
W25X16AVSSIG 16M SOC 8P
6019B0307303
IT8502E-L LQFP 128P ITE
6019B0617001
Don't place any pull-up resistor on GPG0 and GPG6
Pull down is for SPI flash
GPIO groud I are only input mode
Group I and J are not 5V tolerant
GPIO groud J are only output mode
LPC
CIR
FLASH
KBMX
GPIO
SM BUS
PS/2
PWM
WAKE UP
UART
A/D D/A
CLOCK
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SF
KBC ITE8512F
DOC.NUMBER D-CS-1310A2264501-ALG
REV X01
SIZE Custom
CODE X01
SHEET 32 of 36
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009

VGA Board CN

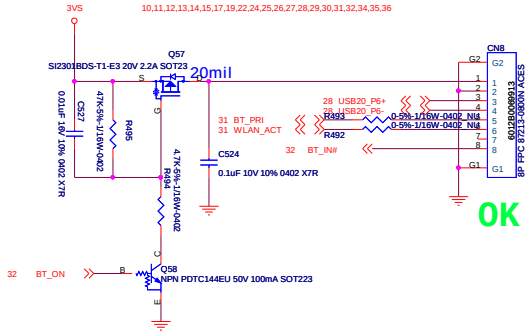
(CRT+ PWR SW)



For JM31,SJM31 only

OK

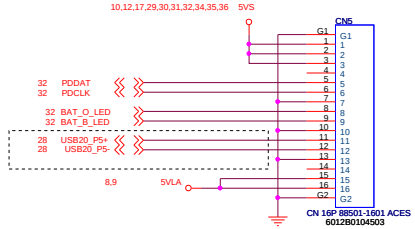
Bluetooth CON.



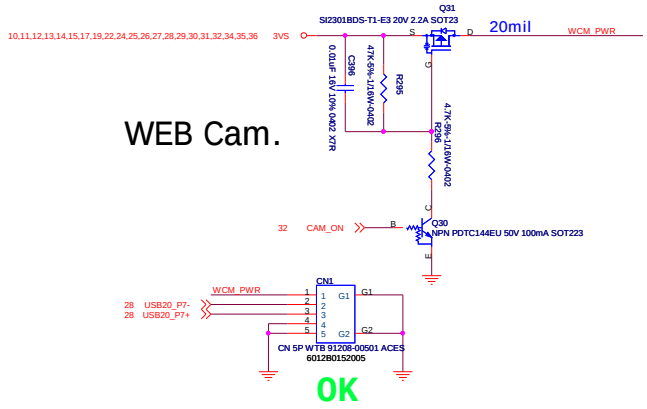
OK

GLIDE PAD Board

For BAP31 only



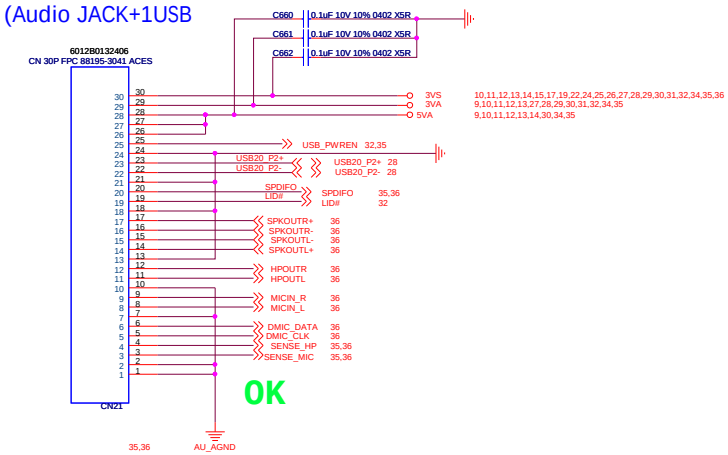
WEB Cam.



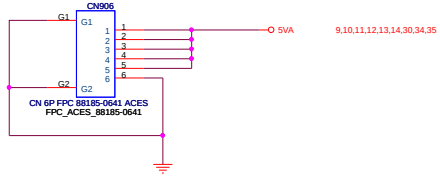
OK

AUDIO Board CN

(Audio JACK+1USB



OK



INVENTEC

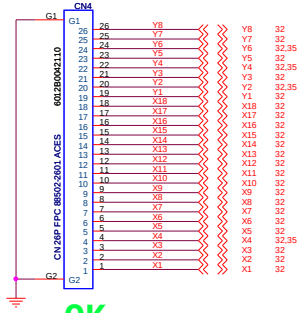
TITLE: BAP31 (Penryn+Cantiga+ICH9M)SI
Daughter Connector

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

SHEET 33 of 36

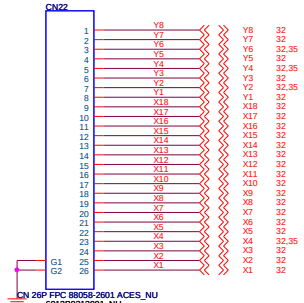
CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

To K/B(For JM31,BAP31)

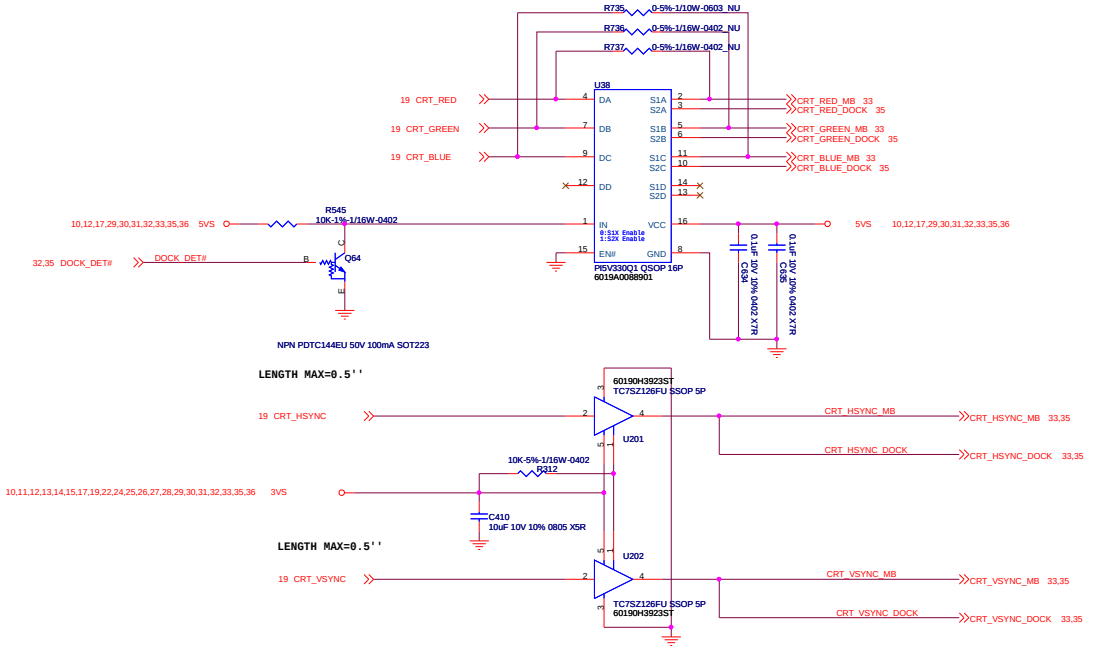


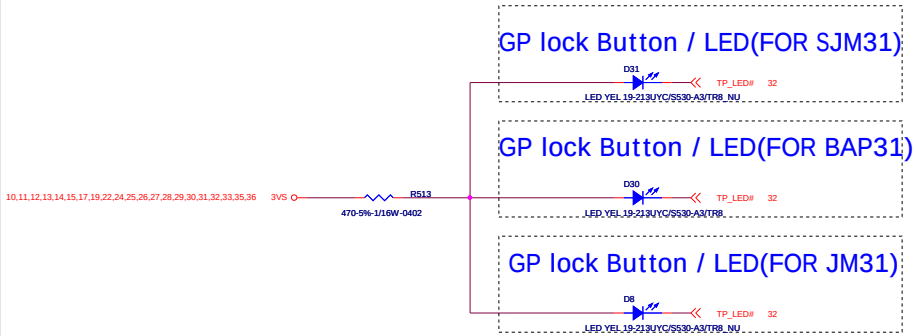
OK

To K/B (For SJM31)

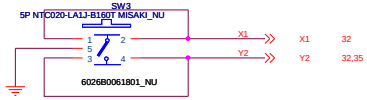


OK



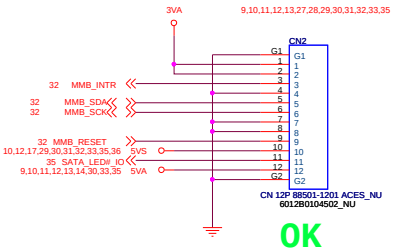


SW (FOR SJM31)



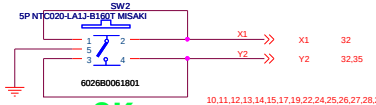
OK

SW Sensor BOARD(For JM31,SJM31)

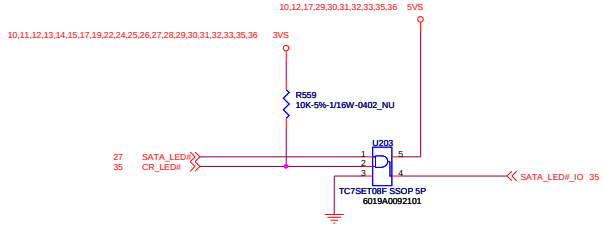


OK

SW (FOR JM31,BAP31)



OK



INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF BDP

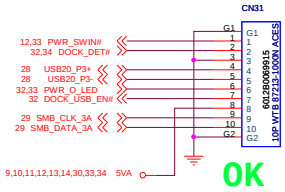
SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

SHEET 34 of 36

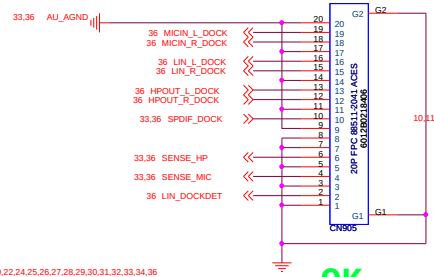
CHANGE by Miles Liu DATE Tuesday, March 10, 2009

For BAP31(EASY/B)

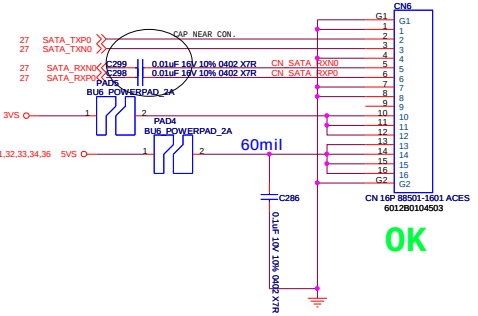
MB(USB) TO EASY/B



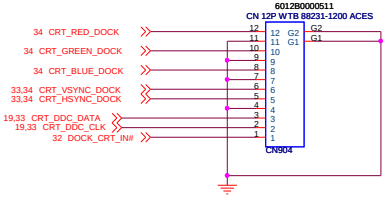
MB(AUDIO) TO EASY/B(For BAP31)



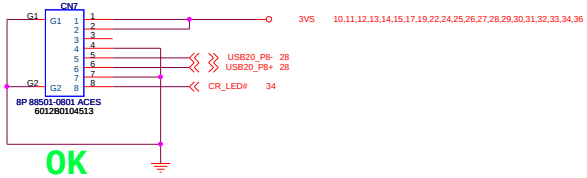
SSD I/F



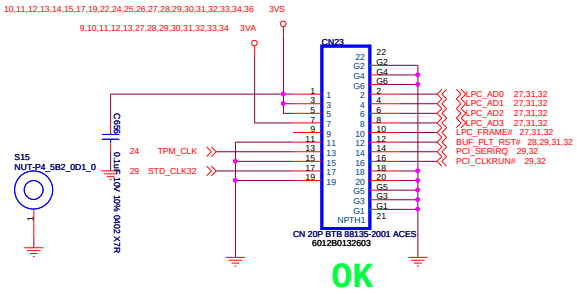
MB(RGB) TO EASY/B



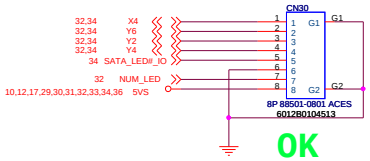
Card Reader BOARD CN

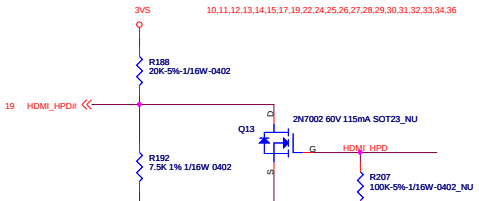


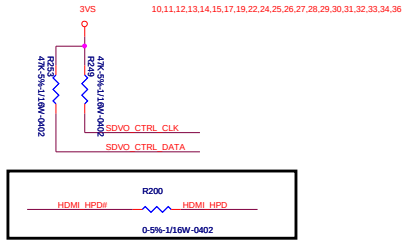
TPM CN



SW/B CN

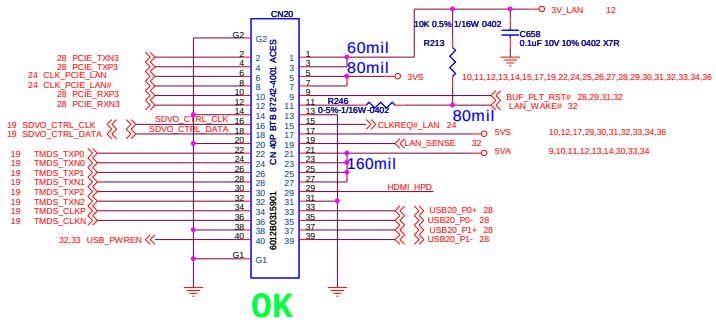






USB Board CN

(LAN+HDMI+2USB)

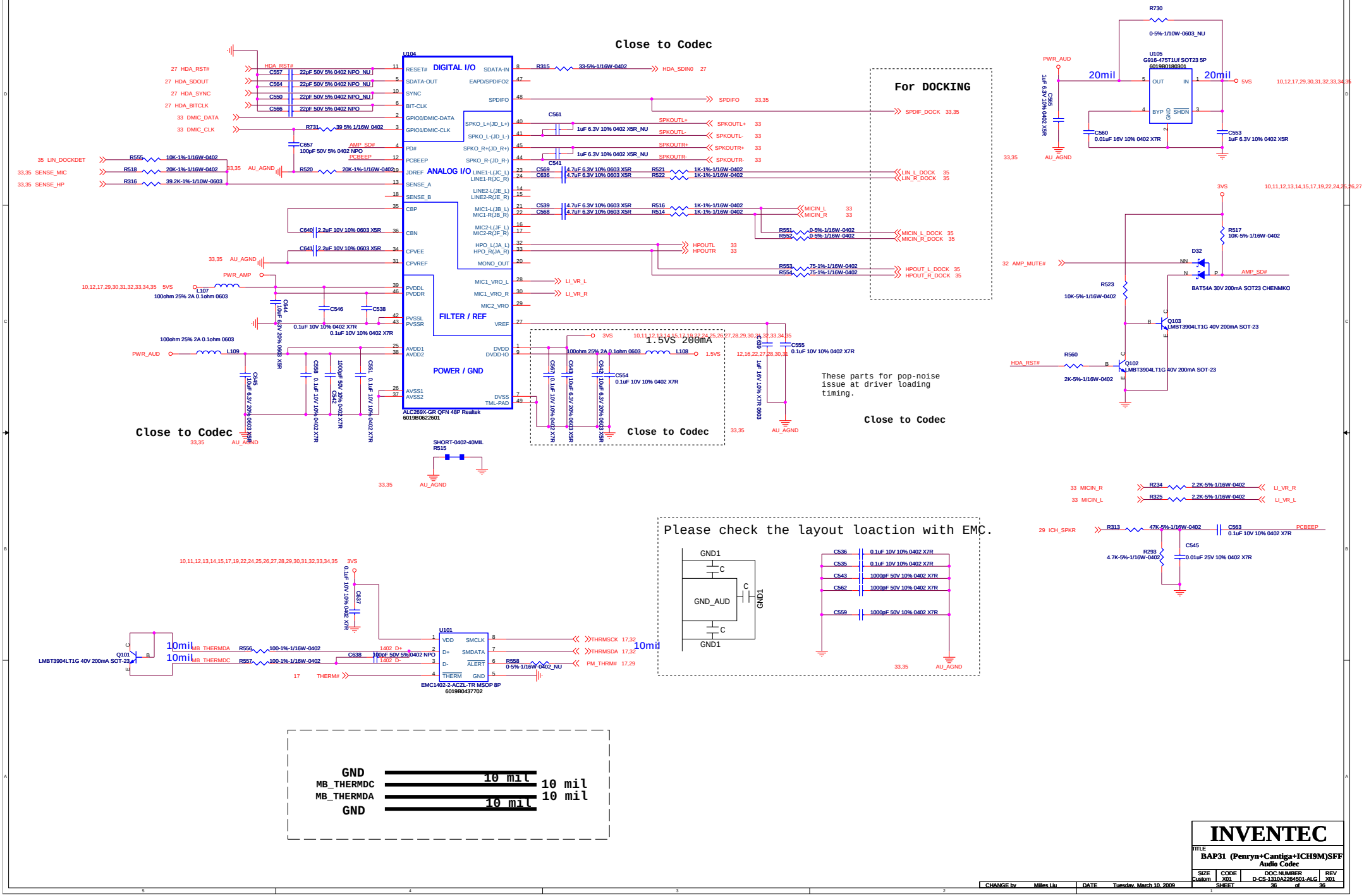


CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF BDP

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01
SHEET		35 of 36	



CHANGE by	Miles Liu
DATE	Tuesday, March 10, 2009

INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF Audio Codec

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01
SHEET	36	of	36