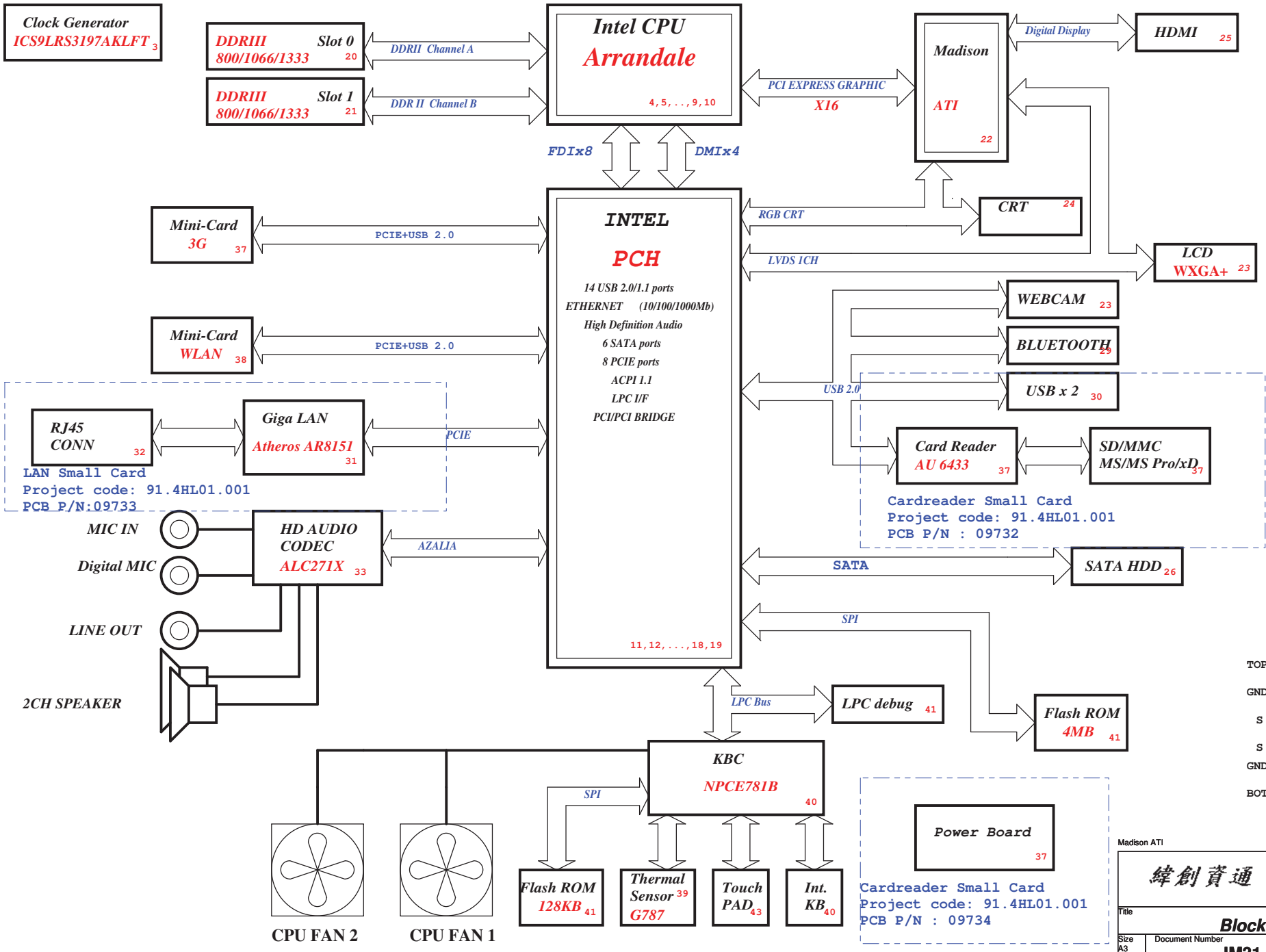
# JM31-CP Block Diagram

Project code: 91.4HL01.001
PCB P/N : 48.4HL01.031
REVISION : 09921-3




| SYSTEM DC/DC RT8223BGQW | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | 5V_S5<br>3D3V_S5<br>49 |

| SYSTEM DC/DC RT8209EGQW | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | 1D5V_S3<br>50 |

| SYSTEM DC/DC RT8209EGQW | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | 1D05V_S0<br>50 |

| SYSTEM DC/DC RT8209EGQW | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | 1D05V_VTT<br>51 |

| CPU DC/DC ISL62882HRTZ-T | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | VCC_CORE<br>47,48 |

| MAXIM CHARGER ISL62881HRTZ-T | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | VCC_GFXCORE<br>53 |

PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

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Title: Block Diagram

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# PCH Strapping

| Name | Schematics Notes |
|---|---|
| SPKR | **Reboot option at power-up**<br>**Default Mode:** Internal weak Pull-down.<br>**No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor. |
| INIT3_3V# | Weak internal pull-down. Do not pull high. |
| GNT3#/ GPIO55 | **Default Mode:** Internal pull-up.<br>**Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor). |
| INTVRMEN | **High (1) = Integrated VRM is enabled**<br>**Low (0) = Integrated VRM is disabled** |
| GNT0#, GNT1# | **Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required.<br>**Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.<br>**Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. |
| GNT2#/ GPIO53 | **Default – Internal pull-up.**<br>**Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops). |
| GPIO33 | **Default:** Do not pull low.<br>**Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor. |
| SPI_MOSI | **Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor<br>**Disable iTPM:** Left floating, no pull-down required. |
| NV_ALE | **Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.<br>**Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor. |
| NC_CLE | Weak internal pull-up. Do not pull low. |
| HAD_DOCK_EN# /GPIO[33] | **Low (0):** Flash Descriptor Security will be overridden.<br>**High (1) :** Flash Descriptor Security will be in effect. |
| HDA_SDO | Weak internal pull-down. Do not pull high. |
| HDA_SYNC | Weak internal pull-down. Do not pull high. |
| GPIO15 | Weak internal pull-down. Do not pull high. |
| GPIO8 | Weak internal pull-up. Do not pull low. |
| GPIO27 | **Default = Do not connect (floating)**<br>High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.<br>Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails. |

# PCIE Routing

| | |
|---|---|
| LANE1 | LAN |
| LANE2 | MiniCard1 |
| LANE3 | MiniCard2 |

# USB Table

| Pair | Device |
|---|---|
| 0 | USB1 |
| 1 | USB2 |
| 2 | USB4 |
| 3 | MINICARD2 |
| 4 | WECAM |
| 5 | Blue Tooth |
| 6 | MINIC1 |
| 7 | Cardreader |
| 8 | NC |
| 9 | NC |
| 10 | NC |
| 11 | NC |
| 12 | NC |
| 13 | NC |

# Processor Strapping

| Pin Name | Strap Description | Configuration (Default value for each bit is 1 unless specified otherwise) | Default Value |
|---|---|---|---|
| CFG[4] | **Embedded DisplayPort Presence** | 1: Disabled - No Physical Display Port attached to Embedded DisplayPort.<br>0: Enabled - An external Display Port device is connected to the Embedded Display Port. | 1 |
| CFG[3] | **PCI-Express Static Lane Reversal** | 1: Normal Operation.<br>0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ... | 1 |
| CFG[0] | **PCI-Express Configuration Select** | 1: Single PCI-Express Graphics<br>0: Bifurcation enabled | 1 |
| CFG[7] | **Reserved – Temporarily used for early Clarksfield samples.** | **Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor<br>**Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].<br>For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality. | 0 |

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Title: **Table of Content**

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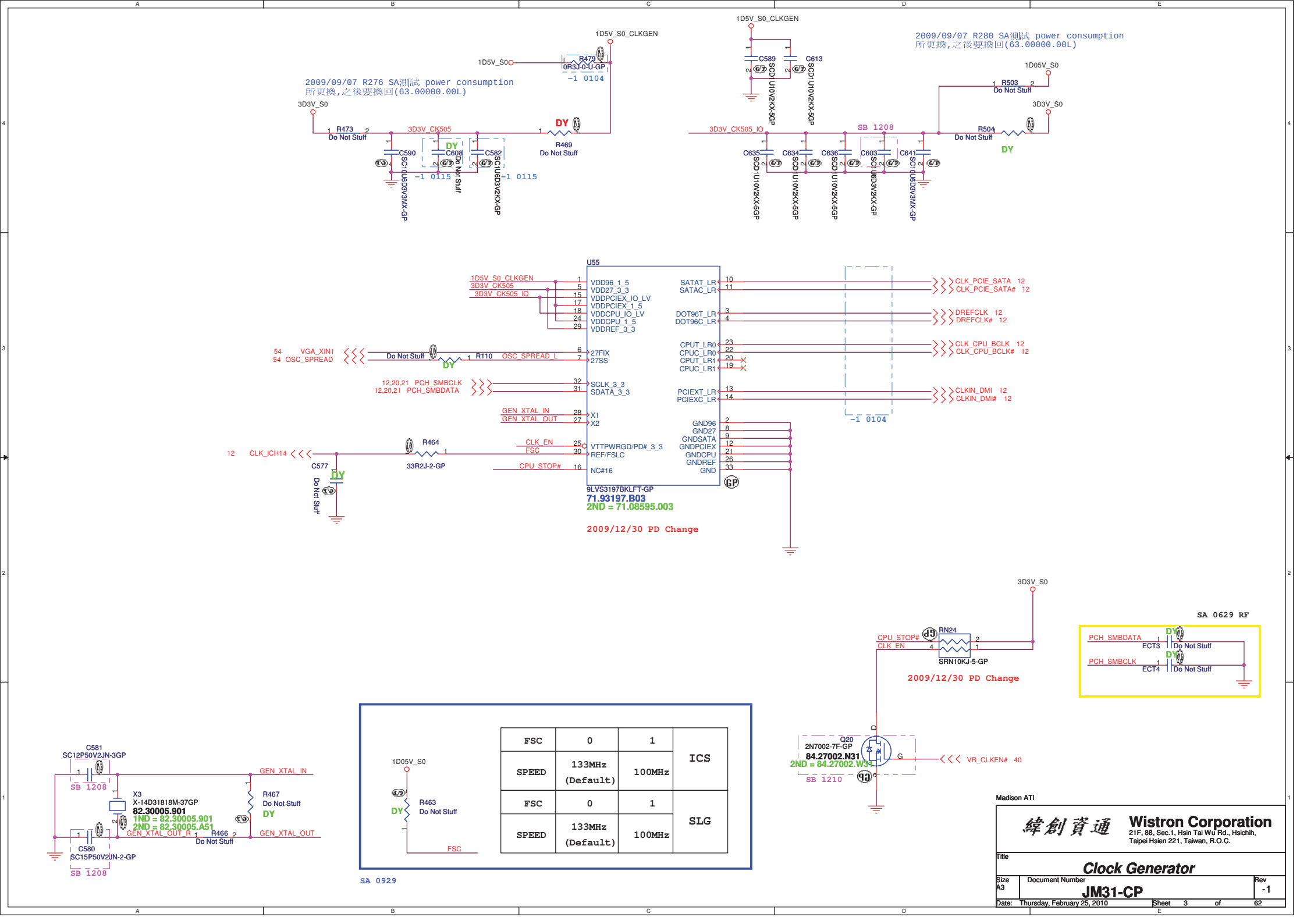


| FSC | 0 | 1 | ICS |
|---|---|---|---|
| SPEED | 133MHz (Default) | 100MHz | |
| FSC | 0 | 1 | SLG |
| SPEED | 133MHz (Default) | 100MHz | |

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Title: **Clock Generator**

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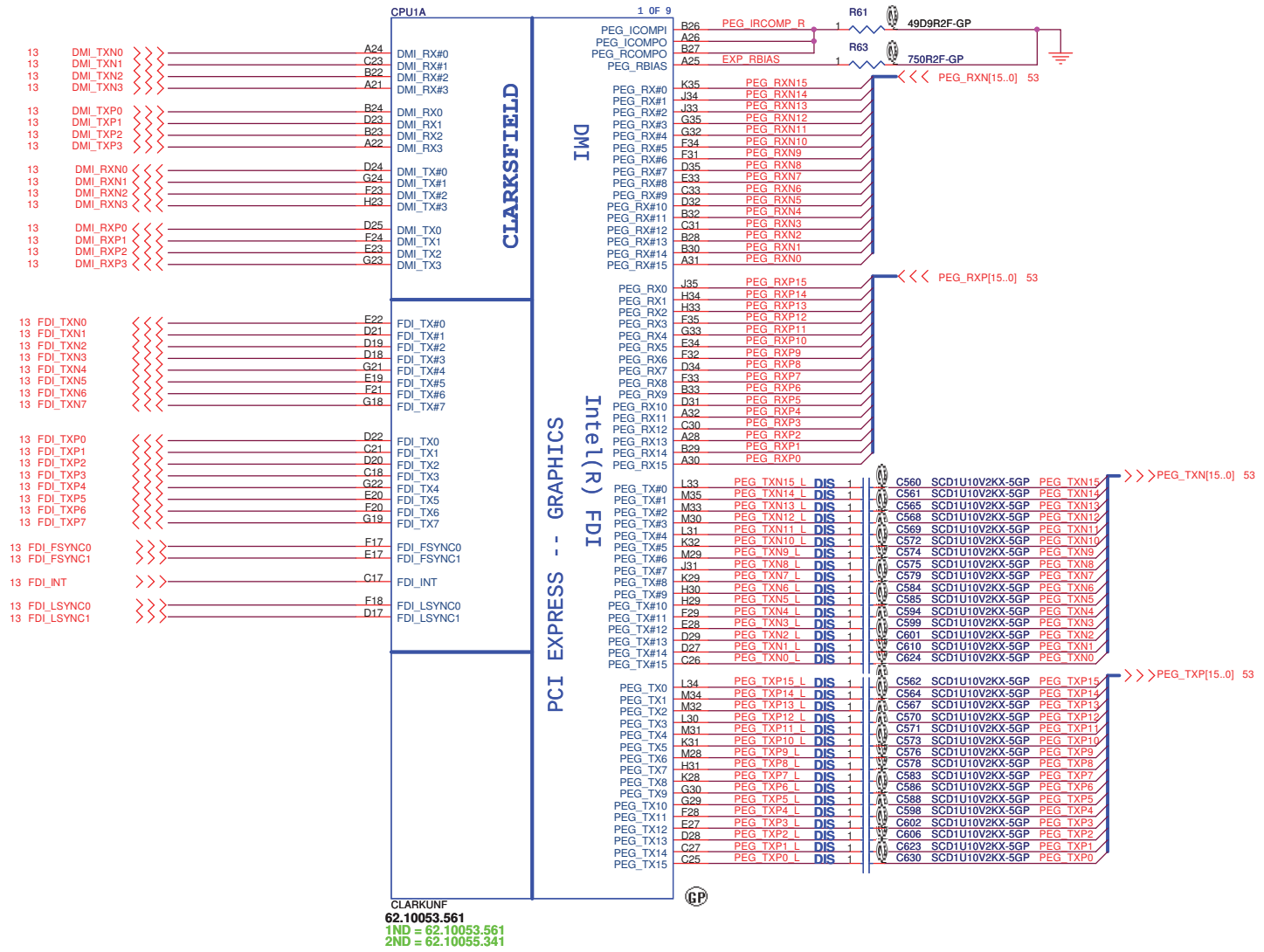


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Title: ***CPU (1/7)***

| Size | Document Number | Rev |
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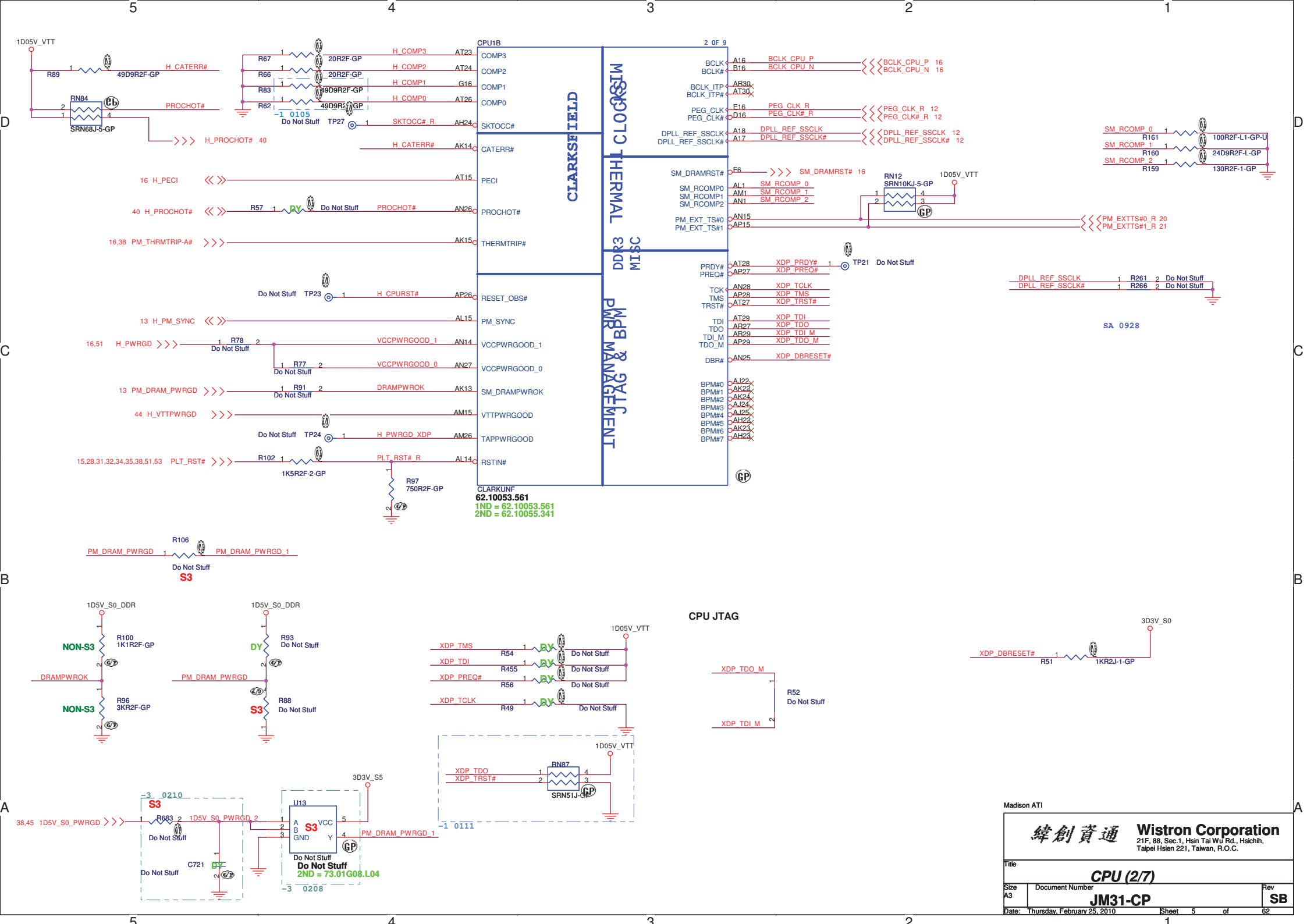
CPU1B
CLARKSFIELD
CLOCKS
THERMAL
MISC
DDR3
PWR MANAGEMENT
CLARKUNF
62.10053.561
1ND = 62.10053.561
2ND = 62.10055.341
CPU JTAG
SA 0928
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Title
CPU (2/7)
Size
A3
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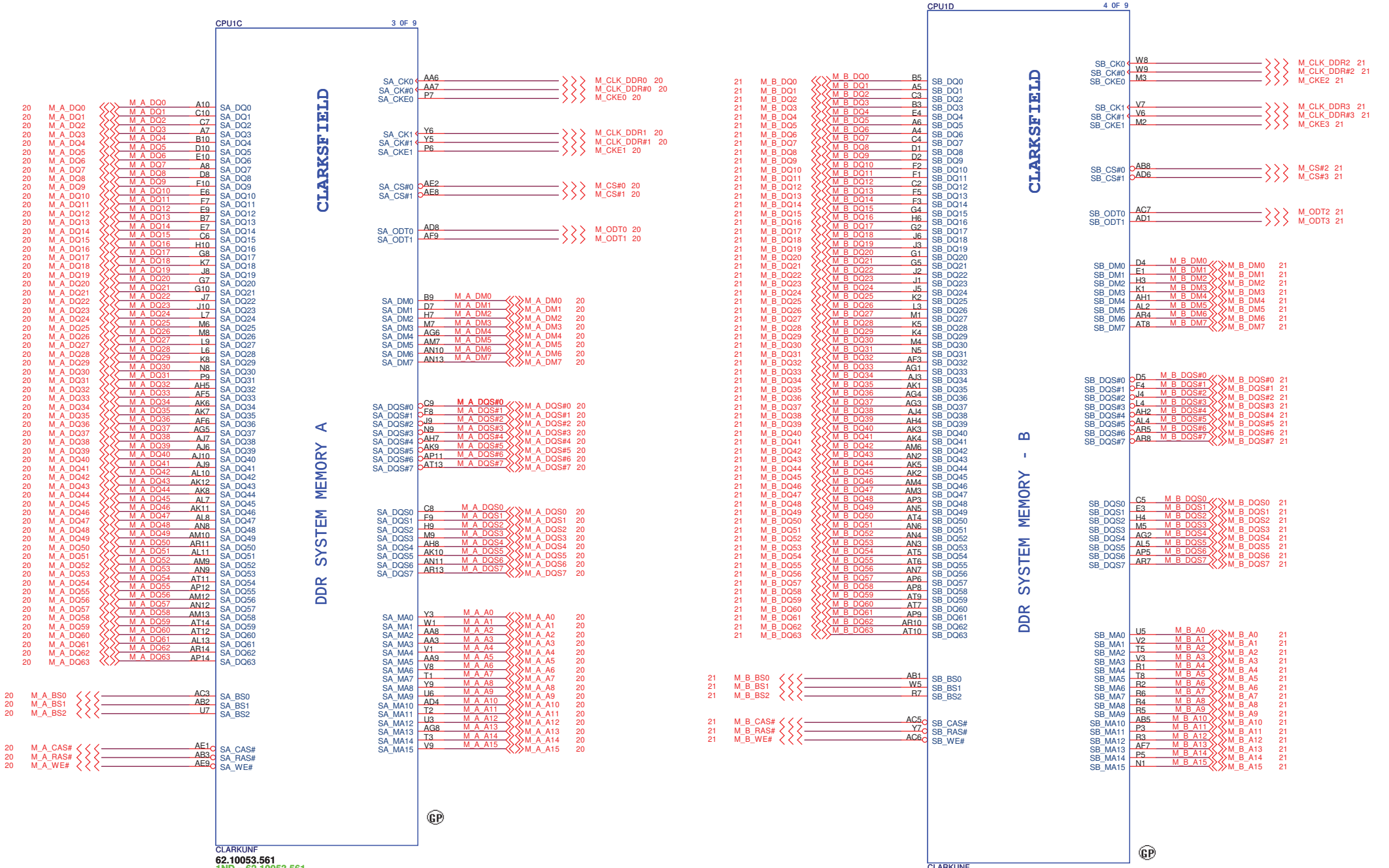


| | |
|---|---|
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| | | |
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| Title | | |
| **CPU (3/7)** | | |
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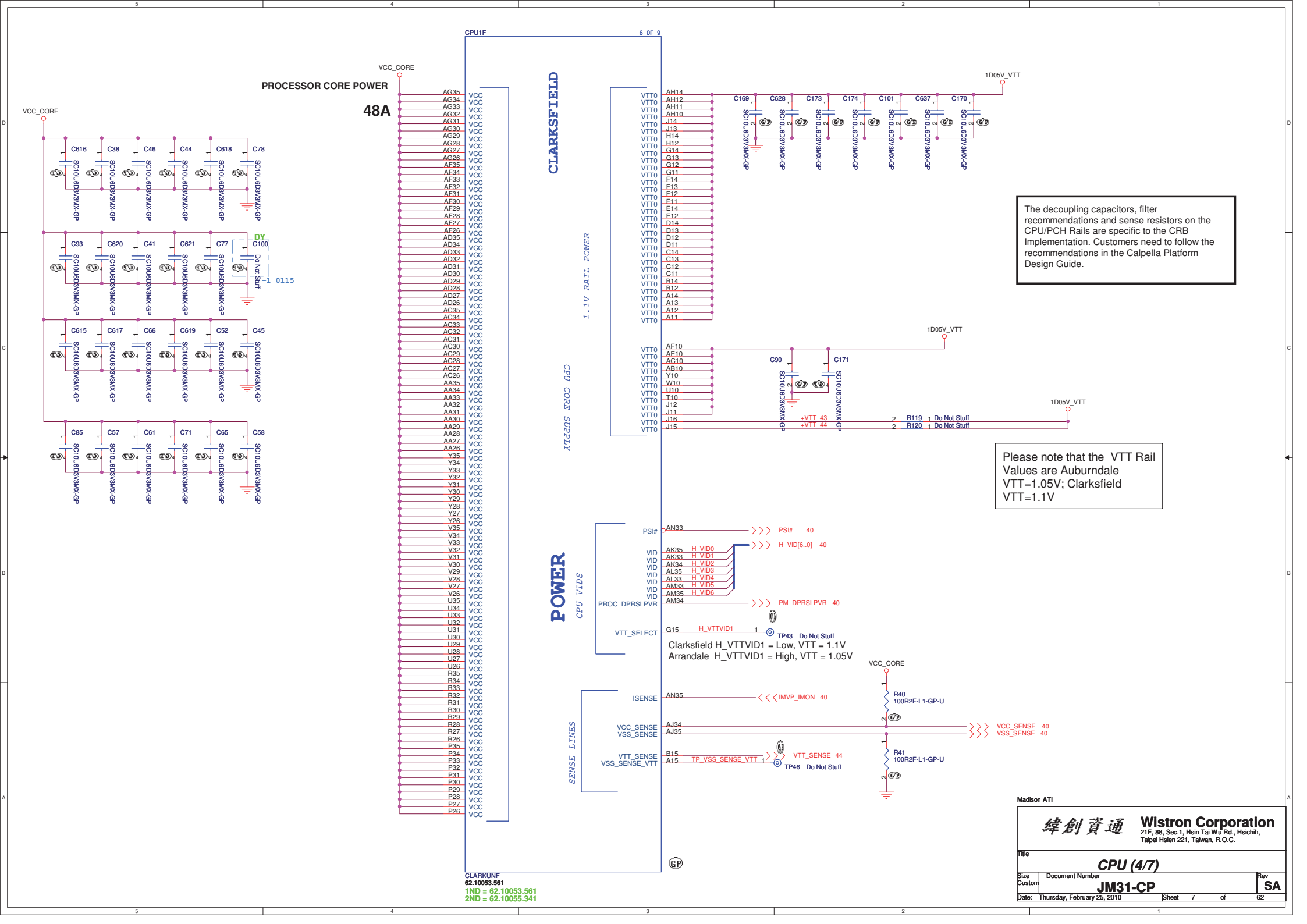
PROCESSOR CORE POWER
48A
VCC_CORE
CPU1F
6 OF 9
CLARKSFIELD
1.1V RAIL POWER
CPU CORE SUPPLY
1D05V_VTT
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
POWER
CPU VIDS
PSI#
H_VID[6..0]
PROC_DPRSLPVR
VTT_SELECT
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V
SENSE LINES
ISENSE
VCC_SENSE
VSS_SENSE
VTT_SENSE
VSS_SENSE_VTT
CLARKUNF
62.10053.561
1ND = 62.10053.561
2ND = 62.10055.341
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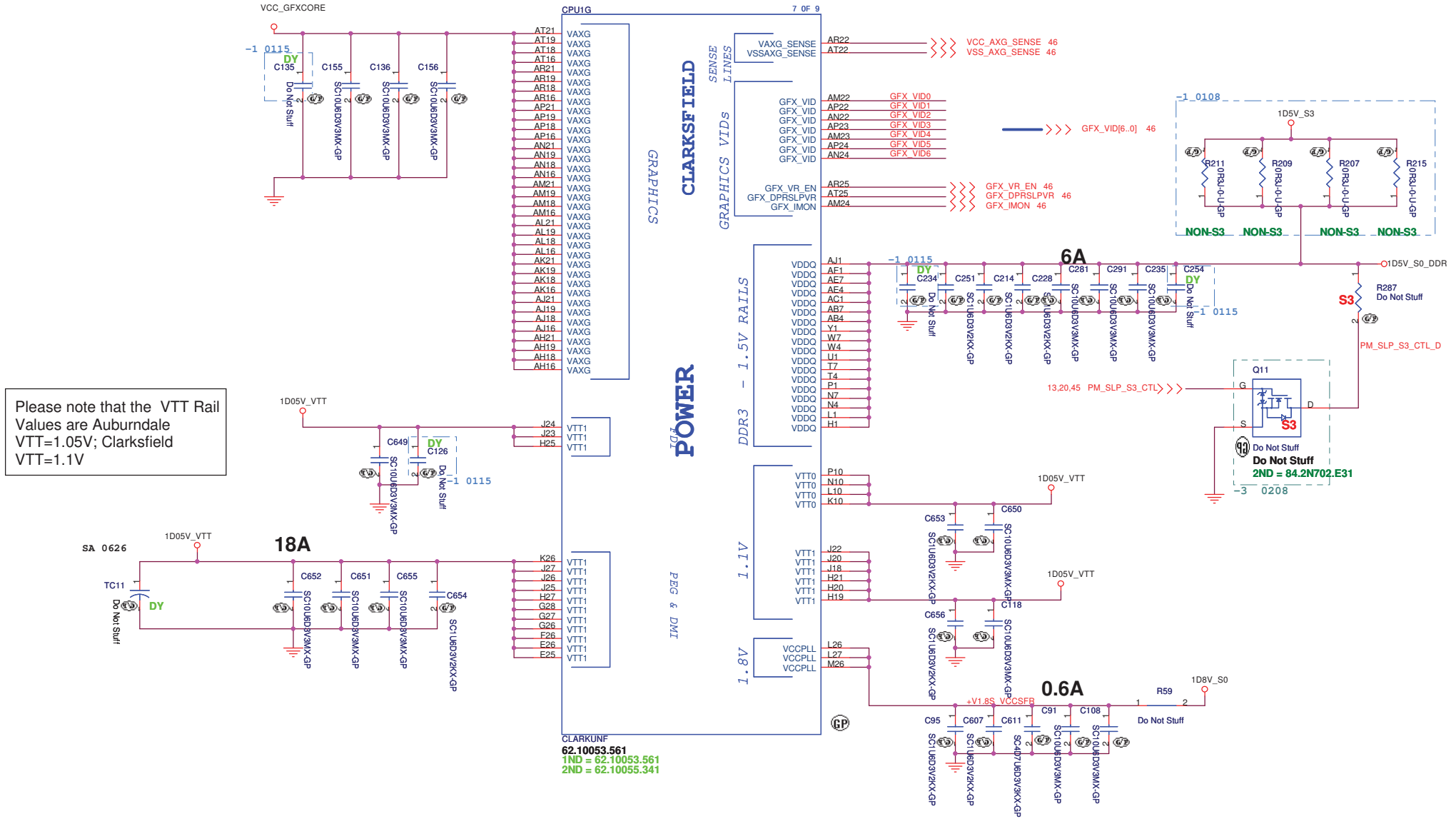


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| | | |
|---|---|---|
| Title | CPU (5/7) | |
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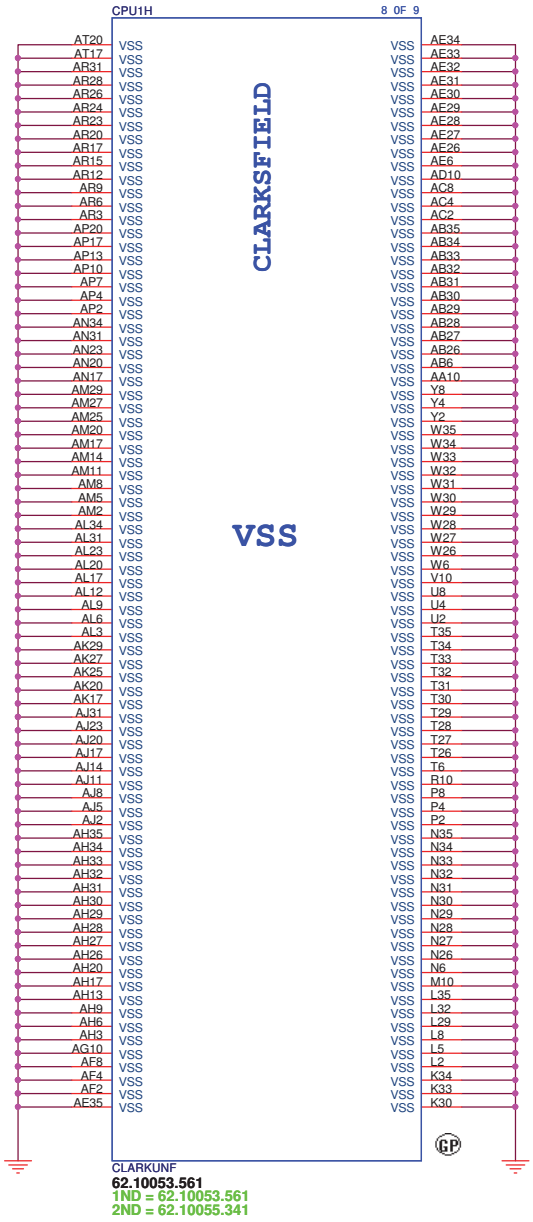


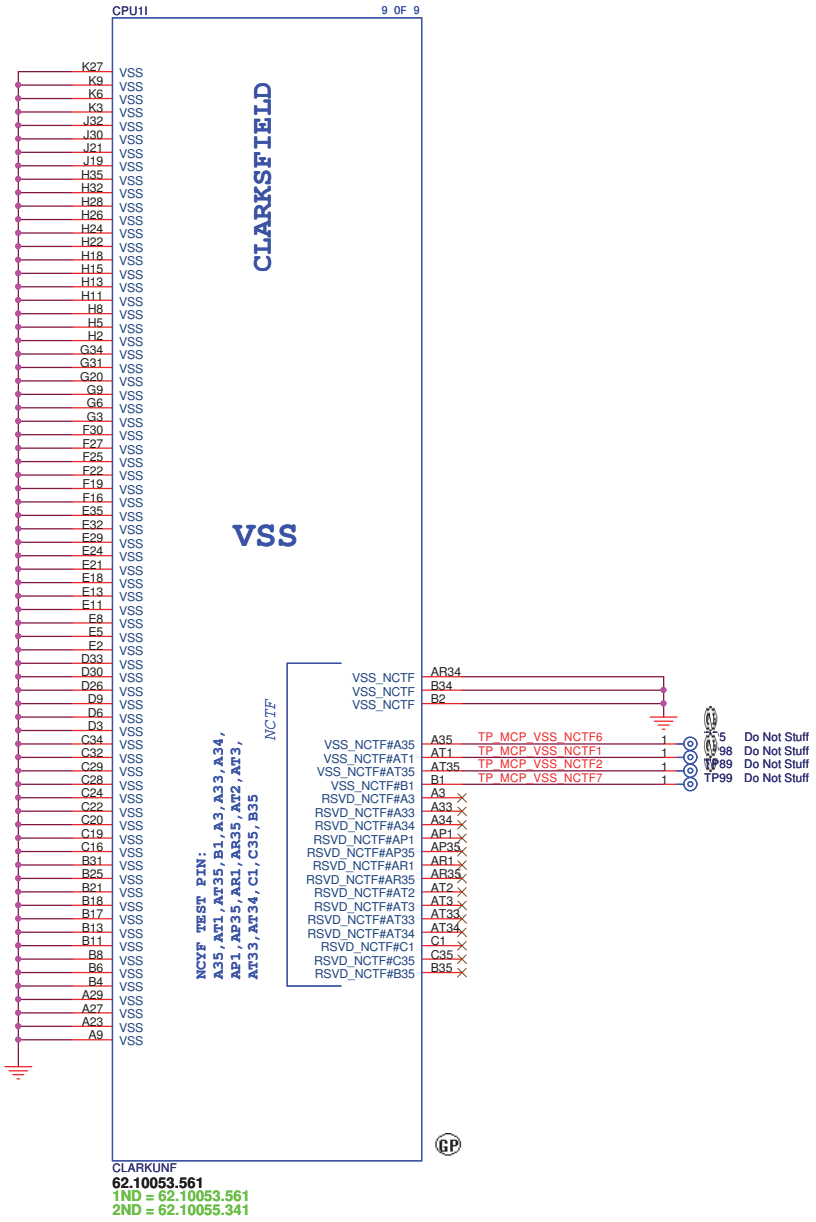


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| | | |
|---|---|---|
| Title: *CPU (6/7)* | | |
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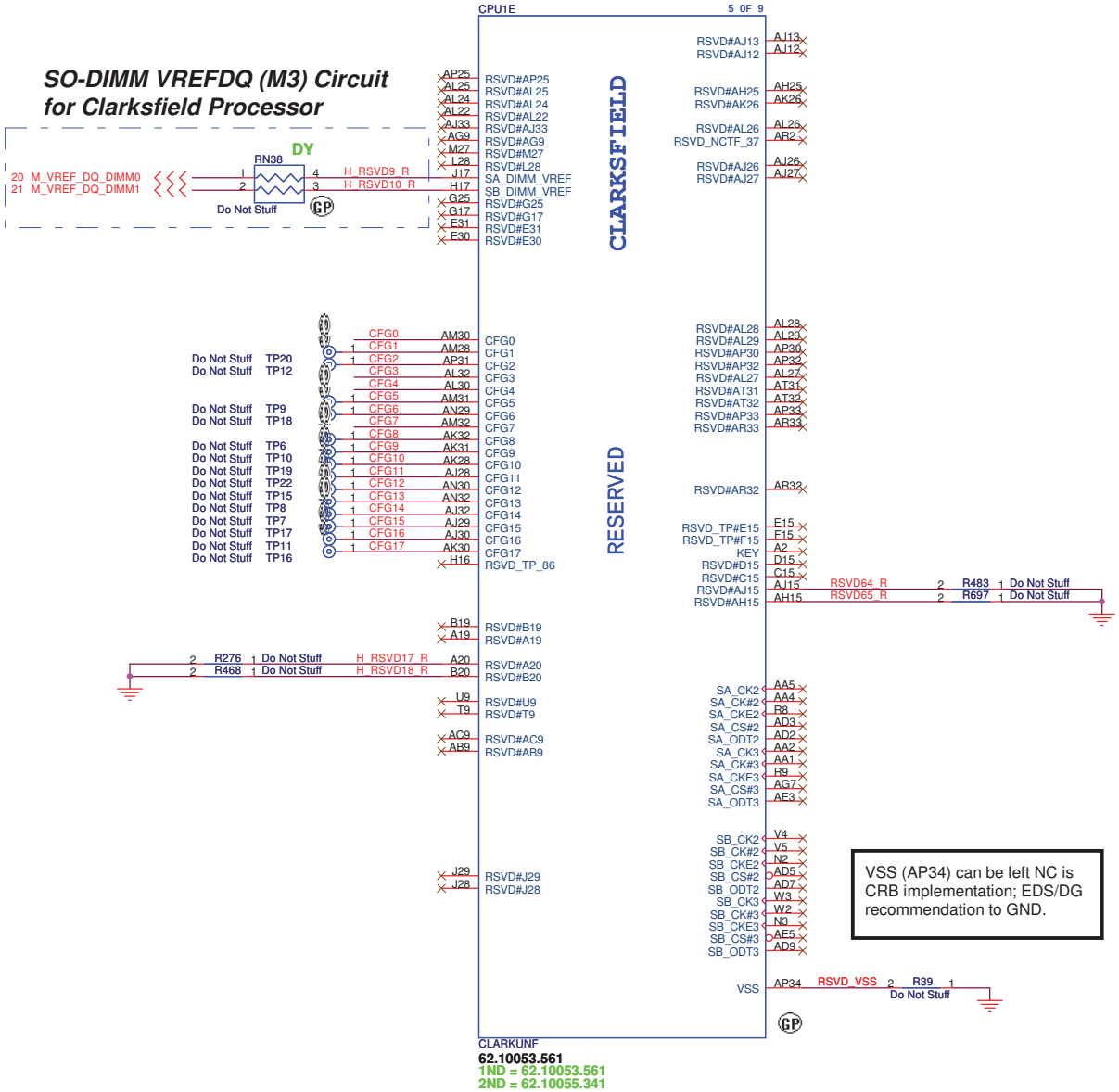
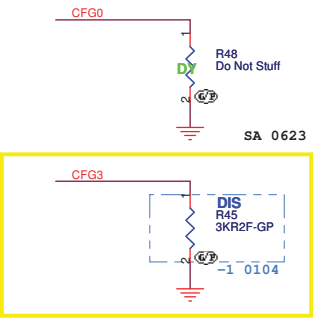
## SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor




VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.




| PCI-Express Configuration Select | |
|---|---|
| CFG0 | 1:Single PEG<br>0:Bifurcation enabled |

| CFG3 - PCI-Express Static Lane Reversal | |
|---|---|
| CFG3 | 1 :Normal Operation<br>0 :Lane Numbers Reversed<br>15 -> 0, 14 -> 1, ... |

| CFG4 - Display Port Presence | |
|---|---|
| CFG4 | 1:Disabled; No Physical Display Port attached to Embedded Display Port<br>0:Enabled; An external Display Port device is connected to the Embedded Display Port |

| CFG7(Reserved) - Temporarily used for early Clarksfield samples. | |
|---|---|
| CFG7 | Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.<br><br>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].<br>For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality. |

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Title: ***CPU (7/7)***

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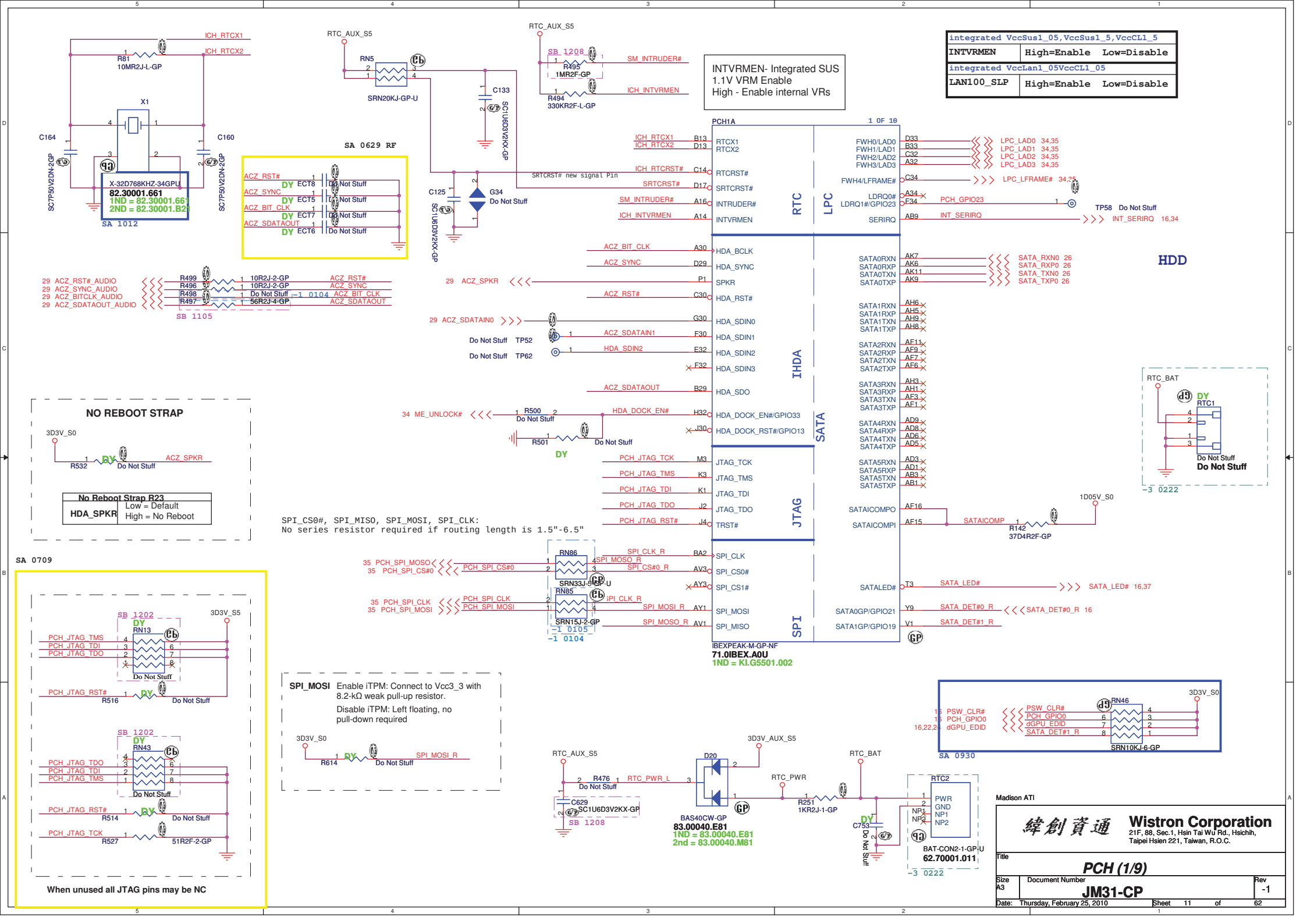
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs
PCH1A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
HDD
NO REBOOT STRAP
No Reboot Strap R23
HDA_SPKR Low = Default High = No Reboot
SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"
SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
When unused all JTAG pins may be NC
SA 0709
SA 0629 RF
SA 1012
SA 1105
SA 0930
IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002
BAS40CW-GP
83.00040.E81
1ND = 83.00040.E81
2nd = 83.00040.M81
BAT-CON2-1-GP-U
62.70001.011
X-32D768KHZ-34GPU
82.30001.661
1ND = 82.30001.661
2ND = 82.30001.B21
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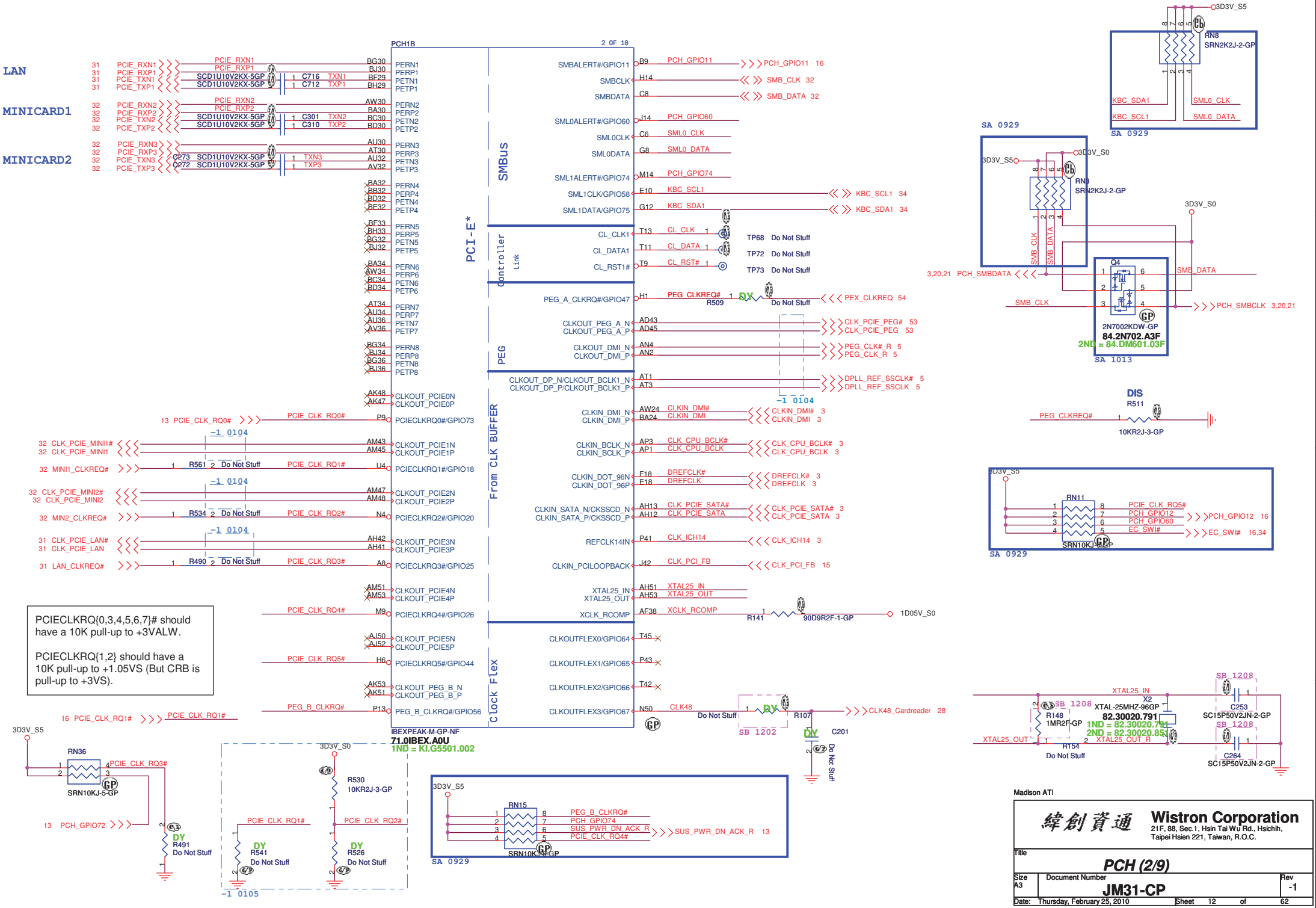
LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002
SMBALERT#/GPIO11
SMBCLK
SMBDATA
SML0ALERT#/GPIO60
SML0CLK
SML0DATA
SML1ALERT#/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
CL_CLK1
CL_DATA1
CL_RST1#
PEG_A_CLKRQ#/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N/CLKOUT_BCLK1_N
CLKOUT_DP_P/CLKOUT_BCLK1_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_BCLK_N
CLKIN_BCLK_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N/CKSSCD_N
CLKIN_SATA_P/CKSSCD_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
PCIECLKRQ0#/GPIO73
PCIECLKRQ1#/GPIO18
PCIECLKRQ2#/GPIO20
PCIECLKRQ3#/GPIO25
PCIECLKRQ4#/GPIO26
PCIECLKRQ5#/GPIO44
PEG_B_CLKRQ#/GPIO56
CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLKOUT_PCIE2N
CLKOUT_PCIE2P
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
SA 0929
SA 1013
DIS
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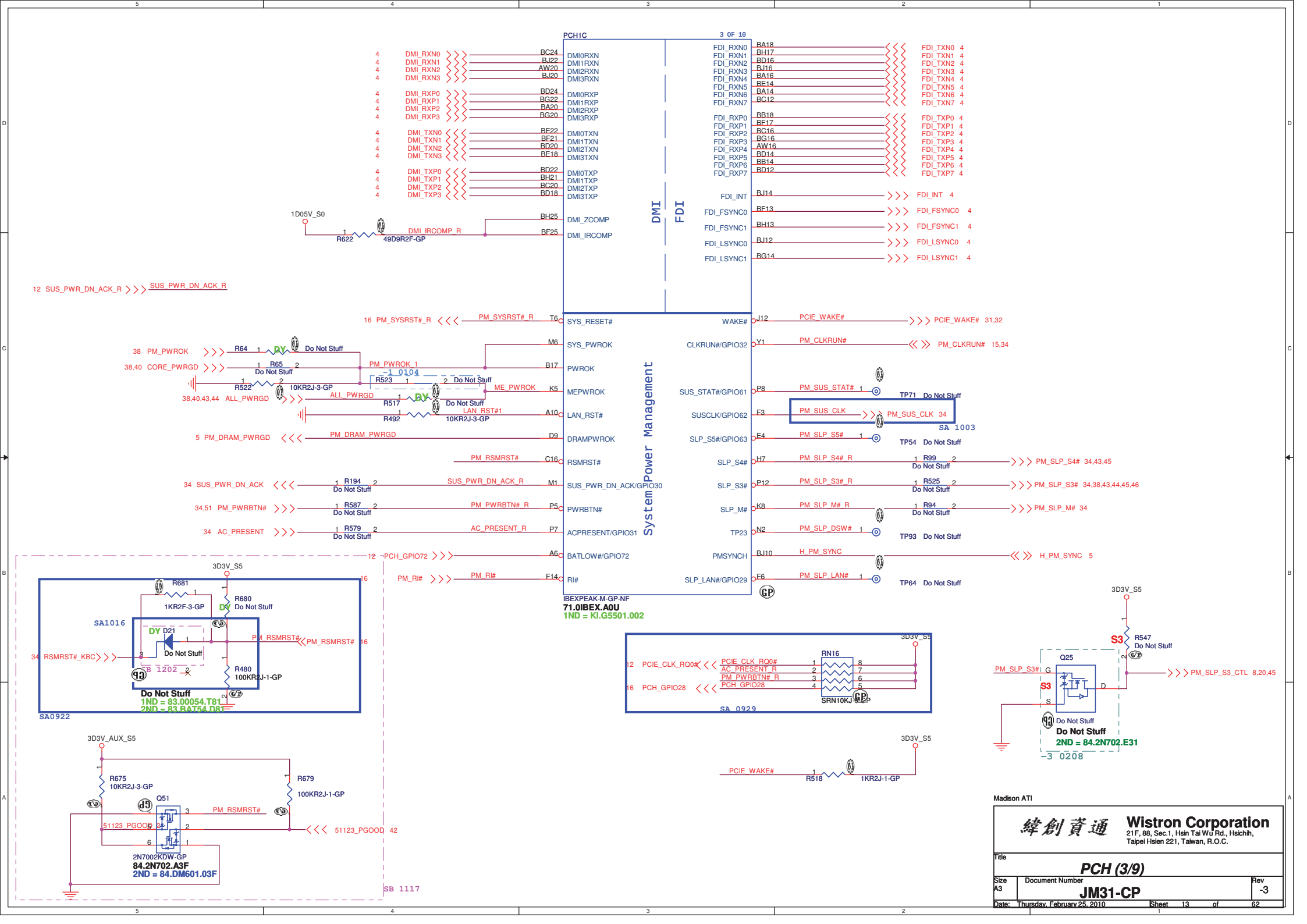
PCH1C
3 OF 10
DMI
FDI
System Power Management
IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002
SA1016
SA0922
SB 1202
SB 1117
SA 0929
-3 0208
SA 1003
Do Not Stuff
1ND = 83.00054.T81
2ND = 83.BAT54.D81
2ND = 84.2N702.E31
84.2N702.A3F
2ND = 84.DM601.03F
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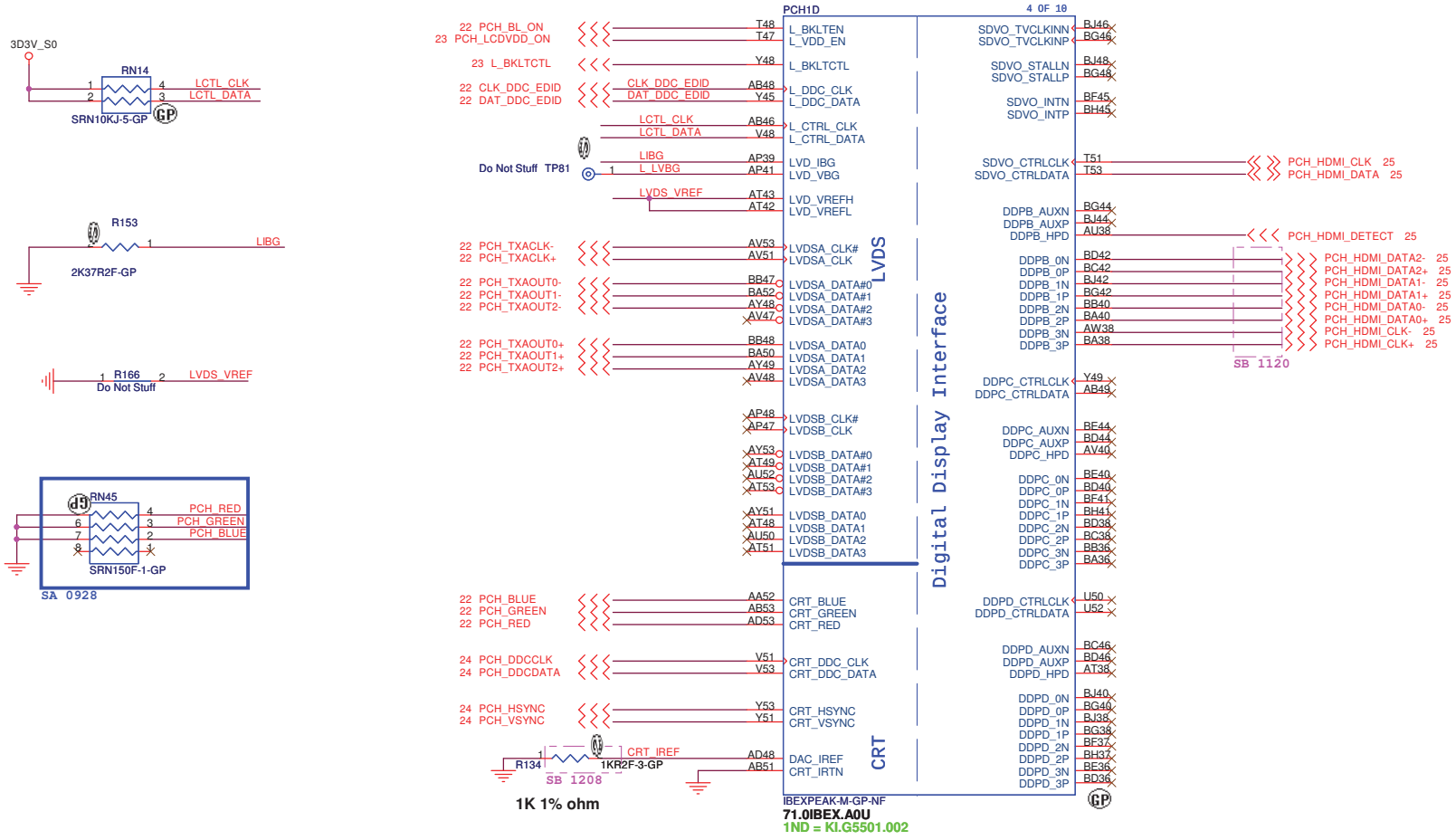


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| | | |
|---|---|---|
| Title | ***PCH (4/9)*** | |
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These pins are left as NC, because the function is disable.

These pins are left as NC, because the function is disable.

| DMI Termination Voltage | |
|---|---|
| NV_CLE | Set to Vss when low.<br>Set to Vcc when high. |

Danbury Technology:
Disabled when Low.
Enable when High.

| BOOT BIOS Strap | | |
|---|---|---|
| PCI_GNT#0 | PCI_GNT#1 | BOOT BIOS Location |
| 0 | 0 | LPC(Default) |
| 1 | 0 | Reserved |
| 0 | 1 | PCI |
| 1 | 1 | SPI |

USE SPI

| A16 swap override Strap/Top-Block Swap Override jumper | |
|---|---|
| PCI_GNT#3 | Low = A16 swap override/Top-Block Swap Override enabled<br>High = Default |

USB

| Pair | Device |
|---|---|
| 0 | EXT USB1 |
| 1 | USB1(on board) |
| 2 | EXT USB2 |
| 3 | MINICARD1 |
| 4 | WECAM |
| 5 | SIM Card |
| 6 | NC |
| 7 | NC |
| 8 | NC |
| 9 | NC |
| 10 | NC |
| 11 | Blue Tooth |
| 12 | MINIC2 |
| 13 | Cardreader |

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Title: PCH (5/9)

| Size | Document Number | Rev |
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| A3 | JM31-CP | SB |

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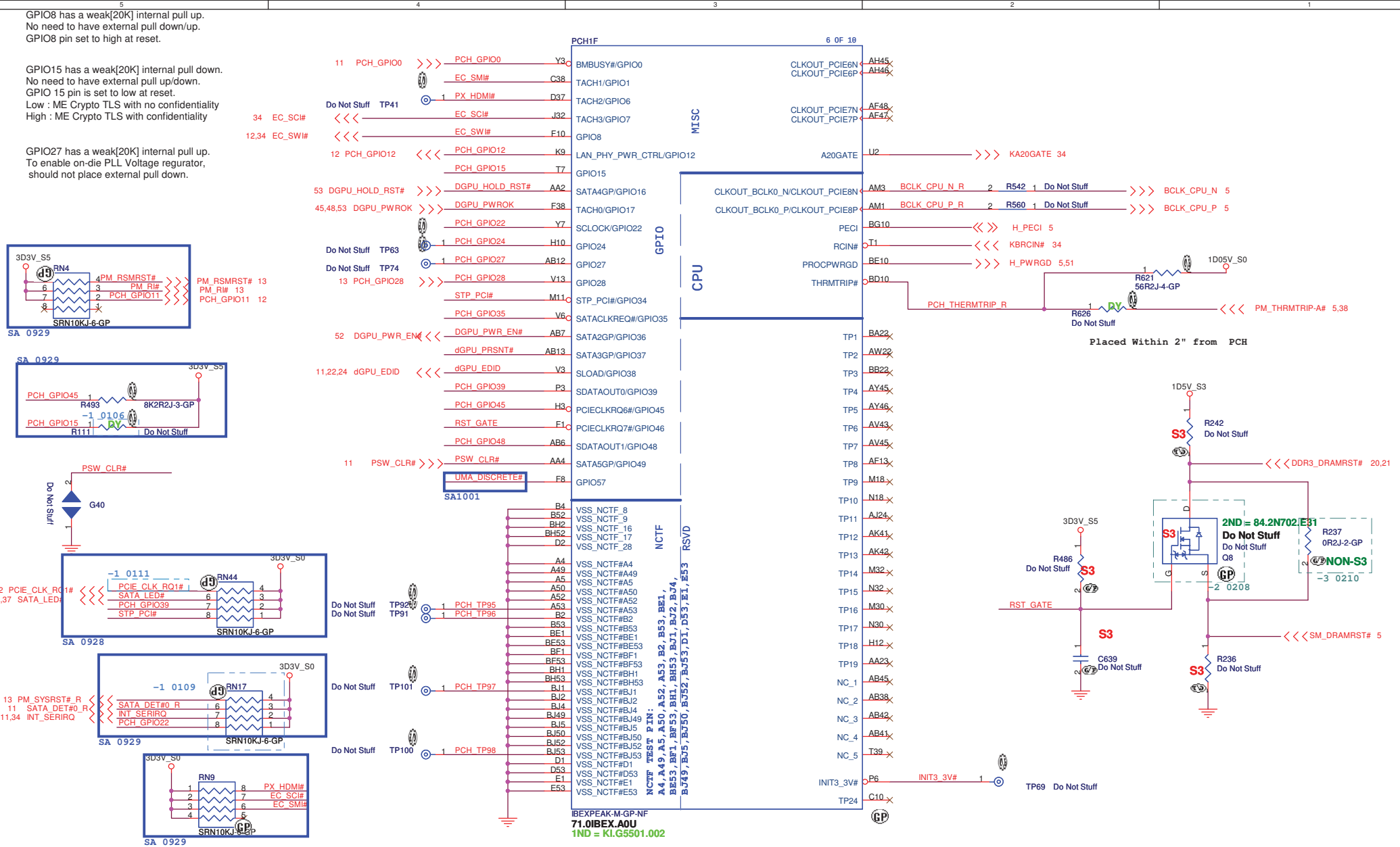
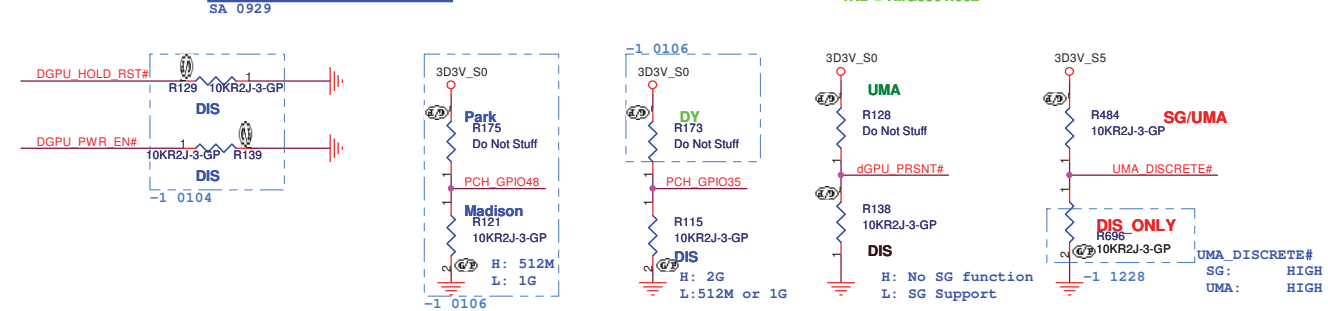
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

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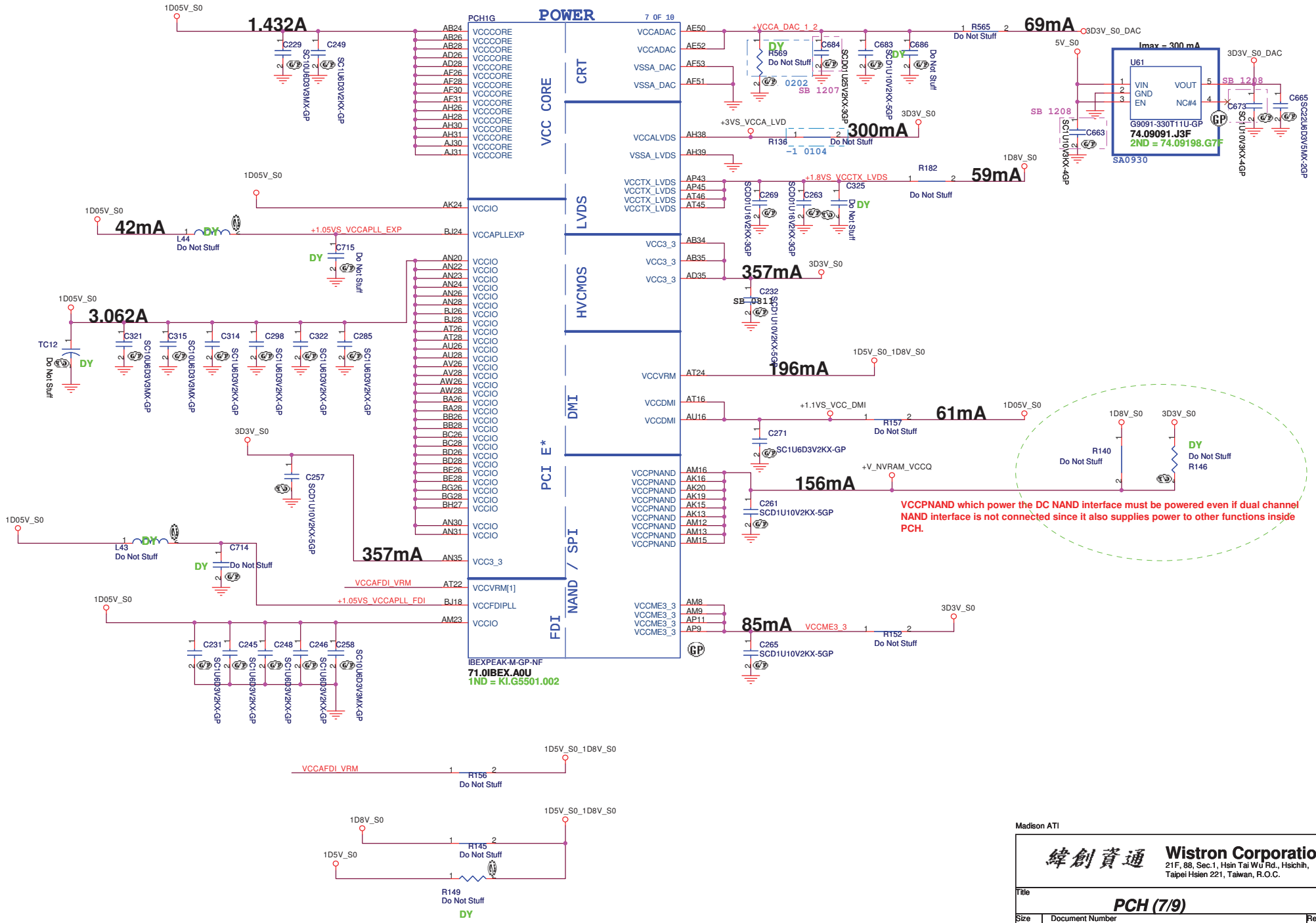
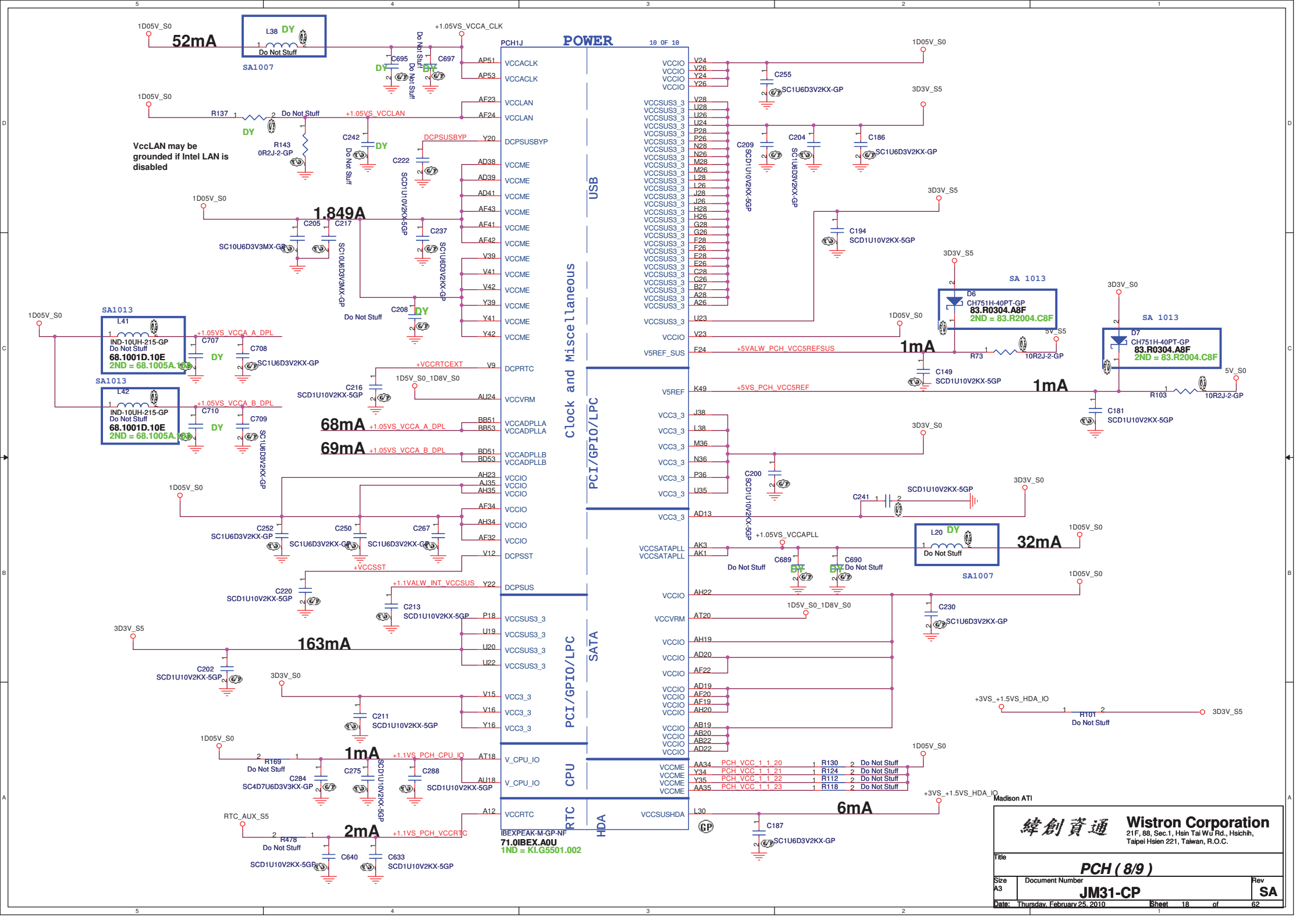
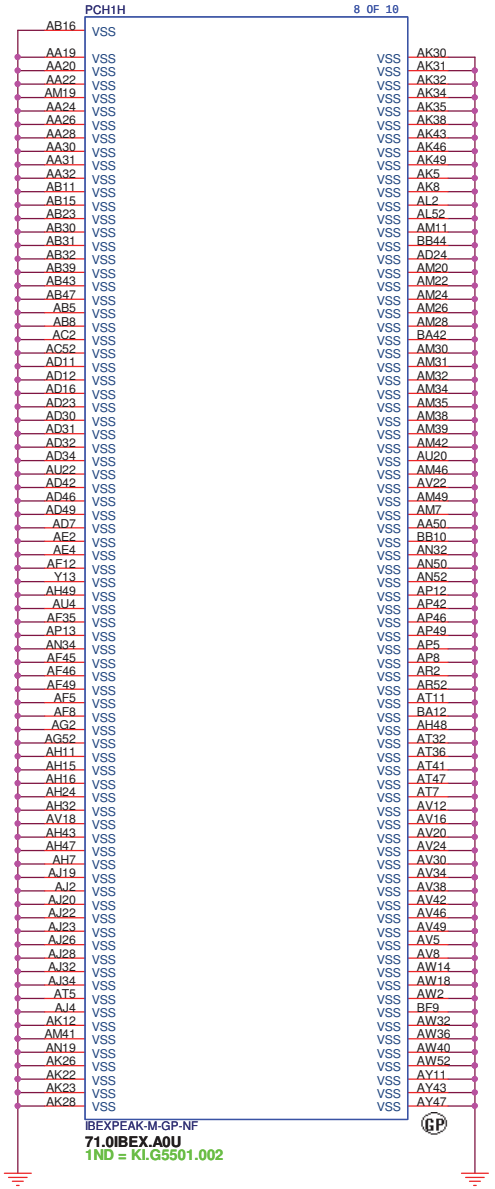
Title: PCH (6/9)

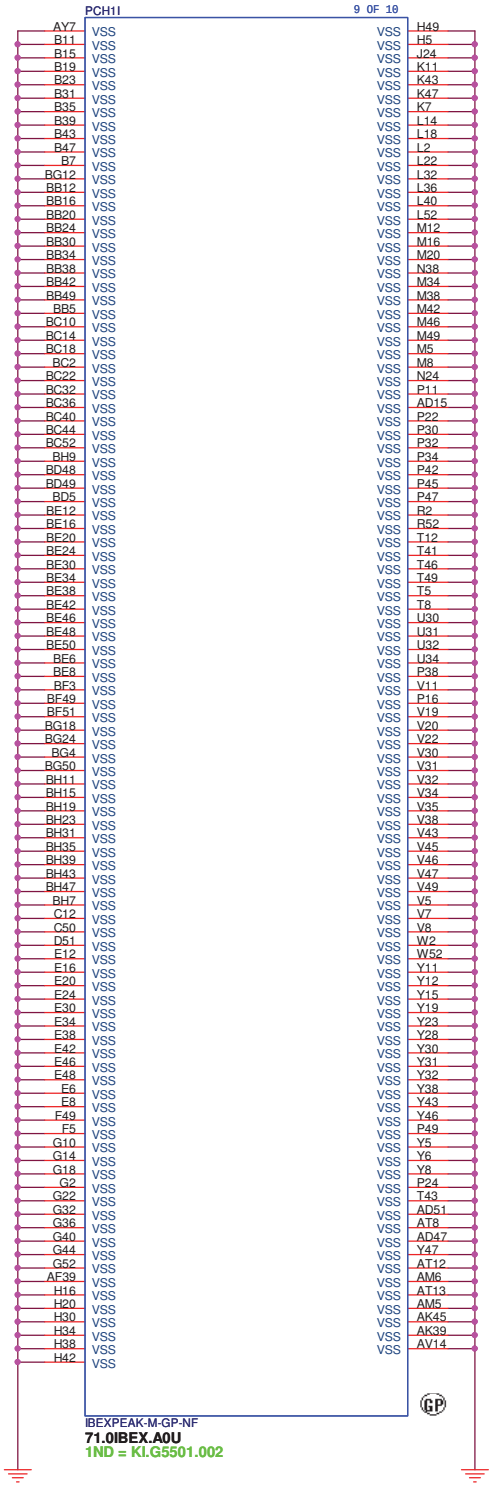
| Size | Document Number | Rev |
|---|---|---|
| A3 | JM31-CP | -1 |

Date: Thursday, February 25, 2010 Sheet 16 of 62


POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.432A
3.062A
42mA
357mA
357mA
196mA
61mA
156mA
85mA
69mA
300mA
59mA
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002
Madison ATI
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (7/9)
Size A3
Document Number
JM31-CP
Rev -1
Date: Thursday, February 25, 2010
Sheet 17 of 62


POWER
PCH1J
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
52mA
1.849A
163mA
68mA
69mA
1mA
32mA
6mA
2mA
SA1007
SA1013
VccLAN may be grounded if Intel LAN is disabled
IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison ATI
PCH ( 8/9 )
JM31-CP
Size A3
Rev SA
Date: Thursday, February 25, 2010
Sheet 18 of 62




Madison ATI

緯創資通 **Wistron Corporation**
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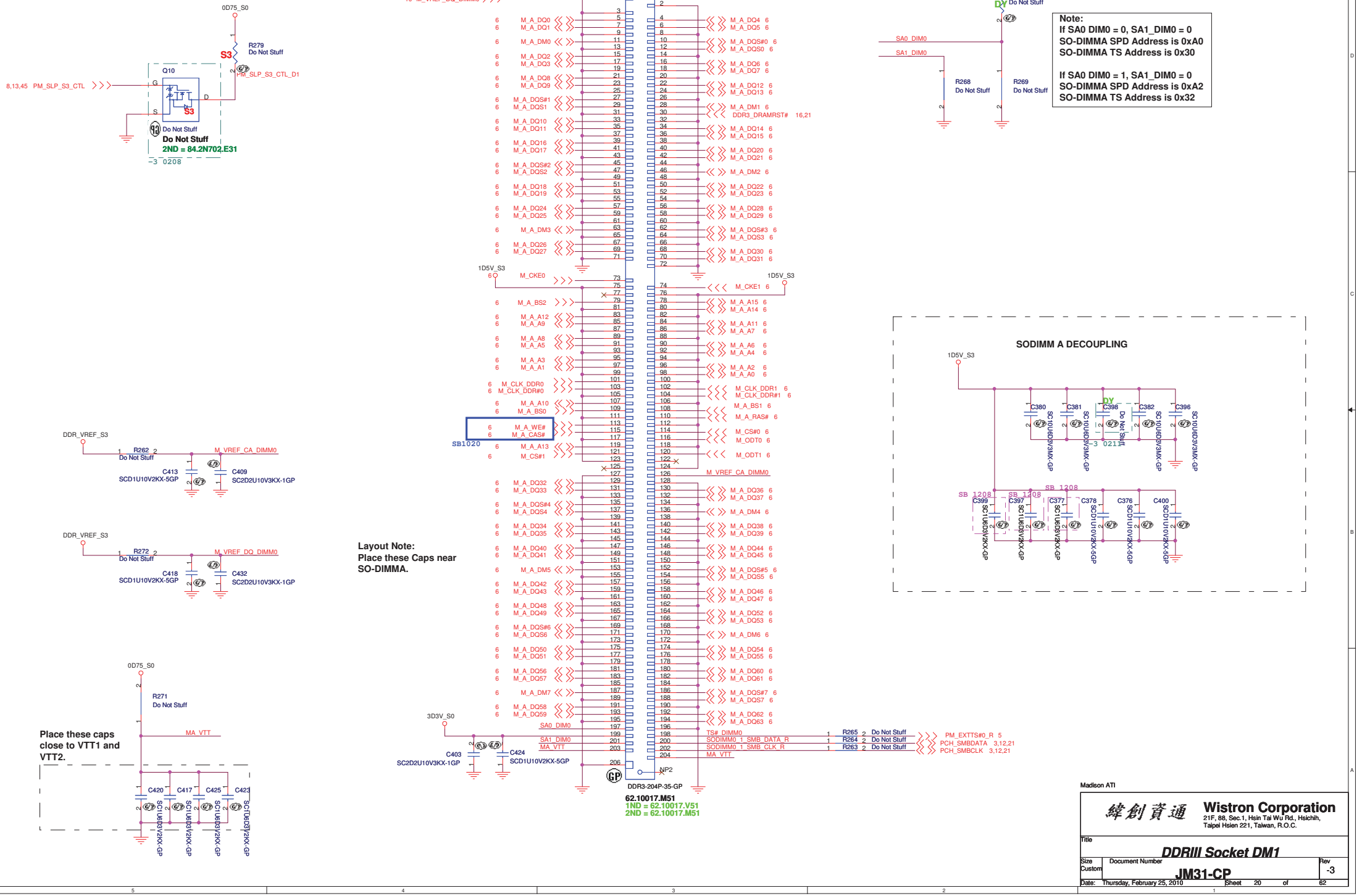
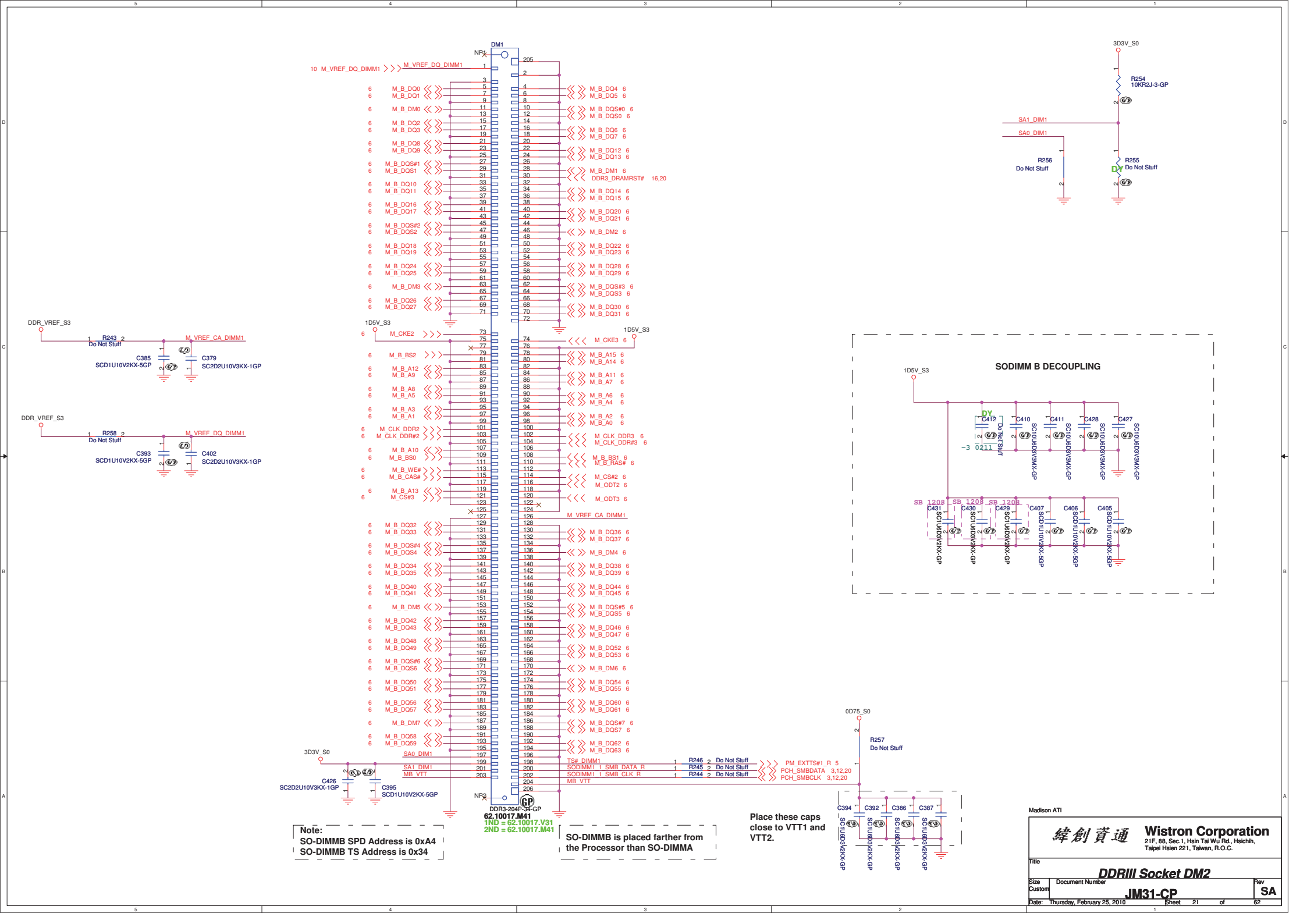
Taipei Hsien 221, Taiwan, R.O.C.

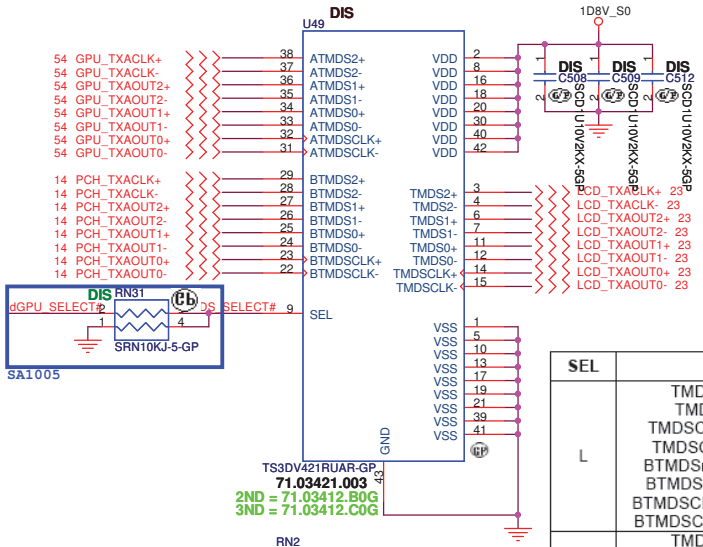
Title: ***PCH ( 9/9 )***

| Size | Document Number | Rev |
|---|---|---|
| A3 | J\M31-CP | SA |

Date: Thursday, February 25, 2010 Sheet 19 of 62


DM2
NP1
NP2
DDR3-204P-35-GP
62.10017.M51
1ND = 62.10017.V51
2ND = 62.10017.M51
M_VREF_DQ_DIMM0
M_CKE0
M_CKE1
M_A_BS2
M_A_BS1
M_A_RAS#
M_A_WE#
M_A_CAS#
M_CS#0
M_CS#1
M_ODT0
M_ODT1
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
M_VREF_CA_DIMM0
DDR3_DRAMRST# 16,21
SB1020
SA0_DIM0
SA1_DIM0
MA_VTT
TS# DIMM0
SODIMM0_1_SMB_DATA_R
SODIMM0_1_SMB_CLK_R
PM_EXTTS#0_R 5
PCH_SMBDATA 3,12,21
PCH_SMBCLK 3,12,21
3D3V_S0
1D5V_S3
0D75_S0
R270 Do Not Stuff
R268 Do Not Stuff
R269 Do Not Stuff
R265 Do Not Stuff
R264 Do Not Stuff
R263 Do Not Stuff
C403 SC2D2U10V3KX-1GP
C424 SCD1U10V2KX-5GP
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
SODIMM A DECOUPLING
C380 C381 C398 C382 C396
C399 C397 C377 C378 C376 C400
SB 1208
Layout Note:
Place these Caps near
SO-DIMMA.
Place these caps
close to VTT1 and
VTT2.
R279 Do Not Stuff
Q10
PM_SLP_S3_CTL_D1
8,13,45 PM_SLP_S3_CTL
Do Not Stuff
2ND = 84.2N702.E31
R262 Do Not Stuff
R272 Do Not Stuff
R271 Do Not Stuff
C413 SCD1U10V2KX-5GP
C409 SC2D2U10V3KX-1GP
C418 SCD1U10V2KX-5GP
C432 SC2D2U10V3KX-1GP
C420 C417 C425 C423
SC1U6D3V2KX-GP
DDR_VREF_S3
M_VREF_CA_DIMM0
M_VREF_DQ_DIMM0
Madison ATI
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRIII Socket DM1
Size Custom
Document Number
JM31-CP
Rev -3
Date: Thursday, February 25, 2010
Sheet 20 of 62


DM1
NP1
NP2
DDR3-204P-34-GP
62.10017.M41
1ND = 62.10017.V31
2ND = 62.10017.M41
M_VREF_DQ_DIMM1
M_VREF_CA_DIMM1
DDR_VREF_S3
R243 Do Not Stuff
R258 Do Not Stuff
C385 SCD1U10V2KX-5GP
C379 SC2D2U10V3KX-1GP
C393 SCD1U10V2KX-5GP
C402 SC2D2U10V3KX-1GP
1D5V_S3
M_CKE2
M_CKE3
M_B_BS2
M_B_A15
M_B_A14
M_B_A12
M_B_A9
M_B_A11
M_B_A7
M_B_A8
M_B_A5
M_B_A6
M_B_A4
M_B_A3
M_B_A1
M_B_A2
M_B_A0
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3
M_B_A10
M_B_BS0
M_B_BS1
M_B_RAS#
M_B_WE#
M_B_CAS#
M_CS#2
M_ODT2
M_B_A13
M_CS#3
M_ODT3
M_B_DQ0
M_B_DQ1
M_B_DM0
M_B_DQ2
M_B_DQ3
M_B_DQ8
M_B_DQ9
M_B_DQS#1
M_B_DQS1
M_B_DQ10
M_B_DQ11
M_B_DQ16
M_B_DQ17
M_B_DQS#2
M_B_DQS2
M_B_DQ18
M_B_DQ19
M_B_DQ24
M_B_DQ25
M_B_DM3
M_B_DQ26
M_B_DQ27
M_B_DQ4
M_B_DQ5
M_B_DQS#0
M_B_DQS0
M_B_DQ6
M_B_DQ7
M_B_DQ12
M_B_DQ13
M_B_DM1
DDR3_DRAMRST# 16,20
M_B_DQ14
M_B_DQ15
M_B_DQ20
M_B_DQ21
M_B_DM2
M_B_DQ22
M_B_DQ23
M_B_DQ28
M_B_DQ29
M_B_DQS#3
M_B_DQS3
M_B_DQ30
M_B_DQ31
M_B_DQ32
M_B_DQ33
M_B_DQS#4
M_B_DQS4
M_B_DQ34
M_B_DQ35
M_B_DQ40
M_B_DQ41
M_B_DM5
M_B_DQ42
M_B_DQ43
M_B_DQ48
M_B_DQ49
M_B_DQS#6
M_B_DQS6
M_B_DQ50
M_B_DQ51
M_B_DQ56
M_B_DQ57
M_B_DM7
M_B_DQ58
M_B_DQ59
M_B_DQ36
M_B_DQ37
M_B_DM4
M_B_DQ38
M_B_DQ39
M_B_DQ44
M_B_DQ45
M_B_DQS#5
M_B_DQS5
M_B_DQ46
M_B_DQ47
M_B_DQ52
M_B_DQ53
M_B_DM6
M_B_DQ54
M_B_DQ55
M_B_DQ60
M_B_DQ61
M_B_DQS#7
M_B_DQS7
M_B_DQ62
M_B_DQ63
SA0_DIM1
SA1_DIM1
MB_VTT
TS#_DIMM1
SODIMM1_1_SMB_DATA_R
SODIMM1_1_SMB_CLK_R
R246 Do Not Stuff
R245 Do Not Stuff
R244 Do Not Stuff
PM_EXTTS#1_R 5
PCH_SMBDATA 3,12,20
PCH_SMBCLK 3,12,20
3D3V_S0
C426 SC2D2U10V3KX-1GP
C395 SCD1U10V2KX-5GP
0D75_S0
R257 Do Not Stuff
C394 C392 C386 C387
SC1U603V2KX-GP
R254 10KR2J-3-GP
R256 Do Not Stuff
R255 Do Not Stuff
DY
SODIMM B DECOUPLING
C412 Do Not Stuff
C410 C411 C428 C427
SC10U6D3V3MX-GP
SB 1208
C431 C430 C429 C407 C406 C405
SC1U6D3V2KX-GP
SC10U10V2KX-5GP
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA
Place these caps close to VTT1 and VTT2.
Madison ATI
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRIII Socket DM2
Size Custom
Document Number
JM31-CP
Rev SA
Date: Thursday, February 25, 2010
Sheet 21 of 62



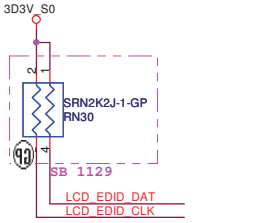

## FUNCTION TABLE

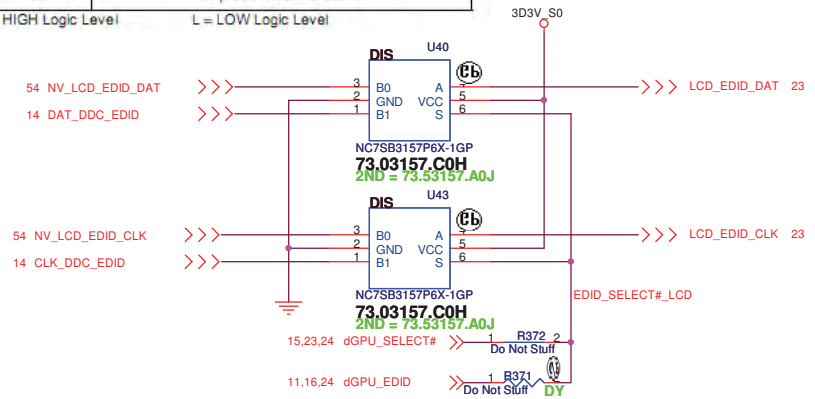
| SEL | FUNCTION | OUTPUT |
|---|---|---|
| L | TMDSn+ = ATMDSn+<br>TMDSn- = ATMDSn-<br>TMDSCLK+ = ATMDSCLK+<br>TMDSCLK- = ATMDSCLK-<br>BTMDSn+ = High Impedance<br>BTMDSn- = High Impedance<br>BTMDSCLK+ = High Impedance<br>BTMDSCLK- = High Impedance | TMDSn+<br>TMDSn-<br>TMDSCLK+<br>TMDSCLK- |
| H | TMDSn+ = BTMDSn+<br>TMDSn- = BTMDSn-<br>TMDSCLK+ = BTMDSCLK+<br>TMDSCLK- = BTMDSCLK-<br>ATMDSn+ = High Impedance<br>ATMDSn- = High Impedance<br>ATMDSCLK+ = High Impedance<br>ATMDSCLK- = High Impedance | TMDSn+<br>TMDSn-<br>TMDSCLK+<br>TMDSCLK- |

## Function Table

| Input (S) | Function |
|---|---|
| L | $B_0$ Connected to A |
| H | $B_1$ Connected to A |

H = HIGH Logic Level L = LOW Logic Level

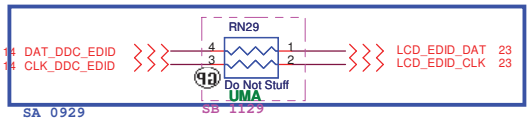


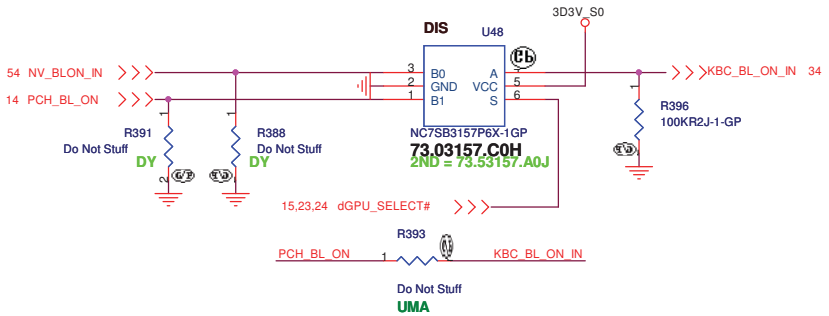



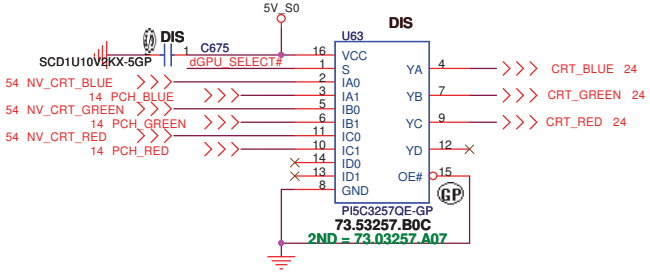

## Function Table

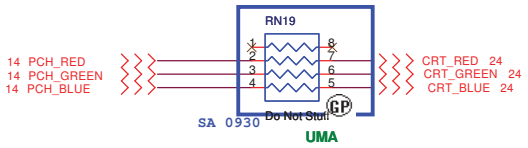
| Input (S) | Function |
|---|---|
| L | $B_0$ Connected to A |
| H | $B_1$ Connected to A |

H = HIGH Logic Level L = LOW Logic Level




| $\overline{E}$ | S | YA | YB | YC | YD | Function |
|---|---|---|---|---|---|---|
| H | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Disable |
| L | L | IA0 | IB0 | IC0 | ID0 | S = 0 |
| L | H | IA1 | IB1 | IC1 | ID1 | S = 1 |

Madison ATI

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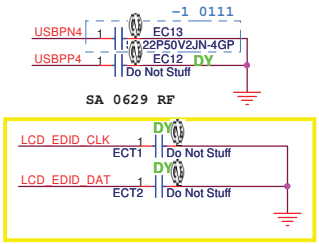
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PX SWITCH**

Size: A3 | Document Number: **JM31-CP** | Rev: **SB**

Date: Thursday, February 25, 2010 | Sheet 22 of 62

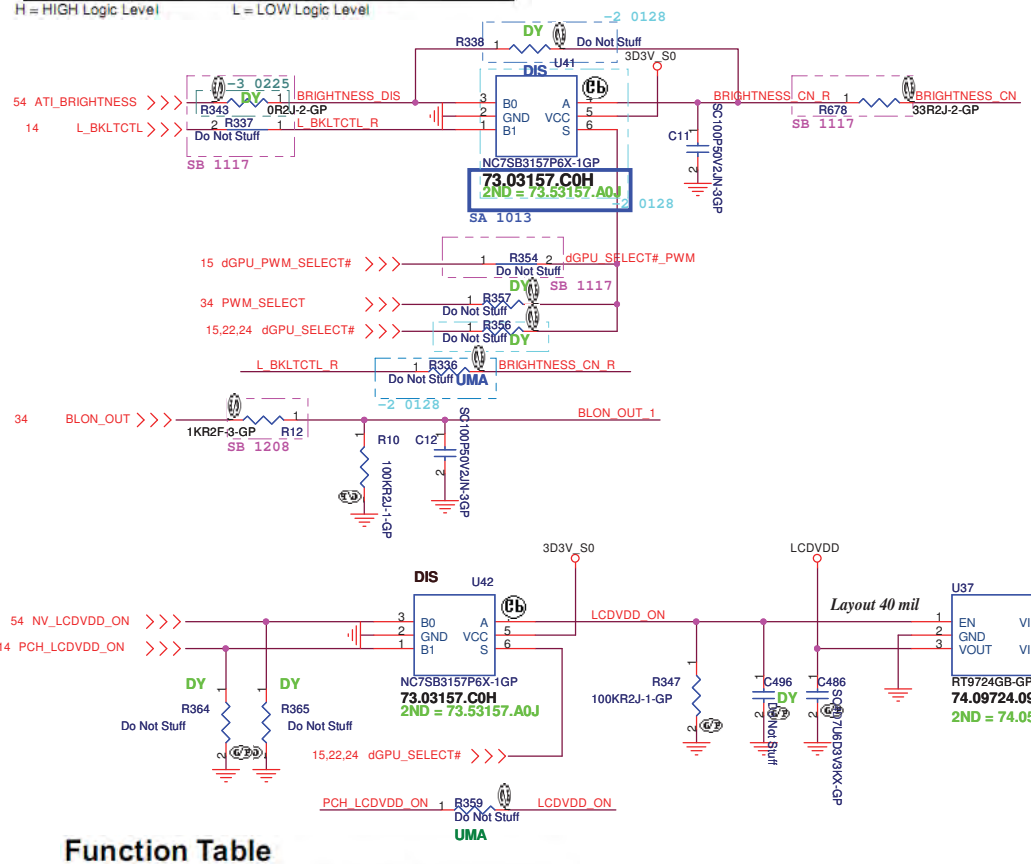
# LCD/INVERTER/CCD CONN




## Function Table

| Input (S) | Function |
|---|---|
| L | $B_0$ Connected to A |
| H | $B_1$ Connected to A |

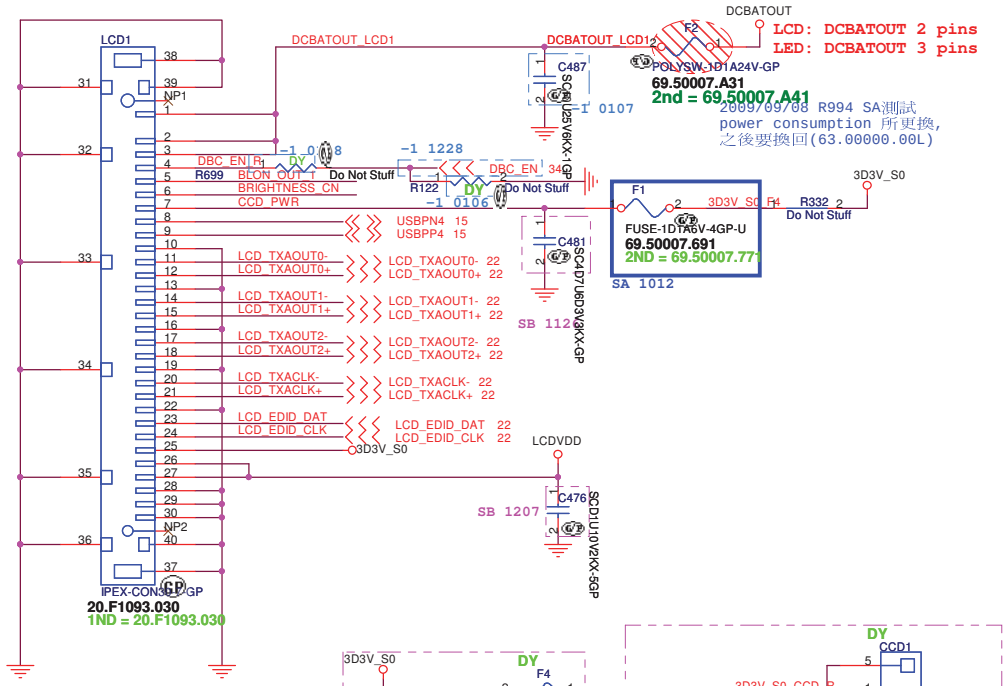
H = HIGH Logic Level  L = LOW Logic Level

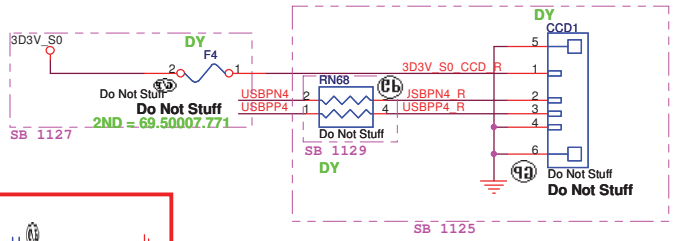


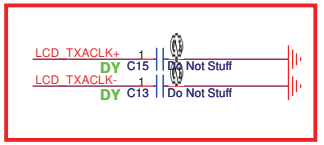

## Function Table

| Input (S) | Function |
|---|---|
| L | $B_0$ Connected to A |
| H | $B_1$ Connected to A |

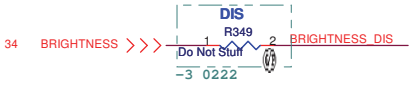
H = HIGH Logic Level  L = LOW Logic Level




modify by RF




Reserve direct connector to KBC

Madison ATI

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN**

| Size | Document Number | Rev |
|---|---|---|
| A3 | JM31-CP | -1 |

Date: Thursday, February 25, 2010  Sheet 23 of 62

Layout Note:
Place these resistors close to the CRT-out connector

22 CRT_RED
22 CRT_GREEN
22 CRT_BLUE

L30 Ferrite bead impedance: 10 ohm@100MHz
FCB1608CF-GP
68.00230.021
L31
FCB1608CF-GP
68.00230.021
L33
FCB1608CF-GP
68.00230.021

CRT_R
CRT_G
CRT_B

RN41
SRN150F-1-GP
SA 0928

C642 Do Not Stuff DY
C645 Do Not Stuff DY
C657 Do Not Stuff DY
C643 SC6D8P50V2DN-GP
C648 SC6D8P50V2DN-GP
C660 SC6D8P50V2DN-GP

*Layout Note:*
** Must be a ground return path between this ground and the ground on the VGA connector.*
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.*

# CRT I/F & CONNECTOR

Do Not Stuff
C659 BY
C664 BY
C668 BY
C672 BY
Do Not Stuff
Do Not Stuff
SA 0929
Do Not Stuff

DAT_DDC1_5
CRT_HSYNC1
CRT_VSYNC1
CLK_DDC1_5

5V_CRT_S0
C681 SCD01U16V2KX-3GP

-1 0113
CRT1
D-SUB-15-45-GP-U
20.20863.015
1ND = 20.20863.015

VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
NC#4
NC#11
GND

DAT_DDC1_5
CLK_DDC1_5
CRT_R
CRT_G
CRT_B
CRT_VSYNC1
CRT_HSYNC1
CRT_IN#_R

34 CRT_DEC#
R568 470R2J-2-GP
SC100P50V2JN-3GP
C682
CRT_IN#_R
D24 DY
Do Not Stuff
5V_S0

6 1 7 2 8 3 9 4 10 5

## Hsync & Vsync level shift

L=>B0 -DIS
H=>B1 -UMA

15,22,23 dGPU_SELECT#
54,57 NV_CRT_HSYNC
54,57 NV_CRT_VSYNC
14 PCH_HSYNC
14 PCH_VSYNC

For DIS CRT
For UMA CRT

U59 DIS
U60
1OE# 1A 2Y GND VCC 2OE# 1Y 2A
SSLVC2G125DP-1GP
73.2G125.A07
2ND = 73.2G125.007

5V_S0
3D3V_S0
DIS R635 10KR2J-3-GP
dGPU_SELECT
DIS Q31 2N7002-7F-GP
84.27002.N31
2ND = 84.27002.W31
SB 1210

CRT_VSYNC1_1 R533 10R2J-2-GP CRT_VSYNC1
CRT_HSYNC1_1 R528 10R2J-2-GP CRT_HSYNC1

R339 Do Not Stuff UMA
1 0104

## DDC_CLK & DATA level shift

5V_CRT_S0
5V_S0
3D3V_S0
F3 FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771
5V_CRT_DDC
D22 RB551V-30-2GP
83.5R003.08F
2ND = 83.R5003.C8F
500mA
RN51 SRN2K2J-1-GP
R673 Do Not Stuff
RN49 SRN10KJ-5-GP
3D3V_S0_DDC

54 NV_CRT_DDCDATA
14 PCH_DDCDATA
54 NV_CRT_DDCCLK
14 PCH_DDCCLK

DIS U65
DIS U66
B0 GND B1 A VCC S
NC7SB3157P6X-1GP
73.03157.C0H
2ND = 73.53157.A0H
SA 1013

DDCDATA
DDCCLK
Q29 2N7002EDW-GP
84.27002.F3F
2ND = 84.DMN66.03F
DAT_DDC1_5
CLK_DDC1_5
dGPU_SELECT#_DDC

15,22,23 dGPU_SELECT#
L=>B0 -DIS
H=>B1 -UMA
R601 Do Not Stuff
SB 1117
11,16,22 dGPU_EDID
R611 Do Not Stuff DY

RN56
14 PCH_DDCDATA
14 PCH_DDCCLK
DDCDATA
DDCCLK
Do Not Stuff
UMA

Madison ATI

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT CONN
Size: A3
Document Number: JM31-CP
Rev: SB
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# Close HDMI1

SB 1209

HDMI1
SKT-HDMI23-1-GP
22.10296.181
1ND = 22.10296.181
2ND = 22.10296.211
-1 0111

HDMI_TX2+ / HDMI_TX2-
HDMI_TX1+ / HDMI_TX1-
HDMI_TX0+ / HDMI_TX0-
HDMI_TXC+ / HDMI_TXC-
HDMI_A_CEC
TP83 Do Not Stuff
TDMS_A_CLK
TDMS_A_DAT
5V_HDMI
HDMI_A_HPD_CN
R637 10KR2J-3-GP -1 0105
R629 100KR2J-1-GP
-2 0127

D26
HDMI_A_HPD_CN
5V_S0
DY
Do Not Stuff

3D3V_S0
RN57
Do Not Stuff
UMA
Do Not Stuff
14 PCH_HDMI_CLK
14 PCH_HDMI_DATA

5V_HDMI
-3 0210
F5
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771
R703 DY Do Not Stuff
-2 0127
-3 0210

RN61
SRN2K2J-1-GP
66.22236.04L
TDMS_A_CLK_R
TDMS_A_DAT_R
D25
BAW56-5-GP
83.00056.Q11
2ND = 83.00056.G11
EC84 DY
EC85 DY
Do Not Stuff

3D3V_VGA
RN25 DY Do Not Stuff
54 NV_HDMI_CLK
54 NV_HDMI_DATA
PCH_HDMI_DATA
PCH_HDMI_CLK
RN71 -1 0105 Do Not Stuff UMA
U20 DY
1OE# VCC
1A 2OE#
1B 2B
GND 2A
5V_S0
TDMS_A_CLK
TDMS_A_DAT
Do Not Stuff
Do Not Stuff
2ND = 73.03306.D0B

SA1001
54 NV_HDMI_CLK
54 NV_HDMI_DATA
3D3V_HDMI
SB 1125
Q7 UMA
TDMS_A_CLK
TDMS_A_DAT
Do Not Stuff
Do Not Stuff
2ND = 84.DMN66.03F
SA1001

From VGA on board
54 NV_HDMI_DATA0-
54 NV_HDMI_DATA0+
54 NV_HDMI_DATA1-
54 NV_HDMI_DATA1+
54 NV_HDMI_DATA2-
54 NV_HDMI_DATA2+
54 NV_HDMI_CLK-
54 NV_HDMI_CLK+
DIS C342 DIS C340 DIS C328 DIS C324 DIS C317 DIS C313 DIS C335 DIS C332
SCD1U10V2KX-5GP
HDMI_TX0- HDMI_TX0+ HDMI_TX1- HDMI_TX1+ HDMI_TX2- HDMI_TX2+ HDMI_TXC- HDMI_TXC+
SB 1207

3D3V_S0
C717 DY C713 DY C705 DY C711 DY
Do Not Stuff
R634 DY R633 DY
SB 1130

From PCH
SA 1002
14 PCH_HDMI_DATA0-
14 PCH_HDMI_DATA0+
14 PCH_HDMI_CLK-
14 PCH_HDMI_CLK+
14 PCH_HDMI_DATA1-
14 PCH_HDMI_DATA1+
14 PCH_HDMI_DATA2-
14 PCH_HDMI_DATA2+

U67
VCC GND
NC#35 NC#34
IN_D1- IN_D1+ IN_D2- IN_D2+ IN_D3- IN_D3+ IN_D4- IN_D4+
OUT_D1- OUT_D1+ OUT_D2- OUT_D2+ OUT_D3- OUT_D3+ OUT_D4- OUT_D4+
HDMI_TX0- HDMI_TX0+ HDMI_TXC- HDMI_TXC+ HDMI_TX1- HDMI_TX1+ HDMI_TX2- HDMI_TX2+
PC0 PC1
REXT RT_EN# OE# DDC_EN
SDA SCL HPD
PCH_HDMI_DATA PCH_HDMI_CLK PCH_HDMI_DETECT
HPD_SINK SDA_SINK SCL_SINK
HDMI_A_HPD_CN TDMS_A_DAT TDMS_A_CLK
Do Not Stuff DY
Do Not Stuff

Recommended Equalization: [PC1,PC0]=01, 4dB
SB 1130
3D3V_S0
R607 DY Do Not Stuff PC0
R606 DY Do Not Stuff PC1
R605 DY Do Not Stuff
REXT_HDMI
PS8101_RT_EN#
OE#_PS8101
DDC_EN_PS8101

SRN0J-6-GP DIS
RN23
SB 1119
PCH_HDMI_DETECT 14
R603 Do Not Stuff DY
R628 Do Not Stuff DY
OE#_PS8101

SB 1125
3D3V_S0 3D3V_VGA
R180 0R2J-2-GP
R179 Do Not Stuff DY
3D3V_HDMI
SB 1210
Q22 2N7002-7F-GP 84.27002.N31 2ND = 84.27002.W31
NV_HDMI_DETECT
34,54 HPD1
PCH_HDMI_DETECT
R178 UMA Do Not Stuff
R524 10KR2J-3-GP -1 0105
SB 1125

HDMI_TX0- HDMI_TX0+ R627 R625
HDMI_TX1- HDMI_TX1+ R619 R617
HDMI_TX2- HDMI_TX2+ R615 R613
HDMI_TXC- HDMI_TXC+ R624 R620
562R2F-GP
DIS 64.49905.6DL/ UMA:64.56205.6DL
SB 1202

Q5 2N7002-7F-GP 84.27002.N31 2ND = 84.27002.W31
SB 1210
3D3V_S0
R201 DY Do Not Stuff
SA 0929

REXT_HDMI
PS8101_RT_EN#
R604 Do Not Stuff DY
R602 Do Not Stuff DY
SB 1202

3D3V_S0
SB 1202
R632 Do Not Stuff DY
DDC_EN_PS8101

PCH_HDMI_CLK- UMA C339 Do Not Stuff HDMI_TXC-
PCH_HDMI_CLK+ UMA C334 Do Not Stuff HDMI_TXC+
PCH_HDMI_DATA0- UMA C344 Do Not Stuff HDMI_TX0-
PCH_HDMI_DATA0+ UMA C341 Do Not Stuff HDMI_TX0+
PCH_HDMI_DATA1- UMA C327 Do Not Stuff HDMI_TX1-
PCH_HDMI_DATA1+ UMA C323 Do Not Stuff HDMI_TX1+
PCH_HDMI_DATA2- UMA C316 Do Not Stuff HDMI_TX2-
PCH_HDMI_DATA2+ UMA C312 Do Not Stuff HDMI_TX2+
SA1001 SB 1207

HDMI_A_HPD_CN
Q36 Do Not Stuff
Do Not Stuff
2ND = 84.27002.W31
DY
SB 1210
DY R631 Do Not Stuff
SB 1207

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Title: HDMI CONNECTOR
Size: A3
Document Number: JM31-CP
Rev: -1
Date: Thursday, February 25, 2010
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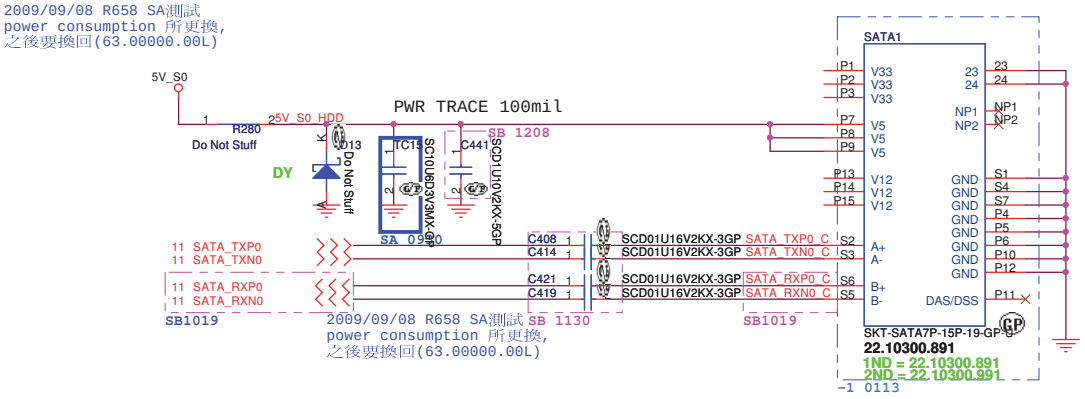
# SATA Connector

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Title: ***HDD CONN***

| Size | Document Number | Rev |
|---|---|---|
| A3 | JM31-CP | -1 |

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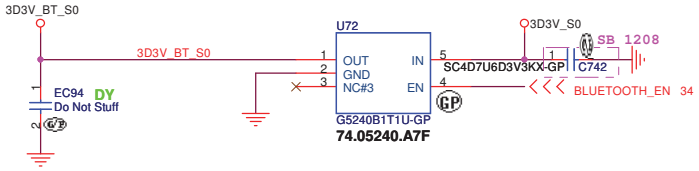
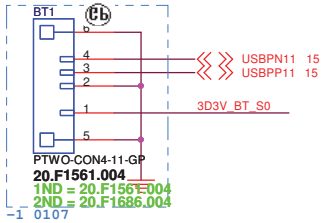
# BLUETOOTH MODULE




EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

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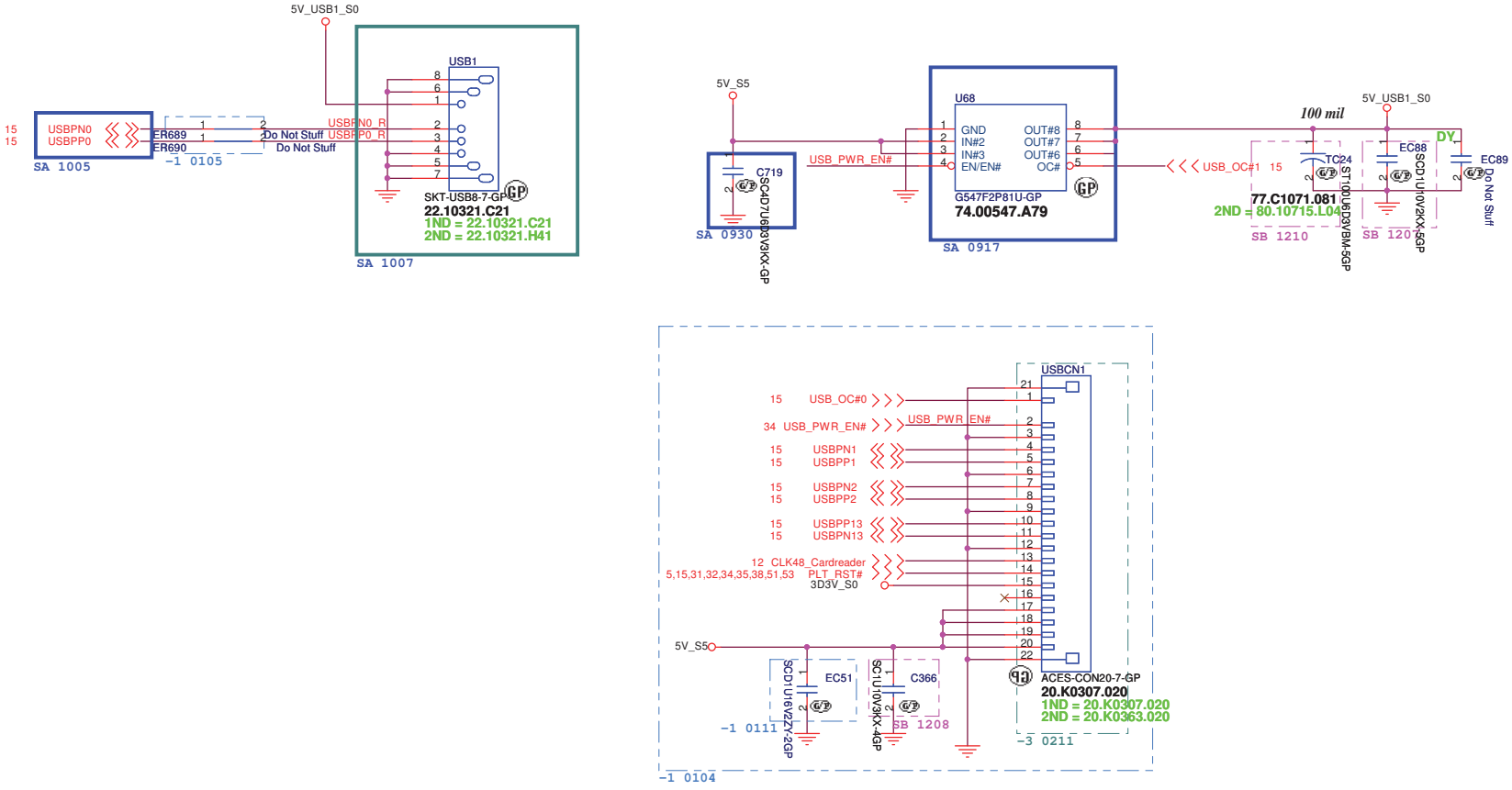
| | | |
|---|---|---|
| Title: ***BLUETOOTH*** | | |
| Size: A3 | Document Number: **JM31-CP** | Rev: -1 |
| Date: Thursday, February 25, 2010 | Sheet 27 of 62 | |

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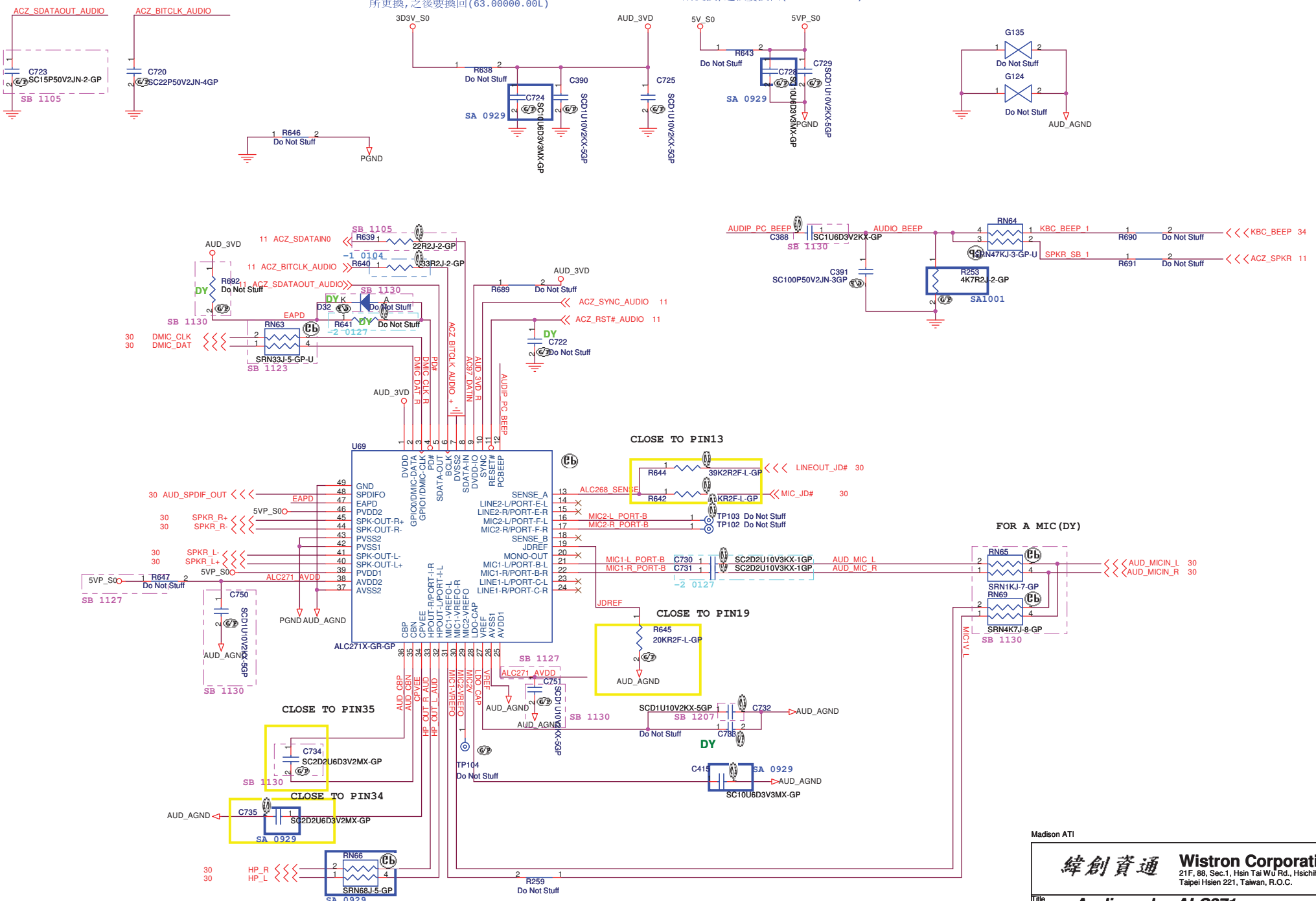
| Title | | |
|---|---|---|
| *USB CONN* | | |
| Size: A3 | Document Number: JM31-CP | Rev: -3 |
| Date: Thursday, February 25, 2010 | Sheet 28 of 62 | |

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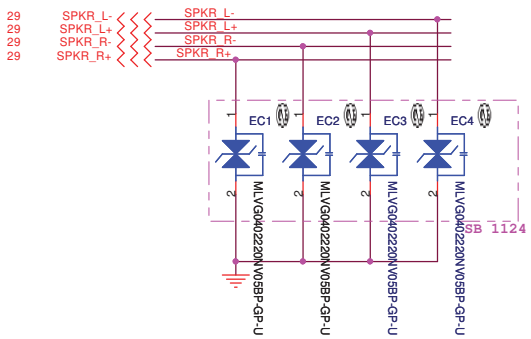
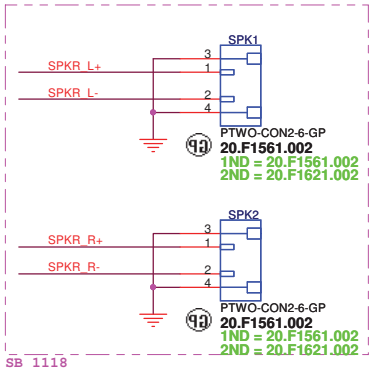
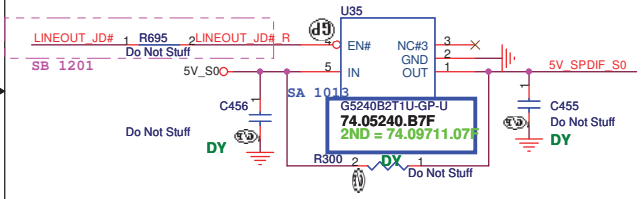
| | | |
|---|---|---|
| Title | Azalia codec ALC271 | |
| Size: A3 | Document Number: JM31-CP | Rev: SB |
| Date: Thursday, February 25, 2010 | Sheet 29 of 62 | |

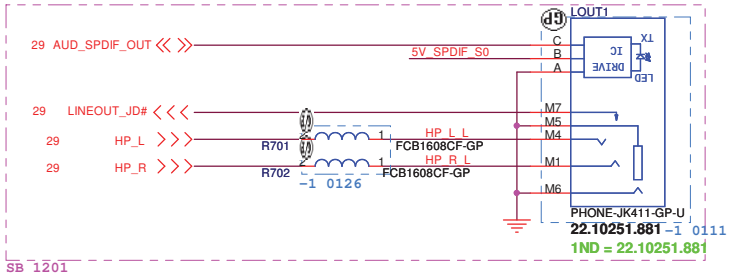
# Internal Speaker

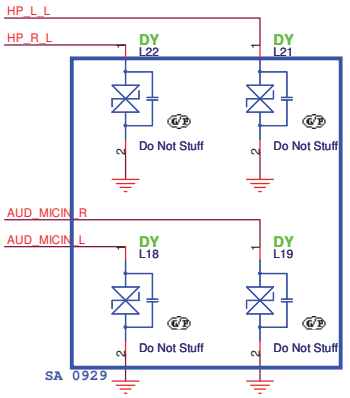


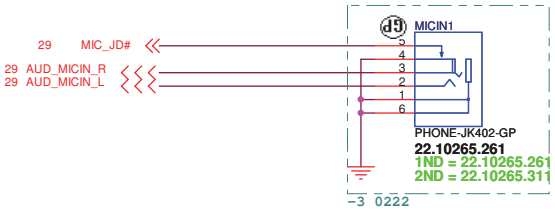

# LINE OUT

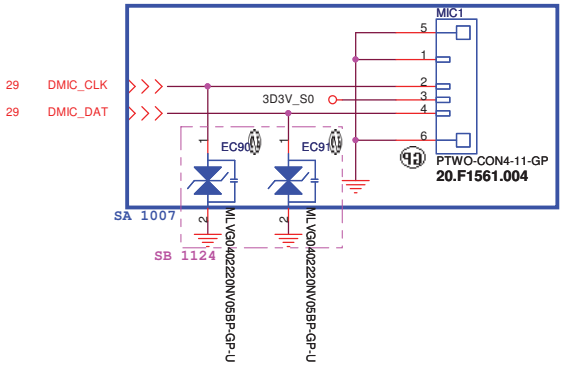



# MIC IN

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| | | |
|---|---|---|
| Title | AUDIO jack | |
| Size A3 | Document Number JM31-CP | Rev -1 |
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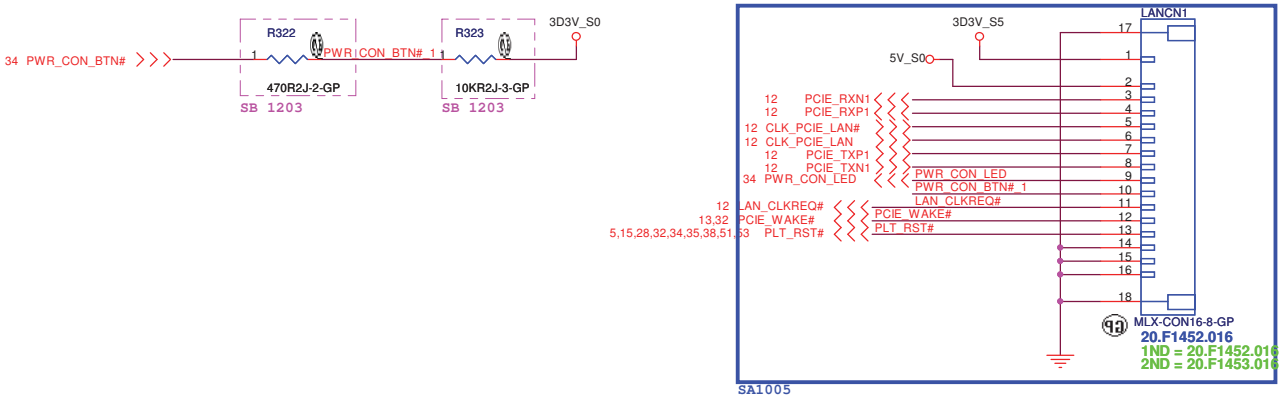


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Title: ***LAN CONN***

| Size | Document Number | Rev |
|---|---|---|
| A3 | JM31-CP | SB |

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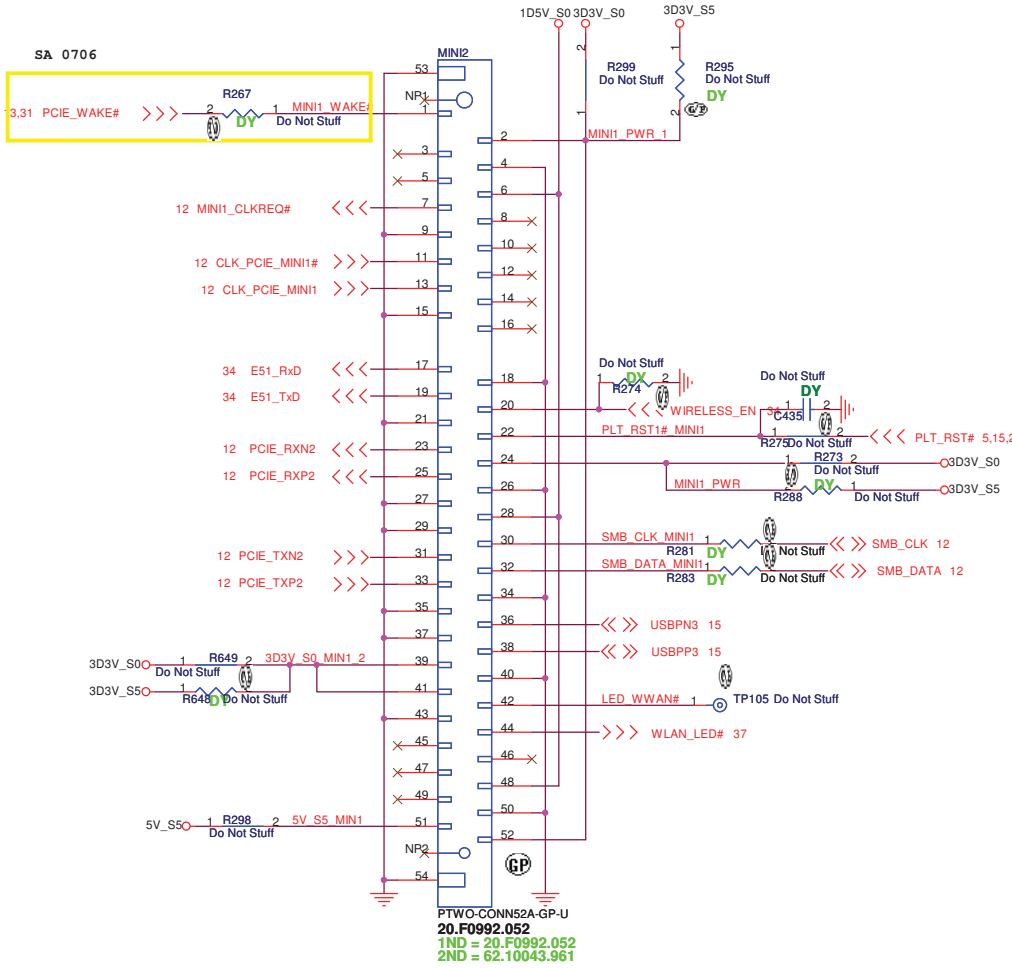
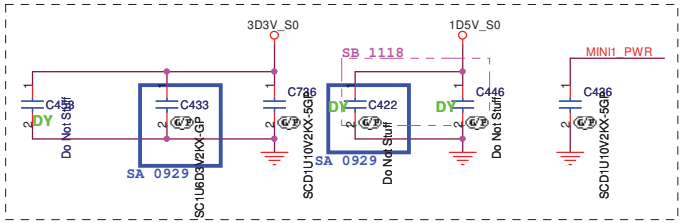
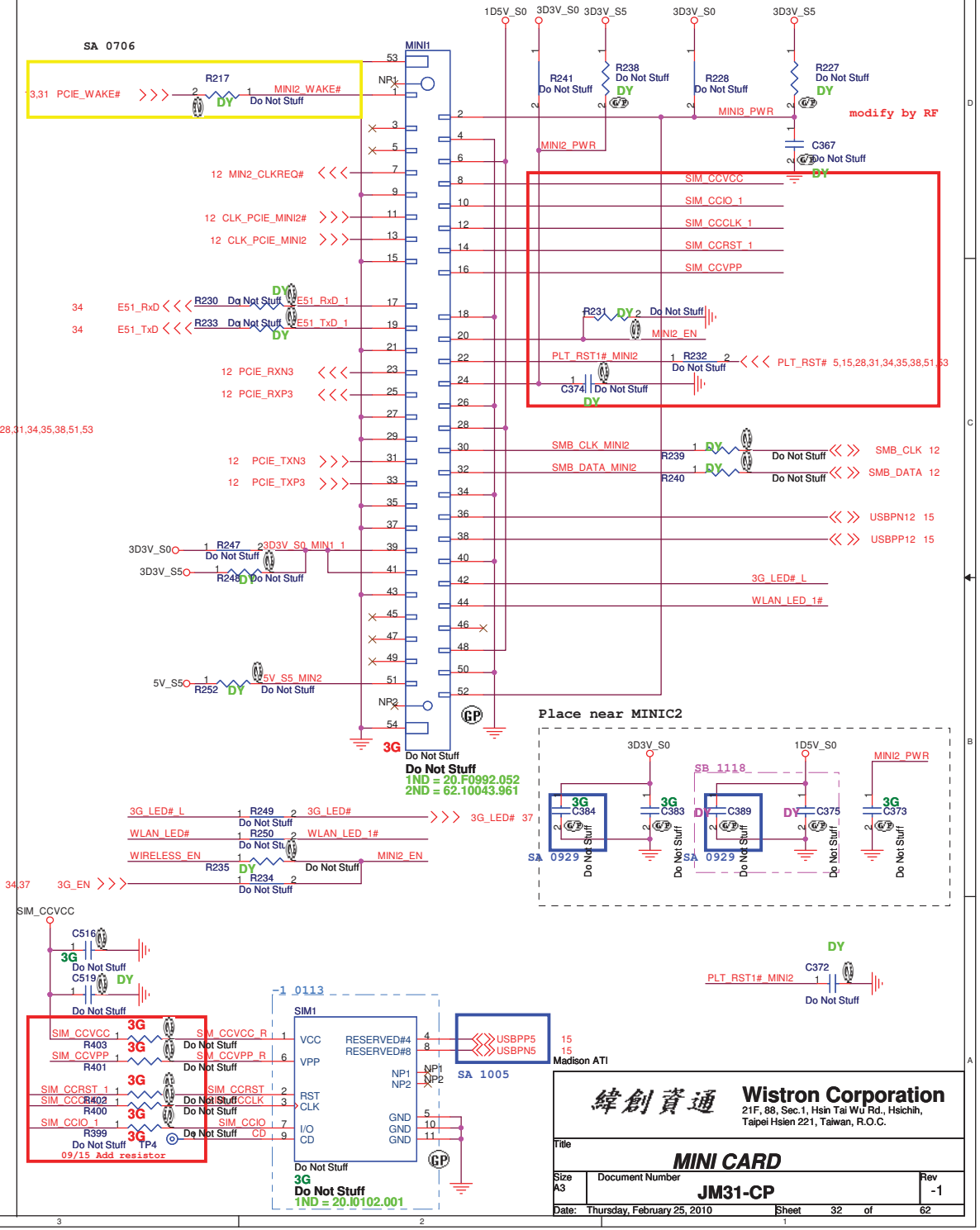
# Mini Card Connector(WLAN)
# Support debug-card




Place near MINI1




# Mini Card Connector(Robson2 and 3G)




| | |
|---|---|
| Wistron Corporation | 緯創資通 |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title: MINI CARD | |
| Size: A3 | Document Number: JM31-CP |
| Rev: -1 | |
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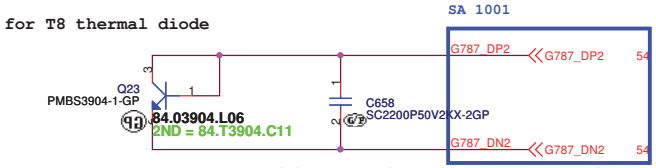
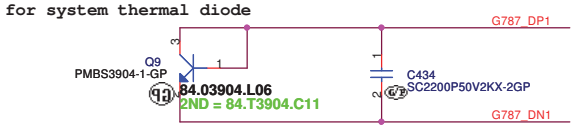
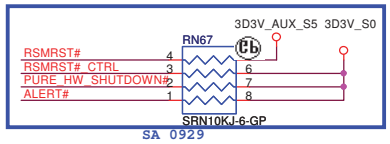
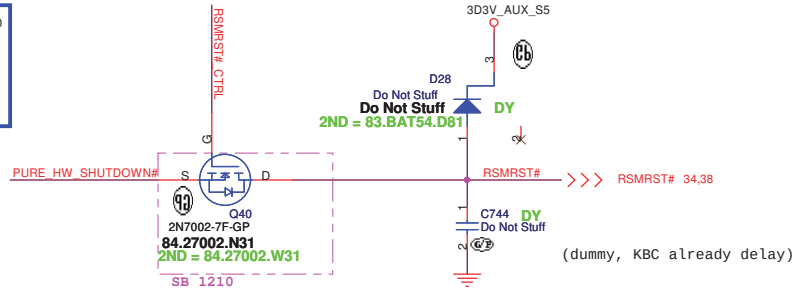
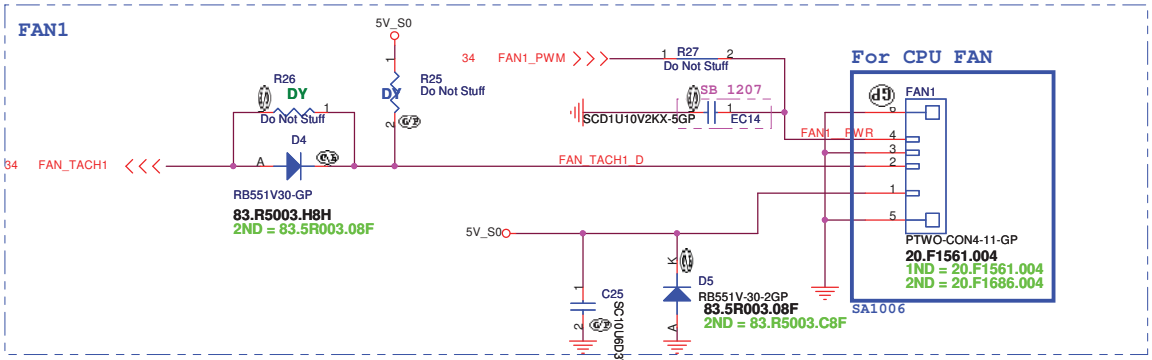


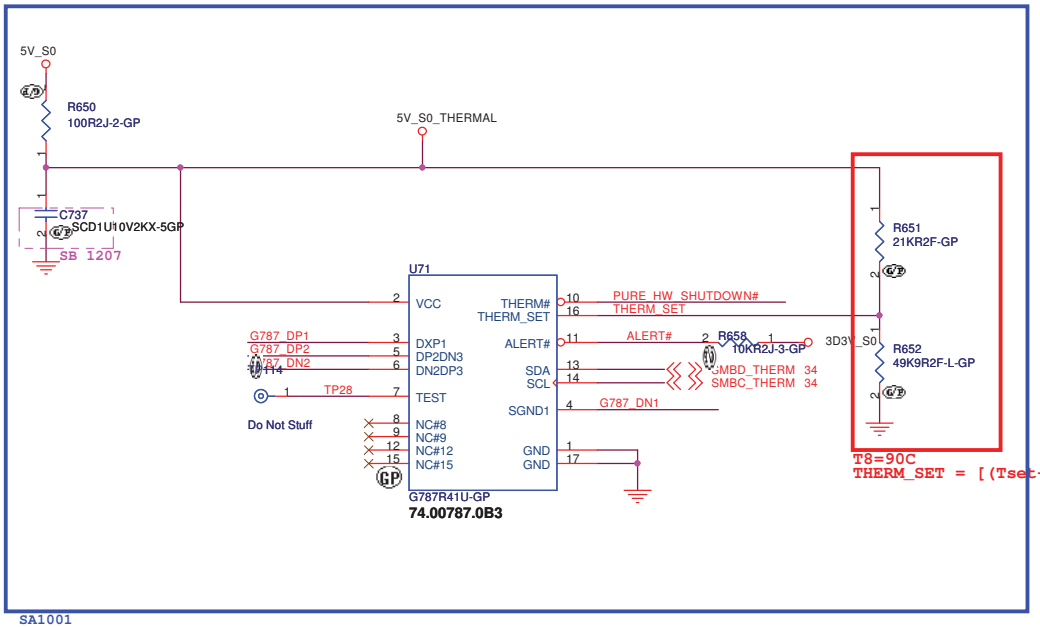

C82 & C561 CLOSE TO G787

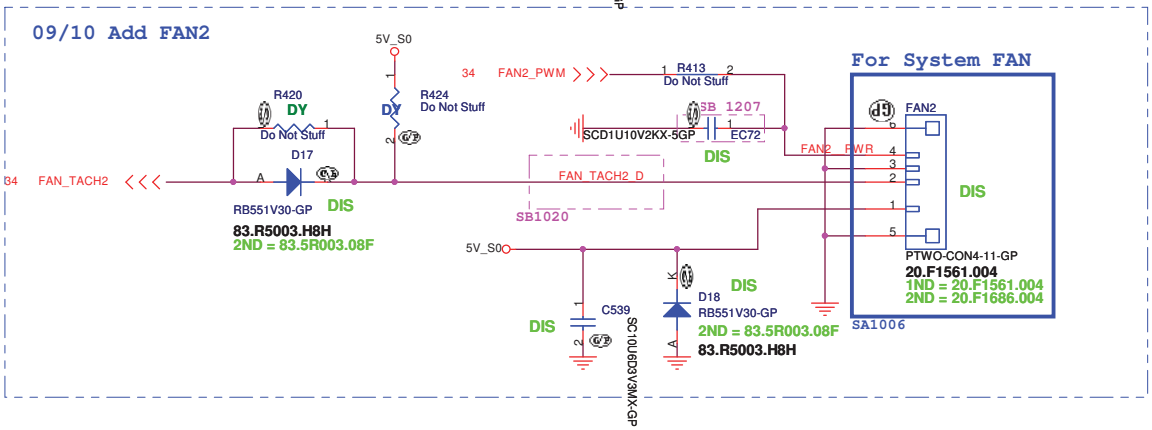
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Title: *Thermal/Fan Connector*

| Size | Document Number | Rev |
|---|---|---|
| A3 | JM31-CP | SB |

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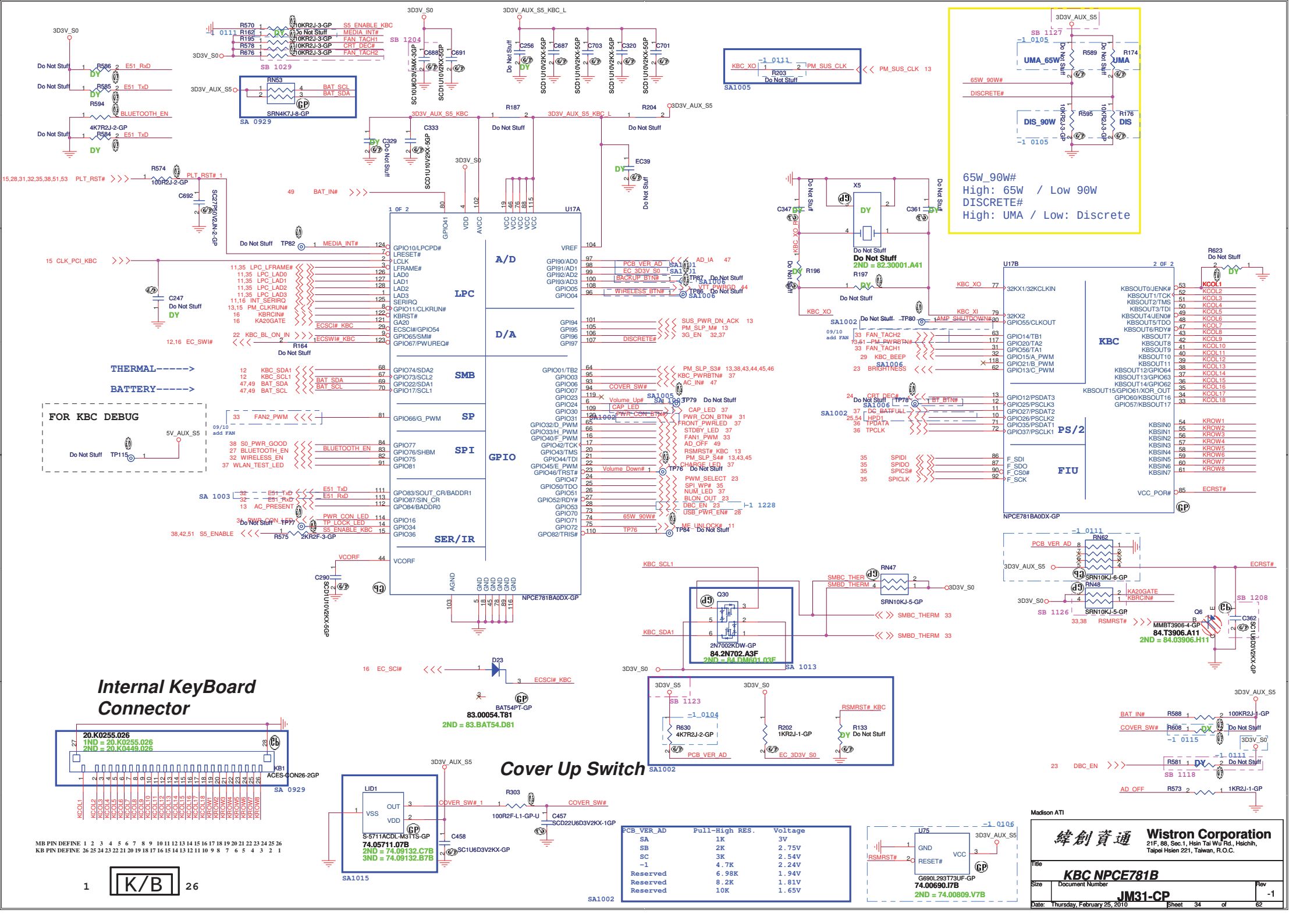
65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete
U17A
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
U17B
KBC
PS/2
FIU
NPCE781BA0DX-GP
FOR KBC DEBUG
THERMAL----->
BATTERY----->
Internal KeyBoard Connector
Cover Up Switch
20.K0255.026
1ND = 20.K0255.026
2ND = 20.K0449.026
KB1
ACES-CON26-2GP
SA 0929
74.05711.07B
2ND = 74.09132.C7B
3ND = 74.09132.B7B
SA1015
MB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
KB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
PCB_VER_AD Pull-High RES. Voltage
SA 1K 3V
SB 2K 2.75V
SC 3K 2.54V
-1 4.7K 2.24V
Reserved 6.98K 1.94V
Reserved 8.2K 1.81V
Reserved 10K 1.65V
SA1002
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緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC NPCE781B
Size
Document Number
JM31-CP
Rev
-1
Date: Thursday, February 25, 2010
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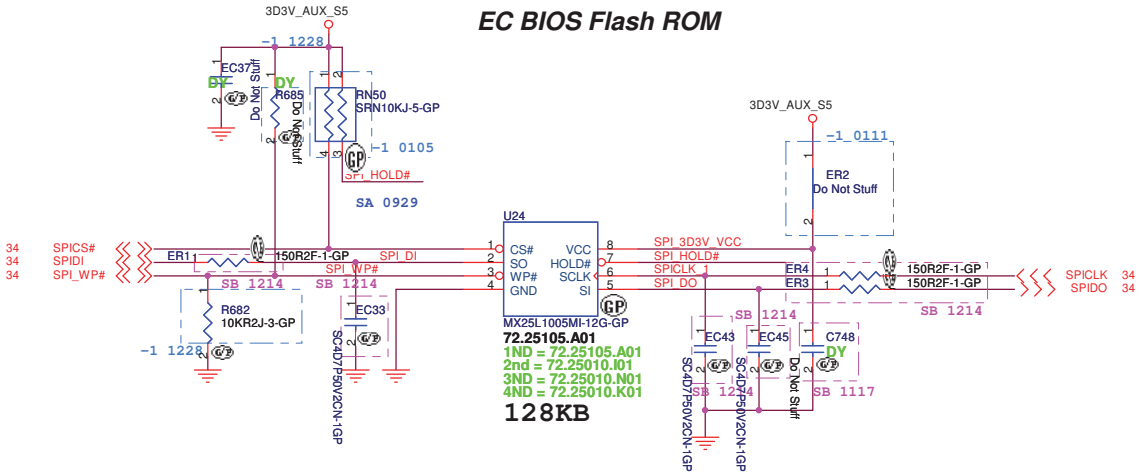
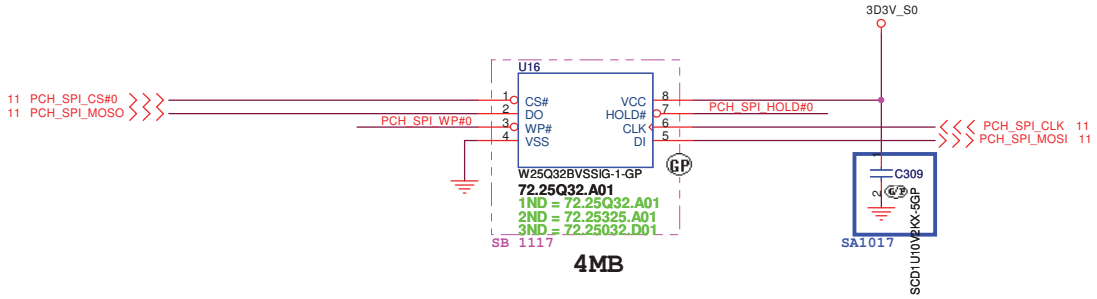
1
K/B
26

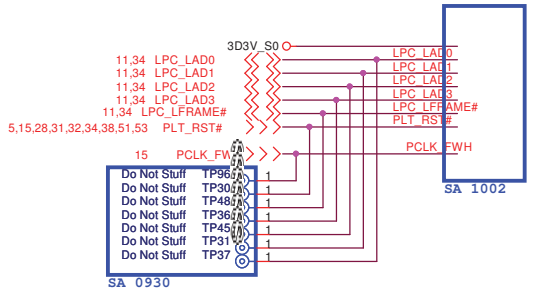
## EC BIOS Flash ROM

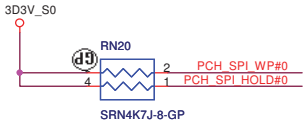



## System BIOS Flash ROM




## GOLDEN FINGER FOR DEBUG BOARD

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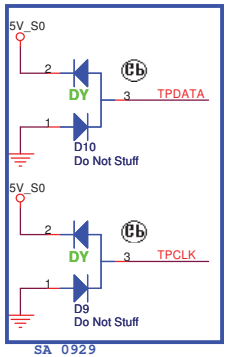
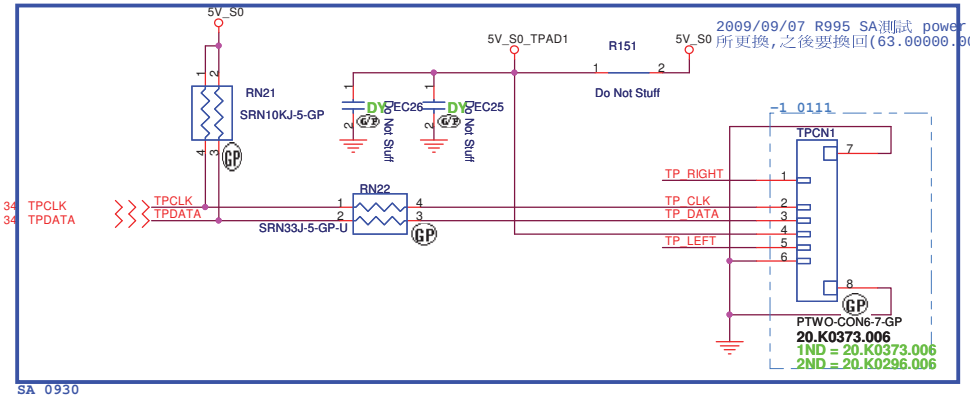
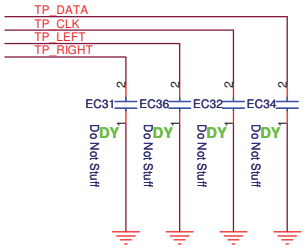
| | | |
|---|---|---|
| Title: **BIOS** | | |
| Size: A3 | Document Number: **JM31-CP** | Rev: -1 |
| Date: Thursday, February 25, 2010 | Sheet 35 of 62 | |

# TOUCH PAD

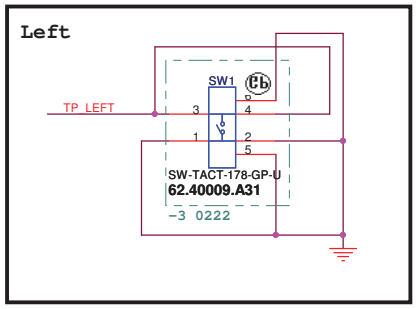


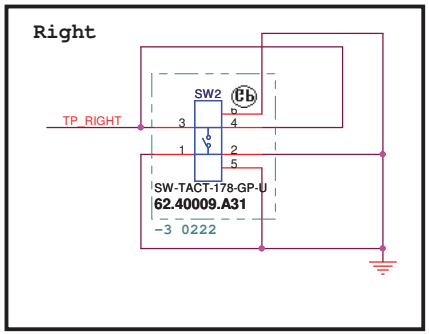



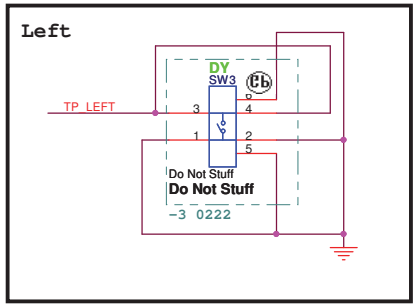



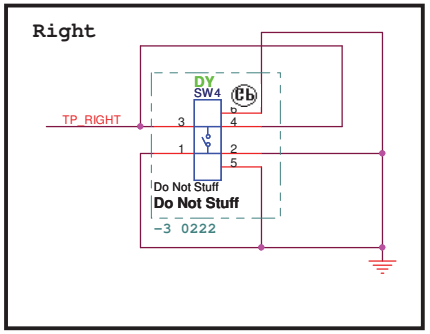

1 12

T/P

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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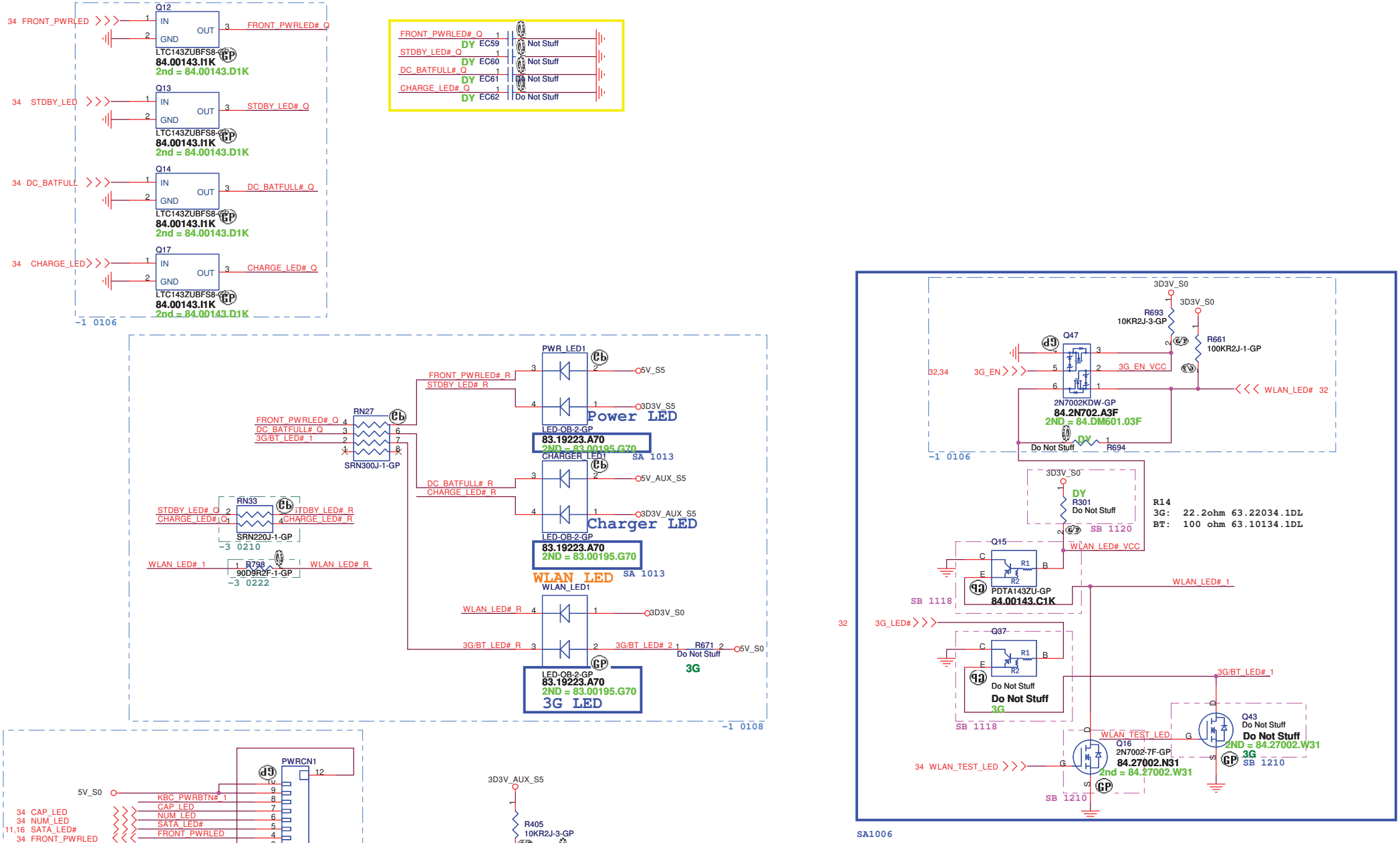
| | | |
|---|---|---|
| Title | Touch PAD | |
| Size A3 | Document Number JM31-CP | Rev -1 |
| Date: Thursday, February 25, 2010 | Sheet 36 of 62 | |

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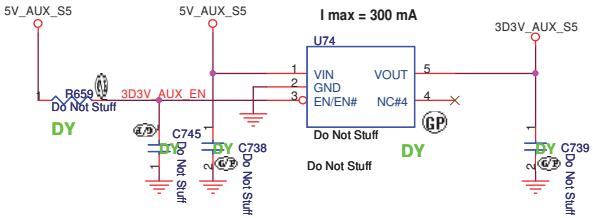
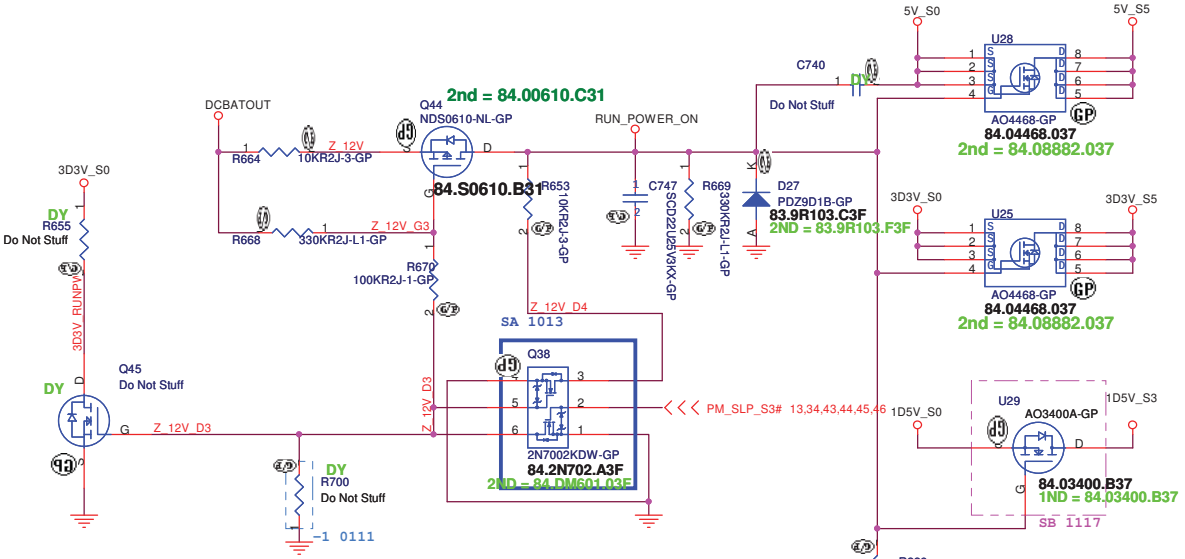
| Title | | |
|---|---|---|
| POWER CONN | | |
| Size: A3 | Document Number: JM31-CP | Rev: -3 |
| Date: Thursday, February 25, 2010 | Sheet 37 of 62 | |

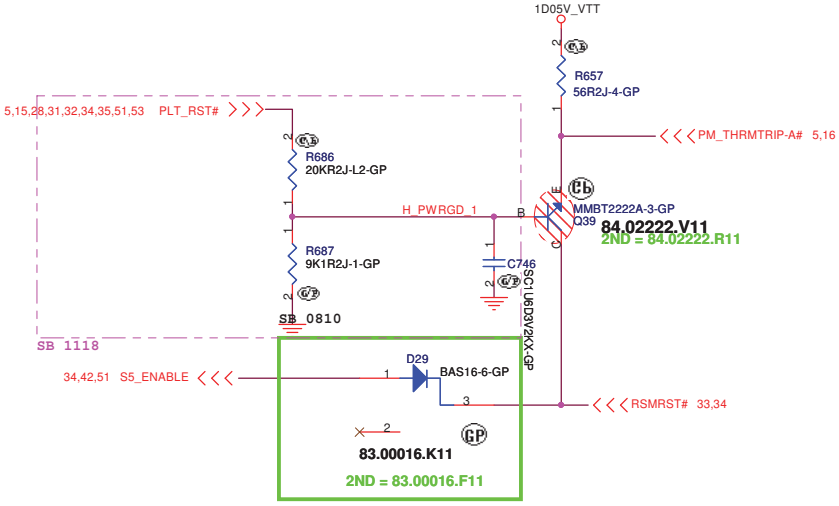
# Run Power

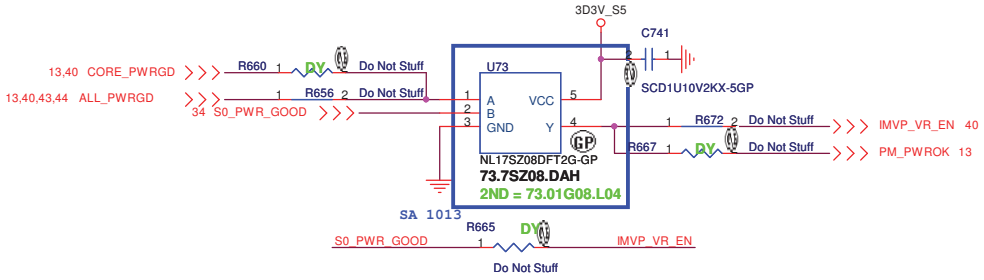
## Aux Power

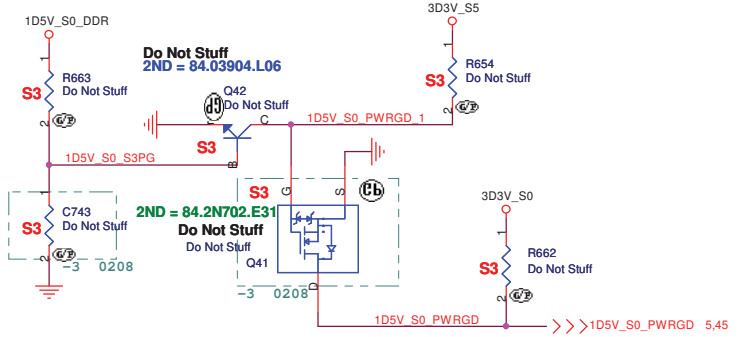
3D3V_AUX_S5

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Title: **RUN POWER and 3D3V_AUX_S5**

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|---|---|---|
| A3 | JM31-CP | -3 |

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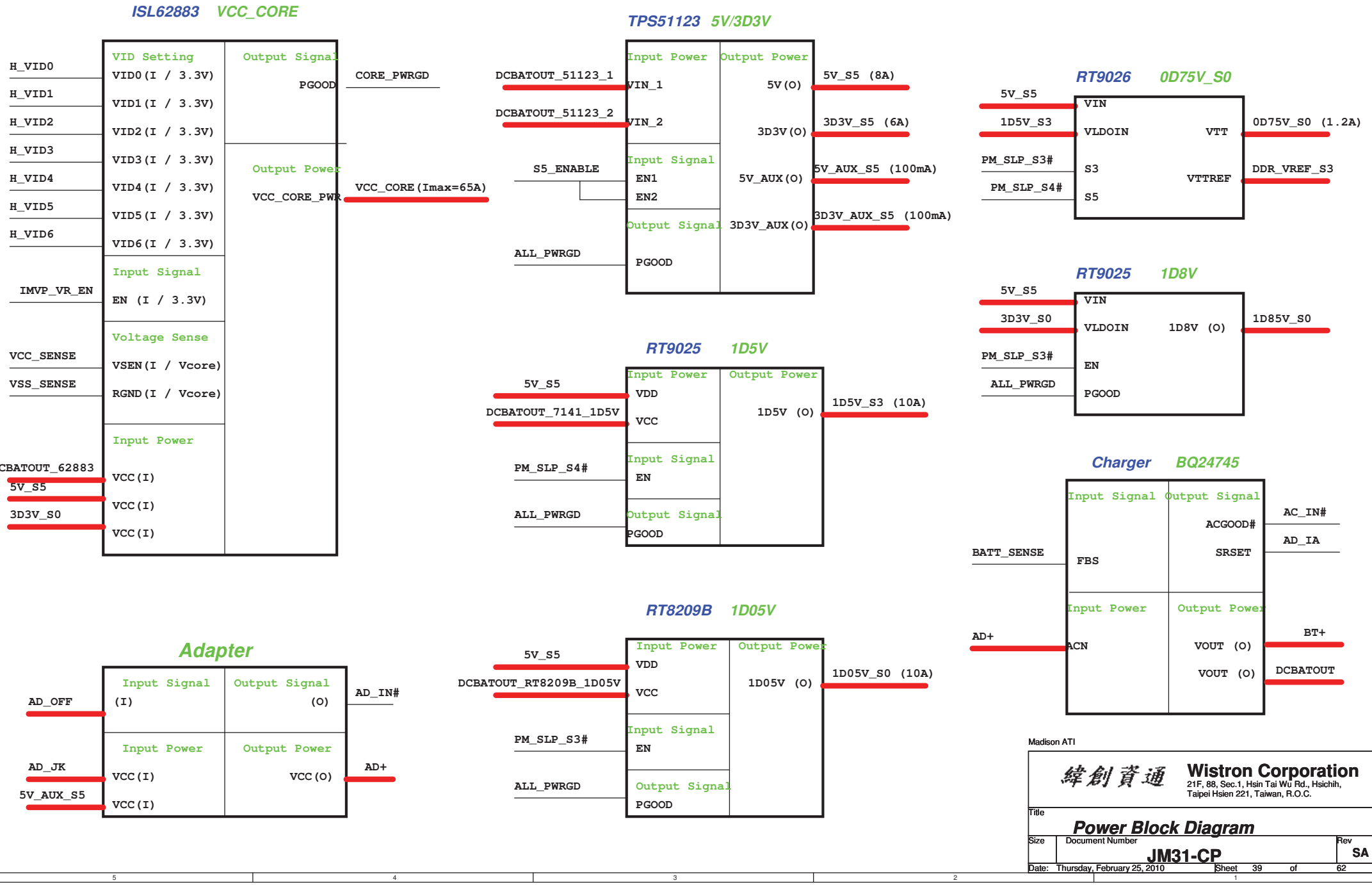


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Title: **Power Block Diagram**

| Size | Document Number | Rev |
|---|---|---|
| | JM31-CP | SA |

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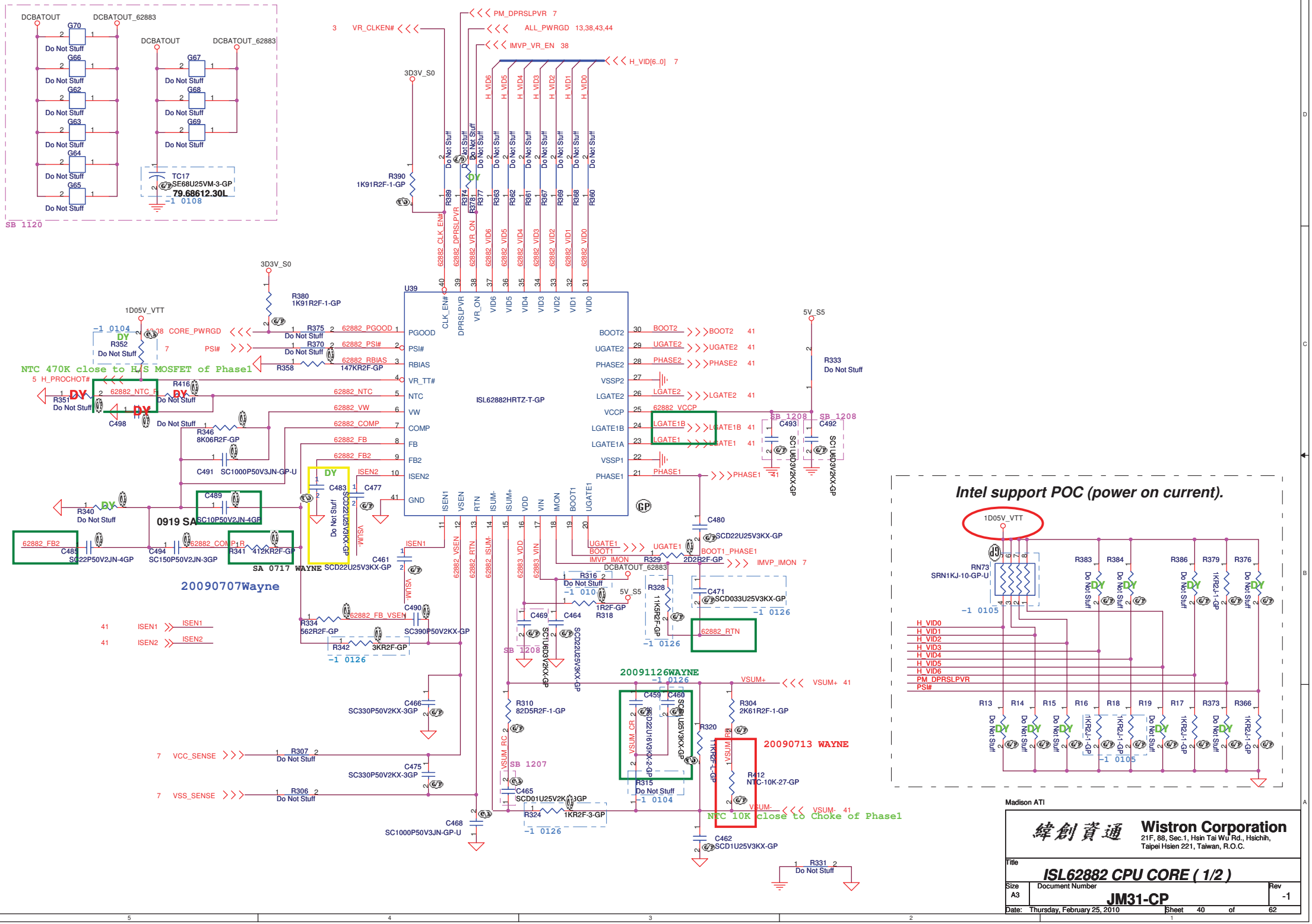


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Title: **ISL62882 CPU CORE ( 1/2 )**

| Size | Document Number | Rev |
|---|---|---|
| A3 | JM31-CP | -1 |

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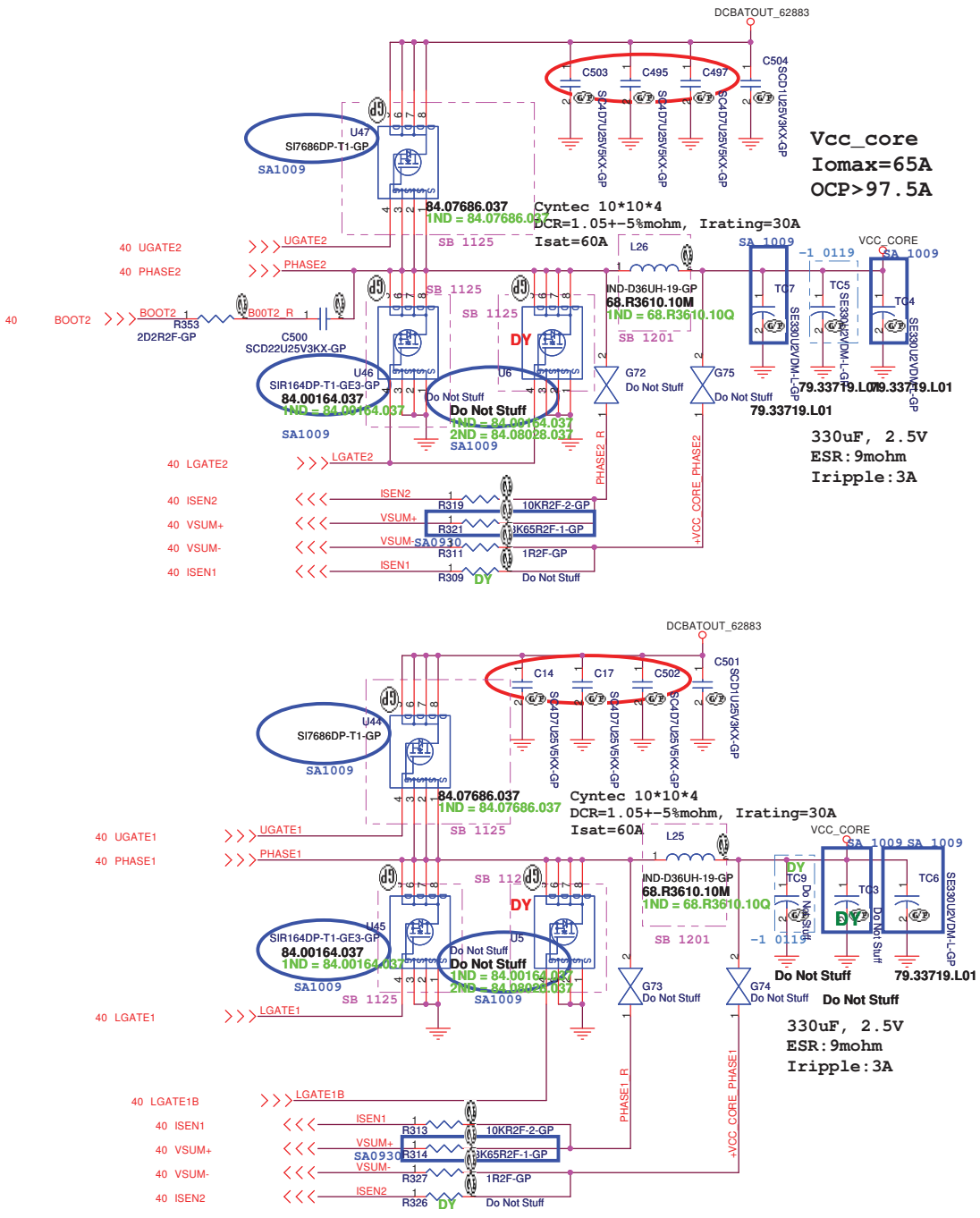


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Title: *ISL62882 CPU CORE ( 2/2 )*

| Size | Document Number | Rev |
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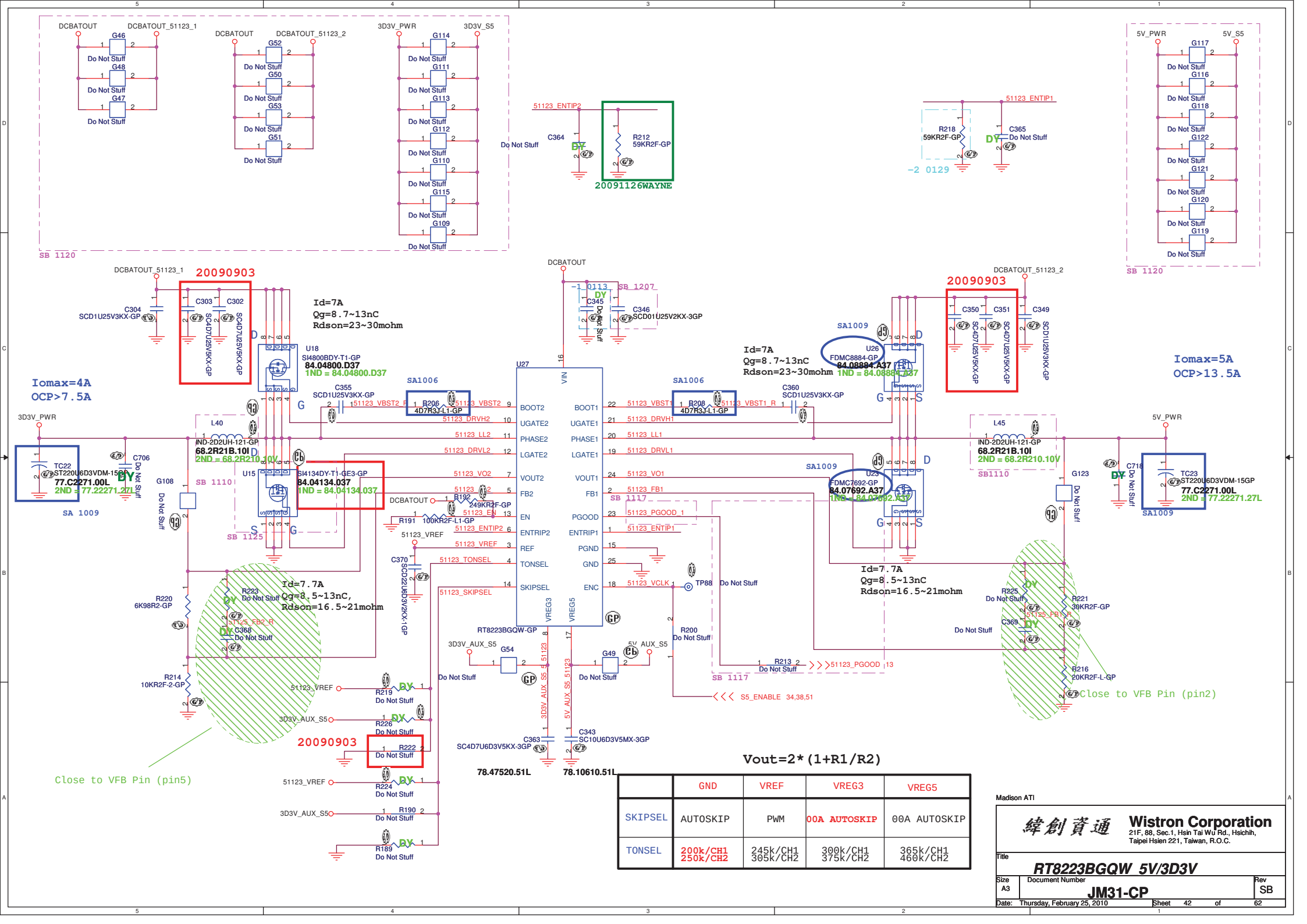


| | GND | VREF | VREG3 | VREG5 |
|---|---|---|---|---|
| SKIPSEL | AUTOSKIP | PWM | 00A AUTOSKIP | 00A AUTOSKIP |
| TONSEL | 200k/CH1<br>250k/CH2 | 245k/CH1<br>305k/CH2 | 300k/CH1<br>375k/CH2 | 365k/CH1<br>460k/CH2 |

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Title: **RT8223BGQW 5V/3D3V**

| Size | Document Number | Rev |
|---|---|---|
| A3 | JM31-CP | SB |

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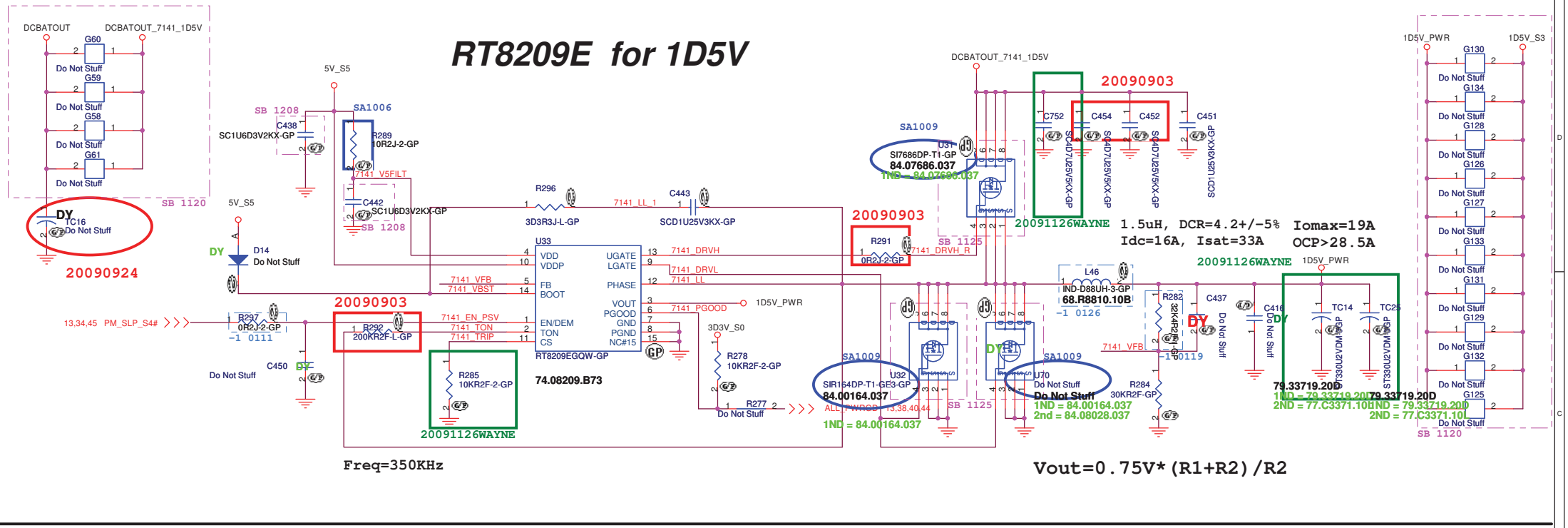
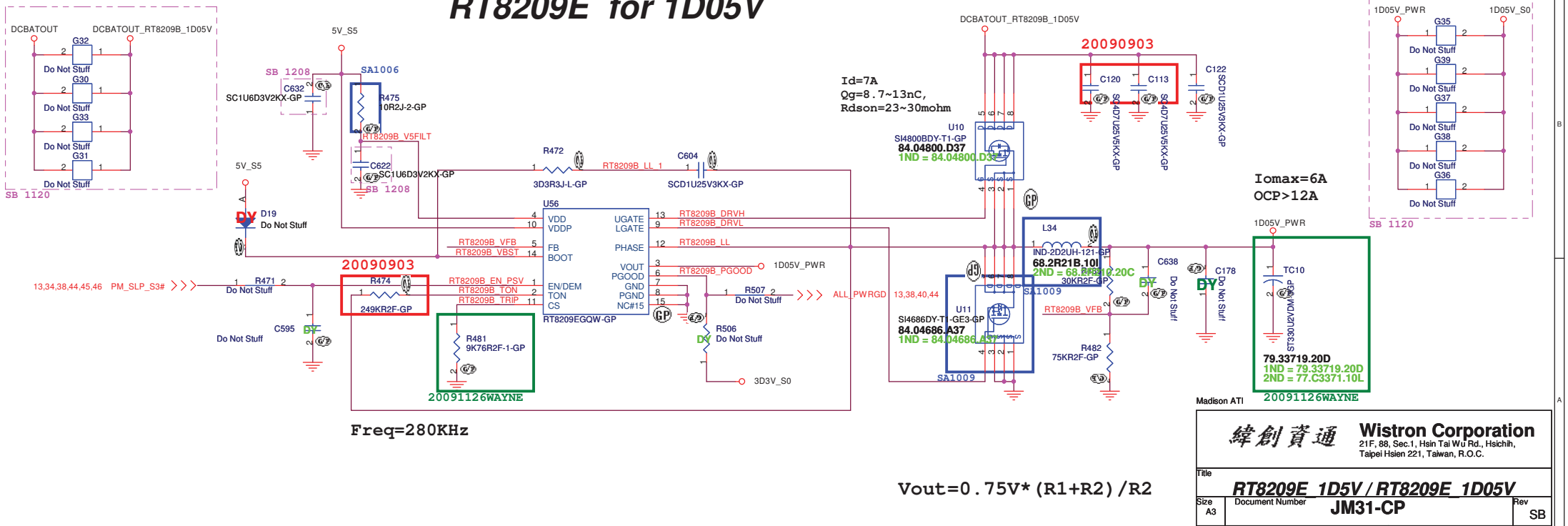
# RT8209E for 1D5V




Vout=0.75V*(R1+R2)/R2

# RT8209E for 1D05V




Vout=0.75V*(R1+R2)/R2

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| | | |
|---|---|---|
| Title | *RT8209E_1D5V / RT8209E_1D05V* | |
| Size A3 | Document Number JM31-CP | Rev SB |
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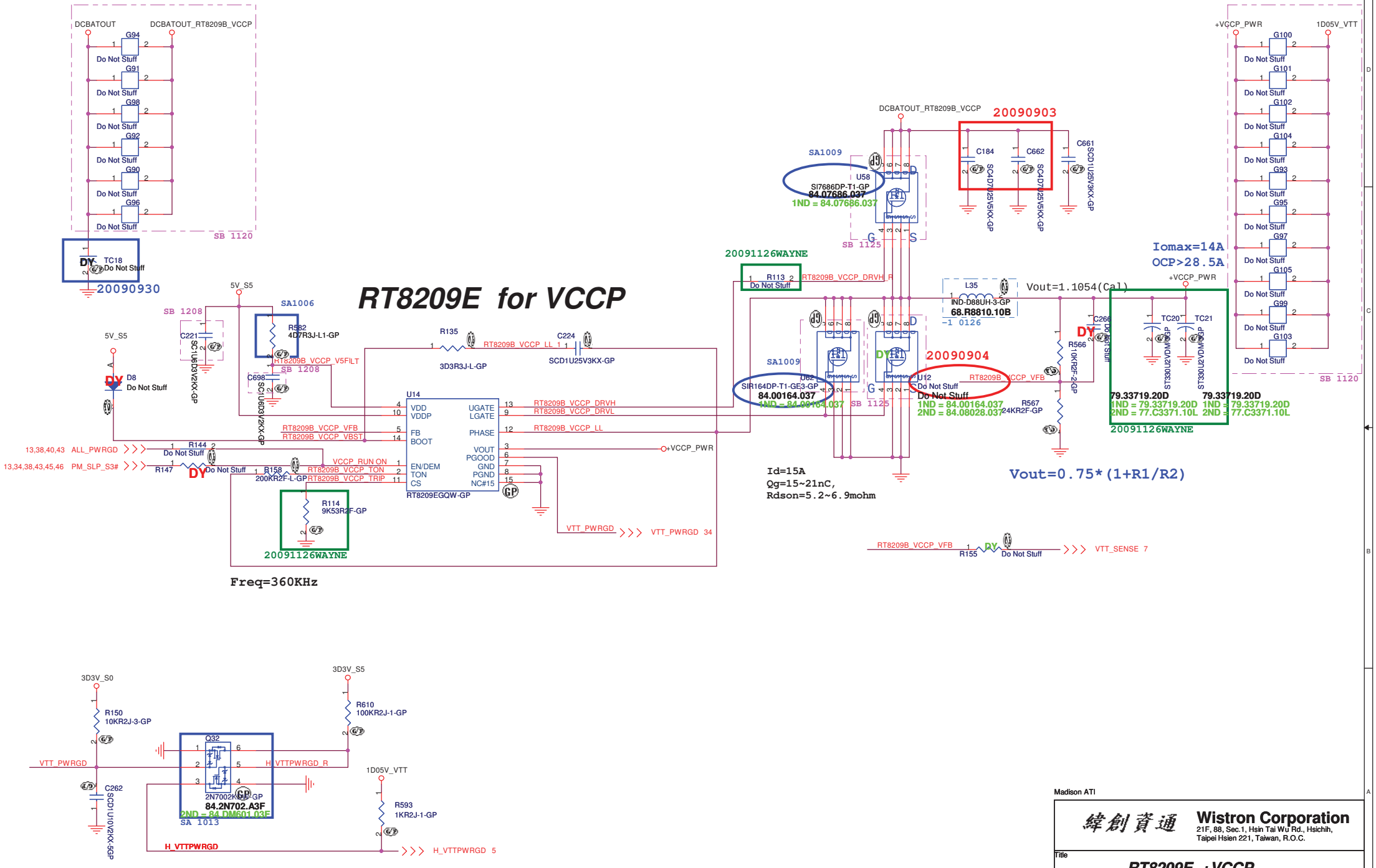
# RT8209E for VCCP

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Title: ***RT8209E +VCCP***

| Size | Document Number | Rev |
|---|---|---|
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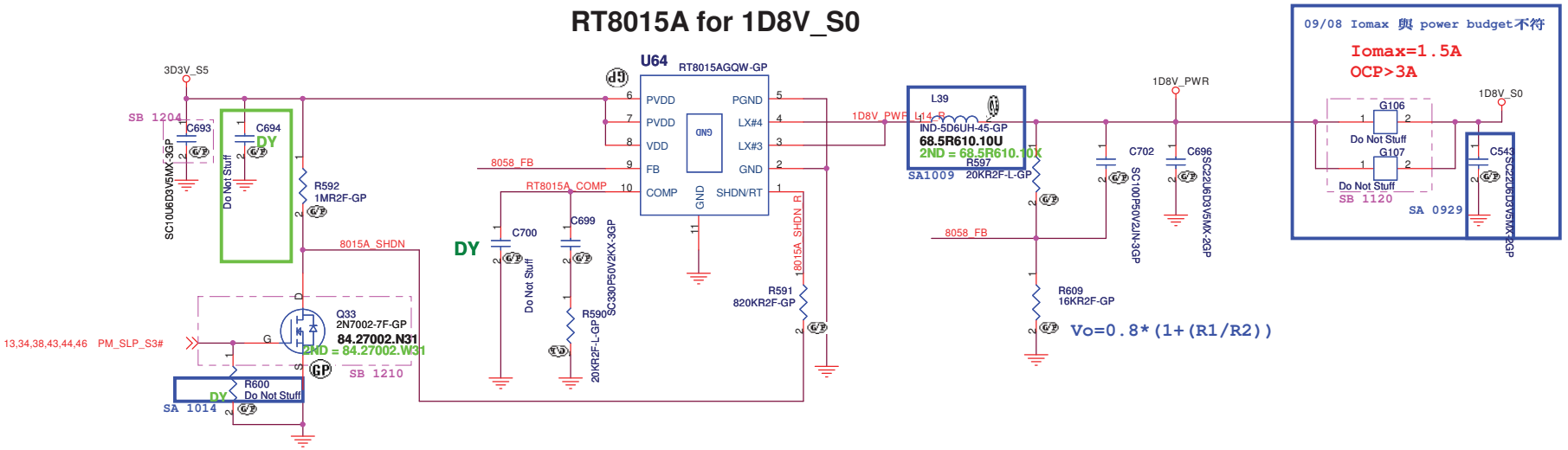
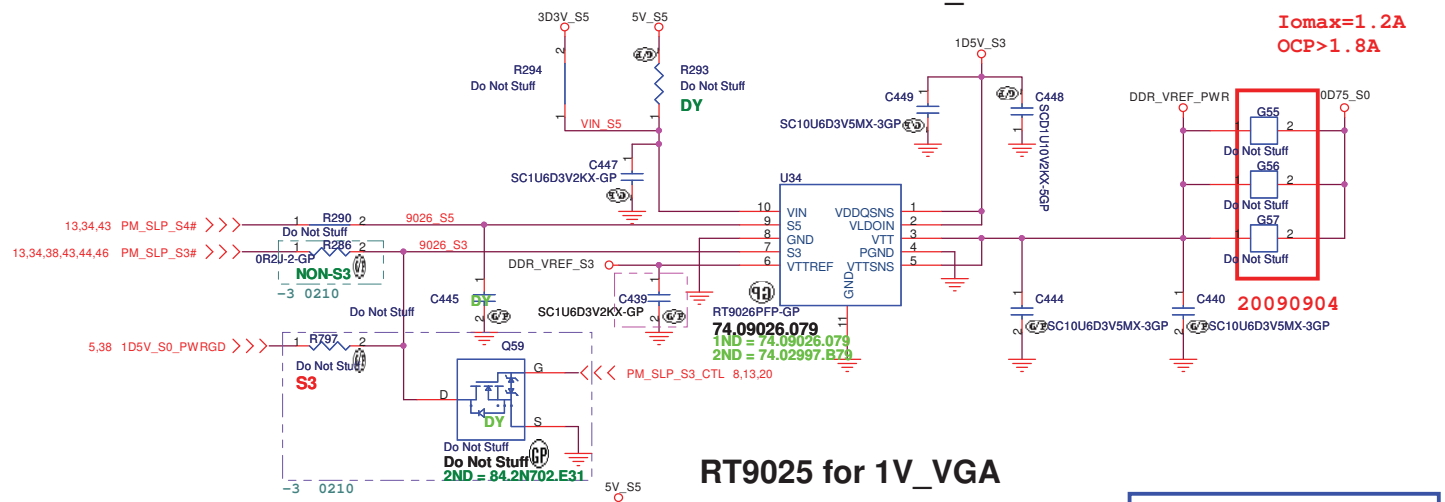
# RT8015A for 1D8V_S0

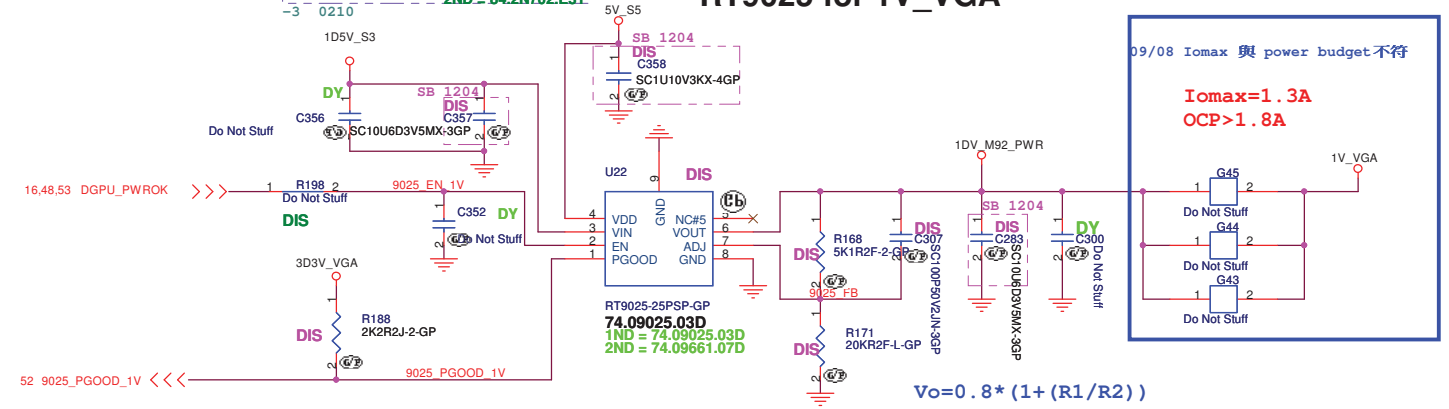



09/08 add 3D3V_S5,R837,R836

# RT9026 for 0D75V_S3




# RT9025 for 1V_VGA

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| | | |
|---|---|---|
| Title | RT9025_1D8V_1V/RT9026_0D75 | |
| Size A3 | Document Number JM31-CP | Rev -3 |
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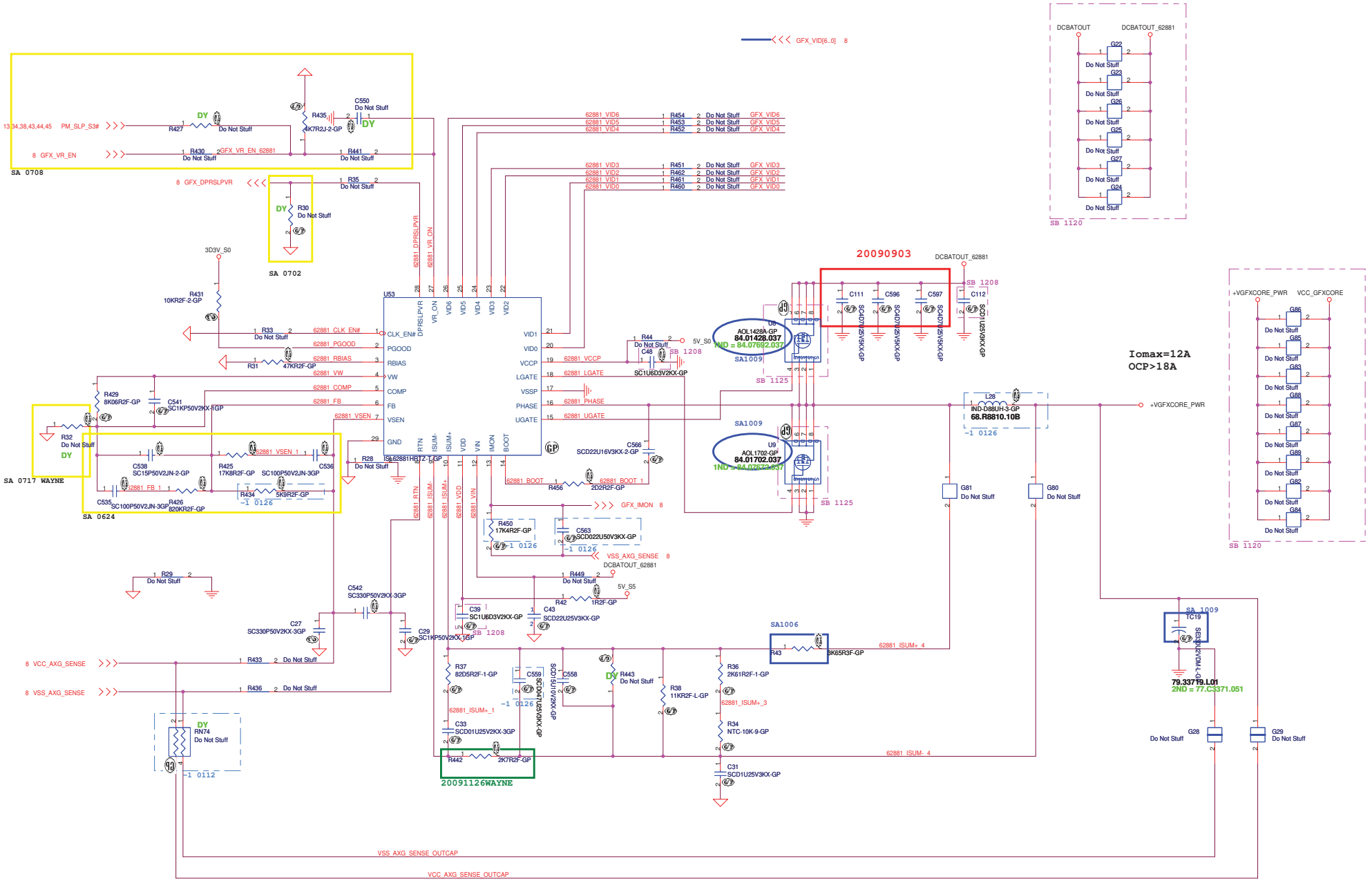
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SB 1120
20090903
DCBATOUT_62881
SB 1208
SB 1125
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OCP>18A
+VGFXCORE_PWR
VCC_GFXCORE
SB 1120
SA 0708
SA 0702
SA 0717 WAYNE
SA 0624
SA1009
SA1006
U53
ISL62881HRTZ-T-GP
U6
AOL1428A-GP
84.01428.037
2ND = 84.07552.037
U9
AOL1702-GP
84.01702.037
2ND = 84.07572.037
L28
IND-D88UH-3-GP
68.R8810.10B
-1 0126
79.33719.L01
2ND = 77.C3371.051
20091126WAYNE
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62881 +VCC_GFXCORE
Size C
Document Number JM31-CP
Rev SB
Date: Thursday, February 25, 2010
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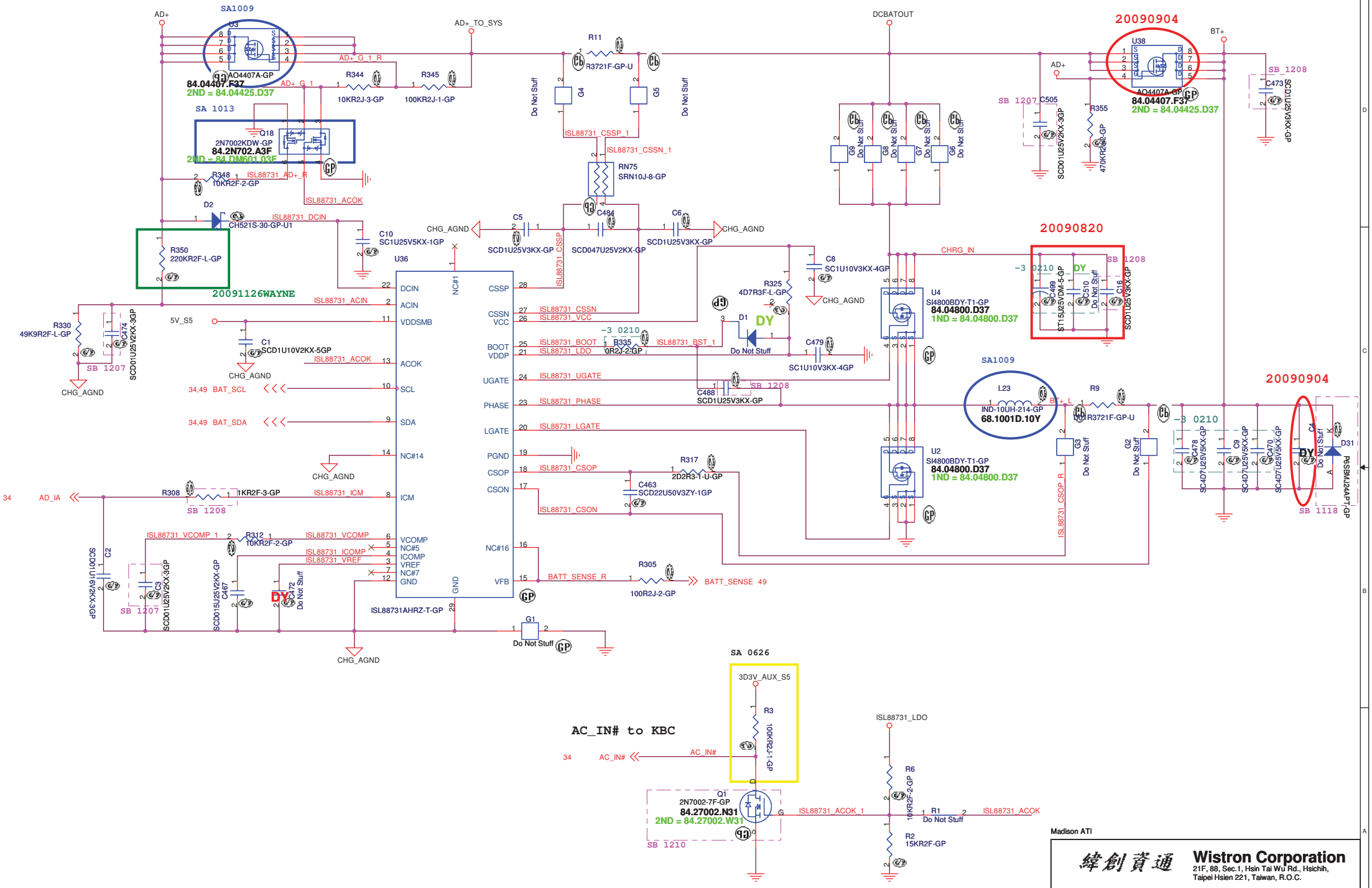
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2ND = 84.04425.D37
SA 1013
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
R3721F-GP-U
RN75
SRN10J-8-GP
CH521S-30-GP-U1
R350
220KR2F-L-GP
20091126WAYNE
U36
ISL88731AHRZ-T-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
SI4800BDY-T1-GP
84.04800.D37
1ND = 84.04800.D37
IND-10UH-214-GP
68.1001D.10Y
20090904
20090820
SA 0626
2N7002-7F-GP
84.27002.N31
2ND = 84.27002.W31
AC_IN# to KBC
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緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL88731A CHARGER
JM31-CP
Rev -3
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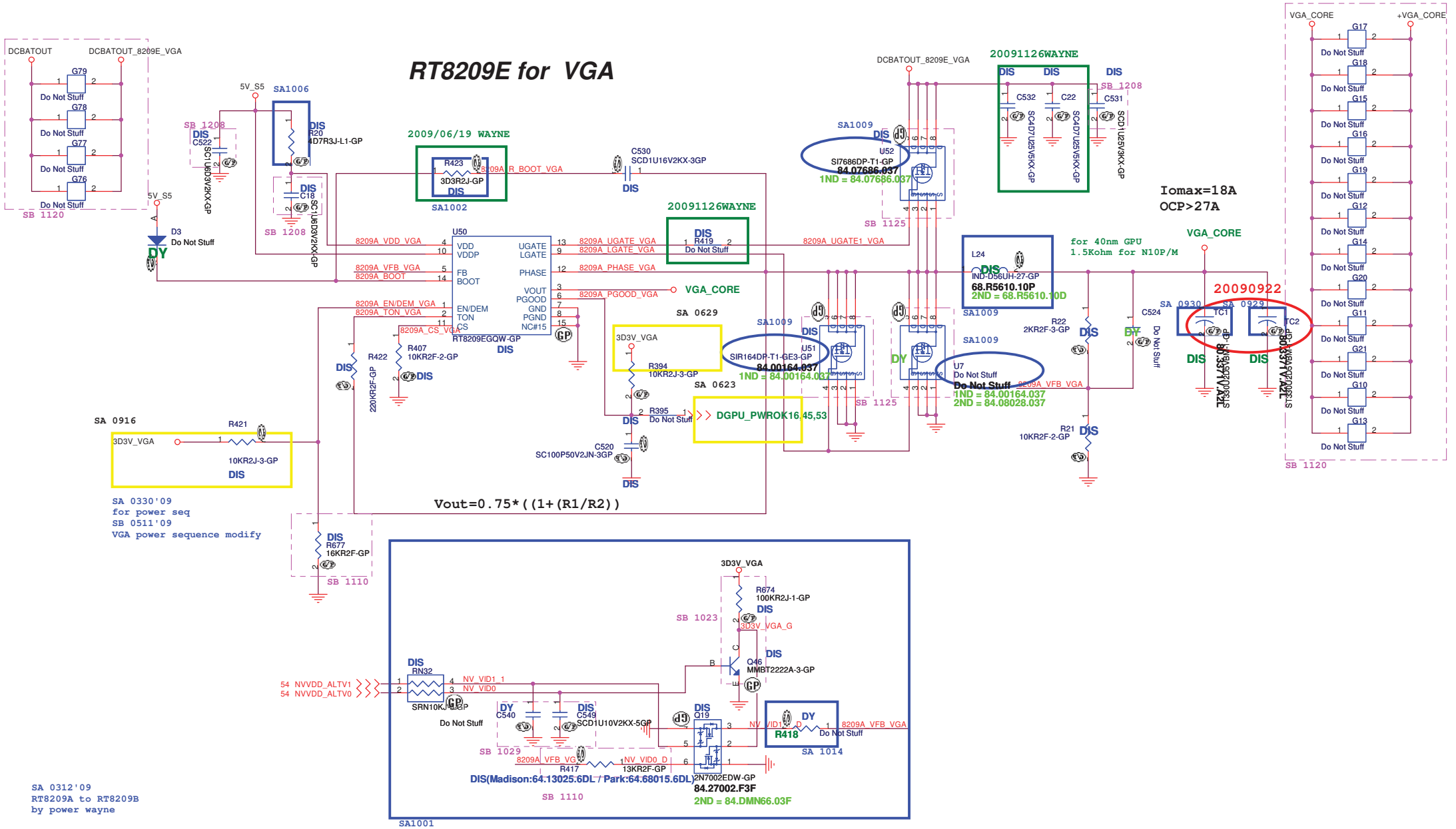
RT8209E for VGA
DCBATOUT
DCBATOUT_8209E_VGA
SB 1120
5V_S5
SA1006
SB 1208
2009/06/19 WAYNE
R423
3D3R2J-GP
8209A_R_BOOT_VGA
SA1002
C530
SCD1U16V2KX-3GP
20091126WAYNE
R419
Do Not Stuff
8209A_UGATE1_VGA
SA1009
U52
SI7686DP-T1-GP
84.07686.037
1ND = 84.07686.037
SB 1125
C532
C22
C531
SC4D7U25V5KX-GP
SCD1U25V3KX-GP
SB 1208
Iomax=18A
OCP>27A
VGA_CORE
+VGA_CORE
for 40nm GPU
1.5Kohm for N10P/M
20090922
D3
Do Not Stuff
DY
U50
RT8209EGQW-GP
8209A_VDD_VGA
8209A_VFB_VGA
8209A_BOOT
8209A_UGATE_VGA
8209A_LGATE_VGA
8209A_PHASE_VGA
8209A_PGOOD_VGA
8209A_EN/DEM_VGA
8209A_TON_VGA
8209A_CS_VGA
SA 0629
SA 0623
3D3V_VGA
R394
10KR2J-3-GP
R395
Do Not Stuff
DGPU_PWROK16,45,53
C520
SC100P50V2JN-3GP
SIR164DP-T1-GE3-GP
84.00164.037
1ND = 84.00164.037
U51
U7
Do Not Stuff
2ND = 84.08028.037
L24
IND-D56UH-27-GP
68.R5610.10P
2ND = 68.R5610.10D
R22
2KR2F-3-GP
R21
10KR2F-2-GP
C524
SA 0930
SA 0929
TC1
TC2
R407
10KR2F-2-GP
R422
220KR2F-GP
SA 0916
R421
10KR2J-3-GP
SA 0330'09
for power seq
SB 0511'09
VGA power sequence modify
R677
16KR2F-GP
SB 1110
Vout=0.75*((1+(R1/R2))
SA1001
R674
100KR2J-1-GP
SB 1023
3D3V_VGA_G
Q46
MMBT2222A-3-GP
RN32
SRN10KJ-5-GP
54 NVVDD_ALTV1
54 NVVDD_ALTV0
NV_VID1_1
NV_VID0
C540
C549
SCD1U10V2KX-5GP
Q19
2N7002EDW-GP
84.27002.F3F
2ND = 84.DMN66.03F
R418
SA 1014
SB 1029
R417
13KR2F-GP
8209A_VFB_VG
NV_VID0_D
DIS(Madison:64.13025.6DL / Park:64.68015.6DL)
SA 0312'09
RT8209A to RT8209B
by power wayne
PARK ( 6.8K)
GPIO15/VID0 VGA_CORE
0 0.90V
1 1.12V
MADISON (13K)
GPIO15/VID0 VGA_CORE
0 0.90V
1 1.02V
Madison ATI
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8209E VGA CORE
Size A3
Document Number JM31-CP
Rev SB
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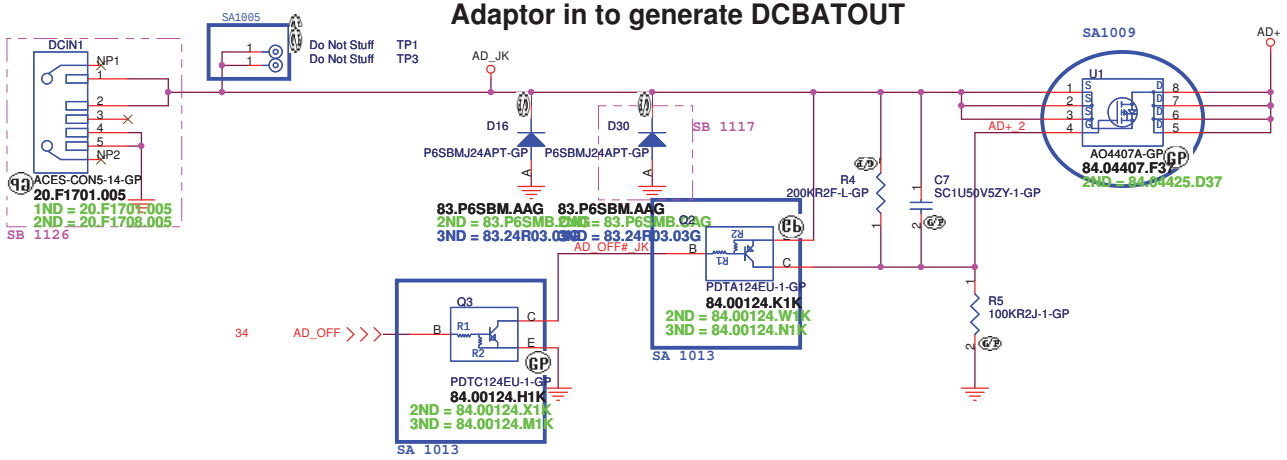
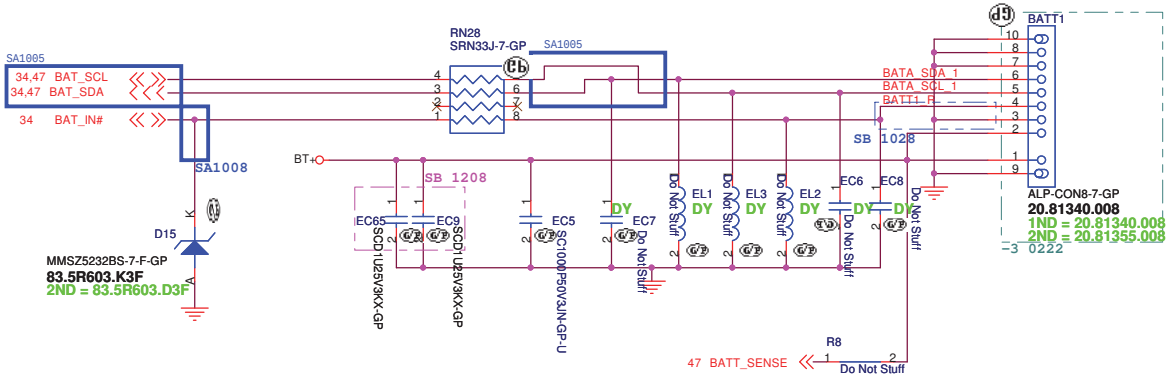
## Adaptor in to generate DCBATOUT




## BATTERY CONNECTOR

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Title: **AD/BATT CONN**

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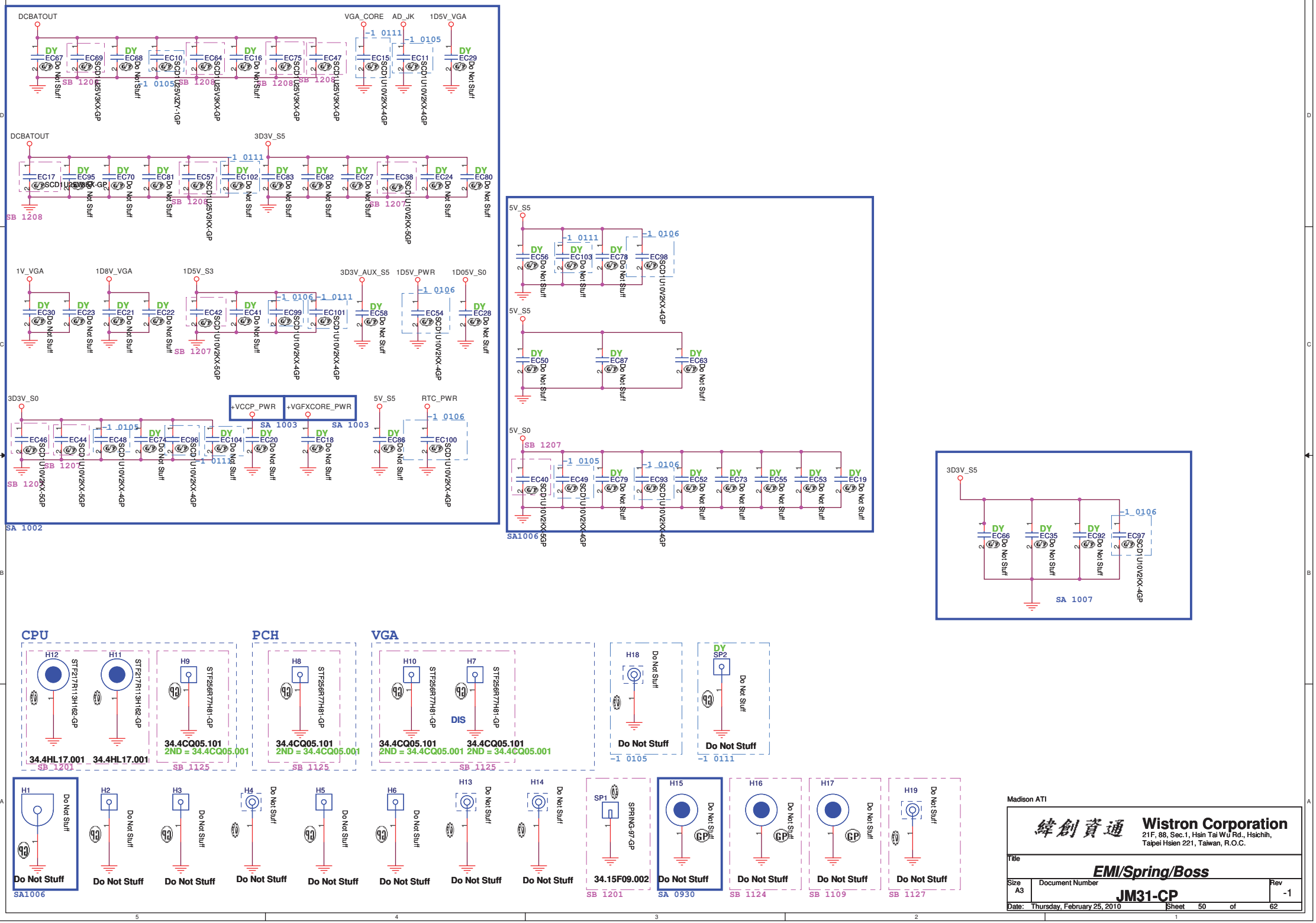


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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

| Size | Document Number | Rev |
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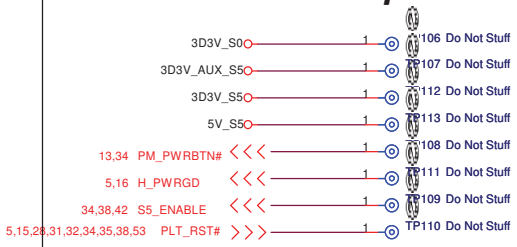
# Check test point




**Test Point放在Dimm Door打開可量測處**

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AFTE TP***

| Size | Document Number | Rev |
|---|---|---|
| A3 | JM31-CP | SA |

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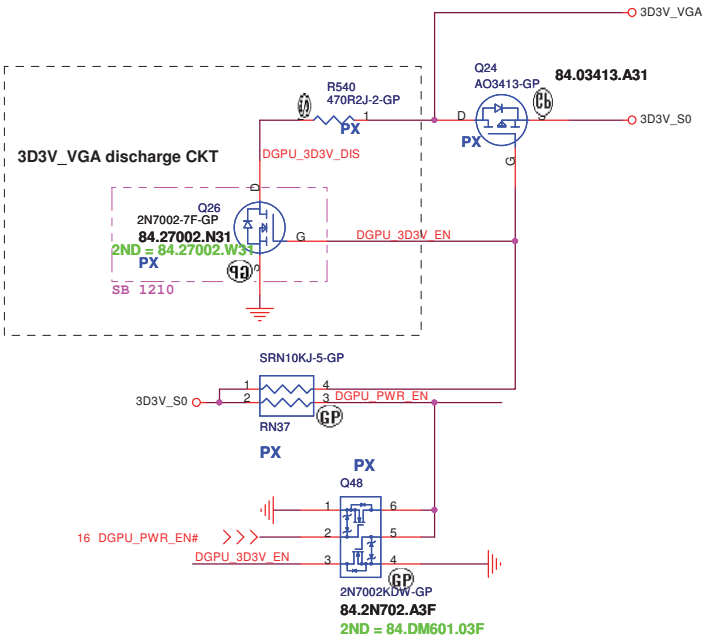
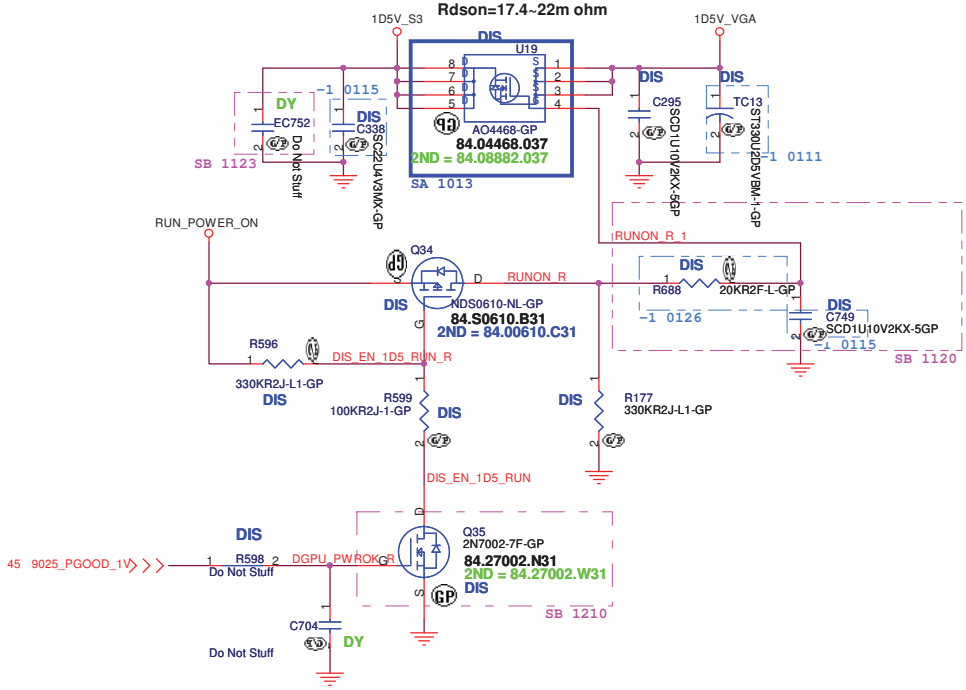
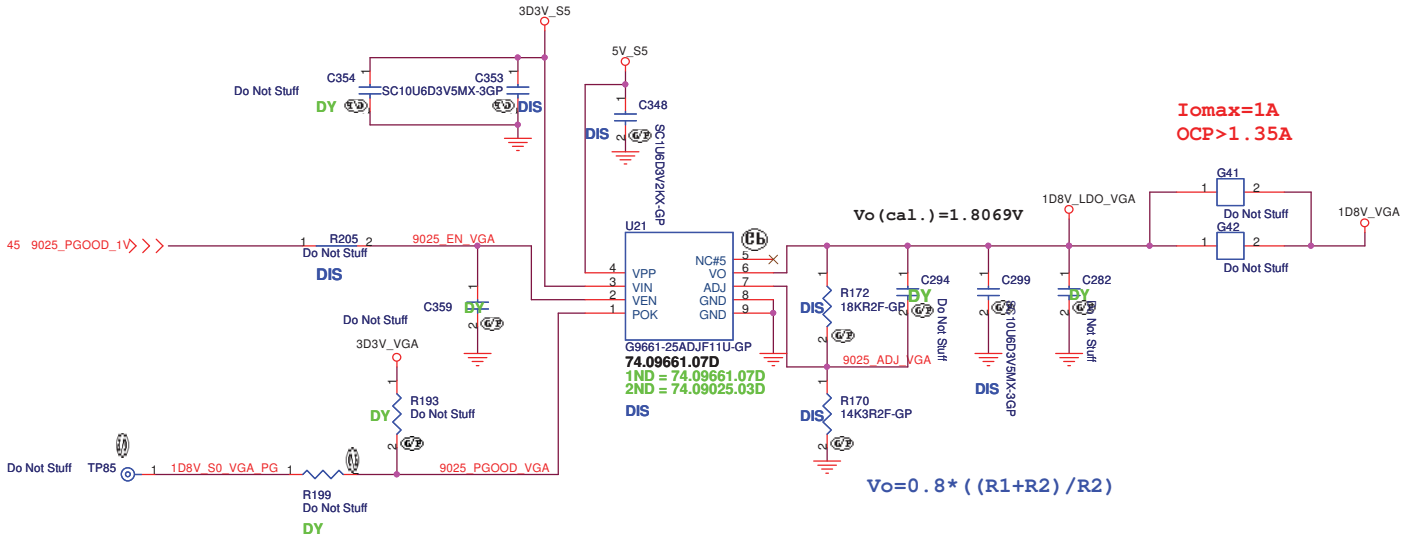
## +3VS to 3.3V_DELAY Transfer




AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm




## G9661 for 1D8V_VGA




Madison ATI

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI POWER**

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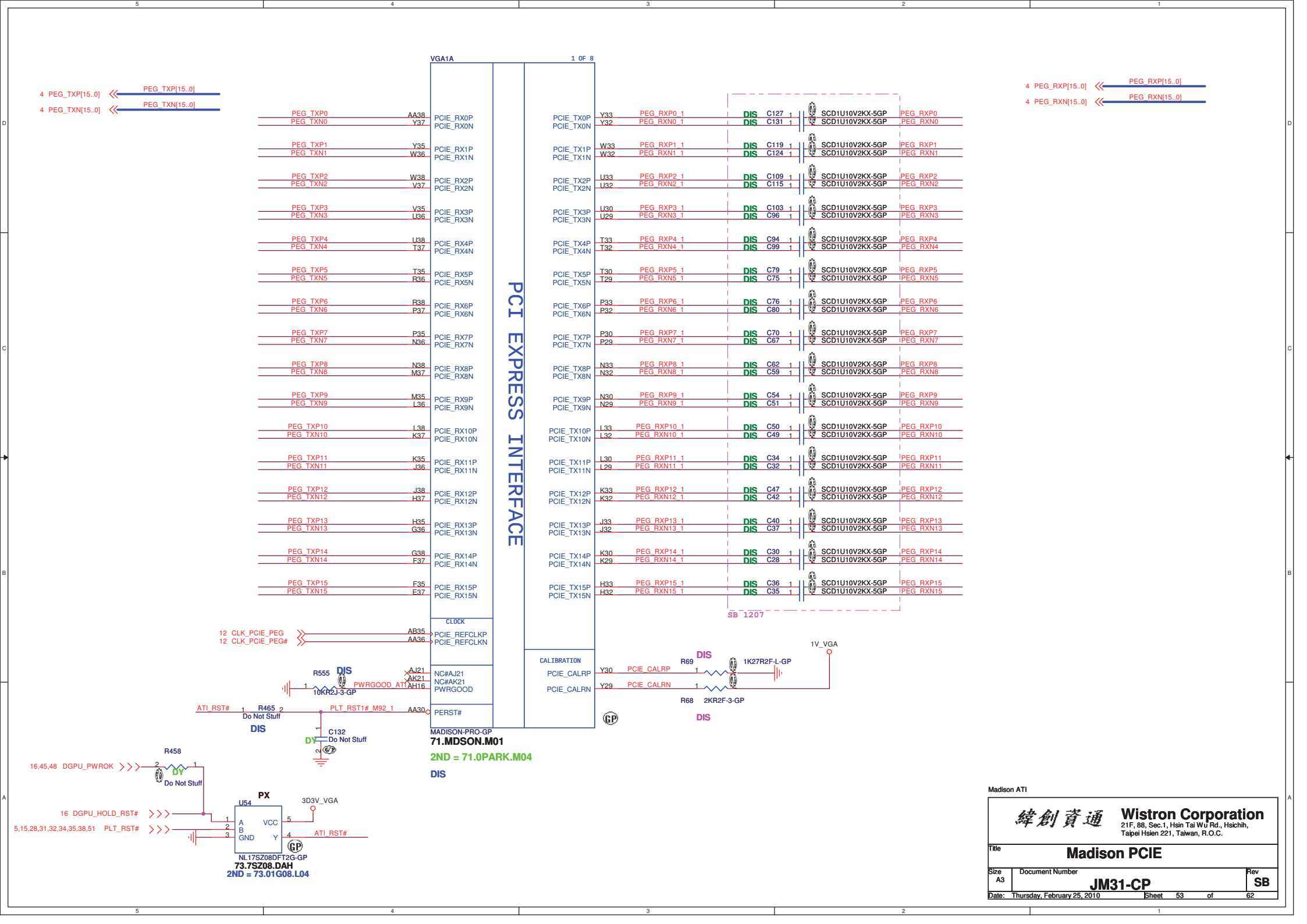
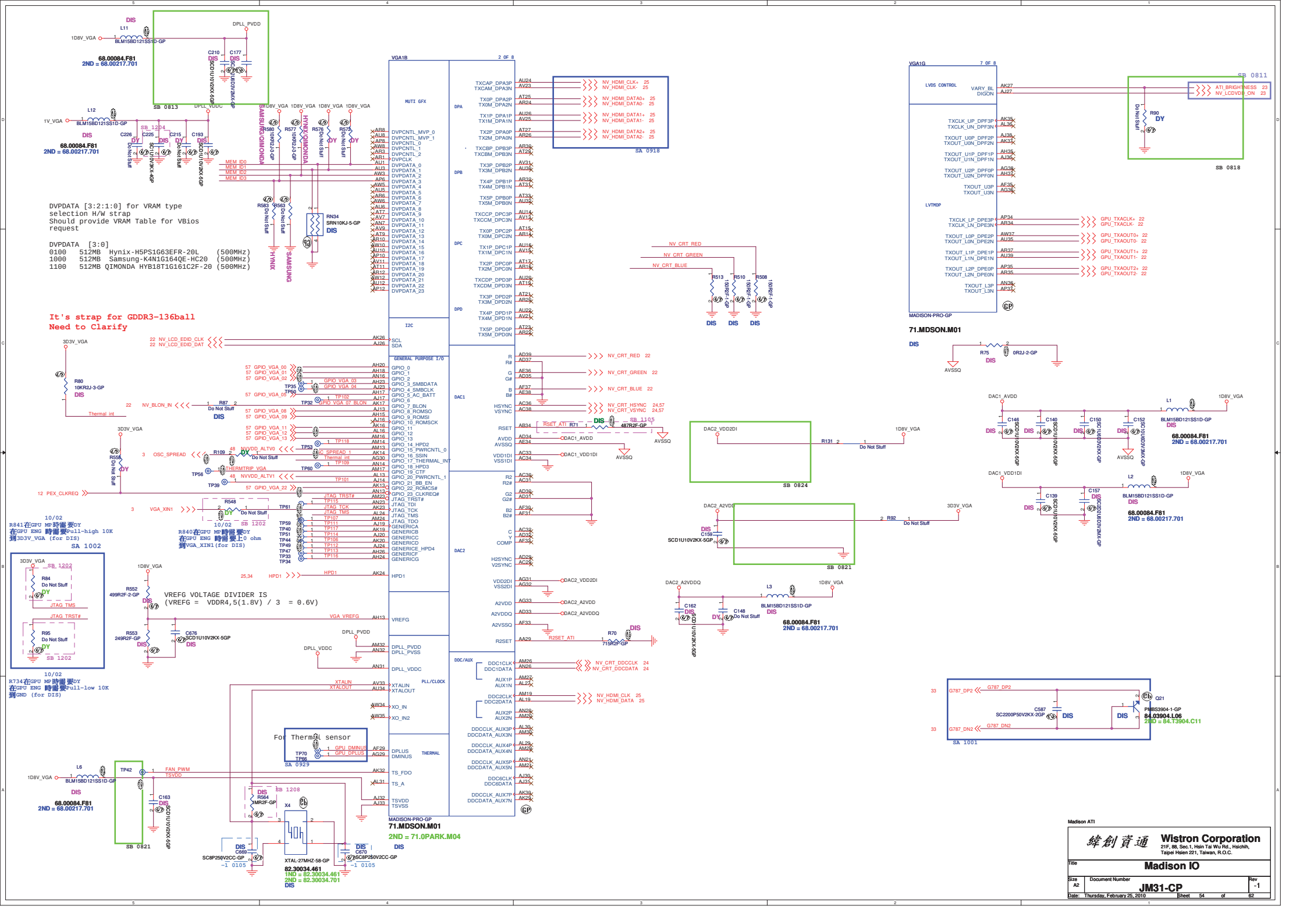



Madison ATI

| | |
|---|---|
| Wistron Corporation | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | Madison PCIE |
| Size: A3 | Document Number: JM31-CP |
| Rev: SB | |
| Date: Thursday, February 25, 2010 | Sheet 53 of 62 |


DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request
DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)
It's strap for GDDR3-136ball
Need to Clarify
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
For Thermal sensor
Madison ATI
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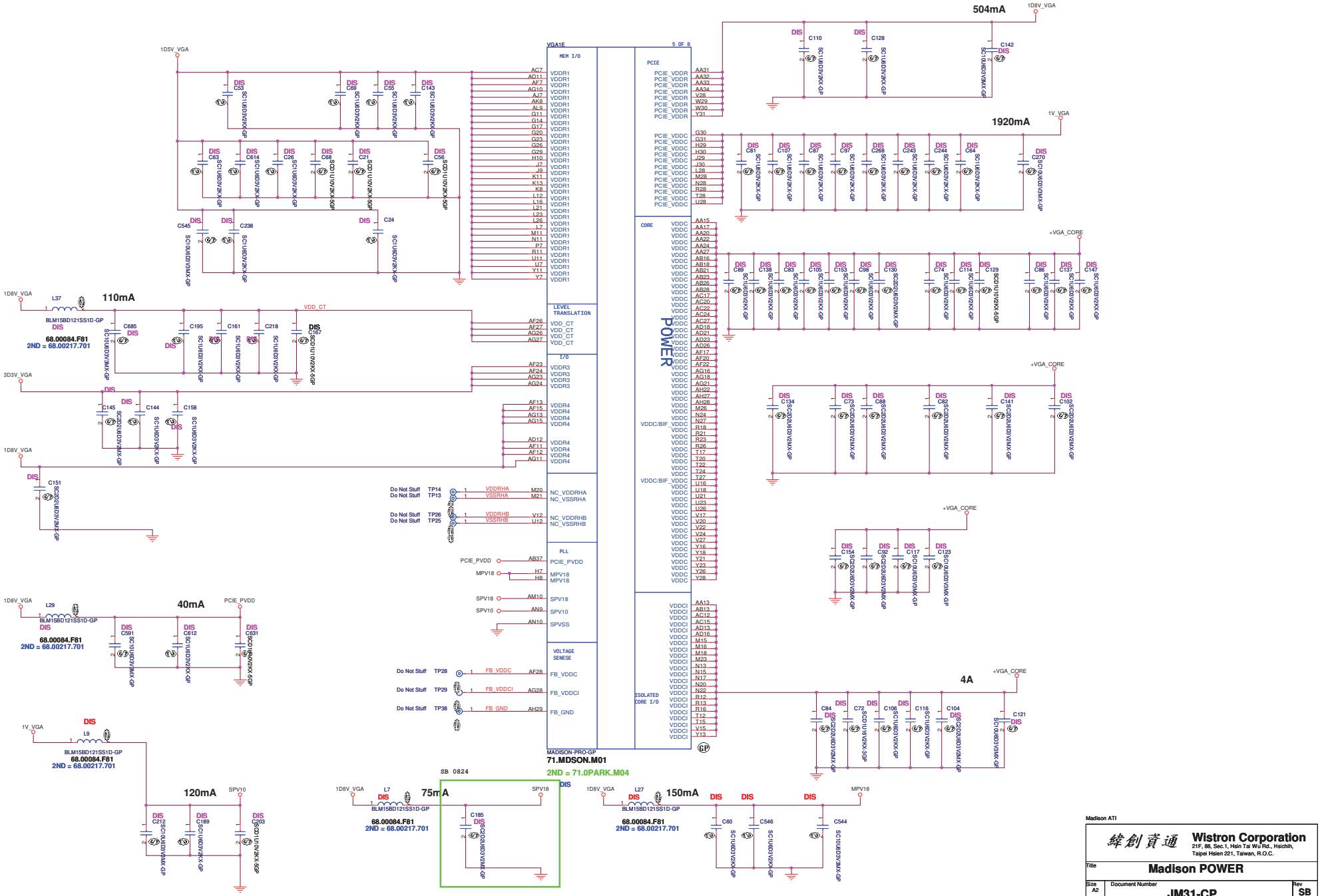
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Madison IO
Size A2
Document Number
JM31-CP
Rev -1
Date: Thursday, February 25, 2010
Sheet 54 of 62

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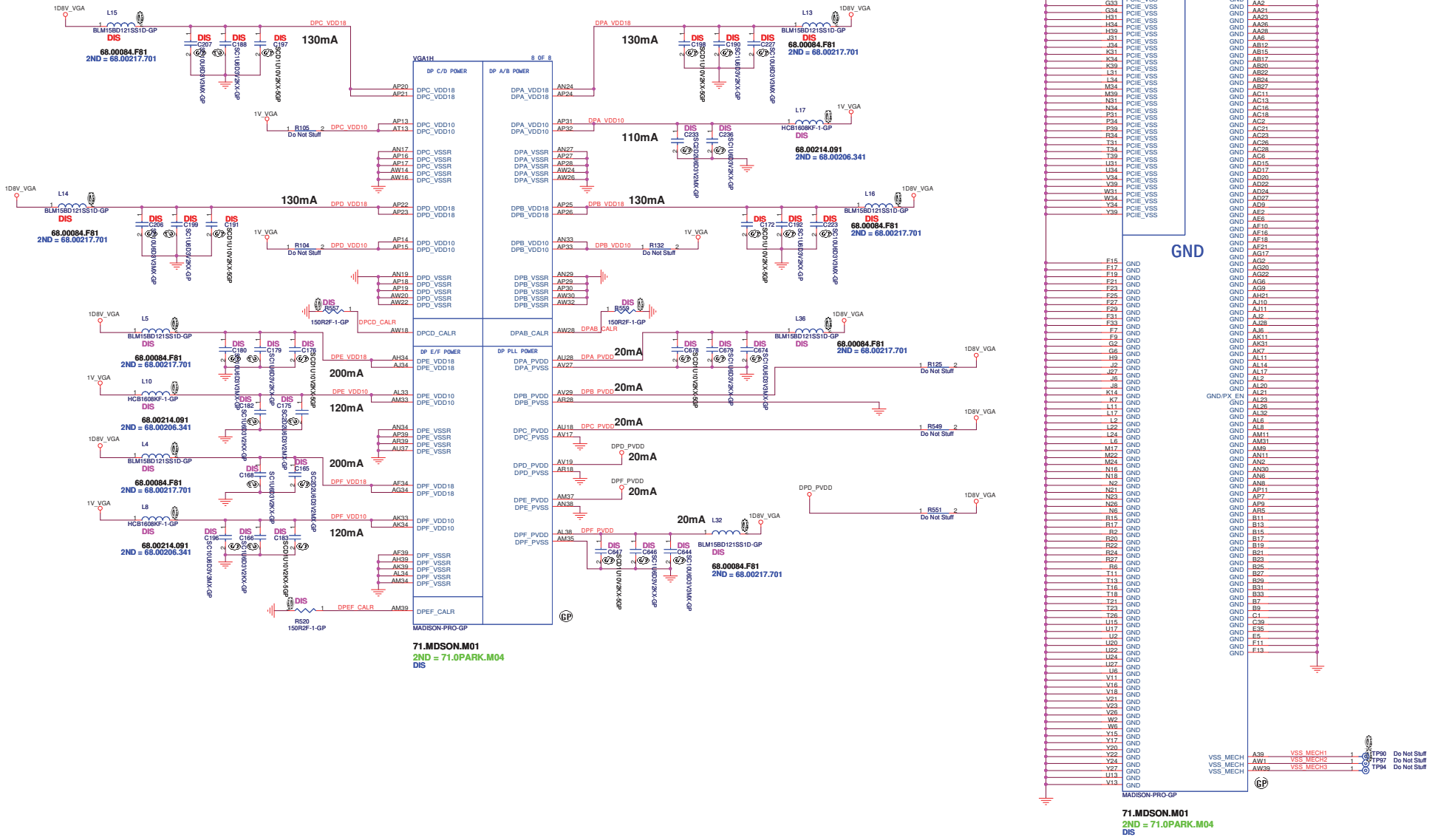
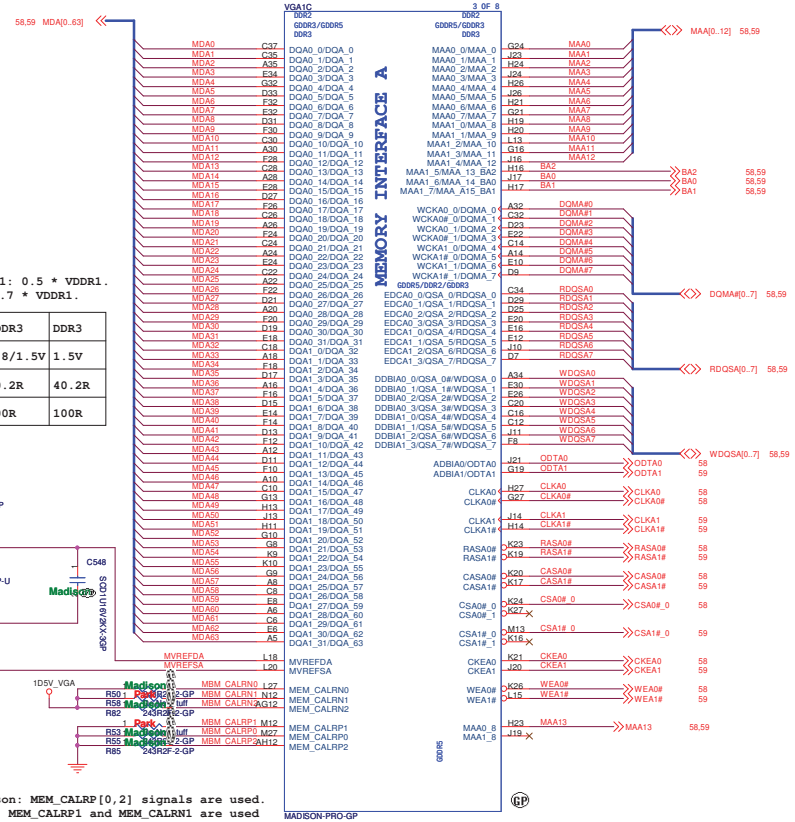
| | | |
|---|---|---|
| Title | Madison POWER | |
| Size A2 | Document Number JM31-CP | Rev SB |
| Date: Thursday, February 25, 2010 | Sheet 55 of 62 | |


VGA1H
8 OF 8
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
MADISON-PRO-GP
71.MDSON.M01
2ND = 71.0PARK.M04
DIS
130mA
110mA
200mA
120mA
20mA
68.00084.F81
2ND = 68.00217.701
68.00214.091
2ND = 68.00206.341
VGA1F
6 OF 8
GND
MADISON-PRO-GP
71.MDSON.M01
2ND = 71.0PARK.M04
DIS
Madison ATI
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DP POWER_GND
Size
A2
Document Number
JM31-CP
Rev
SB
Date: Thursday, February 25, 2010
Sheet 56 of 62

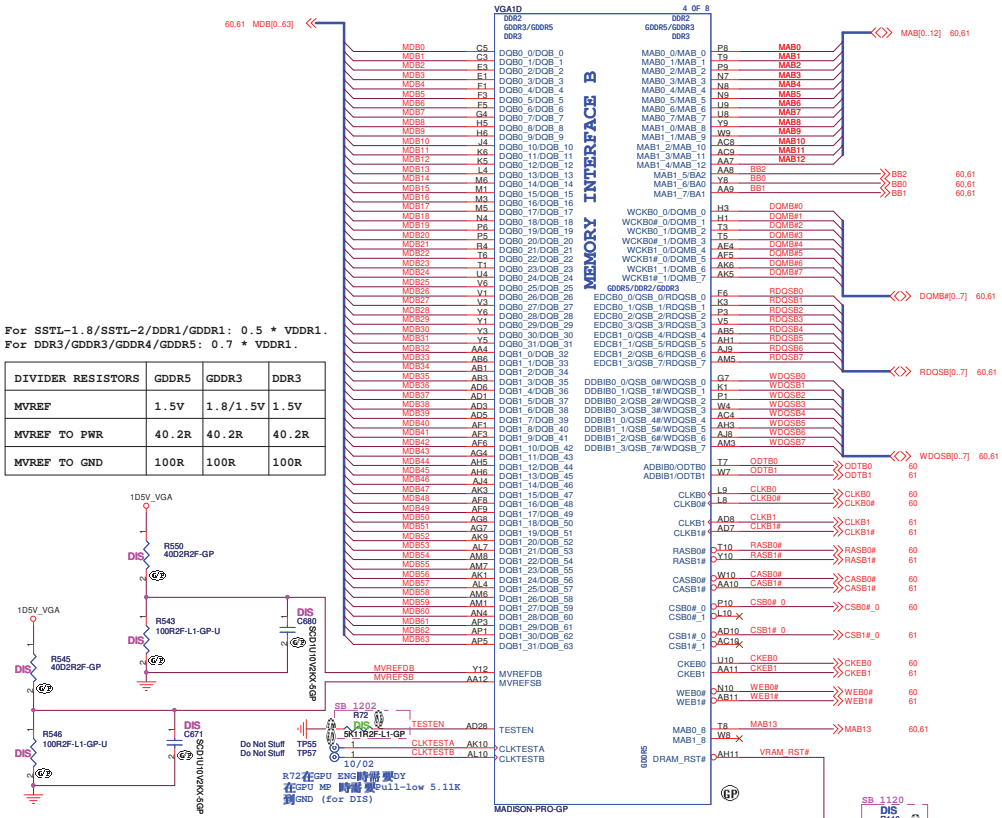



For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

| DIVIDER RESISTORS | GDDR5 | GDDR3 | DDR3 |
|---|---|---|---|
| MVREF | 1.5V | 1.8/1.5V | 1.5V |
| MVREF TO PWR | 40.2R | 40.2R | 40.2R |
| MVREF TO GND | 100R | 100R | 100R |

Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used

71.MDSON.M01
2ND = 71.0PARK.M04
DIS




For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

| DIVIDER RESISTORS | GDDR5 | GDDR3 | DDR3 |
|---|---|---|---|
| MVREF | 1.5V | 1.8/1.5V | 1.5V |
| MVREF TO PWR | 40.2R | 40.2R | 40.2R |
| MVREF TO GND | 100R | 100R | 100R |

71.MDSON.M01
2ND = 71.0PARK.M04
DIS

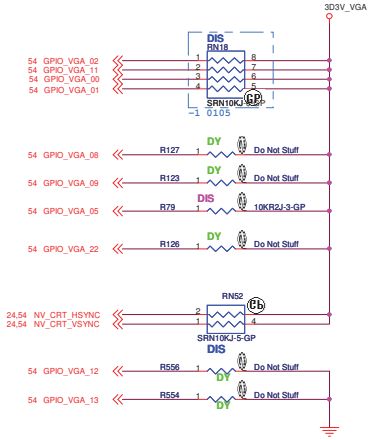
| STRAPS | PIN | DESCRIPTION | RECOMMENDED SETTINGS<br>0= DO NOT INSTALL RESISTOR<br>1 = INSTALL 10K RESISTOR<br>X = DESIGN DEPENDANT<br>NA = NOT APPLICABLE |
|---|---|---|---|
| TX_PWRS_ENB<br>(Internal PD) | GPIO0 | PCIE FULL TX OUTPUT SWING<br>Tansmitter Power Savings Enable<br>0= 50% Tx output swing<br>1= Full Tx output swing | X |
| TX_DEEMPH_EN<br>(Internal PD) | GPIO1 | Transmitter De-emphasis Enable<br>0= Tx de-emphasis disabled<br>1= Tx de-emphasis enabled | X |
| RESERVED | GPIO8 | RESERVED | 0 |
| BIF_VGA_DIS | GPIO9 | VGA ENABLED | 0 |
| RESERVED | GPIO21 | RESERVED | 0 |
| BIOS_ROM_EN | GPIO22_ROMCSB | ENABLE EXTERNAL BIOS ROM | 0 |
| VIP_DEVICE_STRAP_ENA<br>(Internal PD) | GPIO[13,12,11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT<br>if BIOS_ROM_EN=1,then Config[3:0]<br>defines the ROM type<br>if BIOS_ROM_EN=0,then Config[3:0]<br>defines the primary memory apeture size | X X X |
| RSVD | V2SYNC | | 0 |
| RSVD | H2SYNC | | 0 |
| AUD[1]<br>AUD[0]<br>(Internal PD) | VGA_HSYNC<br>VGA_VSYNC | AUD[1:0]<br>00:No audio function<br>01:Audio for DisplayPort and HDMI<br>( if adapter is detected)<br>10:Audio for DisplayPort only<br>11:Audio for both DisplayPort and HDMI | X<br>X |

## AMD RESERVED CONFIGURATION STRAPS

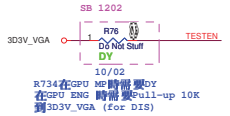
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

| If BIOS_ROM_EN (GPIO22) = 0 | | If BIOS_ROM_EN (GPIO22) = 1 | | |
|---|---|---|---|---|
| Size of the primary memory apertures | GPIO[13,12,11] | Manufacturer | Part Number | GPIO[13,12,11] |
| V 128MB | x000 | ST Microelectronics | M25P05A | 0100 |
| 256MB | x001 | | M25P10A | 0101 |
| 64MB | x010 | | M25P20 | 0101 |
| 32MB | x | | M25P40 | 0101 |
| 512MB | x | | M25P80 | 0101 |
| 1GB | x | Chingis (formerly PMC) | Pm25LV512A | 0100 |
| 2GB | x | | Pm25LV010A | 0101 |
| 4GB | x | | | |




| Designator | For M97-M2 | For Mannhatton |
|---|---|---|
| R_MEM_1 | 10K | 10K |
| R_MEM_2 | 40R/Short | 680R |
| R_MEM_3 | DY | DY |
| C_MEM | 2.2nF | 68pF |




R734在GPU MP 時需要DY
在GPU ENG 時需要Full-up 10K
到3D3V_VGA (for DIS)

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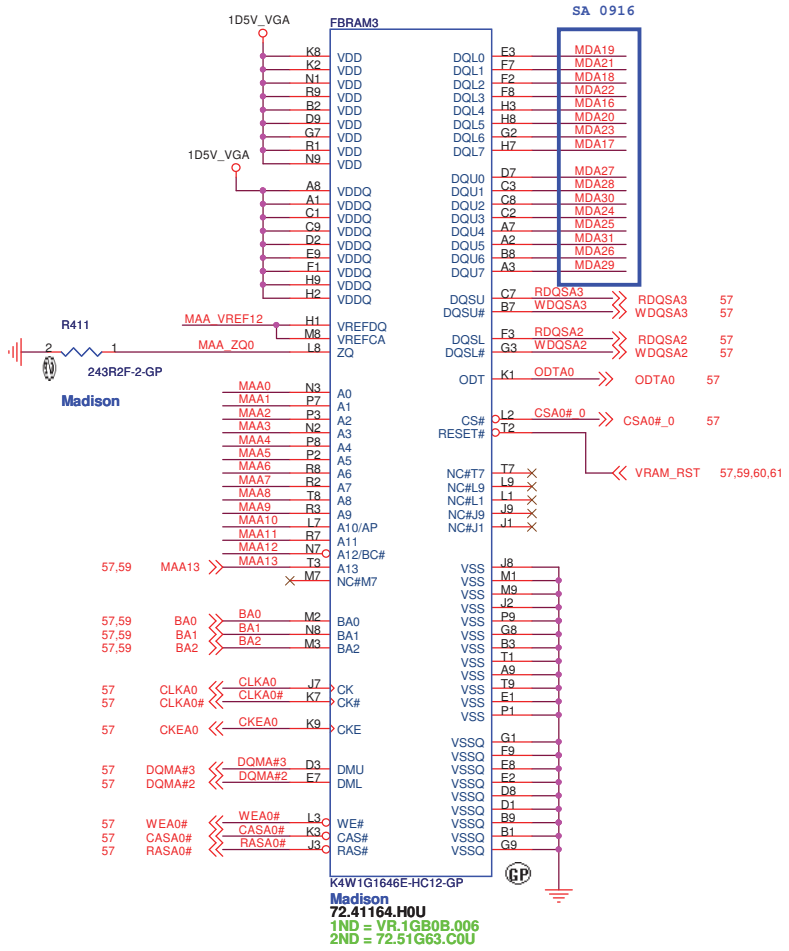
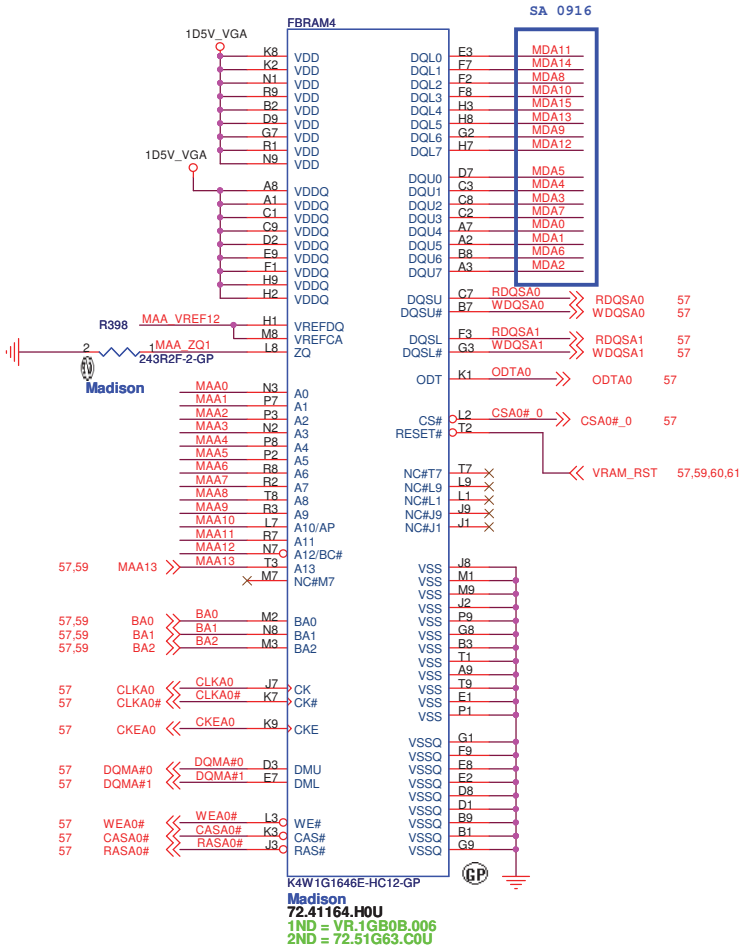
Title: Madison Memory / Straps

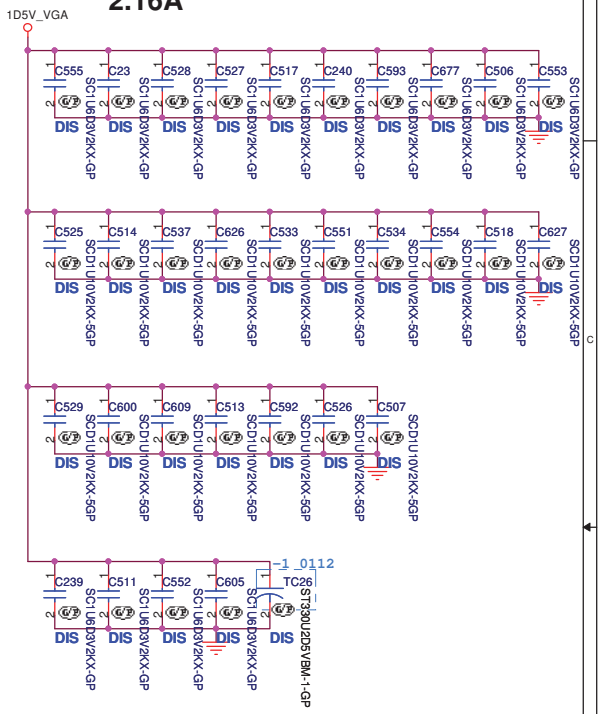
Size: A2 | Document Number: JM31-CP | Rev: SB

Date: Thursday, February 25, 2010 | Sheet 57 of 62

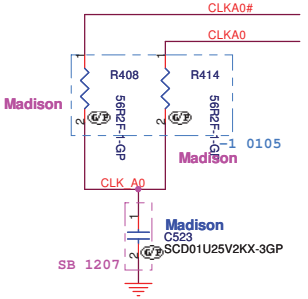
# DDR3

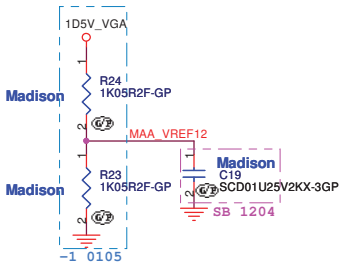



**SAMSUNG: 72.41164.H0U(VR.1GB0B.006)**
**HYNIX: 72.51G63.C0U(VR.1GB0G.004)**




57,59 DQMA#[0..7]
57,59 RDQSA[0..7]
57,59 WDQSA[0..7]
57,59 MAA[0..12] MAA[0..12]
57,59 MDA[0..63] MDA[0..63]

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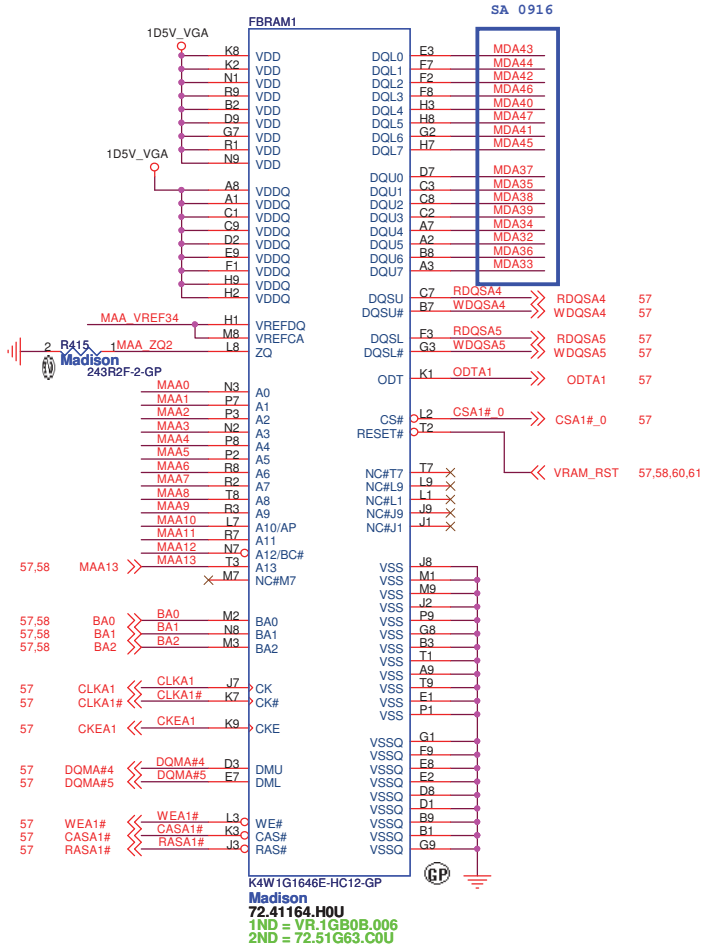
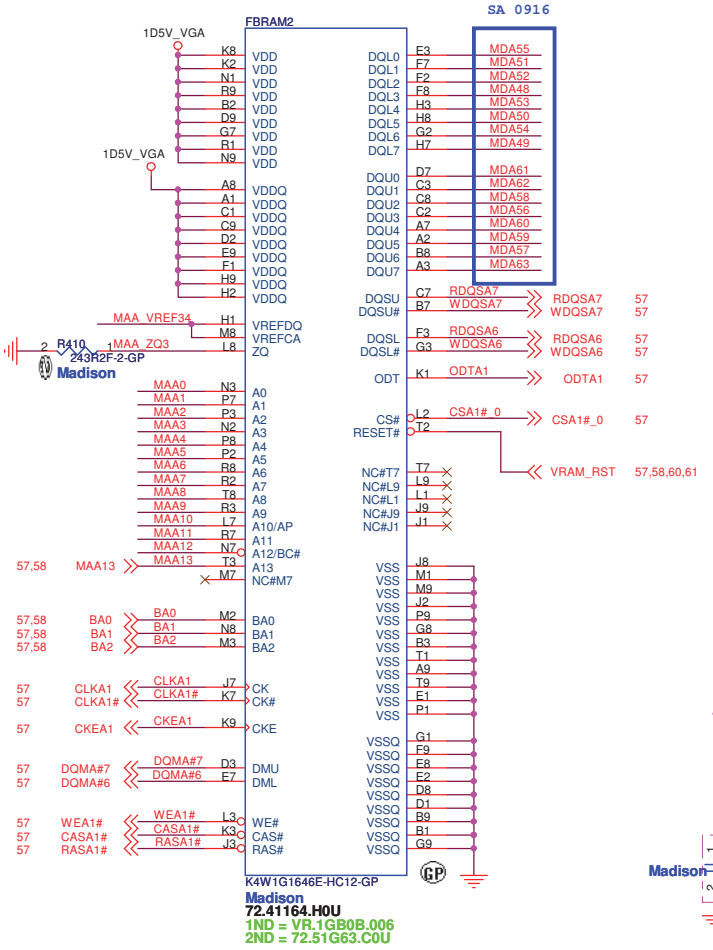
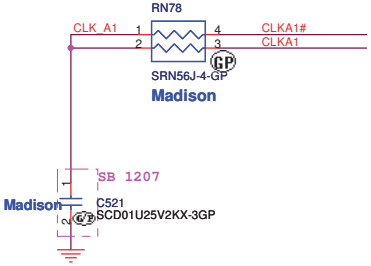
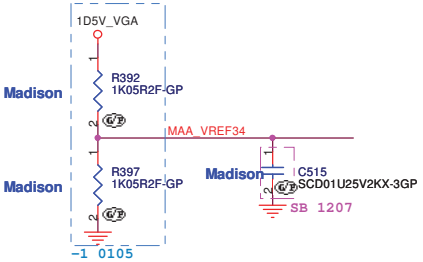
| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: *VRAM(1/4)* | | |
| Size: A3 | Document Number: JM31-CP | Rev: -1 |
| Date: Thursday, February 25, 2010 | Sheet 58 of 62 | |

# DDR3




**SAMSUNG: 72.41164.H0U(VR.1GB0B.006)**
**HYNIX: 72.51G63.C0U(VR.1GB0G.004)**

57,58 DQMA#[0..7]
57,58 RDQSA[0..7]
57,58 WDQSA[0..7]
57,58 MAA[0..12] MAA[0..12]
57,58 MDA[0..63] MDA[0..63]

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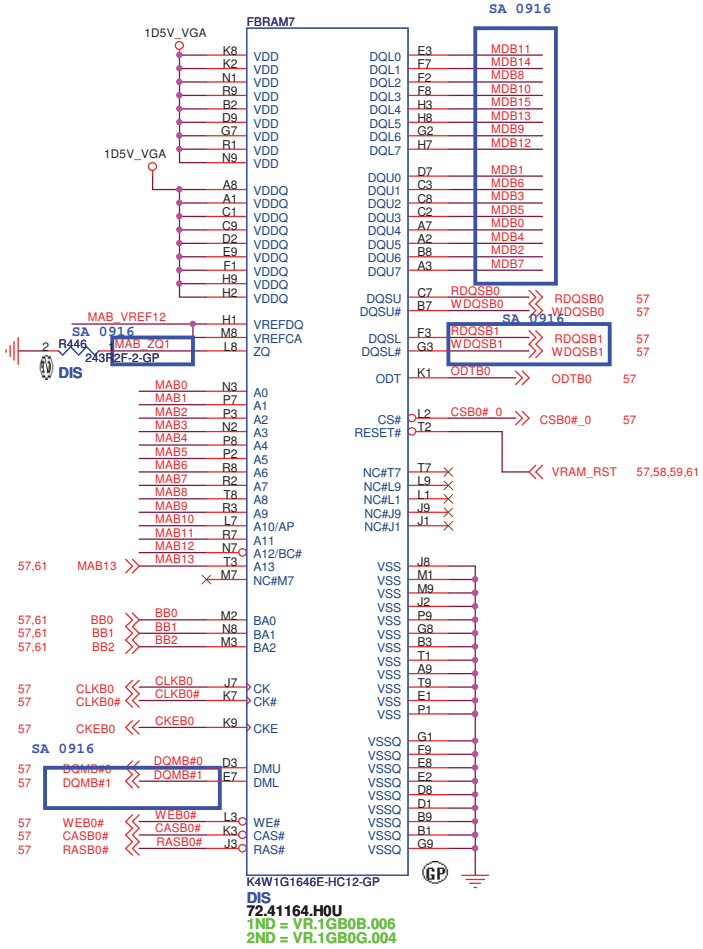
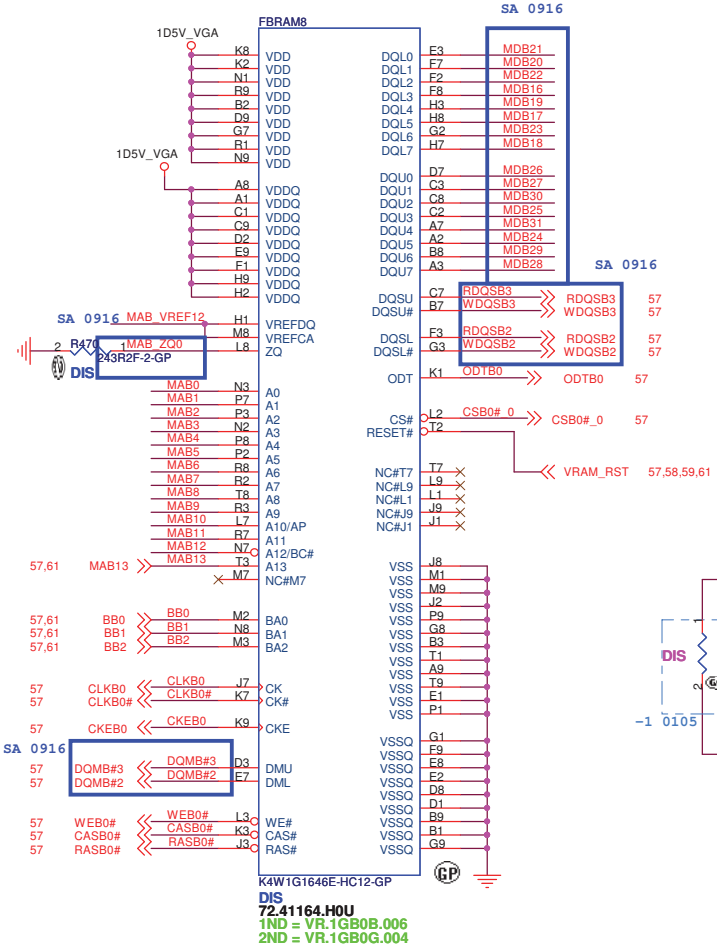
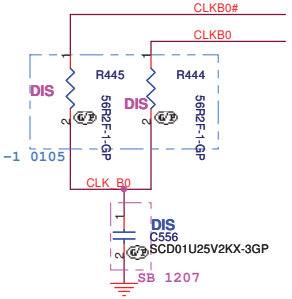
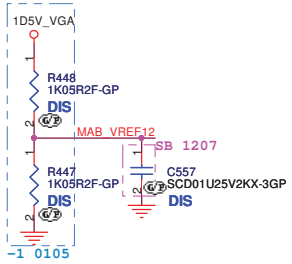
| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: VRAM(2/4) | | |
| Size: A3 | Document Number: JM31-CP | Rev: -1 |
| Date: Thursday, February 25, 2010 | Sheet 59 of 62 | |

# DDR3




**SAMSUNG: 72.41164.H0U(VR.1GB0B.006)**
**HYNIX: 72.51G63.C0U(VR.1GB0G.004)**

57,61 DQMB#[0..7]
57,61 RDQSB[0..7]
57,61 WDQSB[0..7]
57,61 MAB[0..12] MAB[0..12]
57,61 MDB[0..63] MDB[0..63]

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *VRAM(3/4)*

| Size | Document Number | Rev |
|---|---|---|
| A3 | JM31-CP | -1 |

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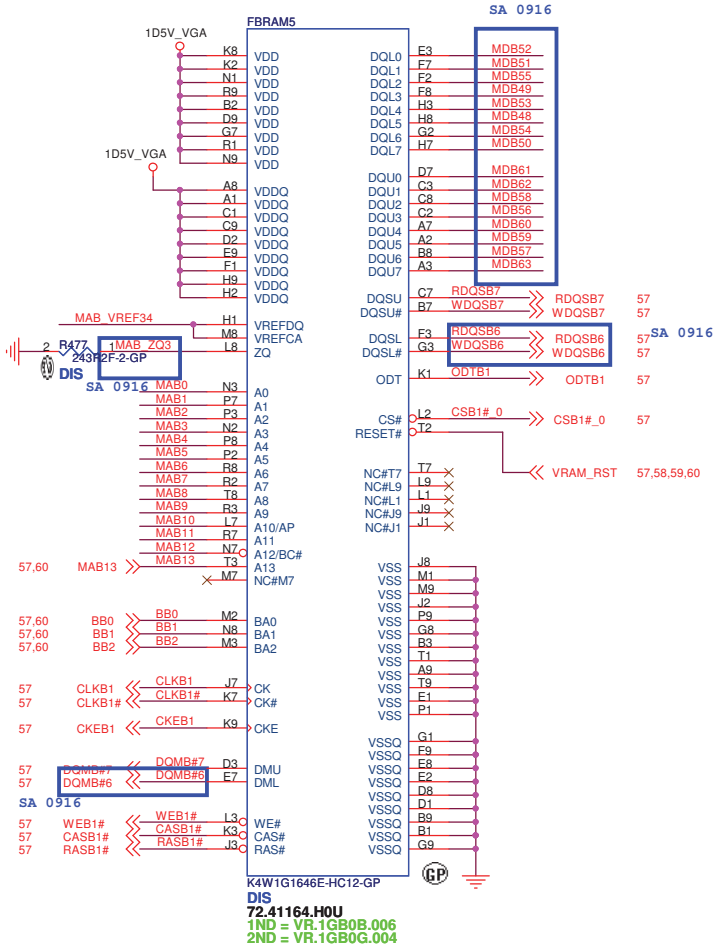
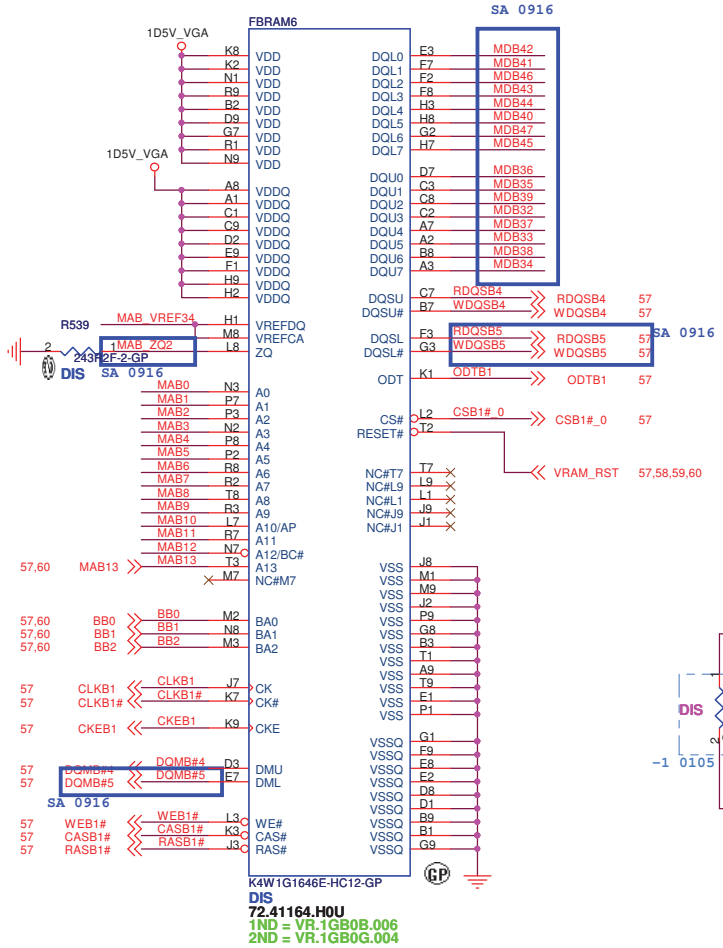
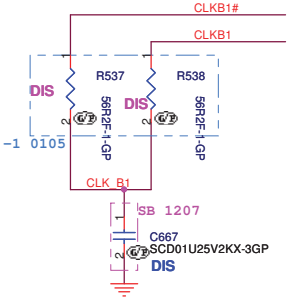
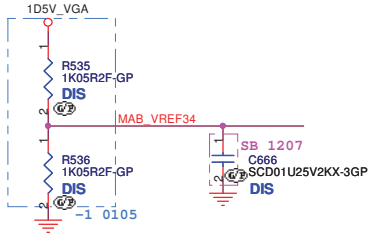
# DDR3

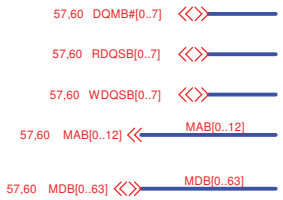



SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)

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| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: VRAM(4/4) | | |
| Size: A3 | Document Number: JM31-CP | Rev: -1 |
| Date: Thursday, February 25, 2010 | Sheet 61 of 62 | |

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Modify History***

| Size | Document Number | Rev |
|---|---|---|
| | JM31-CP | SA |

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