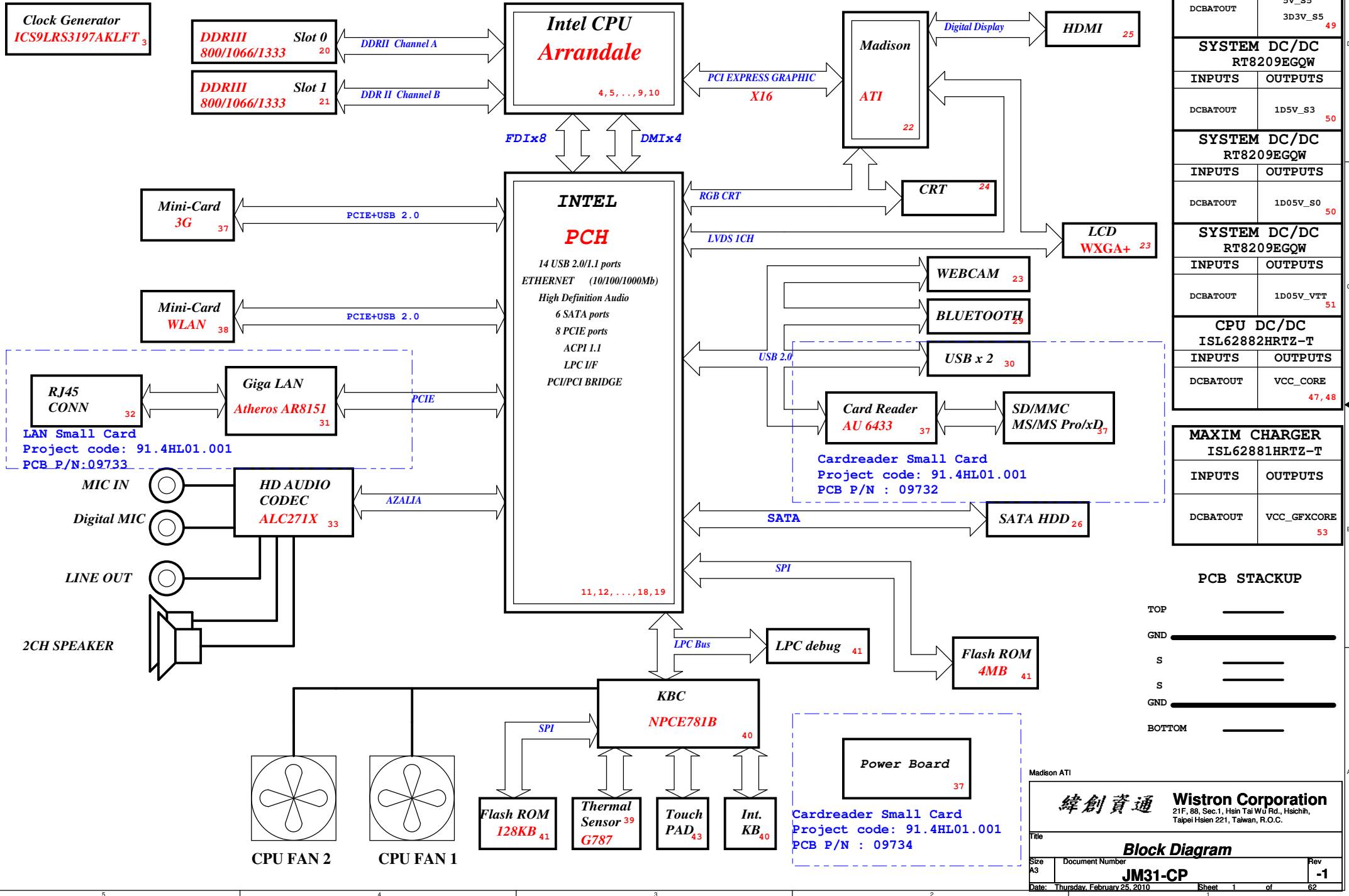


JM31-CP Block Diagram

Project code: 91.4HL01.001

PCB P/N : 48.4HL01.031

REVISION : 09921-3



A B

PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB1
1	USB2
2	USB4
3	MINICARD2
4	WECAM
5	Blue Tooth
6	MINIC1
7	Cardreader
8	NC
9	NC
10	NC
11	NC
12	NC
13	NC

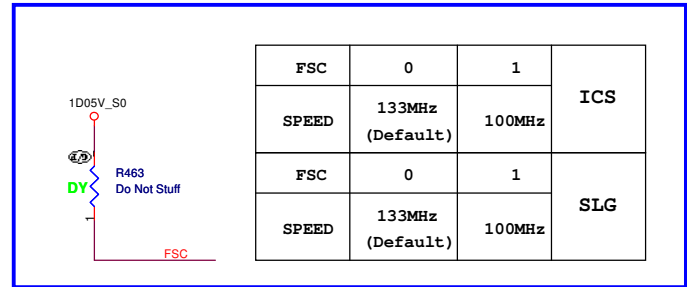
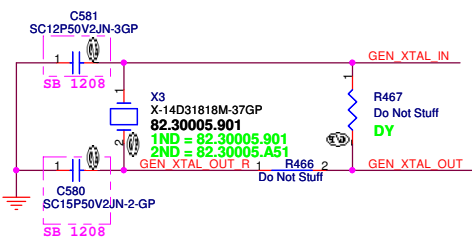
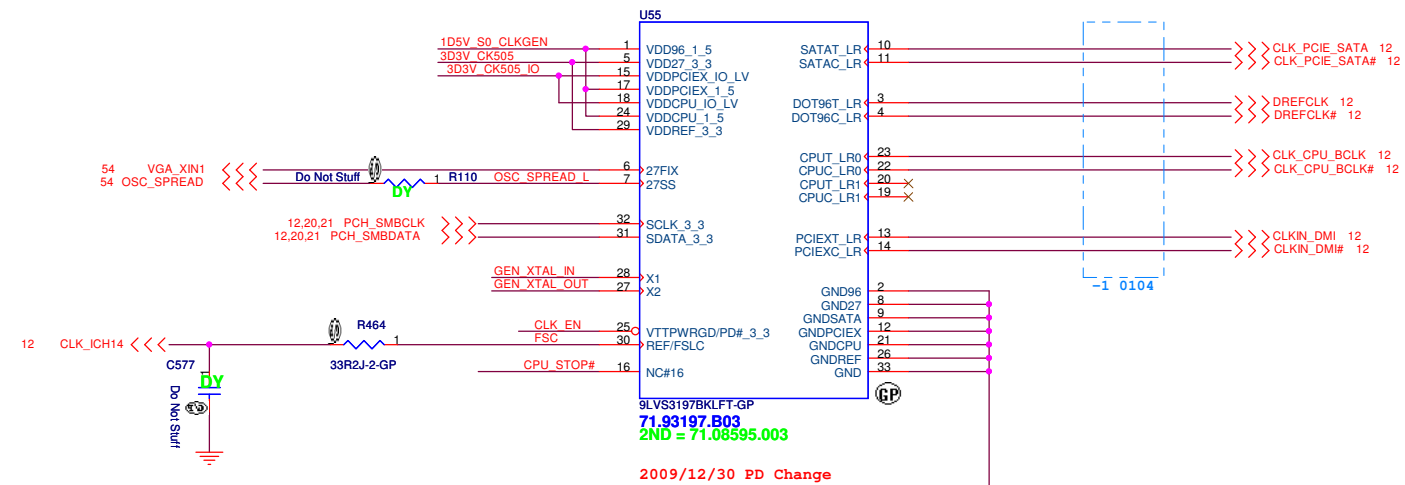
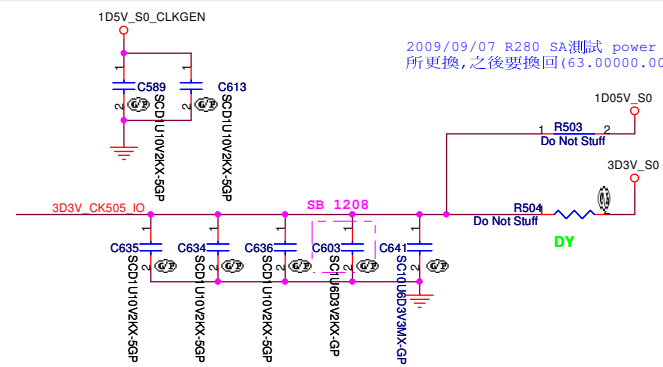
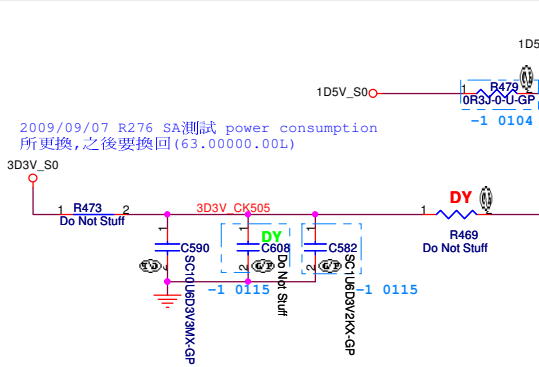
C D E

Processor Strapping

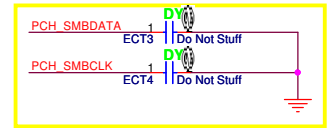
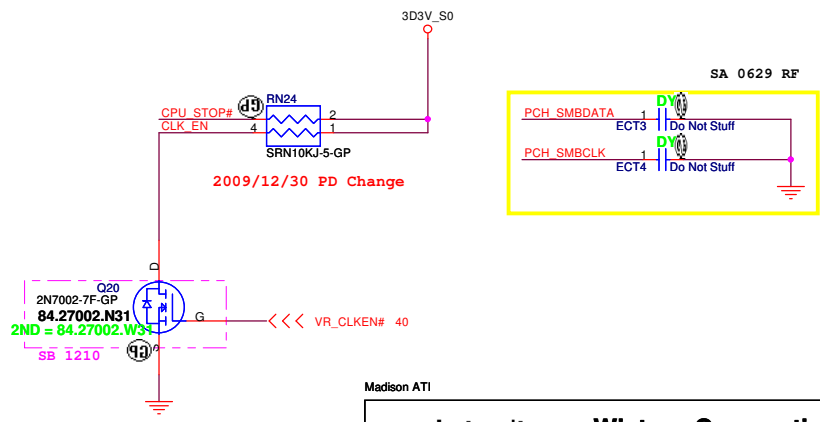
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

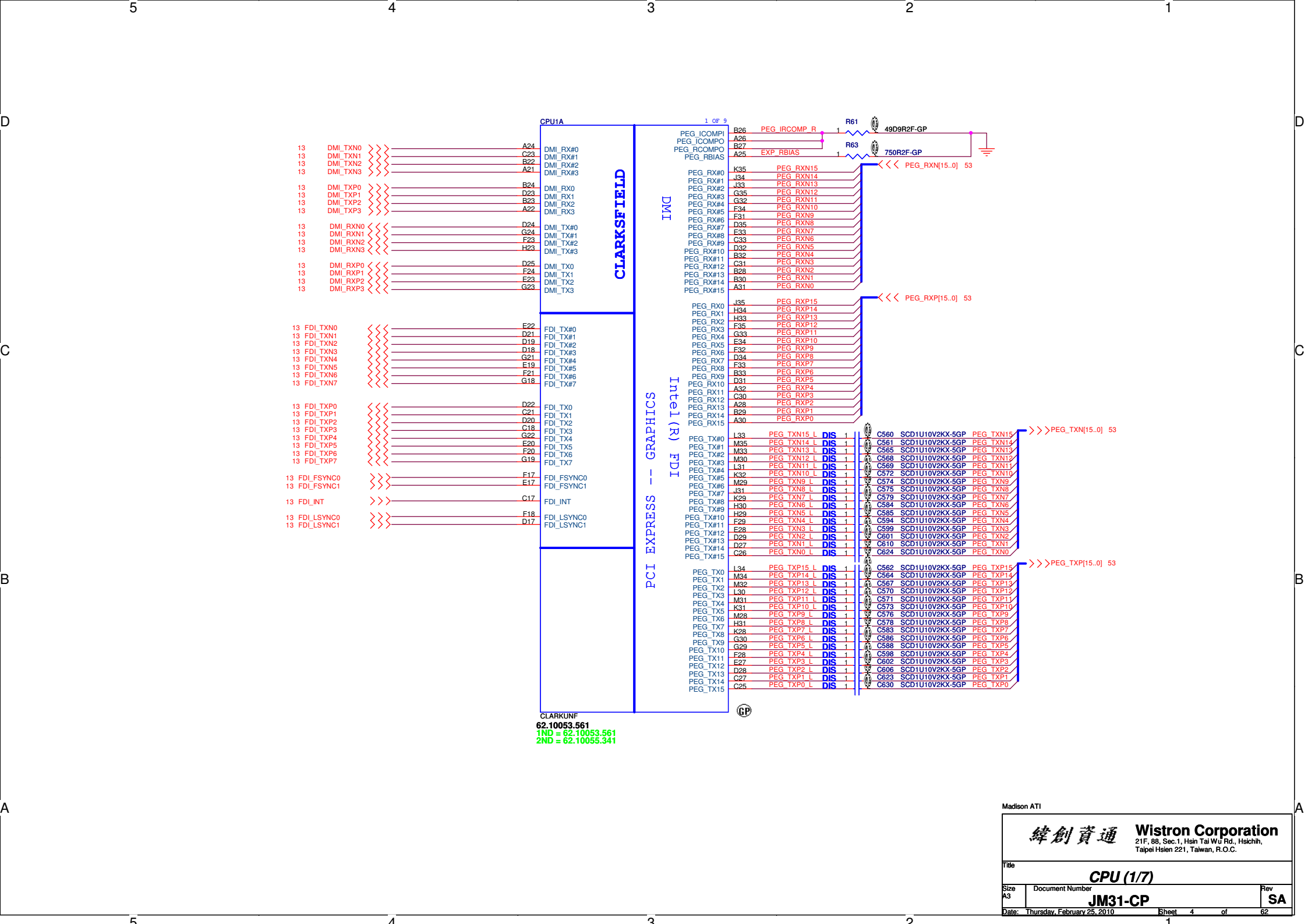
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Title			
Table of Content			
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FSC	0	1	ICS
SPEED	133MHz (Default)	100MHz	
FSC	0	1	SLG
SPEED	133MHz (Default)	100MHz	



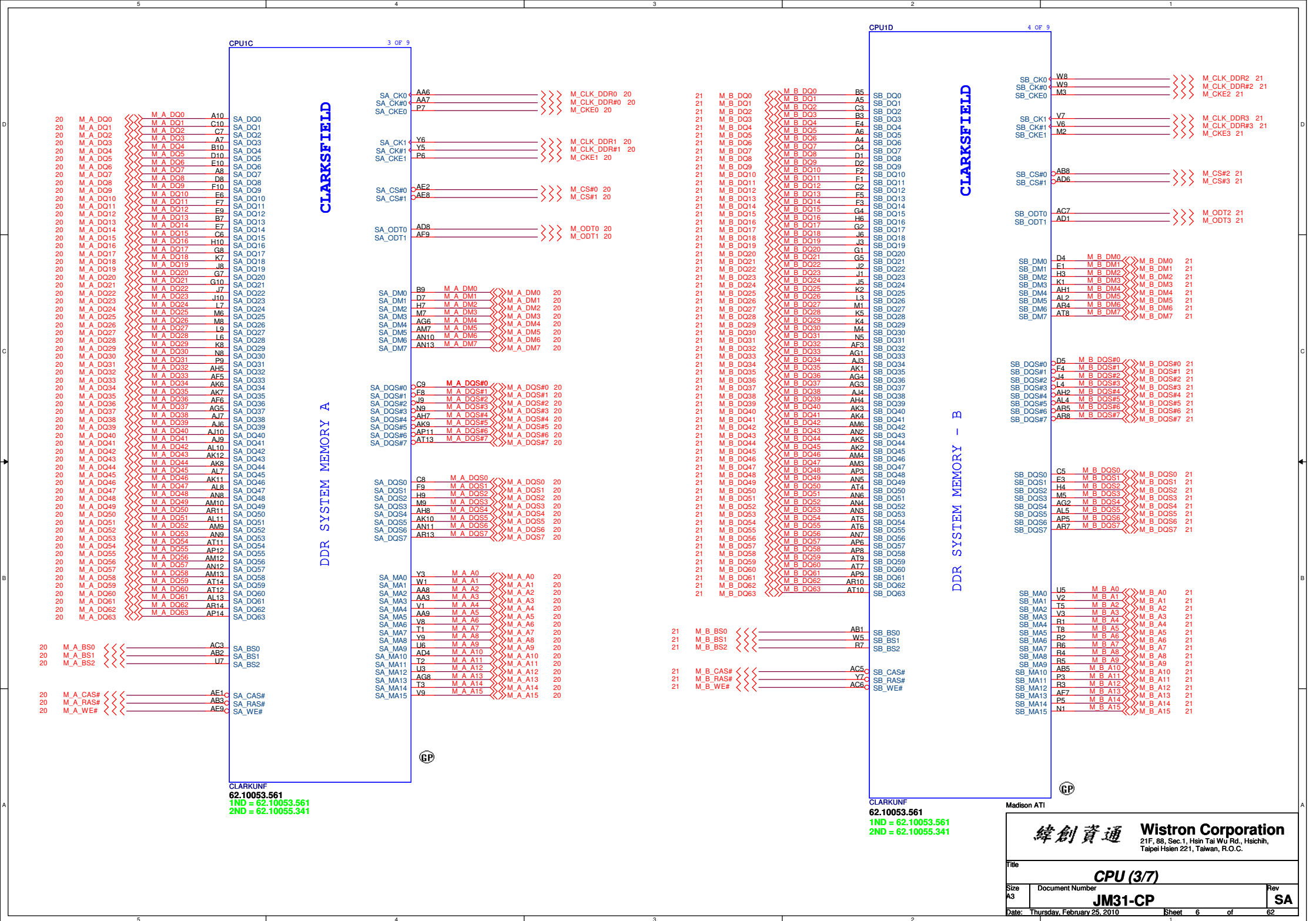


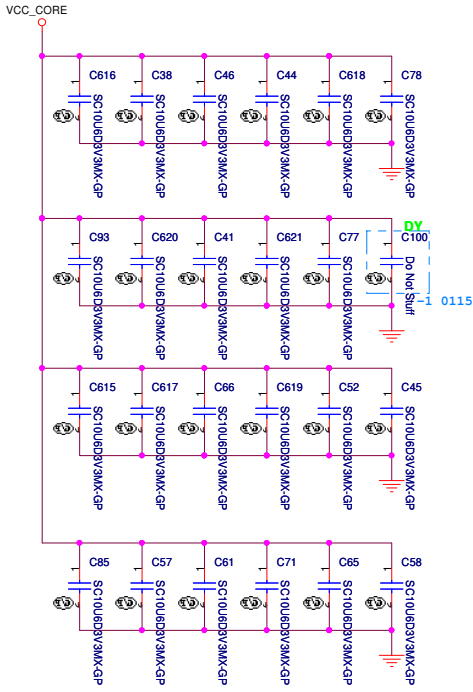
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Title		
CPU (1/7)		
Size	Document Number	Rev
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PROCESSOR CORE POWER

48A

VCC_CORE

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- V35 VCC
- V34 VCC
- V33 VCC
- V32 VCC
- V31 VCC
- V30 VCC
- V29 VCC
- V28 VCC
- V27 VCC
- V26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- P35 VCC
- P34 VCC
- P33 VCC
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- P27 VCC
- P26 VCC

CLARKSFIELD

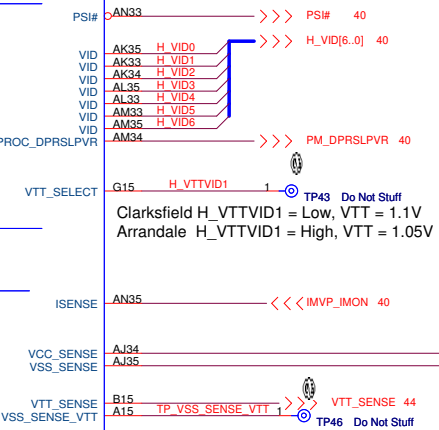
1.1V RAIL POWER

CPU CORE SUPPLY

POWER

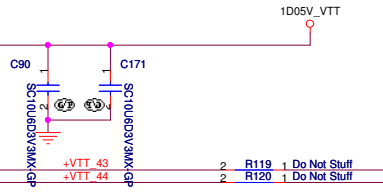
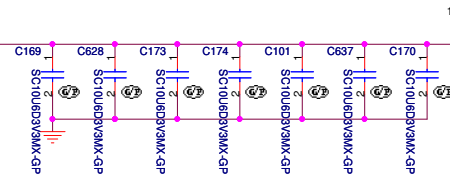
CPD VIDS

SENSE SENSE



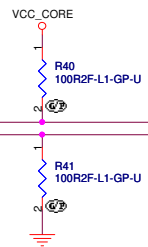
- AH14 VTT0
- AH12 VTT0
- AH11 VTT0
- AH10 VTT0
- J14 VTT0
- J13 VTT0
- H14 VTT0
- H12 VTT0
- G14 VTT0
- G13 VTT0
- G12 VTT0
- F14 VTT0
- F13 VTT0
- F12 VTT0
- F11 VTT0
- E14 VTT0
- E12 VTT0
- D14 VTT0
- D12 VTT0
- D11 VTT0
- C14 VTT0
- C13 VTT0
- C12 VTT0
- C11 VTT0
- B14 VTT0
- B12 VTT0
- A14 VTT0
- A13 VTT0
- A12 VTT0
- A11 VTT0

- AF10 VTT0
- AE10 VTT0
- AC10 VTT0
- AB10 VTT0
- Y10 VTT0
- W10 VTT0
- U10 VTT0
- T10 VTT0
- J12 VTT0
- J11 VTT0
- J16 VTT0
- J15 VTT0

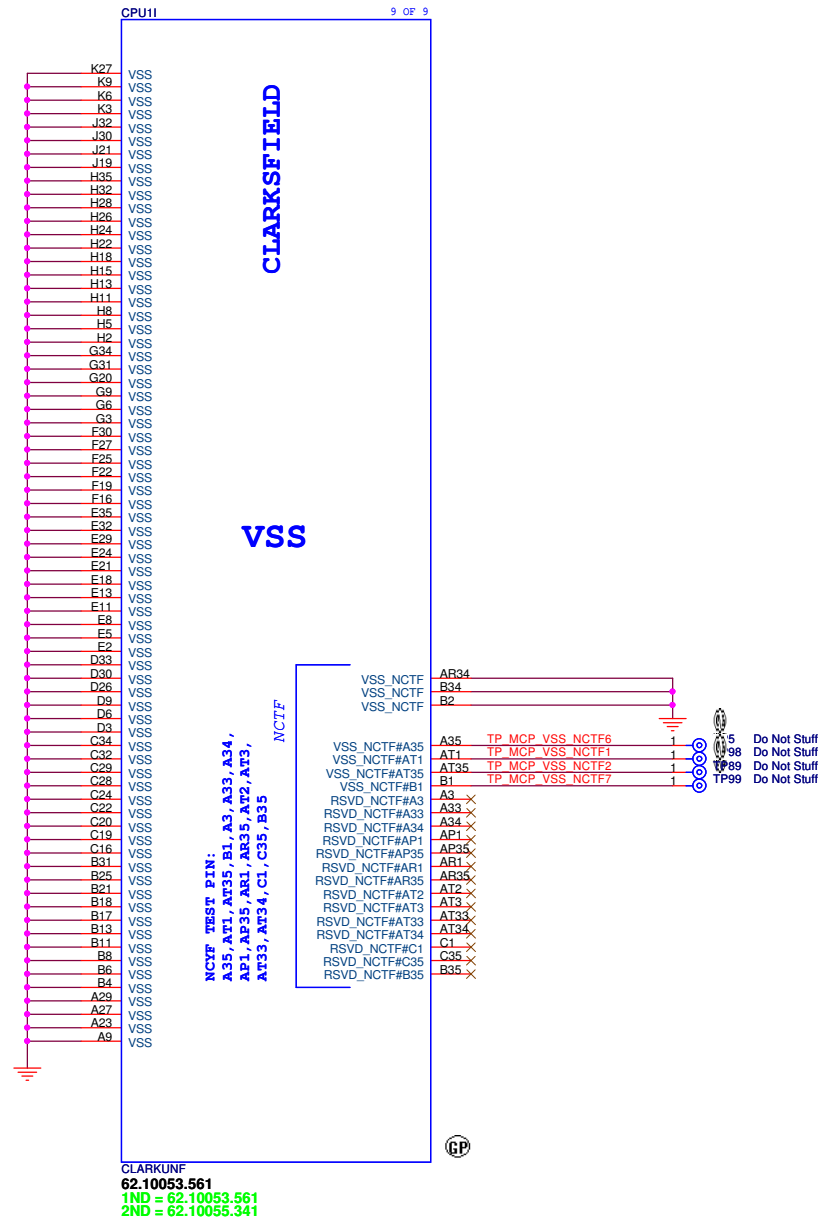
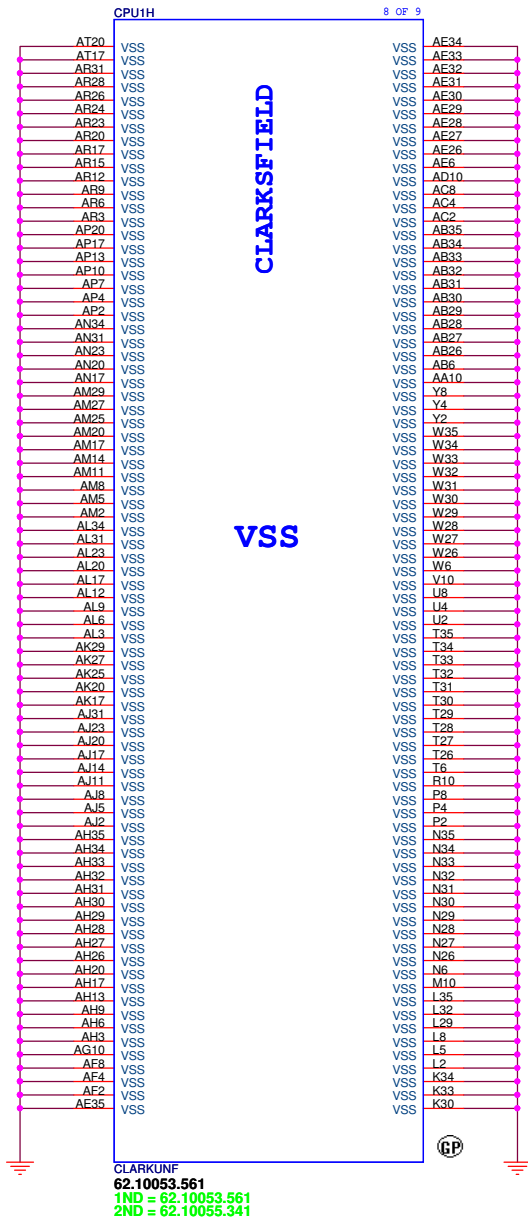


The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarkfield VTT=1.1V



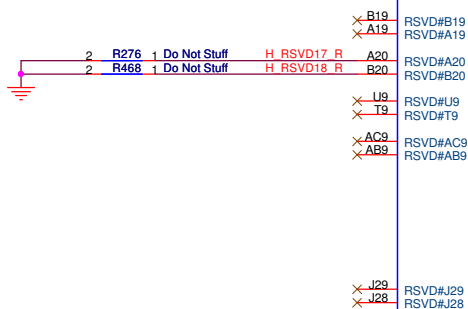
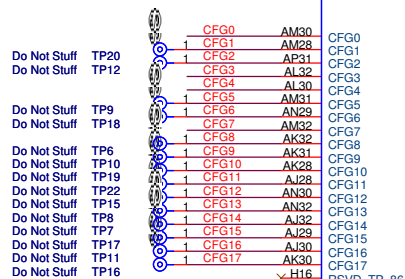
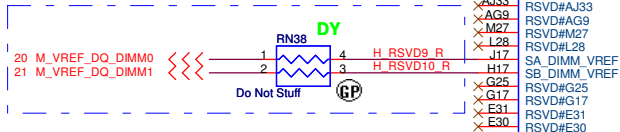
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SO-DIMM VREFDQ (M3) Circuit for Clarkfield Processor



CPU1E

CLARKFIELD

RESERVED

CLARKUNF

62.10053.561

1ND = 62.10053.561

2ND = 62.10055.341

RSVD#AJ13
RSVD#AJ12

RSVD#AH25
RSVD#AK26
RSVD#AL26
RSVD#NCTF_37
RSVD#AJ26
RSVD#AJ27

SA_DIMM_VREF
SB_DIMM_VREF
RSVD#G25
RSVD#G17
RSVD#E31
RSVD#E30

RSVD#AL28
RSVD#AL29
RSVD#AP30
RSVD#AP32
RSVD#AL27
RSVD#AT31
RSVD#AT32
RSVD#AP33
RSVD#AR33

RSVD#AR32

RSVD_TP#E15
RSVD_TP#F15
KEY
RSVD#D15
RSVD#C15
RSVD#AJ15
RSVD#AH15

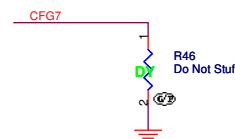
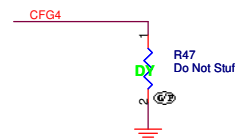
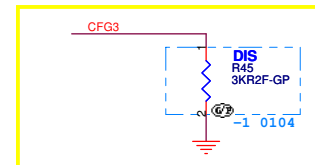
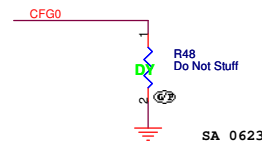
RSVD64 R 2 R483 1 Do Not Stuff
RSVD65 R 2 R697 1 Do Not Stuff

SA_CK2
SA_CK#2
SA_CKE2
SA_CS#2
SA_ODT2
SA_CK3
SA_CK#3
SA_CKE3
SA_CS#3
SA_ODT3

SB_CK2
SB_CK#2
SB_CKE2
SB_CS#2
SB_ODT2
SB_CK3
SB_CK#3
SB_CKE3
SB_CS#3
SB_ODT3

VSS AP34 RSVD VSS 2 R39 1 Do Not Stuff

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

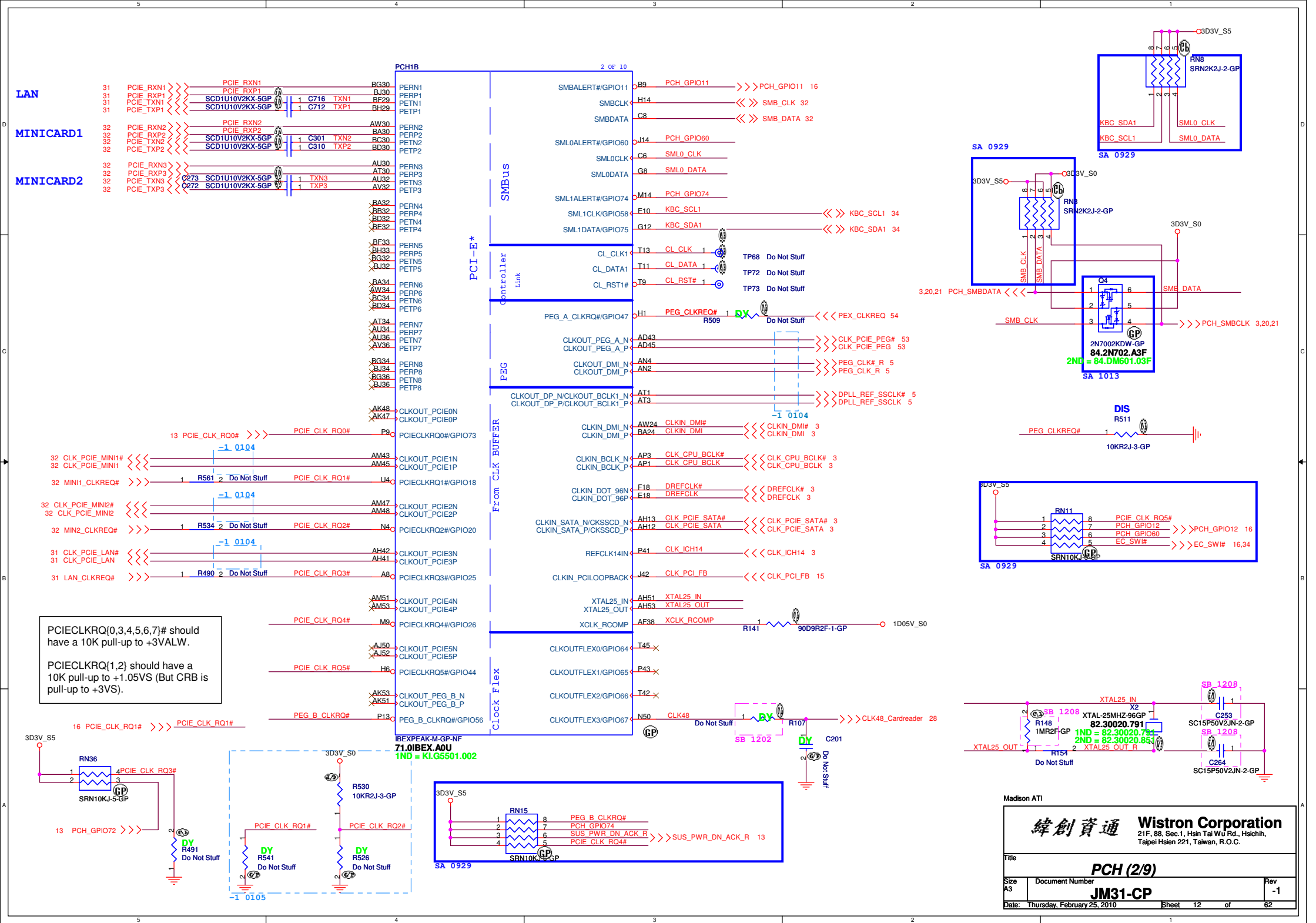
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarkfield samples.	
CFG7	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

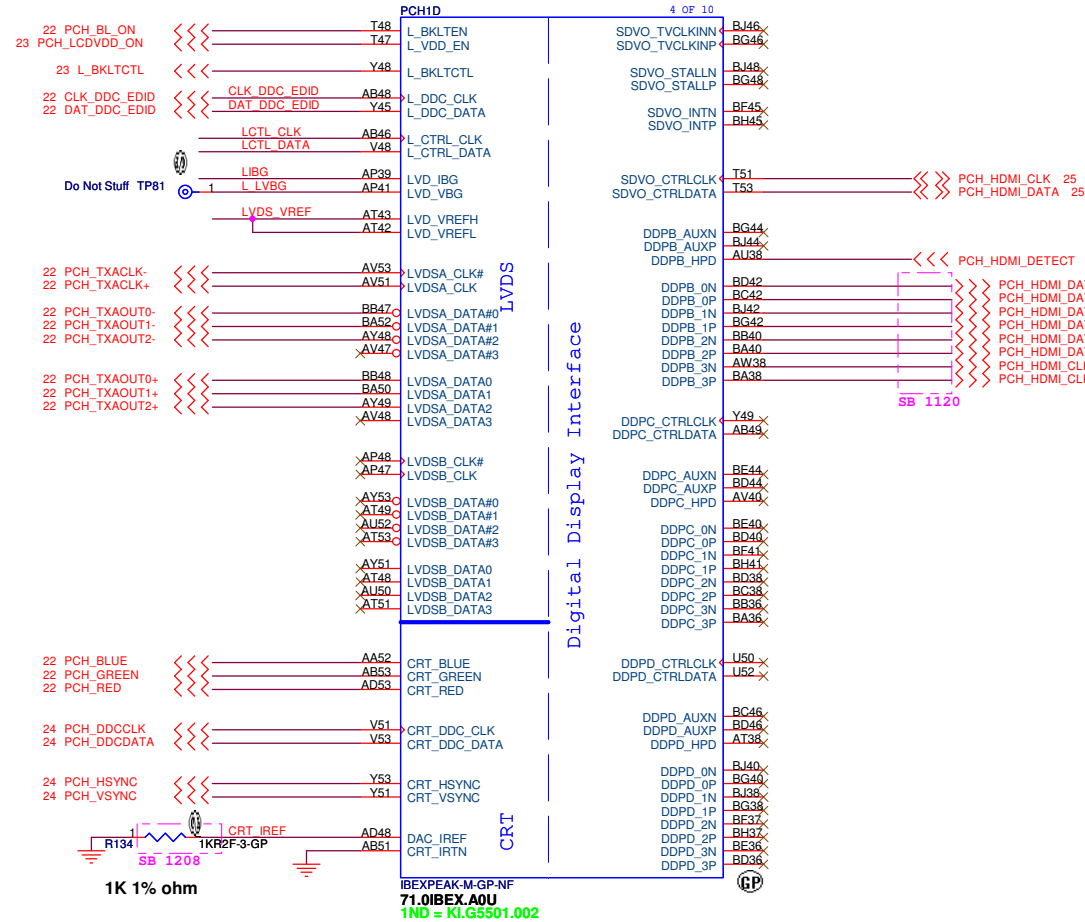
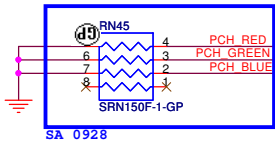
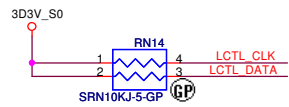
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Title		CPU (7/7)	
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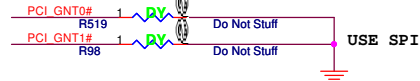
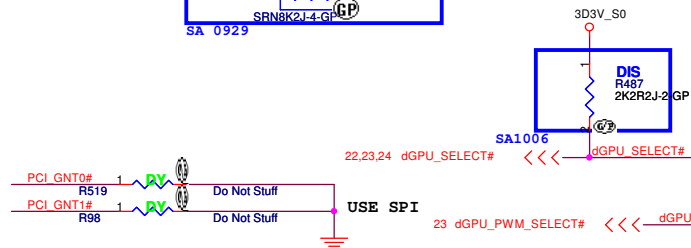
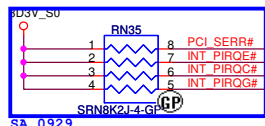
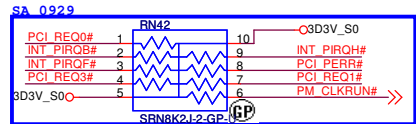
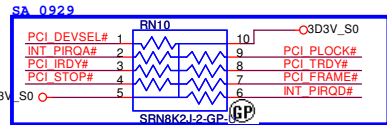




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Title			
PCH (4/9)			
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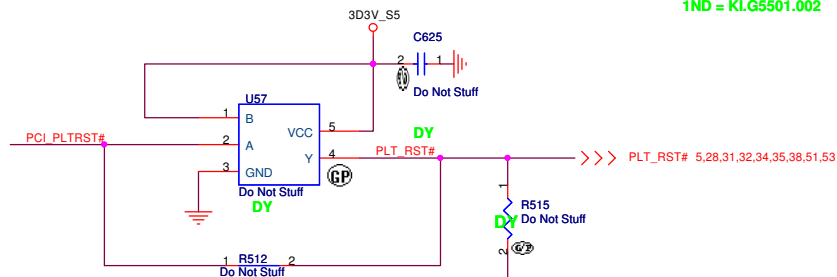
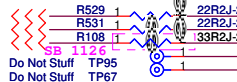
These pins are left as NC,
because the function is disable.



BOOT BIOS Strap

PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC (Default)
1	0	Reserved
0	1	PCI
1	1	SPI

35 POLK_FWH
12 CLK_PCI_FB
34 CLK_PCI_KBC



PCH1E
H40 AD0
N34 AD1
C44 AD2
A38 AD3
C36 AD4
J34 AD5
A40 AD6
D45 AD7
E36 AD8
H48 AD9
E40 AD10
C40 AD11
M48 AD12
M45 AD13
F53 AD14
M40 AD15
M43 AD16
J36 AD17
K48 AD18
F40 AD19
C42 AD20
K46 AD21
M51 AD22
J52 AD23
K51 AD24
L34 AD25
F42 AD26
J40 AD27
G46 AD28
F44 AD29
M47 AD30
H36 AD31

INT PIROA# G38
INT PIROB# H51
INT PIROC# B37
INT PIROD# A44
PCI REQ0# F51
PCI REQ1# A46
PCI REQ2# F45
PCI REQ3# M53
PCI GNT0# F48
PCI GNT1# K46
PCI GNT2# F36
PCI GNT3# H53
INT PIROE# B41
INT PIROF# K53
INT PIROG# A36
INT PIROH# A48
PCI SERR# E44
PCI PERR# E50
PCI IRDY# A42
PCI DEVSSEL# H44
PCI FRAME# C46
PCI PLOCK# D49
PCI STOP# D41
PCI TRDY# C48
ICH PME# M7
PCI PLTRST# D5
CLK_PCI_SIO_R N52
CLK_PCI_FB_R P53
CLK_PCI_KBC_R P46
CLK_PCI_3 P51
CLK_PCI_4 P48

PIROA#
PIROB#
PIROC#
PIROD#
REQ0#
REQ1#/GPIO50
REQ2#/GPIO52
REQ3#/GPIO54
GNT0#
GNT1#/GPIO51
GNT2#/GPIO53
GNT3#/GPIO55
PIROE#/GPIO2
PIROF#/GPIO3
PIROG#/GPIO4
PIROH#/GPIO5
PCIRST#
SERR#
PERR#
IRDY#
PAR
DEVSSEL#
FRAME#
PLOCK#
STOP#
TRDY#
PME#
PLTRST#
CLKOUT_PCI0
CLKOUT_PCI1
CLKOUT_PCI2
CLKOUT_PCI3
CLKOUT_PCI4

IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KL.G5501.002

PCI

USB

USB

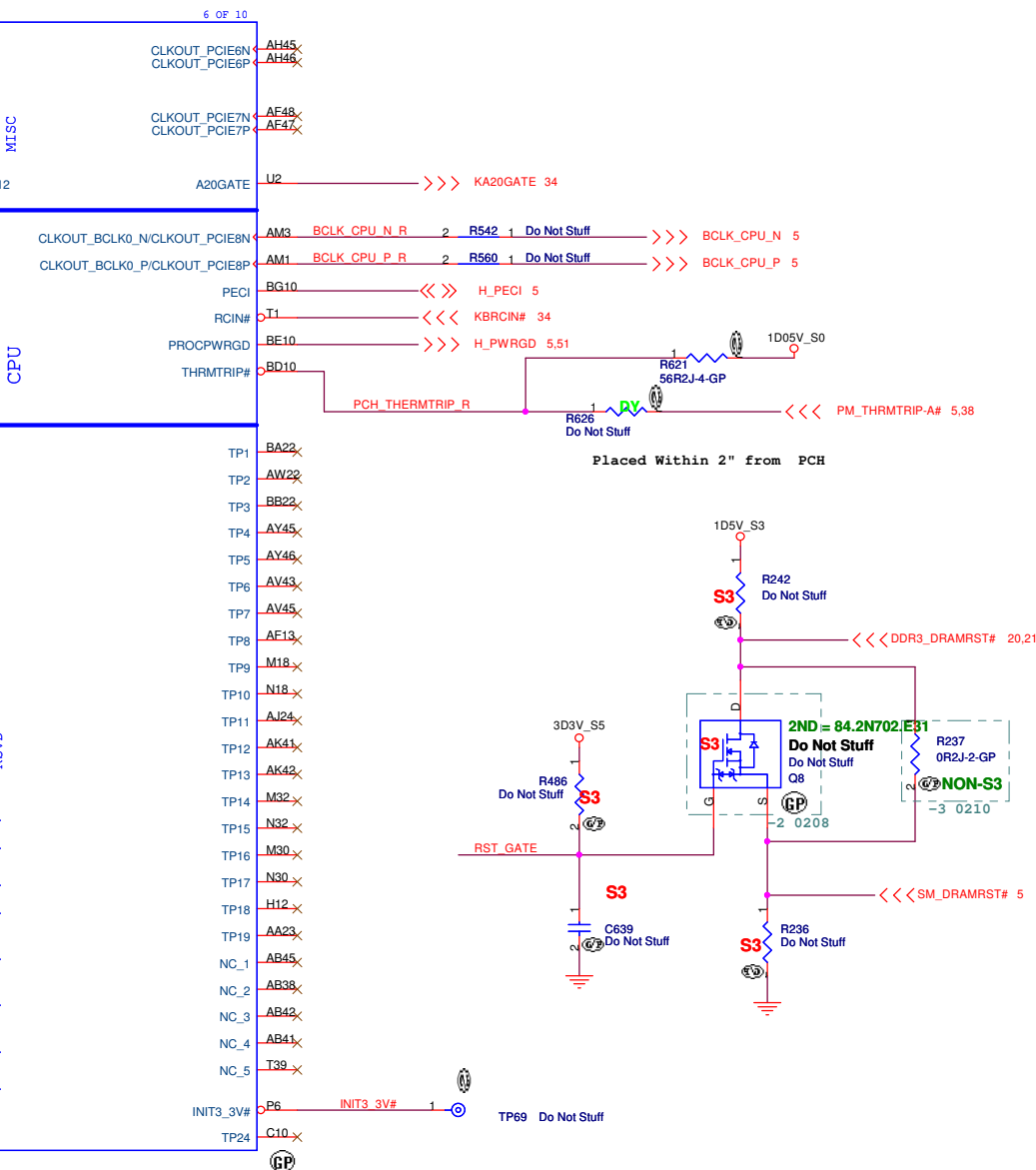
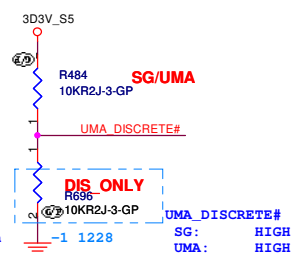
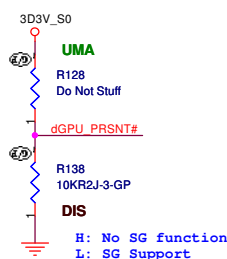
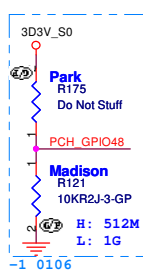
NVRAM

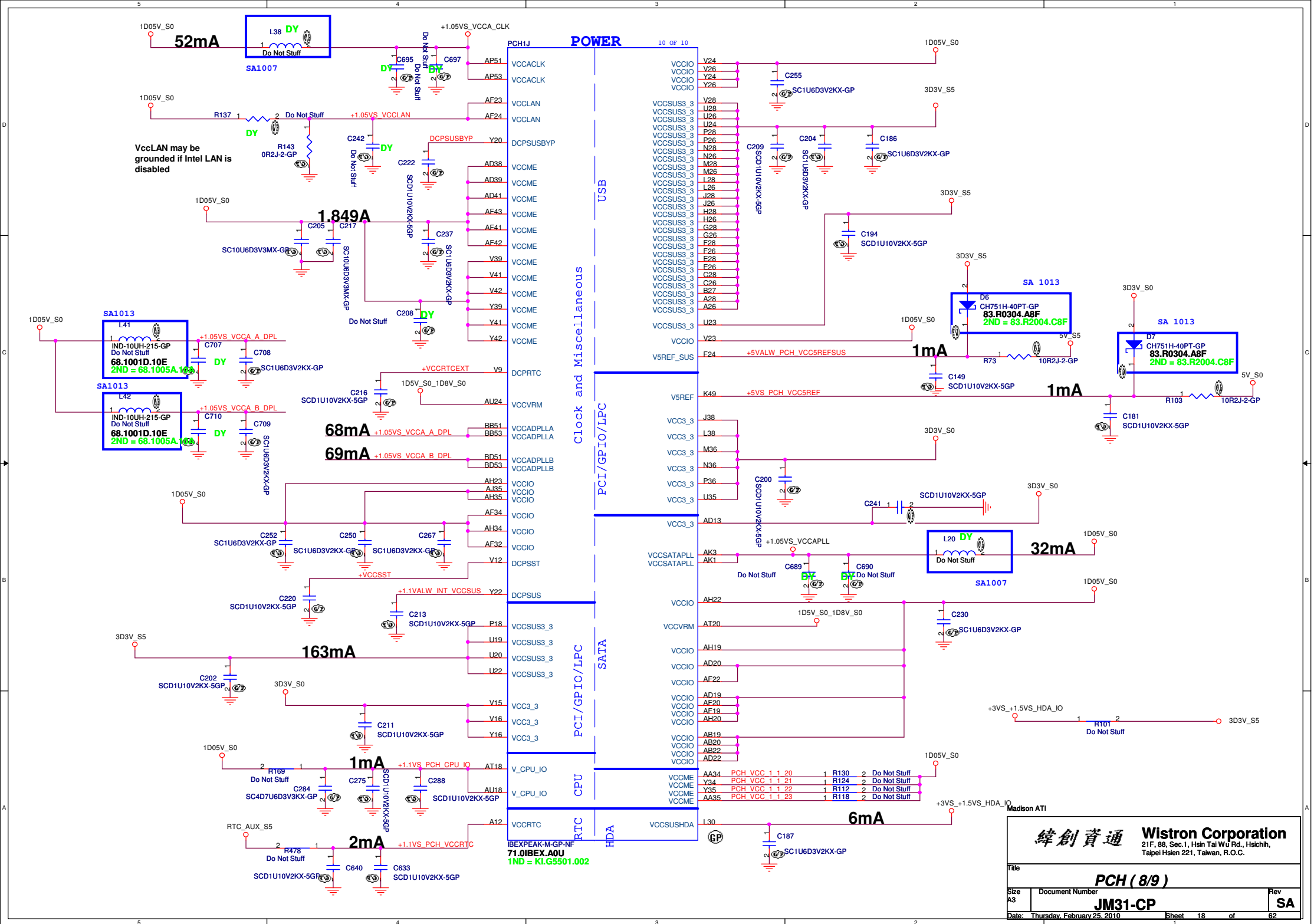
5 OF 10
NV_CE#0
NV_CE#1
NV_CE#2
NV_CE#3
NV_DQ#0
NV_DQ#1
NV_DQ#2
NV_DQ#3
NV_DQ#4
NV_DQ#5
NV_DQ#6
NV_DQ#7
NV_DQ#8
NV_DQ#9
NV_DQ#10
NV_DQ#11
NV_DQ#12
NV_DQ#13
NV_DQ#14
NV_DQ#15
NV_DQ#16
NV_DQ#17
NV_DQ#18
NV_DQ#19
NV_DQ#20
NV_DQ#21
NV_DQ#22
NV_DQ#23
NV_DQ#24
NV_DQ#25
NV_DQ#26
NV_DQ#27
NV_DQ#28
NV_DQ#29
NV_DQ#30
NV_DQ#31
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NV_WR#1_RE#
NV_WE#_CK0
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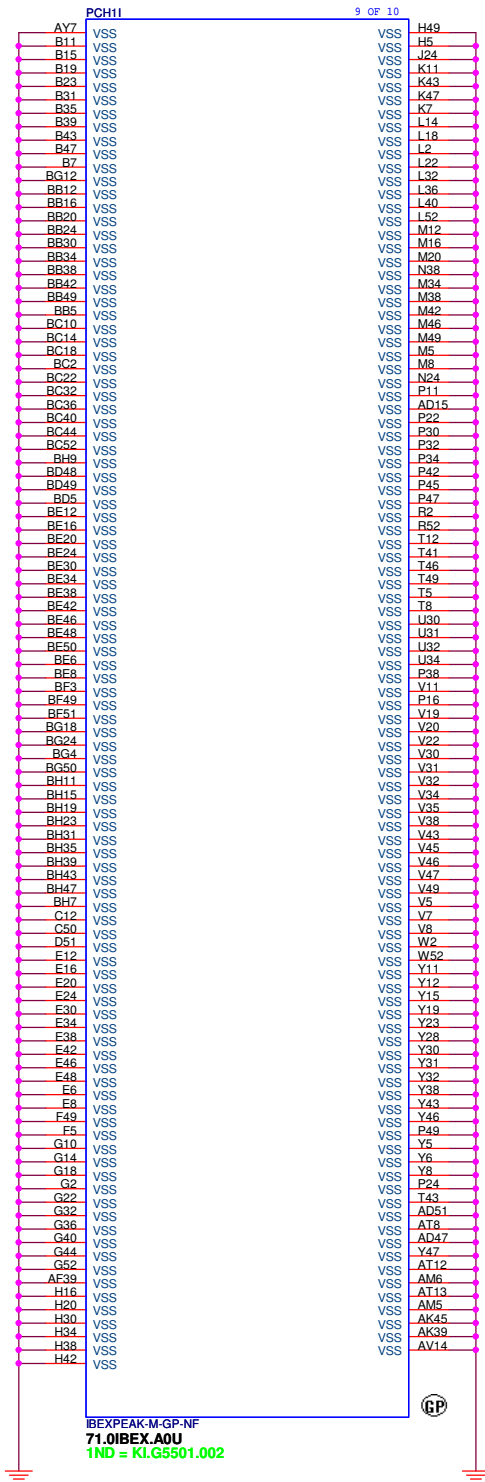
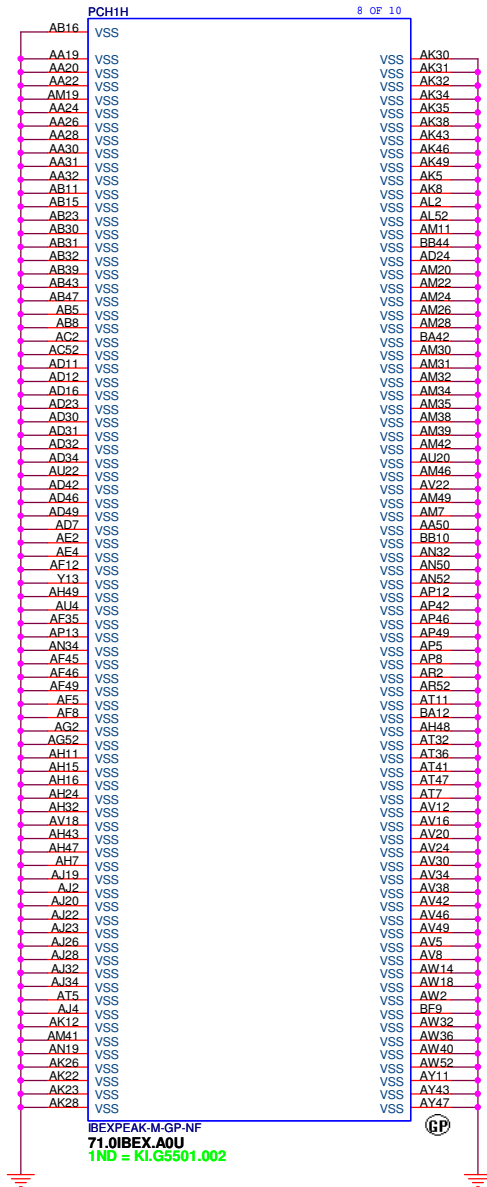
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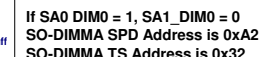
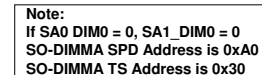
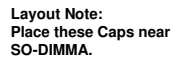
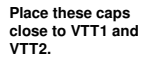
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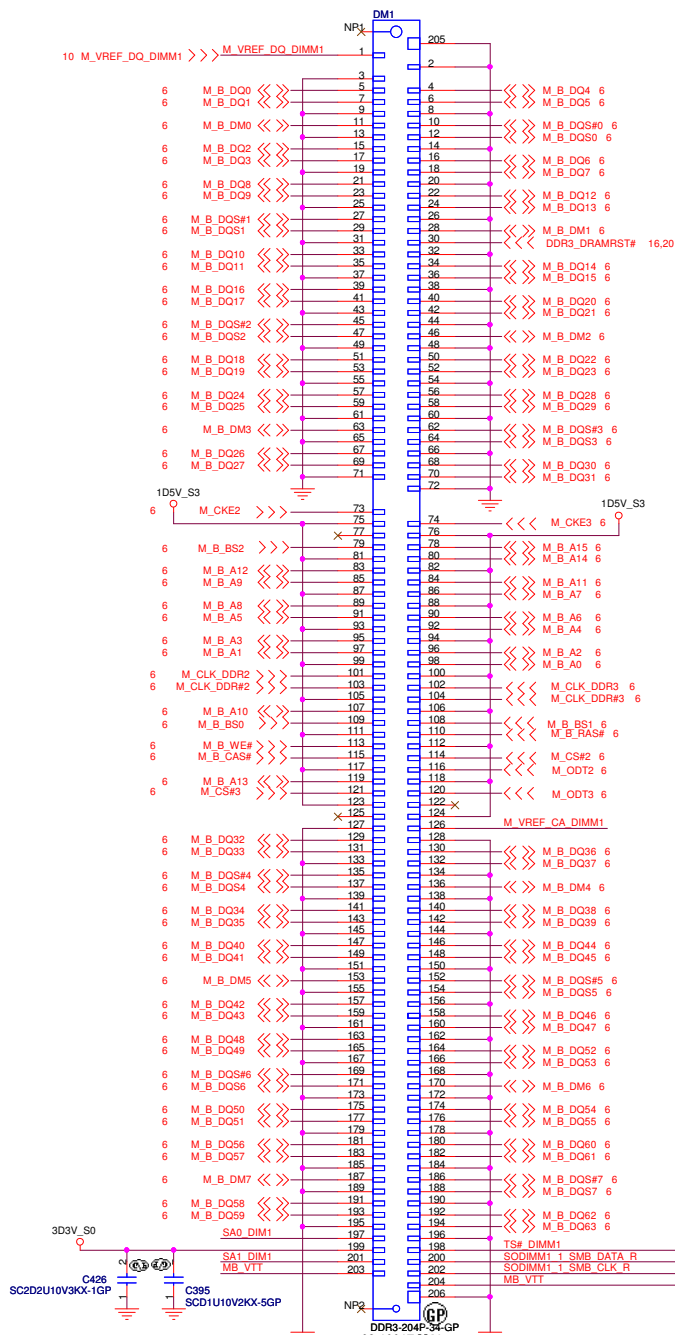
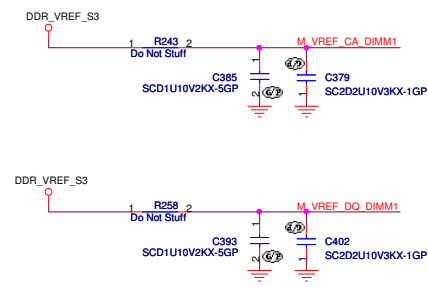
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.







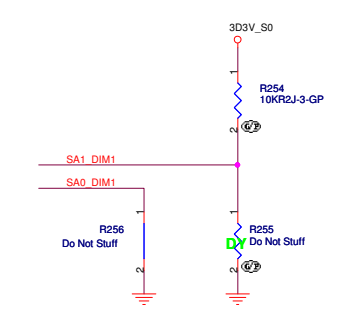
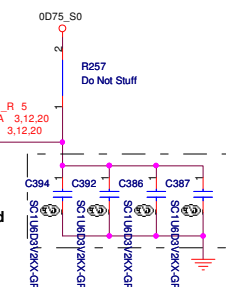
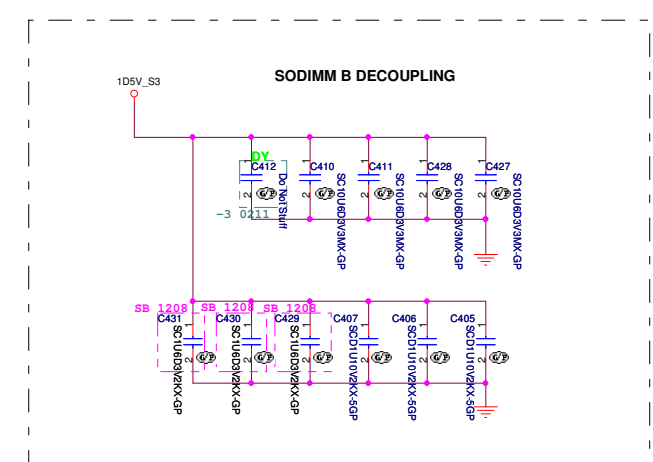


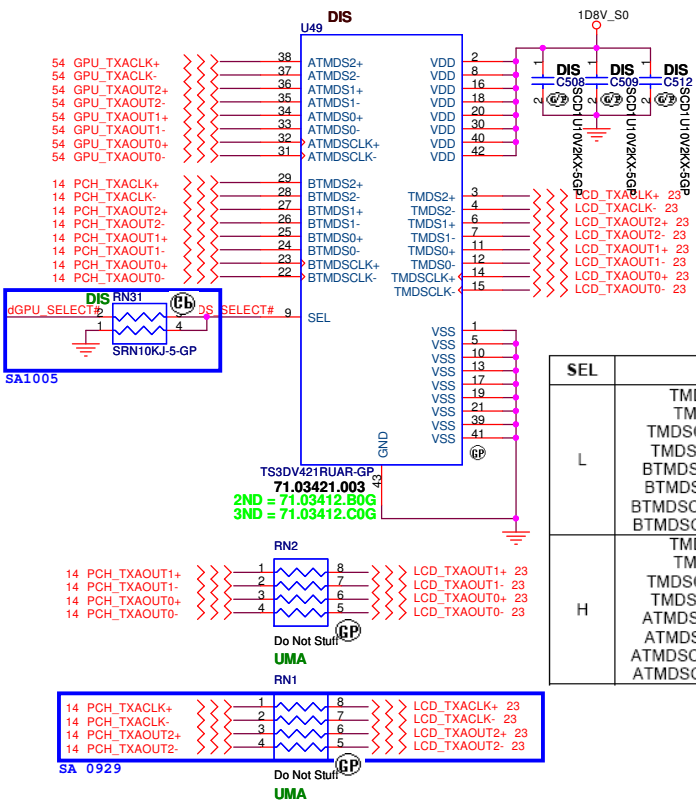


Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from
the Processor than SO-DIMMA

Place these caps
close to VTT1 and
VTT2.

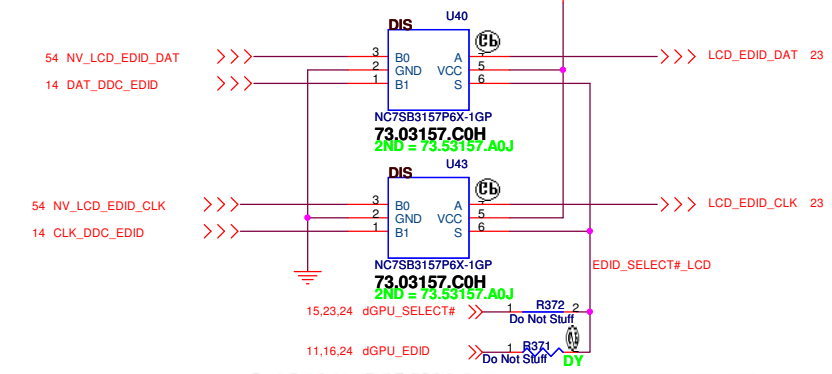




Function Table

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

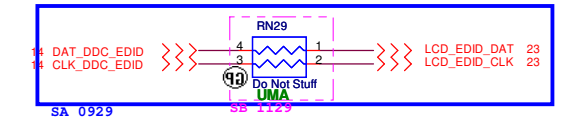
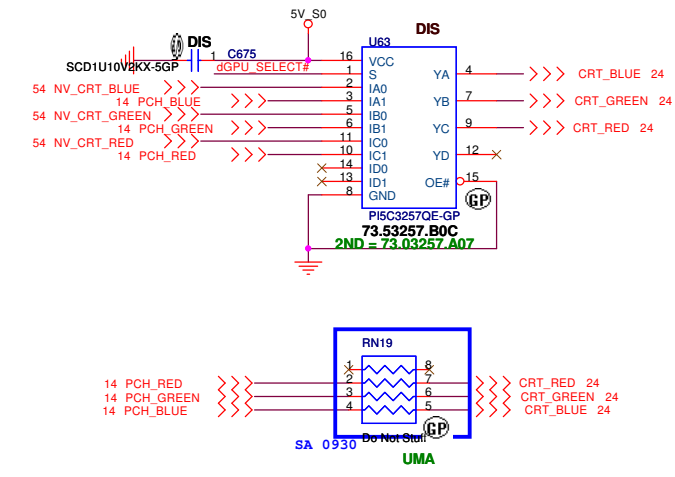
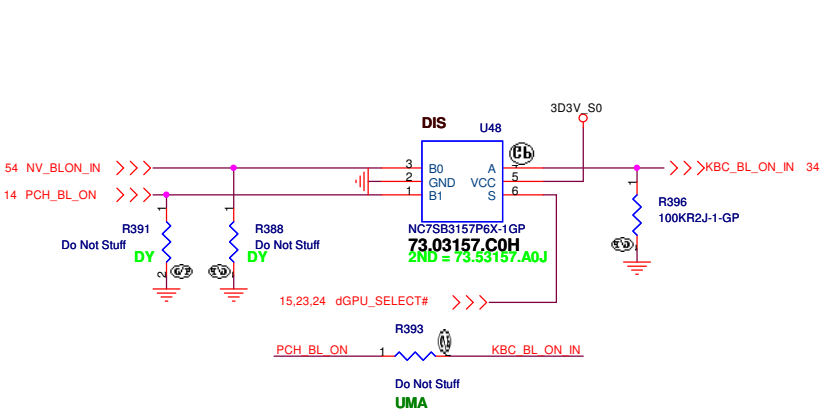
H = HIGH Logic Level L = LOW Logic Level



Function Table

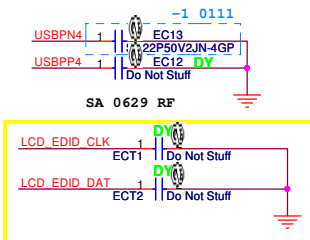
Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

H = HIGH Logic Level L = LOW Logic Level



$\bar{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

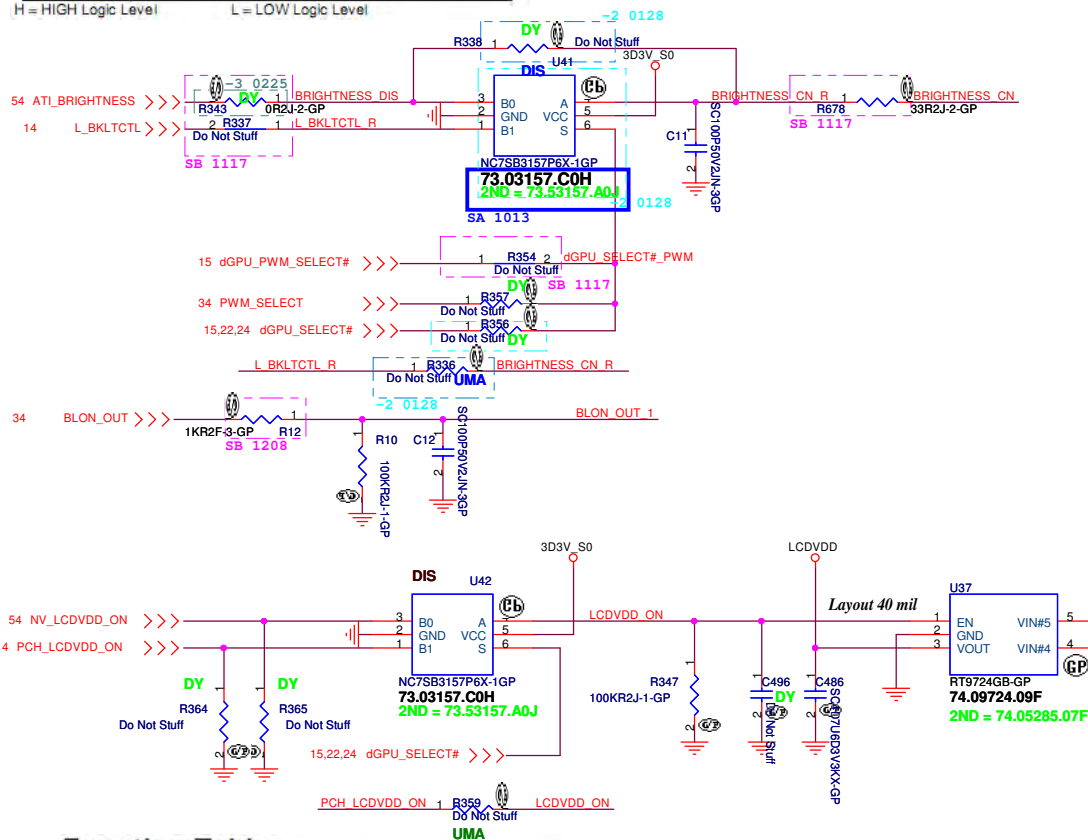
LCD/INVERTER/CCD CONN



Function Table

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

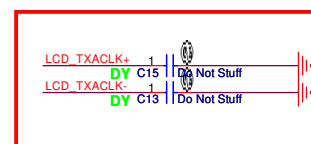
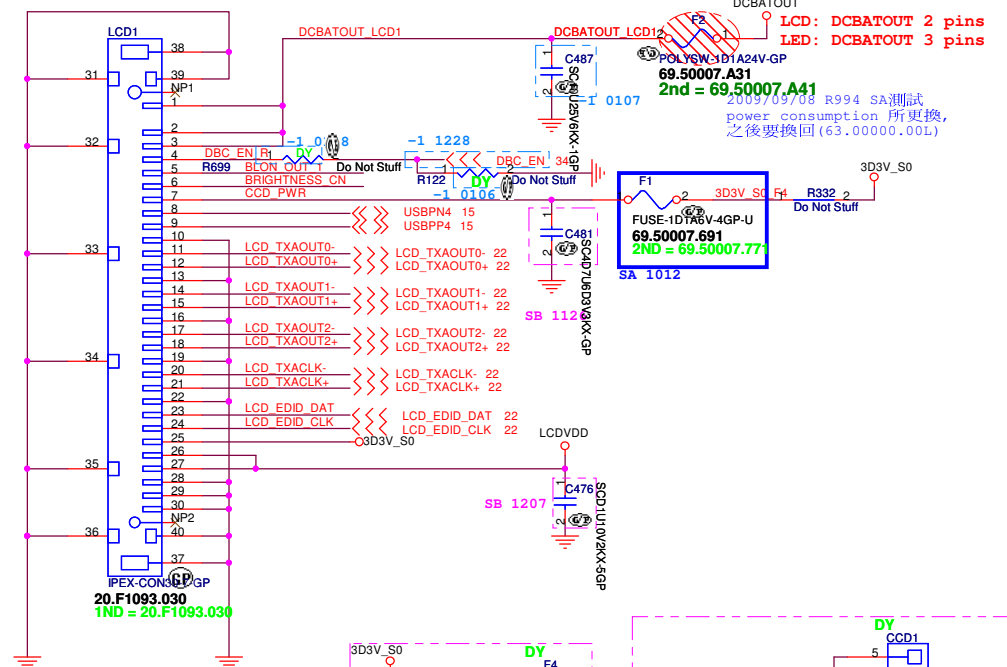
H = HIGH Logic Level L = LOW Logic Level



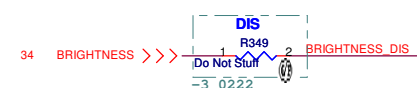
Function Table

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

H = HIGH Logic Level L = LOW Logic Level



modify by RF



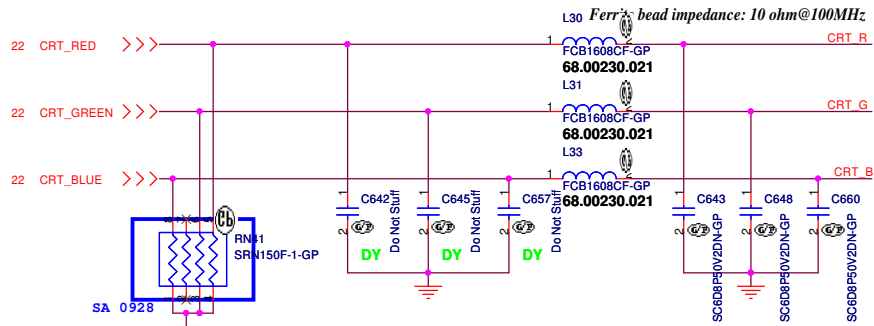
Reserve direct connector to KBC

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LCD CONN		
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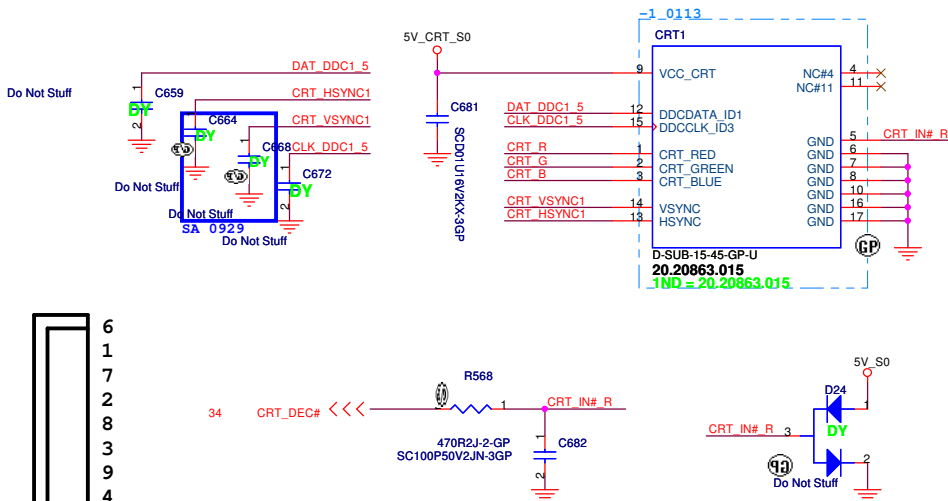
Layout Note:
Place these resistors
close to the CRT-out
connector



Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR



L=>B0 -DIS
H=>B1 -UMA

15,22,23 dGPU_SELECT#

For DIS CRT

54,57 NV_CRT_HSYNC

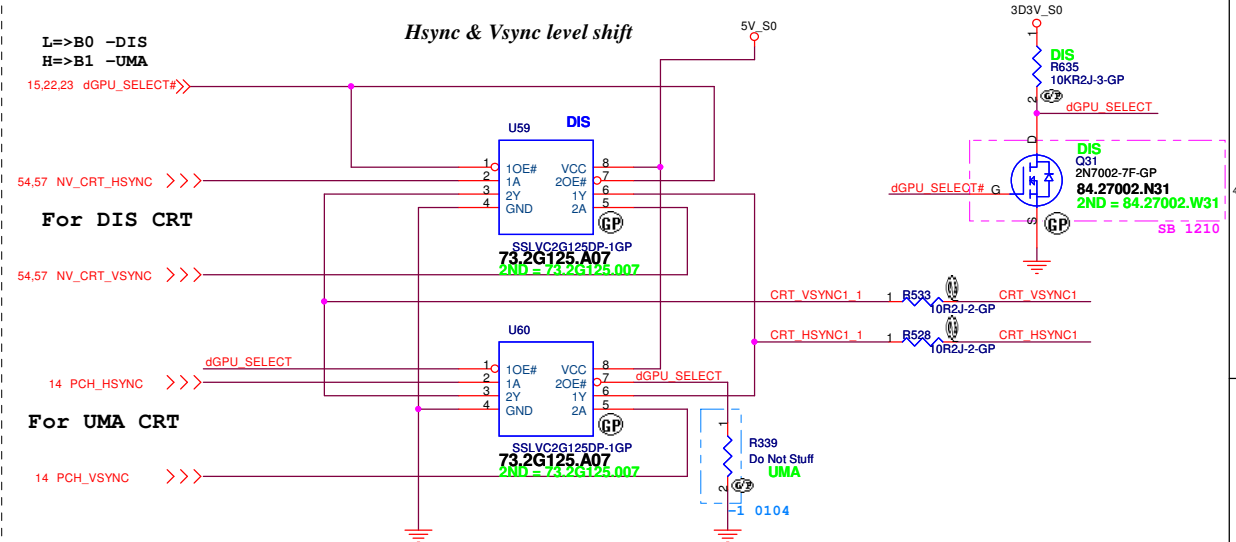
54,57 NV_CRT_VSYNC

For UMA CRT

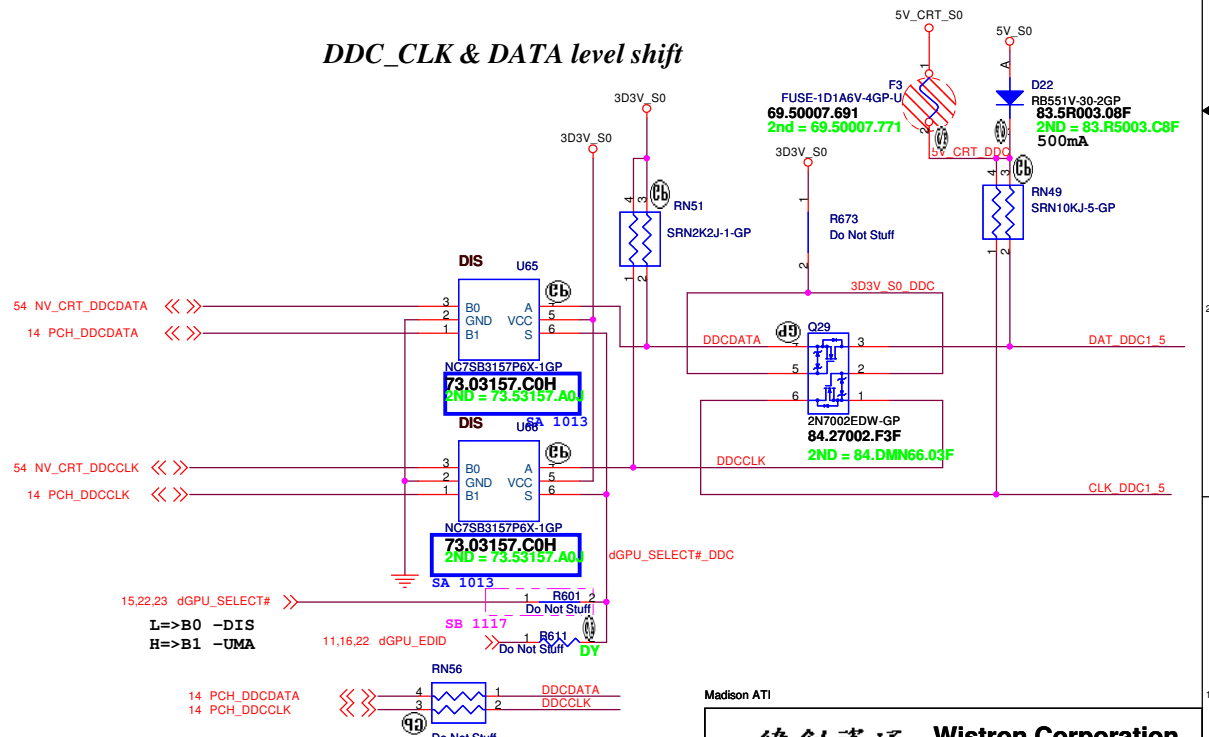
14 PCH_HSYNC

14 PCH_VSYNC

Hsync & Vsync level shift



DDC_CLK & DATA level shift



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Title

CRT CONN

Size

Document Number

JM31-CP

Rev

SB

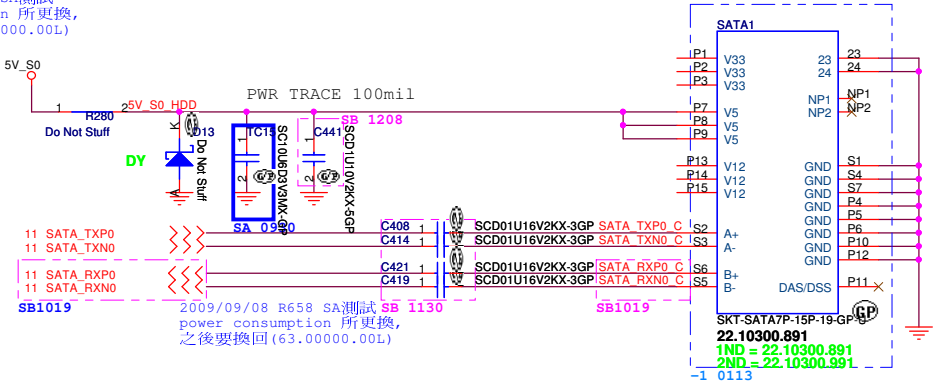
Date: Thursday, February 25, 2010

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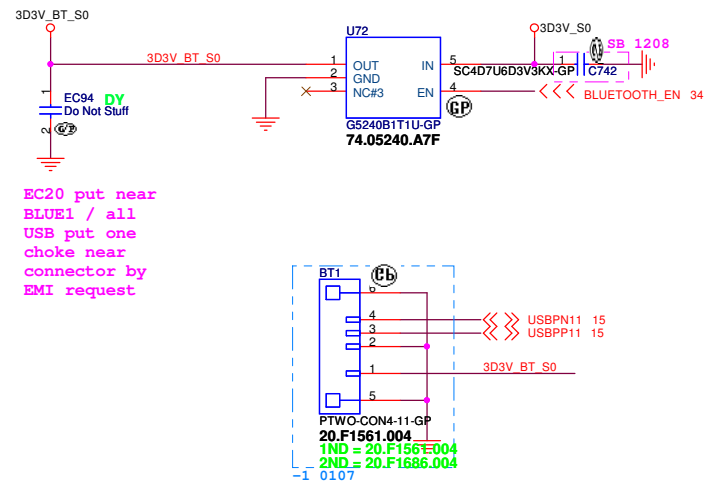
SATA Connector

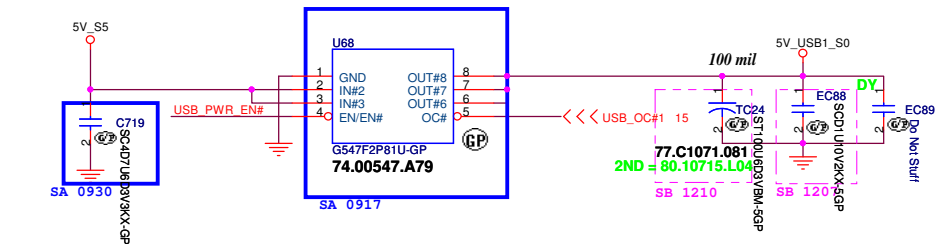
2009/09/08 R658 SA測試
power consumption 所更換,
之後要換回 (63.00000.00L)



2009/09/08 R658 SA測試
power consumption 所更換,
之後要換回 (63.00000.00L)

BLUETOOTH MODULE





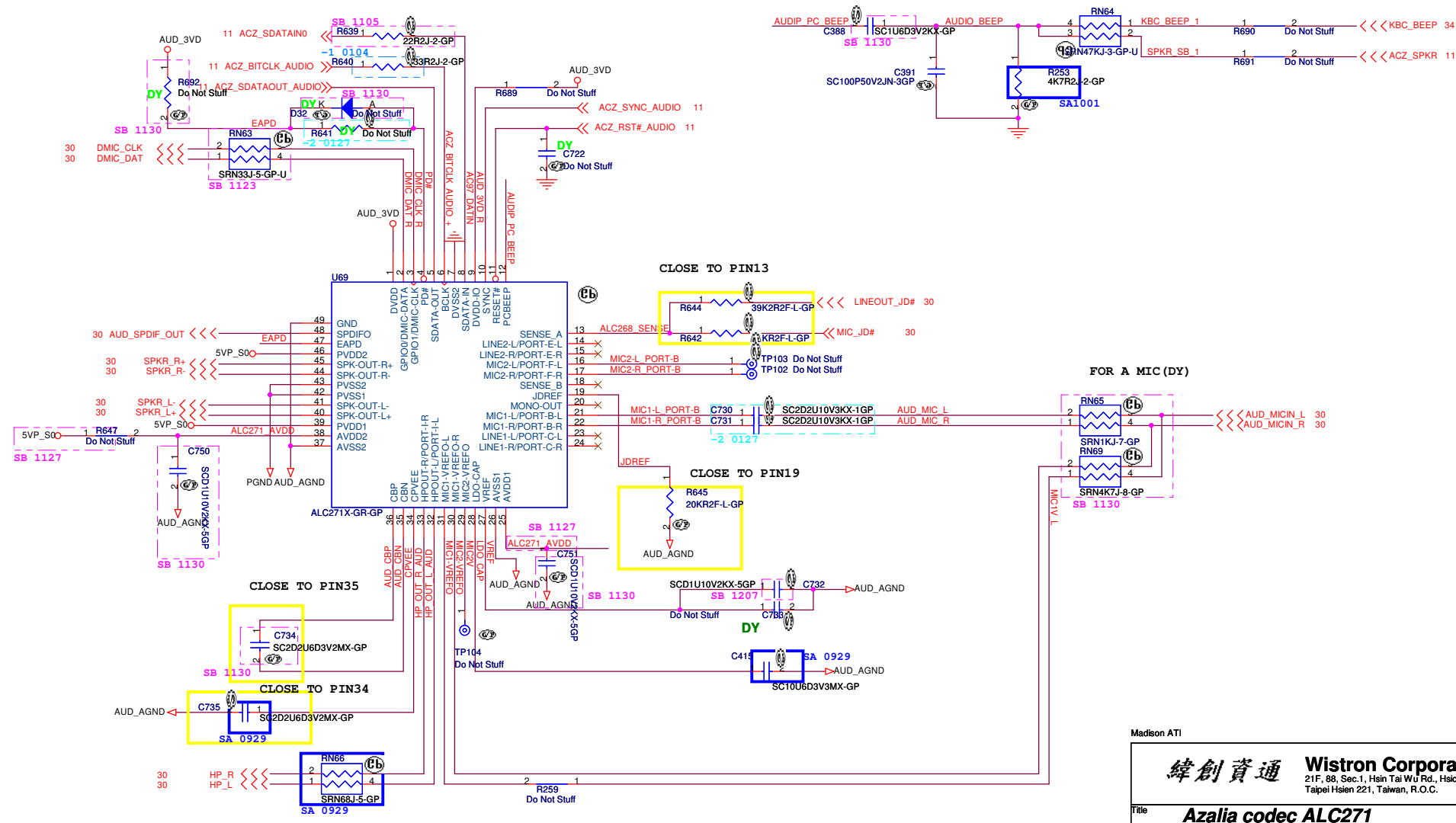
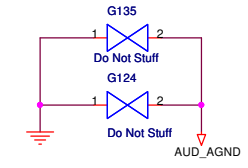
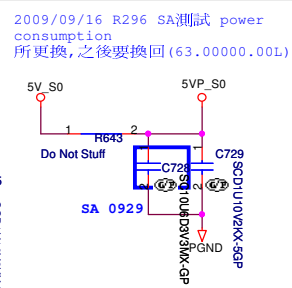
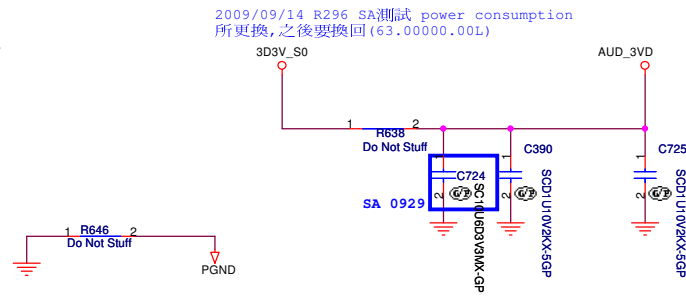
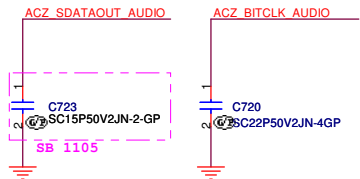
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Taipei Hsien 221, Taiwan, R.O.C.

USB CONN

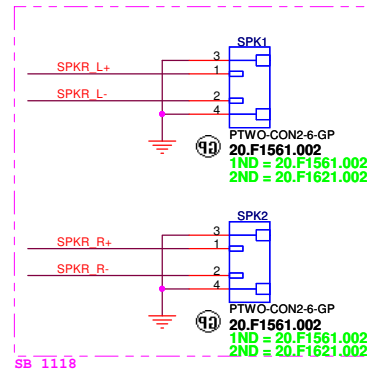
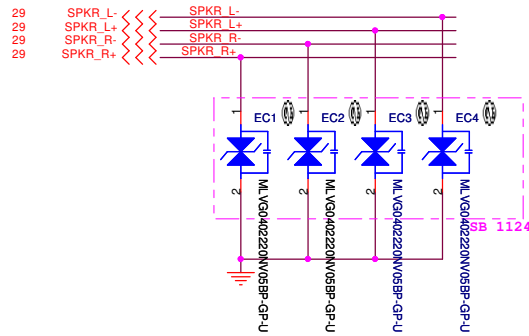
JM31-CP

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-3

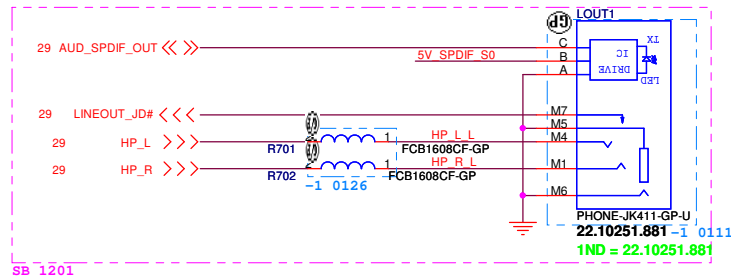
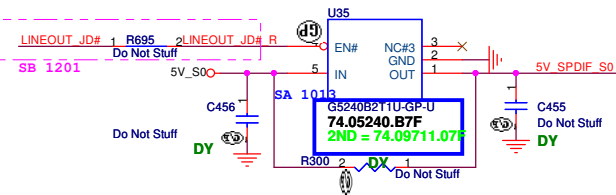
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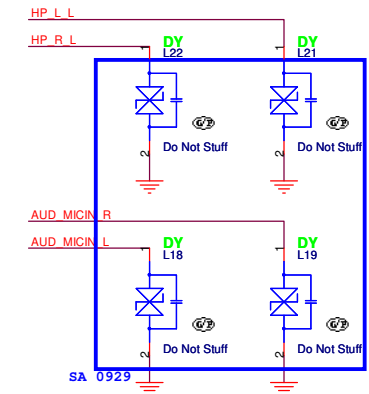
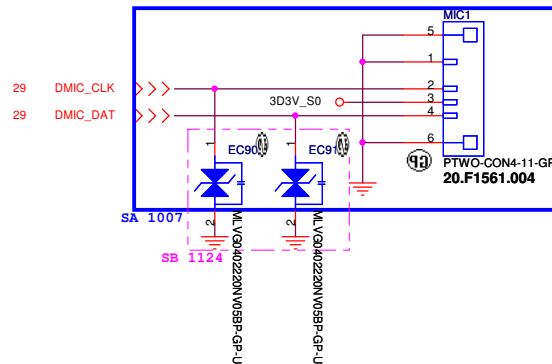
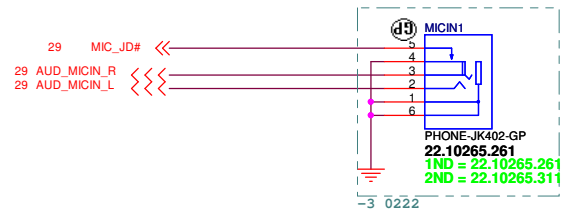
Internal Speaker



LINE OUT



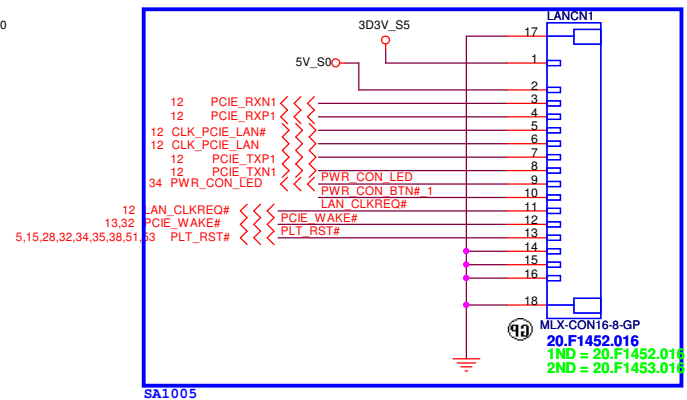
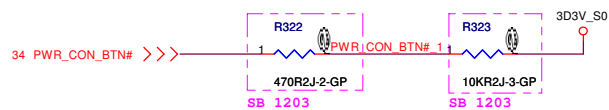
MIC IN



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Title		
AUDIO jack		
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Title

LAN CONN

Size
A3

Document Number

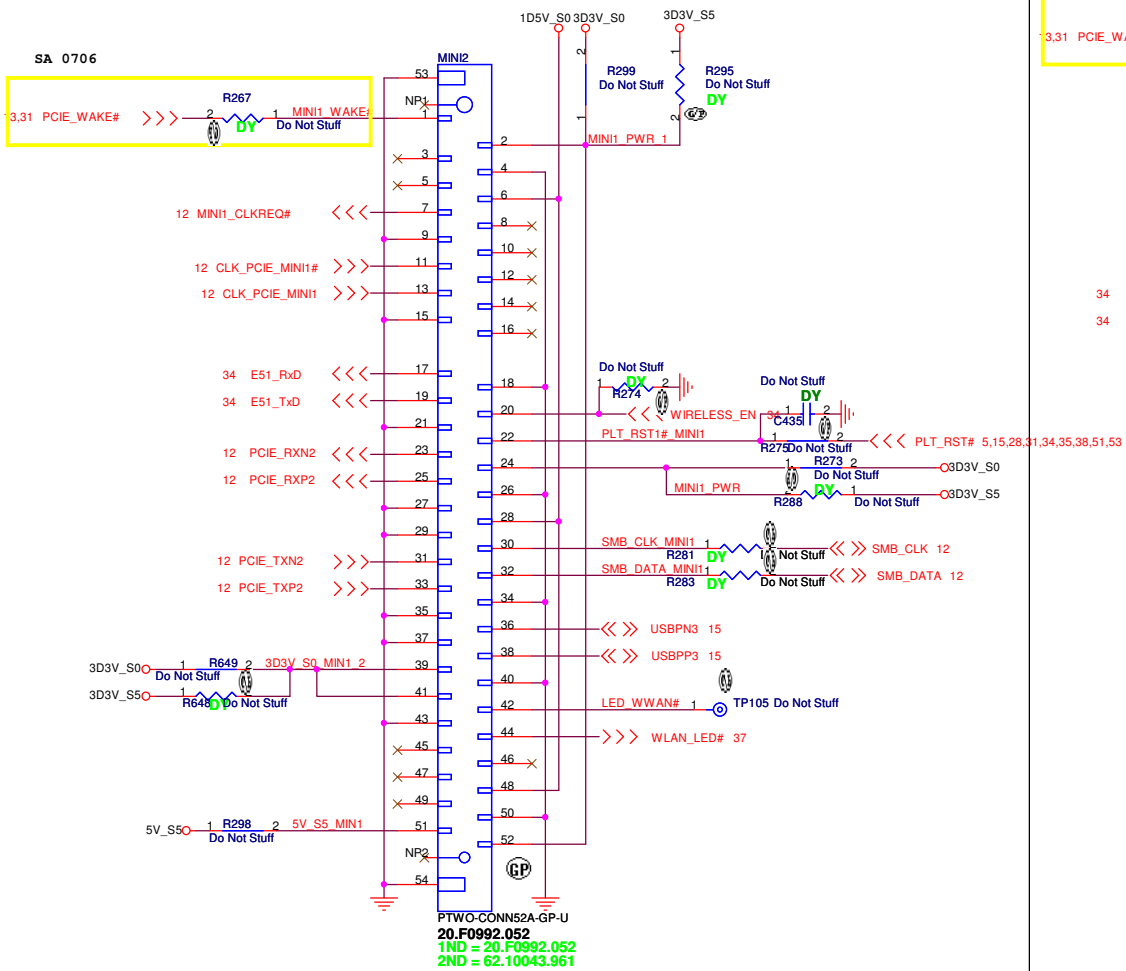
JM31-CP

Rev
SB

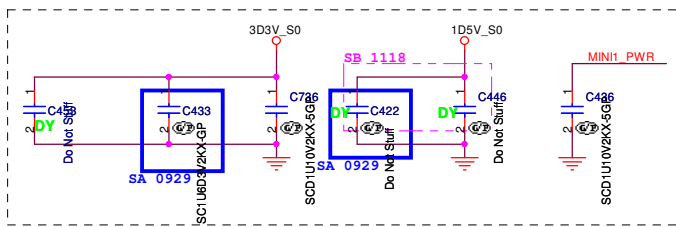
Date: Thursday, February 25, 2010

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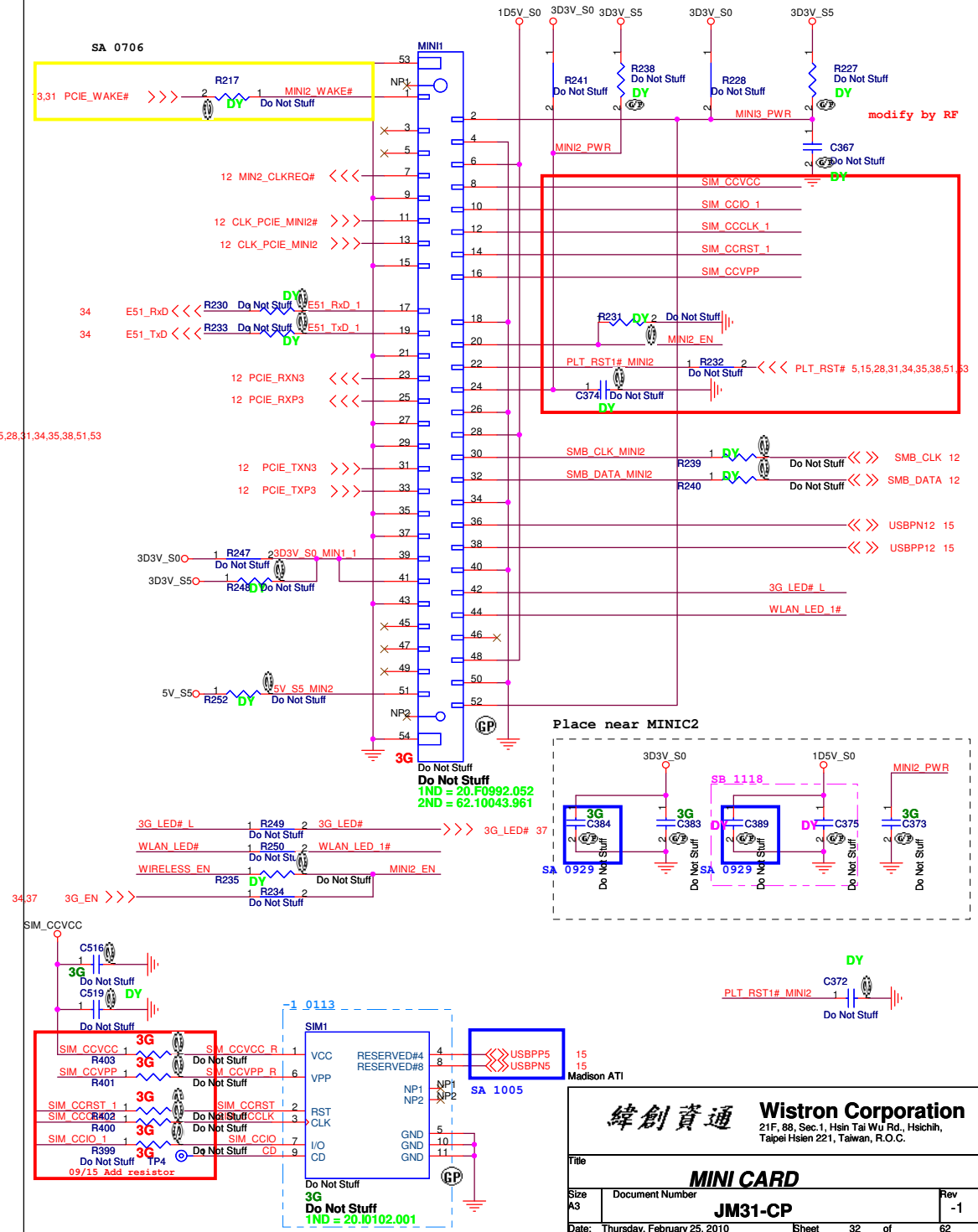
Mini Card Connector(WLAN) Support debug-card



Place near MINI1

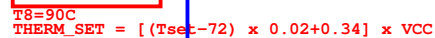
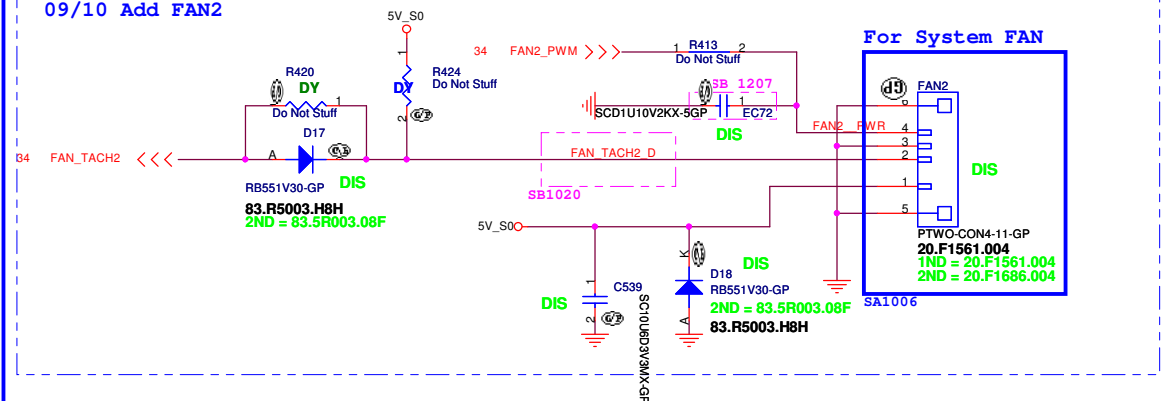
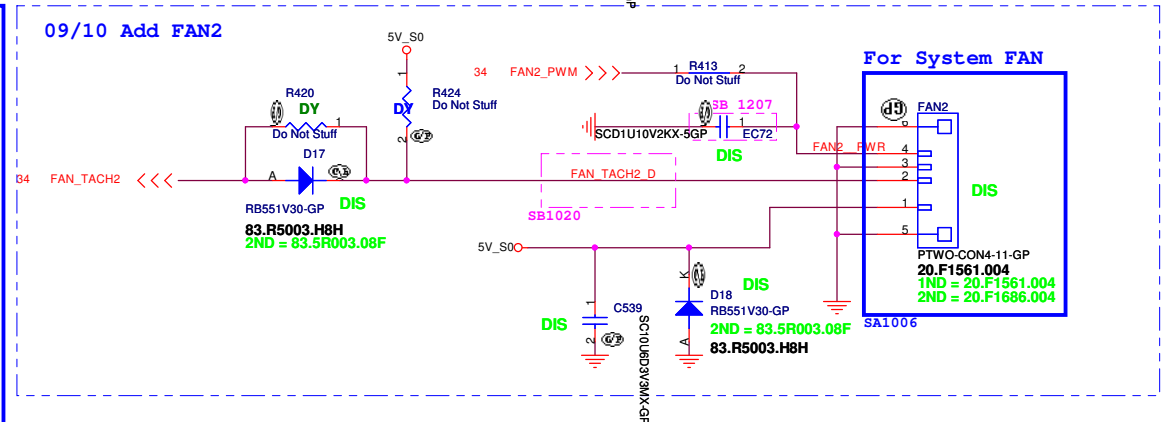
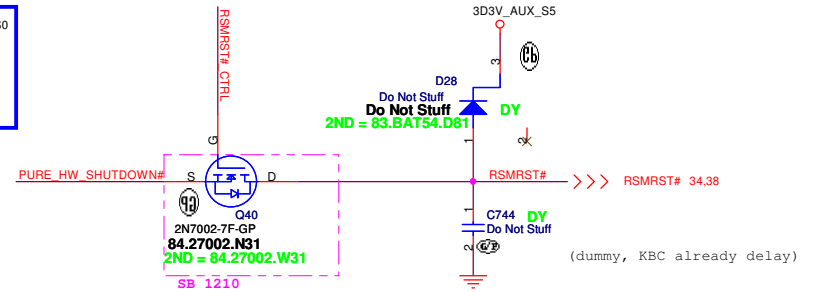
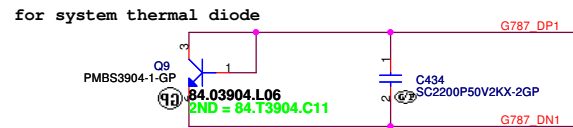


Mini Card Connector(Robson2 and 3G)



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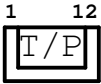
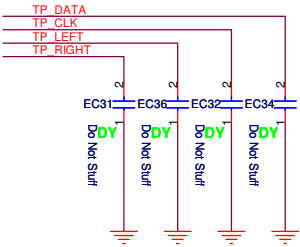
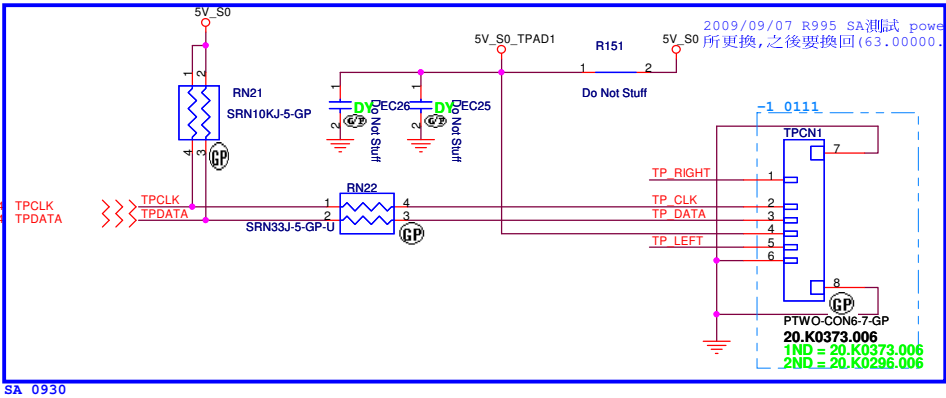
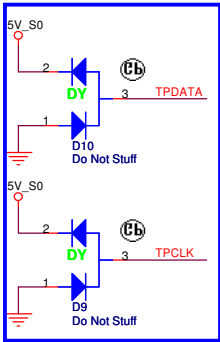
Title			
MINI CARD			
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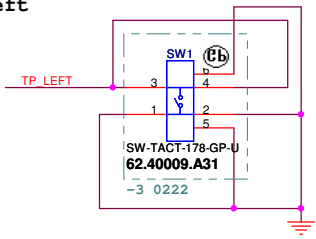
Timing diagram for SA 1002 showing signals and their timing relative to a 15 PCLK_FV clock signal. The signals include LPC_LAD0, LPC_LAD1, LPC_LAD2, LPC_LAD3, LPC_LFRAME#, PLT_RST#, PCLK_FV, and PCLK_FWH. The diagram also shows a 3D3V supply and a 15 PCLK_FV clock signal. The signals are connected to the SA 1002 component.



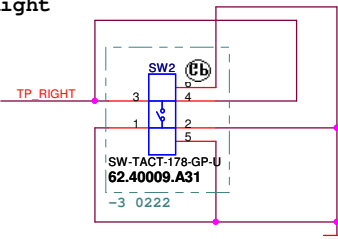
TOUCH PAD



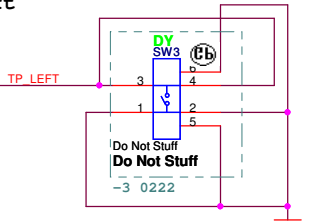
Left



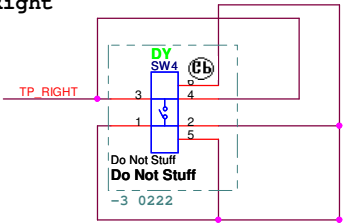
Right



Left



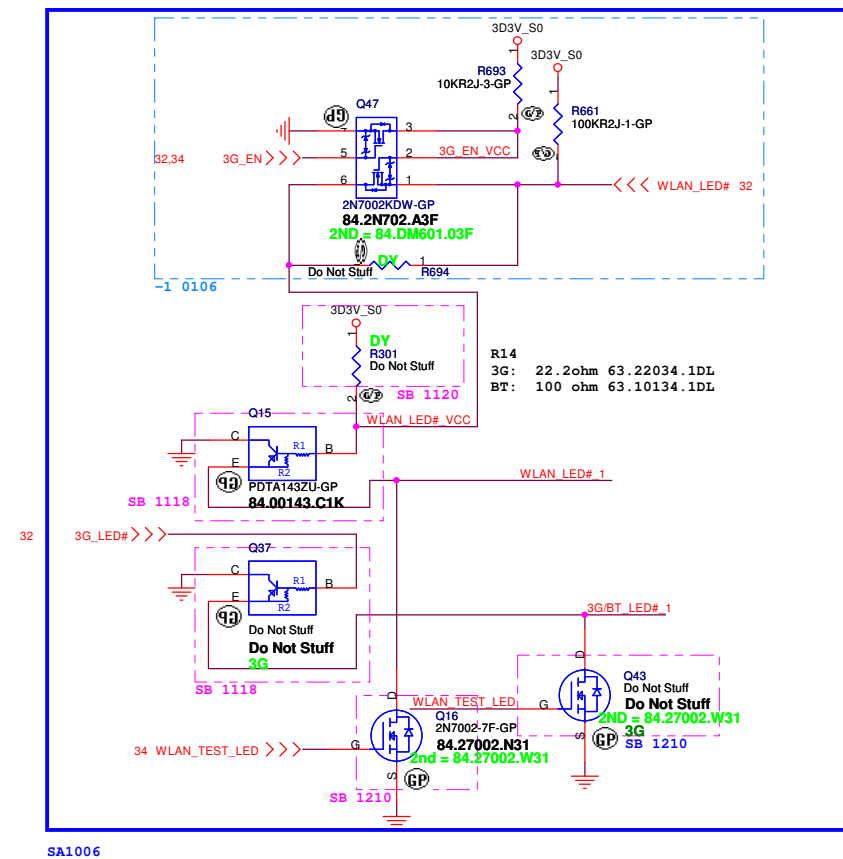
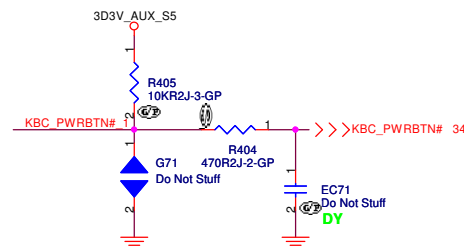
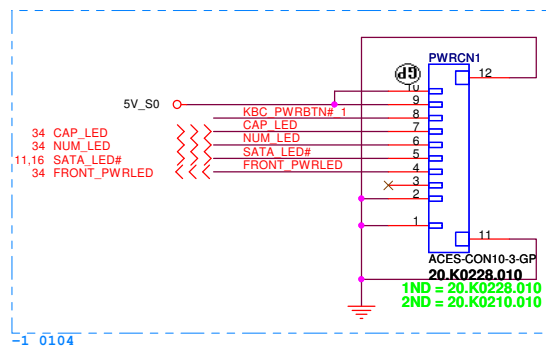
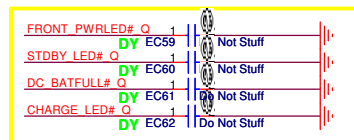
Right



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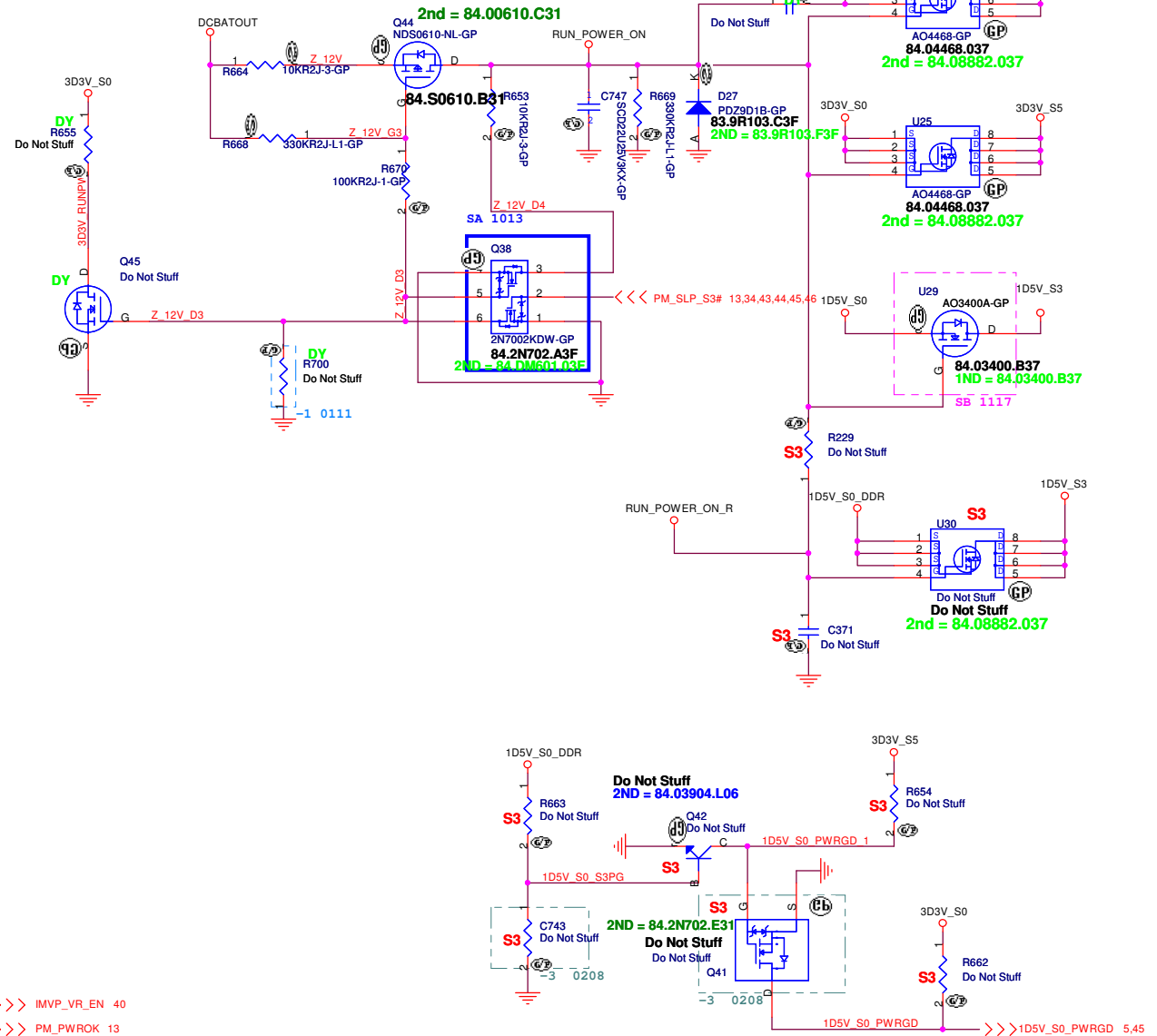
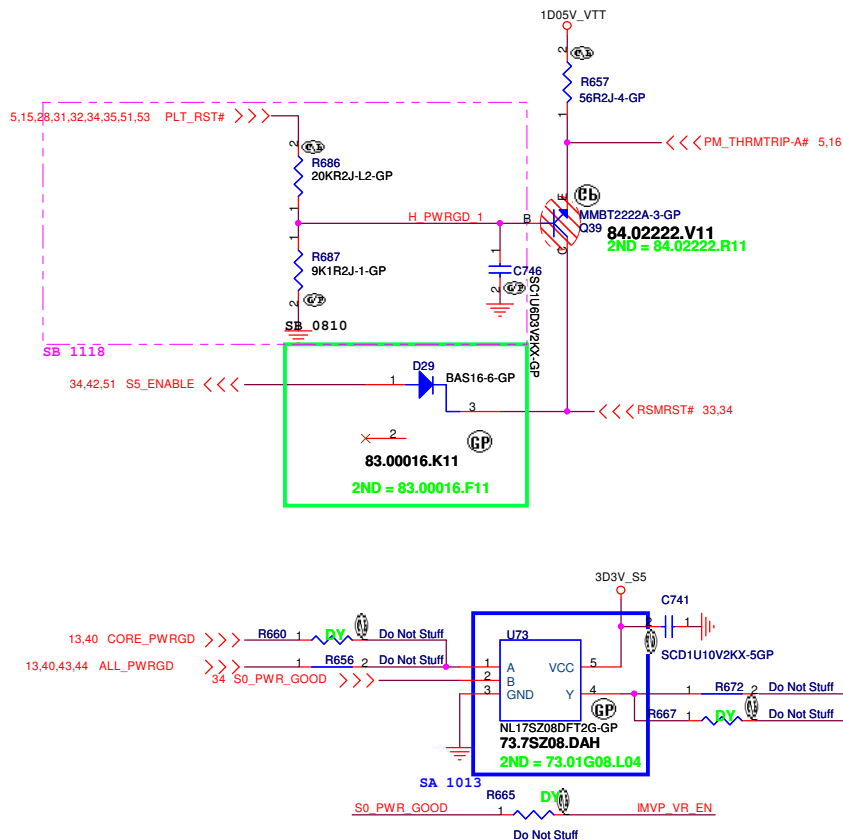
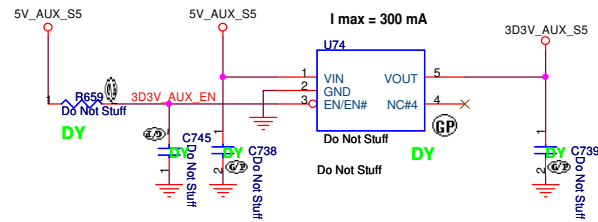
Title			Touch PAD	
Size	Document Number			Rev
A3		JM31-CP		-1
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Run Power

Aux Power

3D3V_AUX_S5



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RUN POWER and 3D3V AUX S5

Size

Document Number

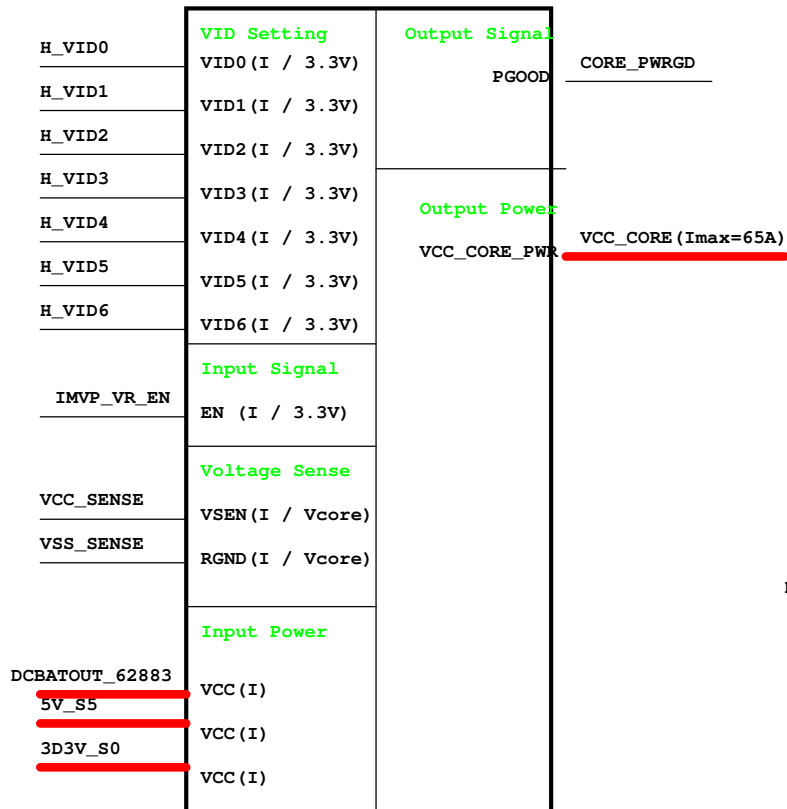
JM31-CP

-3

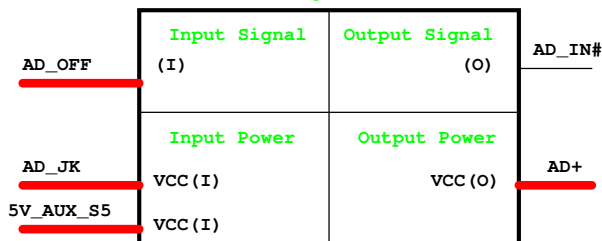
Date: Thursday, February 25, 2010

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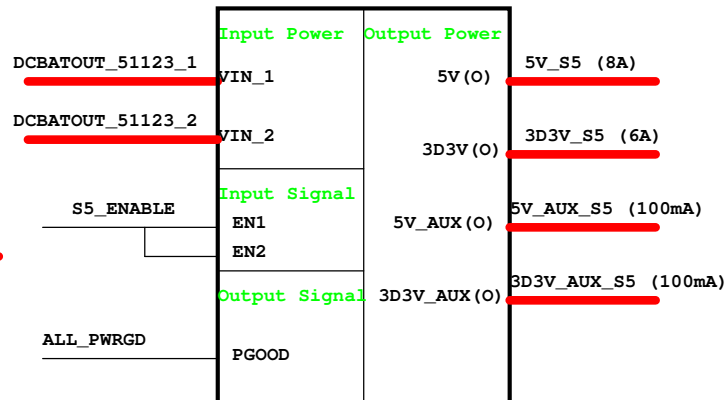
ISL62883 VCC_CORE



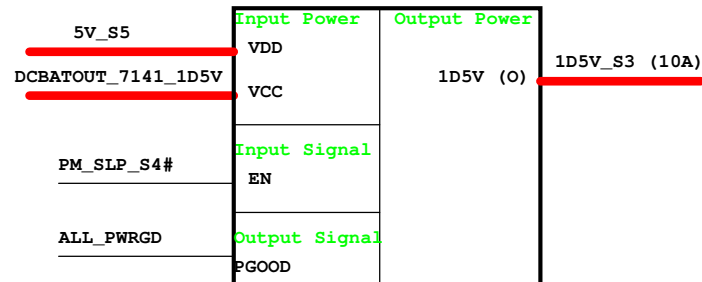
Adapter



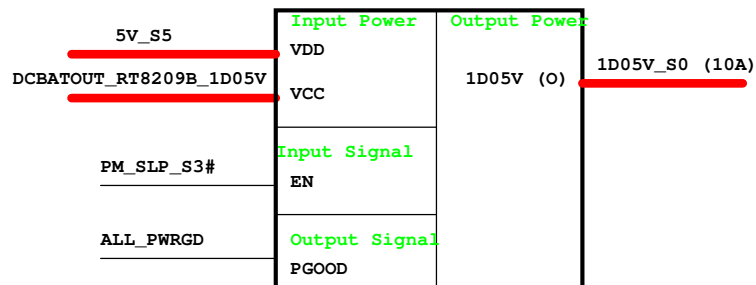
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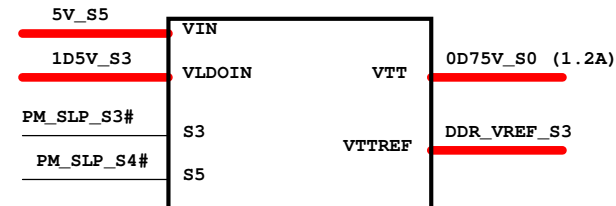
RT9025 1D5V



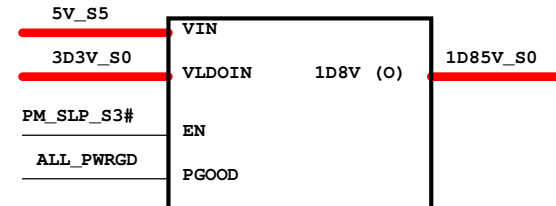
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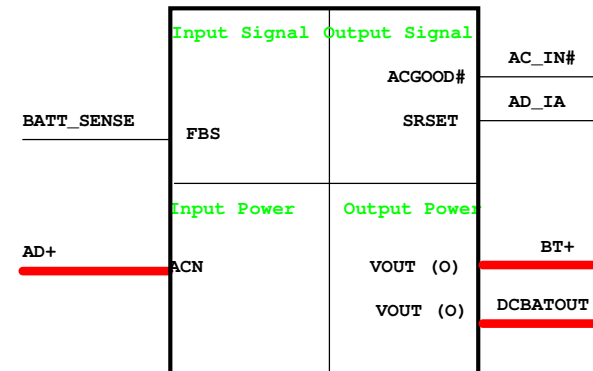
RT9026 0D75V_S0



RT9025 1D8V



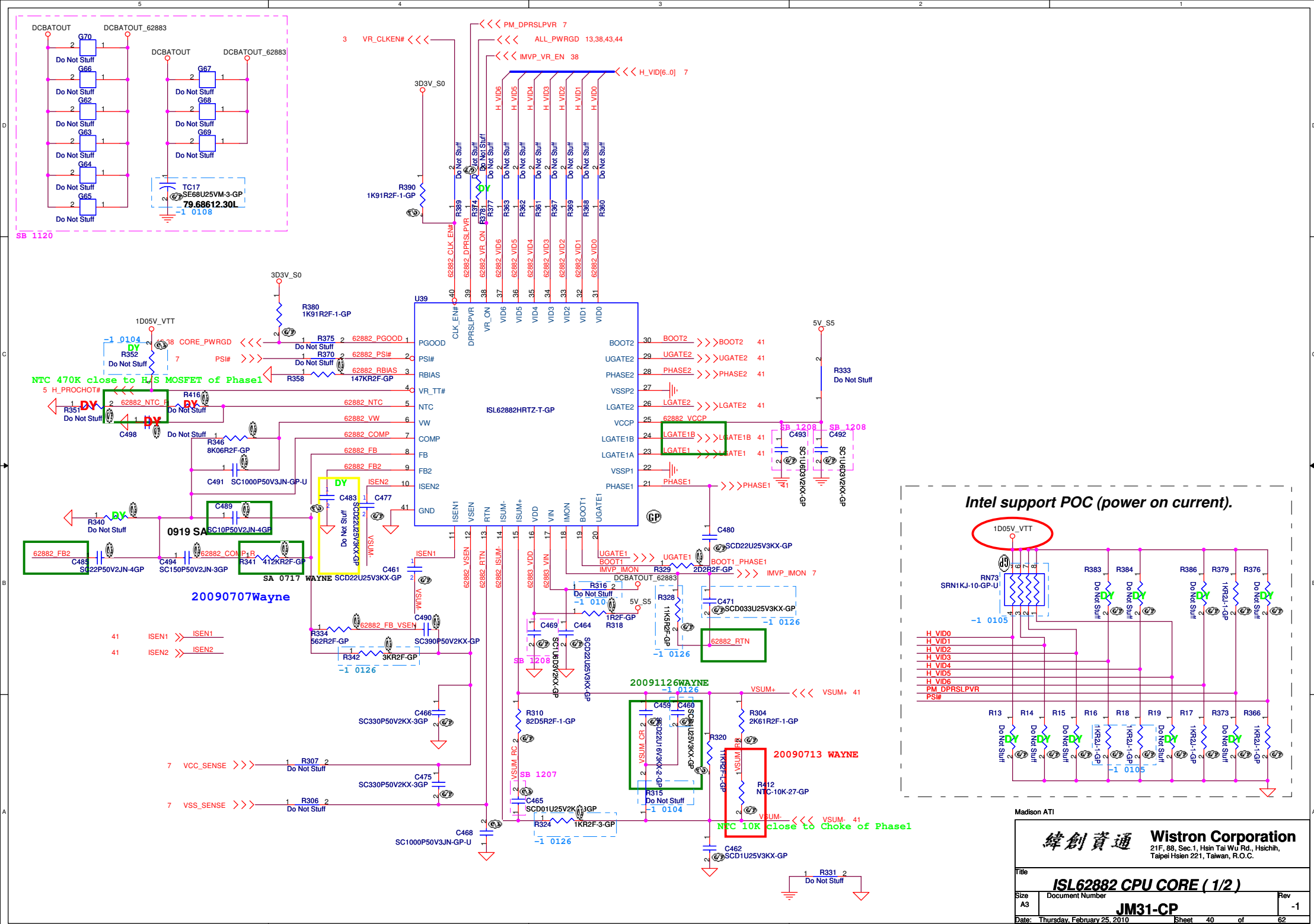
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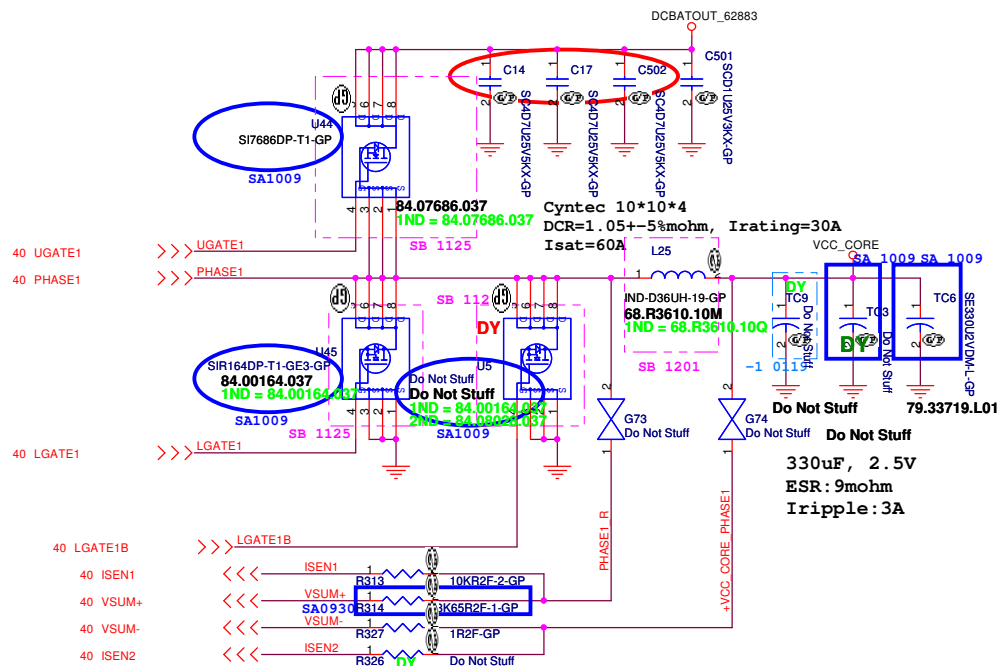
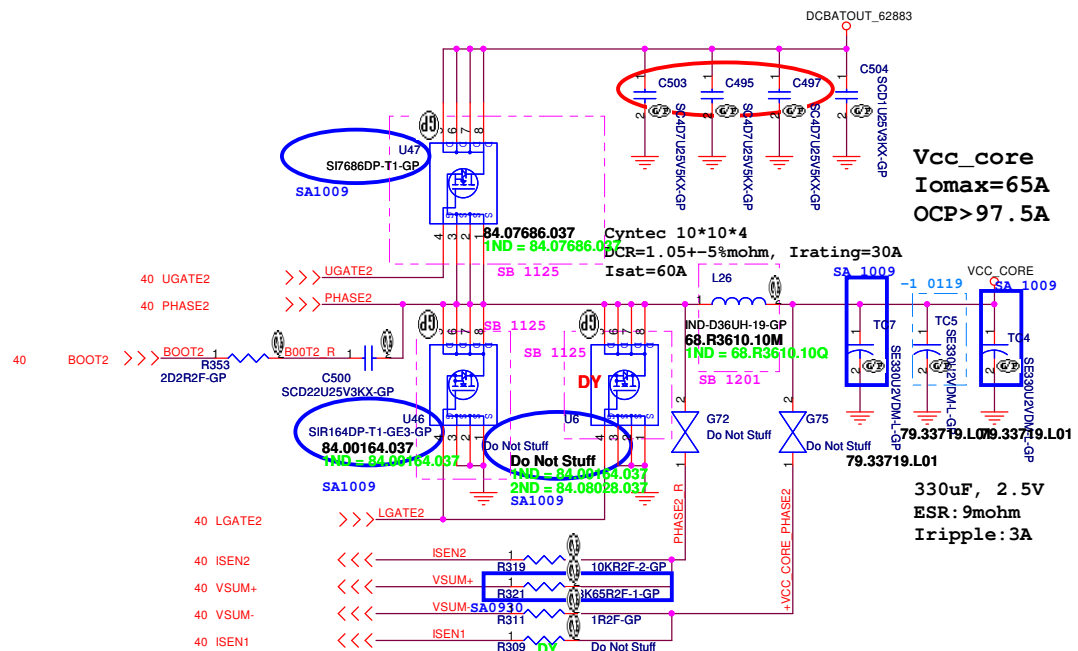


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Taipei Hsien 221, Taiwan, R.O.C.

Title **Power Block Diagram**
Size Document Number **JM31-CP** Rev **SA**
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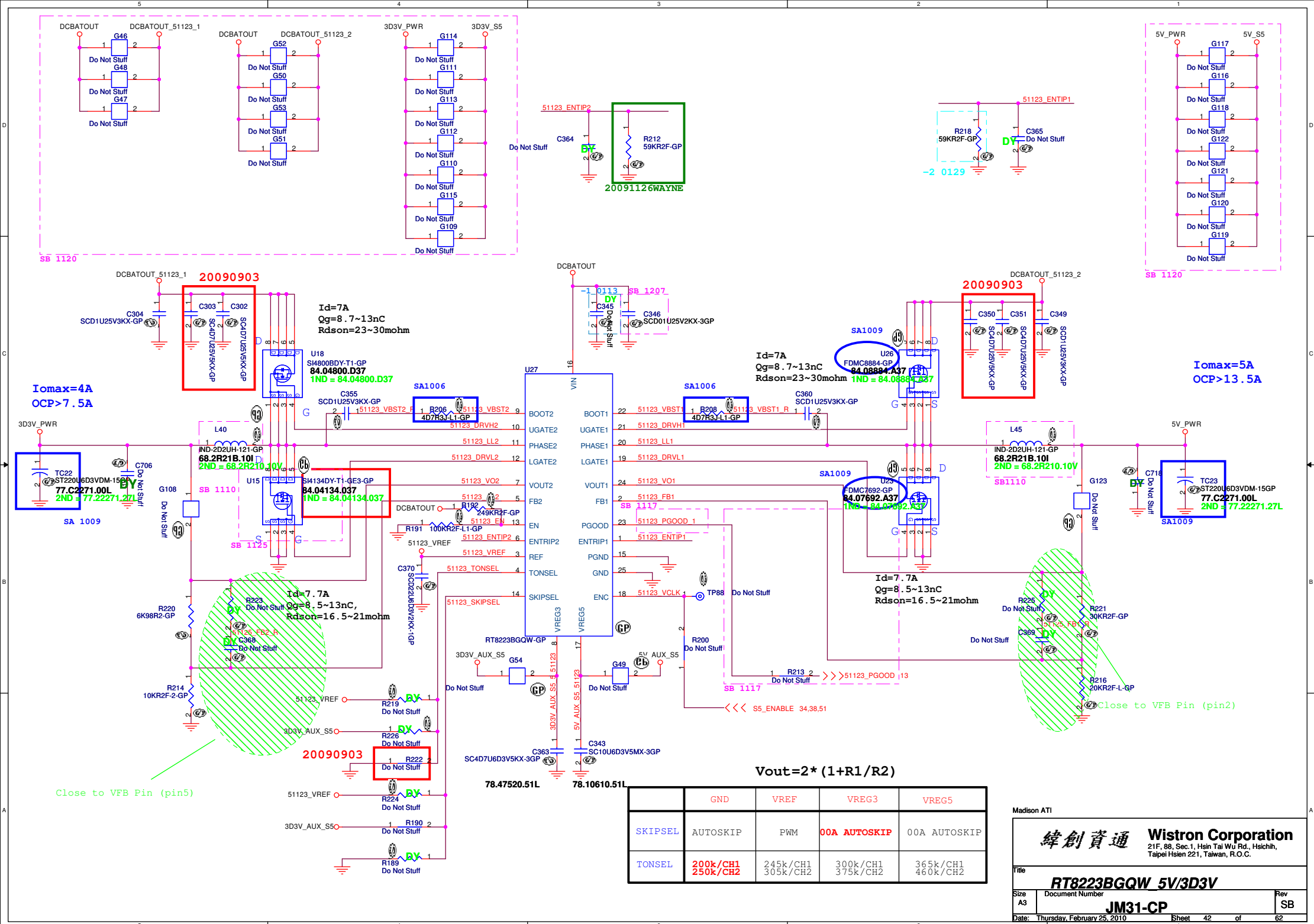




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Title		ISL62882 CPU CORE (2 / 2)	
Size	A3	Document Number	Rev
Date: Thursday, February 25, 2010		JM31-CP	
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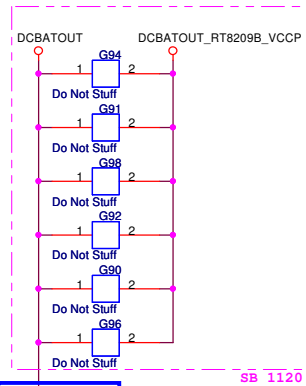


$$V_{out} = 0.75V * (R1 + R2) / R2$$
[illegible]
$$V_{out} = 0.75V * (R1 + R2) / R2$$

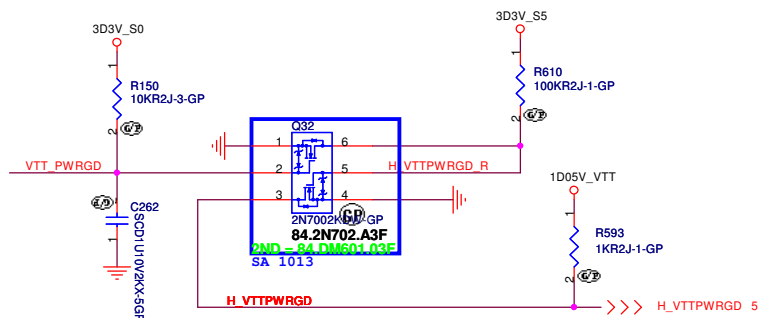
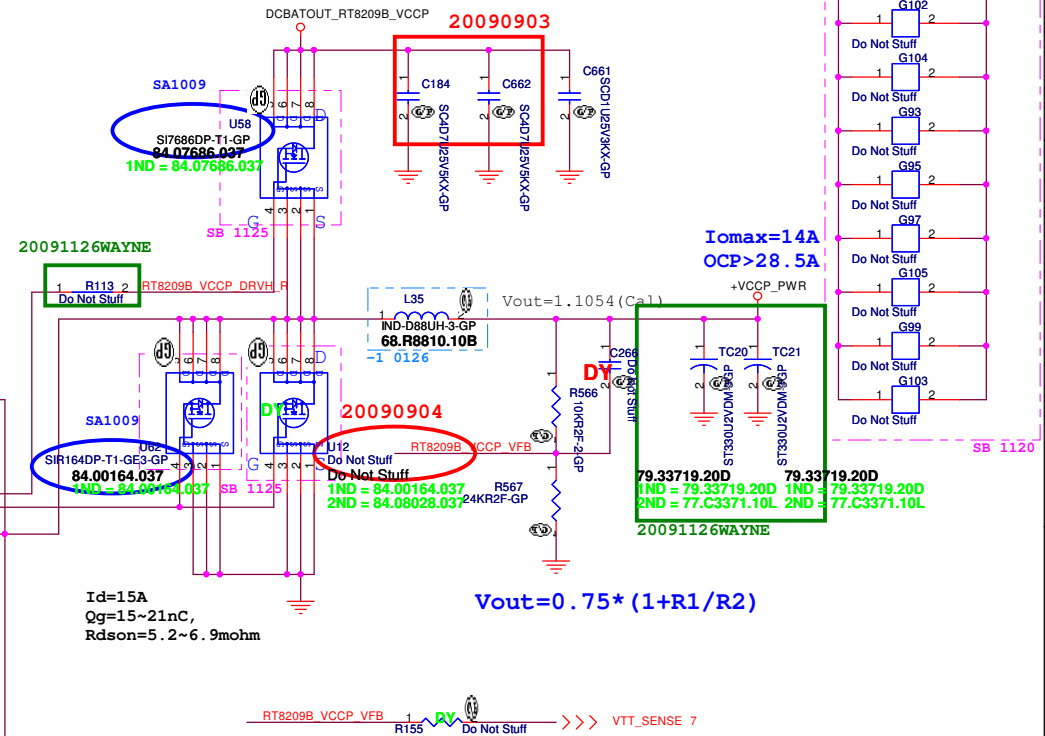
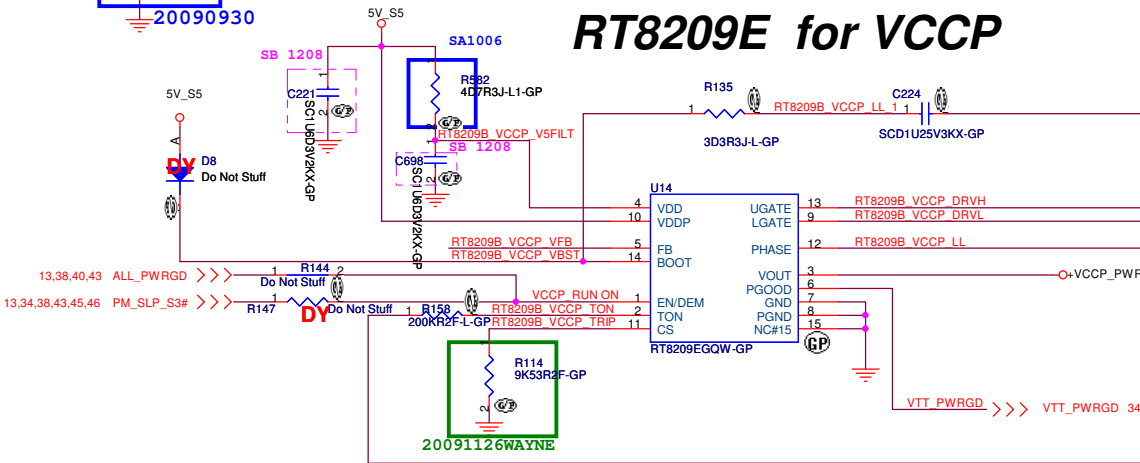
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SR

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RT8209E for VCCP



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Title

Size

A3

Date:

Thursday, February 25, 2010

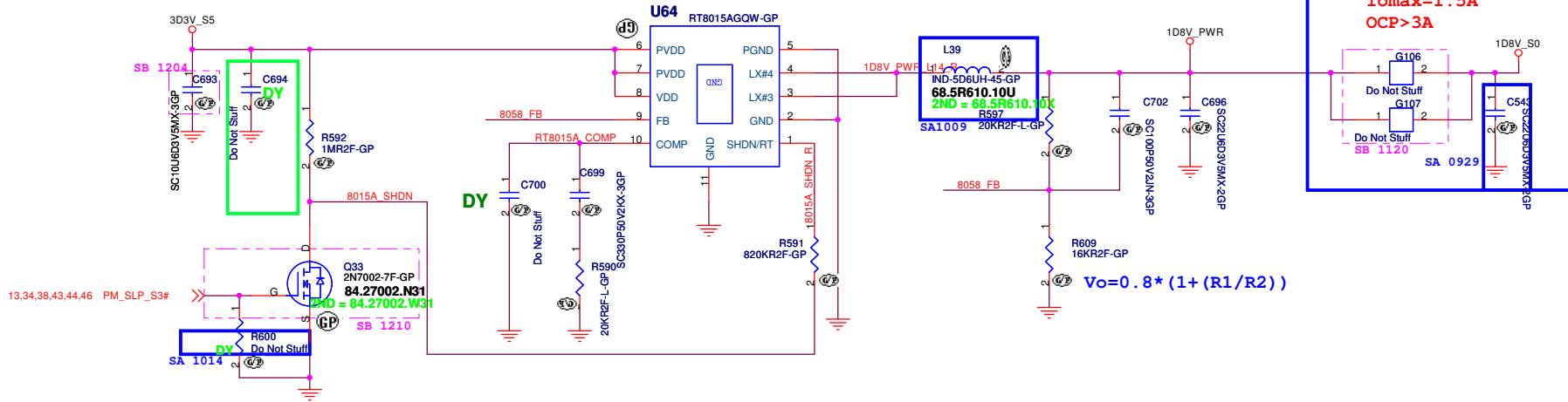
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Rev

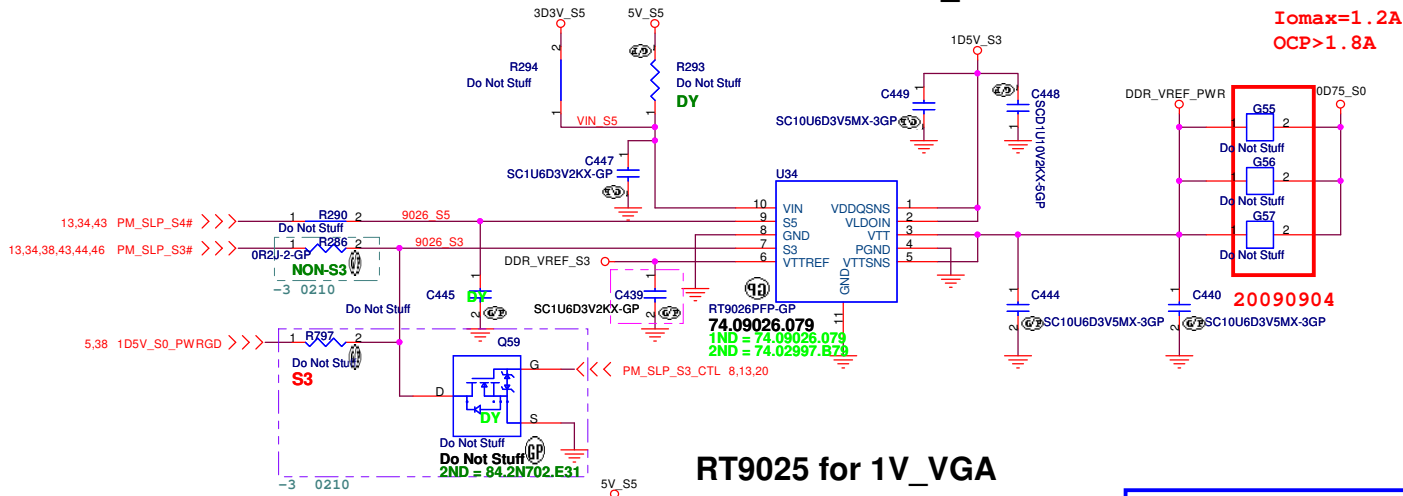
SB

RT8209E +VCCP
JM31-CP

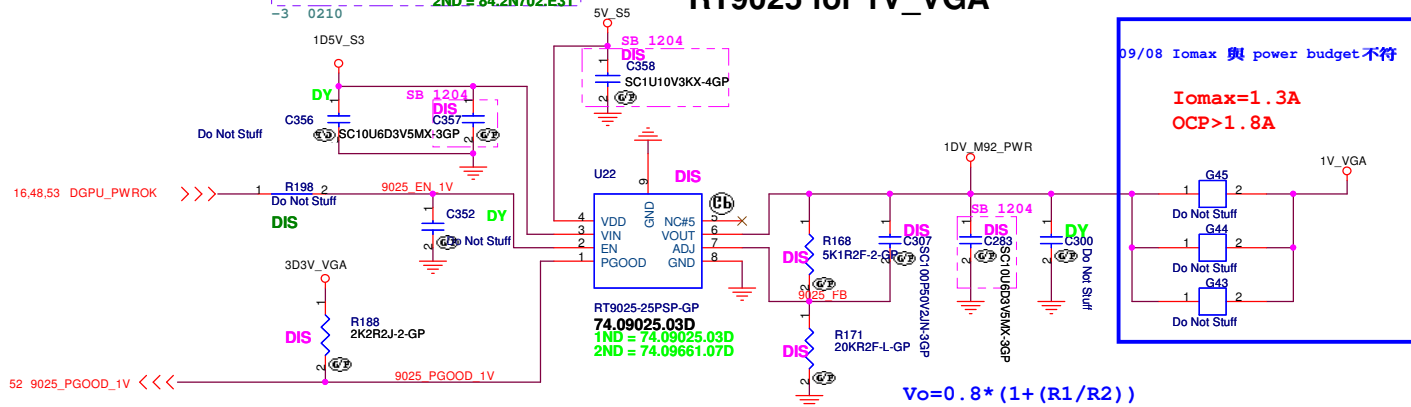
RT8015A for 1D8V_S0



09/08 add 3D3V_S5,R837,R836 RT9026 for 0D75V_S3



RT9025 for 1V_VGA



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Title

RT9025 1D8V 1V/RT9026 0D75

Size

A3	
Date: Thursday, February 25, 2010	

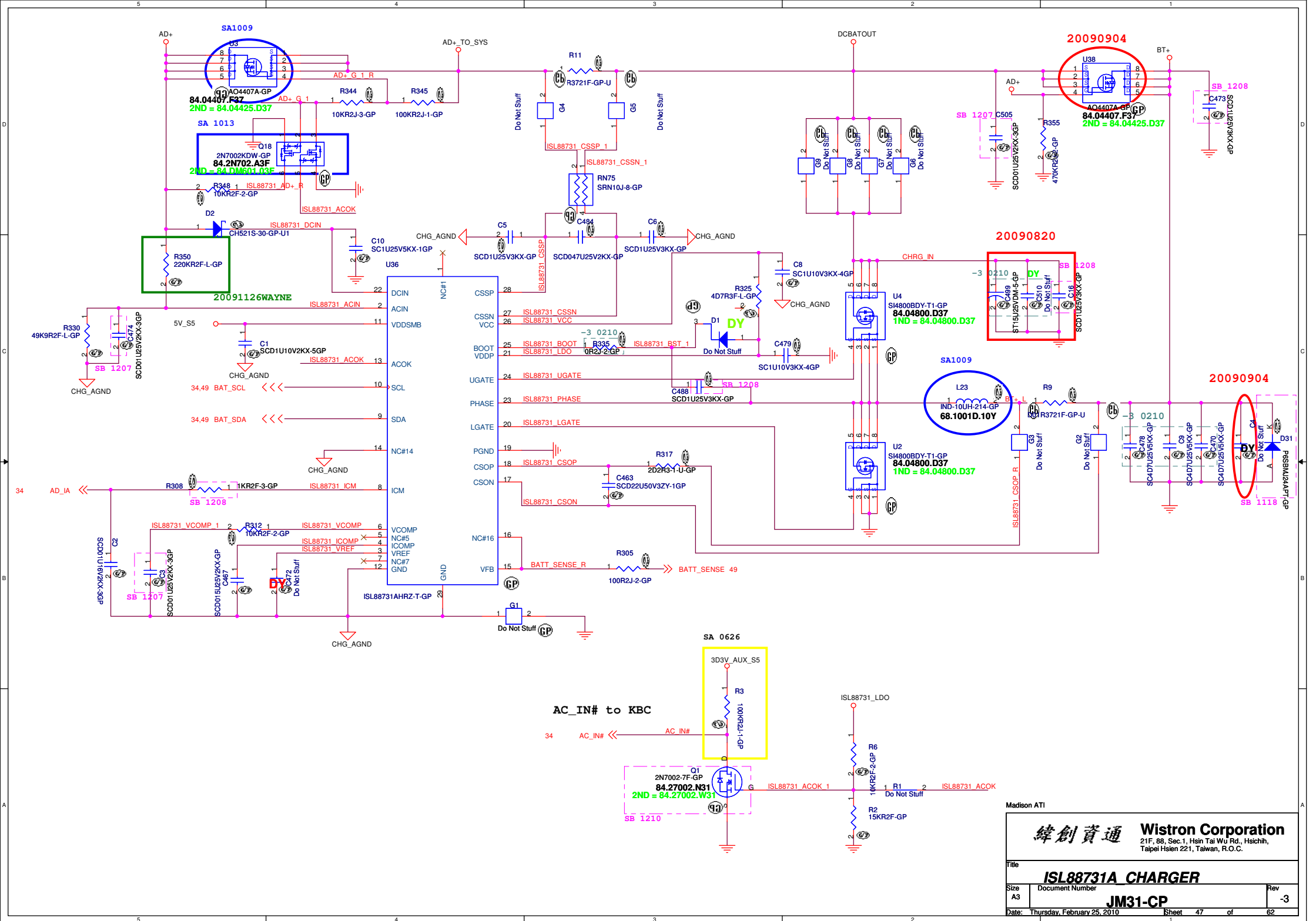
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ISL88731A CHARGER		
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20091126WAYNE

for 40nm GPU
1.5Kohm for N10P/M

20090922

>> DGPU_PWROK16,45,53

SA 0312'09
RT8209A to RT8209B
by power wayne

GPIO15/VID0	VGA_CORE
0	0.90V
1	1.12V

GPIO15/VID0	VGA_CORE
0	0.90V
1	1.02V

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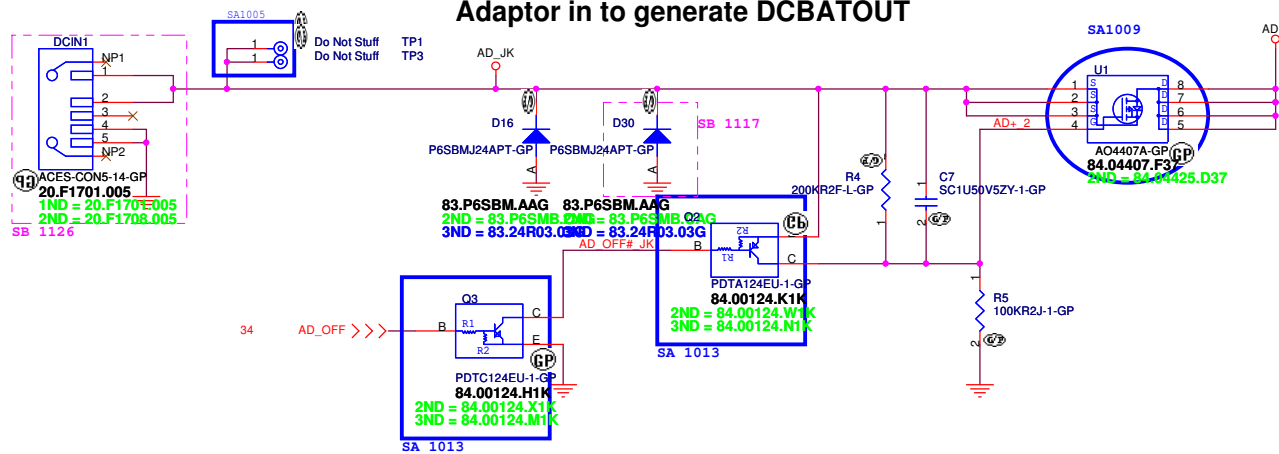
RT8209E VGA CORE

JM31-CP

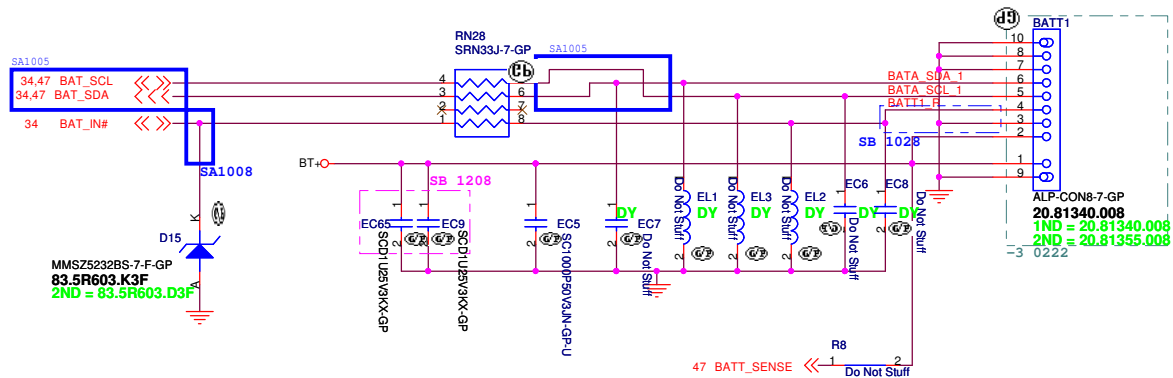
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SB

Adaptor in to generate DCBATOUT



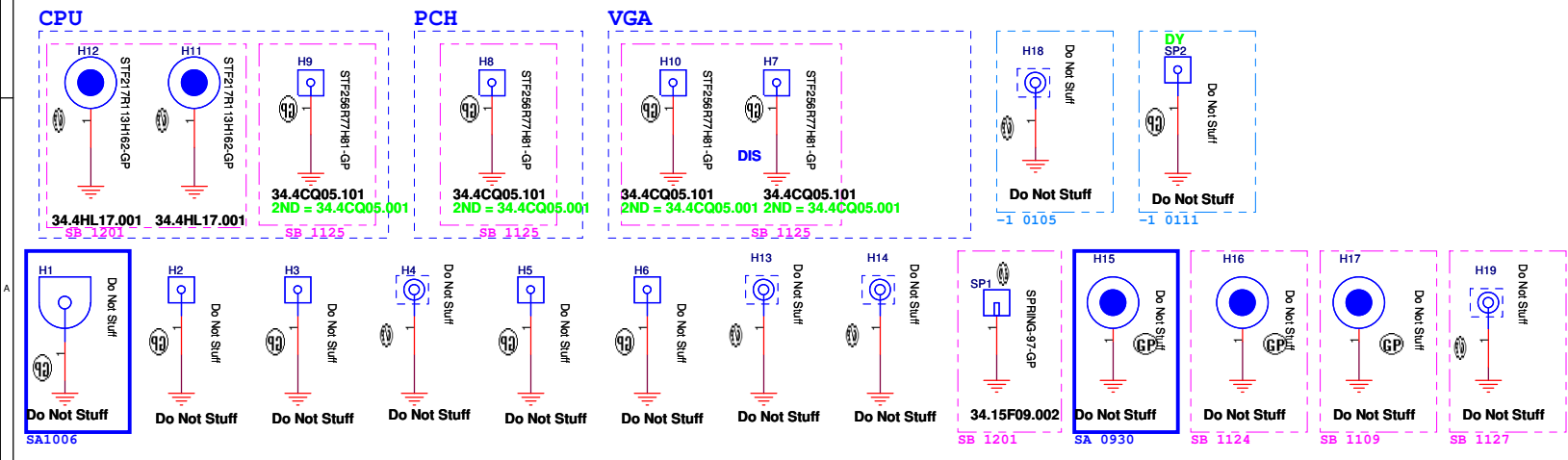
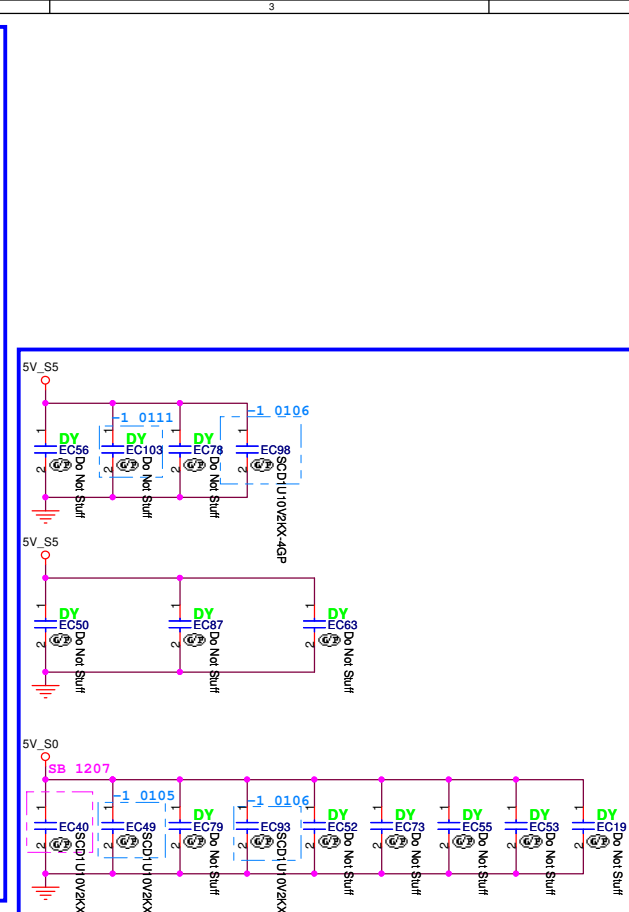
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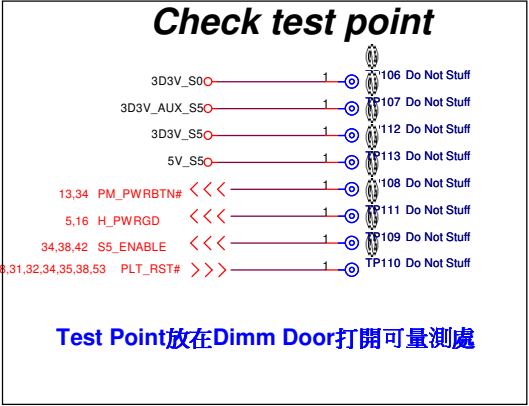


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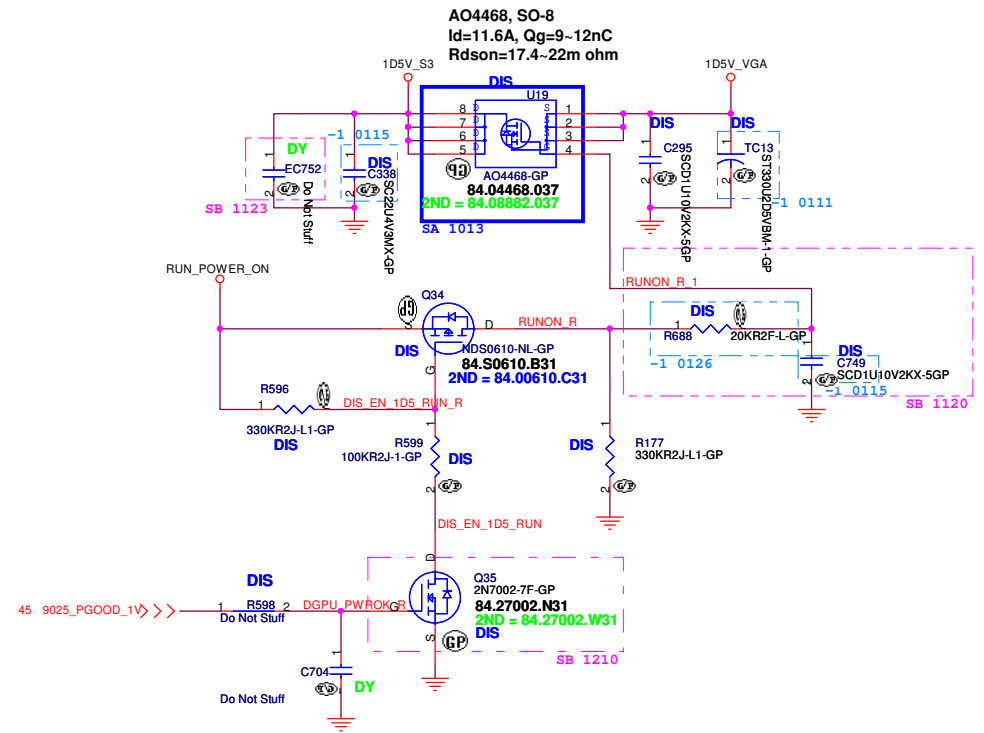
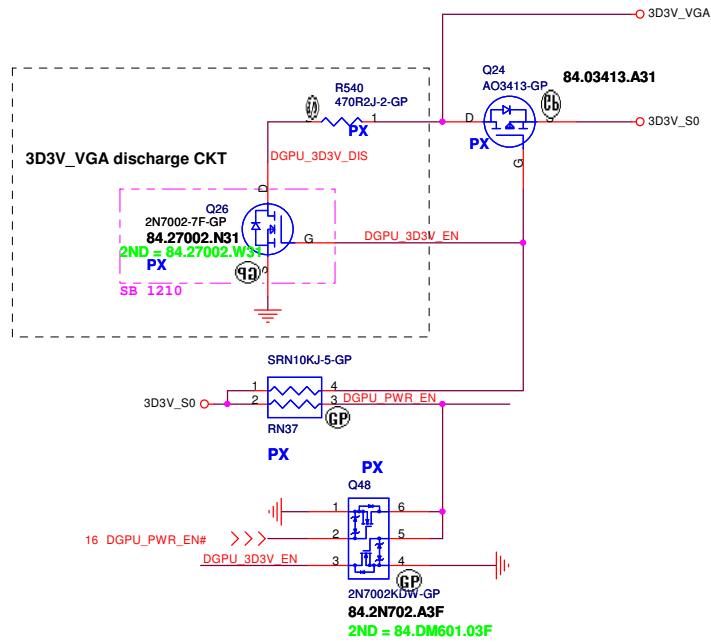
緯創資通 Wistron Corporation
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Title		
AD/BATT CONN		
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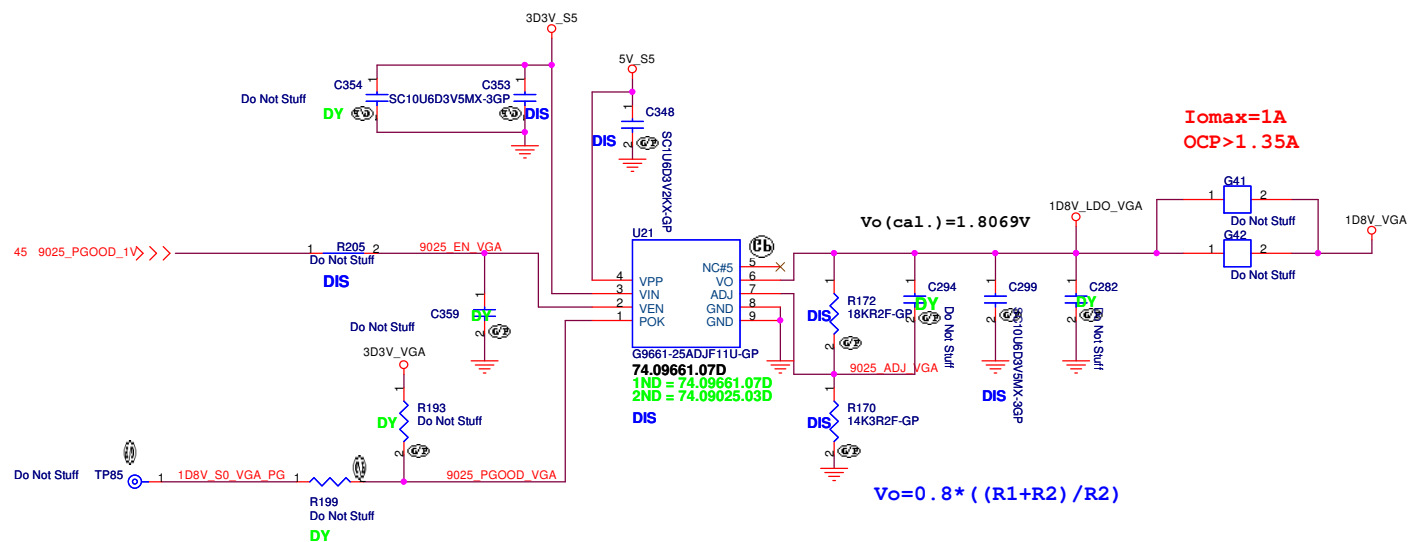




+3VS to 3.3V_DELAY Transfer



G9661 for 1D8V_VGA



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Title

ATI POWER

Size	A3
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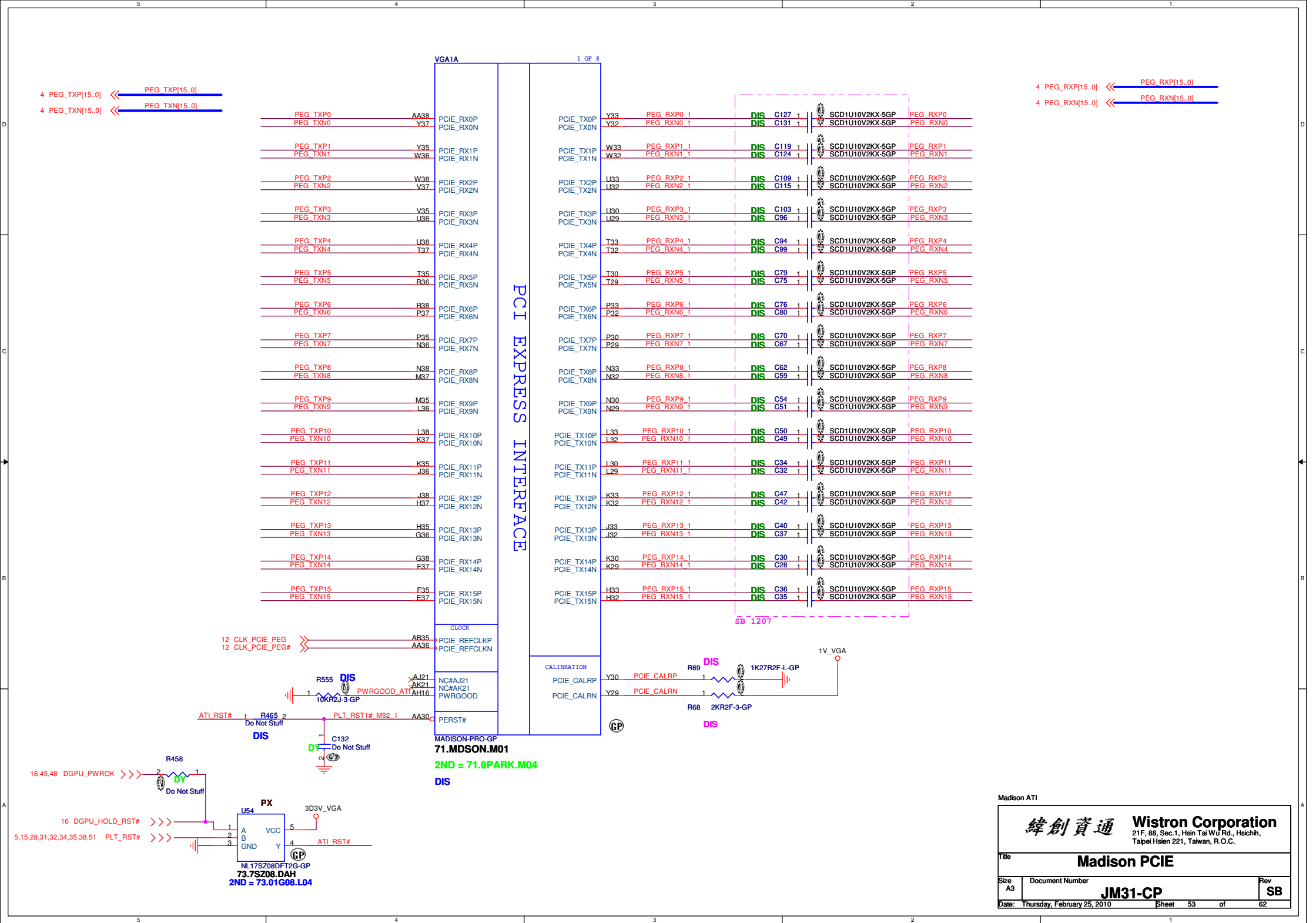
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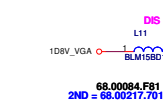
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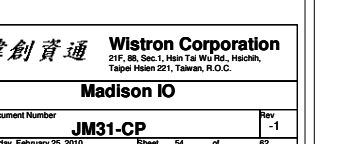
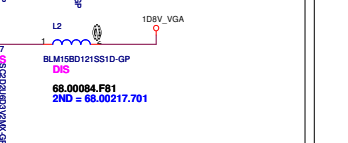
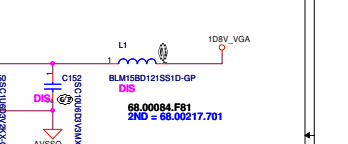
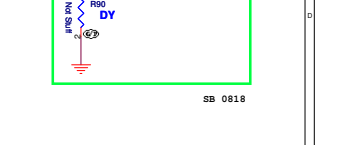
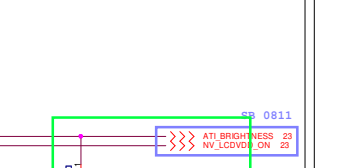
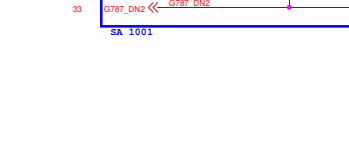
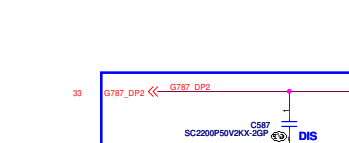
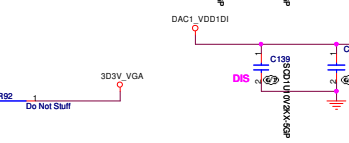
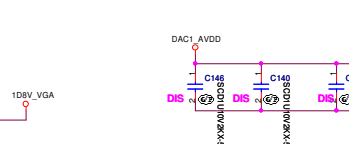
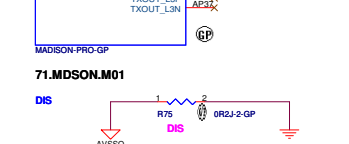
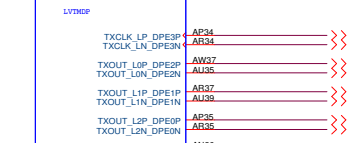
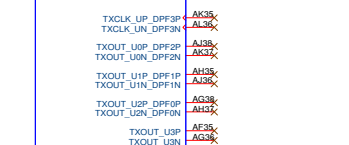
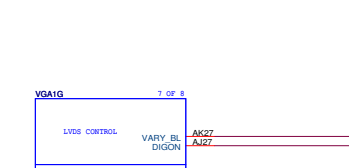
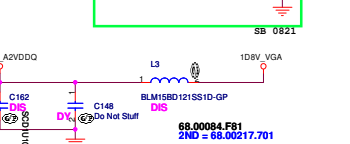
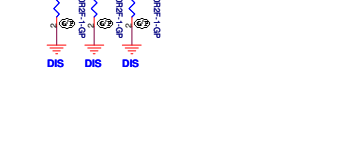
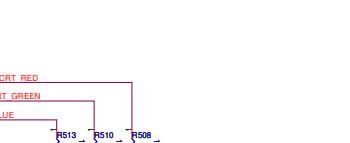
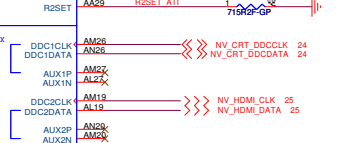
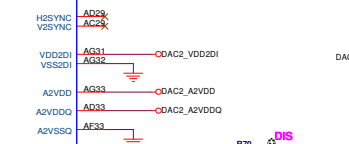
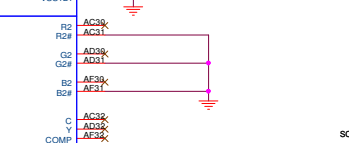
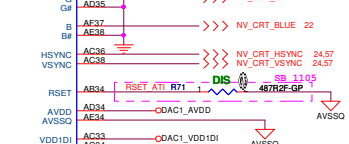
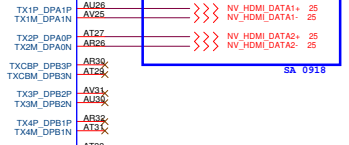
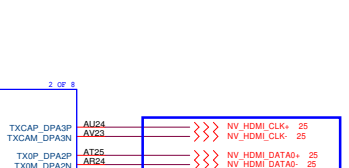
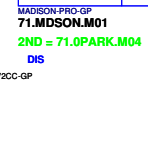
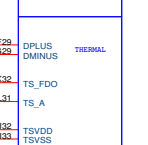
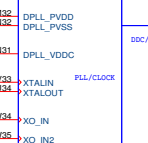
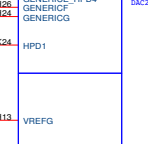
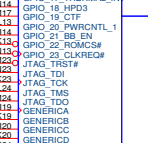
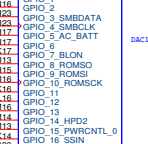
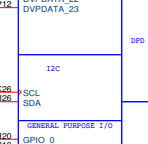
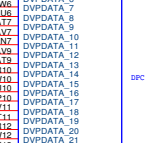
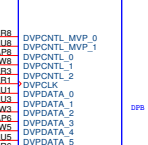
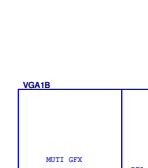
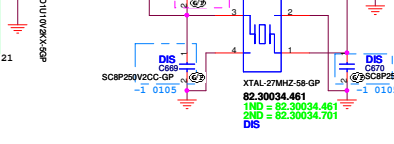
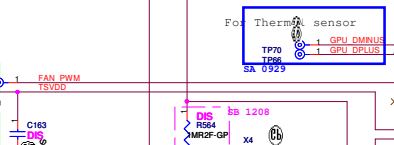
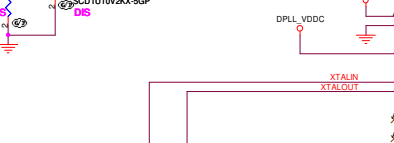
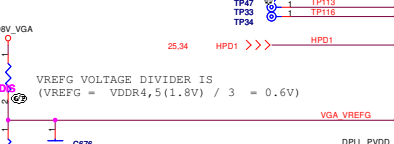
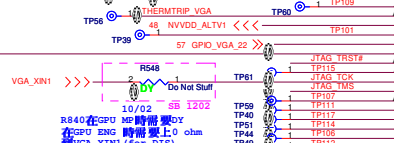
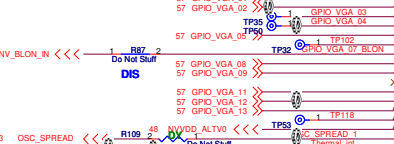
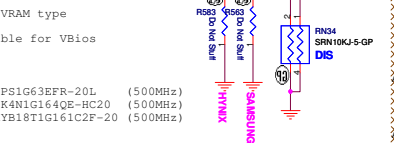
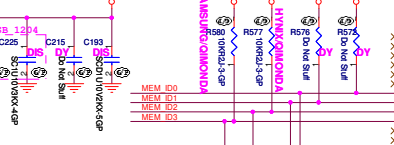
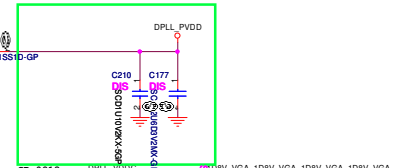
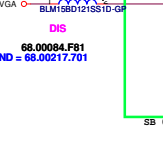
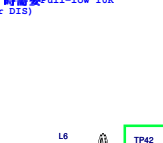
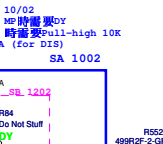
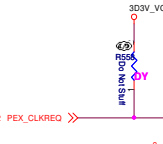
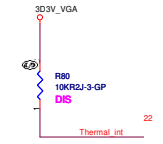


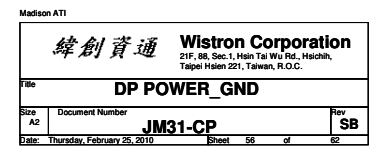
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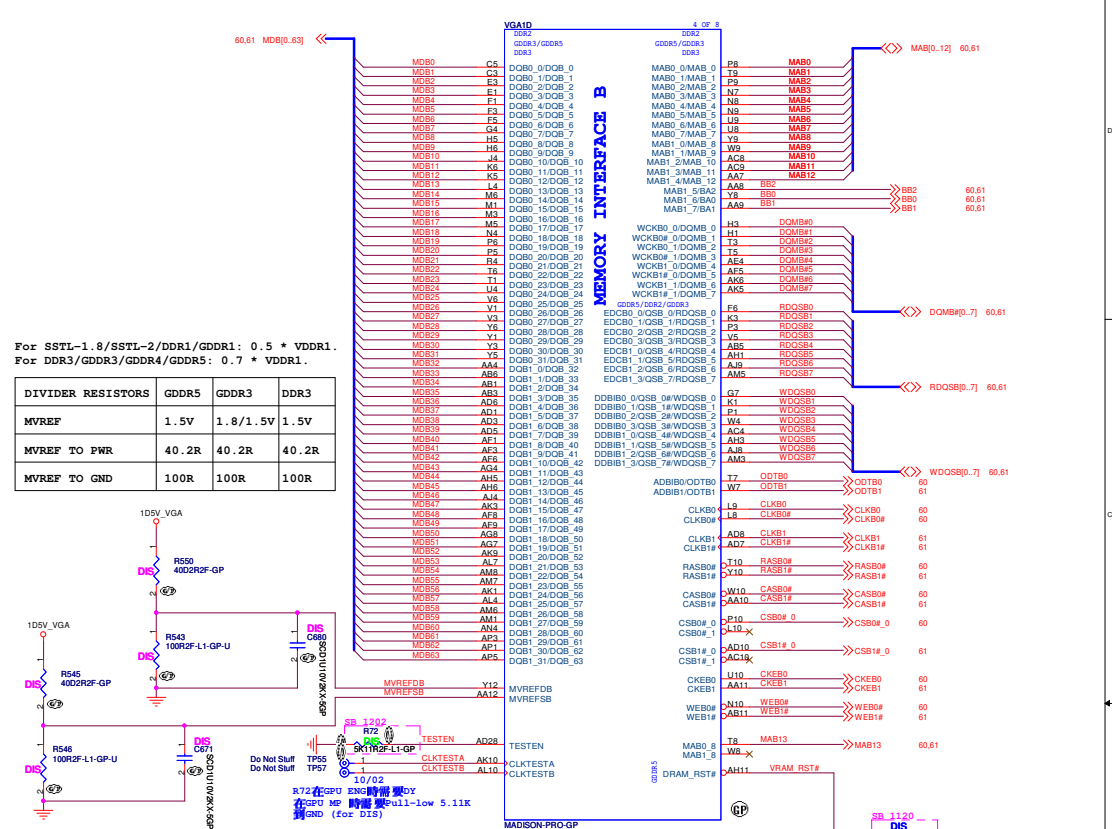
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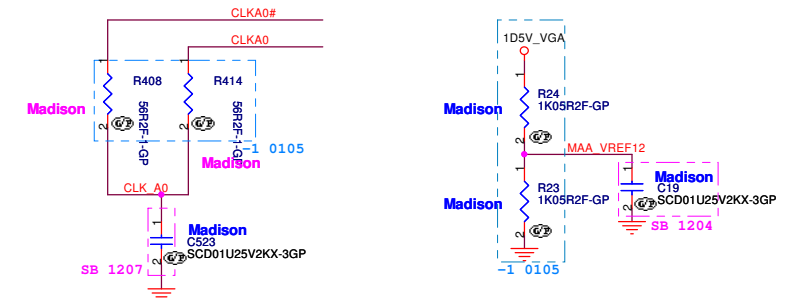
0100	512MB	Hynix-H5PS1G63EFR-20L	(500MHz)
1000	512MB	Samsung-K4N1G164QE-HC20	(500MHz)
1100	512MB	QIMONDA-HYB18T1G161C2P-20	(500MHz)

It's strap for GDDR3-136ball
Need to Clarify





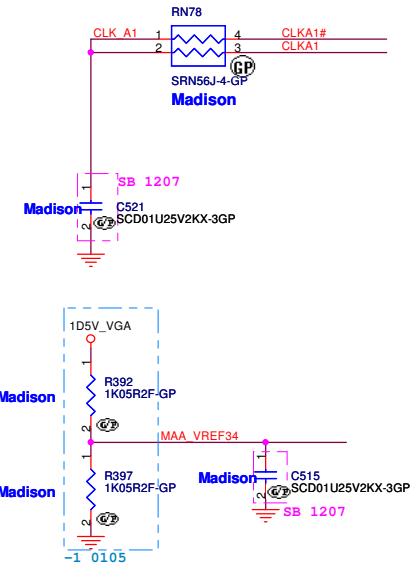
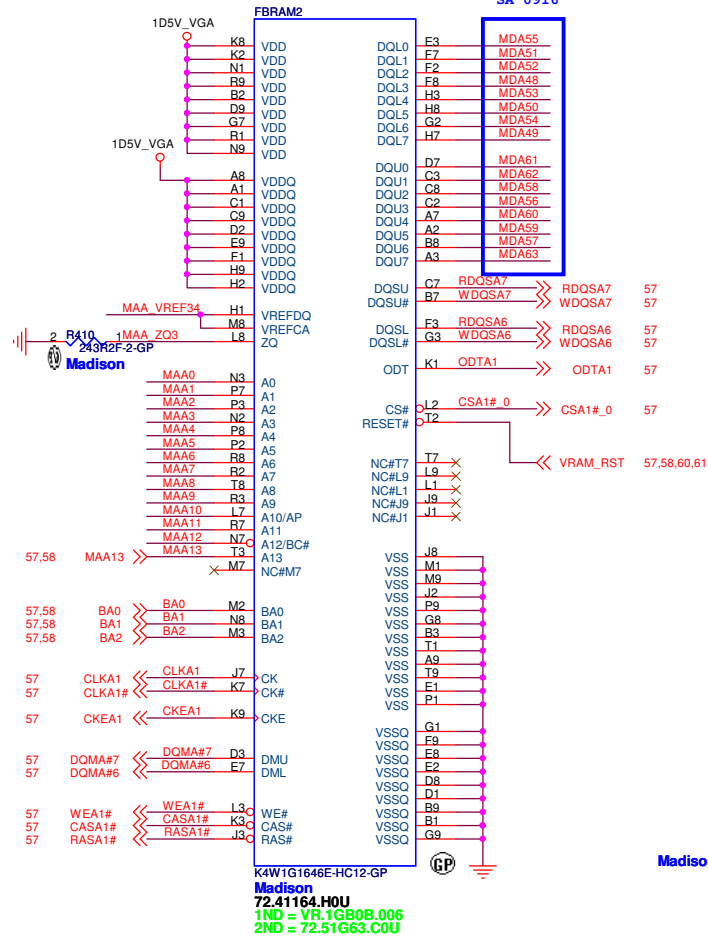
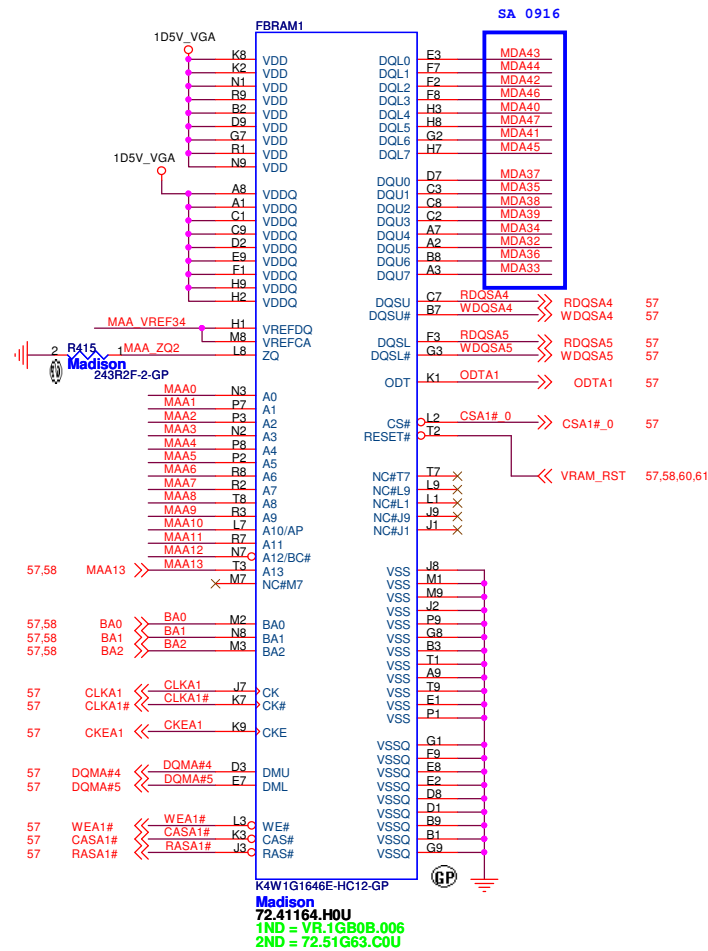
[illegible]



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HYNIX: 72.51G63.C0U (VR.1GB0G.004)

57,58 DQMA[0..7] <<>

57,58 RDQSA[0..7] <<>

57,58 WDQSA[0..7] <<>

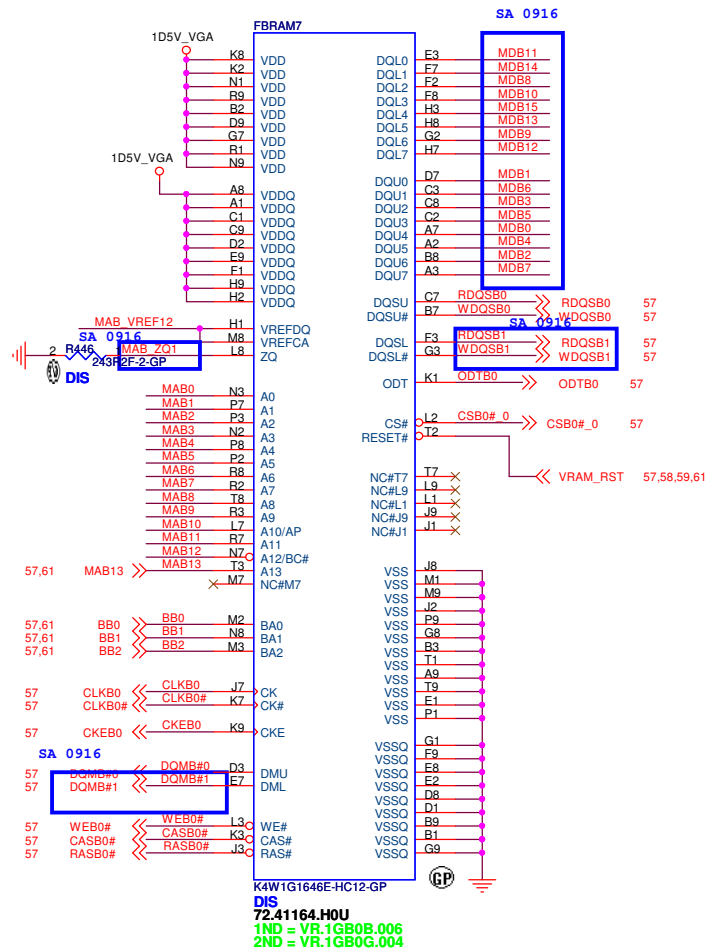
57,58 MAA[0..12] <<>

57,58 MDA[0..63] <<>

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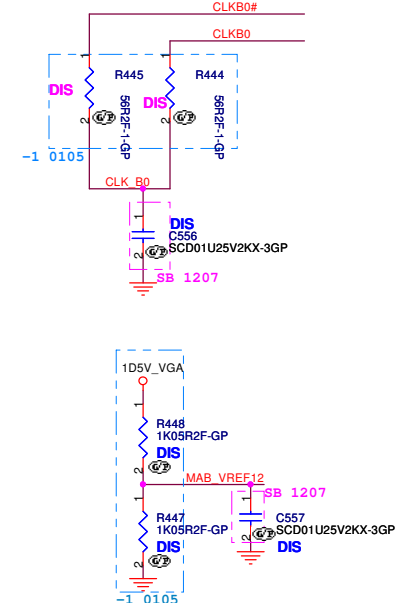
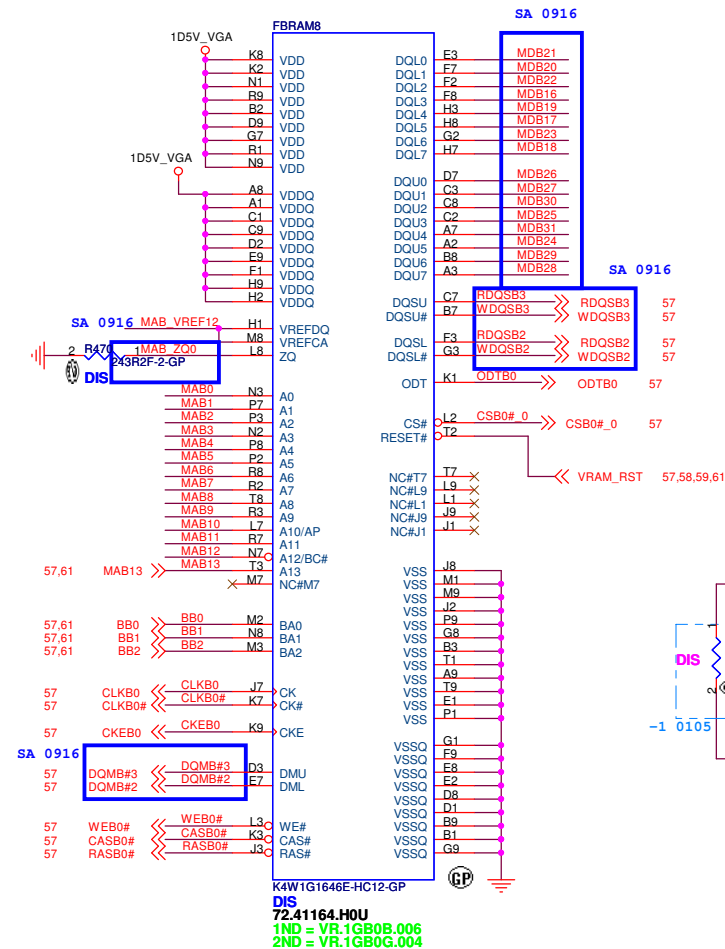
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Title			
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HYNIX: 72.51G63.C0U (VR.1GB0G.004)



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Document Number

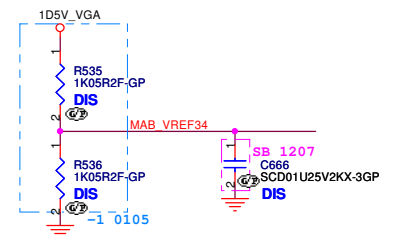
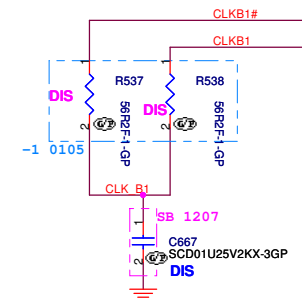
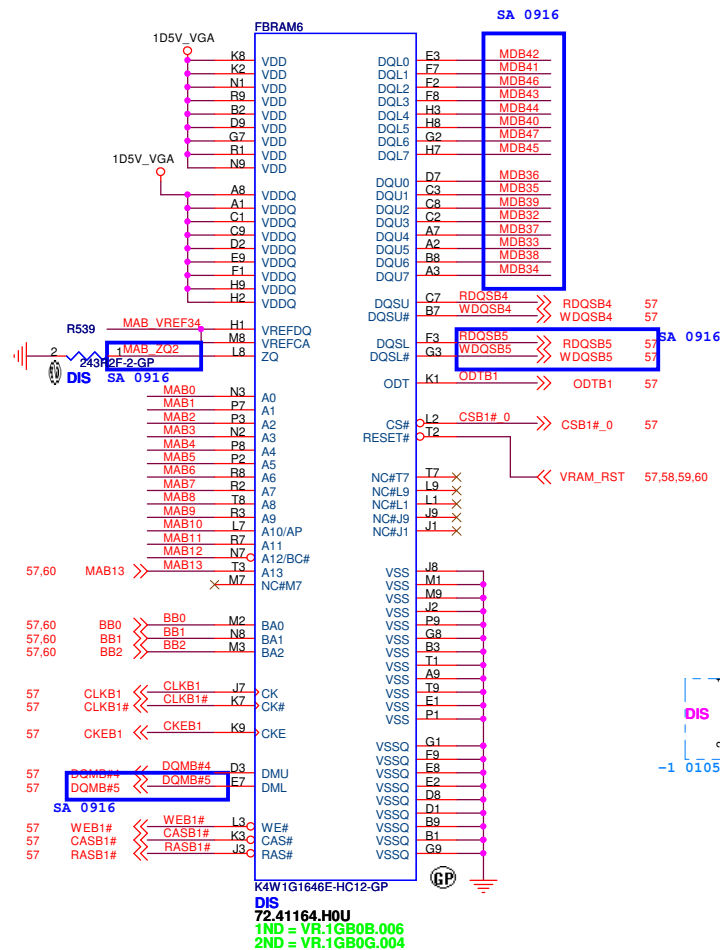
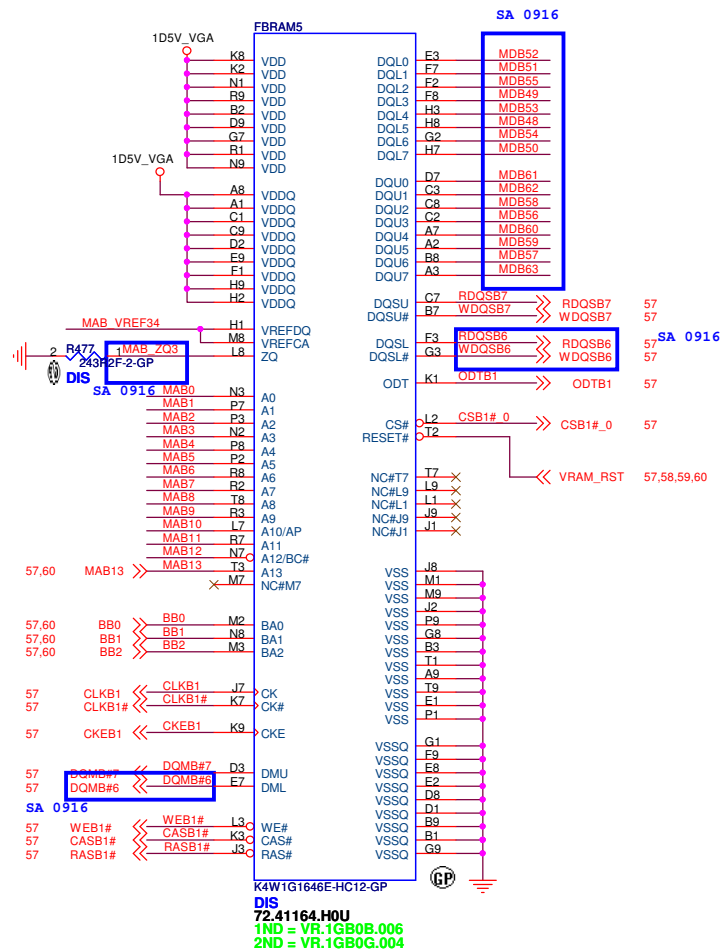
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57,60 DOMB#[0..7] <<>

57,60 RDQSB[0..7] <<>

57,60 WDQSB[0..7] <<>

57,60 MAB[0..12] <<>

57,60 MDB[0..63] <<>

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HYNIX: 72.51G63.C0U (VR.1GB0G.004)

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