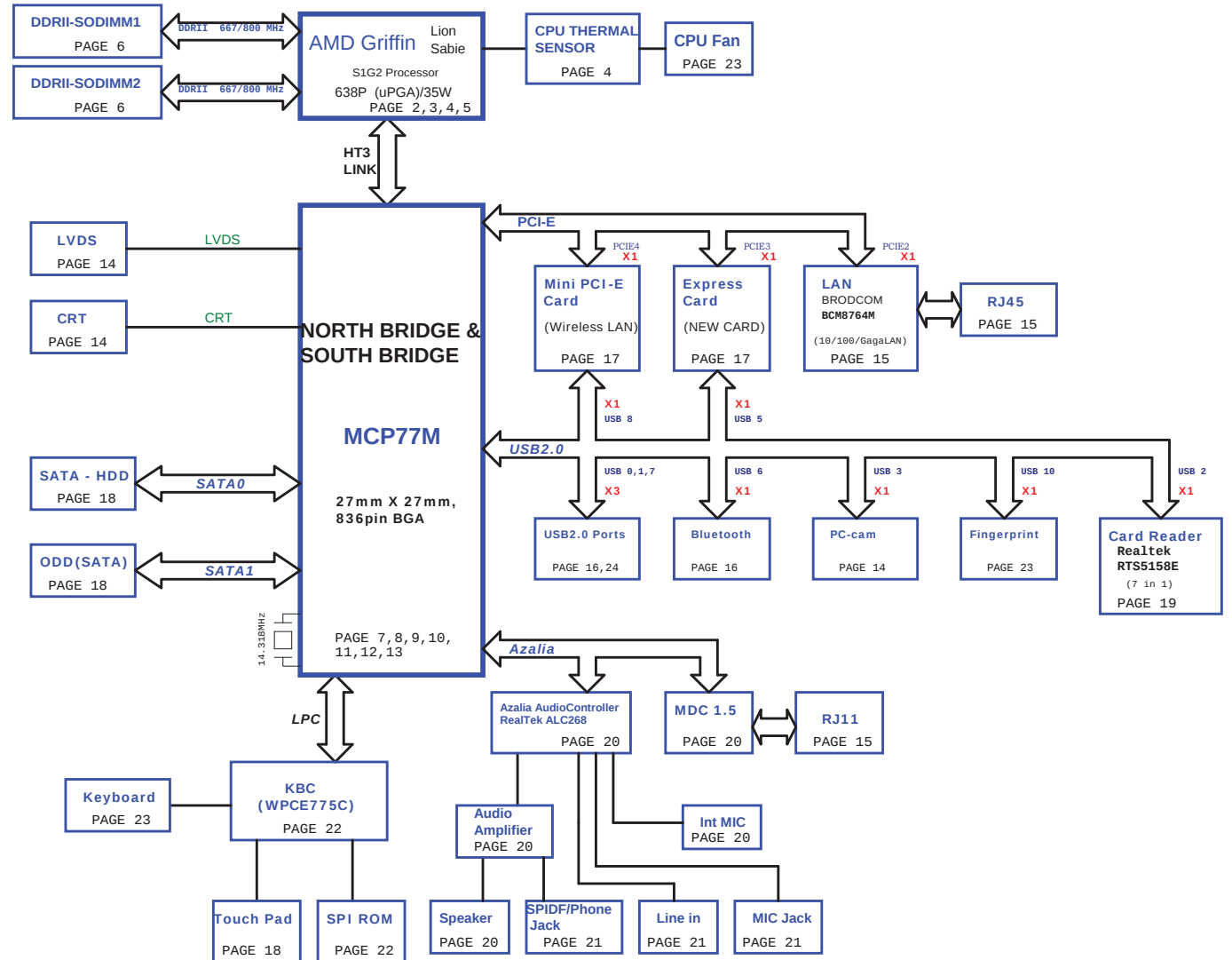


Z05 SYSTEM BLOCK DIAGRAM



CPU CORE / VDDNB (ISL6265A)	PAGE 26
NB_CORE +1.1V (RT8202)	PAGE 28
+1.1V_NB (RT8202)	PAGE 27
DDR II SMDRR_VTERM 1.8VSUS(TPSS116REGR)	PAGE 29
SYSTEM POWER (ISL6237)	PAGE 25
SYSTEM CHARGER (ISL6251A)	PAGE 24



PCB STACK UP

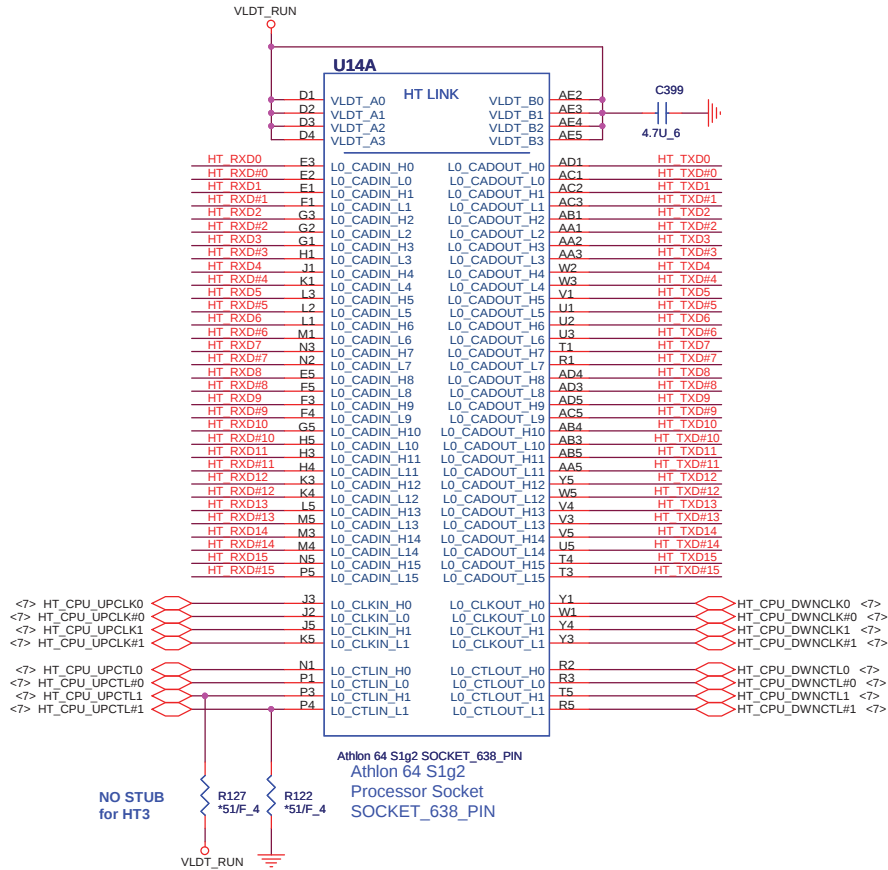
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

<7> HT_RXD#[15..0] HT_RXD[15..0]
 <7> HT_TXD#[15..0] HT_TXD[15..0]

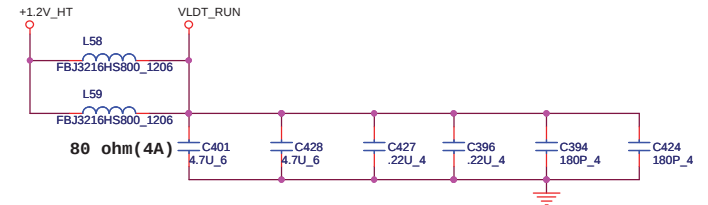


PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



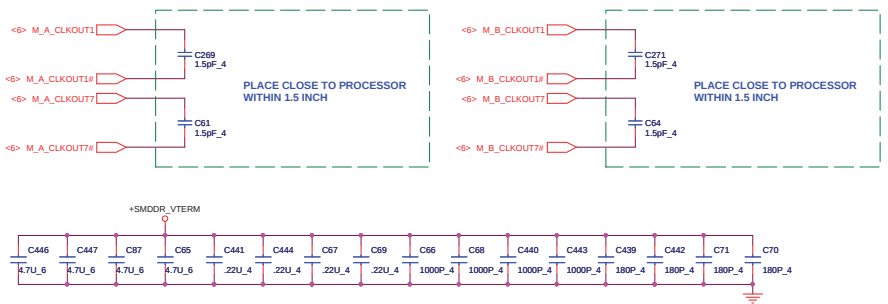
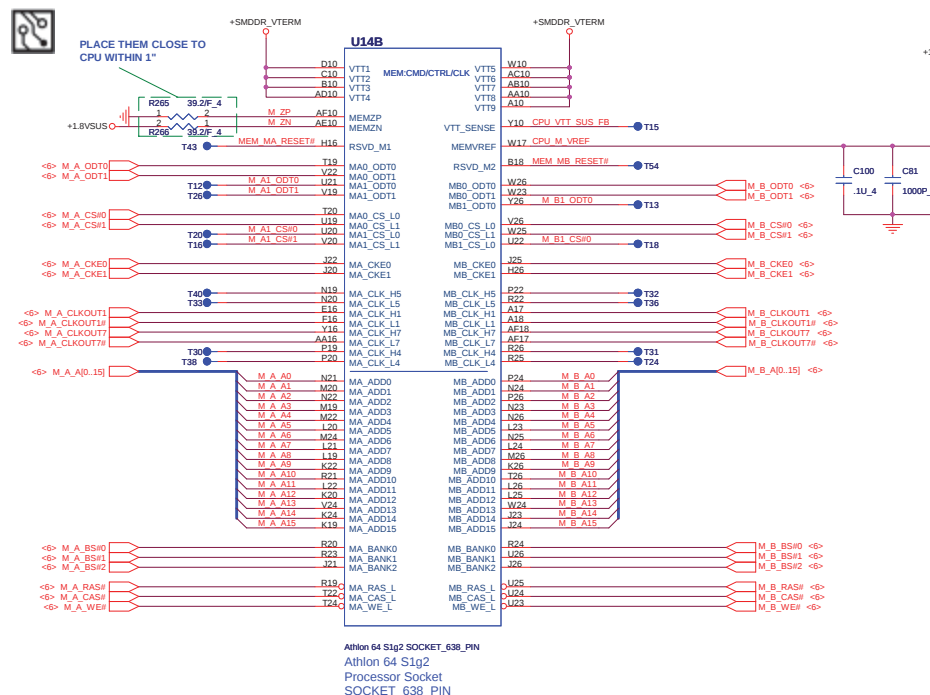
Note: on MCP77, (HT=+1.1V) and CPU(HT=+1.2V) and therefore cannot be connected to the same HT power rail.



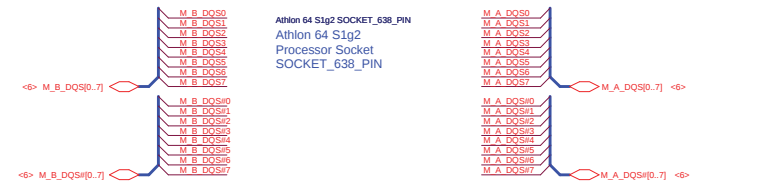
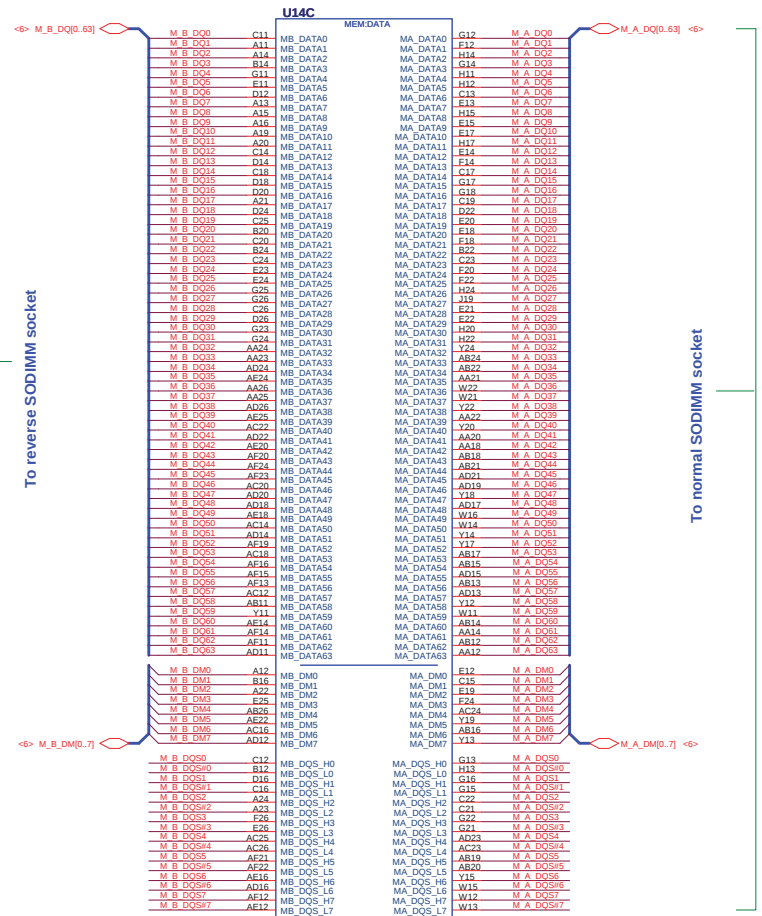
LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
 PLACE CLOSE TO VLDTO POWER PINS

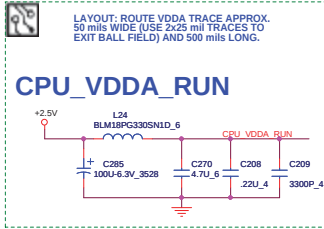
		Quanta Computer Inc. PROJECT : Z05
Size	Document Number	Rev 1A
AMD Griffin HT I/F		
Date: Monday, February 25, 2008	Sheet 2 of 34	



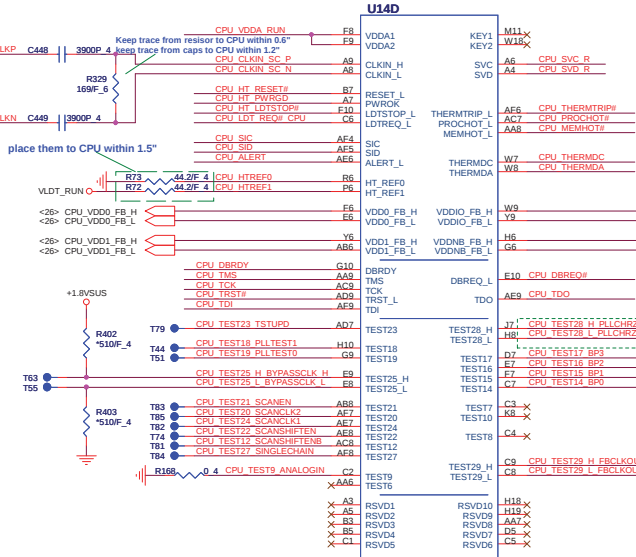
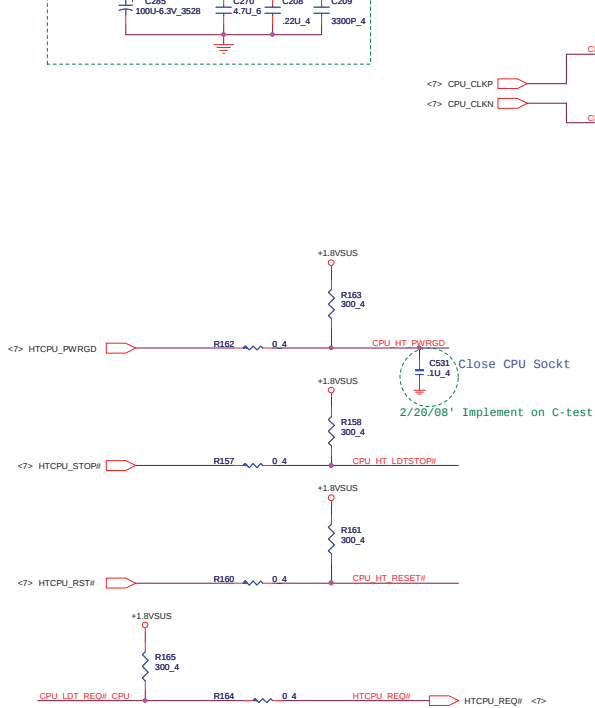
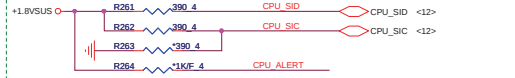
Processor DDR2 Memory Interface



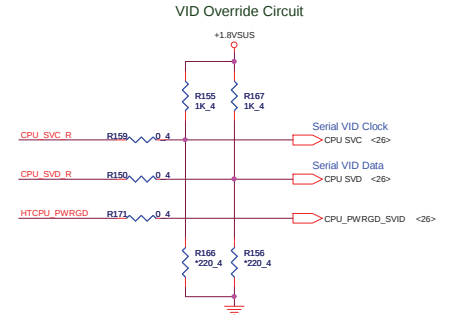
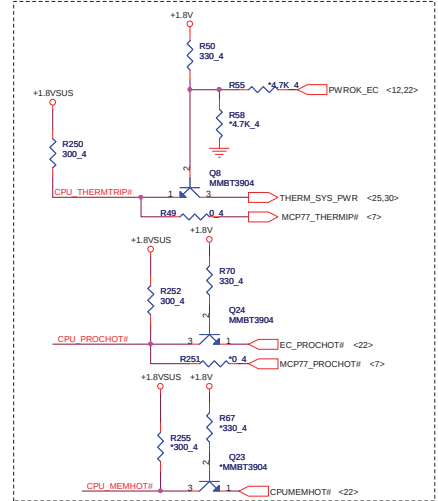
ATHLON Control and Debug



If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 390- (±5%) pulldown to VSS.

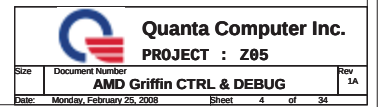
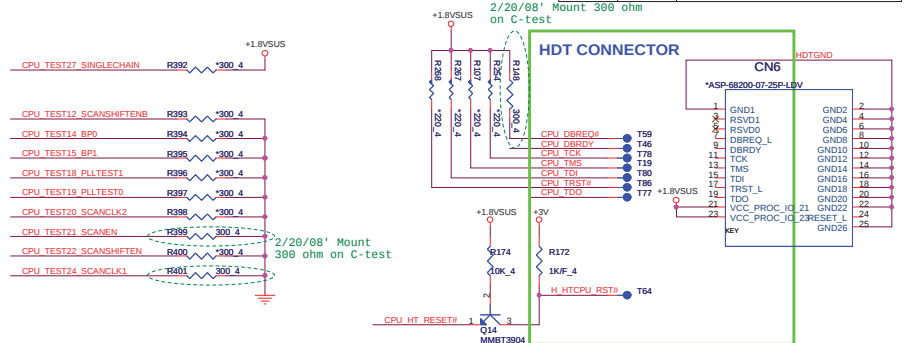
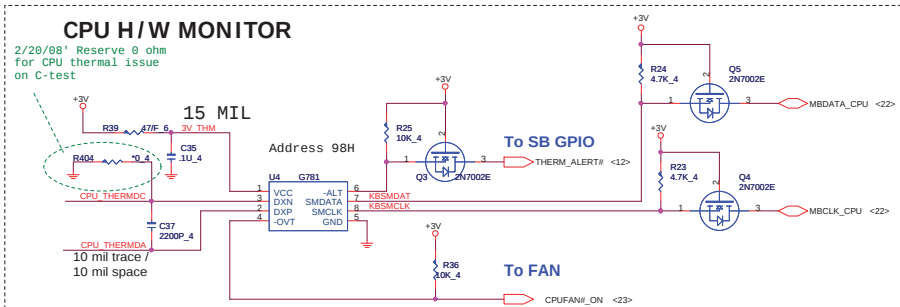


Athlon 64 S1g2 SOCKET_638_PIN

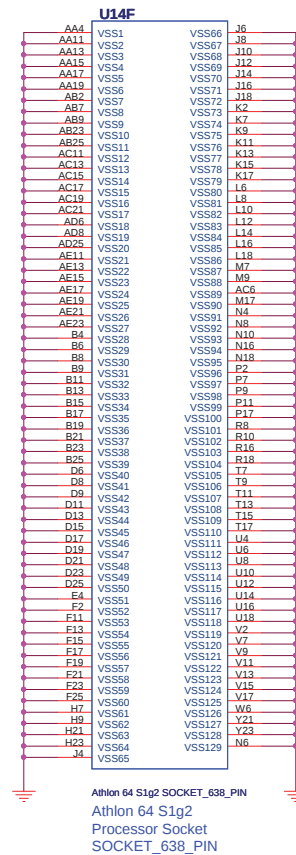
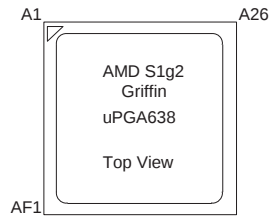
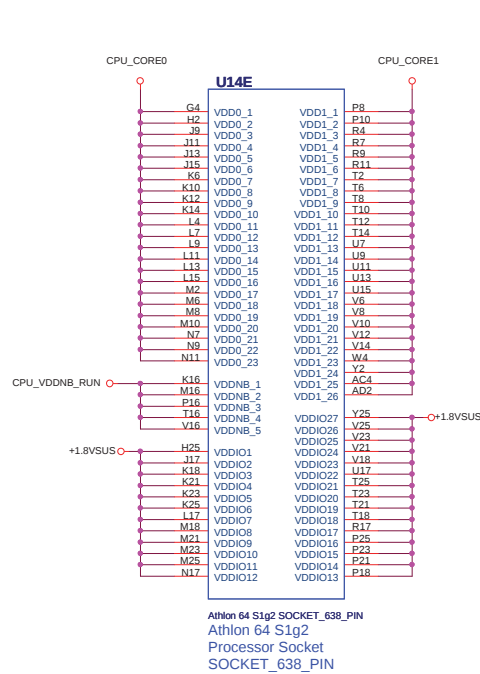


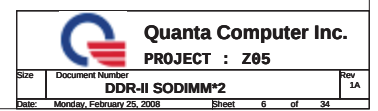
VID Override Circuit

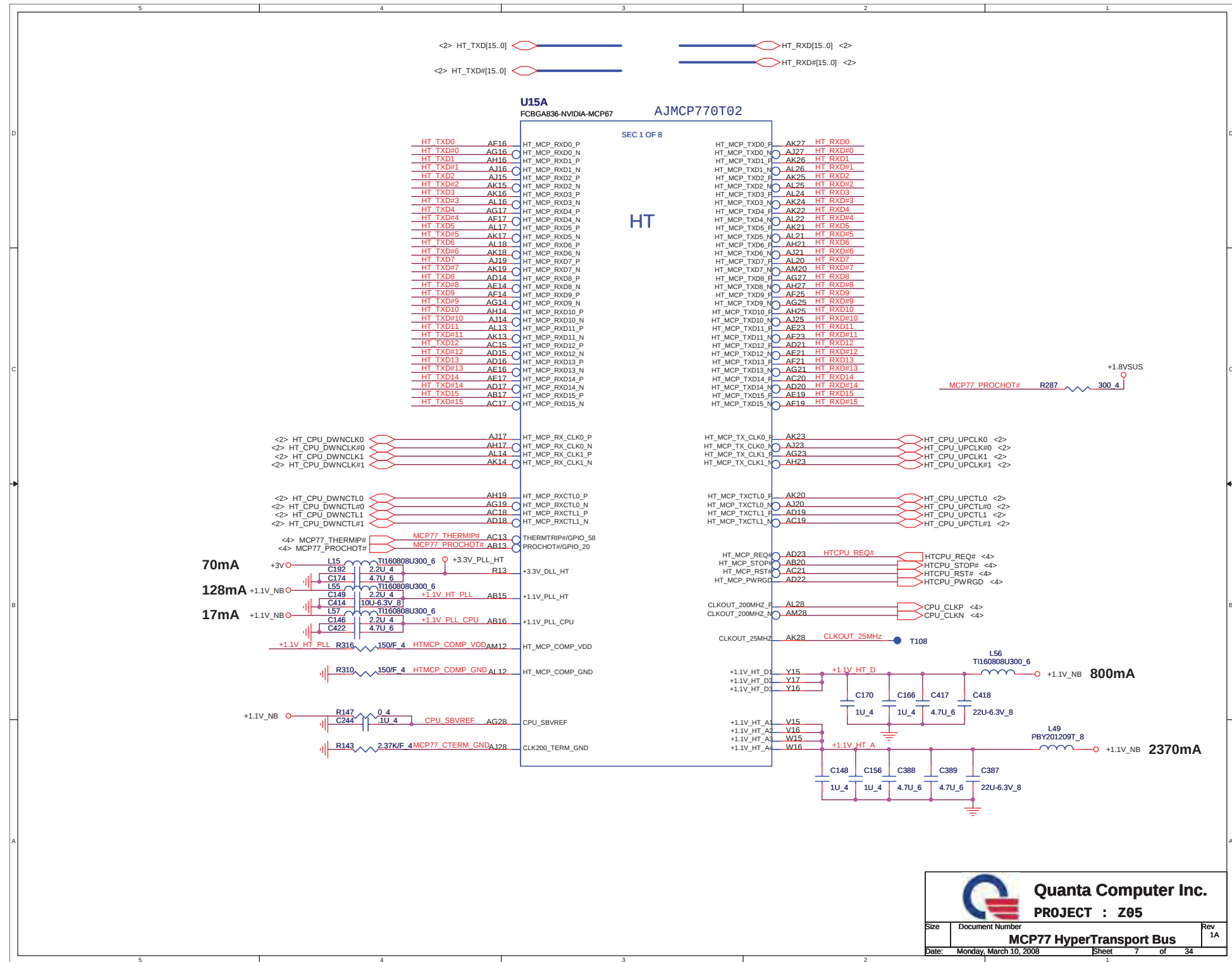
SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

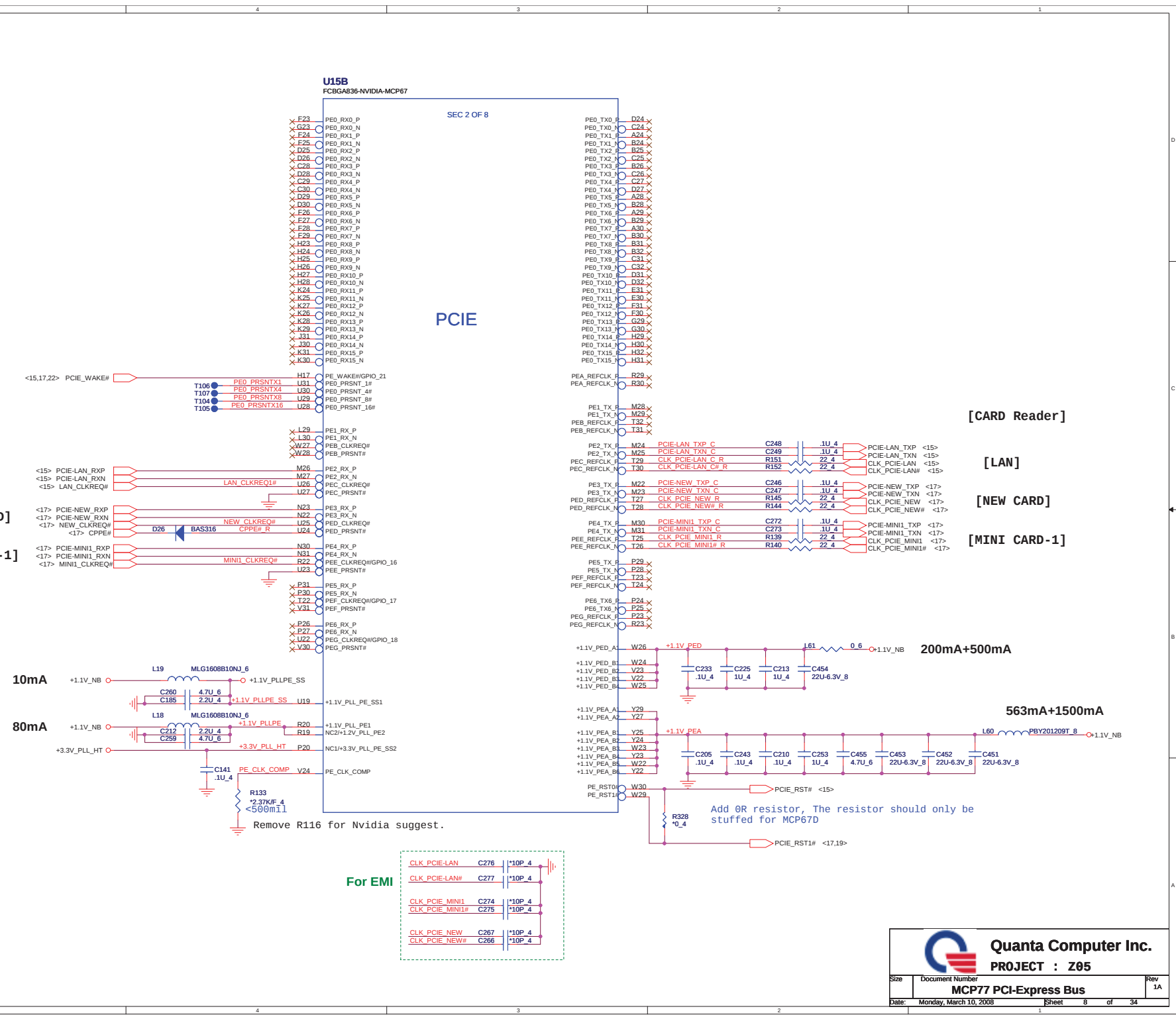


PROCESSOR POWER AND GROUND









U15B
FCBGA36-NVIDIA-MCP67

SEC 2 OF 8

PCIE

[LAN]

[NEW CARD]

[MINI CARD-1]

[CARD Reader]

[LAN]

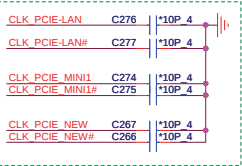
[NEW CARD]

[MINI CARD-1]

Remove R116 for Nvidia suggest.

Add 0R resistor, The resistor should only be stuffed for MCP67D

For EMI



Quanta Computer Inc.
PROJECT : Z05

Size	Document Number	Rev
	MCP77 PCI-Express Bus	1A
Date:	Monday, March 10, 2008	Sheet 8 of 34

U15D

FCBGA836-NVIDIA-MCP67

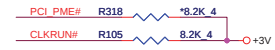
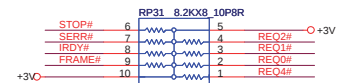
PCI

MCP77
SEC 4 OF 8

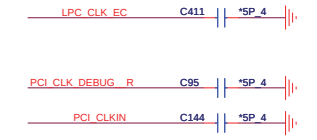
LPC

IDE

PCI/LPC PULL-UP

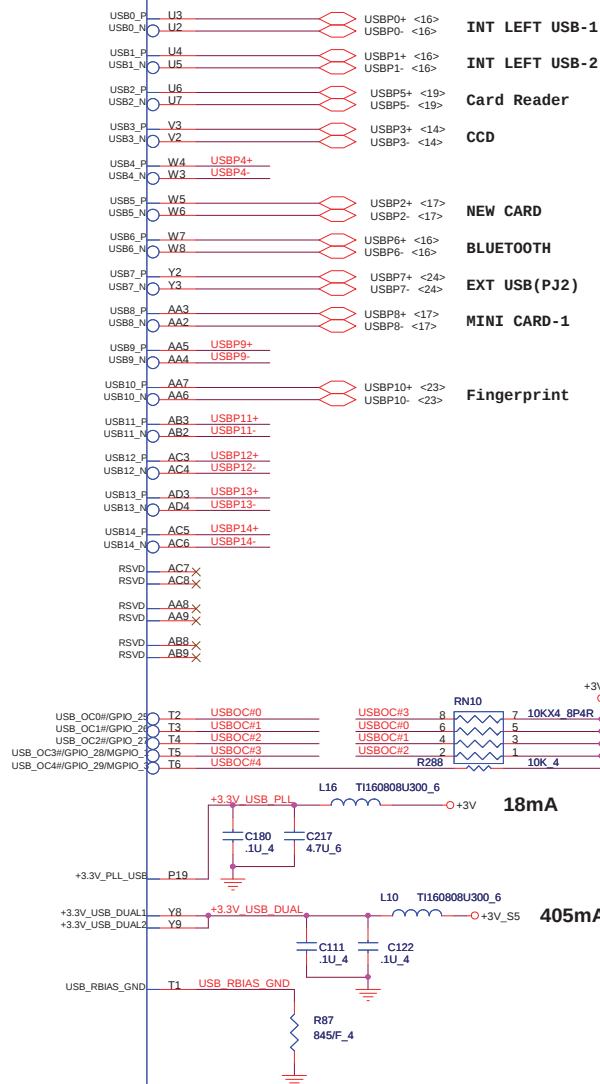
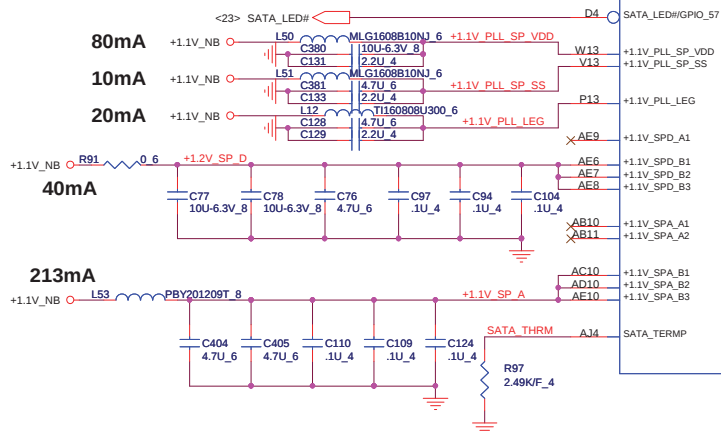
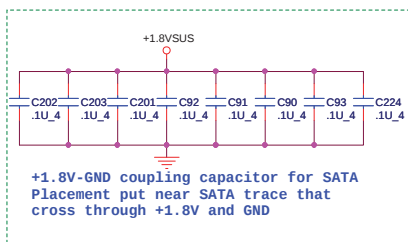


CLOCK BYPASS



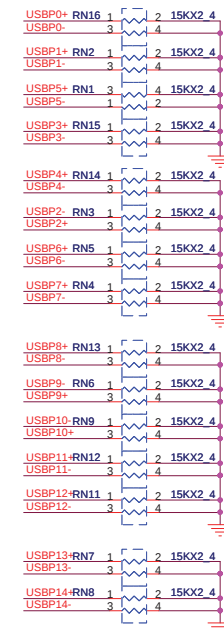


USB



2007/11/29: Page11 the resistor R87 from 909ohm change to 845ohm(follow NV suggest)

USB PULL-DOWN



Quanta Computer Inc.
PROJECT : Z05

Size	Document Number MCP77 SATA and USB	Rev 1A
Date:	Sunday, March 09, 2008	Sheet 11 of 34

Date: Sunday, March 09, 2008 Sheet 11 of 34

U15F FCBGA836-NVIDIA-MCP67

HDA

MISC

HDA

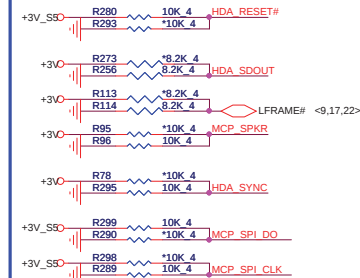
HDA_SDOUT	R74	22 4	HDA_SDOUT_ADO	<20>
HDA_SYNC	R77	22 4	HDA_SDOUT_MDC	<20>
HDA_BITCLK	R285	22 4	HDA_SYNC_ADO	<20>
HDA_RESET#	R292	22 4	HDA_SYNC_MDC	<20>
	R81	22 4	HDA_BITCLK_ADO	<20>
	R86	22 4	HDA_BITCLK_MDC	<20>
	R284	22 4	HDA_RESET#_ADO	<20>
	R291	22 4	HDA_RESET#_MDC	<20>

EMI Solution

HDA_SDOUT	C373	10P 4
HDA_SYNC	C395	10P 4
HDA_RESET#	C393	10P 4
HDA_BITCLK	C392	10P 4

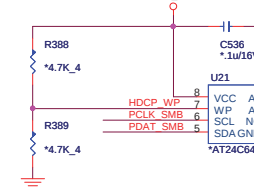
MCP77 STRAPPING

HDA_RESET# (LAN)	0	MII
HDA_SDOUT_B (L1RAMI# (BIOS)	0	L1C (DEFAULT)
HDA_SYNC_R (SIO CLOCK)	0	14.318MHz (DEFAULT)
SPI_DO SPI_CLK (SPI CLOCK)	0	31MHz
	01	42MHz
	10	25MHz
	11	1MHz

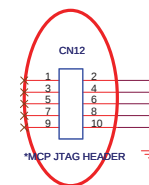


Acer Suggest Reserve HDCP EEPROM 2007/12/05

HDCP EEPROM



NO PN



M/B ID for 14"/17"

ID0	ID1	ID2	M/B
0	0	0	17" D
0	0	1	X
0	1	0	15" D
1	0	0	15" U
1	0	1	14" Dual Core CPU & MXM
1	1	0	14" Dual Core CPU & UMA
1	1	1	14" Single Core CPU & UMA

Delay 10ms
after S5 powerOK

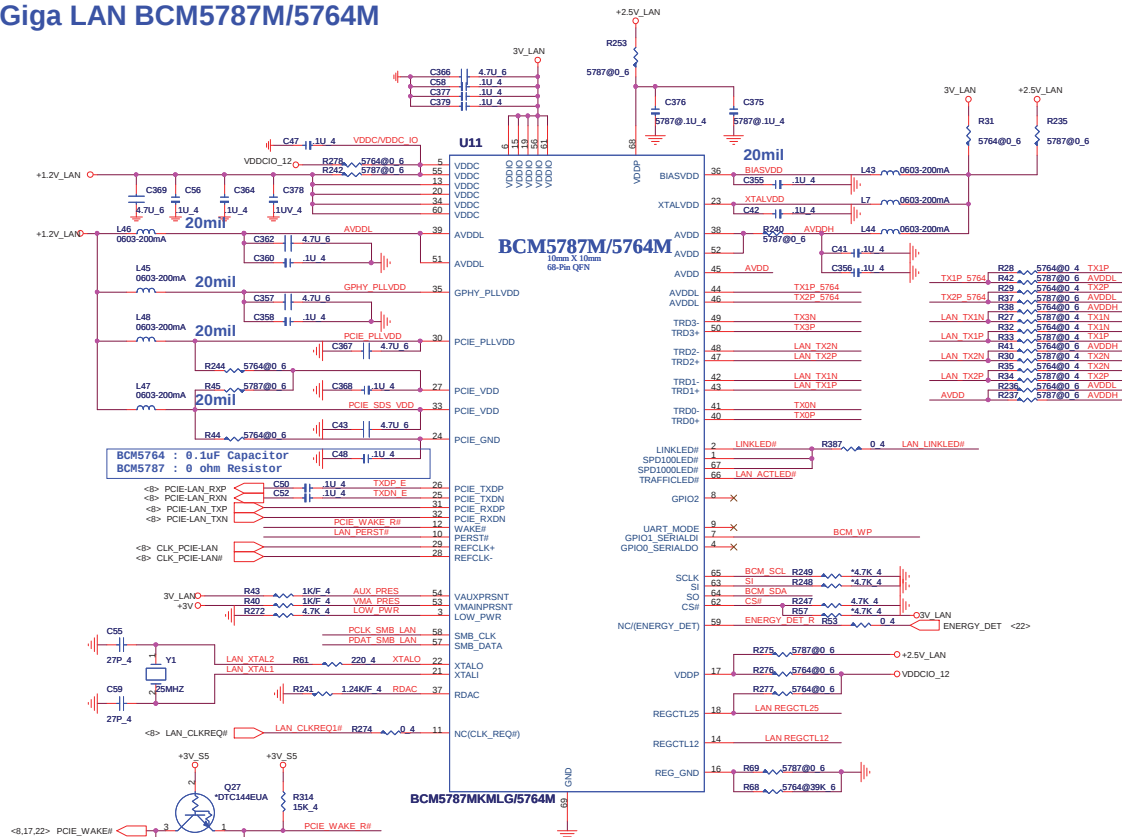
2007/11/28-Edison: Removethese part
R315, R317, R326, R324, C423, Q28, Q29

SINGLE_CH

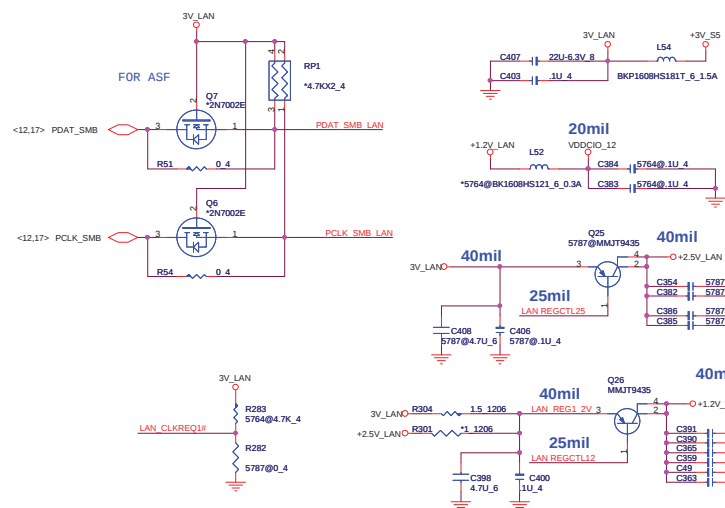


Delete TVOUT MiniDIN

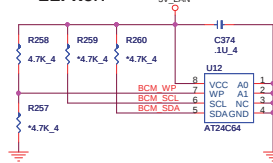
Giga LAN BCM5787M/5764M



LAN POWER



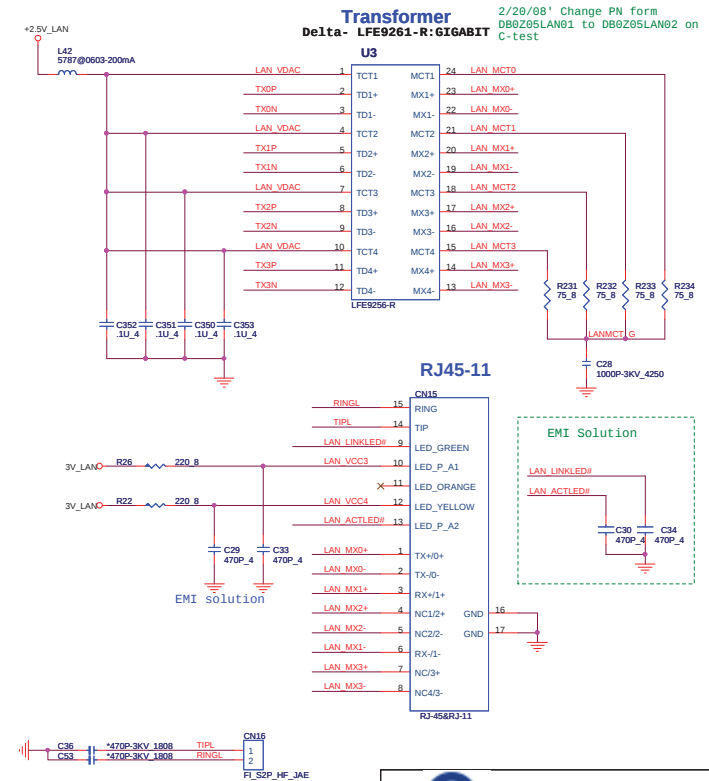
EEPROM



EEPROM Strapping

	S0	SI	CS#	SCLK
24c64	1	1	0	1

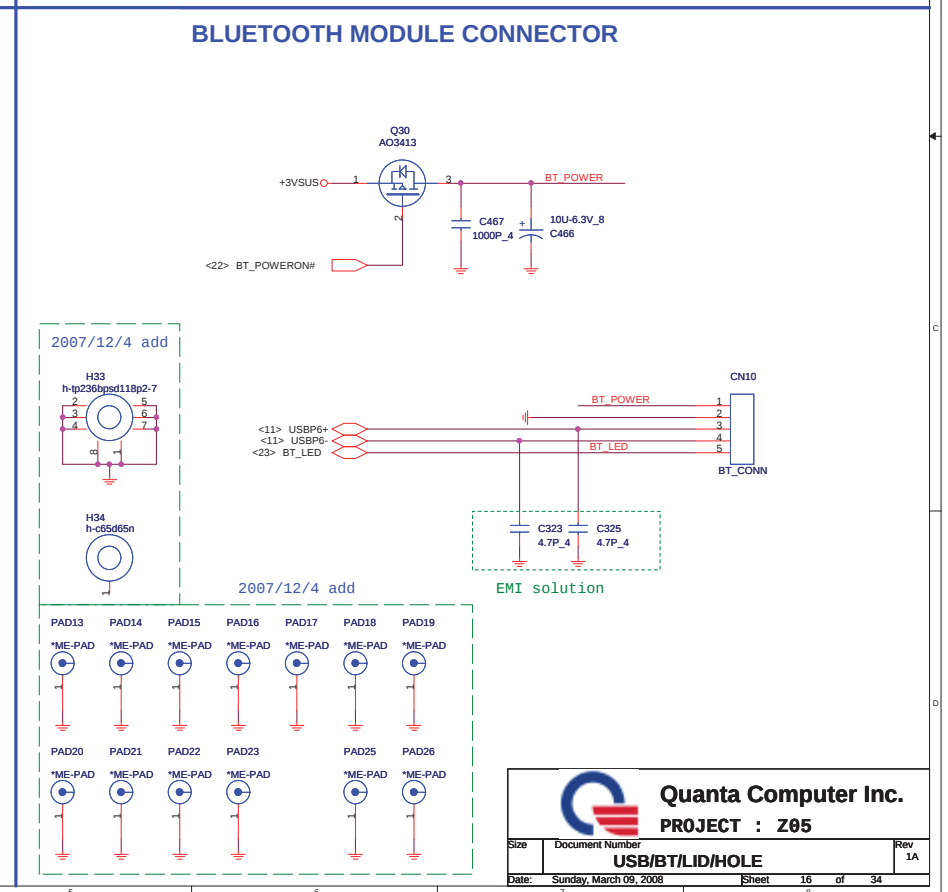
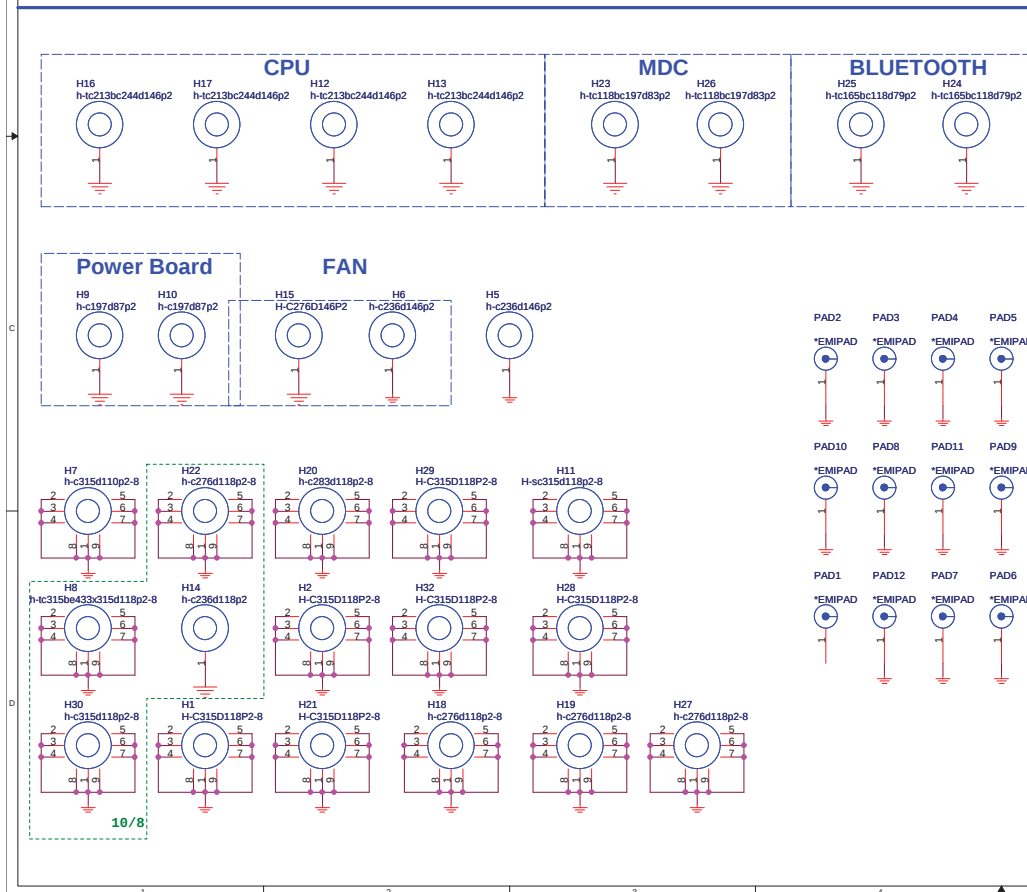
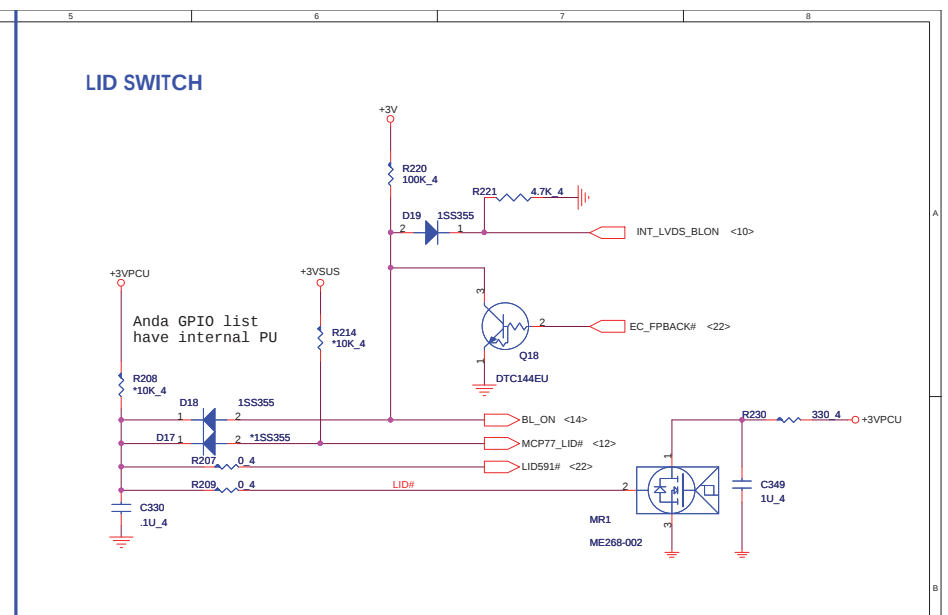
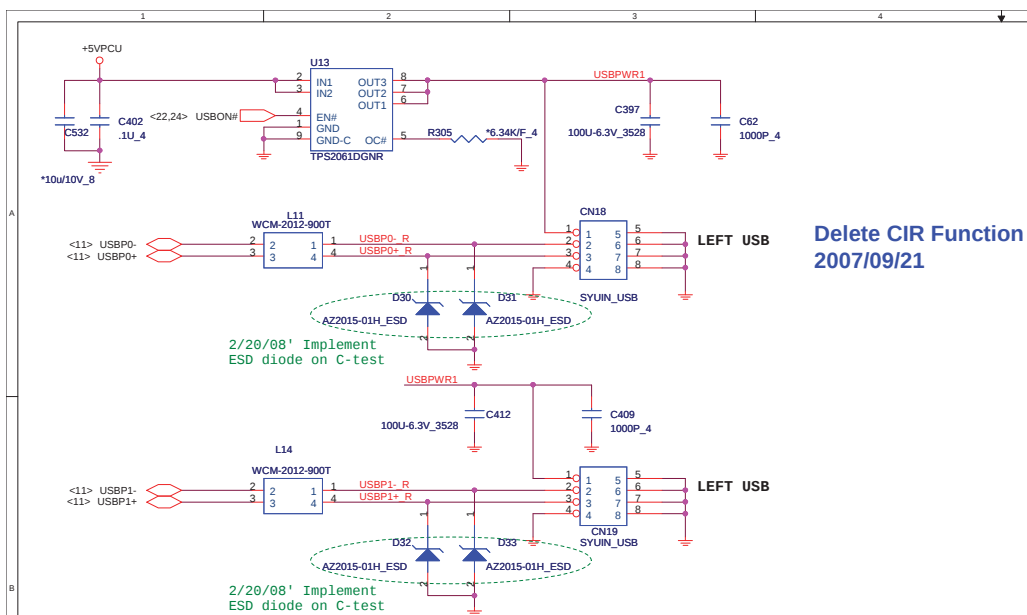
Delete LAN within DOCK Selector



Quanta Computer Inc.
PROJECT : Z05

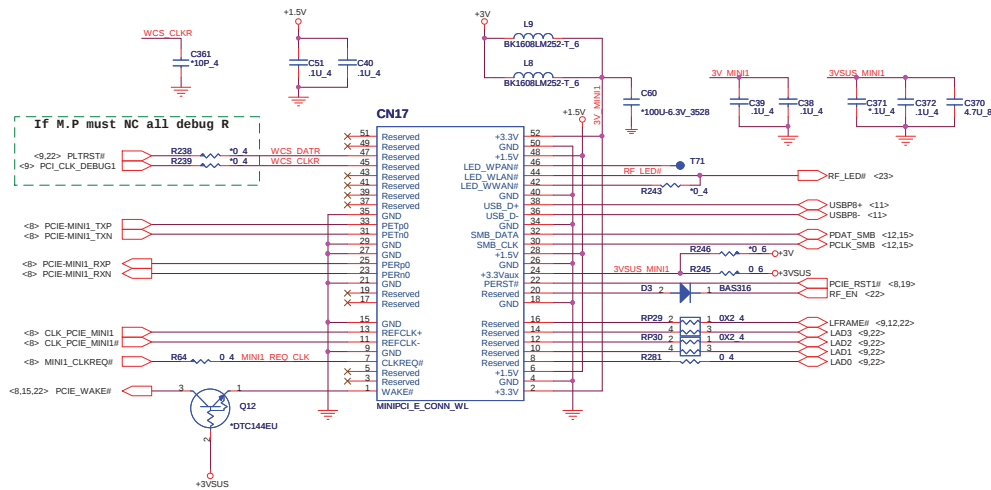
Size	Document Number			Rev
	GigaLAN BCM5787/RJ45 & RJ11			1
Date:	Friday, March 07, 2008	Sheet	15	of 34

Date: Friday, March 07, 2008 Sheet 15 of 34



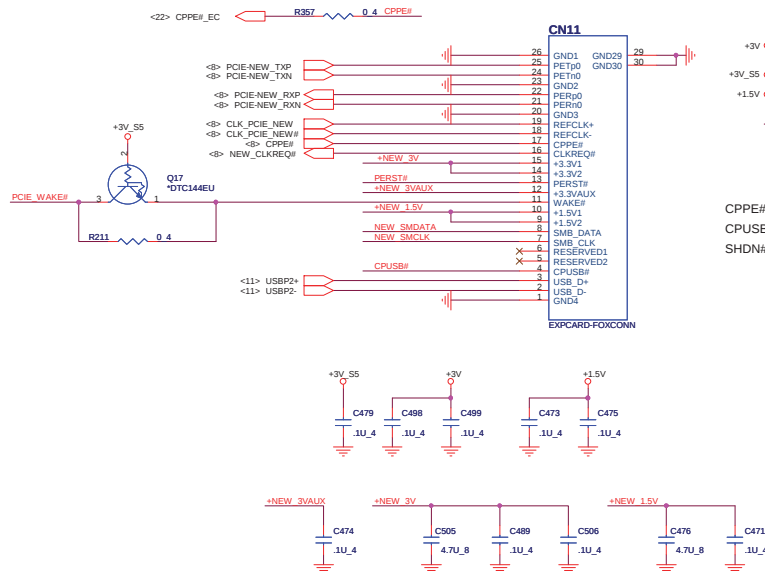
MINI-Card

MINI-Card Port-1

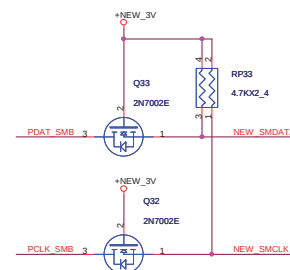
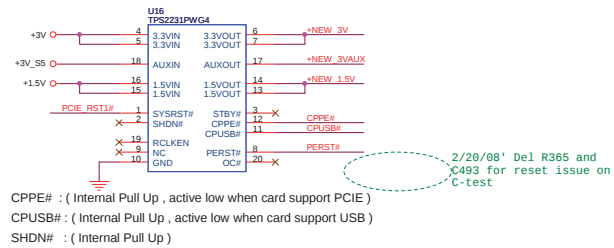


Delete MINI-Card Port-2

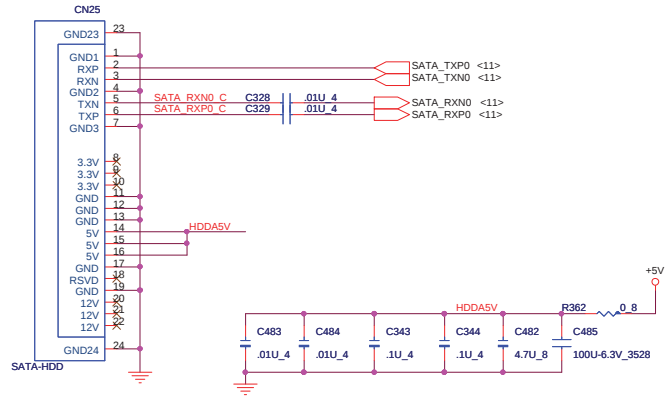
New card



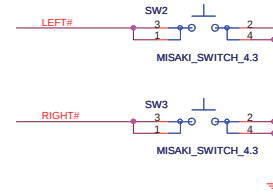
NEW CARD'S POWER SWITCH



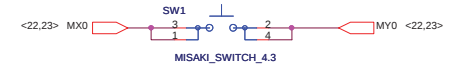
SATA HDD



TP SWITCH

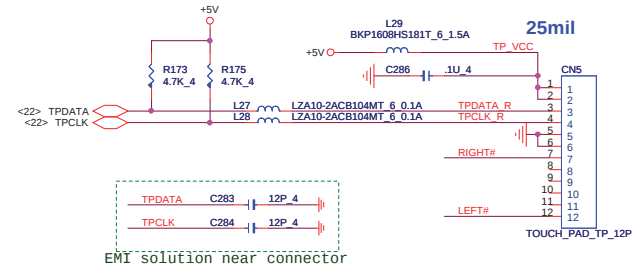


E-KEY

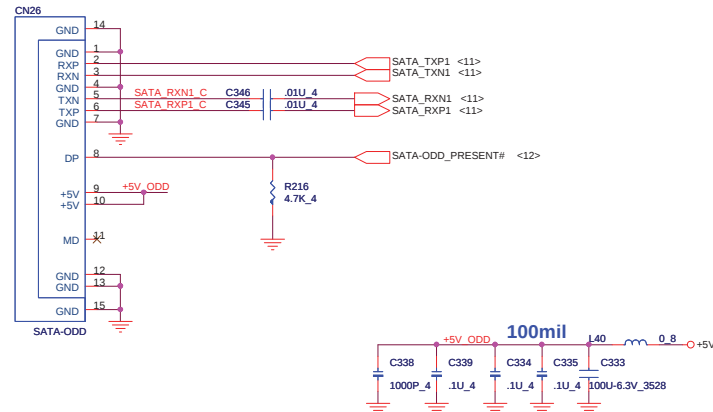


MX0 MY0:E-Key

TP CONN



ODD (SATA)



[illegible]

Three circuit diagrams showing the connection of capacitors C533, C534, and C535. Each capacitor is connected between ADOGND and a CPGND pin (CPGND_3, CPGND_2, and CPGND_1 respectively). The capacitors are labeled with a value of *1U_4.

AGC_Attack (4 pin)	Attack time
LOW	1 ms
Hi	2 ms

AGC ON/OFF selection

AGC_ON/OFF (6 pin)	AGC ON/OFF
LOW	ON
Hi	OFF

AGC Recovery1 (10 pin)	AGC Recovery2 (11 pin)	Recovery Time
LOW	LOW	1.0 s
LOW	Hi	2.0 s
Hi	LOW	4.0 s
Hi	Hi	8.0 s

AGC Lv1 (2 pin)	AGC Lv2 (3 pin)	AGC ON Level	Output Po (RL=8 ohm)
LOW	LOW	9.8 dBV	1.2 W
LOW	Hi	9.0 dBV	1.0 W
Hi	LOW	8.1 dBV	0.8 W
Hi	Hi	6.0 dBV	0.5 W

The schematic diagram illustrates the speaker output stage. It features a differential amplifier configuration using MOSFETs M1 and M2. The gates of M1 and M2 are biased by a current source (M3) connected to VDD and a tail current source (M4) connected to ADPGND. The drains of M1 and M2 are connected to a load resistor (R1) and a speaker (S1) respectively. The speaker is connected to a 4-pin connector labeled SPEAKER_H1_95. The circuit is powered by VDD and ADPGND, with decoupling capacitors C301, C297, C290, and C289.

SP_STBY1 (33 pin)	SP_STBY2 (34 pin)	SP_STBY ON/OFF
LOW	LOW	ON
LOW	Hi	OFF
Hi	LOW	OFF
Hi	Hi	OFF

HP_STBY1 (35 pin)	HP_STBY2 (36 pin)	HP_STBY ON/OFF
LOW	LOW	ON
LOW	Hi	OFF
Hi	LOW	OFF
Hi	Hi	OFF

MUTE FUNCTION

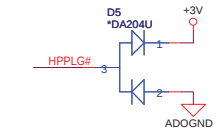
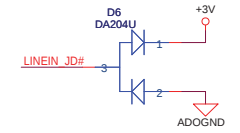
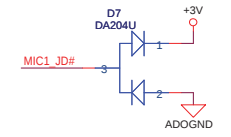
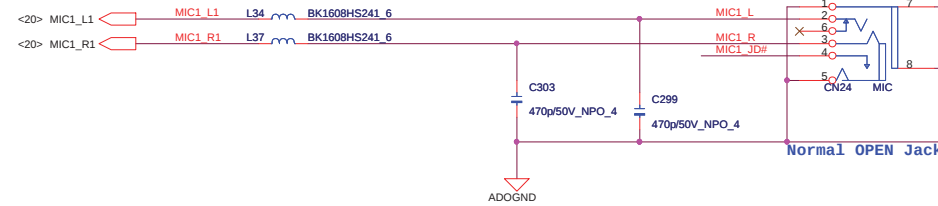
The diagram shows two comparators, U1B and U2D, configured as voltage detectors. Both comparators have their non-inverting inputs (pin 1) connected to a +3V supply. The inverting inputs (pin 2) are connected to the MUTE signals: AMP_MUTE# for U1B and HP_MUTE# for U2D. The outputs (pin 4) of both comparators are connected to ground through resistors R37 and R36, respectively. The resistors are labeled with a value of 33V, likely indicating a 33kΩ value. The comparators are labeled 1TCS75.

U17

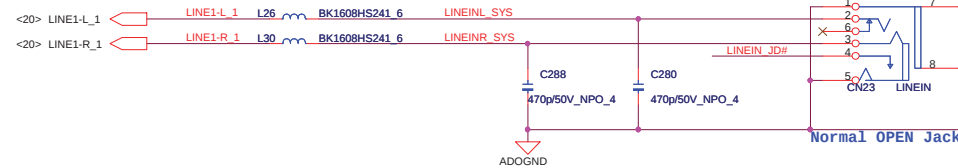
Panasonic AN12948A

CPGND -- ISOLATED GND
Modify CPGND to CPGND_1~4

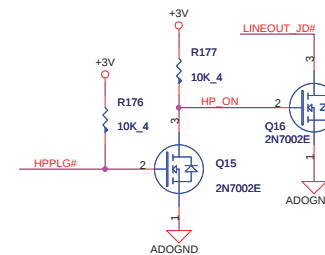
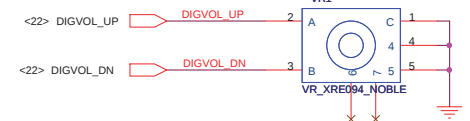
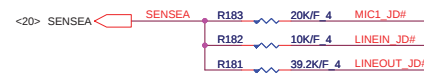
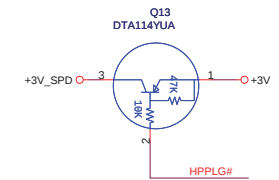
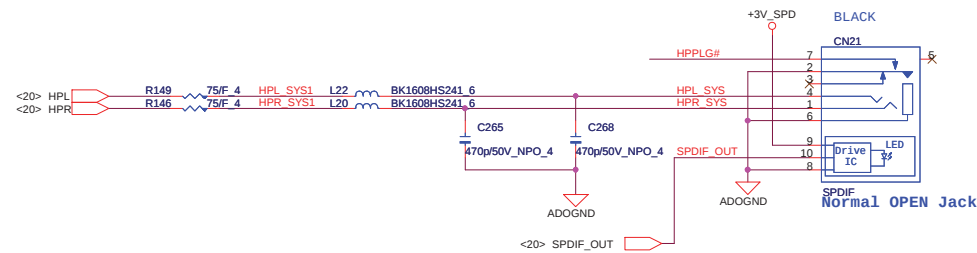
MIC



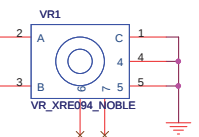
LINE IN



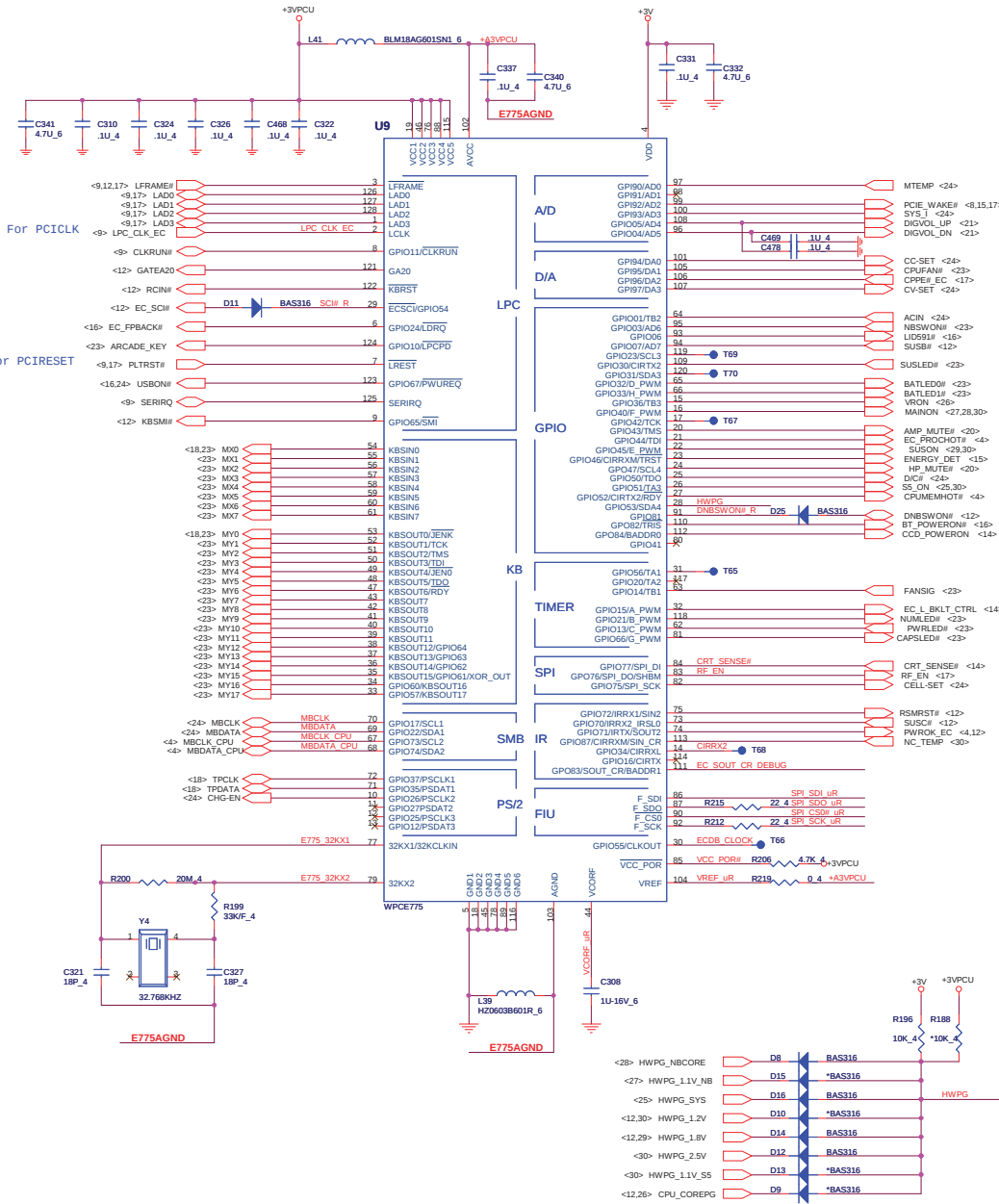
HeadPhone OUT/SPDIF



VR



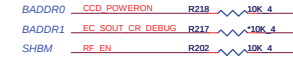
WPCE775C



I/O ADDRESS SETTING

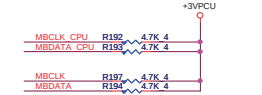
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

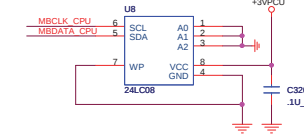


Disabled (*) if using FW device on LPC.
Enabled (*) if using SPI flash for both system BIOS and EC firmware

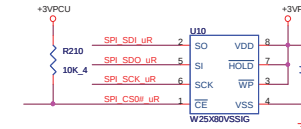
SMBUS PULL-UP



ACER ID



SPI FLASH



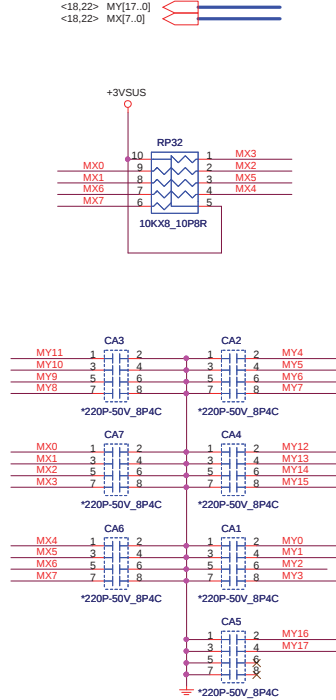
INTERNAL KEYBOARD STRIP SET



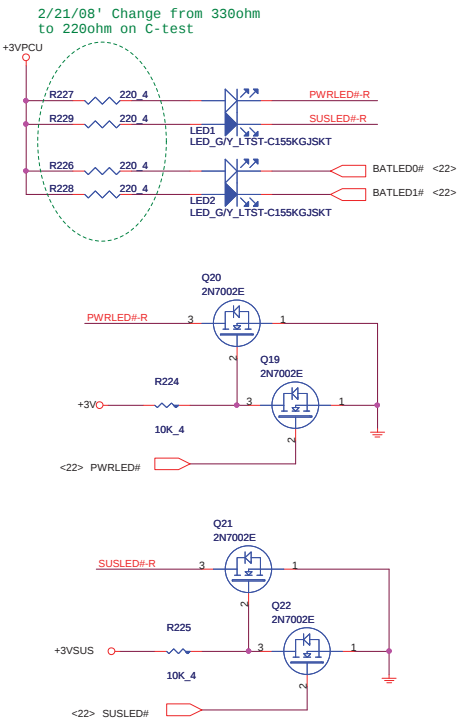
INT K/B

CN4	1	MY0
	2	MY1
	3	MY2
	4	MY3
	5	MY4
	6	MY5
	7	MY6
	8	MY7
	9	MY8
	10	MY9
	11	MY10
	12	MY11
	13	MY12
	14	MY13
	15	MY14
	16	MY15
	17	MY16
	18	MY17
	19	MX7
	20	MX6
	21	MX5
	22	MX4
	23	MX3
	24	MX2
	25	MX1
	26	MX0

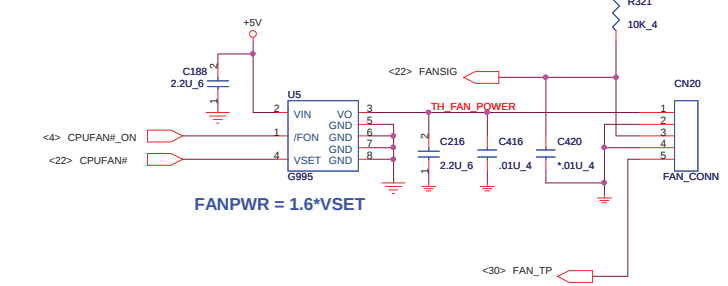
FFC_26P_KB



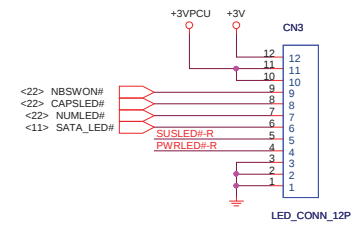
LED



CPU FAN



LED BOARD CONN.



Debug

Delete Debug Port(PCI & IDE)

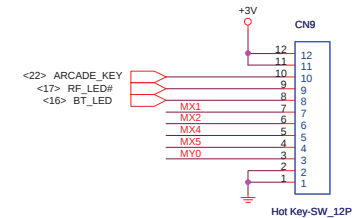
Fingerprint BOARD CONN.

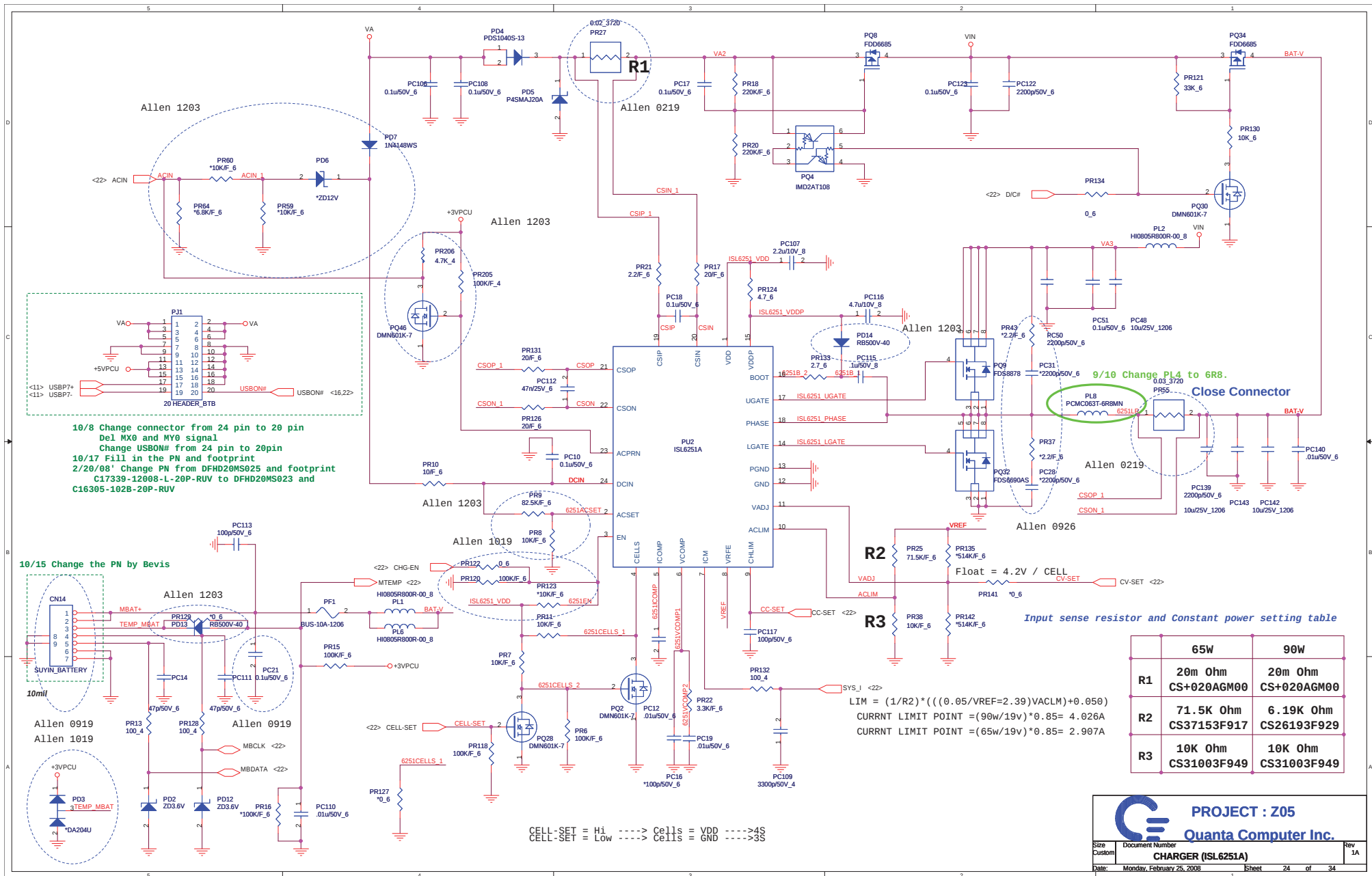


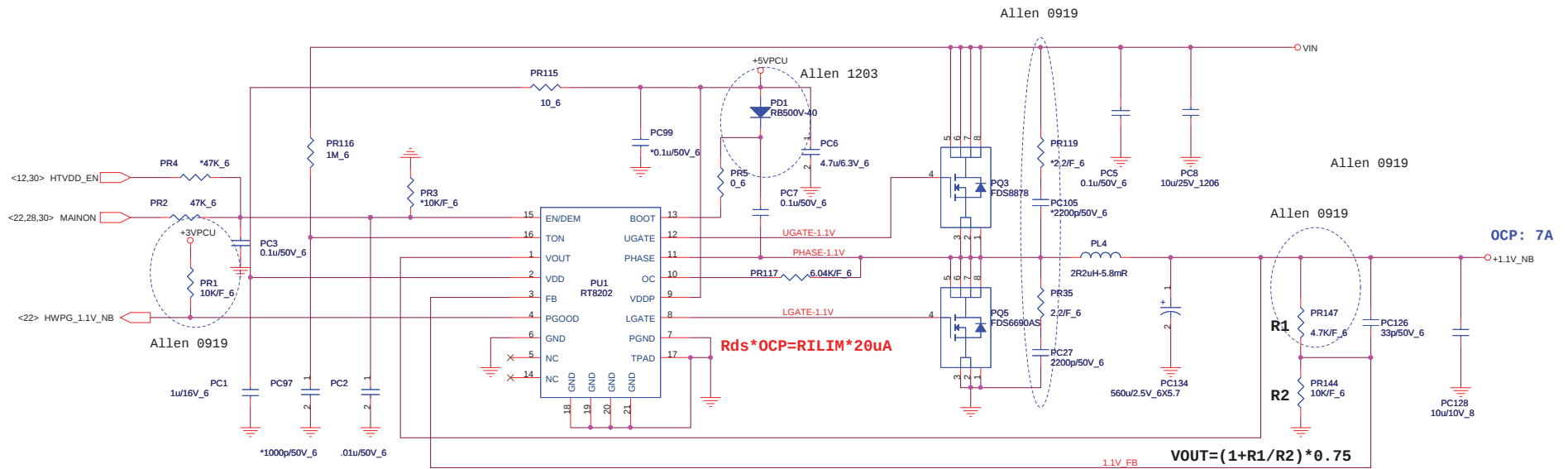
Button BOARD CONN.

BUTTON MATRIX

	MY0
MX1	MAIL
MX2	WWW
MX4	WIRELESS
MX5	BLUETOOTH

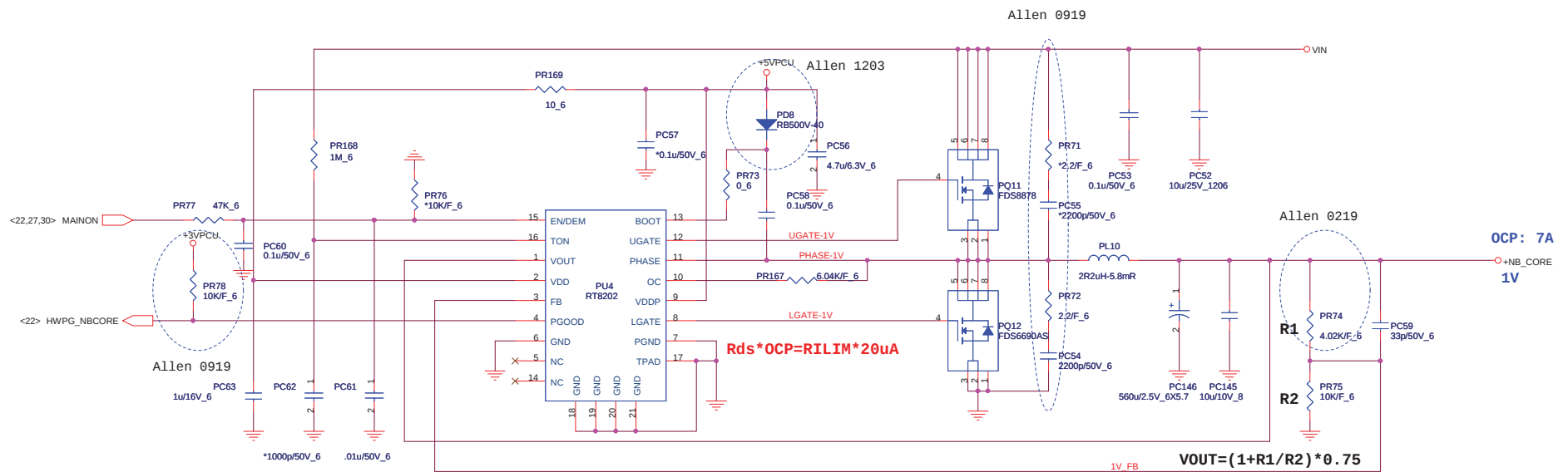






PROJECT : Z05
Quanta Computer Inc.

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	NB_VCC (RT8202)	1A
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$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

FDS6690AS $R_{ds} = 12 \sim 15m\Omega$

OCP = 7 - 0.8A

$$L(ripple\ current) = (19 - 1) * 1 / (2.2u * 272k * 19) \sim 1.58A$$

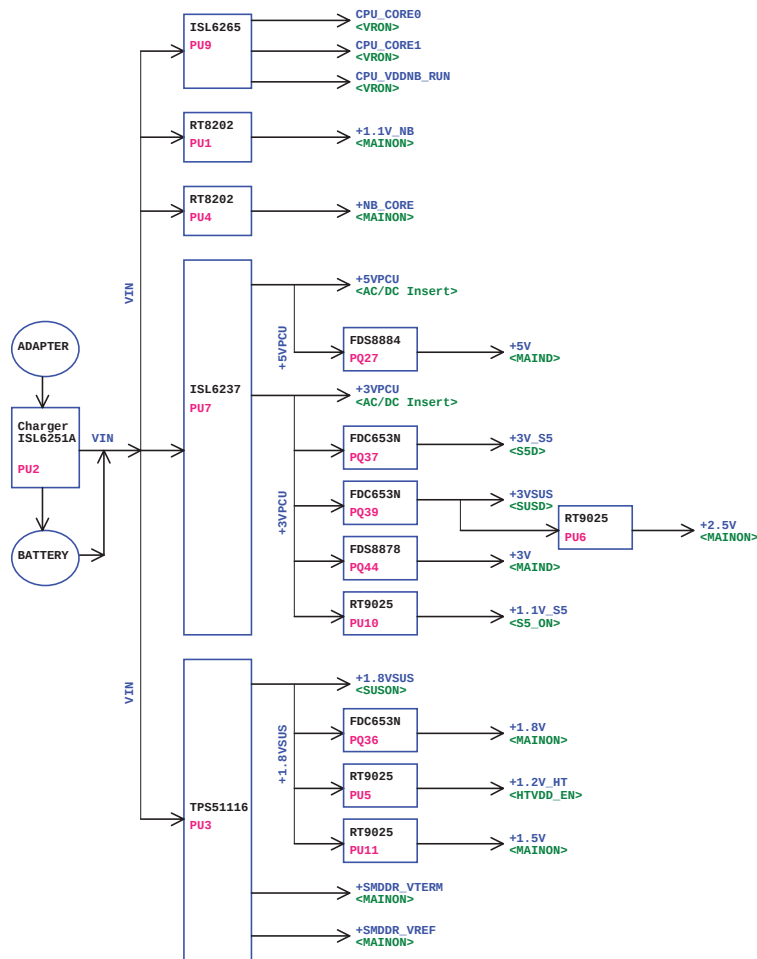
$$12m * 6 = R_{ILIM} * 20\mu A$$

$$R_{ILIM} = 3.6K (2.5 \sim 8K)$$



PROJECT : Z05
Quanta Computer Inc.

Size	Document Number	Rev
	NB_VCC (RT8202)	1A
Date:	Monday, February 25, 2008	Sheet 28 of 34



1. +1.1V_S5MCP77M Power(+1.1V_DUAL)
2. +5VPCUPower IC VCC, USB PORT POWER(S3 control)
3. +5VAudio, FAN, Touch pad, SATA HDD, ODD, CRT
4. +3V_S5MCP77M, New Card, LAN Power
5. +3VPCUKBC WPCE755C,SPI ROM, LED, LID Switch, Fingerprint Module
6. +3VSUSBluetooth, Mini Card, MDC
7. +3VCPU Thermal Sense, MCP77M, System Memory, LCD Panel, PC Camera, Mini card, New Card, Audio, Codec, Card Reader, KBC WPCE775C, LED
8. +2.5VCPU VDDA
9. +3V_LANLAN Power(BCM5764M)
10. +1.2V_LANLAN Power(BCM5764M)
11. +2.5V_LANLAN Power(BCM5787M)
12. +1.5VMini Card, New Card
13. +1.8VSUSCPU VDD I/O, System Memory
14. SMDDR_VTEMCPU Memory Interface , SYSTEM DDR DIMM Memory Termination
15. +1.8VMCP77M LCD Interface
16. +1.1V_NBMCP77M (HT Interface, PCI-E Interface, I/O Power, SATA Interface)
17. +NB_COREMCP77M Core Power
18. +1.2V_HTCPU HT Power
19. CPU_CORE0 CPU Power
20. CPU_CORE1 CPU Power
21. CPU_VDDNB_RUNCPU NB Power
- 22.