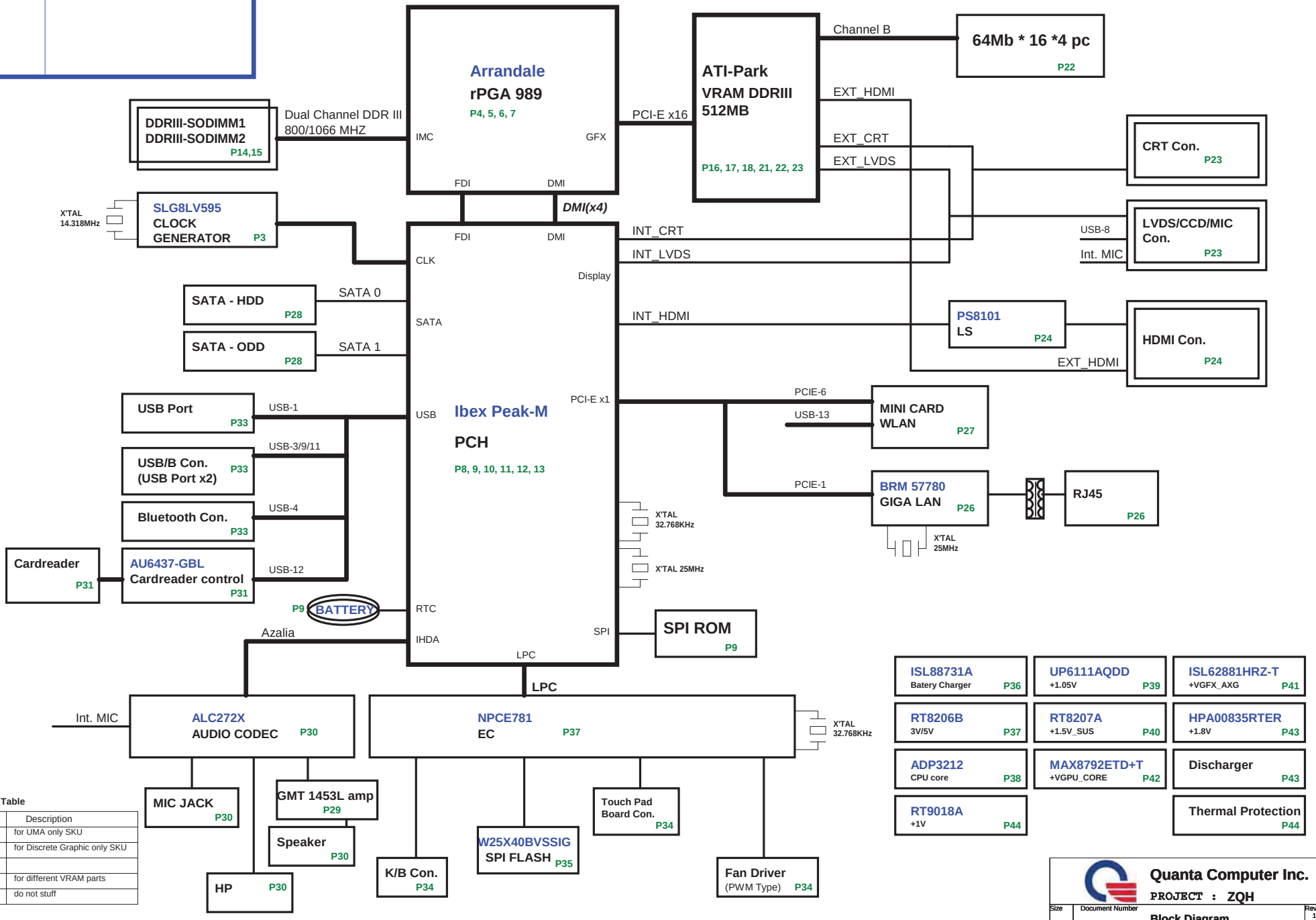
VER : 1A

BOM P/N	Description

ZQH SYSTEM BLOCK DIAGRAM



BOM Option Table

Reference	Description
IV@	for UMA only SKU
EV@	for Discrete Graphic only SKU
VRAM@	for different VRAM parts
*	do not stuff

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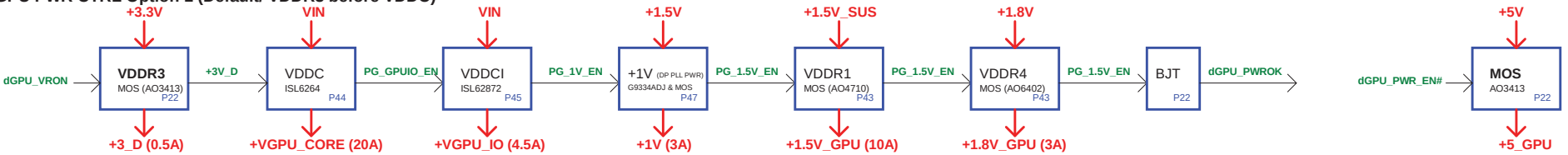
PROJECT : ZQH

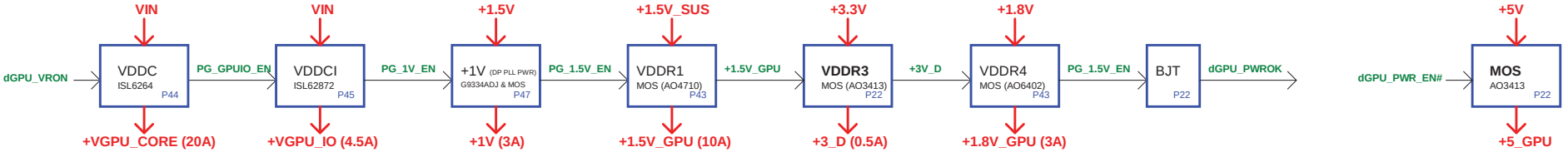
Size	Document Number	Rev
	Block Diagram	1A

Date: Monday, March 14, 2011 Sheet 1 of 35

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



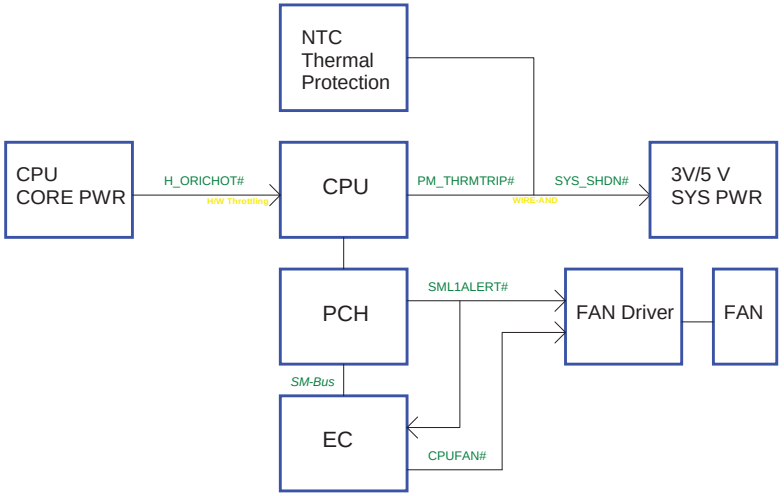
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



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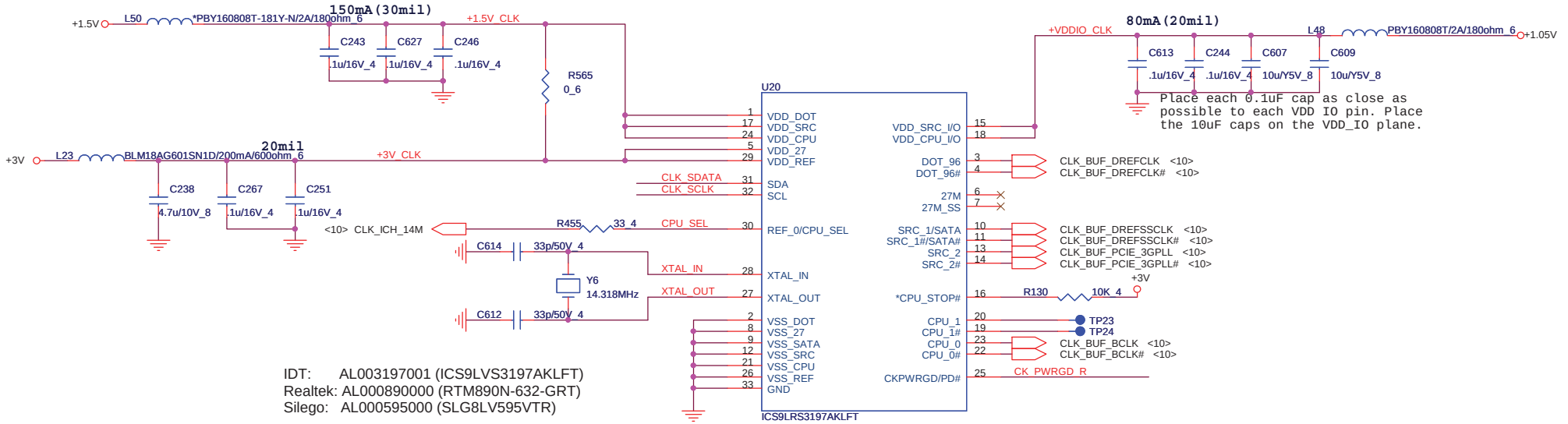
PROJECT : ZQH

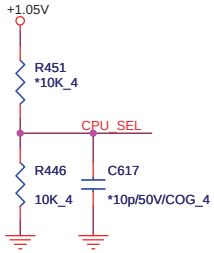
Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

Date: Monday, March 14, 2011 Sheet 2 of 45



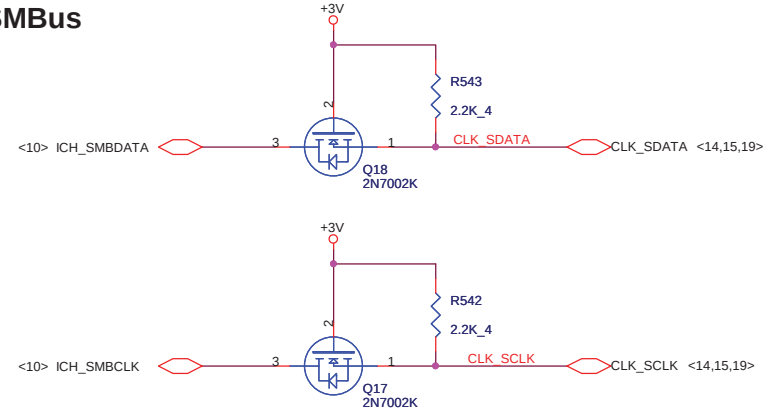
IDT: AL003197001 (ICS9LVS3197AKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

CPU_CLK select

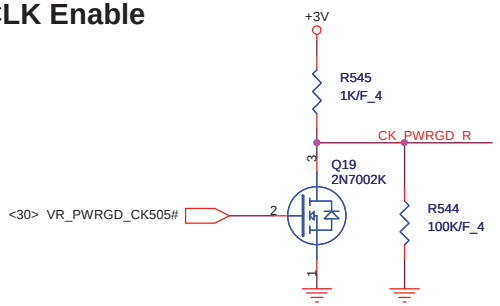


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



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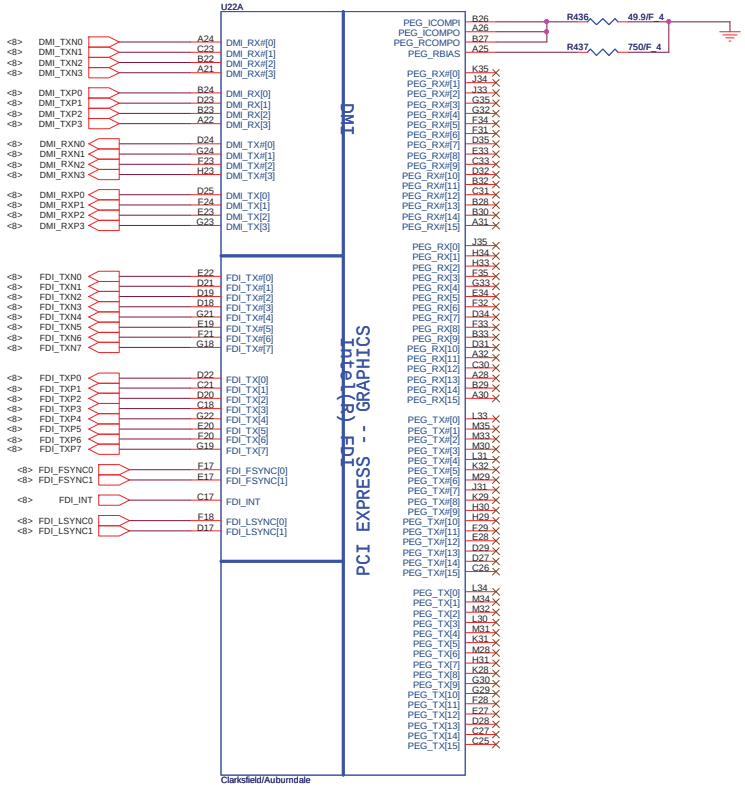
PROJECT : ZQH

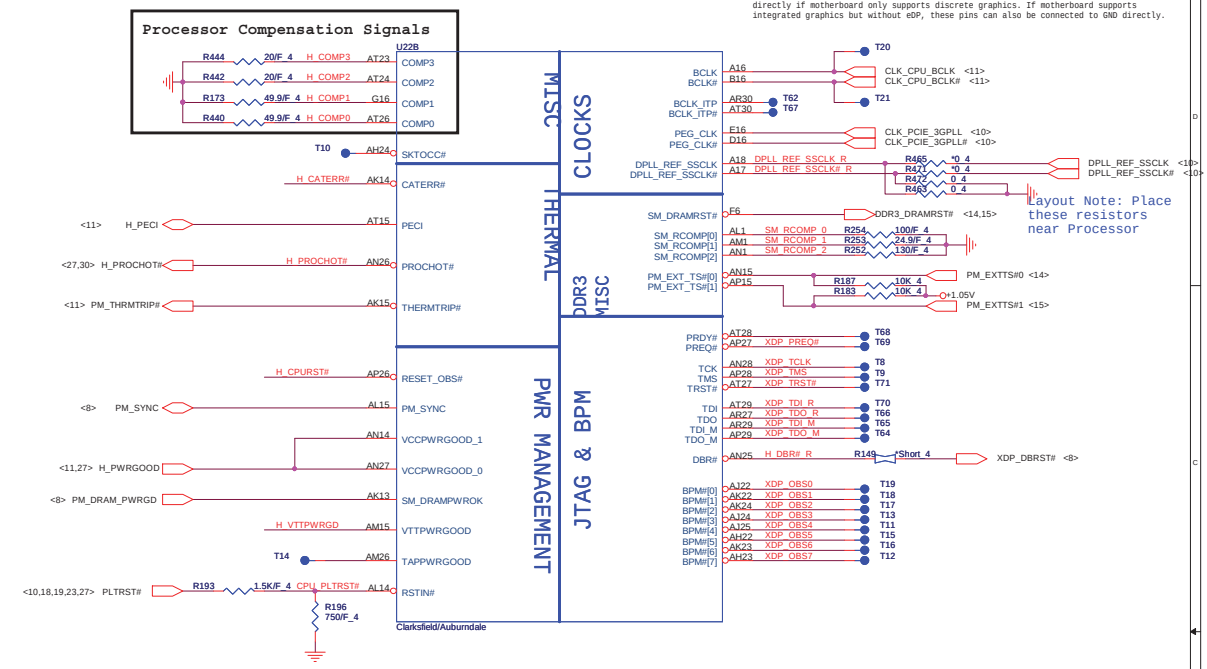
Size	Document Number	Rev
	Clock Generator	1A
Date: Monday, March 14, 2011	Sheet 3 of 45	

AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

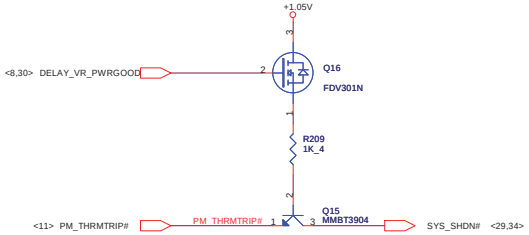


AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

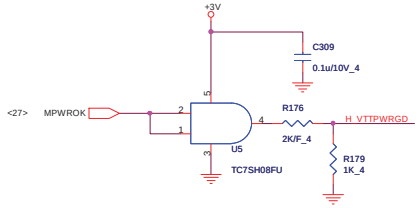
DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on Arrandale directly if motherboard only supports discrete graphics. If motherboard supports integrated graphics but without eDP, these pins can also be connected to GND directly.



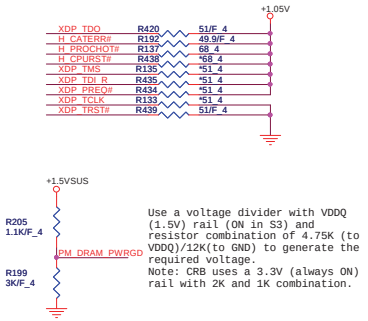
Thermaltrip protect



VTT PWR_Good

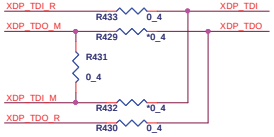


Processor pull-up



Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.

JTAG MAPPING



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

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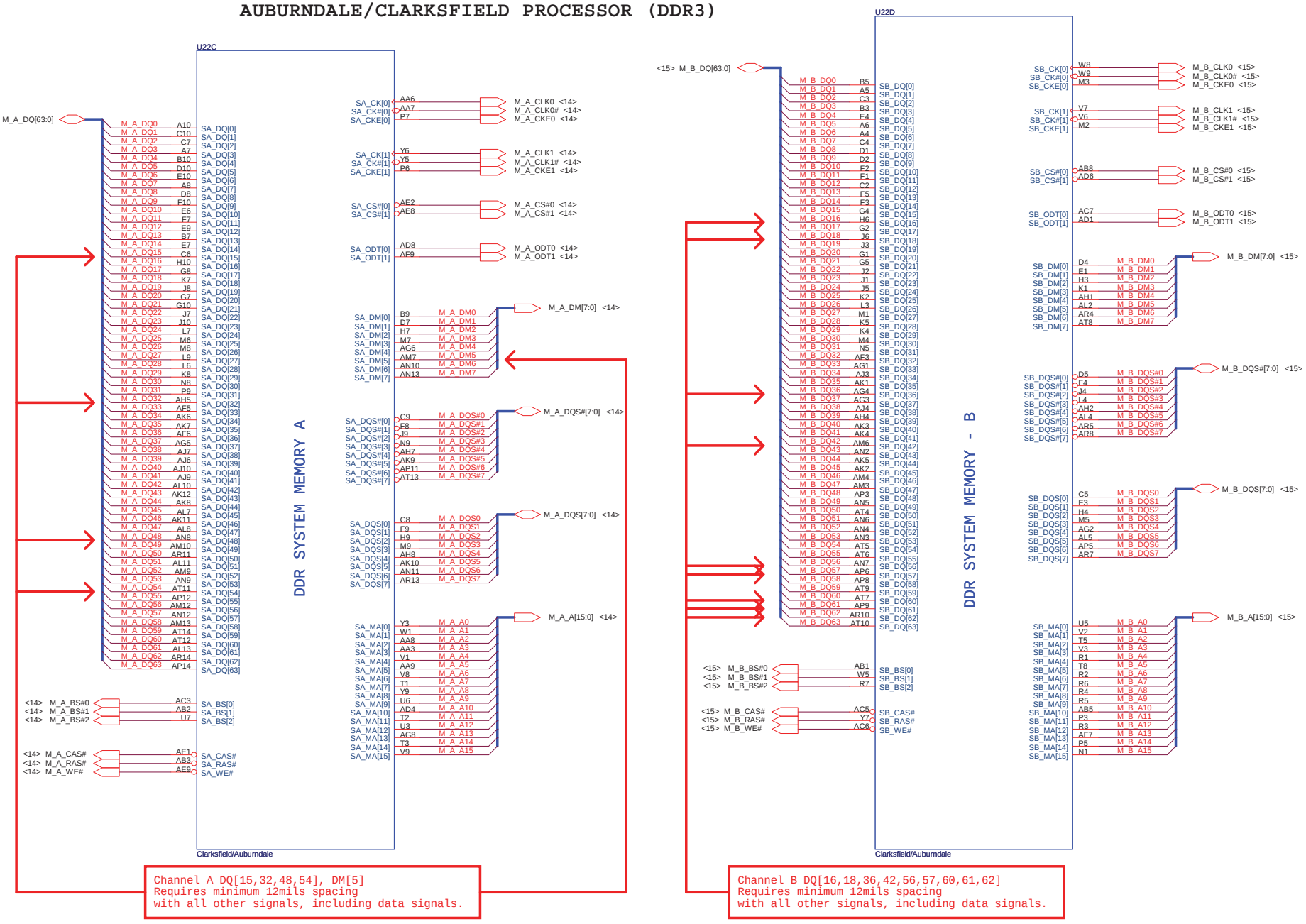
PROJECT : ZQH

Size	Document Number	Rev
	AUBURNDA 1/4	1A

Date: Monday, March 14, 2011 Sheet 4 of 45

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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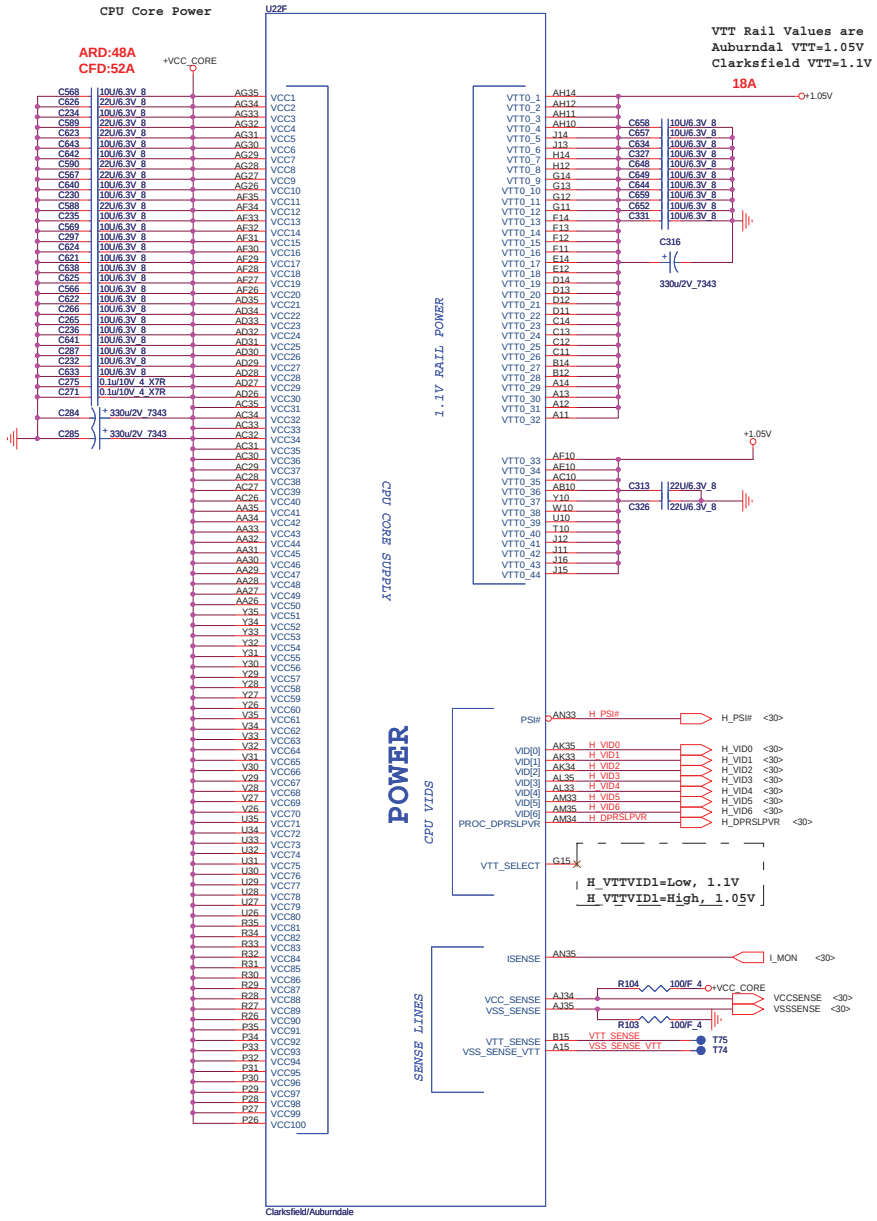
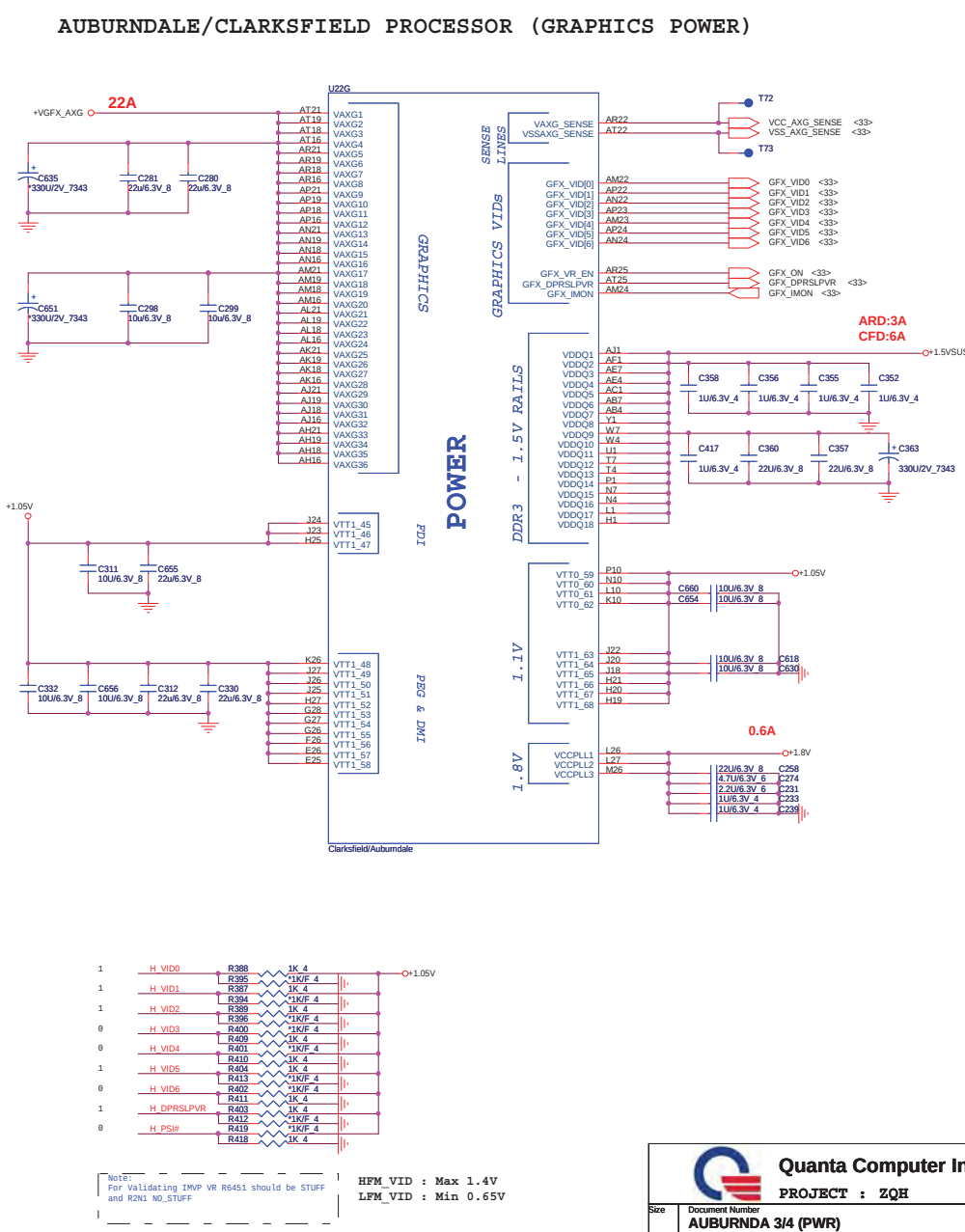
PROJECT : ZQH			
Size	Document Number		Rev
	AUBURNDA 2/4		1A
Date: Monday, March 14, 2011		Sheet 5 of 45	





AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

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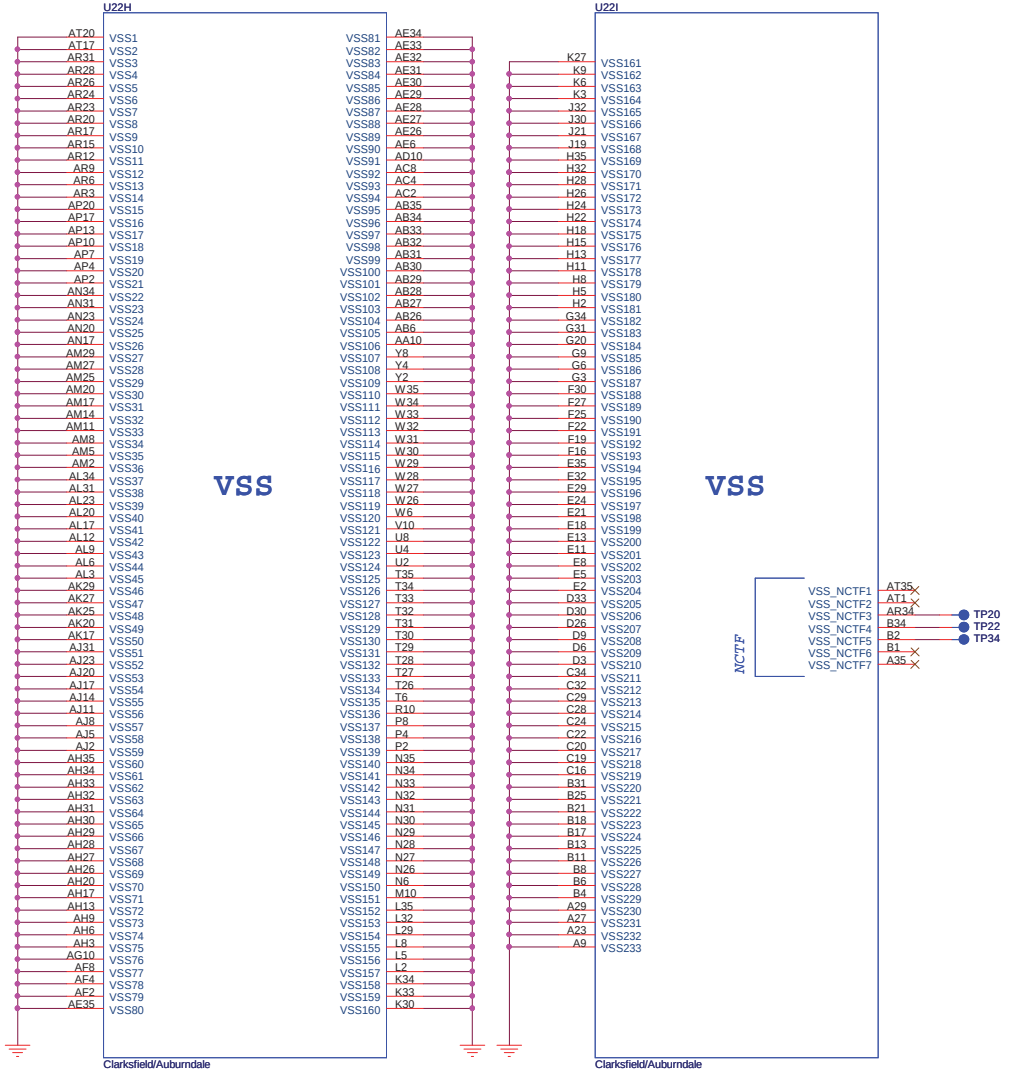
PROJECT : ZQH

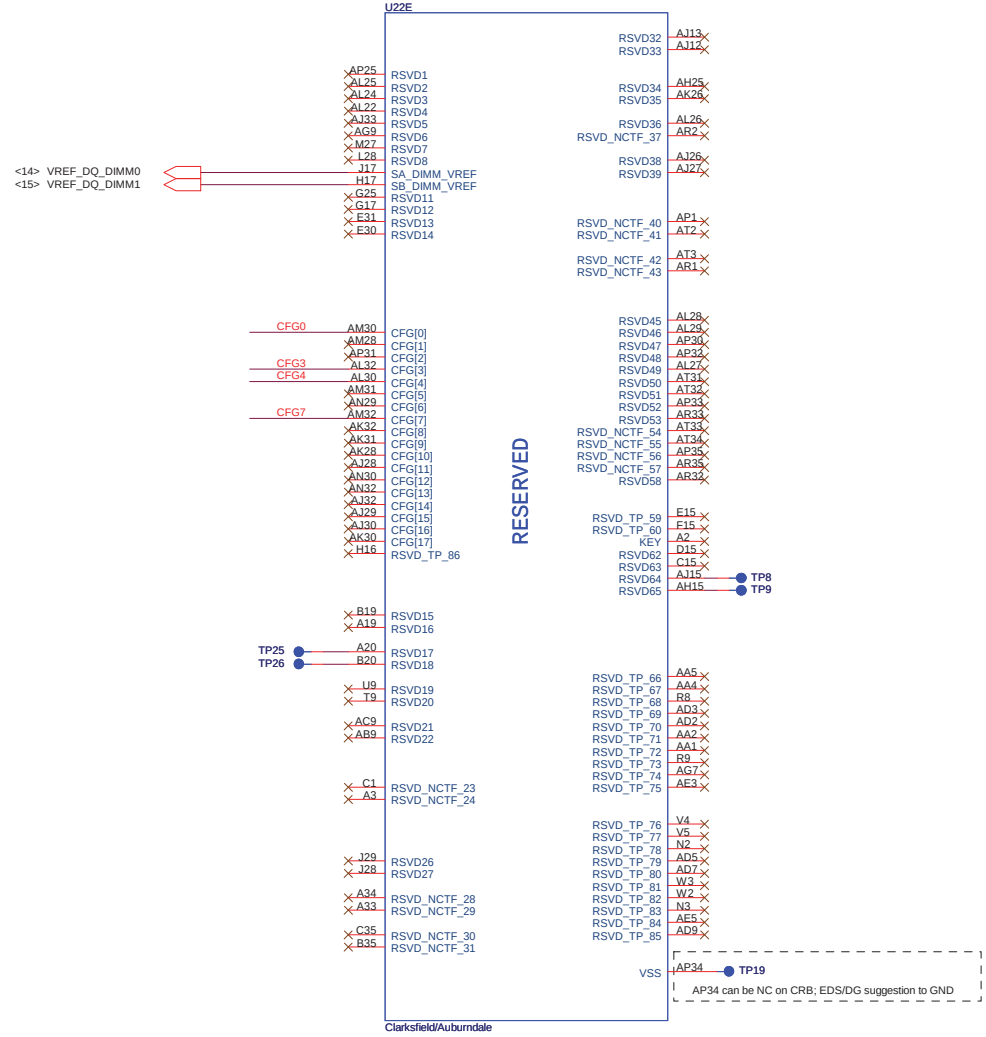
Size	Document Number	Rev
	AUBURNDA 3/4 (PWR)	1A

Date: Monday, March 14, 2011 Sheet 6 of 45

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R128 *3.01K_NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R125 3.01K/F_4
CFG4 (Embended Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R127 *3.01K
T h b e d B P				CFG7 R126 *3.01K/F_4

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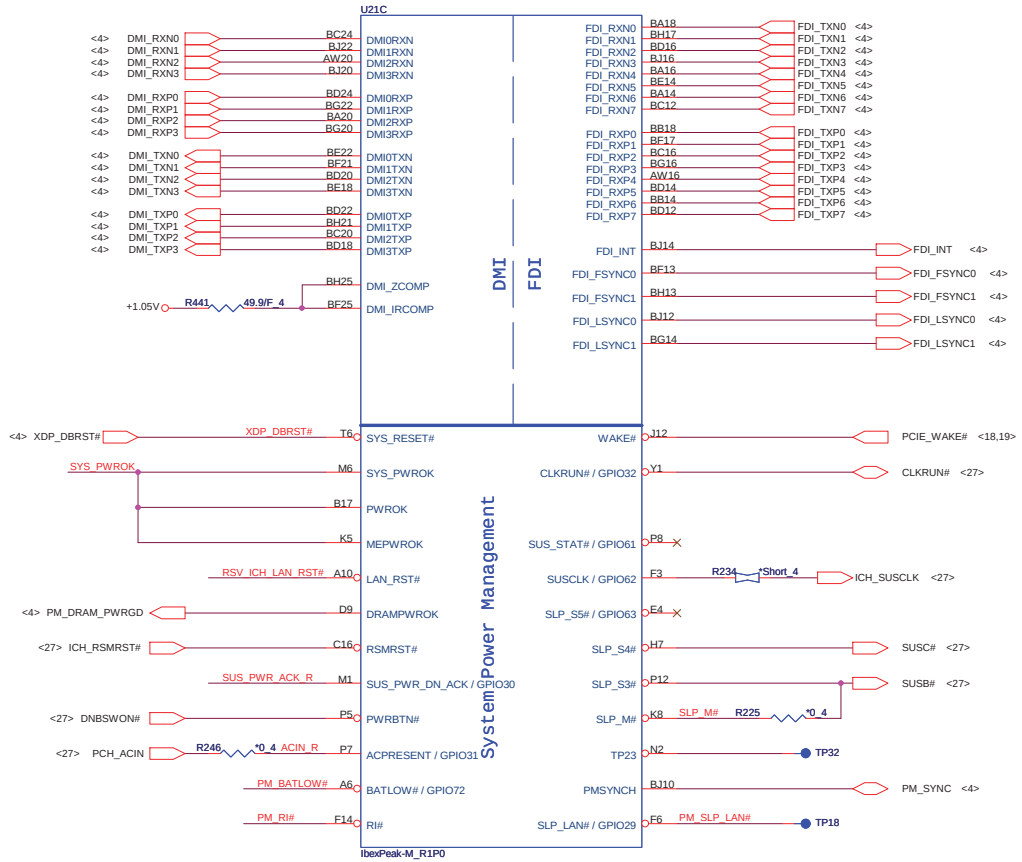
PROJECT : ZQH

Size	Document Number	Rev
	AUBURNDA 4/4	1A

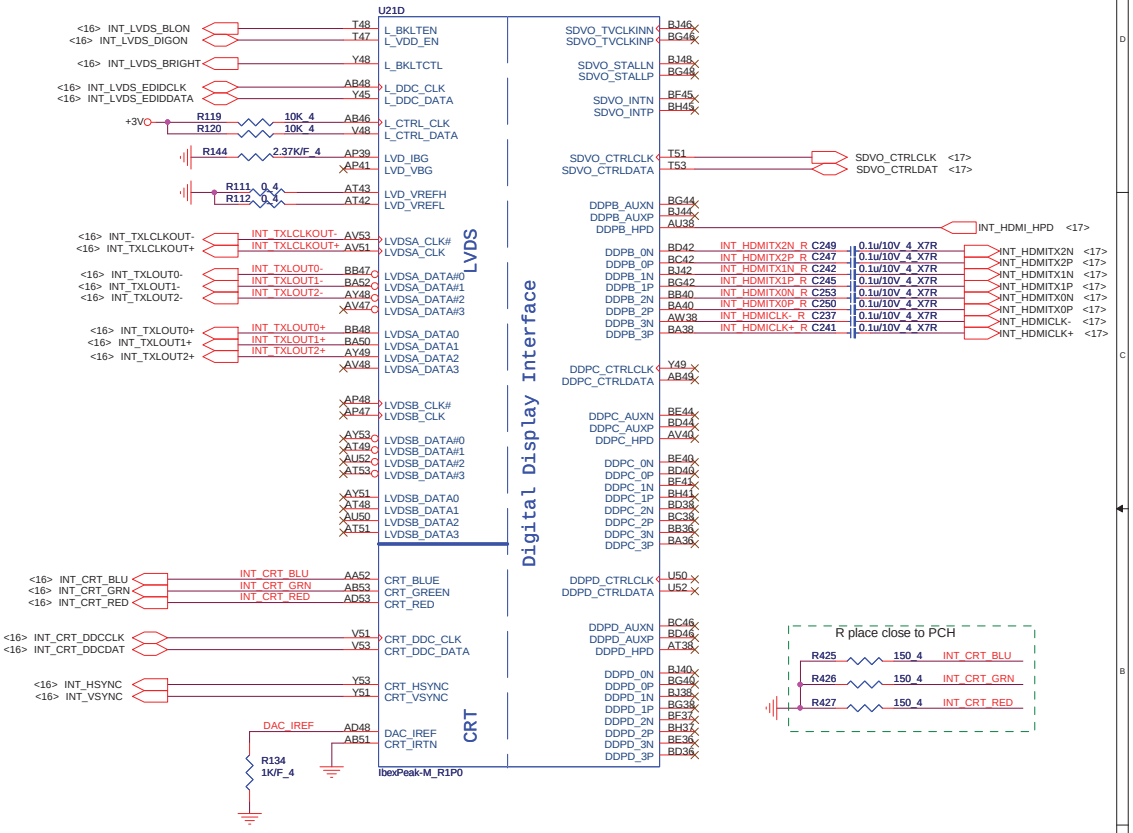
Date: Monday, March 14, 2011 Sheet 7 of 45

IBEX PEAK-M (DMI,FDI,GPIO)

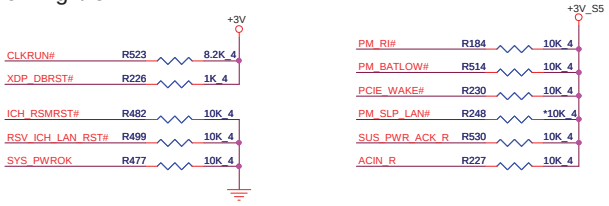


AC-coupling CAP place close to PCH

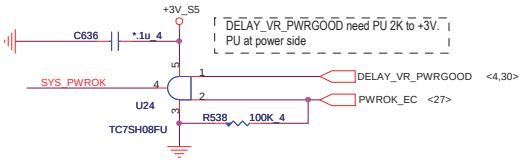
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low

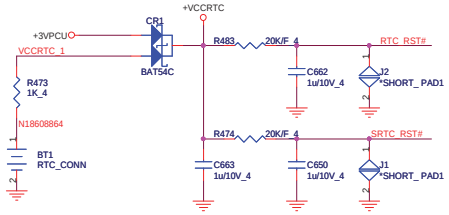


System PWR_OK

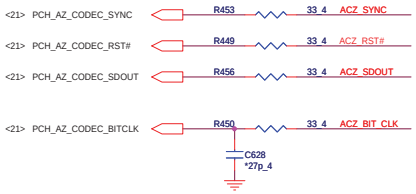


Quanta Computer Inc.		
PROJECT : ZQH		
Size	Document Number: IBEX PEAK-M 1/6	Rev: 1A
Date: Monday, March 14, 2011	Sheet 8 of 45	

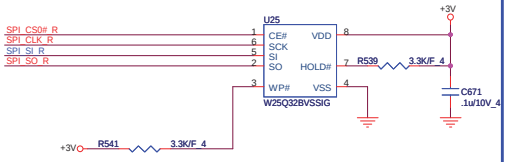
RTC Circuitry



HDA Bus

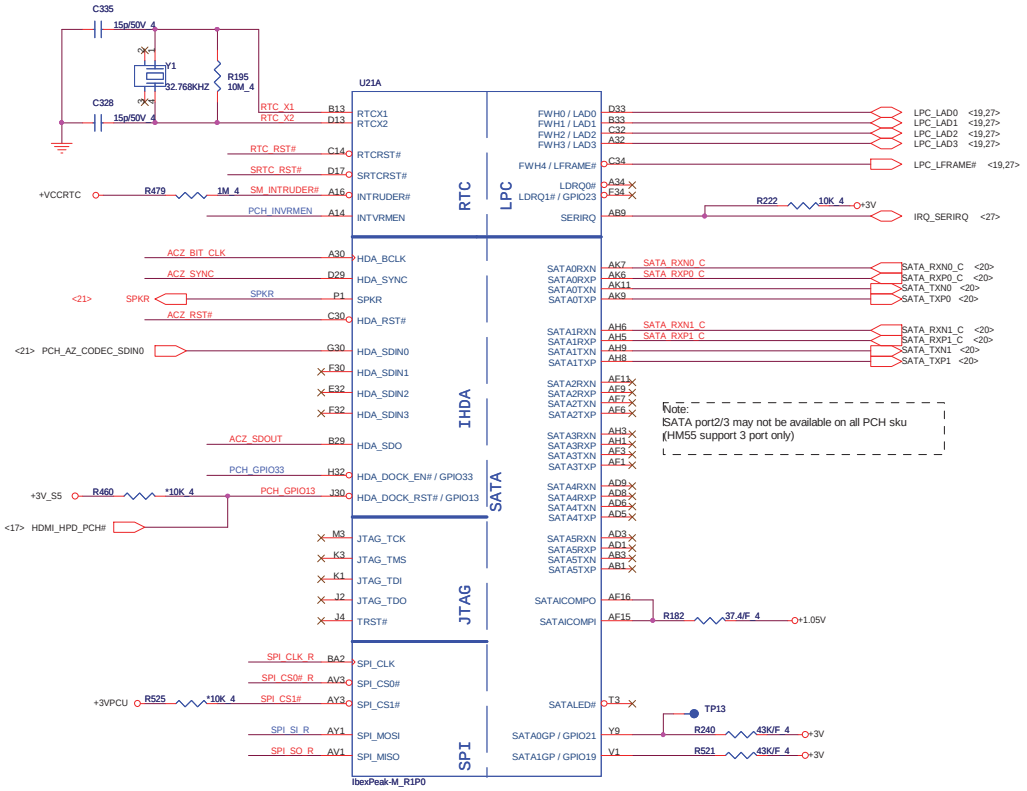


PCH SPI



HDA_SYNC (PCH strap pin)

Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V



PCH Strap Pin Configuration Table-1

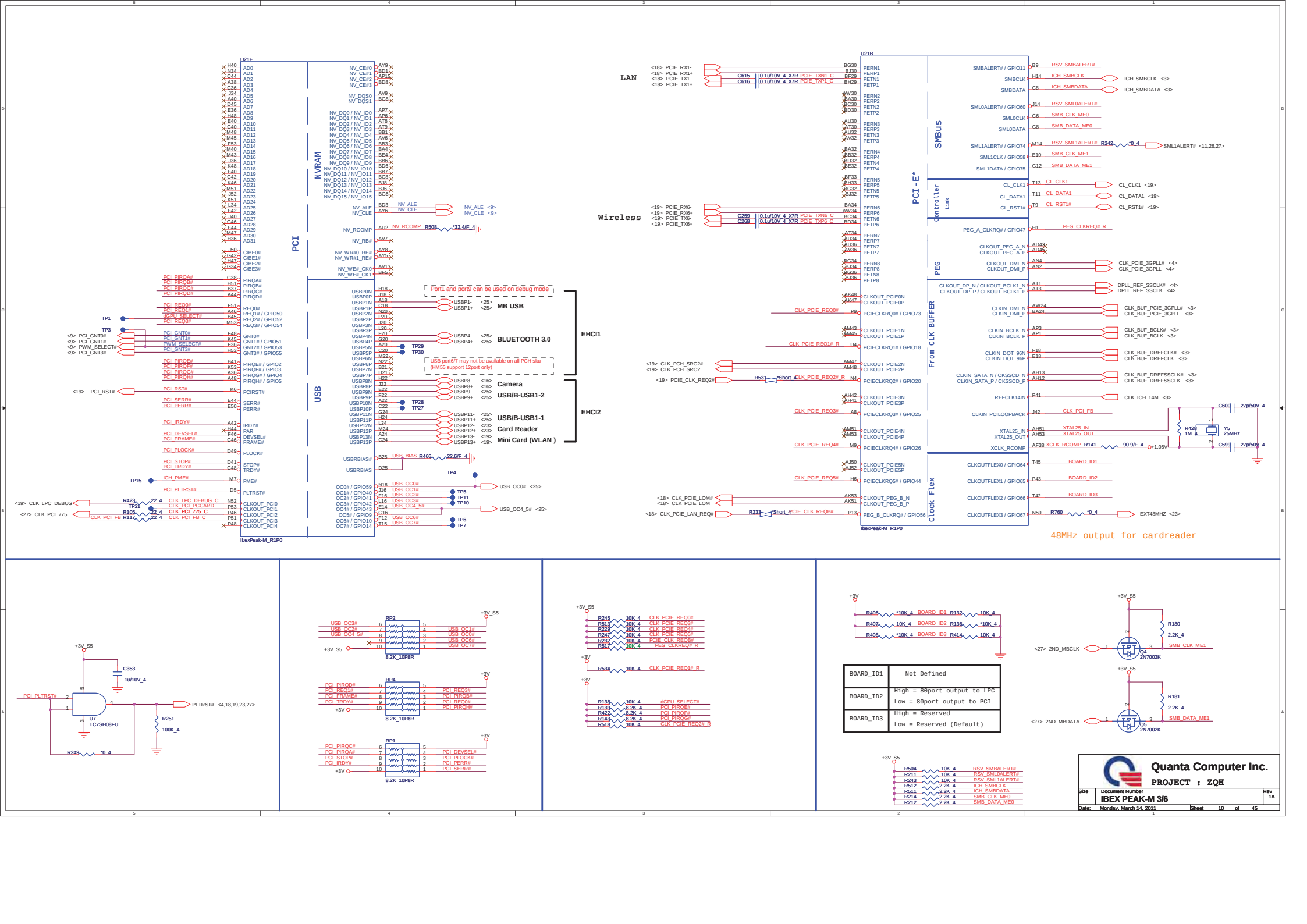
INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R489 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R540 *1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R532 *1K/F_4 SPKR
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R164 *1K/F_4 R145 *10K_4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	R129 1K_4 R122 1K_4 R123 *1K_4 R131 *1K_4 +3V <10> PCI_GNT0# <10> PCI_GNT1#
GNT2#/ GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	<10> PWM_SELECT# R158 *1K/F_4
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	<10> PCI_GNT3# R421 *10K/F_4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	<10> NV_ALE R202 *1K/F_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	<10> NV_CLE R206 *1K/F_4 +1.8V

GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	<11> RSV_GPIO8 R204 10K_4 +3V_S5 R203 *1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	<11> CR_WAKE# R244 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	<11> PCH_GPIO27 R221 *10K_4

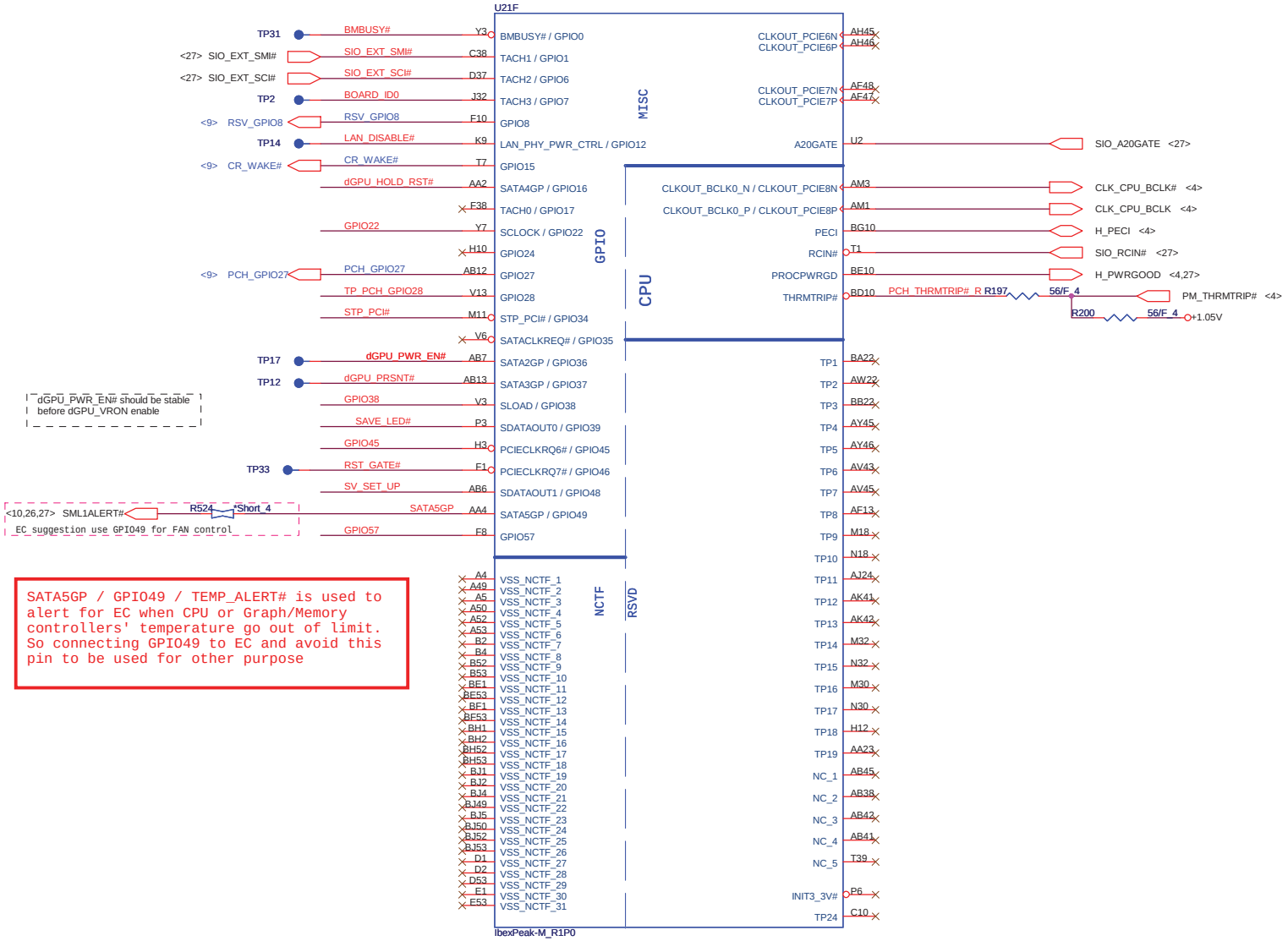
Quanta Computer Inc.
PROJECT : ZQH

Size	Document Number	Rev
	IBEX PEAK-M 2/6	1A

Date: Monday, March 14, 2011 Sheet 9 of 45


U21E
PCI
NVRAM
USB
IbexPeak-M_R1P0
Port1 and port9 can be used on debug mode
EHCI1
MB USB
BLUETOOTH 3.0
USB port6/7 may not be available on all PCH sku
(HM55 support 12port only)
EHCI2
Camera
USB/B-USB1-2
USB/B-USB1-1
Card Reader
Mini Card (WLAN)
U21B
PCI-E*
SMBUS
Controller
Link
PEG
From CLK BUFFER
Clock Flex
LAN
Wireless
48MHz output for cardreader
U7
TC7SH08FU
BOARD_ID1 Not Defined
BOARD_ID2 High = 80port output to LPC
Low = 80port output to PCI
BOARD_ID3 High = Reserved
Low = Reserved (Default)
Quanta Computer Inc.
PROJECT : ZQH
IBEX PEAK-M 3/6
Size
Document Number
Rev 1A
Date: Monday, March 14, 2011
Sheet 10 of 45

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

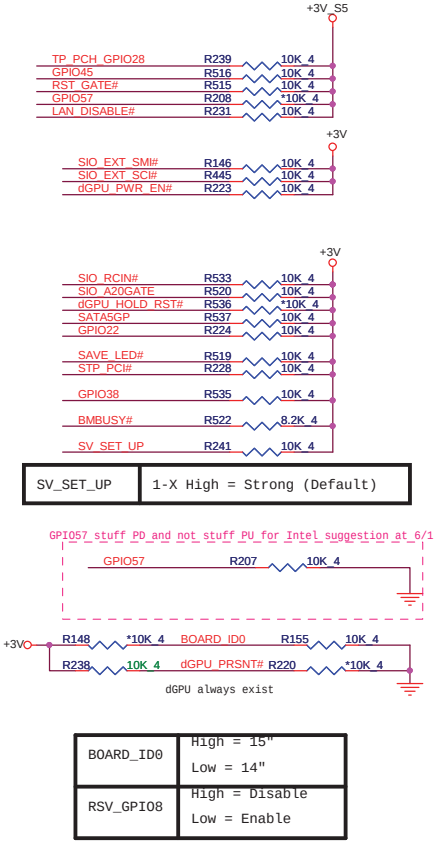


dGPU_PWR_EN# should be stable before dGPU_VRON enable

SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU RST#

GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)

GPIO57 stuff PD and not stuff PU for Intel suggestion at 6/1

BOARD_ID0	High = 15" Low = 14"
RSV_GPIO8	High = Disable Low = Enable

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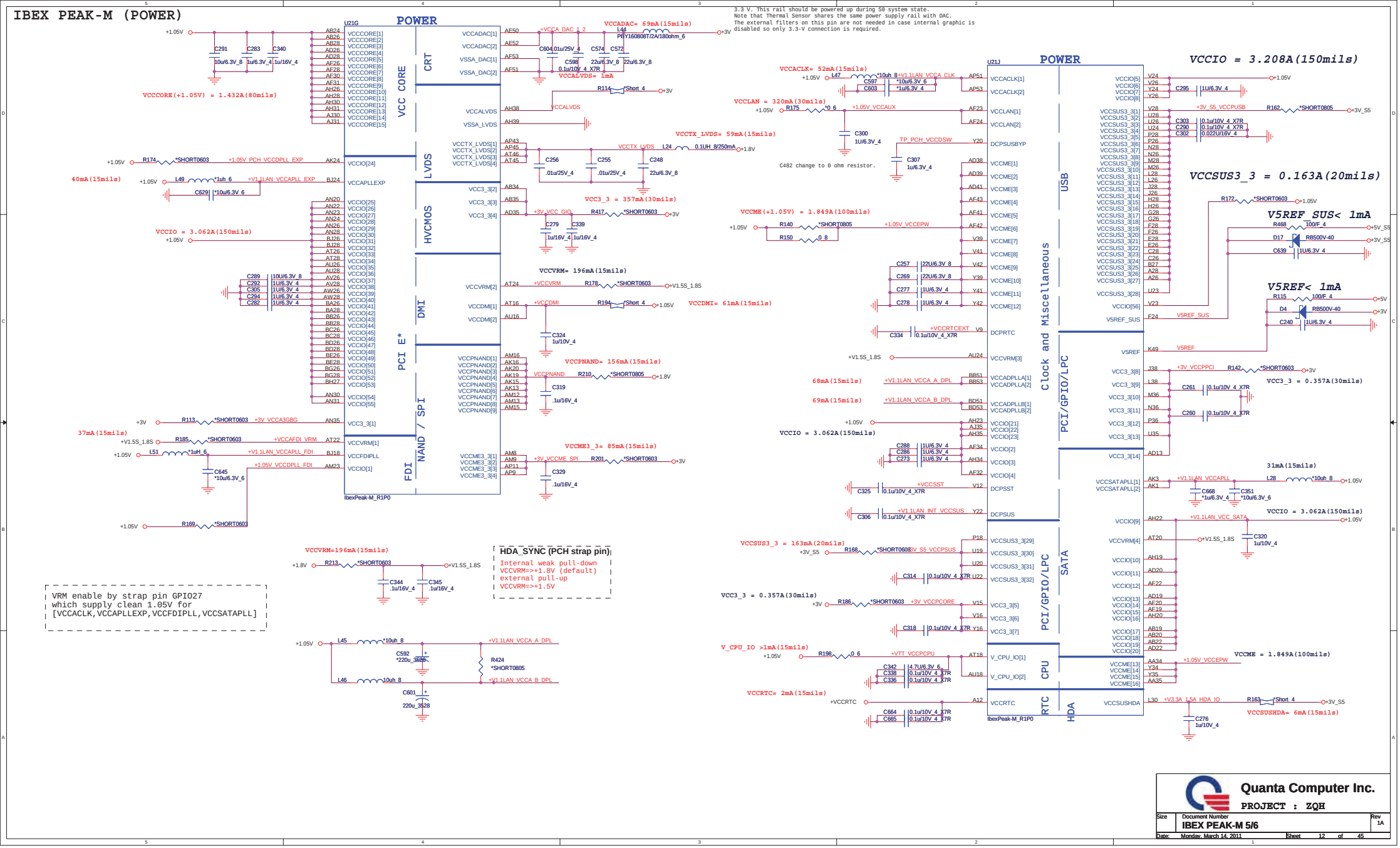
PROJECT : ZQH

Size	Document Number	Rev
	IBEX PEAK-M 4/6	1A

Date: Monday, March 14, 2011 Sheet 11 of 45

IBEX PEAK-M (POWER)

3.3 V. This rail should be powered up during S0 system state.
Note that Thermal Sensor shares the same power supply rail with DAC.
The external filters on this pin are not needed in case internal graphic is disabled so only 3.3-V connection is required.



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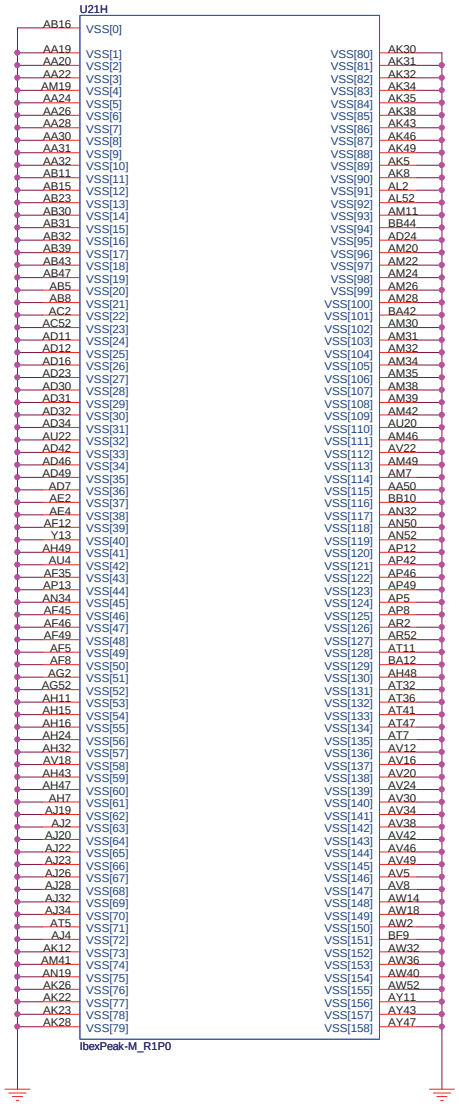
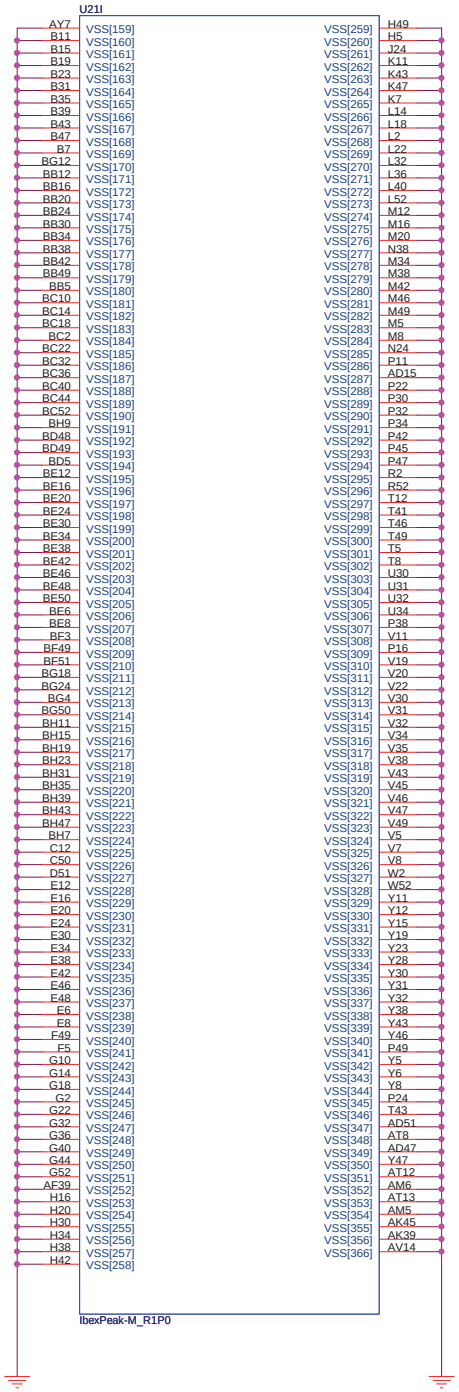
PROJECT : ZQH			
Size	Document Number		Rev
	IBEX PEAK-M 5/6		1A
Date: Monday, March 14, 2011	Sheet 12 of 45		

IBEX PEAK-M (GND)





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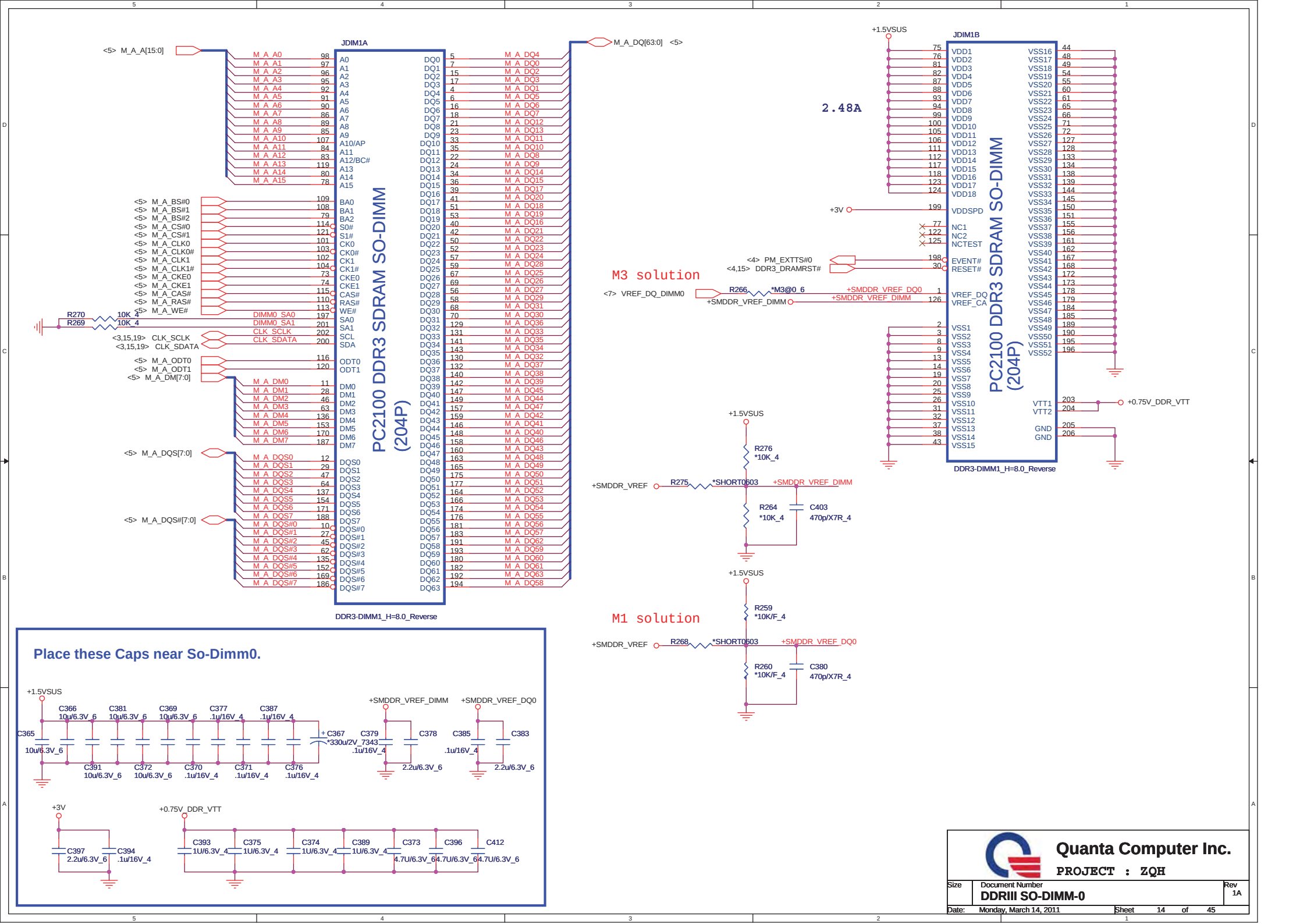
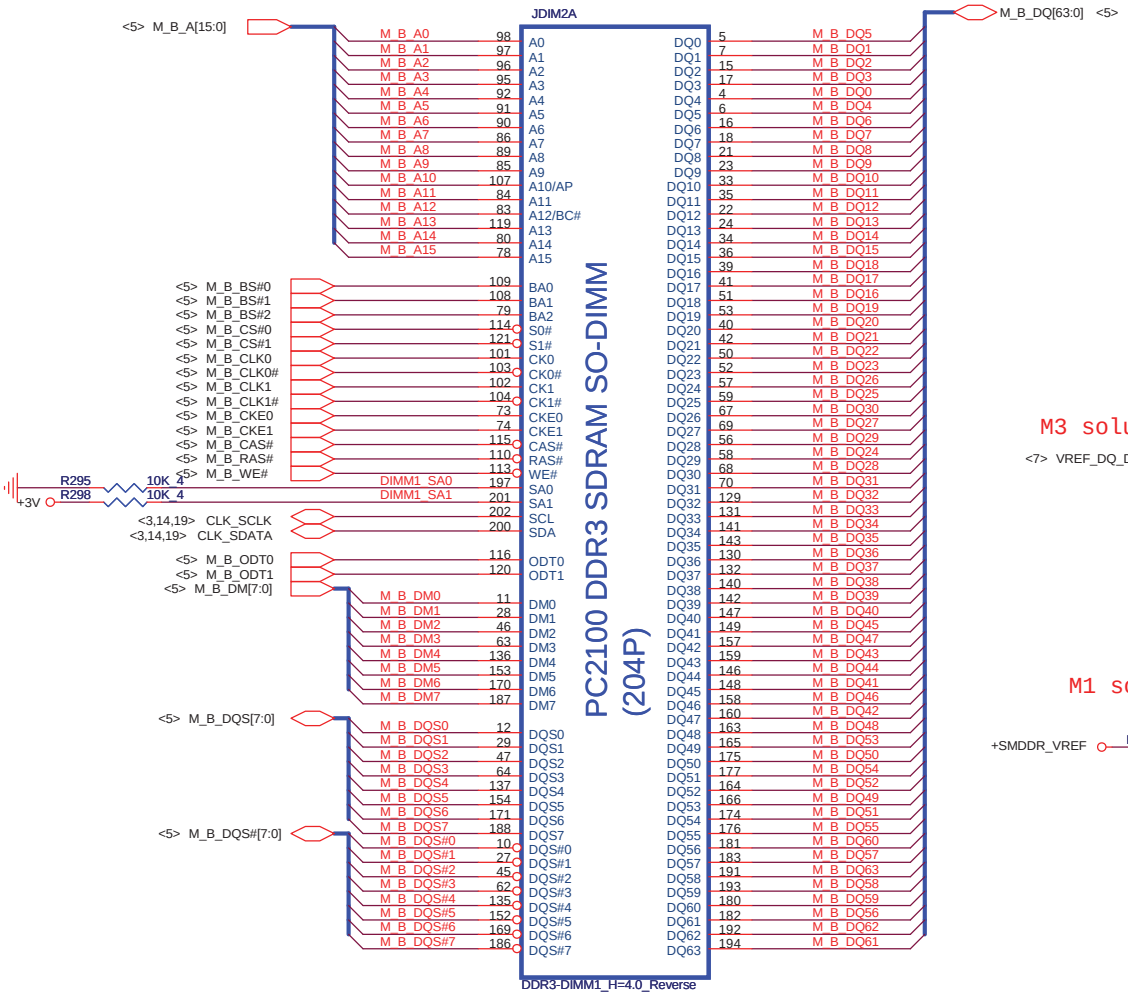
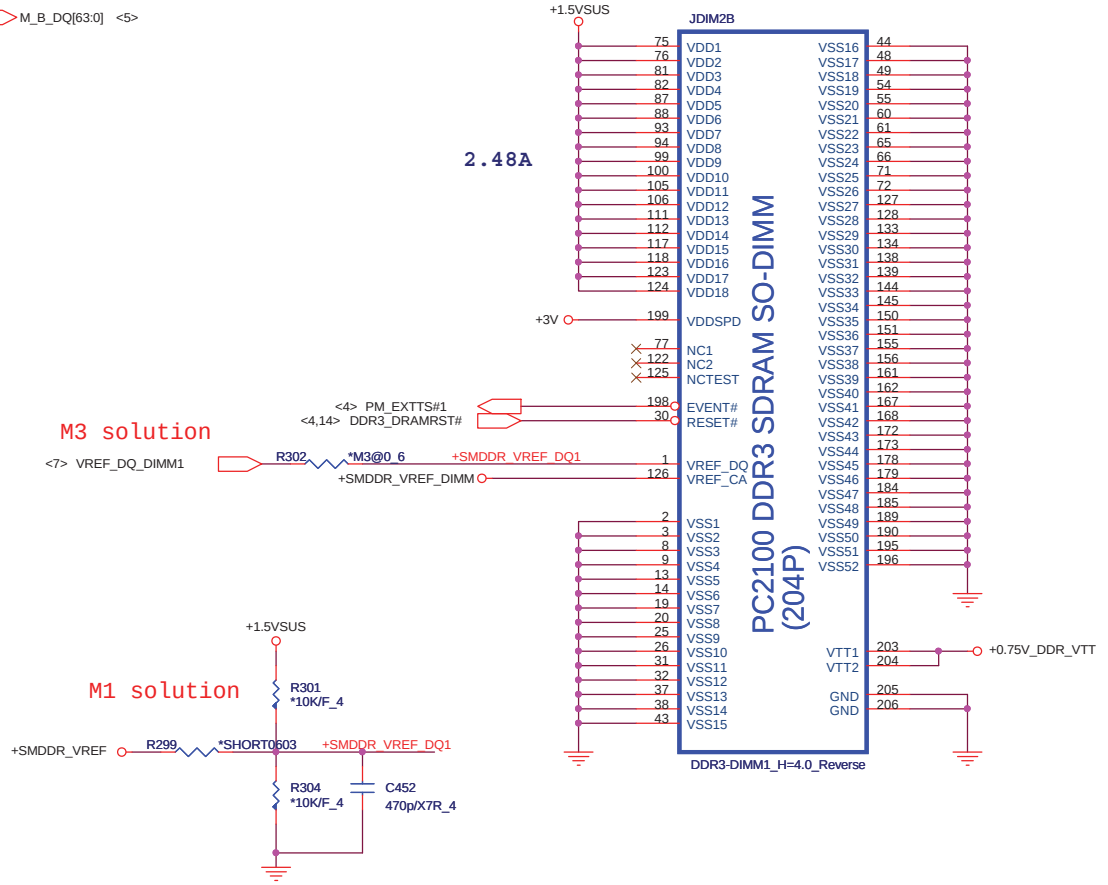
PROJECT : ZQH

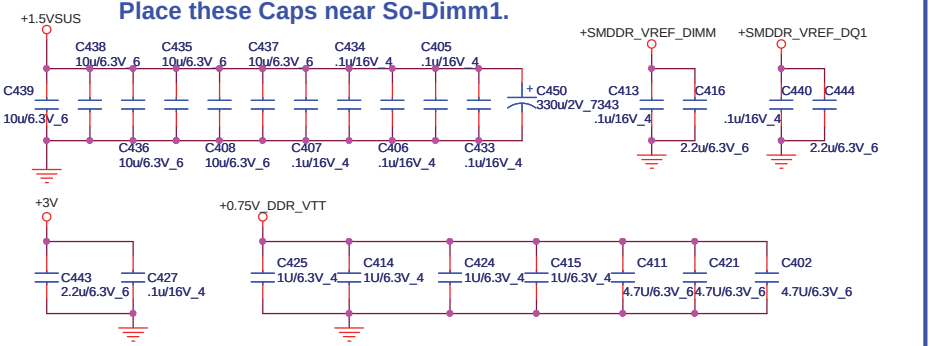
Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A

Date: Monday, March 14, 2011 Sheet 13 of 45


JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=8.0_Reverse
<5> M_A_A[15:0]
M_A_DQ[63:0] <5>
<5> M_A_BS#0
<5> M_A_BS#1
<5> M_A_BS#2
<5> M_A_CS#0
<5> M_A_CS#1
<5> M_A_CLK0
<5> M_A_CLK0#
<5> M_A_CLK1
<5> M_A_CLK1#
<5> M_A_CKE0
<5> M_A_CKE1
<5> M_A_CAS#
<5> M_A_RAS#
<5> M_A_WE#
R270 10K_4
R269 10K_4
DIMM0_SA0
DIMM0_SA1
<3,15,19> CLK_SCLK
<3,15,19> CLK_SDATA
CLK_SCLK
CLK_SDATA
<5> M_A_ODT0
<5> M_A_ODT1
<5> M_A_DM[7:0]
<5> M_A_DQS[7:0]
<5> M_A_DQS#[7:0]
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=8.0_Reverse
+1.5VSUS
+3V
+0.75V_DDR_VTT
2.48A
<4> PM_EXTTS#0
<4,15> DDR3_DRAMRST#
M3 solution
<7> VREF_DQ_DIMM0
R266 *M3@0_6
+SMDDR_VREF_DIMM
+SMDDR_VREF_DQ0
+SMDDR_VREF_DIMM
M1 solution
+SMDDR_VREF
R275 *SHORT0603
R276 *10K_4
R264 *10K_4
C403 470p/X7R_4
R268 *SHORT0603
R259 *10K/F_4
R260 *10K/F_4
C380 470p/X7R_4
Place these Caps near So-Dimm0.
C366 10u/6.3V_6
C381 10u/6.3V_6
C369 10u/6.3V_6
C377 .1u/16V_4
C387 .1u/16V_4
C365 10u/6.3V_6
C367 *330u/2V_7343
C391 10u/6.3V_6
C372 10u/6.3V_6
C370 .1u/16V_4
C371 .1u/16V_4
C376 .1u/16V_4
C379 .1u/16V_4
C378 2.2u/6.3V_6
C385 .1u/16V_4
C383 2.2u/6.3V_6
C397 2.2u/6.3V_6
C394 .1u/16V_4
C393 1U/6.3V_4
C375 1U/6.3V_4
C374 1U/6.3V_4
C389 1U/6.3V_4
C373 4.7U/6.3V_6
C396 4.7U/6.3V_6
C412 4.7U/6.3V_6
Quanta Computer Inc.
PROJECT : ZQH
Size
Document Number
DDRIII SO-DIMM-0
Rev 1A
Date: Monday, March 14, 2011
Sheet 14 of 45







Quanta Computer Inc.

PROJECT : ZQH

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date: Monday, March 14, 2011	Sheet 15 of 35	

CRT Switch

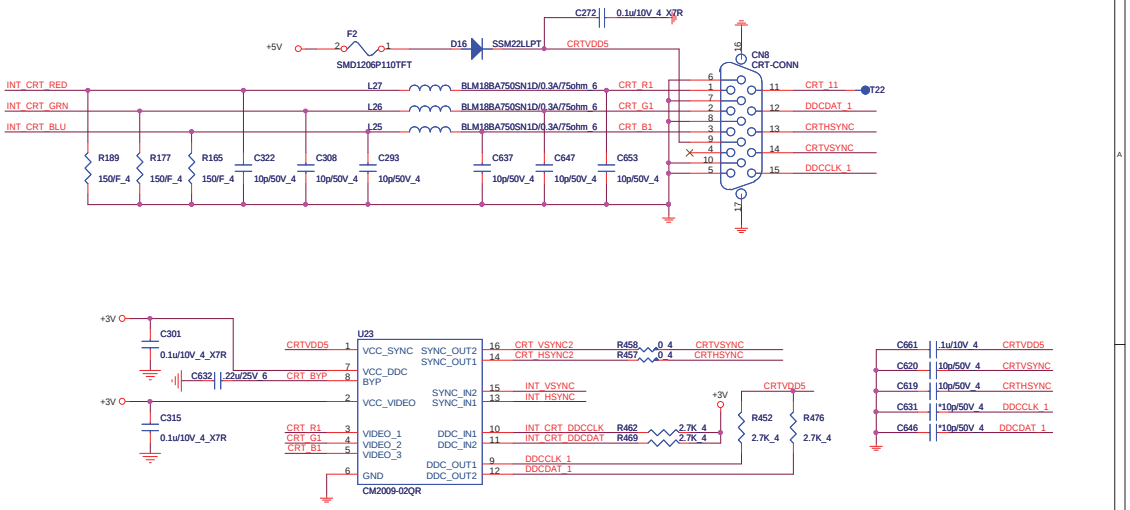
0_ohm Resistor place close to Joint-Point

<8> INT_CRT_RED — INT_CRT_RED
<8> INT_CRT_GRN — INT_CRT_GRN
<8> INT_CRT_BLU — INT_CRT_BLU

<8> INT_VSYNC — INT_VSYNC
<8> INT_HSYNC — INT_HSYNC

<8> INT_CRT_DDCDAT — INT_CRT_DDCDAT
<8> INT_CRT_DDCCLK — INT_CRT_DDCCLK

CRT



LVDS

0_ohm Resistor place close to Joint-Point

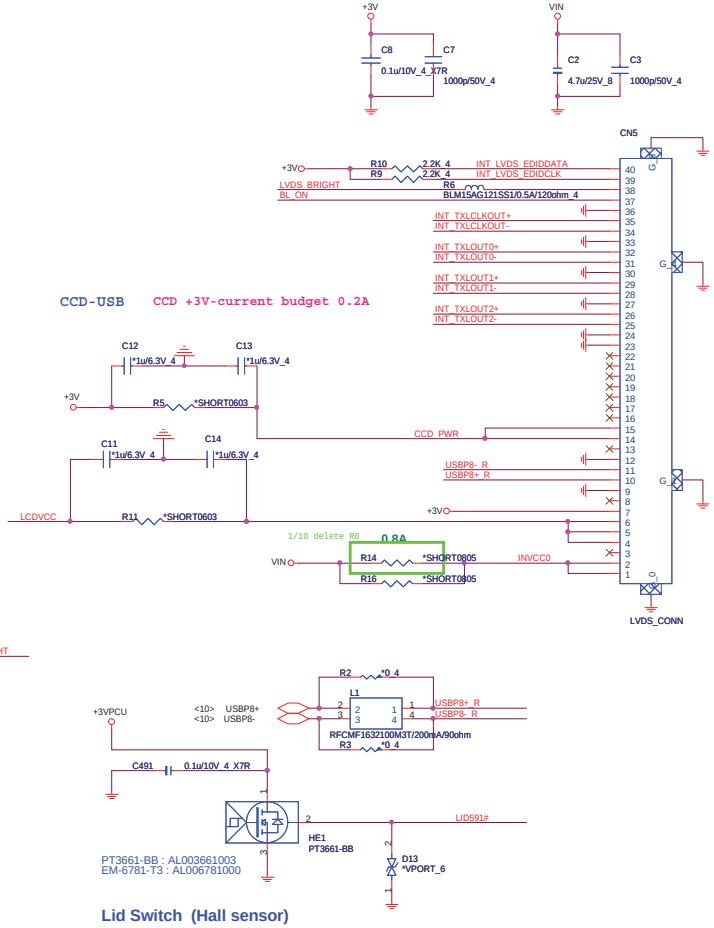
<8> INT_LVDS_EDIDCLK — INT_LVDS_EDIDCLK
<8> INT_LVDS_EDIDDATA — INT_LVDS_EDIDDATA

<8> INT_LVDS_DIGON — INT_LVDS_DIGON
<8> INT_LVDS_BLON — INT_LVDS_BLON

<8> INT_TXLCLKOUT+ — INT_TXLCLKOUT+
<8> INT_TXLCLKOUT- — INT_TXLCLKOUT-
<8> INT_TXLOUT0+ — INT_TXLOUT0+
<8> INT_TXLOUT0- — INT_TXLOUT0-
<8> INT_TXLOUT1+ — INT_TXLOUT1+
<8> INT_TXLOUT1- — INT_TXLOUT1-
<8> INT_TXLOUT2+ — INT_TXLOUT2+
<8> INT_TXLOUT2- — INT_TXLOUT2-

<27> CONTRAST — R7 *0_4 — LVDS_BRIGHT
<8> INT_LVDS_BRIGHT — R13 0_4 — LVDS_BRIGHT

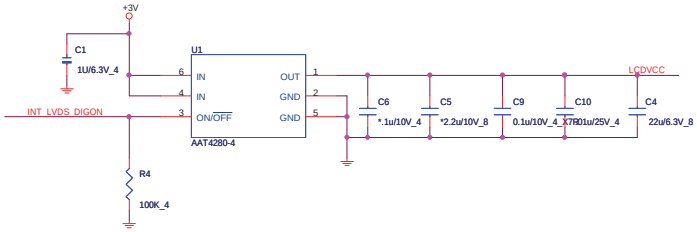
CCD-USB CCD +3V-current budget 0.2A



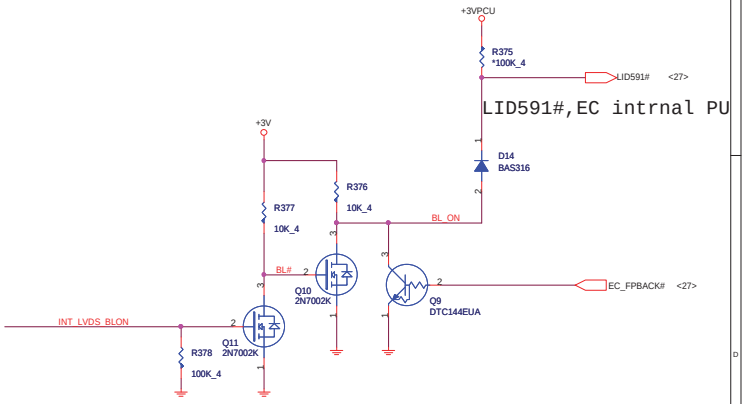
PT3661-BB : AL003661003
EM-6781-T3 : AL006781000

Lid Switch (Hall sensor)

LCD Power

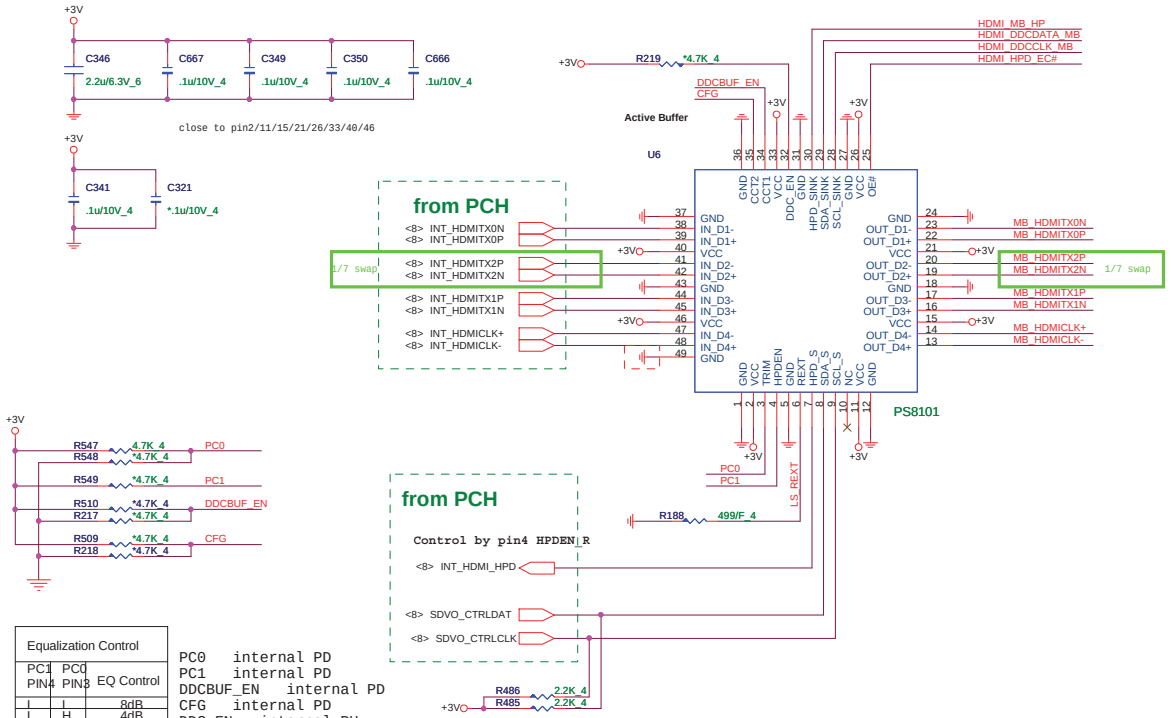


Backlight Control



Quanta Computer Inc.		
PROJECT : ZQH		
Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A
Date: Monday, March 14, 2011	Sheet 16 of 35	

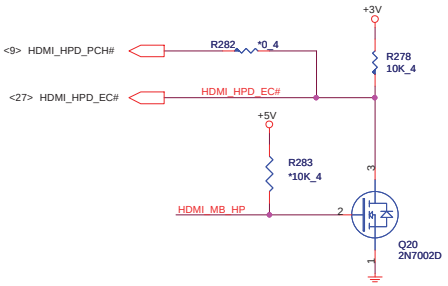
HDMI LEVEL SHIFTER



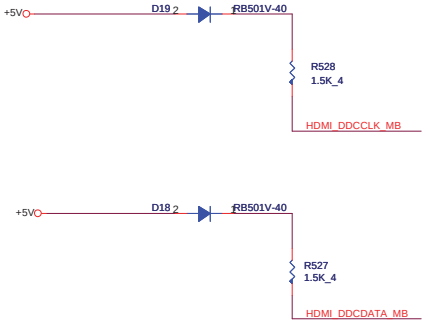
Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

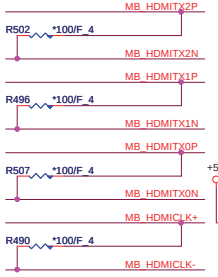
HDMI-detect

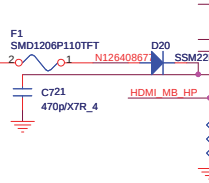


I2C

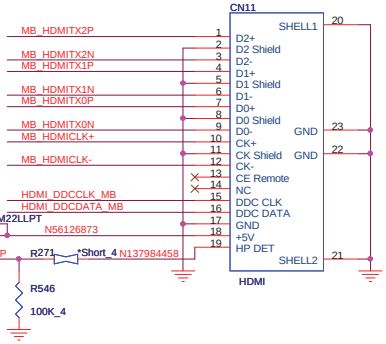


EMI





HDMI connector



Quanta Computer Inc.			
PROJECT : ZQH			
Size	Document Number	HDMI (PS8101)	Rev 1A
Date: Monday, March 14, 2011		Sheet 17 of 35	

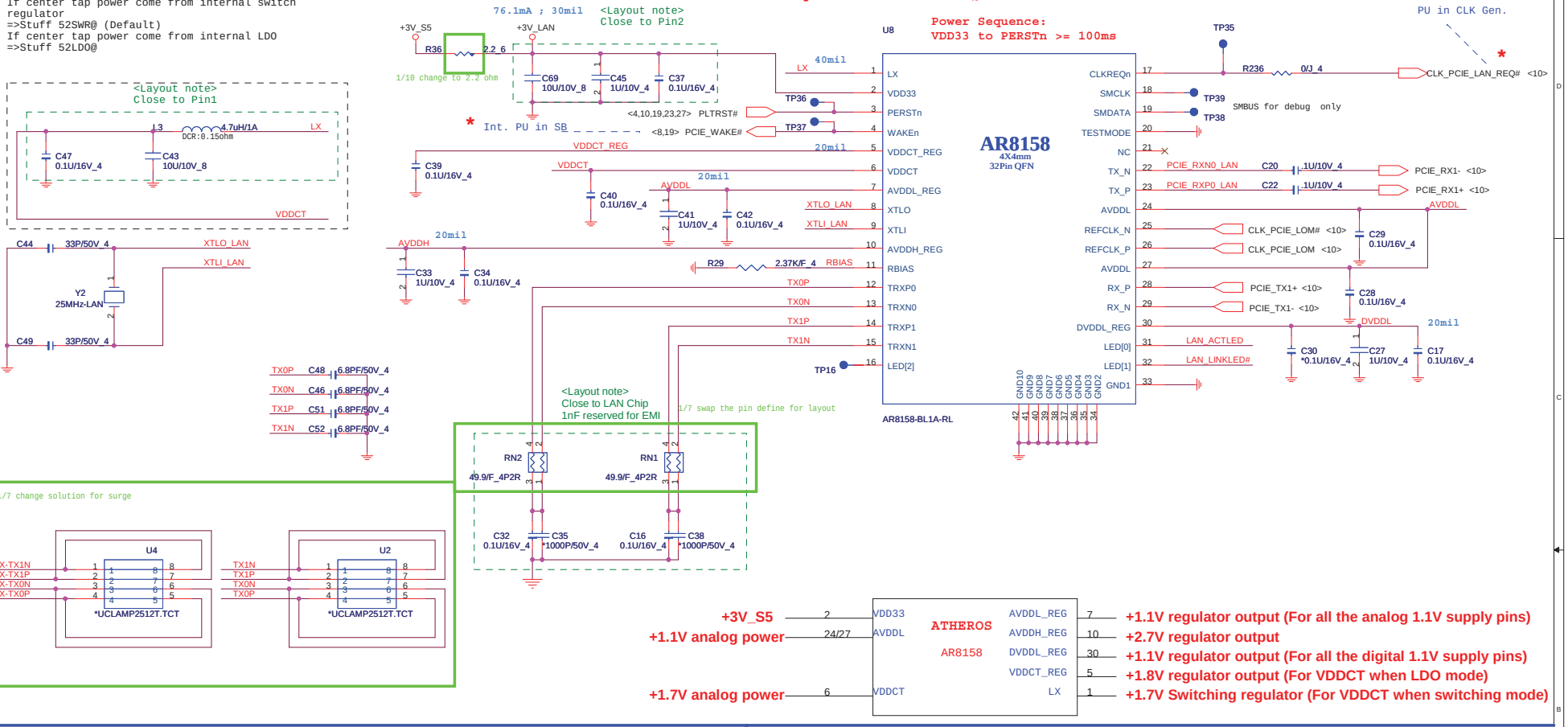
LAN (LAN)

<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@

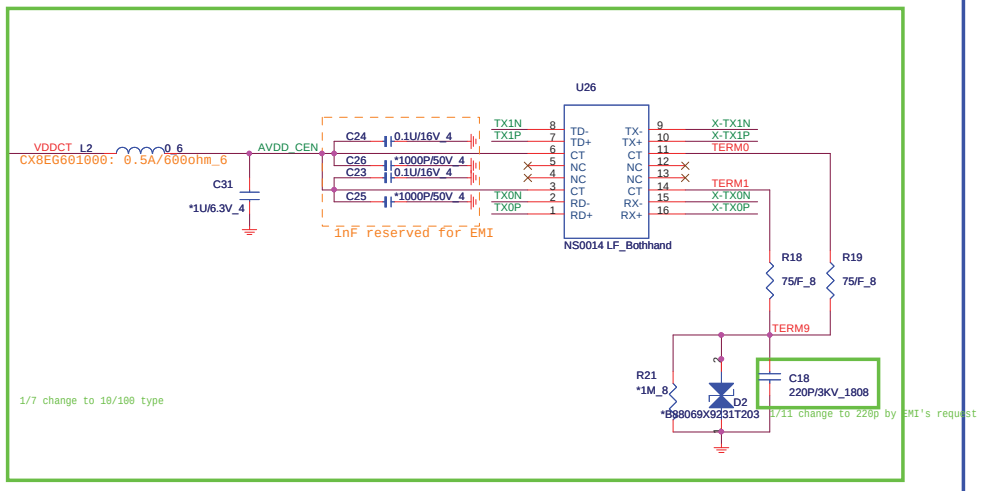
* Why does Pin17 CLKREQn connect to Pin16(LED2) and Pin30(DVDDL)?

Power Sequence:
VDD33 to PERSTn >= 100ms

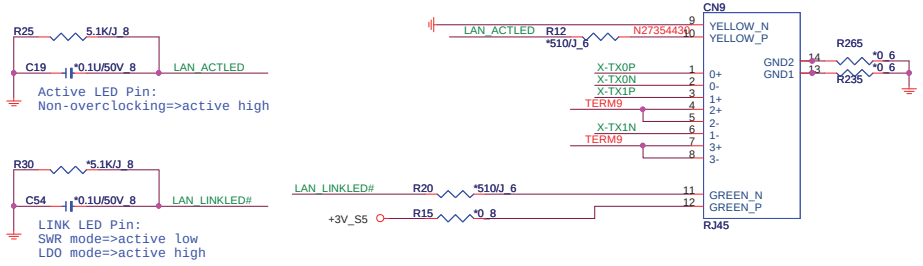
PU in CLK Gen.



TRANSFORMER (LAN)



RJ45 Connector (LAN)



Quanta Computer Inc.	PROJECT : ZQH	
Size	Document Number: LAN AR8158L	Rev: 1A
Date: Monday, March 14, 2011	Sheet 18 of 35	

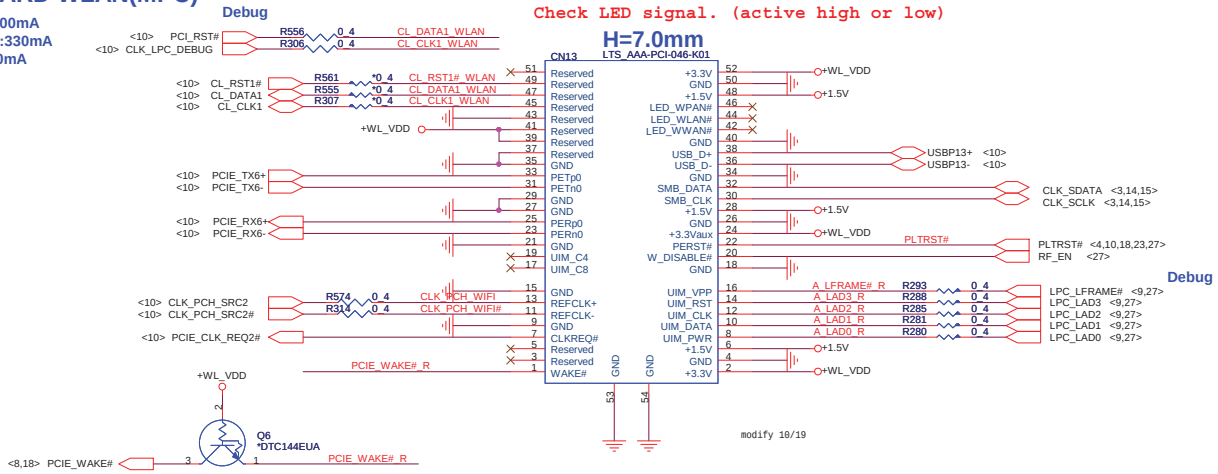
MINI-CARD WLAN(MPC)

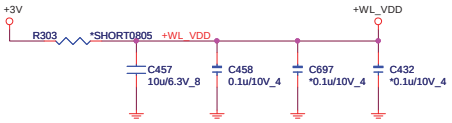
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

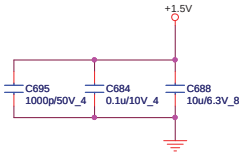
Debug

Check LED signal. (active high or low)

H=7.0mm







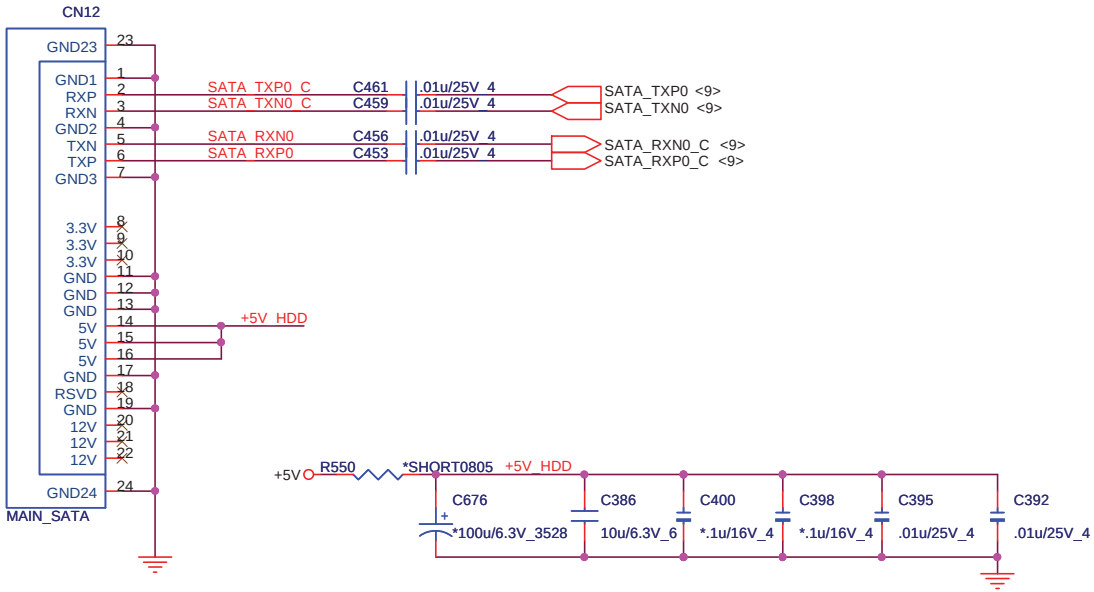
Quanta Computer Inc.

PROJECT : ZQH

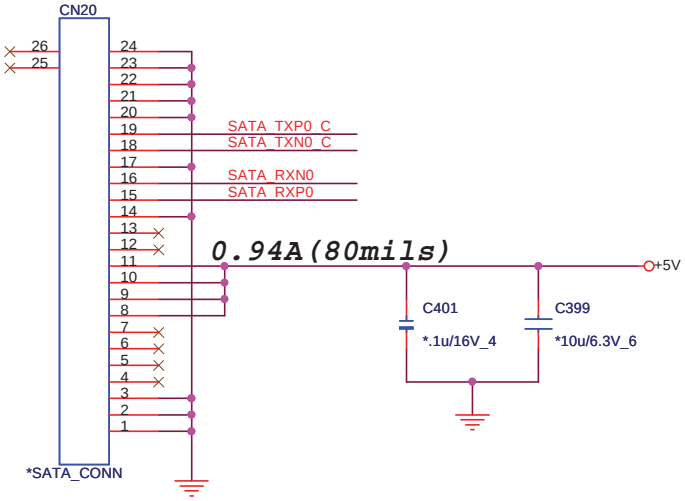
Size	Document Number	Rev
	MINI PCI-E card/TV	1A

Date: Monday, March 14, 2011 Sheet 19 of 45

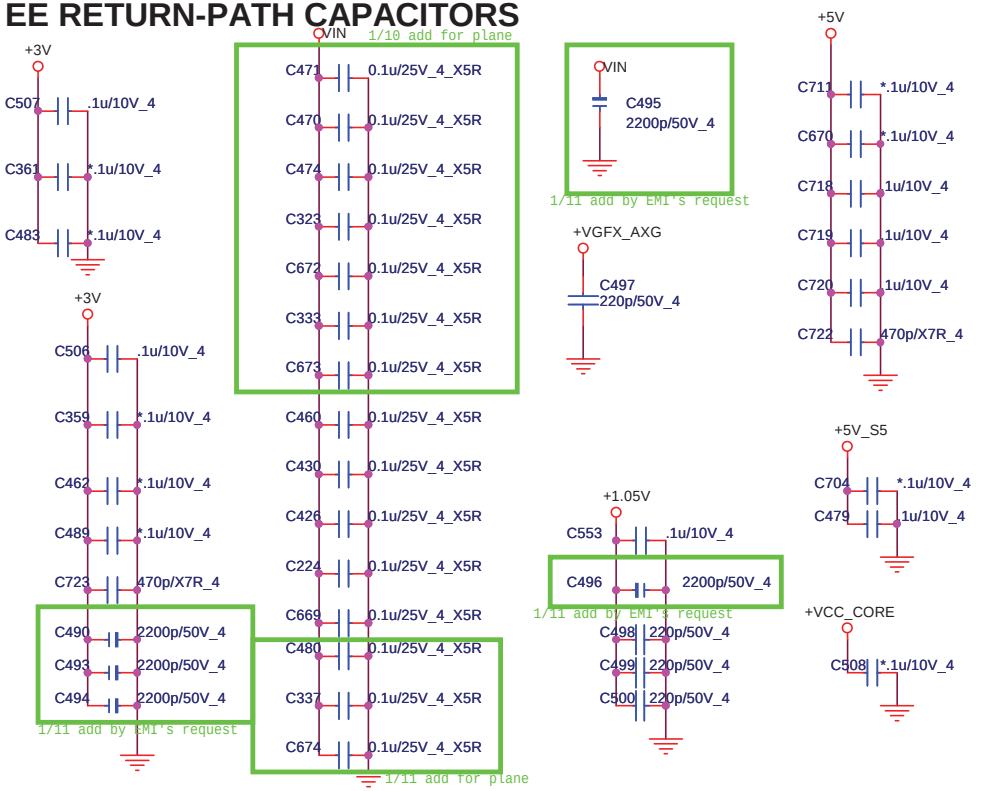
MAIN SATA HDD



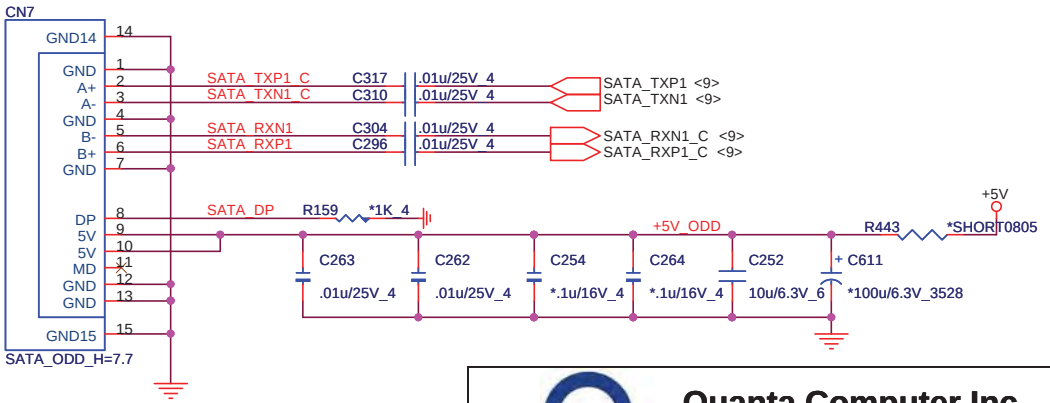
2.5" SATA HDD



EE RETURN-PATH CAPACITORS



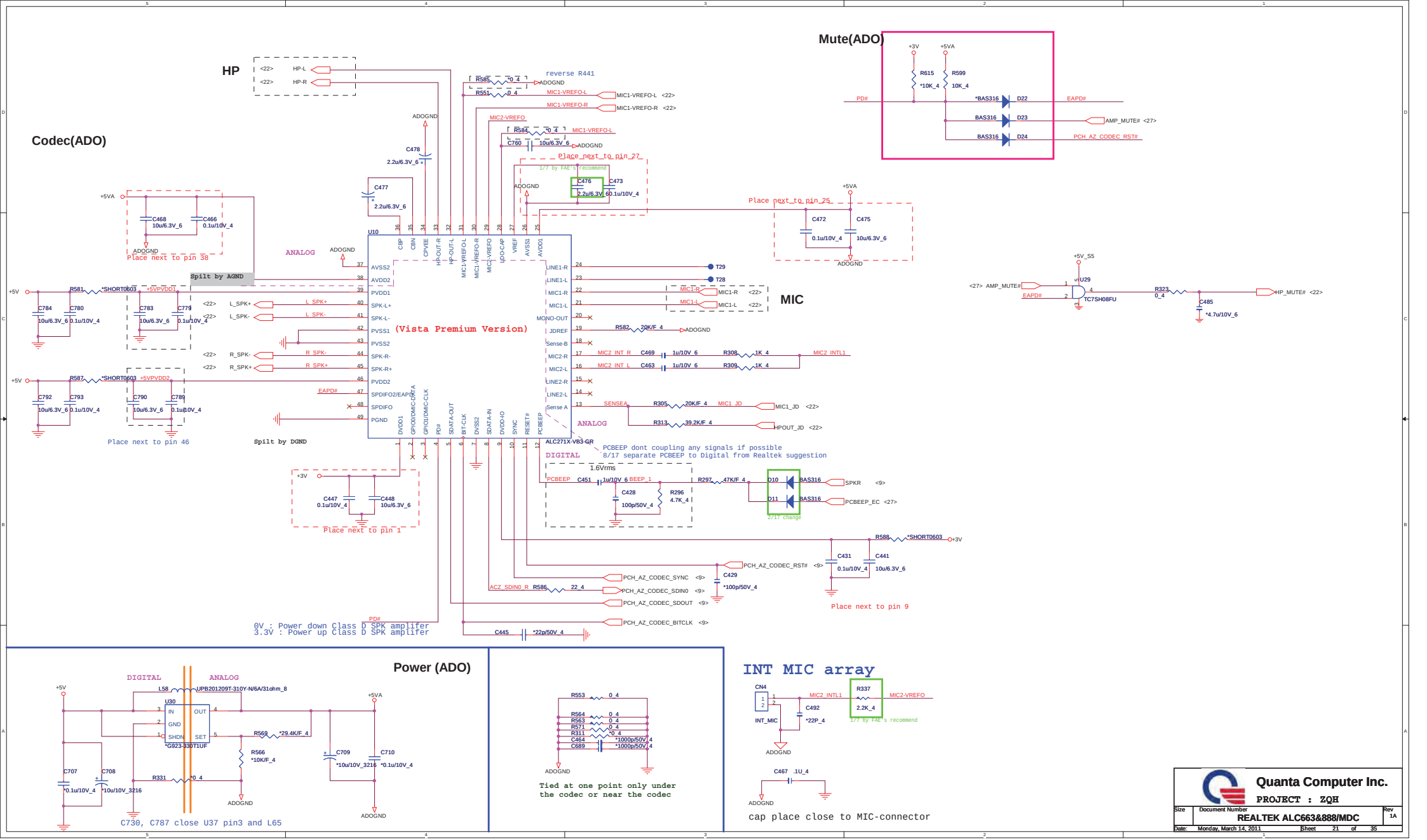
ODD (SATA)



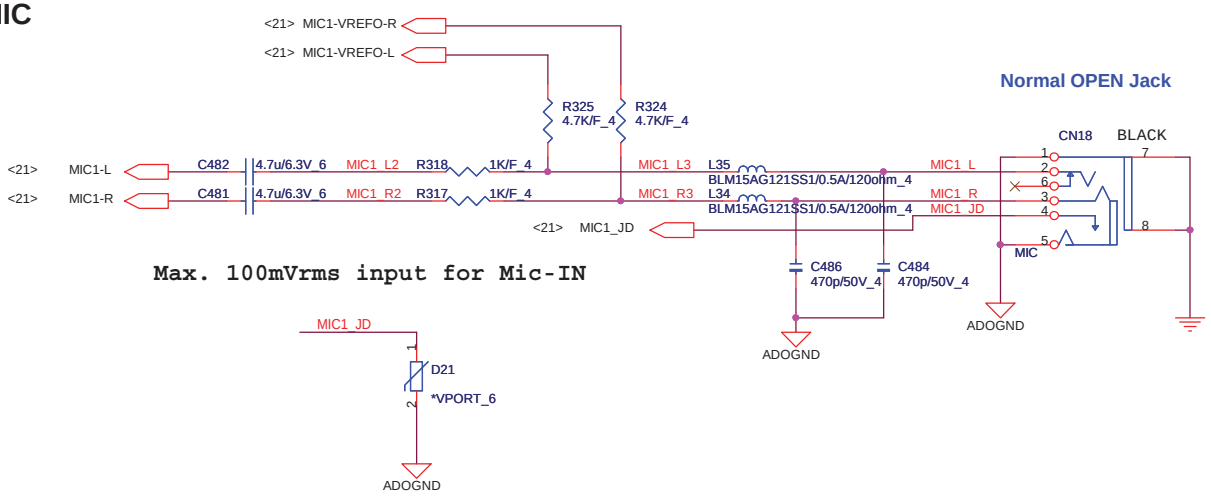
Quanta Computer Inc.

PROJECT : ZQH

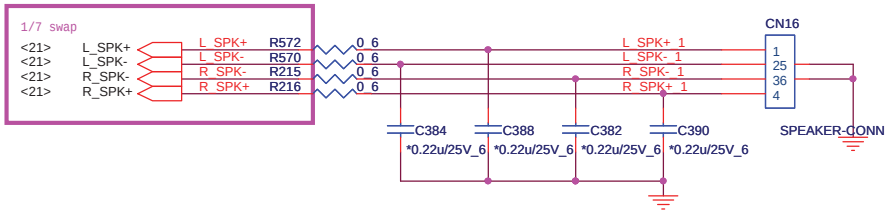
Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A
Date: Monday, March 14, 2011	Sheet 20 of 35	


HP
Codec(ADO)
Mute(ADO)
MIC
ANALOG
DIGITAL
(Vista Premium Version)
ALC271X-VB3-GR
Spilt by AGND
Spilt by DGND
Place next to pin 38
Place next to pin 46
Place next to pin 1
Place next to pin 27
Place next to pin 25
Place next to pin 9
reverse R441
PCBEEP dont coupling any signals if possible
8/17 separate PCBEEP to Digital from Realtek suggestion
1.6Vrms
0V : Power down Class D SPK amplifier
3.3V : Power up Class D SPK amplifier
Power (ADO)
C730, C787 close U37 pin3 and L65
Tied at one point only under
the codec or near the codec
INT MIC array
cap place close to MIC-connector
Quanta Computer Inc.
PROJECT : ZQH
REALTEK ALC663&888/MDC
Monday, March 14, 2011
Sheet 21 of 35

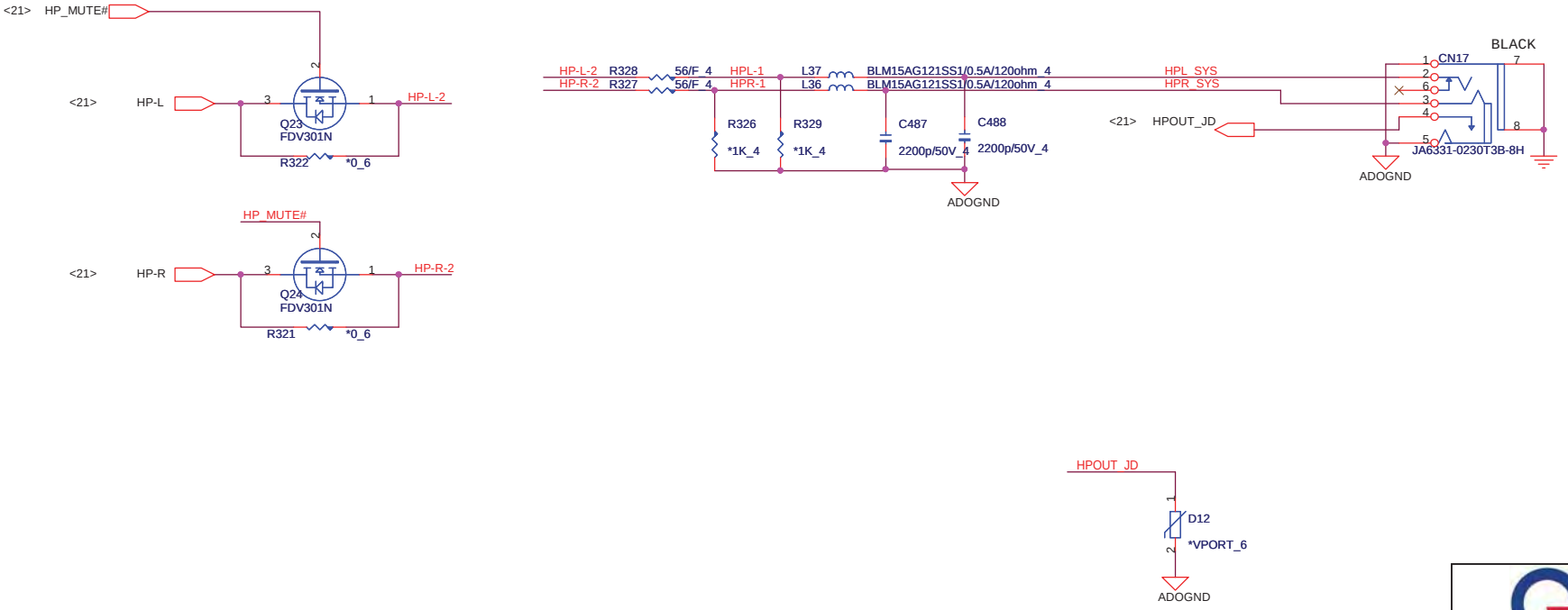
MIC



Internal Speaker



HP/SPDIF

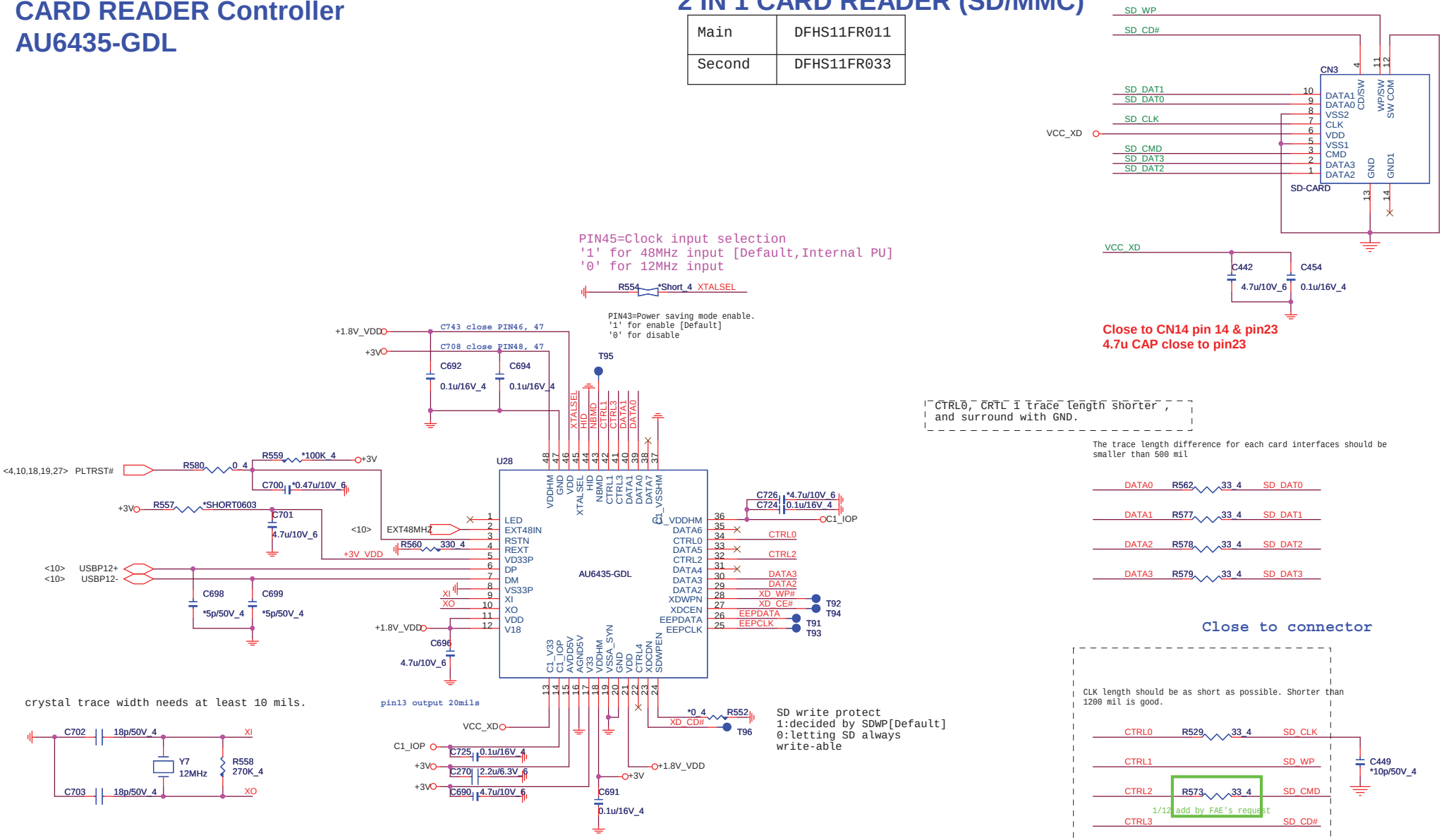


Quanta Computer Inc.		
PROJECT : ZQH		
Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
Date: Monday, March 14, 2011	Sheet 22 of 35	

CARD READER Controller
AU6435-GDL

2 IN 1 CARD READER (SD/MMC)

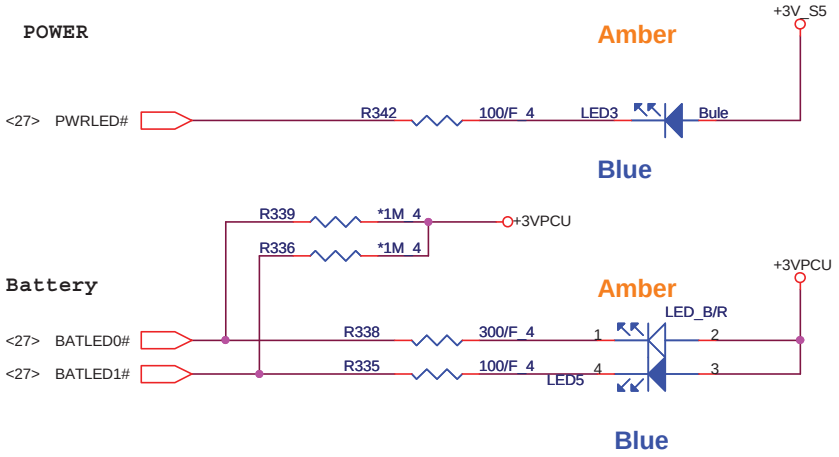
Main	DFHS11FR011
Second	DFHS11FR033



PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	AU6433 CardReader	1A
Date: Monday, March 14, 2011	Sheet 23 of 43	

LED

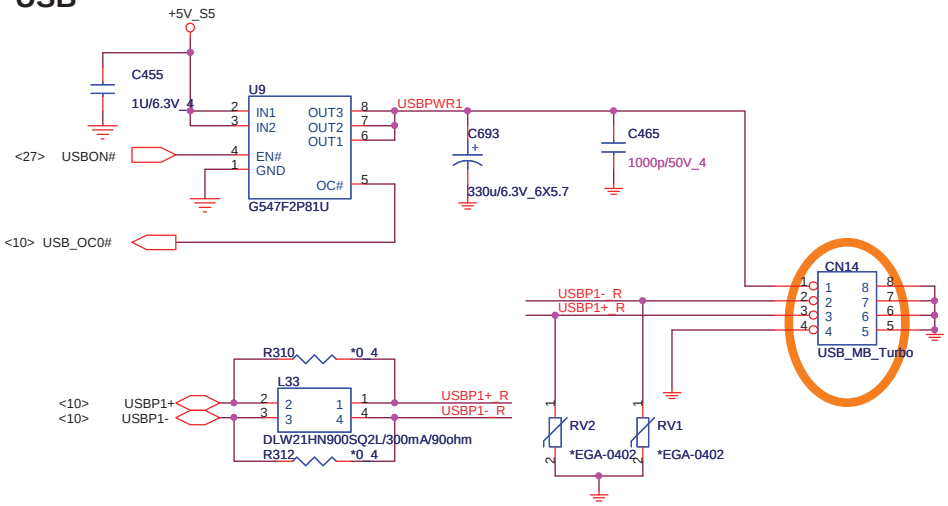


Quanta Computer Inc.

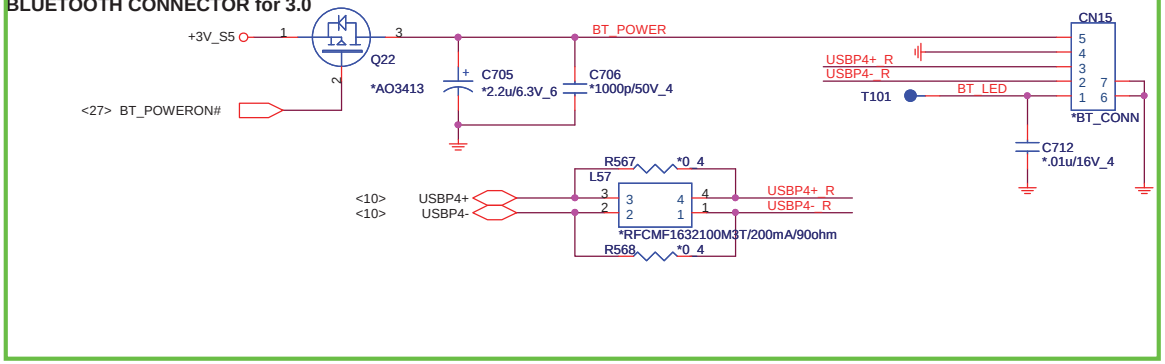
PROJECT : ZQH

Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A
Date: Monday, March 14, 2011	Sheet 24 of 35	

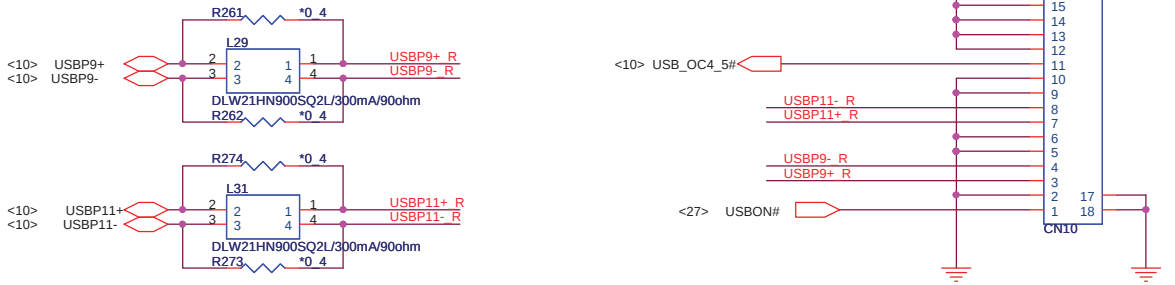
USB



BLUETOOTH CONNECTOR for 3.0



USB/B

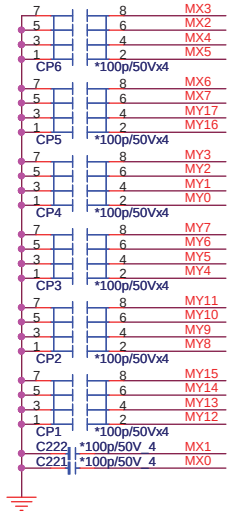


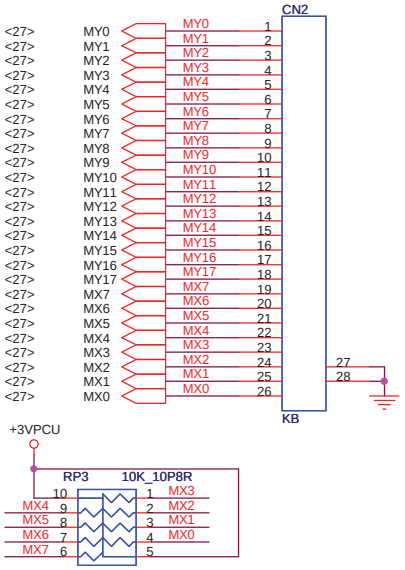
Quanta Computer Inc.

PROJECT : ZQH

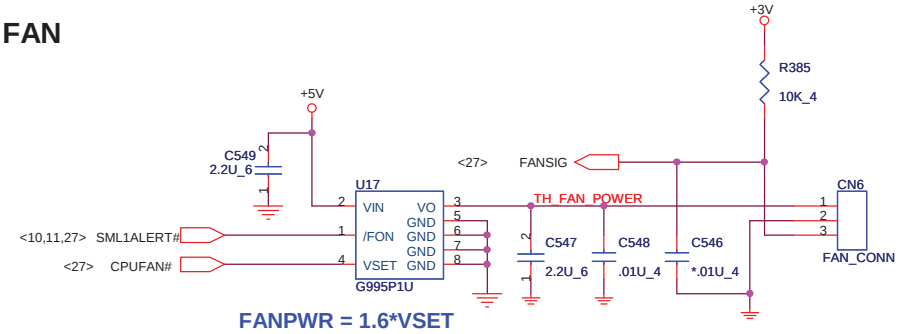
Size	Document Number	Rev
	USB/ BT	1A
Date: Monday, March 14, 2011	Sheet 25 of 35	

K/B



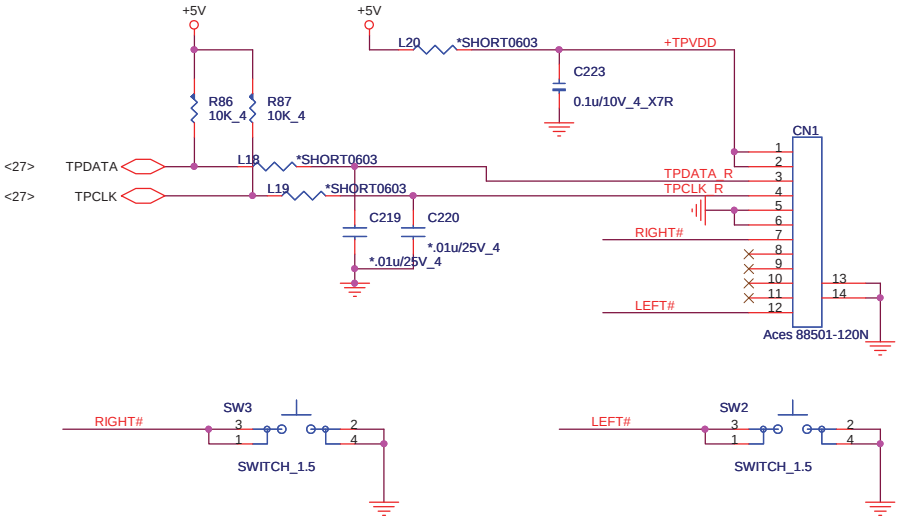


CPU FAN

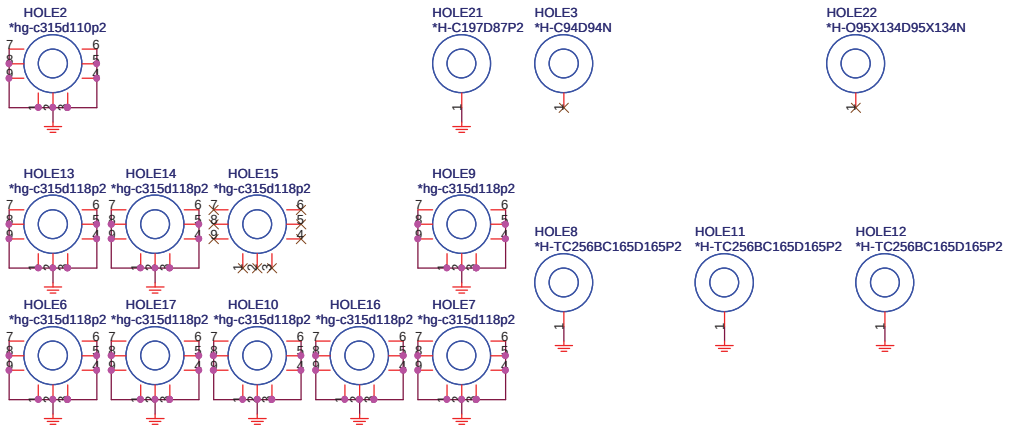


FANPWR = 1.6*VSET

TOUCHPAD & Switch CONN.

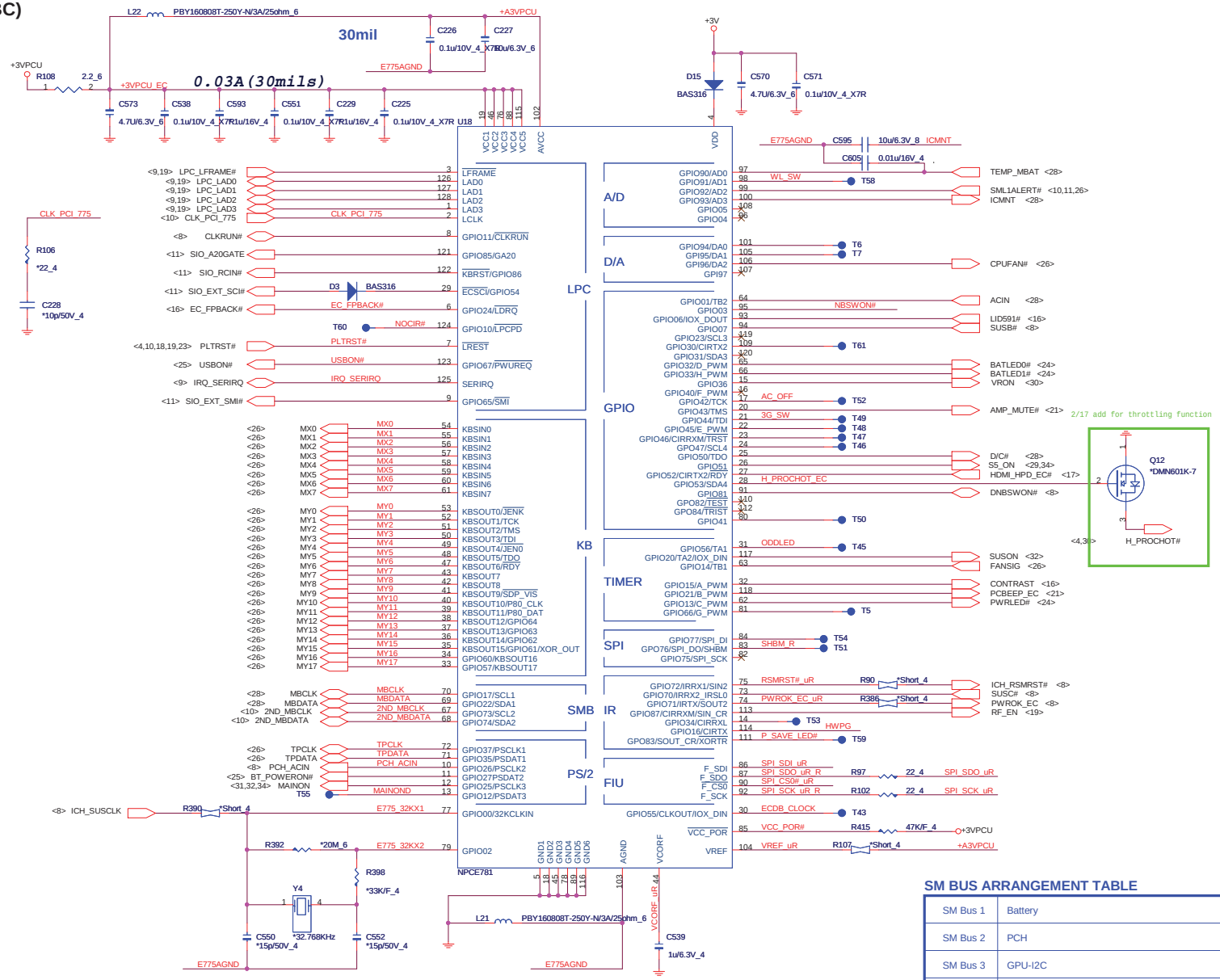


HOLE



Quanta Computer Inc.		
PROJECT : ZQH		
Size	Document Number: KB/FAN/TP+FP	Rev: 1A
Date: Monday, March 14, 2011	Sheet 26 of 35	

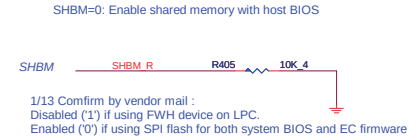
EC(KBC)



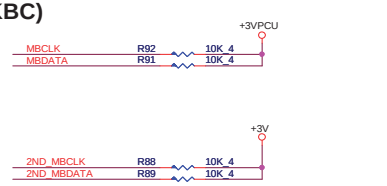
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU-I2C
SM Bus 4	N/A

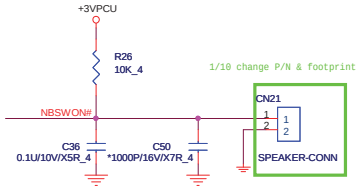
I/O ADDRESS SETTING(KBC)



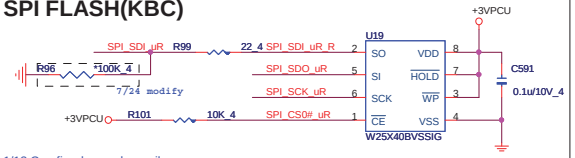
SM BUS PU(KBC)



PWR/B

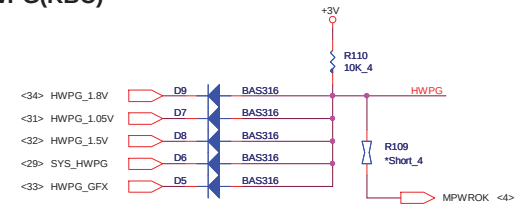


SPI FLASH(KBC)

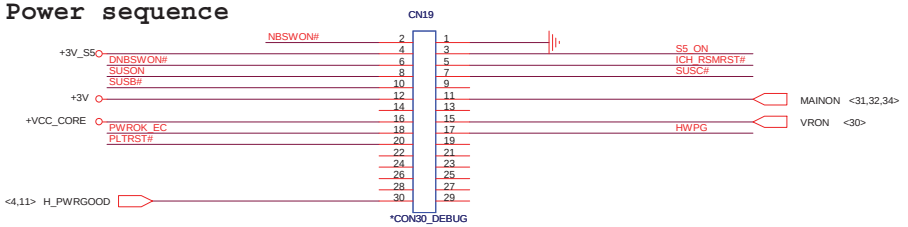


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

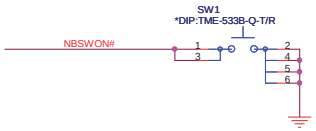
HWPG(KBC)



Power sequence

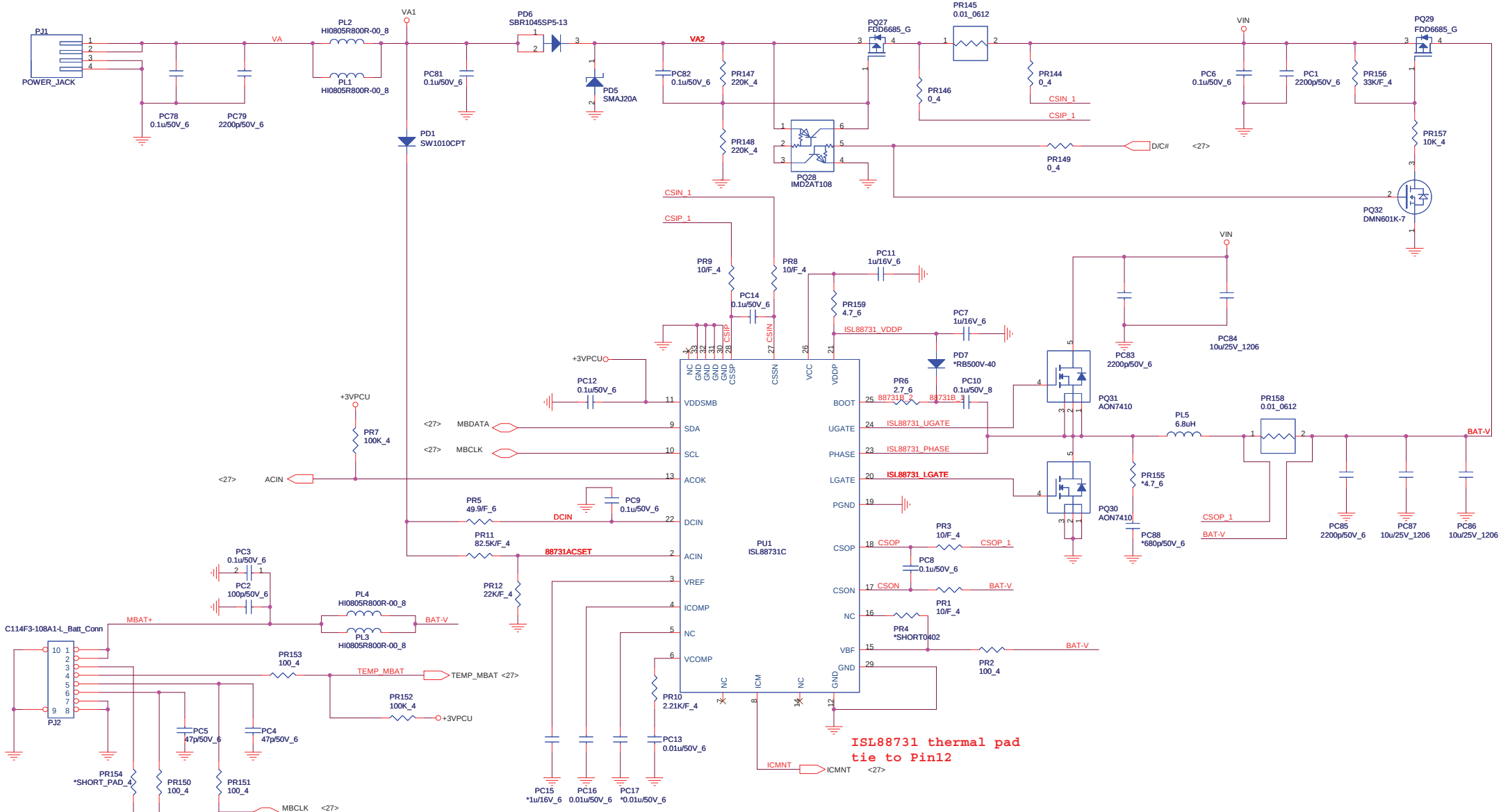


POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

Quanta Computer Inc.			
PROJECT : ZQH			
Size	Document Number		Rev
	WPCE781 & FLASH		1A
Date: Monday, March 14, 2011		Sheet 27 of 35	



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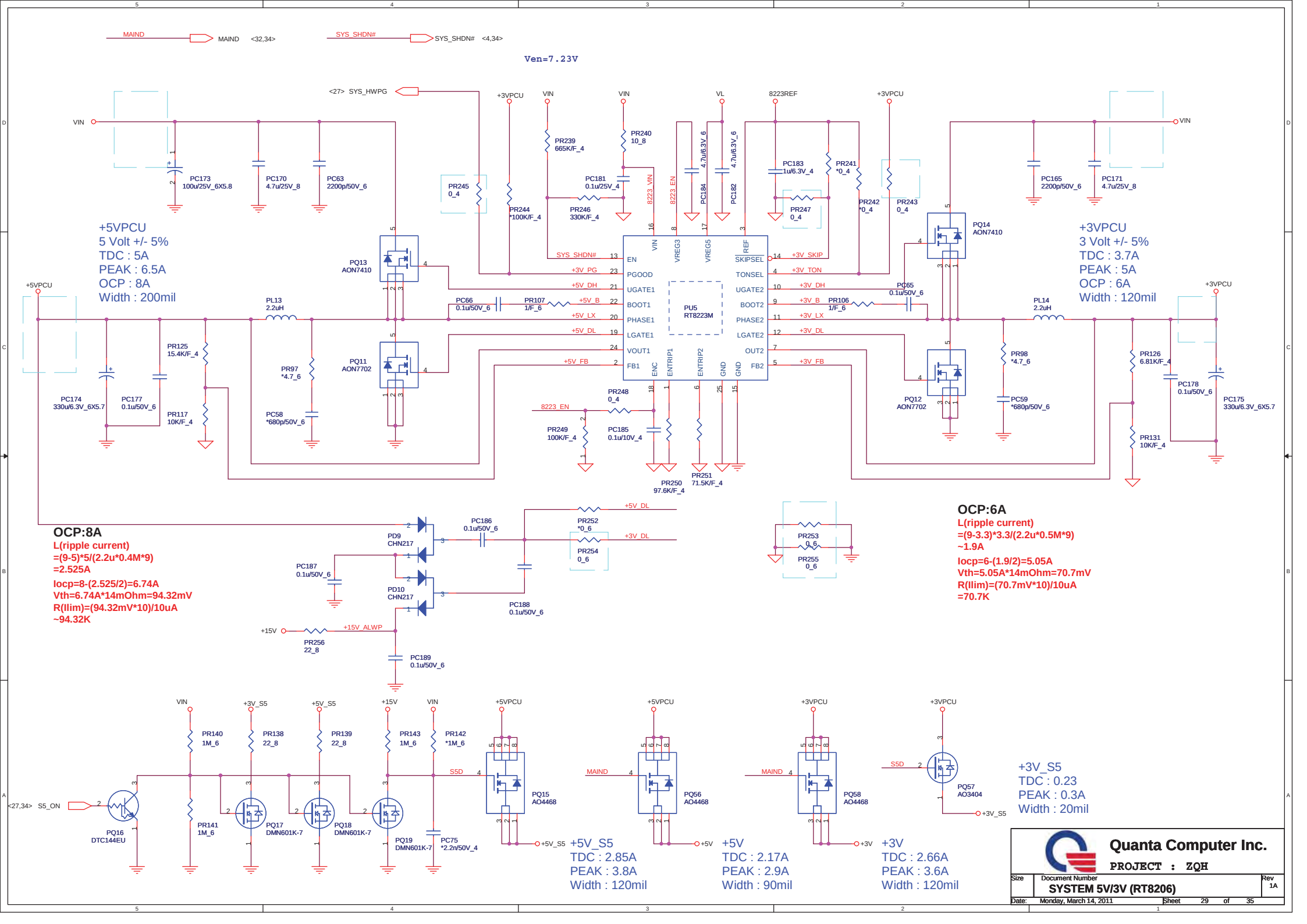
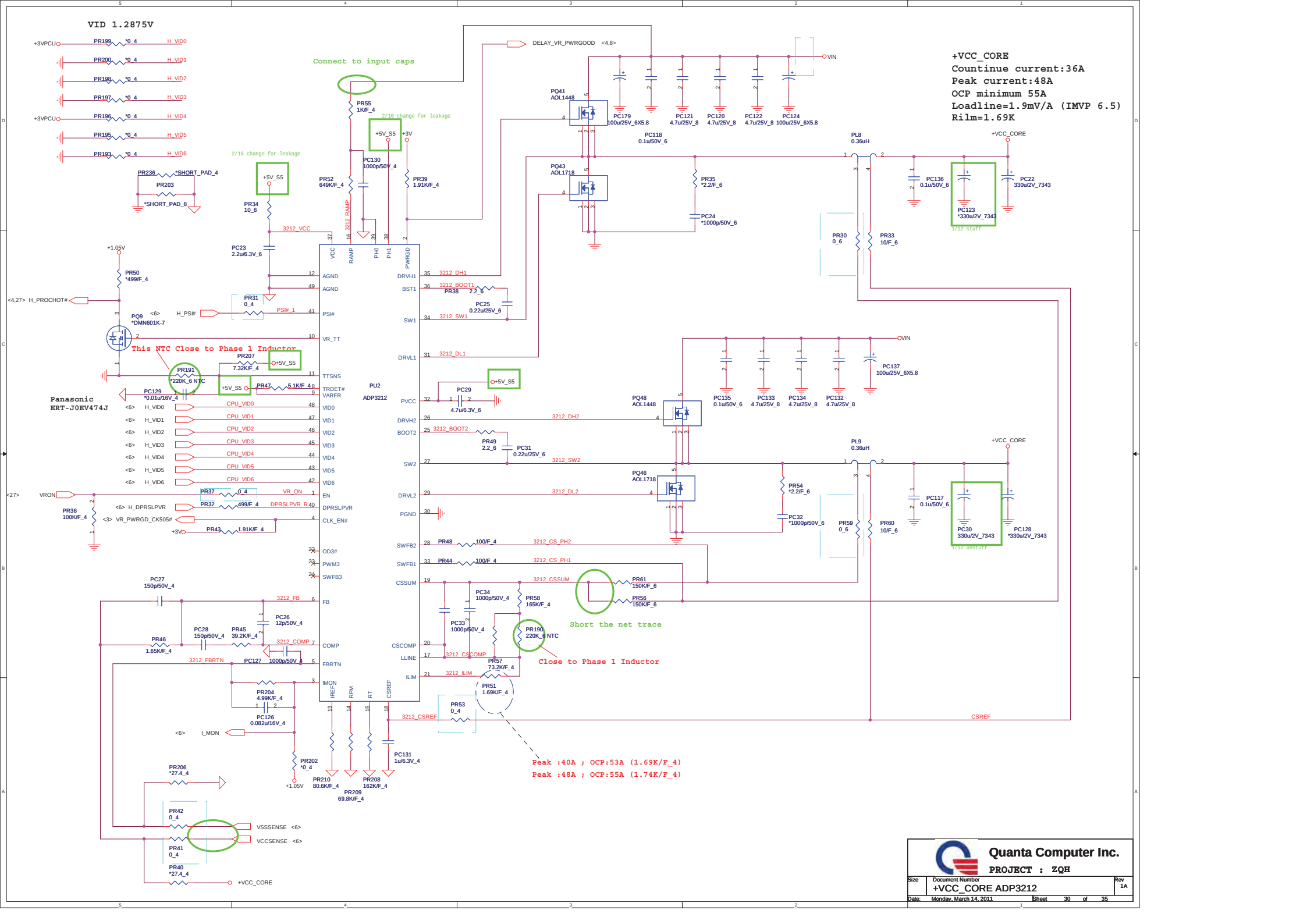
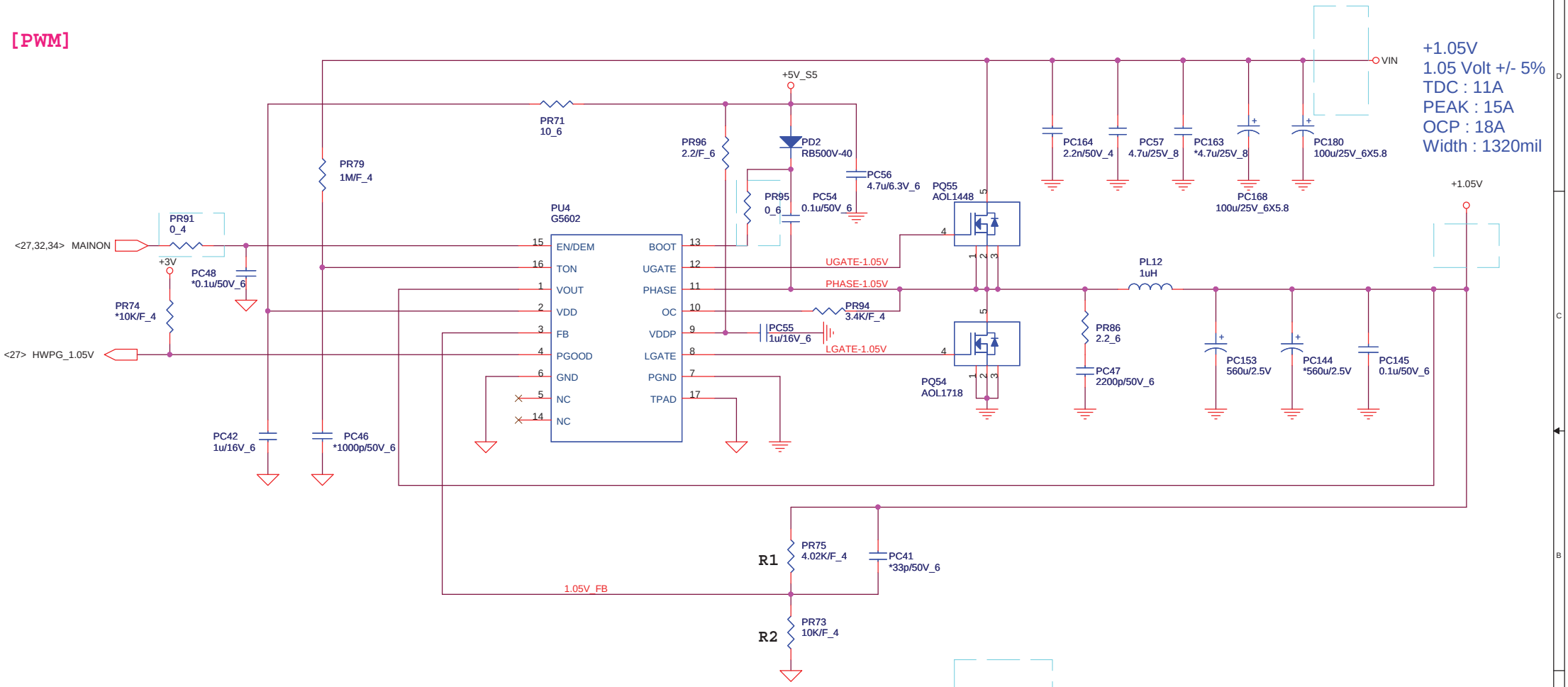
PROJECT : ZQH

Size	Document Number	Rev
	Charger(ISL88731A)	1A
Date: Monday, March 14, 2011	Sheet 28 of 35	


MAIND
MAIND <32,34>
SYS_SHDN#
SYS_SHDN# <4,34>
Ven=7.23V
<27> SYS_HWPG
+5VPCU
5 Volt +/- 5%
TDC : 5A
PEAK : 6.5A
OCP : 8A
Width : 200mil
+3VPCU
3 Volt +/- 5%
TDC : 3.7A
PEAK : 5A
OCP : 6A
Width : 120mil
PU5
RT8223M
OCP:8A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=8-(2.525/2)=6.74A
Vth=6.74A*14mOhm=94.32mV
R(Ilim)=(94.32mV*10)/10uA
~94.32K
OCP:6A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=6-(1.9/2)=5.05A
Vth=5.05A*14mOhm=70.7mV
R(Ilim)=(70.7mV*10)/10uA
=70.7K
<27,34> S5_ON
+3V_S5
TDC : 0.23
PEAK : 0.3A
Width : 20mil
+5V_S5
TDC : 2.85A
PEAK : 3.8A
Width : 120mil
+5V
TDC : 2.17A
PEAK : 2.9A
Width : 90mil
+3V
TDC : 2.66A
PEAK : 3.6A
Width : 120mil
Quanta Computer Inc.
PROJECT : ZQH
SYSTEM 5V/3V (RT8206)
Rev 1A
Monday, March 14, 2011
Sheet 29 of 35


VID 1.2875V
+VCC_CORE
Countinue current:36A
Peak current:48A
OCP minimum 55A
Loadline=1.9mV/A (IMVP 6.5)
Rilm=1.69K
Connect to input caps
This NTC Close to Phase 1 Inductor
Panasonic
ERT-J0EV474J
Short the net trace
Close to Phase 1 Inductor
Peak :40A ; OCP:53A (1.69K/F_4)
Peak :48A ; OCP:55A (1.74K/F_4)
PU2
ADP3212
Quanta Computer Inc.
PROJECT : ZQH
+VCC_CORE ADP3212
Monday, March 14, 2011

[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.647A

RILIM=4.3mohm*18-1.823/20uA=3.477Kohm

I(choke)peak=21.647A

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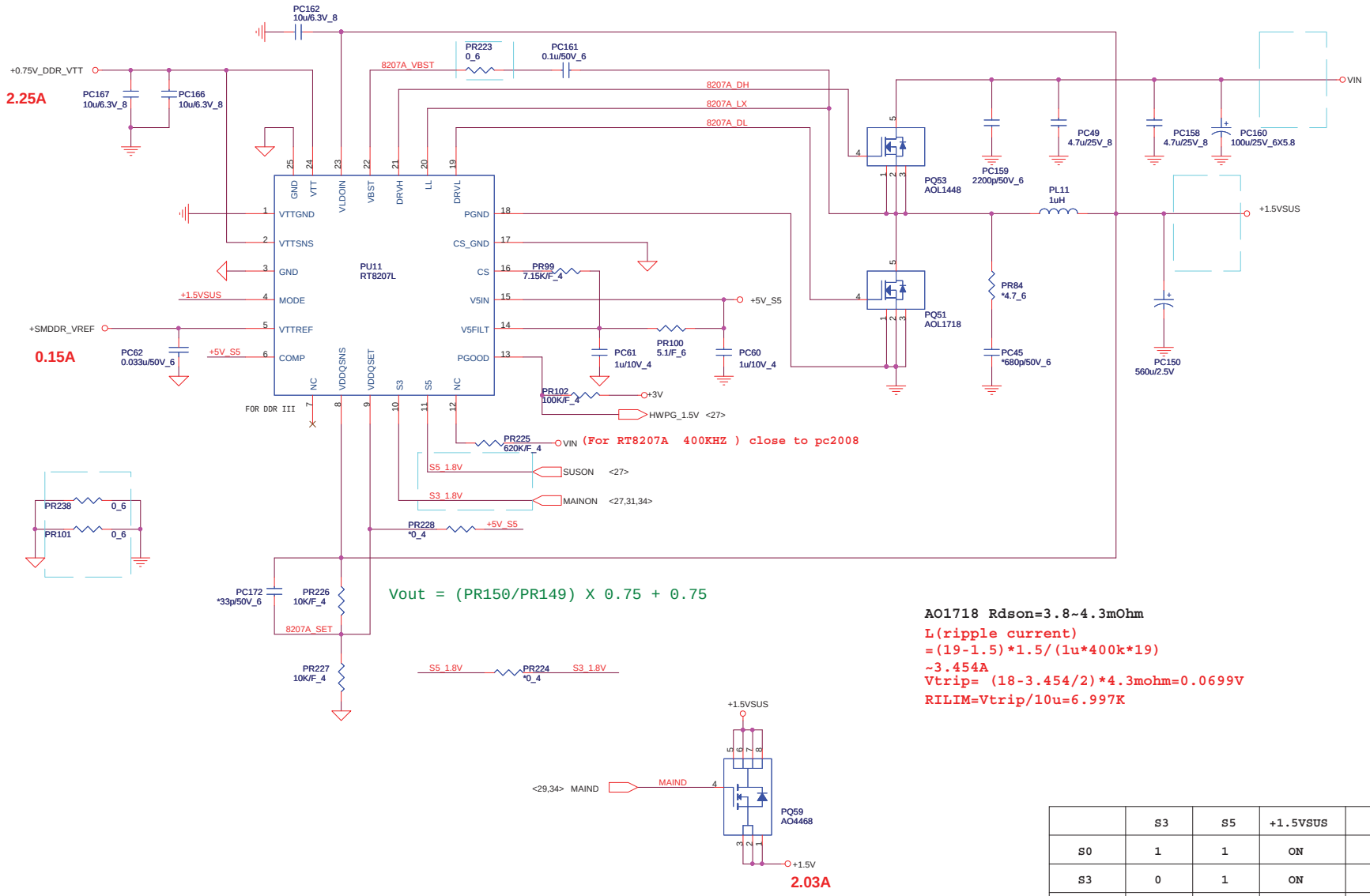
PROJECT : ZQH

Size	Document Number	Rev
	+VTT (G5602R41U)	1A

Date: Monday, March 14, 2011 Sheet 31 of 35

[PWM]



+1.5V_SUS
1 Volt +/- 5%
TDC : 12A
PEAK : 16A
OCP : 18A
Width : 480mil

AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(19-1.5)*1.5/(1u*400k*19)
~3.454A
Vtrip= (18-3.454/2)*4.3mohm=0.0699V
RILIM=Vtrip/10u=6.997K

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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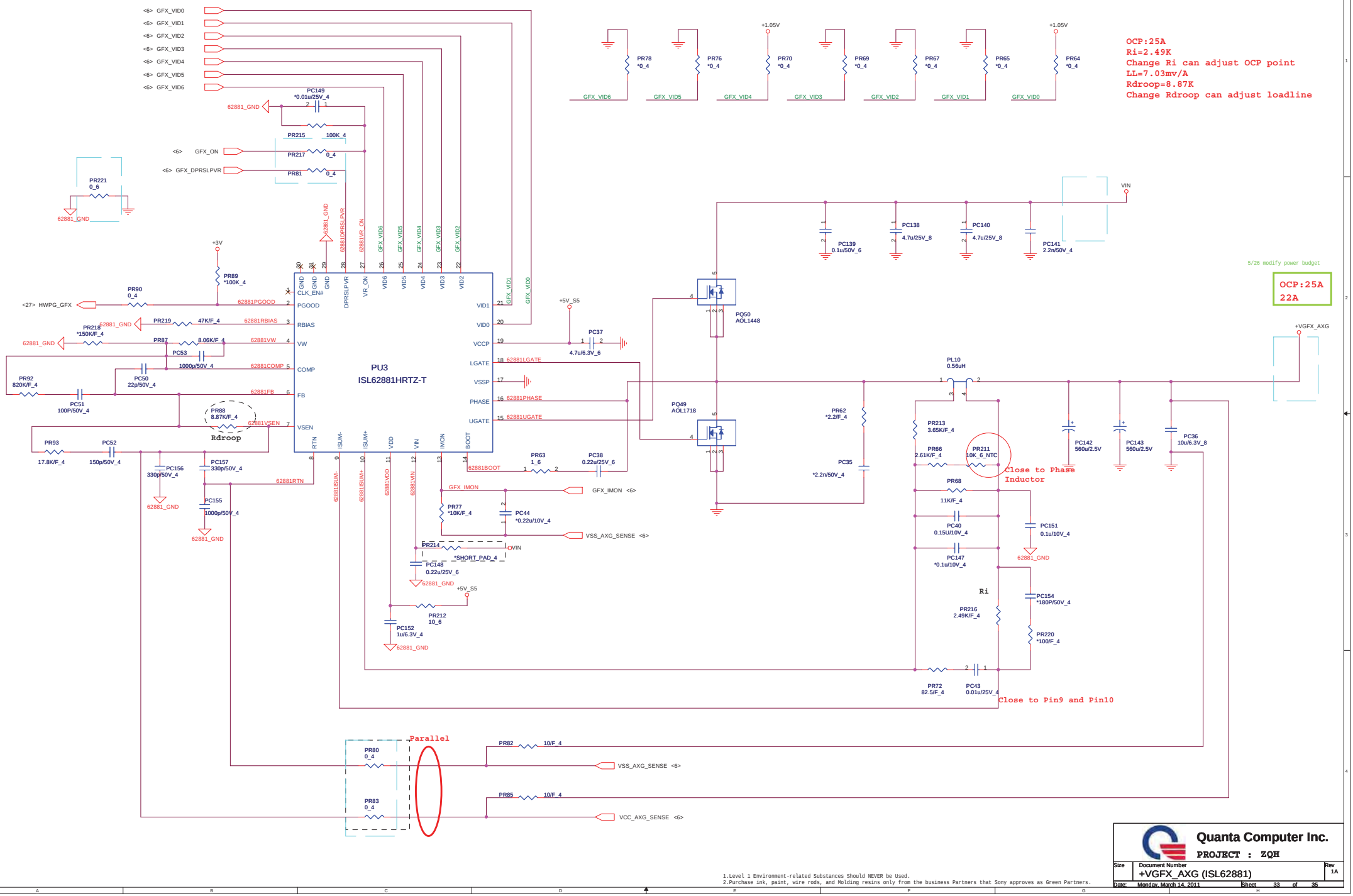
PROJECT : ZQH

Size	Document Number	Rev
	DDR 1.5V(RT8207A)	1A

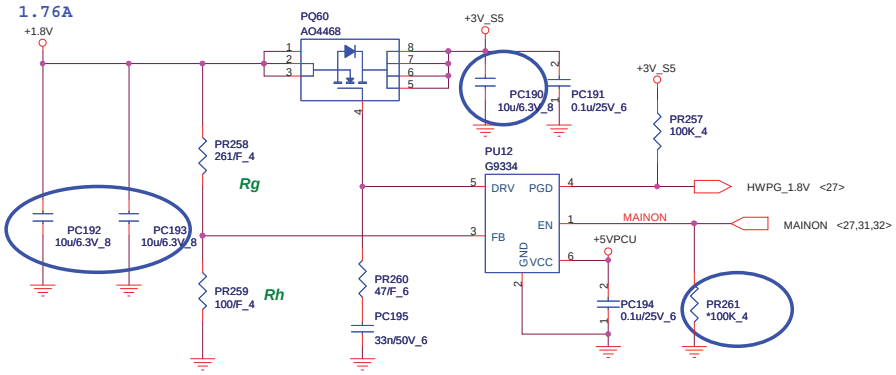
Date: Monday, March 14, 2011 Sheet 32 of 35

Int_VGA [PWM]



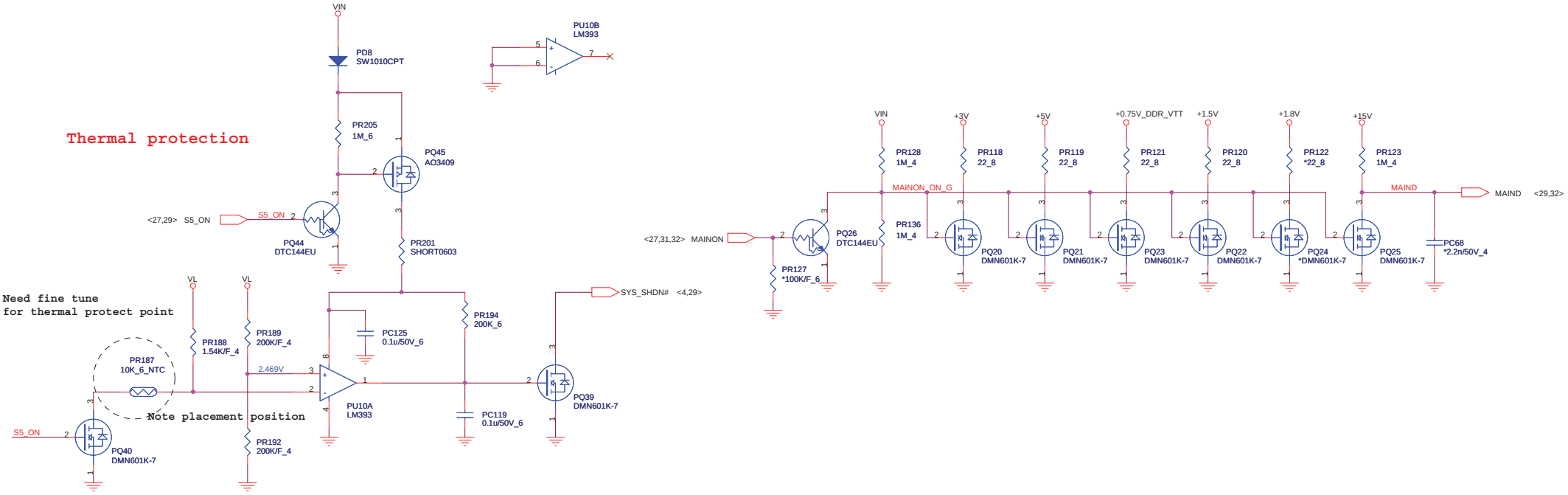
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

+1.8V
1.8 Volt +/- 5%
TDC : 0.76A
PEAK : 1.01A
Width : 40mil



*Vout1 = (1+Rg/Rh)*0.5*

For EC control thermal protection (output 3.3V)



Quanta Computer Inc.
PROJECT : ZQH

Size	Document Number	Rev
	Discharge/1.8V)	1A
Date: Monday, March 14, 2011	Sheet 34 of 35	

1 7/7 modify

Model	REV	CHANGE LIST
ZQH	1A	1/7 page.24 U6 HDMI pin 16,20 & pin 41,42 swap for layout page.30 CN16 speaker conn. pins 1,2,3,4 swap for layout page.25 X26 transformer change to 60/500 type page.25 U1, U4 change type, add D1, R11 for surge solution. page.25 PN1, RN2 swap the pin define for layout page.29 R327 change to 3.3K, R479 change to 10u by FAE's recommend 1/10 page.18 delete R6 page.20 add C353, C355, C370, C371, C374, C672, C673 for HiV plane page.27 change CN23 MXM/H connector P/N & footprint page.18 change R55 to 3.3 ohm 1/11 page.20 add C405, C357, 2X74 for HiV plane page.24 delete LVS USB power circuit page.29 add C400, C402, C404, C405, C406 by EMI's request page.18 change C16 to 22UF by EMI's request 1/18 page.38 stuff PC115, unstuff PC98 page.23 add R572 for FAE's request
	2A	2/14 Test Point change footprint. TP36F6 change to TP36/5. TP4850 change to TP3550 2/14 page.21 add R174 & R175 page.21 R164 chane to 10K ohm resistor 2/14 page.38 PC115 unstuff , PC98 stuff. page.27 unstuff SW1 & CN19 page.31 unstuff Bluetooth group. page.31 EMI : CP1, CP2, CP3, CP5, CP6 stuff 330pF cap array page.31 EMI : stuff C311 , add C361/C463/C567,C457,C458,C465,C466 page.31 EMI : stuff C519/C520 2/14 page30 Reserve C300 2/14 page29 LED9 , PT01 connect to+BATLEDDN & PT00 connect to+BATLEDUP 2/14 page16 add R10 C671 & C46 change to TOP side. 2/14 FSI : delete R141/R161/R167/R171/R167 , R414/R478/R481/R487/R494/R499/R500/R505/R464/R472/R478/R479/R491/R502/R512/R533 change to 0402short : R140/R154/R153/R151/R158/R214/R163/R184/R171/R554/R557/R188/R400/R504/R56 2/14 change to 0402short : R113/R116/R168/R169/R180/R173/R178/R180/R281/R313/R417/R420/R473/R482/R5/R11/R53/R55/R67/R60/R61.../L36 2/14 page.16 Add C46/C66/C61/C62 2/15 PHASE cahnge to shortpad 2/15 page21 delete R130 & R131, Add C674. C100 & C684 change to TOP Add C333 , C348 page31 stuff C361 2/16 page.38 change +5V_PCU power to +5V_S5 for leakage 2/17 page.21 remove R174, R175 & add R16, R11 2/17 page.27 add Q12 and use GPIO23 for throttling function for 90W adaptor 2/17 page.21 change R16 P/N 2/17 page.14 change R11, R16 to 0805 shortpad page.15 change R12 to 0805 shortpad page.12 change R140, R142, R219,R424 to 0805 shortpad page.19 change R363 to 0805 shortpad page.38 change R421, R538 to 0805 shortpad 2/17 page.35 change R279 to 120K shortpad 2/17 page.16 unstuff C35
	3C	3/10 page.27 unstuff Q12 3/14 page25 L33 exchange order for USB signal routing. 3/16 page.16 R12 & R35 unstuff , R13 change to 0805 resistor and unstuff. 3/16 page.16 Add R214 & R174 , 0 ohm or CAP depend on result. 3/16 page.32 delete shortpad , PR223 & PR236
	4A	

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PROJECT : ZQH

Change list

DOC NO.	PROJECT MODEL :	ZQH	APPROVED BY:		DATE:
	PART NUMBER:		DRAWING BY:		REVISON: