ZQ2 SYSTEM DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

IV@ -----> iGPU
SW@ -----> dGPU
SP@ -----> option notice
SIDE@ -----> sideport

sideport-L75,L76,R583,R392,C832,R455,R550,R502
NB A11-R105,R108
SB A12-R267,R271
JV/JM-CN16,R450,R456
EC-D8,D27
UMA-R461
VRAM-R358,R359,R360,R363,R365,R72

DDR3-SODIMM1 PAGE 5,6 — DDR3 channel A
DDR3-SODIMM2 PAGE 5,6 — DDR3 channel B
AMD Champlain 35mm X 35mm S1G4 Processor 638P (PGA)45W/35W PAGE 2,3,4
CPU THERMAL SENSOR PAGE 4
CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK
From SB CLOCK GEN
HT3
PCI-E
PCI-Express 8X
NORTH BRIDGE RS880 A12 21mm X 21mm, 528pin BGA PAGE 7,8,9,10
Side port
DDR3 RAM PAGE 7
ATI Park XT 128-bit M2 Pkg 29mm X 29mm PAGE 16,17,18 19,20,21
800MHz VRAM DDR3 64MX16X4,64 bit 64MX16X8,128 bit PAGE 22
VGA Park
HDMI PAGE 24
CRT PAGE 23
LVDS PAGE 23
X1 LAN Atheros PCIE-LAN AR8151 (10/100/1000) PAGE 25
X2 Mini PCI-E Card (Wireless LAN) PAGE 26
RJ45 PAGE 25
ALINK X4
SATA - HDD1 PAGE 27 — SATA0 150MB
SATA - CD-ROM PAGE 27 — SATA1 150MB
SOUTH BRIDGE SB820 21mm X 21mm, 528pin BGA A11 4.5W(Ext) 4.3W(Int) PAGE 12,13,14,15,16
BT PAGE 32
USB1.1
USB2.0
USB2.0 Ports X1 PAGE 30
Webcam PAGE 23
CardReader AU6437 PAGE 29
WLAN conn PAGE 26
10,11,12
USB BOARD USB2.0 Ports x3 PAGE 30
Power BOARD PAGE 30
Switch BOARD PAGE 30
LPC
Azalia
Winbond KBC NPCE781L PAGE 33
Codec RTL ALC271X PAGE 28
Keyboard PAGE 32
Touch Pad PAGE 32
CPU FAN PAGE 32
SPI PAGE 33
Digital MIC PAGE 28
AUDIO CONN (Phone/ MIC) PAGE 28
Speaker PAGE 28

CPU
- AMD CPU CORE (ISL6265) PAGE 36

NB
- NB_CORE (UP6111AQDD) PAGE 38
- +VGPU_CORE (MAX8792ETD) PAGE 40
- +1V/+1.5_GPU/+1.8_GPU PAGE 41
- 0.9V/DDR 1.5V(RT8207) PAGE 39
- SYSTEM 5V/3V (RT8206) PAGE 35
- 1.1V(UP6111AQDD) PAGE 37
- Discharge /Thermal protec PAGE 42

PROJECT : ZQ2
Quanta Computer Inc.
Size | Document Number: Block Diagram | Rev 1A
Date: Wednesday, May 27, 2009 | Sheet 1 of 46

S1G4

1.1V@1.5A

SI Change from AMD request

CPU CLK

Keep trace from resistor to CPU within 0.6"
keep trace from caps to CPU within 1.2"

SideBand Temp sense I2C

HT LINK

SOCKET_638_PIN

FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)

The RS880 family does not support CLMC architecture
The LDTREQ# connection from the CPU to ALLOW_LDTSTOP
of the Northbridge is no longer required.

for debug only

S1g4 does not support MEMHOT#

Serial VID

SI Change from AMD request

PV stage:add +1.5VSUS option
R540 R541 for Caspian CPU
power leakge issue

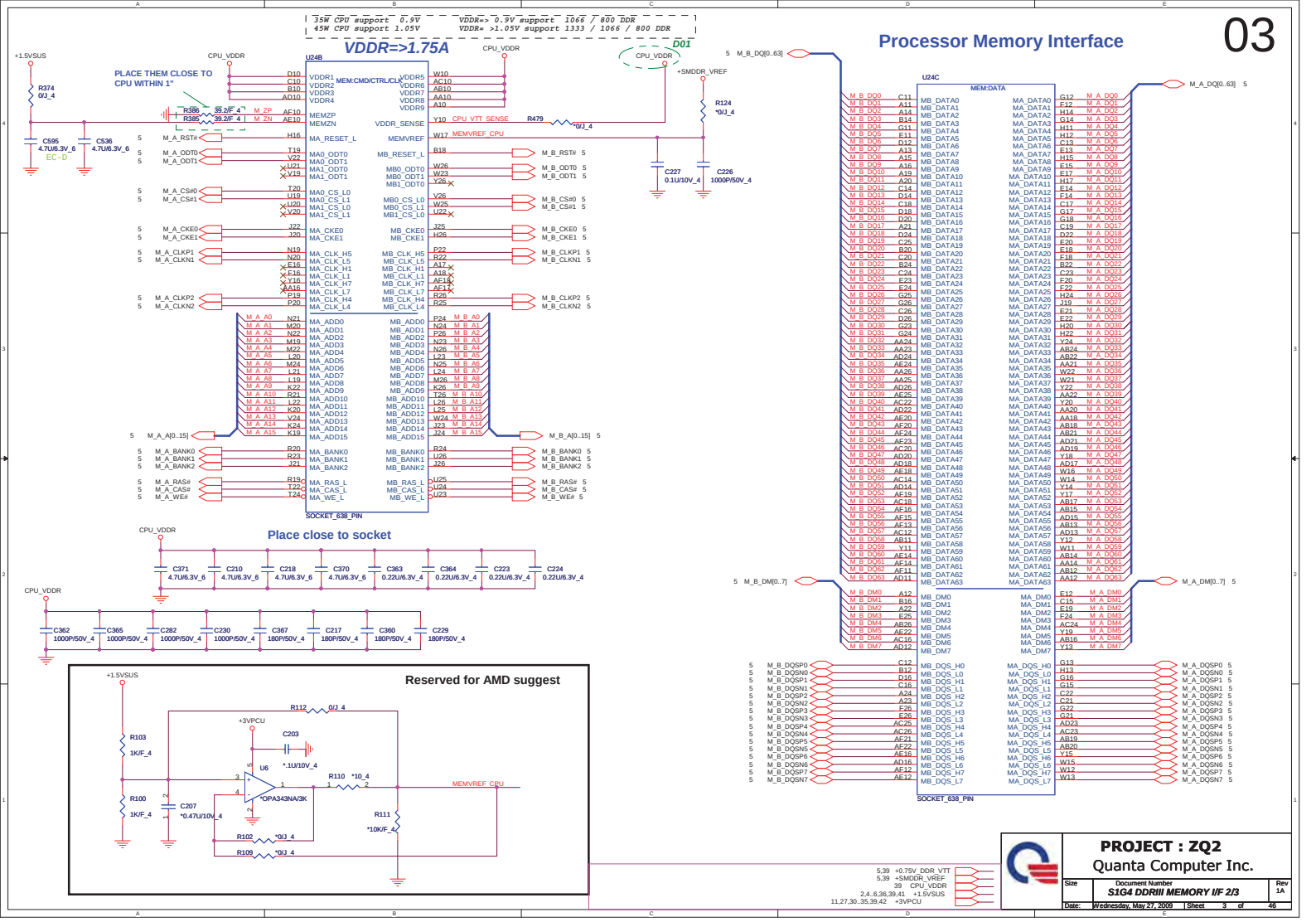
VFIX MODE — VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

HDT Connector

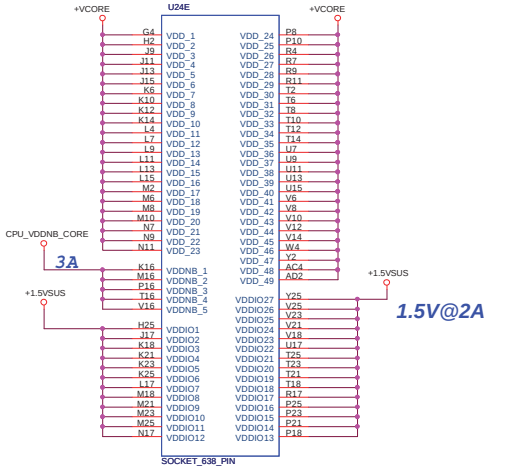
S1G4

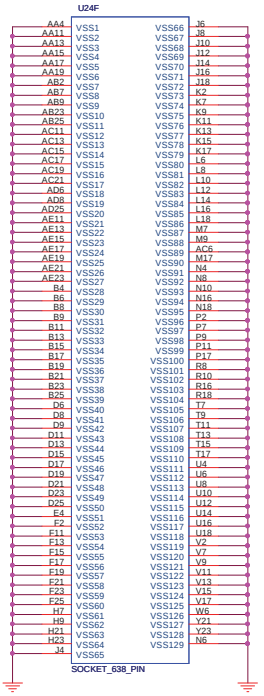
PROJECT :	ZQ2
Quanta Computer Inc.	
Size	Document Number: S1G4 HT,CTL I/F 1/3 — Rev: 1A
Date: Wednesday, May 27, 2009	Sheet 2 of 46

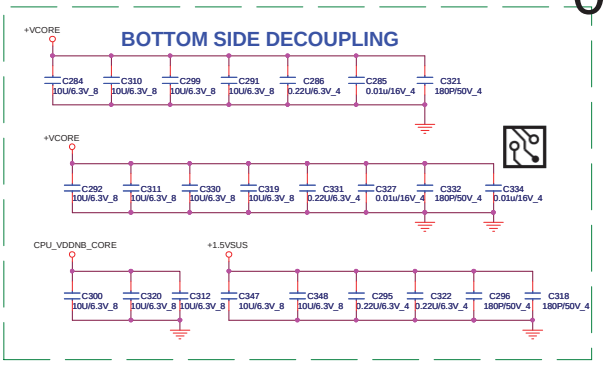


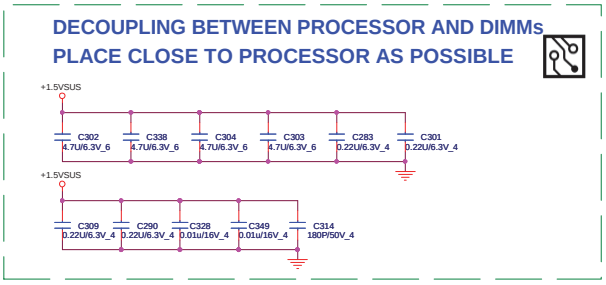
03
Processor Memory Interface
35W CPU support 0.9V
45W CPU support 1.05V
VDDR=> 0.9V support 1066 / 800 DDR
VDDR= >1.05V support 1333 / 1066 / 800 DDR
VDDR=>1.75A
D01
U24B
MEM:CMD/CTRL/CLK
PLACE THEM CLOSE TO CPU WITHIN 1"
SOCKET_638_PIN
Place close to socket
U24C
MEM:DATA
Reserved for AMD suggest
U6
*OPA343NA/3K
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
S1G4 DDRIII MEMORY I/F 2/3
Rev
1A
Date: Wednesday, May 27, 2009
Sheet 3 of 46

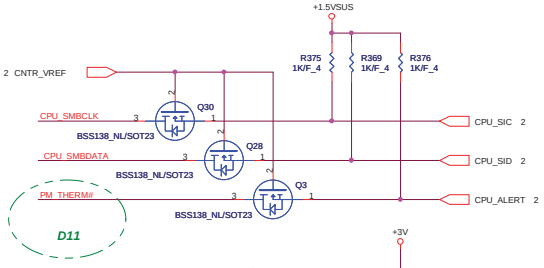
PROCESSOR POWER AND GROUND

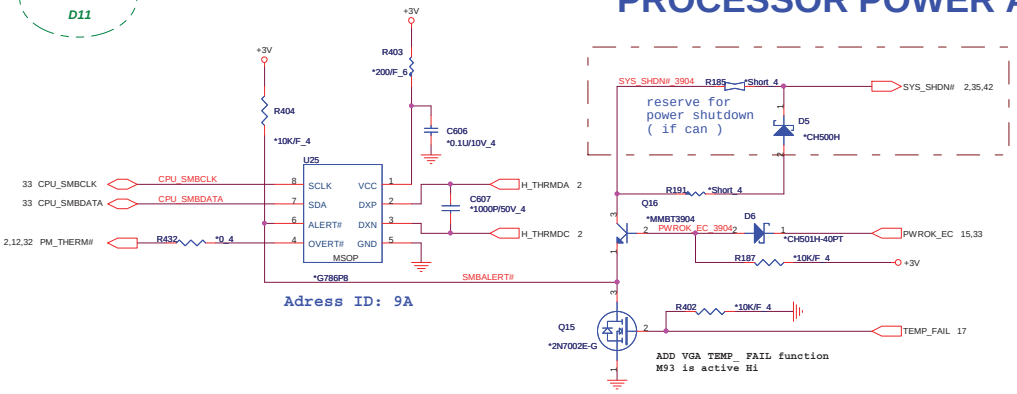




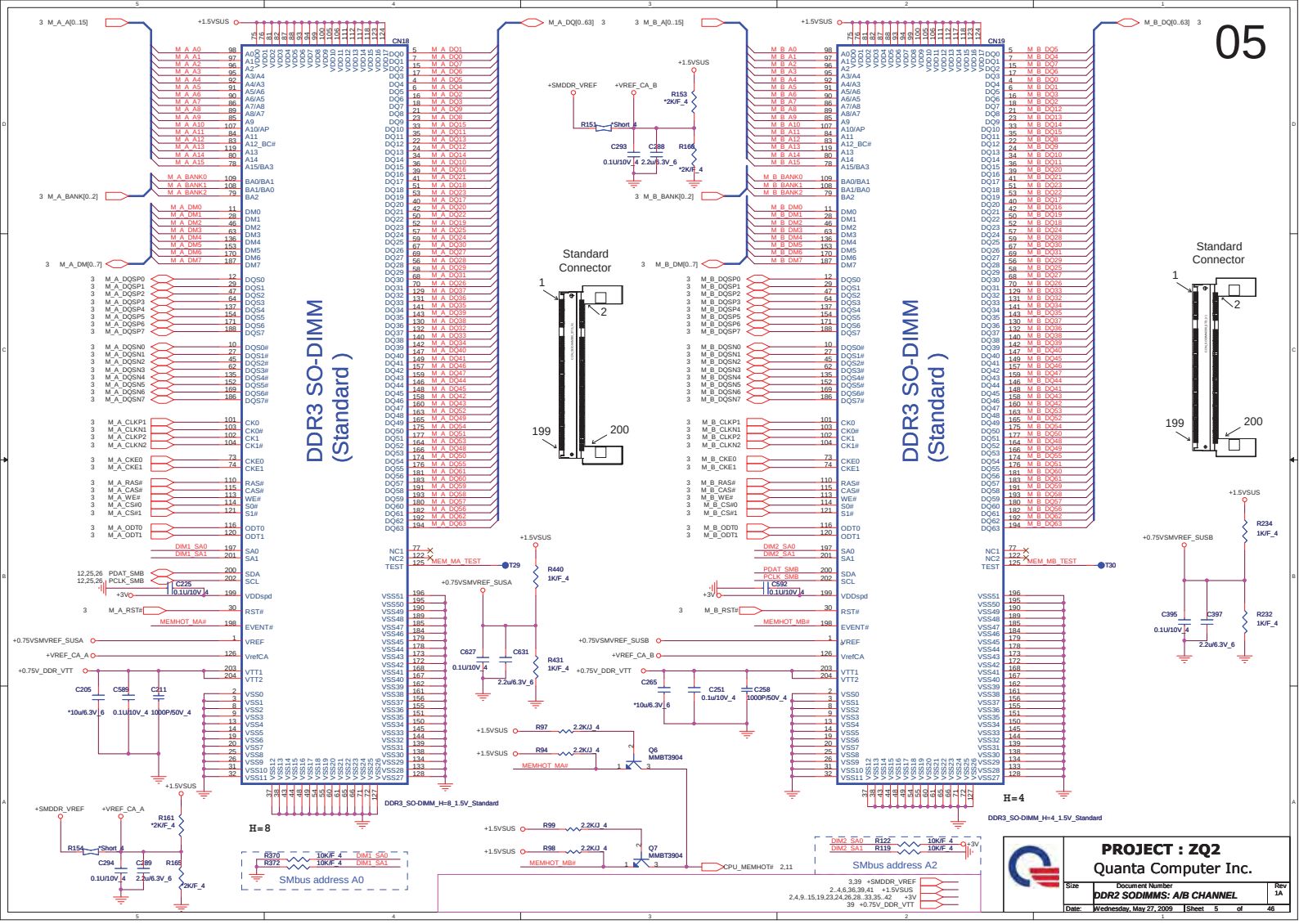




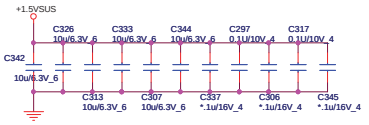




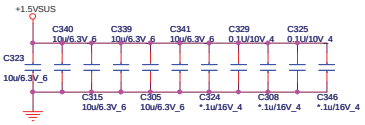
	PROJECT : ZQ2 Quanta Computer Inc.	
Size	Document Number *S1G4 PWR & GND 3/3*	Rev 1A
Date: Wednesday, May 27, 2009	Sheet 4 of 46	


05
DDR3 SO-DIMM (Standard)
CN18
CN19
Standard Connector
H=8
H=4
DDR3_SO-DIMM_H=8_1.5V_Standard
DDR3_SO-DIMM_H=4_1.5V_Standard
SMbus address A0
SMbus address A2
PROJECT : ZQ2
Quanta Computer Inc.
DDR2 SODIMMS: A/B CHANNEL
Wednesday, May 27, 2009
Sheet 5 of 46

Place these Caps near So-Dimm H=8.



Place these Caps near So-Dimm H=4.



	PROJECT : ZQ2 Quanta Computer Inc.	
Size	Document Number *DDR3 SODIMMS TERMINATIONS*	Rev 1A
Date: Wednesday, May 27, 2009	Sheet 6 of 46	

SIDE PORT

11/4

07

U22A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

RS880/RX881

signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

This block is for UMA only , Discrete can remove all component

U39

SPM_VREFCA
SPM_VREFDQ
SPM_A0 SPM_A1 SPM_A2 SPM_A3 SPM_A4 SPM_A5 SPM_A6 SPM_A7 SPM_A8 SPM_A9 SPM_A10 SPM_A11 SPM_A12 SPM_A13
SPM_BA0 SPM_BA1 SPM_BA2
SPM_CLKP SPM_CLKN SPM_CKE
SPM_ODT SPM_CS# SPM_RAS# SPM_CAS# SPM_WE#
SPM_DQS0P SPM_DQS1P
SPM_DM0 SPM_DM1
SPM_DQS0N SPM_DQS1N
SPM_DQ0 … SPM_DQ15

100-BALL SDRAM DDR3

SIDE@H5TQ1G63AFR-14C

U22D

PAR 4 OF 6

SBD_MEM / DVO_I / F

RS880/RX881

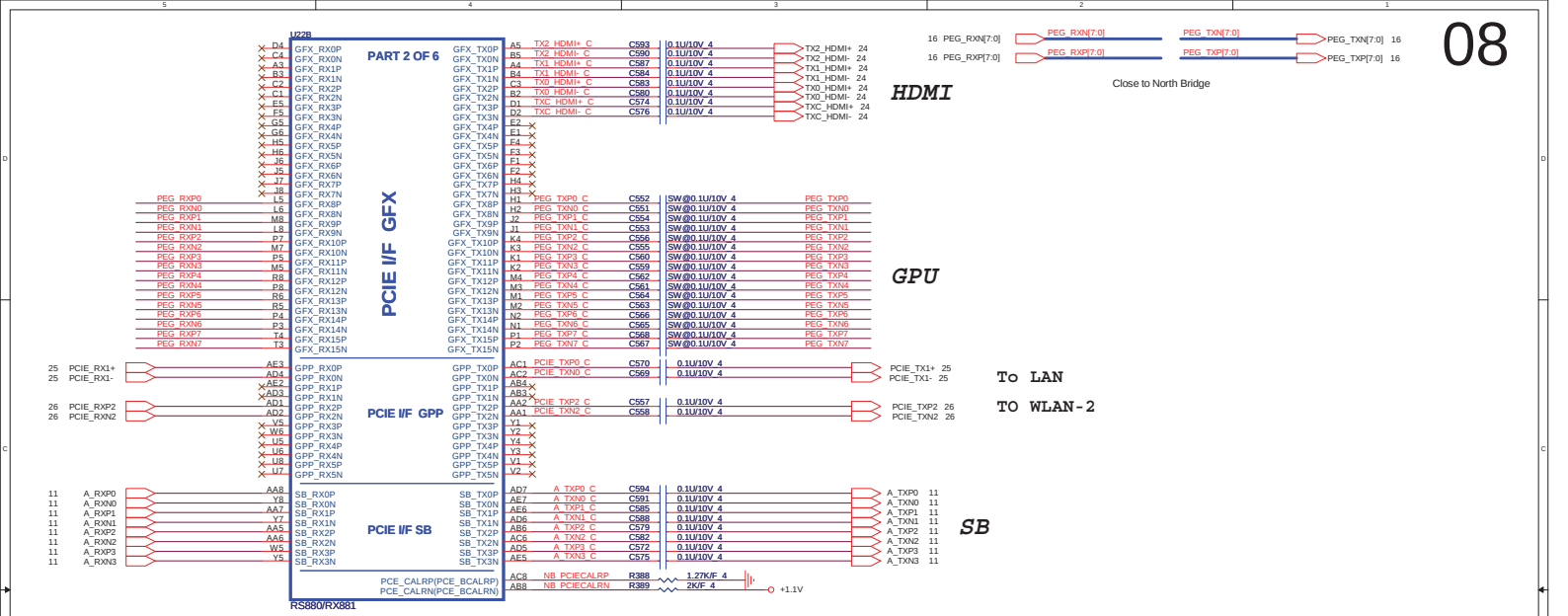
IOPLLVDD18 - memory PLL not applicable to RX881

40 mil~50 mil

	W/I SP	W/O SP
R583	1K	0
L75	Bead	0
L76	Bead	0

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-HT LINK I/F 1/4	1A
Date: Wednesday, May 27, 2009	Sheet 7 of 46	



RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

2,7,9,10,14,37 +1.1V

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-PCIE I/F 2/4	1A

Date: Wednesday, May 27, 2009 Sheet 8 of 46

For Check list JTAG

R130 *4.7K_4 NB_PWRGD_IN
R115 *4.7K_4 INT_EDIDDATA
R118 *4.7K_4 INT_EDIDCLK
R107 *4.7K_4 HDMI_DDC_DATA

All RS880 variants do not support analog TV-out functionality. As such, Y, C_Pr, and COMP_Pb

U2C — PART 3 OF 6 — RS880/RX881

CRT/TVOUT
- AVDD1(NC) F12
- AVDD2(NC) F14
- AVDDDI(NC) G15
- AVSSDI(NC) H15
- AVDDQ(NC) H14
- AVSSQ(NC) E17
- C_Pr(DFT_GPIO5) F17
- Y(DFT_GPIO2) F15
- COMP_Pb(DFT_GPIO4)
- REd(DFT_GPIO0) G18
- REDb(NC) G17
- GREEN(DFT_GPIO1) E18
- GREENb(NC) F18
- BLUE(DFT_GPIO3) E19
- BLUEb(NC) F19
- DAC_HSYNC(PWM_GPIO4) A11
- DAC_VSYNC(PWM_GPIO6) B11
- DAC_SDA(PCE_TCALRN) E8
- DAC_SCL(PCE_RCALRN) F8
- DAC_RSET(PWM_GPIO1) G14

PLL PWR
- PLLVDD(NC) A12
- PLLVDD18(NC) D14
- PLLVSS(NC) B12
- VDDA18HTPLL H17
- VDDA18PCIEPLL1 D7
- VDDA18PCIEPLL2 E7

PM LVTM
- SYSRESETb D8
- POWERGOOD A10
- LDTSTOPb C10
- ALLOW_LDTSTOP C12

CLOCKs
- HT_REFCLKP C25
- HT_REFCLKN C24
- REFCLK_P(OSCIN/OSCIN) E11
- REFCLK_N(PWM_GPIO3) F11
- GFX_REFCLKP T2
- GFX_REFCLKN T1
- GPP_REFCLKP U1
- GPP_REFCLKN U2
- GPPSB_REFCLKP(SB_REFCLKP) V4
- GPPSB_REFCLKN(SB_REFCLKN) V3

MIS.
- I2C_DATA A9
- I2C_CLK B9
- DDC_DATA/AUX0N(NC) B8
- DDC_CLK/AUX0P(NC) A8
- AUX1P(NC) B7
- AUX1N(NC) A7
- STRP_DATA B10
- RSVD G11
- AUX_CAL(NC) C8

TXOUT_L0P(NC) A22 — LA_DATAP0 23
TXOUT_L0N(NC) B22 — LA_DATAN0 23
TXOUT_L1P(NC) A21 — LA_DATAP1 23
TXOUT_L1N(NC) B21 — LA_DATAN1 23
TXOUT_L2P(NC) B20 — LA_DATAP2 23
TXOUT_L2N(DBG_GPIO0) A20 — LA_DATAN2 23
TXOUT_L3P(NC) A19
TXOUT_L3N(DBG_GPIO2) B19
TXOUT_U0P(NC) B18
TXOUT_U0N(NC) A18
TXOUT_U1P(PCIE_RESET_GPIO3) A17
TXOUT_U1N(PCIE_RESET_GPIO2) B17
TXOUT_U2P(NC) D20
TXOUT_U2N(NC) D21
TXOUT_U3P(PCIE_RESET_GPIO5) D18
TXOUT_U3N(NC) D19
TXCLK_LP(DBG_GPIO1) B16 — LA_CLK 23
TXCLK_LN(DBG_GPIO3) A16 — LA_CLK# 23
TXCLK_UP(PCIE_RESET_GPIO4) D16
TXCLK_UN(PCIE_RESET_GPIO1) D17

VDDLTP18(NC) A13 — +1.8V_VDDLTP18_NB — 15mA
VSSLTP18(NC) B13
VDDLT18_1(NC) A15 — +1.8V_VDDLT_18_NB — 300mA
VDDLT18_2(NC) B15
VDDLT33_1(NC) A14
VDDLT33_2(NC) B14
VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22

LVDS_DIGON(PCE_TCALRP) E9 — INT_LVDS_DIGON 23
LVDS_BLON(PCE_RCALRP) E7 — INT_DPST_PWM 23
LVDS_ENA_BL(PWM_GPIO2) G12 — INT_LVDS_BLON 23

TMDS_HPD(NC) D9 — INT_HDMI_HPD 24
HPD(NC) D10
TVCLKIN(PWM_GPIO5) D12 — SUS_STAT# NB — R79 *Short_4 — SUS_STAT# 12
THERMALDIODE_P AE8
THERMALDIODE_N AD8
TESTMODE D13 — TEST_EN — R137 1.8K/F_4
R80 *3K/J_4

VGA
23 INT_CRT_RED — R394 140/F_4 — G18
23 INT_CRT_GRE — R395 150/F_4 — G17
23 INT_CRT_BLU — R396 150/F_4 — E18
23 INT_CRT_HSYNC — INT_CRT_HSYNC — A11
23 INT_CRT_VSYNC — INT_CRT_VSYNC — B11
23 INT_DDCDATA — E8
23 INT_DDCCLK — F8
R140 715/F_6 — DAC_RSET_NB — G14

20mA +1.8V_VDDA18HTPLL
120mA +1.8V_VDDA18PCIEPLL
+1.1V_PLLVDD
+1.8V_PLLVDD18
11,33 A_RST#_SB
12,15 NB_PWRGD_IN — NB_LDT_STOP#
NB_ALLOW_LDTSTOP
11 CLK_NB_HTREFP_PR
11 CLK_NB_HTREFN_PR
11 CLK_NB_REF_CLKP — CLK_NB_REF_CLKP
11 CLK_NB_REF_CLKN — CLK_NB_REF_CLKN
R101 4.7K_4 — NBGFX_CLKP
R96 4.7K_4 — NBGFX_CLKN
T73 — GPP_REFCLKP
T72 — GPP_REFCLKN
11 CLK_SBLINKP
11 CLK_SBLINKN
23 INT_EDIDDATA
23 INT_EDIDCLK
24 HDMI_DDC_DATA
24 HDMI_DDC_CLK
DDC_DATA & DDC_CLK Not applicable to RX881
38 +NB_CORE_ON — +NB_CORE_ON
T74 — RS880_AUX_CAL

For A11 version
B18
R108 *SP@49.9/F_4 CLK_SBLINKP
R105 *SP@49.9/F_4 CLK_SBLINKN

2,7,8,10,14,37 +1.1V
7,10,15,31,36,41,42 +1.8V
2,4,5,10..15,19,23,24,26,28..33,35..42 +3V

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M
1 Disable V
0 Enable

INT_CRT_VSYNC — R391 3K_4 — +3V

RS880M: Enables Side port memory

RS880M:INT_CRT_HSYNC

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG.CLK_TOP_SPARE_D[1]

INT_CRT_HSYNC — for B — R392 *SP@3K_4 — R393 SIDE@3K_4 — +3V

For extrnal EEPROM Debug only

RS780/RX780/RS880

+NB_CORE_ON — R390 2K/F_4

Display Port interface from PCIeGraphics (RS880/rs880M only)

RS880_AUX_CAL — R387 *150/F_4

Check----> no need DP

RS880M --- ADD

L19 BLM18PG221SN1D(220_1.4A)_6 — +3V_AVDD_NB
C208 2.2U/6.3V_6
C539 1u/6.3V_4
AVDD-DAC Analog not applicable to RX780

L63 BLM18PG221SN1D(220_1.4A)_6 — +1.1V_PLLVDD
C600 2.2U/6.3V_6
PLLVDD - Graphics PLL not applicable to RX780

L25 BLM18PG221SN1D(220_1.4A)_6 — +1.8V_VDDLTP18_NB
C242 2.2U/6.3V_6
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

R148 *Short_6 — +1.8V_AVDDDI_NB
C278 0.1U/10V_4
AVDDI-DAC Digital not applicable to RX780

L18 BLM18PG221SN1D(220_1.4A)_6 — +1.8V_AVDDQ_NB
C209 2.2U/6.3V_6
AVDDQ-DAC Bandgap Reference not applicable to RX780

L27 BLM18PG221SN1D(220_1.4A)_6 — +1.8V_PLLVDD18
C250 *10U/6.3V_8
C248 4.7U/6.3V_6
PLLVDD18 - Graphics PLL not applicable to RX780

BLM21PG221SN1D(220,100M,2A)_8 — +1.8V_VDDLT_18_NB
L30
C268 4.7U/6.3V_6
C266 0.1U/10V_4
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

VDDA18PCIEPLL -PCIE PLL — 20mils width
L23 BLM18PG221SN1D_6 — +1.8V_VDDA18PCIEPLL
C228 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL — 20mils width
L28 BLM18PG221SN1D_6 — +1.8V_VDDA18HTPLL
C260 2.2U/6.3V_6

2,11 CPU_LDT_STOP# — U5 74LVC07 (Open Drain) — R81 2.2K/J_4 — NB_LDT_STOP#

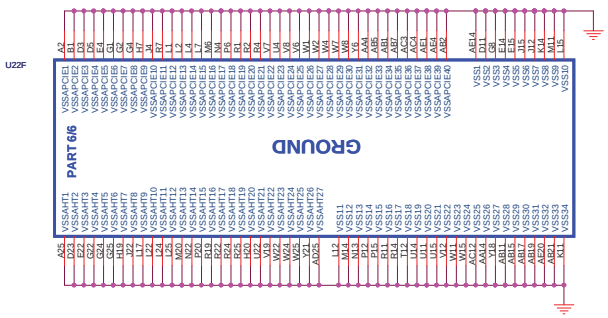
0n3 based CPU : Level shifted to 1.8 V on the Northbridge side using an open-drain buffer and pulled up to 1.8V_S0 through a 2.2k Ohm 5% resistor on the Northbridge side.

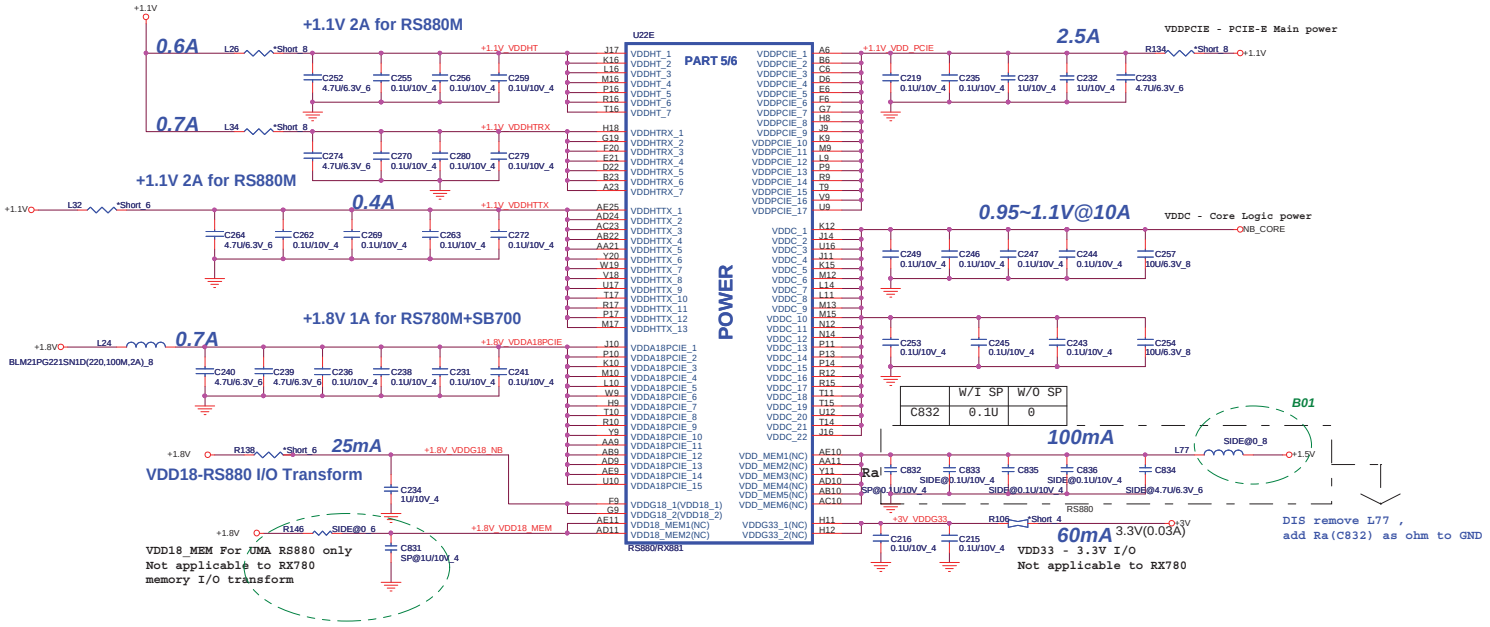
2 CPU_LDT_REQ# — R123 *0_4 — for B — R129 *Short_4 — R132 1K/F_4 — NB_ALLOW_LDTSTOP
11 ALLOW_LDTSTOP

The RS880 family does not support CLMC architecture The LDTREQ# connection from the CPU to ALLOW_LDTSTOP of the Northbridge is no longer required.

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-SYSTEM I/F 3/4	1A
Date: Wednesday, May 27, 2009	Sheet 9 of 46	



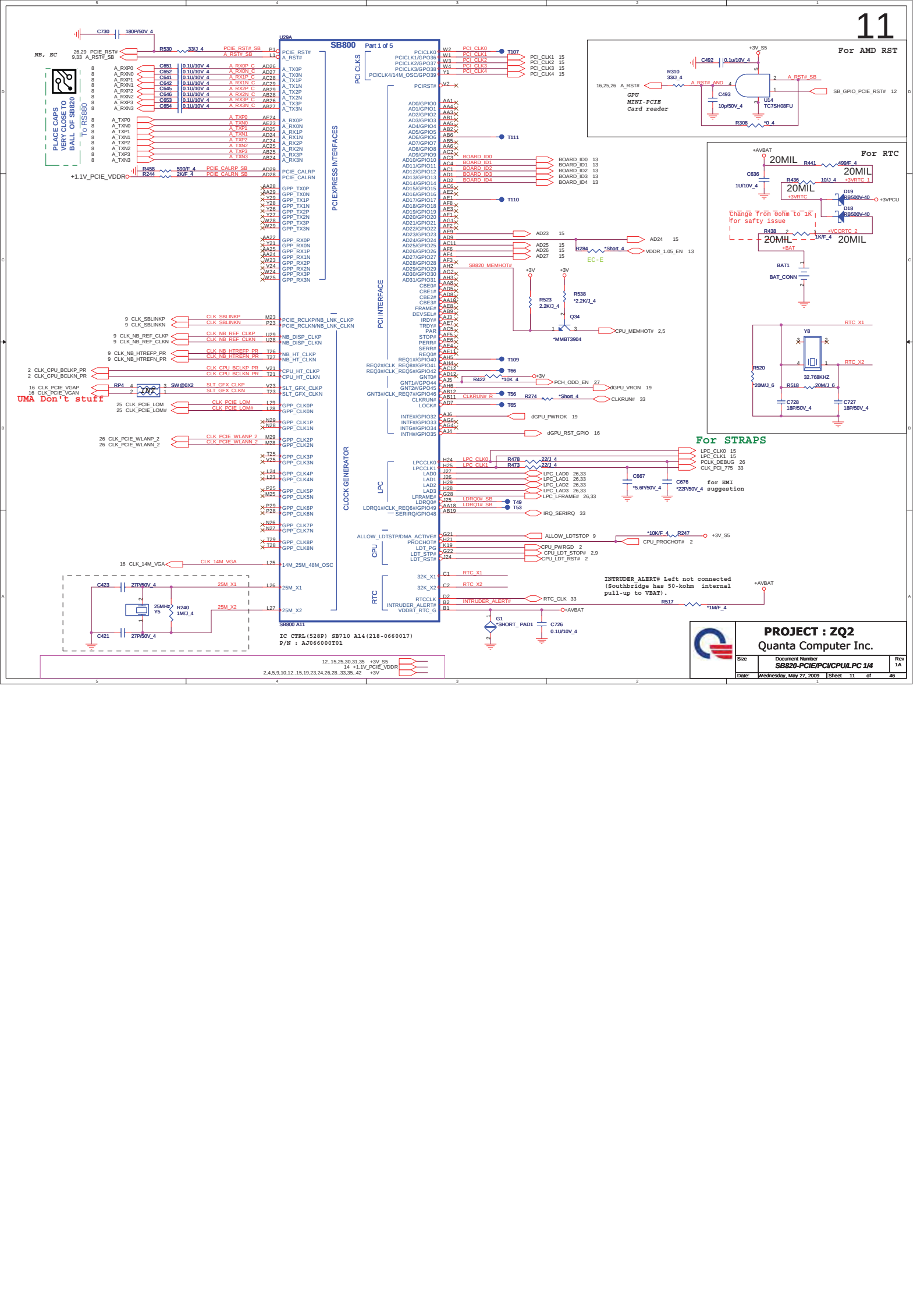


	W/I SP	W/O SP
C832	0.1U	0

31,38	NB_CORE
2,7,9,14,37	+1.1V
7,9,15,31,36,41,42	+1.8V
2,4,5,9,11..15,19,23,24,26,28..33,35..42	+3V

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-POWER4/4	1A
Date: Wednesday, May 27, 2009	Sheet 10 of 46	


SB800
Part 1 of 5
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
PCI CLKS
NB, EC
PLACE CAPS VERY CLOSE TO BALL OF SB820
To RS880
UMA Don't stuff
For AMD RST
GPU MINI-PCIE Card reader
For RTC
Change from 0ohm to 1K for safty issue
For STRAPS
for EMI suggestion
EC-E
INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).
IC CTRL(528P) SB710 A14(218-0660017)
P/N : AJ066000T01
PROJECT : ZQ2
Quanta Computer Inc.
SB820-PCIE/PCI/CPU/LPC 1/4
Wednesday, May 27, 2009
Sheet 11 of 46

NC only ,Can't be install

+3V_S5 R514 *2.2K/J_4 SB_TEST0
R313 *2.2K/J_4 SB_TEST1
R305 *2.2K/J_4 SB_TEST2

11,13..15,25,30,31,35 +3V_S5
2,4,5,9..11,13..15,19,23,24,26,28..33,35..42 +3V

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

+3V R249 2.2K/J_4 PCLK_SMB
R246 2.2K/J_4 PDAT_SMB
SCL0/SDATA0 is 3V tolerance AMD datasheet define it
Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

+3V_S5 SCL1/SDATA1 is 3V/S5 tolerance AMD datasheet define it
R287 10K_4 SB_SMBCLK1
R306 10K_4 SB_SMBDATA1

+3V_S5 SCL2/SDATA2 is 3V/S5 tolerance AMD datasheet define it
R252 10K_4 SB_SCLK2
R248 10K_4 SB_SDATA2

+3V R296 4.7K/J_4 SUS_STAT#

U29D

SB800 Part 4 of 5

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMLS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS
USB 1.1 USB MISC

T69 SUSB# SUSC# SB_TEST0 SB_TEST1 SB_TEST2
SIO_A20GATE SIO_RCIN# LANLINK_STATE#
T105 SIO_EXT_SMI# SIO_EXT_SCI#
T108 SYS_RST#
PCIE_WAKE# IR_RX1
T106 R295 *Short_4 SB_THERMTRIP#
NB_PWRGD_IN
ICH_RSMRST#

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_14_48M T83
USB_RCOMP_SB R270 11.8K/F_6

USB_FSD1P/GPIO186 USB_FSD1N
USB_FSD0P/GPIO185 USB_FSD0N
USB_FSD12P T62
USB_FSD12N T58

USB_HSD13P USB_HSD13N
USB_HSD12P USB_HSD12N
USB_HSD11P USB_HSD11N
USB_HSD10P USB_HSD10N
USB_HSD9P USB_HSD9N
USB_HSD8P USB_HSD8N
USB_HSD7P USB_HSD7N
USB_HSD6P USB_HSD6N
USB_HSD5P USB_HSD5N
USB_HSD4P USB_HSD4N
USB_HSD3P USB_HSD3N
USB_HSD2P USB_HSD2N
USB_HSD1P USB_HSD1N
USB_HSD0P USB_HSD0N

USBP13+ USBP13- CAMERA EC-C
USBP12+ USBP12- USBX3 board
USBP11+ USBP11- USBX3 board
USBP10+ USBP10- Card reader EC-C
USBP9+ USBP9- BLUETOOTH
USBP8+ USBP8- USBX3 board EC-C
USBP4+ USBP4- WLAN Min-Card
USBP0+ USBP0- On Board USB Connector

Only USB Port0 can be configured as debug port.

USB 2.0
GPIO
USB OC

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN

11 SB_GPIO_PCIE_RST# SB_GPIO_PCIE_RST#
25 CLK_PCIE_LAN_REQ#
19 dGPU_PWR_EN
T51 SB_GPIO59
28 SPKR
5,25,26 PCLK_SMB PCLK_SMB
5,25,26 PDAT_SMB PDAT_SMB
SB_SMBCLK1
SB_SMBDATA1
26 CLK_PCIE_2_REQ# R427 *Short_4 A_REQ#_GPIO61
17 VGA_REQ#
EC-E
7 SP_DDR3_RST#

11/04 need check
T118 E_SB_OSC

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#

30 OC_7#
30 OC_6#
2,4,32 PM_THERM#
30 OC_4#
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

HD audio interface is +3VS5 voltage

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

HD AUDIO

15 ACZ_SDOUT R533 *10K_4 ACZ_BCLK
ACZ_SDOUT
R535 *10K_4 ACZ_SDIN0
R294 *10K_4 ACZ_SDIN1
R304 *10K_4 ACZ_SDIN2
R292 *10K_4 ACZ_SDIN3
ACZ_SYNC
ACZ_RST#

SCL2/GPIO193 D25 SB_SCLK2
SDA2/GPIO194 F23 SB_SDATA2
SCL3_LV/GPIO195 B26 SB_GPIO195
SDA3_LV/GPIO196 E26 SB_GPIO196
EC_PWM0/EC_TIMER0/GPIO197 F25 T122
EC_PWM1/EC_TIMER1/GPIO198 F22
EC_PWM2/EC_TIMER2/GPIO199 F22 GPIO199 15
EC_PWM3/EC_TIMER3/GPIO200 E21 GPIO200 15

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D29
KSI_5/GPIO206 D28
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28

KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22

EMBEDDED CTRL

+3V B05
R501 8.2K_4 CLK_PCIE_LAN_REQ#
R551 8.2K_4 CLK_PCIE_2_REQ#

+3V_S5 D03
R301 10K_4 GBE_COL
R291 10K_4 GBE_CRS
R293 10K_4 GBE_MDIO
R300 10K_4 GBE_RXERR
R290 10K_4 GBE_PHY_INTR

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR

GBE LAN

T50 ADP_PRES0

PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPIO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

EMBEDDED CTRL

SB800 A11

To Azalia

ACZ_SDOUT R532 33/J_4 ACZ_SDOUT_AUDIO 28
C732 *10P/50V_4
ACZ_SYNC R531 33/J_4 ACZ_SYNC_AUDIO 28
C731 *10P/50V_4
ACZ_BCLK R534 33/J_4 ACZ_BITCLK_AUDIO 28
C733 *10P/50V_4
ACZ_RST# R529 33/J_4 ACZ_RST#_AUDIO 28
ACZ_SDIN0 ACZ_SDIN0 28

+3V_S5 CN12 C485 10P/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG
JTAG DEBUG

Check list
SB_GPIO195 R245 10K/F_4
SB_GPIO196 R243 10K/F_4

PROJECT : ZQ2
Quanta Computer Inc.

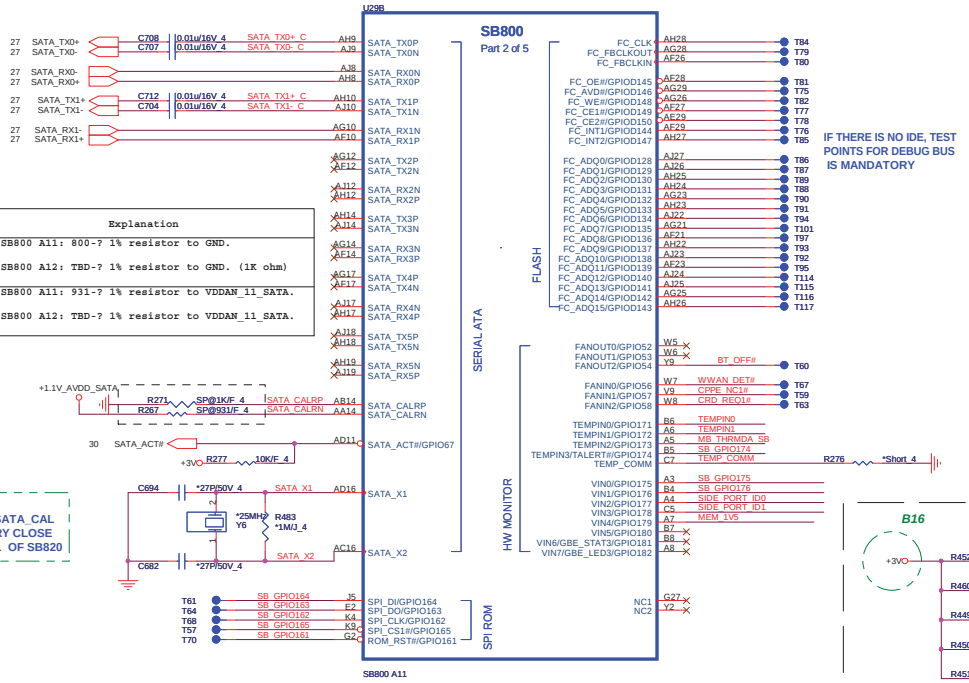
Size	Document Number	Rev
	SB820-ACPI/GPIO/USB 2/4	1A

Date: Wednesday, May 27, 2009 Sheet 12 of 46

SATA PORT 0,1,2,3 can support AHCI mode

SATA HDD

SATA ODD



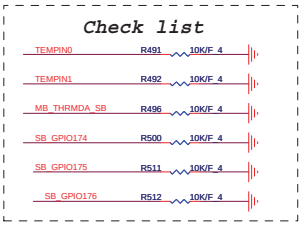
Signal Name	Explanation
SATA_CALRP	SB800 A11: 800-? 1% resistor to GND. SB800 A12: TBD-? 1% resistor to GND. (1K ohm)
SATA_CALRN	SB800 A11: 931-? 1% resistor to VDDAN_11_SATA. SB800 A12: TBD-? 1% resistor to VDDAN_11_SATA.

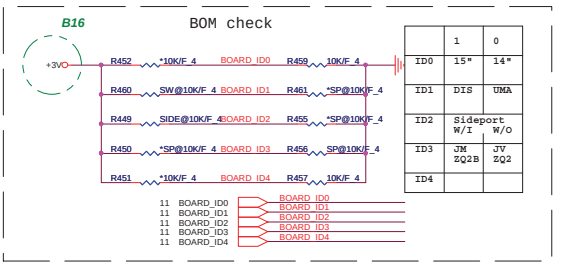
E-SATA

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820

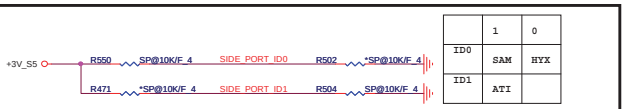
IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

Check list





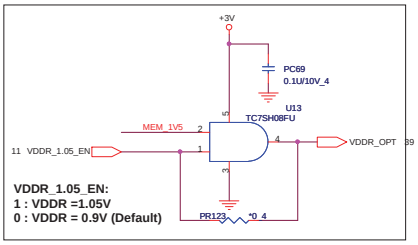
	1	0
ID0	15"	14"
ID1	DIS	UMA
ID2	Sideport W/I	Sideport W/O
ID3	JM ZQ2B	JV ZQ2
ID4		



	1	0
ID0	SAM	HYX
ID1	ATI	

DDR3 Sideport Memory Device

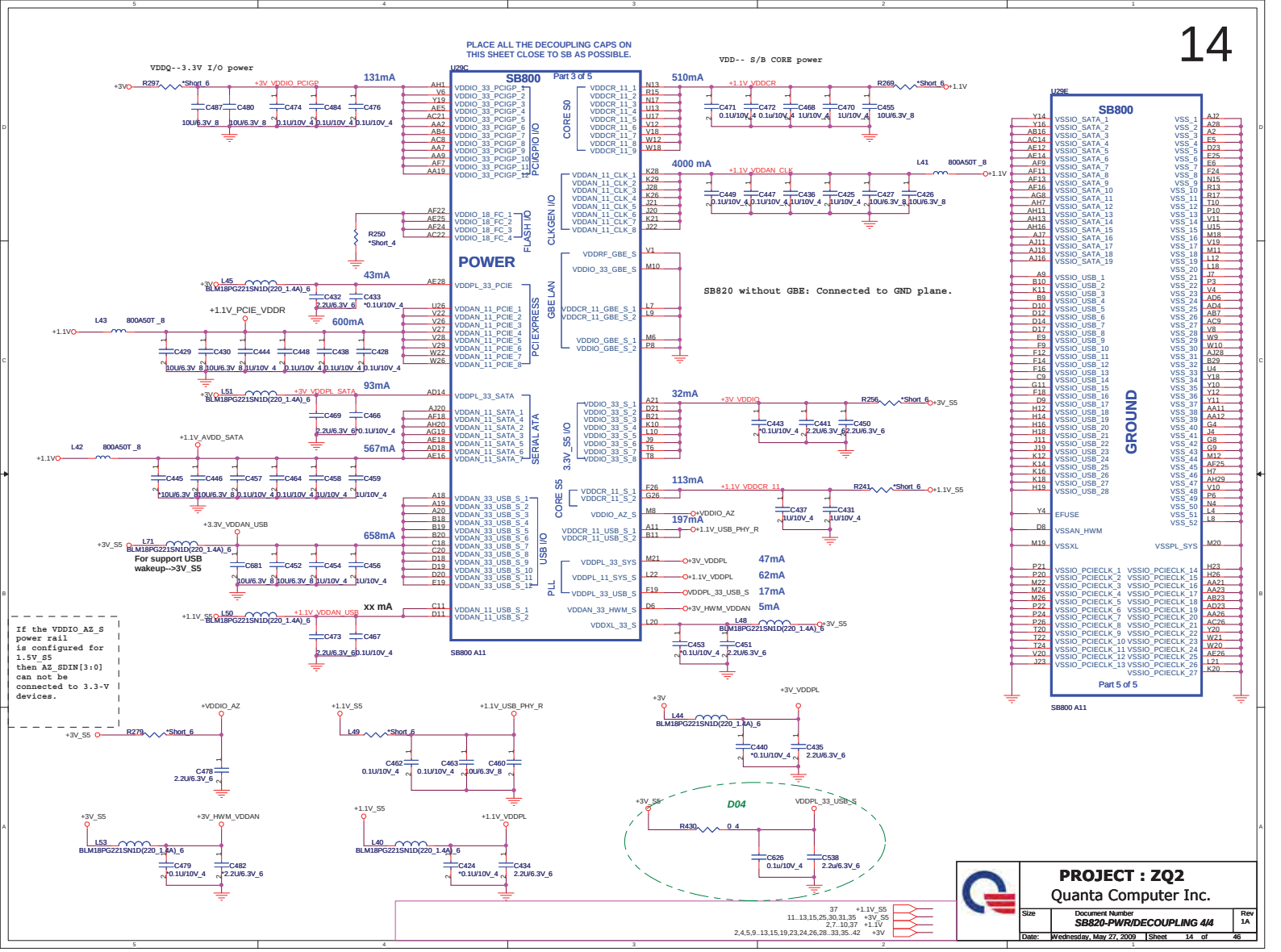
Vendor	Vendor P/N	STN B/S P/N	BOARD_ID2 GPIO12	SIDE_PORT_ID1 GPIO178	SIDE_PORT_ID0 GPIO177
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	0 (WO/Sideport)	0	0
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1 (W/Sideport)	0	1
ATI	23EY2387MA12-SZ	AKD5LGGT700 (64M*16)	1 (W/Sideport)	1	0



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-SATA/IDE/SPI 3/4	1A

Date: Wednesday, May 27, 2009 Sheet 13 of 46

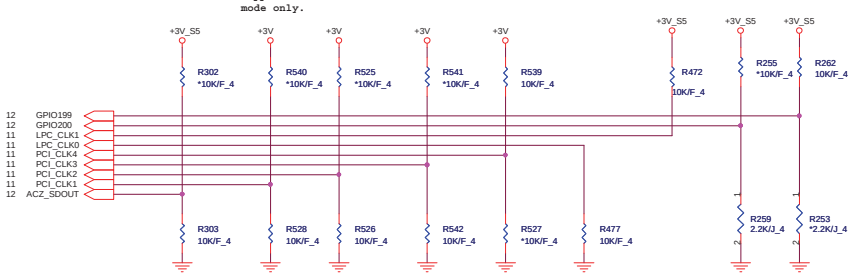

14
PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.
VDDQ--3.3V I/O power
VDD-- S/B CORE power
SB800
Part 3 of 5
POWER
SB800 A11
SB820 without GBE: Connected to GND plane.
GROUND
Part 5 of 5
131mA
510mA
4000 mA
43mA
600mA
93mA
567mA
32mA
113mA
197mA
658mA
xx mA
47mA
62mA
17mA
5mA
D04
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.
For support USB wakeup-->3V_S5
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
SB820-PWR/DECOUPLING 4/4
Rev
1A
Date: Wednesday, May 27, 2009
Sheet 14 of 46

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

SB820M is supported Gen1 mode only.

For internal clock GEN.



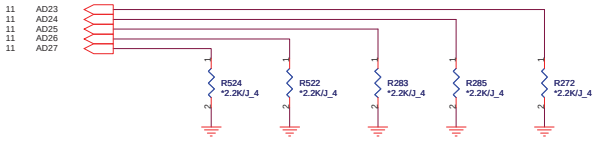
11..14,25,30,31,35 +3V_S5
7,9,10,31,36,41,42 +1.8V
2,4,5,9..14,19,23,24,26,28..33,35..42 +3V

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
D02								
PULL HIGH	This is required as the low power mode is not supported on the SB8xx	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM DEFAULT L, L=FWH ROM

internal have pull Hi 10K

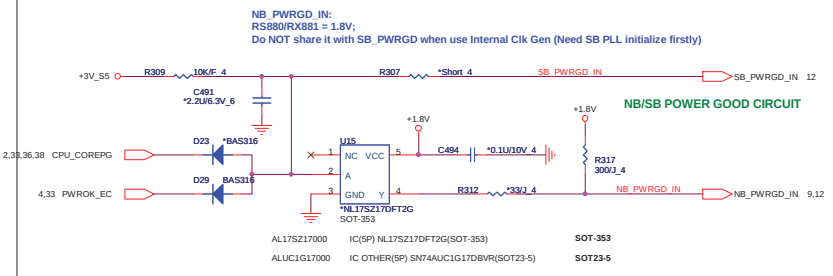
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

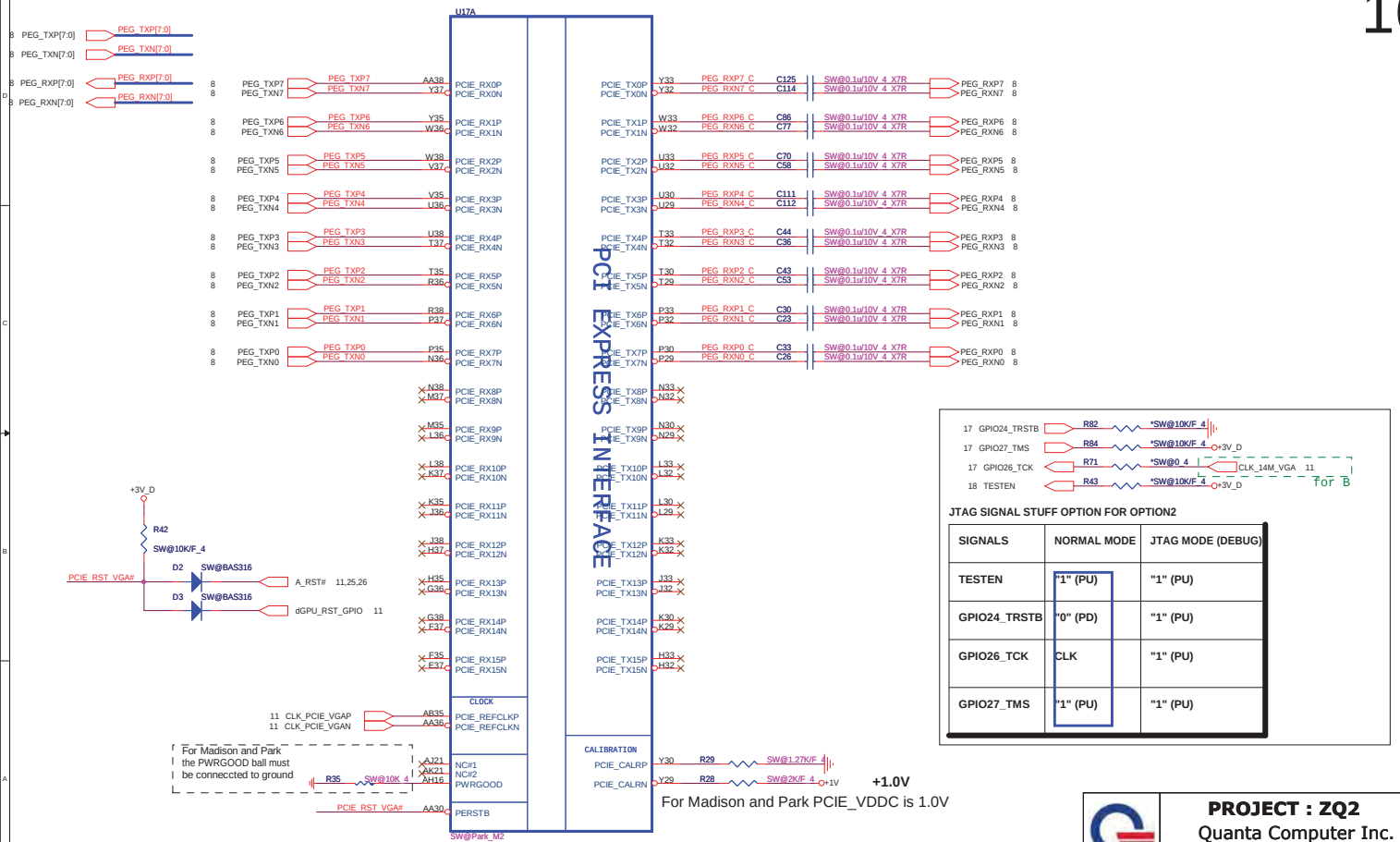


AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-STRAPS	1A

Date: Wednesday, May 27, 2009 Sheet 15 of 46



JTAG SIGNAL STUFF OPTION FOR OPTION2

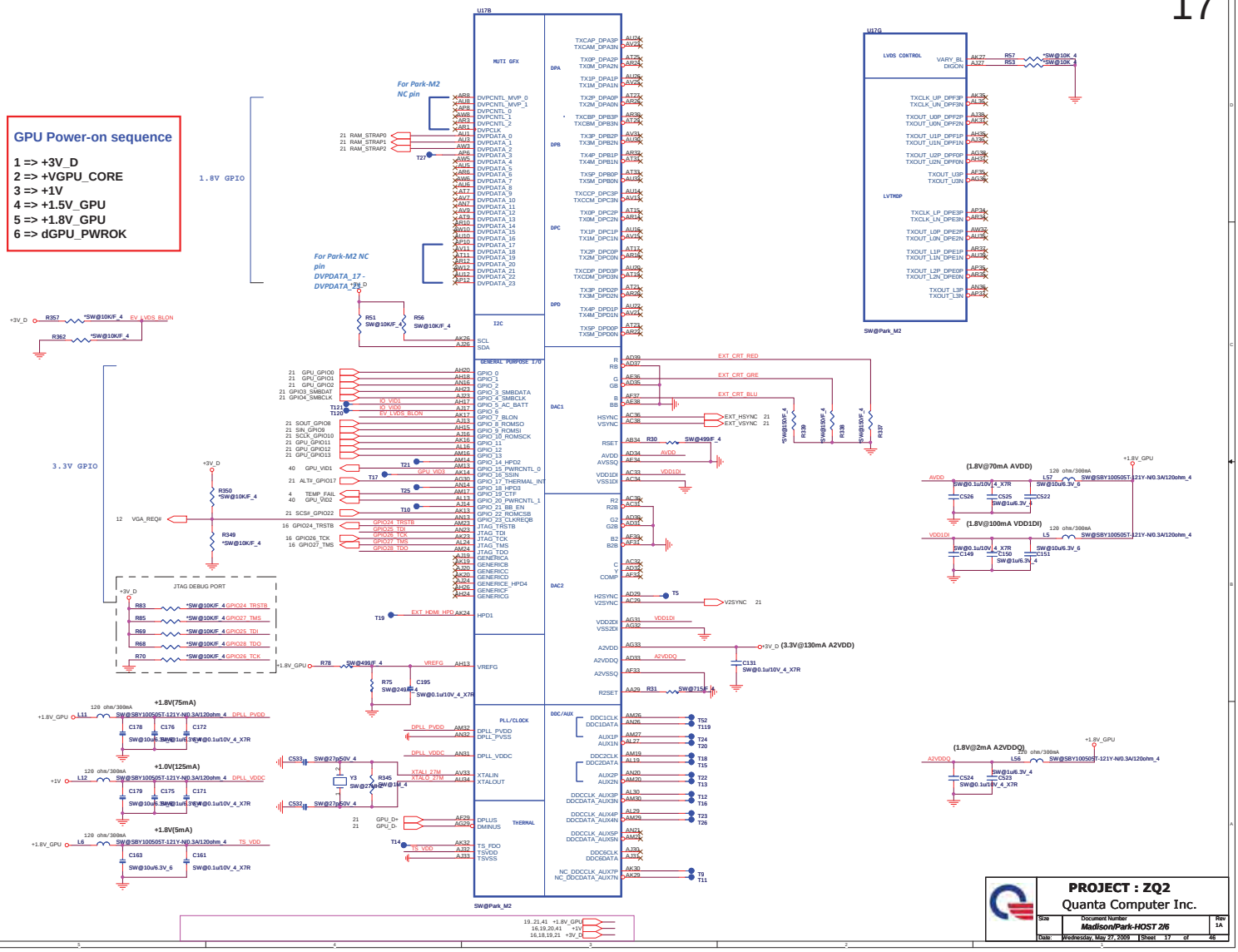
SIGNALS	NORMAL MODE	JTAG MODE (DEBUG)
TESTEN	"1" (PU)	"1" (PU)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)

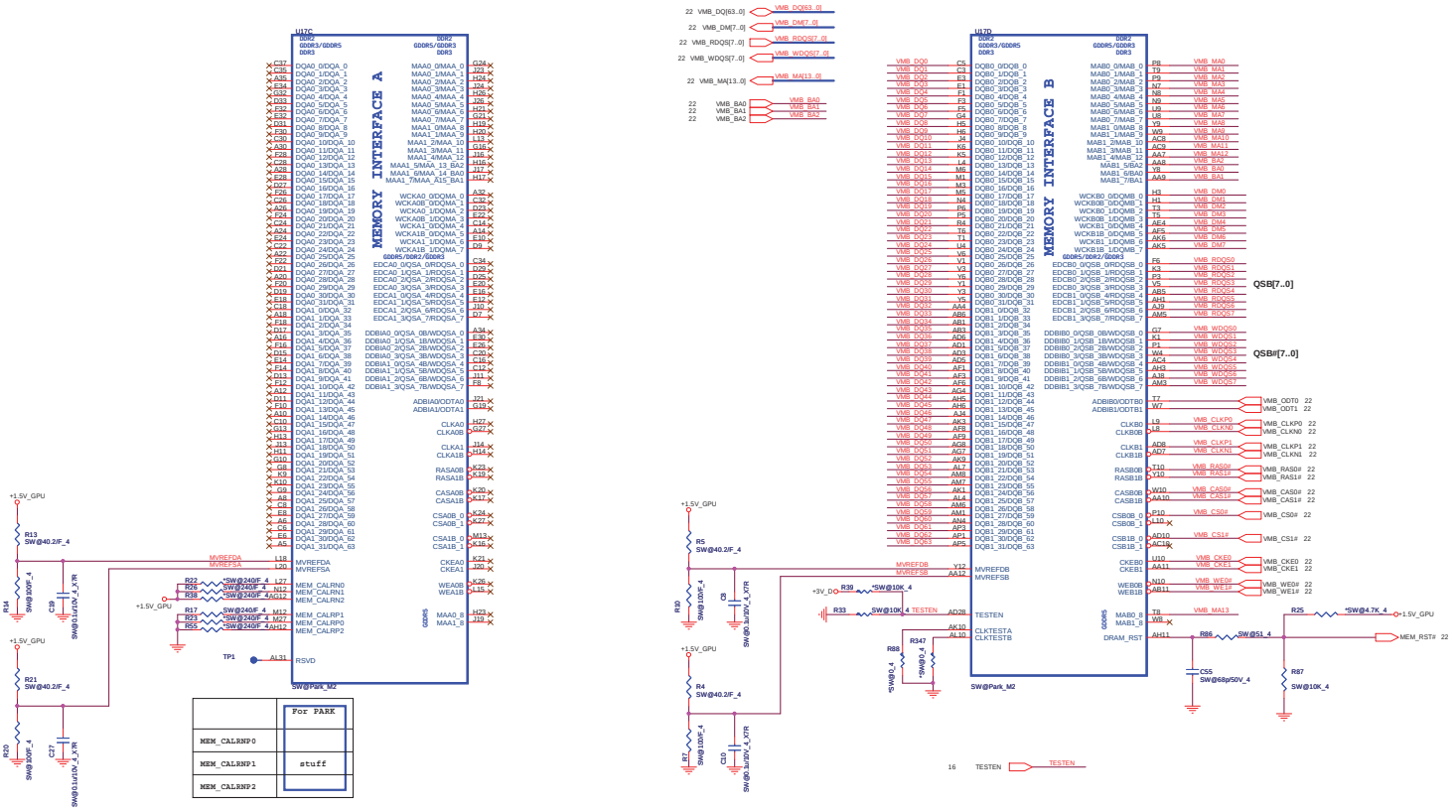
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Madison/Park-PCIE 1/6	1A
Date: Wednesday, May 27, 2009	Sheet 16 of 46	

GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +1V
4 => +1.5V_GPU
5 => +1.8V_GPU
6 => dGPU_PWROK





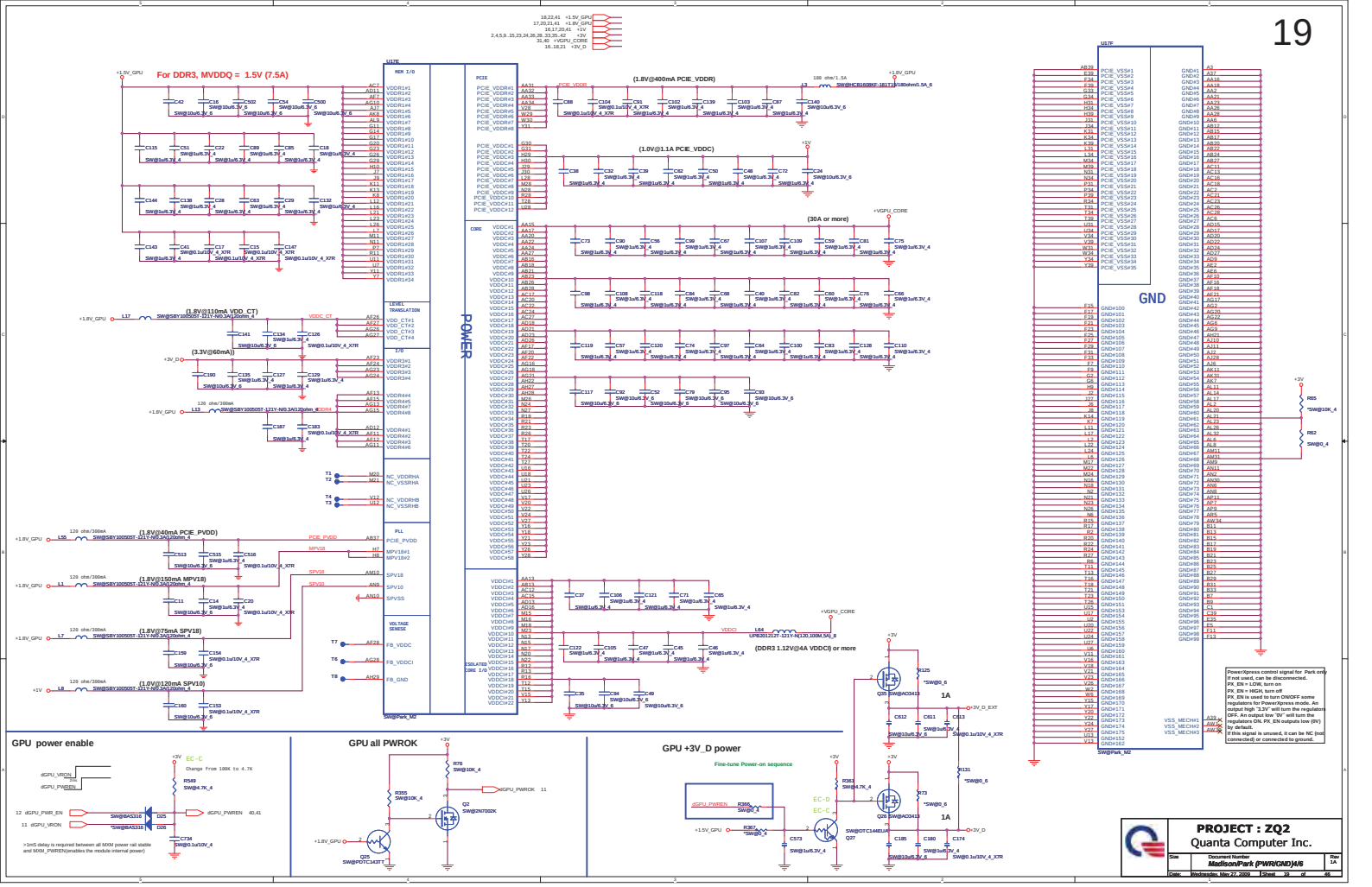
	For PARK
MEM_CALRNP0	
MEM_CALRNP1	stuff
MEM_CALRNP2	

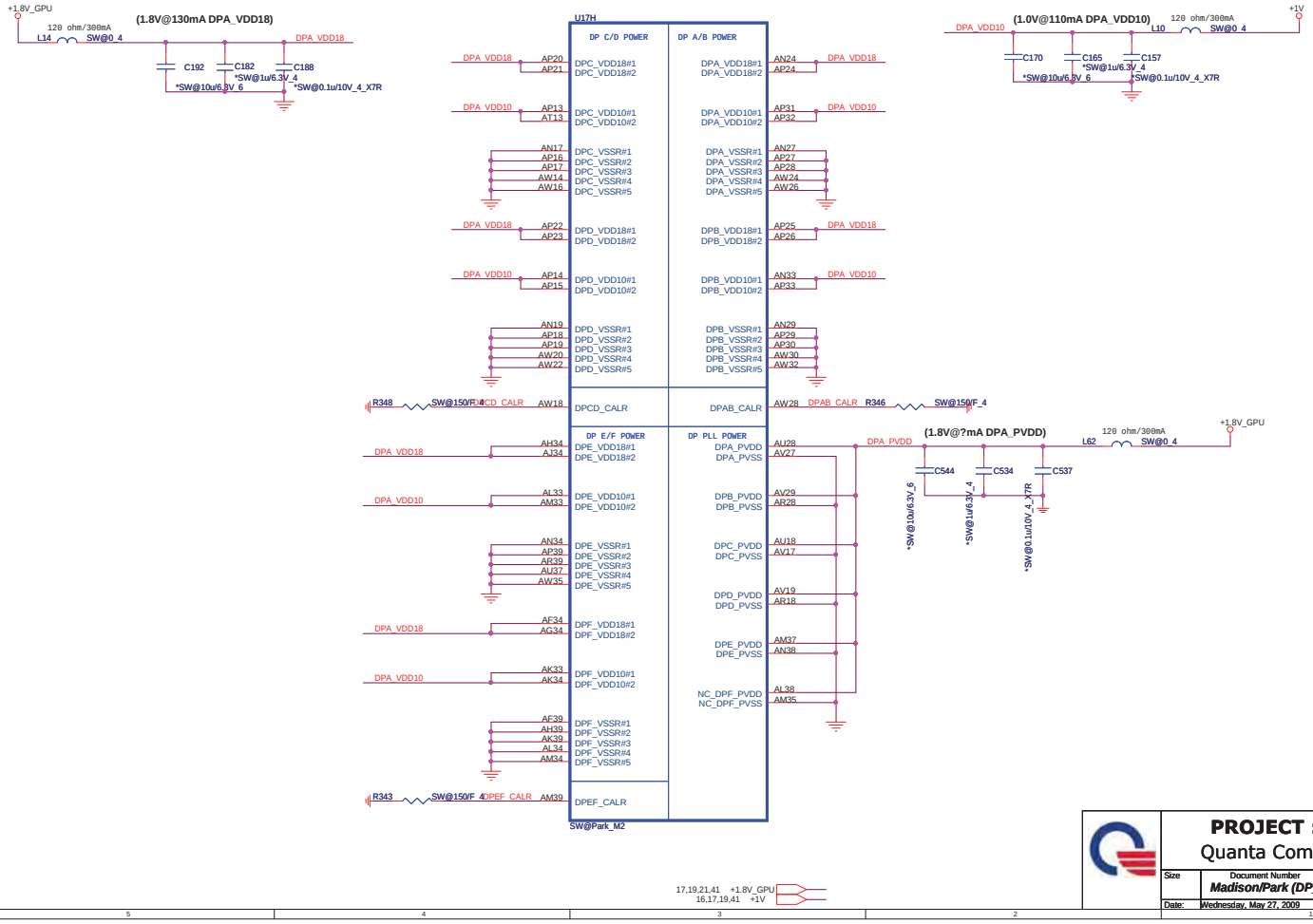
DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

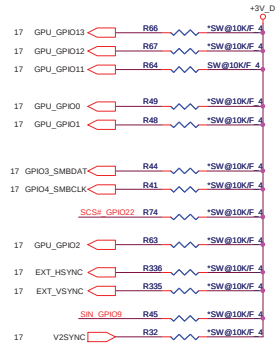
Designator	For M97-M2	For Mannhatton
Ra	10K	10K
Rb	0R/Short	680R
Rc	DNI	DNI
Ca	2.2nF	68pF

PROJECT : ZQ2			
Quanta Computer Inc.			
Size	Document Number		Rev 1A
	Madison/Park-MEM 3/6		
Date: Wednesday, May 27, 2009	Sheet 18	of	46


For DDR3, MVDDQ = 1.5V (7.5A)
(1.8V@400mA PCIE_VDDR)
(1.0V@1.1A PCIE_VDDC)
(30A or more)
(1.8V@110mA VDD_CT)
(3.3V@60mA))
(1.8V@40mA PCIE_PVDD)
(1.8V@150mA MPV18)
(1.8V@75mA SPV18)
(1.0V@120mA SPV10)
(DDR3 1.12V@4A VDDCI) or more
POWER
GND
GPU power enable
GPU all PWROK
GPU +3V_D power
Fine-tune Power-on sequence
PROJECT : ZQ2
Quanta Computer Inc.
Madison/Park (PWR/GND)4/6


+1.8V_GPU
120 ohm/300mA
L14
SW@0_4
(1.8V@130mA DPA_VDD18)
DPA_VDD18
C192
C182
*SW@1u/6.3V_4
C188
*SW@10u/6.3V_6
*SW@0.1u/10V_4_X7R
U17H
DP C/D POWER
DP A/B POWER
DPC_VDD18#1
DPC_VDD18#2
DPA_VDD18#1
DPA_VDD18#2
DPC_VDD10#1
DPC_VDD10#2
DPA_VDD10#1
DPA_VDD10#2
DPC_VSSR#1
DPC_VSSR#2
DPC_VSSR#3
DPC_VSSR#4
DPC_VSSR#5
DPA_VSSR#1
DPA_VSSR#2
DPA_VSSR#3
DPA_VSSR#4
DPA_VSSR#5
DPD_VDD18#1
DPD_VDD18#2
DPB_VDD18#1
DPB_VDD18#2
DPD_VDD10#1
DPD_VDD10#2
DPB_VDD10#1
DPB_VDD10#2
DPD_VSSR#1
DPD_VSSR#2
DPD_VSSR#3
DPD_VSSR#4
DPD_VSSR#5
DPB_VSSR#1
DPB_VSSR#2
DPB_VSSR#3
DPB_VSSR#4
DPB_VSSR#5
DPCD_CALR
DPAB_CALR
R348
SW@150/F_4
R346
DP E/F POWER
DP PLL POWER
DPE_VDD18#1
DPE_VDD18#2
DPA_PVDD
DPA_PVSS
DPE_VDD10#1
DPE_VDD10#2
DPB_PVDD
DPB_PVSS
DPE_VSSR#1
DPE_VSSR#2
DPE_VSSR#3
DPE_VSSR#4
DPE_VSSR#5
DPC_PVDD
DPC_PVSS
DPD_PVDD
DPD_PVSS
DPF_VDD18#1
DPF_VDD18#2
DPE_PVDD
DPE_PVSS
DPF_VDD10#1
DPF_VDD10#2
NC_DPF_PVDD
NC_DPF_PVSS
DPF_VSSR#1
DPF_VSSR#2
DPF_VSSR#3
DPF_VSSR#4
DPF_VSSR#5
DPEF_CALR
R343
SW@150/F_4
SW@Park_M2
(1.0V@110mA DPA_VDD10)
+1V
L10
C170
C165
C157
(1.8V@?mA DPA_PVDD)
L62
C544
C534
C537
17,19,21,41 +1.8V_GPU
16,17,19,41 +1V
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
Madison/Park (DP_PWR/GND)5/6
Rev 1A
Date: Wednesday, May 27, 2009
Sheet 20 of 46

PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

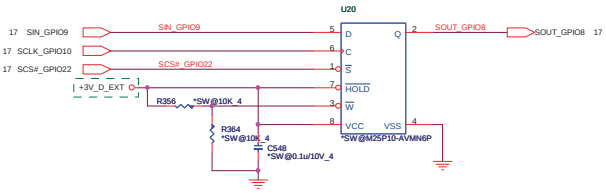
ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

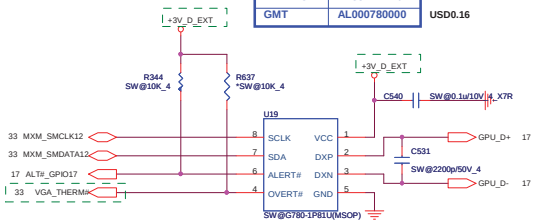
EEPROM



Thermal Sensor

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16



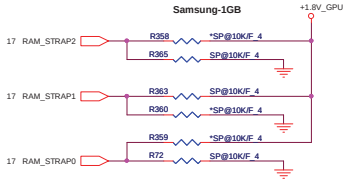
Address ID: 98H

DDR3 Memory Aperture size

DDR3 Memory Aperture size

Vendor	Vendor P/N	STN B/S P/N	GPU	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	Park	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	Madison	1	0	0
			2Gb	1	1	1
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	Park	0	1	0
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	Madison	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2Gb	0	0	1
AMD	23EY2387MA12-SZ	AKD5LGGT700	Park	0	1	1
	23EY2387MA12-SZ	AKD5LGGT700	Madison	1	0	1

D09



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Medison/Park Strip/Thermal 6/6	1A

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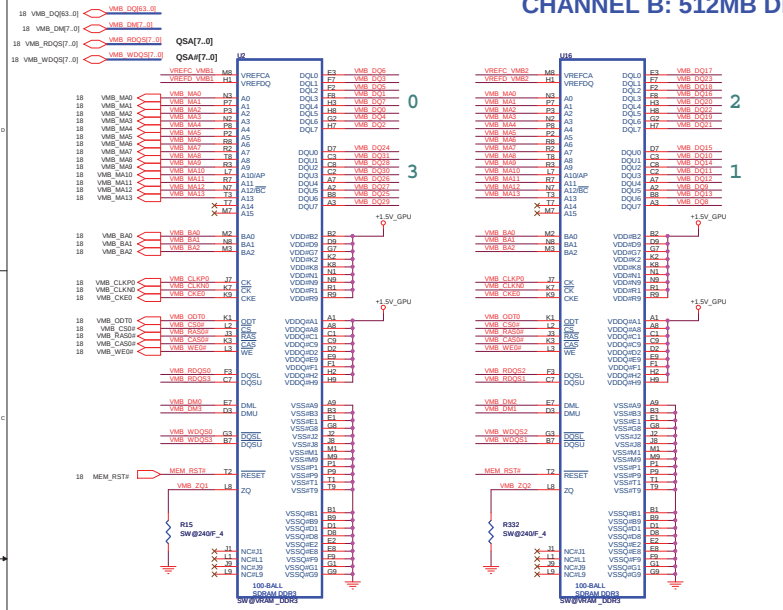
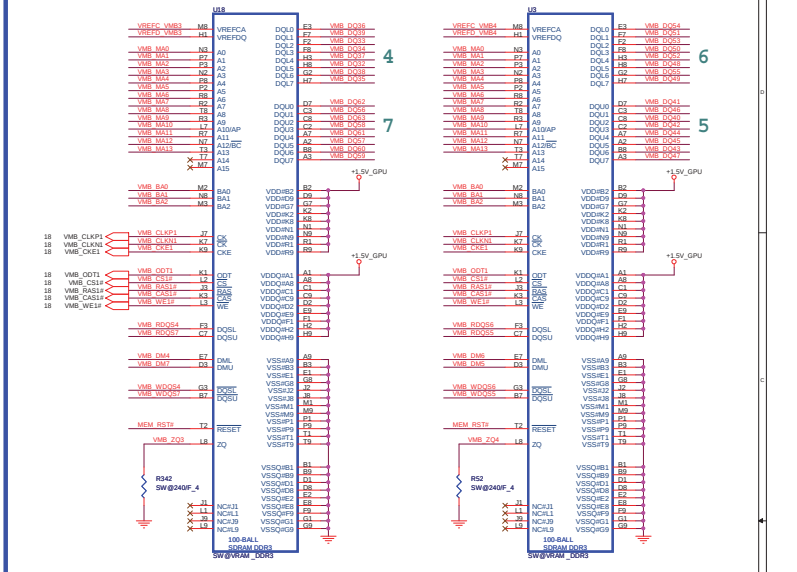
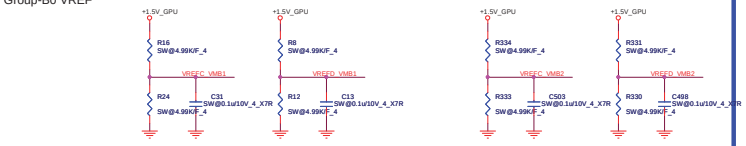
CHANNEL B: 512MB DDR3 (64M*16*4pcs)

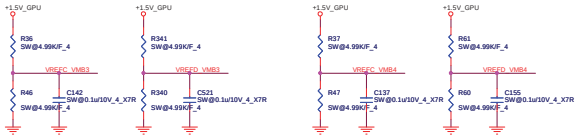




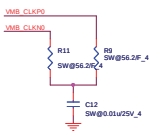
Group-B0 VREF



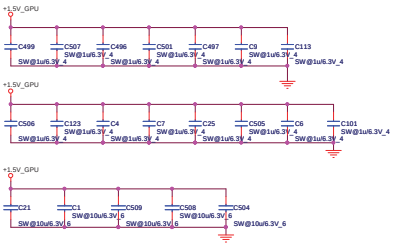
Group-B1 VREF



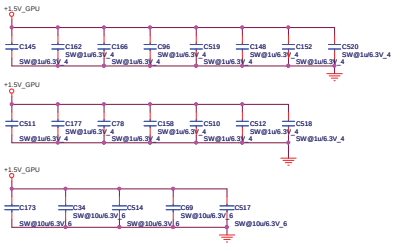
MEM_B0 CLK



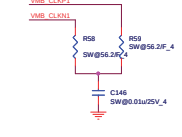
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	MEMORY 2 channel B	1A
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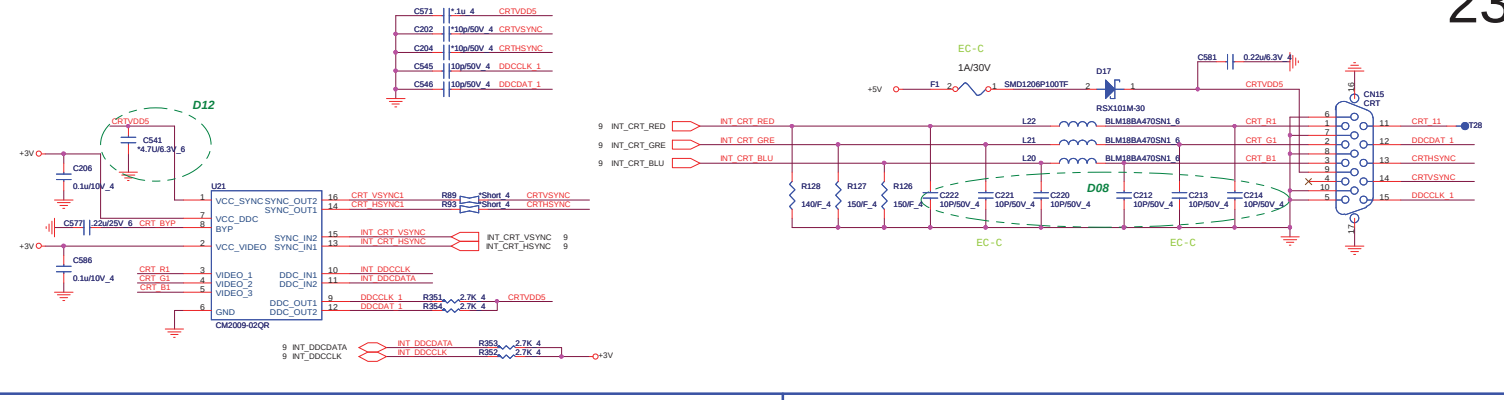
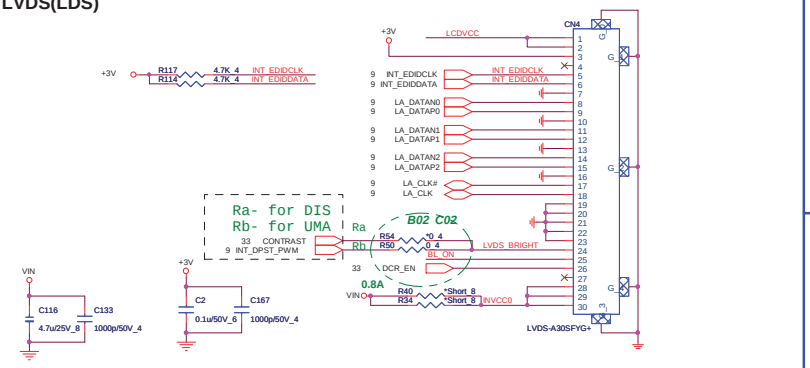
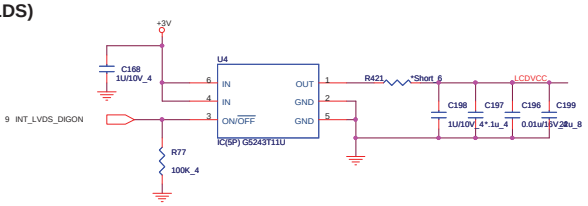
CRT



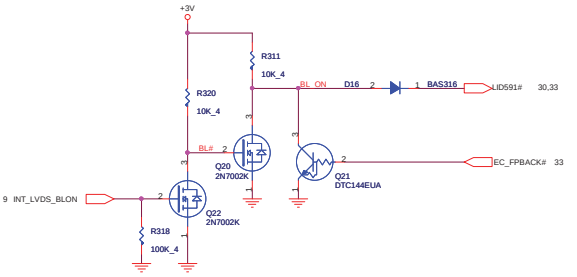
LVDS(LDS)



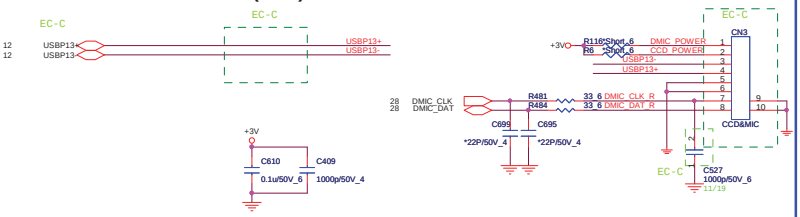
LCD PW(LDS)



Backlight Control(LDS)



CAMERA Module(CCD)



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	CRT/LVDS/LID	1A

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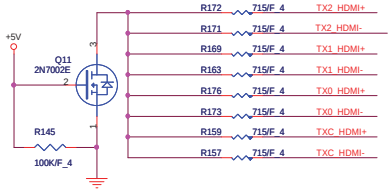
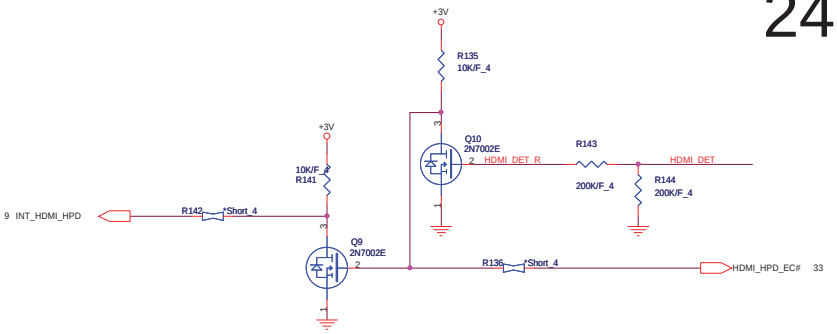
(HDM)

Close to HDMI Connector



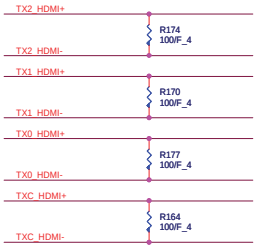
USE RS880M to display the HDMI
Stuff 715 ohm P/N--> CS17152FB17

HDMI HPD SENSE



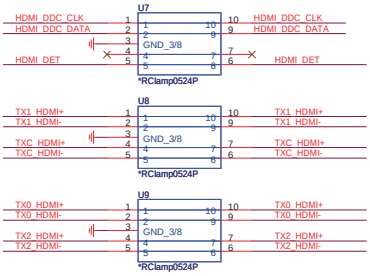
EMI reserve for HDMI(HDM)

Close connector

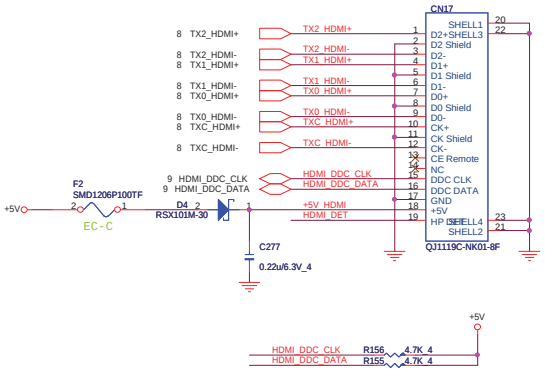


ESD Protect

close to HDMI connector



HDMI PORT



+5V 23,27,28,32,35,42
+3V 2,4,5,9..15,19,23,26,28..33,35..42

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Quanta Computer Inc.

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	HDMI	1A
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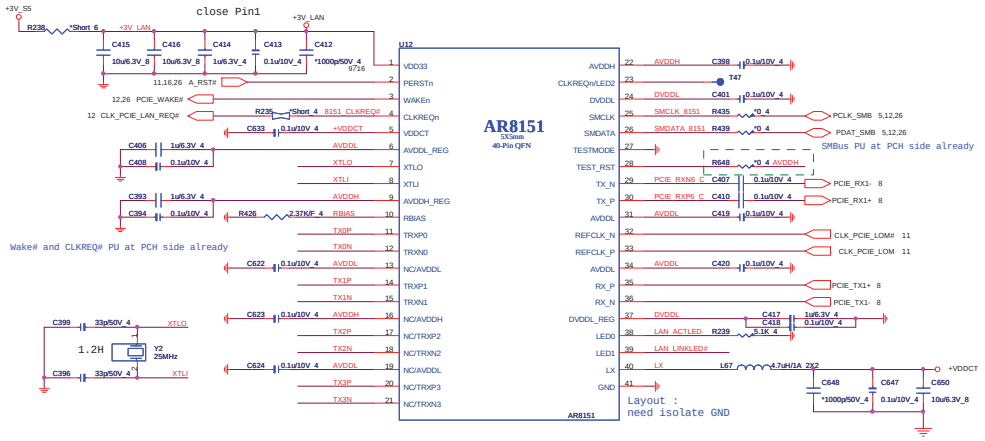
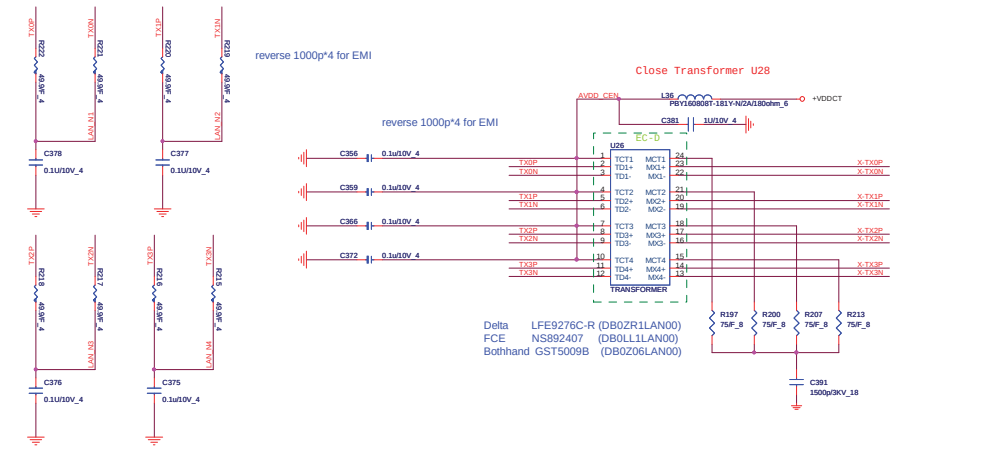
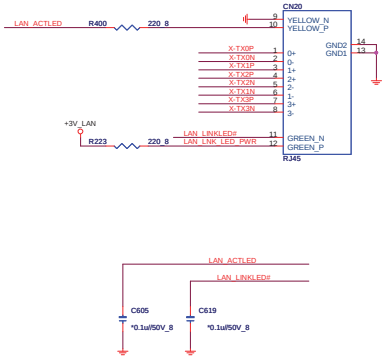
Giga-LAN AR8151



TRANSFORMER(LAN)



RJ45(LAN)



PROJECT : ZQ2			
Quanta Computer Inc.			
Size	Document Number		Rev
	LAN (AR8151)		1A
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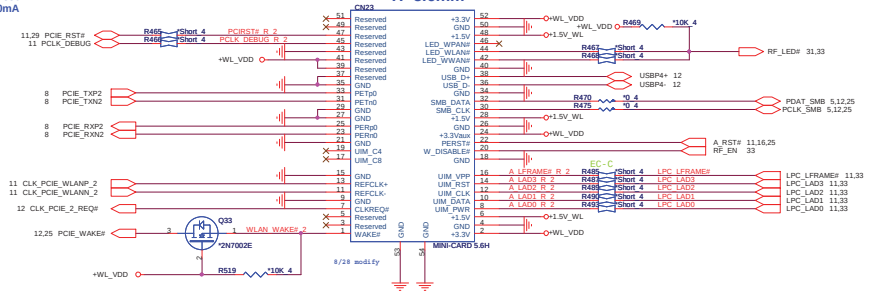
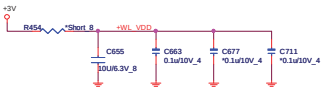
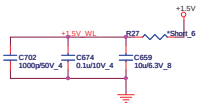
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

H=5.6mm







PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Mini-Card/WL	1A
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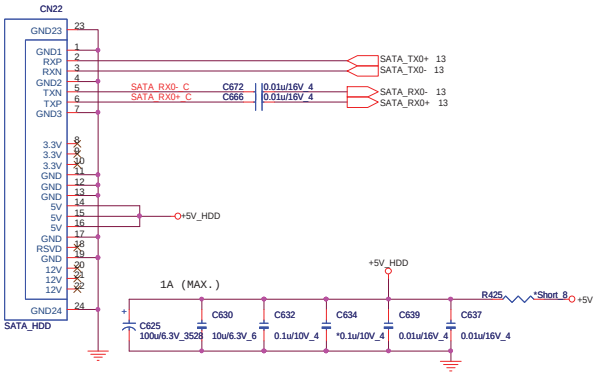
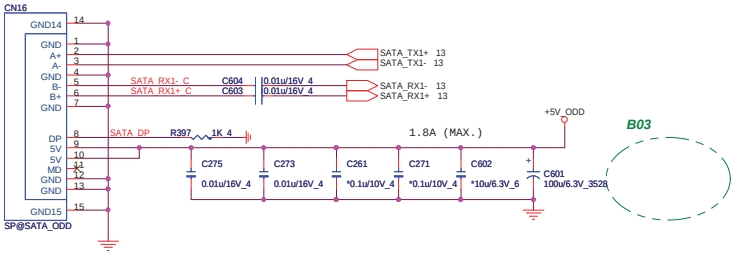
SATA HDD(HDD)



SATA ODD (ODD)



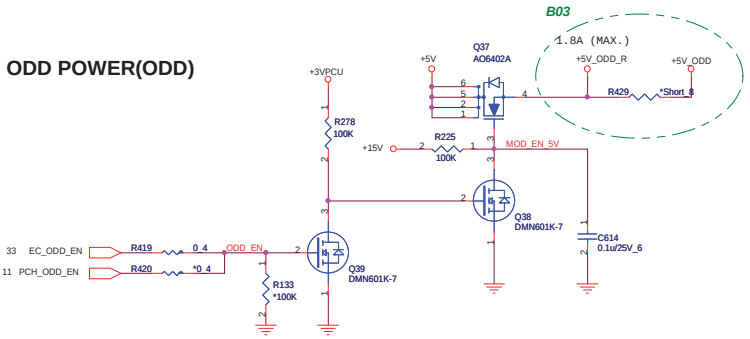
JV-12.7mm(H=5.5mm)-ZQ2

Main	DFHS13FR017	
Second	DFHS13FR006,	DFHS13FR005

JM-9.5mm(H=2.4mm)-ZQ2B

Main	DFHS13FR078,	DFHS13FR077
Second	DFHS13FR075	

ODD POWER(ODD)

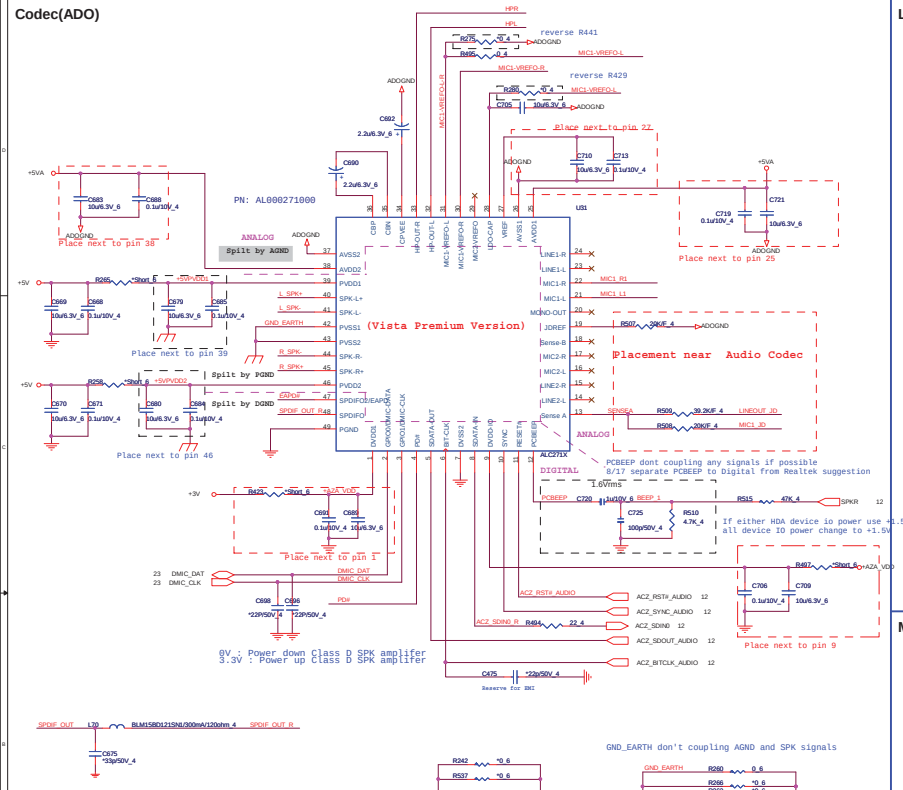


PROJECT : ZQ2

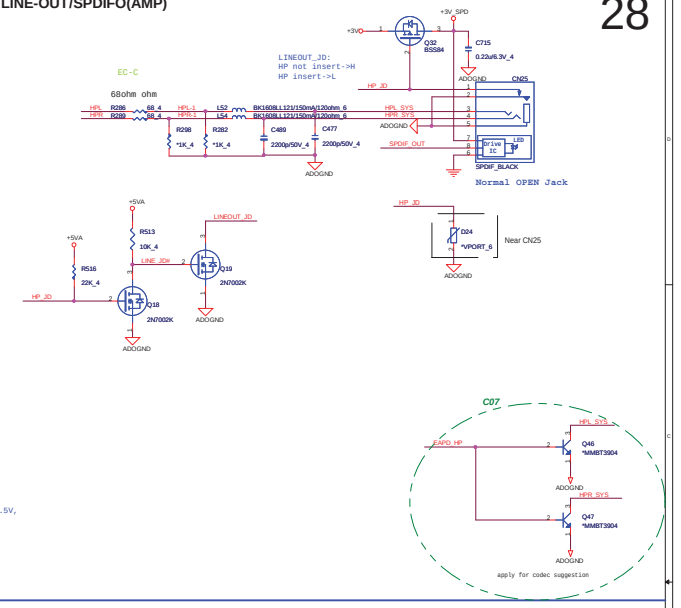
Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A
Date: Wednesday, May 27, 2009	Sheet 27 of 46	

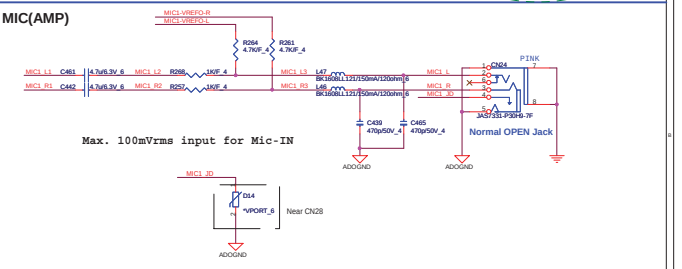
Codec(ADO)



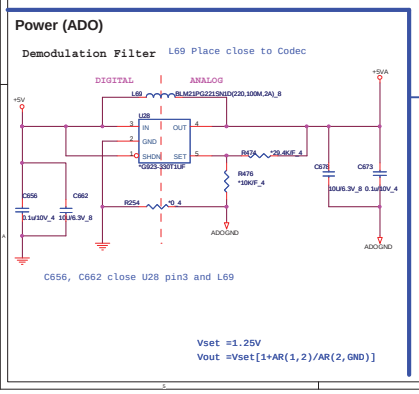
LINE-OUT/SPDIFO(AMP)



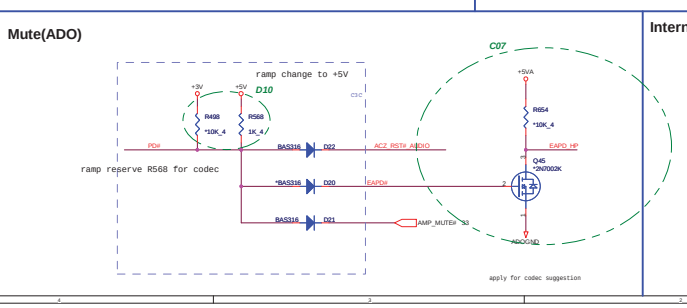
MIC(AMP)



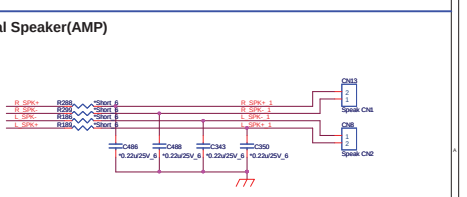
Power (ADO)



Mute(ADO)



Internal Speaker(AMP)



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Quanta Computer Inc.		
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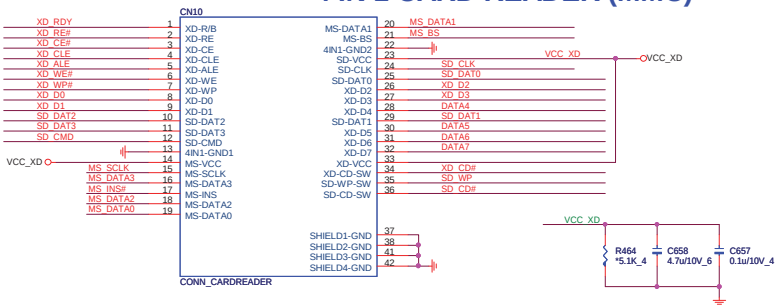
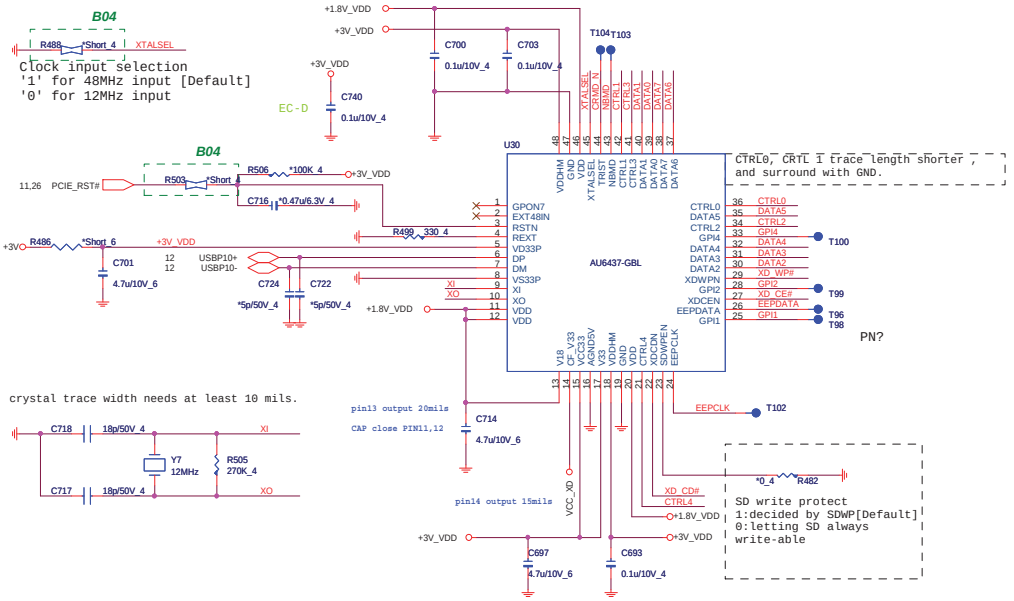
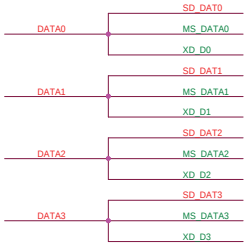
4 IN 1 CARD READER (MMC)

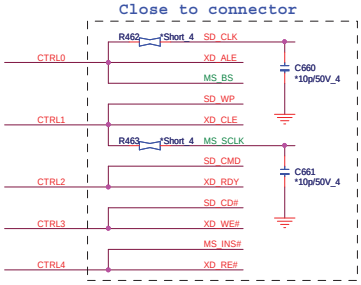
Main	??
Second	??



Close to CN10 pin 14 & pin23
4.7u CAP close to pin23



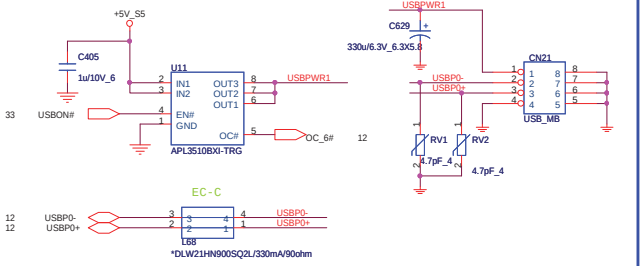




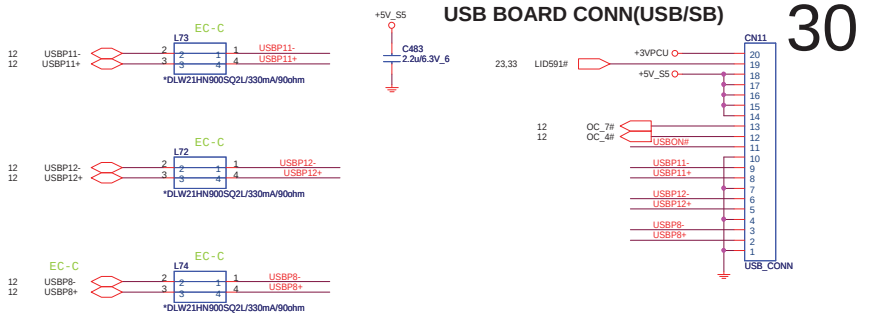
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	AU6437 CardReader	1A
Date: Wednesday, May 27, 2009	Sheet 29 of 46	

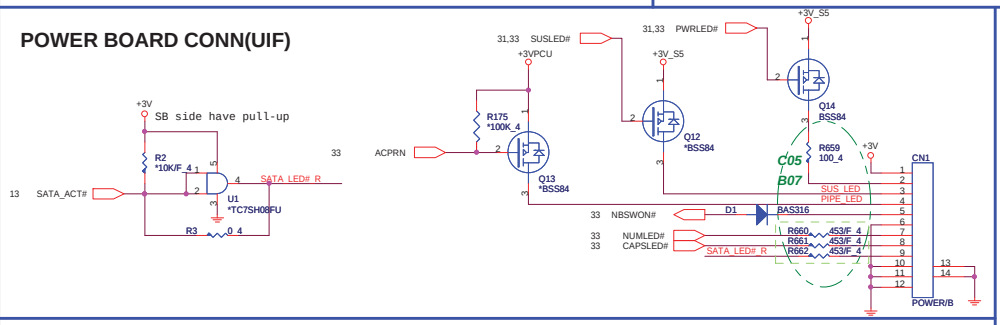
USB PORT(USB/MB)



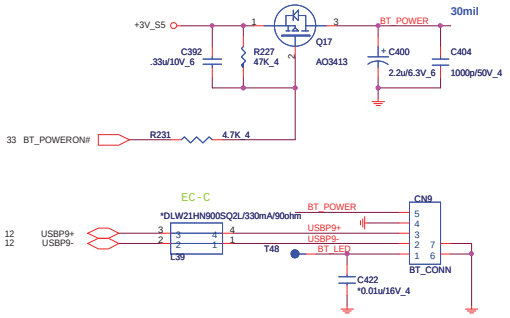
USB BOARD CONN(USB/SB)



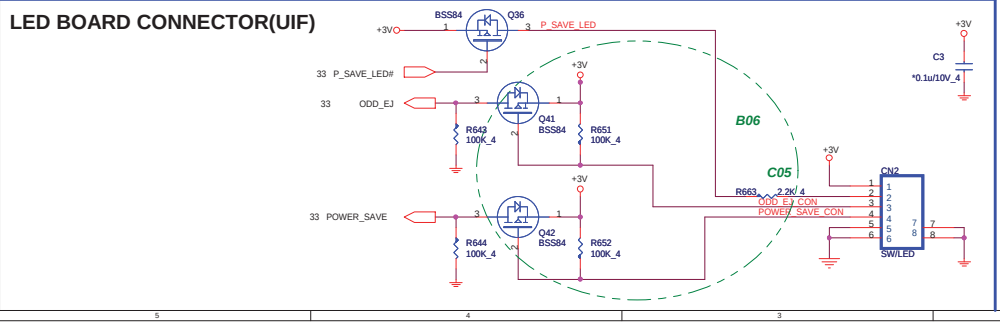
POWER BOARD CONN(UIF)



BLUETOOTH CONN(BTM)



LED BOARD CONNECTOR(UIF)



PROJECT : ZQ2

Quanta Computer Inc.

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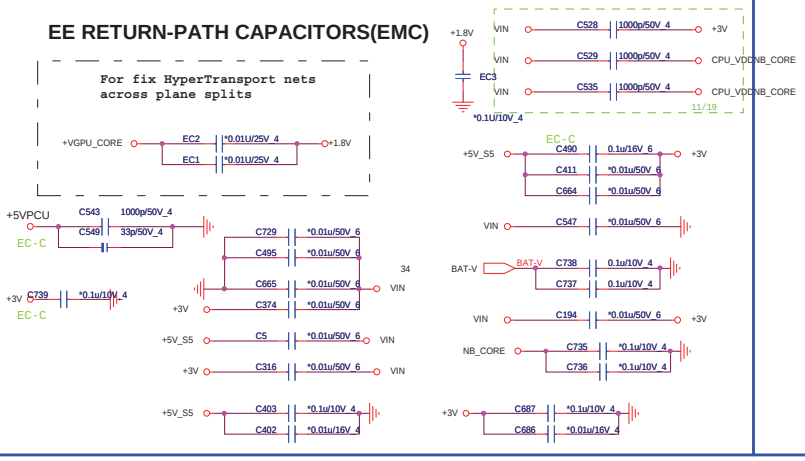
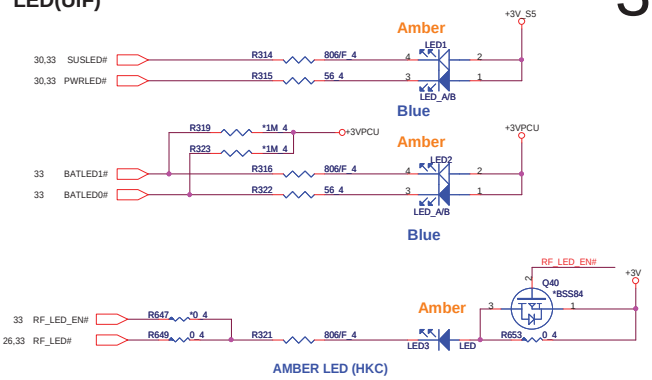
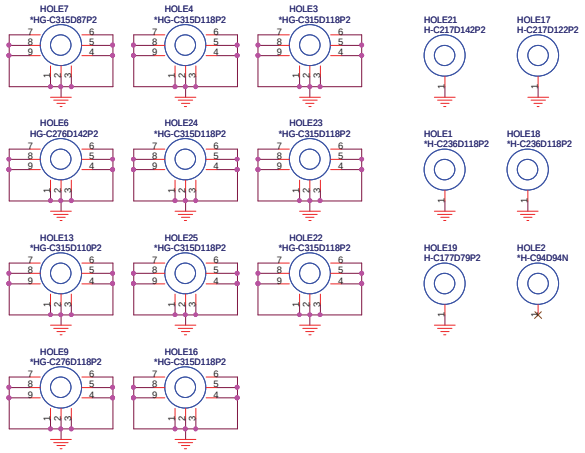
EE RETURN-PATH CAPACITORS(EMC)



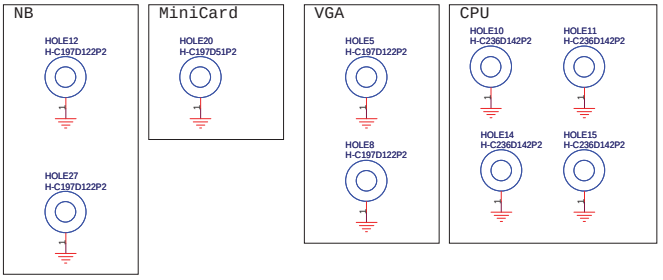
LED(UIF)

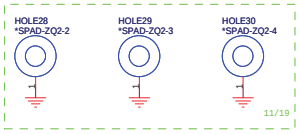


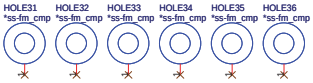
HOLE(OTH)



EC-C
DEL Hole26







PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	POWER/USB/BT/TP/MDC	1A
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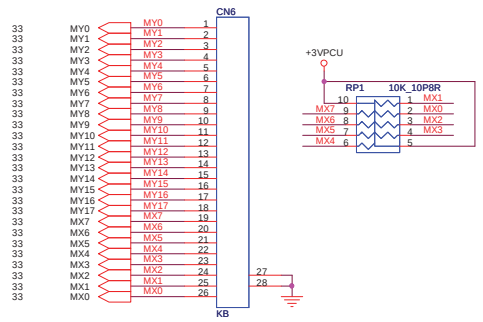
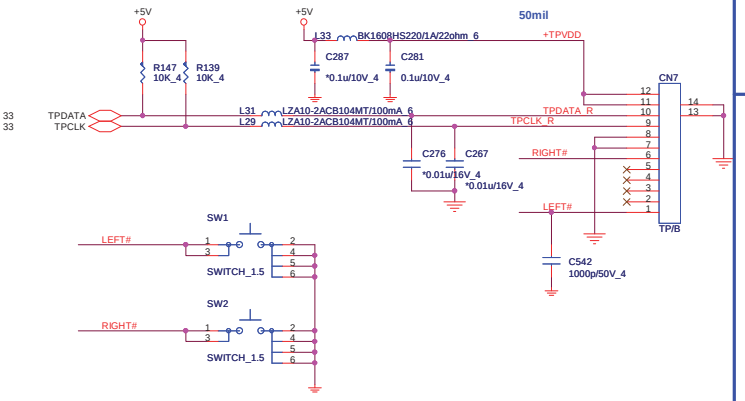
K/B(KBC)



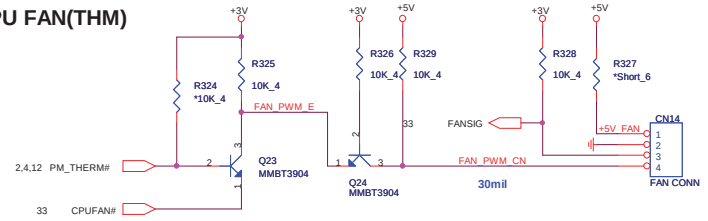
EC-C

Del CAP

TOUCHPAD BOARD CONN(TPD)



CPU FAN(THM)



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Quanta Computer Inc.

Size	Document Number	Rev
	KB/FAN/EE RETURN CAP	1A
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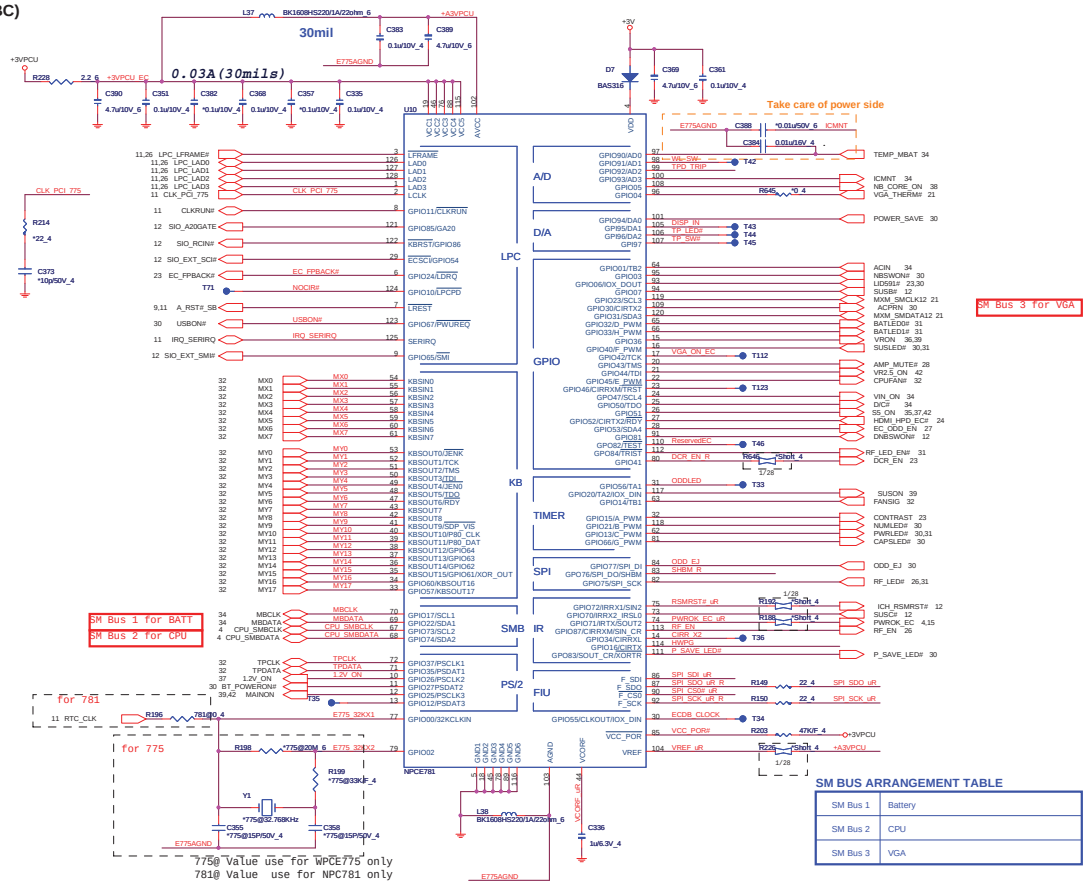
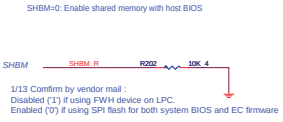
EC(KBC)

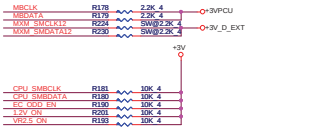


I/O ADDRESS SETTING(KBC)

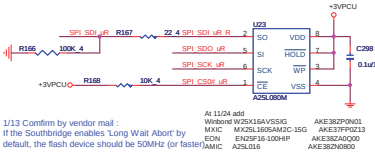
33



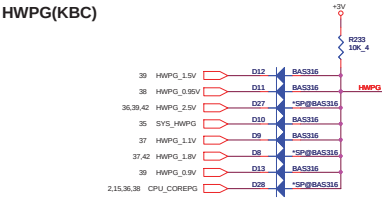
SM BUS PU(KBC)



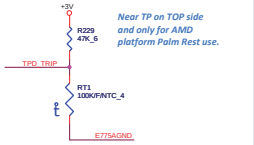
SPI FLASH(KBC)



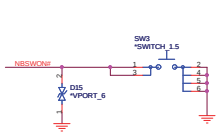
HWPG(KBC)



Palm Rest Thermal Sensor(THM)



POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

PROJECT : ZQ2	
Quanta Computer Inc.	
Size	Document Number: WPCE775C_0DG & FLASH
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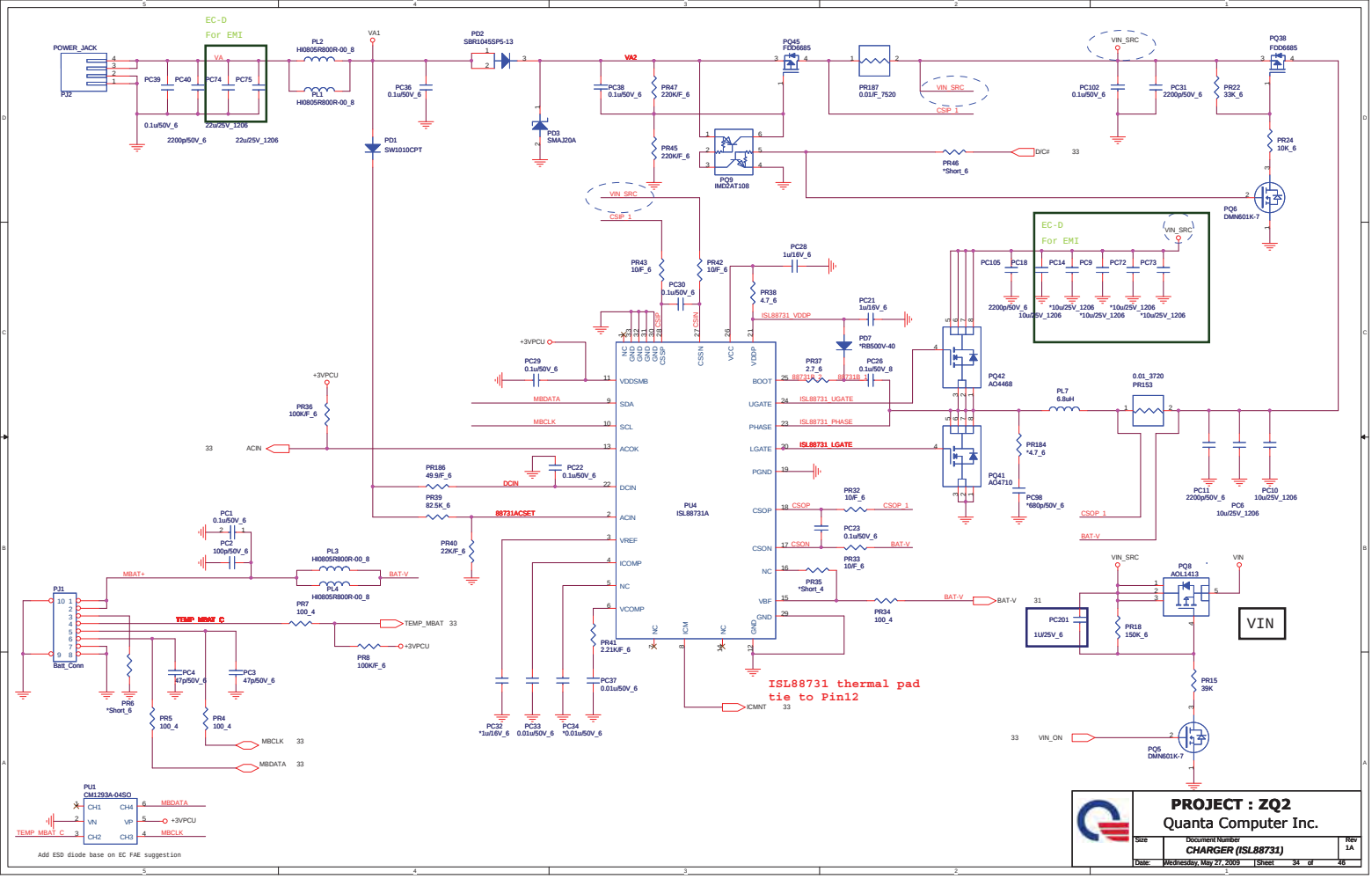
EC-D
For EMI
POWER_JACK
PJ2
PC39
PC40
PC74
PC75
0.1u/50V_6
2200p/50V_6
22u/25V_1206
PL2
HI0805R800R-00_8
PL1
HI0805R800R-00_8
VA1
PC36
0.1u/50V_6
PD1
SW1010CPT
PD2
SBR1045SP5-13
PD3
SMAJ20A
VA2
PC38
0.1u/50V_6
PR47
220K/F_6
PR45
220K/F_6
PQ45
FDD6685
PR187
0.01/F_7520
VIN_SRC
CSIP_1
PC102
0.1u/50V_6
PC31
2200p/50V_6
PR22
33K_6
PQ38
FDD6685
PR24
10K_6
PR46
*Short_6
D/C#
33
PQ9
IMD2AT108
PQ6
DMN601K-7
PR43
10/F_6
PR42
10/F_6
PC30
0.1u/50V_6
PC28
1u/16V_6
PR38
4.7_6
PC21
1u/16V_6
ISL88731_VDDP
PD7
*RB500V-40
PC26
0.1u/50V_8
PR37
2.7_6
88731B_1
88731A_1
PC29
0.1u/50V_6
+3VPCU
MBDATA
MBCLK
PR36
100K/F_6
33
ACIN
PR186
49.9/F_6
DCIN
PC22
0.1u/50V_6
PR39
82.5K_6
88731ACSET
PR40
22K/F_6
PC1
0.1u/50V_6
PC2
100p/50V_6
PL3
HI0805R800R-00_8
PL4
HI0805R800R-00_8
MBAT+
BAT-V
PJ1
Batt_Conn
TEMP_MBAT_C
PR7
100_4
TEMP_MBAT
33
PR8
100K/F_6
+3VPCU
PR6
*Short_6
PC4
47p/50V_6
PC3
47p/50V_6
PR5
100_4
PR4
100_4
MBCLK
33
MBDATA
33
PU4
ISL88731A
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
CSOP_1
CSON
BAT-V
PR32
10/F_6
PC23
0.1u/50V_6
PR33
10/F_6
PR35
*Short_4
PR34
100_4
PR41
2.21K/F_6
PC37
0.01u/50V_6
PC32
*1u/16V_6
PC33
0.01u/50V_6
PC34
*0.01u/50V_6
ICMNT
33
ISL88731 thermal pad
tie to Pin12
PQ42
AO4468
PQ41
AO4710
PL7
6.8uH
0.01_3720
PR153
PR184
*4.7_6
PC98
*680p/50V_6
PC11
2200p/50V_6
PC10
10u/25V_1206
PC8
10u/25V_1206
PC105
2200p/50V_6
PC18
10u/25V_1206
PC14
*10u/25V_1206
PC9
*10u/25V_1206
PC72
*10u/25V_1206
PC73
*10u/25V_1206
PC201
1U/25V_6
PQ8
AOL1413
PR18
150K_6
PR15
39K
VIN
PQ5
DMN601K-7
33
VIN_ON
PU1
CM1293A-04SO
CH1
CH4
VIN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT_C
Add ESD diode base on EC FAE suggestion
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
CHARGER (ISL88731)
Rev
1A
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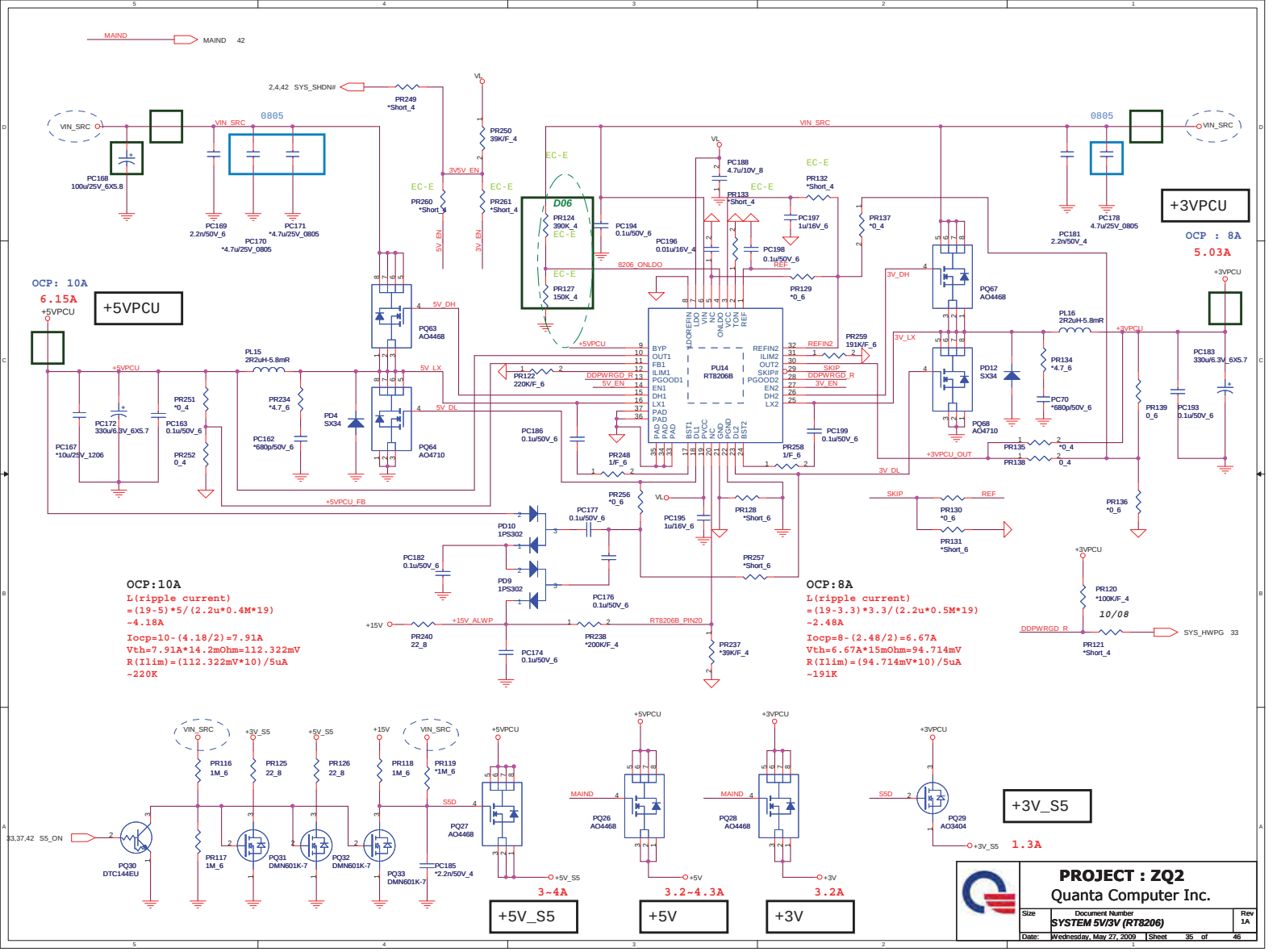
MAIND
MAIND 42
2,4,42 SYS_SHDN#
PR249 *Short_4
VL
PR250 39K/F_4
VIN_SRC
0805
3V5V_EN
EC-E
PR260 *Short_4
PR261 *Short_4
5V_EN
3V_EN
D06
PR124 390K_4
PR127 150K_4
PC194 0.1u/50V_6
PC196 0.01u/16V_4
PC188 4.7u/10V_8
PR133 *Short_4
PR132 *Short_4
PC197 1u/16V_6
PC198 0.1u/50V_6
REF
PR129 *0_6
8206_ONLDO
PR137 *0_4
3V_DH
3V_LX
PQ67 AO4468
PC181 2.2n/50V_4
PC178 4.7u/25V_0805
+3VPCU
OCP : 8A
5.03A
OCP: 10A
6.15A
+5VPCU
PC168 100u/25V_6X5.8
PC169 2.2n/50V_6
PC170 *4.7u/25V_0805
PC171 *4.7u/25V_0805
PQ63 AO4468
5V_DH
5V_LX
5V_DL
PL15 2R2uH-5.8mR
PR251 *0_4
PR252 0_4
PC172 330u/6.3V_6X5.7
PC163 0.1u/50V_6
PC167 *10u/25V_1206
PR234 *4.7_6
PC162 *680p/50V_6
PD4 SX34
PQ64 AO4710
+5VPCU_FB
PU14 RT8206B
DDPWRGD_R
5V_EN
SKIP
REFIN2
PR259 191K/F_6
PR122 220K/F_6
PR248 1/F_6
PR258 1/F_6
PC199 0.1u/50V_6
PC186 0.1u/50V_6
PR256 *0_6
PC177 0.1u/50V_6
PC195 1u/16V_6
PR128 *Short_6
PR257 *Short_6
PD10 1PS302
PD9 1PS302
PC182 0.1u/50V_6
PC176 0.1u/50V_6
+15V
+15V_ALWP
RT8206B_PIN20
PR240 22_8
PR238 *200K/F_4
PC174 0.1u/50V_6
PR237 *39K/F_4
PQ68 AO4710
PD12 SX34
PL16 2R2uH-5.8mR
PR134 *4.7_6
PC70 *680p/50V_6
PR135 *0_4
PR138 0_4
+3VPCU_OUT
PC183 330u/6.3V_6X5.7
PR139 0_6
PC193 0.1u/50V_6
PR130 *0_6
PR131 *Short_6
PR136 *0_6
PR120 *100K/F_4
10/08
DDPWRGD_R
SYS_HWPG 33
PR121 *Short_4
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
PR116 1M_6
PR125 22_8
PR126 22_8
PR118 1M_6
PR119 *1M_6
+3V_S5
+5V_S5
S5D
PQ27 AO4468
PR117 1M_6
PQ30 DTC144EU
PQ31 DMN601K-7
PQ32 DMN601K-7
PQ33 DMN601K-7
PC185 *2.2n/50V_4
33,37,42 S5_ON
PQ26 AO4468
PQ28 AO4468
MAIND
+5V
+3V
PQ29 AO3404
+3V_S5
1.3A
3~4A
3.2~4.3A
3.2A
+5V_S5
+5V
+3V
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1A
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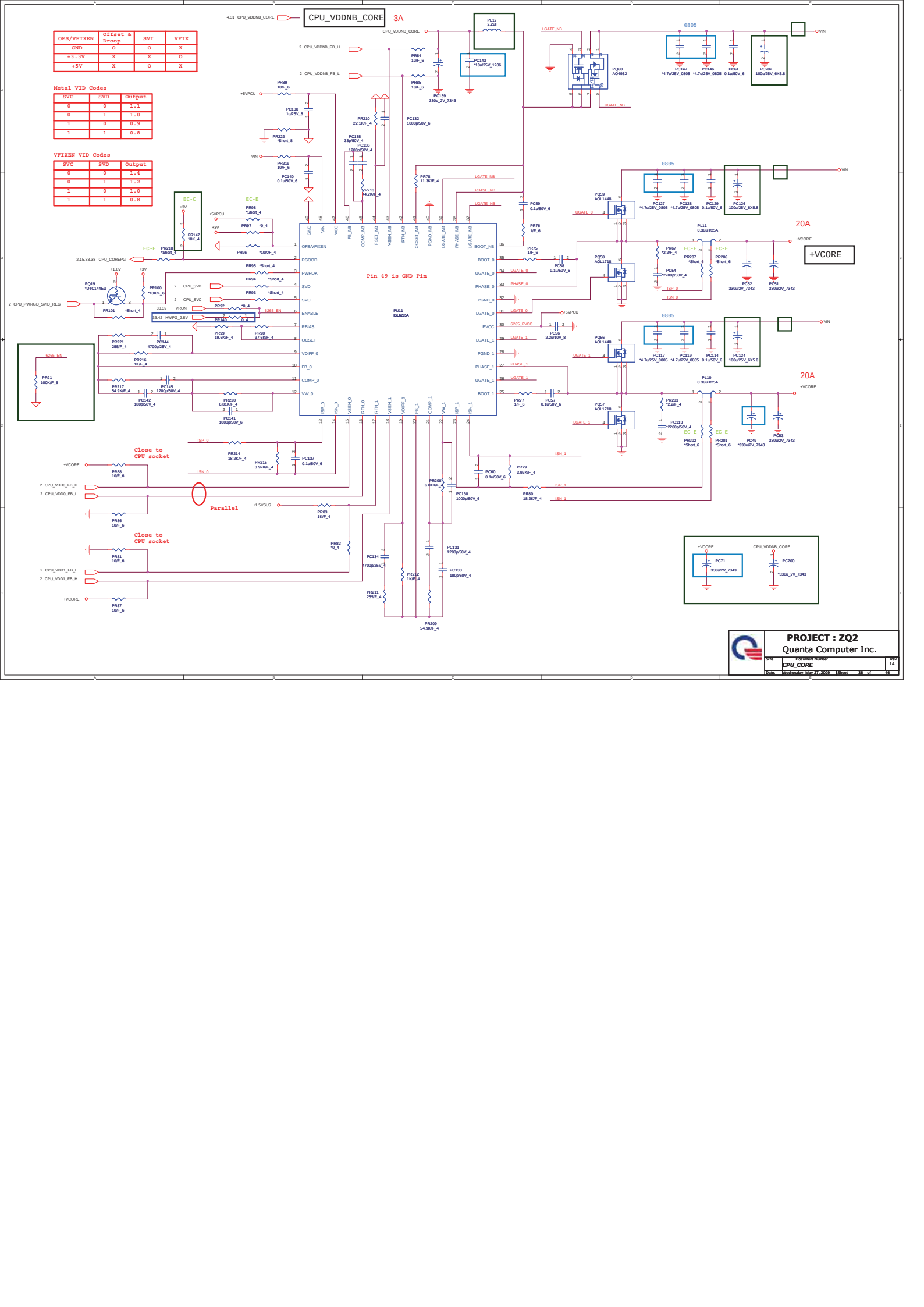
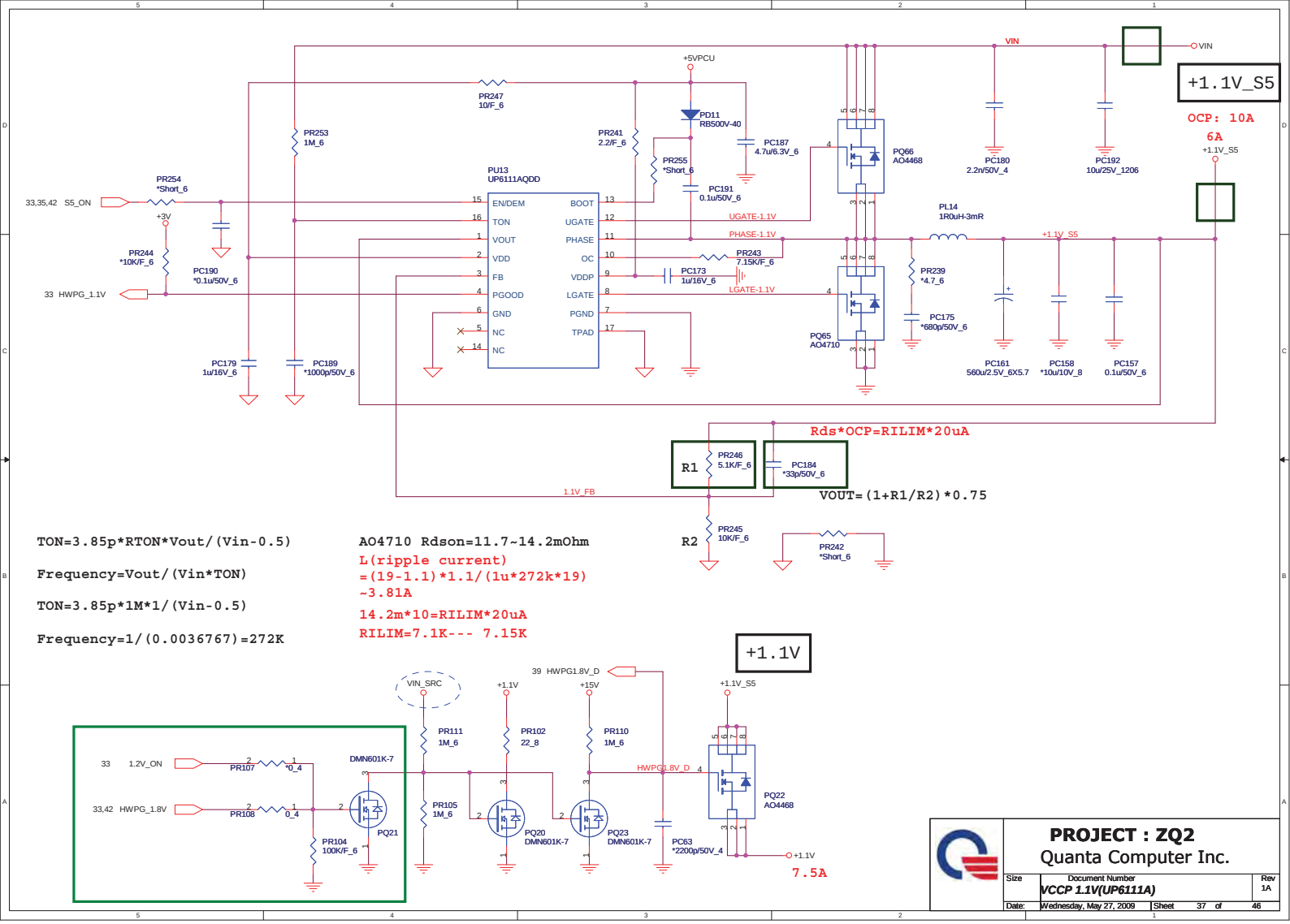

CPU_VDDNB_CORE
3A
OFS/VFIXEN | Offset & Droop | SVI | VFIX
GND | O | O | X
+3.3V | X | X | O
+5V | X | O | X
Metal VID Codes
SVC | SVD | Output
0 | 0 | 1.1
0 | 1 | 1.0
1 | 0 | 0.9
1 | 1 | 0.8
VFIXEN VID Codes
SVC | SVD | Output
0 | 0 | 1.4
0 | 1 | 1.2
1 | 0 | 1.0
1 | 1 | 0.8
Pin 49 is GND Pin
ISL6265A
Close to CPU socket
Parallel
Close to CPU socket
20A
+VCORE
PROJECT : ZQ2
Quanta Computer Inc.
CPU_CORE
Wednesday, May 27, 2009



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
~3.81A

14.2m*10=RILIM*20uA

RILIM=7.1K--- 7.15K

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Quanta Computer Inc.

Size	Document Number	Rev
	VCCP 1.1V(UP6111A)	1A
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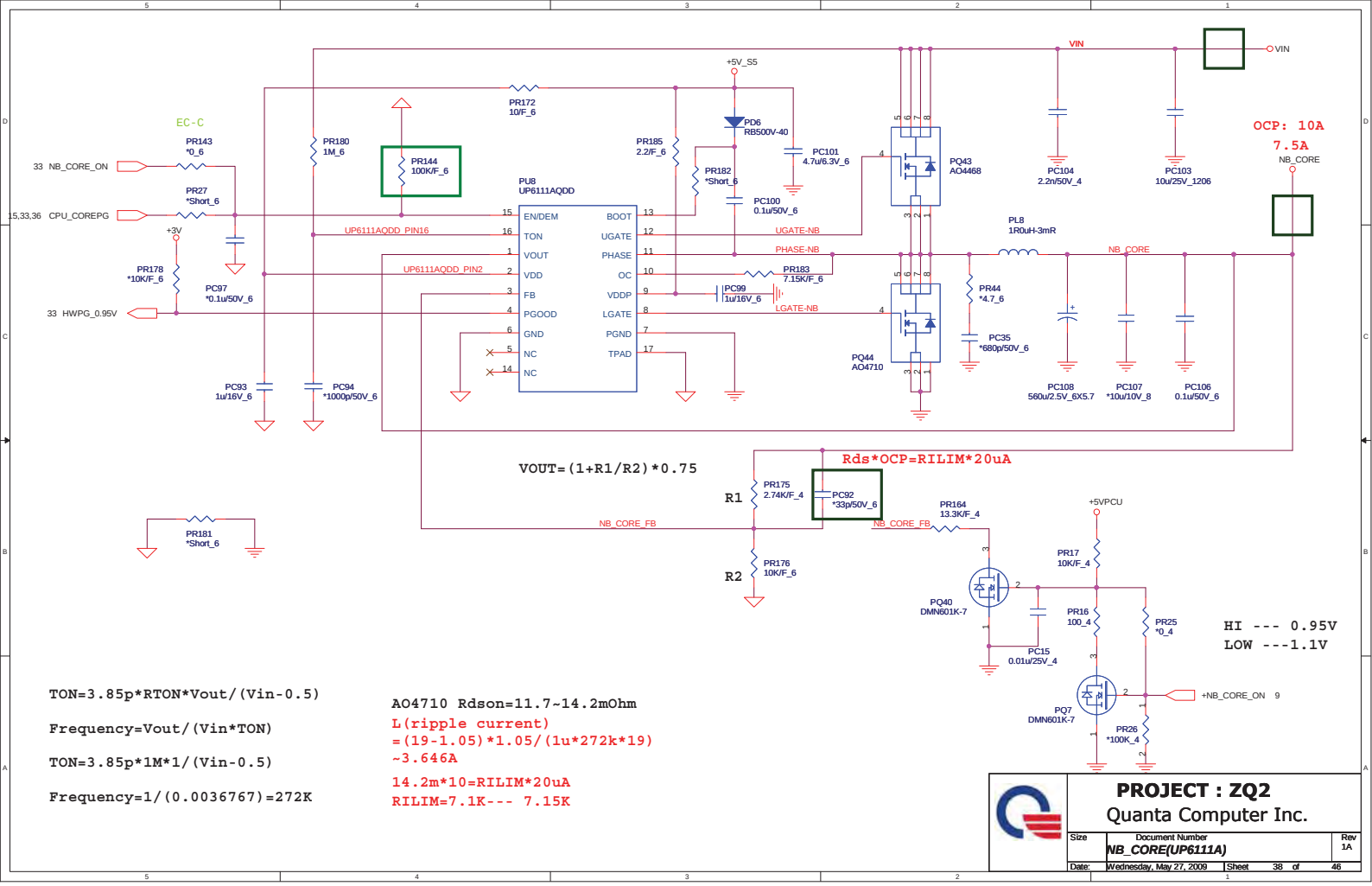

PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	NB_CORE(UP6111A)	1A
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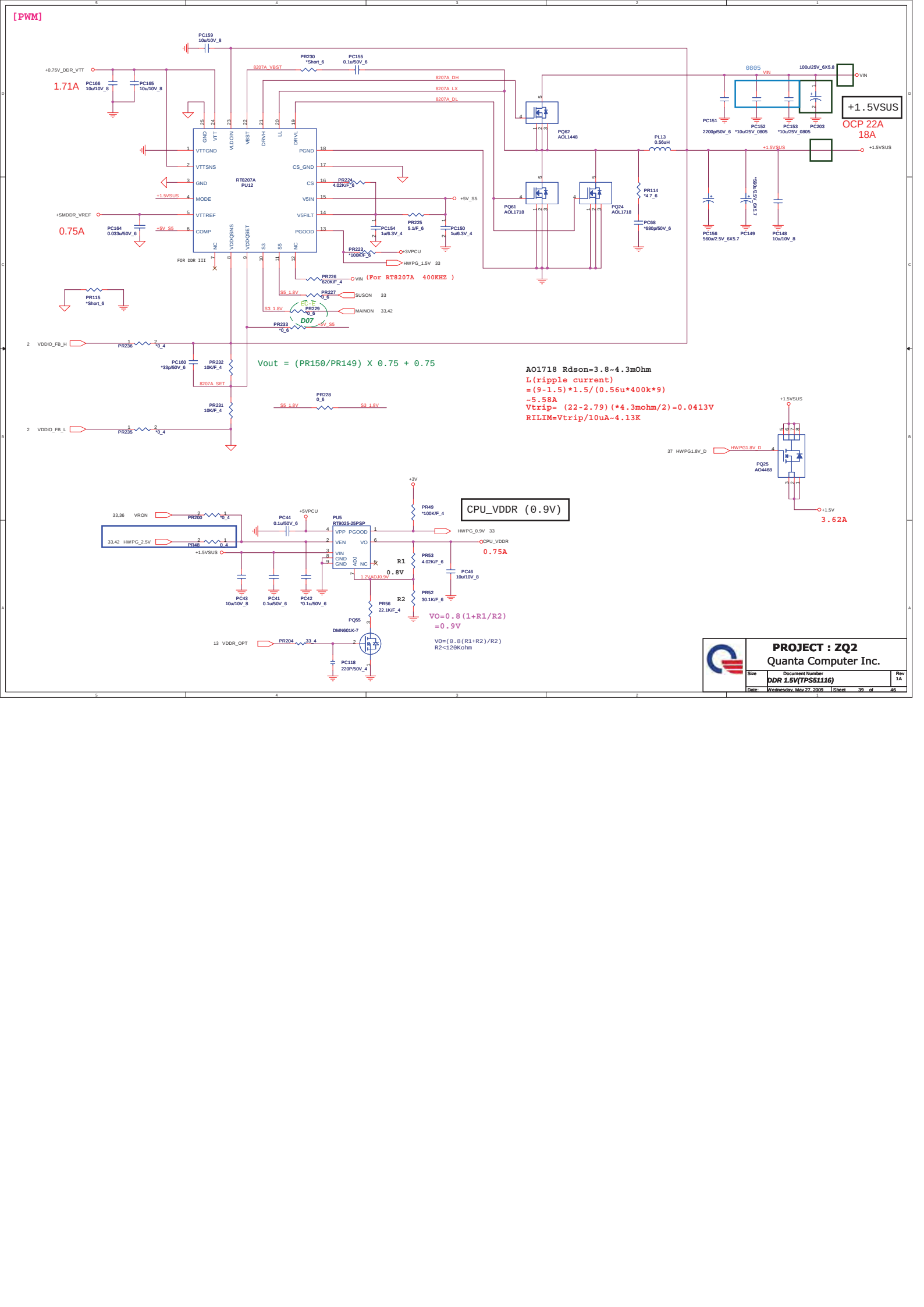
[PWM]
PC159 10u/10V_8
+0.75V_DDR_VTT
1.71A
PC166 10u/10V_8
PC165 10u/10V_8
PR230 *Short_6
PC155 0.1u/50V_6
8207A_VBST
8207A_DH
8207A_LX
8207A_DL
RTB207A PU12
VTTGND
VTTSNS
GND
MODE
VTTREF
COMP
PGND
CS_GND
CS
V5IN
V5FILT
PGOOD
PR224 4.02K/F_6
PR225 5.1/F_6
PC154 1u/6.3V_4
PC150 1u/6.3V_4
+5V_S5
+SMDDR_VREF
0.75A
PC164 0.033u/50V_6
PR223 *100K/F_6
+3VPCU
HWPG_1.5V 33
PR226 620K/F_4
VIN
(For RT8207A 400KHZ)
PR227 0_6
SUSON 33
PR229 *0_6
MAINON 33,42
D07
PR233 *0_6
PR115 *Short_6
VDDIO_FB_H
PR236 *0_4
PC160 *33p/50V_6
PR232 10K/F_4
8207A_SET
PR231 10K/F_4
PR228 0_6
VDDIO_FB_L
PR235 *0_4
PQ62 AOL1448
PQ61 AOL1718
PQ24 AOL1718
PL13 0.56uH
PR114 *4.7_6
PC68 *680p/50V_6
0805
VIN
100u/25V_6X5.8
PC151 2200p/50V_6
PC152 *10u/25V_0805
PC153 *10u/25V_0805
PC203
+1.5VSUS
OCP 22A
18A
+1.5VSUS
PC156 560u/2.5V_6X5.7
PC149 *560u/2.5V_6X5.7
PC148 10u/10V_8
AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(9-1.5)*1.5/(0.56u*400k*9)
~5.58A
Vtrip= (22-2.79)(*4.3mohm/2)=0.0413V
RILIM=Vtrip/10uA~4.13K
Vout = (PR150/PR149) X 0.75 + 0.75
+1.5VSUS
37 HWPG1.8V_D
HWPG1.8V_D
PQ25 AO4468
+1.5V
3.62A
CPU_VDDR (0.9V)
33,36 VRON
PR200 *0_4
33,42 HWPG_2.5V
PR48 0_4
+1.5VSUS
PC44 0.1u/50V_6
+5VPCU
PU5 RT9025-25PSP
VPP PGOOD
VEN VO
VIN
GND
GND ADJ NC
1.2VADJ0.9V
+3V
PR49 *100K/F_4
HWPG_0.9V 33
CPU_VDDR
0.75A
R1
0.8V
PR53 4.02K/F_6
PC46 10u/10V_8
R2
PR52 30.1K/F_6
PR56 22.1K/F_4
VO=0.8(1+R1/R2)
=0.9V
VO=(0.8(R1+R2)/R2)
R2<120Kohm
PC43 10u/10V_8
PC41 0.1u/50V_6
PC42 *0.1u/50V_6
PQ55 DMN601K-7
13 VDDR_OPT
PR204 33_4
PC118 220P/50V_4
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Quanta Computer Inc.
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DDR 1.5V(TPS51116)
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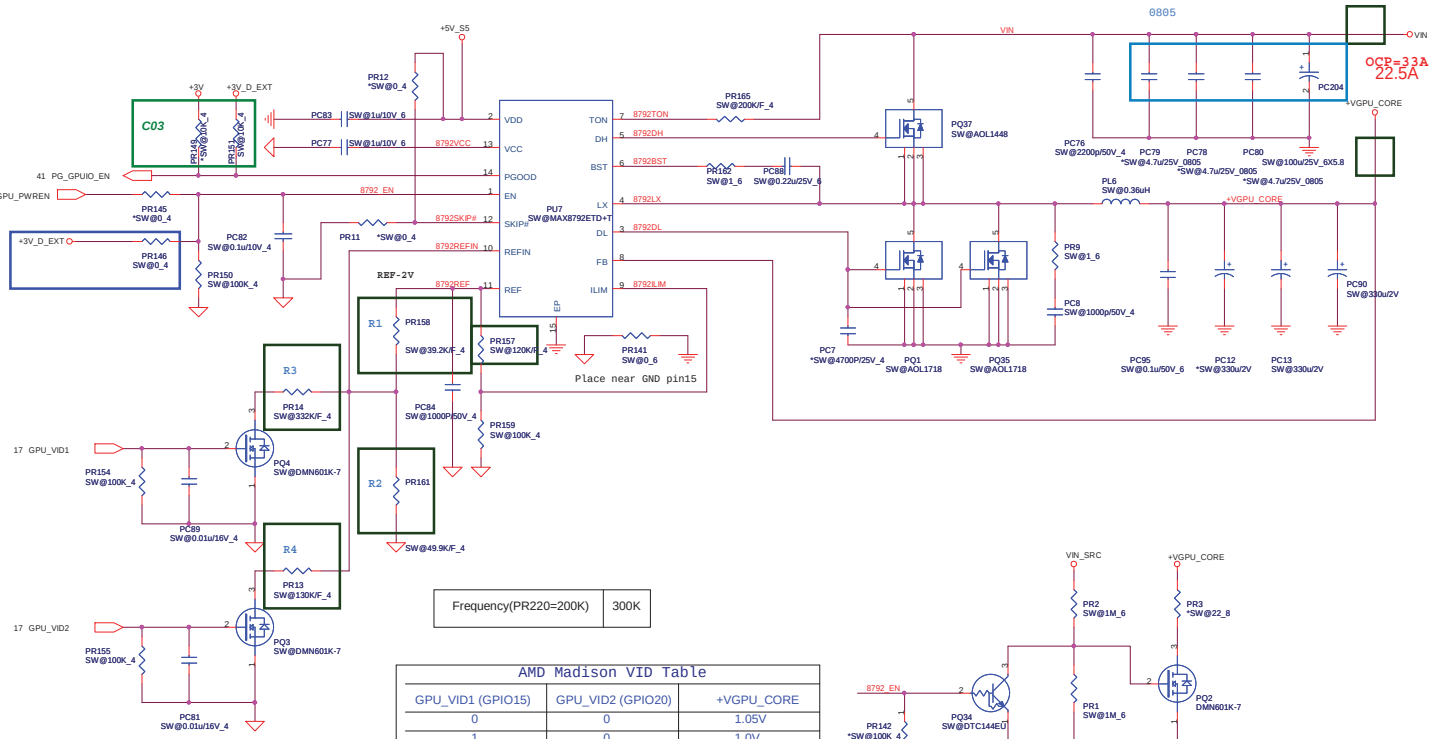
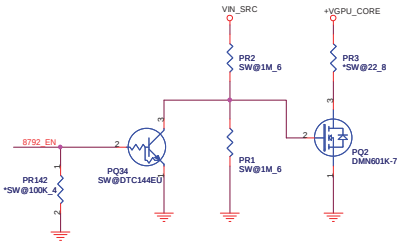
+VGPU_CORE





Frequency(PR220=200K)	300K

AMD Madison VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
1	1	0.9V

Park -XT

GPU_VID1 (GPIO15)	*GPU_VID2 (GPIO20)*	*+VGPU_CORE*
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

R3	*R4*	*R1*	*R2*	*VREF*
332K	130K	39.2K	49.9K	2V

R1 change to 39.2K/F_4 (CS33922FB15)
R3 change to 332K/F_4 (CS43322FB15)
R4 change to 130K/F_4 (CS41302FB00)

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	GPU CORE(MAX8792)	1A

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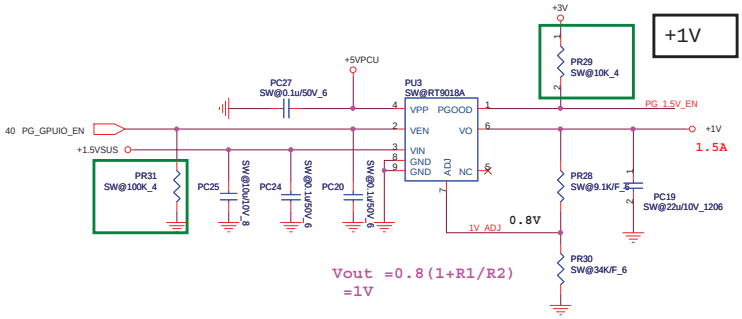

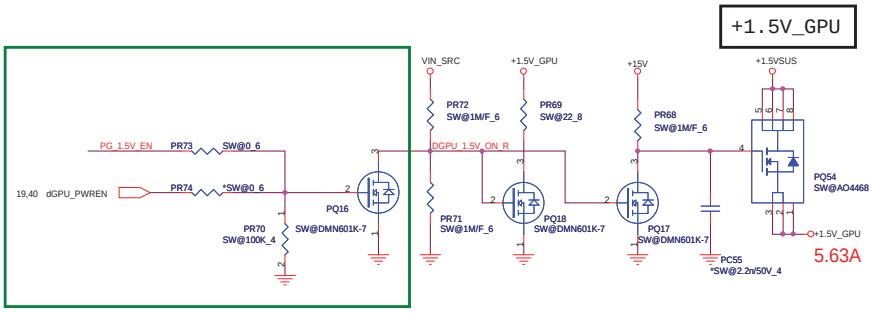

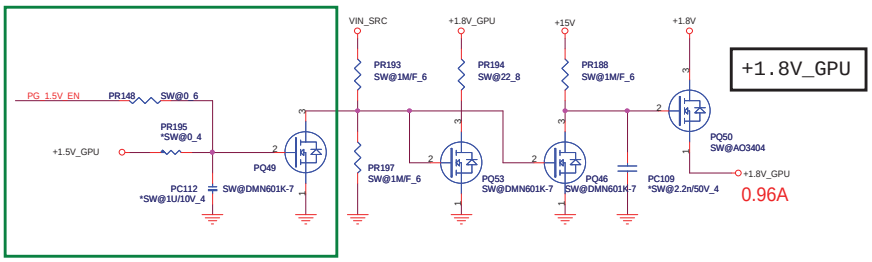

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Quanta Computer Inc.

Size	Document Number	Rev
	+1V/+1.5_GPU/+1.8_GPU	1A
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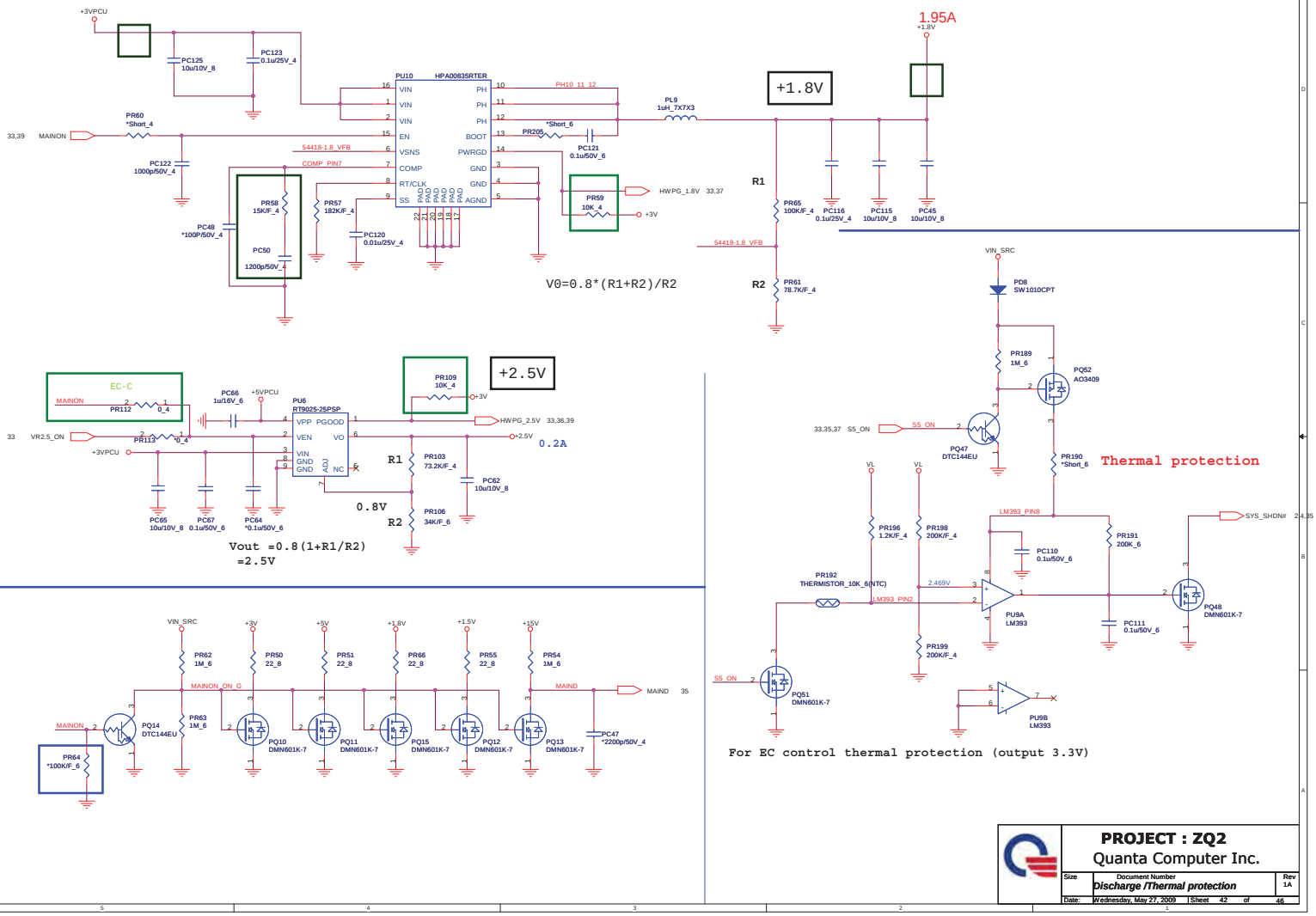

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Quanta Computer Inc.

Size	Document Number	Rev
	Discharge /Thermal protection	1A
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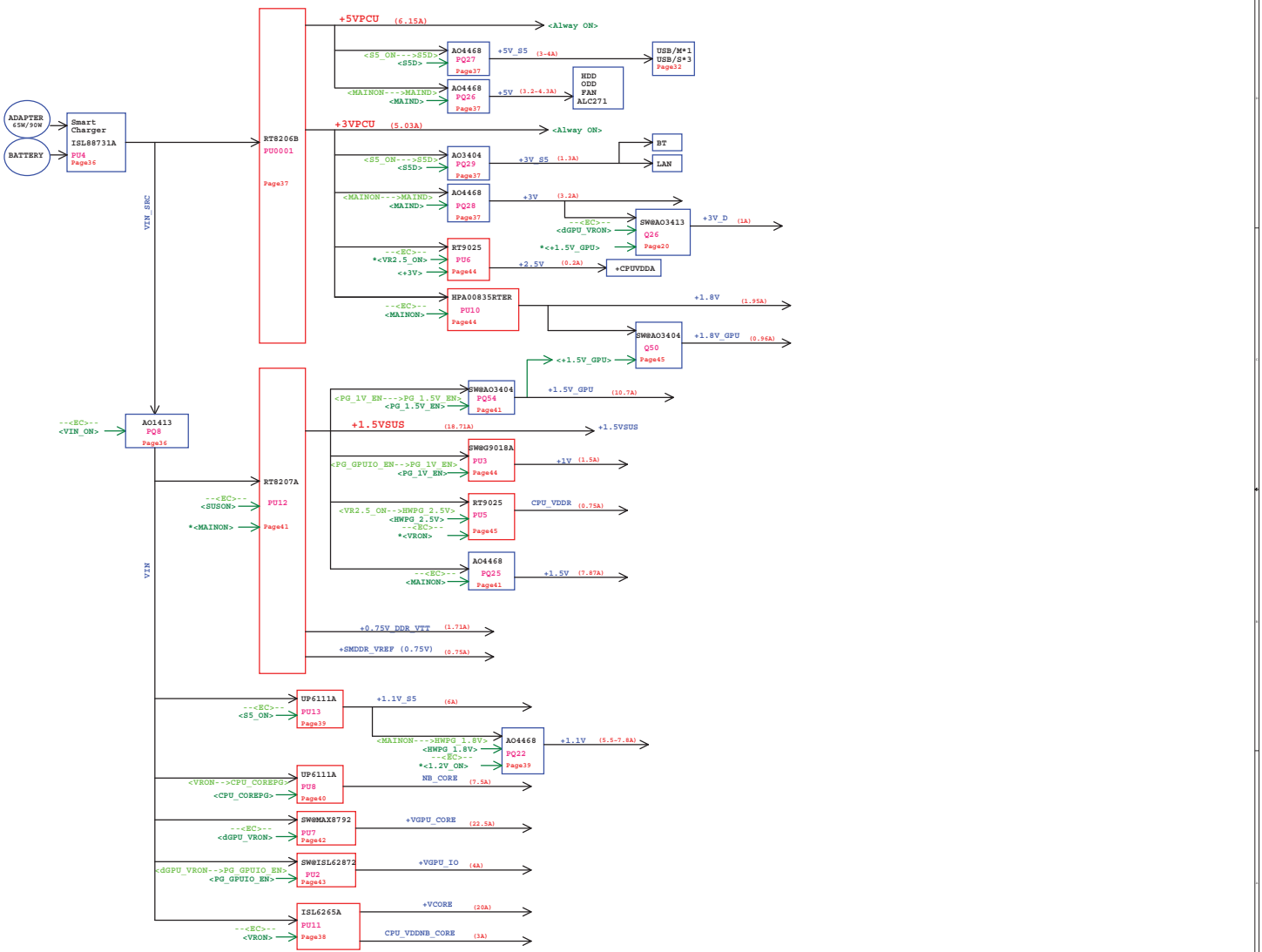
ZQ2 Power tree



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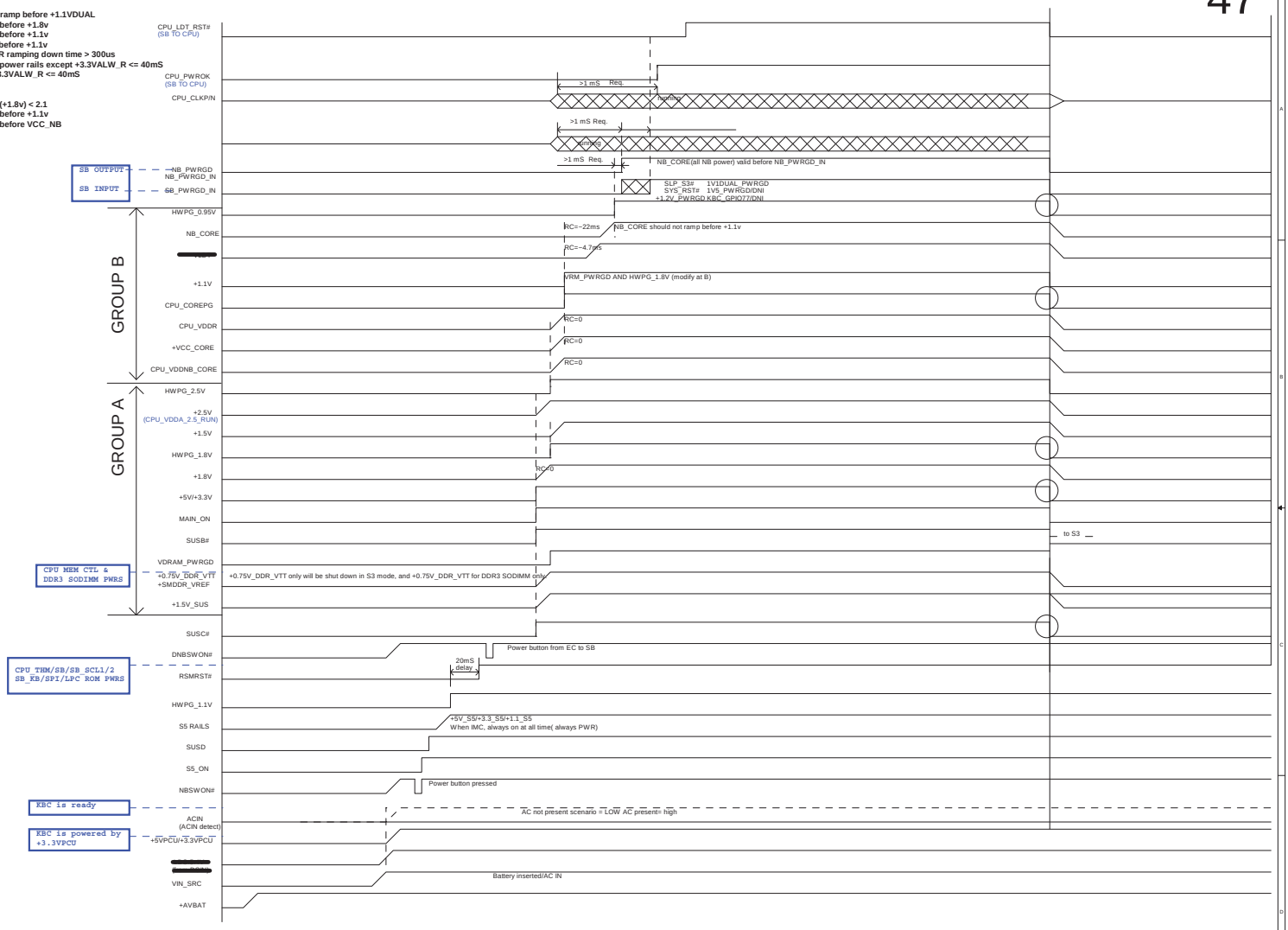
Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB



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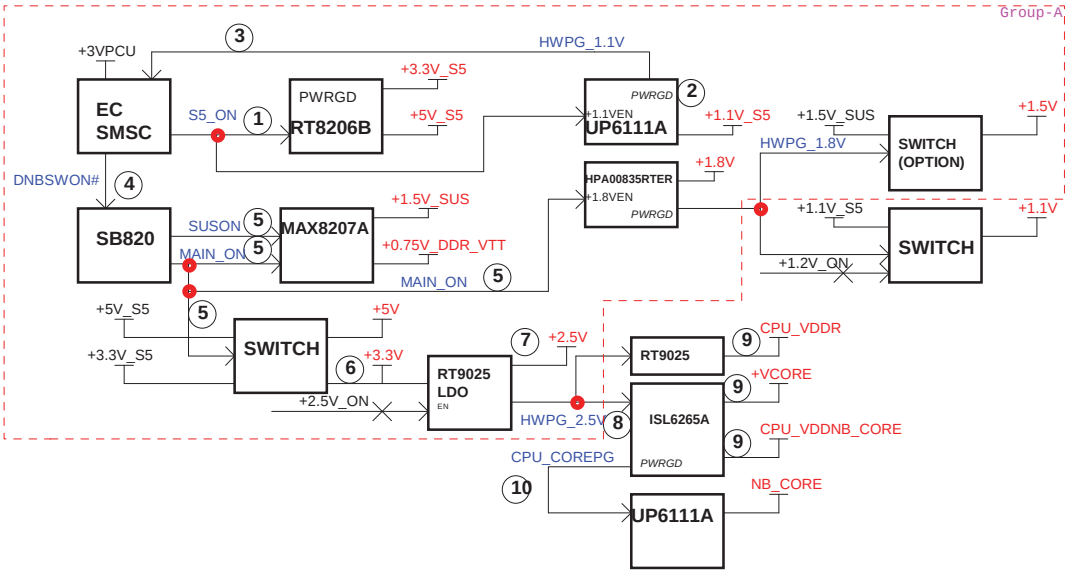

Power on Sequence required:

SB800:
1, +3.3V_S5 ramp before +1.1_S5
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB

POWER RAILS Sequencing

1	S5_ON	13	+1.8V
2	+3.3V_S5	14	HWPG_1.8V
3	+5V_S5	15	+1.5V
4	+1.1V_S5	16	+2.5V
5	HWPG_1.1V	17	HWPG_2.5V
6	DNBSWON#	18	CPU_VDDNB_CORE
7	SUSON	19	+VCC_CORE
8	+1.5V_SUS	20	CPU_VDDR
9	+SMDDR_VTERM	21	CPU_COREPG
10	MAIN_ON	22	+1.1V
11	+5V	23	NB_CORE
12	+3.3V	24	

SB820 Sequencing

1	+3.3V_S5
2	ICH_RSMRST#
3	S0 POWER
4	PCIE_RCLKP/N
5	PCICLK[4:0]
6	SB_PWRGD_IN
7	NB_PWRGD_IN
8	LDT_PG
9	KBRST#
10	A_RST#
11	PCIRST#
12	LDT_RST#

RS880 Sequencing

1	+3.3V
2	NB POWER RAILS
3	ATX PS_PWRGD
4	NB INPUT CLOCKS
5	CPUCLK
6	NB_PWRGD
7	SB_PWRGD
8	LDT_PG/CPU_PWRGD
9	PCIRST#,NB_RST#
10	LDT_RST#
11	
12	

EC Sequencing

1	3VPCU
2	NBSWON#
3	VIN_ON
4	S5_ON
5	ICH_RSMRST#
6	-DNBSWON#
7	SUSB#/SUSC#
8	SUSON/USB_ON#
9	MAIN_ON/HWPG
10	VRON
11	PWROK
12	

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	Hole, Nuts	1A
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CHANGE LIST

Model: ZQ2 MB

REV 1A

1. A01 del Ext-CLK Gen component
2. A02 del Power VGPU-IO
3. A03 page 7,9,10 add side-port
4. A04 page9 R123 no stuff ,R129 stuff for A-test boot issue
5. A05 page9 U22.D8 change to A_RST#_SB
6. A06 page11 move dGPU_PWROK from U29.AA4 to U29.AJ6
7. A07 page11 move BOARD_ID[0:5] to U29.AC3
8. A08 page12,17 add VGA_REQ# for VGA_CLK request
9. A09 page13 move MEM_1V5 to U29.A7
10. A10 page13 update Board_ID table
11. A11 page13 add sideport table
12. A12 page 15 del R471 for just only use int-clkgen
13. A13 page 11,16 add CLK_14M_VGA for Park boot
14. A14 page 17 modify GPU_VID gpio relation
15. A15 page18 modify R86 from 680 to 51
16. A16 page19 add +3V_D_EXT for leakage issue
17. A17 page20 del don't use port for cost down

2A

B01	Page10	modify L77 footprint
B02	Page23	modify R54 stuff for Discrete,R50 for UMA
B03	Page27	modify ODD power connection
B04	Page	change 0-ohm R185,R89,R93,R136,R142,R485,R487,R488,R489,R490,R493,R503 to short pad
B05	Page12	add CLK request pull up R501,R551
B06	Page30	add Q41,Q42,R651,R652,R633 from LED board
B07	Page	add R659,R660,R661,R662 from power board
B08	Page	modify R314,R315,R316,R322 follow ZQ1
B09	Page	add Q40,and RF_LED_EN# with RF_LED# to EC
B10	Page	change U26,CN10,U12 footprint
B11	Page	C534 C537 C154 C147 C144 C129 C14 C20 C18 C17 C15 C32 C39 C50 C62 C72 C88 C87 C103 C102 C29 from CC0402-C to CC0402. L8 R48 R41 R30 L1 L14 from RC0402-C to RC0402.
B12	Page	R377 stuff ,R247 no stuff follow AMD sch.
B13	Page	change D2,D3,D23,D25,D26,D29 to BAS316
B14	Page	reserve R152,R423,L4 (USBP2)option for CCD issue
B15	Page	change U26,CN10,U12 footprint
B16	Page13	Change board ID power rail from +3V_S5 to +3V.
B17	Page10	W/O Sideport ,R146 no-stuff, C831 connect to GND
B18	Page9	no-stuff R108,R105
B19	Page28	del D20,D21,D22 &R498 from 10K->1K & add Q43,Q44,Q45

B01

3A

C01	Page02	Add H/W shutdown function and add CPU_COREPG shutdown design(add Q43,R152)
C02	Page23	Option brightness switch control just only by NB R50
C03	Page40	Change PG_GPUIO_EN pull high power rail from +3V to +3V_D_EXT. For Park GPU SG mode hang up issue.
C04	Page42	Change PR60 from 10k to 0ohm.
C05	Page30	chang LED R R660,R661,R662,R663,R314,R316,R321
C06	PageX	change R 0ohm to short pad
C07	PageX	audio for codec suggestion
C08	PageX	X.
C09	PageX	X
C10	PageX	X.
C11	PageX	X.
C12	PageX	X.

4A

D01	Page03	Change CPU VDDR_SENSE pull high power rail to CPU_VDDR and remove trace connect to controller IC.
D02	Page15	Modify text note.
D03	Page12	Change "GBE_COL" ,"GBE_CRS" ,"GBE_RXERR" to GND follow SCL V1.04 version.
D04	Page14	Change USB PLL power rail source to separate VDDPL_33_USB_S follow SCL V1.04 version.
D05	Page04	R409 no stuff, R413 stuff
D06	Page09	del PD5, PR124-390k for panasonic battery low power protect issue.
D07	Page36	PR229 no stuff
D08	Page23	C212,C213,C214,C220,C221,C222 from 33p to 10p
D09	Page21	modify DDR3 Memory table
D10	Page28	R568 stuff and R498 no stuff for Audio issue
D11	Page2/4	Q3 pin 3 change to PM_THERM#,Q3 pin 8 add PM_THERM#
D12	Page23	reserve C541 for monitor test issue

3C

MODEL	ZQ2 FROM	ZQ2 To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B

DOC NO.	PROJECT MODEL :	ZQ2	APPROVED BY:		DATE: 2009/08/13
	PART NUMBER:		DRAWING BY:		REVISON: 1A

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	Change list	1A
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