

VER : 1A

ZQ2B SOLE UMA SYSTEM DIAGRAM



Danube Platform
(Main Stream)

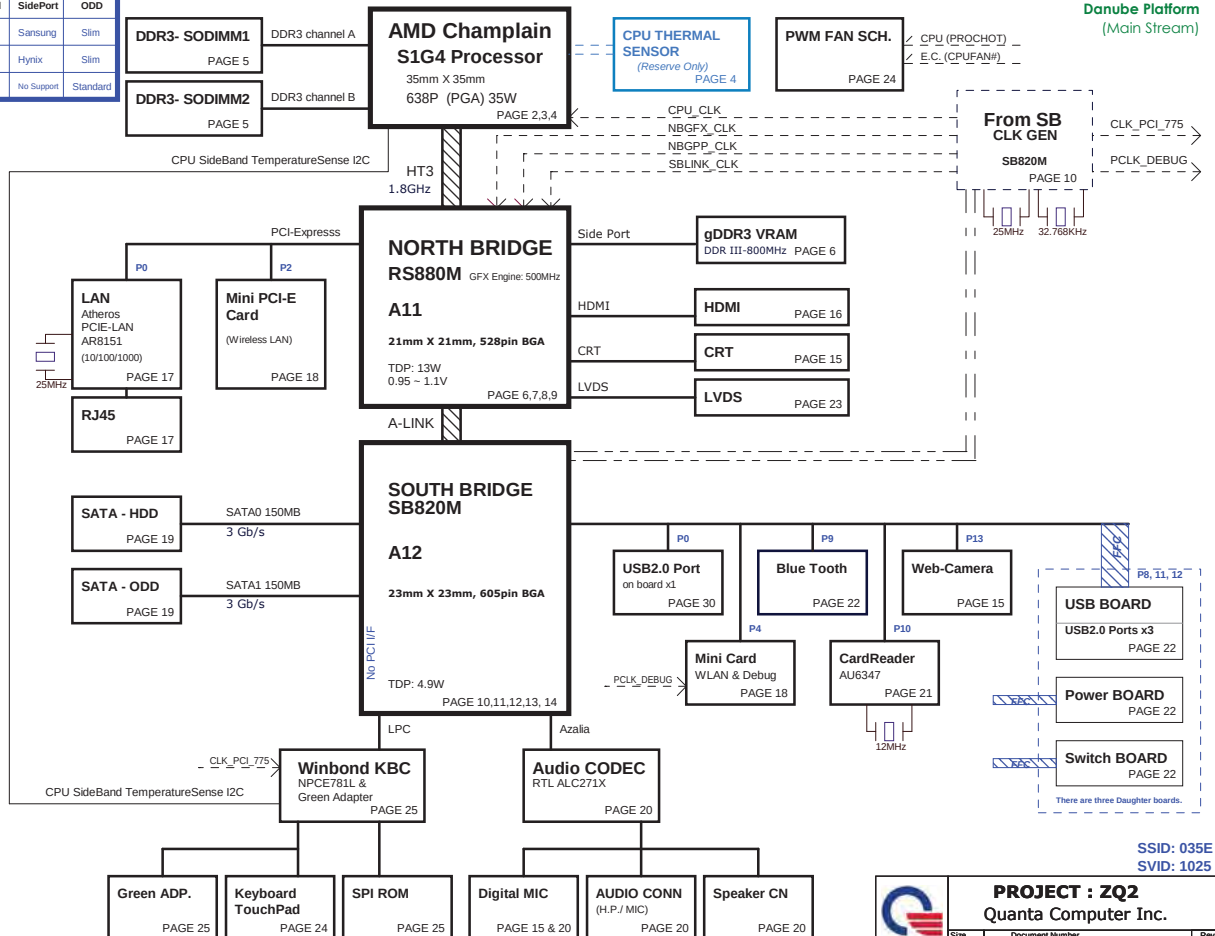
BOM P/N	Description	Model	SidePort	ODD
31ZQ2MB00A0	ZQ2B 6L JM MB (WIGRN,SAM,WIO CPU)ASSY	JM	Samsung	Slim
31ZQ2MB00E0	ZQ2B 6L JM MB (WIGRN,HYU,WIO CPU)ASSY	JM	Hynix	Slim
31ZQ2MB00H0	ZQ2B 6L JV MB (WIGRN,WIO CPU,VRAM)ASSY	JV	No Support	Standard

PCB STACK UP

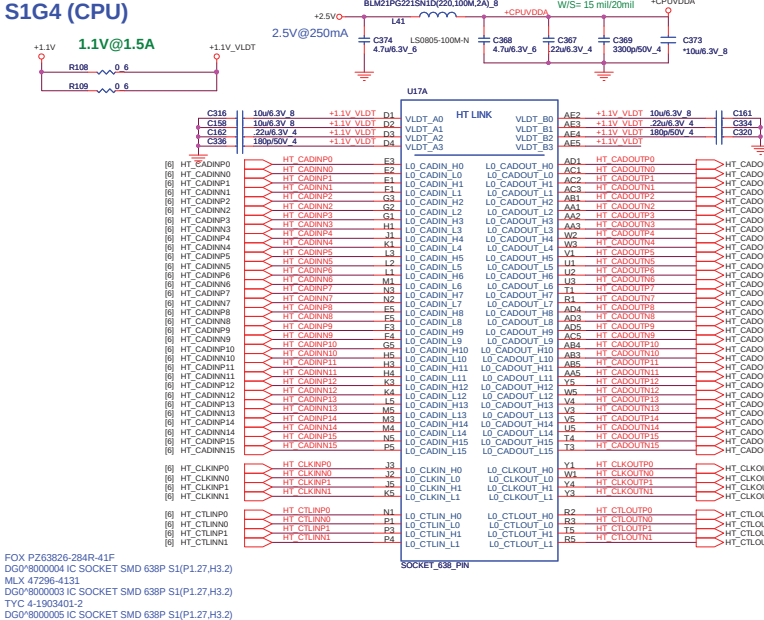
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

IV@ -> IGPU
SP@ -> Option Notice
SIDE@ -> SidePort VRAM
GA@ -> Green Adapter (Default stuff)

Sideport-L75,L76,R583,R392,C832,R455,R550,R502
NB A11-R105,R108
SB A12-R267,R271
JV/JM-CN16,R450,R456
EC-D8,D27
UMA-R461
VRAM-R358,R359,R360,R363,R365,R72

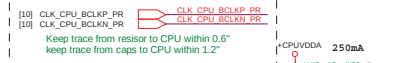


S1G4 (CPU)

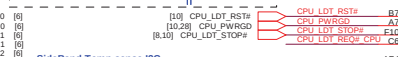


FOX PZ63268-284R-41F
DGO#8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DGO#8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DGO#8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)

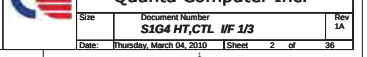
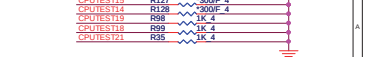
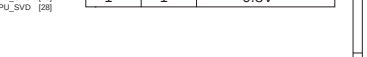
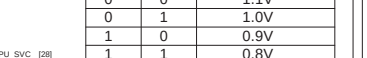
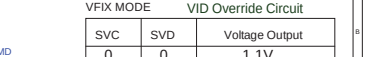
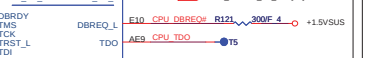
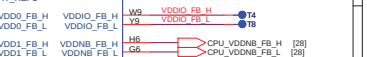
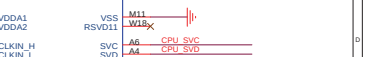
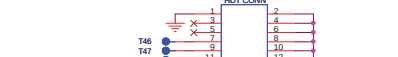
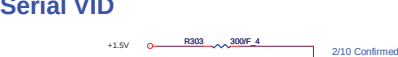
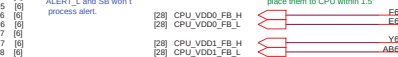
CPU CLK



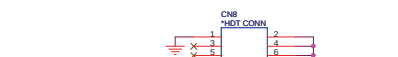
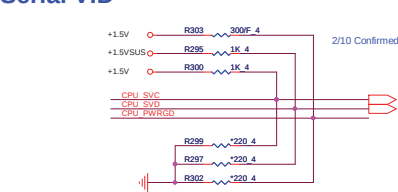
Keep trace from resistor to CPU within 0.6"
Keep trace from caps to CPU within 1.2"



SideBand Temp sense I2C
Ellet (02/26)
Current Agessa bios
Alert L and SB won't
process alert.



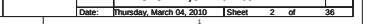
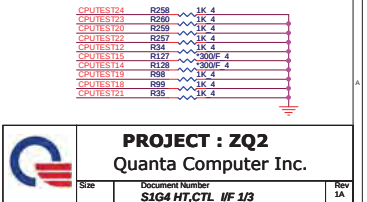
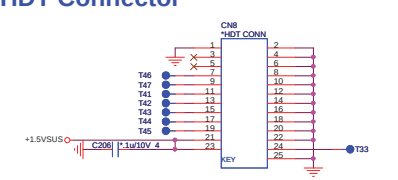
Serial VID



VFX MODE VID Override Circuit

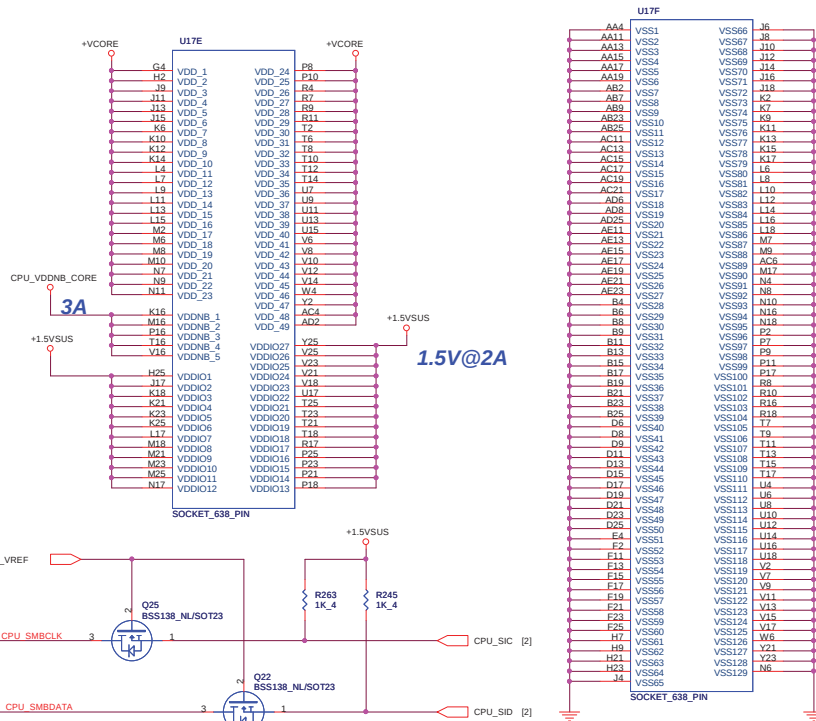
SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

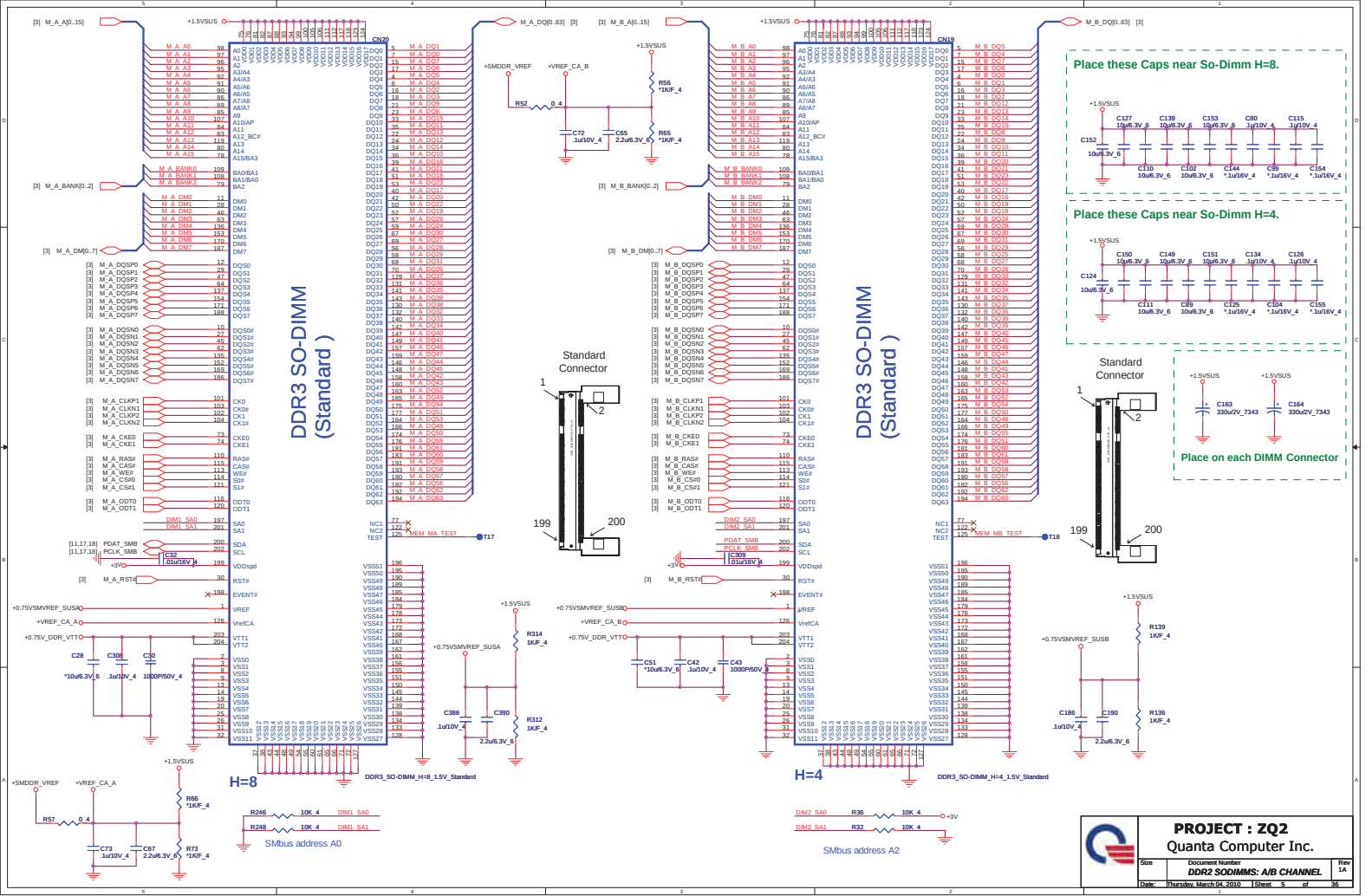
HDT Connector



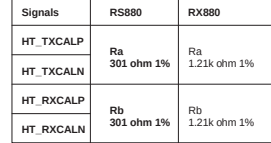
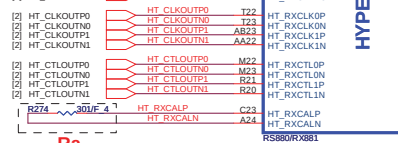
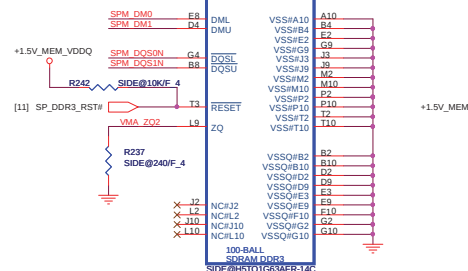
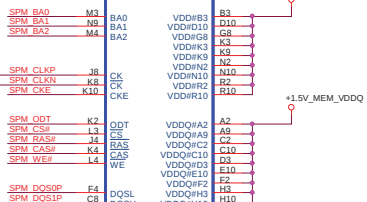
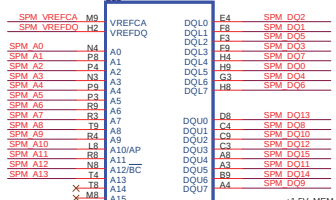
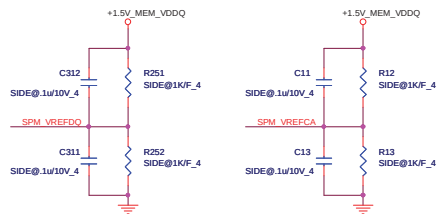
Size Document Number
S1G4 HT,CTL IF #13

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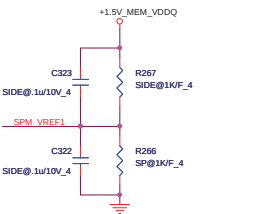
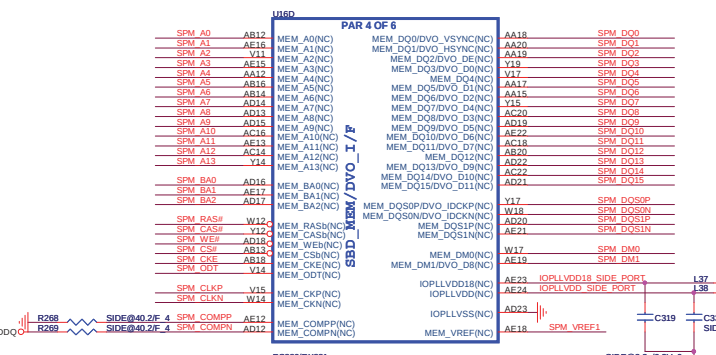


SIDE PORT

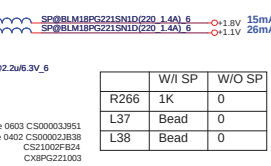


RES CHIP 1.21K 1/16W +/-1%(0402)
P/N : CS21212FB18

This block is for Side-Port only



IOPLLVD18 - memory PLL
not applicable to RX881



PROJECT : ZQ2
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Size	Document Number RS880M-HT LINK I/F 1/4	F
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For Check list JTAG

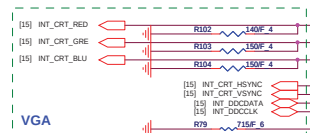


For A11 version

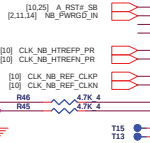
(02/10) Don't need 49.9 ohm PD.



All RS880 variants do not support analog TV-out functionality. As such, Y, C, Pr, and COMP_Pb



20mA
120mA



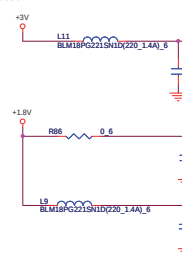
[16] HDMI_DDC_DATA

[16] HDMI_DDC_CLK

[00] +NB_CORE_ON

T74

RS880M --- ADD



STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO.

RS880M	1 Disable	V
0 Enable		

INT_CRT_HSYNC R277 3K 4 -> +3V

RS880M: Enables Side port memory

RS880M:INT_CRT_HSYNC

Selects if Memory SIDE PORT is available or not

1 = Memory Side Port Not available

0 = Memory Side port available

Register Readback of strap: NB_CLKCFG.CLK_TOP_SPARE_D[1]



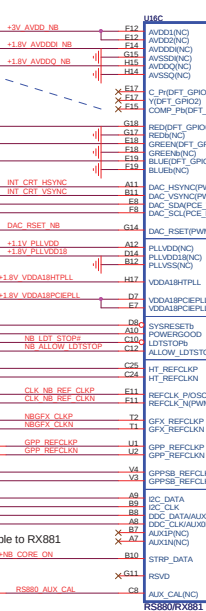
For extrnal EEPROM Debug only

RS780/RX780/RS880

+NB_CORE_ON R278 20K 4 -> +3V

Display Port interface from PCIeGraphics (RS880/rs880M only)

RS880 AUX_CAL R282 150F 4 -> +3V



PART 3 OF 6

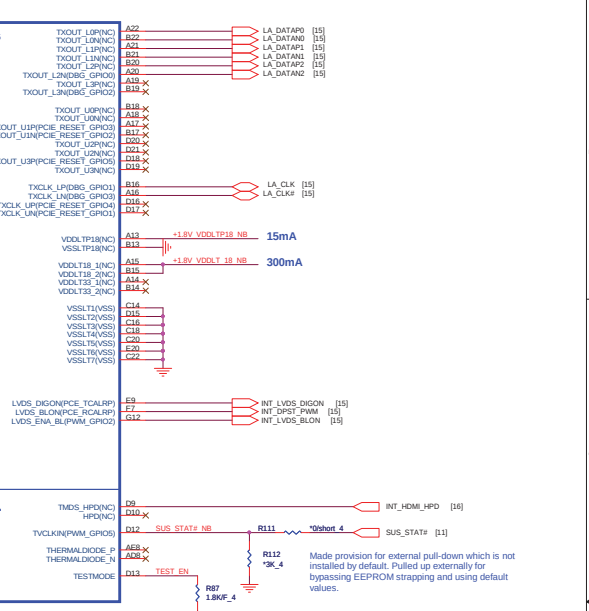
CRTVOUT

PLL PWR

LVTM

CLOCKS

MIS.

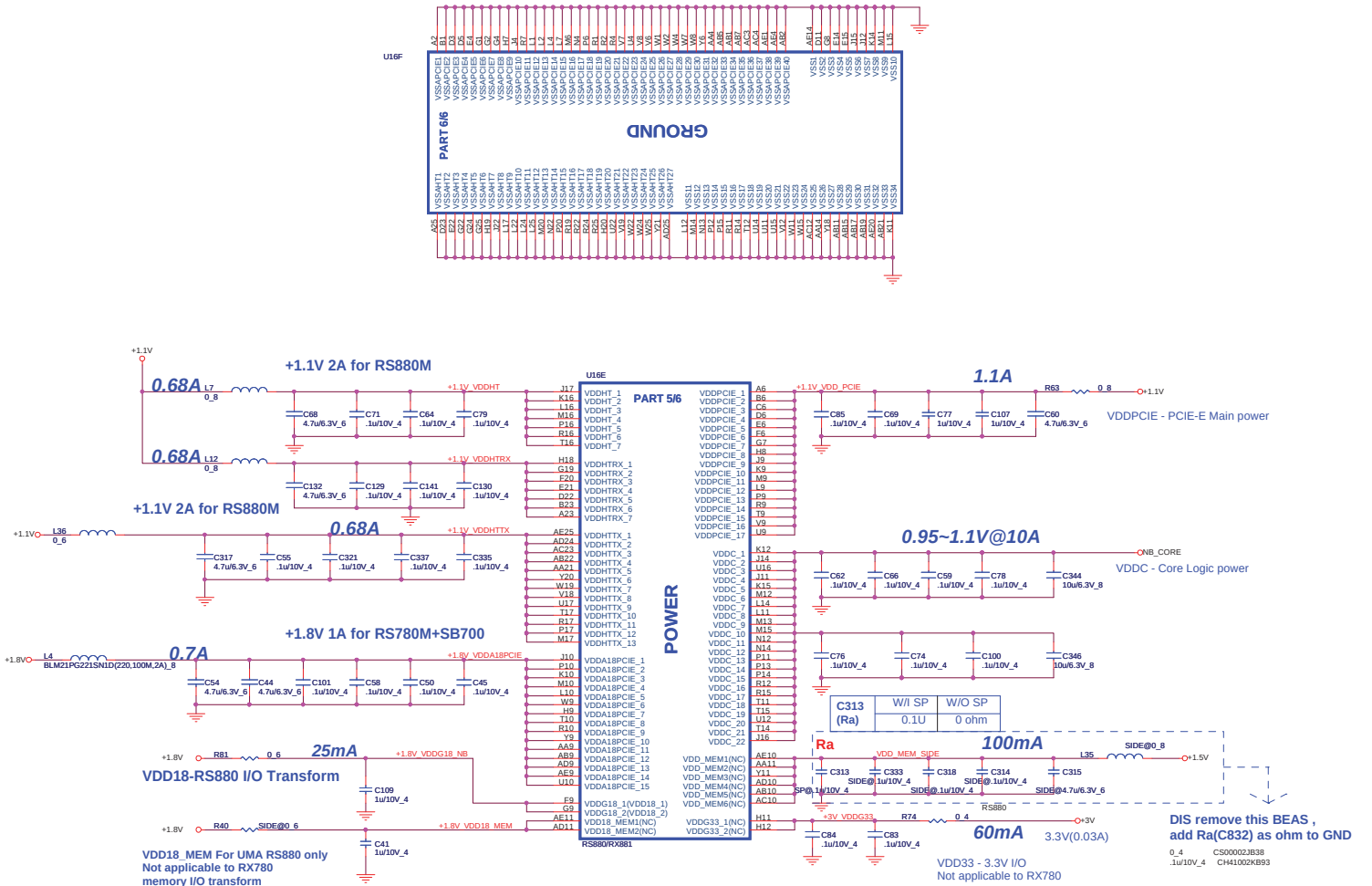


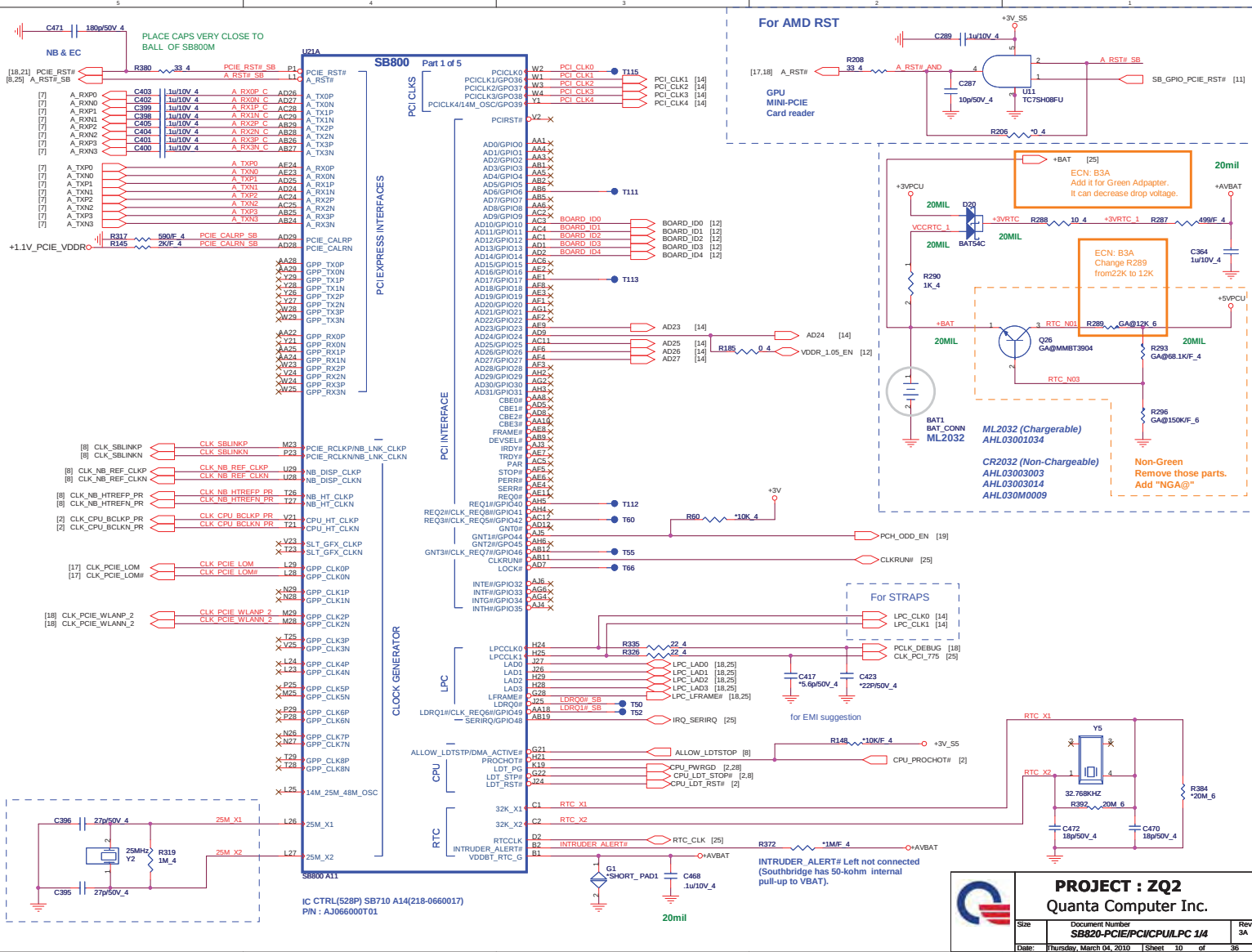
Made provision for external pull-down which is not installed by default. Pulled up externally for bypassing EEPROM strapping and using default values.



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	RS880M-SYSTEM I/F 3/4	1A
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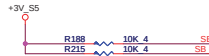
NC only ,Can't be install



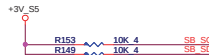
SCL0/SDATA0 is 3V tolerance. AMD datasheet define it
Clk Gen/ Robson/ TV tuner/ DDR2/ Thermal/ Accelerometer



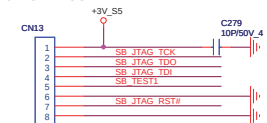
SCL1/SDATA1 is 3V/5S tolerance
AMD datasheet define it



SCL2/SDATA2 is 3V/5S tolerance.
AMD datasheet define it

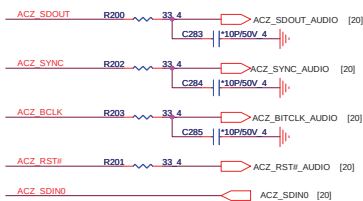


JTAG DEBUG



*SW JTAG DEBUG

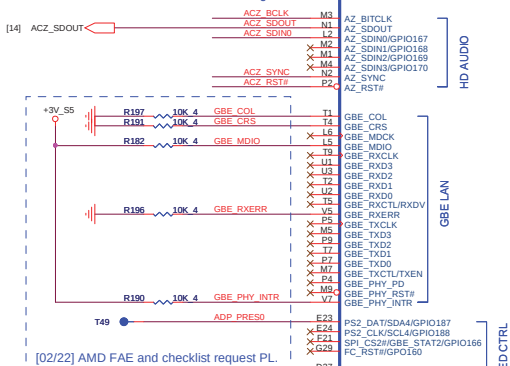
To Azalia



Elitor (02/26)

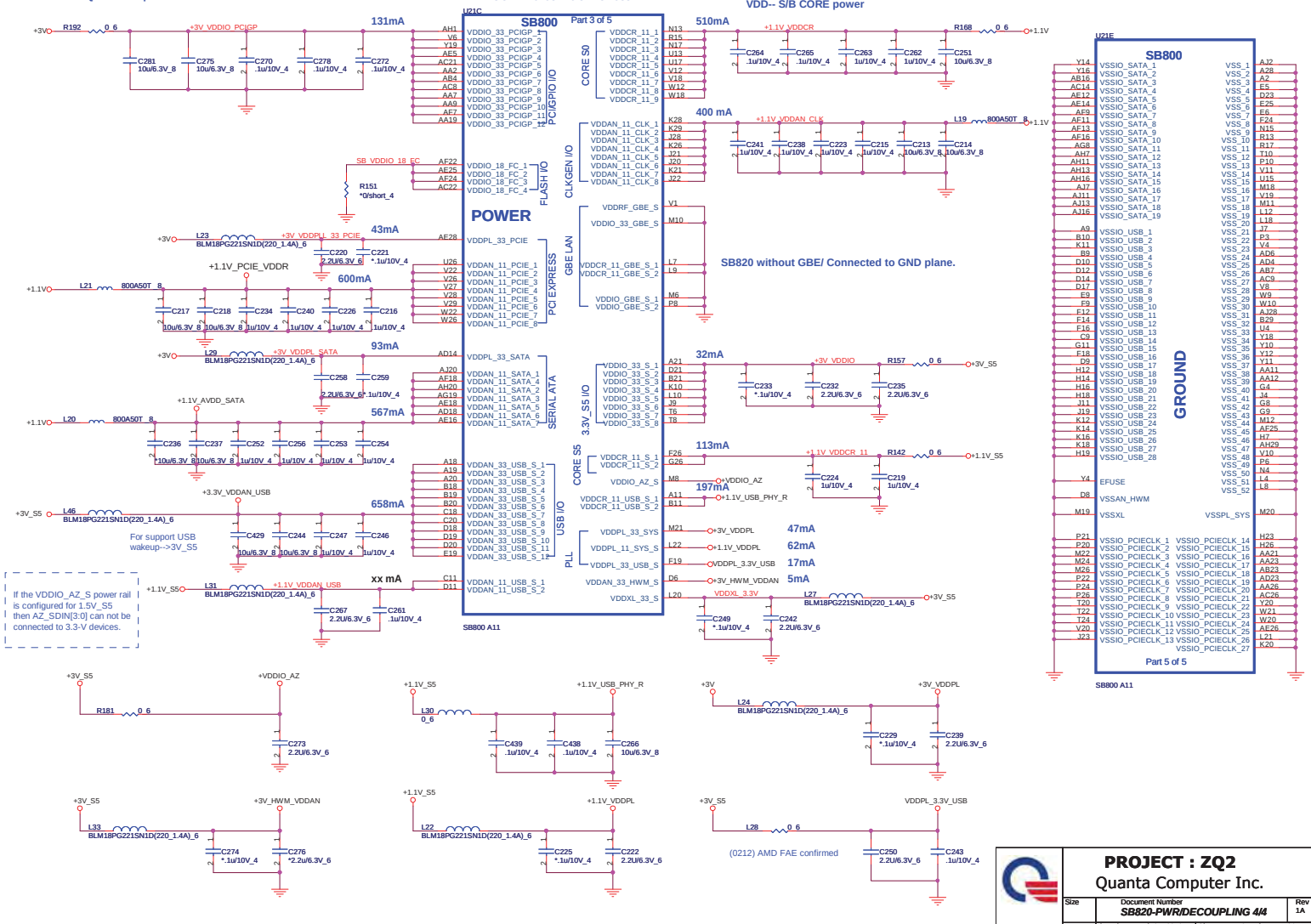
Current Agesa bios doesn't
program ALERT_L and SB
won't process alert.

HD audio interface is +3V5S voltage



PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

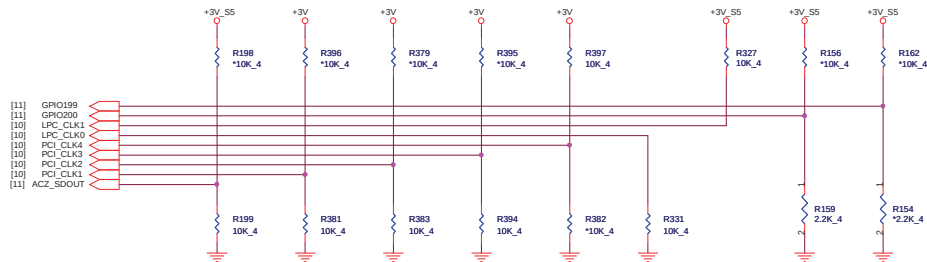
PROJECT : ZQ2
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REQUIRED STRAPS

SB820M is supported Gen1 mode only.

For internal clock GEN.

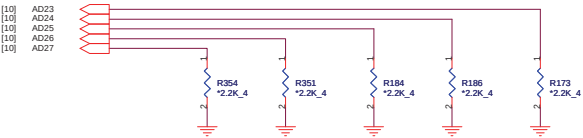


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM L, L=FWH ROM	DEFAULT

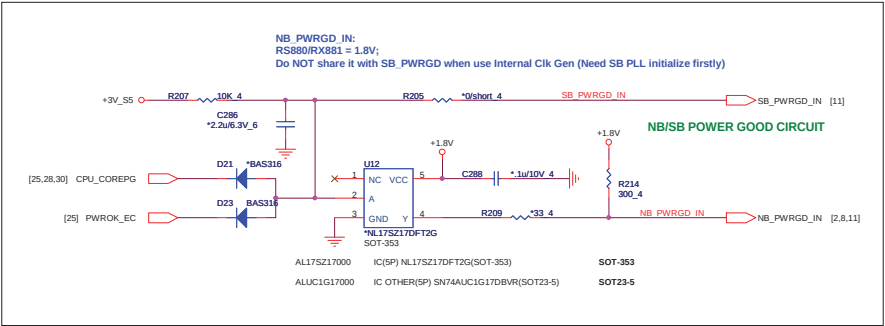
internal have pull Hi 10K

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



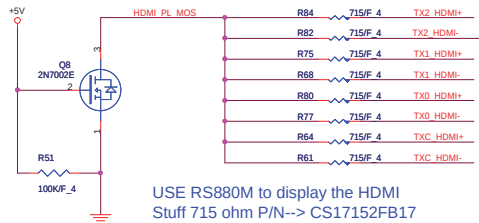
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



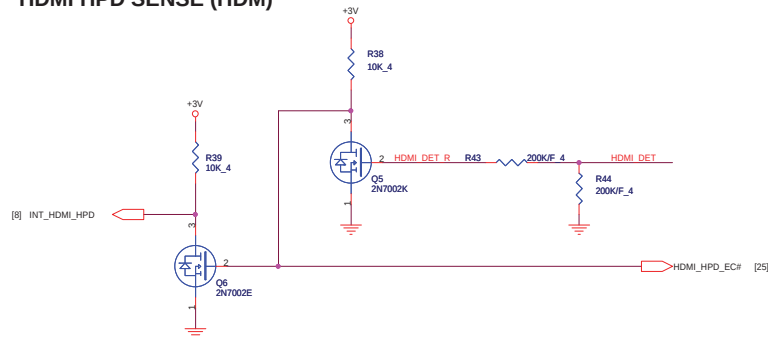
HDMI (HDM)



Close to HDMI Connector



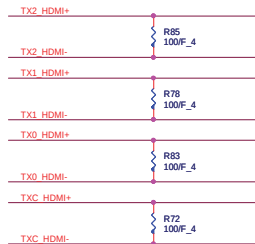
HDMI HPD SENSE (HDM)



HDMI PORT (HDM)

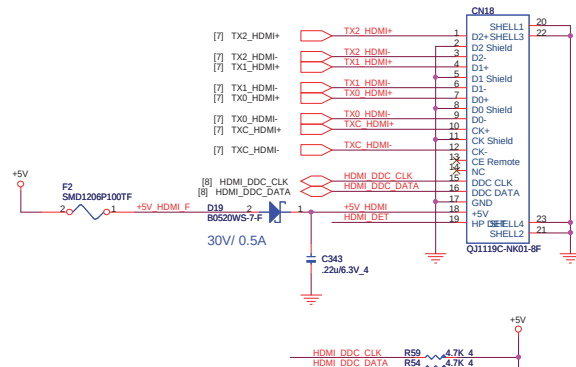
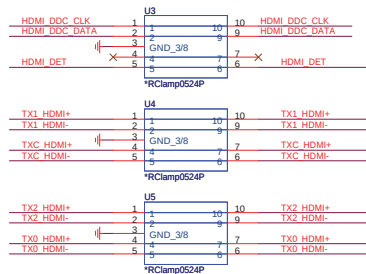
EMI reserve for HDMI(EMC)

Close connector



ESD Protect (EMC)

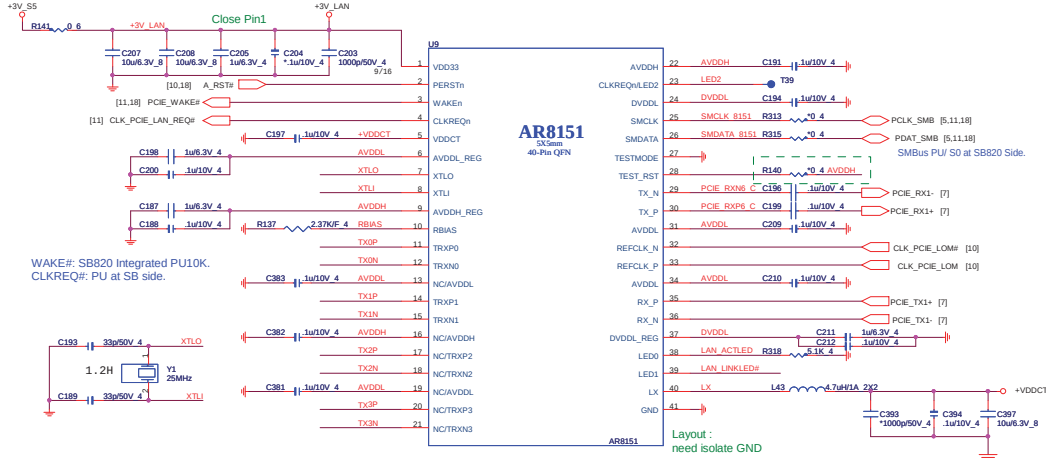
close to HDMI connector



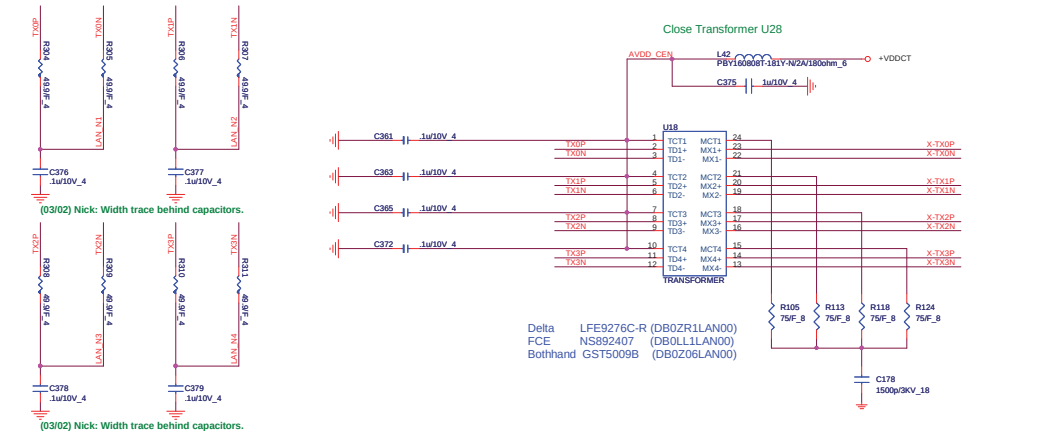
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Quanta Computer Inc.

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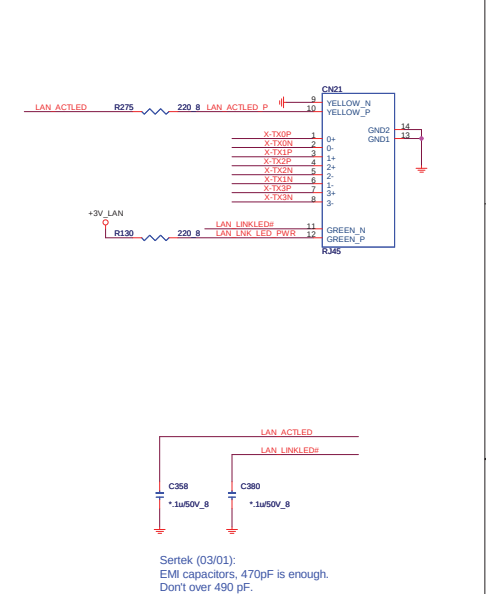
Giga-LAN AR8151



TRANSFORMER(LAN)



RJ45(LAN)



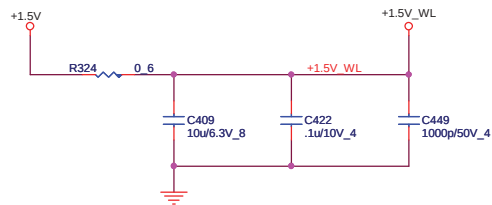
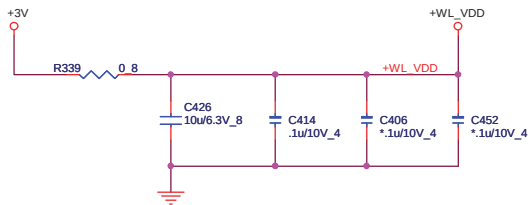
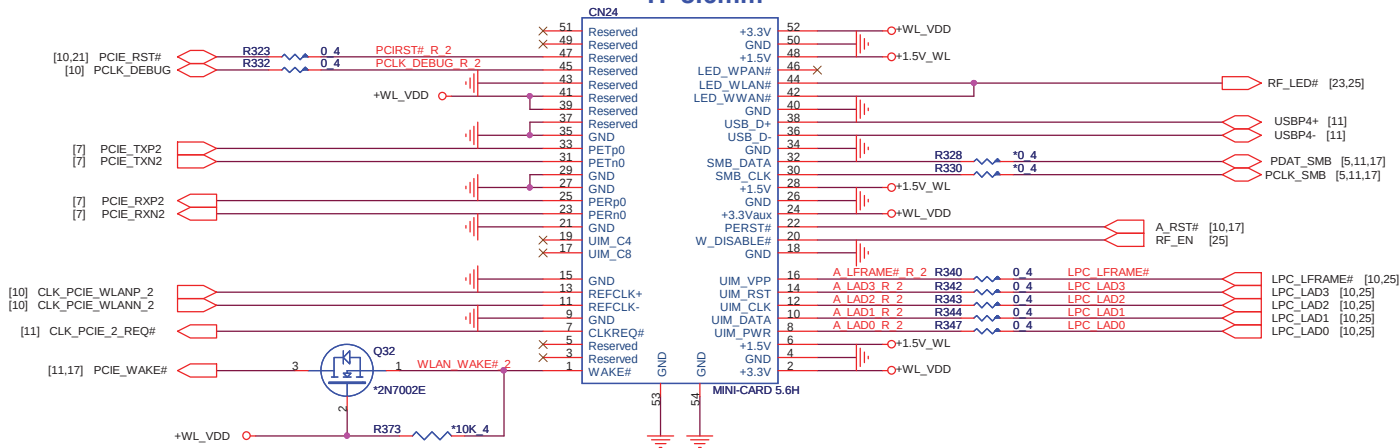


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MINI-CARD WLAN(MNC)

H=5.6mm



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	Mini-Card/WL	1A
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4



1

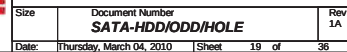


C

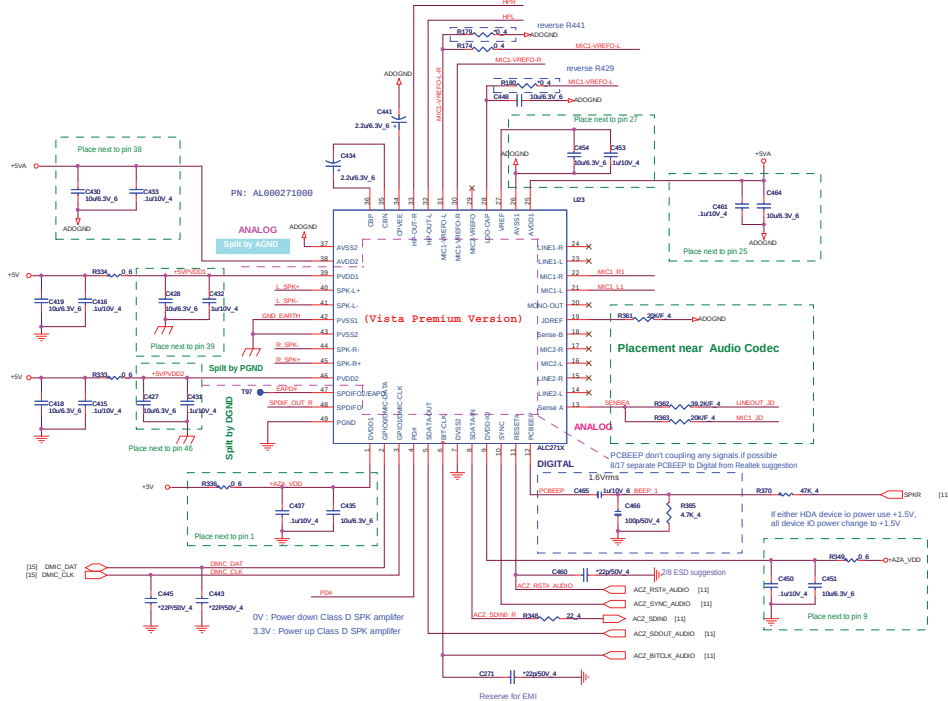


1

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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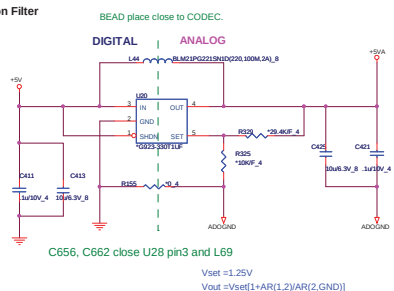


Codec(ADO)

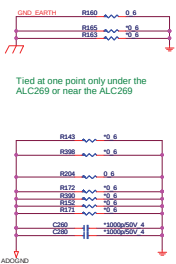


Power (ADO)

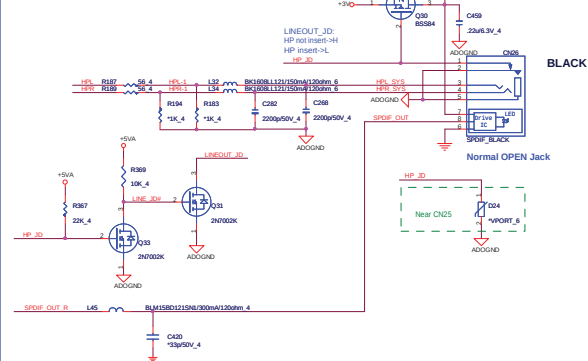
Demodulation Filter



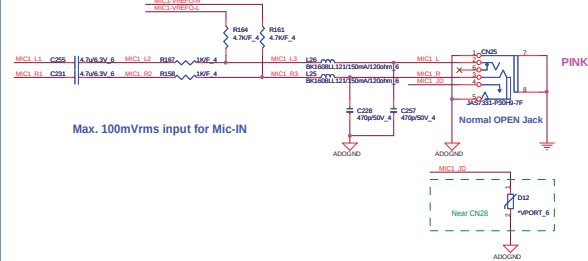
GND_EARTH don't coupling AGND and SPK signals



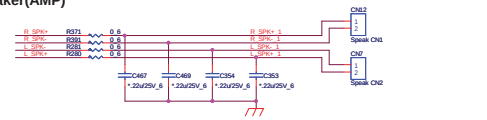
LINE-OUT/SPDIFO(AMP)



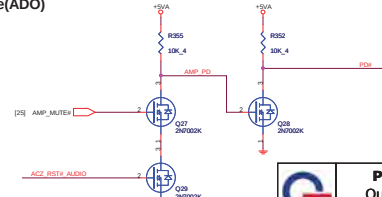
MIC(AMP)



Internal Speaker(AMP)

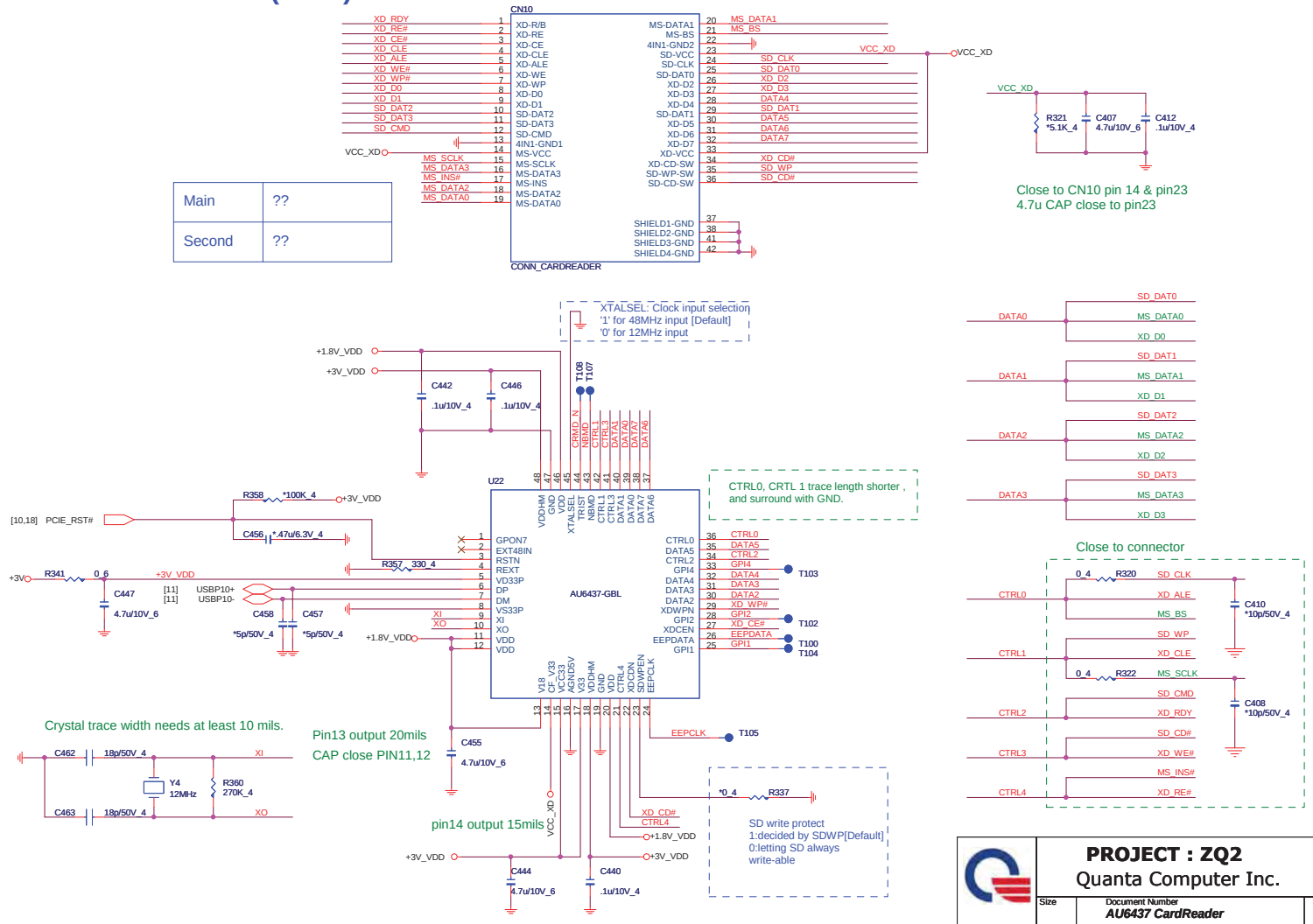


Mute(ADO)

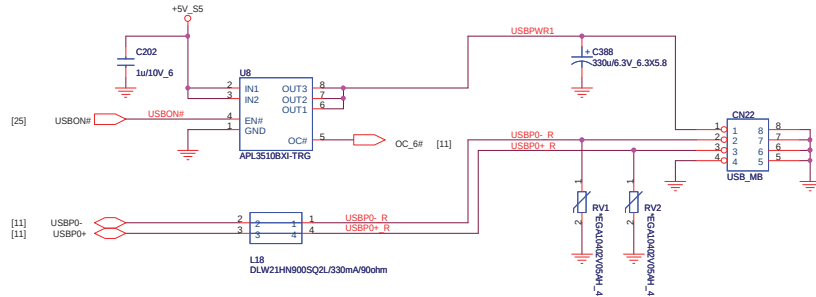


4 IN 1 CARD READER (MMC)

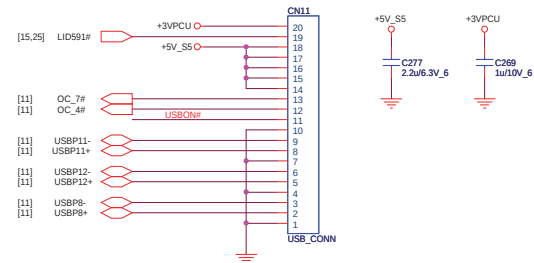
Main	??
Second	??



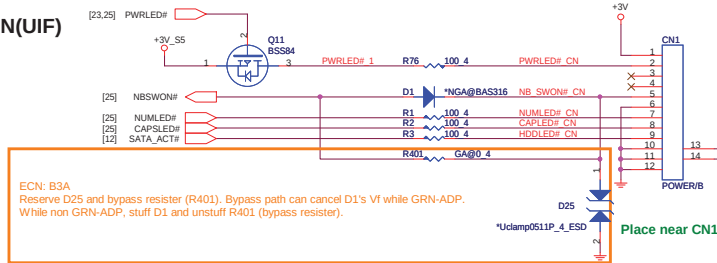
USB PORT(USB/MB)



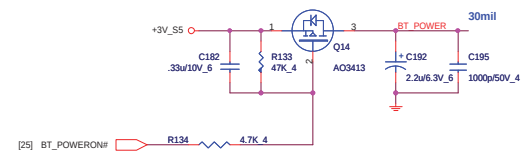
USB BOARD CONN(USB/SB)



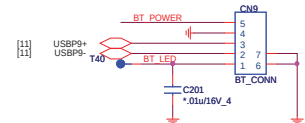
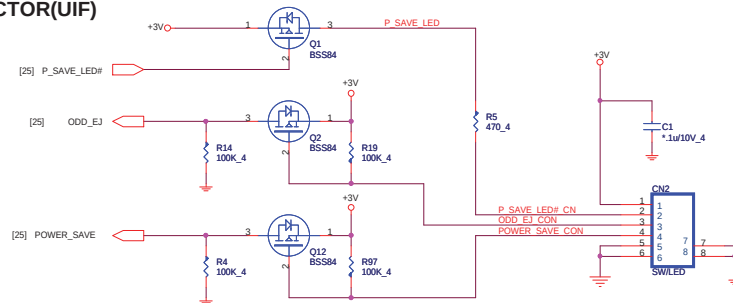
POWER BOARD CONN(UIF)



BLUETOOTH CONN(BTM)



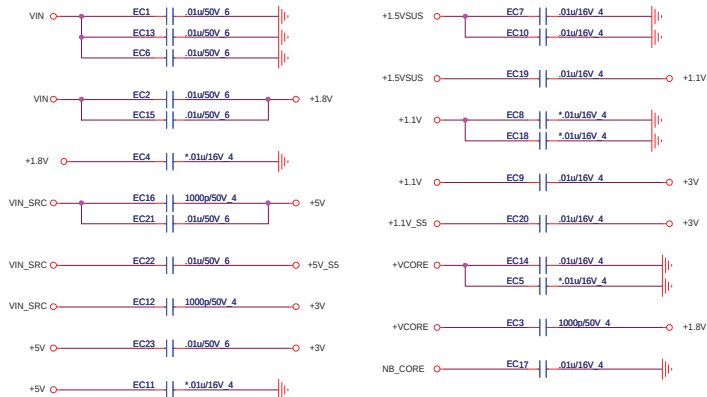
LED BOARD CONNECTOR(UIF)



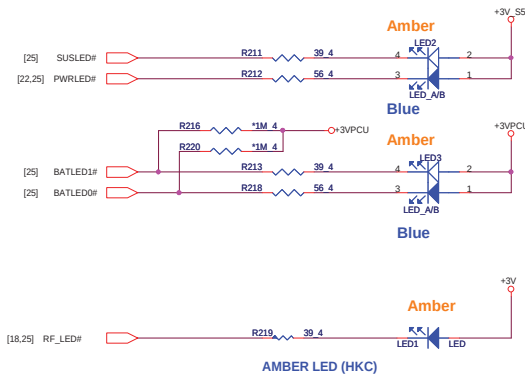
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Quanta Computer Inc.

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	USB/BT/TP	3A
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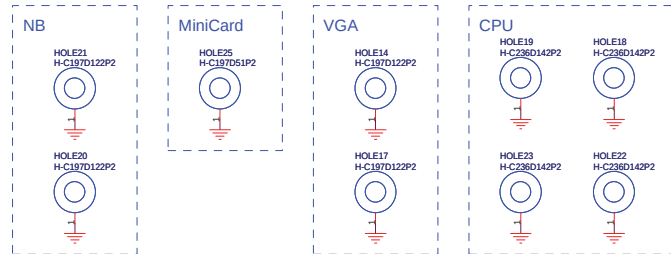
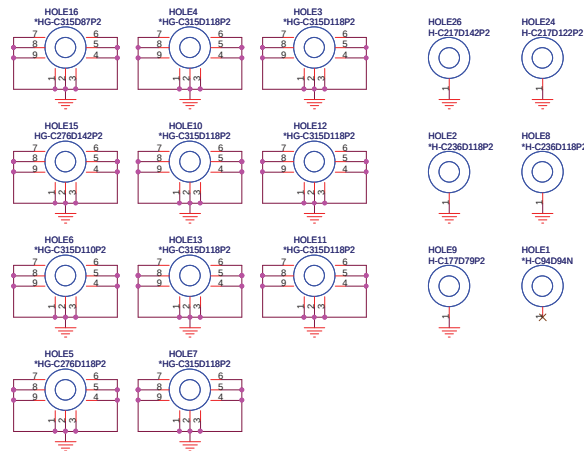
EE RETURN-PATH CAPACITORS(EMC)



LED(UIF)



HOLE(OTH)



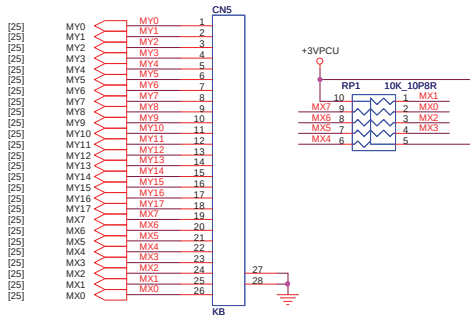


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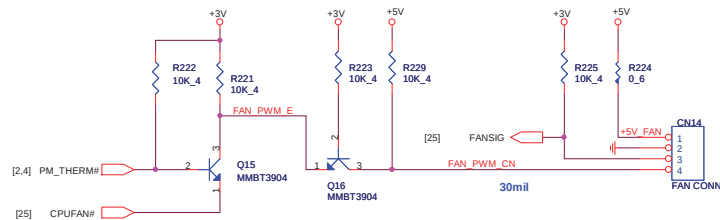
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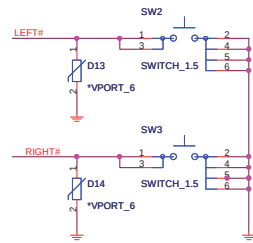
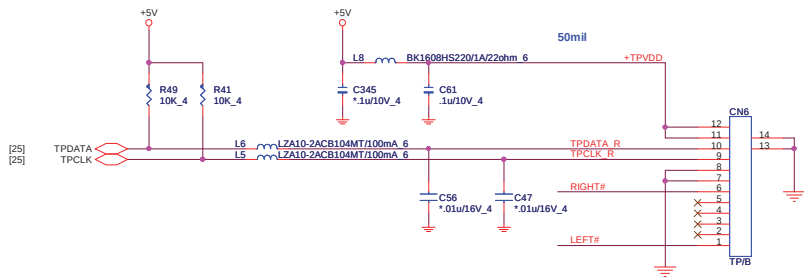
K/B(KBC)



CPU FAN(THM)

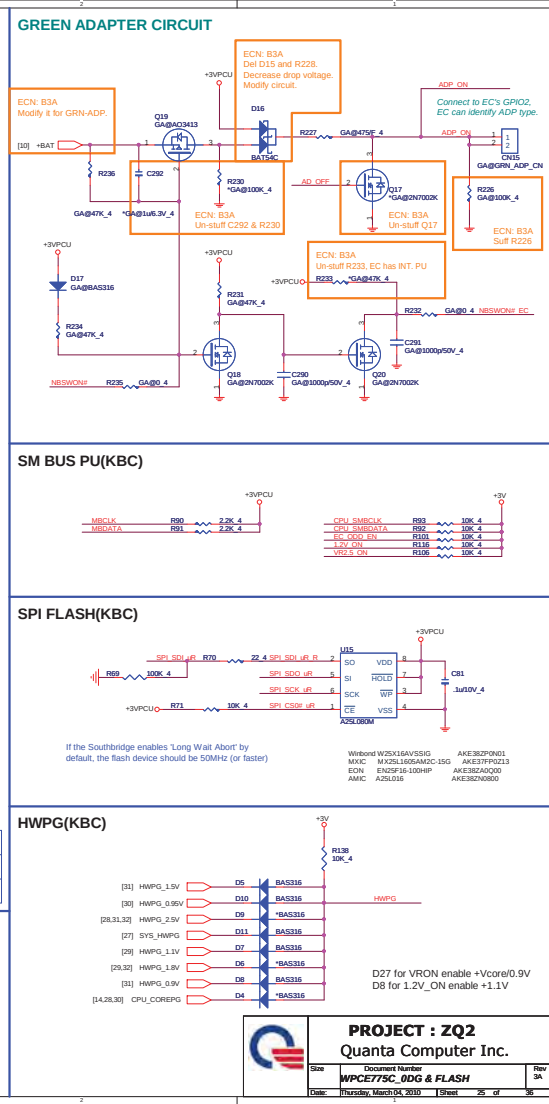
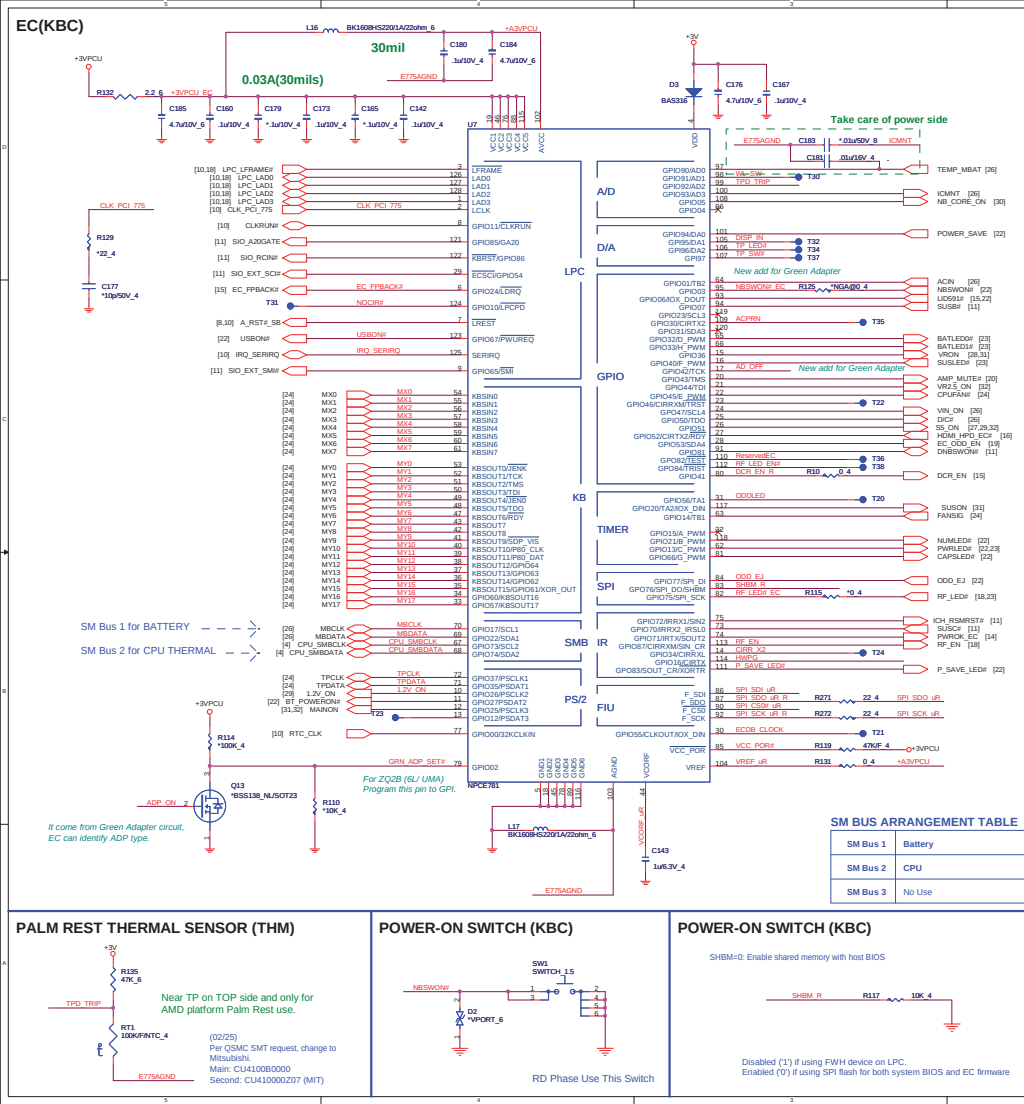


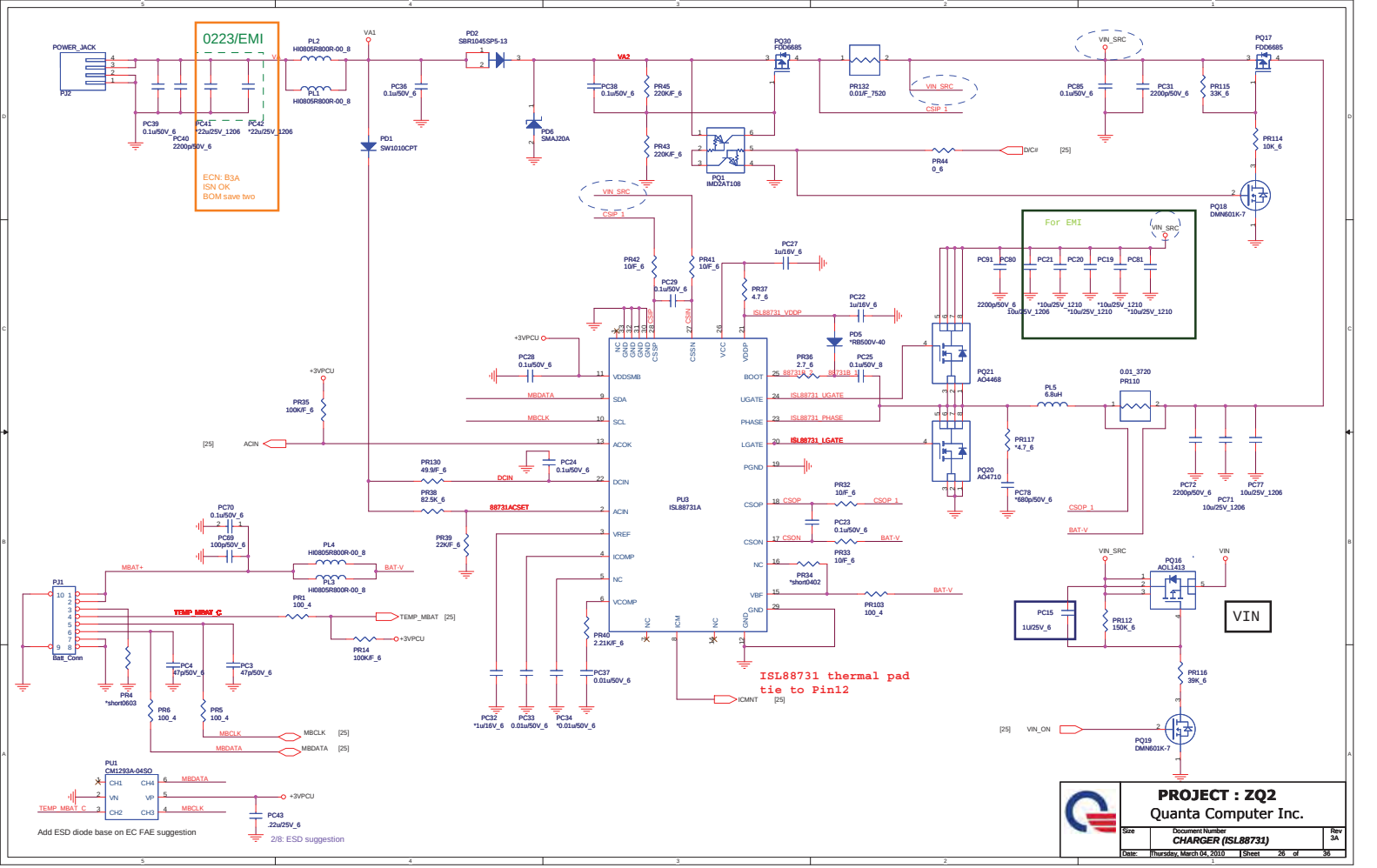
TOUCHPAD BOARD CONN(TPD)

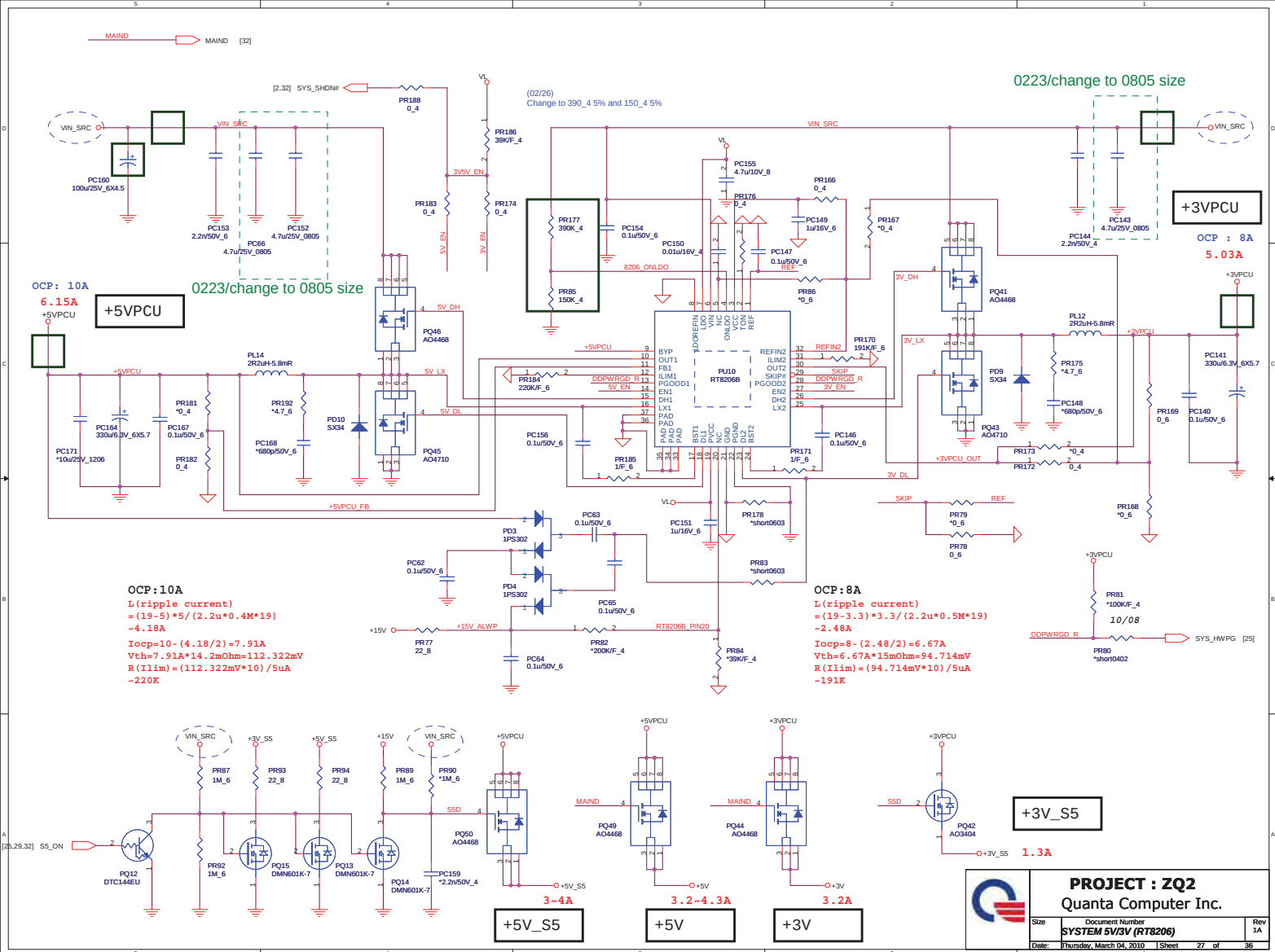


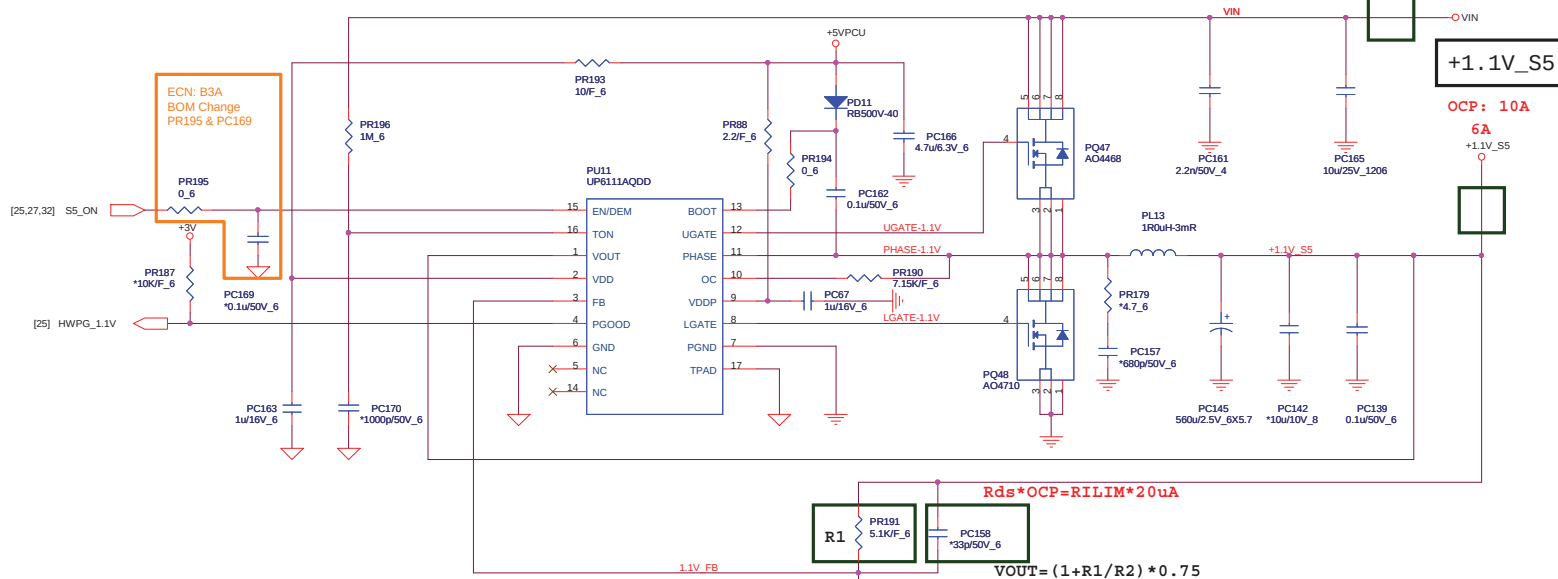
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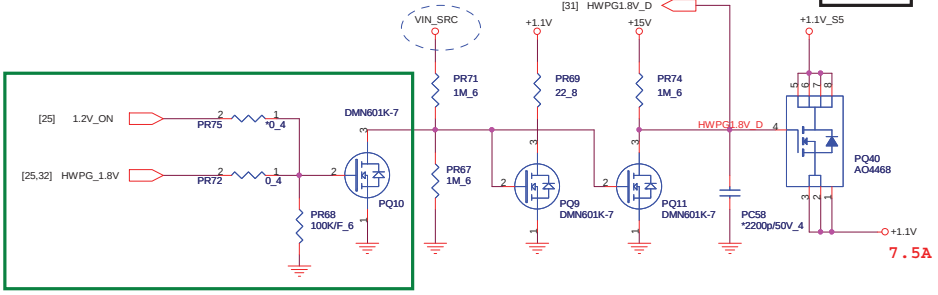




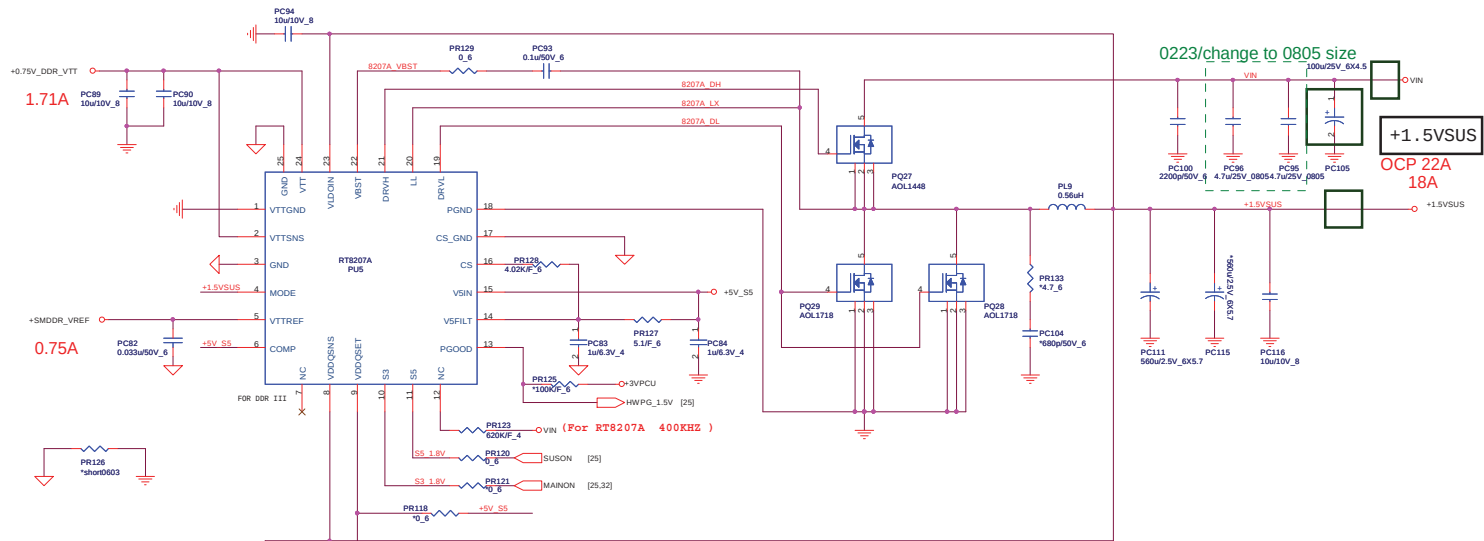
$TON = 3.85p \cdot RTON \cdot Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin \cdot TON)$
 $TON = 3.85p \cdot 1M \cdot 1 / (Vin - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

AO4710 $R_{dson} = 11.7 \sim 14.2m\Omega$
 $L(\text{ripple current}) = (19 - 1.1) \cdot 1.1 / (1u \cdot 272k \cdot 19) \sim 3.81A$
 $14.2m \cdot 10 = RILIM \cdot 20uA$
 $RILIM = 7.1K \sim 7.15K$

$R_{ds} \cdot OCP = RILIM \cdot 20uA$
 $VOUT = (1 + R1/R2) \cdot 0.75$

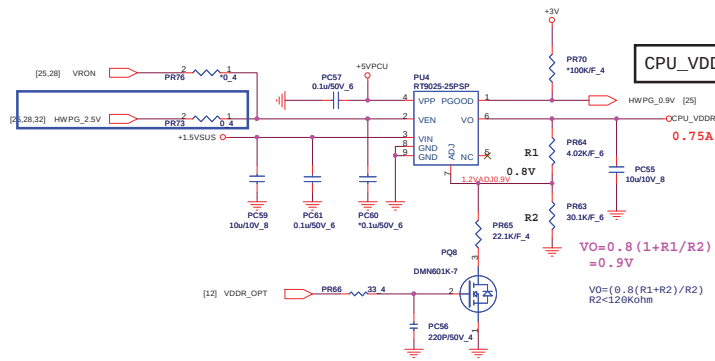
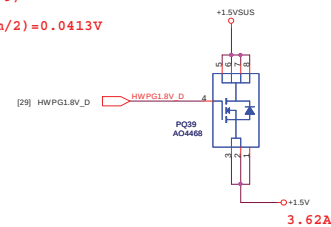


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	VCCP 1.1V(UP6111A)		
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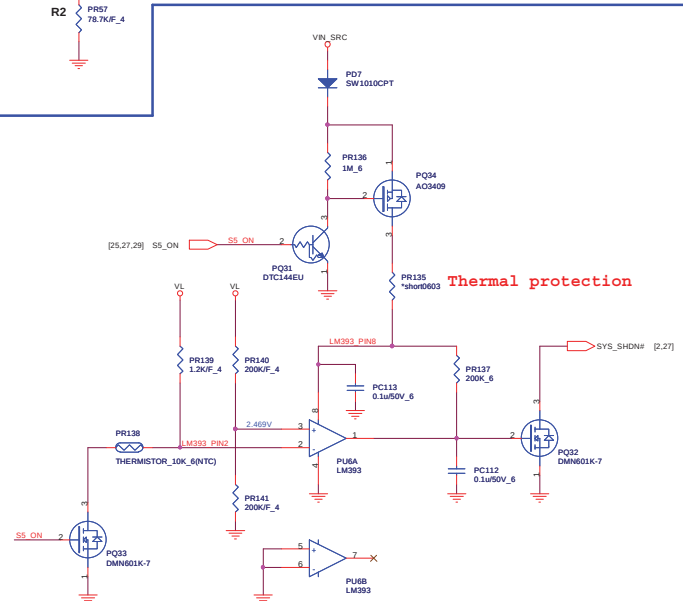
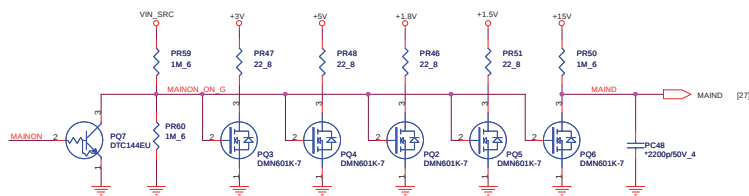
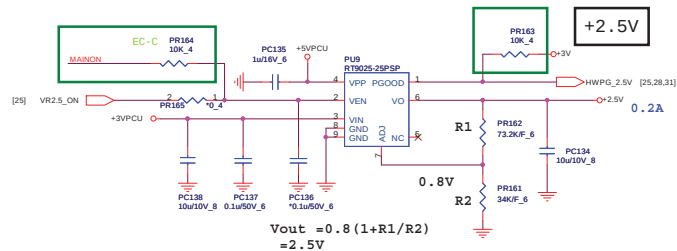
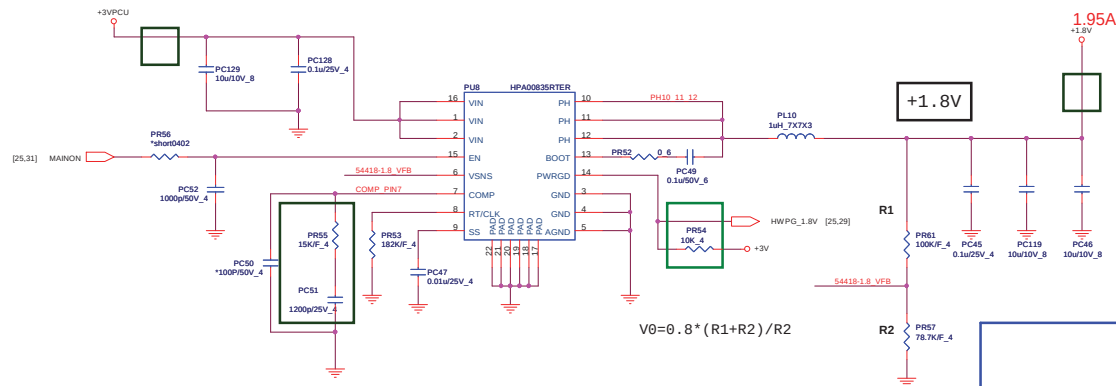


$$V_{out} = (PR_{150}/PR_{149}) \times 0.75 + 0.75$$

```
A01718 Rdson=3.8~4.3mOhm
L(ripple current)
=(9-1.5)*1.5/(0.56u*400k*9)
~5.58A
Vtrip= (22-2.79) (*4.3mohm/2)=0.0413V
RILIM=Vtrip/10uA~4.13K
```

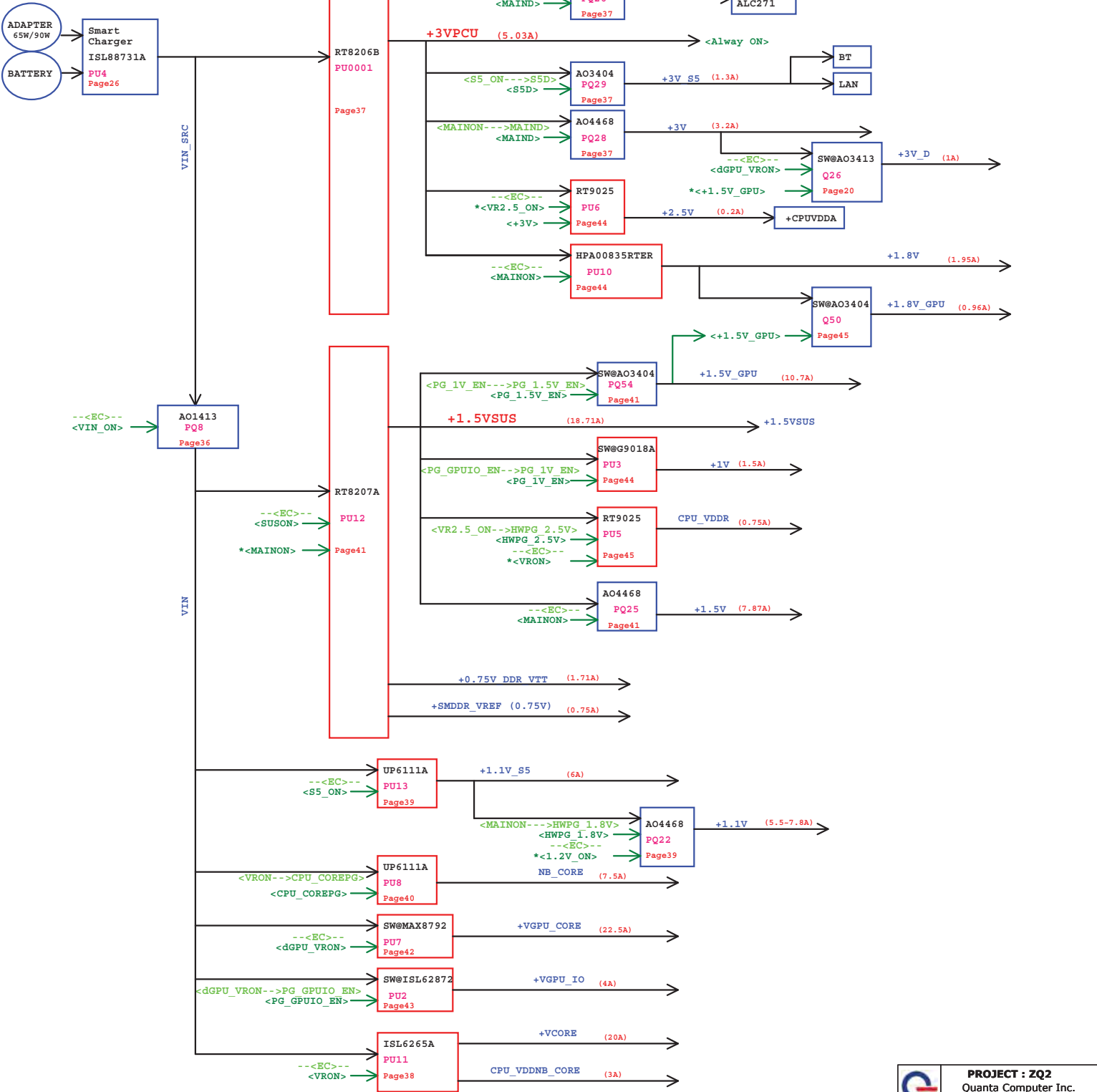


CPU_VDDR (0.9V)



For EC control thermal protection (output 3.3V)

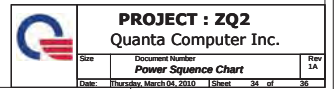
ZQ2B Power tree

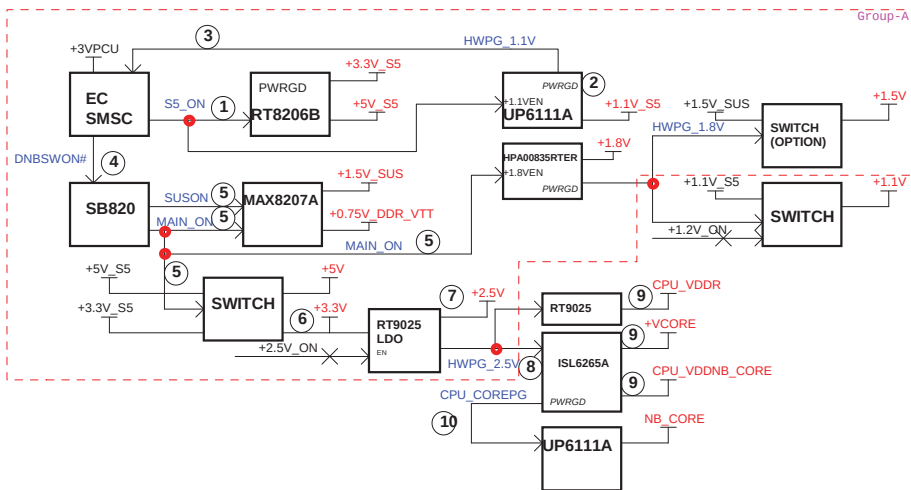


SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 3
6, 50uS <= All power rails except +3.3V
7, 100uS <= +3.3VALW_R <= 40mS

RS880:

- 1, $0 < (+3.3V) - (+1.8V) < 2.1$
- 2, +1.8V ramp before +1.1V
3. +1.1V ramp before VCC_NB





Power on Sequence required:

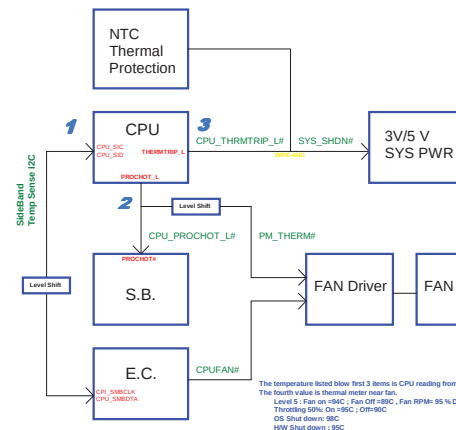
SB800:

1. +3.3V_S5 ramp before +1.1_S5
2. +3.3V ramp before +1.8v
3. +1.8v ramp before +1.1v
4. +3.3v ramp before +1.1v
5. +3.3VALW_R ramping down time > 300us
6. 50uS <= All power rails except +3.3VALW_R <= 40mS
7. 100uS <= +3.3VALW_R <= 40mS

RS880:

1. $0 < (+3.3V) - (+1.8v) < 2.1$
2. +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB

H/W Thermal Follow Chart



POWER RAILS Sequencing

1	S5_ON	13	+1.8V
2	+3.3V_S5	14	HWP_G_1.8V
3	+5V_S5	15	+1.5V
4	+1.1V_S5	16	+2.5V
5	HWP_G_1.1V	17	HWP_G_2.5V
6	DNBSWON#	18	CPU_VDDNB_CORE
7	SUSON	19	+VCC_CORE
8	+1.5V_SUS	20	CPU_VDDR
9	+SMDR_VTERM	21	CPU_COREPG
10	MAIN_ON	22	+1.1V
11	+5V	23	NB_CORE
12	+3.3V	24	

SB820 Sequencing

1	+3.3V_S5
2	ICH_RSMRST#
3	S0 POWER
4	PCIE_RCLKP/N
5	PCICLK[4:0]
6	SB_PWRGD_IN
7	NB_PWRGD_IN
8	LDT_PG
9	KBRST#
10	A_RST#
11	PCIRST#
12	LDT_RST#

RS880 Sequencing

1	+3.3V
2	NB POWER RAILS
3	ATX PS_PWRGD
4	NB INPUT CLOCKS
5	CPUCLK
6	NB_PWRGD
7	SB_PWRGD
8	LDT_PG/CPU_PWRGD
9	PCIRST#_NB_RST#
10	LDT_RST#
11	
12	

EC Sequencing

1	3VPCU
2	NBSWON#
3	VIN_ON
4	S5_ON
5	ICH_RSMRST#
6	-DNBSWON#
7	SUSB#/SUSC#
8	SUSON/USB_ON#
9	MAIN_ON/HWP_G
10	VRON
11	PWROK
12	



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