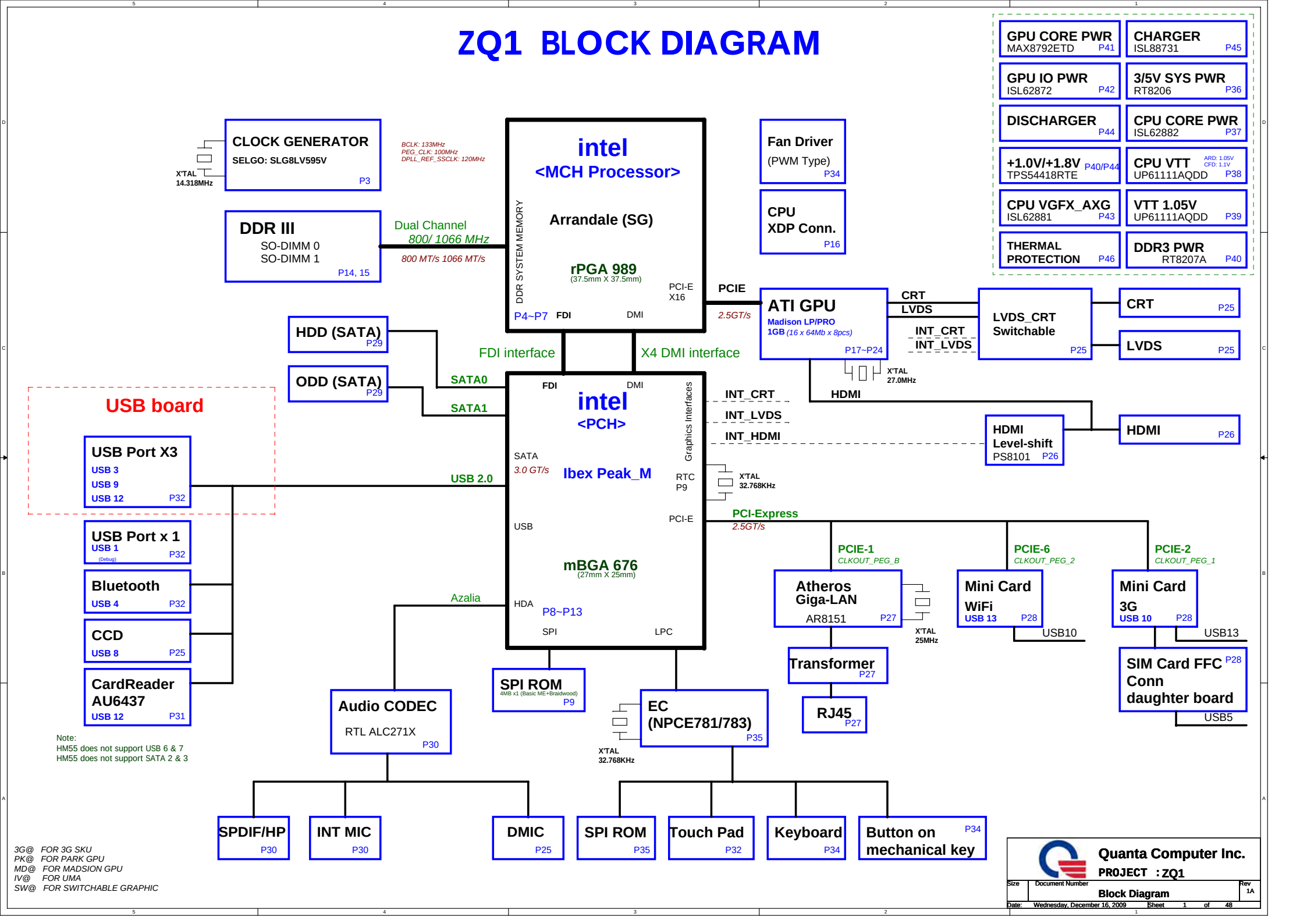
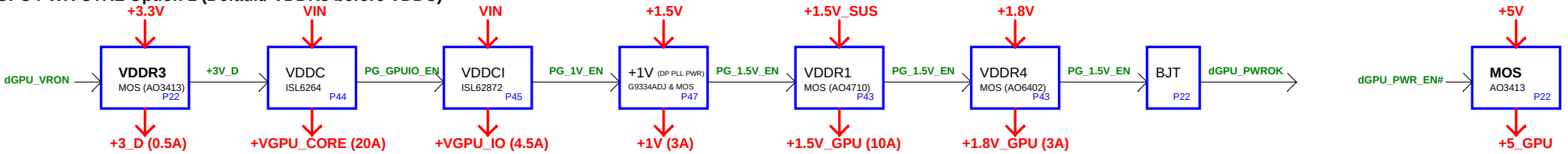
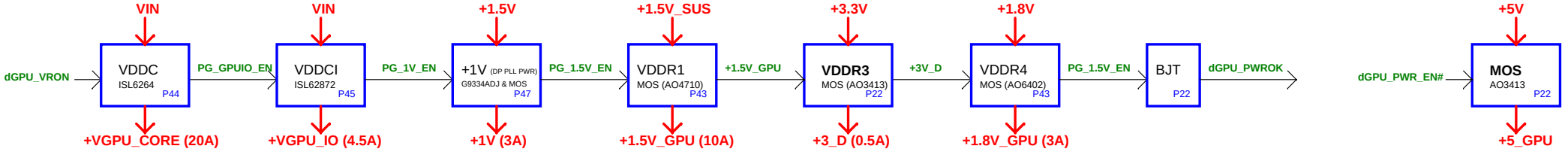
ZQ1 BLOCK DIAGRAM



GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



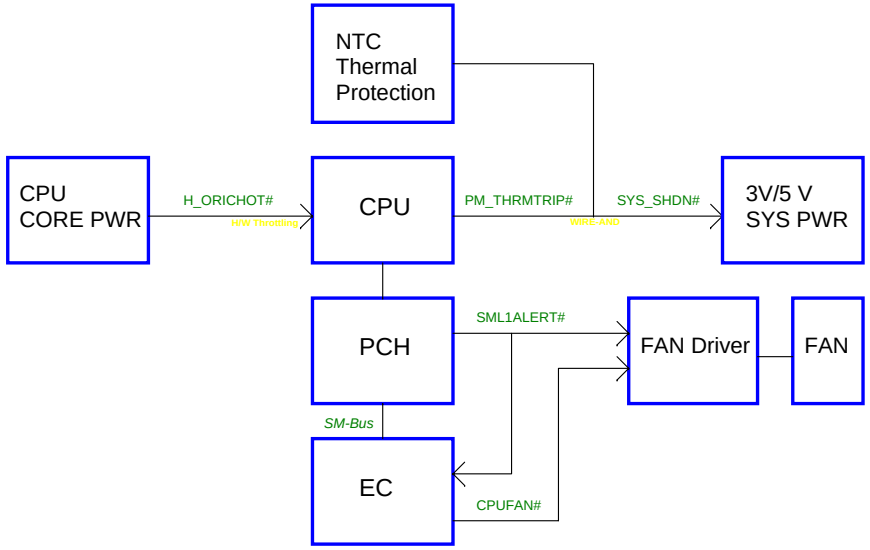
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0~S5
+RTC_CELL	+3V~+3.3V	RTC		S0~S5
+3VPCU	+3.3V	8051 POWER	ALWON	S0~S5
+5VPCU	+5V	CHARGE POWER	ALWON	S0~S5
+15V	+15V	LARGE POWER	+15V_ALWP	S0~S5
3V_LAN_S5	+3.3V	LAN POWER	AUX_ON	
+5VSUS	+5V		SUSD	
+3VSUS	+3.3V		SUSD	
+1.5V_SUS	+1.5V	SODIMM POWER	SUSON	
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAINON	
+5V	+5V		MAIND	
+3V	+3.3V		MAIND	
+1.8V	+1.8V		MAINON	
+1.5V	+1.5V	PCH POWER	MAIND	
+1.1V_VTT	+1.05V~+1.1V	CPU POWER	MAINON	
+1.05V	+1.05V	PCH POWER	MAINON	
+VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	
LCDVCC	+3.3V	LCD Power	LVDS_VDDEN	
MBAT+	+10V~+17V	MAIN BATTERY		
+5V_S5	+5V		S5_ON	
+3V_S5	+3.3V		S5D	

Thermal Follow Chart



Quanta Computer Inc.
PROJECT : ZQ1

Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

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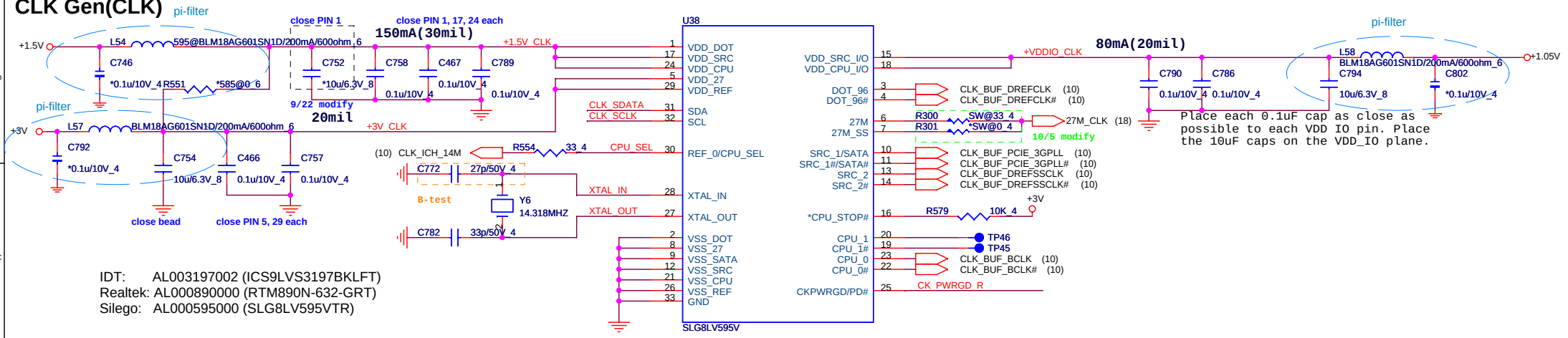
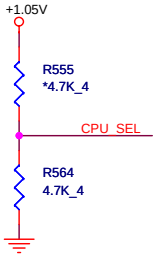
CLK Gen(CLK)



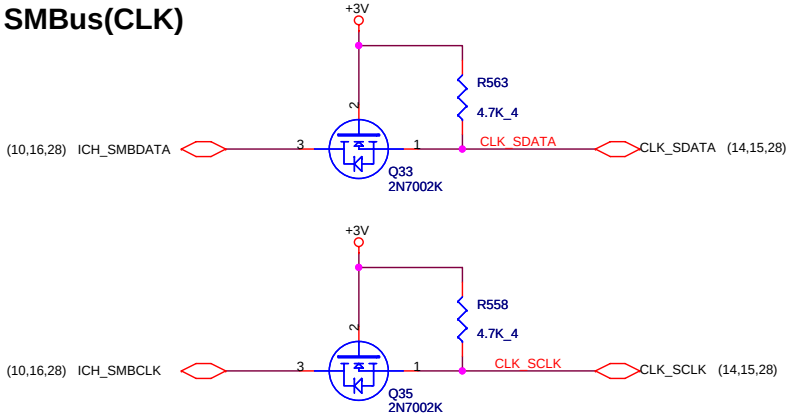
IDT: AL003197002 (ICS9LVS3197BKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

CPU_CLK select(CLK)

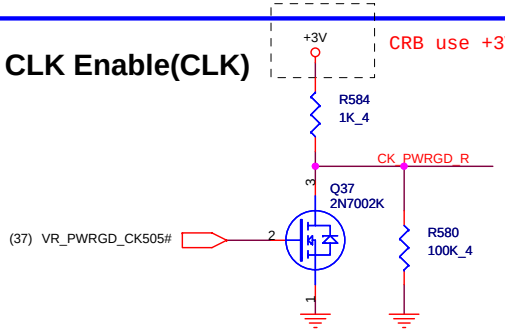


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus(CLK)



CLK Enable(CLK)



Quanta Computer Inc.
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	Clock Generator	1A
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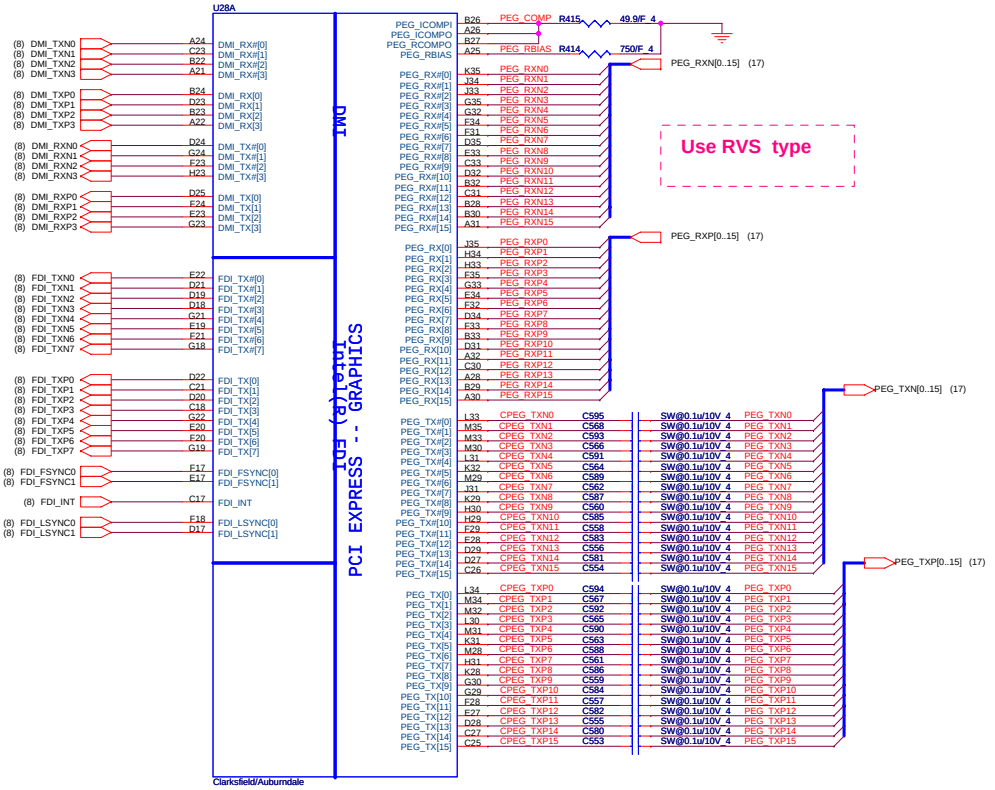
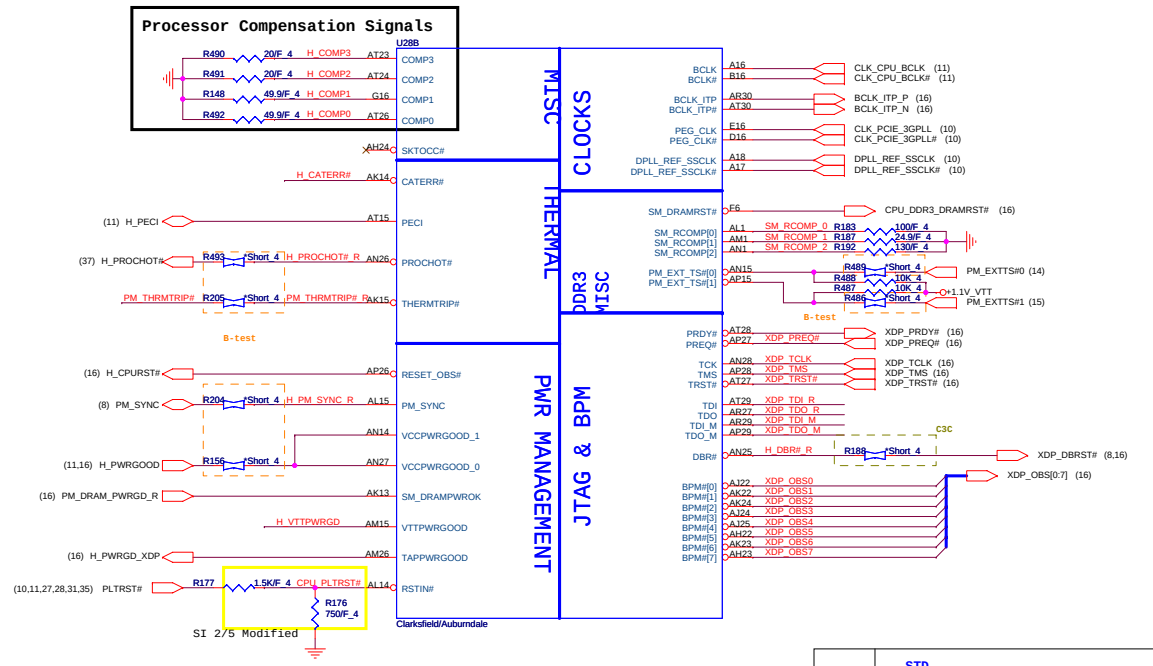
Arrandale_1(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



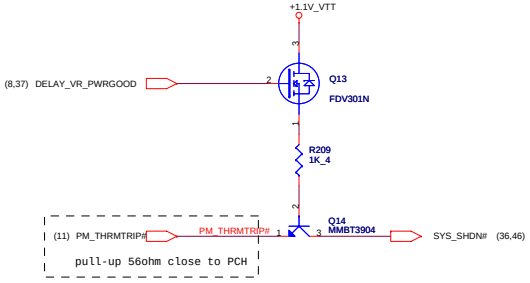
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



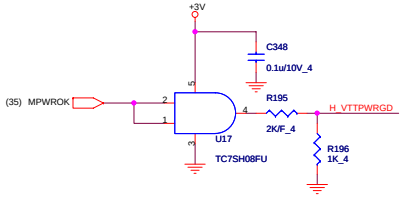
	STD
FOX	DGG^9000024
LTS	DGG^9000022
SUY	
MLX	

Standard: rpga989-aca-zif-069-k01-socket
Reverse: PZ98927-364R-01F-SOCKET

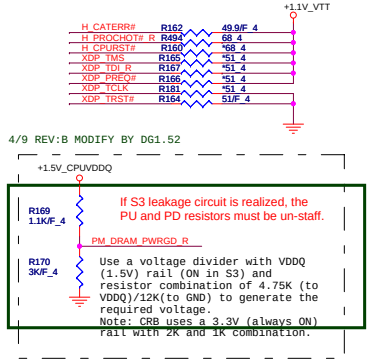
Thermaltrip protect(CPU)



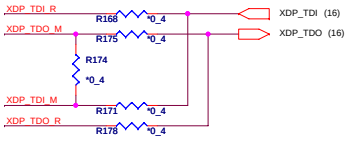
VTT PWR_Good(CPU)



Processor pull-up(CPU)



JTAG MAPPING(CPU)



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

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	AUBURNDA 1/4	1A

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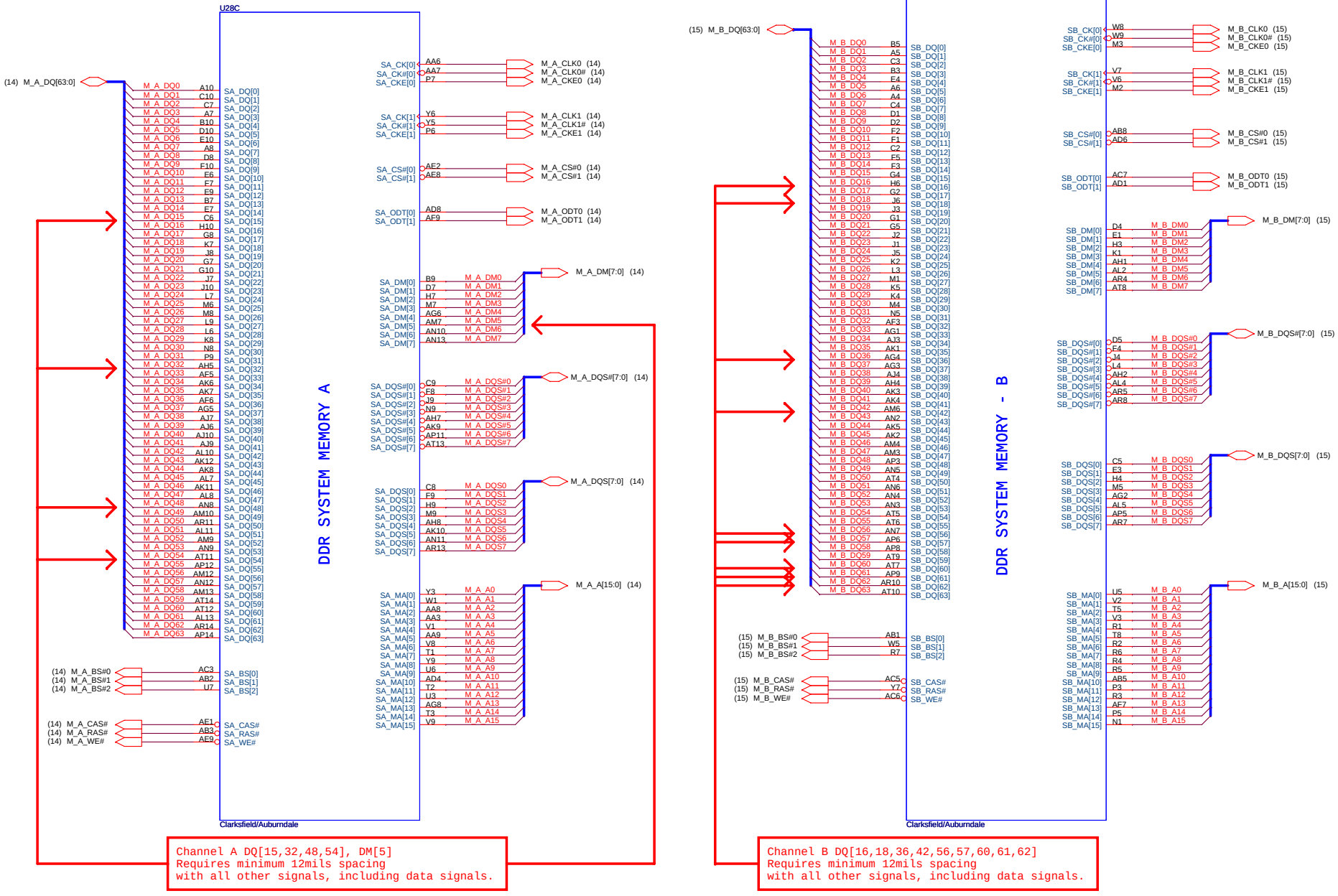
Arrandale_2(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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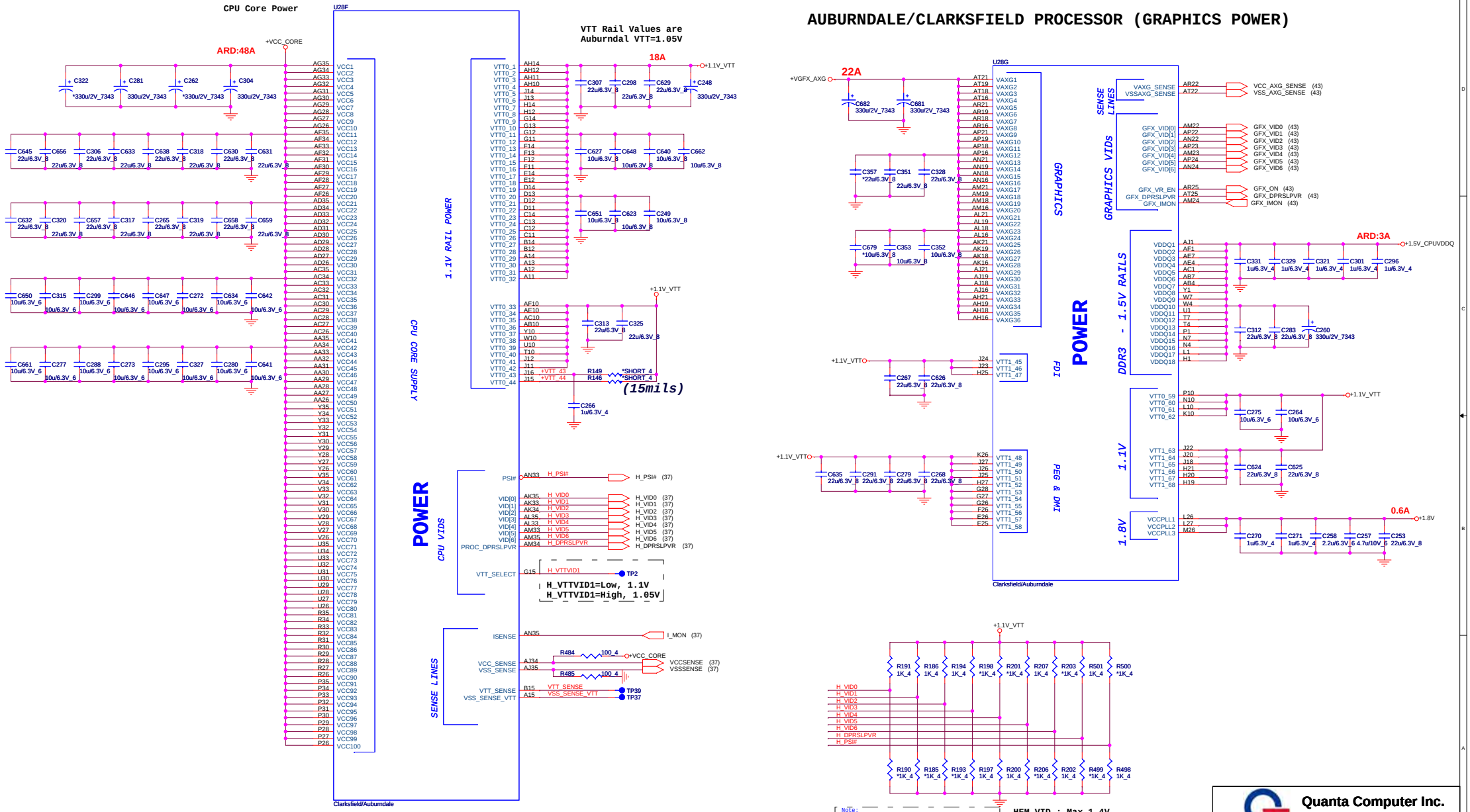
Arrandale_3(CPU)



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	AUBURNDA 3/4 (PWR)	1A
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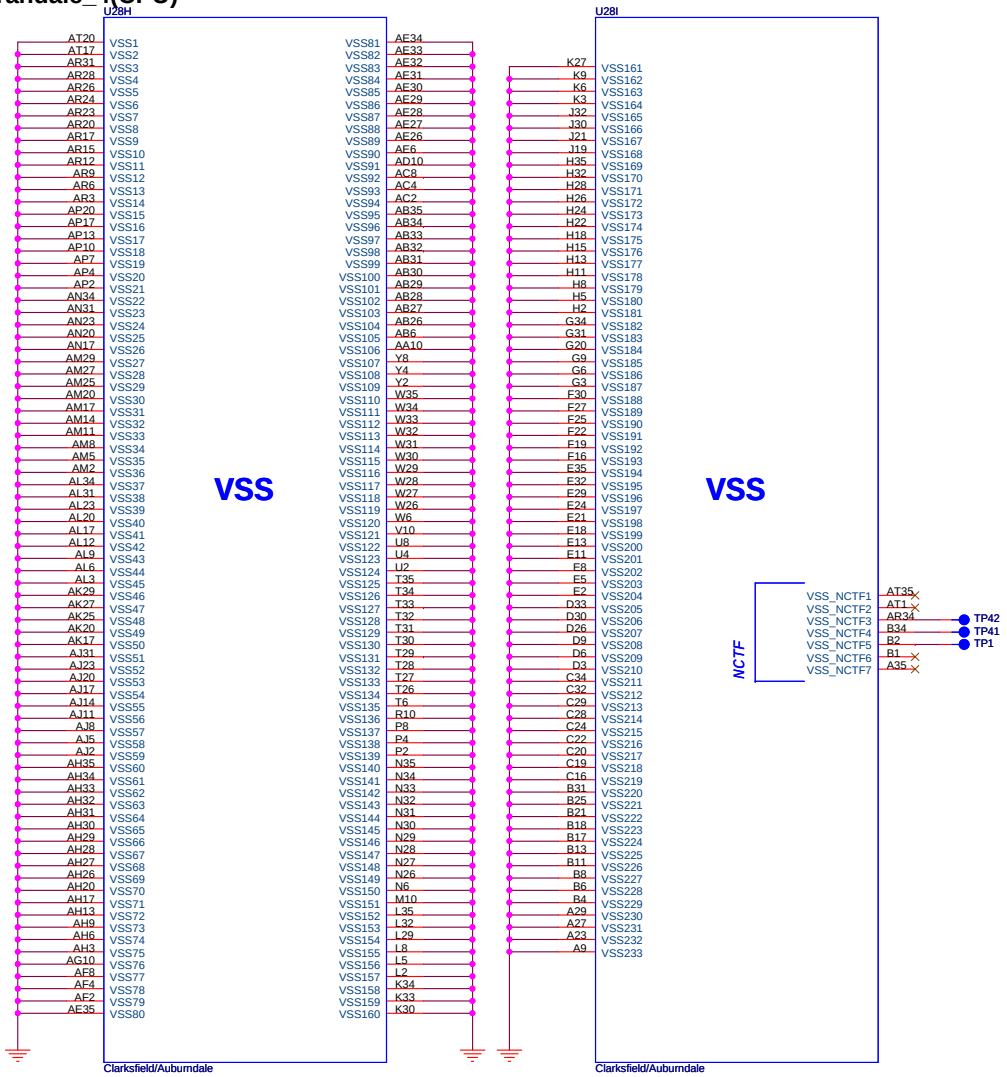
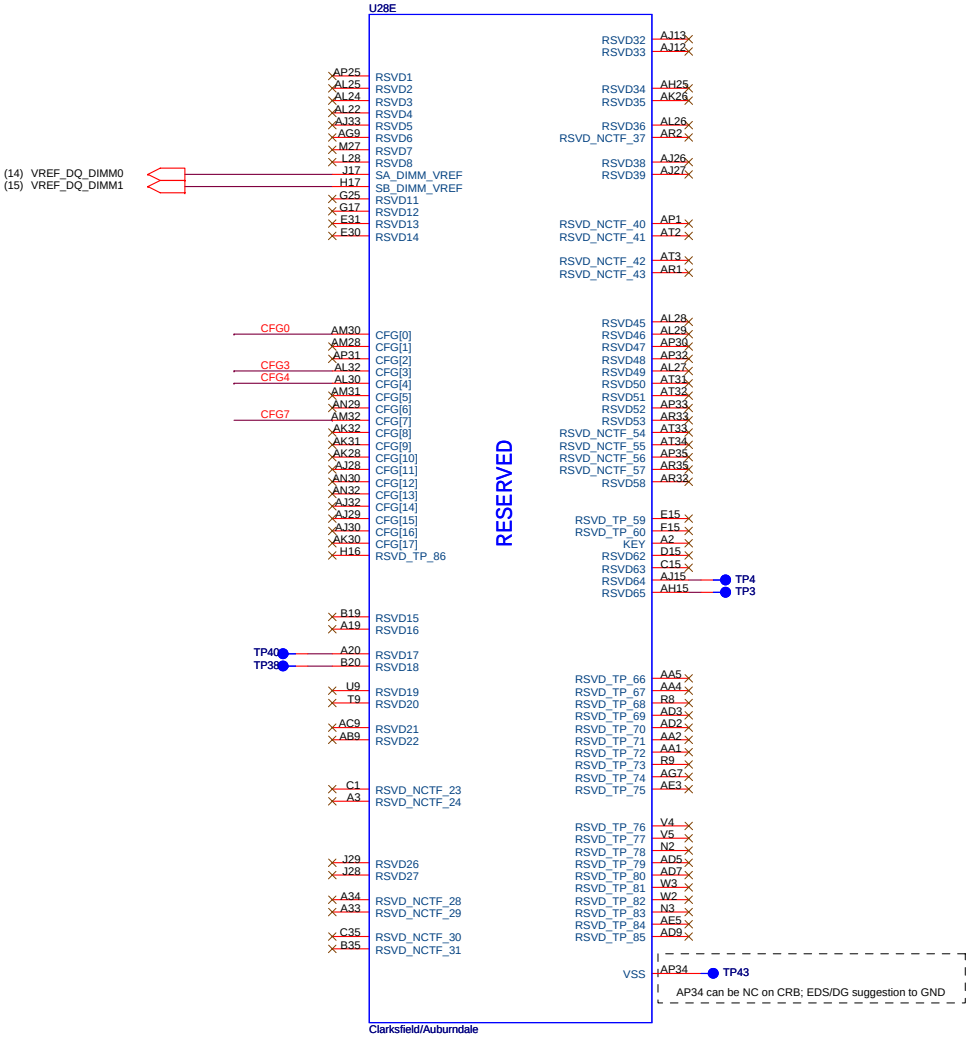
Arrandale_4(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

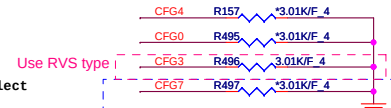


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**



Use RVS type

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

Quanta Computer Inc.
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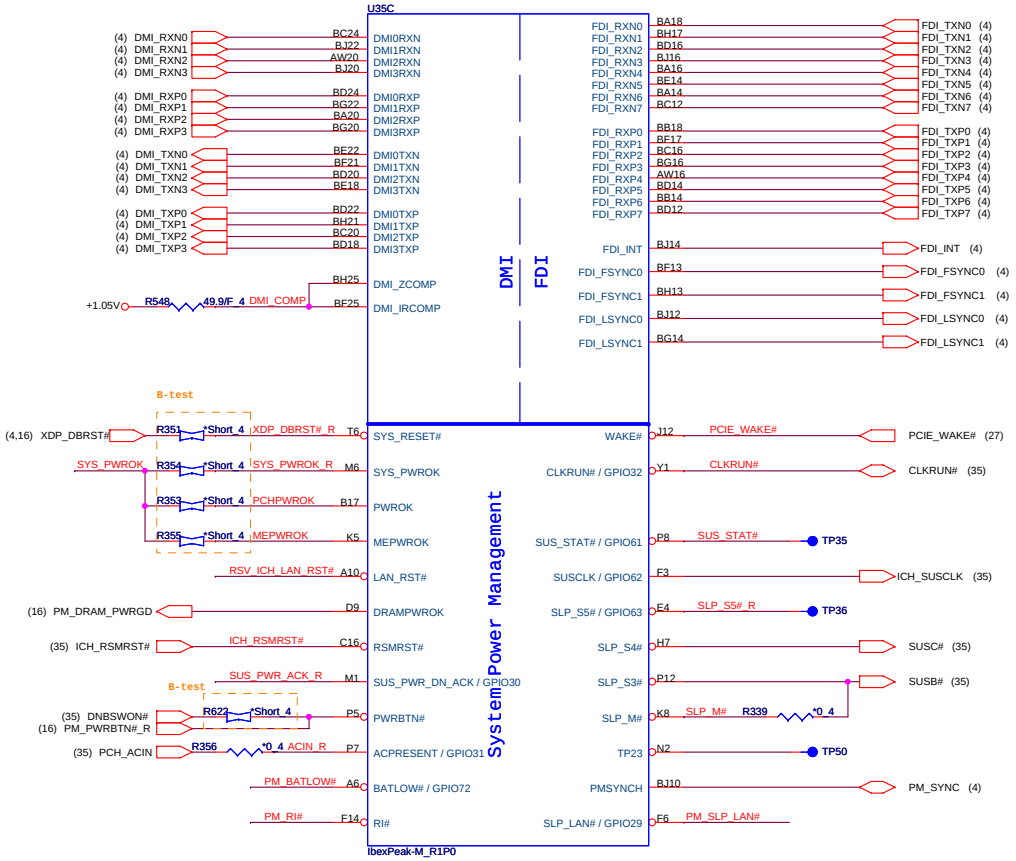
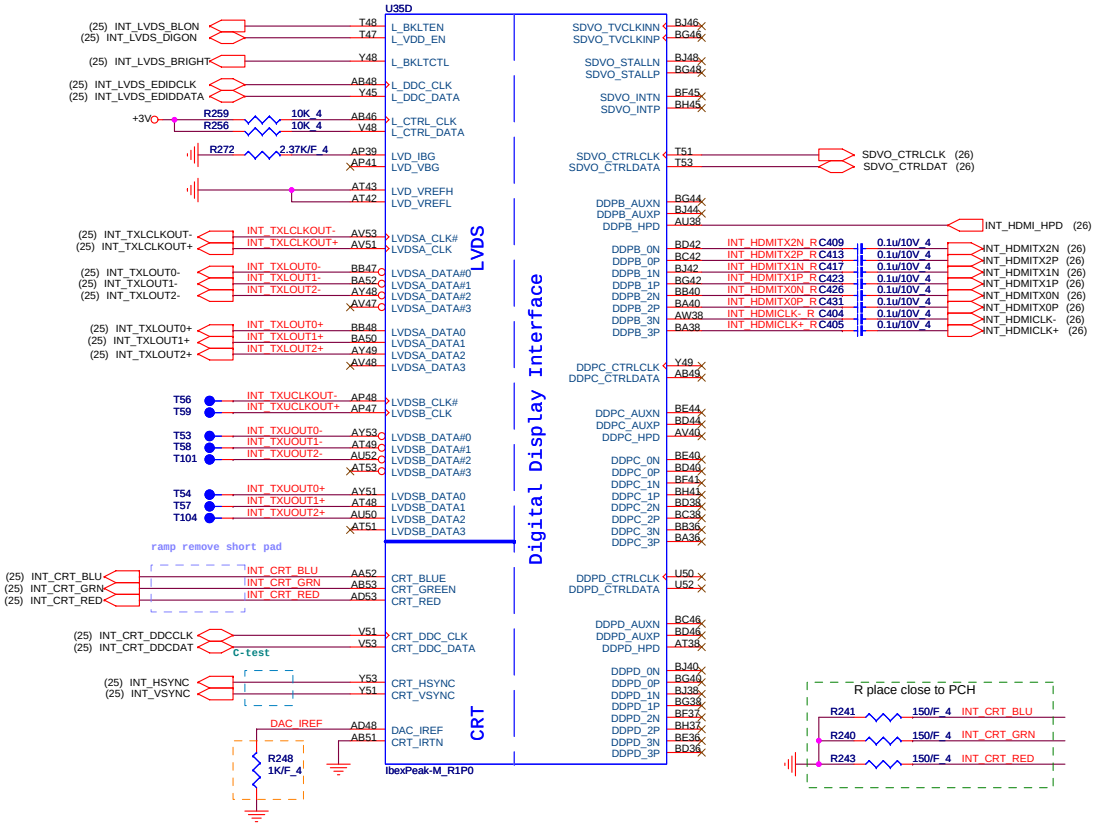
PCH1(CLG)

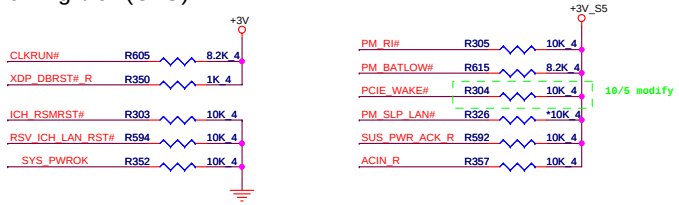
IBEX PEAK-M (DMI,FDI,GPIO)



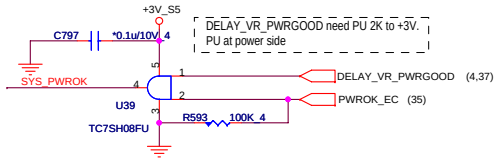
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low(CLG)



System PWR_OK(CLG)



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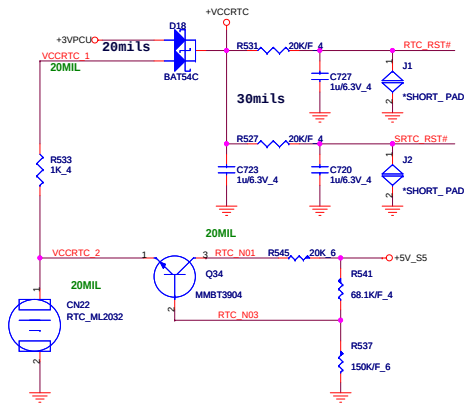
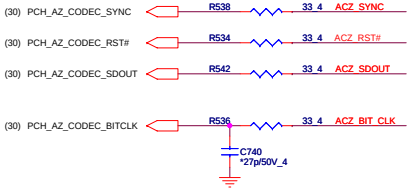
RTC Circuitry(RTC)

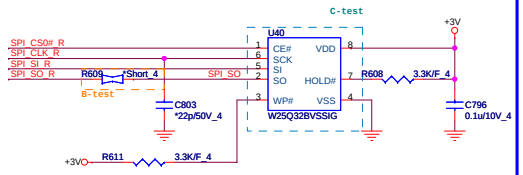


HDA Bus(CLG)

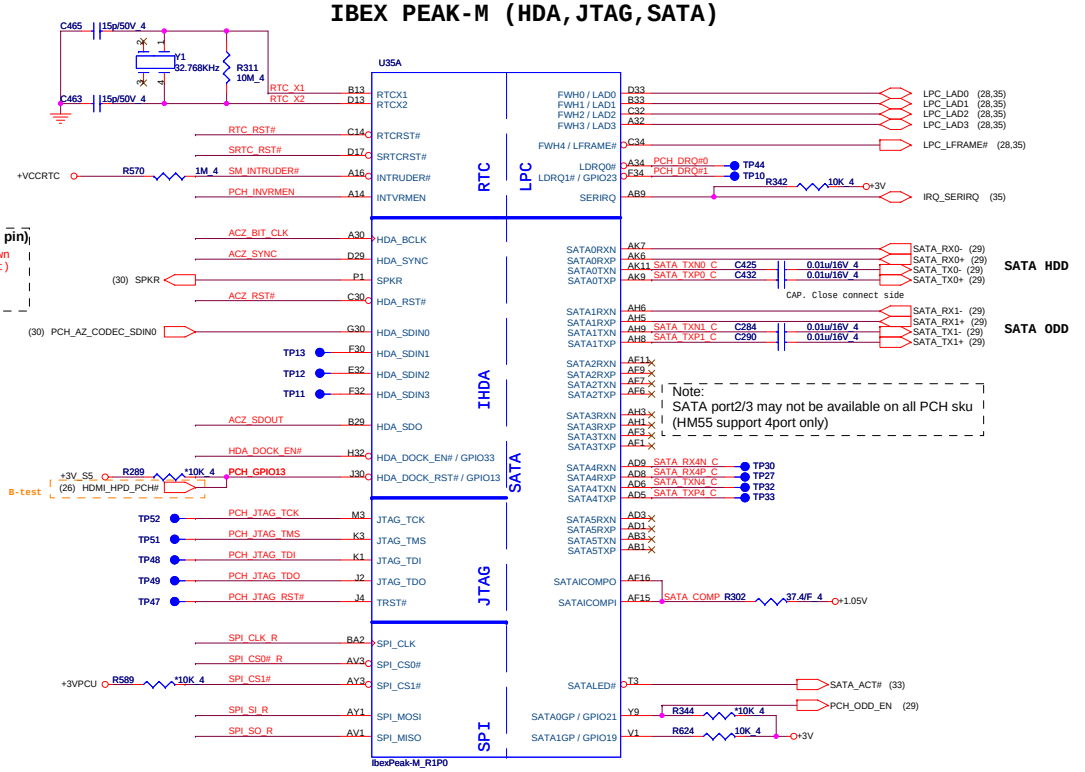


Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI(CLG)



PCH2(CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZQ1 note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R601 *10K_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R517 *10K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+VCCRTC R567 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] +3V R249 1K_4 R245 1K_4 C-test R255 *1K_4 R254 *1K_4 PCI_GNT0# (10) PCI_GNT1# (10)
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R590 *1K_4 NV_ALE NV_ALE (10)
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R591 *1K_4 NV_CLE NV_CLE (10)
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V R277 *1K_4 R273 *10K_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R627 *1K_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R340 10K_4 RSV_GPIO8 (11)
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 R349 1K_4 CR_WAKE# (11)

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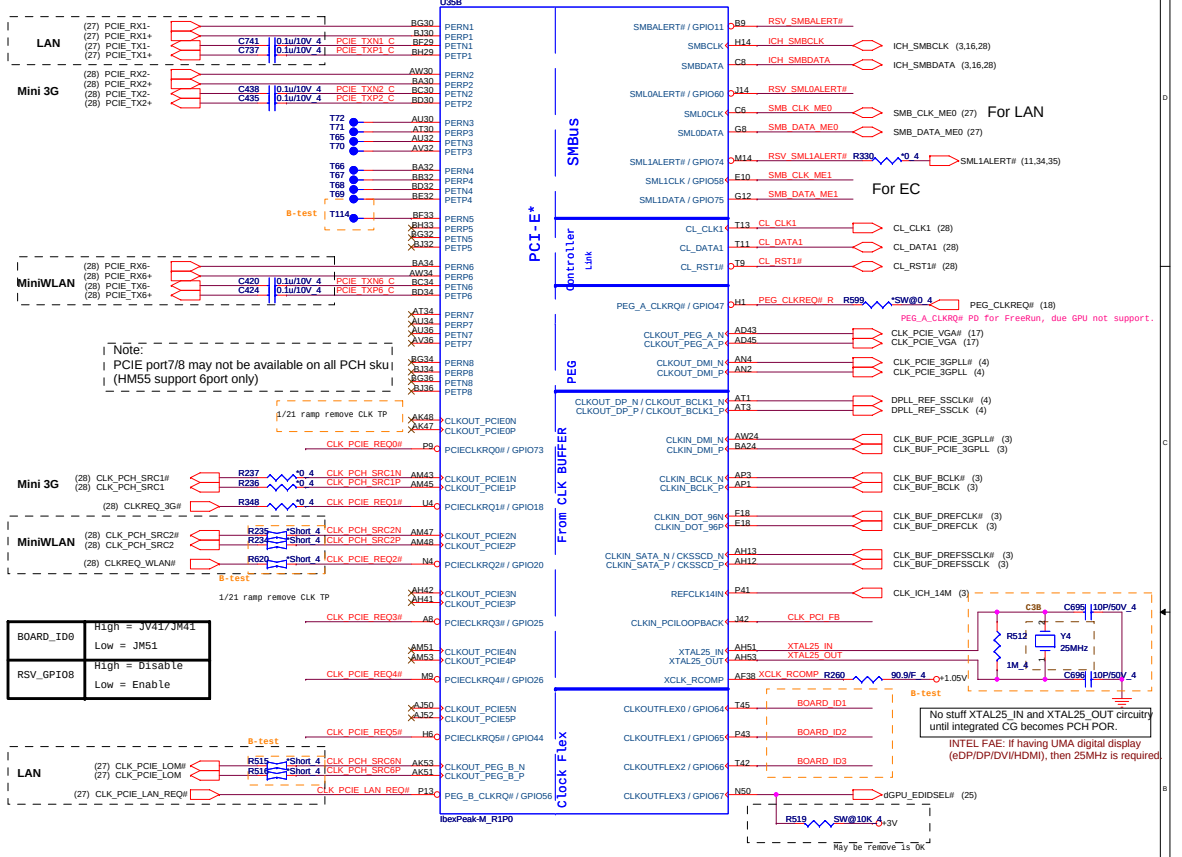
PCH3(CLG)

IBEX PEAK-M (PCI,USB,NVRAM)

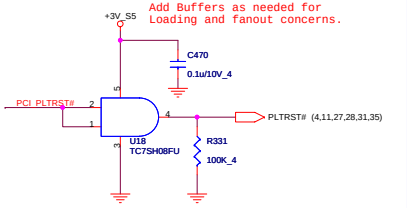
IBEX PEAK-M (PCI-E,SMBUS,CLK)

8/13 Swap Lan and WLAN/ Lan chagne to port 1

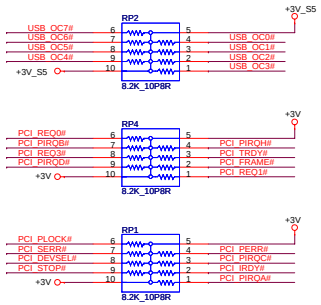


BOARD_ID0	High = JV41/JM41 Low = JM51
RSV_GPIO8	High = Disable Low = Enable

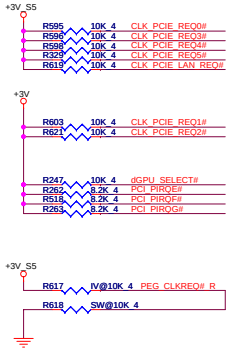
PLTRST#(CLG)



PCI/USBOC# Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



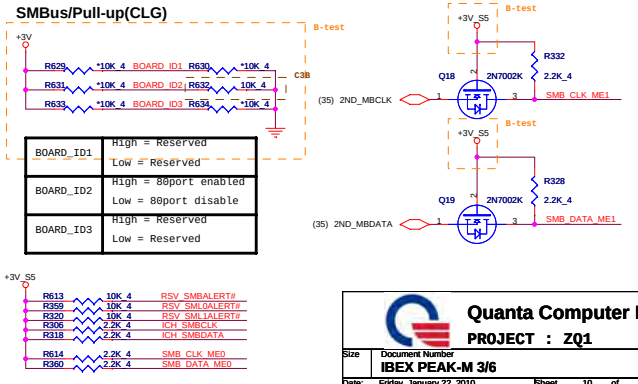
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

SMBus/Pull-up(CLG)



BOARD_ID1	High = Reserved Low = Reserved
BOARD_ID2	High = 80port enabled Low = 80port disable
BOARD_ID3	High = Reserved Low = Reserved

Quanta Computer Inc.
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	IBEX PEAK-M 3/6	1A
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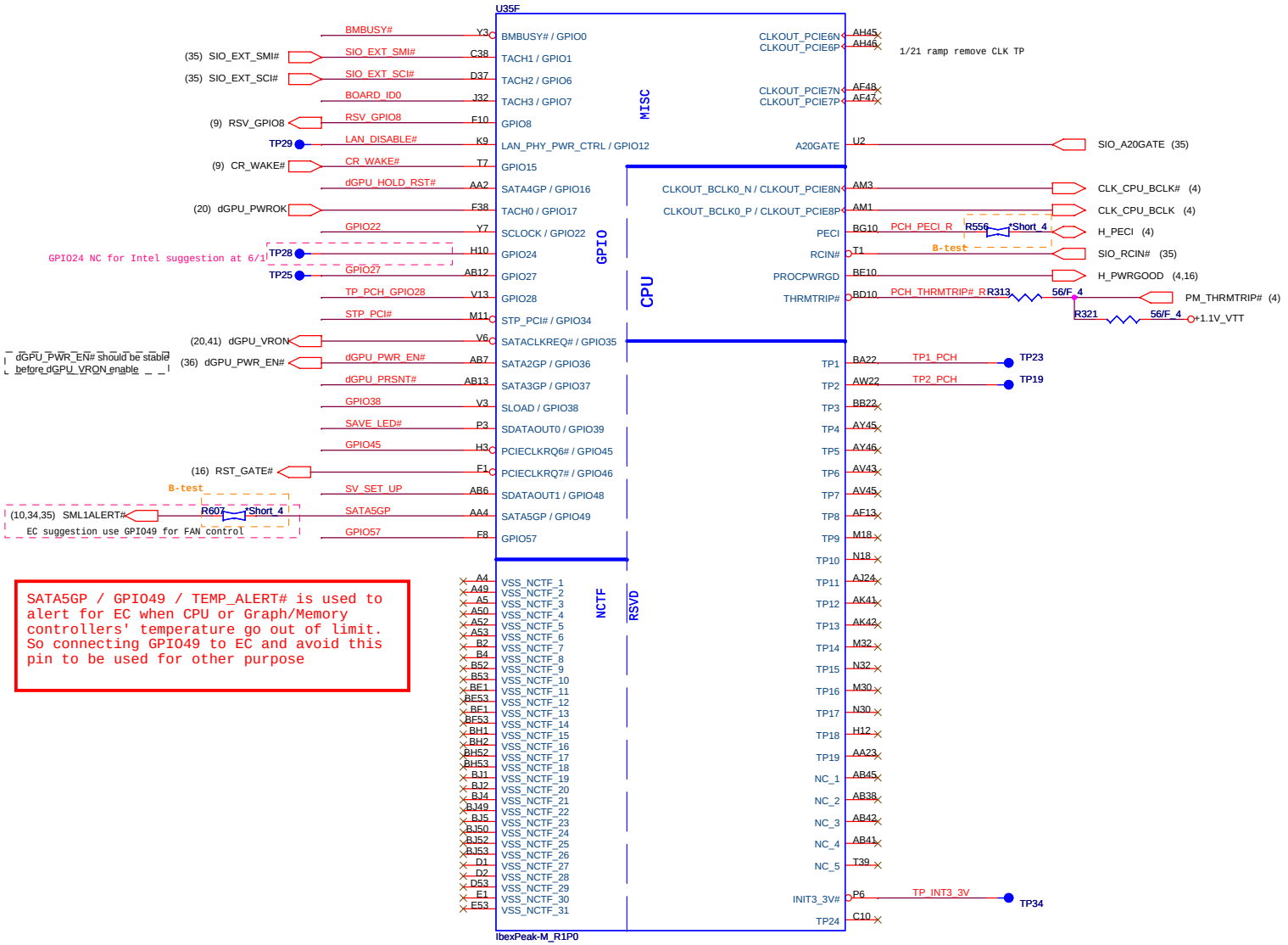
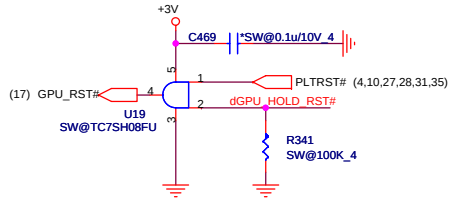
PCH4(CLG)

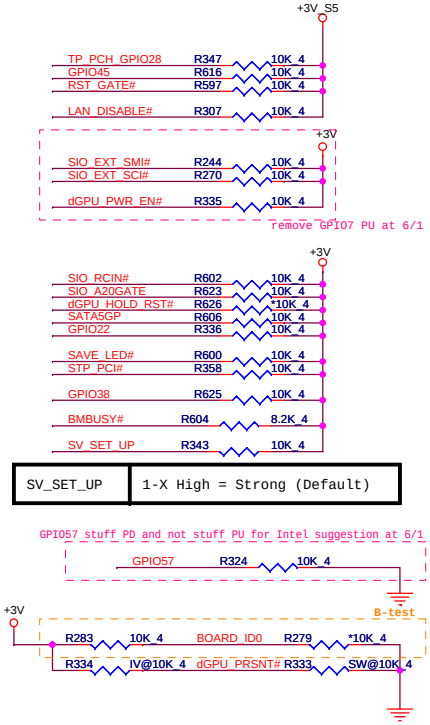
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



GPU RST#(CLG)



GPIO Pull-up/Pull-down(CLG)



SV_SET_UP	1-X High = Strong (Default)

BOARD_ID0	High = JV41/JM41 Low = JM51
RSV_GPIO8	High = Disable Low = Enable

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	IBEX PEAK-M 4/6	1A

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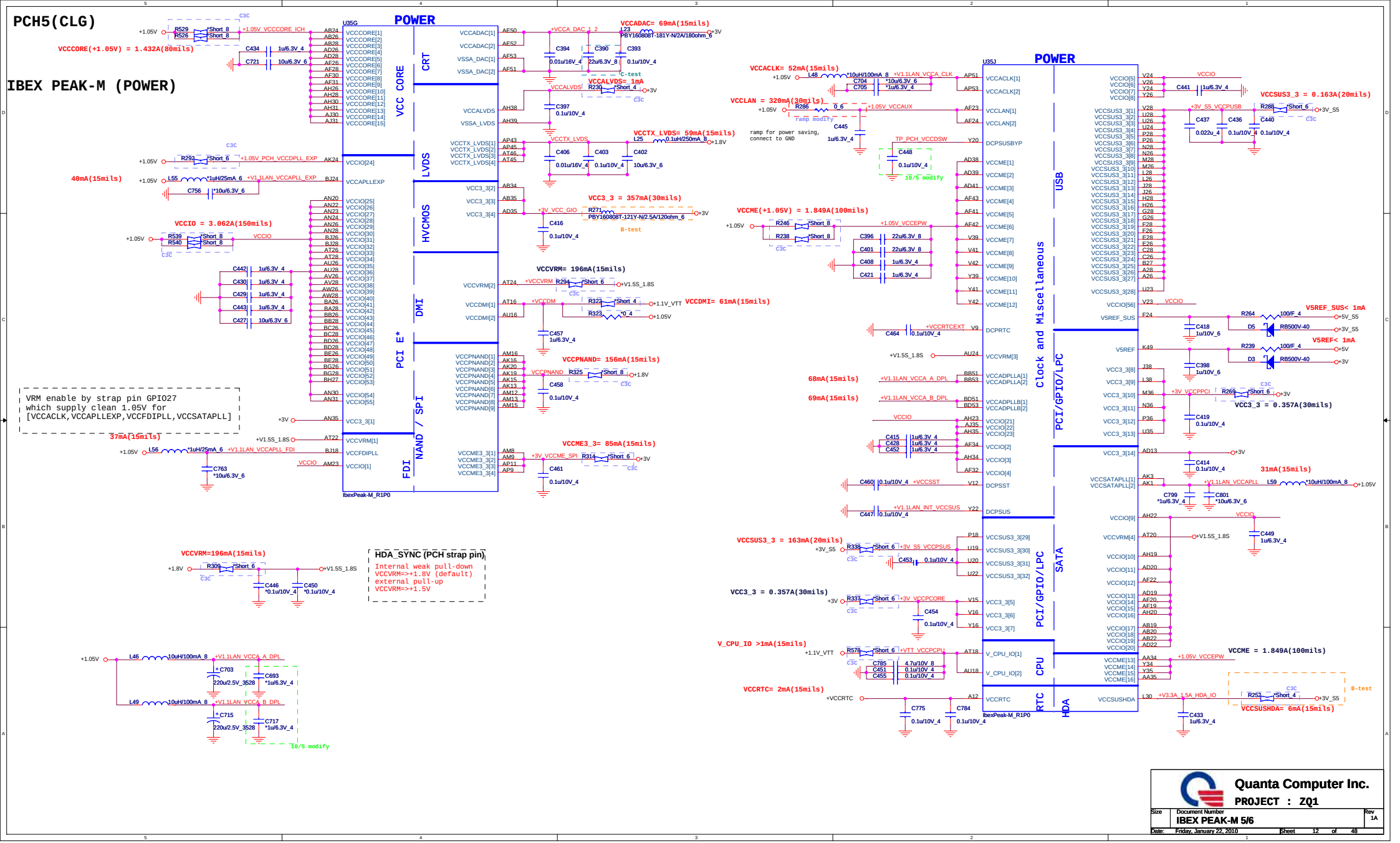
PCH5(CLG)

IBEX PEAK-M (POWER)



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	IBEX PEAK-M 5/6	1A

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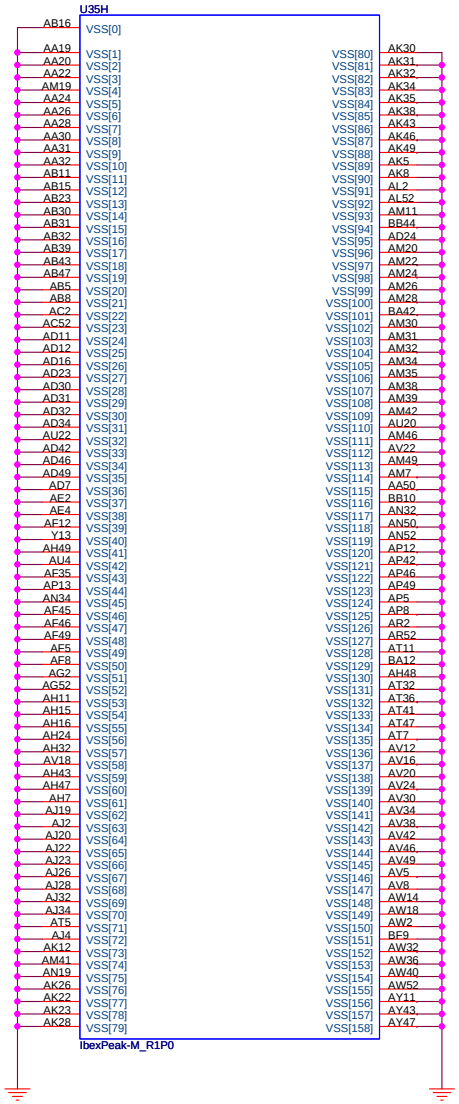
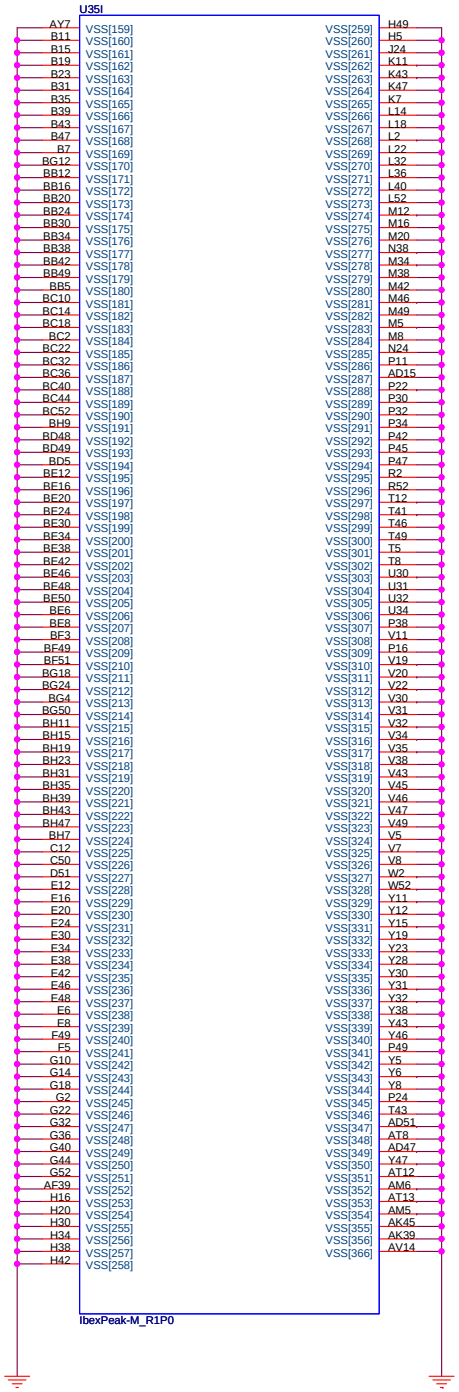
IBEX PEAK-M (GND)





Quanta Computer Inc.

PROJECT : ZQ1

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A

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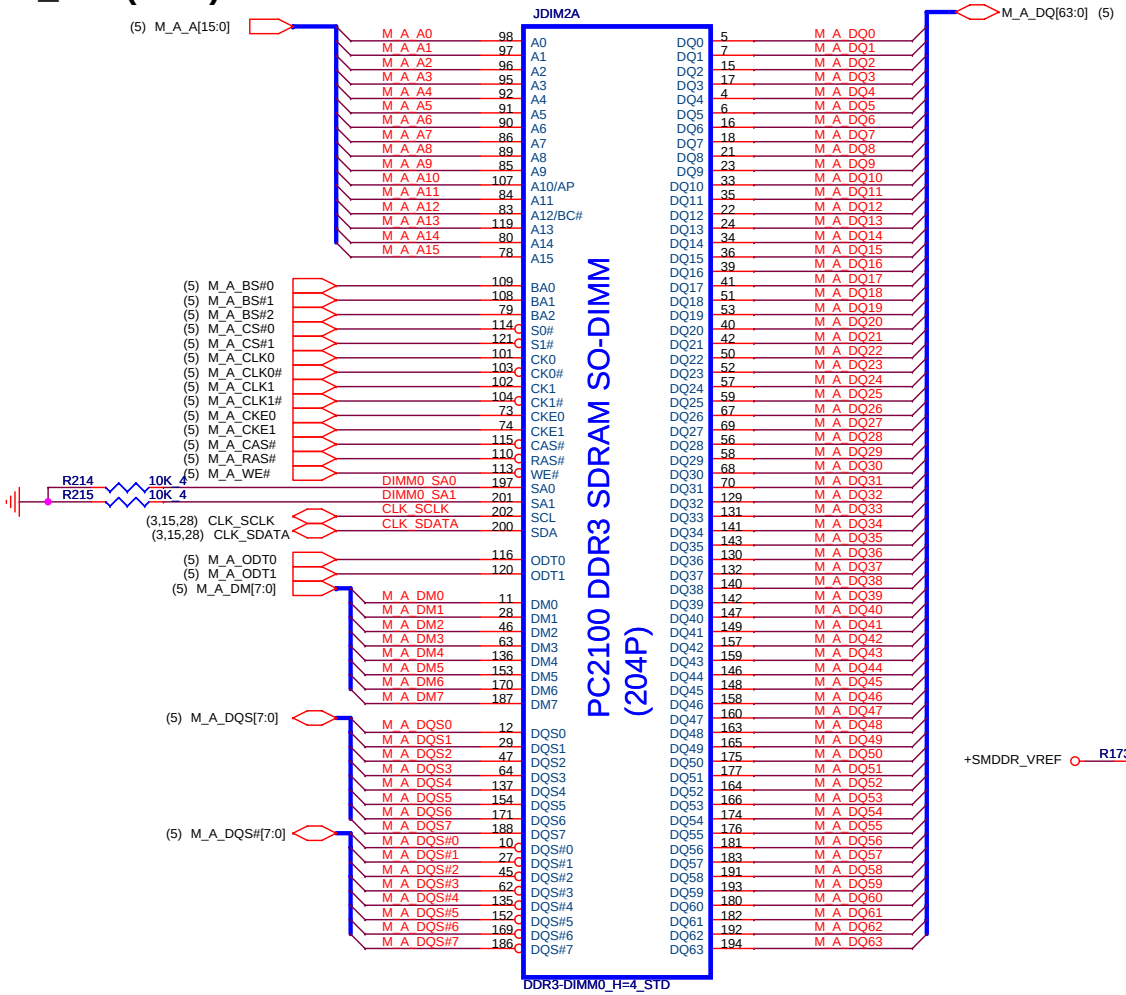
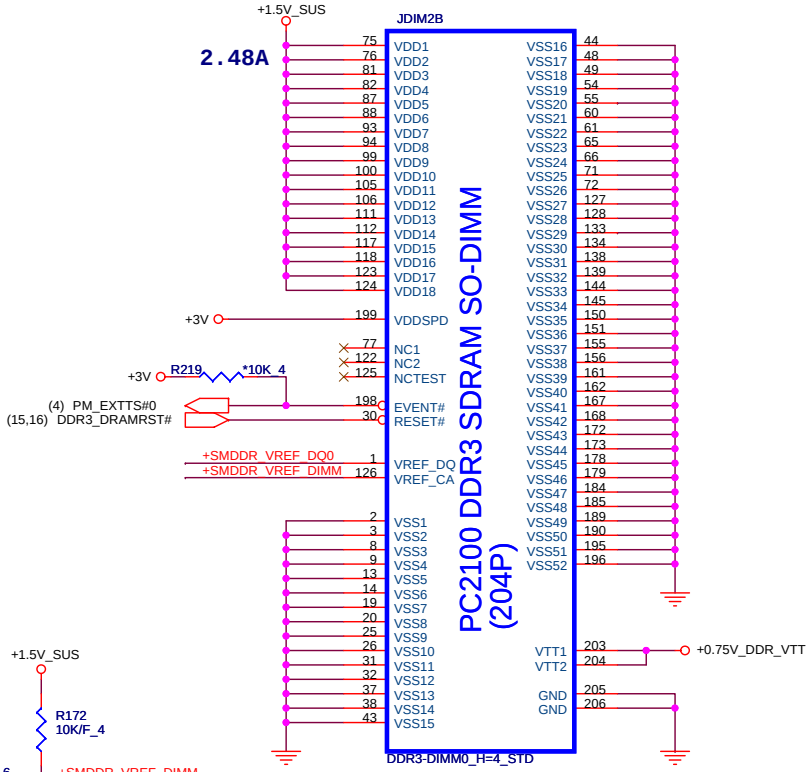
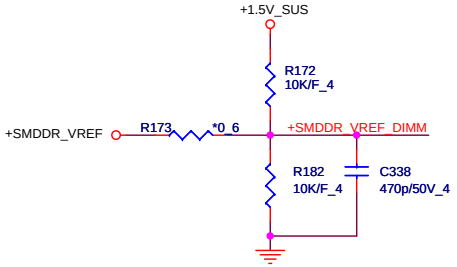
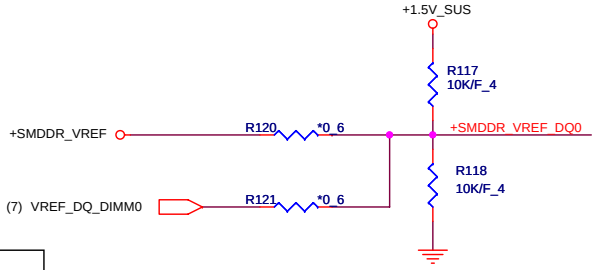
DDR_STD(DDR)

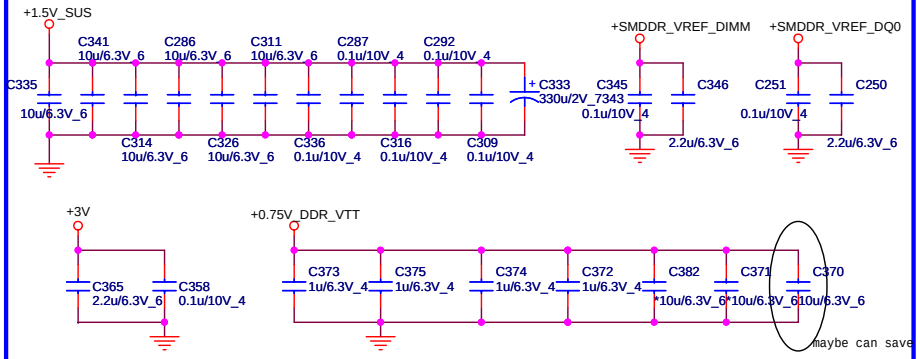








Place these Caps near So-Dimm0.



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 4H type:DDR-C-2013289-204p		

M1:PWR SMDRR_VREF
M1+:voltage divider(Default)
M3:CPU VREF_DQ_DIMM0

Quanta Computer Inc.

PROJECT : ZQ1

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	DDRIII SO-DIMM-0	1A
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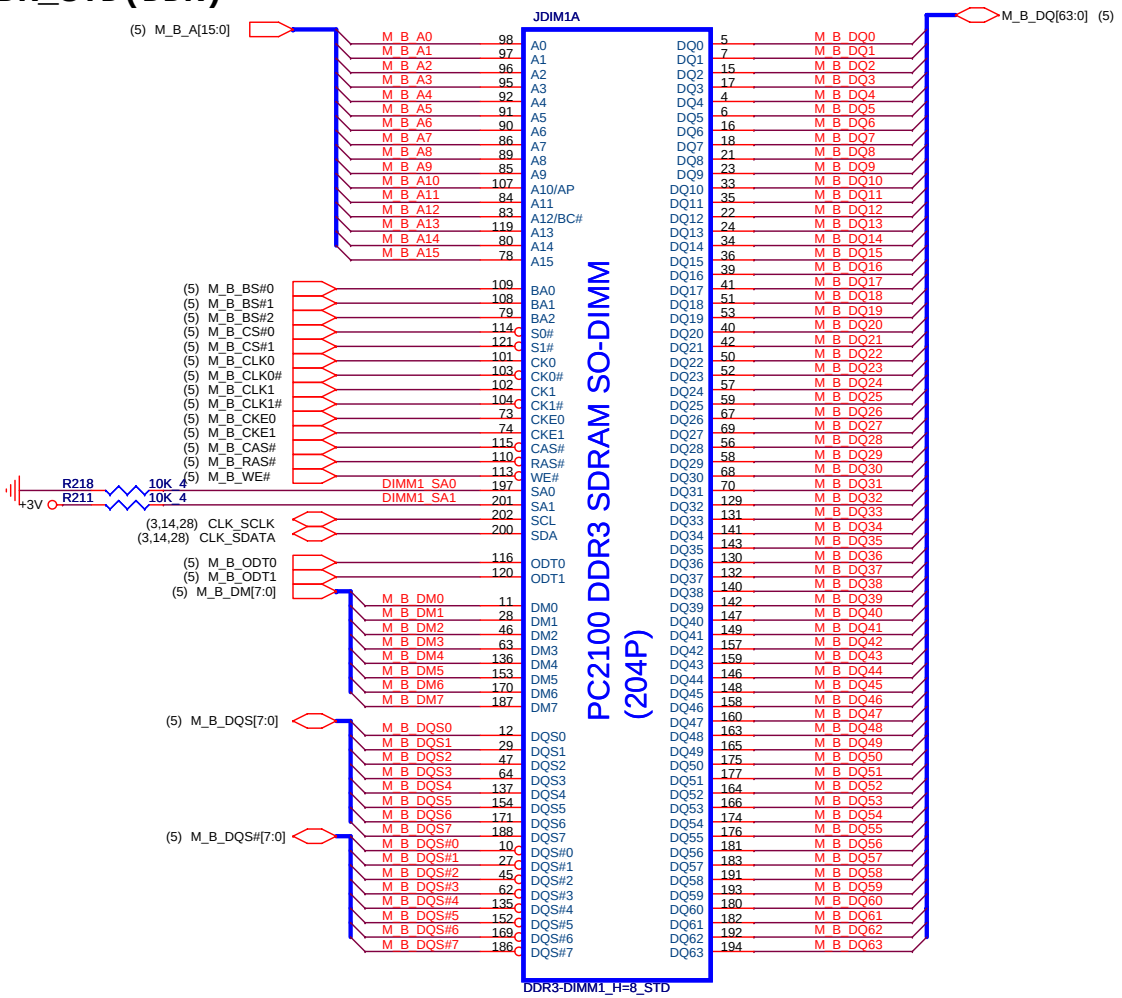
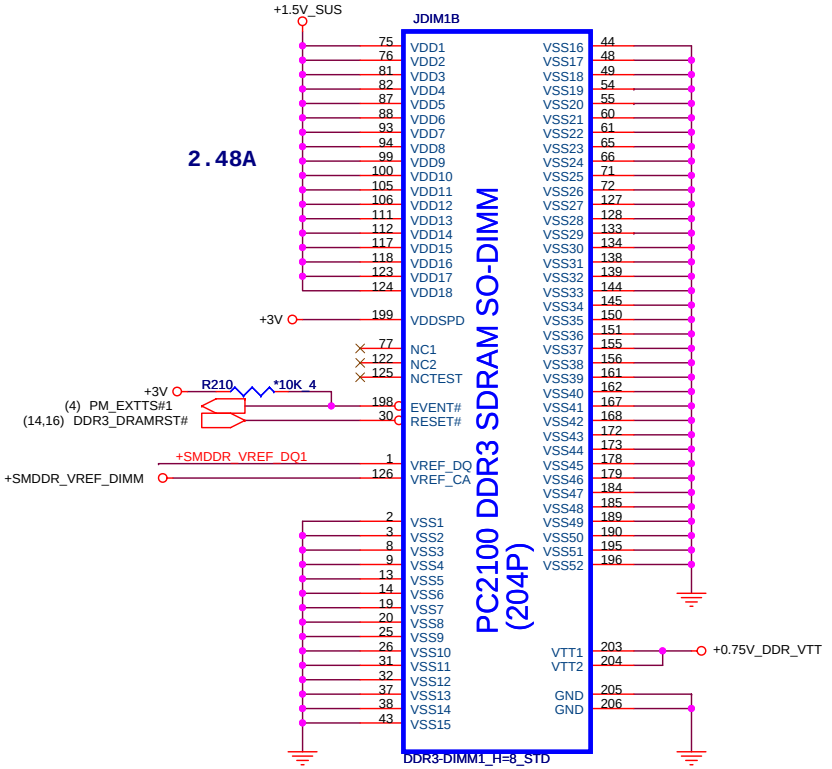
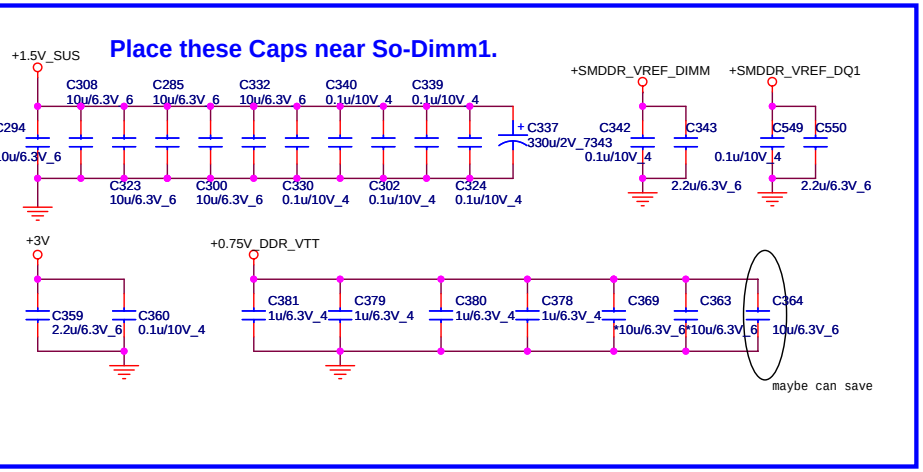
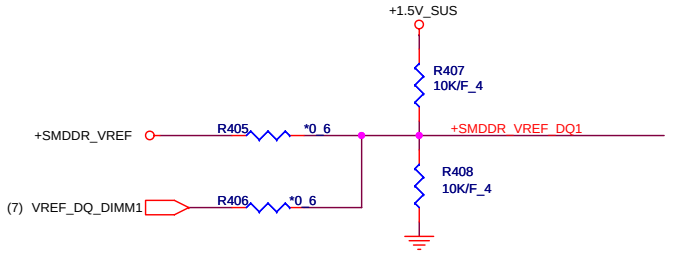
DDR_STD(DDR)









	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 8H type:DDR-C-2013310-204p-1		

M1:PWR SMDRR_VREF
M1+:voltage divider(Default)
M3:CPU VREF_DQ_DIMM0

Quanta Computer Inc.
PROJECT : ZQ1

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
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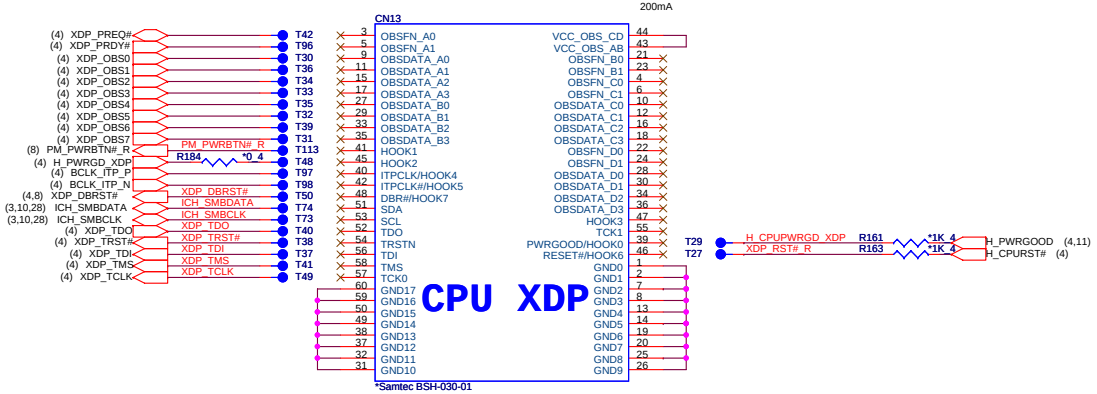
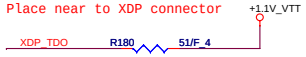
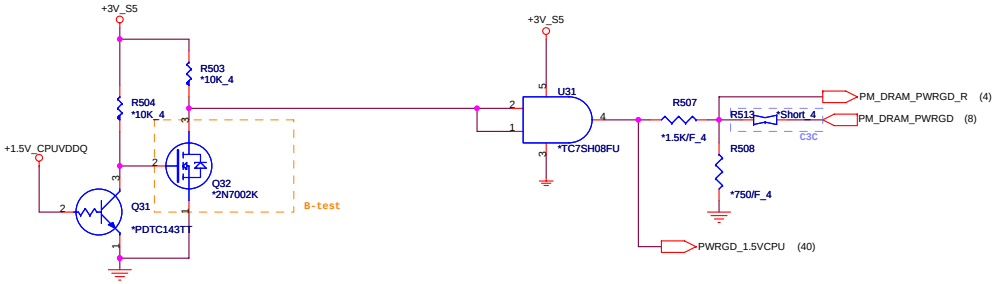
CPU XDP Connector(CPU)

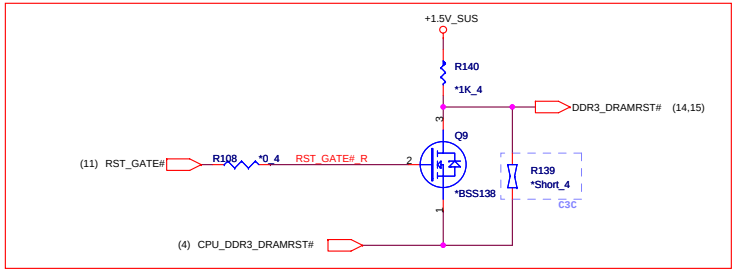


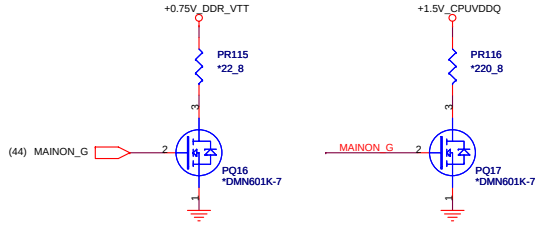
Place near to XDP connector

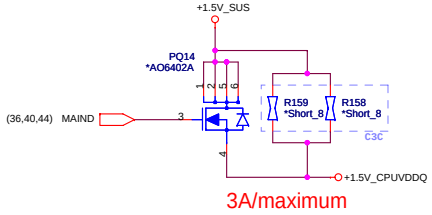


S3 leakage solution(CLG)









Quanta Computer Inc.
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	XDP	1A
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GPU_1(VGA)

(4) PEG_TXP[0..15] PEG_TXP[0..15]
(4) PEG_TXN[0..15] PEG_TXN[0..15]
(4) PEG_RXP[0..15] PEG_RXP[0..15]
(4) PEG_RXN[0..15] PEG_RXN[0..15]

U23A

0518 SWAP PCIE for VGA side

(4) PEG_TXP15 / (4) PEG_TXN15	PEG_TXP15 / PEG_TXN15	AA38 / Y37	PCIE_RX0P / PCIE_RX0N	
(4) PEG_TXP14 / (4) PEG_TXN14	PEG_TXP14 / PEG_TXN14	Y35 / W36	PCIE_RX1P / PCIE_RX1N	
(4) PEG_TXP13 / (4) PEG_TXN13	PEG_TXP13 / PEG_TXN13	W38 / V37	PCIE_RX2P / PCIE_RX2N	
(4) PEG_TXP12 / (4) PEG_TXN12	PEG_TXP12 / PEG_TXN12	V35 / U36	PCIE_RX3P / PCIE_RX3N	
(4) PEG_TXP11 / (4) PEG_TXN11	PEG_TXP11 / PEG_TXN11	U38 / T37	PCIE_RX4P / PCIE_RX4N	
(4) PEG_TXP10 / (4) PEG_TXN10	PEG_TXP10 / PEG_TXN10	T35 / R36	PCIE_RX5P / PCIE_RX5N	
(4) PEG_TXP9 / (4) PEG_TXN9	PEG_TXP9 / PEG_TXN9	R38 / P37	PCIE_RX6P / PCIE_RX6N	
(4) PEG_TXP8 / (4) PEG_TXN8	PEG_TXP8 / PEG_TXN8	P35 / N36	PCIE_RX7P / PCIE_RX7N	
(4) PEG_TXP7 / (4) PEG_TXN7	PEG_TXP7 / PEG_TXN7	N38 / M37	PCIE_RX8P / PCIE_RX8N	
(4) PEG_TXP6 / (4) PEG_TXN6	PEG_TXP6 / PEG_TXN6	M35 / L36	PCIE_RX9P / PCIE_RX9N	
(4) PEG_TXP5 / (4) PEG_TXN5	PEG_TXP5 / PEG_TXN5	L38 / K37	PCIE_RX10P / PCIE_RX10N	
(4) PEG_TXP4 / (4) PEG_TXN4	PEG_TXP4 / PEG_TXN4	K35 / J36	PCIE_RX11P / PCIE_RX11N	
(4) PEG_TXP3 / (4) PEG_TXN3	PEG_TXP3 / PEG_TXN3	J38 / H37	PCIE_RX12P / PCIE_RX12N	
(4) PEG_TXP2 / (4) PEG_TXN2	PEG_TXP2 / PEG_TXN2	H35 / G36	PCIE_RX13P / PCIE_RX13N	
(4) PEG_TXP1 / (4) PEG_TXN1	PEG_TXP1 / PEG_TXN1	G38 / F37	PCIE_RX14P / PCIE_RX14N	
(4) PEG_TXP0 / (4) PEG_TXN0	PEG_TXP0 / PEG_TXN0	F35 / E37	PCIE_RX15P / PCIE_RX15N	

CLOCK

(10) CLK_PCIE_VGA — AB35 — PCIE_REFCLKP
(10) CLK_PCIE_VGA# — AA36 — PCIE_REFCLKN

For Broadway, Madison and Park
the PWRGOOD ball must be connecctd to ground

R61 SW@10K_4

AJ21 NC#1
AK21 NC#2
AH16 PWRGOOD

(11) GPU_RST# — AA30 — PERSTB

SW@Madison/Park_M2

PCI EXPRESS INTERFACE

0518 SWAP PCIE for VGA side

PCIE_TX0P / PCIE_TX0N	Y33 / Y32	CPEG_RXP15 / CPEG_RXN15	C150 / C160	SW@0.1u/10V_4	PEG_RXP15 (4)	PEG_RXN15 (4)
PCIE_TX1P / PCIE_TX1N	W33 / W32	CPEG_RXP14 / CPEG_RXN14	C139 / C148	SW@0.1u/10V_4	PEG_RXP14 (4)	PEG_RXN14 (4)
PCIE_TX2P / PCIE_TX2N	U33 / U32	CPEG_RXP13 / CPEG_RXN13	C127 / C137	SW@0.1u/10V_4	PEG_RXP13 (4)	PEG_RXN13 (4)
PCIE_TX3P / PCIE_TX3N	U30 / U29	CPEG_RXP12 / CPEG_RXN12	C125 / C120	SW@0.1u/10V_4	PEG_RXP12 (4)	PEG_RXN12 (4)
PCIE_TX4P / PCIE_TX4N	T33 / T32	CPEG_RXP11 / CPEG_RXN11	C118 / C110	SW@0.1u/10V_4	PEG_RXP11 (4)	PEG_RXN11 (4)
PCIE_TX5P / PCIE_TX5N	T30 / T29	CPEG_RXP10 / CPEG_RXN10	C107 / C103	SW@0.1u/10V_4	PEG_RXP10 (4)	PEG_RXN10 (4)
PCIE_TX6P / PCIE_TX6N	P33 / P32	CPEG_RXP9 / CPEG_RXN9	C101 / C91	SW@0.1u/10V_4	PEG_RXP9 (4)	PEG_RXN9 (4)
PCIE_TX7P / PCIE_TX7N	P30 / P29	CPEG_RXP8 / CPEG_RXN8	C89 / C83	SW@0.1u/10V_4	PEG_RXP8 (4)	PEG_RXN8 (4)
PCIE_TX8P / PCIE_TX8N	N33 / N32	CPEG_RXP7 / CPEG_RXN7	C73 / C70	SW@0.1u/10V_4	PEG_RXP7 (4)	PEG_RXN7 (4)
PCIE_TX9P / PCIE_TX9N	N30 / N29	CPEG_RXP6 / CPEG_RXN6	C68 / C60	SW@0.1u/10V_4	PEG_RXP6 (4)	PEG_RXN6 (4)
PCIE_TX10P / PCIE_TX10N	L33 / L32	CPEG_RXP5 / CPEG_RXN5	C57 / C54	SW@0.1u/10V_4	PEG_RXP5 (4)	PEG_RXN5 (4)
PCIE_TX11P / PCIE_TX11N	L30 / L29	CPEG_RXP4 / CPEG_RXN4	C48 / C43	SW@0.1u/10V_4	PEG_RXP4 (4)	PEG_RXN4 (4)
PCIE_TX12P / PCIE_TX12N	K33 / K32	CPEG_RXP3 / CPEG_RXN3	C37 / C41	SW@0.1u/10V_4	PEG_RXP3 (4)	PEG_RXN3 (4)
PCIE_TX13P / PCIE_TX13N	J33 / J32	CPEG_RXP2 / CPEG_RXN2	C31 / C34	SW@0.1u/10V_4	PEG_RXP2 (4)	PEG_RXN2 (4)
PCIE_TX14P / PCIE_TX14N	K30 / K29	CPEG_RXP1 / CPEG_RXN1	C25 / C24	SW@0.1u/10V_4	PEG_RXP1 (4)	PEG_RXN1 (4)
PCIE_TX15P / PCIE_TX15N	H33 / H32	CPEG_RXP0 / CPEG_RXN0	C29 / C27	SW@0.1u/10V_4	PEG_RXP0 (4)	PEG_RXN0 (4)

CALIBRATION

PCIE_CALRP — Y30 — R45 SW@1.27K/F_4
PCIE_CALRN — Y29 — R40 SW@2K/F_4 — +1V

+1.0V

For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

Madison	AJ007720T02
Park	AJ077400T08

Quanta Computer Inc.
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	Madison/Park M2-PCIE I/F	1A

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GPU_2(VGA)

GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK

1.8V GPIO

3.3V GPIO

NC on Park

NC on Park

(22) RAM_STRAP0
(22) RAM_STRAP1
(22) RAM_STRAP2
T85

R66 SW@10K_4
R67 SW@10K_4

Channel D N.C for Park-M2

SW@Madison/Park_M2

SW@Madison/Park_M2

ramp remove short pad

1/21 ramp remove IO_VID0

DAC2 will be NC on future ASIC

9/29 modify

(1.8V@70mA AVDD)
(1.8V@100mA VDD1DI)
(1.8V@2mA A2VDDQ)
(1.8V@130mA A2VDD)

+1.8V(75mA)
+1.0V(125mA)
+1.8V(5mA)

HDMI
DDC AUX4 NC for Park_M2
LVDS
CRT
DDC AUX7 NC for Park_M2

C-test

Quanta Computer Inc.		
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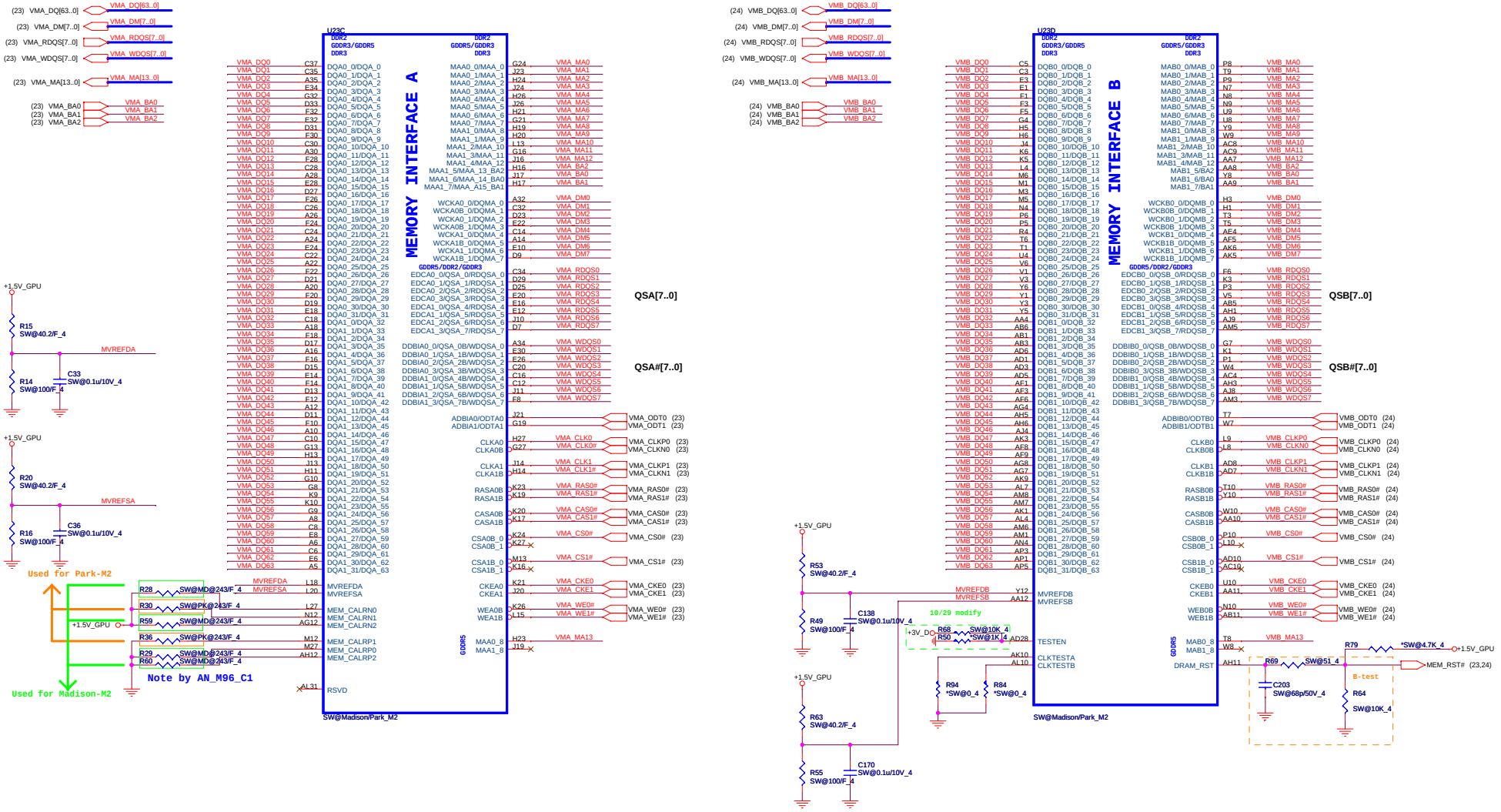
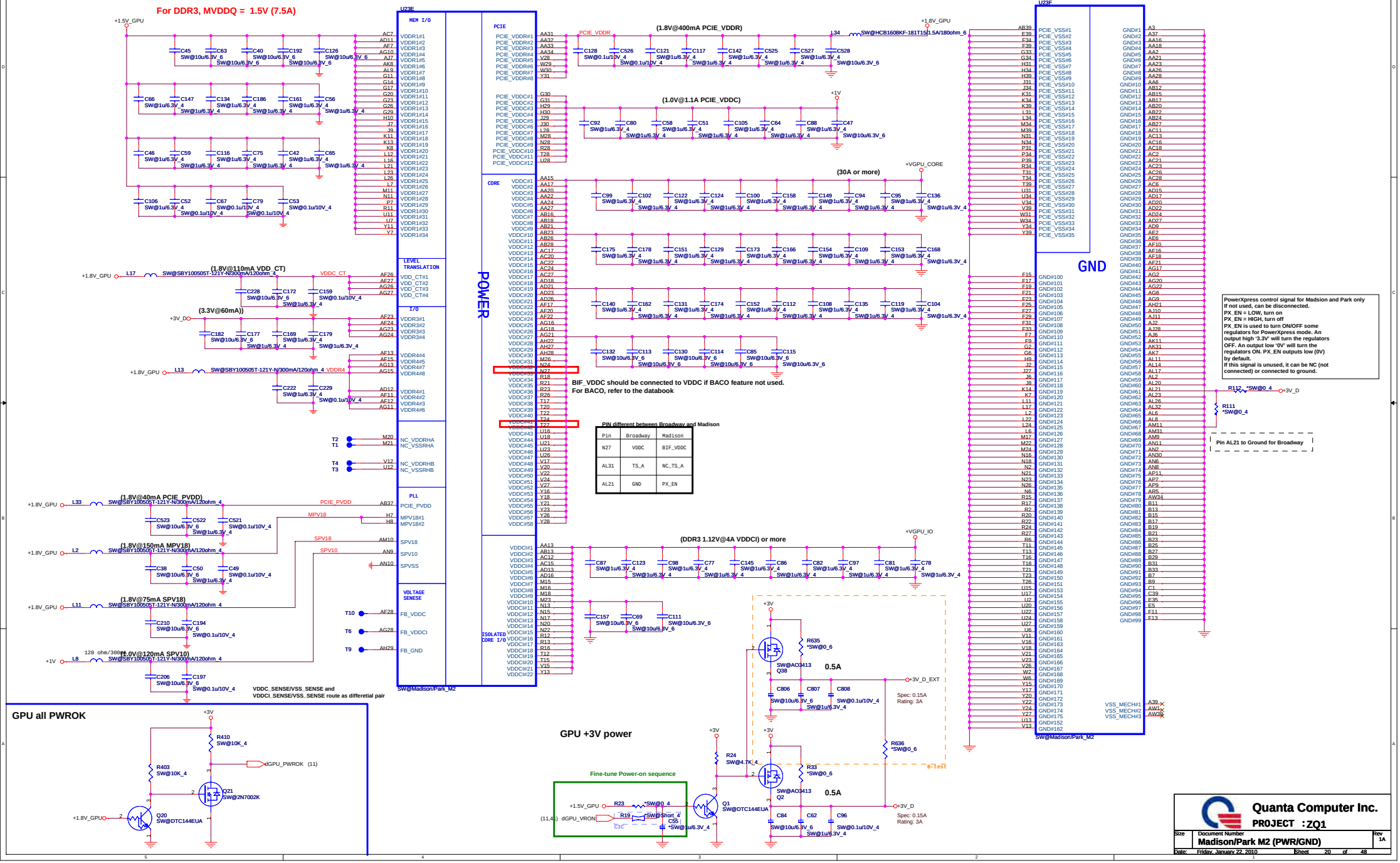
GPU_3(VGA)

Park M2-channel B used(S3 package use Channel A)



GPU_4(VGA)



Quanta Computer Inc.	
PROJECT : ZQ1	
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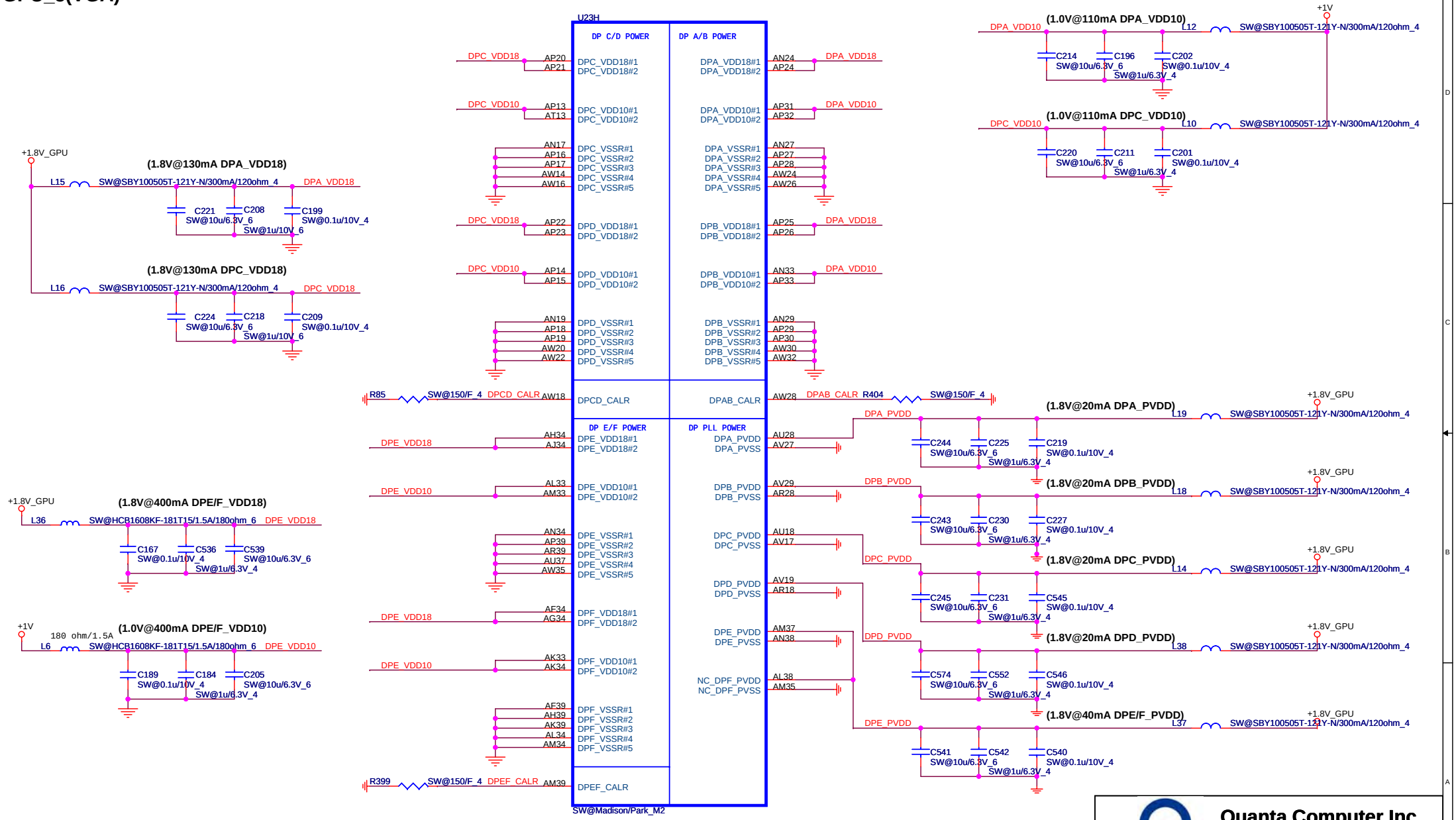
GPU_5(VGA)



Quanta Computer Inc.			
PROJECT : ZQ1			
Size	Document Number		Rev
	Madison/Park M2 (DP_PWR/GND)		1A
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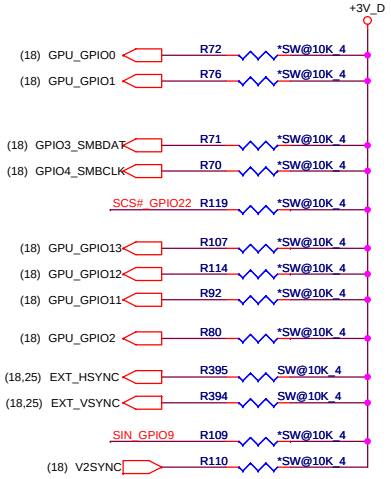
PIN STRAPS(VGA)



ROM Table		
Manufacturer	**Part Number**	**Code**
Numonyx ST Microelectronics	M25P05A	100
	M25P10A	101
	M25P20	101
	M25P40	101
	M25P80	101
Chingis PMC	Pm25LV512A	100
	Pm25LV010A	101

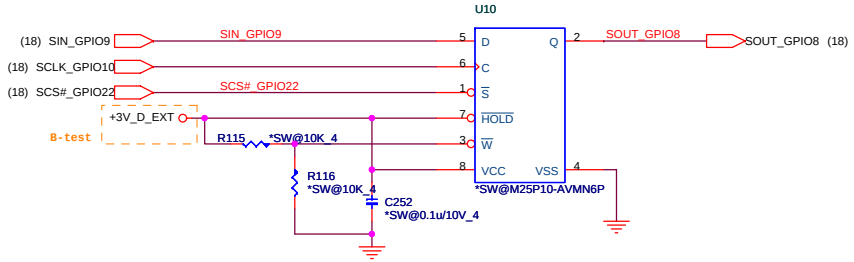
ROM Table		
EXT_HSYNC	**EXT_VSYNC**	**Discription**
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	1	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	101	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

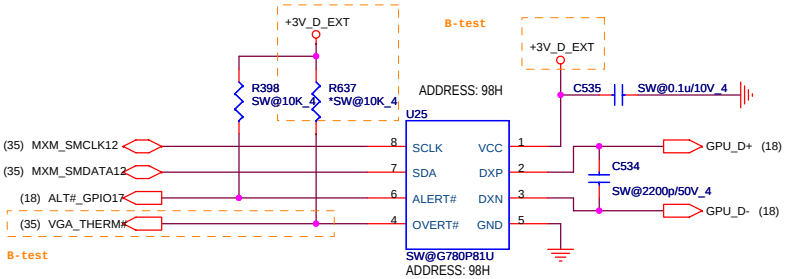
EEPROM(VGA)



Thermal Sensor(VGA)

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

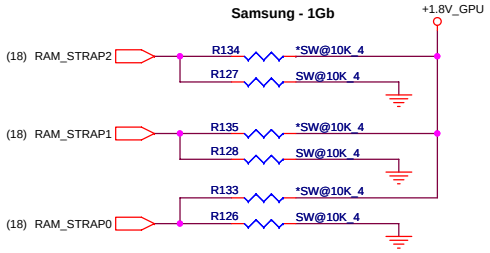
USD0.16



DDR3 Memory Aperture size(GPU)

DDR3 Memory Aperture size						
Vendor	**Vendor P/N**	**STN B/S P/N**	**Size**	**RAM_STRAP2** DVPDATA_2	**RAM_STRAP1** DVPDATA_1	**RAM_STRAP0** DVPDATA_0
Hynix			512Mb	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1Gb	1	0	0
			2Gb	1	0	1
Samsung			512Mb			
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1Gb	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2Gb	0	0	1
AMD	23EY2387MA12-SZ	AKD5LGGT700	1Gb	0	1	0

C-test



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

Quanta Computer Inc.
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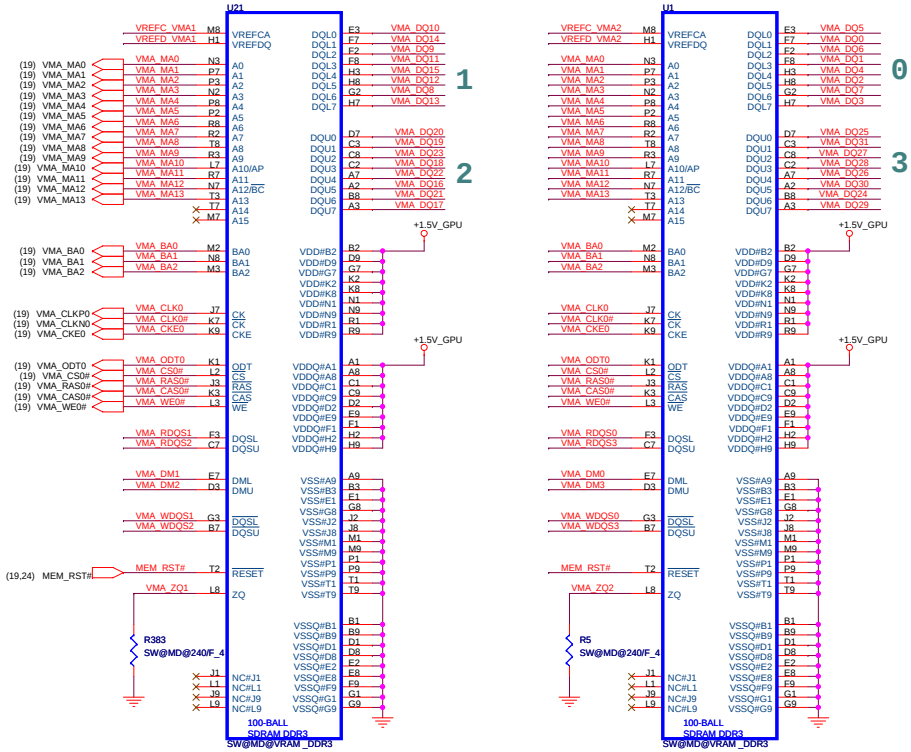
CHANNEL A: 512MB DDR3 (16*64M*4pcs)

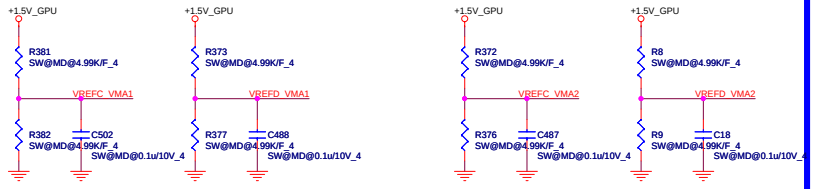
Park, M92M Use Channel B Memory Interface Only

(19) VMA_DQ[63..0] — VMA_DQ[63..0]
(19) VMA_DM[7..0] — VMA_DM[7..0]
(19) VMA_RDQS[7..0] — VMA_RDQS[7..0] — QSA[7..0]
(19) VMA_WDQS[7..0] — VMA_WDQS[7..0] — QSA#[7..0]

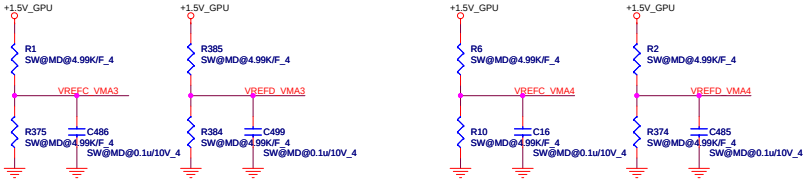


TOP Left | BOT Left | BOT Right | TOP Right

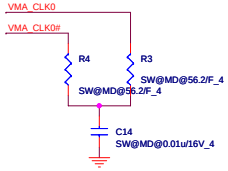
Group-A0 VREF



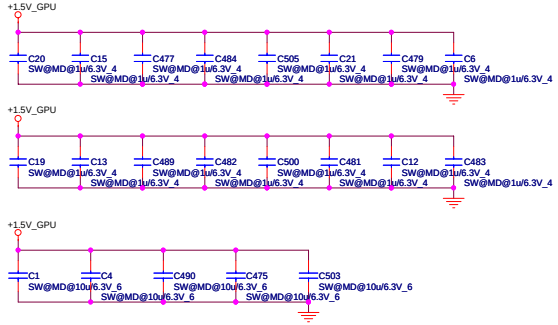
Group-A1 VREF



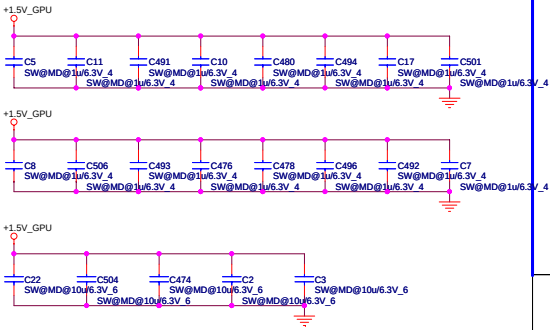
MEM_A0 CLK



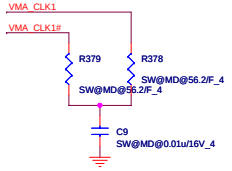
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK

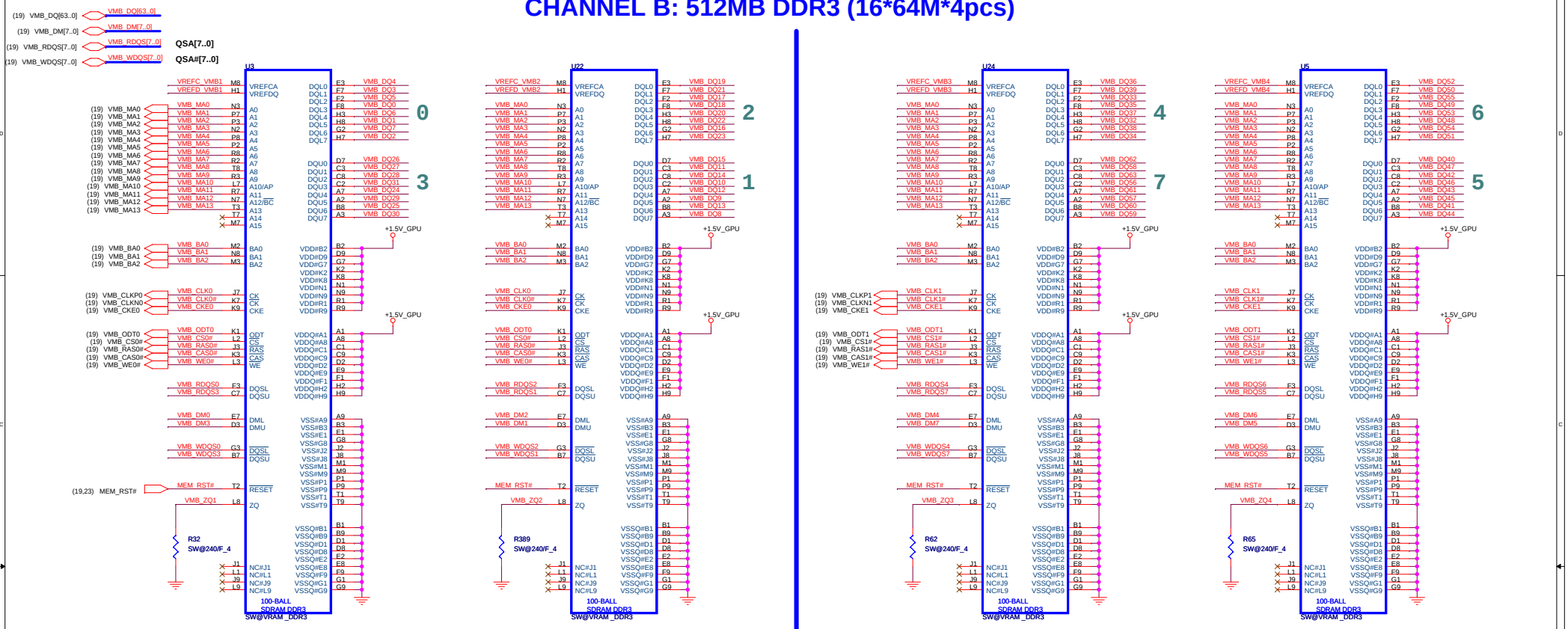


Quanta Computer Inc.
PROJECT : ZQ1

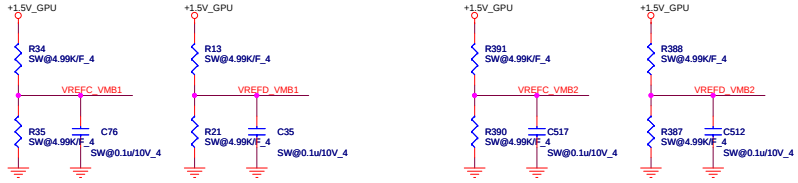
Size	Document Number	Rev
	MEMORY 1 channel A	1A

Date: Friday, January 22, 2010 Sheet 23 of 48

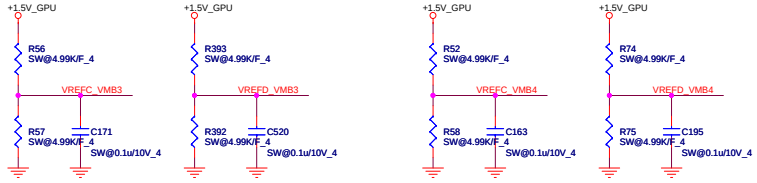
CHANNEL B: 512MB DDR3 (16*64M*4pcs)



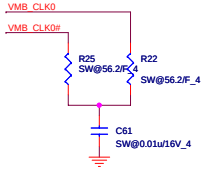
Group-B0 VREF



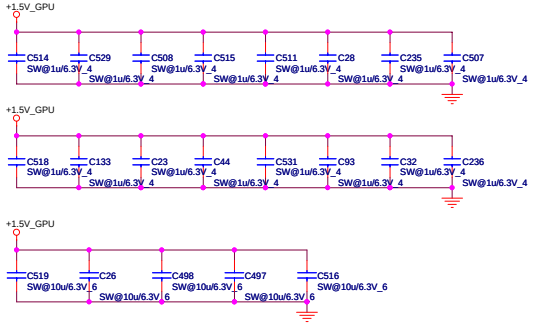
Group-B1 VREF



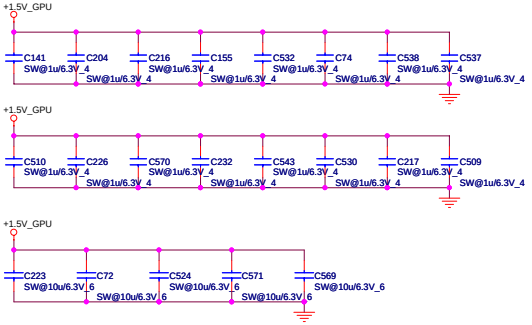
MEM_B0 CLK



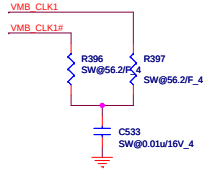
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK

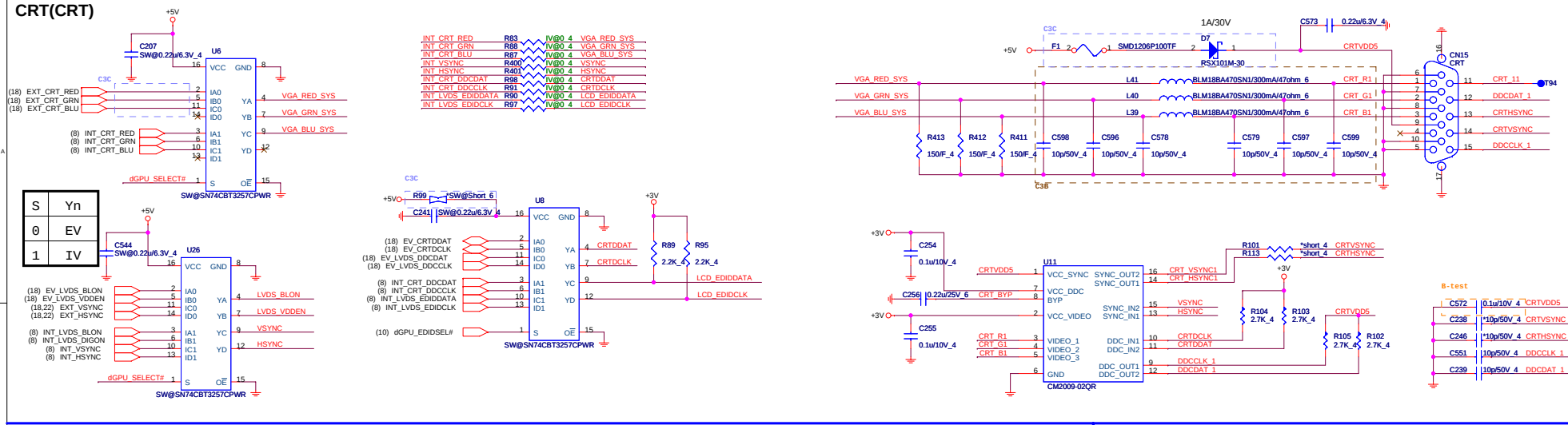


Quanta Computer Inc.

PROJECT : ZQ1

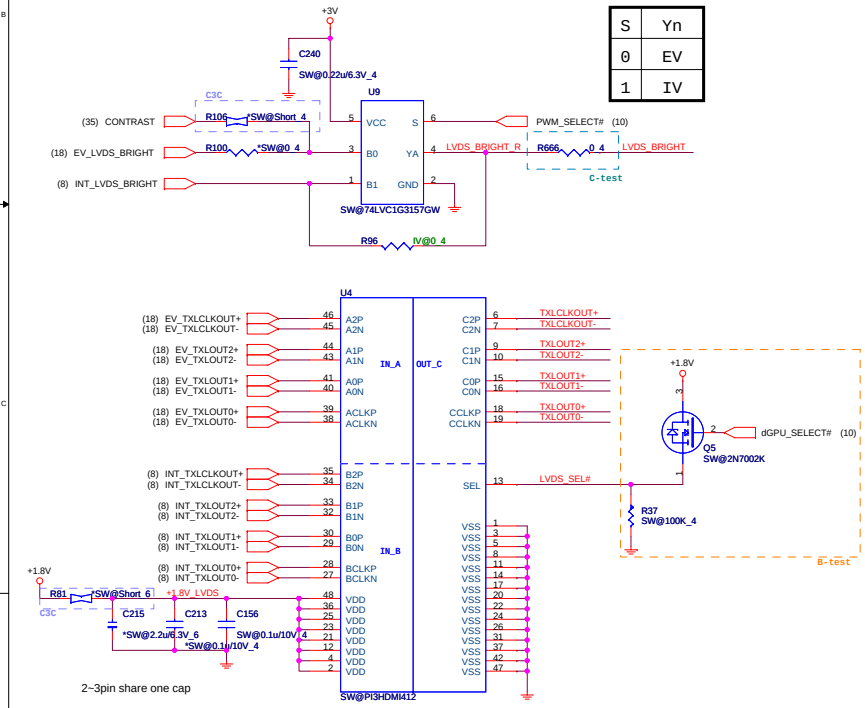
Size	Document Number	Rev
	MEMORY 2 channel B	1A
Date: Friday, January 22, 2010	Sheet 24 of 48	

CRT(CRT)

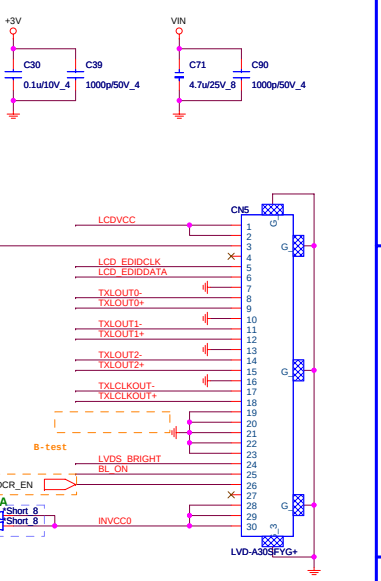


S	Yn
0	EV
1	IV

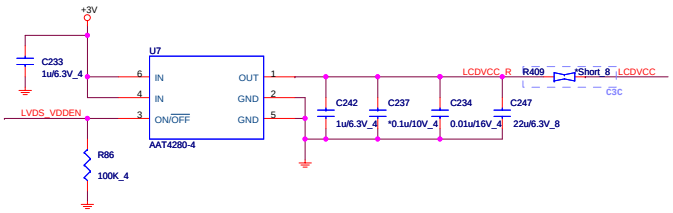
LVDS(LDS)



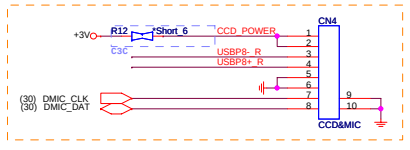
S	Yn
0	EV
1	IV



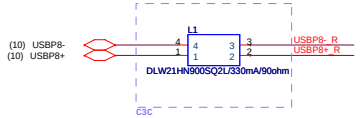
LCD Power(LDS)



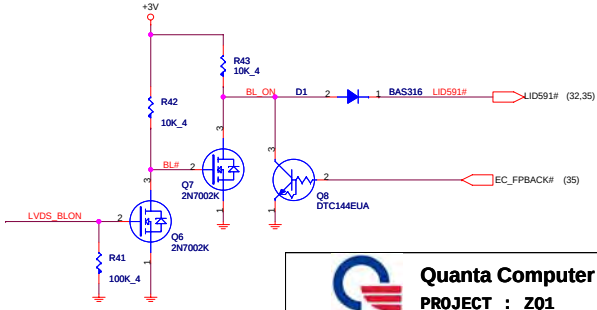
CCD&DMIC Conn.(CCD)



CAMERA Module(CCD)

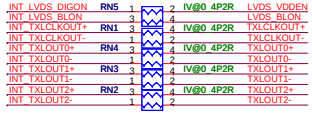


Backlight Control(LDS)



TI	AL3DV421V00
Pericom	AL000412W00

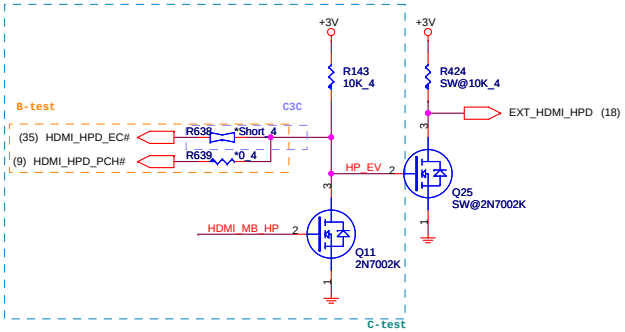
dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS



Quanta Computer Inc.
PROJECT : ZQ1

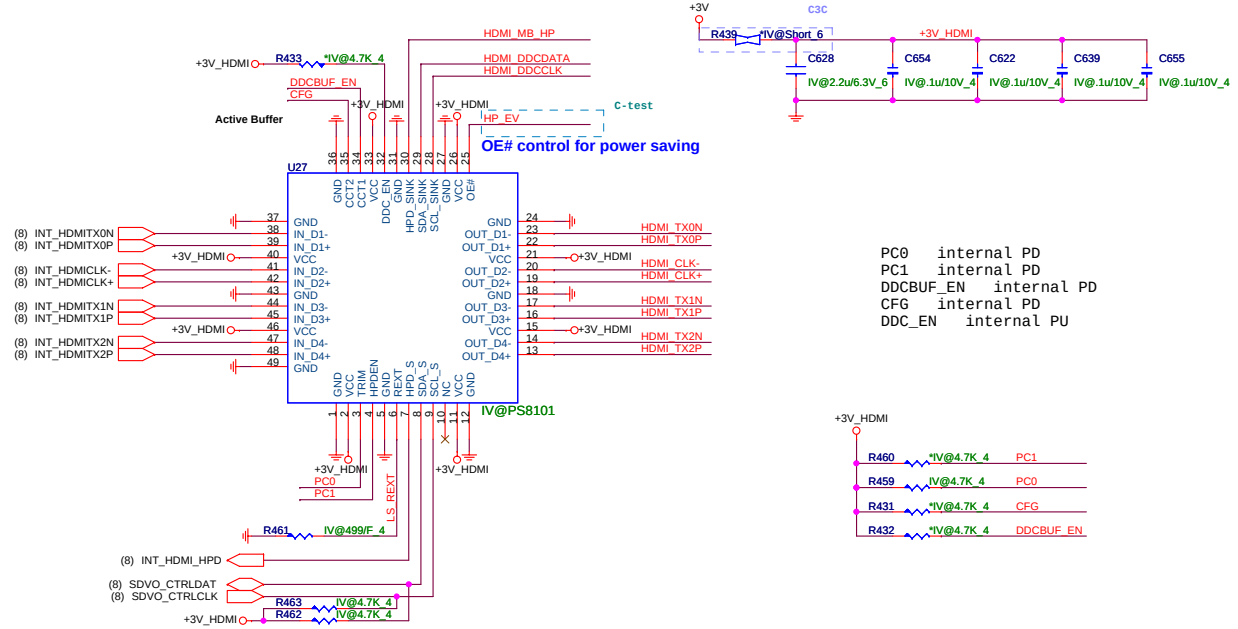
Size	Document Number	Rev
	CRT/LVDS	1A
Date: Friday, January 22, 2010	Sheet 25 of 48	

HDMI HPD(HDM)



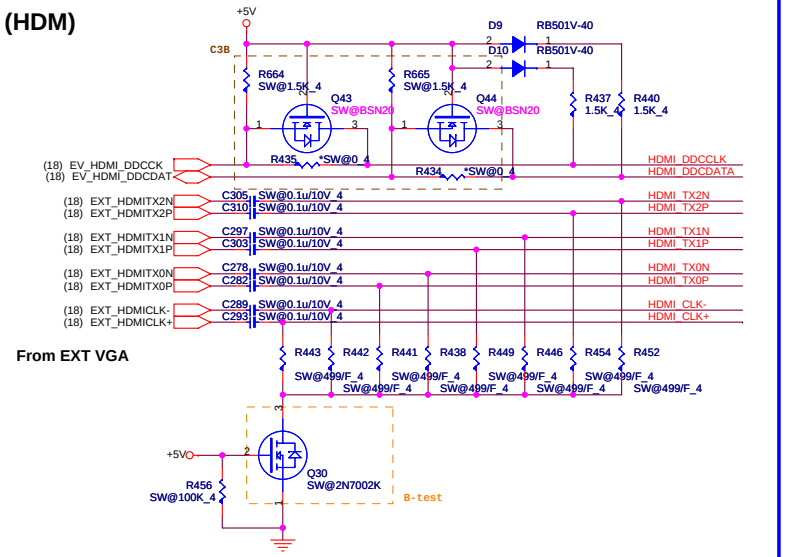
HDMI LEVEL SHIFTER(HDM)

PS8101 :: AL008101000

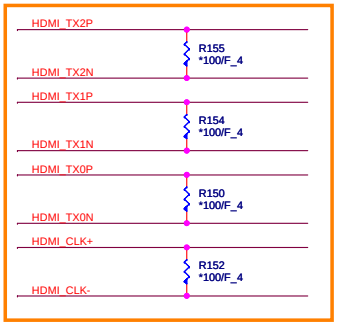


Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

(HDM)

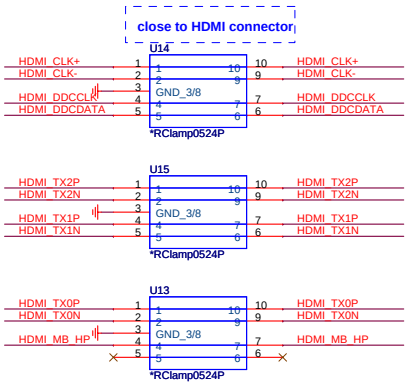


EMI reserve for HDMI(HDM)

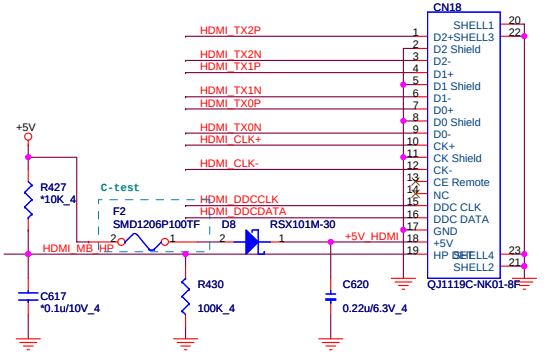


Close connector

ESD Protect



HDMI connector(HDM)



Quanta Computer Inc.

PROJECT : ZQ1

Size	Document Number	Rev
	HDMI	1A
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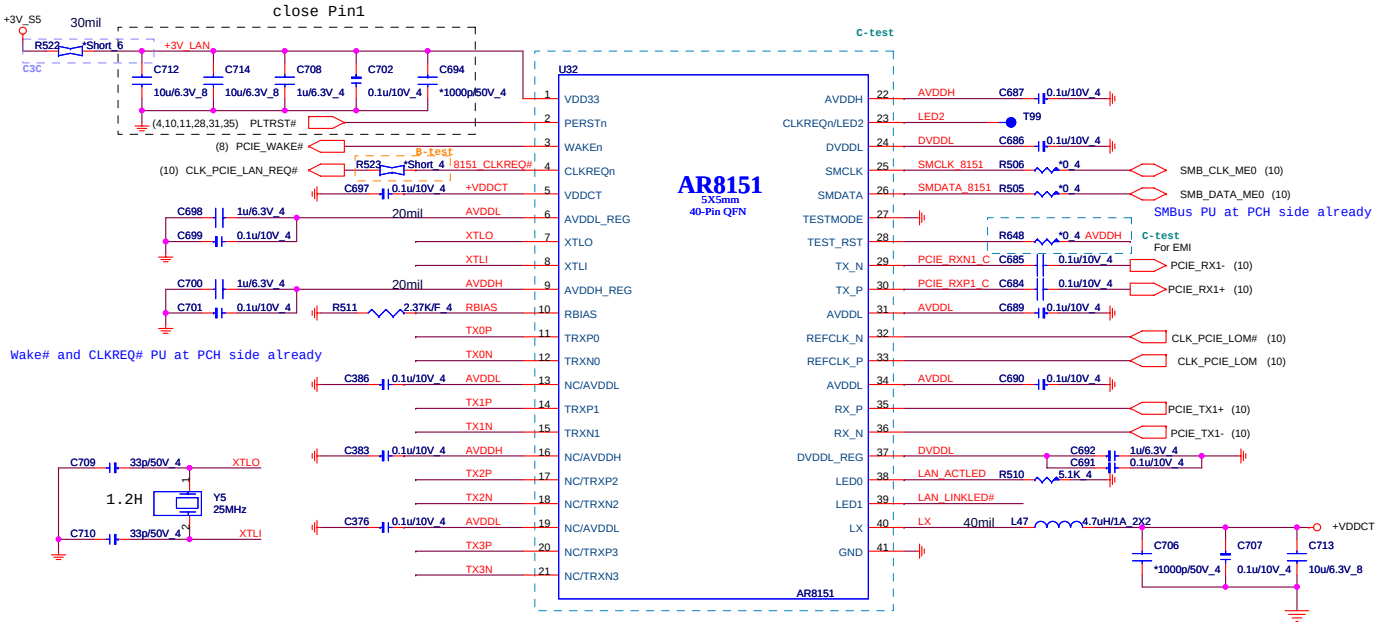
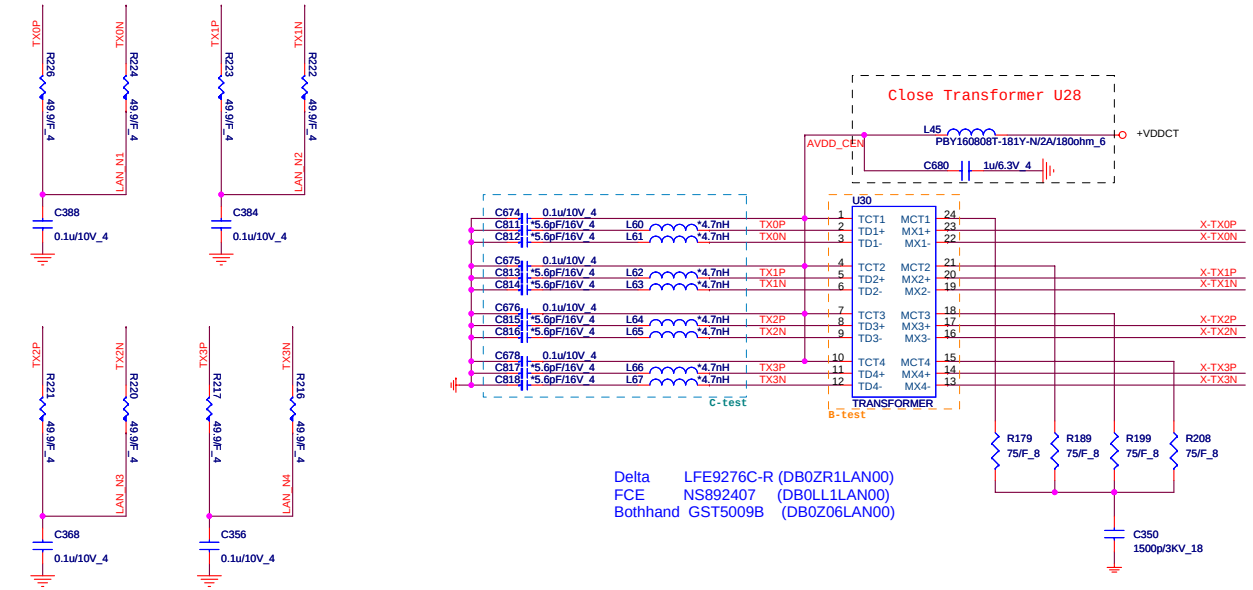
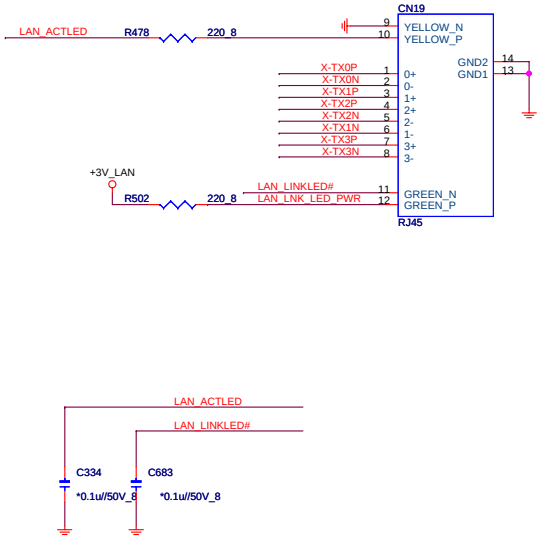
Giga-LAN AR8151(LAN)



TRANSFORMER(LAN)



RJ45(LAN)



Quanta Computer Inc.

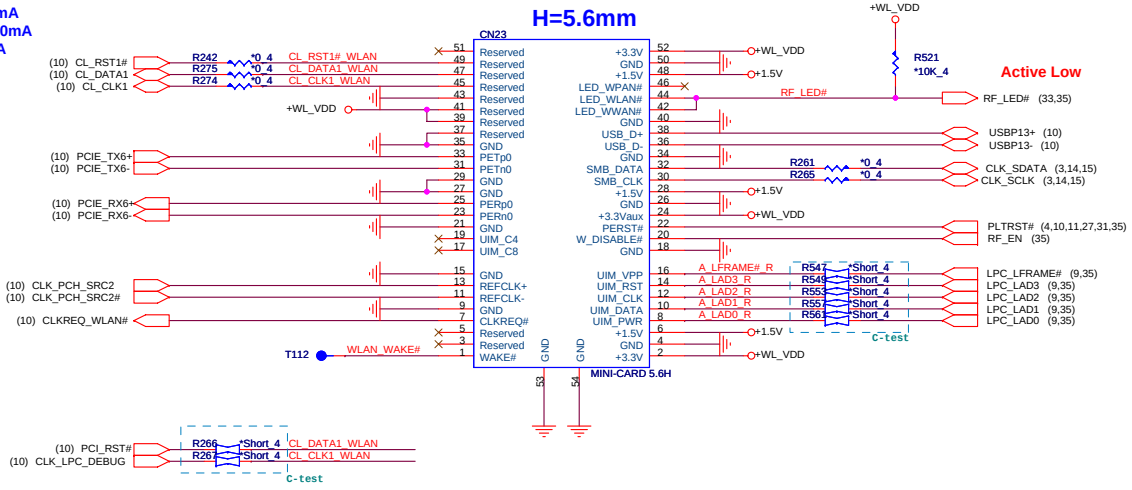
PROJECT : ZQ1

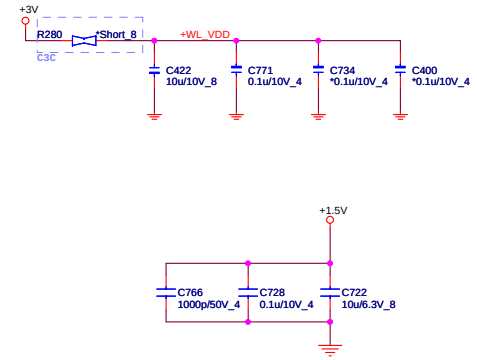
Size	Document Number	Rev
	LAN (AR8151)	1A

Date: Friday, January 22, 2010 Sheet 27 of 48

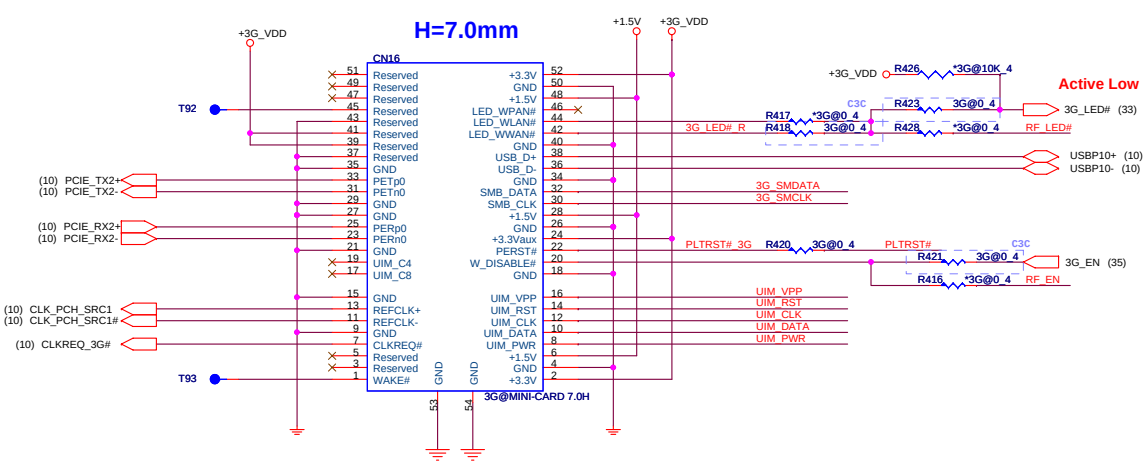
MINI-CARD WLAN(MPC)

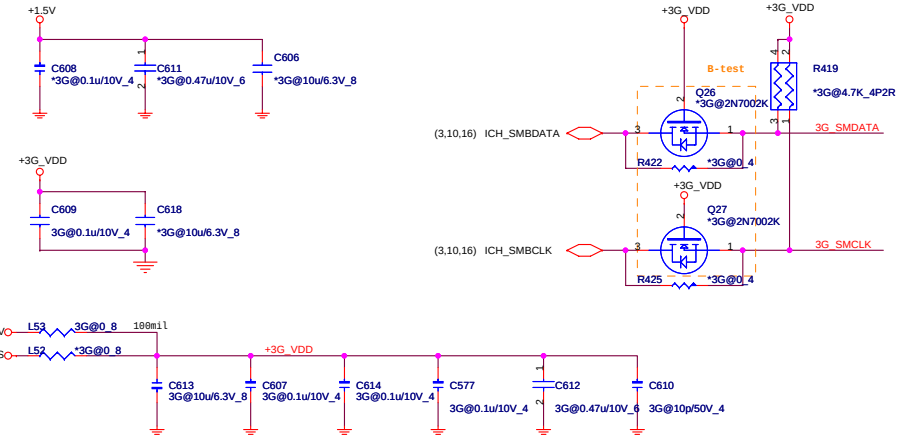
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA





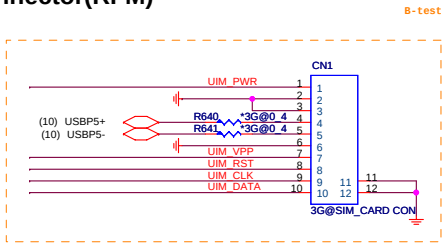
MINI-CARD 3G(MNC)Reserve for JV41-CP





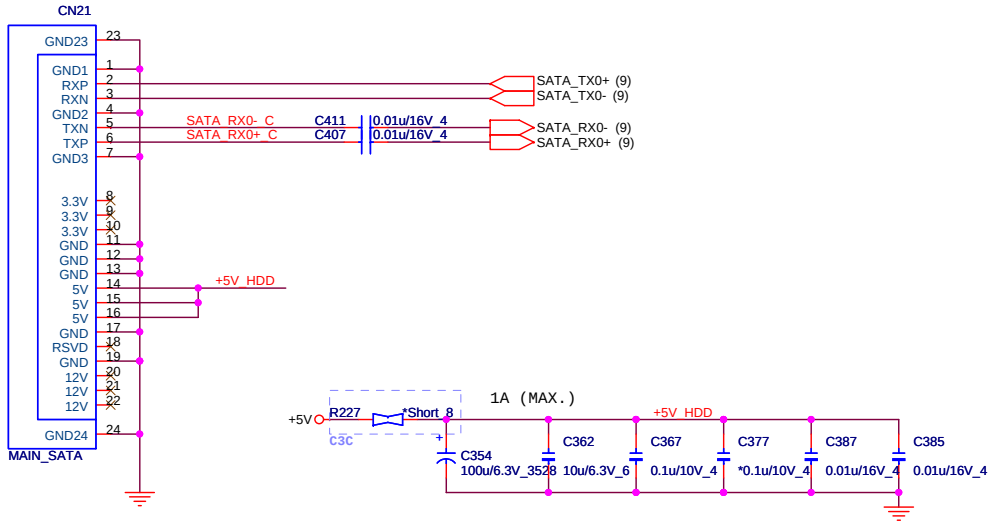
A:(10/17)FAE confirm:
3G module need +3VSUS and no need +1.5V and no need SMBUS

SIM CARD FFC connector(RFM)

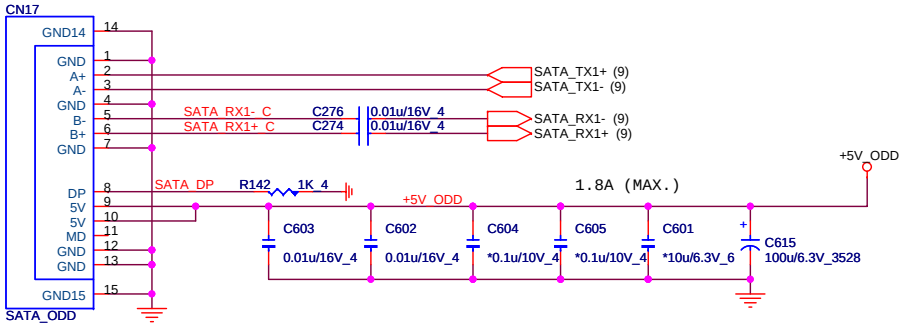


Quanta Computer Inc.		
PROJECT : ZQ1		
Size	Document Number: Mini-Card/WL/3G/SIM	Rev: 1A
Date: Friday, January 22, 2010	Sheet 28 of 48	

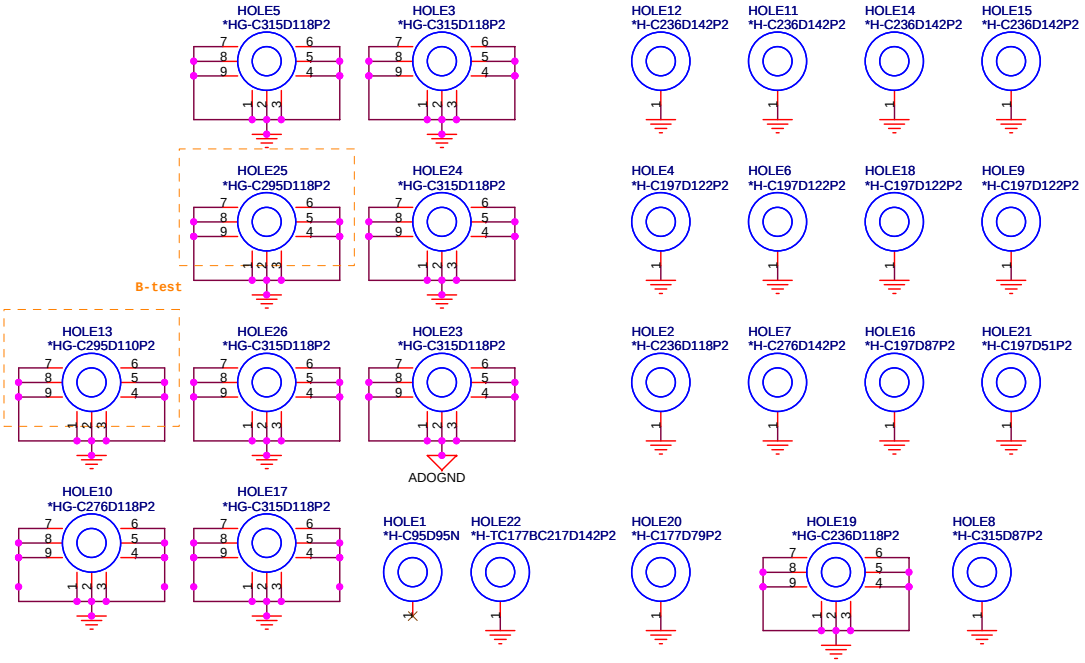
SATA HDD(HDD)



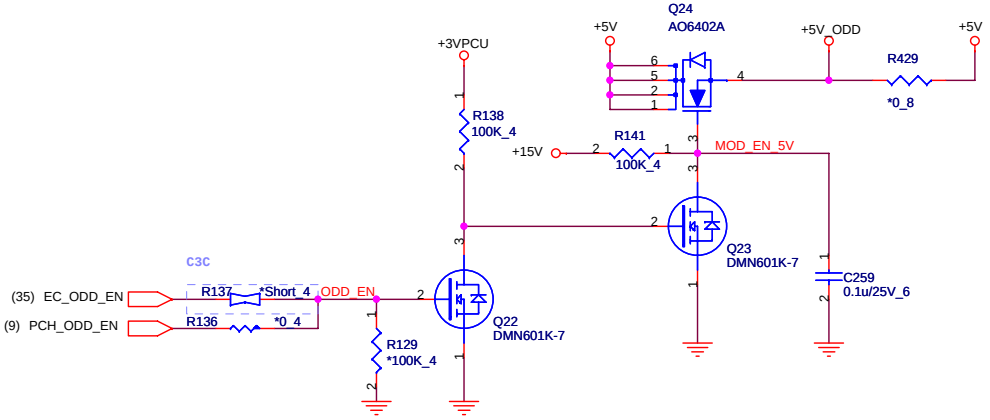
SATA ODD (ODD)



HOLE(OTH)



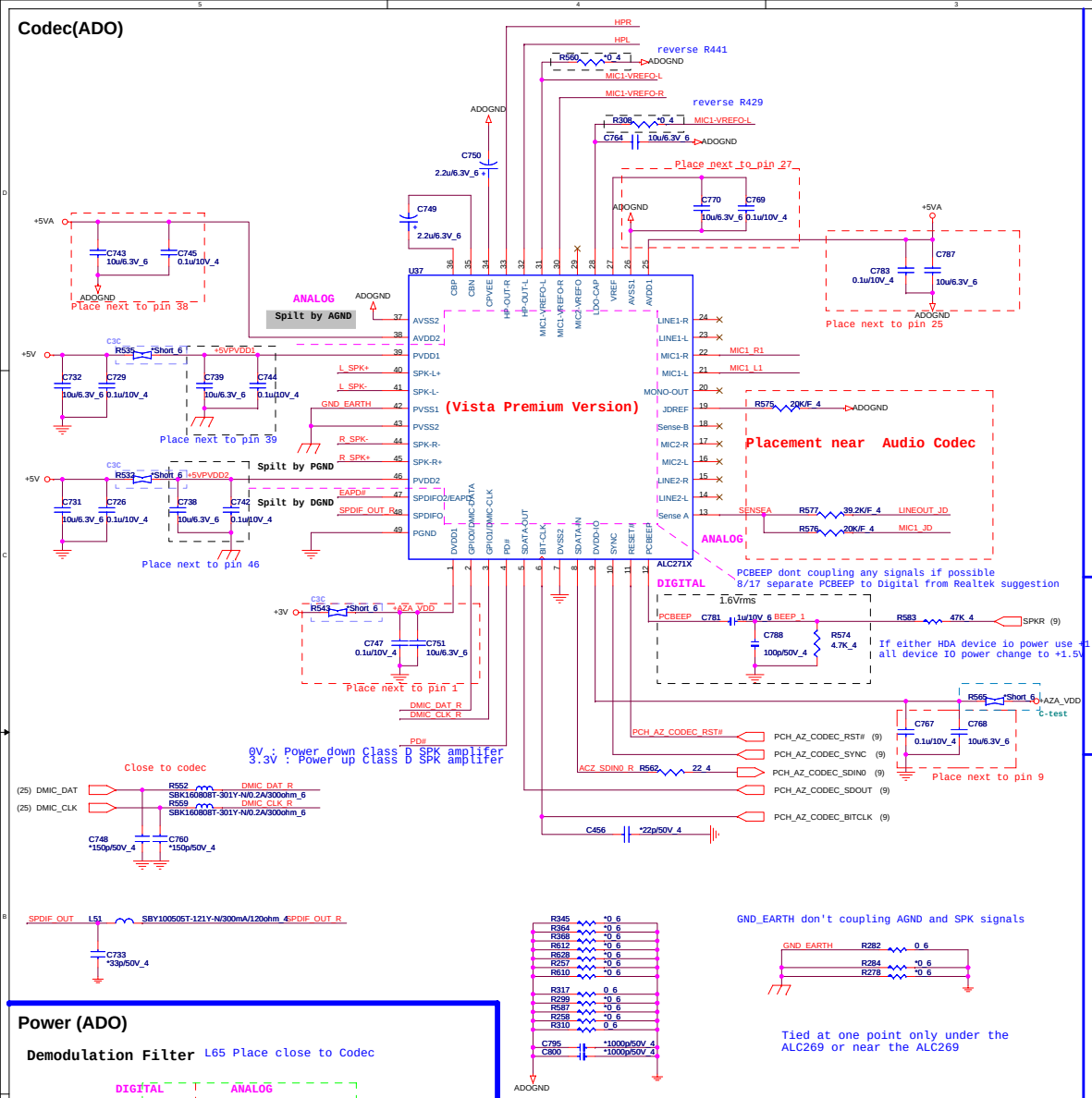
ODD POWER(ODD)



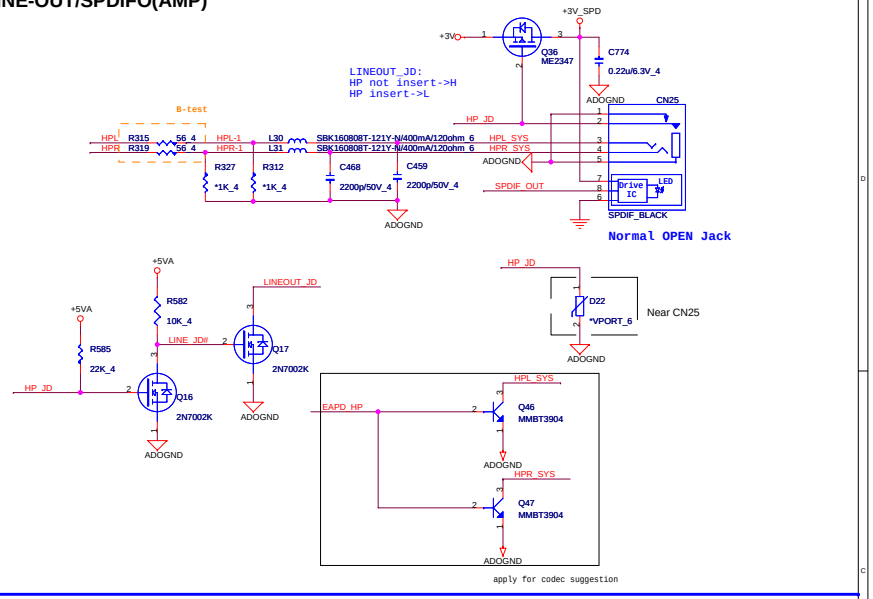
Connect to PCH(GPIO21) pin Y9
and EC pin28(GPIO53)

Quanta Computer Inc.		
PROJECT : ZQ1		
Size	Document Number: SATA-HDD/ODD/HOLE	Rev: 1A
Date: Friday, January 22, 2010	Sheet 29 of 48	

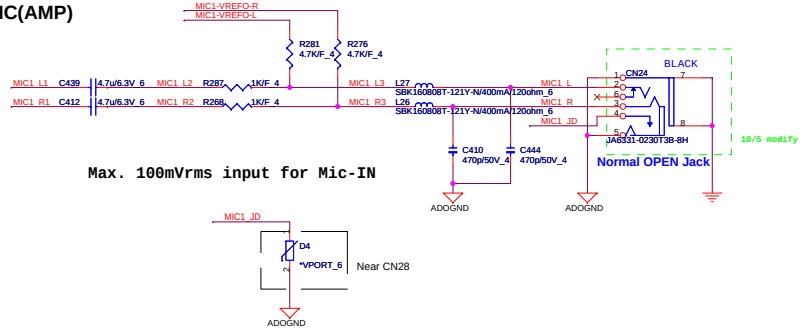
Codec(ADO)



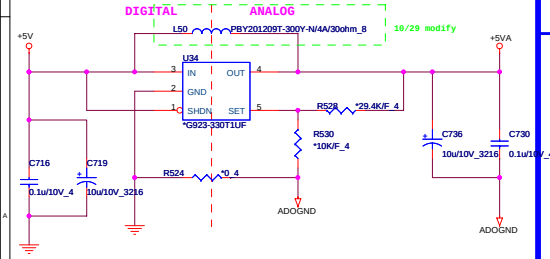
LINE-OUT/SPDIFO(AMP)



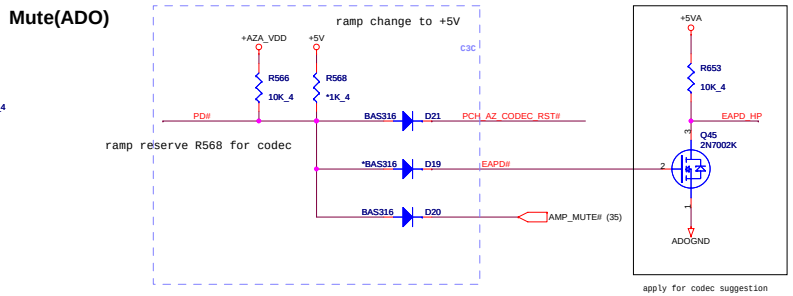
MIC(AMP)



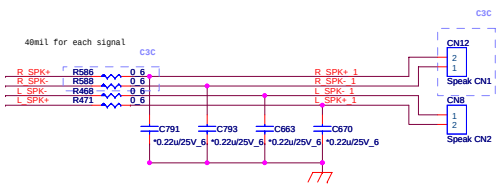
Power (ADO)



Mute(ADO)



Internal Speaker(AMP)



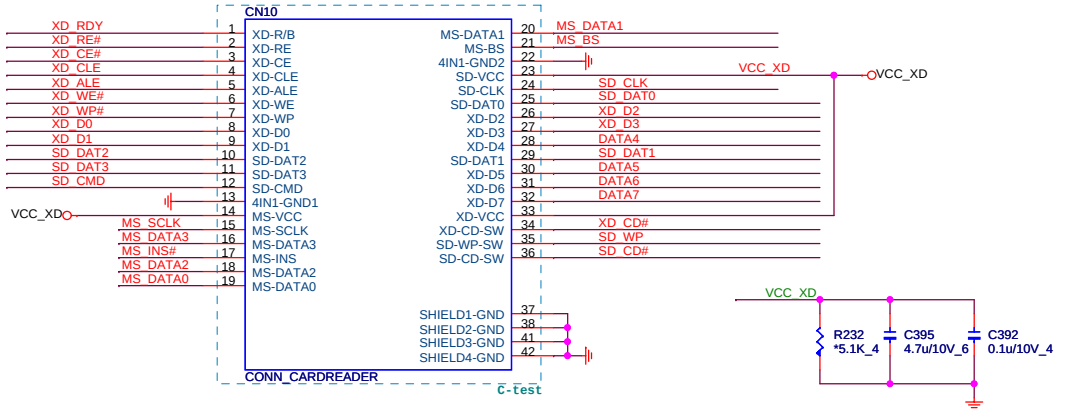
GND_EARTH don't coupling AGND and SPK signals

Tied at one point only under the ALC269 or near the ALC269

Quanta Computer Inc.			
PROJECT : ZQ1			
Size	Document Number		Rev
	ALC271X / AMP / SPK		1A
Date: Friday, January 22, 2010		Sheet 30 of 48	

Cardreader(MMC)

4 IN 1 CARD READER (MMC)



Main	DFHD36MS012
Second	DFHD38MS013

Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

C-test

R550 *Short_4 XTALSEL

Clock input selection
'1' for 48MHz input [Default]
'0' for 12MHz input

+1.8V_VDD
+3V_VDD
C759 0.1u/10V_4
C765 0.1u/10V_4
T111 T110

U36

CTRL0, CRTL 1 trace length shorter , and surround with GND.

(4,10,11,27,28,35) PLTRST#
R571 *Short_4
R572 *100K_4 +3V_VDD
C-test
C776 *0.47u/6.3V_4
R581 330_4
C3C
+3V
R546 *Short_6
+3V_VDD
C762 4.7u/10V_6
(10) USBP12+
(10) USBP12-
C778 *5p/50V_4
C777 *5p/50V_4
+1.8V_VDD
XI
XO

AU6437-GBL

GPON7
EXT48IN
RSTN
REXT
VD33P
DP
DM
VS33P
XI
XO
VDD
VDD

CTRL0
DATA5
CTRL2
GPI4
DATA4
DATA3
DATA2
XD_WP#
GPI2
XD_CE#
EEPDATA
GPI1

T106
T107
T105
T108

crystal trace width needs at least 10 mils.

C779 18p/50V_4
Y7 12MHz
R573 270K_4
C780 18p/50V_4
XI
XO

pin13 output 20mils
CAP close PIN11,12
C773 4.7u/10V_6

EEPCLK T109

pin14 output 15mils
VCC_XD

*0_4 R544
XD_CD#
CTRL4

SD write protect
1:decided by SDWP[Default]
0:letting SD always write-able

+1.8V_VDD
+3V_VDD
+3V_VDD
C755 4.7u/10V_6
C753 0.1u/10V_4

DATA0 SD_DAT0 MS_DATA0 XD_D0
DATA1 SD_DAT1 MS_DATA1 XD_D1
DATA2 SD_DAT2 MS_DATA2 XD_D2
DATA3 SD_DAT3 MS_DATA3 XD_D3

Close to connector

CTRL0 SD_CLK R525 SBK160808T-121Y-N/400mA/120ohm_6 XD_ALE C718 *10p/50V_4
MS_BS
B-test SD_WP
CTRL1 XD_CLE
MS_SCLK R233 SBK160808T-121Y-N/400mA/120ohm_6
SD_CMD C391 *10p/50V_4
CTRL2 XD_RDY
SD_CD#
CTRL3 XD_WE#
MS_INS#
CTRL4 XD_RE#

Quanta Computer Inc.
PROJECT : ZQ1

Size	Document Number	Rev
	AU6437 CardReader	1A
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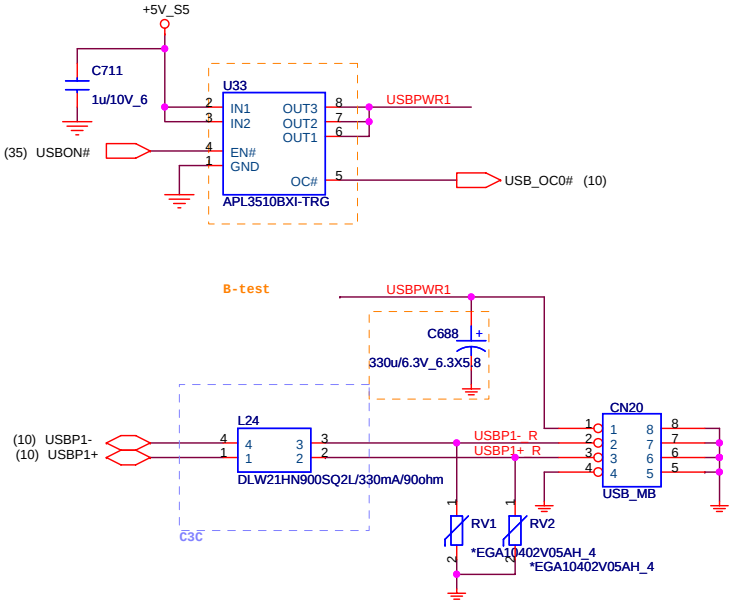
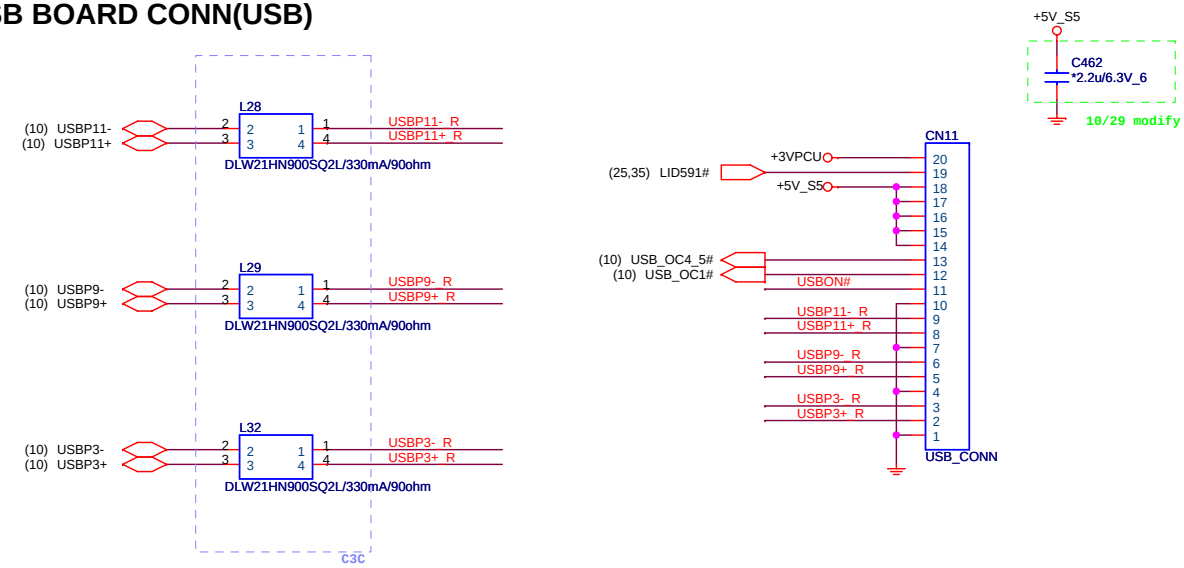
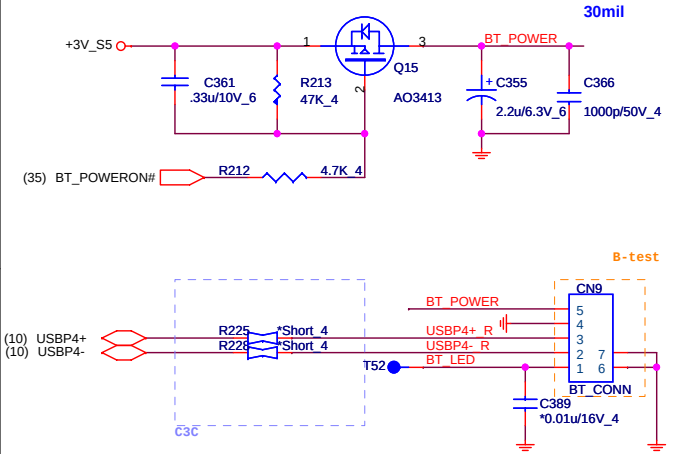
USB PORT(USB)



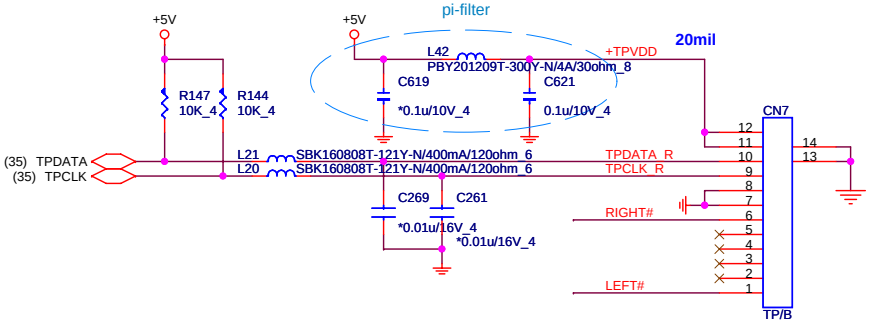
USB BOARD CONN(USB)



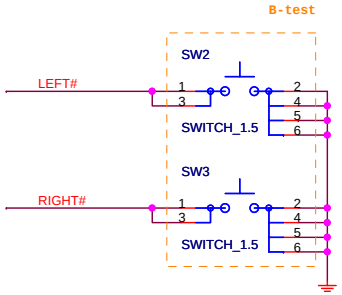
BLUETOOTH CONN(BTM)



TOUCHPAD BOARD CONN(TPD)



TP SWITCH(UIF)



Quanta Computer Inc.		
PROJECT : ZQ1		
Size	Document Number	Rev
	eSATA/USB	1A
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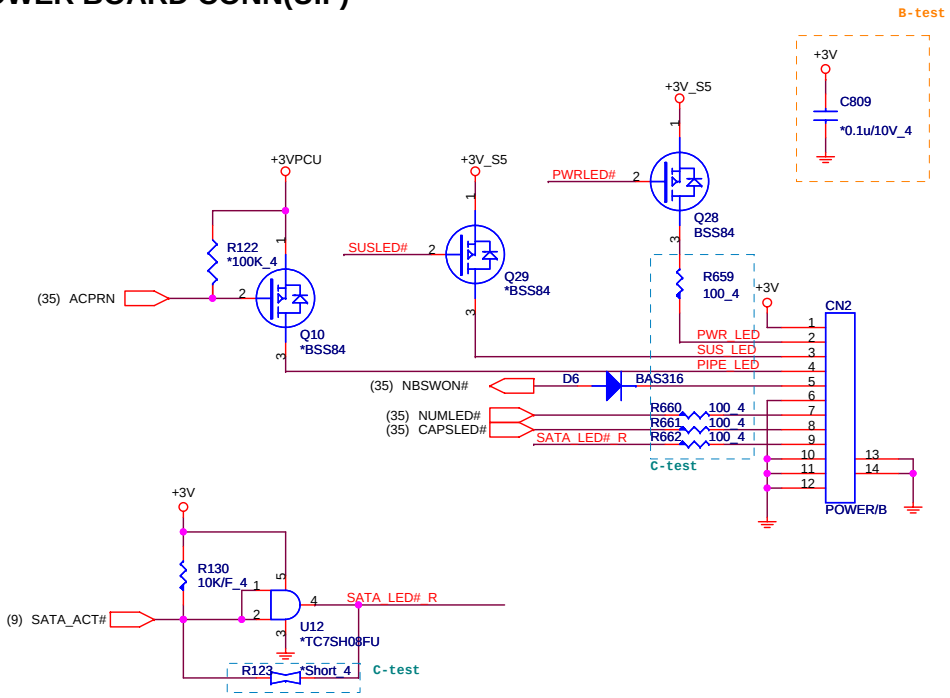
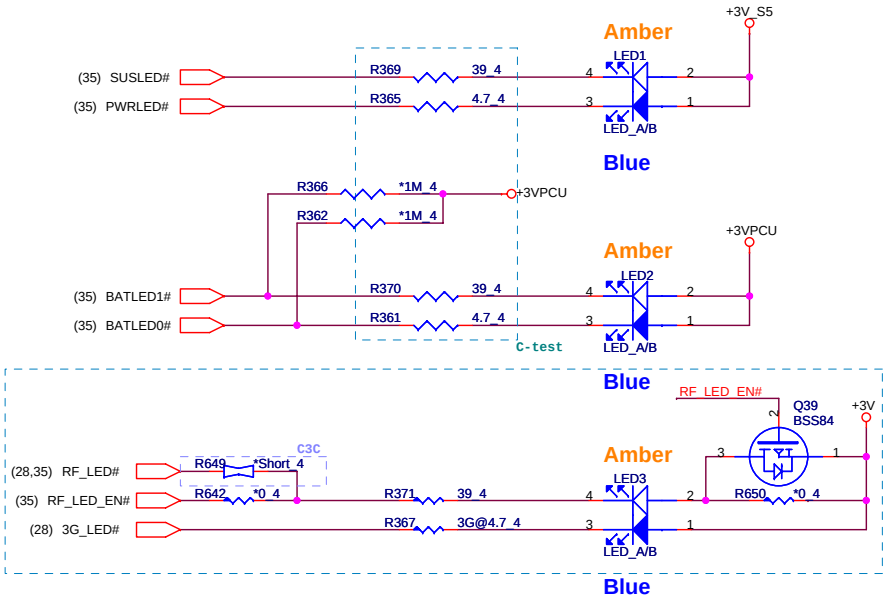
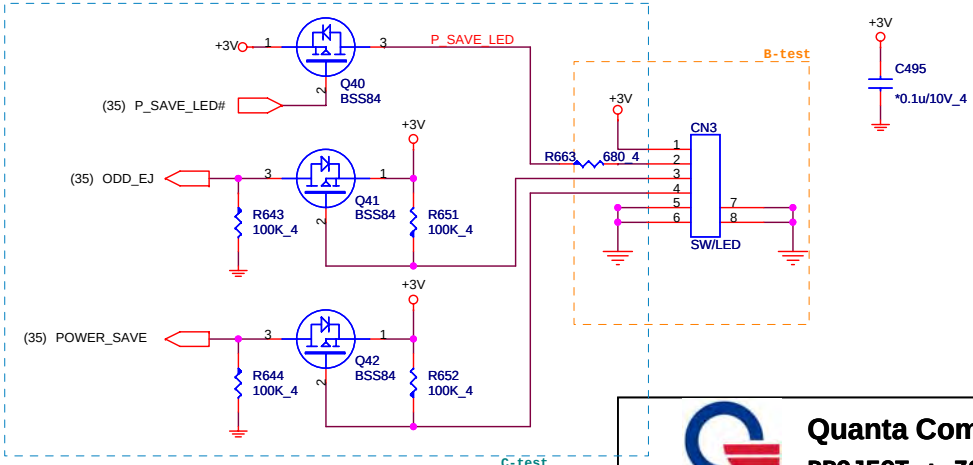
POWER BOARD CONN(UIF)



LED(UIF)



SW BOARD CONNECTOR(UIF)



Quanta Computer Inc.

PROJECT : ZQ1

Size	Document Number	Rev
	POWER BOARD/LED/SW DB	1A

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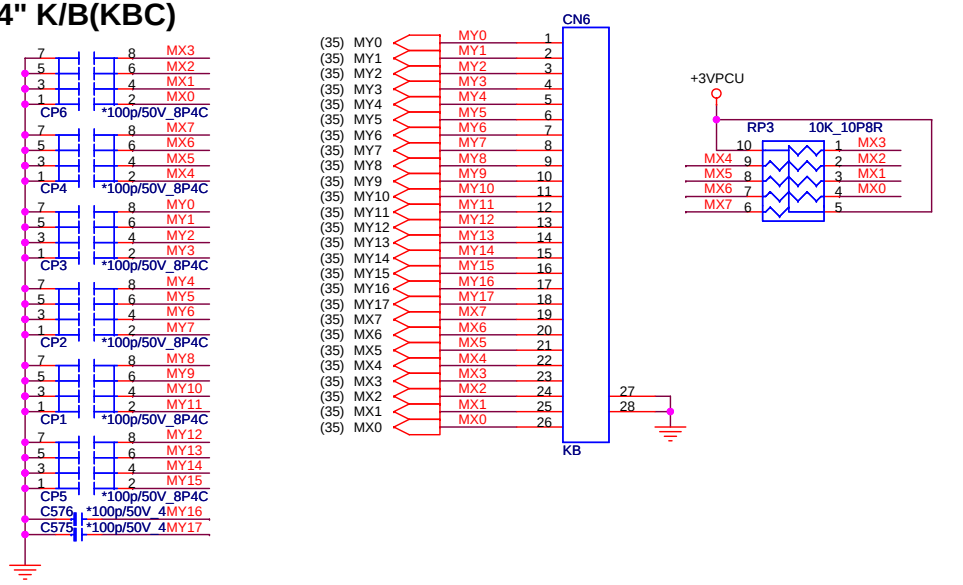
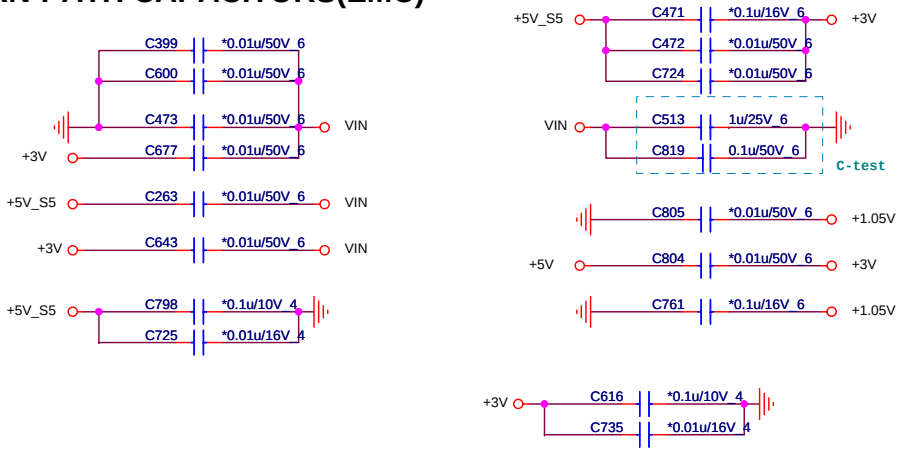
14" K/B(KBC)

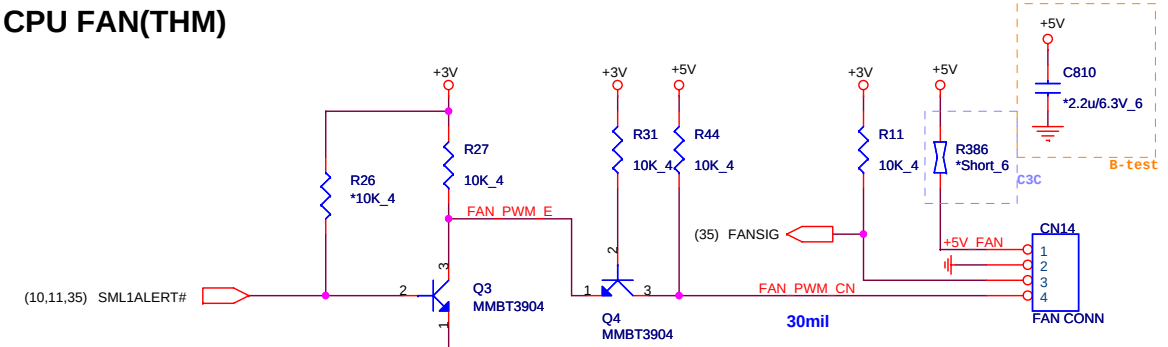


EE RETURN-PATH CAPACITORS(EMC)



STITCHING for LPC

CPU FAN(THM)



Quanta Computer Inc.		
PROJECT : ZQ1		
Size	Document Number: KB/FAN/EE RETURN CAP	Rev: 1A
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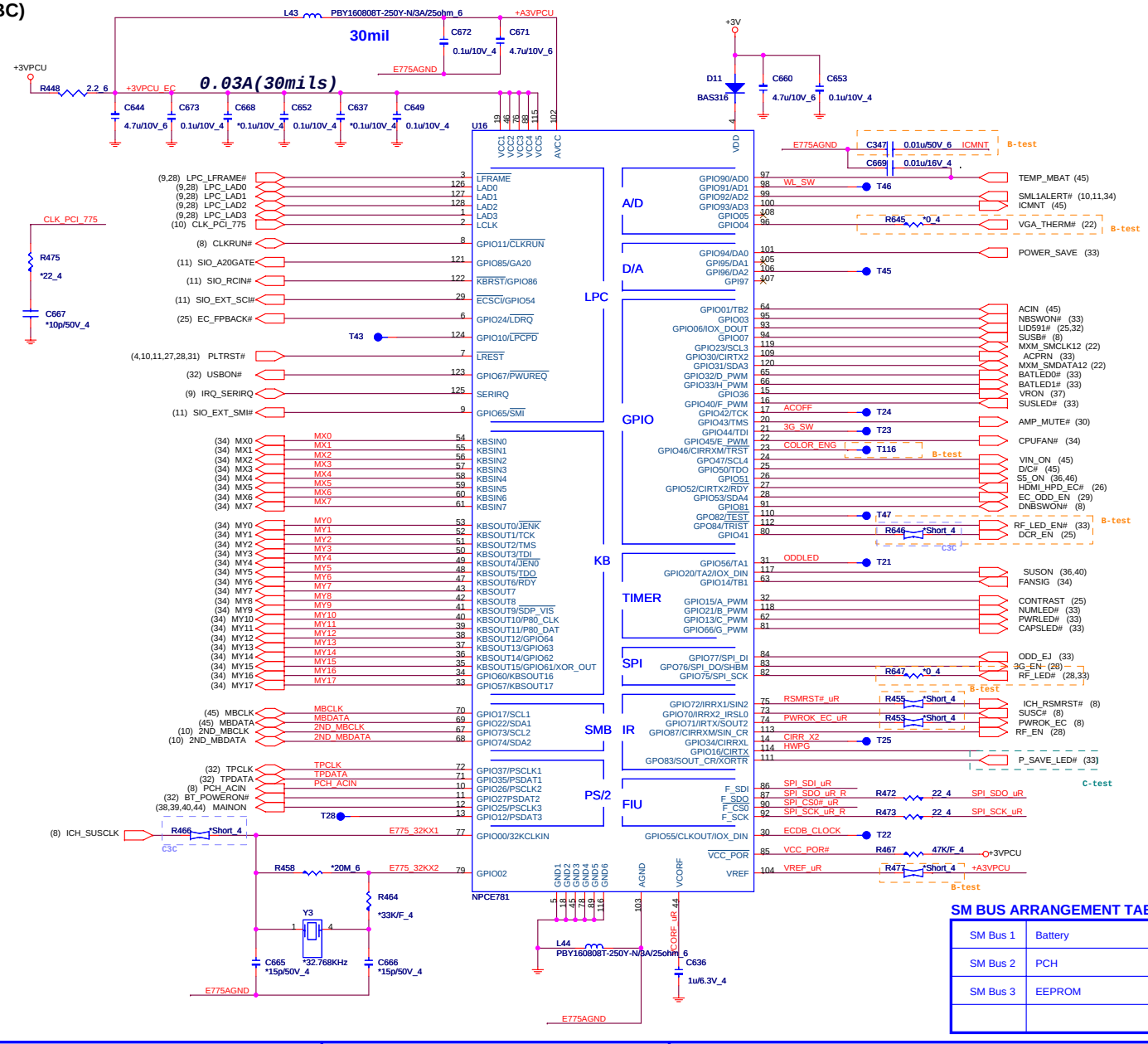
EC(KBC)



SM BUS ARRANGEMENT TABLE

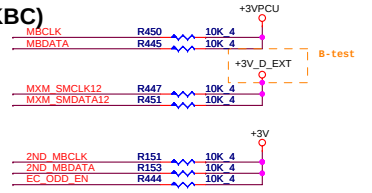
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	EEPROM

I/O ADDRESS SETTING(KBC)

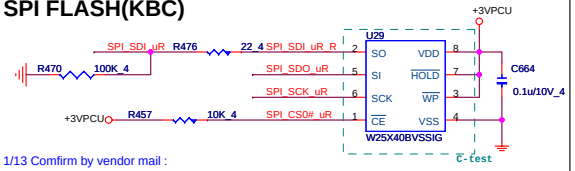
SHBM=0: Enable shared memory with host BIOS

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)

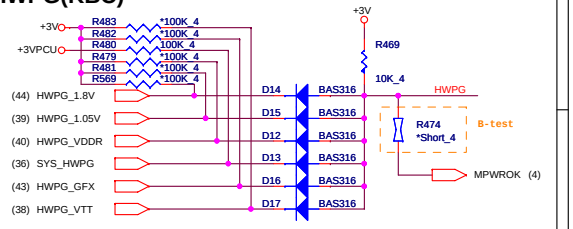


SPI FLASH(KBC)

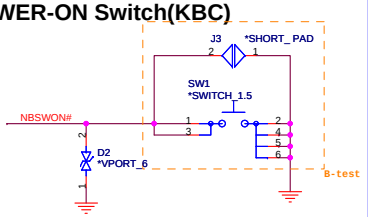


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

HWPG(KBC)



POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

Quanta Computer Inc.
PROJECT : ZQ1

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A

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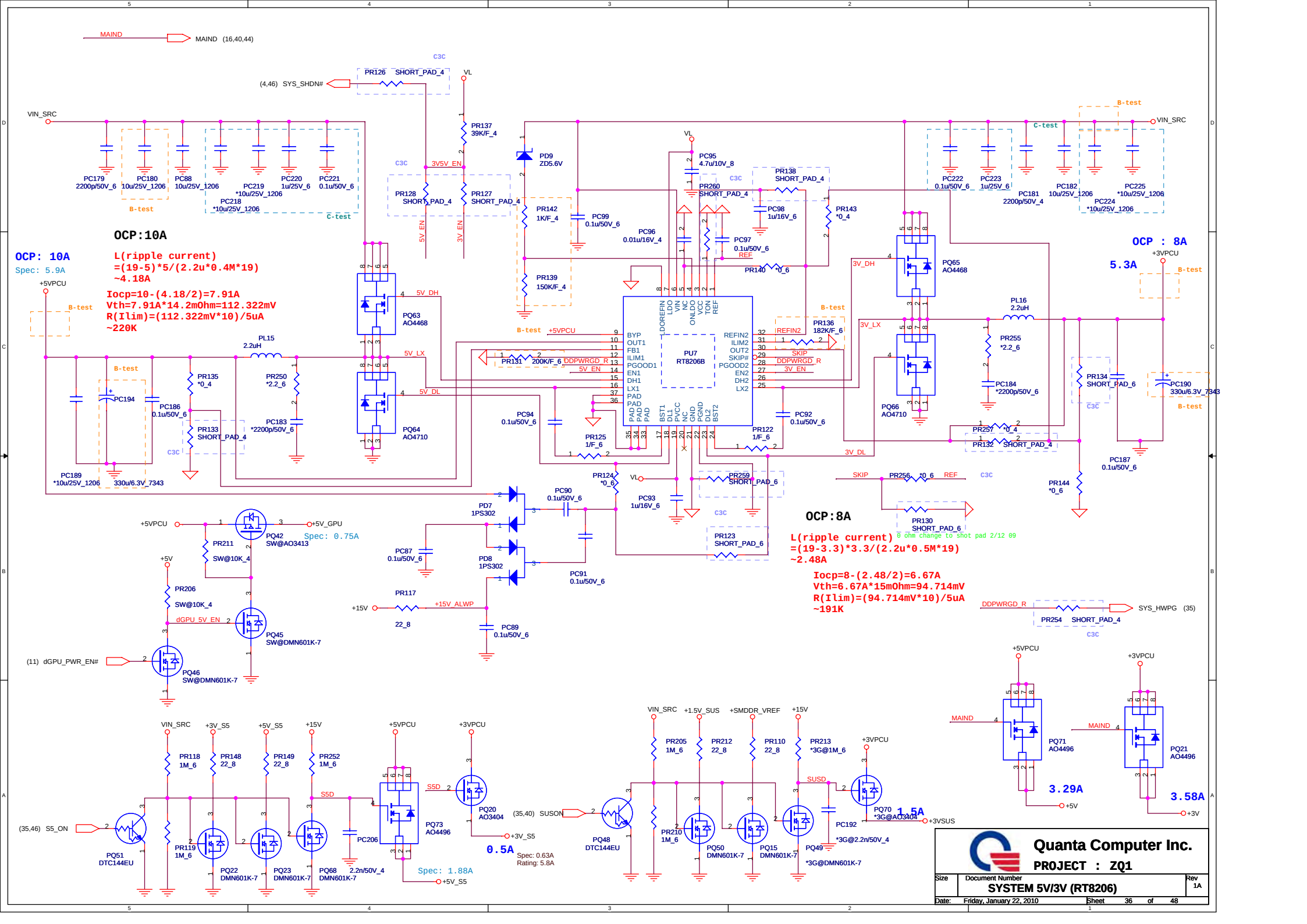
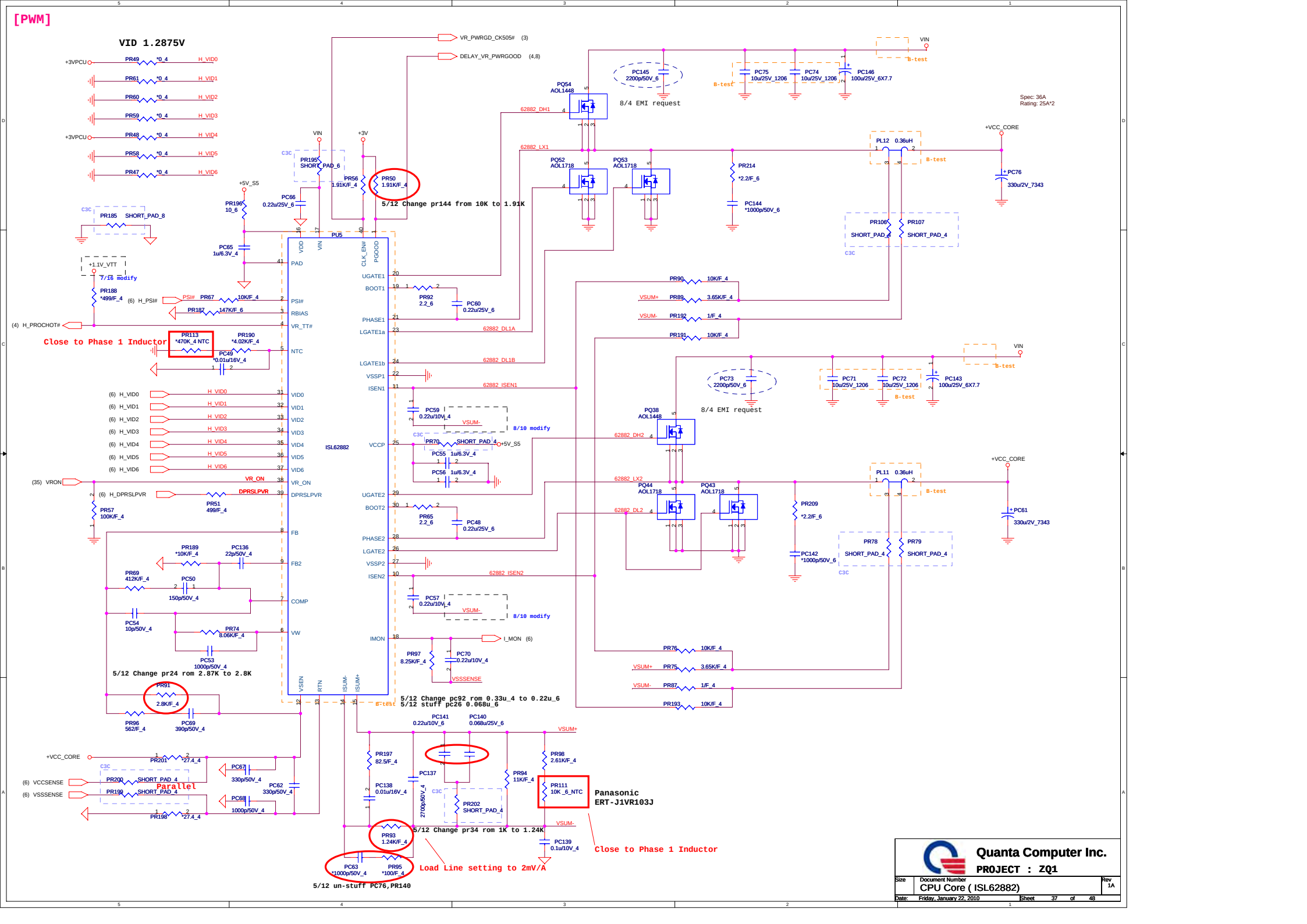

MAIND
MAIND (16,40,44)
(4,46) SYS_SHDN#
VIN_SRC
PR126 SHORT_PAD_4
VL
PR137 39K/F_4
3V5V_EN
PR128 SHORT_PAD_4
PR127 SHORT_PAD_4
PD9 ZD5.6V
PR142 1K/F_4
PR139 150K/F_4
PC99 0.1u/50V_6
PC96 0.01u/16V_4
PC95 4.7u/10V_8
PR260 SHORT_PAD_4
PC97 0.1u/50V_6
PR140 *0_6
PR138 SHORT_PAD_4
PC98 1u/16V_6
PR143 *0_4
PC179 2200p/50V_6
PC180 10u/25V_1206
PC88 10u/25V_1206
PC219 *10u/25V_1206
PC218 *10u/25V_1206
PC220 1u/25V_6
PC221 0.1u/50V_6
PC222 0.1u/50V_6
PC223 1u/25V_6
PC181 2200p/50V_4
PC182 10u/25V_1206
PC224 *10u/25V_1206
PC225 *10u/25V_1206
B-test
C-test
C3C
OCP:10A
OCP: 10A
Spec: 5.9A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
OCP : 8A
5.3A
+3VPCU
+5VPCU
PQ63 AO4468
PQ64 AO4710
PQ65 AO4468
PQ66 AO4710
5V_DH
5V_LX
5V_DL
3V_DH
3V_LX
3V_DL
PL15 2.2uH
PL16 2.2uH
PR135 *0_4
PR250 *2.2_6
PR183 *2200p/50V_6
PR133 SHORT_PAD_4
PC194
PC186 0.1u/50V_6
PC189 *10u/25V_1206
330u/6.3V_7343
PR255 *2.2_6
PC184 *2200p/50V_6
PR134 SHORT_PAD_6
PC190 330u/6.3V_7343
PR251 *0_4
PR132 SHORT_PAD_4
PC187 0.1u/50V_6
PR144 *0_6
PU7 RT8206B
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
PAD
PAD
PAD
LDOREFIN
LDO
VIN
NC
ONLOD
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
DL1
PVCC
NC
GND
DL2
BST2
PR131 200K/F_6
DDPWRGD_R
5V_EN
3V_EN
SKIP
REFIN2
PR136 182K/F_6
PR125 1/F_6
PR122 1/F_6
PC94 0.1u/50V_6
PC92 0.1u/50V_6
PR124 *0_6
PC93 1u/16V_6
PR259 SHORT_PAD_6
PR123 SHORT_PAD_6
PR256 *0_6
PR130 SHORT_PAD_6
0 ohm change to shot pad 2/12 09
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
PD7 1PS302
PD8 1PS302
PC90 0.1u/50V_6
PC91 0.1u/50V_6
PC87 0.1u/50V_6
PC89 0.1u/50V_6
PR117 22_8
+15V_ALWP
+5V_GPU
PQ42 SW@AO3413
Spec: 0.75A
PR211 SW@10K_4
PR206 SW@10K_4
dGPU_5V_EN
PQ45 SW@DMN601K-7
PQ46 SW@DMN601K-7
(11) dGPU_PWR_EN#
DDPWRGD_R
SYS_HWPG (35)
PR254 SHORT_PAD_4
VIN_SRC
+3V_S5
+5V_S5
+15V
PR118 1M_6
PR148 22_8
PR149 22_8
PR252 1M_6
S5D
PC206
PQ73 AO4496
PQ20 AO3404
PQ51 DTC144EU
PQ22 DMN601K-7
PQ23 DMN601K-7
PQ68 DMN601K-7
2.2n/50V_4
Spec: 1.88A
0.5A
Spec: 0.63A
Rating: 5.8A
(35,46) S5_ON
(35,40) SUSON
+1.5V_SUS
+SMDDR_VREF
PR205 1M_6
PR212 22_8
PR110 22_8
PR213 *3G@1M_6
SUSD
PQ48 DTC144EU
PQ50 DMN601K-7
PQ15 DMN601K-7
PQ49 *3G@DMN601K-7
PQ70 *3G@AO3404
PC192 *3G@2.2n/50V_4
1.5A
+3VSUS
MAIND
PQ71 AO4496
PQ21 AO4496
3.29A
3.58A
+5V
+3V
Quanta Computer Inc.
PROJECT : ZQ1
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1A
Date: Friday, January 22, 2010
Sheet 36 of 48


[PWM]
VID 1.2875V
+3VPCU
PR49 *0_4 H_VID0
PR61 *0_4 H_VID1
PR60 *0_4 H_VID2
PR59 *0_4 H_VID3
PR48 *0_4 H_VID4
PR58 *0_4 H_VID5
PR47 *0_4 H_VID6
VR_PWRGD_CK505# (3)
DELAY_VR_PWRGOOD (4,8)
VIN
+3V
+5V_S5
PR195 SHORT_PAD_6
PR56 1.91K/F_4
PR50 1.91K/F_4
5/12 Change pr144 from 10K to 1.91K
PR196 10_6
PC66 0.22u/25V_6
PC65 1u/6.3V_4
PR185 SHORT_PAD_8
+1.1V_VTT
7/16 modify
PR188 *499/F_4
(6) H_PSI#
PR67 10K/F_4
PR187 147K/F_6
(4) H_PROCHOT#
Close to Phase 1 Inductor
PR113 *470K_4 NTC
PR190 *4.02K/F_4
PC49 *0.01u/16V_4
PU5
ISL62882
VDD
VIN
CLK_EN#
PGOOD
PAD
PSI#
RBIAS
VR_TT#
NTC
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSLPVR
FB
FB2
COMP
VW
VSEN
RTN
ISUM-
ISUM+
UGATE1
BOOT1
PHASE1
LGATE1a
LGATE1b
VSSP1
ISEN1
VCCP
UGATE2
BOOT2
PHASE2
LGATE2
VSSP2
ISEN2
IMON
(35) VRON
(6) H_DPRSLPVR
PR57 100K/F_4
PR51 499/F_4
PR189 *10K/F_4
PC136 22p/50V_4
PR69 412K/F_4
PC50 150p/50V_4
PC54 10p/50V_4
PR74 8.06K/F_4
PC53 1000p/50V_4
5/12 Change pr24 rom 2.87K to 2.8K
PR91 2.8K/F_4
PR96 562/F_4
PC69 390p/50V_4
PR92 2.2_6
PC60 0.22u/25V_6
PR65 2.2_6
PC48 0.22u/25V_6
PC59 0.22u/10V_4
PC55 1u/6.3V_4
PC56 1u/6.3V_4
PC57 0.22u/10V_4
PR97 8.25K/F_4
PC70 0.22u/10V_4
I_MON (6)
VSSSENSE
62882_DH1
62882_LX1
62882_DL1A
62882_DL1B
62882_ISEN1
62882_DH2
62882_LX2
62882_DL2
62882_ISEN2
VSUM+
VSUM-
8/10 modify
PQ54 AOL1448
PQ52 AOL1718
PQ53 AOL1718
PC145 2200p/50V_6
8/4 EMI request
PC75 10u/25V_1206
PC74 10u/25V_1206
PC146 100u/25V_6X7.7
B-test
Spec: 36A
Rating: 25A*2
PR214 *2.2/F_6
PC144 *1000p/50V_6
PL12 0.36uH
+VCC_CORE
PC76 330u/2V_7343
PR106 SHORT_PAD_4
PR107 SHORT_PAD_4
C3C
PR90 10K/F_4
PR89 3.65K/F_4
PR192 1/F_4
PR191 10K/F_4
PQ38 AOL1448
PC73 2200p/50V_6
PC71 10u/25V_1206
PC72 10u/25V_1206
PC143 100u/25V_6X7.7
PQ44 AOL1718
PQ43 AOL1718
PR209 *2.2/F_6
PC142 *1000p/50V_6
PL11 0.36uH
PC61 330u/2V_7343
PR78 SHORT_PAD_4
PR79 SHORT_PAD_4
PR76 10K/F_4
PR75 3.65K/F_4
PR87 1/F_4
PR193 10K/F_4
PC141 0.22u/10V_6
PC140 0.068u/25V_6
PR197 82.5/F_4
PC137
PC138 0.01u/16V_4
2700p/50V_4
PR94 11K/F_4
PR98 2.61K/F_4
PR111 10K_6_NTC
Panasonic
ERT-J1VR103J
PR202 SHORT_PAD_4
5/12 Change pr34 rom 1K to 1.24K
PR93 1.24K/F_4
PC139 0.1u/10V_4
Close to Phase 1 Inductor
PC63 *1000p/50V_4
PR95 *100/F_4
Load Line setting to 2mV/A
5/12 un-stuff PC76,PR140
5/12 Change pc92 rom 0.33u_4 to 0.22u_6
5/12 stuff pc26 0.068u_6
+VCC_CORE
PR201 *27.4_4
PR200 SHORT_PAD_4
PR199 SHORT_PAD_4
PR198 *27.4_4
PC67 330p/50V_4
PC62 330p/50V_4
PC68 1000p/50V_4
Parallel
(6) VCCSENSE
(6) VSSSENSE
Quanta Computer Inc.
PROJECT : ZQ1
Size
Document Number
CPU Core (ISL62882)
Rev
1A
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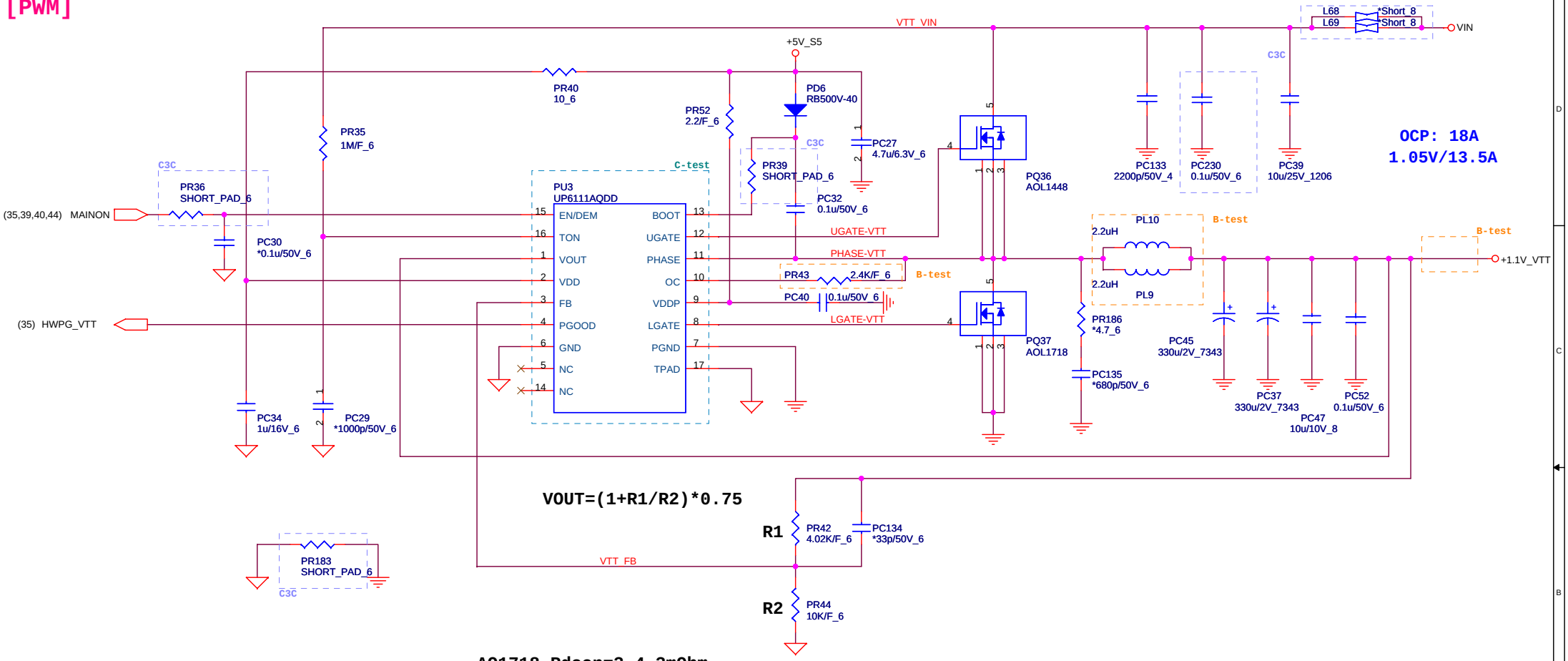
[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A

4.3m*18=RILIM*20uA
RILIM=3.87K --- 3.92K

Quanta Computer Inc.		
PROJECT : ZQ1		
Size	Document Number: +VTT (UP6111A)	Rev: 1A
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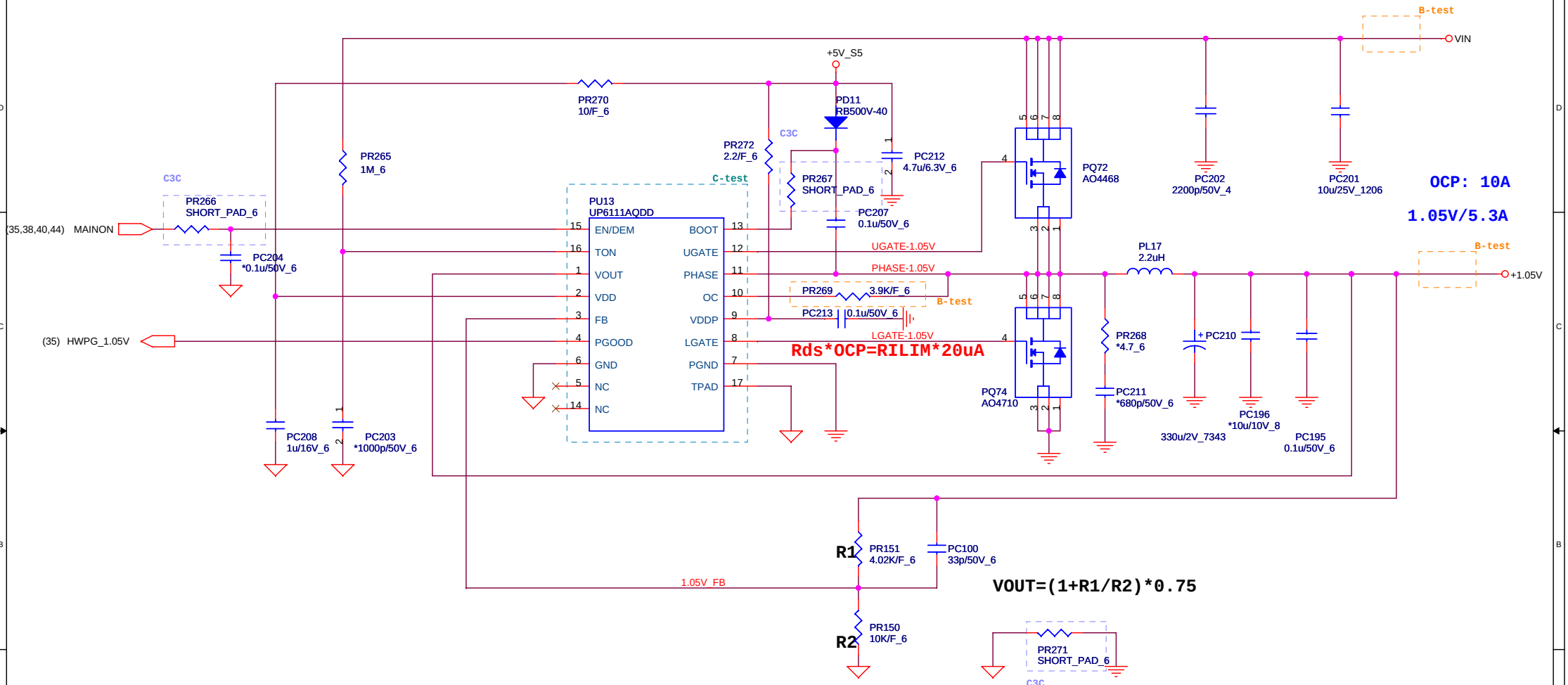


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

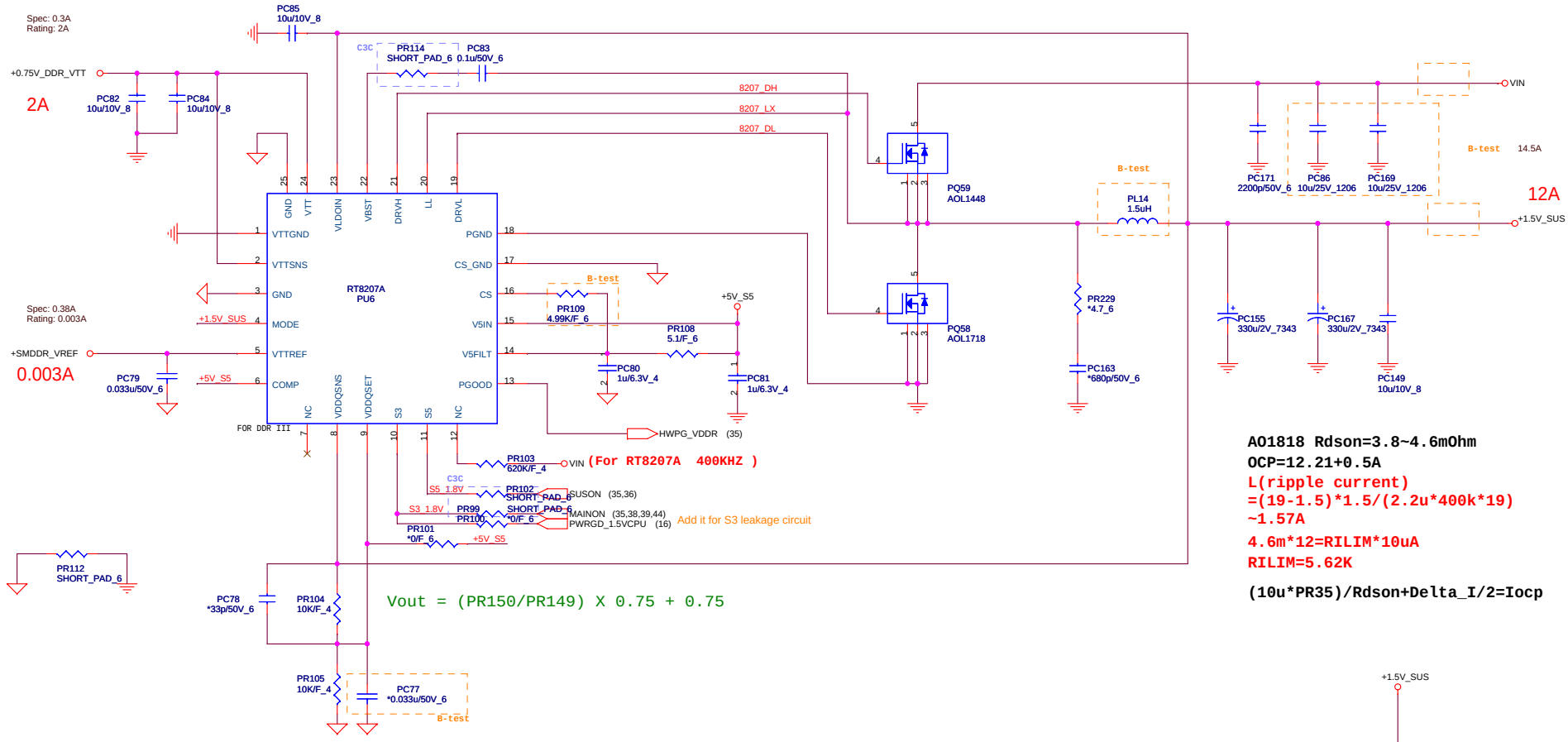
AO4710 Rdson=11.7~14.2mOhm

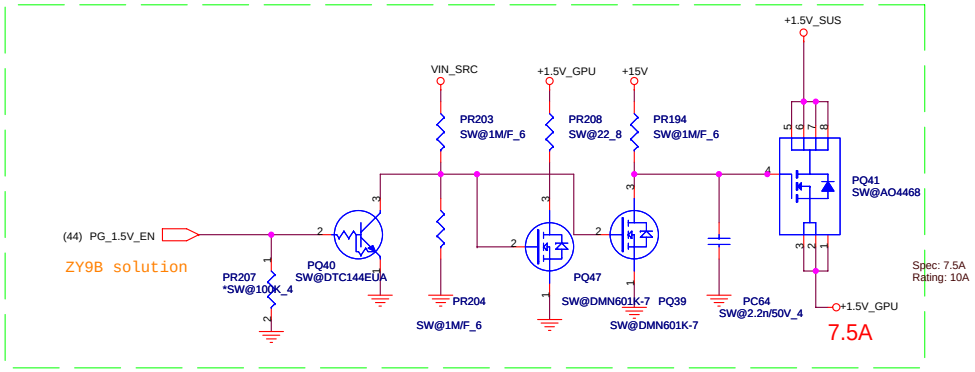
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

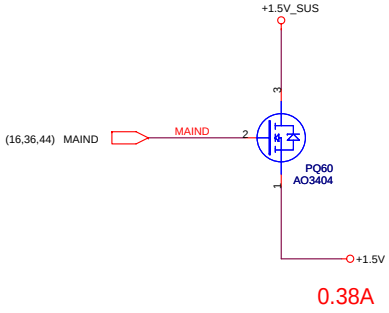
14.2m*10=RILIM*20uA

RILIM=7.1K--- 7.15K

Quanta Computer Inc.		
PROJECT : ZQ1		
Size	Document Number: VCCP 1.05V(UP6111A)	Rev: 1A
Date: Friday, January 22, 2010	Sheet 39 of 48	







Quanta Computer Inc.

PROJECT : ZQ1

Size	Document Number	Rev
	DDR III 1.5V(TPS51116)	1A

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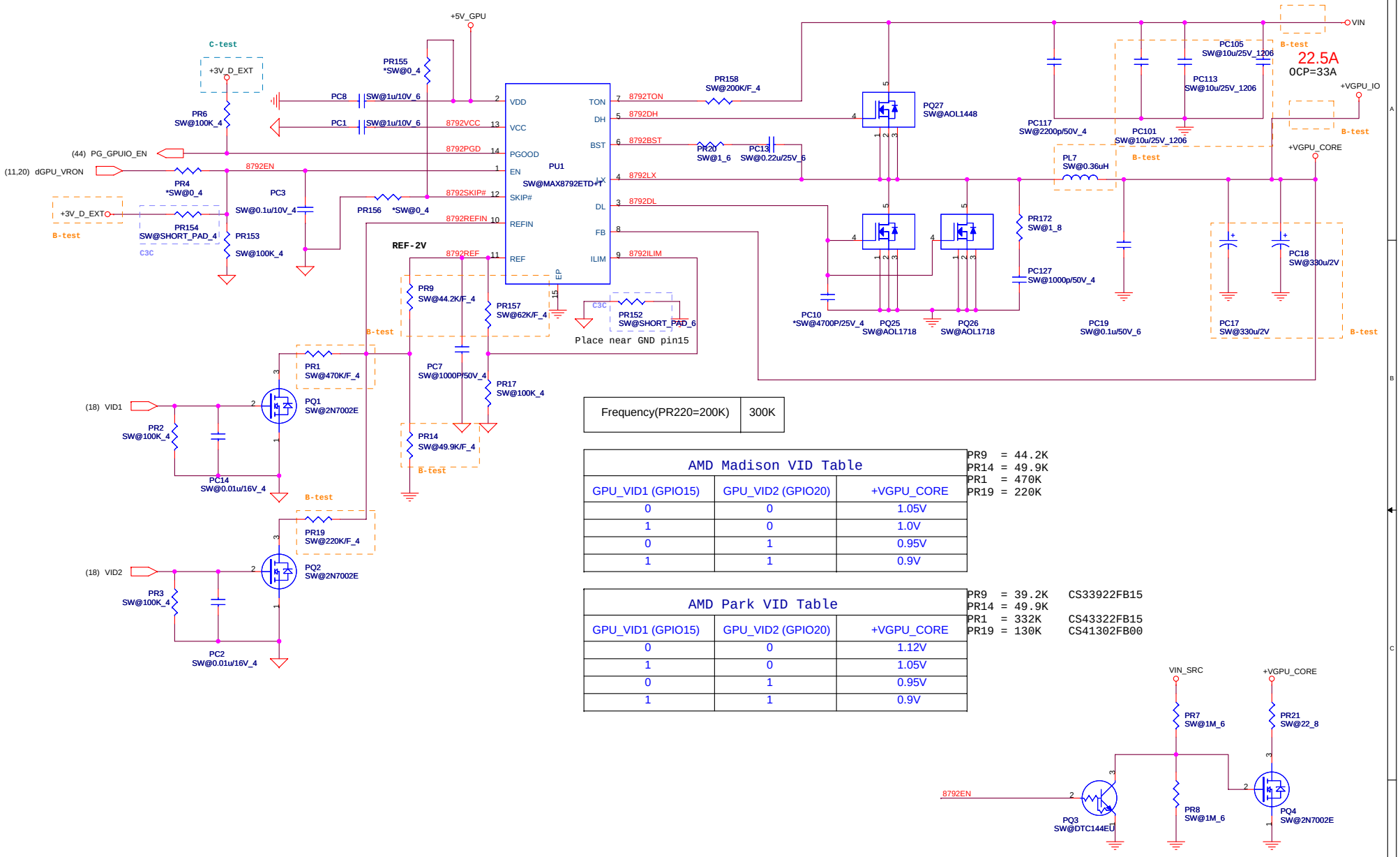

Frequency(PR220=200K)	300K

AMD Madison VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
1	1	0.9V

PR9 = 44.2K
PR14 = 49.9K
PR1 = 470K
PR19 = 220K

AMD Park VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

PR9 = 39.2K CS33922FB15
PR14 = 49.9K
PR1 = 332K CS43322FB15
PR19 = 130K CS41302FB00

Quanta Computer Inc.
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Size	Document Number	Rev
	GPU CORE(MAX8792)	1A

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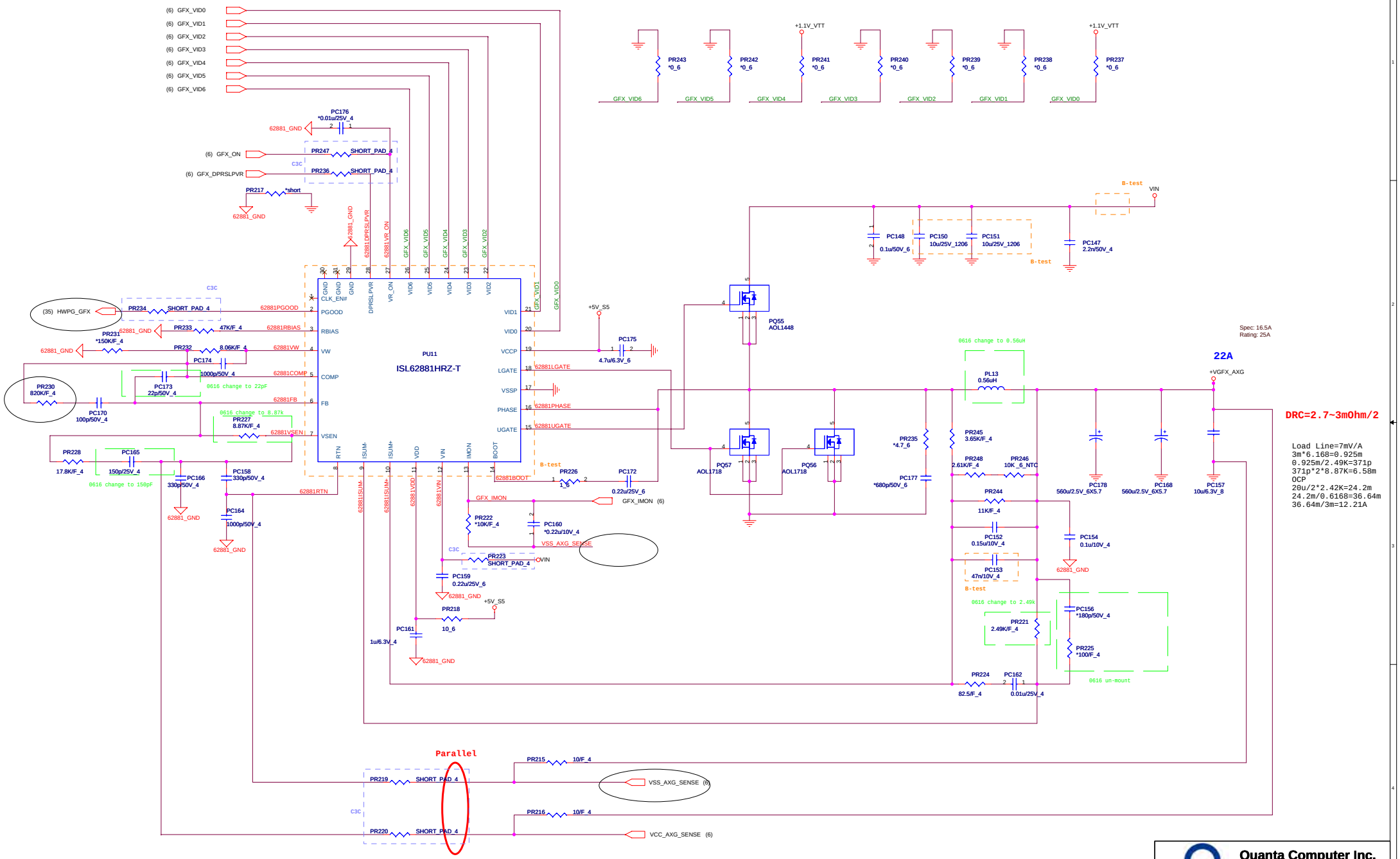
Int_VGA [PWM]



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

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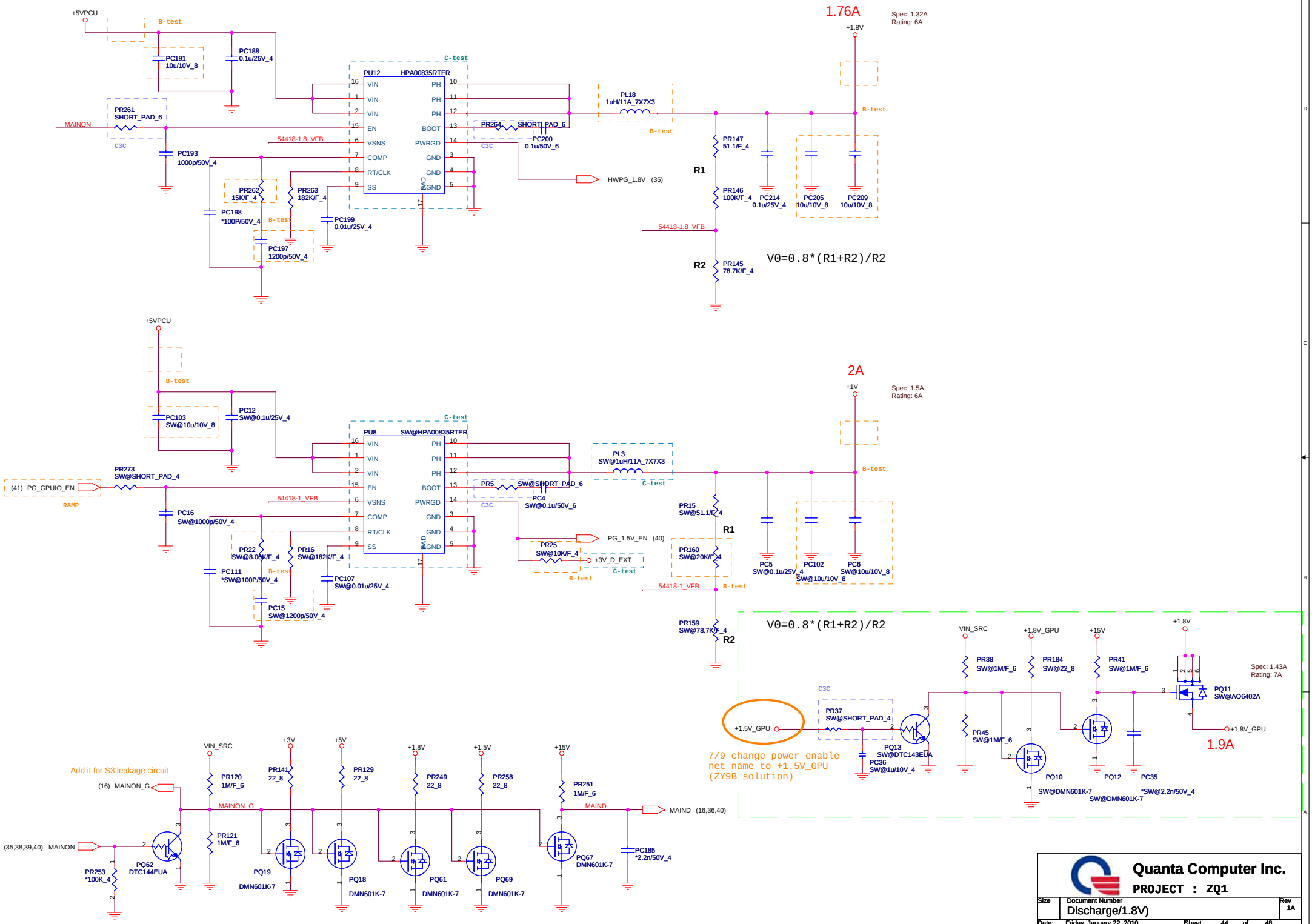
1.76A
Spec: 1.32A
Rating: 6A
+5VPCU
B-test
PC191 10u/10V_8
PC188 0.1u/25V_4
C-test
PU12 HPA00835RTER
VIN
PH
EN
BOOT
VSNS
PWRGD
COMP
GND
RT/CLK
SS
PAD
PR261 SHORT_PAD_6
MAINON
C3C
PC193 1000p/50V_4
54418-1.8_VFB
PR262 15K/F_4
PR263 182K/F_4
PC198 *100P/50V_4
PC197 1200p/50V_4
PC199 0.01u/25V_4
PR264 SHORT_PAD_6
PC200 0.1u/50V_6
PL18 1uH/11A_7X7X3
HWPG_1.8V (35)
+1.8V
R1
PR147 51.1/F_4
PR146 100K/F_4
PC214 0.1u/25V_4
PC205 10u/10V_8
PC209 10u/10V_8
R2
PR145 78.7K/F_4
V0=0.8*(R1+R2)/R2
2A
Spec: 1.5A
Rating: 6A
+1V
PC103 SW@10u/10V_8
PC12 SW@0.1u/25V_4
PU8 SW@HPA00835RTER
PR273 SW@SHORT_PAD_4
(41) PG_GPUIO_EN
RAMP
PC16 SW@1000p/50V_4
54418-1_VFB
PR22 SW@8.06K/F_4
PR16 SW@182K/F_4
PC111 *SW@100P/50V_4
PC15 SW@1200p/50V_4
PC107 SW@0.01u/25V_4
PR5 SW@SHORT_PAD_6
PC4 SW@0.1u/50V_6
PL3 SW@1uH/11A_7X7X3
PG_1.5V_EN (40)
PR25 SW@10K/F_4
+3V_D_EXT
PR15 SW@51.1/F_4
PR160 SW@20K/F_4
PR159 SW@78.7K/F_4
PC5 SW@0.1u/25V_4
PC102 SW@10u/10V_8
PC6 SW@10u/10V_8
V0=0.8*(R1+R2)/R2
VIN_SRC
+1.8V_GPU
+15V
PR38 SW@1M/F_6
PR184 SW@22_8
PR41 SW@1M/F_6
PR37 SW@SHORT_PAD_4
+1.5V_GPU
PR45 SW@1M/F_6
PQ13 SW@DTC143EUA
PC36 SW@1u/10V_4
PQ10 SW@DMN601K-7
PQ12 SW@DMN601K-7
PC35 *SW@2.2n/50V_4
PQ11 SW@AO6402A
Spec: 1.43A
Rating: 7A
1.9A
7/9 change power enable net name to +1.5V_GPU (ZY9B solution)
Add it for S3 leakage circuit
(16) MAINON_G
MAINON_G
(35,38,39,40) MAINON
PR120 1M/F_6
PR121 1M/F_6
PR253 *100K_4
PQ62 DTC144EUA
+3V
+5V
+1.8V
+1.5V
+15V
PR141 22_8
PR129 22_8
PR249 22_8
PR258 22_8
PR251 1M/F_6
MAIND
MAIND (16,36,40)
PQ19 DMN601K-7
PQ18 DMN601K-7
PQ61 DMN601K-7
PQ69 DMN601K-7
PQ67 DMN601K-7
PC185 *2.2n/50V_4
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Discharge/1.8V)
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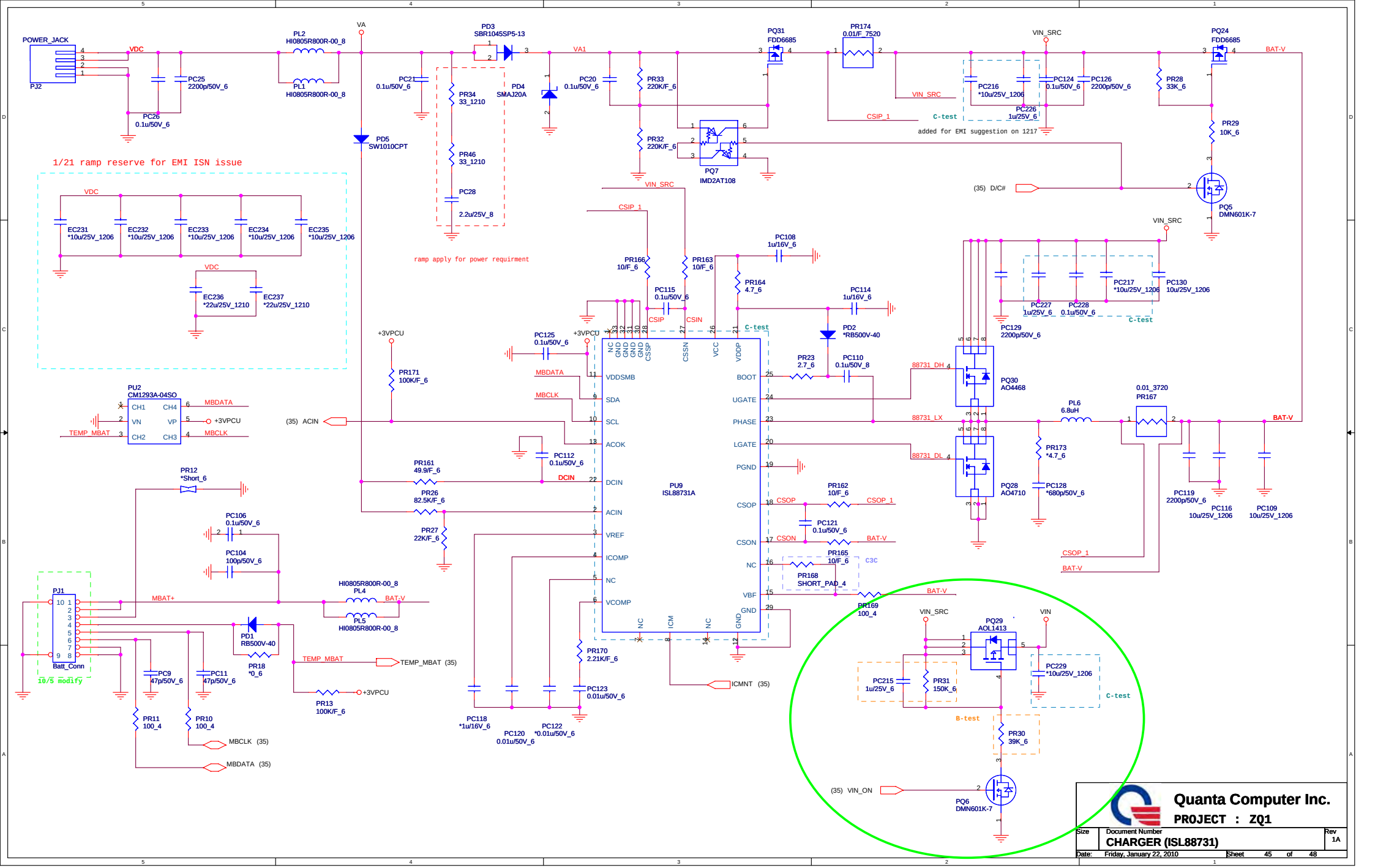
POWER_JACK
PJ2
VDC
PC25 2200p/50V_6
PC26 0.1u/50V_6
PL2 HI0805R800R-00_8
PL1 HI0805R800R-00_8
VA
PD3 SBR1045SP5-13
PC21 0.1u/50V_6
PR34 33_1210
PR46 33_1210
PC28 2.2u/25V_8
PD4 SMAJ20A
PD5 SW1010CPT
VA1
PC20 0.1u/50V_6
PR33 220K/F_6
PR32 220K/F_6
PQ31 FDD6685
PR174 0.01/F_7520
VIN_SRC
CSIP_1
C-test
PC216 *10u/25V_1206
PC226 1u/25V_6
PC124 0.1u/50V_6
PC126 2200p/50V_6
added for EMI suggestion on 1217
PQ7 IMD2AT108
PR28 33K_6
PQ24 FDD6685
BAT-V
PR29 10K_6
(35) D/C#
PQ5 DMN601K-7
1/21 ramp reserve for EMI ISN issue
EC231 *10u/25V_1206
EC232 *10u/25V_1206
EC233 *10u/25V_1206
EC234 *10u/25V_1206
EC235 *10u/25V_1206
EC236 *22u/25V_1210
EC237 *22u/25V_1210
ramp apply for power requirment
PR166 10/F_6
PR163 10/F_6
PC115 0.1u/50V_6
PR164 4.7_6
PC108 1u/16V_6
PC114 1u/16V_6
PD2 *RB500V-40
PC217 *10u/25V_1206
PC130 10u/25V_1206
PC227 1u/25V_6
PC228 0.1u/50V_6
PC129 2200p/50V_6
PU2 CM1293A-04SO
MBDATA
MBCLK
TEMP_MBAT
+3VPCU
(35) ACIN
PR171 100K/F_6
PC125 0.1u/50V_6
PR23 2.7_6
PC110 0.1u/50V_8
PQ30 AO4468
PQ28 AO4710
PL6 6.8uH
0.01_3720
PR167
PR173 *4.7_6
PC128 *680p/50V_6
PC119 2200p/50V_6
PC116 10u/25V_1206
PC109 10u/25V_1206
88731_DH
88731_LX
88731_DL
PU9 ISL88731A
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
VBF
GND
CSSP
CSSN
VCC
VDDP
PC112 0.1u/50V_6
PR161 49.9/F_6
PR26 82.5K/F_6
PR27 22K/F_6
PR12 *Short_6
PC106 0.1u/50V_6
PC104 100p/50V_6
PR162 10/F_6
PC121 0.1u/50V_6
PR165 10/F_6
PR168 SHORT_PAD_4
PR169 100_4
PR170 2.21K/F_6
PC123 0.01u/50V_6
PC118 *1u/16V_6
PC120 0.01u/50V_6
PC122 *0.01u/50V_6
ICMNT (35)
PJ1
Batt_Conn
10/5 modify
MBAT+
HI0805R800R-00_8
PL4
PL5
PD1 RB500V-40
PR18 *0_6
PC9 47p/50V_6
PC11 47p/50V_6
PR11 100_4
PR10 100_4
PR13 100K/F_6
TEMP_MBAT (35)
MBCLK (35)
MBDATA (35)
PQ29 AOL1413
PC215 1u/25V_6
PR31 150K_6
PC229 *10u/25V_1206
B-test
PR30 39K_6
(35) VIN_ON
PQ6 DMN601K-7
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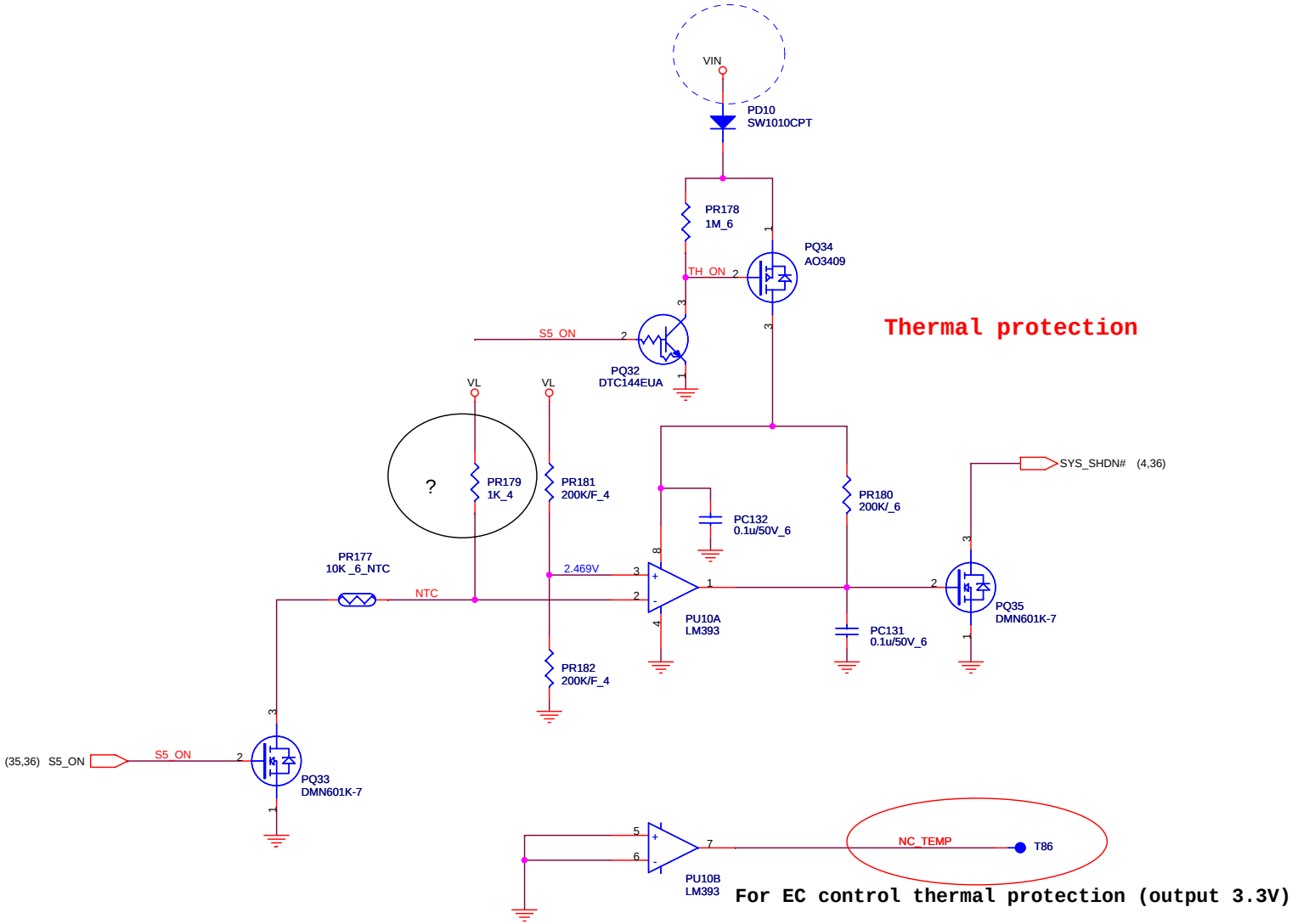

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