

Compal Confidential

Model Name : Bellemere_BE
Compal Project Name : B5W1E
File Name : LA-D121P

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B5W1E Schematics Document

AMD "Beema" Platform

AMD 15W APU With Puma+ Core

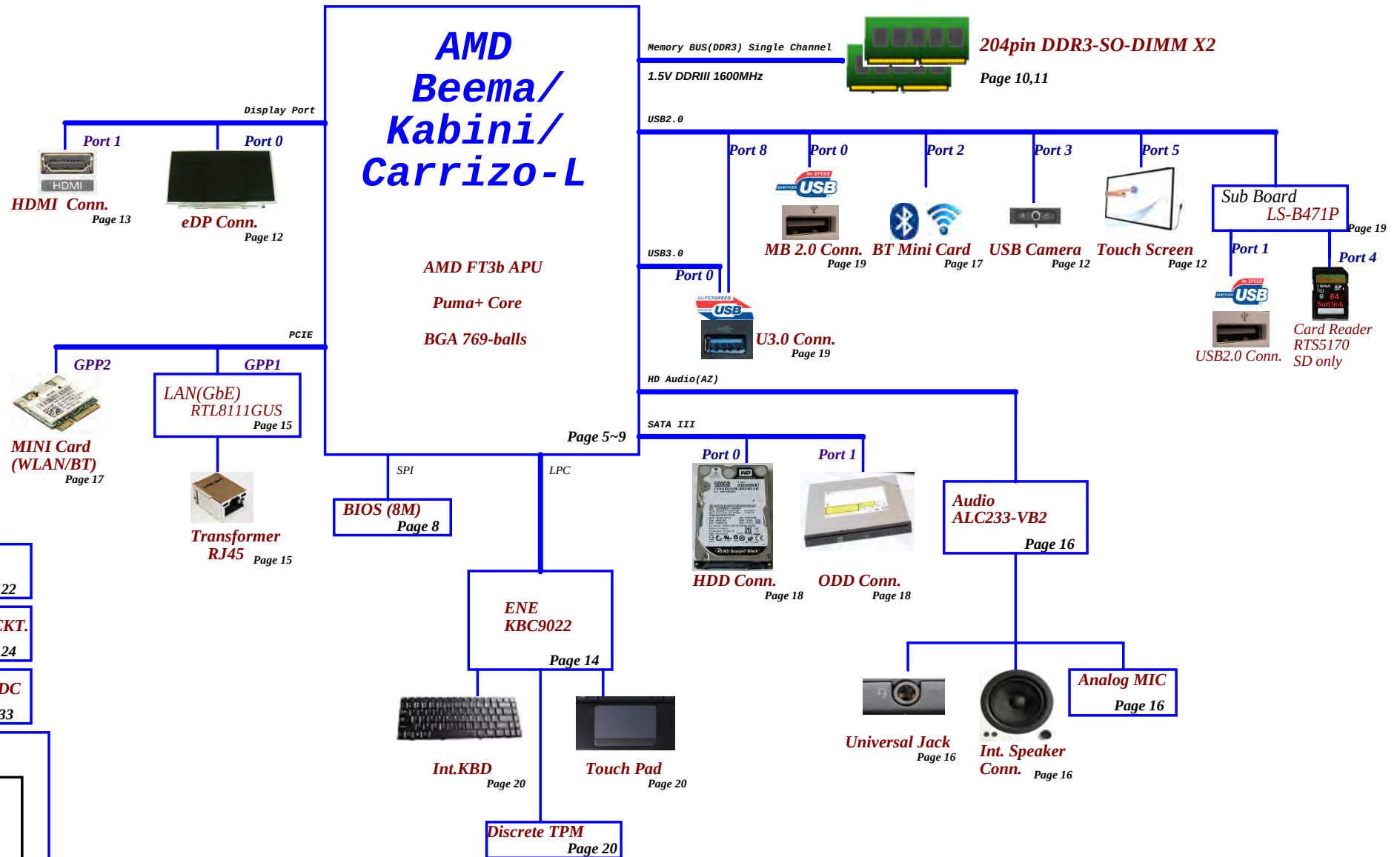
LA-D121P REV: 1.0

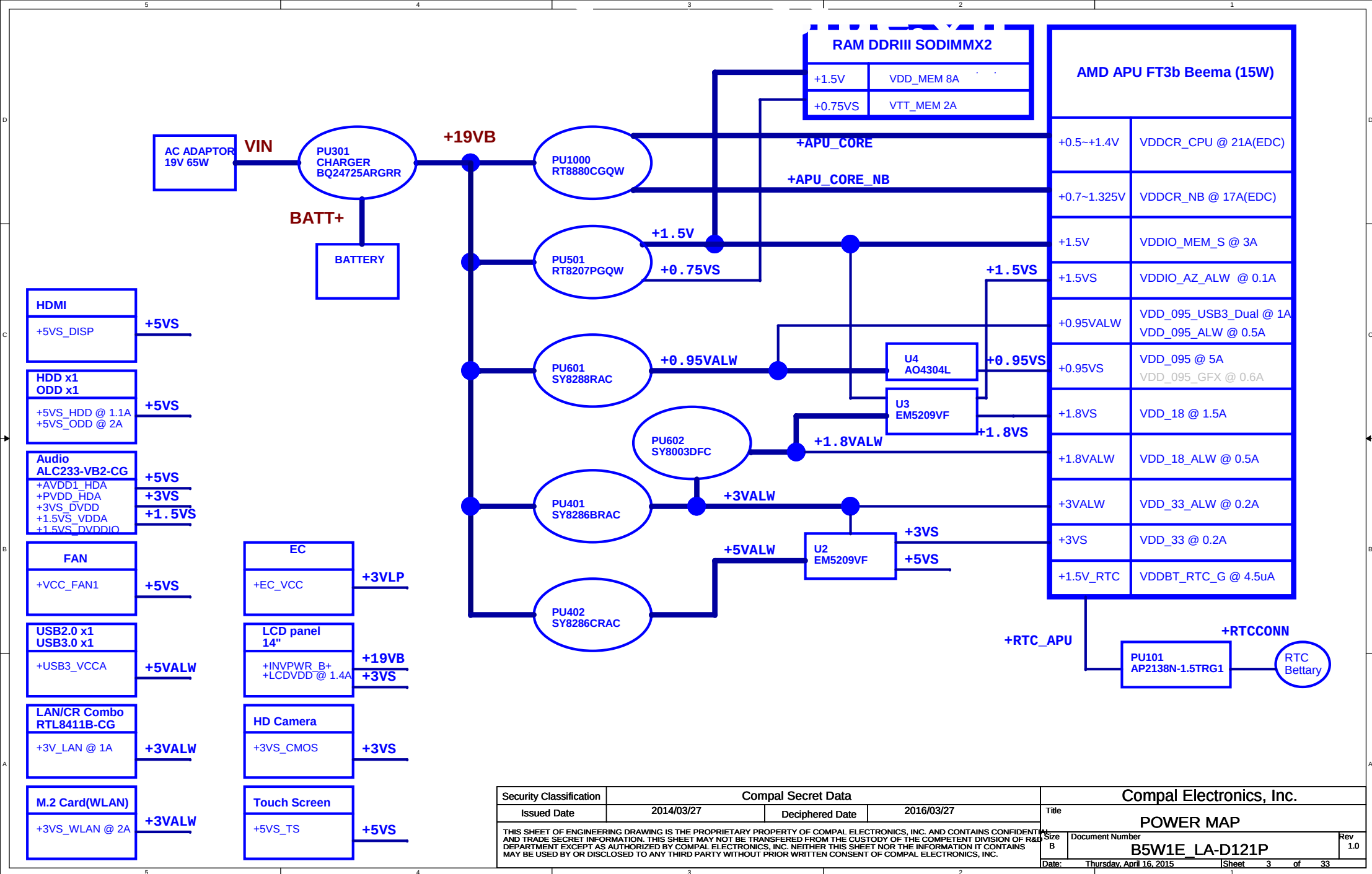
2015-04-16

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Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title	COVER PAGE	
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				Date	Tuesday, April 21, 2015	Sheet 1 of 33

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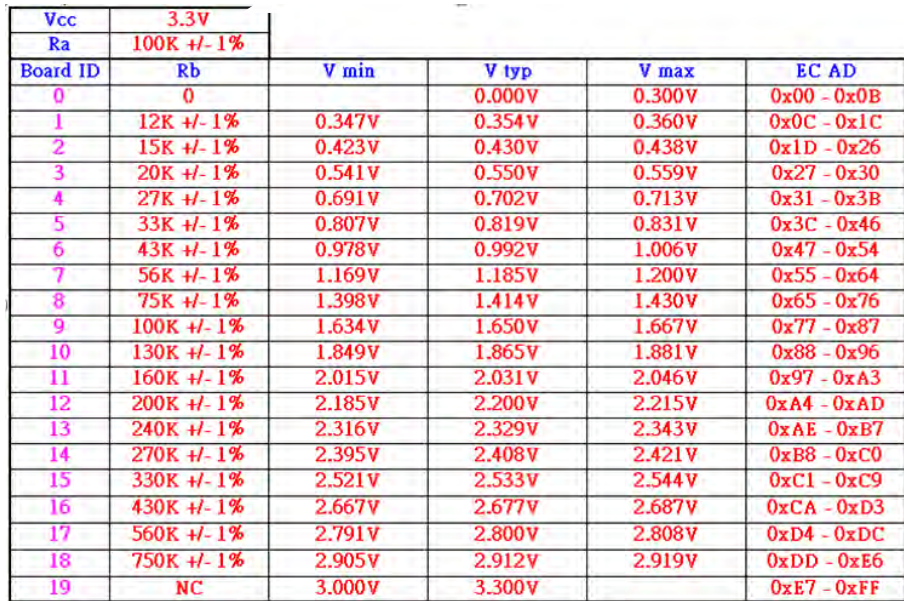
Model Name : B5W1E
B5W1K
B5W1R





[illegible]

EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H



BOM Structure	BTO Item
@	Unpop
CONN@	Connector part control by ME
KBN@	Stuff when use Kabini APU
BMA@	Stuff when use Beema APU
CZL@	Stuff when use CZ-L APU
233@	Use for Audio Codec ALC233-VB2
255@	Use for Audio Codec ALC255
283@	Use for Audio Codec ALC283
EMC@	EMI pop component
@EMC@	EMI unpop component
SP@	Short pad for clear CMOS
HDT@	HDT+ for test phase, MP remove
RS@	R-short
45@	HDMI royalty
9012@	Use KBC9012
9022@	Use KBC9022
BL@	Keyboard backlight
TPM@	Use discrete TPM module
ECI2C@	Use EC I2C T/P
TPUSB@	Use USB to I2C IC for T/P
BYOC@	Stuff when support BYOC
NBYOC@	Stuff when non-support BYOC
JP@	Jump
TP@	Test point

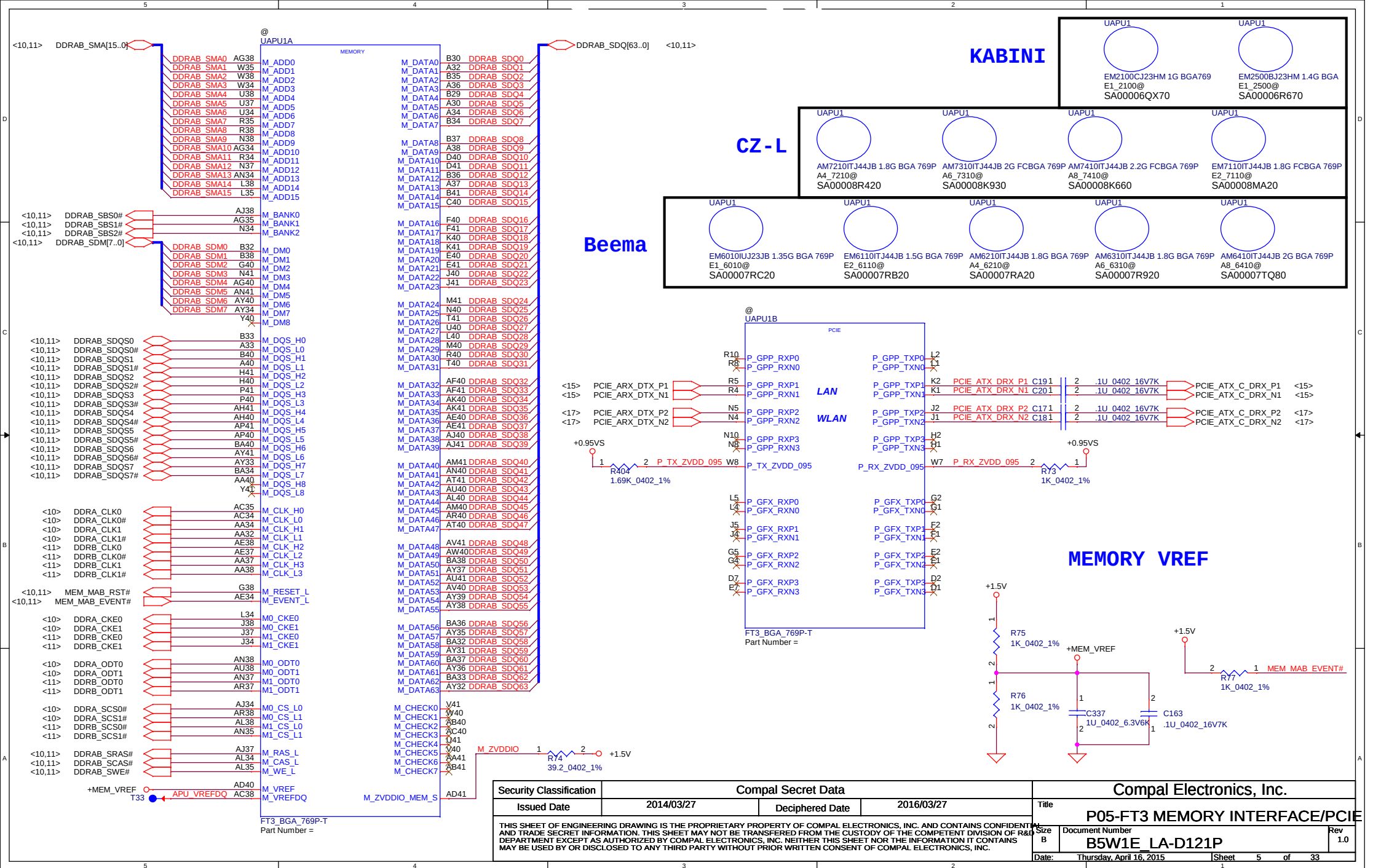
Board ID	PCB Revision
12	EVT
13	DVT
14*	PVT
15	Pre-MP
16	
17	
18	
19	

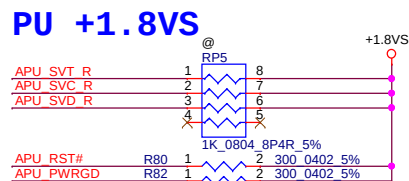
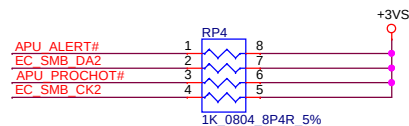
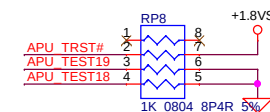
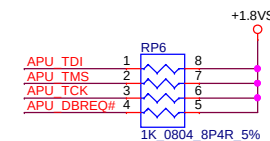
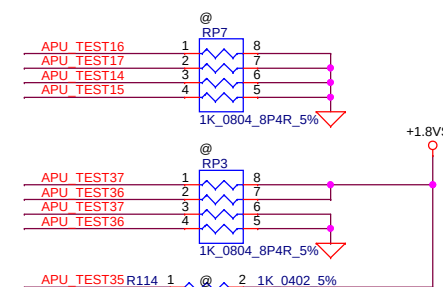
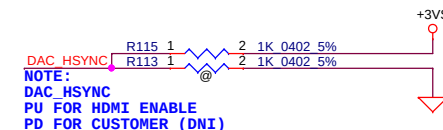
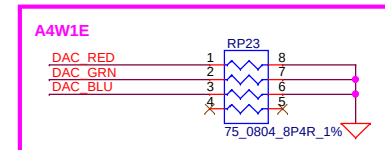
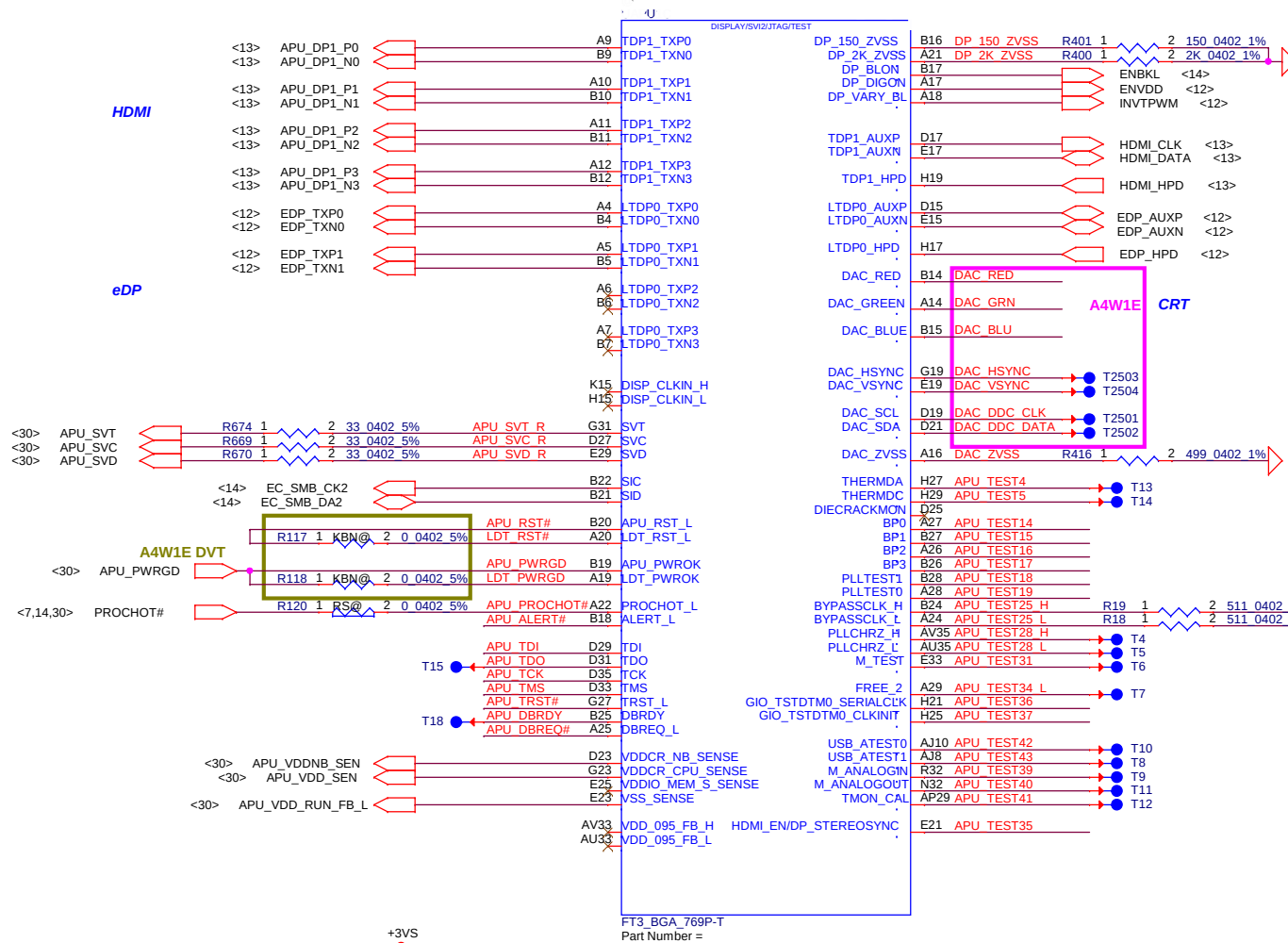
SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

The diagram shows the timing of five groups of signals (G-A to G-E) relative to a common clock. Each group is represented by a vertical line on the left, with individual signal names listed to its right. The signals are:

- G-A:** +RTC, EC_ON
- G-B:** +3VALW/+5VALW, +1.8VALW, +0.95VALW
- G-C:** SYSON, +1.5V, SUSP#
- G-D:** +3VS, +1.8VS, +1.5VS, +0.95VS
- G-E:** VR_ON, +APU_CORE, +APU_CORE_NB

The timing shows that the signals are grouped into five distinct time intervals, each corresponding to one of the G-A through G-E labels. The signals within each group are active during the same time interval, with some signals (like EC_ON, SYSON, and VR_ON) showing a single pulse, while others (like the VALW and VS signals) show a sustained high level.

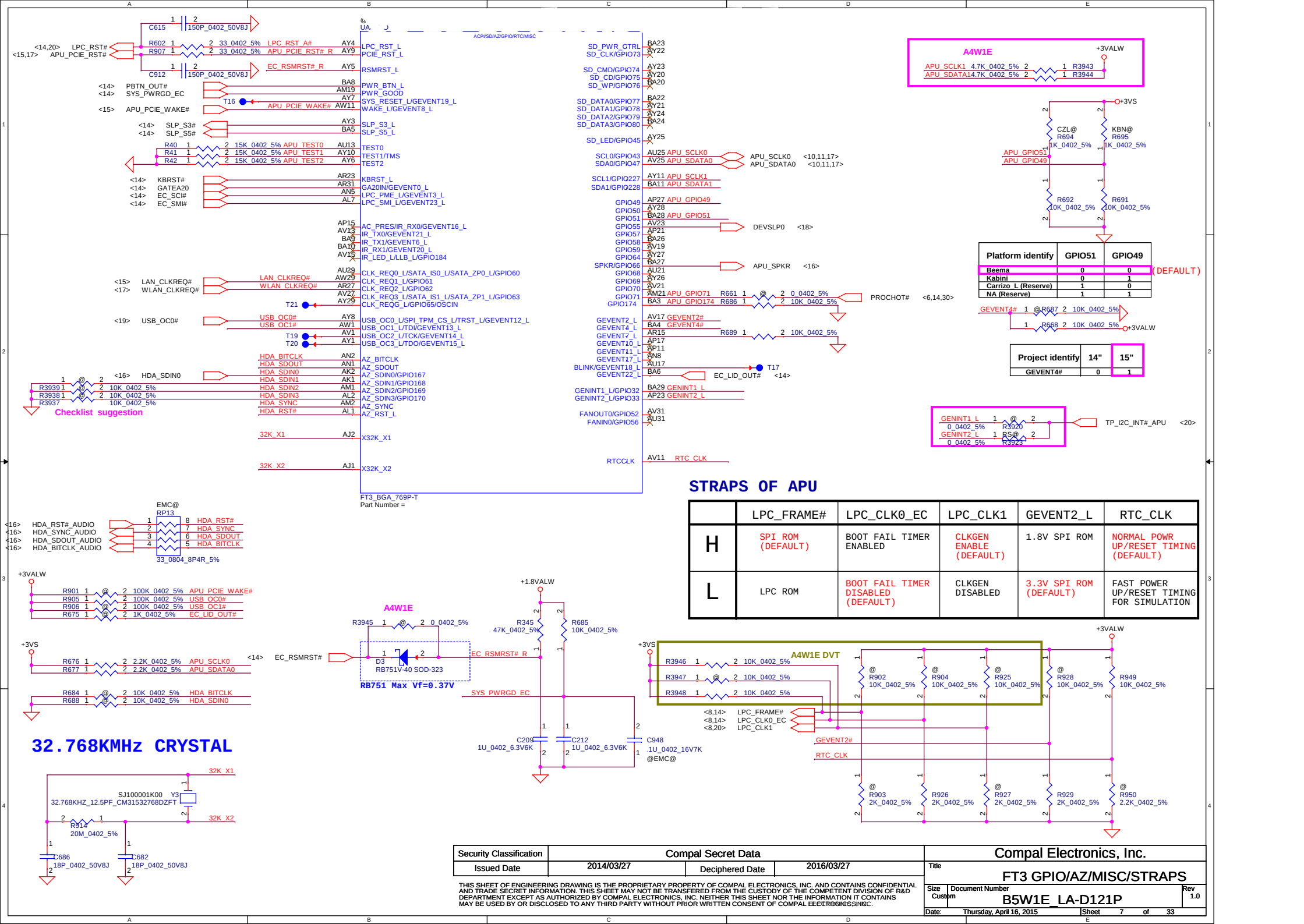


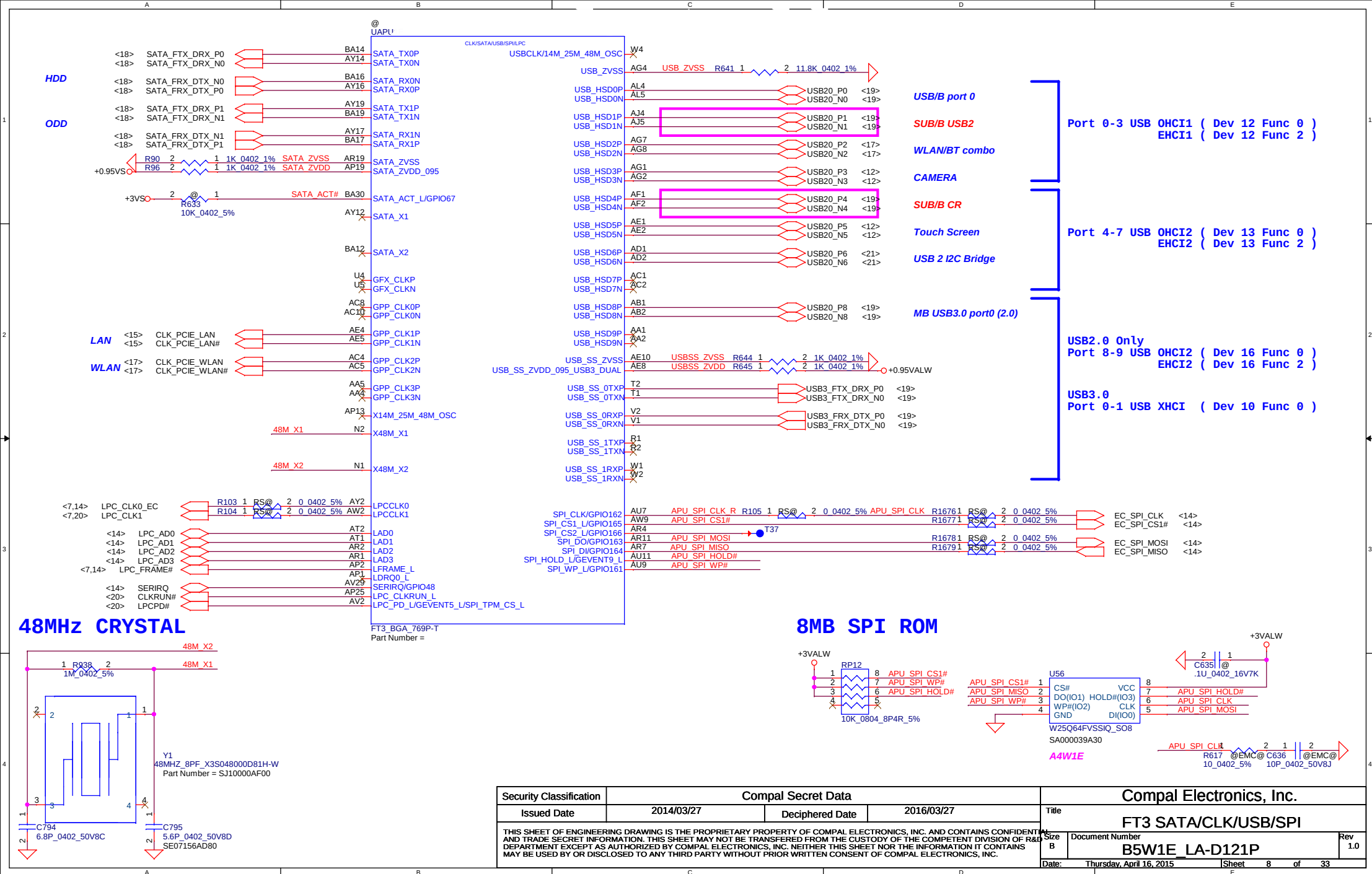


Close To PU1000

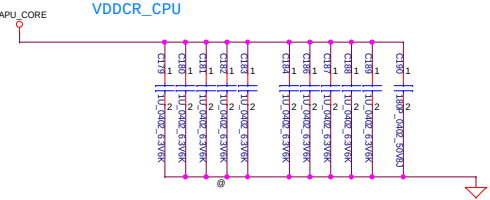
Close To APU's Pin

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				B5W1E_LA-D121P	
				Date: Thursday, April 16, 2015	Sheet 6 of 33

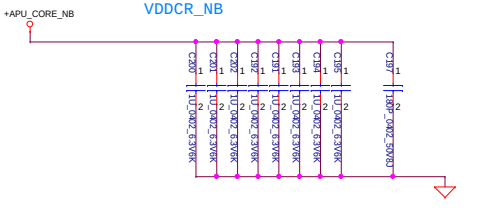




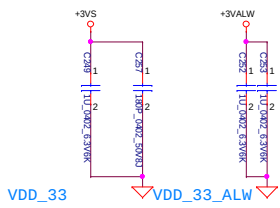
CORE POWER OF APU



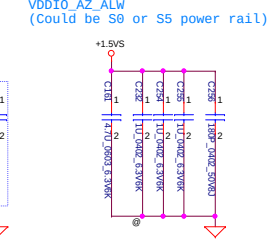
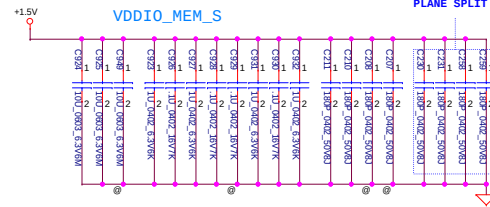
INTEGRATED GPU POWER OF APU



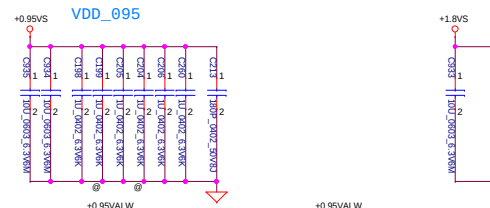
+3VALW/+3VS OF APU



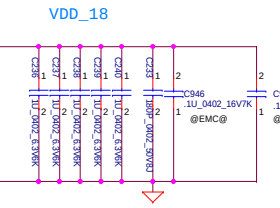
+1.5V/+1.5VS OF APU



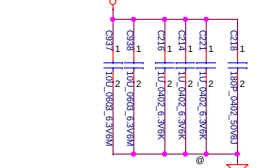
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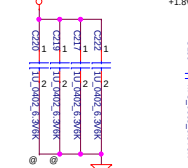
+1.8VALW/+1.8VS OF APU



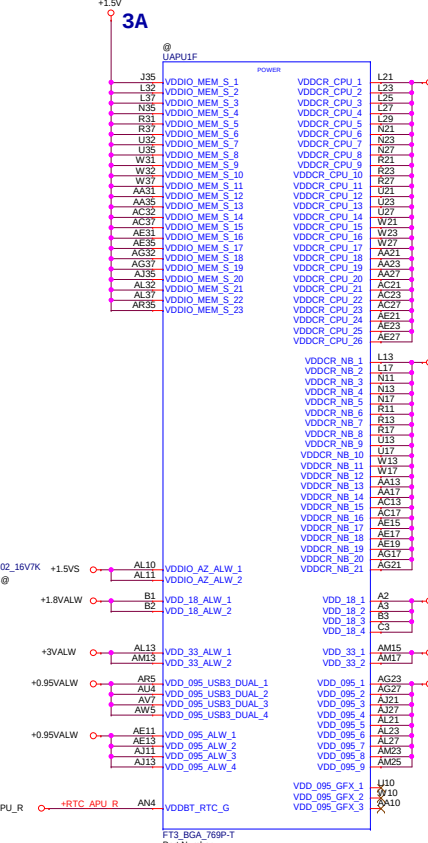
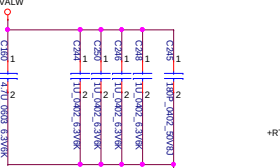
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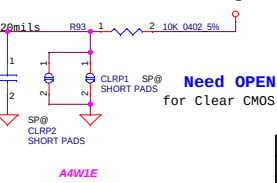
VDD_095_ALW



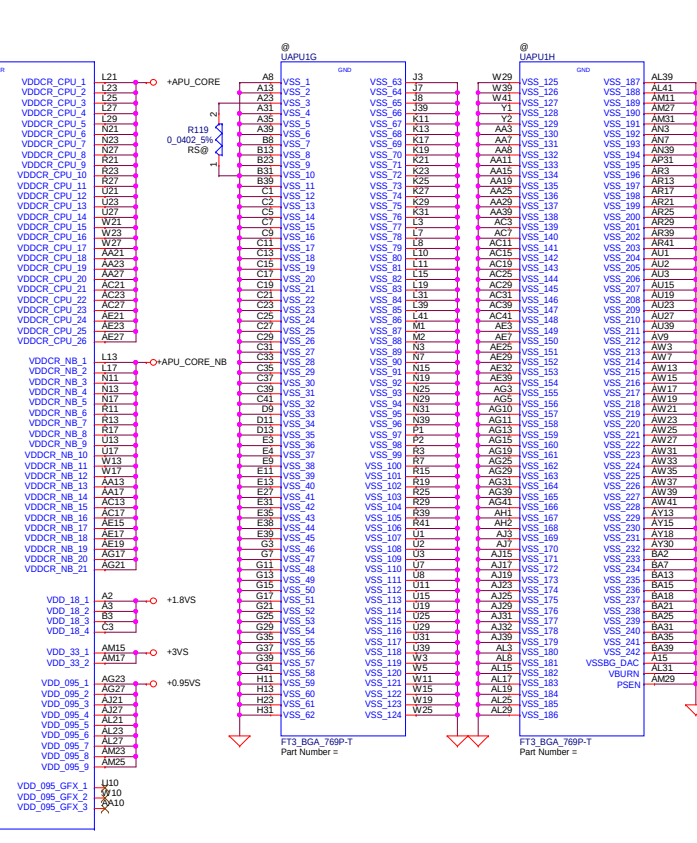
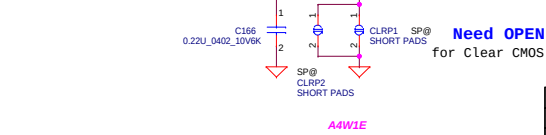
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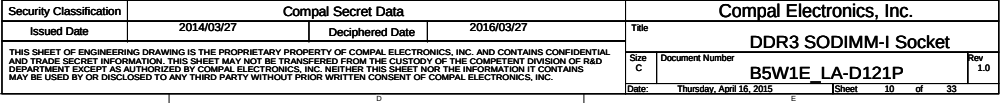


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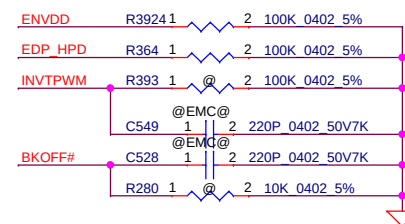
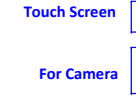
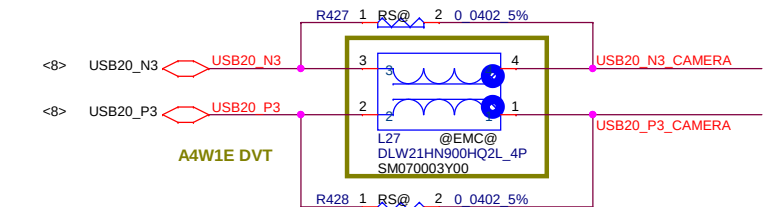
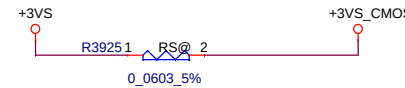
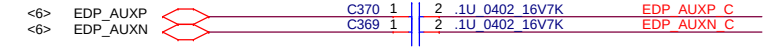
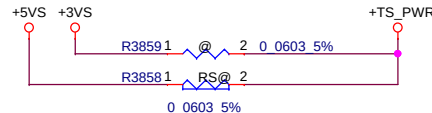
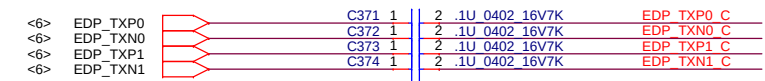
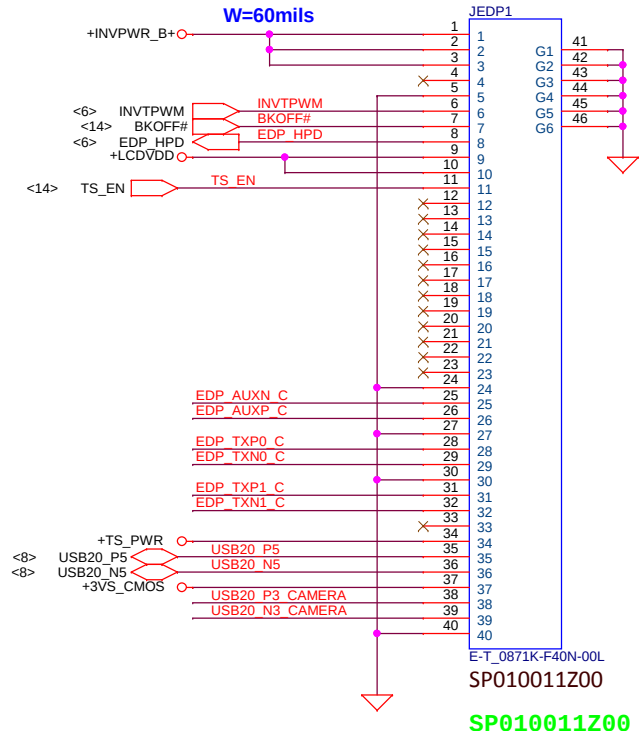
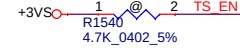
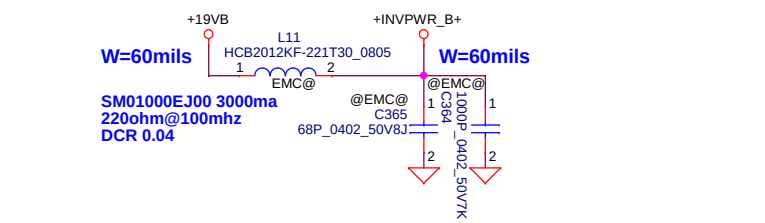


RTC OF APU

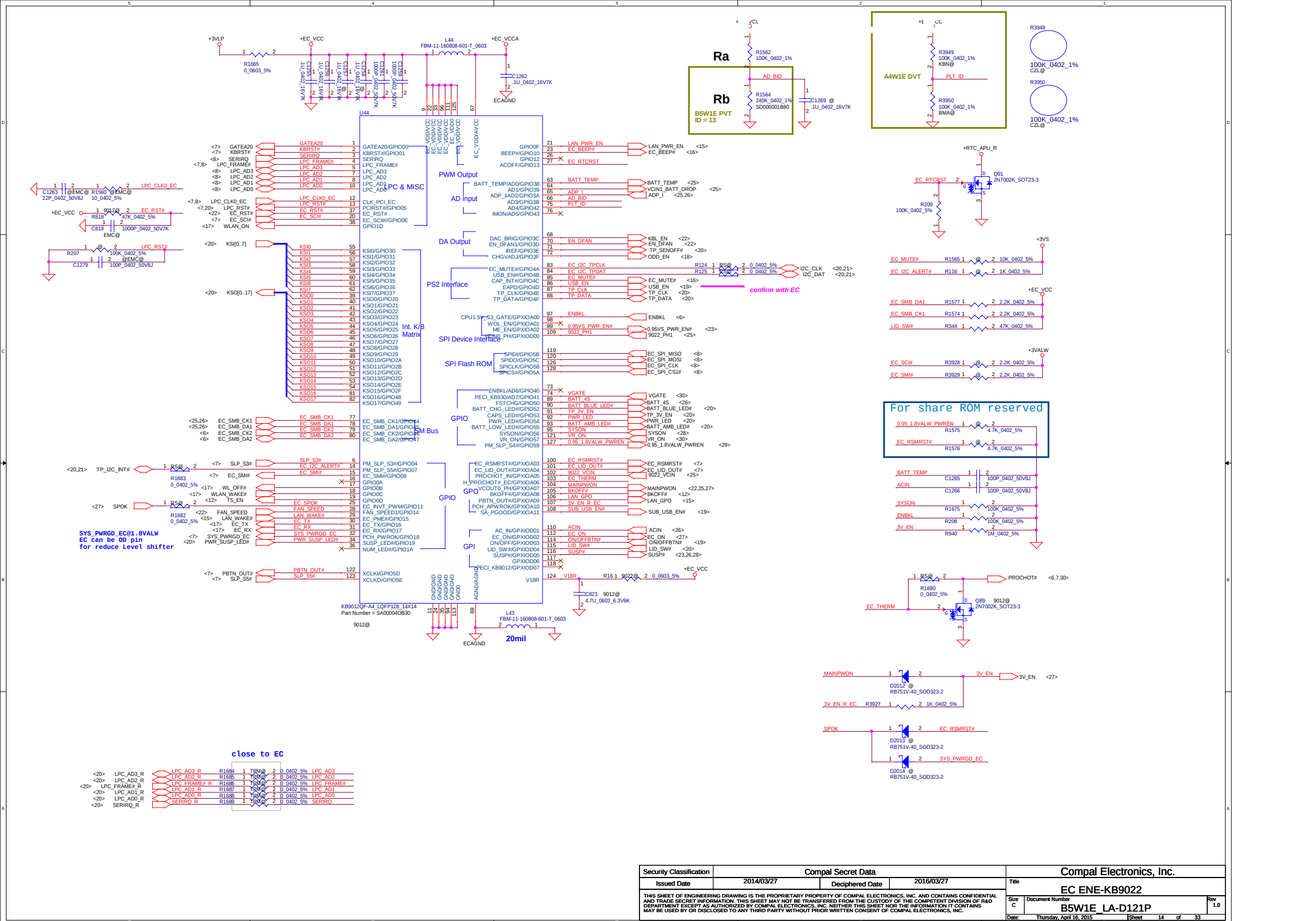


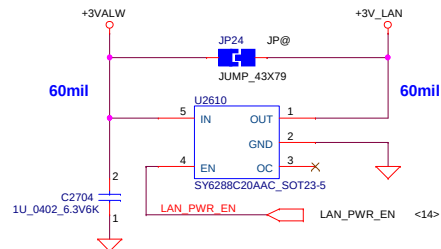


3/13 Change Pin define to follow Z5W1M

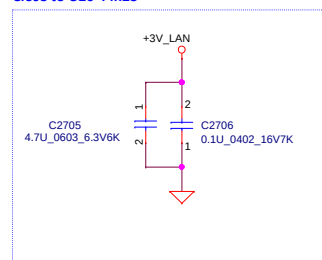


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				Custom	1.0		
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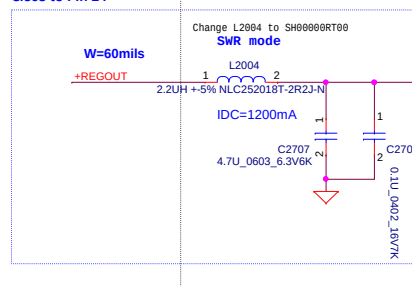




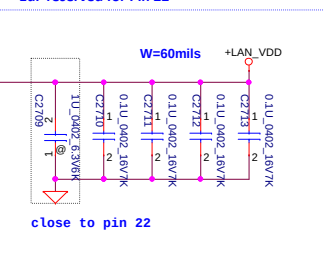
Close to U20 Pin23



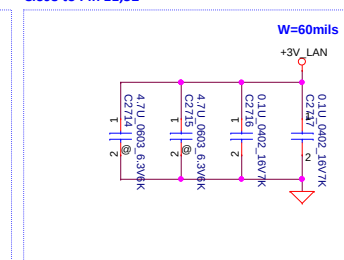
(Should be place within 200 mils)
Close to Pin 24



Close to Pin 3,8,22,30
1uF reserved for Pin 22

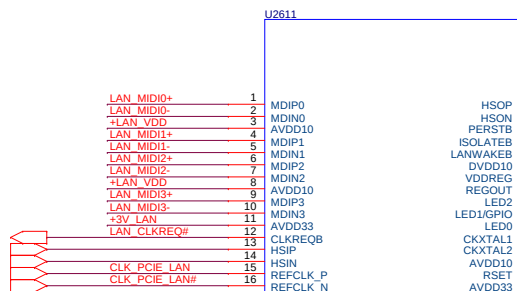


Close to Pin 11,32



PU to +3VS at PCH side

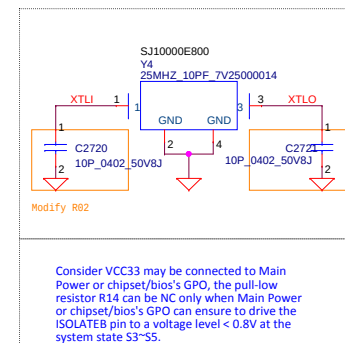
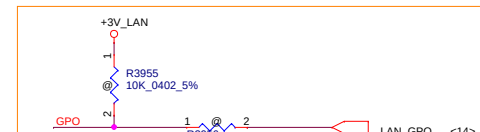
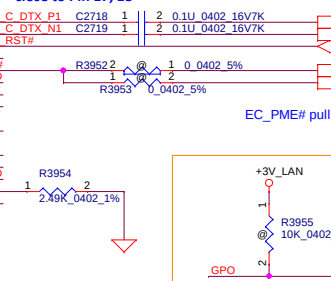
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<5> PCIE_ATX_C_DRX_N1
<8> CLK_PCIE_LAN
<8> CLK_PCIE_LAN#



RTL8111GS-CG_QFN32_4X4
SA00006ML00

Use 8111GS symbol , pop 8111GUS part

close to Pin 17, 18

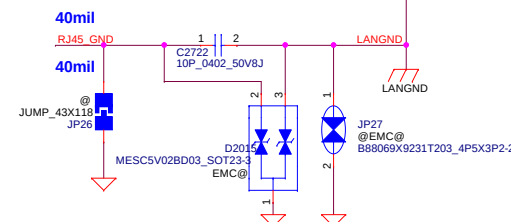
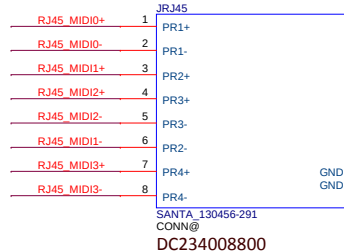


Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S3~S5.

Place close to TCT pin



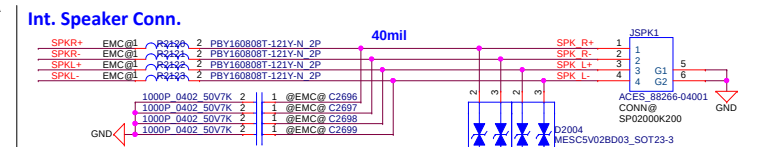
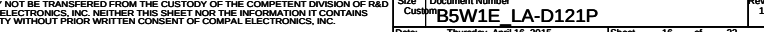
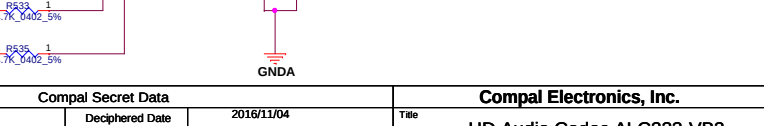
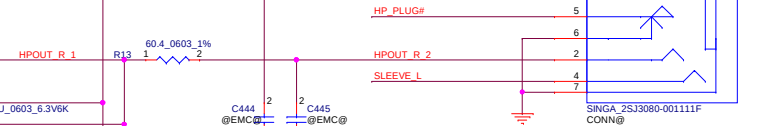
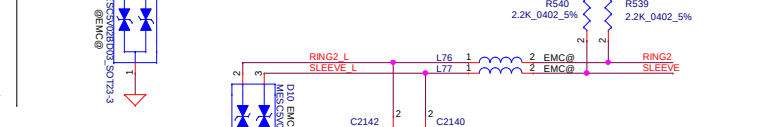
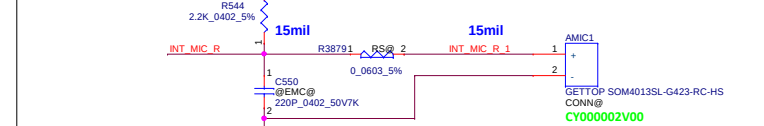
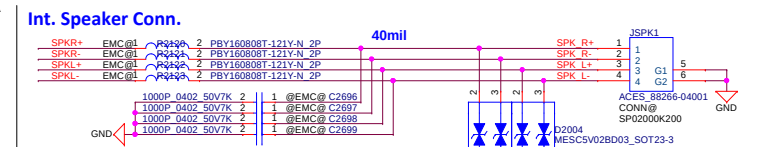
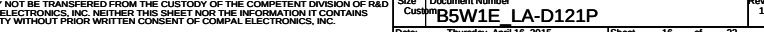
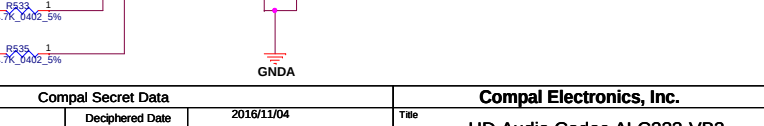
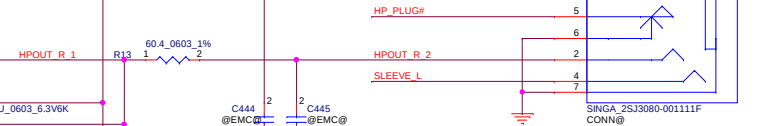
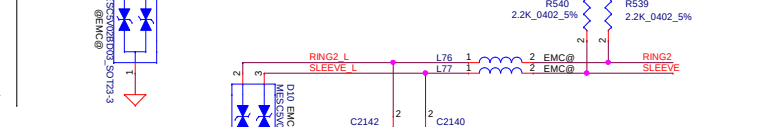
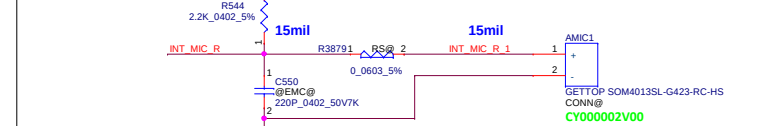
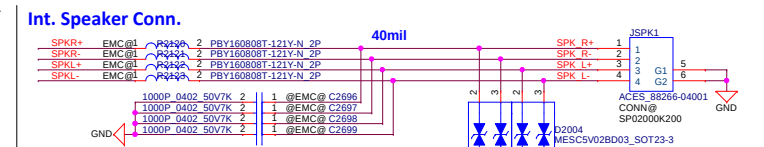
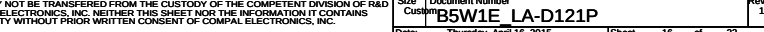
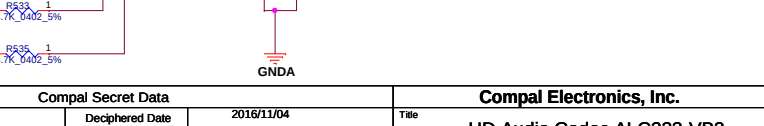
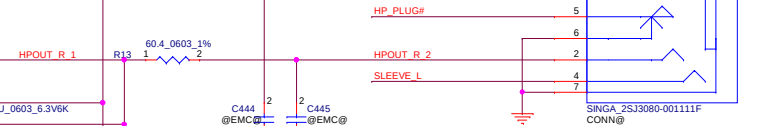
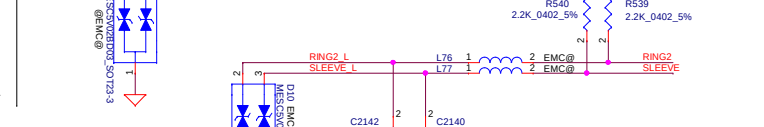
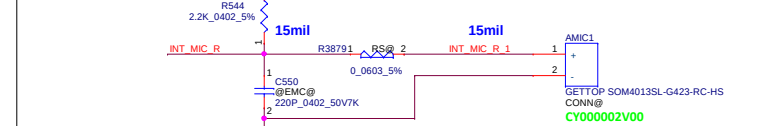
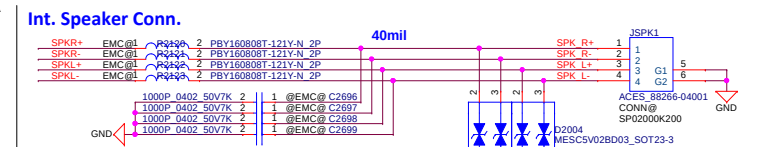
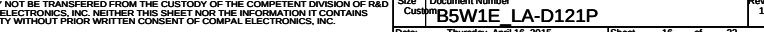
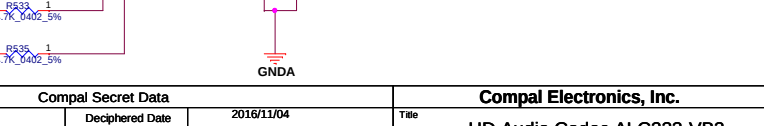
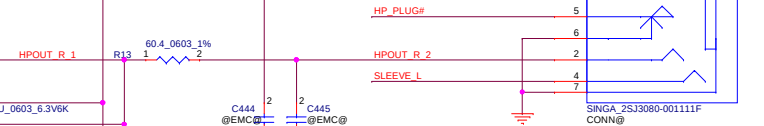
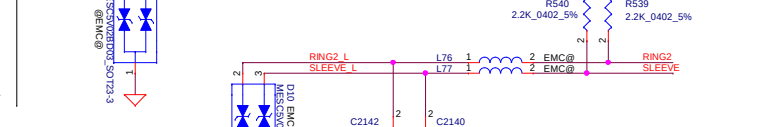
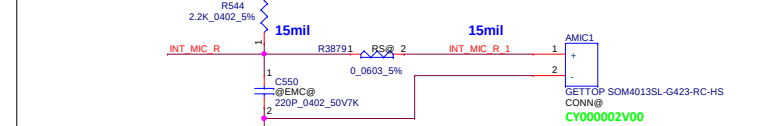
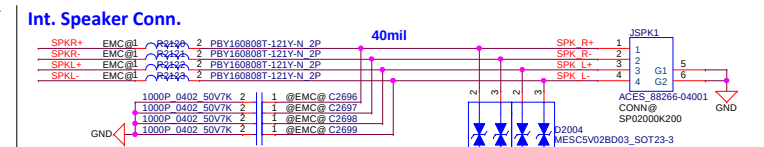
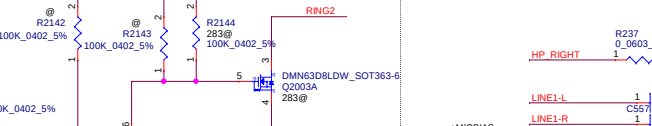
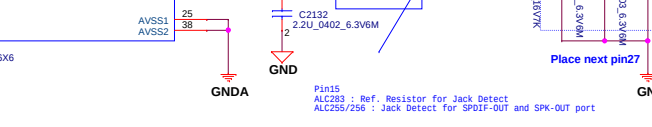
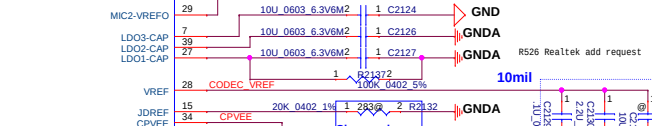
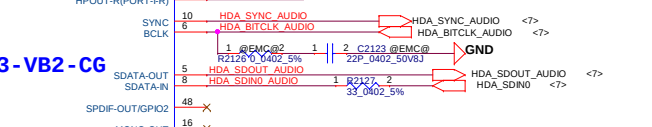
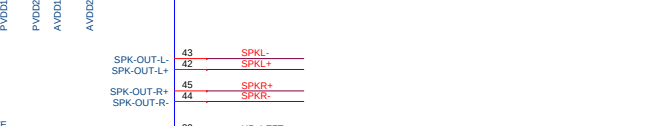
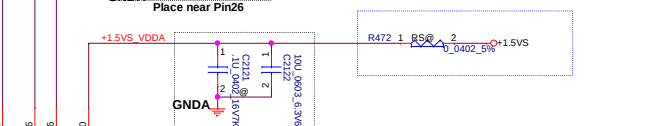
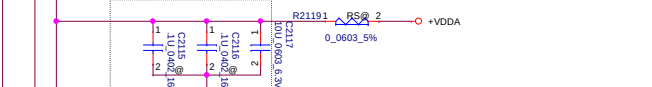
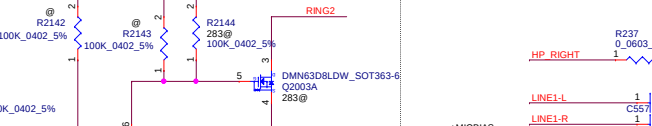
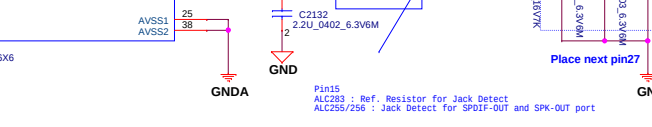
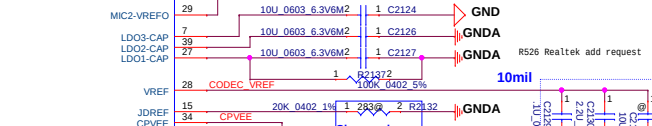
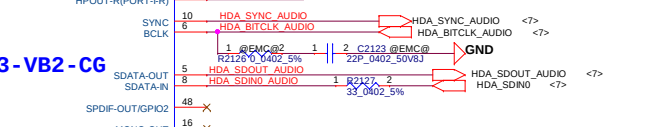
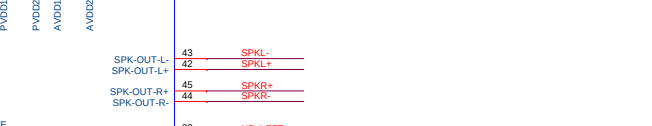
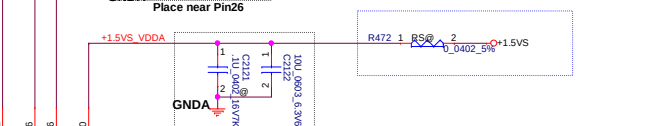
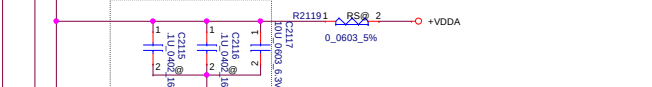
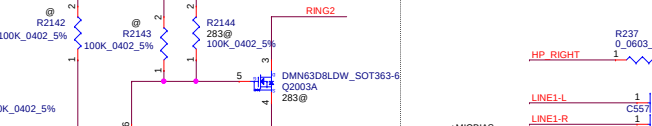
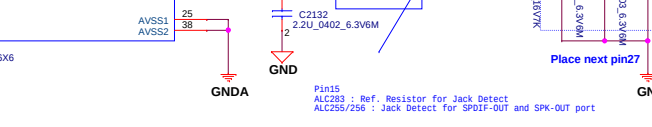
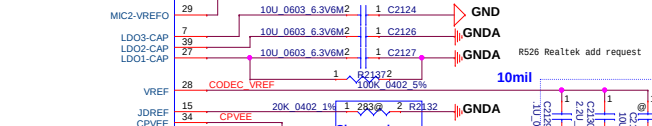
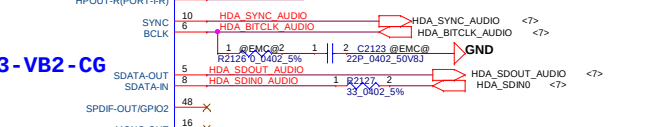
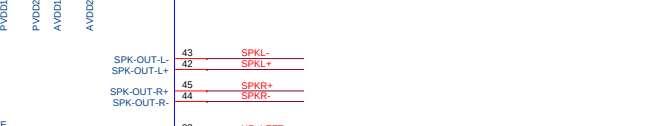
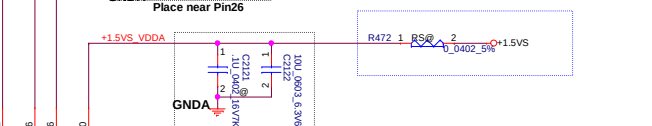
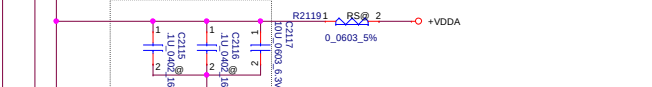
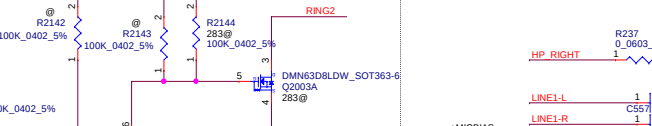
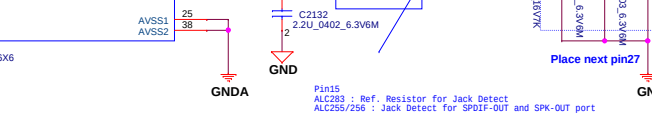
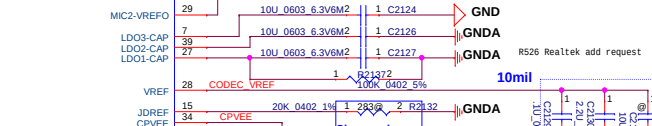
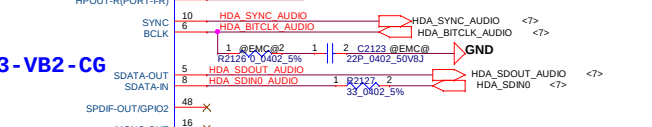
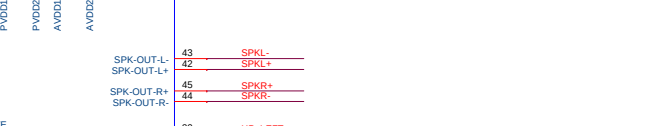
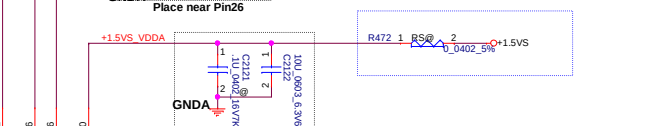
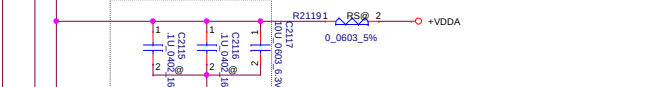
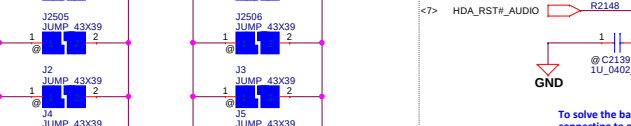
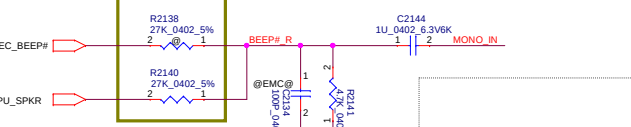
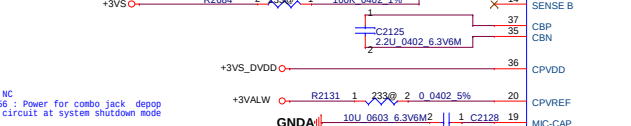
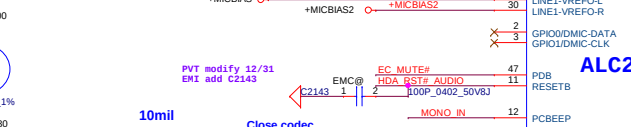
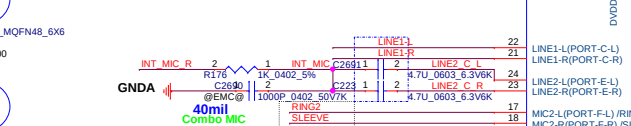
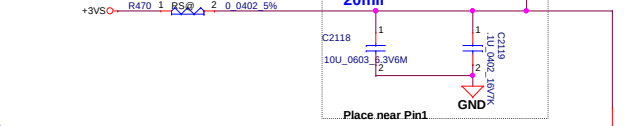
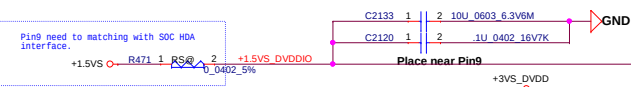
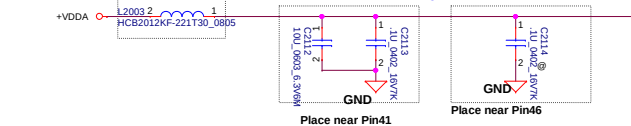
LAN Connector



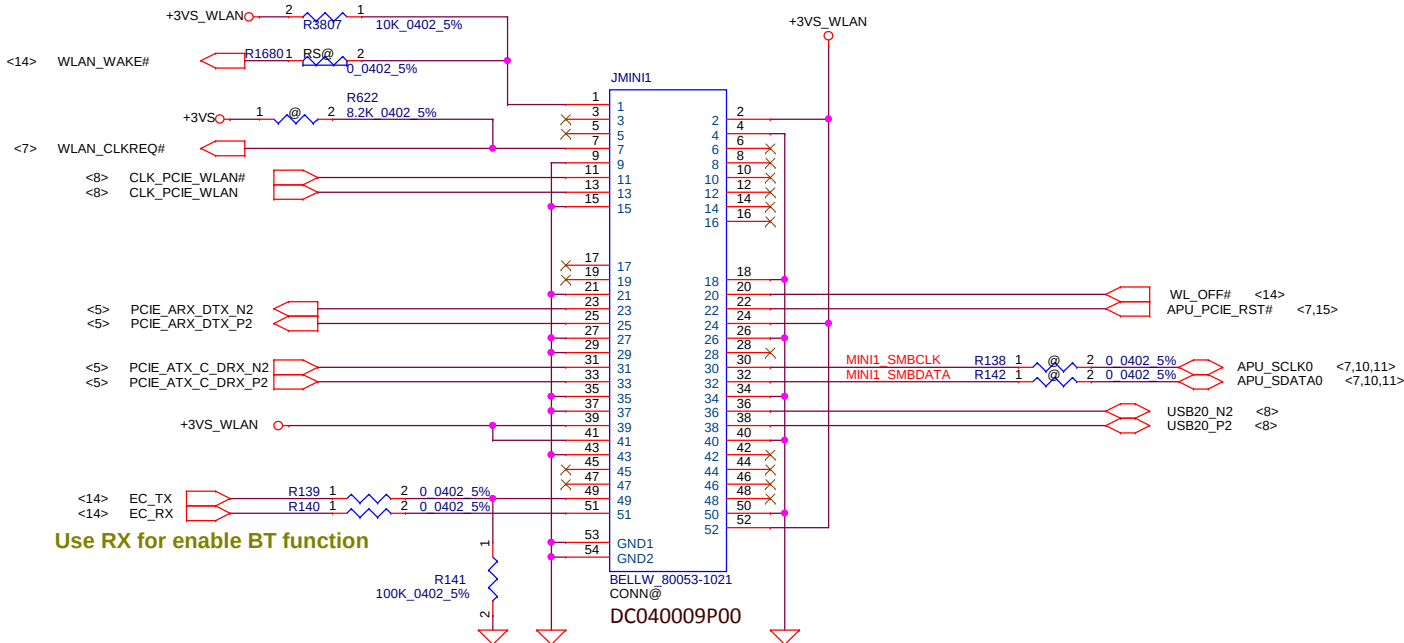
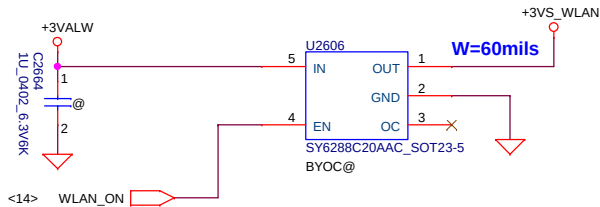
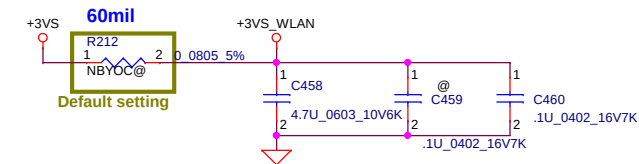
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SANTA 130456-291 CONN@ DC234008800				1.0
MESC5V02B8D03_SOT23-3 EMC@				Rev
JP27 @EMC@ B88069X9231T203_4P5X3P2-2				1.0
Date: Thursday, April 16, 2015				Sheet 15 of 33

HD Audio Codec

SM01000EJ00 3000ma 220ohm@100mhz DCR 0.04

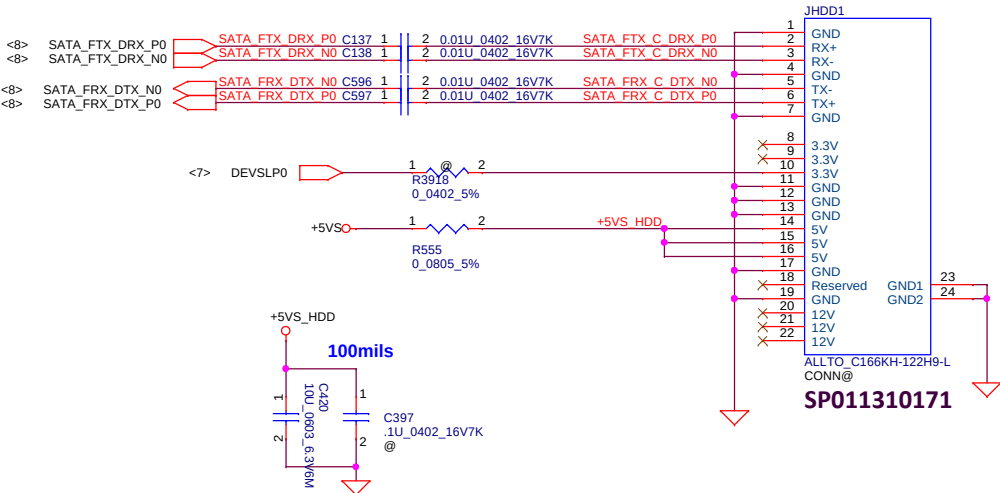


Wireless LAN

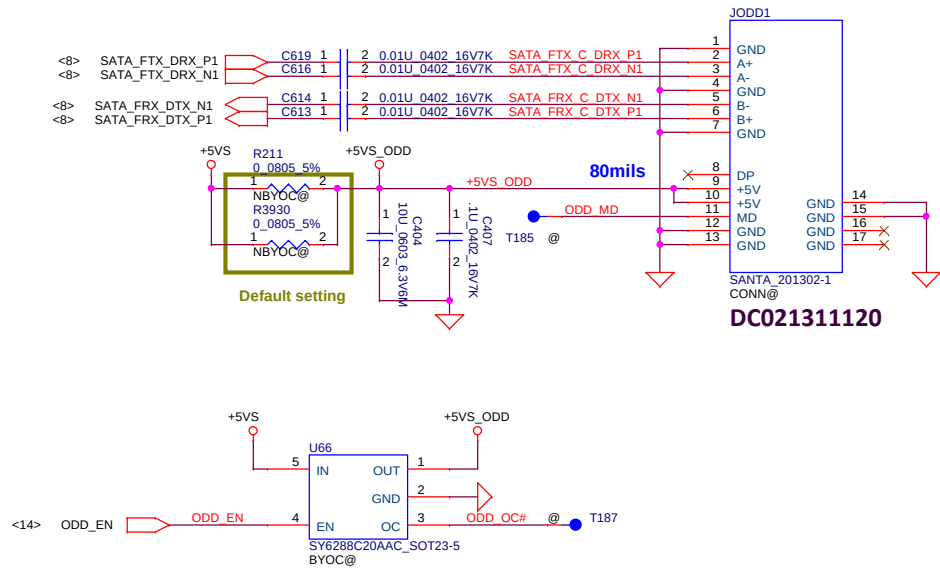


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SATA HDD Conn.

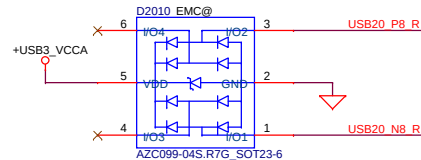
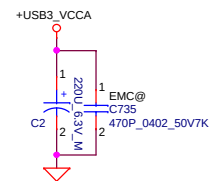
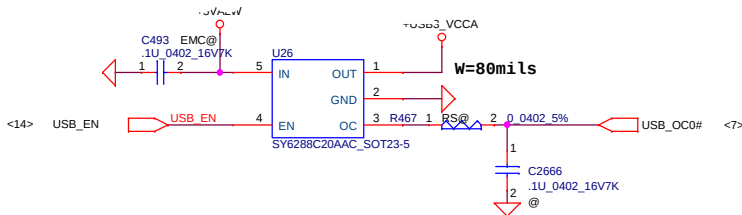
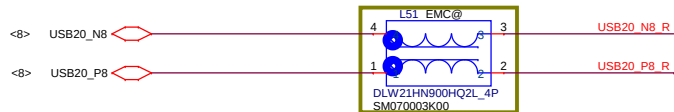


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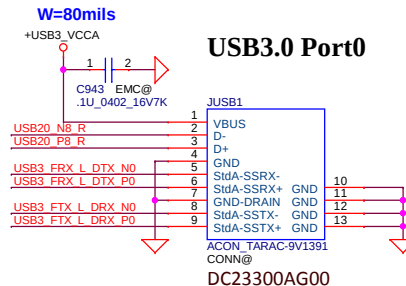
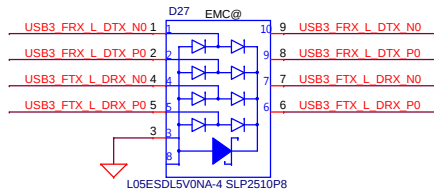


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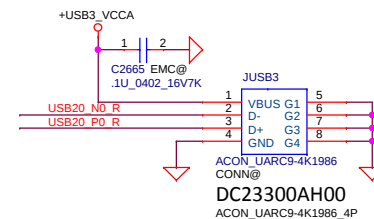
change L51 from SM070003Y00 to SM070003K00



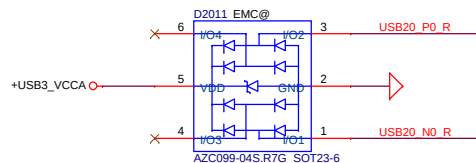
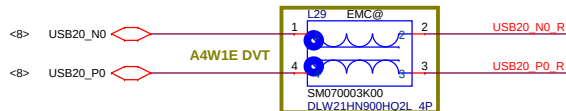
For ESD request



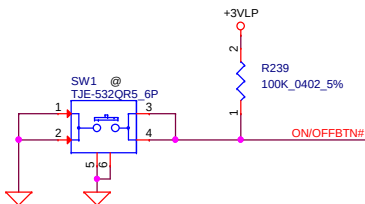
USB2.0 Port0



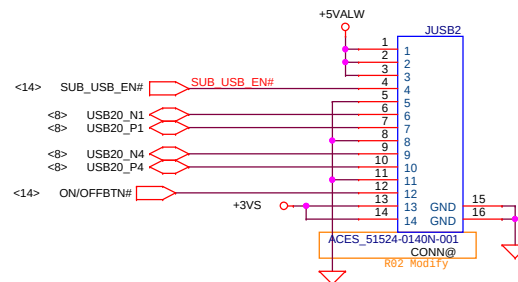
change L29 from SM070003Y00 to SM070003K00



ON/OFF BTN

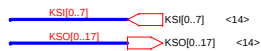


USB & CR/B

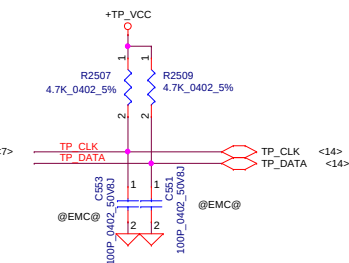
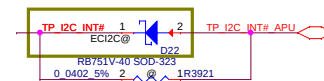
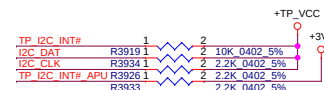
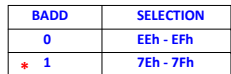


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				Size	Document Number	Rev
				Custom	B5W1E_LA-D121P	1.0
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KB Conn.

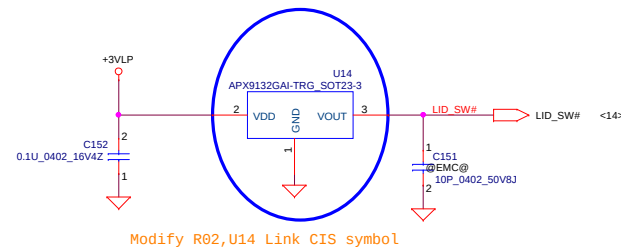


TPM Board for 2015



Lid Switch

(Hall Effect Switch)

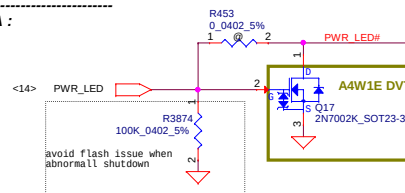


Dual Amber+Blue

LED

LTST-S115TBKF-CA (SC50000C500)

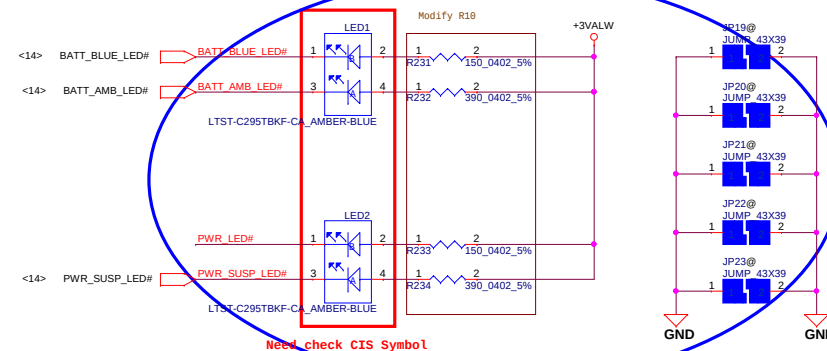
V_f @ 5 mA :



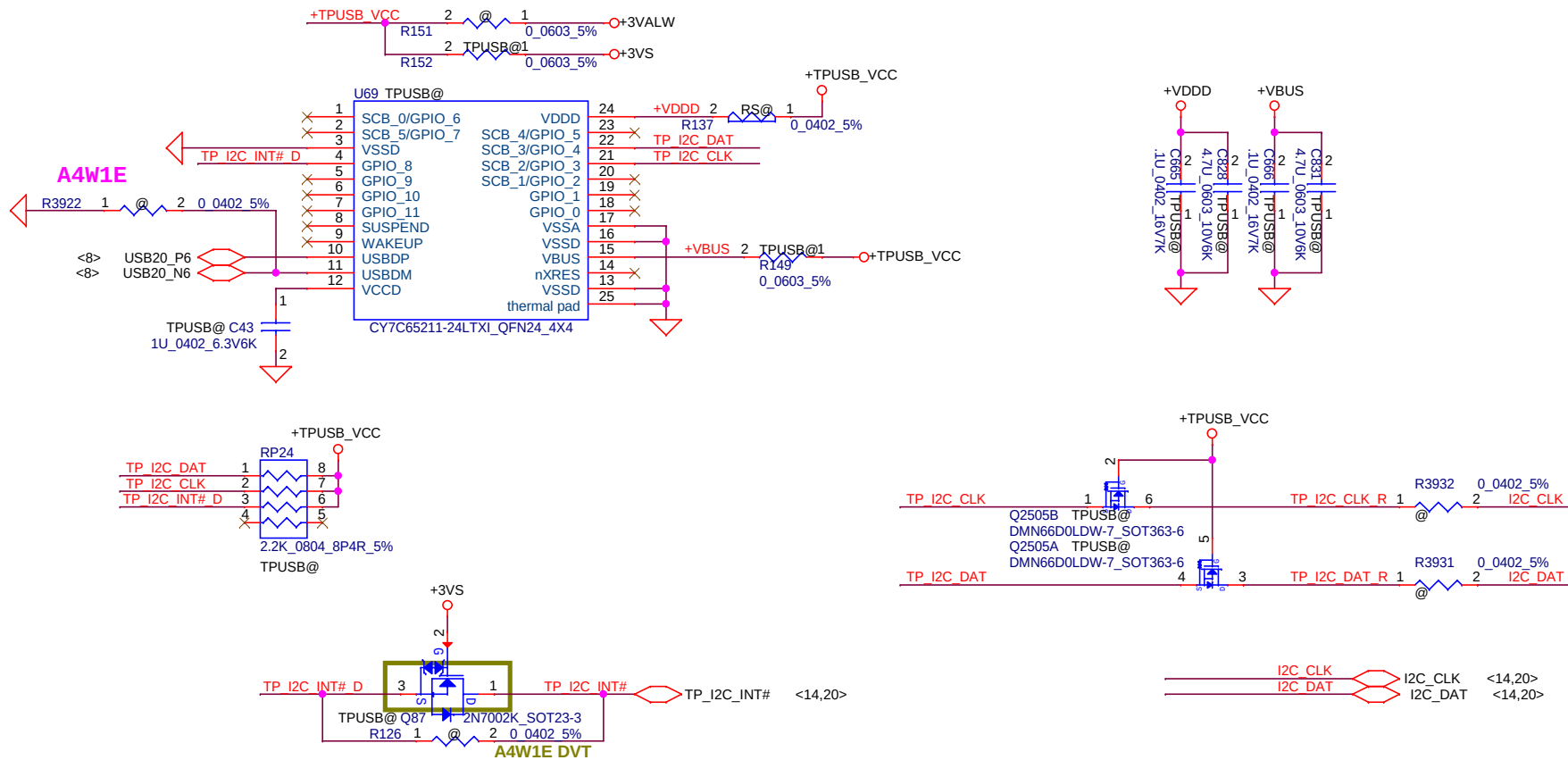
UD5: 1.7 ~ 2.3V
 $(3.3-1.7)/300=5.71 \text{ mA}$
 $(3.3-2.3)/300=3.57 \text{ mA}$
 R min: 100 ohm
 R max 700 ohm

CB5: 2.65~3.05V
 (3.3-2.65)/50=13.00 mA
 (3.3-3.05)/100=5.0 mA
 R min: 50 ohm
 R max:475 ohm

100 1%:SD034100080
150 1%:SD034150080
301 1%:SD034301080
680 1%:SD034680080
120 5%:SD028120080
560 5%:SD028560080
200 5%:SD028200080



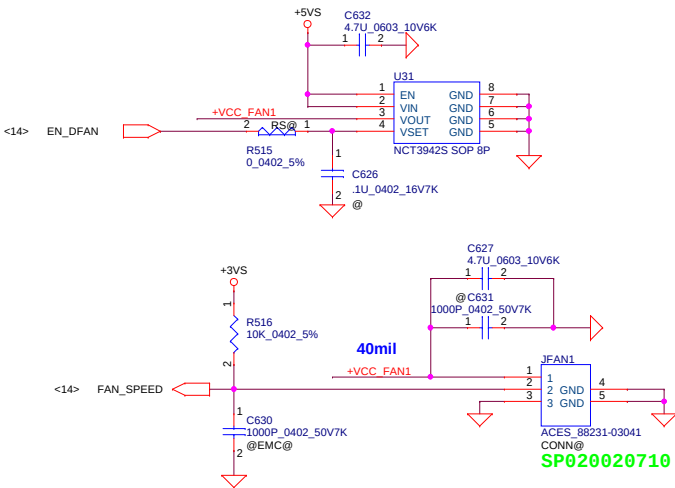
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2014/11/04	Deciphered Date	2016/11/04	Title		
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				Size	Document Number	Rev
				Custom	B5W1E LA-D121P	1.0
Date:	Thursday, April 16, 2015	Sheet	20	of	22	



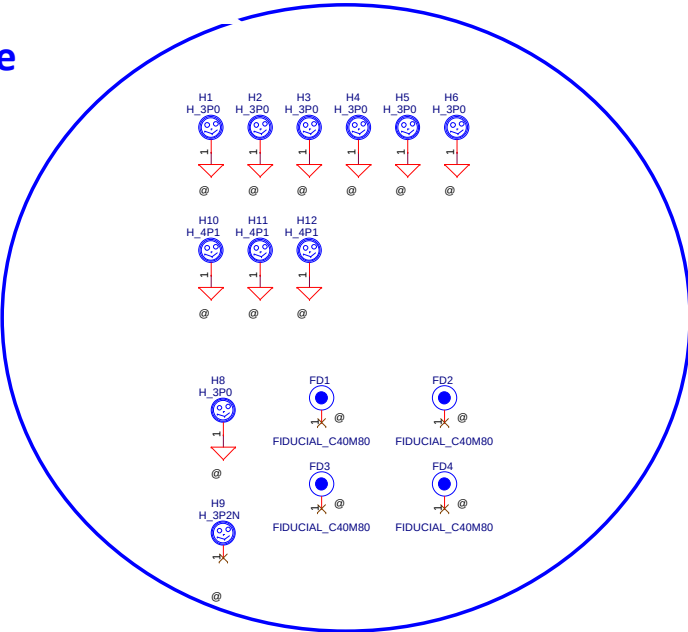
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Issued Date	2014/11/04	Deciphered Date	2016/11/04	Title	
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Size Custom		Document Number B5W1E_LA-D121P			Rev 1.0
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FAN1 Conn

FAN Conn

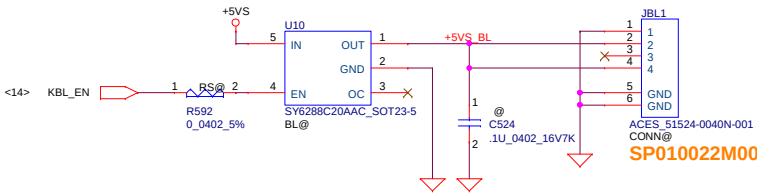


Screw Hole

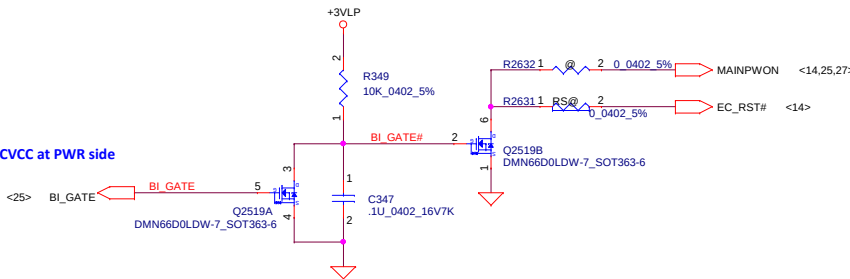


KB BackLight Conn. Reserve

Reset Circuit



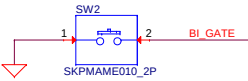
BI_GATE PH to +RTCVCC at PWR side



Del BI button

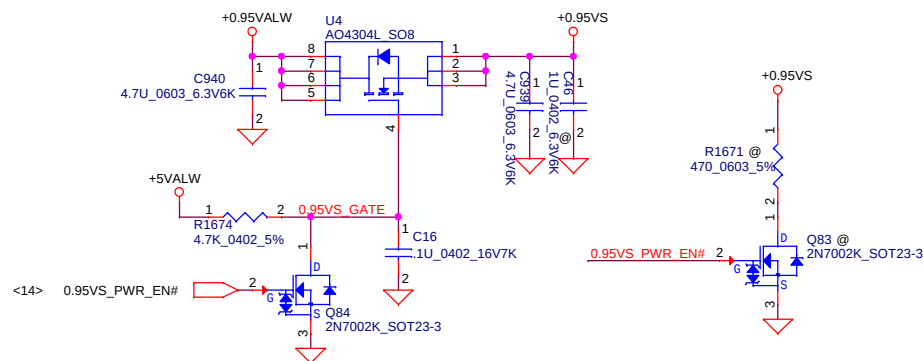
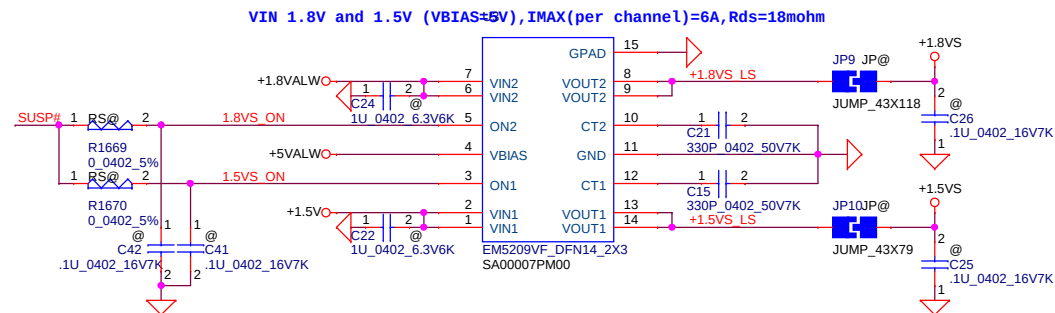
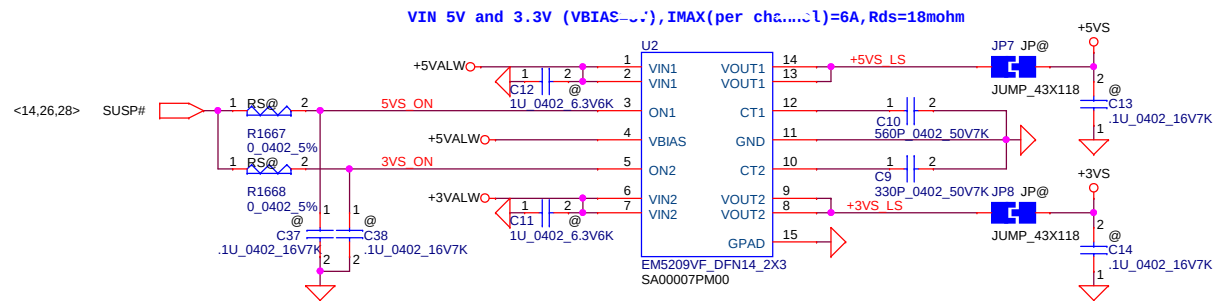
Reset Button

Reset Button

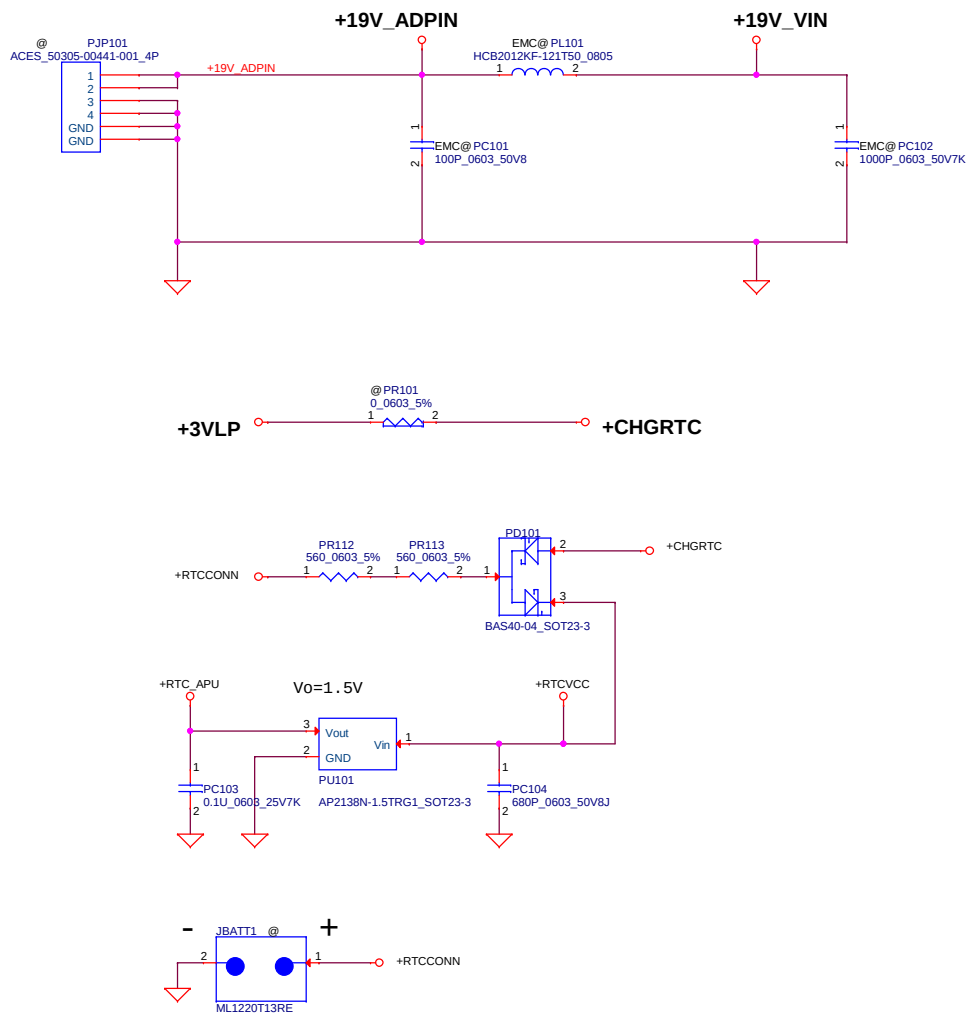


+1.8VALW TO +1.8VS
+1.5V TO +1.5VS
Load switch

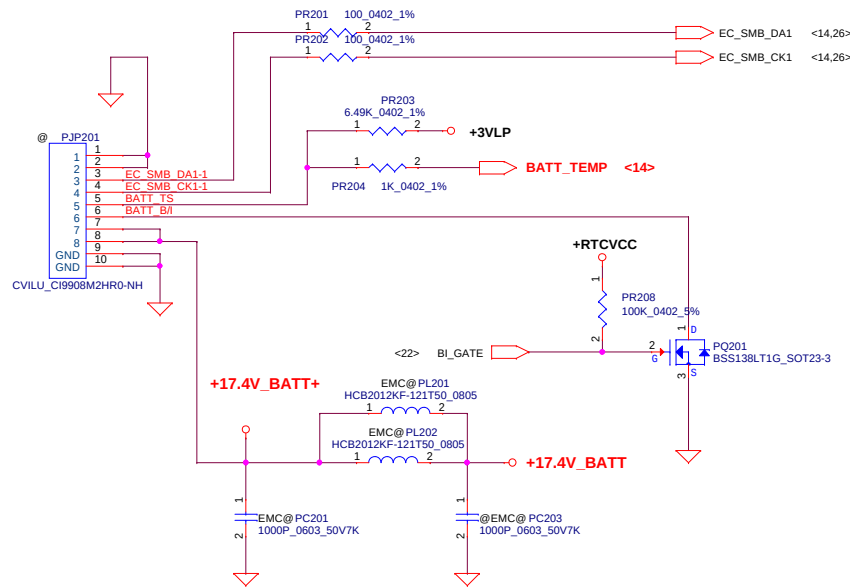
+0.95VALW to +0.95VS



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Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title	P22-DC INTERFACE	
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				DCIN
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---Battery_pin define---

PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TS
PIN6 B/I
PIN7 Batt+
PIN8 Batt+

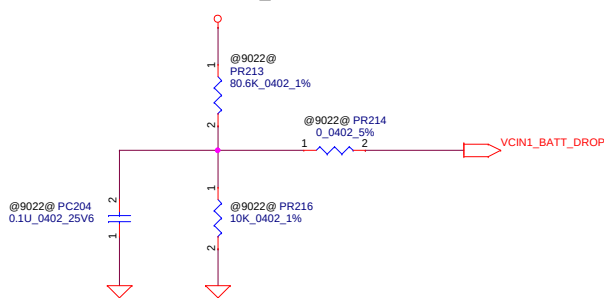
---Battery Con_pin define---

PIN8 GND
PIN7 GND
PIN6 SMD
PIN5 SMC
PIN4 TS
PIN3 B/I
PIN2 Batt+
PIN1 Batt+

2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Reserve for 2-cell design

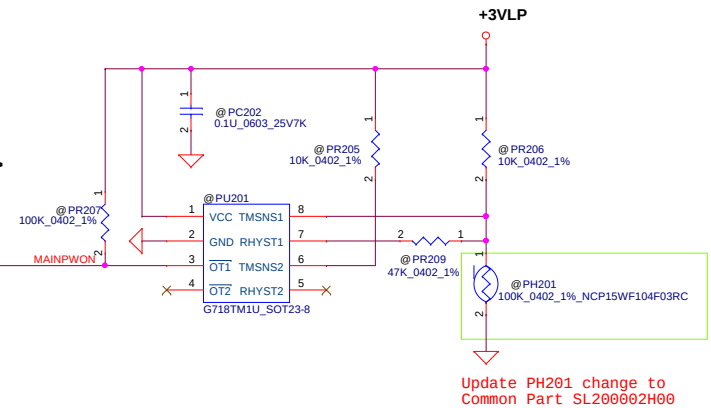
+19VB_5V



For 45W adapter==>action 48.15W , Recovery 38.7W
48.15W:
 $I_{ada} = 0 \sim 2.253A$ ($48.15W/19V=2.534A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 2.534 * 0.02 = 1.01$
38.7W:
 $I_{ada} = 0 \sim 2.036A$ ($38.7W/19V=2.036A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 2.036 * 0.02 = 0.814$
 $CP = 45W * 0.85 = 38.25W$

For 65W adapter==>action 69.55W , Recovery 55.9W
69.55W:
 $I_{ada} = 0 \sim 3.661A$ ($69.55W/19V=3.661A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 3.661 * 0.02 = 1.464$
55.9W:
 $I_{ada} = 0 \sim 2.942A$ ($55.9W/19V=2.942A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 2.942 * 0.02 = 1.177$
 $CP = 65W * 0.85 = 55.25W$

<45, 47>
<14,22,27> MAINPWON

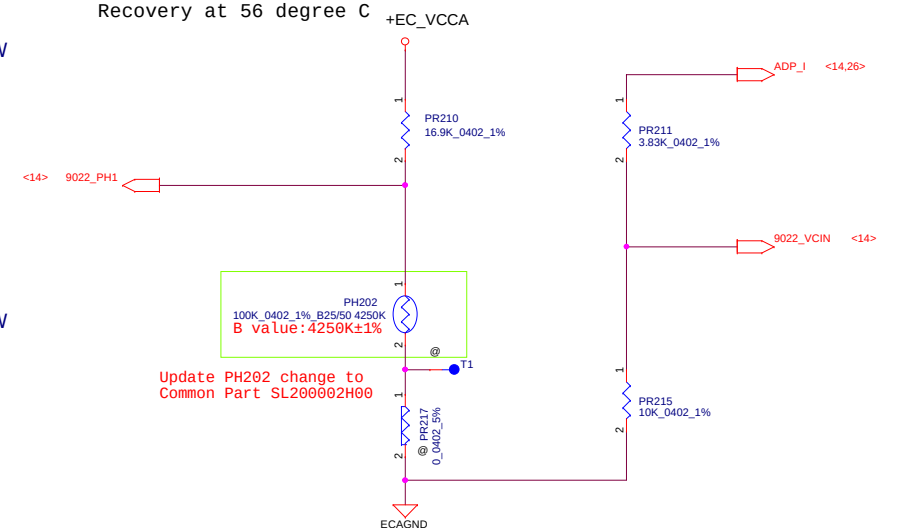


Update PH201 change to
Common Part SL200002H00

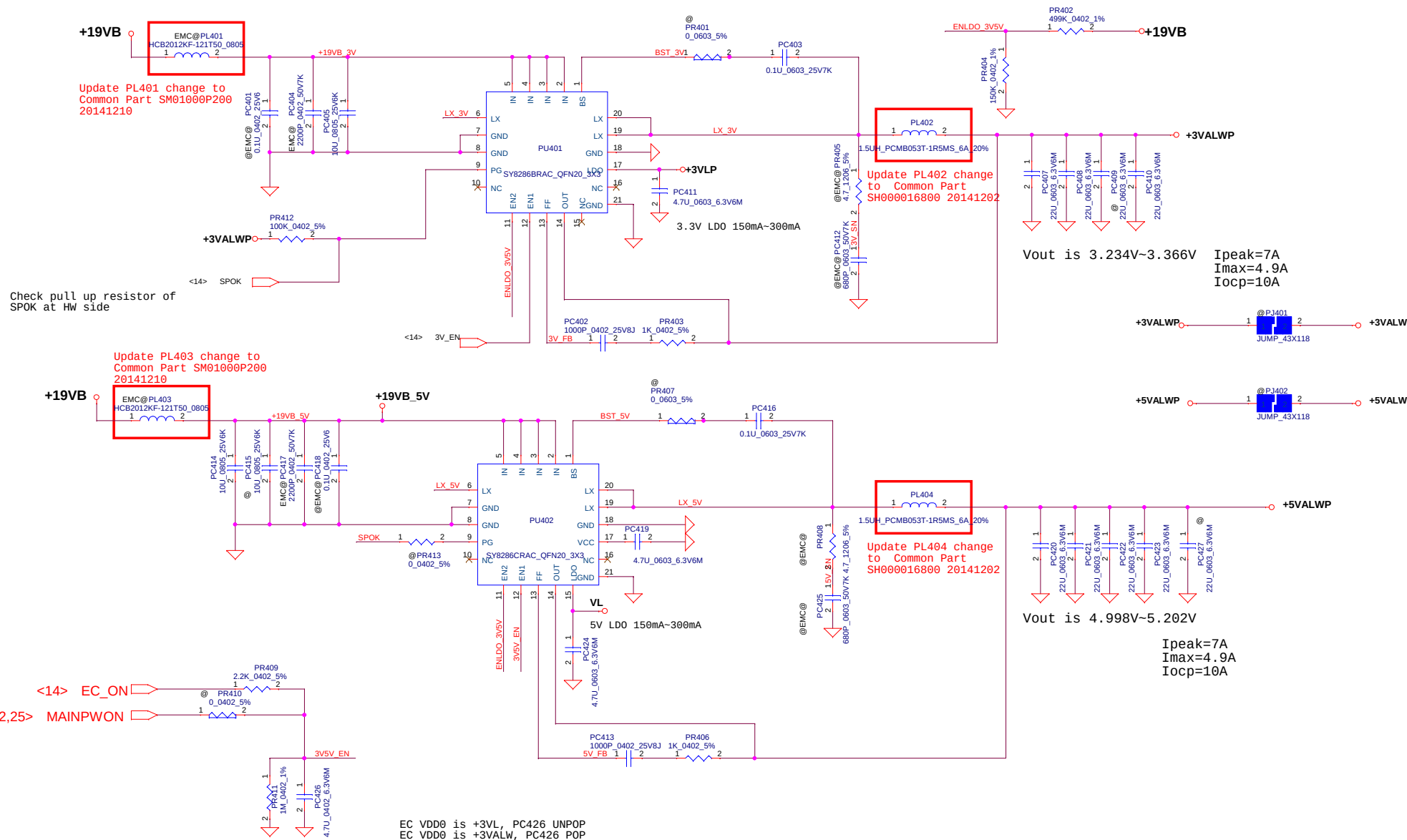
For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92C, 1V	56C, 2.V
PH202(ohm)	7.3K	26.11K

For KB9012 sense 20mΩ	Active	Recovery
45W	48.15W, 0.73V	38.7W, 0.59V
65W	69.55W, 0.73V	55.9W, 0.59V

PH202 under CPU bottom side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C



Update PH202 change to
Common Part SL200002H00



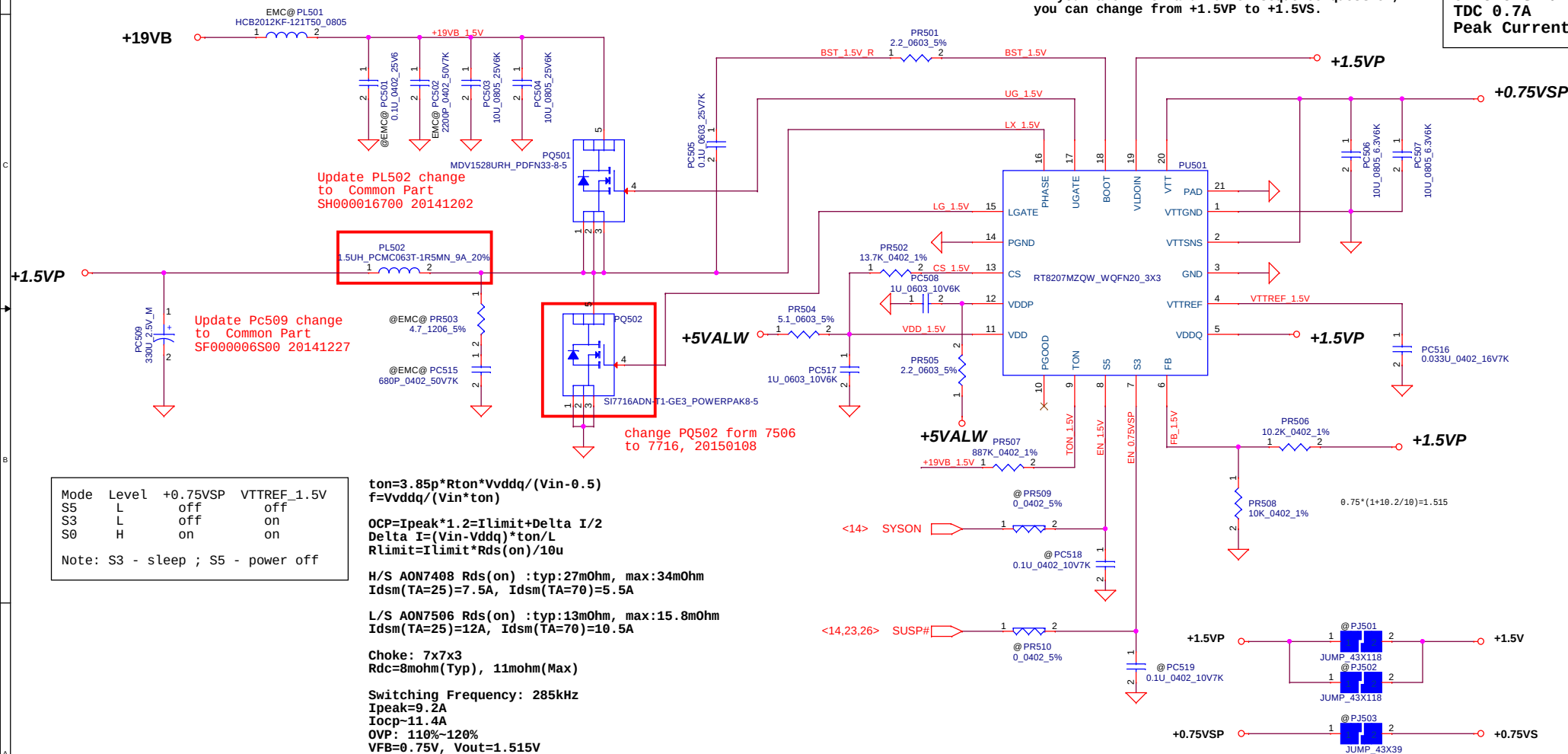
Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2014/10/20		Deciphered Date		2016/10/20		Title		+3VALW/+5VALW			
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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

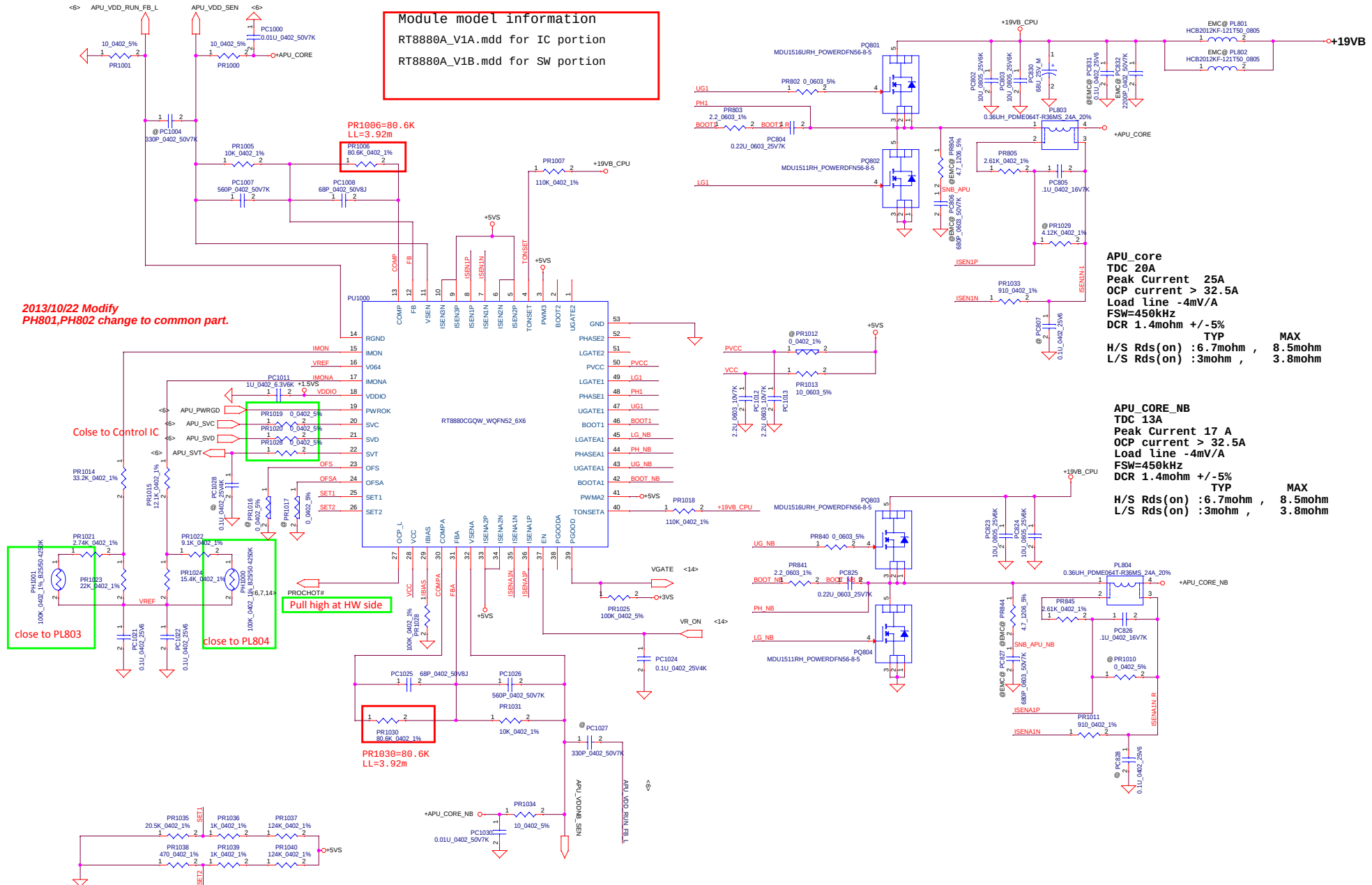
Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



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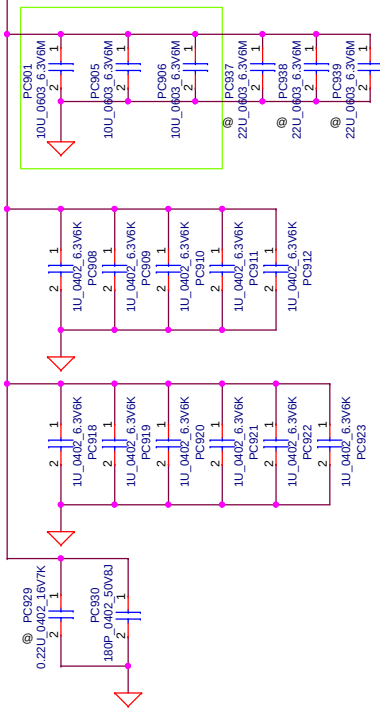
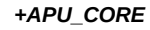
2013/10/16 Modify
PQ801,PQ803 change to AON6552.
PQ802,PQ804,PQ805 change to AON6554.



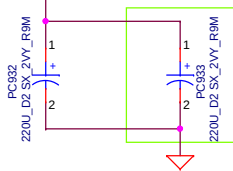
Delete PR834.PR835.PR836.PR839.PR840.PR841,
follow vender FAE suggest.
2013/11/29 modify.

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				Rev	1.0

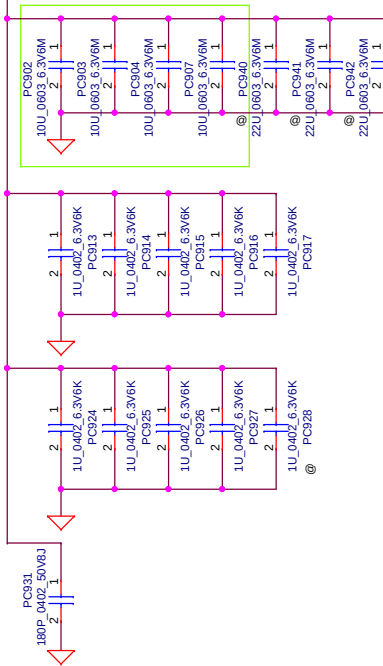
+APU_CORE (36.4)



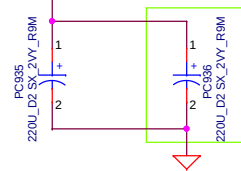
+APU_CORE



+APU_CORE_NB (36.5)



+APU_CORE_NB



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for PWR

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Item	Page	Date	Reason for change	Phase
01		2015/02/05	modify form A4W1E, i/o copy from Z5W1M	DVT
02	11	2015/02/06	update to DIMM*2	
03	06		del JHDT1 circuit	
04	20	2015/02/09	for TP diff device	
05	18		del EXT HDD connector	
06	14	2015/02/11	define 15" EVT	
07			Change all EMI/ESD BS to EMC@	
08	15	2015/02/13	del JP25 (confirm with EMI Eddie)	
09	21	2015/02/24	schematic update	
10	07			
11	14			
12	15			
13	15			
14		2015/02/25	update power circuit.	
15	14		for common use Z5W1M I/O board	
16	17		schematic update	
17	23	2015/02/26	schematic update	
18	17			
19	08			
20	07			
21	07			
22	18	2015/03/03	schematic update	
23	14			
24	05			
25	13,19,21			
26	13	2015/03/04	schematic update	
27	15			
28	19			
29	5	2015/03/05	schematic update	
30	4	2015/03/06	schematic update	
31	23	2015/03/07	schematic update	
32	5	2015/03/10	schematic update	
33	15	2015/03/10		
34	12	2015/03/13	schematic update	
35	1,2	2015/03/18	schematic update	
36	13,15,19	2015/04/08	schematic update	
37		2015/04/09	update power circuit to 0409	
38		2015/04/09	Change 0 ohm to 0ohm R-S	
39		2015/04/10		

Security Classification

Issued Date

2014/03/27

Deciphered Date

2016/03/27

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