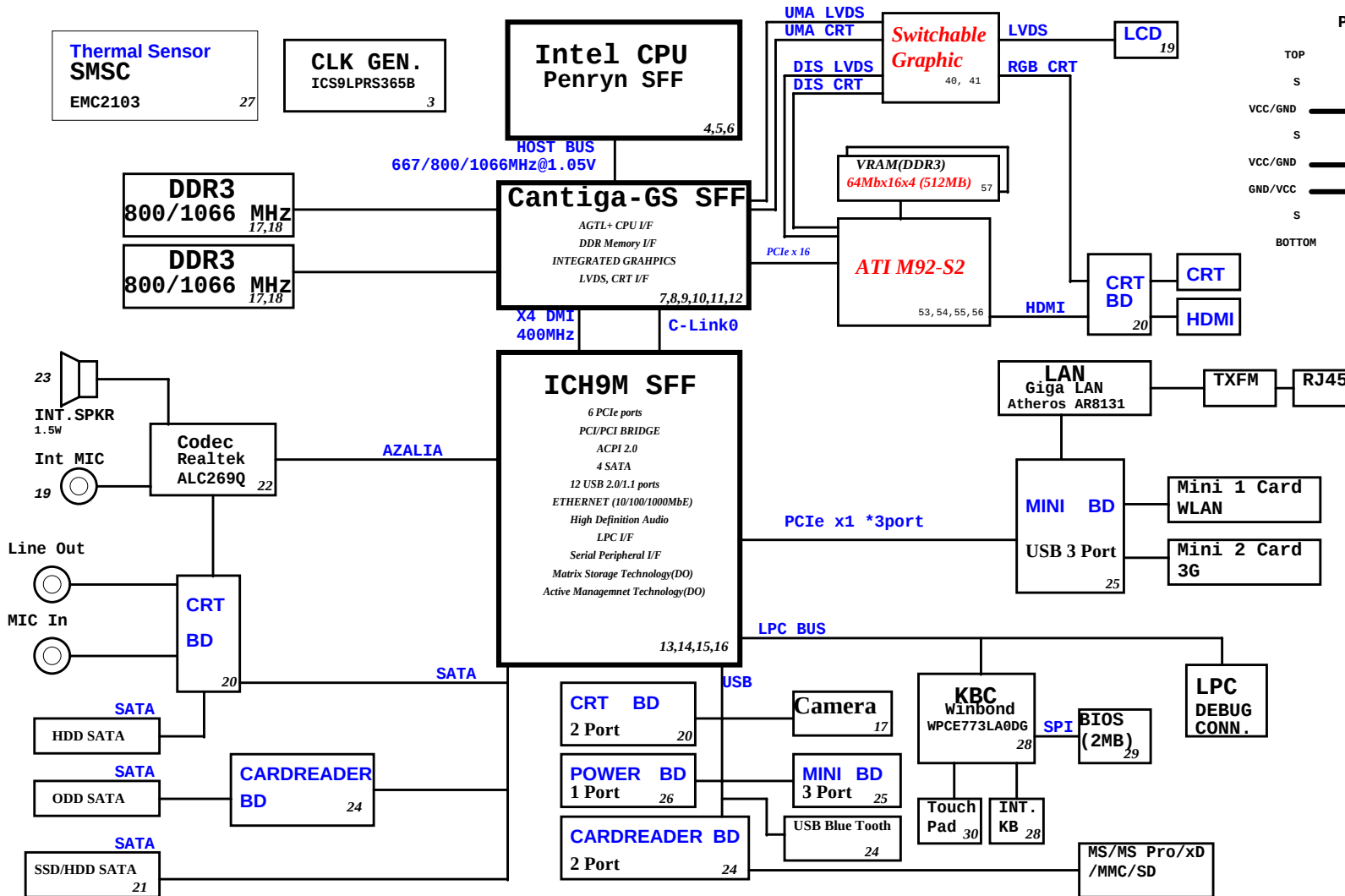
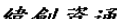


JM41/JM51 Discrete Block Diagram

Project code: 91.4CQ01.001
PCB P/N : 48.4CQ01.0SB
REVISION : 08274-1



SYSTEM DC/DC	
TPS51125	36
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (6A) 3D3V_S5 (5A) 5V_AUX_S5 3D3V_AUX_S5
RT8202	37
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 (10A)
RT8202	38
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 (11A)
RT9026	39
INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 (1.2A)
CHARGER	
MAX8731A	41
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
CPU DC/DC	
ADP3207A	35
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0-1.3V 64A
VGA	
ISL6263A	40
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

DIS			
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Title			
BLOCK DIAGRAM			
Size Custom	Document Number	JM41 Discrete	Rev -2
Date:	Tuesday, April 28, 2009	Sheet 1 of	48

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

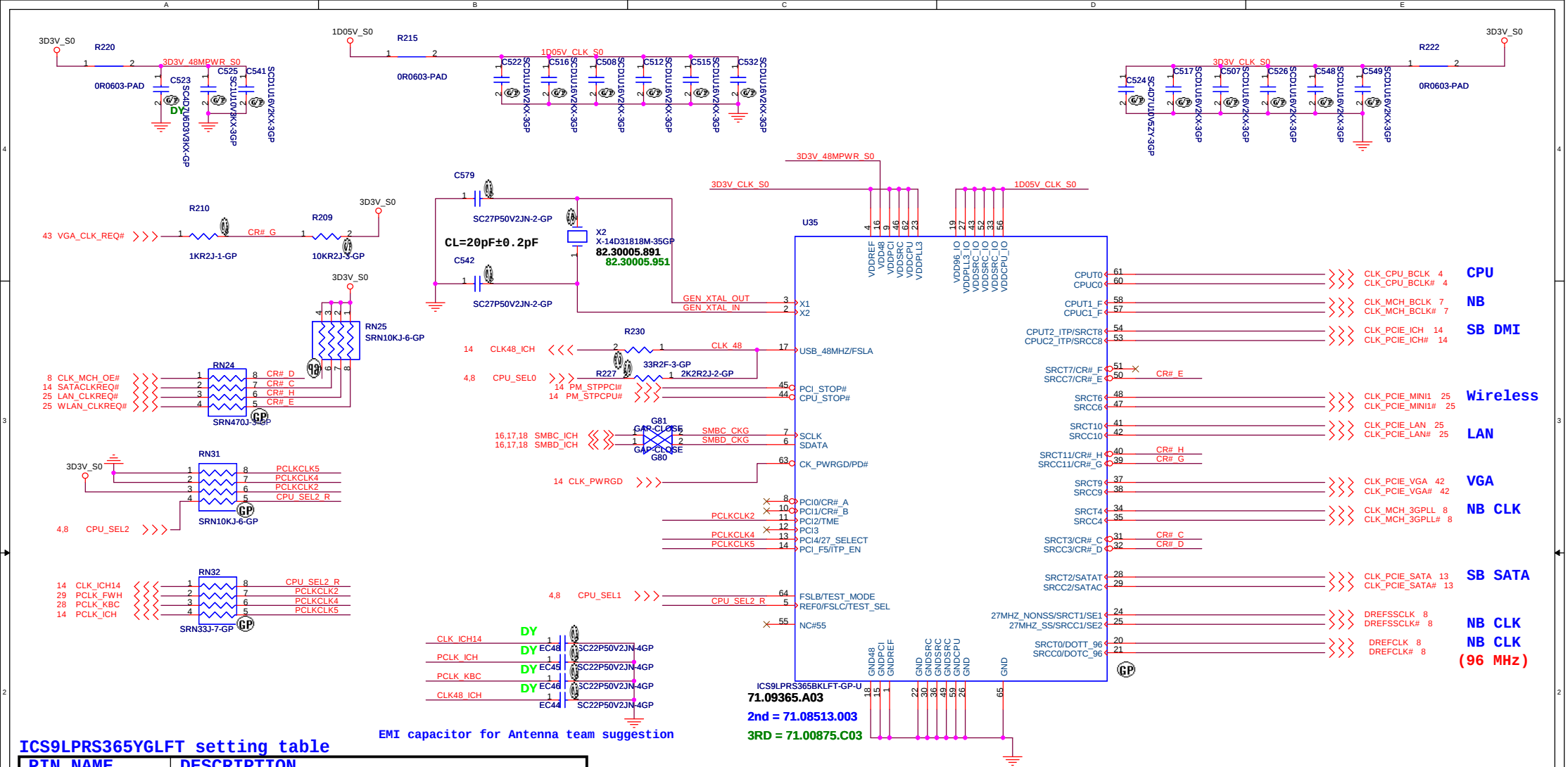
SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCie are operating simulatanuously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.



ICS9LPRS365YGLFT setting table

PIN	NAME	DESCRIPTION
43	VGA_CLK_REQ#	>>>
8	CLK_MCH_OE#	>>>
14	SATACLKREQ#	>>>
25	LAN_CLKREQ#	>>>
25	WLAN_CLKREQ#	>>>
14	CLK_ICH14	>>>
29	PCLK_FWH	>>>
28	PCLK_KBC	>>>
14	PCLK_ICH	>>>
4,8	CPU_SEL2	>>>
4,8	CPU_SEL1	>>>
14	CLK_ICH14	DY
29	PCLK_FWH	DY
28	PCLK_KBC	DY
14	PCLK_ICH	DY

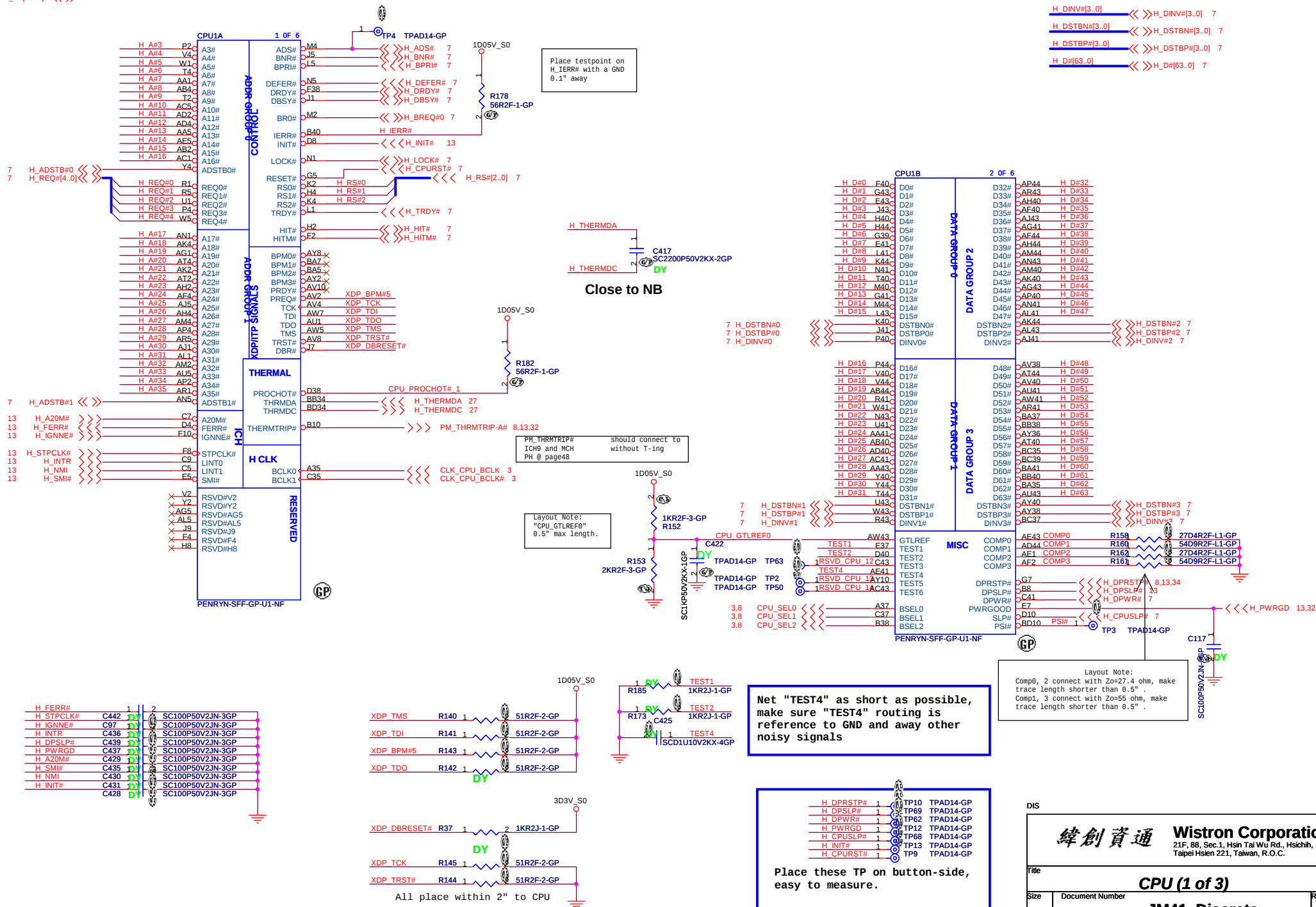
EMI capacitor for Antenna team suggestion

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7 enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

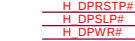
SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

DIS

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Title Clock Generator	
Size	Document Number JM41 Discrete
Date: Tuesday, April 28, 2009	Sheet 3 of 48
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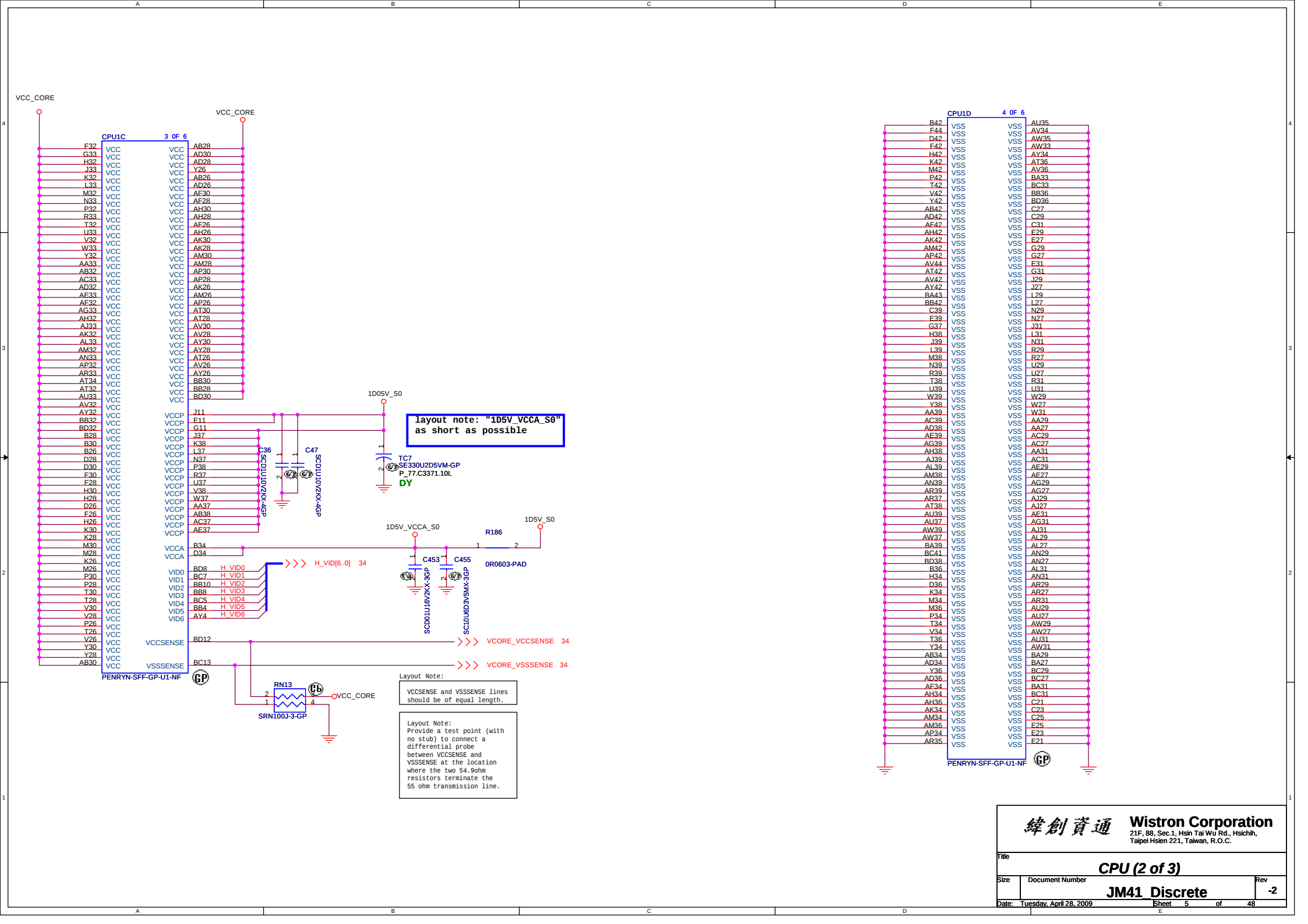
Net "TEST4" as short as possible,
make sure "TEST4" routing is
reference to GND and away other
noisy signals



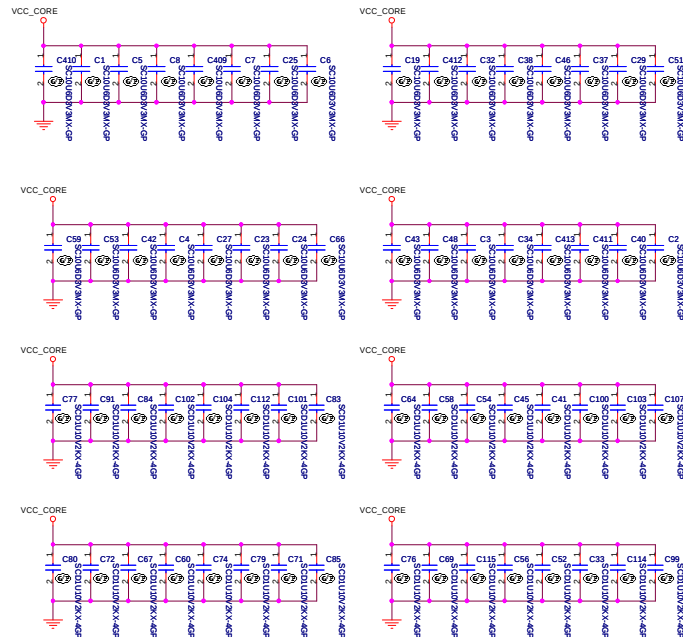
TP Pin	TPAD14-GP Pin
TP1	TP10
TP2	TP11
TP3	TP12
TP4	TP13
TP5	TP14
TP6	TP15
TP7	TP16
TP8	TP17
TP9	TP18

Place these TP on button-side, easy to measure.

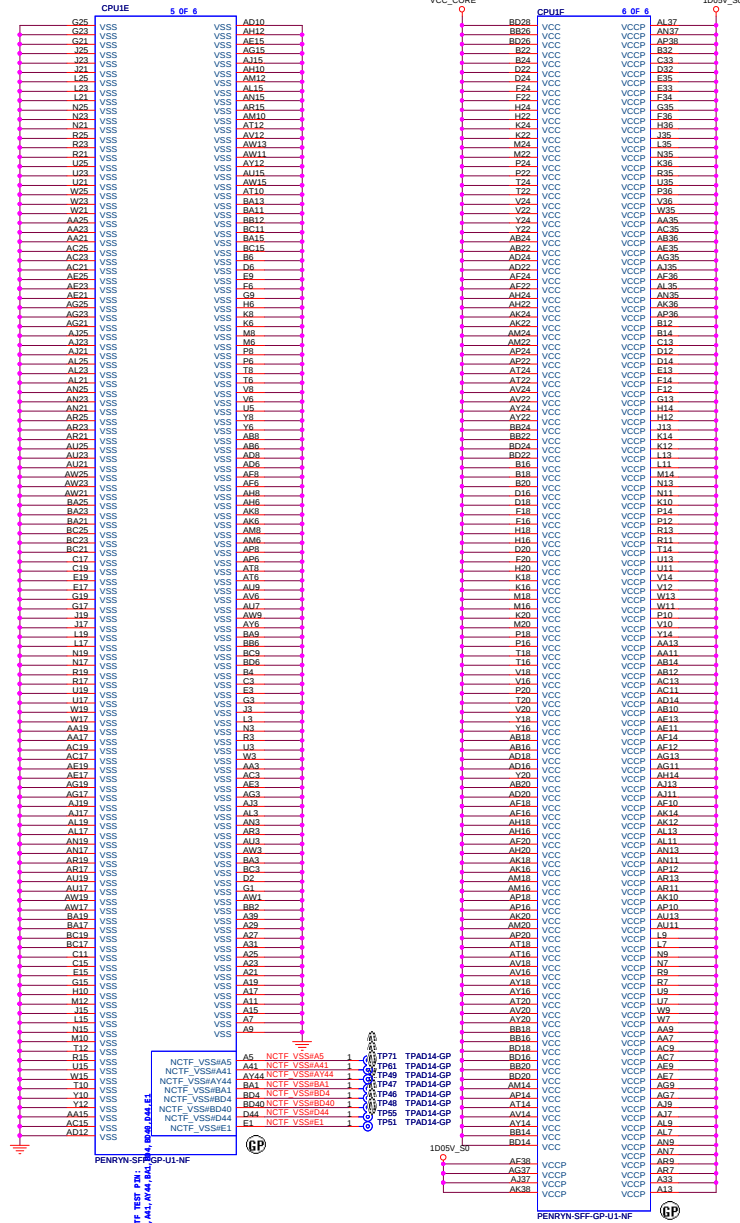
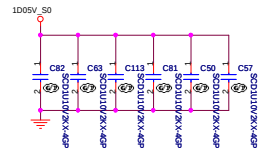
Layout Note:
Comp0, 2 connect with $Z_0=27.4\ \Omega$, make trace length shorter than $0.5''$.
Comp1, 3 connect with $Z_0=55\ \Omega$, make trace length shorter than $0.5''$.



Place these inside socket cavity on L8(North side Secondary)



Place these inside socket cavity on L8(North side Secondary)

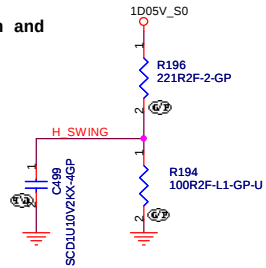


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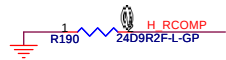
CPU (3 of 3)			Rev
Size	Document Number	JM41 Discrete	-2
Date: Tuesday, April 28, 2009	Pages: 8	of 88	

H_SWING routing Trace width and Spacing use 10 / 20 mil

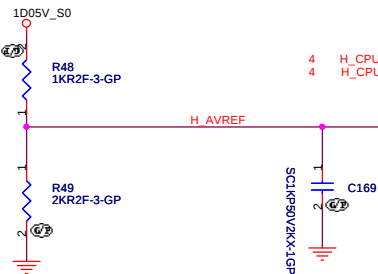
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5"



H D#0	J7	H D#0	J7
H D#1	H6	H D#1	H6
H D#2	L11	H D#2	L11
H D#3	J3	H D#3	J3
H D#4	H4	H D#4	H4
H D#5	G3	H D#5	G3
H D#6	K10	H D#6	K10
H D#7	K12	H D#7	K12
H D#8	L1	H D#8	L1
H D#9	M10	H D#9	M10
H D#10	M6	H D#10	M6
H D#11	N11	H D#11	N11
H D#12	L7	H D#12	L7
H D#13	K6	H D#13	K6
H D#14	M4	H D#14	M4
H D#15	K4	H D#15	K4
H D#16	P6	H D#16	P6
H D#17	W9	H D#17	W9
H D#18	V6	H D#18	V6
H D#19	V2	H D#19	V2
H D#20	P10	H D#20	P10
H D#21	W7	H D#21	W7
H D#22	N9	H D#22	N9
H D#23	P4	H D#23	P4
H D#24	U9	H D#24	U9
H D#25	V4	H D#25	V4
H D#26	U1	H D#26	U1
H D#27	W3	H D#27	W3
H D#28	V10	H D#28	V10
H D#29	U7	H D#29	U7
H D#30	W11	H D#30	W11
H D#31	U11	H D#31	U11
H D#32	AC11	H D#32	AC11
H D#33	AC9	H D#33	AC9
H D#34	V4	H D#34	V4
H D#35	Y10	H D#35	Y10
H D#36	AB6	H D#36	AB6
H D#37	AA9	H D#37	AA9
H D#38	AB10	H D#38	AB10
H D#39	AA1	H D#39	AA1
H D#40	AC3	H D#40	AC3
H D#41	AC7	H D#41	AC7
H D#42	AD12	H D#42	AD12
H D#43	AB4	H D#43	AB4
H D#44	Y6	H D#44	Y6
H D#45	AD10	H D#45	AD10
H D#46	AA11	H D#46	AA11
H D#47	AB2	H D#47	AB2
H D#48	AD4	H D#48	AD4
H D#49	AE7	H D#49	AE7
H D#50	AD2	H D#50	AD2
H D#51	AD6	H D#51	AD6
H D#52	AE3	H D#52	AE3
H D#53	AC9	H D#53	AC9
H D#54	AG7	H D#54	AG7
H D#55	AE11	H D#55	AE11
H D#56	AK6	H D#56	AK6
H D#57	AF6	H D#57	AF6
H D#58	AJ9	H D#58	AJ9
H D#59	AH6	H D#59	AH6
H D#60	AE12	H D#60	AE12
H D#61	AH4	H D#61	AH4
H D#62	AJ7	H D#62	AJ7
H D#63	AE9	H D#63	AE9

H_SWING B6
H_RCOMP D4

4 H_CPURST# J11
4 H_CPUSLP# G9

H_AVREF L17
H_DVREF K18

CANTIGA-GS-GP-NF

HOST

1 OF 10

H_A#_3
H_A#_4
H_A#_5
H_A#_6
H_A#_7
H_A#_8
H_A#_9
H_A#_10
H_A#_11
H_A#_12
H_A#_13
H_A#_14
H_A#_15
H_A#_16
H_A#_17
H_A#_18
H_A#_19
H_A#_20
H_A#_21
H_A#_22
H_A#_23
H_A#_24
H_A#_25
H_A#_26
H_A#_27
H_A#_28
H_A#_29
H_A#_30
H_A#_31
H_A#_32
H_A#_33
H_A#_34
H_A#_35

L15
B14
C15
D12
F14
G17
B12
J15
D16
C17
D14
K16
F16
B16
C21
D18
J19
B18
D22
G19
J17
L21
L19
G21
D20
K22
F18
K20
E20
F22
B20
A19

H_A#3
H_A#4
H_A#5
H_A#6
H_A#7
H_A#8
H_A#9
H_A#10
H_A#11
H_A#12
H_A#13
H_A#14
H_A#15
H_A#16
H_A#17
H_A#18
H_A#19
H_A#20
H_A#21
H_A#22
H_A#23
H_A#24
H_A#25
H_A#26
H_A#27
H_A#28
H_A#29
H_A#30
H_A#31
H_A#32
H_A#33
H_A#34
H_A#35

H_ADS#
H_ADSTB#_0
H_ADSTB#_1
H_BNR#
H_BPRI#
H_BREQ#
H_DEFER#
H_DBSY#
HPLL_CLK#
HPLL_CLK#
H_DPWR#
H_DRDY#
H_HIT#
H_HITM#
H_LOCK#
H_TRDY#

F10
A15
C19
C9
B8
C11
E5
D8
AH10
AJ11
G11
H2
C7
E8
A11
D8

H_ADS# 4
H_ADSTB#0 4
H_ADSTB#1 4
H_BNR# 4
H_BPRI# 4
H_BREQ#0 4
H_DEFER# 4
H_DBSY# 4
CLK_MCH_BCLK# 3
CLK_MCH_BCLK# 3
H_DPWR# 4
H_DRDY# 4
H_HIT# 4
H_HITM# 4
H_LOCK# 4
H_TRDY# 4

H_DINV#_0
H_DINV#_1
H_DINV#_2
H_DINV#_3

L9
N7
AA7
AG3

H_DINV#3.0] <<< H_DINV#3.0] 4
H_DSTBN#3.0] <<< H_DSTBN#3.0] 4
H_DSTBP#3.0] <<< H_DSTBP#3.0] 4

H_DSTBN#_0
H_DSTBN#_1
H_DSTBN#_2
H_DSTBN#_3

K2
N3
AA3
AF4

H_DSTBP#_0
H_DSTBP#_1
H_DSTBP#_2
H_DSTBP#_3

L3
M2
Y2
AF2

H_REQ#_0
H_REQ#_1
H_REQ#_2
H_REQ#_3
H_REQ#_4

J13
L13
C13
G13
G15

H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4

H_RS#_0
H_RS#_1
H_RS#_2

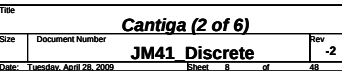
F4
F2
G7

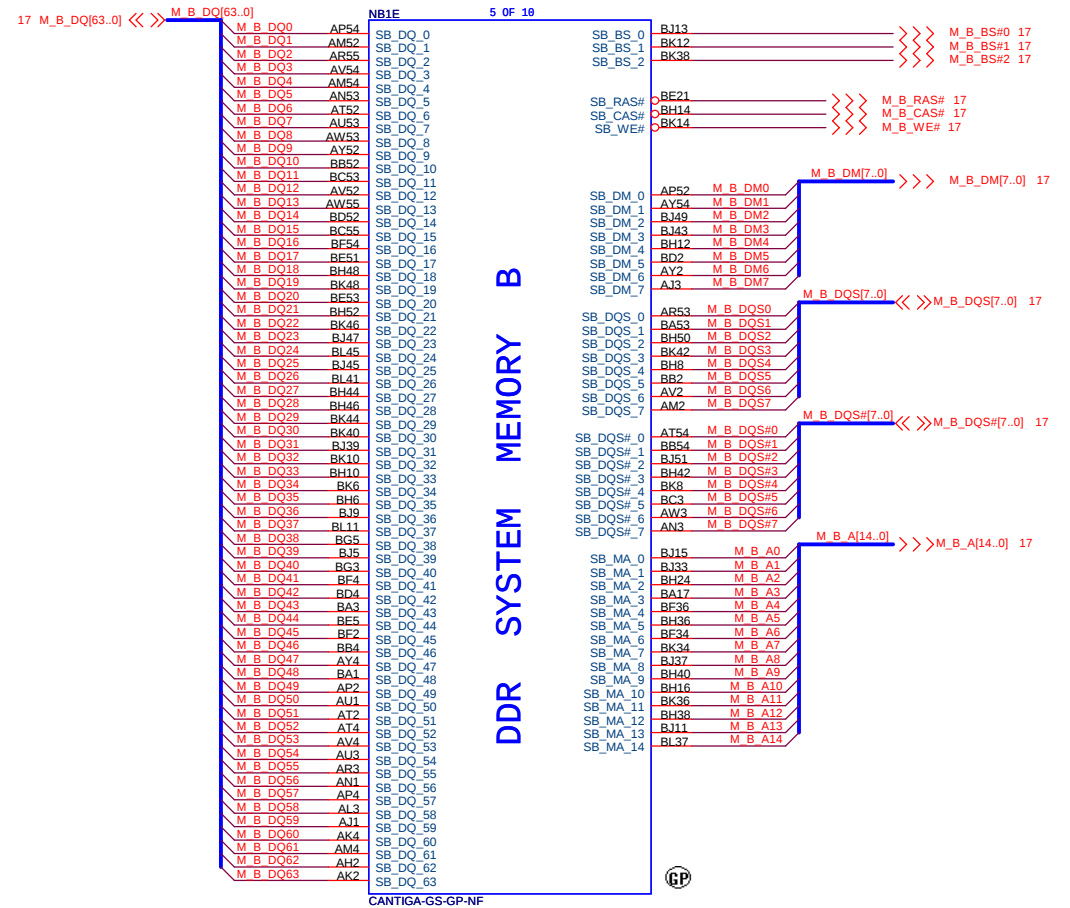
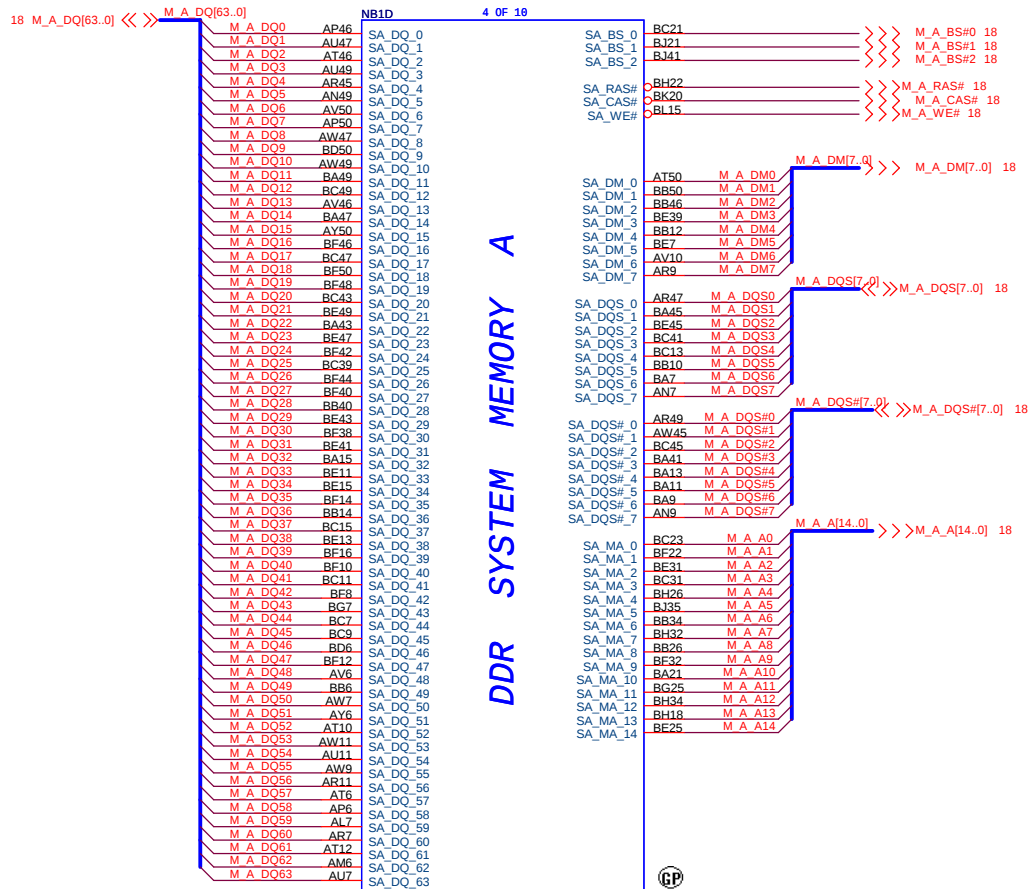
H_RS#0
H_RS#1
H_RS#2

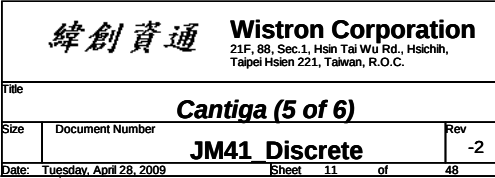
DIS

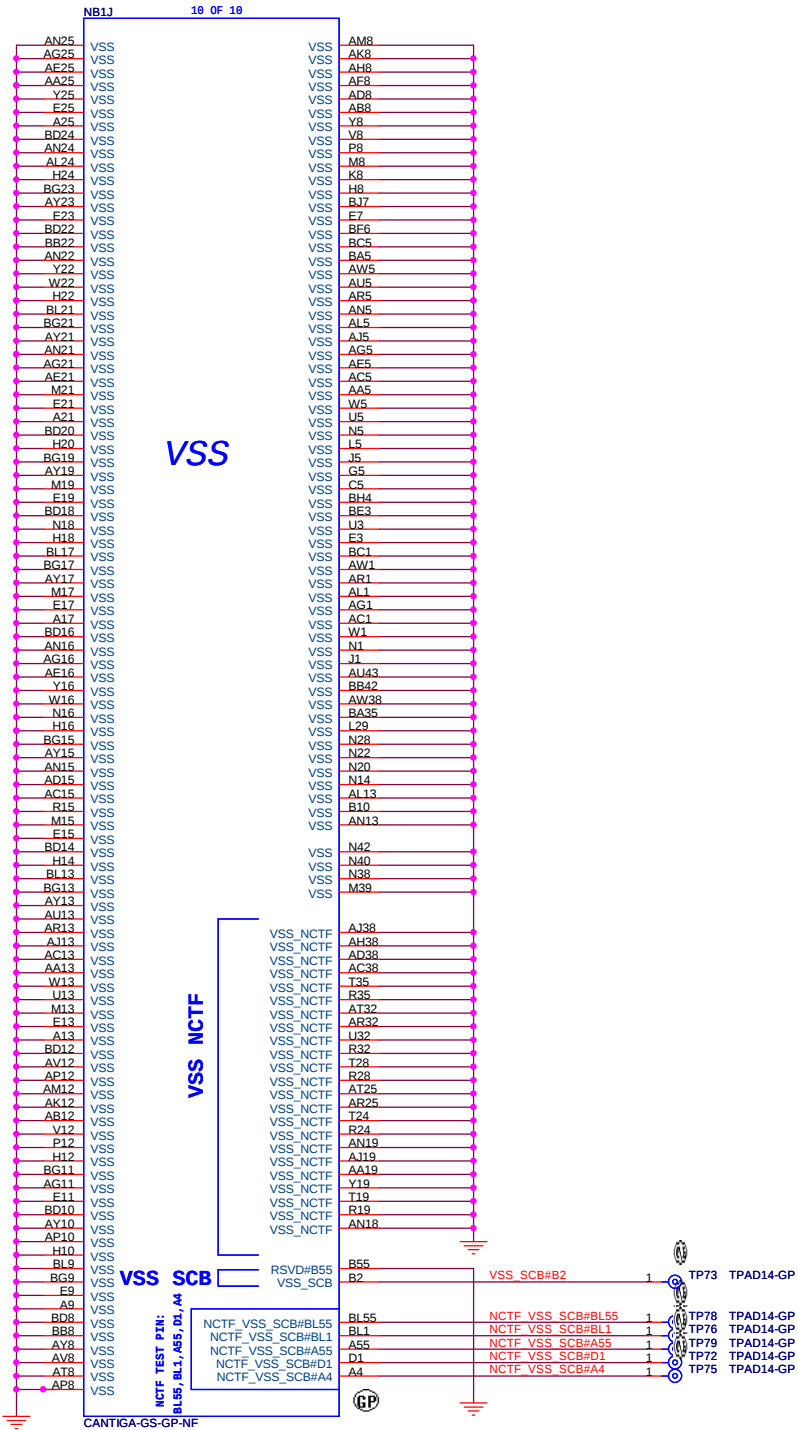
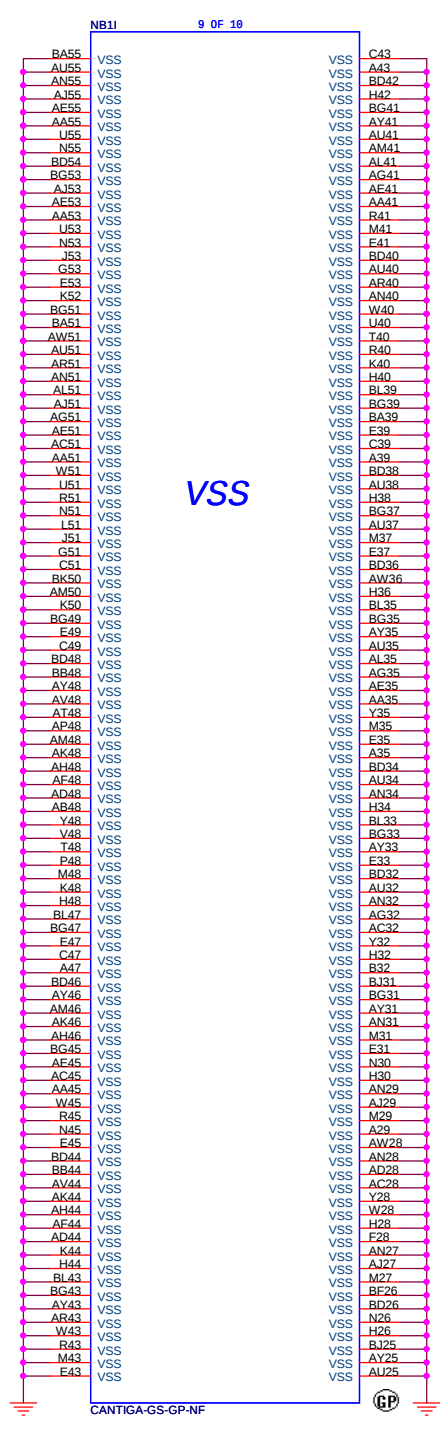
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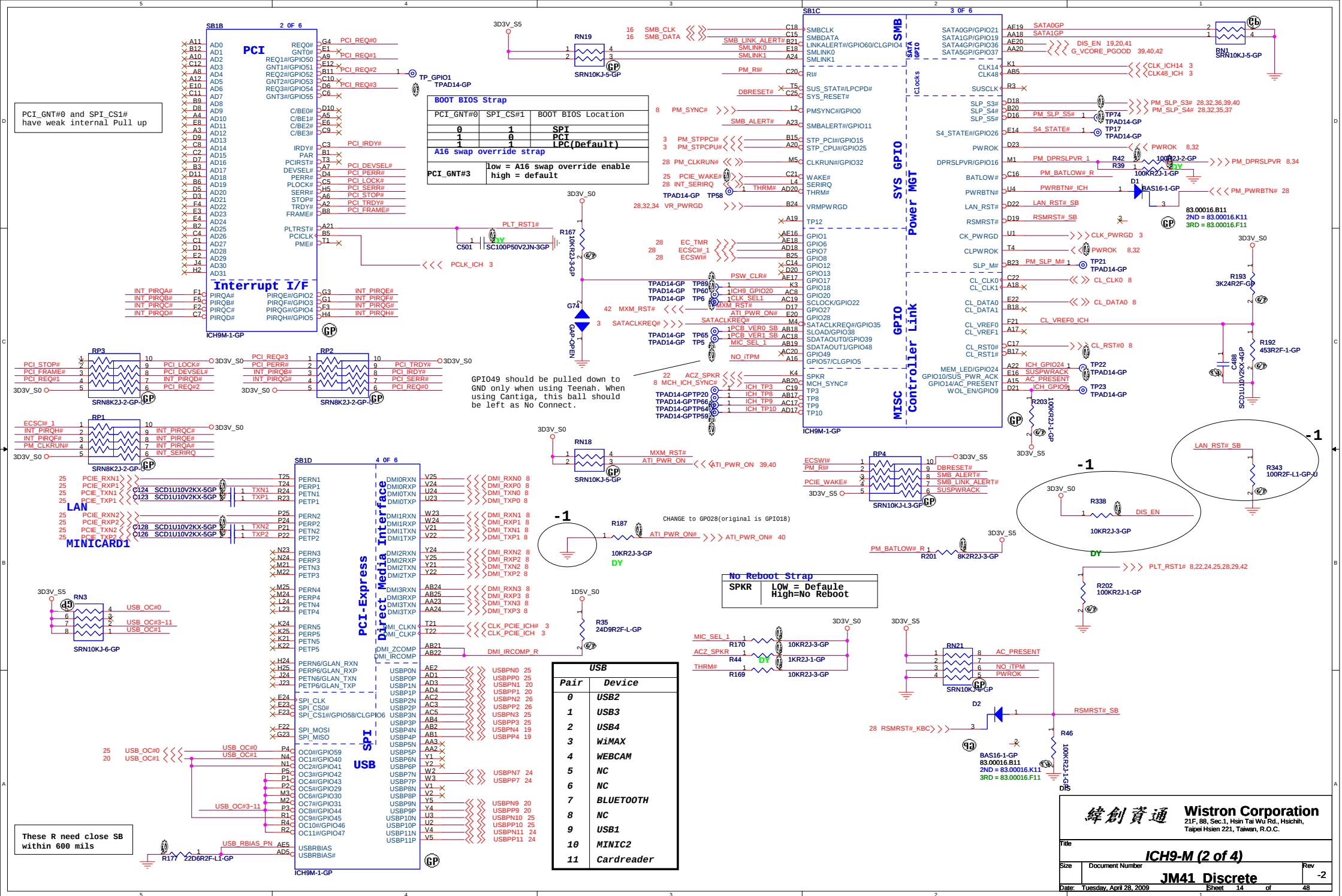
Title
Size Document Number
Date: Tuesday, April 28, 2009
Cantiga (1 of 6)
JM41 Discrete
Rev
-2
Sheet 7 of 48











657mA

6uA in G3

1.13A

23mA

50mA

1mA

VCC3_3=278mA

32mA

32mA

177mA

18mA

47mA

SATA+USB=1.56A

USBPLL=10mA

23mA

80mA

2mA

2mA

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

Layout Note:
Place near ICH9

Layout Note: Place near ICH9M

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title

ICH9-M (3 of 4)

Size

Document Number

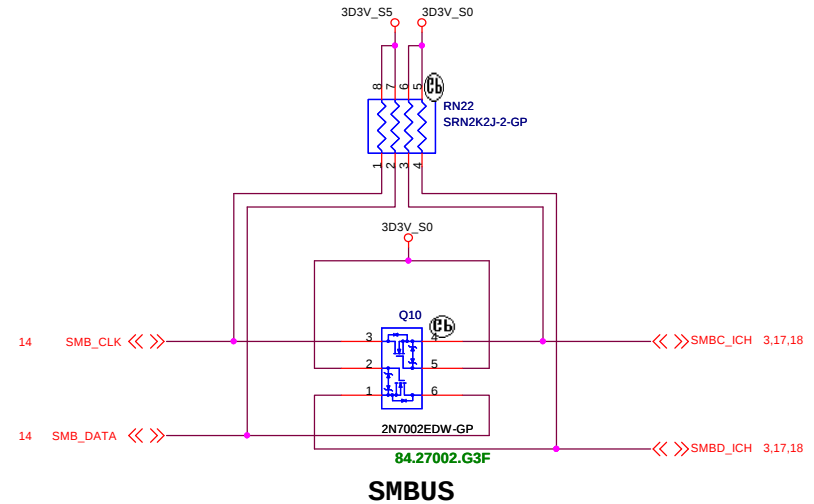
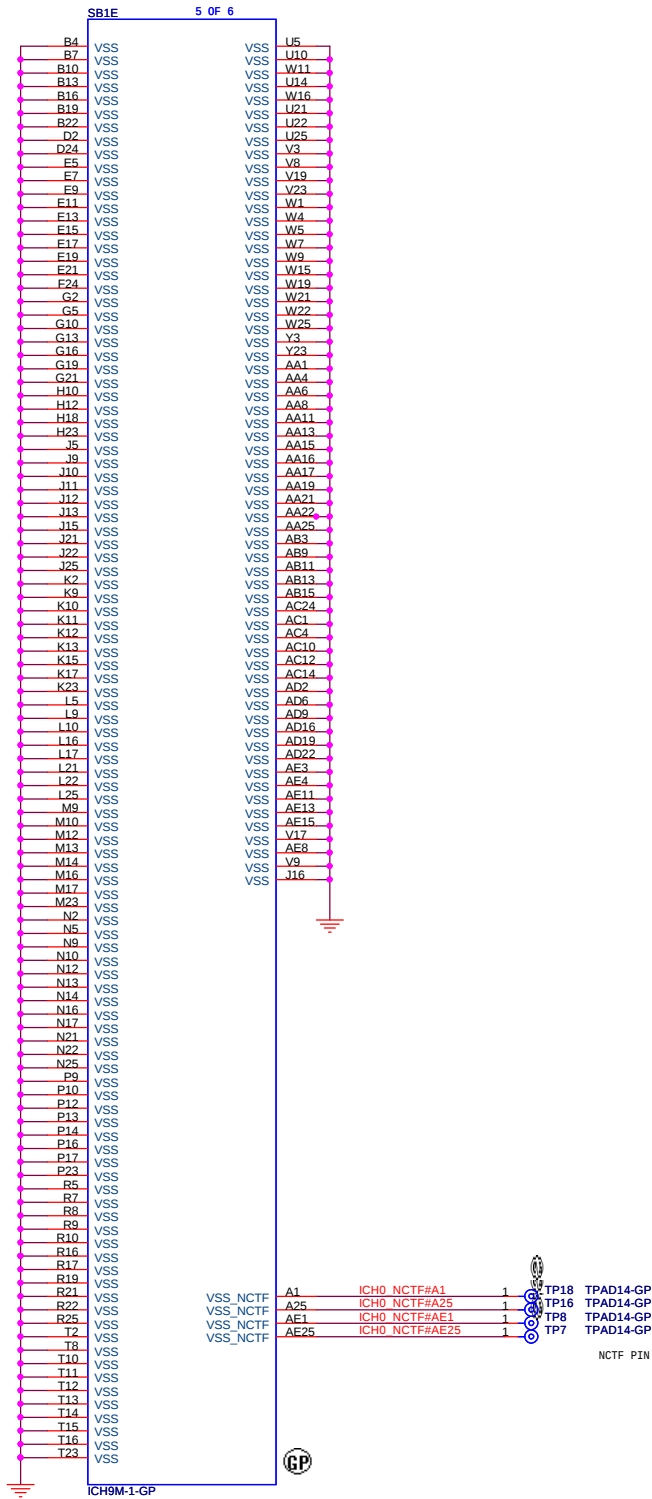
Date: Tuesday, April 28, 2009

Sheet 15 of 48

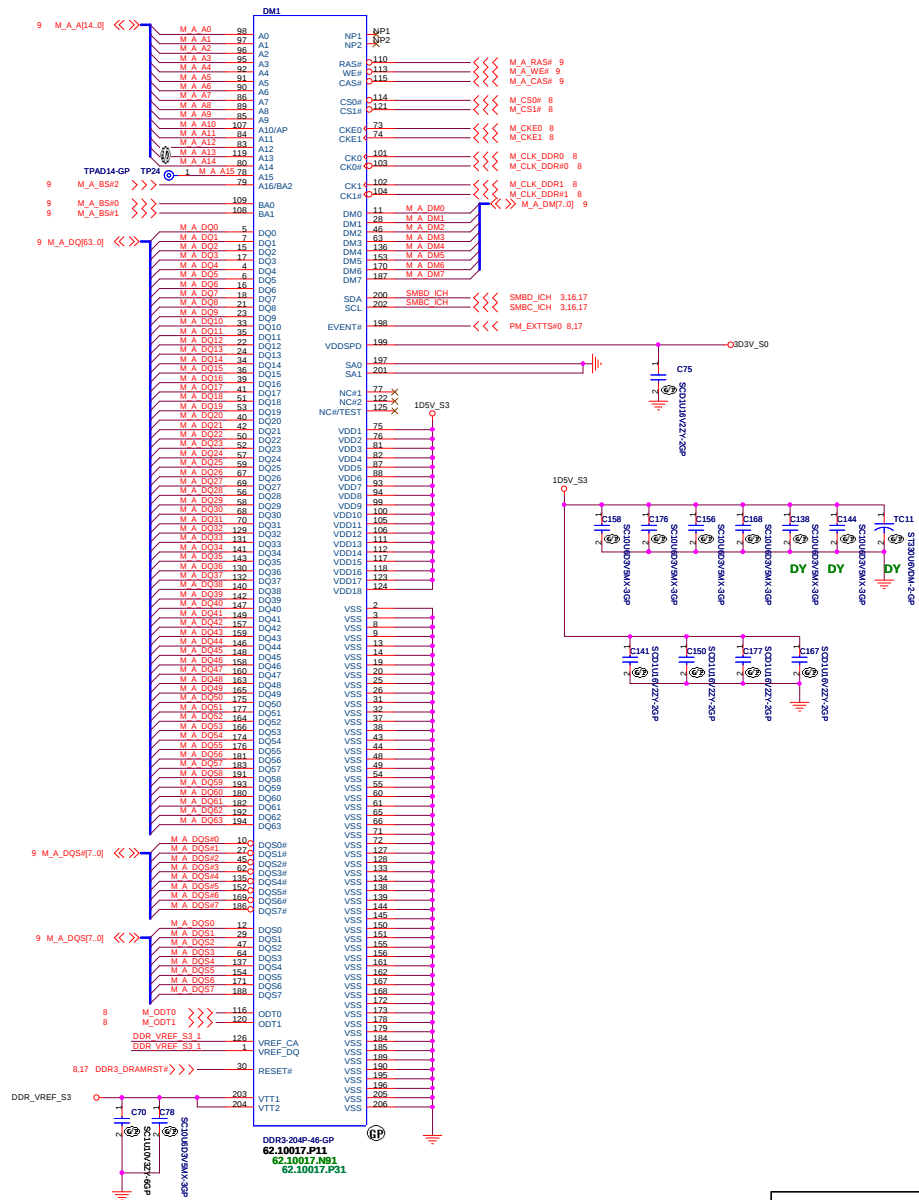
Rev

-2

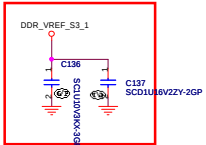
JM41 Discrete



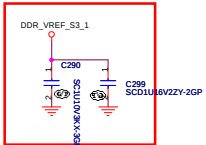
DDR3 SOCKET_2



Layout Note : Near Pin 126

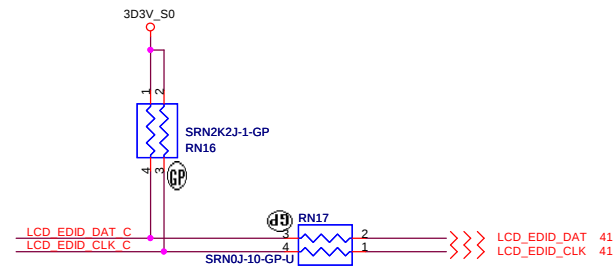
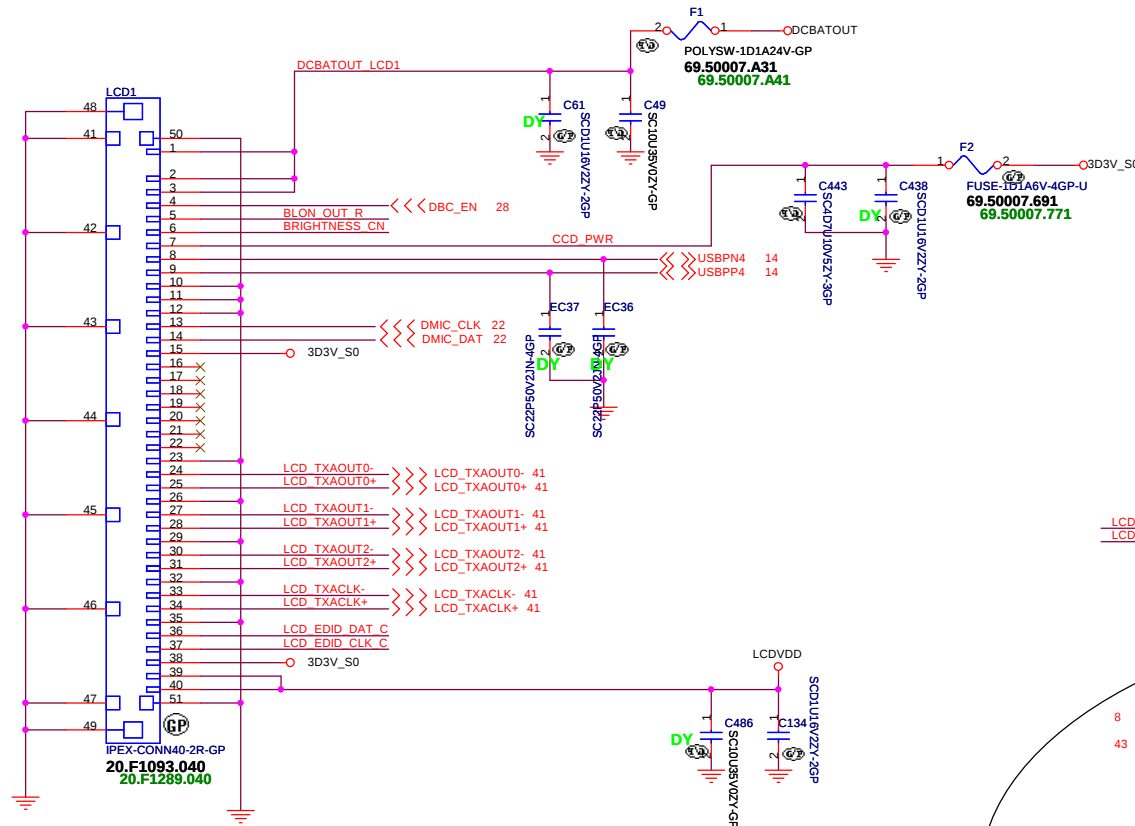


Layout Note : Near Pin 1

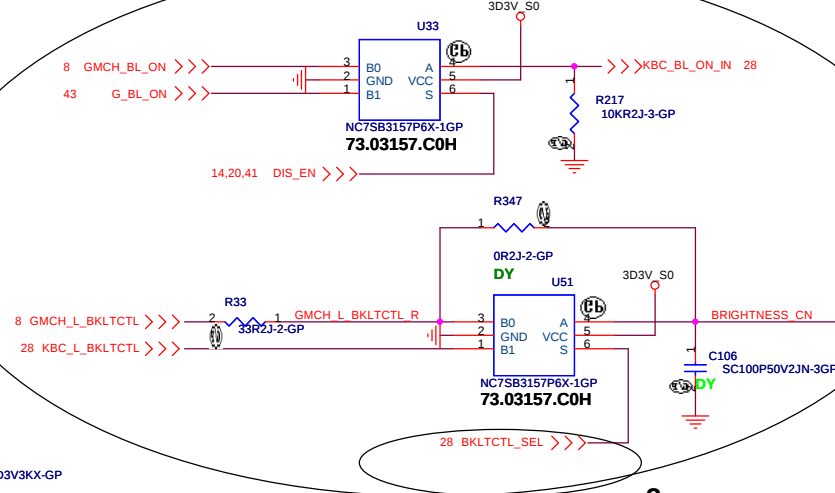


LCD/CCD CONN

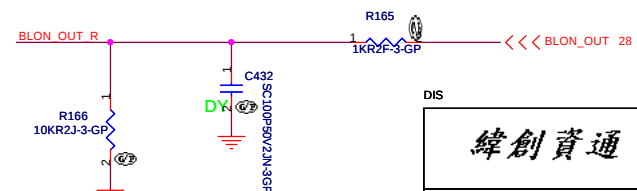
Internal MIC



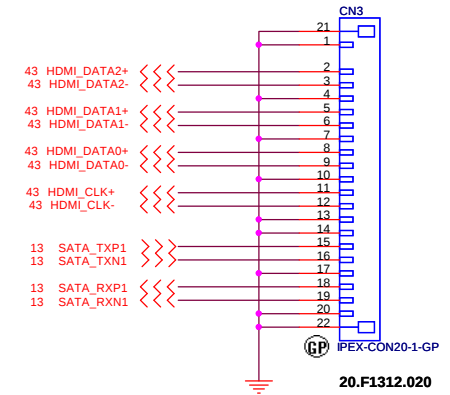
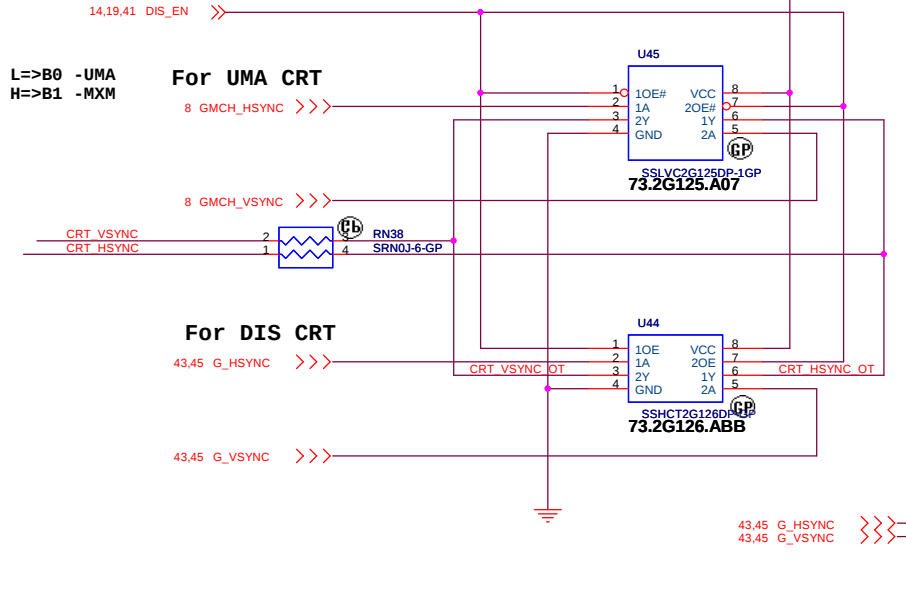
-1



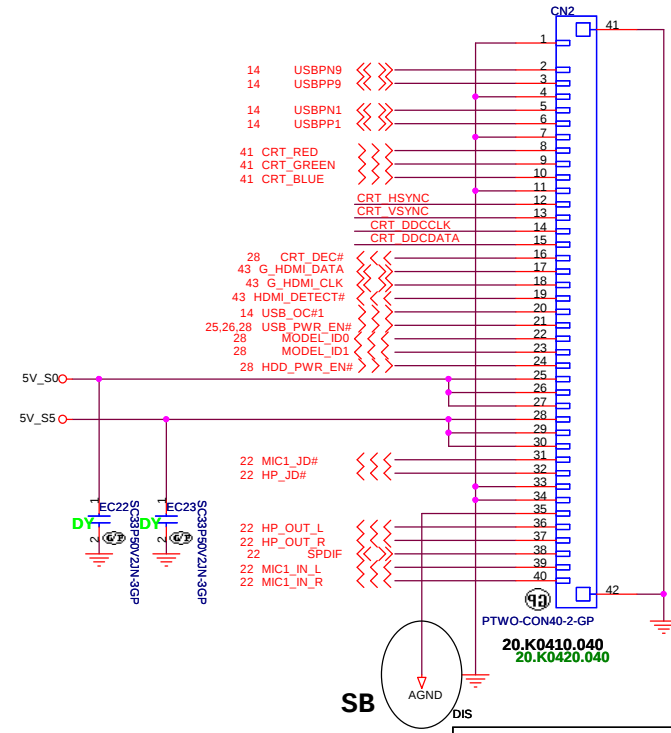
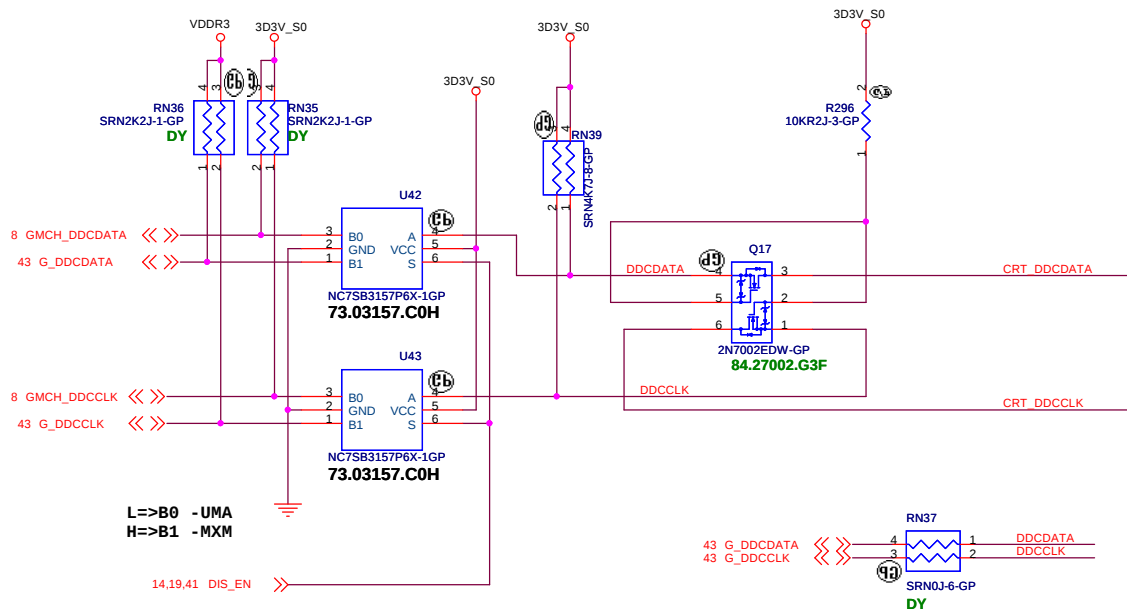
-2



Hsync & Vsync level shift

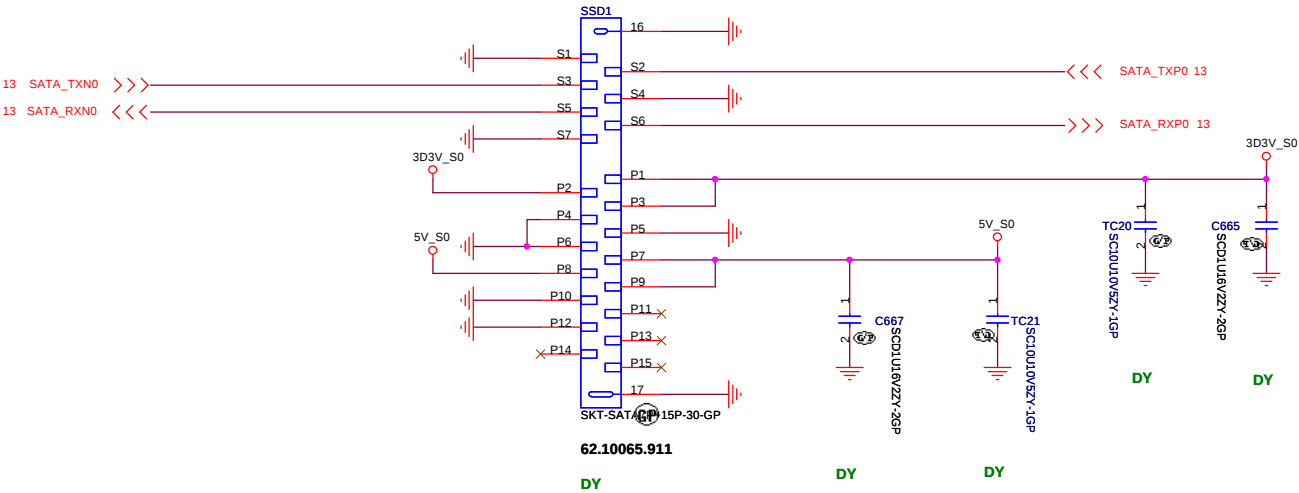


DDC_CLK & DATA level shift

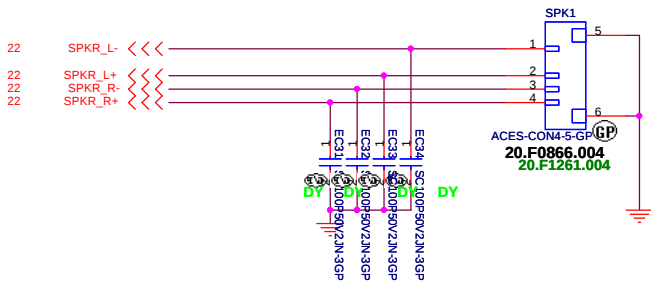


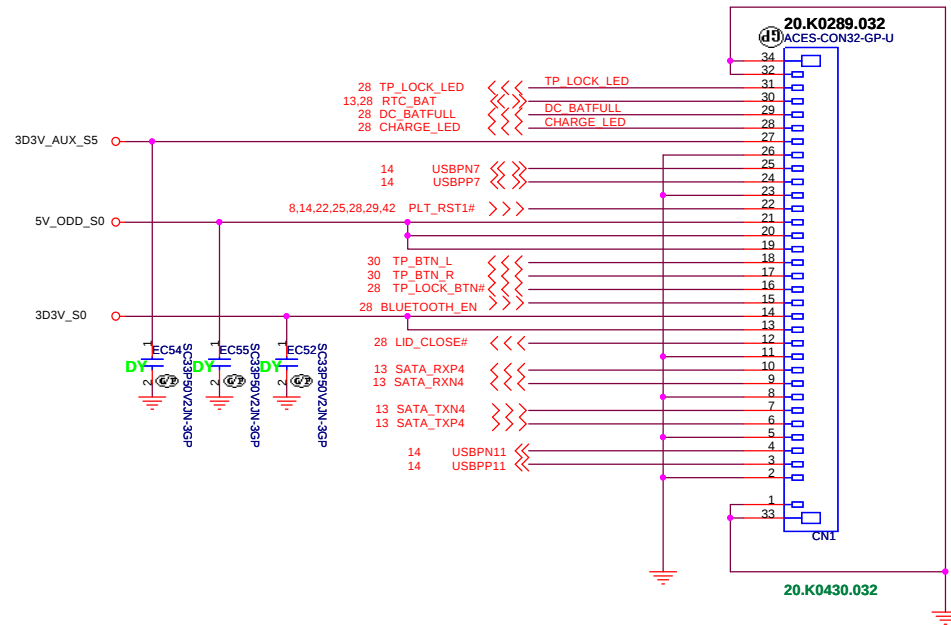
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

SSD SATA Connector



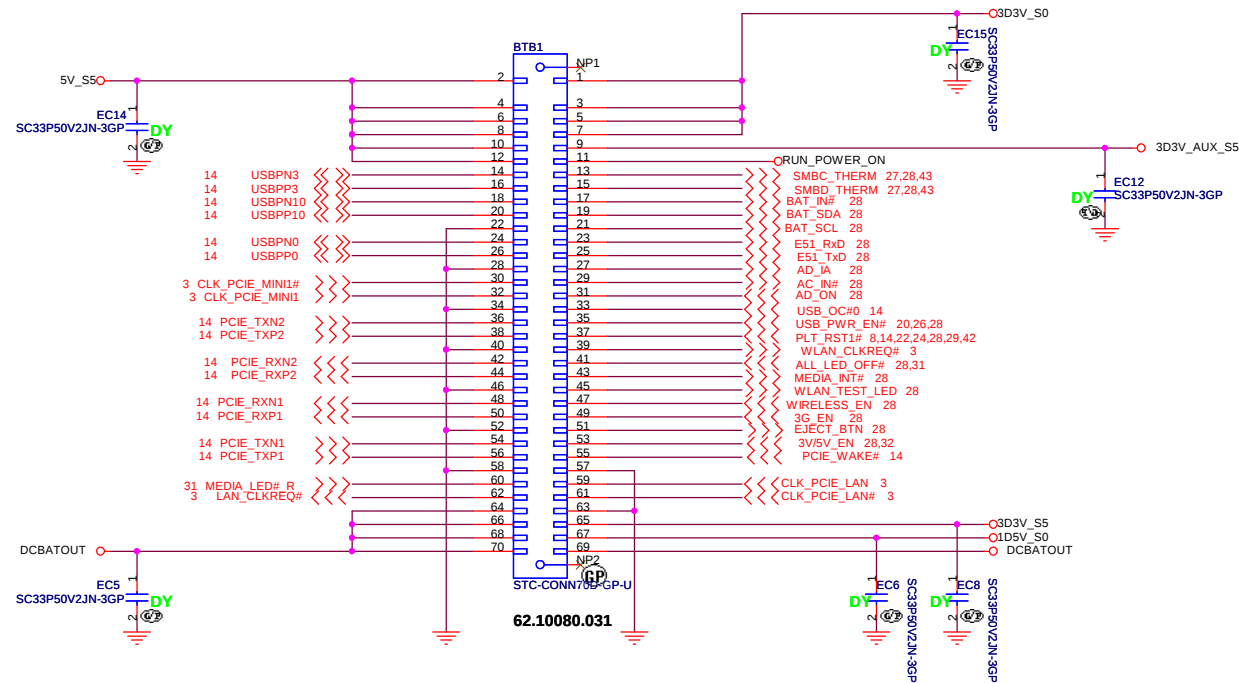
Internal Speaker





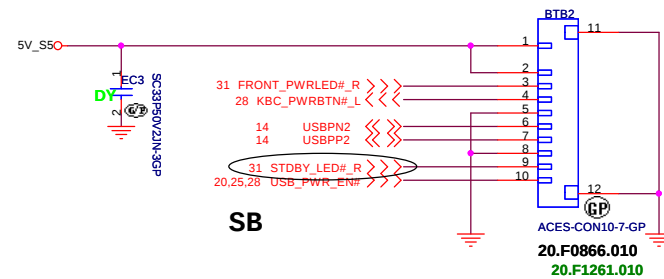
DIS

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CARDREADER BD CONN			
Size	Document Number	Rev	
		JM41 Discrete -2	
Date: Tuesday, April 28, 2009	Sheet	24	of 48



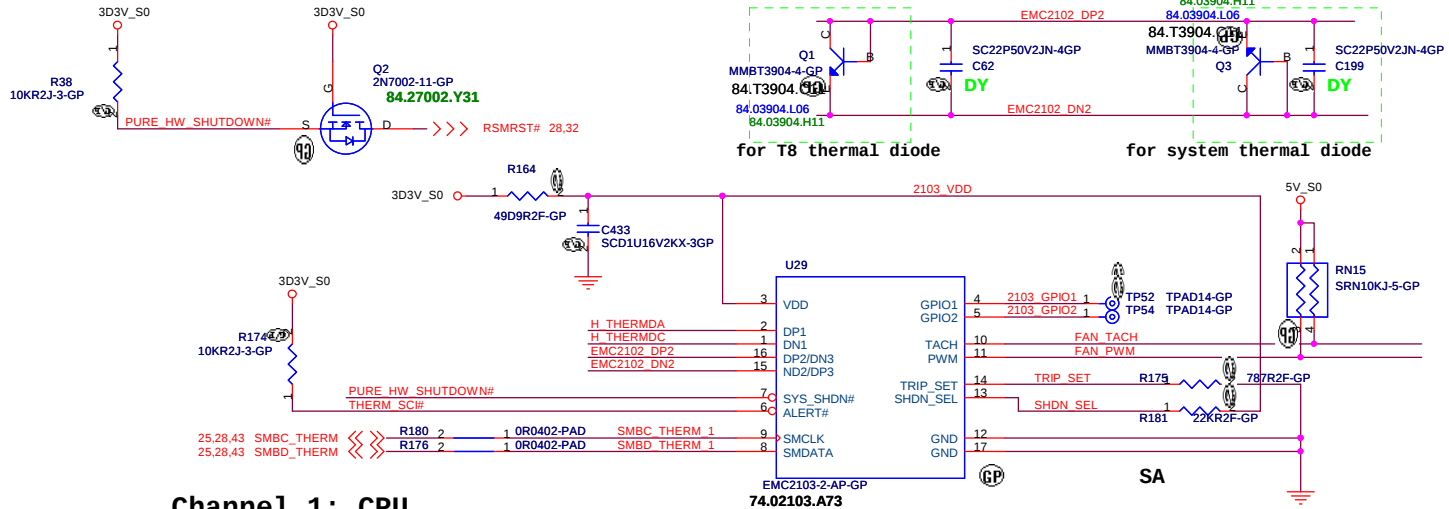
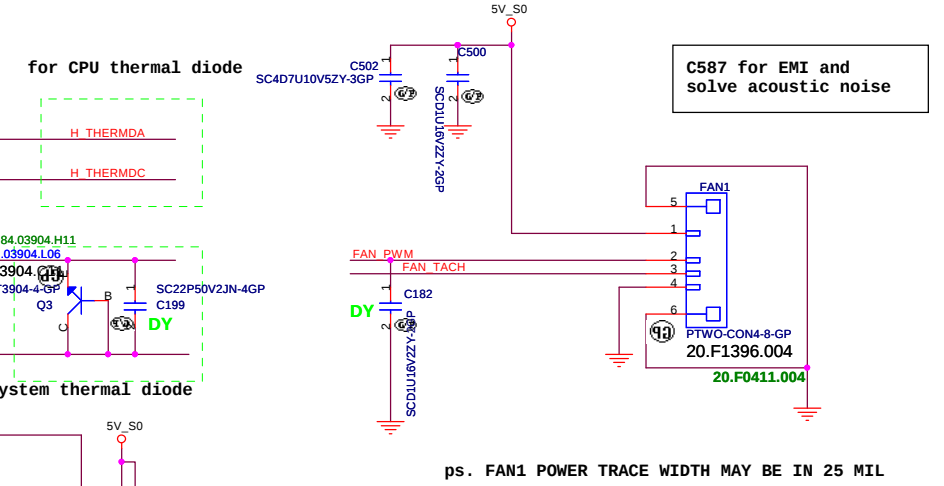
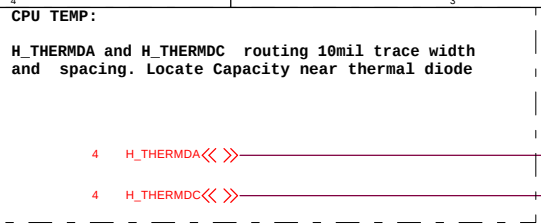
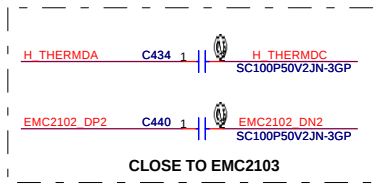
DIS

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
MINI BD CONN			
Size	Document Number	Rev	
A3	JM41_Discrete	-2	
Date:	Tuesday, April 28, 2009	Sheet	25 of 48



DIS

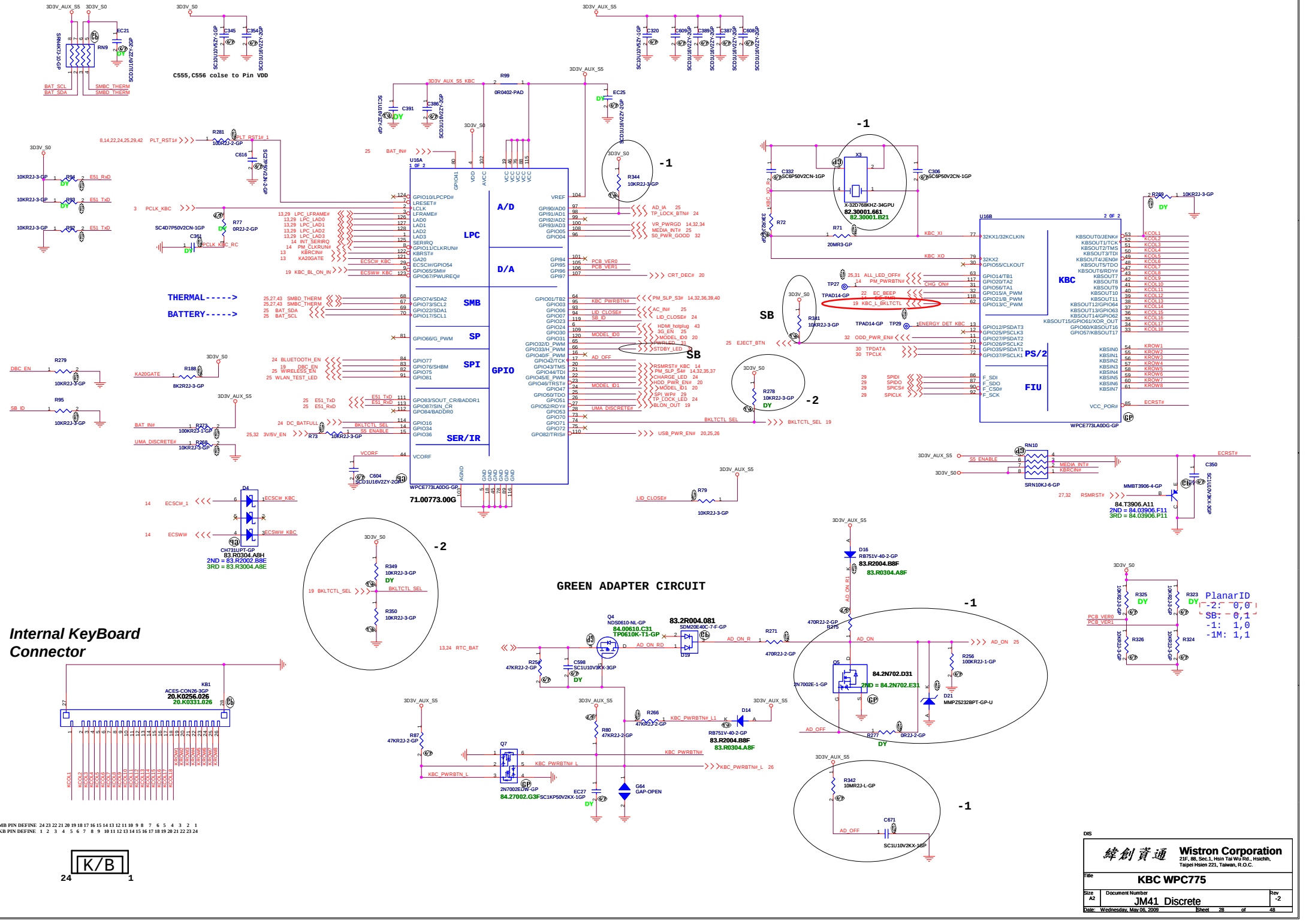
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
POWER BUTTON CONN			
Size A3	Document Number JM41_Discrete		Rev -2
Date:	Tuesday, April 28, 2009	Sheet	26 of 48



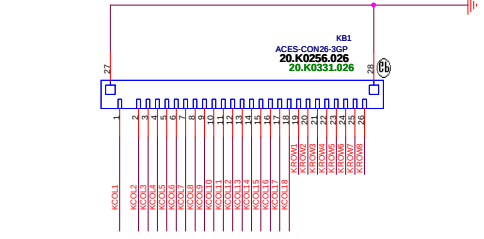
Channel 1: CPU
Channel 2: Palmrest
Channel 3: T8

SHDN SEL	
PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED, REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED, REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED

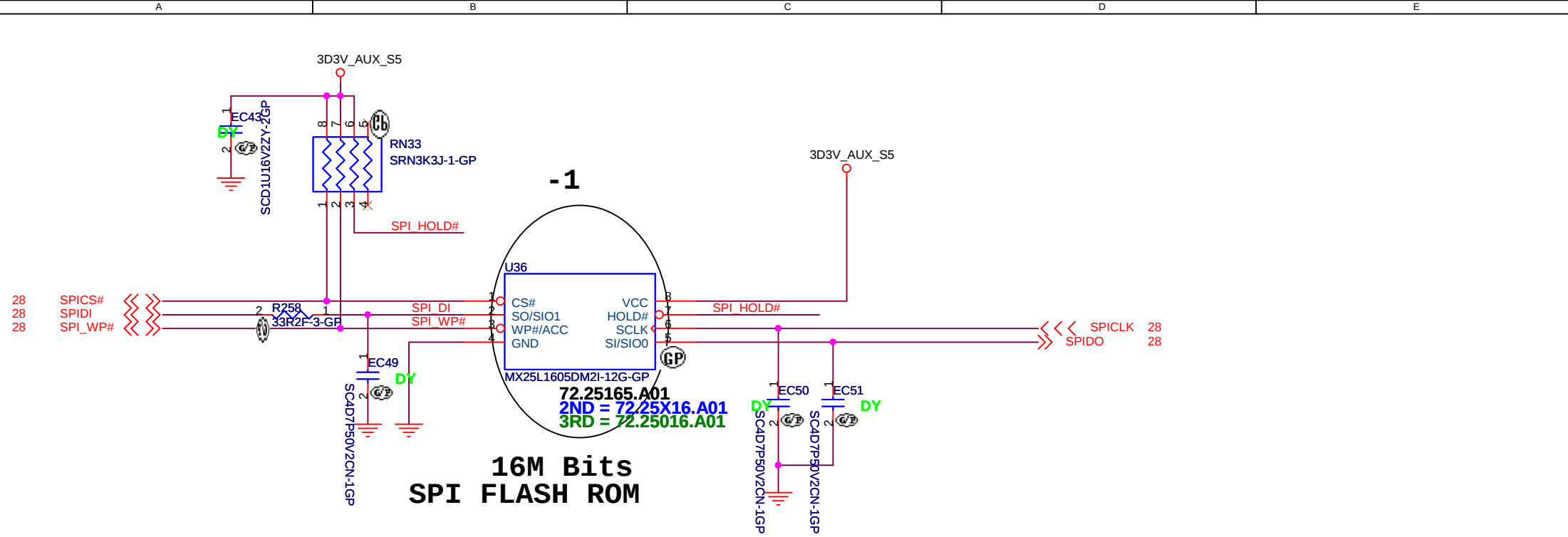
TRIP SET	
Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100



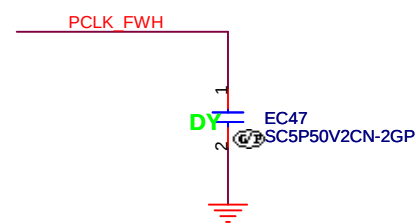
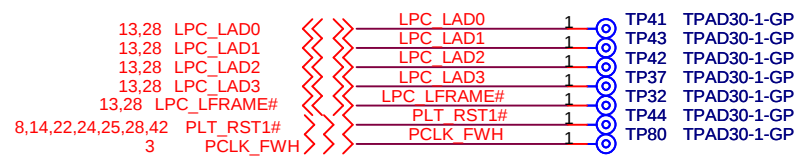
Internal KeyBoard Connector



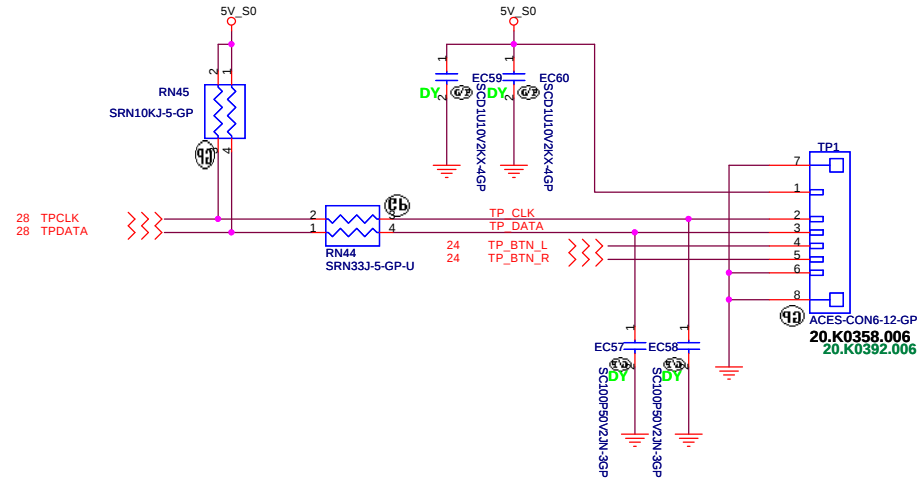
MB PIN DEFINE	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
KB PIN DEFINE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24



GOLDEN FINGER FOR DEBUG BOARD

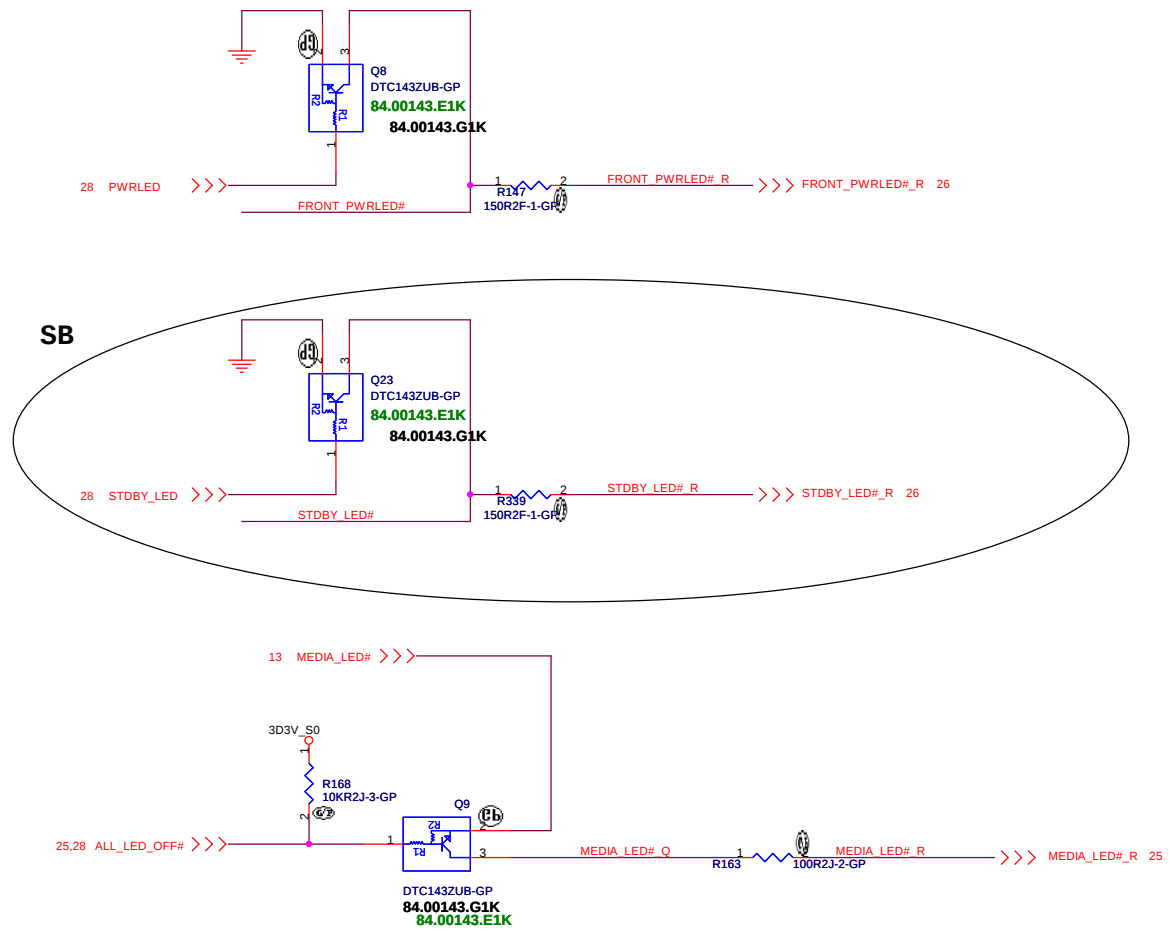


TOUCH PAD

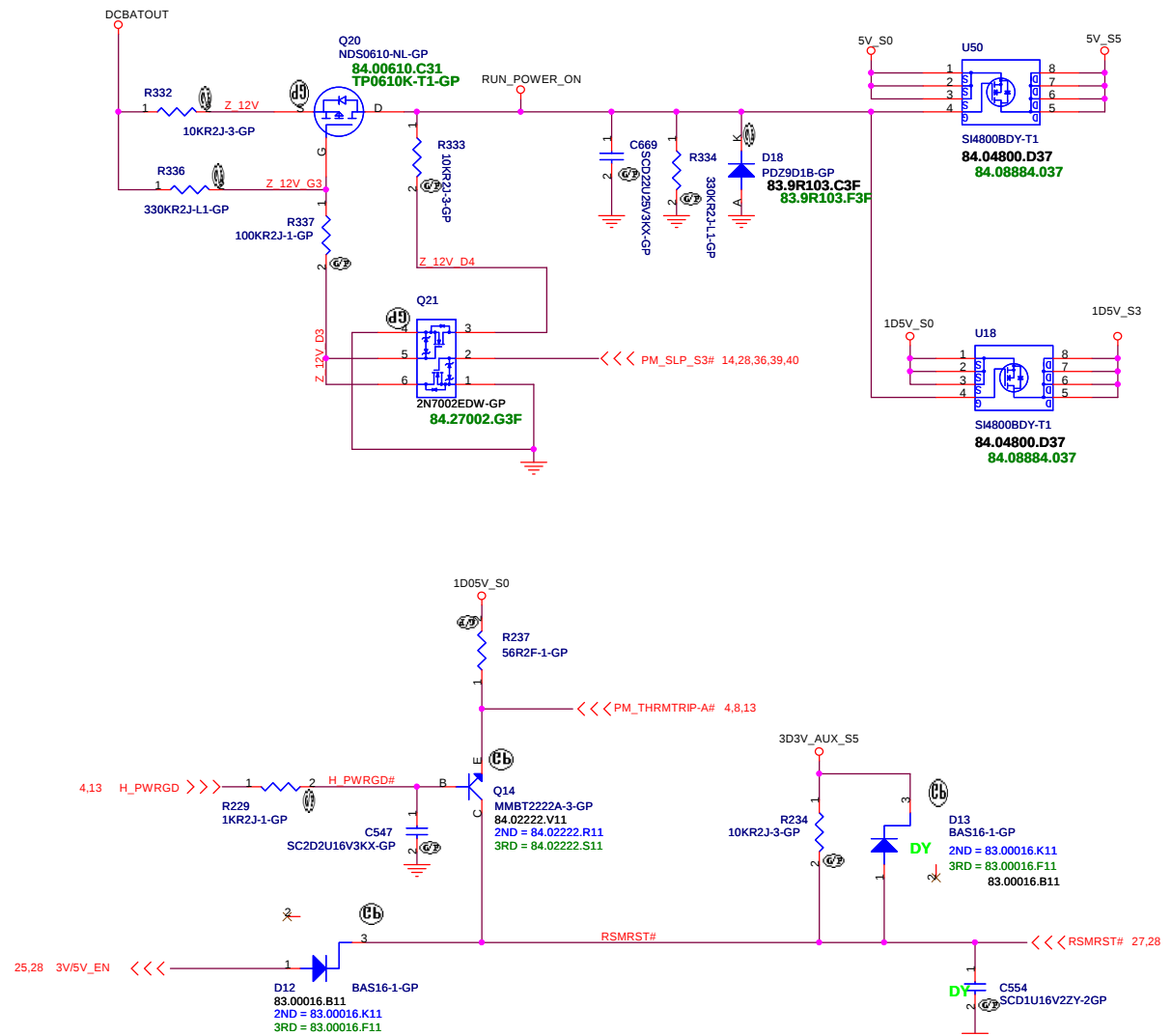


DIS

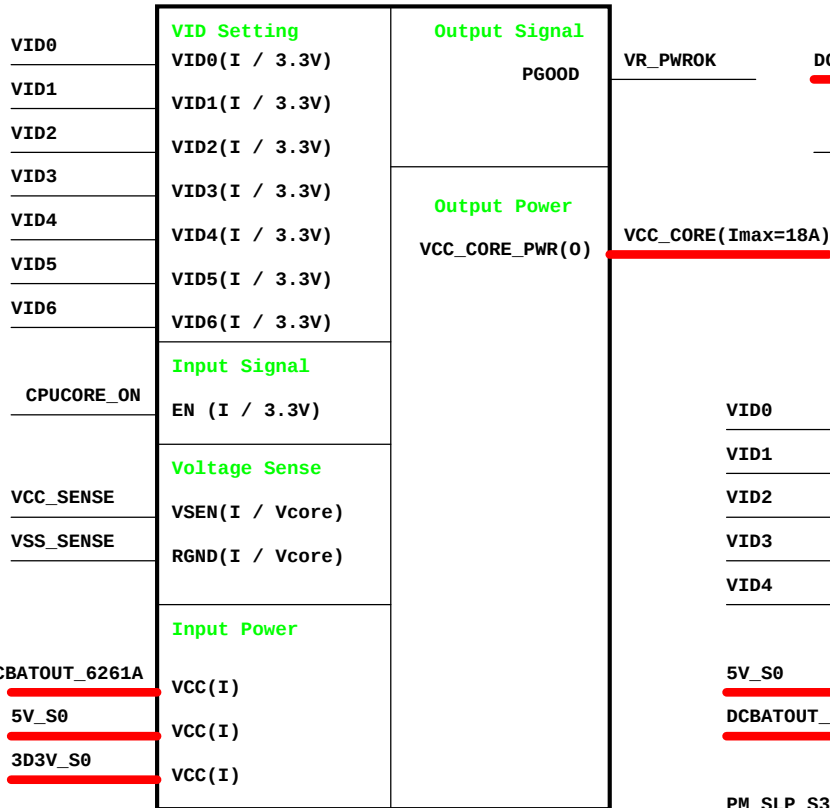
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Touch PAD			
Size	Document Number		Rev
	JM41 Discrete		-2
Date: Tuesday, April 28, 2009		Sheet 30 of 48	



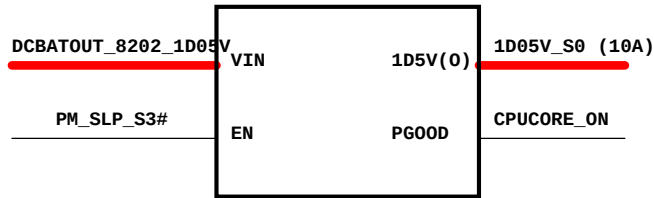
Run Power



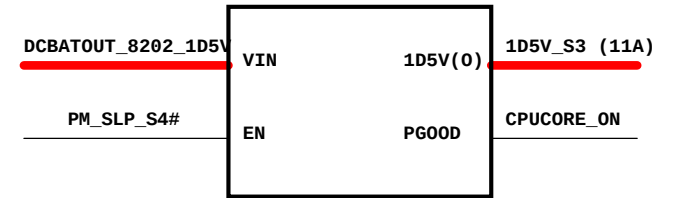
CPU_CORE
ISL6261A



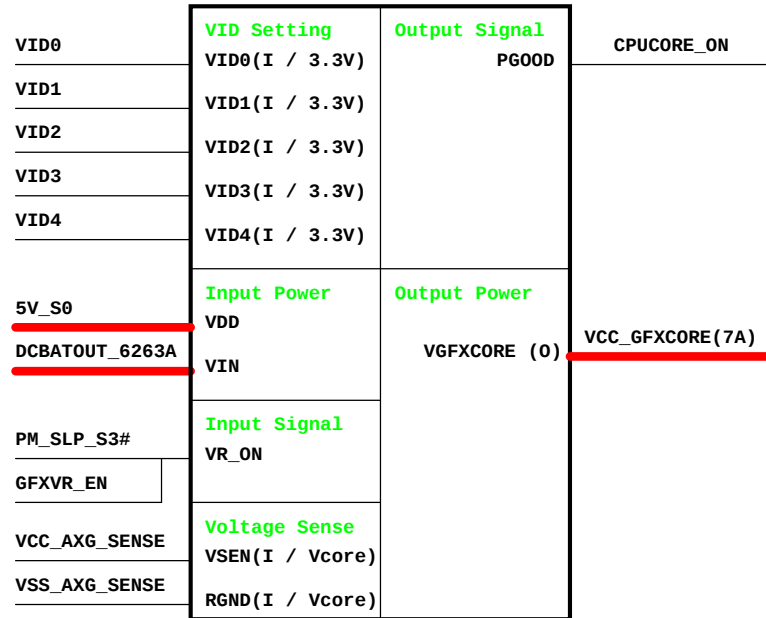
RT8202 1D05V_S0



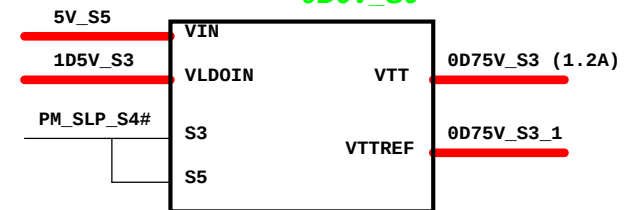
RT8202 1D5V_S3



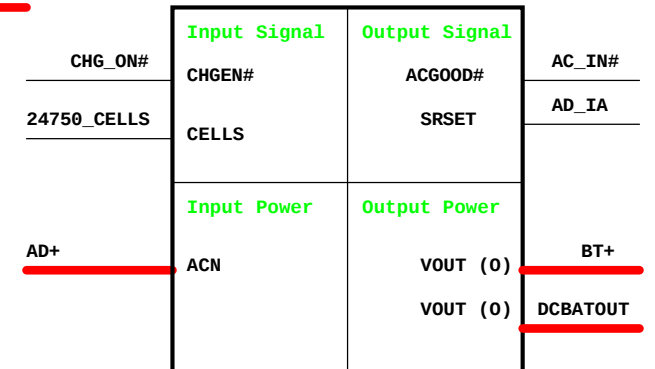
GFX_CORE
ISL6263A



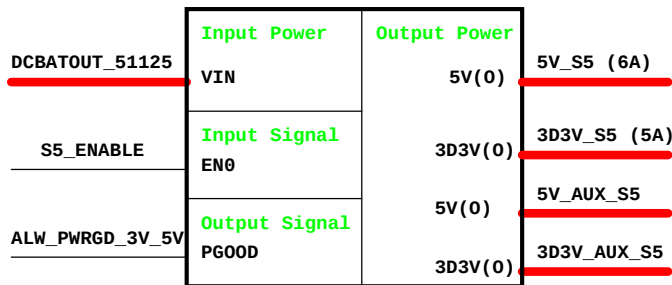
RT9026 0D9V_S0



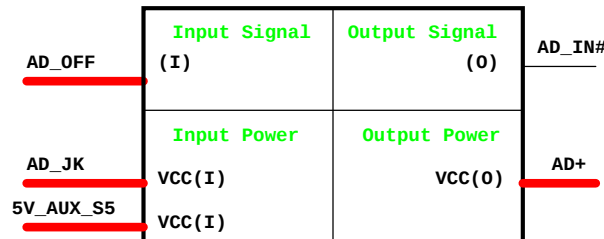
Charger MAX8731A



TPS51125
5V/3D3V

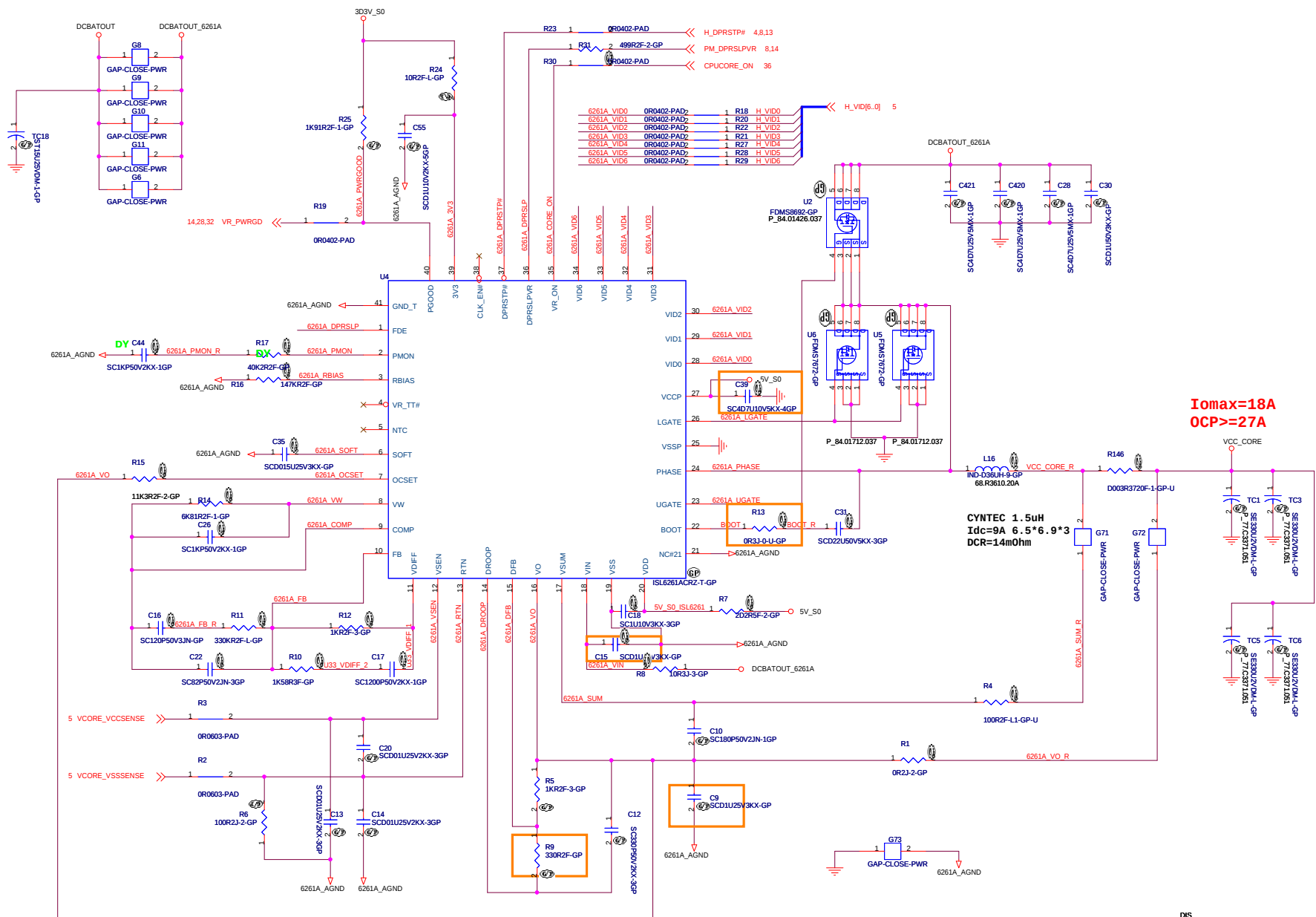


Adapter



緯創資通

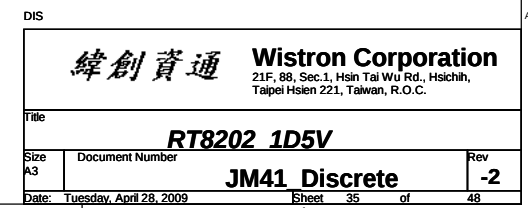
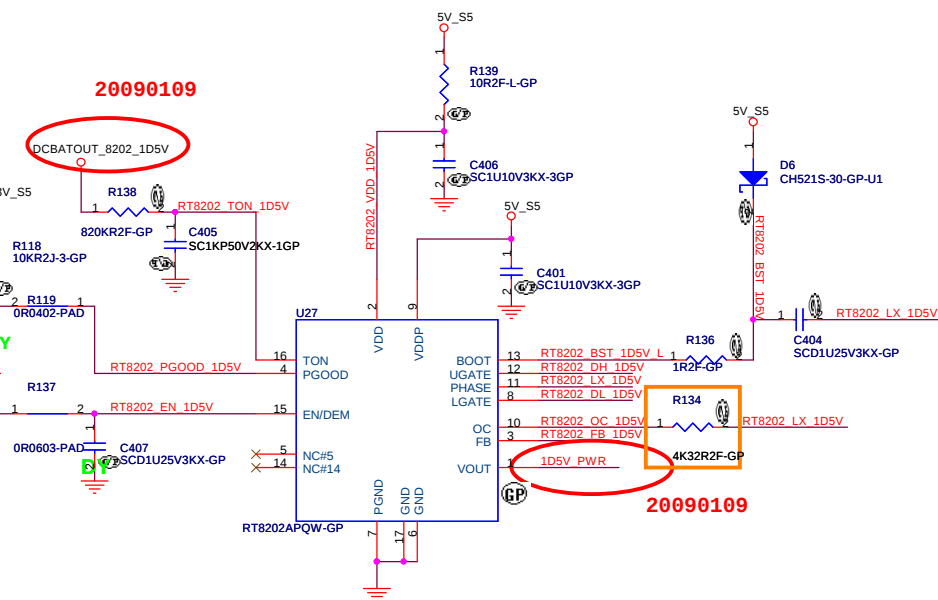
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

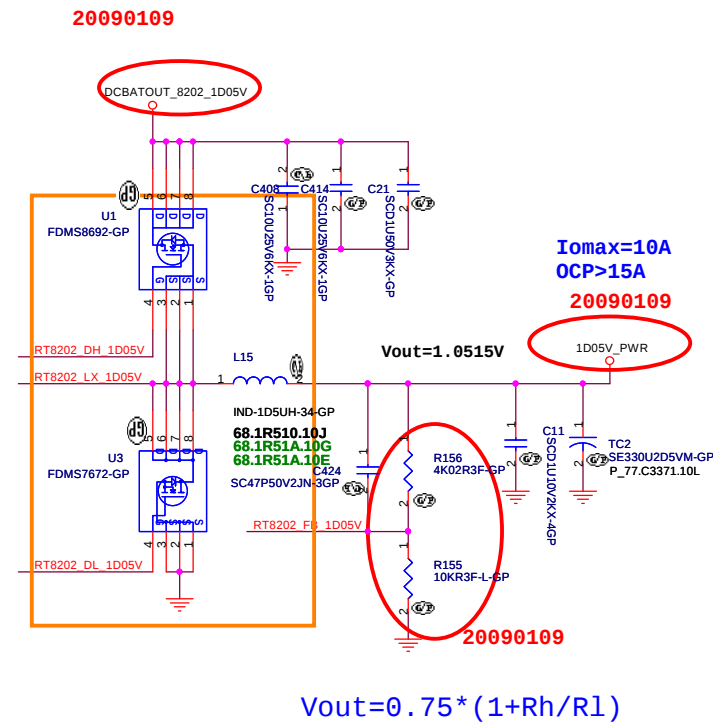
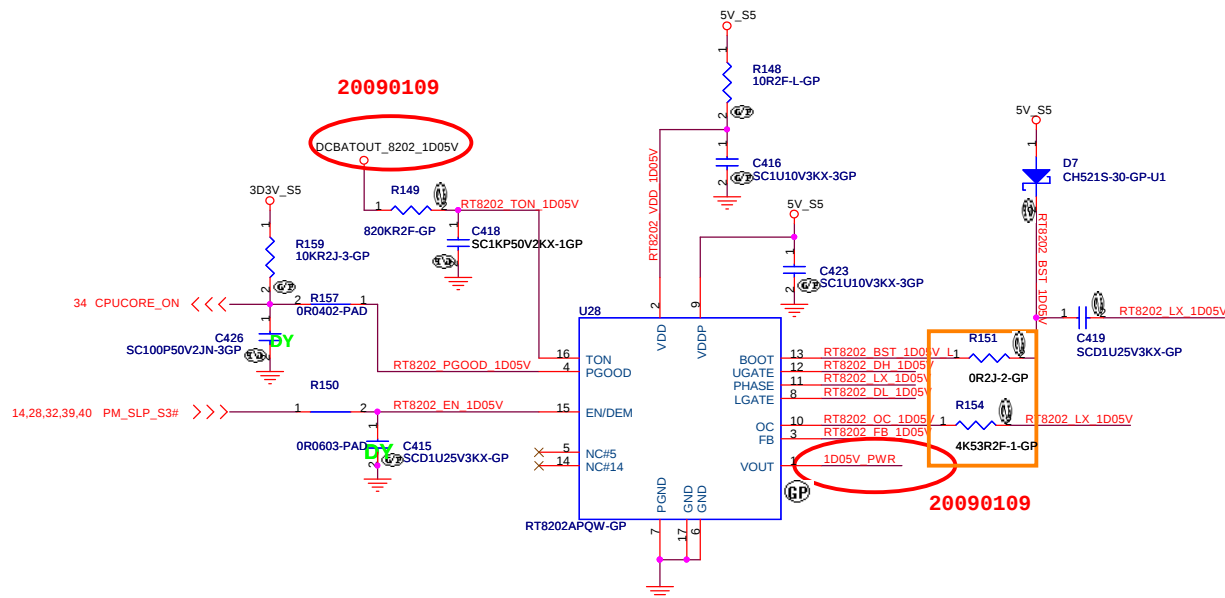
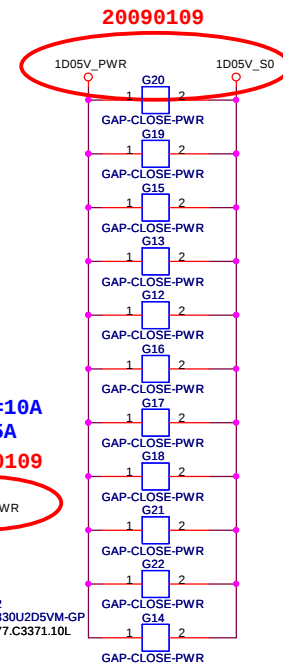
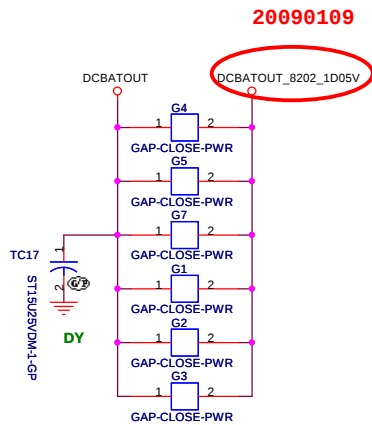


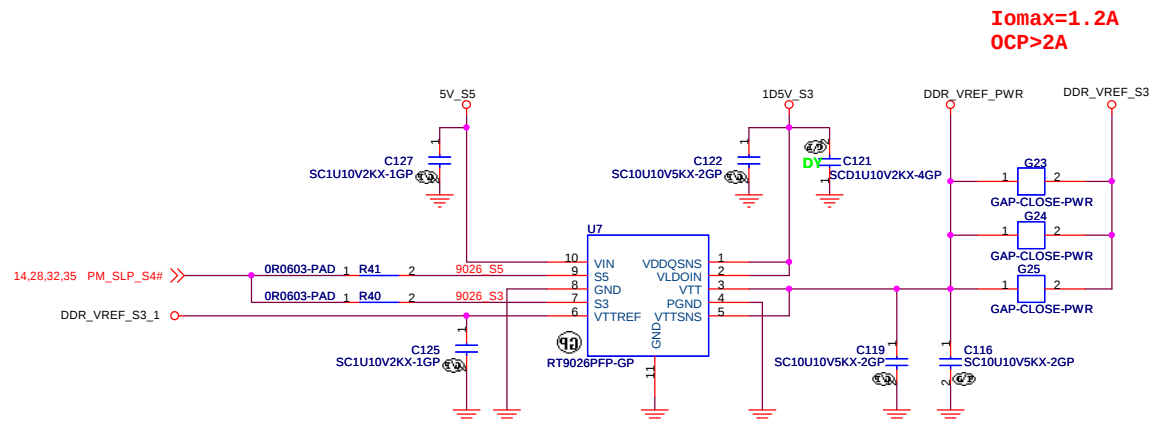
DIS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title ISL6261A CPU CORE
Size Custom Document Number JM41 Discrete
Date: Tuesday, April 28, 2009 Sheet 34 of 48 Rev -2

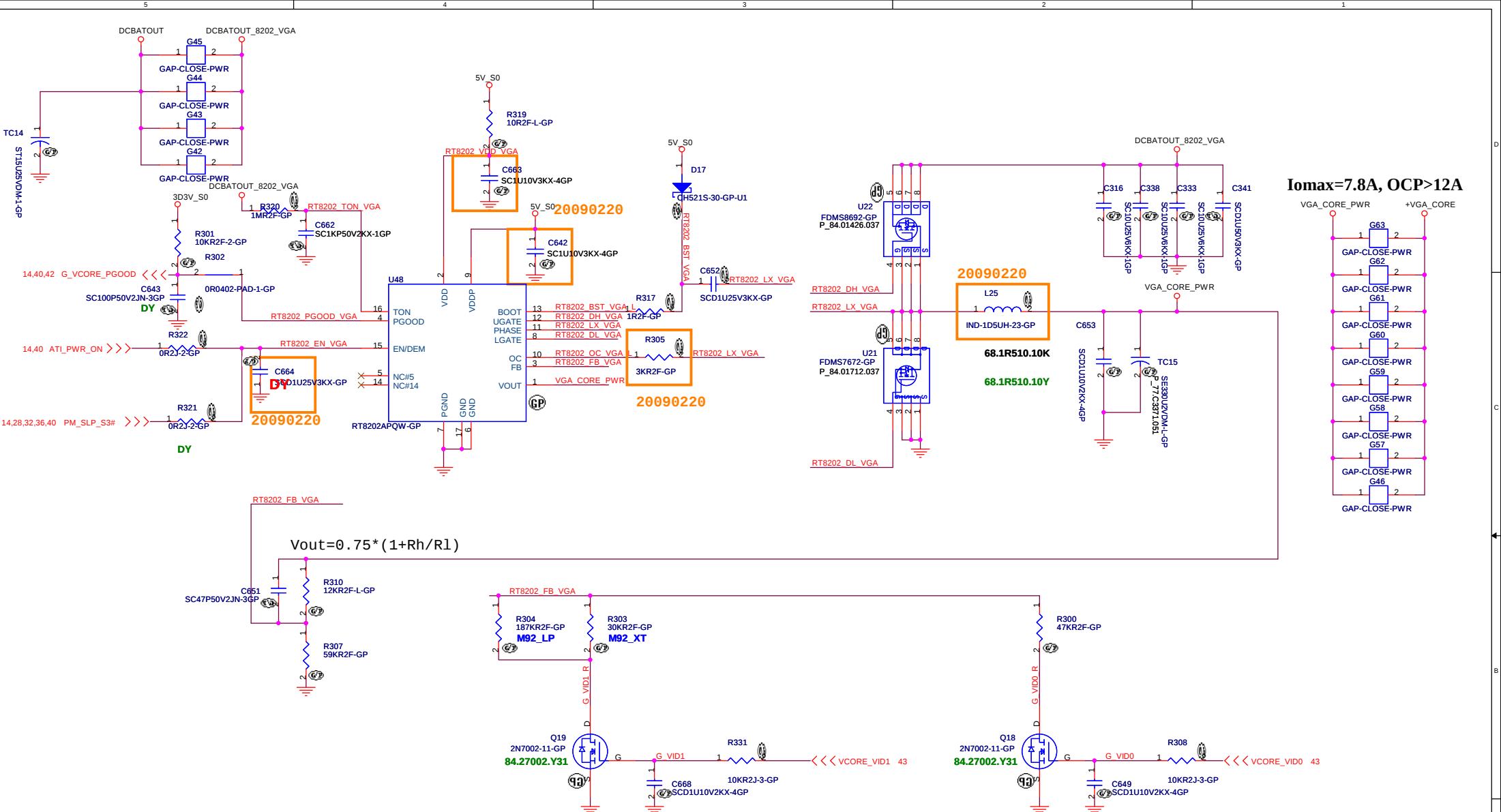






DIS

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
RT9026 0D75V			
Size	Document Number	Rev	
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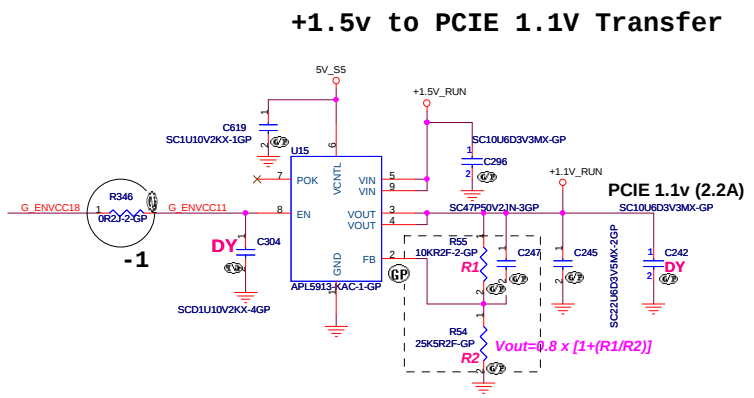
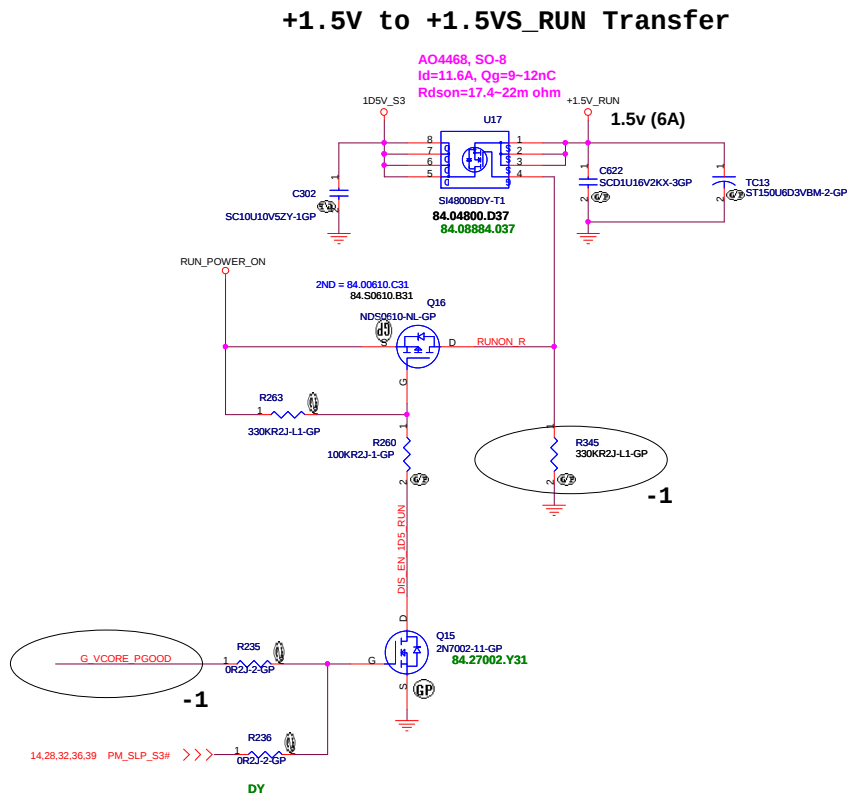
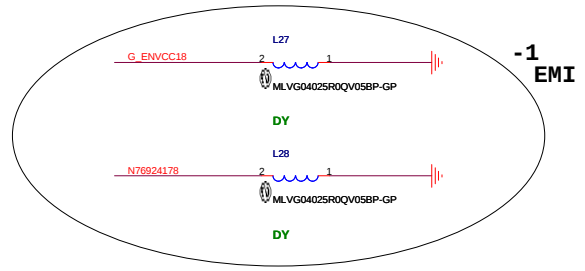
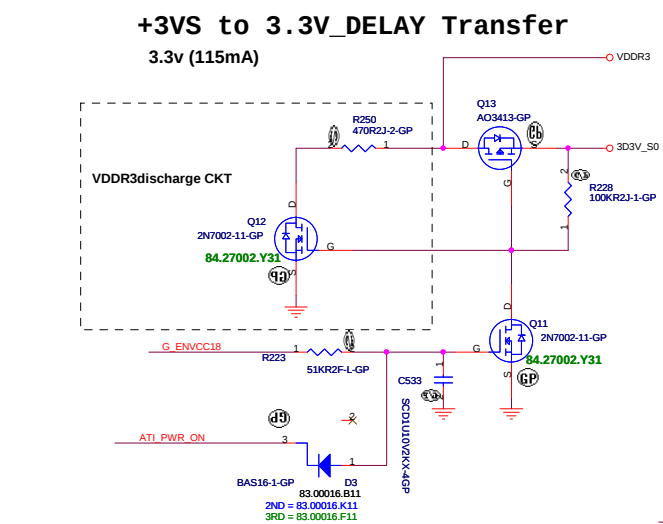
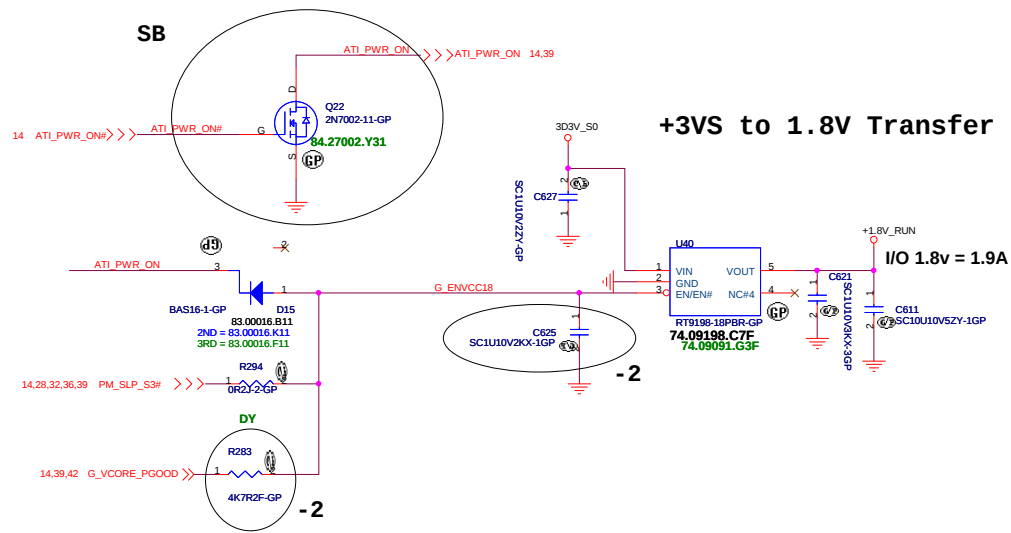
$$V_{out} = 0.75 * (1 + R_h / R_l)$$

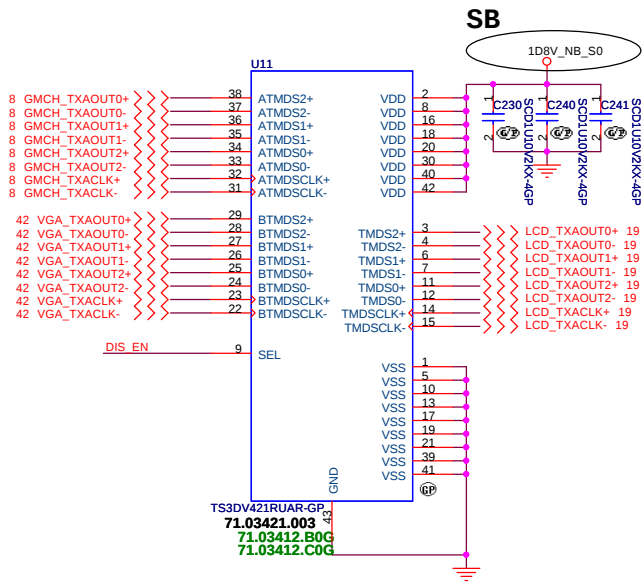
M92_LP core power

ALTV1	ALTV0	Vout
0	0	0.90V
0	1	1.09V
1	0	0.95V

M92_XT core power

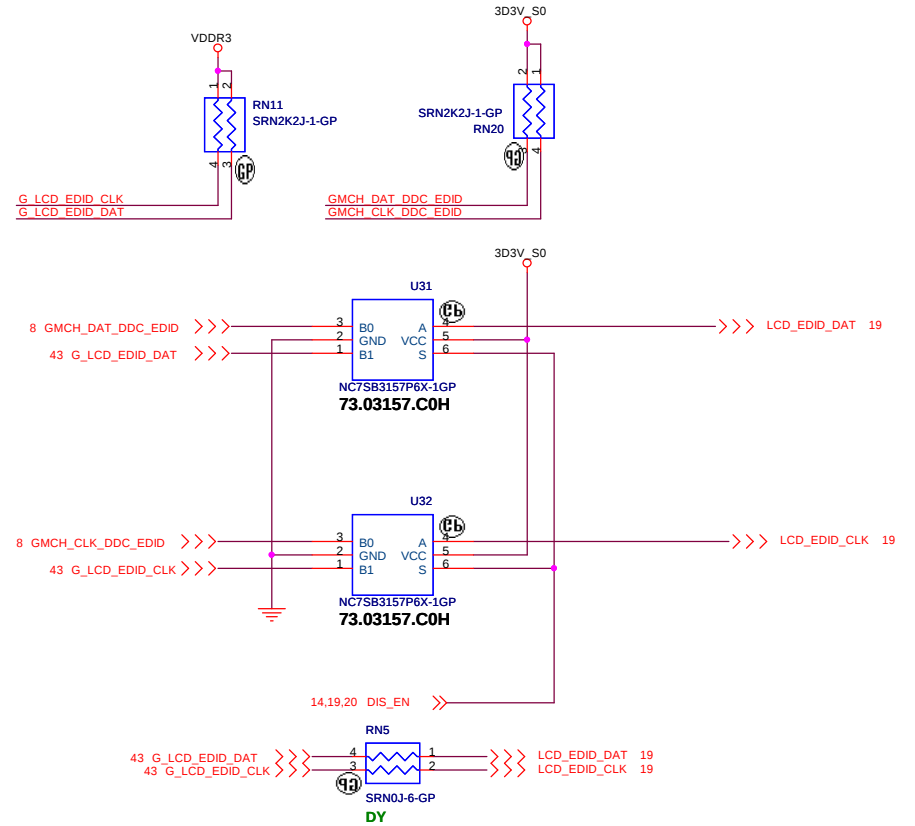
ALTV1	ALTV0	Vout
0	0	0.90V
0	1	1.09V
1	0	1.2V



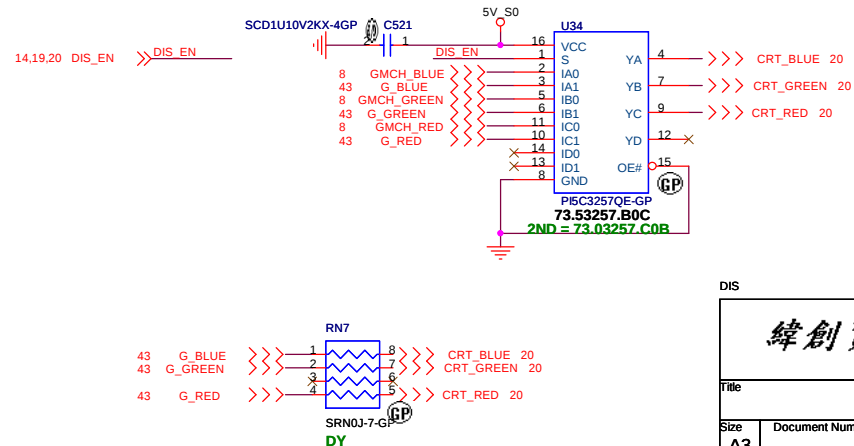
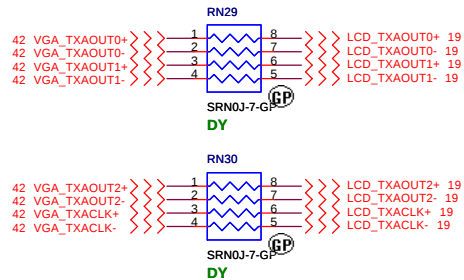


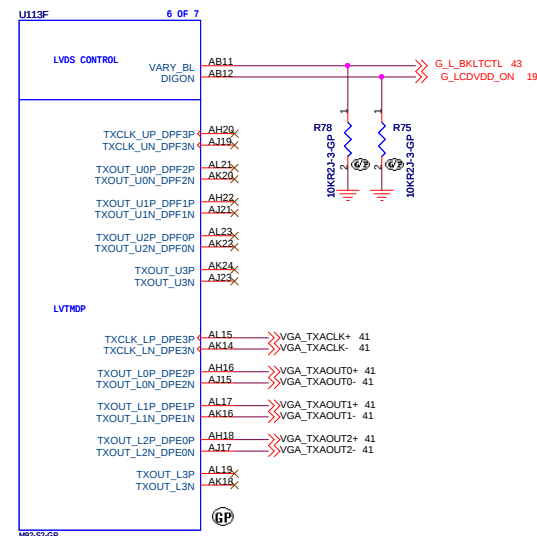
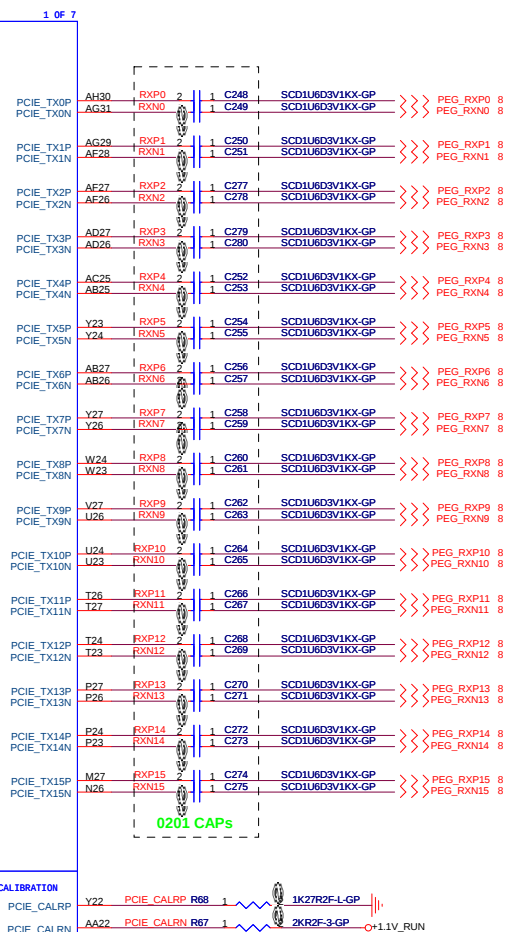
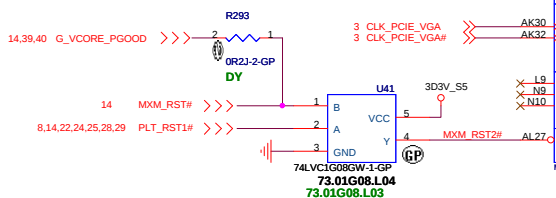
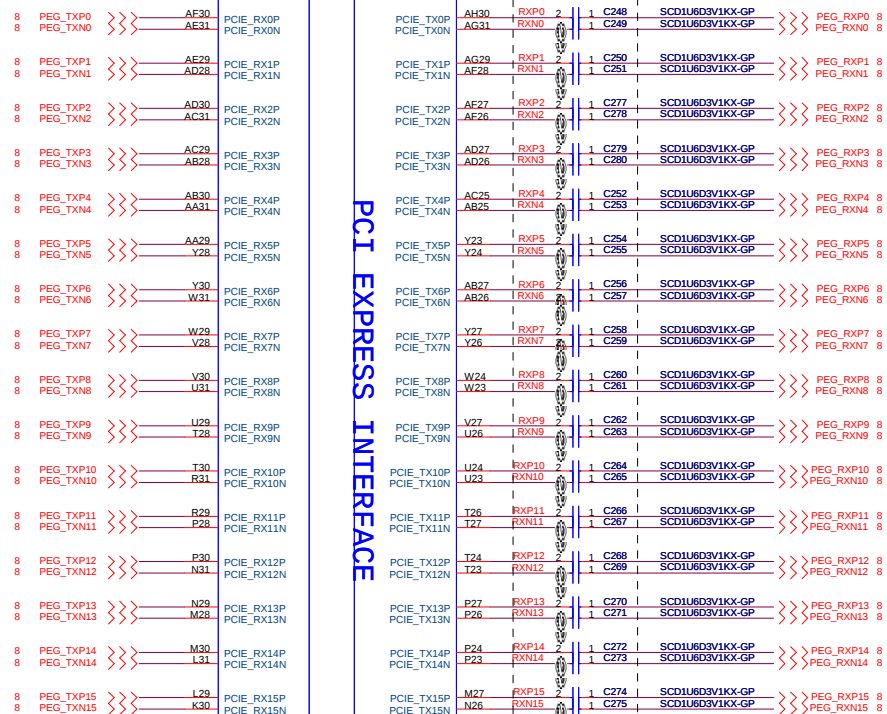
FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMSn+ = ATMDSn+ TMSn- = ATMDSn- TMSCLK+ = ATMDSCLK+ TMSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMSn+ TMSn- TMSCLK+ TMSCLK-
H	TMSn+ = BTMDSn+ TMSn- = BTMDSn- TMSCLK+ = BTMDSCLK+ TMSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMSn+ TMSn- TMSCLK+ TMSCLK-



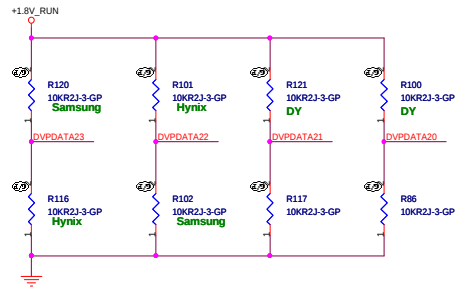
$\bar{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



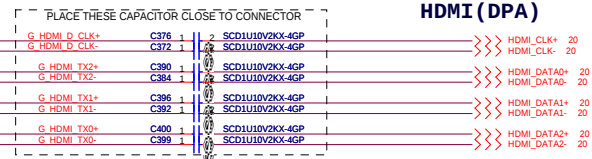
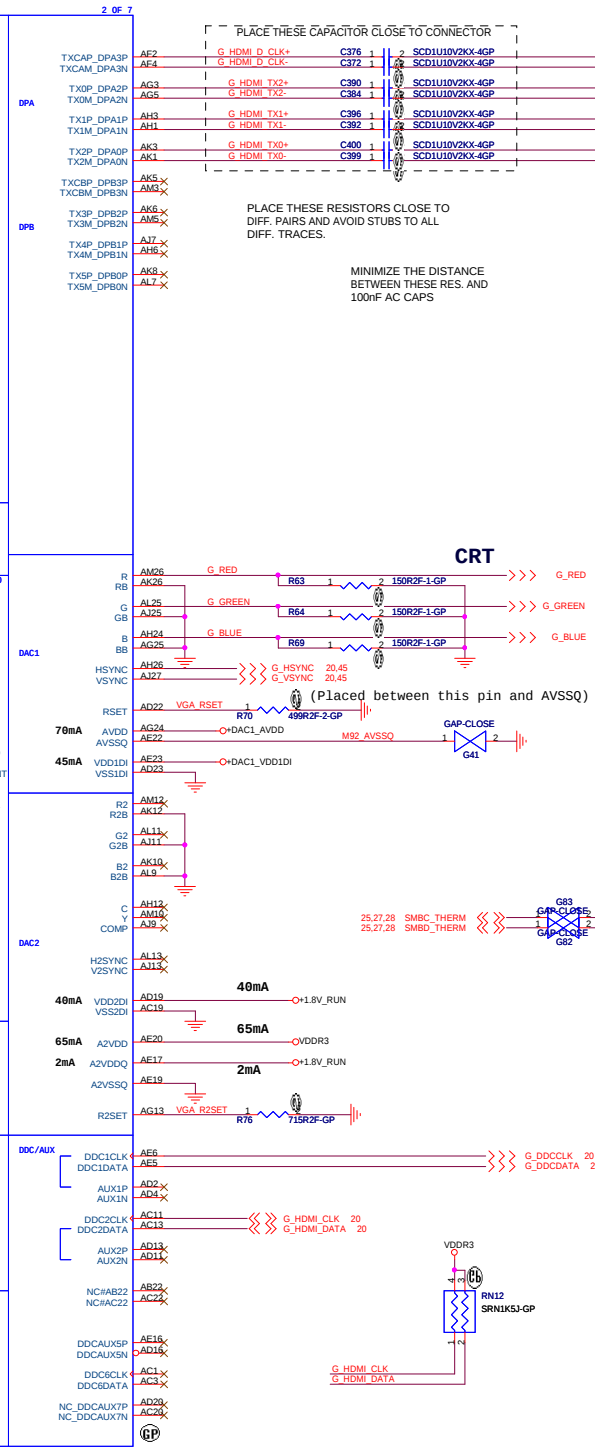
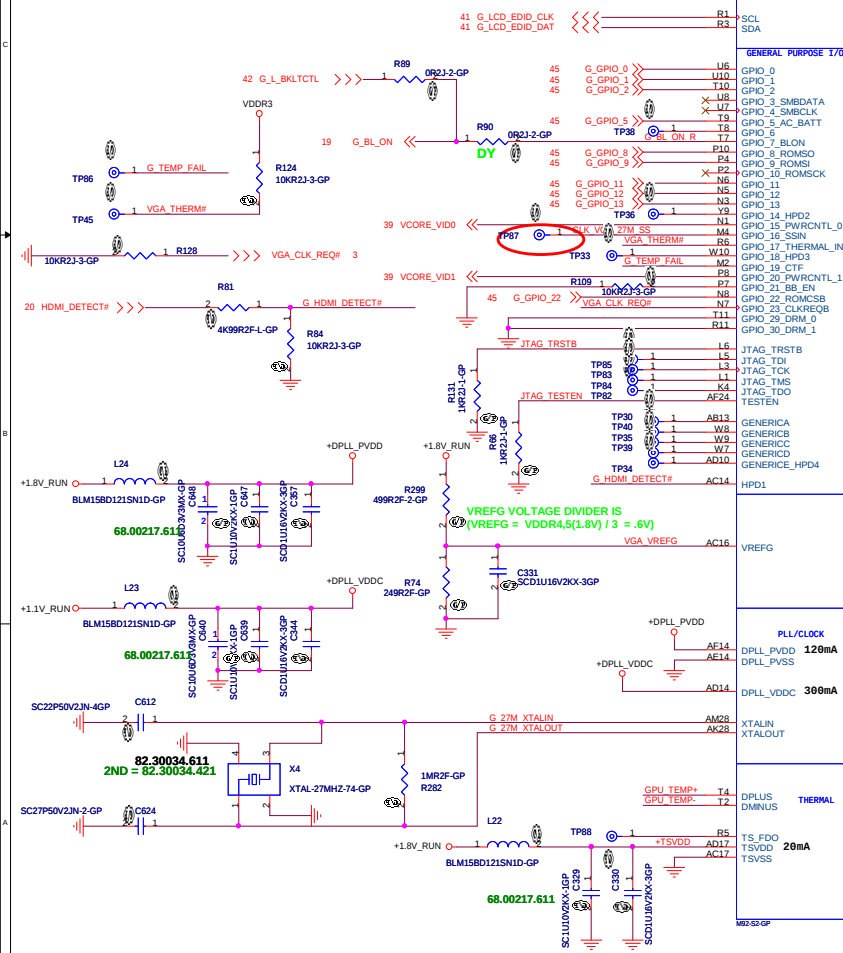


SSID = VIDEO

```
DVPDATA [3:0]
0100 64Mx16 Hynix
1000 64Mx16 Samsung
```

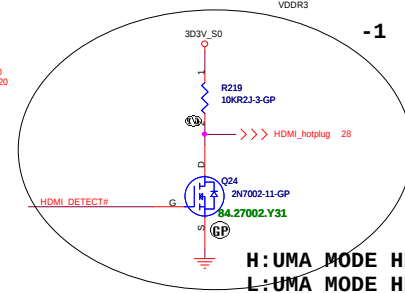
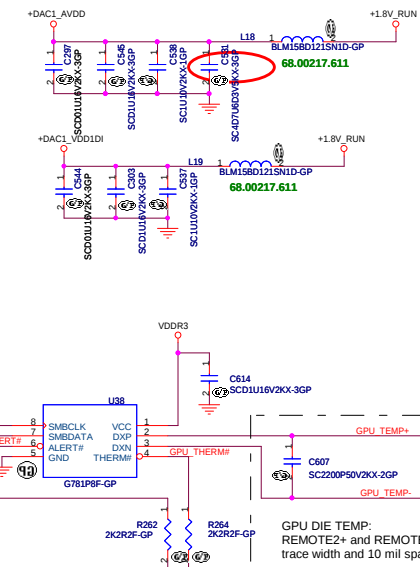


STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(23:20) (Internal PD)	MEMORY TYPE, MAKE AND SIZE INFO
		0000 - GDDR3 16Mx32 Qimonda
		0001 - GDDR3 32Mx32 Hynix
		0010 - GDDR3 32Mx32 Qimonda
		0011 - GDDR3 32Mx32 Samsung



PLACE THESE RESISTORS CLOSE TO
DIFF. PAIRS AND AVOID STUBS TO ALL
DIFF. TRACES.

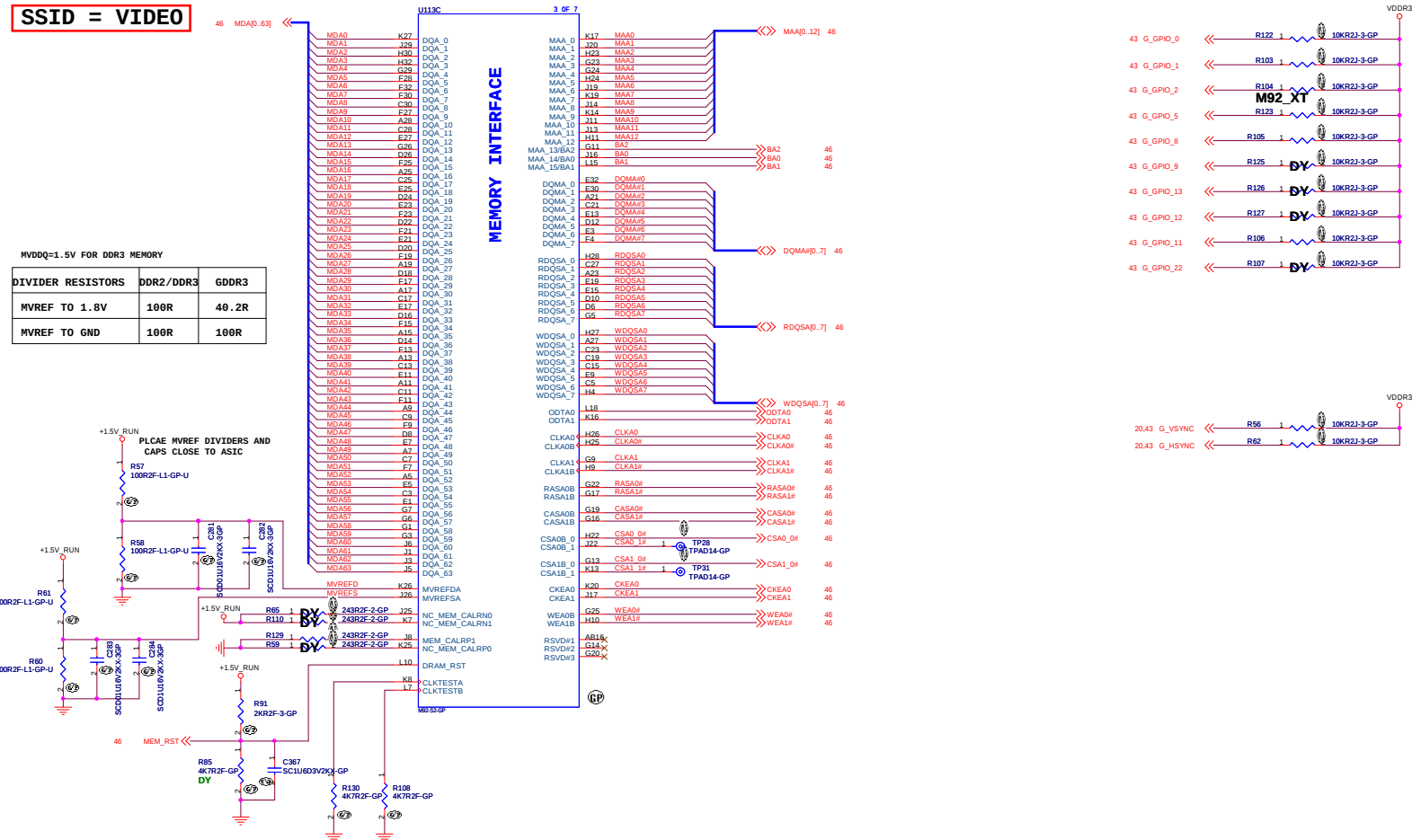
MINIMIZE THE DISTANCE
BETWEEN THESE RES. AND
100nF AC CAPS



```
H:UMA MODE HDMI PLUG_OUT
L:UMA MODE HDMI PLUG_IN
```

[illegible]

SSID = VIDEO



ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESE

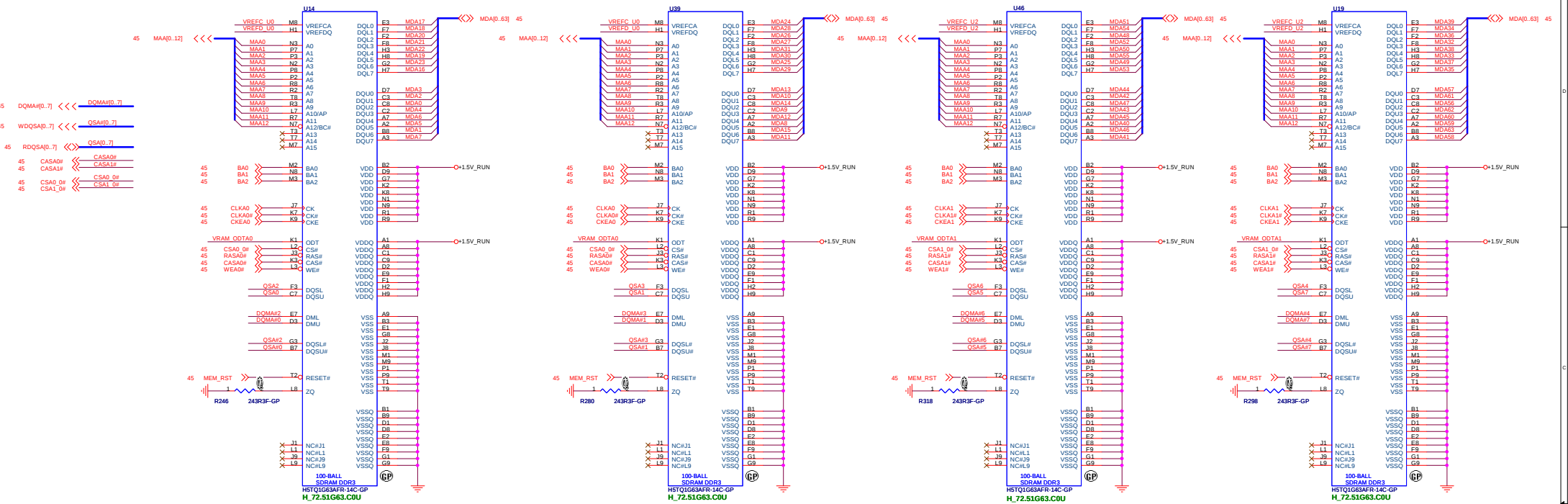
GPI03 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[9,13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V	128MB	x000	ST Microelectronics	0100
	256MB	x001		0101
	64MB	x010		0101
	32MB	x		0101
	512MB	x		0101
	16B	x	Chinglis (formerly PMC)	0100
	26B	x		0101
	46B	x		

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing ✓
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	✓ 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	0= Disable CLKREQ# power management capability 1= Enable CLKREQ# power management capability ✓
ROMIDCFG3[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	✓ Enable external BIOS ROM device 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00: No audio function 01: Audio for DisplayPort and HDMI (if adapter is detected) 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI ✓

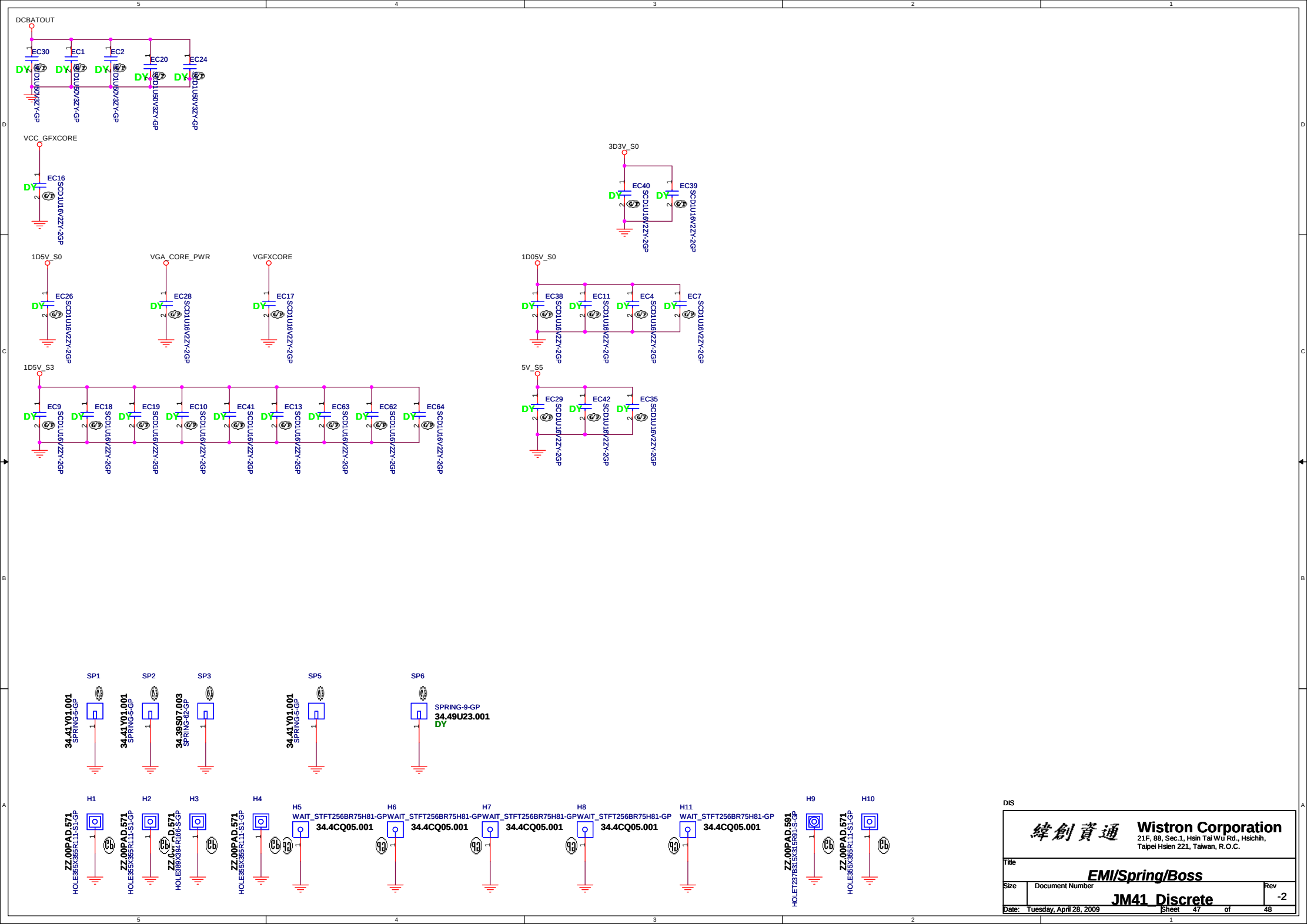
512MB DDR3



Samsung : K4W1G1646E-EC12

Hynix : H5TQ1G63BFR-12C





EC #/ Page / Description / Part Affected
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EC SC12/41/change U11 power plane to 1D8V_NB_S0