# Columbia/Tangiz Block Diagram

Project code: 91.4T301.001
PCB P/N : 48.4T301.01M
REVISION : -1M

CLK GEN.
ICS 9LPRS502
(RTM875T-605) 3
71.09502.00W

Mobile CPU
Merom 479
2G/2.33G
2.0G : 71.MEROM.A0U
2.33G : 71.MEROM.B0U 4, 5

G792 20

HOST BUS 667/800MHz@1.05V

DDR2 533/667 MHz 12,13
DDR2 533/667 MHz 12,13
533/667MHz
533/667MHz

Crestline
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CREST.00U 6,7,8,9,10,11

X4 DMI 400MHz
C-Link0

TV Out 14
CRT 15
LCD 14
DVI 44
VGA Borad 28

PCB STACKUP
TOP
VCC
S
S
GND
BOTTOM

ICH8M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
3 SATA
1 PATA 66/100
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
71.0ICH8.A0U
16,17,18,19

Line In
MIC In 14
31 INT.SPKR
Line Out (No-SPDIF)
Codec ALC268 30
AZALIA
OP AMP G1431Q 31
OP AMP G1412 31
RJ11
MODEM MDC Card 22

PCI BUS
TI PCI7412
Cardbus Cardreader
25/26
PCMCIA I/F
PWR SW CP2211F 26
PCMCIA SLOT Support TypeII 27
1394 CONN 27
MS/MS Pro/xD/ MMC/SD 5 in 1 27

LAN GIGA BCM5787M 23
TXFM 24
RJ45 24
PCIex1
Mini Card Kedron a/b/g/n 29

LPC BUS
KBC Winbond WPC8768L 32
SPI I/F
BIOS W25X80-VSS 34
LPC DEBUG CONN. 35
Touch Pad 33
INT. KB 33
FIR 32

New card 29
PCI Express
P2231NFC1 29
SATA
HDD 21
PATA
CDROM 21
USB
MINI USB BlueTooth 22
Finger print 34
USB 4 Port 22
CAMERA 13

SYSTEM DC/DC
MAX8744 38

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | 5V_S5(6A)<br>3D3V_S5(7A) |

SYSTEM DC/DC
Max8717 39

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | 1D05V_S0(9.5A)<br>1D8V_S3(8.5A) |

TPS51100 41

| | |
|---|---|
| 1D8V_S3 | DDR_VREF_S0 (1.5A)<br>DDR_VREF_S3 |

APL5915 41

| | |
|---|---|
| 1D8V_S3 | 1D25V_S0 (2A) |

APL531230

| | |
|---|---|
| 3D3V_S0 | 2D5V_S0 (300mA) |

APW5912 40

| | |
|---|---|
| 3D3V_S5 | 1D5V_S3 (7.5A) |

ISL CHARGER
ISL6255 41

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | CHG_PWR 18V 4.0A<br>UP+5V 5V 100mA |

CPU DC/DC
MAX8770 35,36

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | VCC_CORE_S0 0~1.3V 47A |

<Core Design>
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Title: BLOCK DIAGRAM
Size: A3 | Document Number: Columbia/Tangiz | Rev: -1M
Date: Monday, January 14, 2008 | Sheet 1 of 45

# ICH8M Functional Strap Definitions

ICH8-M EDS 21762 2.0V1 page 16

| Signal | Usage/When Sampled | Comment |
|---|---|---|
| HDA_SDOUT | XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK | Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h) |
| HDA_SYNC | PCIE config1 bit0, Rising Edge of PWROK. | This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h) |
| GNT2# | PCIE config2 bit0, Rising Edge of PWROK. | This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h) |
| GPIO20 | Reserved | This signal should not be pulled high. |
| GNT1#/ GPIO51 | ESI Strap (Server Only) Rising Edge of PWROK | ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile. |
| GNT3# | Top-Block Swap Override. Rising Edge of PWROK. | Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down. |
| GNT0#/ SPI_CS1# | Boot BIOS Destination Selection. Rising Edge of PWROK. | Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC. |
| INTVRMEN | Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled. | Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high |
| LAN100_SLP | Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled. | Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high |
| SATALED# | PCI Express Lane Reversal. Rising Edge of PWROK. | Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8) |
| SPKR | No Reboot. Rising Edge of PWROK. | If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit. |
| TP3 | XOR Chain Entrance. Rising Edge of PWROK. | This signal should not be pull low unless using XOR Chain testing. |
| GPIO33/ HDA_DOCK _EN# | Flash Descriptor Security Override Strap Rising Edge of PWROK | This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments. |

# ICH8M IDE Integrated Series Termination Resistors

| | |
|---|---|
| DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ | approximately 33 ohm |

# PCI Routing

page 17

| | IDSEL | INT | REQ | GNT |
|---|---|---|---|---|
| TI7412 | AD22 | G:CARDBUS B:1394 F:Flash Media G:SD Host | 0 | 0 |

# PCIE Routing

| | |
|---|---|
| LANE1 | LAN BCM5787M |
| LANE2 | MiniCard WLAN |
| LANE3 | NewCard WLAN |

# USB Table

| USB | |
|---|---|
| Pair | Device |
| 0 | USB1 |
| 1 | NC |
| 2 | USB2 |
| 3 | USB4 |
| 4 | USB3 |
| 5 | BLUETOOTH |
| 6 | WEBCAM |
| 7 | FT |
| 8 | MINICARD |
| 9 | NEW1 |

# ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

| SIGNAL | Resistor Type/Value |
|---|---|
| HDA_BIT_CLK | PULL-DOWN 20K |
| HDA_RST# | NONE |
| HDA_SDIN[3:0] | PULL-DOWN 20K |
| HDA_SDOUT | PULL-DOWN 20K |
| HDA_SYNC | PULL-DOWN 20K |
| GNT[3:0] | PULL-UP 20K |
| GPIO[20] | PULL-DOWN 20K |
| LDA[3:0]#/FHW[3:0]# | PULL-UP 20K |
| LAN_RXD[2:0] | PULL-UP 10K |
| LDRQ[0] | PULL-UP 20K |
| LDRQ[1]/GPIO23 | PULL-UP 20K |
| PME# | PULL-UP 20K |
| PWRBTN# | PULL-UP 20K |
| SATALED# | PULL-UP 15K |
| SPI_CS1# | PULL-UP 20K |
| SPI_CLK | PULL-UP 20K |
| SPI_MOSI | PULL-UP 20K |
| SPI_MISO | PULL-UP 20K |
| TACH_[3:0] | PULL-UP 20K |
| SPKR | PULL-DOWN 20K |
| TP[3] | PULL-UP 20K |
| USB[9:0][P,N] | PULL-DOWN 15K |
| CL_RST# | PULL-UP 13K |

# Crestline Strapping Signals and Configuration

Crestline EDS 20954 1.0 page 7

| Pin Name | Strap Description | Configuration |
|---|---|---|
| CFG[2:0] | FSB Frequency Select | 001 = FSB533<br>011 = FSB667<br>010 = FSB800<br>others = Reserved |
| CFG[4:3] | Reserved | |
| CFG5 | DMI x2 Select | 0 = DMI x2<br>1 = DMI x4 (Default) |
| CFG[8:6] | Reserved | |
| | Low Power PCI Express | 0 = Normal mode<br>**1 = Low Power mode** (Default) |
| CFG9 | PCI Express Graphics Lane Reversal | 0 = Reverse Lanes,15->0,14->1 ect..<br>**1= Normal operation(Default):Lane Numbered in order** |
| CFG[11:10] | Reserved | |
| CFG[13:12] | XOR/ALL Z test straps | 00 = Reserved<br>01 = XOR mode enabled<br>10 = All Z mode enabled<br>**11 = Normal Operation** (Default) |
| CFG[15:14] | Reserved | Reserved |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT Disabled<br>**1 = Dynamic ODT Enabled (Default)** |
| CFG[18:17] | Reserved | |
| CFG19 | DMI Lane Reversal | **0 = Normal operation (Default):lane Numbered in order**<br>1 =Reverse Lane,4->0,3->1 ect... |
| CFG20 | SDVO/PCIE Concurrent | **0 = Only SDVO or PCIE x1 is operational (Default)**<br>1 =SDVO and PCIE x1 are operating simultaneously via the PEG port |
| SDVOCRTL _DATA | SDVO Present | **0 = No SDVO Card present** (Default)<br>1= SDVO Card present |

**NOTE:** All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

# History

UMA

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Title: Reference

Size: A3 | Document Number: Columbia/Tangiz | Rev: -1M

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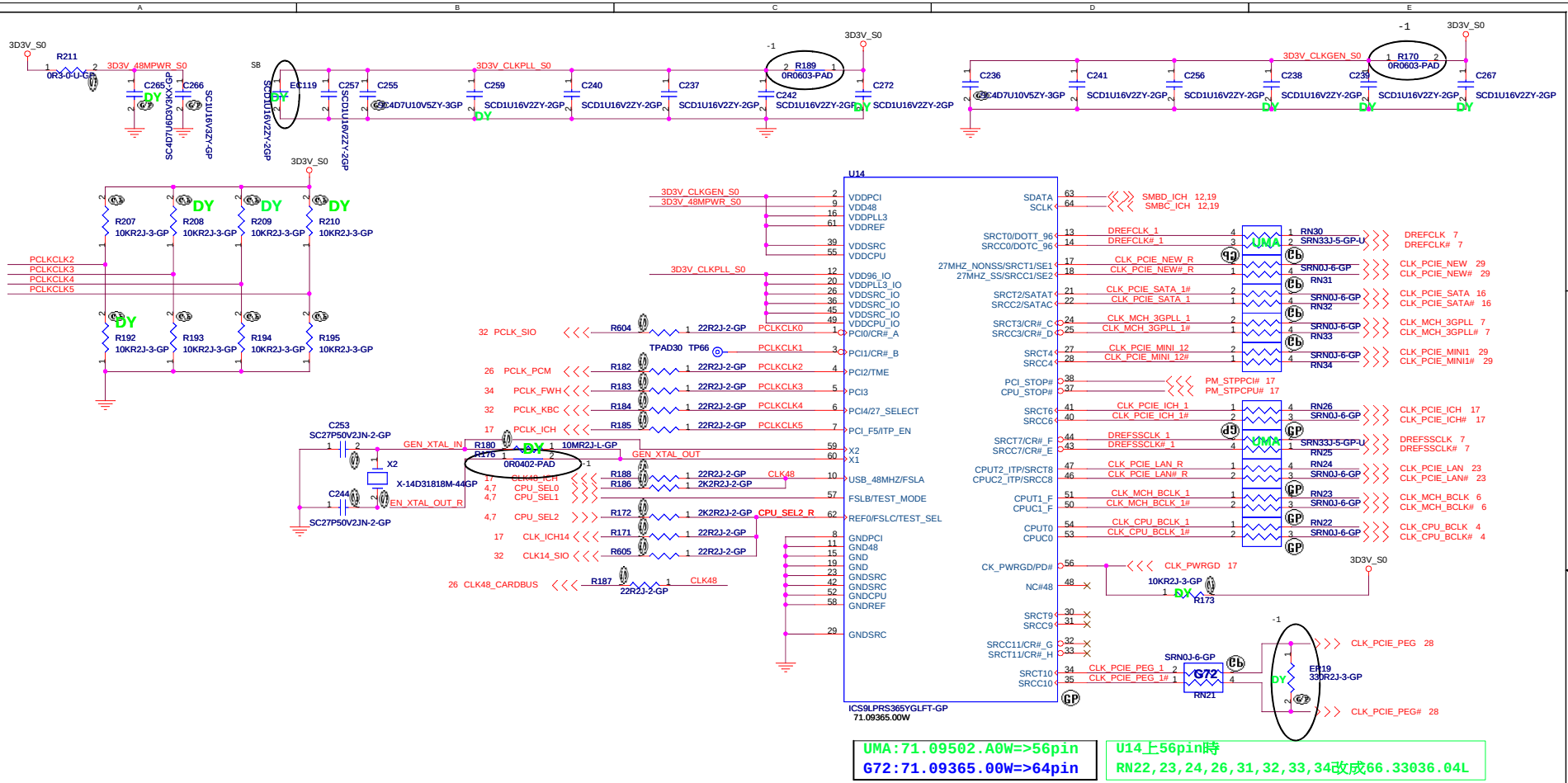


## ICS9LPR502HGLFT-GP setting table

| PIN NAME | DESCRIPTION |
|---|---|
| PCI0/CR#_A | Byte 5, bit 7<br>0 = PCI0 enabled (default)<br>1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair<br>Byte 5, bit 6<br>0 = CR#_A controls SRC0 pair (default),<br>1= CR#_A controls SRC2 pair |
| PCI1/CR#_B | Byte 5, bit 5<br>0 = PCI1 enabled (default)<br>1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair<br>Byte 5, bit 4<br>0 = CR#_B controls SRC1 pair (default)<br>1= CR#_B controls SRC4 pair |
| PCI2/TME | 0 = Overclocking of CPU and SRC Allowed<br>1 = Overclocking of CPU and SRC NOT allowed |
| | |
| PCI4/SRC5_EN | 0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#.<br>1 = Pins29,30 as SRC-5 differential pair. |
| PCI_F5/ITP_EN | 0 =SRC8/SRC8#<br>1 = ITP/ITP# |

## RTM875T-605 setting table

| PIN NAME | DESCRIPTION |
|---|---|
| PCI0/CR#_A | Byte 5, bit 7<br>0 = PCI0 enabled (default)<br>1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair<br>Byte 5, bit 6<br>0 = CR#_A controls SRC0 pair (default),<br>1= CR#_A controls SRC2 pair |
| PCI1/CR#_B | Byte 5, bit 5<br>0 = PCI1 enabled (default)<br>1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair<br>Byte 5, bit 4<br>0 = CR#_B controls SRC1 pair (default)<br>1= CR#_B controls SRC4 pair |
| PCI2/TME | 0 = Overclocking of CPU and SRC Allowed<br>1 = Overclocking of CPU and SRC NOT allowed |
| PCI3/SRC-5_EN | 0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#.<br>1 = Pins29,30 as SRC-5 differential pair. |
| PCI4/27M_SEL | 0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96#<br>1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0# |
| PCI_F5/ITP_EN | 0 =SRC8/SRC8#<br>1 = ITP/ITP# |

| SEL2 FSC | SEL1 FSB | SEL0 FSA | CPU | FSB |
|---|---|---|---|---|
| 1 | 0 | 1 | 100M | X |
| 0 | 0 | 1 | 133M | X |
| 0 | 1 | 1 | 166M | 667M |
| 0 | 1 | 0 | 200M | 800M |

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Title: Clock Generator

Size | Document Number: Columbia/Tangiz | Rev: -1M

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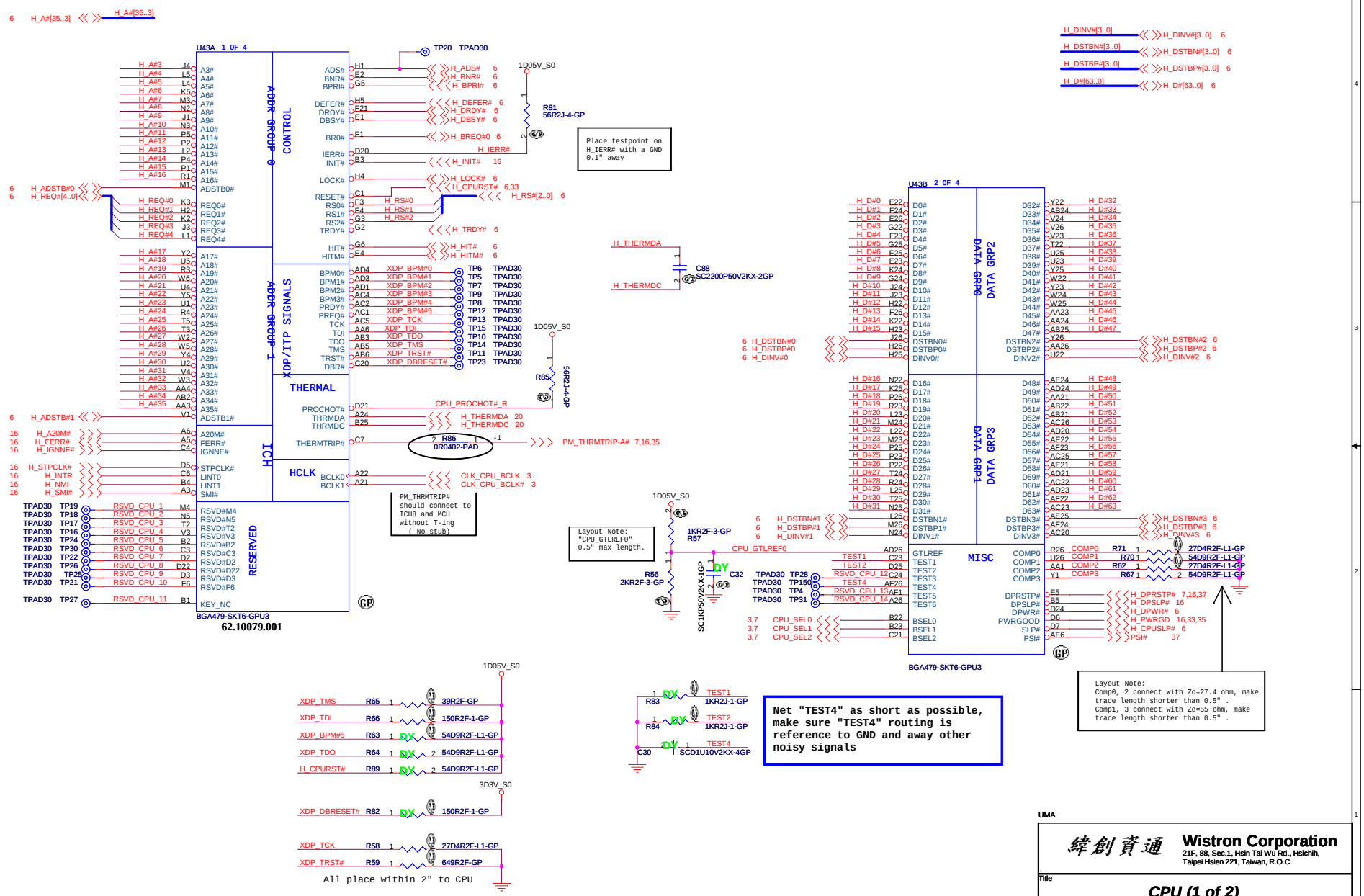
U43A 1 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
BGA479-SKT6-GPU3
62.10079.001
U43B 2 OF 4
DATA GRP0
DATA GRP1
DATA GRP2
DATA GRP3
MISC
BGA479-SKT6-GPU3
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH8 and MCH without T-ing ( No stub)
Layout Note: "CPU_GTLREF0" 0.5" max length.
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
All place within 2" to CPU
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
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Title
CPU (1 of 2)
Size
Document Number
Columbia/Tangiz
Rev
-1M
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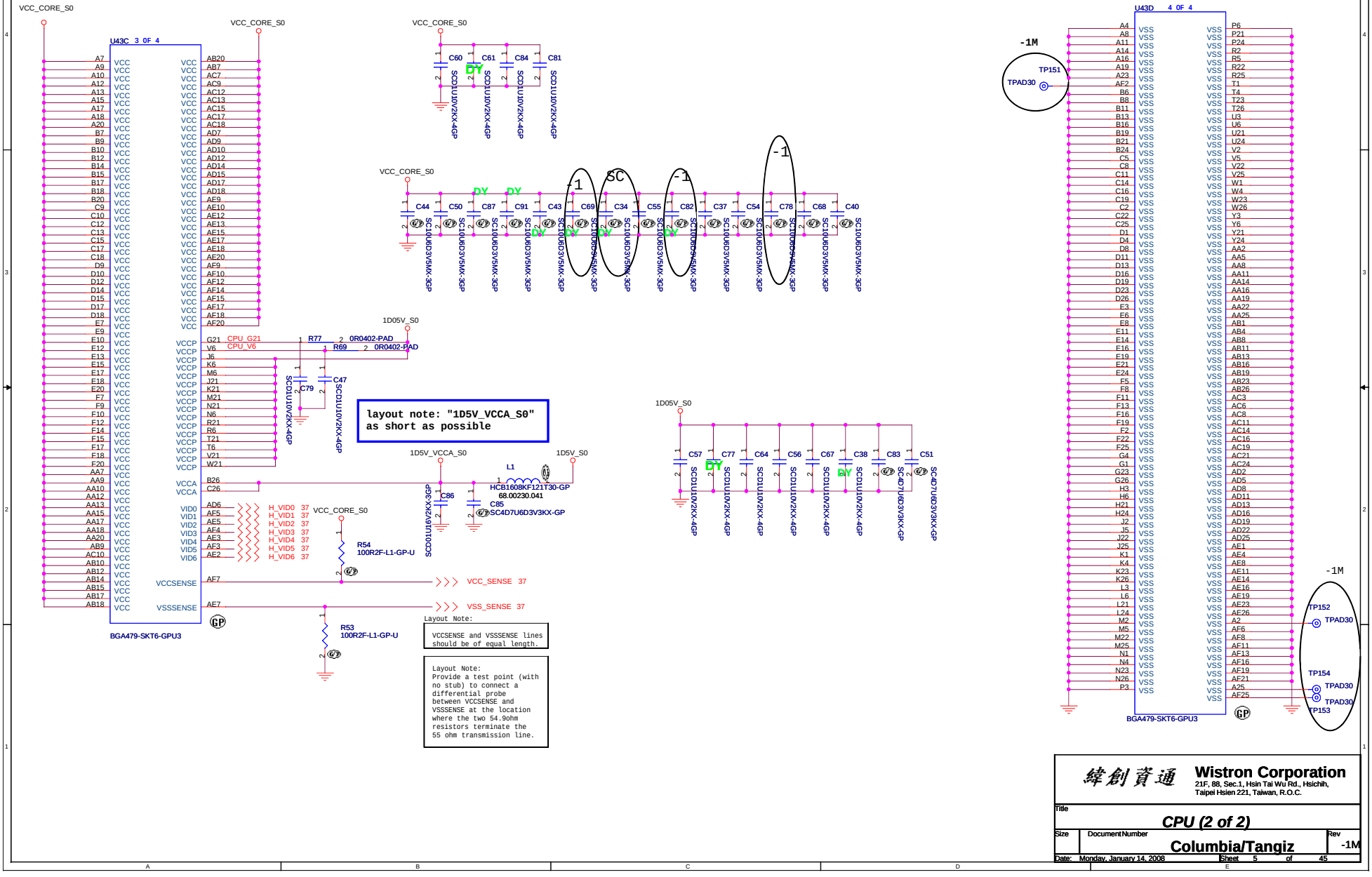
VCC_CORE_S0
U43C 3 OF 4
BGA479-SKT6-GPU3
1D05V_S0
layout note: "1D5V_VCCA_S0" as short as possible
1D5V_VCCA_S0
L1
HCB1608KF121T30-GP
68.00230.041
R77 0R0402-PAD
R69 0R0402-PAD
R54 100R2F-L1-GP-U
R53 100R2F-L1-GP-U
VCC_SENSE 37
VSS_SENSE 37
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
U43D 4 OF 4
-1M
TP151
TPAD30
TP152
TP154
TP153
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CPU (2 of 2)
Columbia/Tangiz
-1M
Monday, January 14, 2008
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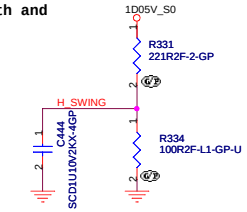
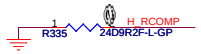
**H_SWING routing Trace width and Spacing use 10 / 20 mil**

**H_SWING Resistors and Capacitors close MCH 500 mil ( MAX )**



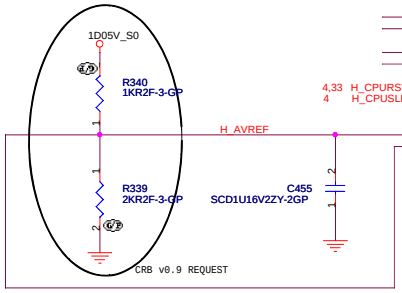

**H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil ( MAX )**

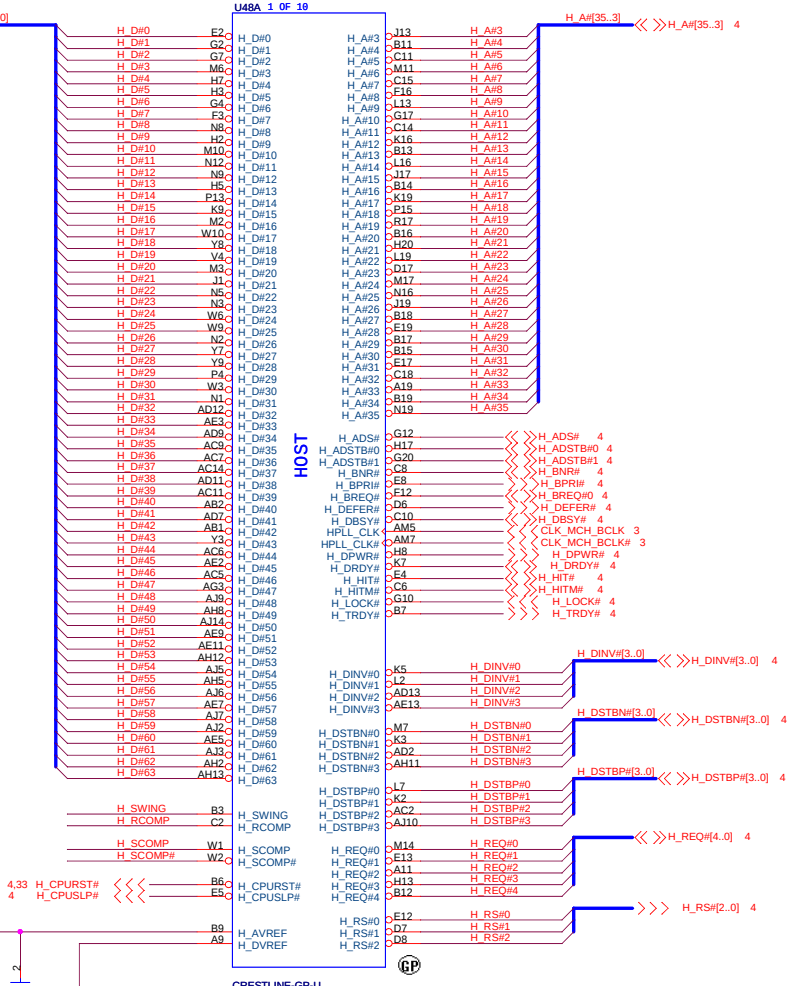

**H_RCOMP routing Trace width and Spacing use 10 / 20 mil**




**Place them near to the chip ( < 0.5")**

**H_REF Decoupling Crestline close Crestline 100 mil**

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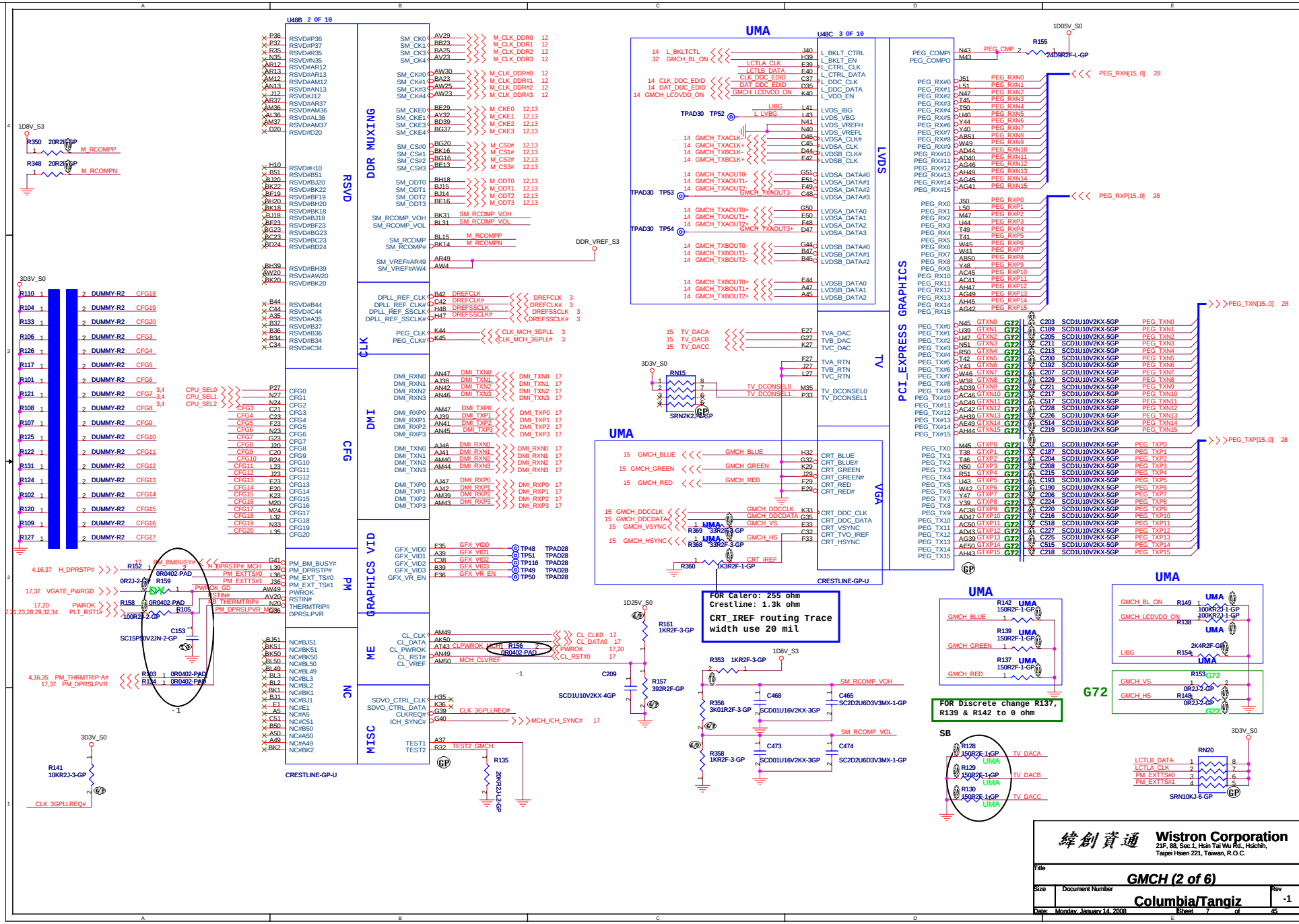
U48B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
PM
GRAPHICS VID
ME
NC
MISC
U48C 3 OF 10
UMA
LVDS
TV
VGA
PCI_EXPRESS GRAPHICS
CRESTLINE-GP-U
FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace
width use 20 mil
FOR Discrete change R137,
R139 & R142 to 0 ohm
SB
G72
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Title
GMCH (2 of 6)
Size
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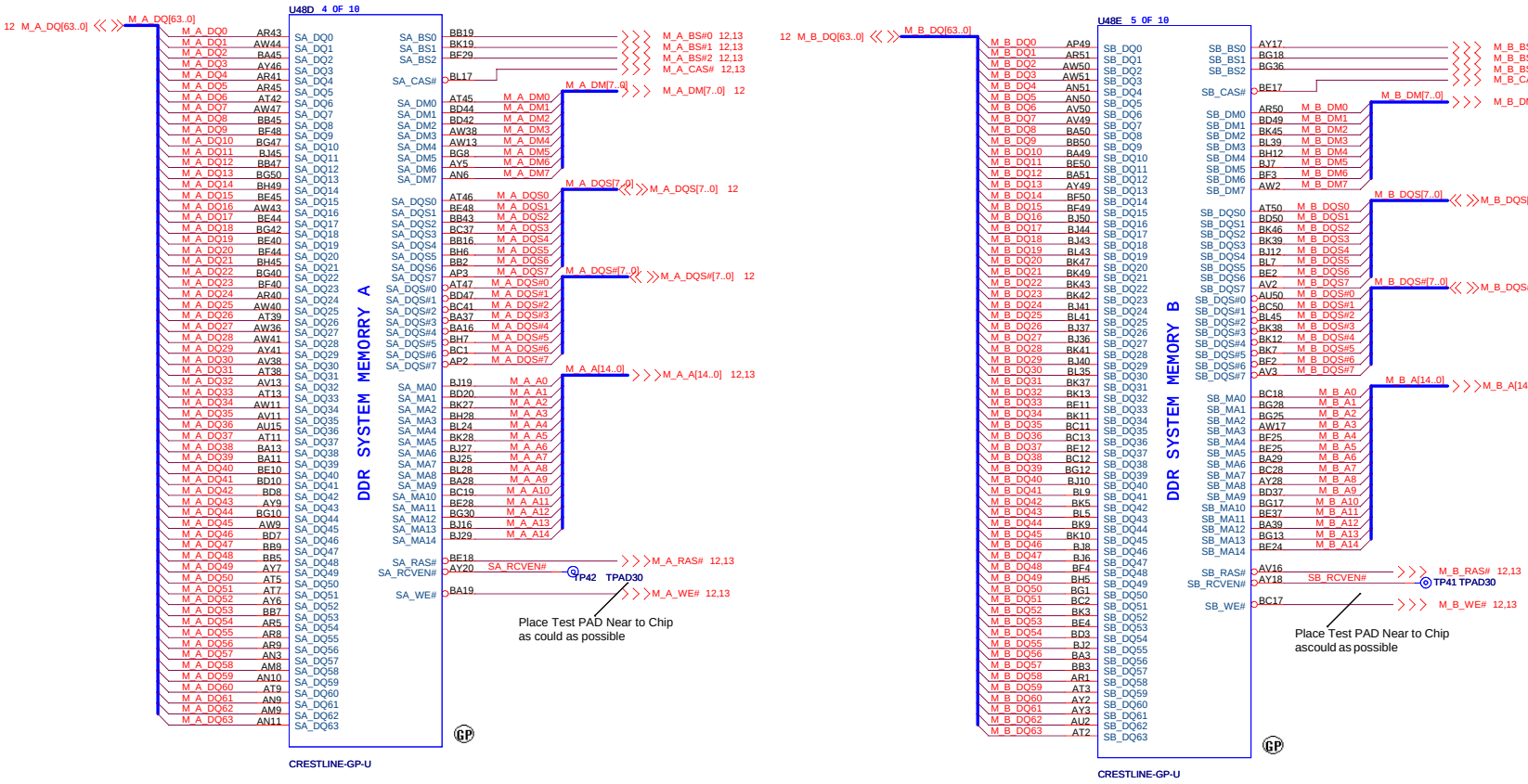


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|---|---|---|
| | **Columbia/Tangiz** | -1 |

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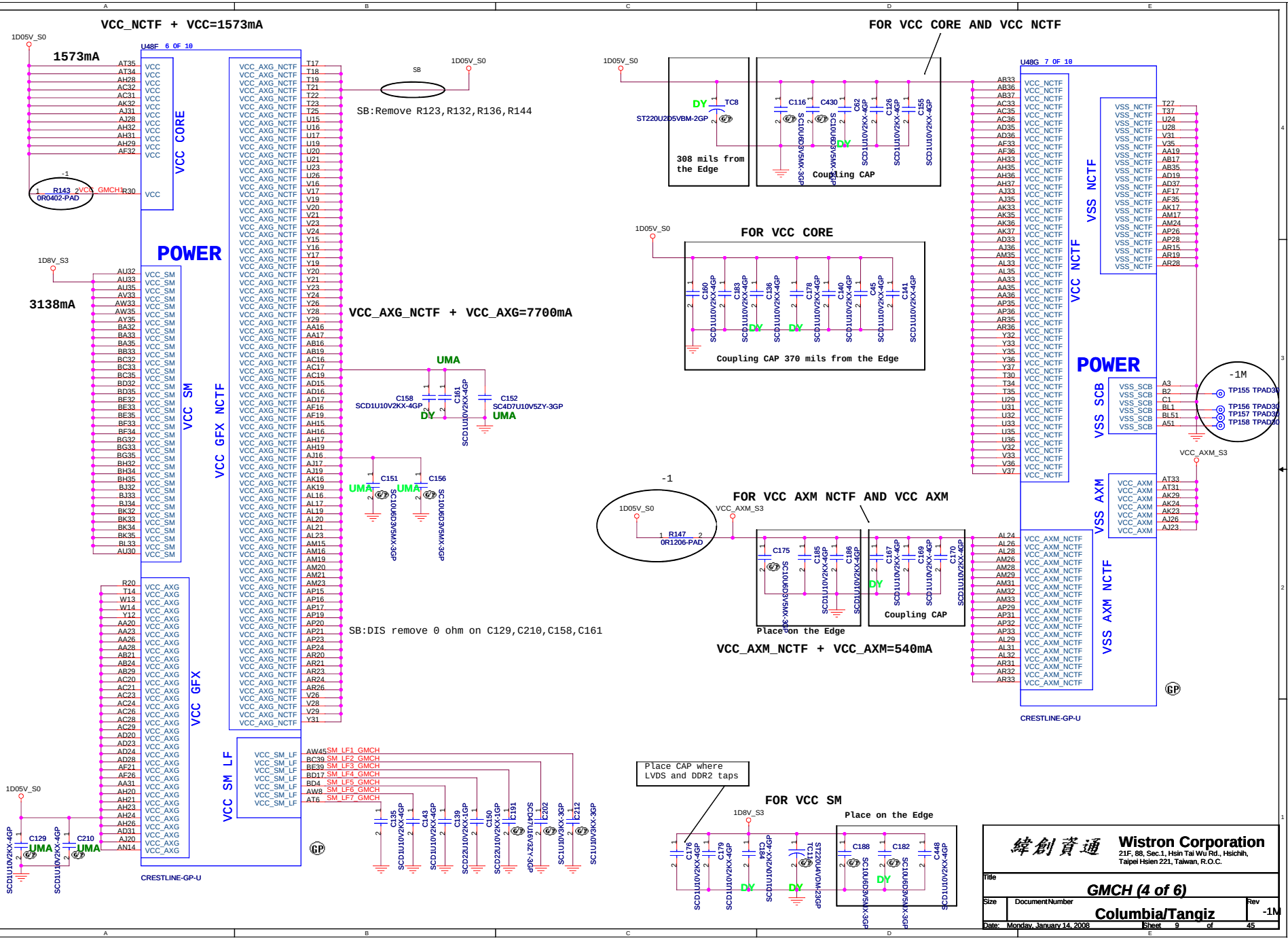
VCC_NCTF + VCC=1573mA
1573mA
U48F 6 OF 10
VCC CORE
POWER
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
CRESTLINE-GP-U
SB:Remove R123,R132,R136,R144
VCC_AXG_NCTF + VCC_AXG=7700mA
3138mA
SB:DIS remove 0 ohm on C129,C210,C158,C161
FOR VCC CORE AND VCC NCTF
FOR VCC CORE
Coupling CAP 370 mils from the Edge
308 mils from the Edge
Coupling CAP
U48G 7 OF 10
VCC NCTF
VSS NCTF
POWER
VSS SCB
VSS AXM
VSS AXM NCTF
VCC_AXM_S3
FOR VCC AXM NCTF AND VCC AXM
Place on the Edge
VCC_AXM_NCTF + VCC_AXM=540mA
Place CAP where LVDS and DDR2 taps
FOR VCC SM
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GMCH (4 of 6)
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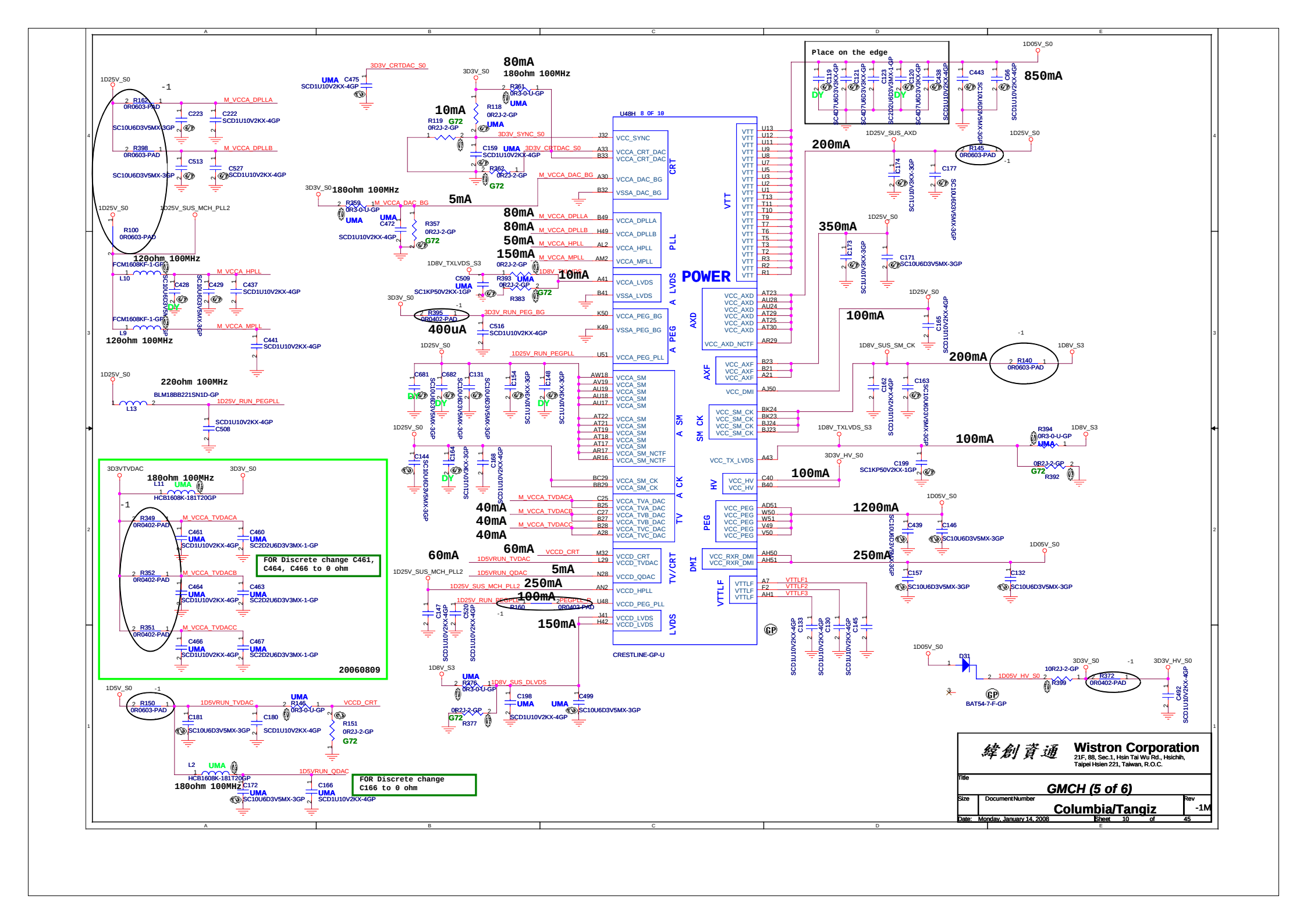
POWER
U48H 8 OF 10
CRESTLINE-GP-U
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
TV/CRT
LVDS
VTT
AXD
AXF
SM CK
HV
PEG
DMI
VTTLF
Place on the edge
180ohm 100MHz
120ohm 100MHz
220ohm 100MHz
FOR Discrete change C461, C464, C466 to 0 ohm
20060809
FOR Discrete change C166 to 0 ohm
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GMCH (5 of 6)
Columbia/Tangiz
-1M
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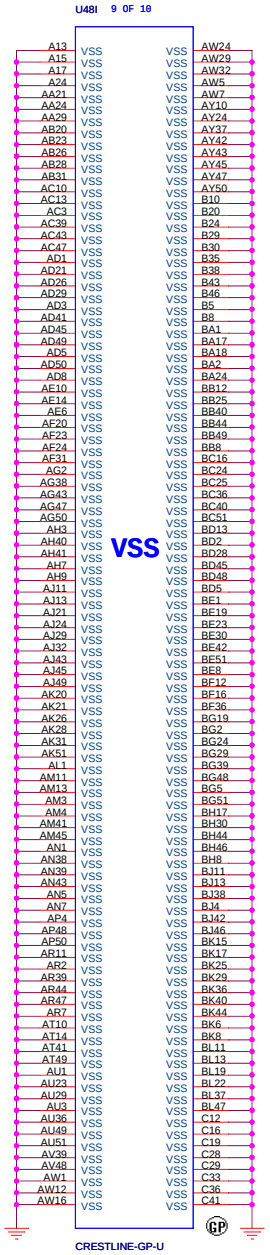


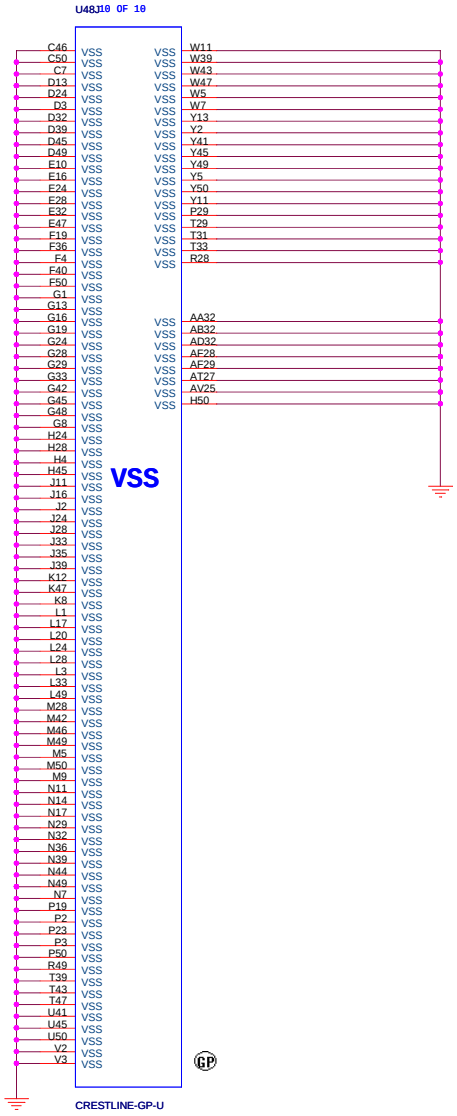


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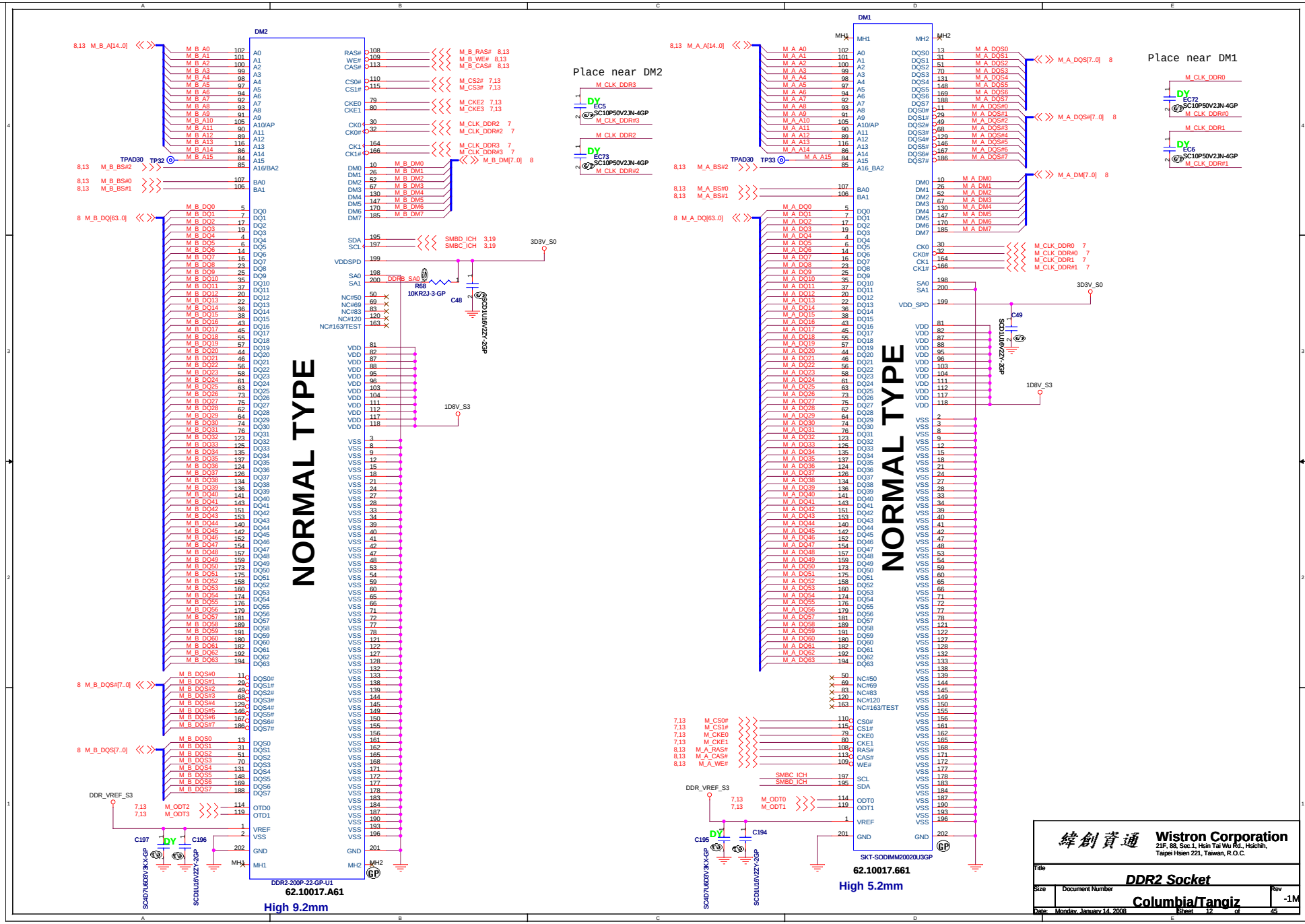
DM2
NORMAL TYPE
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
Place near DM2
M_CLK_DDR3
EC5
SC10P50V2JN-4GP
M_CLK_DDR#3
M_CLK_DDR2
EC73
SC10P50V2JN-4GP
M_CLK_DDR#2
R68
10KR2J-3-GP
C48
SCD1U16V2ZY-2GP
3D3V_S0
1D8V_S3
DDR_VREF_S3
C197
C196
C195
C194
SCD1U16V2ZY-2GP
SCD7U6D3V3KX-GP
DM1
NORMAL TYPE
SKT-SODIMM20020U3GP
62.10017.661
High 5.2mm
Place near DM1
EC72
EC6
SC10P50V2JN-4GP
C49
SCD1U16V2ZY-4GP
TPAD30
TP32
TP33
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 Socket
Size
Document Number
Columbia/Tangiz
Rev
-1M
Date: Monday, January 14, 2008
Sheet 12 of 45

# PARALLEL TERMINATION

*Put decap near power(0.9V) and pull-up resistor*

DDR_VREF_S0

RN13 SRN56J-5-GP: M_A_A12, M_A_A8 — M_CKE0 7,12; M_A_BS#2 8,12
RN12 SRN56J-5-GP: M_B_A8, M_B_A9, M_B_A5
RN14 SRN56J-5-GP: M_B_A12 — M_CKE3 7,12; M_B_BS#2 8,12; M_CKE2 7,12
RN7 SRN56J-5-GP: M_B_A3, M_B_A1, M_B_A10 — M_B_WE# 8,12
RN1 SRN56J-5-GP: M_B_A13 — M_ODT2 7,12; M_ODT3 7,12; M_B_RAS# 8,12
RN5 SRN56J-5-GP: M_B_A2, M_B_A0, M_B_A4 — M_B_BS#1 8,12
RN9 SRN56J-5-GP: M_B_A14, M_B_A11, M_B_A7, M_B_A6
RN4 SRN56J-5-GP: M_B_BS#0 8,12; M_B_CAS# 8,12; M_CS3# 7,12; M_CS2# 7,12
RN3 SRN56J-5-GP: M_A_A13 — M_ODT0 7,12; M_CS0# 7,12; M_A_RAS# 8,12
RN8 SRN56J-5-GP: M_A_A0, M_A_A2, M_A_A4 — M_A_BS#1 8,12
RN2 SRN56J-5-GP: M_A_CAS# 8,12; M_ODT1 7,12; M_CS1# 7,12
RN10 SRN56J-5-GP: M_A_A9, M_A_A14, M_A_A5, M_A_A3
RN11 SRN56J-5-GP: M_A_A6, M_A_A7, M_A_A11 — M_CKE1 7,12
RN6 SRN56J-5-GP: M_A_A1, M_A_A10 — M_A_BS#0 8,12; M_A_WE# 8,12

# Decoupling Capacitor

*Put decap near power(0.9V) and pull-up resistor*

DDR_VREF_S0

M_A_A[14..0] — M_A_A[14..0] 8,12
M_B_A[14..0] — M_B_A[14..0] 8,12

C110 C134 C117 C109 C103 C115 C125 C112 C97 C118 C128
C138 C104 C98 C106 C107 C127 C105 C101 C99 C137 C102
SCD1U16V2ZY-2GP (DY)

## Place these Caps near DM1

1D8V_S3

C446 C436 C432 C424 C417
C421 C427 C434 C442
SC2D2U6D3V8MX-1-GP (DY)

## Place these Caps near DM2

1D8V_S3

C447 C440 C433 C426 C418
C445 C435 C431 C423
SC2D2U6D3V8MX-1-GP (DY)

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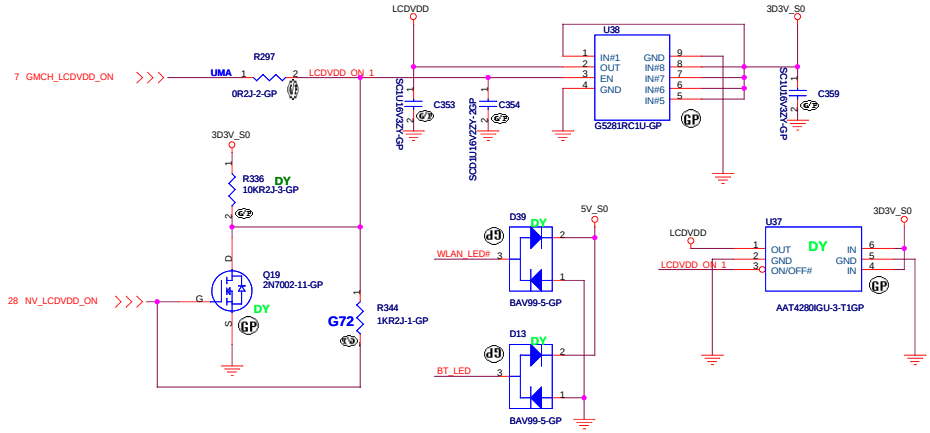
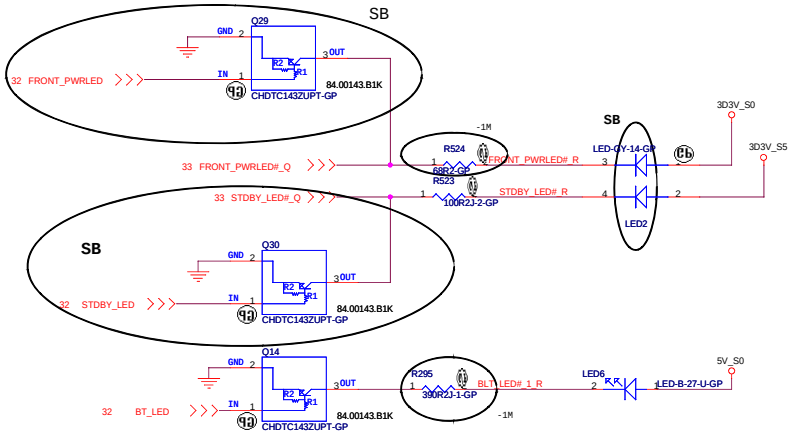
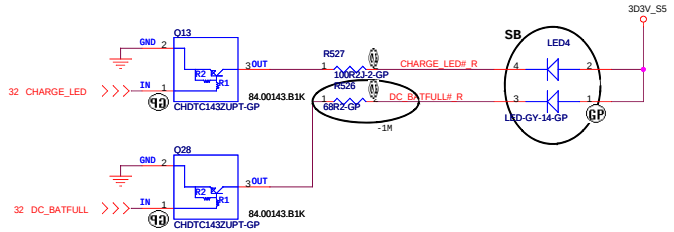
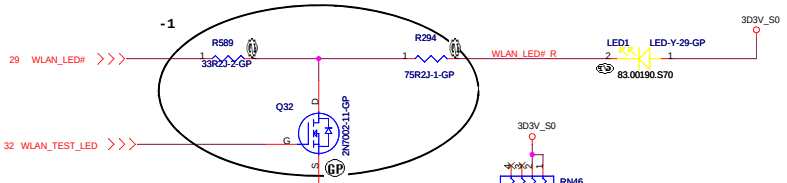
Title: ***DDR2 Termination Resistor***
Size | Document Number: **Columbia/Tangiz** | Rev: -1M
Date: Monday, January 14, 2008 | Sheet 13 of 45

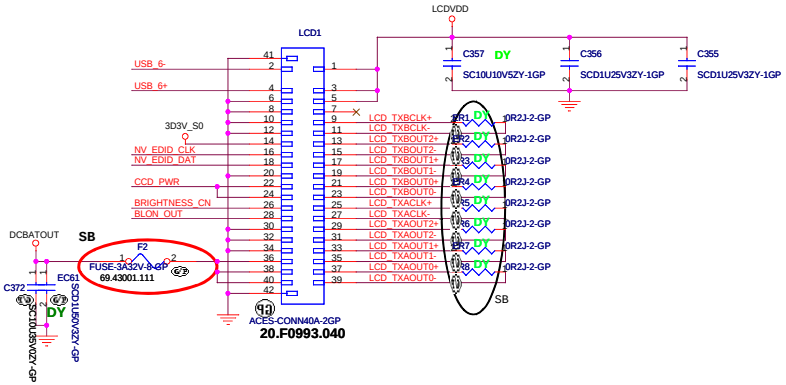
# LCD/INVERTER CONN

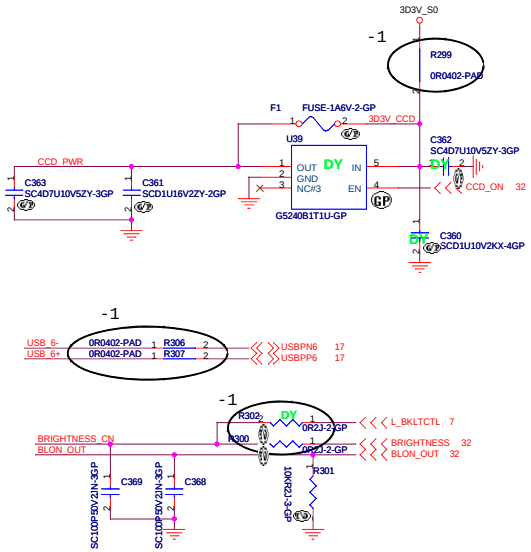


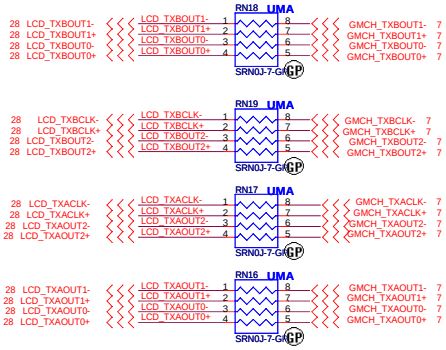



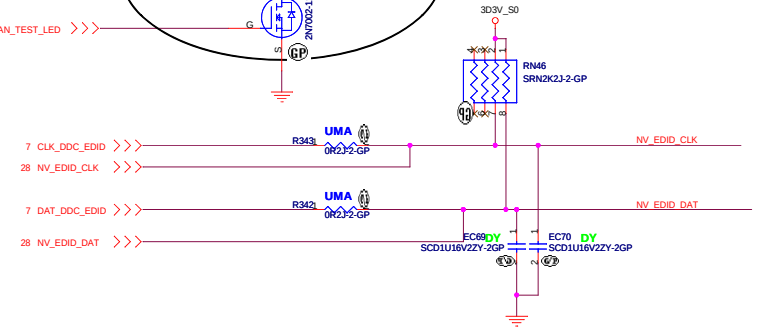





<Variant Name>

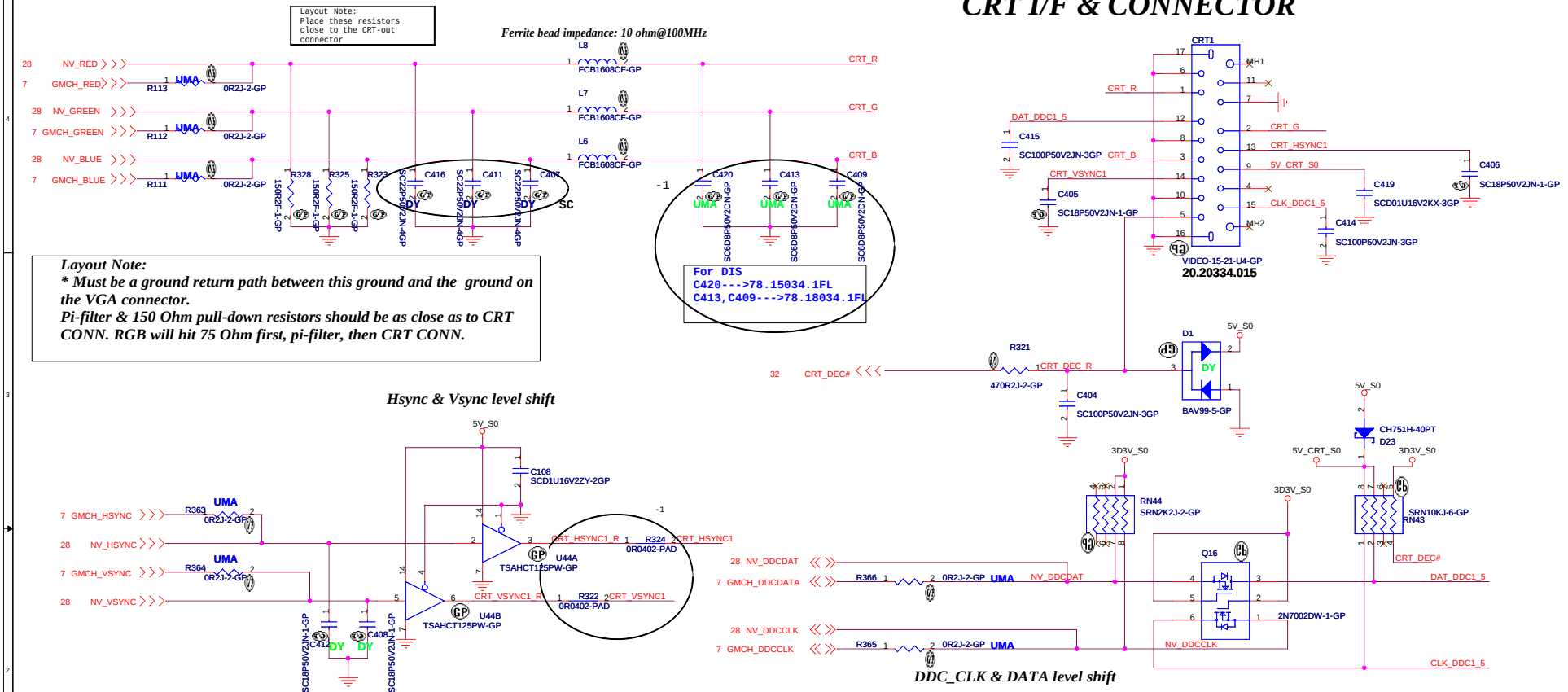
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN & LED

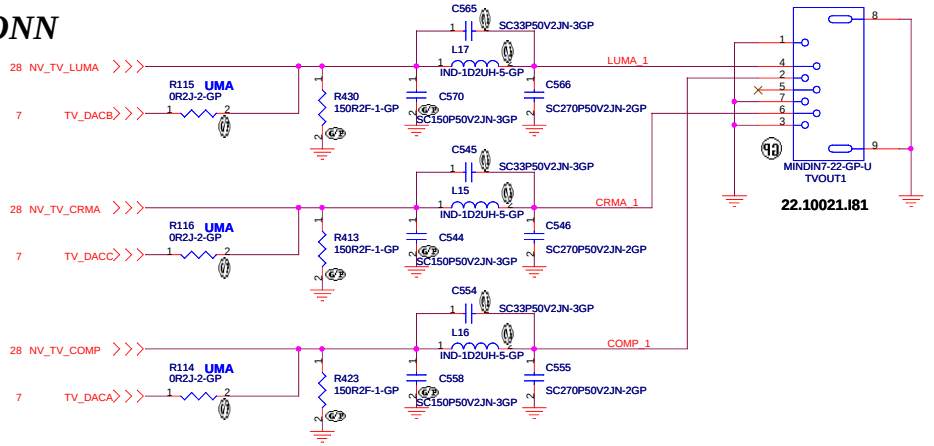
Size | Document Number: Columbia/Tangiz | Rev: -1

Date: Monday, January 14, 2008 | Sheet 14 of 45

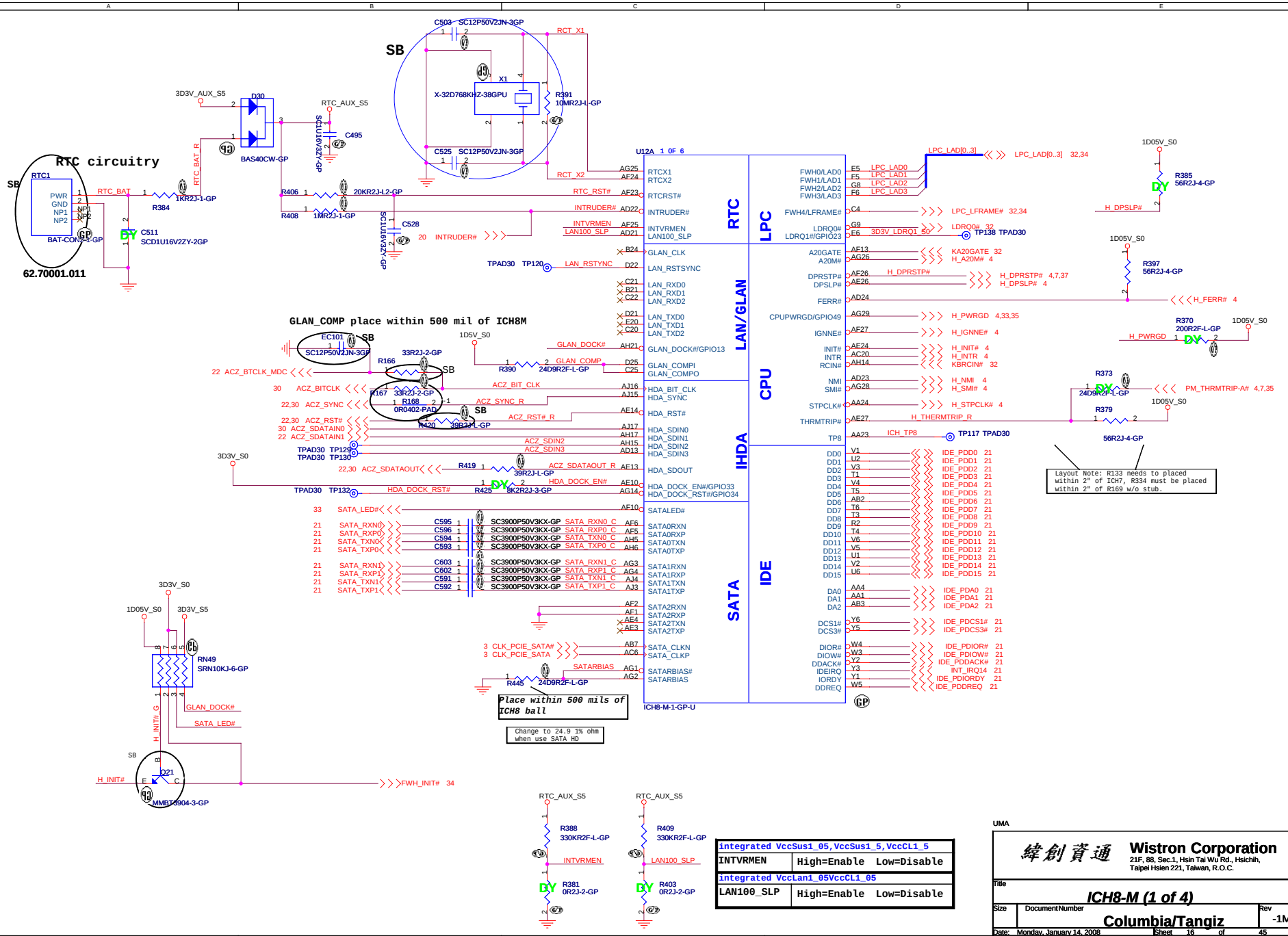
# CRT I/F & CONNECTOR




# TV CONN




| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | *CRT/TV Connector* | |
| Size | Document Number: Columbia/Tangiz | Rev: -1 |
| Date: Monday, January 14, 2008 | Sheet 15 of 45 | |


RTC circuitry
62.70001.011
BAT-CON2-1-GP
RTC1
RTC_BAT
1KR2J-1-GP
R384
C511
SCD1U16V2ZY-2GP
BAS40CW-GP
D30
3D3V_AUX_S5
RTC_AUX_S5
C495
SCD1U16V2ZY-2GP
RTC_BAT_R
X-32D768KHZ-38GPU
X1
C503 SC12P50V2JN-3GP
C525 SC12P50V2JN-3GP
R391 10MR2J-L-GP
SB
R406 20KR2J-L2-GP
R408 1MR2J-1-GP
C528
SCD1U16V3ZY-6P
INTRUDER#
RCT_X1
RCT_X2
RTC_RST#
INTVRMEN
LAN100_SLP
LAN_RSTSYNC
TPAD30 TP120
U12A 1 OF 6
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
RTC
LAN/GLAN
CPU
IHDA
SATA
LPC
IDE
ICH8-M-1-GP-U
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LPC_LAD[0..3]
LPC_LFRAME#
3D3V_LDRQ1
TP138 TPAD30
KA20GATE
H_A20M#
H_DPRSTP#
H_DPSLP#
H_FERR#
H_PWRGD
H_IGNNE#
H_INIT#
H_INTR
KBRCIN#
H_NMI
H_SMI#
H_STPCLK#
H_THERMTRIP_R
ICH_TP8
TP117 TPAD30
IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_PDA0
IDE_PDA1
IDE_PDA2
IDE_PDCS1#
IDE_PDCS3#
IDE_PDIOR#
IDE_PDIOW#
IDE_PDDACK#
INT_IRQ14
IDE_PDIORDY
IDE_PDDREQ
R385 56R2J-4-GP
R397 56R2J-4-GP
R370 200R2F-L-GP
R373 24D9R2F-L-GP
R379 56R2J-4-GP
PM_THRMTRIP-A#
Layout Note: R133 needs to placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.
GLAN_COMP place within 500 mil of ICH8M
EC101 SC12P50V2JN-3GP
R166 33R2J-2-GP
R167 33R2J-2-GP
R168 0R0402-PAD
R420 39R2F-L-GP
R390 24D9R2F-L-GP
ACZ_BTCLK_MDC
ACZ_BITCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDATAIN0
ACZ_SDATAIN1
ACZ_BIT_CLK
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDIN2
ACZ_SDIN3
ACZ_SDATAOUT
ACZ_SDATAOUT_R
R419 39R2J-L-GP
R425 8K2R2J-3-GP
HDA_DOCK_RST#
HDA_DOCK_EN#
SATA_LED#
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
C595 C596 C594 C593
C603 C602 C591 C592
SC3900P50V3KX-GP
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
SATA_RXN1_C
SATA_RXP1_C
SATA_TXN1_C
SATA_TXP1_C
CLK_PCIE_SATA#
CLK_PCIE_SATA
SATARBIAS
R445 24D9R2F-L-GP
Place within 500 mils of ICH8 ball
Change to 24.9 1% ohm when use SATA HD
RN49 SRN10KJ-6-GP
GLAN_DOCK#
SATA_LED#
H_INIT#
Q21 MMBT3904-3-GP
FWH_INIT# 34
R388 330KR2F-L-GP
R409 330KR2F-L-GP
R381 0R2J-2-GP
R403 0R2J-2-GP
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (1 of 4)
Size
Document Number
Columbia/Tangiz
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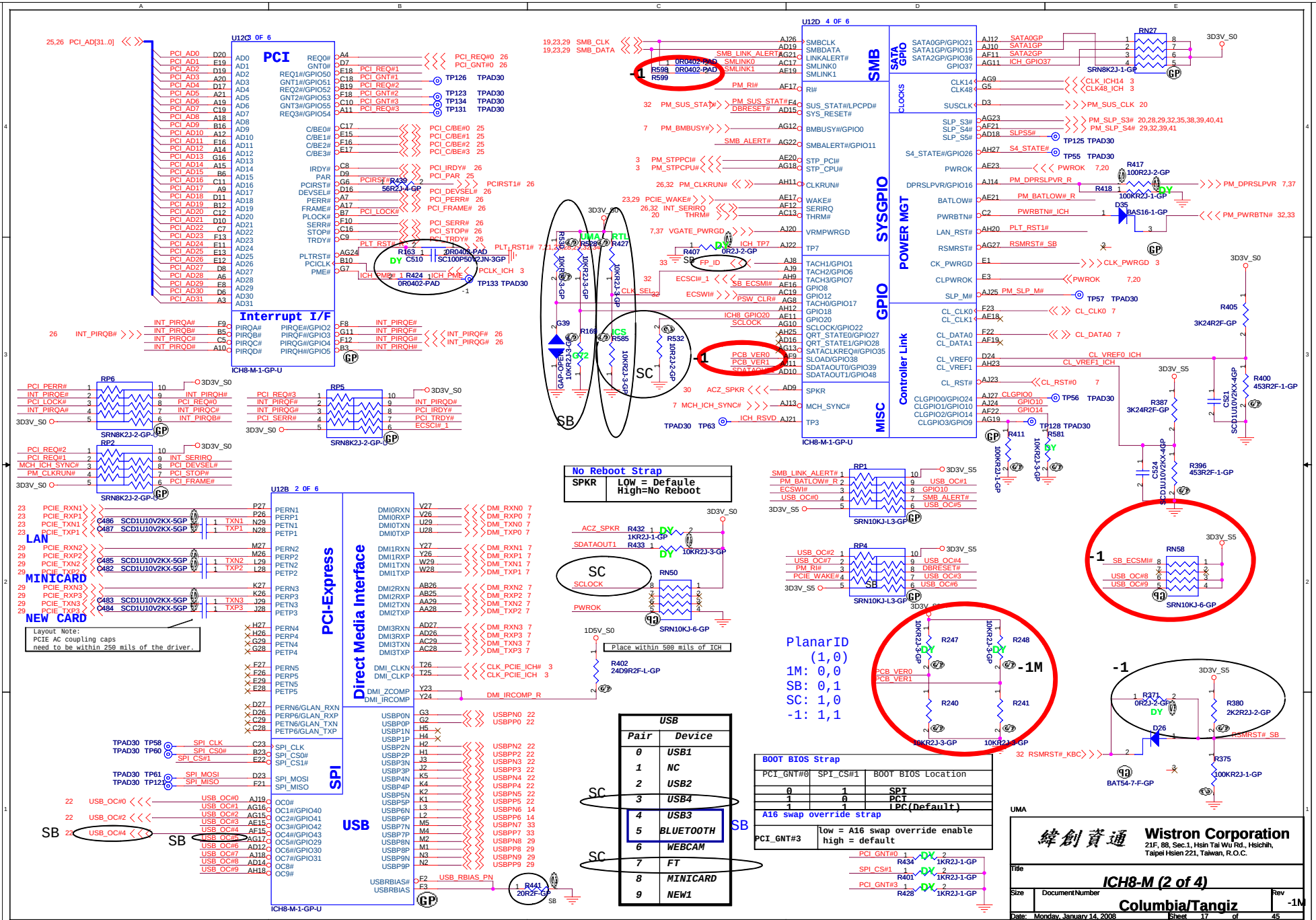
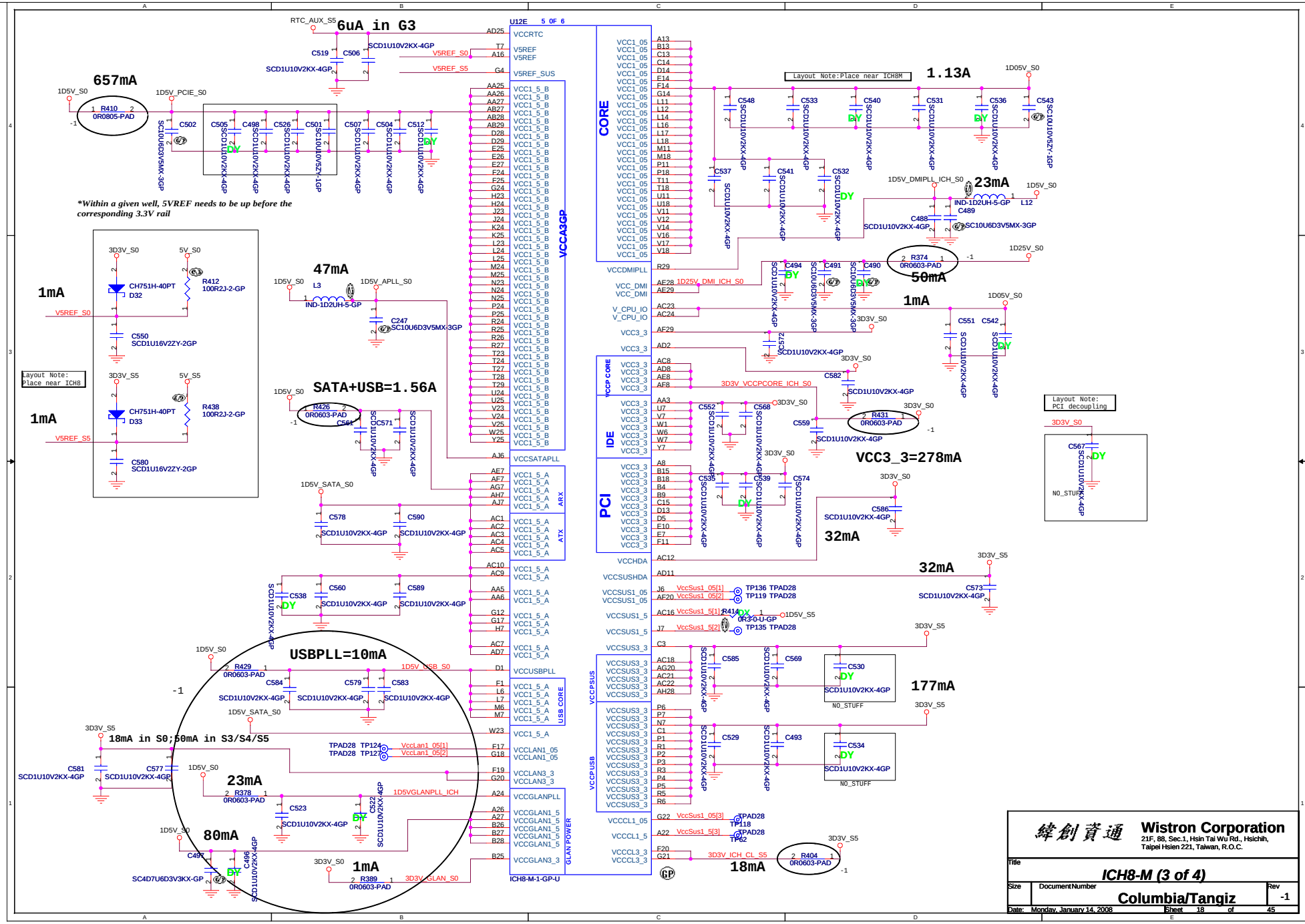

PCI
Interrupt I/F
ICH8-M-1-GP-U
SMB
SATA GPIO
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
CLOCKS
SB
SC
-1
-1M
No Reboot Strap
SPKR LOW = Defaule High=No Reboot
PCI-Express
Direct Media Interface
USB
SPI
LAN
MINICARD
NEW CARD
Layout Note: PCIE AC coupling caps need to be within 250 mils of the driver.
Place within 500 mils of ICH
PlanarID (1,0)
1M: 0,0
SB: 0,1
SC: 1,0
-1: 1,1
USB
Pair Device
0 USB1
1 NC
2 USB2
3 USB4
4 USB3
5 BLUETOOTH
6 WEBCAM
7 FT
8 MINICARD
9 NEW1
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable high = default
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (2 of 4)
Size Document Number Rev
Columbia/Tangiz -1M
Date: Monday, January 14, 2008 Sheet 17 of 45


6uA in G3
657mA
1.13A
23mA
50mA
1mA
47mA
SATA+USB=1.56A
VCC3_3=278mA
32mA
177mA
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
23mA
80mA
1mA
18mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH8M
Layout Note: Place near ICH8
Layout Note: PCI decoupling
U12E 5 OF 6
ICH8-M-1-GP-U
CORE
IDE
PCI
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH8-M (3 of 4)
Columbia/Tangiz
-1
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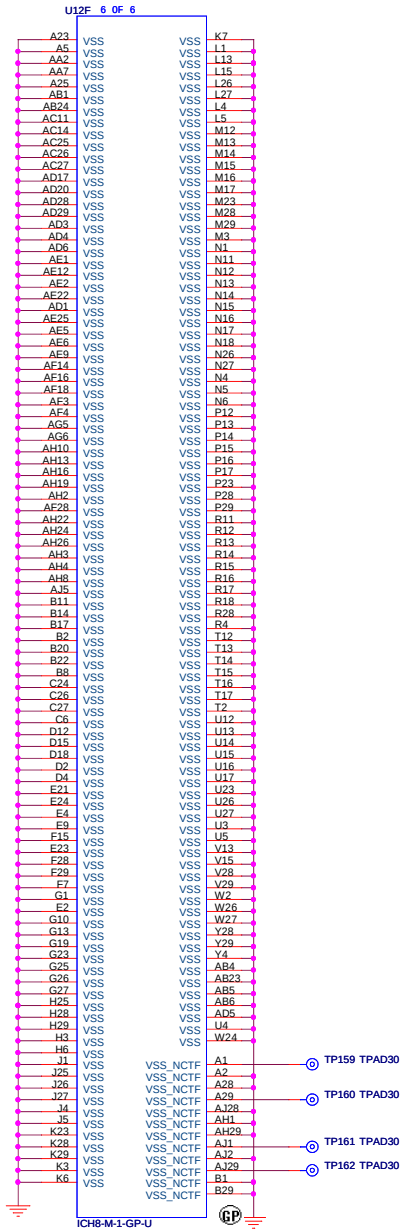
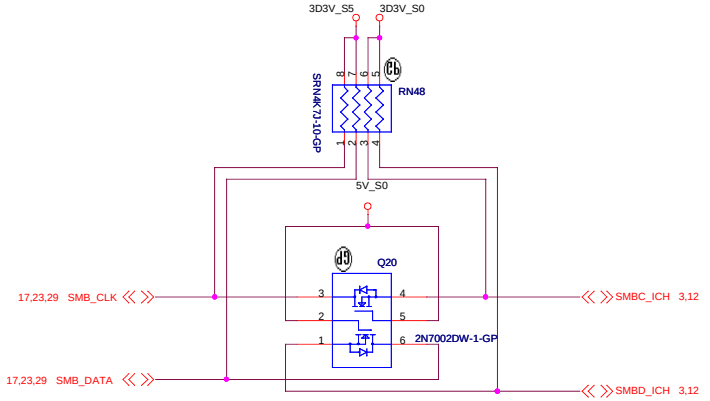


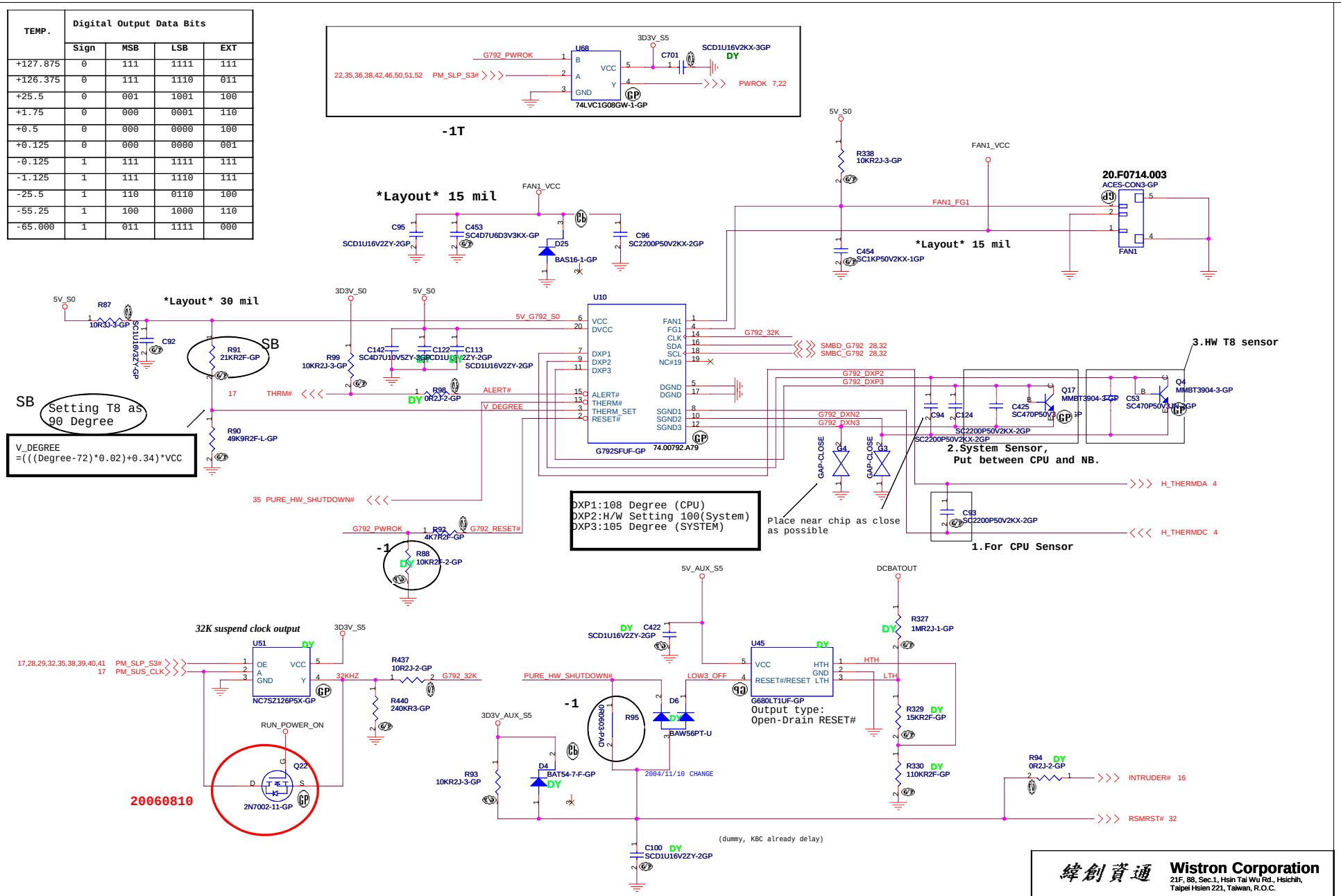

*Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance*

## SMBUS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | *ICH8-M (4 of 4)* | |
| Size | Document Number: **Columbia/Tangiz** | Rev: -1 |
| Date: Monday, January 14, 2008 | Sheet 19 of 45 | |

| TEMP. | Digital Output Data Bits | | | |
|---|---|---|---|---|
| | Sign | MSB | LSB | EXT |
| +127.875 | 0 | 111 | 1111 | 111 |
| +126.375 | 0 | 111 | 1110 | 011 |
| +25.5 | 0 | 001 | 1001 | 100 |
| +1.75 | 0 | 000 | 0001 | 110 |
| +0.5 | 0 | 000 | 0000 | 100 |
| +0.125 | 0 | 000 | 0000 | 001 |
| -0.125 | 1 | 111 | 1111 | 111 |
| -1.125 | 1 | 111 | 1110 | 111 |
| -25.5 | 1 | 110 | 0110 | 100 |
| -55.25 | 1 | 100 | 1000 | 110 |
| -65.000 | 1 | 011 | 1111 | 000 |





緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.


Title: Thermal/Fan Controllor

Size | DocumentNumber: Columbia/Tangiz | Rev: -1M

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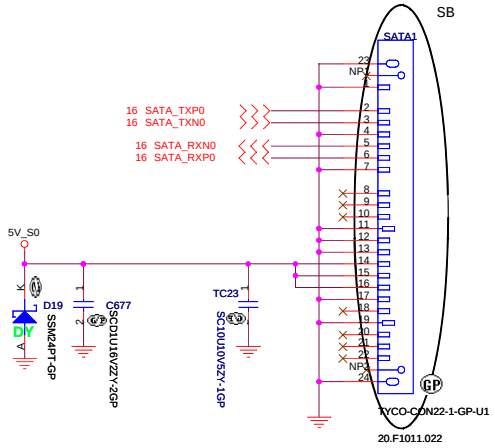
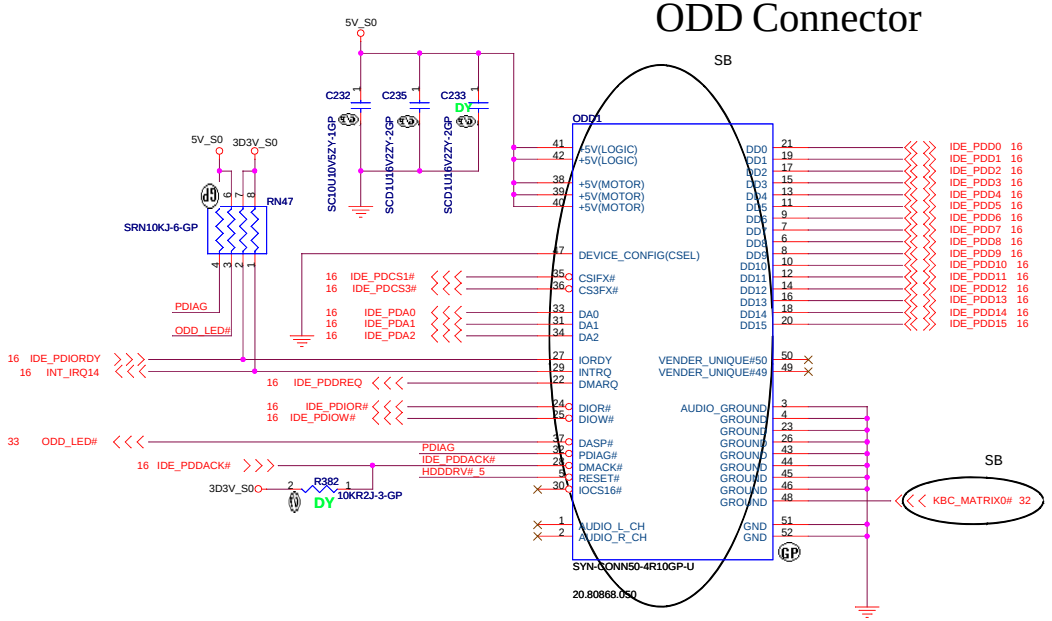
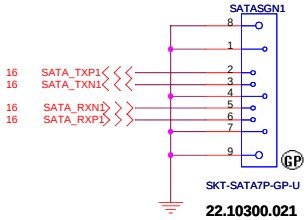
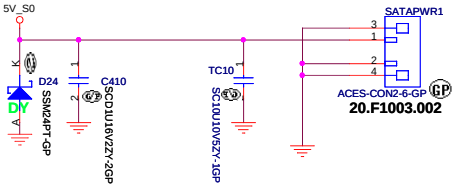
# SATA HD Connector

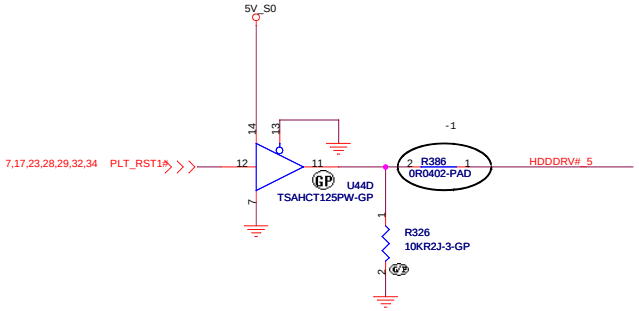



# ODD Connector



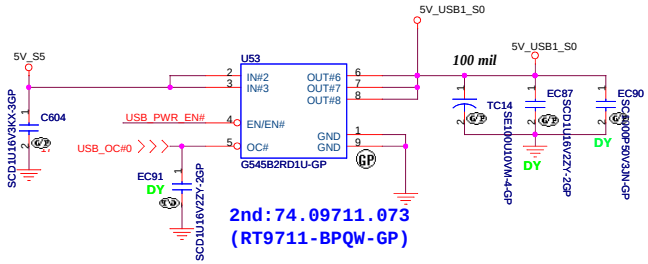



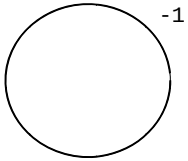



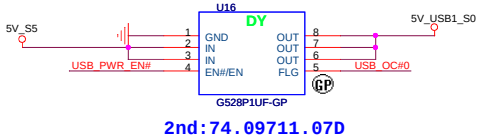




bom1

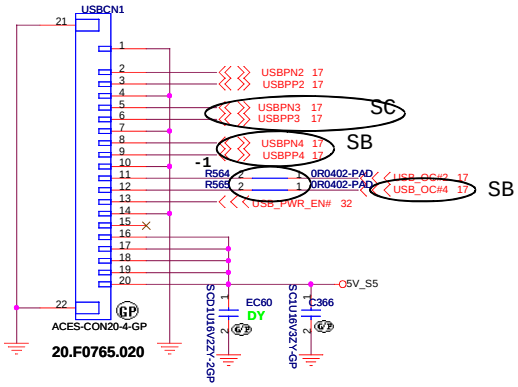
| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | ***HDD and CDROM*** | |
| Size | DocumentNumber<br>**Columbia/Tangiz** | Rev<br>-1M |
| Date: Monday, January 14, 2008 | Sheet 21 of 45 | |

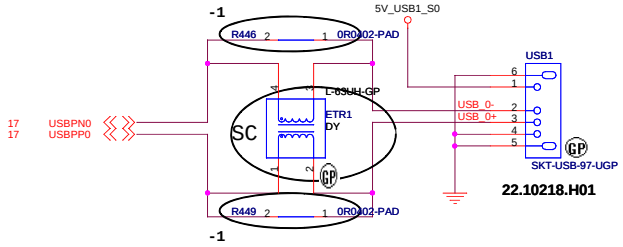


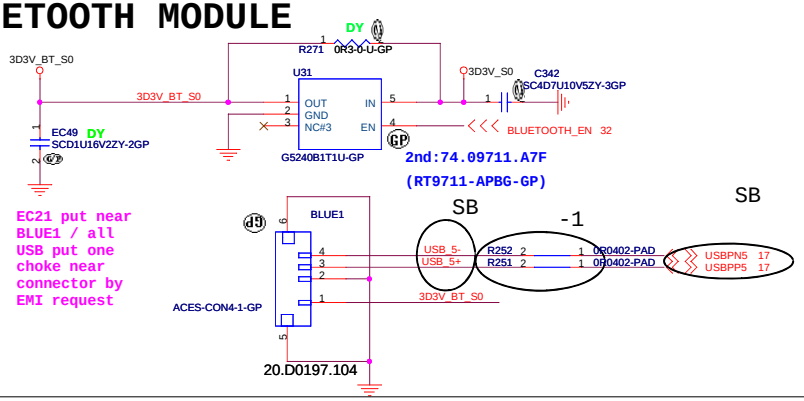




2nd:74.09711.07D
(RT9711-BPS-GP)

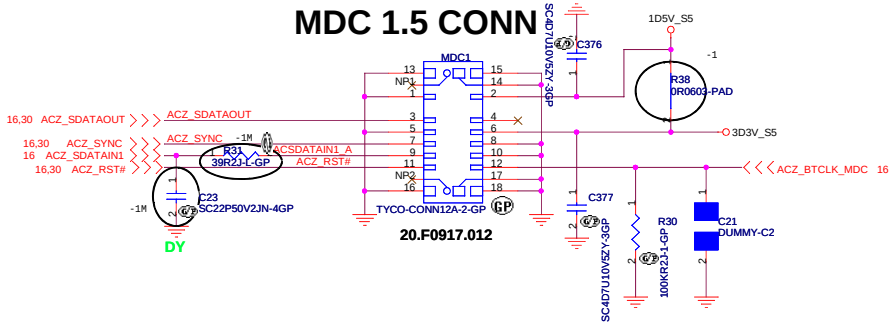


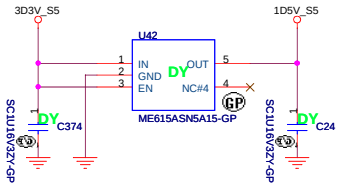




# BLUETOOTH MODULE




# MDC 1.5 CONN



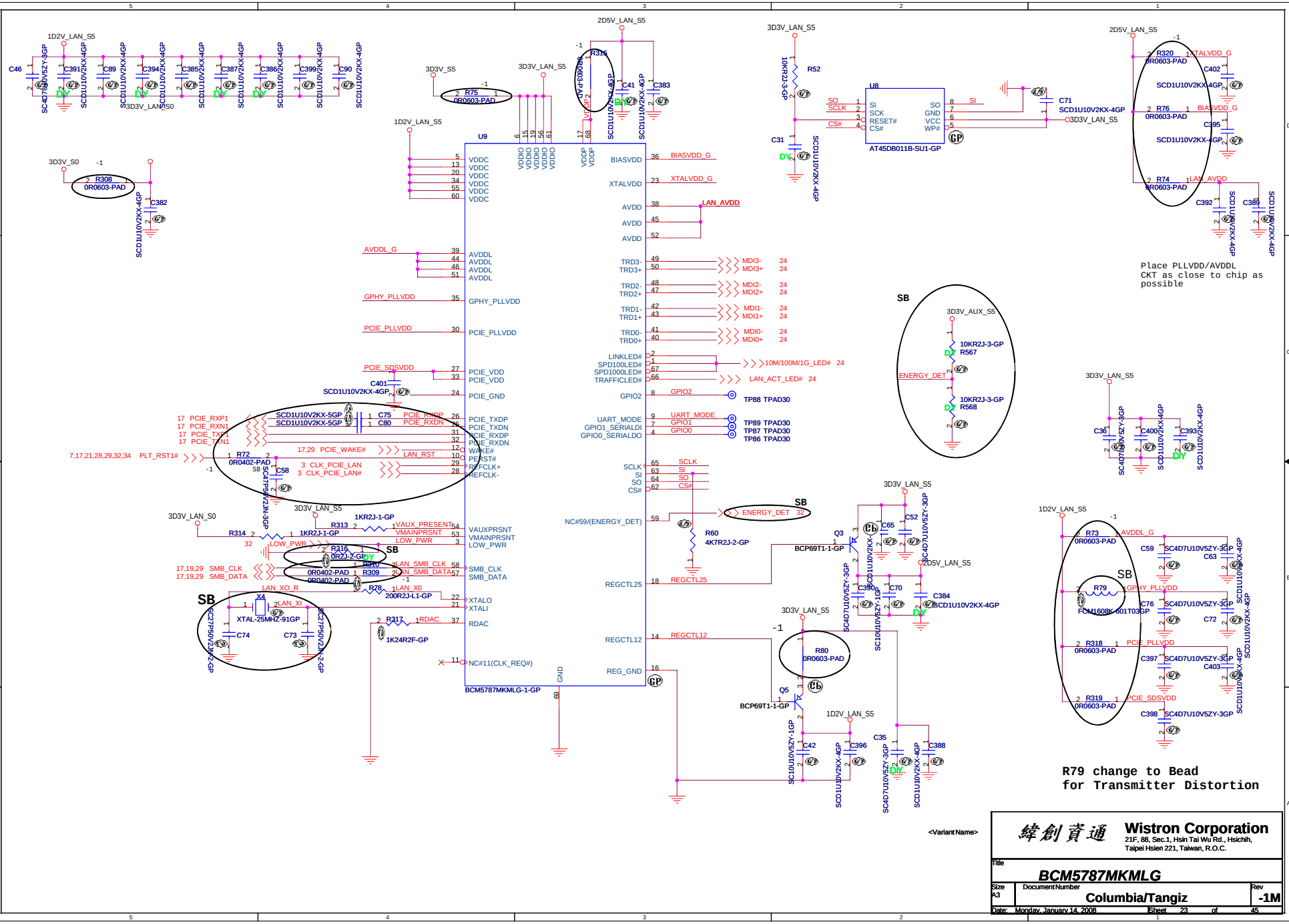

bom1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB / MDC / BLUETOOTH***

| Size | Document Number | Rev |
|---|---|---|
| | Columbia/Tangiz | -1M |

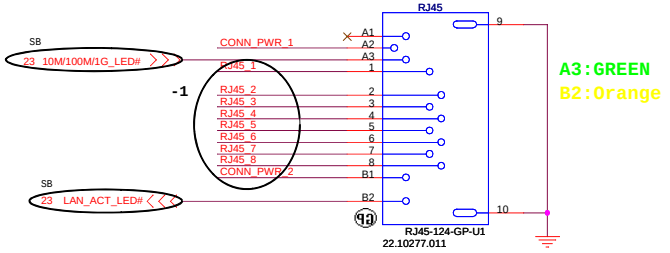
Date: Monday, January 14, 2008 Sheet 22 of 45


U9
BCM5787MKMLG-1-GP
U8
AT45DB011B-SU1-GP
Q3
BCP69T1-1-GP
Q5
BCP69T1-1-GP
Place PLLVDD/AVDDL CKT as close to chip as possible
R79 change to Bead for Transmitter Distortion
<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5787MKMLG
Size A3
Document Number Columbia/Tangiz
Rev -1M
Date: Monday, January 14, 2008
Sheet 23 of 45

# LAN Connector

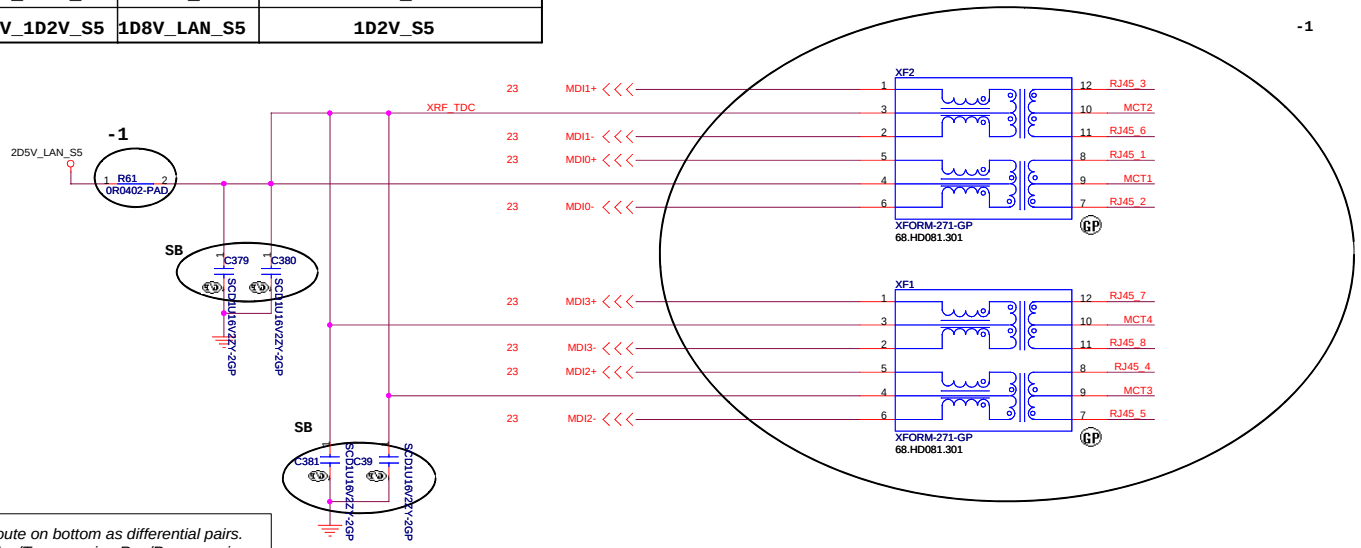
| Voltage Rail | 4401E | 5789 | 5787 |
|---|---|---|---|
| VDDIO_PCI | 3D3V_LAN_S5 | 3D3V_S0 | Don't Care |
| VDDC | 1D8V_LAN_S5 | 1D2V_LAN_S5 | |
| VDDIO | 3D3V_LAN_S5 | 3D3V_LAN_S5 | |
| VESD | 3D3V_LAN_S5 | 3D3V_S0 | Don't Care |
| VDDP | Don't Care | 2D5V_S5 | |
| 3D3V_2D5V_S5 | 3D3V_S5 | 2D5V_S5 | |
| 1D8V_1D2V_S5 | 1D8V_LAN_S5 | 1D2V_S5 | |

*GIGA Lan Transformer*




LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

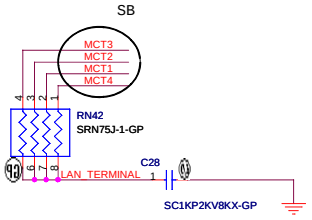


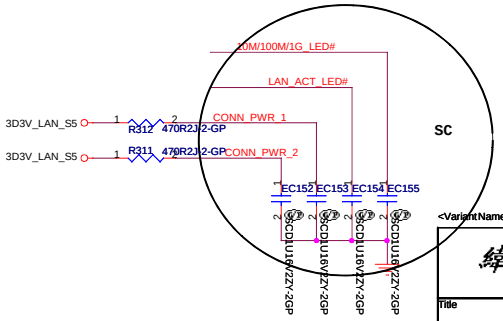

*1.route on bottom as differential pairs.*
*2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.*
*3.No vias, No 90 degree bends.*
*4.pairs must be equal lengths.*
*5.6mil trace width,12mil separation.*
*6.36mil between pairs and any other trace.*
*7.Must not cross ground moat,except RJ-45 moat.*

**RJ11 signal must leave the other signal or power plane 100mil.**

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

| 10/100 LAN Transformer | RJ45 PIN |
|---|---|
| TD+ --> TX+ | RJ45-1 |
| TD- --> TX- | RJ45-2 |
| RD+ --> RX+ | RJ45-3 |
| RD- --> RX- | RJ45-6 |




*CLOSE TO TRANSFORMER*

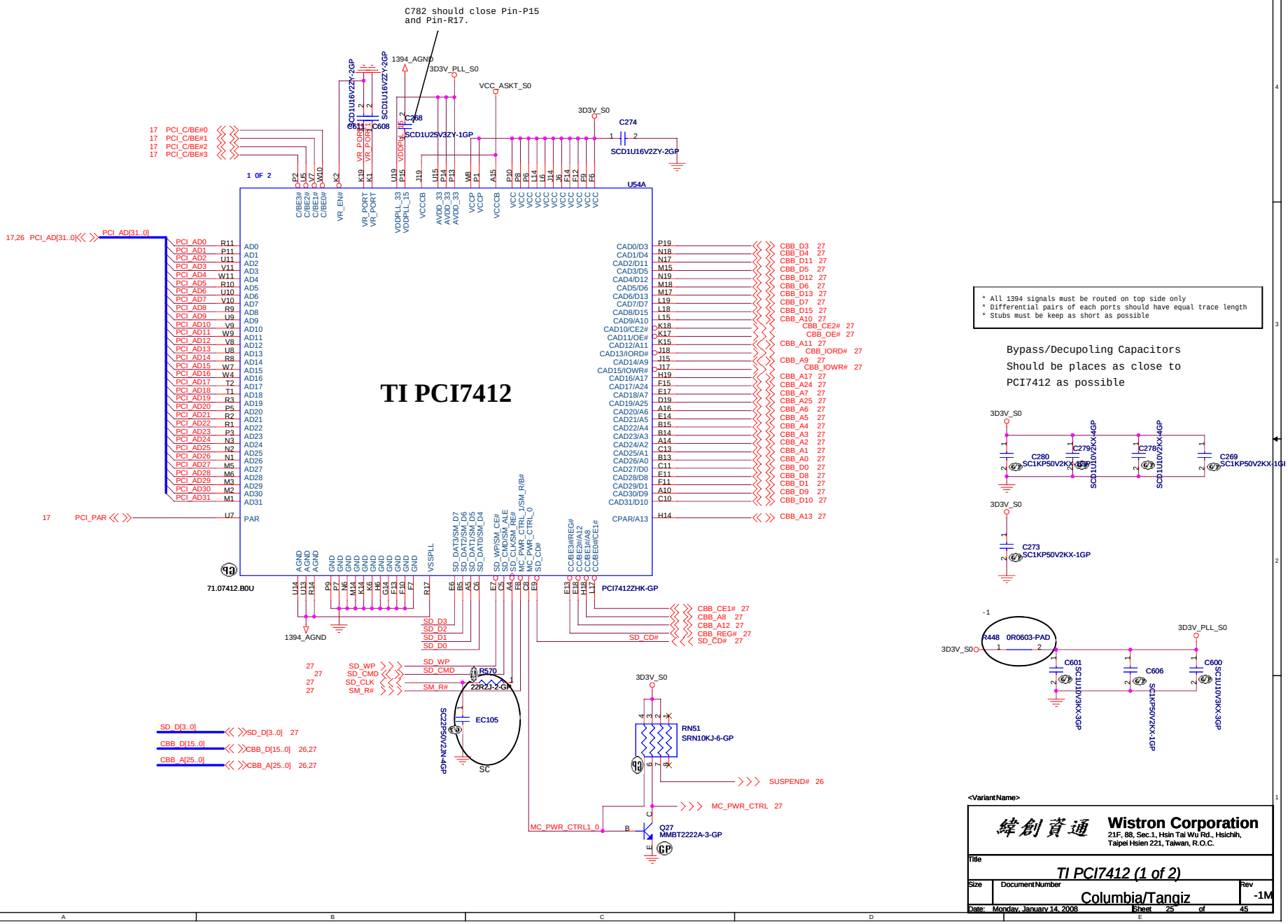
<variant_name>

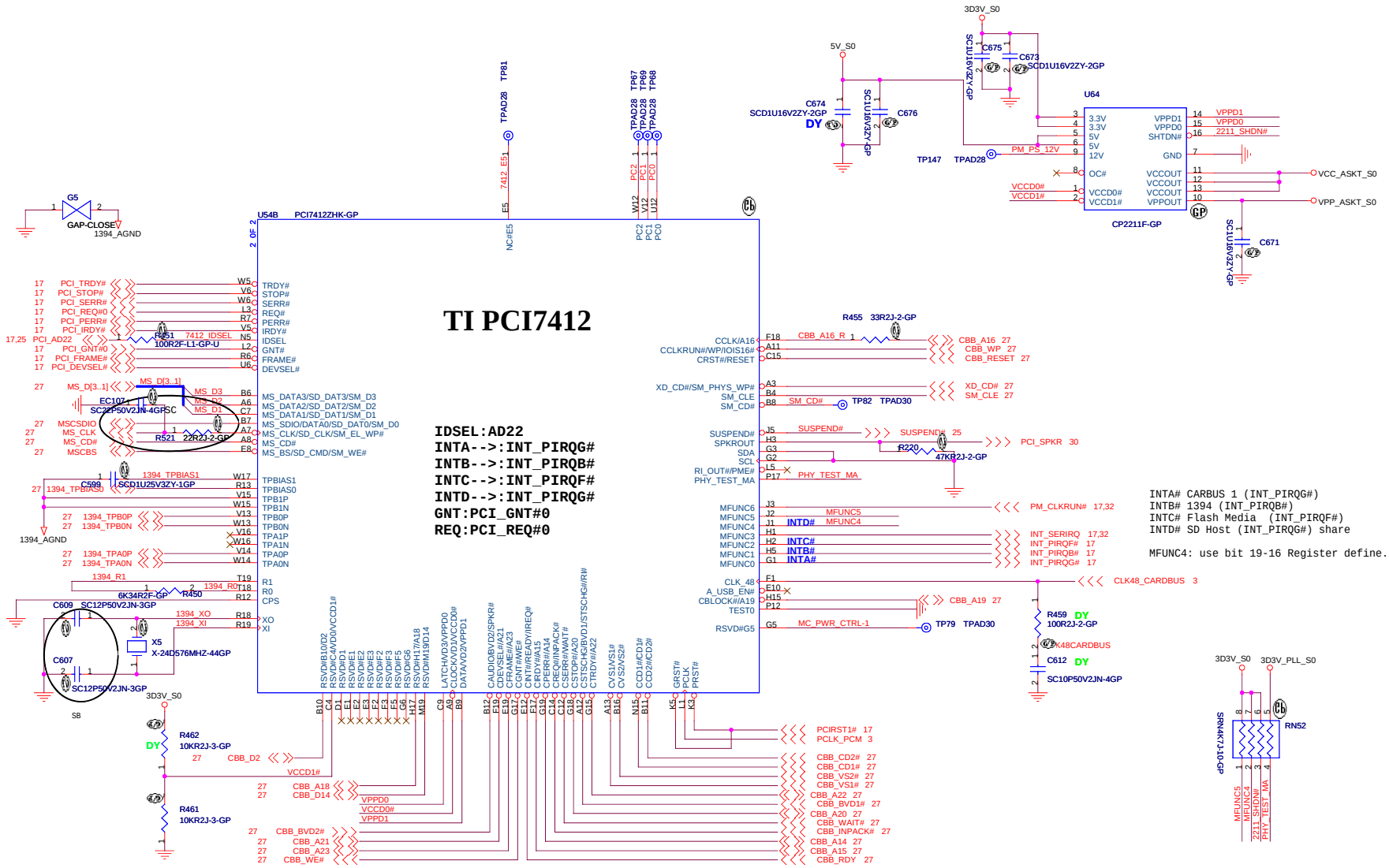
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

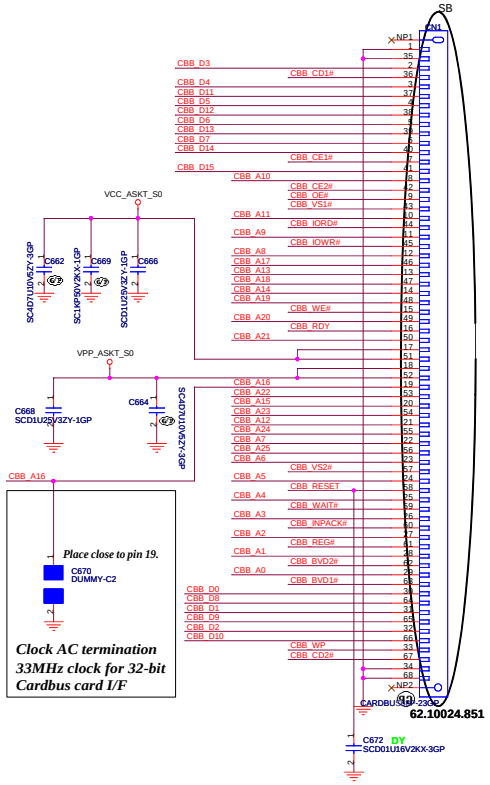
| Size | Document Number | Rev |
|---|---|---|
| A3 | Columbia/Tangiz | -1M |

Date: Monday, January 14, 2008 Sheet 24 of 45

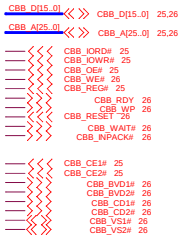

C782 should close Pin-P15
and Pin-R17.
TI PCI7412
U54A
1 OF 2
PCI_AD[31..0]
PCI_C/BE#0
PCI_C/BE#1
PCI_C/BE#2
PCI_C/BE#3
PCI_PAR
71.07412.B0U
PCI7412ZHK-GP
1394_AGND
3D3V_PLL_S0
VCC_ASKT_S0
3D3V_S0
SCD1U16V2ZY-2GP
SCD1U25V3ZY-1GP
SD_D[3..0]
CBB_D[15..0]
CBB_A[25..0]
SD_WP
SD_CMD
SD_CLK
SM_R#
22R2J-2-GP
EC105
RN51
SRN10KJ-6-GP
SUSPEND# 26
MC_PWR_CTRL 27
MC_PWR_CTRL1_0
Q27
MMBT2222A-3-GP
* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible
Bypass/Decupoling Capacitors
Should be places as close to
PCI7412 as possible
R448 0R0603-PAD
<VariantName>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TI PCI7412 (1 of 2)
Size
Document Number
Columbia/Tangiz
Rev
-1M
Date: Monday, January 14, 2008
Sheet 25 of 45

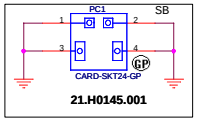

TI PCI7412
IDSEL:AD22
INTA-->:INT_PIRQG#
INTB-->:INT_PIRQB#
INTC-->:INT_PIRQF#
INTD-->:INT_PIRQG#
GNT:PCI_GNT#0
REQ:PCI_REQ#0
INTA# CARBUS 1 (INT_PIRQG#)
INTB# 1394 (INT_PIRQB#)
INTC# Flash Media (INT_PIRQF#)
INTD# SD Host (INT_PIRQG#) share
MFUNC4: use bit 19-16 Register define.
U54B PCI7412ZHK-GP
U64 CP2211F-GP
3D3V_S0
5V_S0
1394_AGND
GAP-CLOSE
X5 X-24D576MHZ-44GP
R455 33R2J-2-GP
R459 DY 100R2J-2-GP
R462 DY 10KR2J-3-GP
R461 10KR2J-3-GP
RN52 SRN4K7J-10-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TI PCI7412 (2 of 2)
Columbia/Tangiz
Size
Document Number
Rev
-1M
Date: Monday, January 14, 2008
Sheet 26 of 45

# PCMCIA Socket

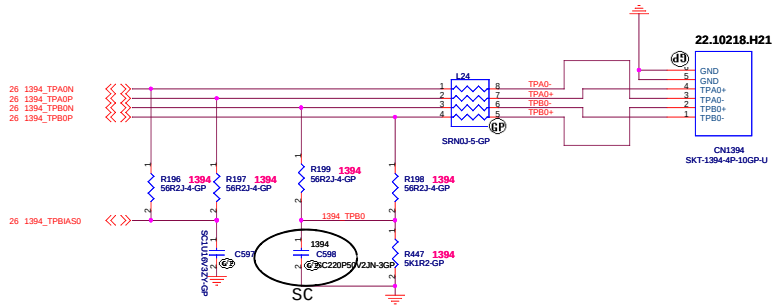


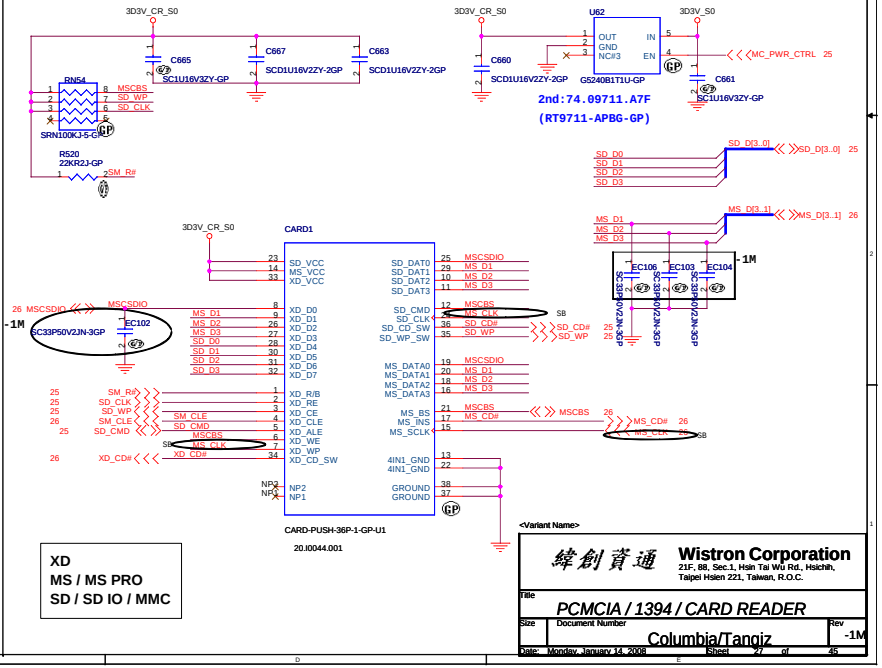

## Cardbus I/F




# 1394 Connector





緯創資通 Wistron Corporation
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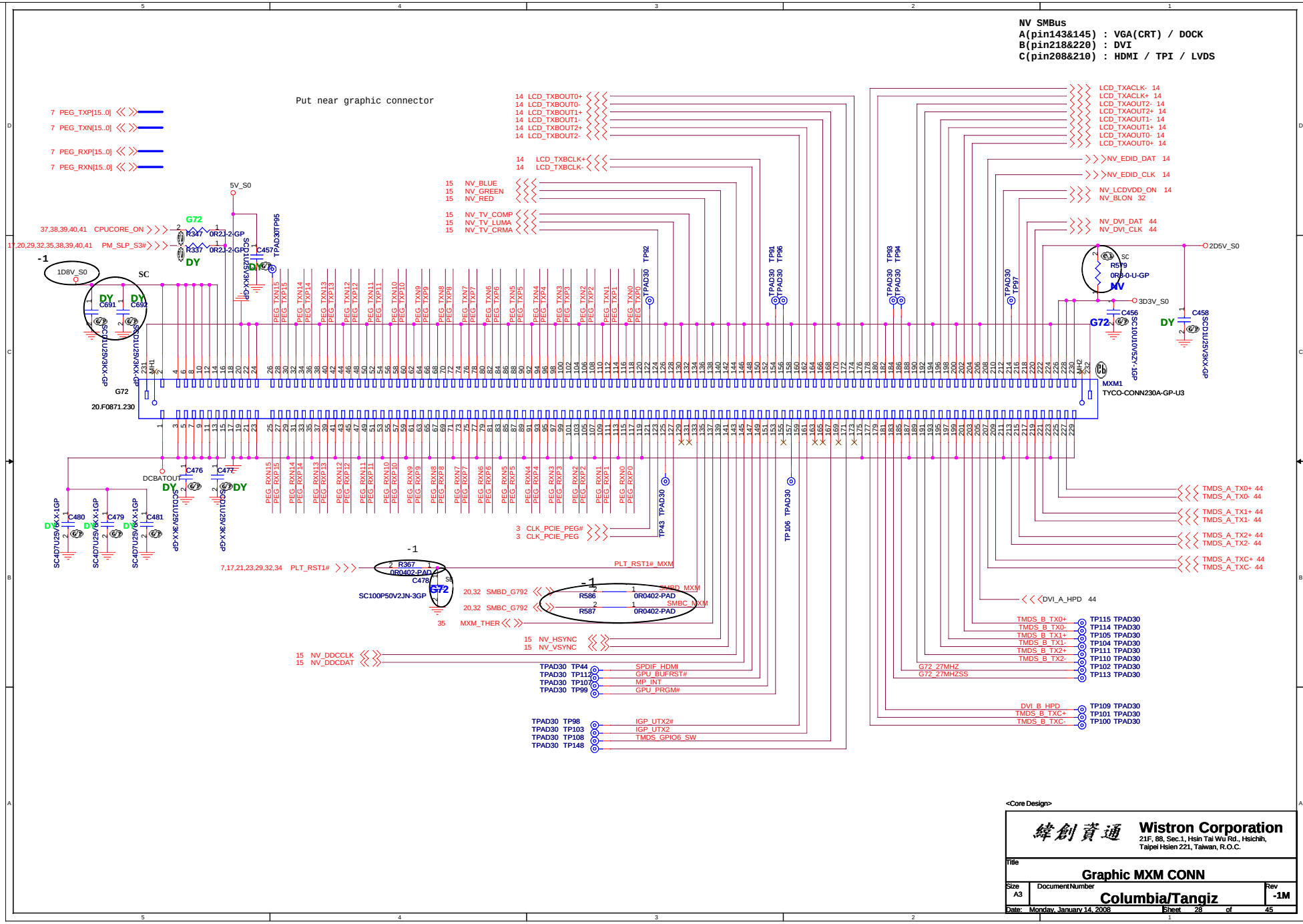
Taipei Hsien 221, Taiwan, R.O.C.


Title: PCMCIA / 1394 / CARD READER

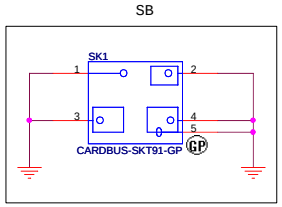
Size | Document Number: Columbia/Tangiz | Rev: -1M

Date: Monday, January 14, 2008 | Sheet 27 of 45

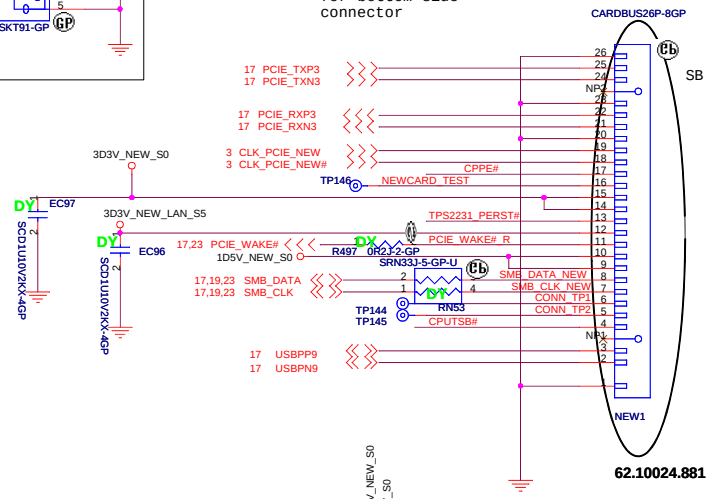

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS
Put near graphic connector
MXM1
TYCO-CONN230A-GP-U3
20.F0871.230
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Graphic MXM CONN
Size A3
Document Number
Columbia/Tangiz
Rev -1M
Date: Monday, January 14, 2008
Sheet 28 of 45

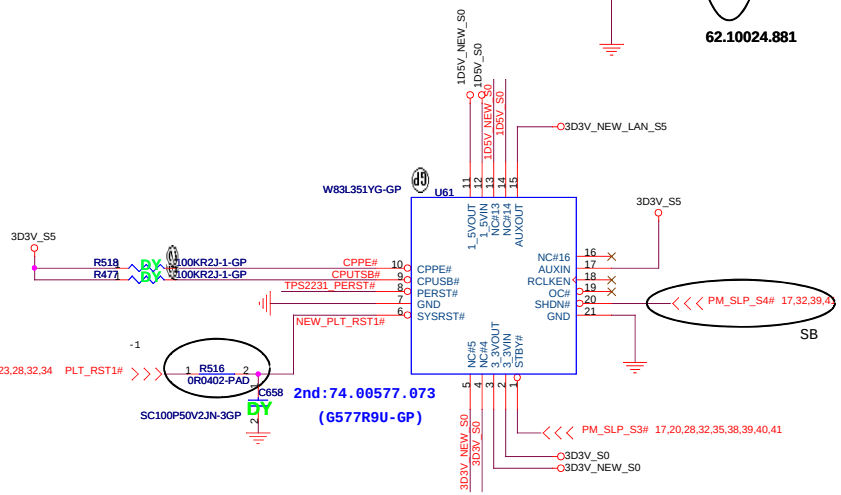
# Mini Card Connector

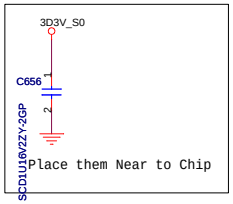
## NEWCARD Connector

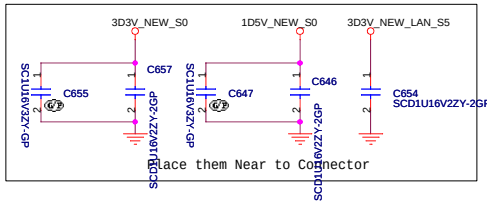


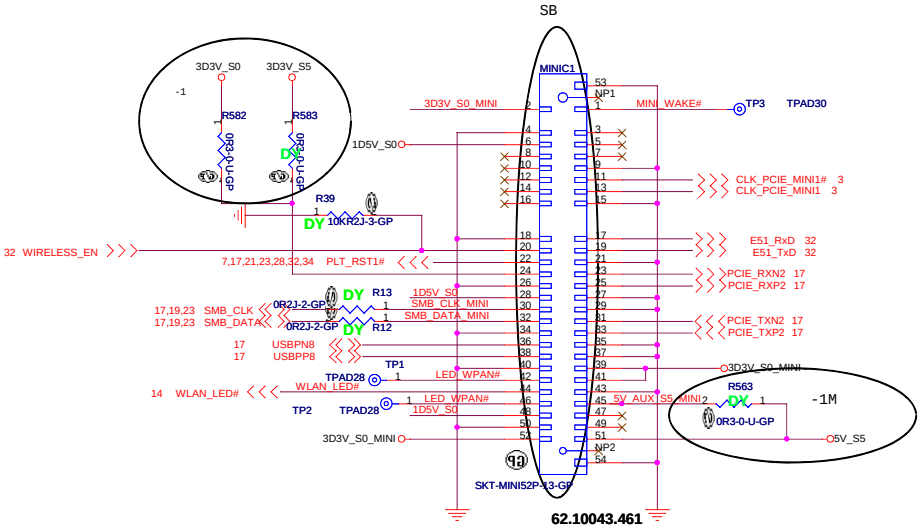

Reserve the symbol for bottom side connector

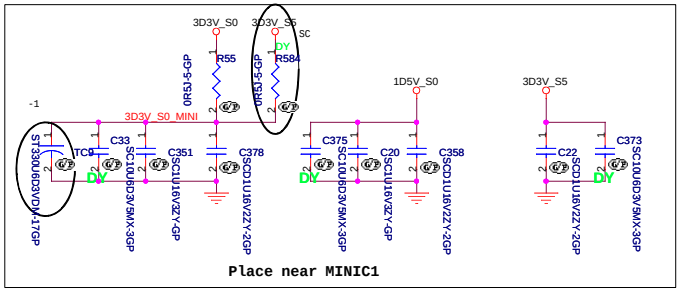


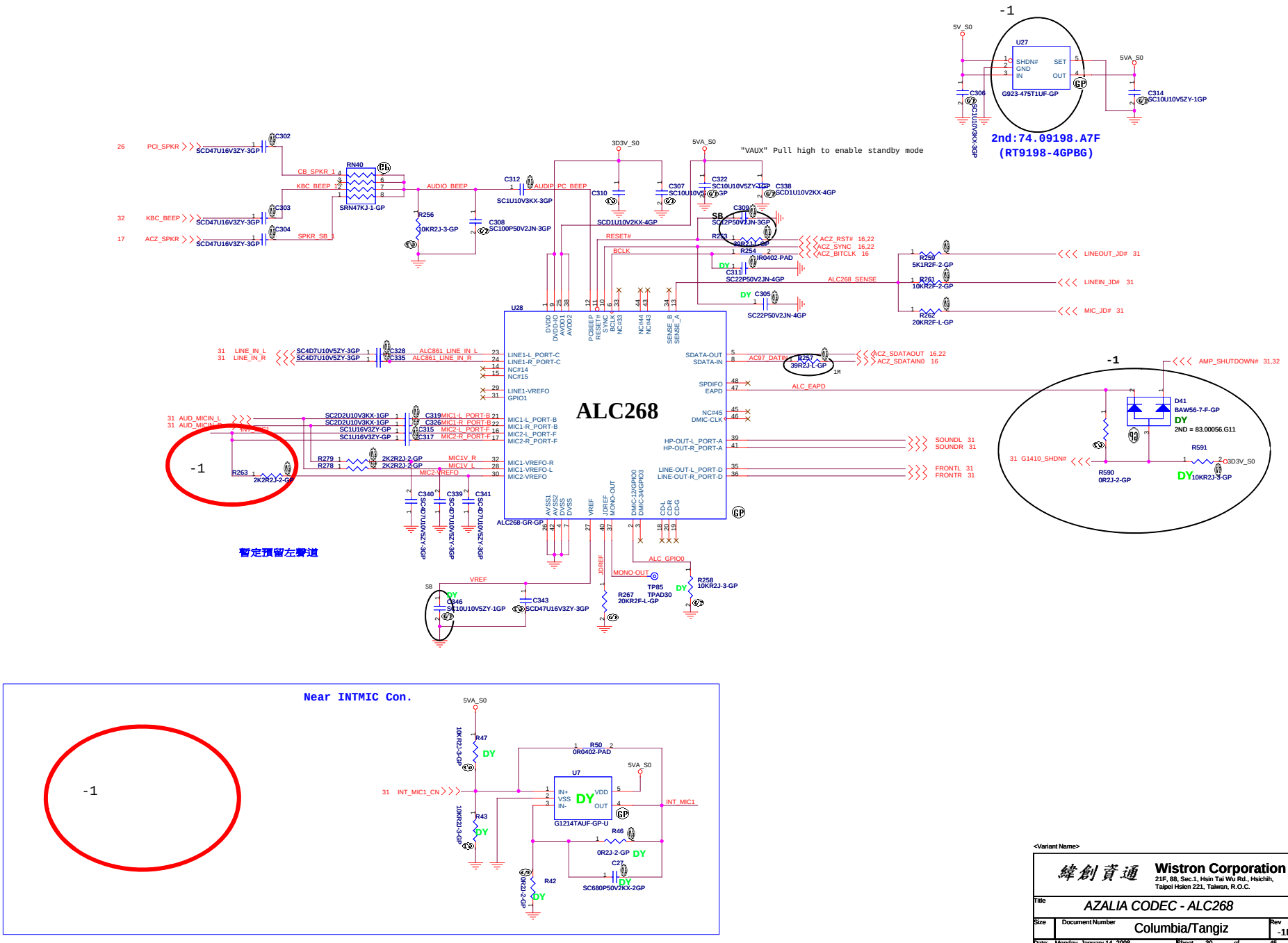




bom1

| | |
|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |
| Title | **MINI CARD / NEW CARD** |
| Size | Document Number: **Columbia/Tangiz** Rev: -1M |
| Date: Monday, January 14, 2008 | Sheet 29 of 45 |





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: AZALIA CODEC - ALC268

Size | Document Number: Columbia/Tangiz | Rev: -1M

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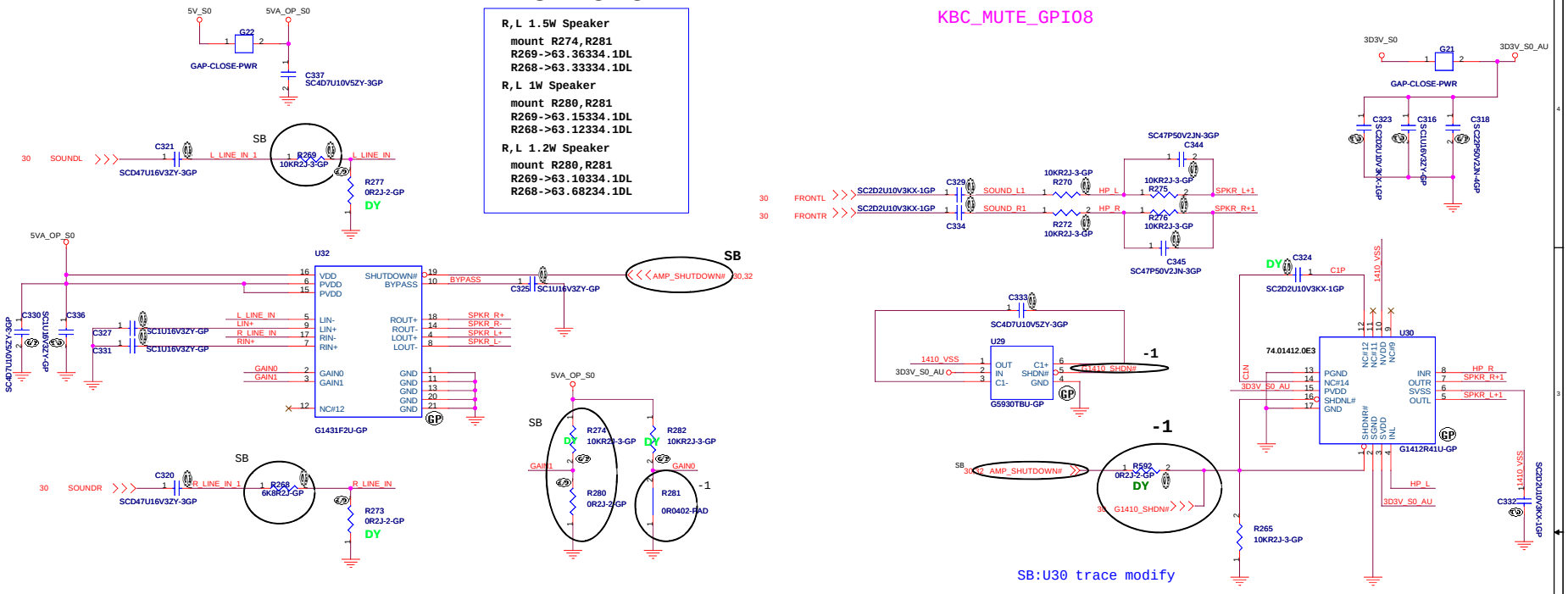
# AUDIO OP AMPLIFIER

**R,L 1.5W Speaker**
mount R274,R281
R269->63.36334.1DL
R268->63.33334.1DL

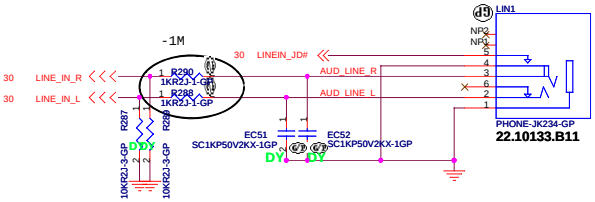
**R,L 1W Speaker**
mount R280,R281
R269->63.15334.1DL
R268->63.12334.1DL

**R,L 1.2W Speaker**
mount R280,R281
R269->63.10334.1DL
R268->63.68234.1DL

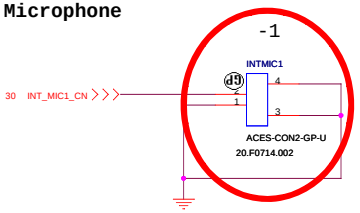
KBC_MUTE_GPIO8



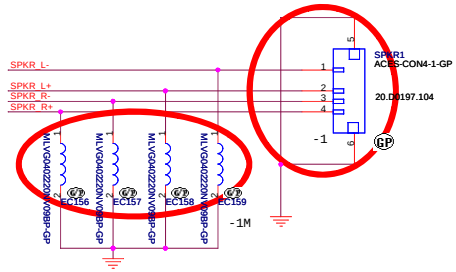

## LINE IN



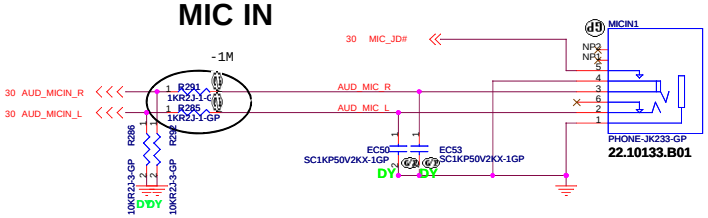

## Internal Microphone



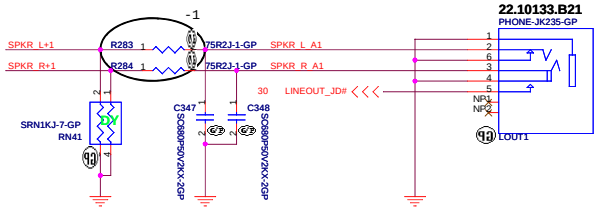

## Internal Speaker




## MIC IN

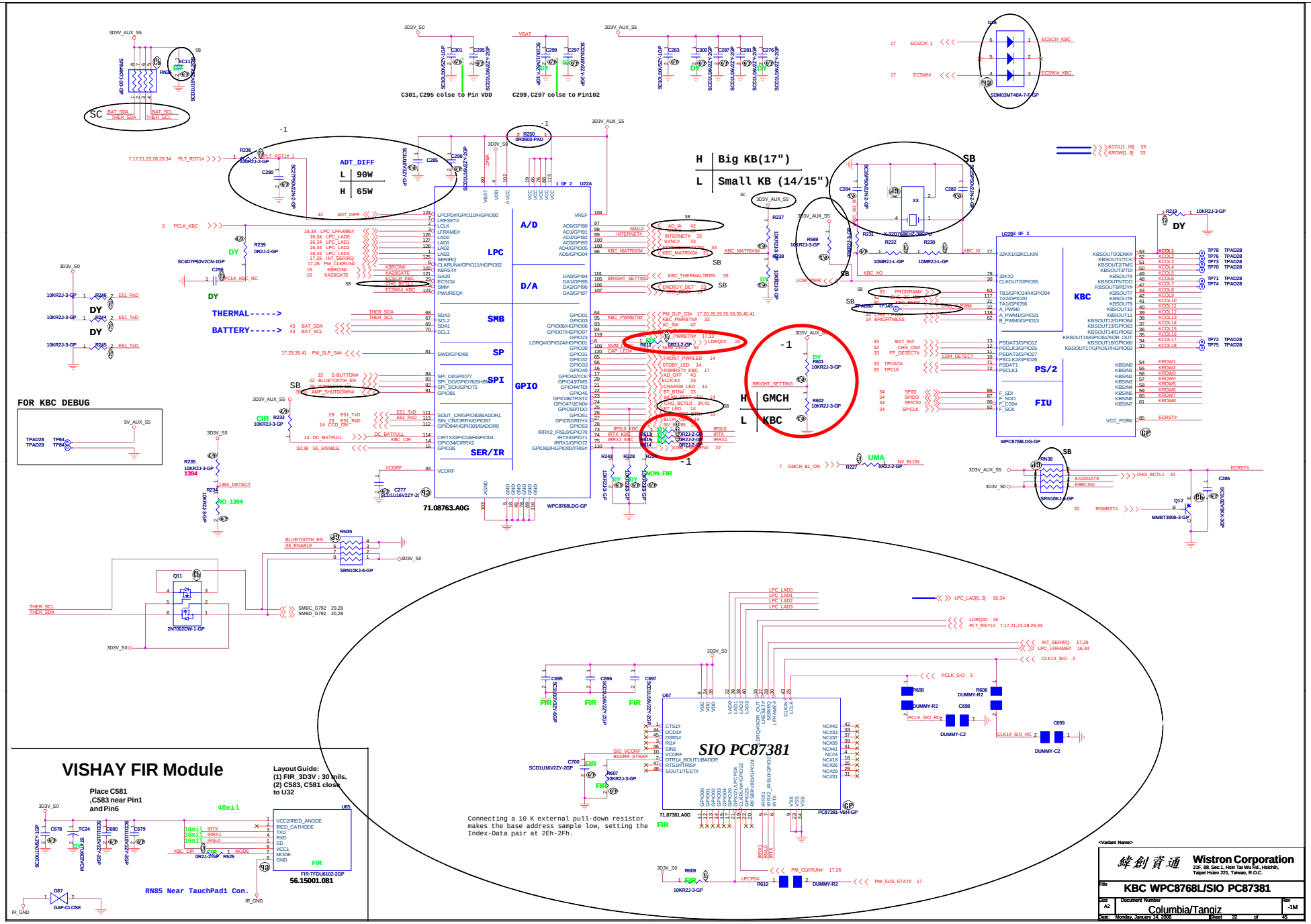


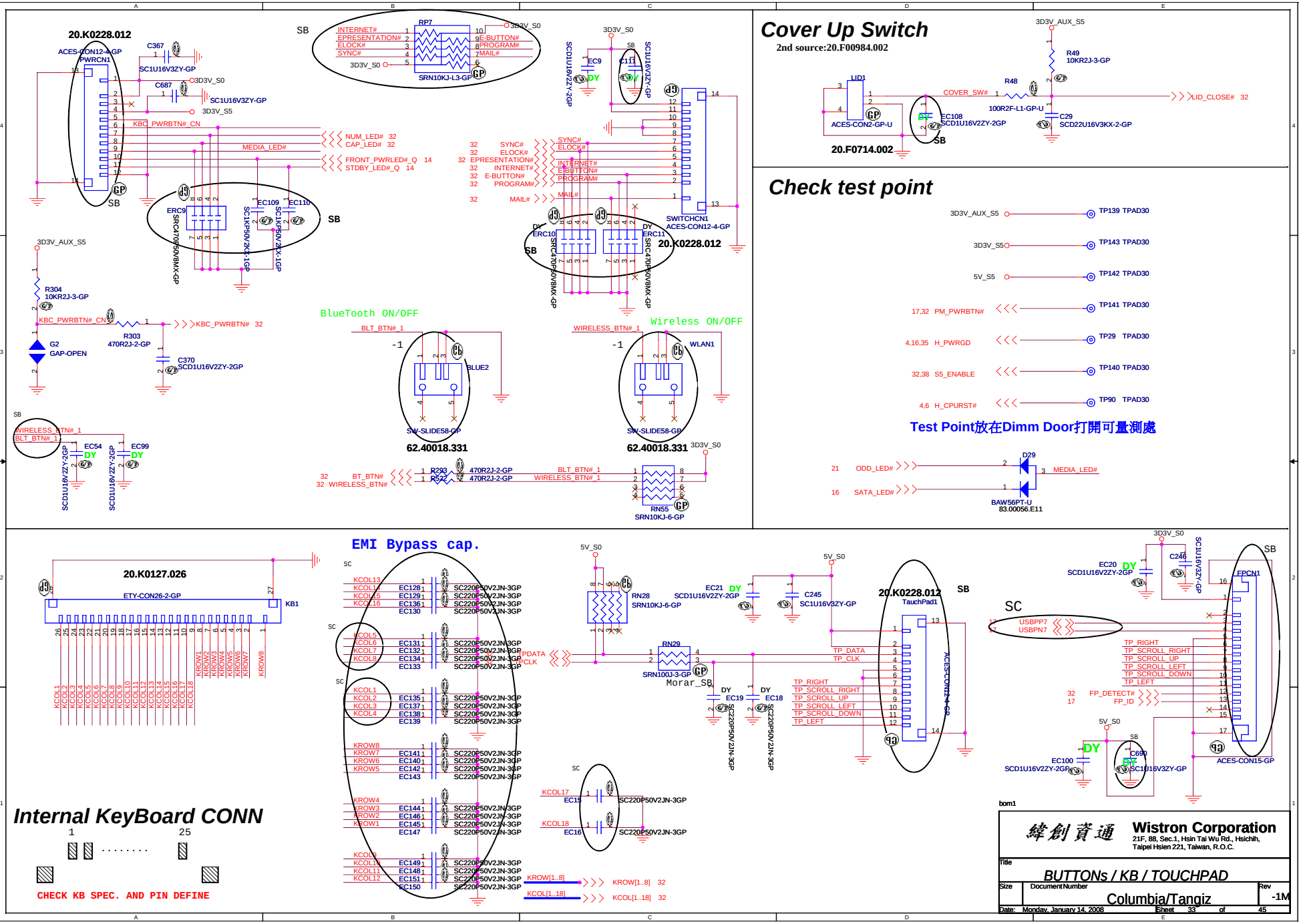

## LINE OUT




<Variant Name>

| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | *AUDIO AMP AND JACK* | |
| Size | Document Number: Columbia/Tangiz | Rev: -1 |
| Date: Monday, January 14, 2008 | Sheet 31 of 45 | |


ADT_DIFF
L 90W
H 65W
H Big KB(17")
L Small KB (14/15")
C301,C295 colse to Pin VDD
C299,C297 colse to Pin102
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
THERMAL----->
BATTERY----->
FOR KBC DEBUG
H GMCH
L KBC
NON_FIR
UMA
71.08763.A0G
WPC8768LDG-GP
SIO PC87381
71.87381.A0G
PC87381-VBH-GP
VISHAY FIR Module
Place C581 ,C583 near Pin1 and Pin6
Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32
RN85 Near TauchPad1 Con.
56.15001.081
Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L/SIO PC87381
Columbia/Tangiz
Monday, January 14, 2008


20.K0228.012
ACES-CON12-4-GP
PWRCN1
C367
SC1U16V3ZY-GP
C687
SC1U16V3ZY-GP
3D3V_S0
3D3V_S5
KBC_PWRBTN#_CN
MEDIA_LED#
NUM_LED# 32
CAP_LED# 32
FRONT_PWRLED#_Q 14
STDBY_LED#_Q 14
SB
ERC9
SRC470P50V8MX-GP
EC109
EC110
SC1KP50V2KX-1GP
RP7
SRN10KJ-L3-GP
INTERNET#
EPRESENTATION#
ELOCK#
SYNC#
E-BUTTON#
PROGRAM#
MAIL#
SC1D1U16V2ZY-2GP
EC9
EC111
SC1U16V3ZY-GP
SWITCHCN1
ACES-CON12-4-GP
ERC10
ERC11
20.K0228.012
3D3V_AUX_S5
R304
10KR2J-3-GP
KBC_PWRBTN#_CN
R303
470R2J-2-GP
KBC_PWRBTN# 32
G2
GAP-OPEN
C370
SCD1U16V2ZY-2GP
WIRELESS_BTN#_1
BLT_BTN#_1
EC54
EC99
SCD1U16V2ZY-2GP
BlueTooth ON/OFF
Wireless ON/OFF
BLUE2
WLAN1
SW-SLIDE58-GP
62.40018.331
BT_BTN#
WIRELESS_BTN#
R293
R522
470R2J-2-GP
RN55
SRN10KJ-6-GP
Cover Up Switch
2nd source:20.F00984.002
LID1
ACES-CON2-GP-U
COVER_SW#
R48
100R2F-L1-GP-U
R49
10KR2J-3-GP
EC108
SCD1U16V2ZY-2GP
C29
SCD22U16V3KX-2GP
LID_CLOSE# 32
20.F0714.002
Check test point
TP139 TPAD30
TP143 TPAD30
TP142 TPAD30
TP141 TPAD30
TP29 TPAD30
TP140 TPAD30
TP90 TPAD30
17,32 PM_PWRBTN#
4,16,35 H_PWRGD
32,38 S5_ENABLE
4,6 H_CPURST#
Test Point放在Dimm Door打開可量測處
D29
BAW56PT-U
83.00056.E11
ODD_LED#
SATA_LED#
MEDIA_LED#
20.K0127.026
ETY-CON26-2-GP
KB1
EMI Bypass cap.
SC220P50V2JN-3GP
RN28
SRN10KJ-6-GP
RN29
SRN100J-3-GP
Morar_SB
EC21
SCD1U16V2ZY-2GP
C245
SC1U16V3ZY-GP
EC19
EC18
20.K0228.012
TauchPad1
ACES-CON15-GP
TP_DATA
TP_CLK
TP_RIGHT
TP_SCROLL_RIGHT
TP_SCROLL_UP
TP_SCROLL_LEFT
TP_SCROLL_DOWN
TP_LEFT
PDATA
PCLK
KROW[1..8]
KCOL[1..18]
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
EC20
SCD1U16V2ZY-2GP
C246
SC1U16V3ZY-GP
FPCN1
USBPP7
USBPN7
FP_DETECT#
FP_ID
EC100
SCD1U16V2ZY-2GP
C690
SC1U16V3ZY-GP
ACES-CON15-GP
bom1
緯創資通
Wistron Corporation
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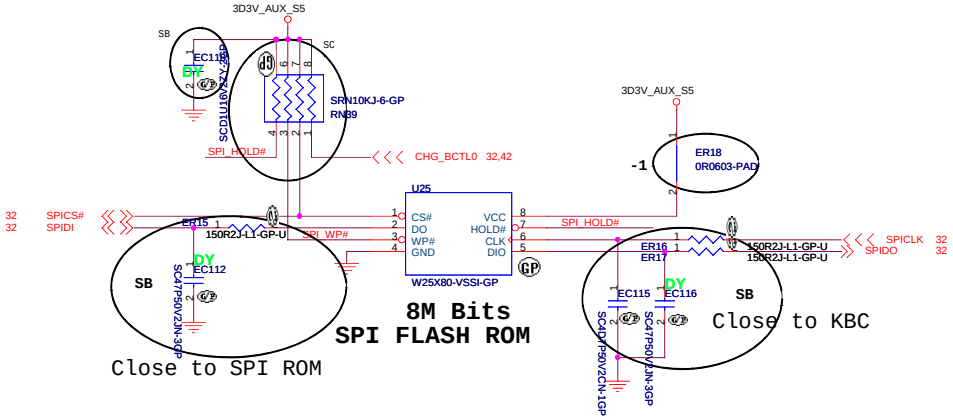
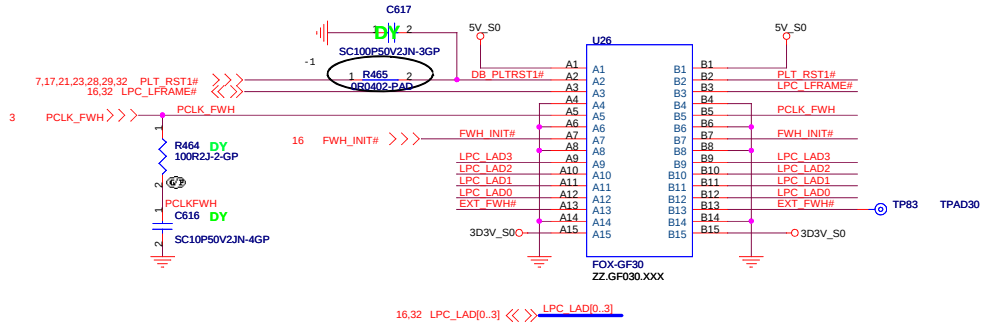
Taipei Hsien 221, Taiwan, R.O.C.
Title
BUTTONs / KB / TOUCHPAD
Size
Document Number
Columbia/Tangiz
Rev
-1M
Date: Monday, January 14, 2008
Sheet 33 of 45



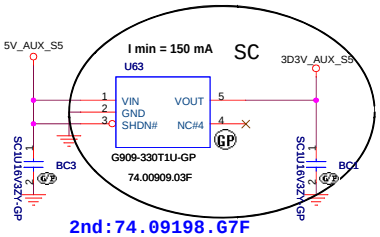

## GOLDEN FINGER FOR DEBUG BOARD

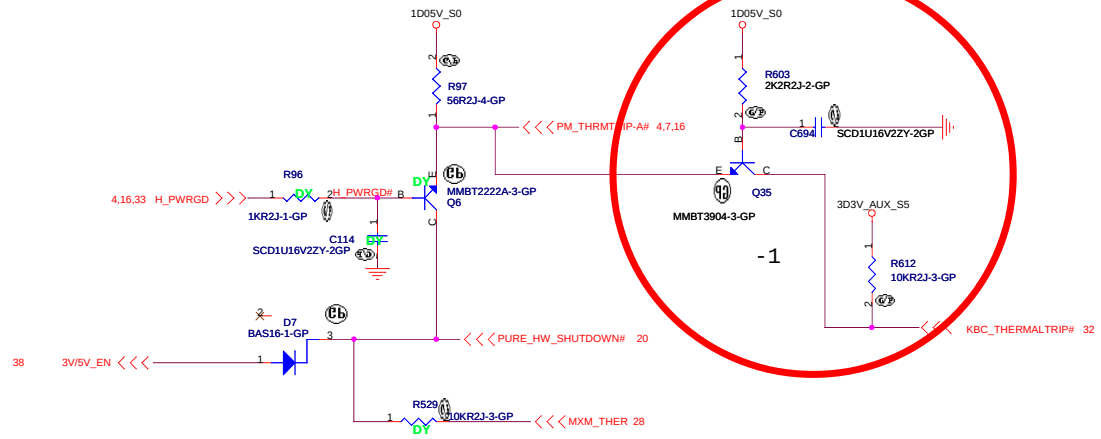



<VariantName>

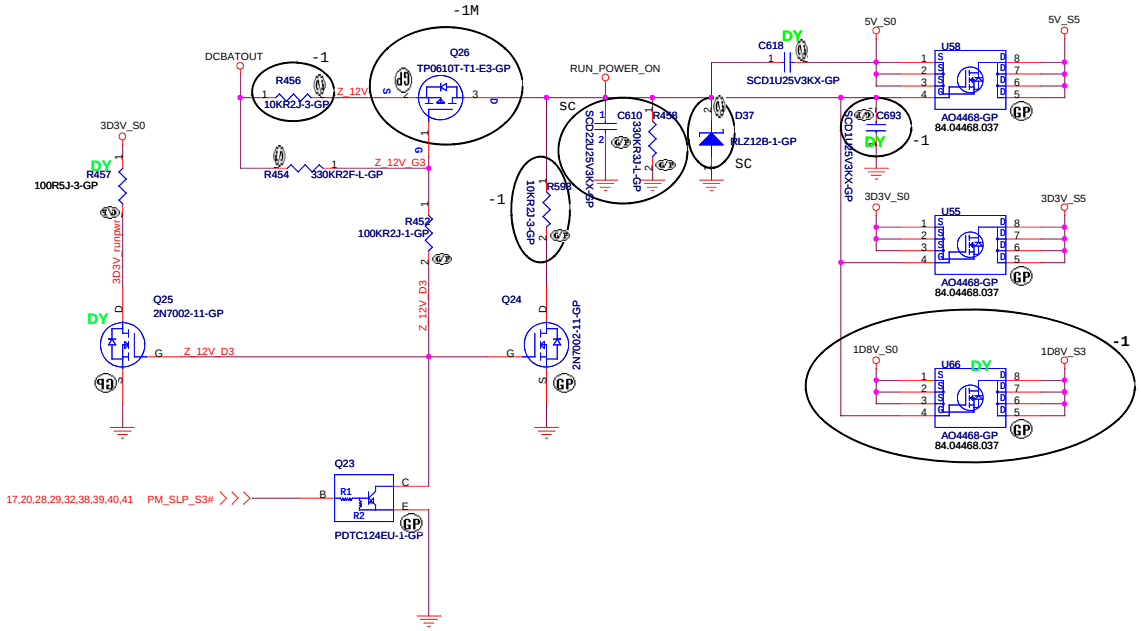
| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title: BIOS | | |
| Size: A3 | Document Number: Columbia/Tangiz | Rev: -1M |
| Date: Monday, January 14, 2008 | Sheet 34 of 45 | |

# Aux Power 3D3V_AUX_S5



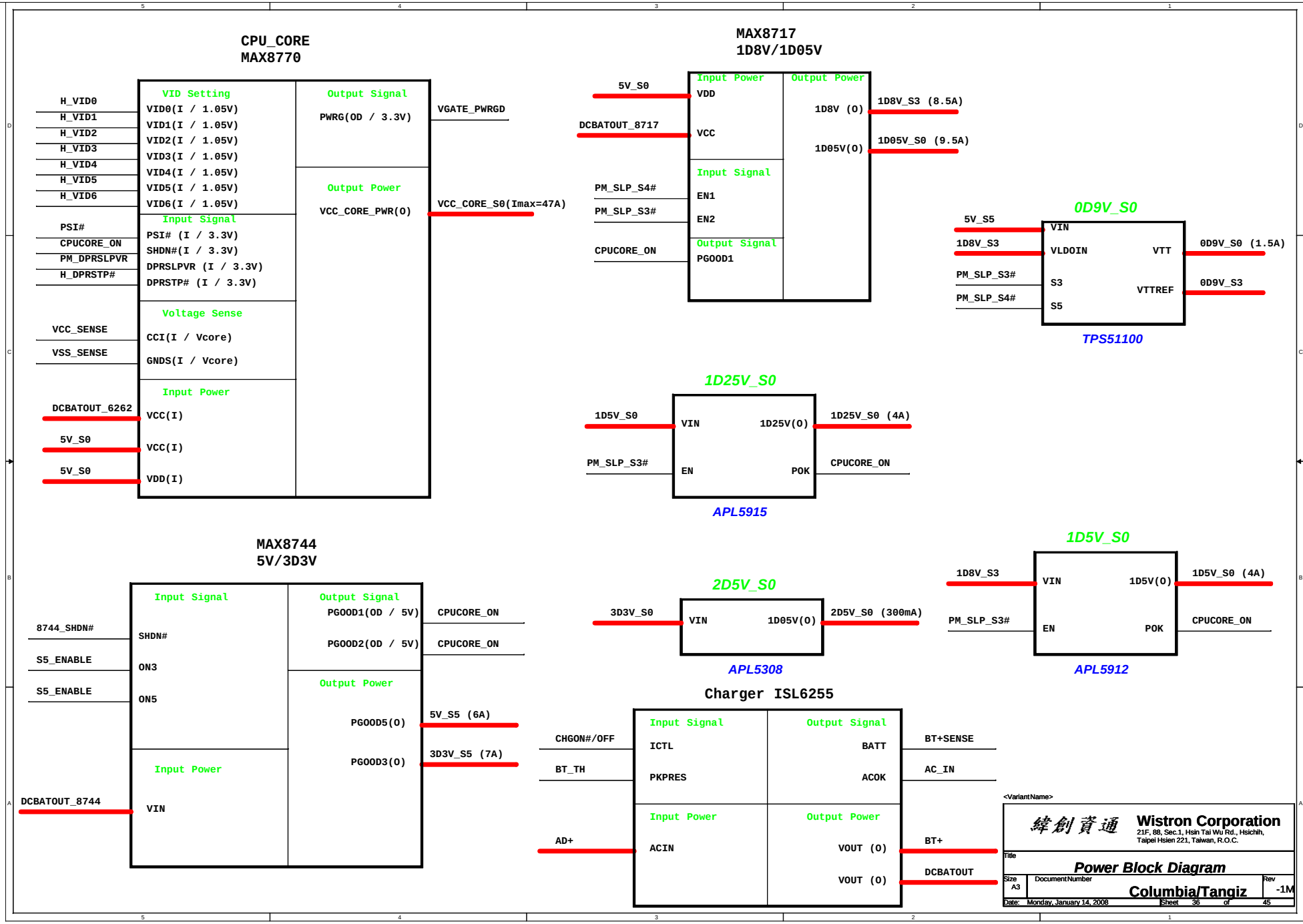



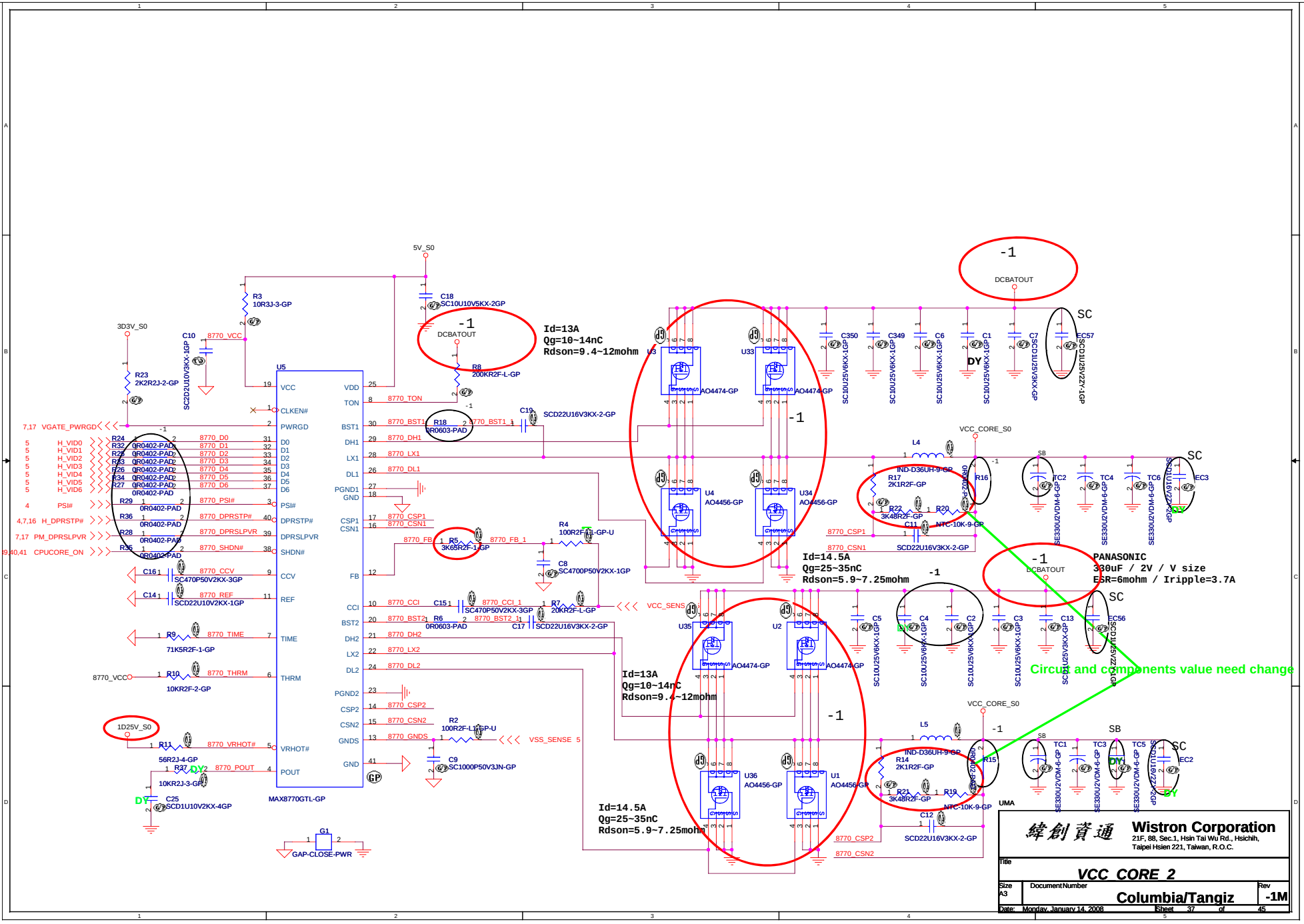

# Run Power




UMA

| | | |
|---|---|---|
| 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: RUN POWER and 3D3V_AUX_S5 | | |
| Size | Document Number: Columbia/Tangiz | Rev: -1M |
| Date: Monday, January 14, 2008 | Sheet 35 of 45 | |


CPU_CORE
MAX8770
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
VID Setting
VID0(I / 1.05V)
VID1(I / 1.05V)
VID2(I / 1.05V)
VID3(I / 1.05V)
VID4(I / 1.05V)
VID5(I / 1.05V)
VID6(I / 1.05V)
Output Signal
PWRG(OD / 3.3V)
VGATE_PWRGD
Output Power
VCC_CORE_PWR(O)
VCC_CORE_S0(Imax=47A)
PSI#
CPUCORE_ON
PM_DPRSLPVR
H_DPRSTP#
Input Signal
PSI# (I / 3.3V)
SHDN#(I / 3.3V)
DPRSLPVR (I / 3.3V)
DPRSTP# (I / 3.3V)
VCC_SENSE
VSS_SENSE
Voltage Sense
CCI(I / Vcore)
GNDS(I / Vcore)
DCBATOUT_6262
5V_S0
5V_S0
Input Power
VCC(I)
VCC(I)
VDD(I)
MAX8717
1D8V/1D05V
5V_S0
DCBATOUT_8717
Input Power
VDD
VCC
Output Power
1D8V (O)
1D05V(O)
1D8V_S3 (8.5A)
1D05V_S0 (9.5A)
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON
Input Signal
EN1
EN2
Output Signal
PGOOD1
0D9V_S0
5V_S5
1D8V_S3
PM_SLP_S3#
PM_SLP_S4#
VIN
VLDOIN
S3
S5
VTT
VTTREF
0D9V_S0 (1.5A)
0D9V_S3
TPS51100
1D25V_S0
1D5V_S0
PM_SLP_S3#
VIN
EN
1D25V(O)
POK
1D25V_S0 (4A)
CPUCORE_ON
APL5915
MAX8744
5V/3D3V
8744_SHDN#
S5_ENABLE
S5_ENABLE
DCBATOUT_8744
Input Signal
SHDN#
ON3
ON5
Input Power
VIN
Output Signal
PGOOD1(OD / 5V)
PGOOD2(OD / 5V)
CPUCORE_ON
CPUCORE_ON
Output Power
PGOOD5(O)
PGOOD3(O)
5V_S5 (6A)
3D3V_S5 (7A)
2D5V_S0
3D3V_S0
VIN
1D05V(O)
2D5V_S0 (300mA)
APL5308
1D5V_S0
1D8V_S3
PM_SLP_S3#
VIN
EN
1D5V(O)
POK
1D5V_S0 (4A)
CPUCORE_ON
APL5912
Charger ISL6255
CHGON#/OFF
BT_TH
AD+
Input Signal
ICTL
PKPRES
Input Power
ACIN
Output Signal
BATT
ACOK
Output Power
VOUT (O)
VOUT (O)
BT+SENSE
AC_IN
BT+
DCBATOUT
<VariantName>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Block Diagram
Size A3
Document Number
Columbia/Tangiz
Rev -1M
Date: Monday, January 14, 2008
Sheet 36 of 45


5V_S0
3D3V_S0
1D25V_S0
8770_VCC
U5
MAX8770GTL-GP
VCC
VDD
CLKEN#
PWRGD
D0
D1
D2
D3
D4
D5
D6
PSI#
DPRSTP#
DPRSLPVR
SHDN#
CCV
REF
TIME
THRM
VRHOT#
POUT
TON
BST1
DH1
LX1
DL1
PGND1
GND
CSP1
CSN1
FB
CCI
BST2
DH2
LX2
DL2
PGND2
CSP2
CSN2
GNDS
GAP-CLOSE-PWR
DCBATOUT
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
AO4474-GP
AO4456-GP
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
VCC_CORE_S0
IND-D36UH-9-GP
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
Circuit and components value need change
UMA
DY
SB
SC
VCC_SENS
VSS_SENSE
Wistron Corporation
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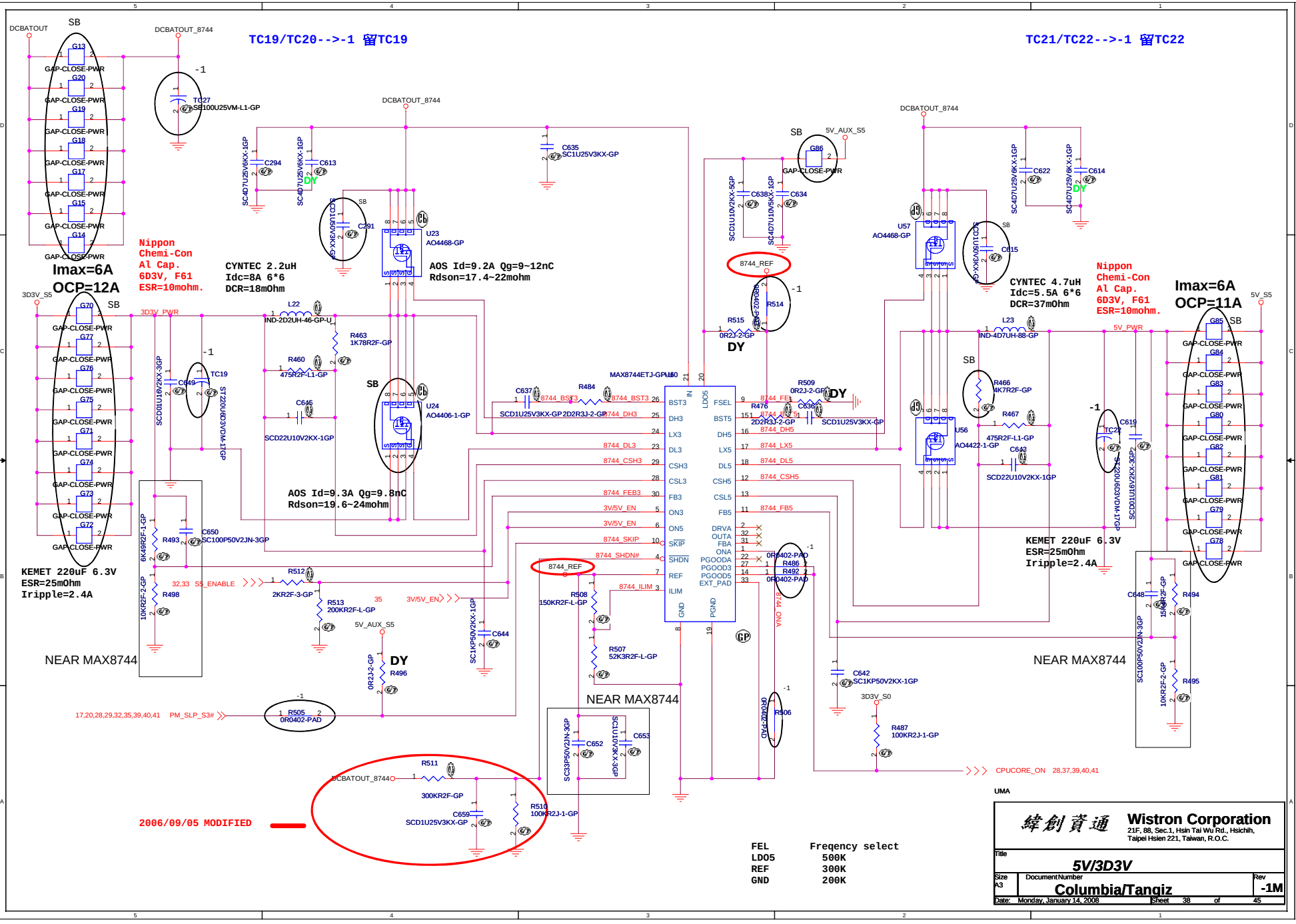
Taipei Hsien 221, Taiwan, R.O.C.
VCC_CORE_2
Columbia/Tangiz
-1M
Monday, January 14, 2008


TC19/TC20-->-1 留TC19
TC21/TC22-->-1 留TC22
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
Imax=6A OCP=12A
CYNTEC 2.2uH Idc=8A 6*6 DCR=18mOhm
AOS Id=9.2A Qg=9~12nC Rdson=17.4~22mohm
AOS Id=9.3A Qg=9.8nC Rdson=19.6~24mohm
KEMET 220uF 6.3V ESR=25mOhm Iripple=2.4A
CYNTEC 4.7uH Idc=5.5A 6*6 DCR=37mOhm
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
Imax=6A OCP=11A
KEMET 220uF 6.3V ESR=25mOhm Iripple=2.4A
NEAR MAX8744
NEAR MAX8744
NEAR MAX8744
MAX8744ETJ-GPU60
2006/09/05 MODIFIED
FEL Freqency select
LDO5 500K
REF 300K
GND 200K
UMA
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5V/3D3V
Columbia/Tangiz
-1M
Monday, January 14, 2008
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45

TC15/TC16-->-1 留TC15

TC17/TC18-->-1 留TC17

1D05V Iomax=12A
OCP>19A

Vcal.=1.0511V

Rs2 = L / DCR / Cs2

CYNTEC 1uH
Idc=11A, Isat=22A
DCR=9mOhm

Id=13A
Qg=10~14nC,
Rdson=9.4~12mohm

Id=14.5A
Qg=25~35nC,
Rdson=13.5~16.5mohm

Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm

Id=9.6A
Qg=18nC,
Rdson=13.5~16.5mohm

1D8V Iomax=9.5A
OCP>17A

Vcal.=1.8V

CYNTEC 2.2uH
Irms=14A Isat=16A
DCR=5.8~7mOhm

Rs1 = L / DCR / Cs1

Vout=(1+Ra/Rb)*1

Panasonic 330uF
2.5V ESR=15mOhm
Iripple=3.1A

Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm

2006.0928 add

Panasonic 220uF
2.5V ESR=25mOhm
Iripple=1.8A

Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm

Vout=(1+(Rc/Rd))*1

SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping

FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz

Adjust the current limit threshold from R14, R15

VILIM = 0.5V~2.0V

Output Current =
ILIM / 10 / LDCR - dI/2

MAX8717ETI-T-GP

UMA

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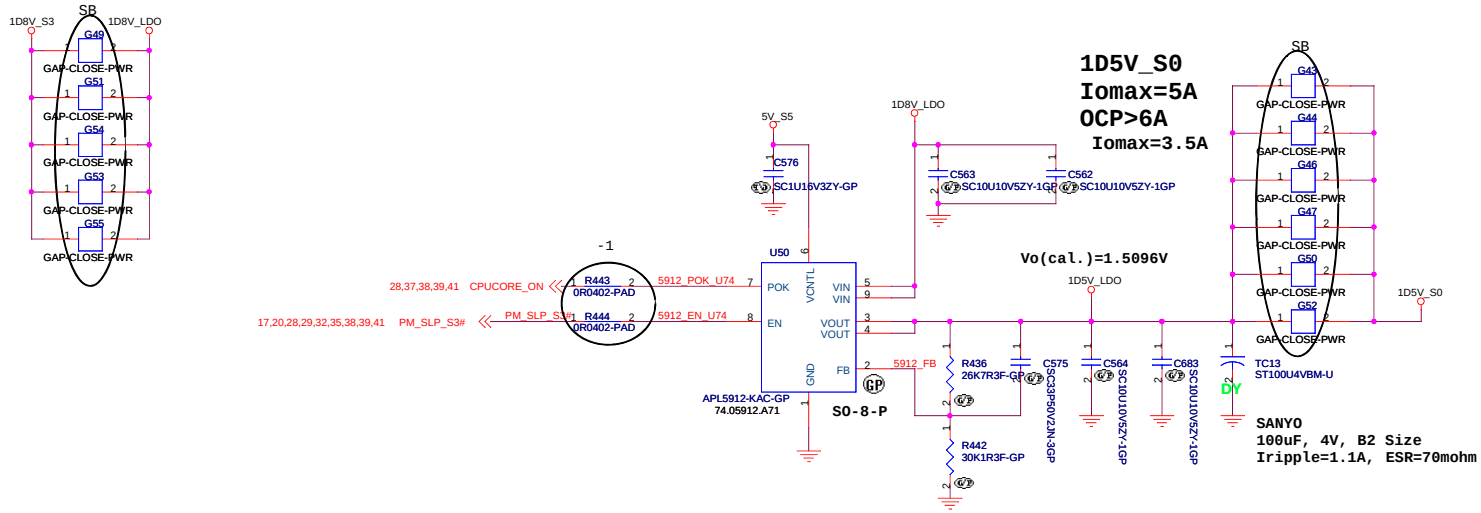
Title: MAX8717_1D8V_1D05V

Size: A3 | Document Number: Columbia/Tangiz | Rev: -1M

Date: Monday, January 14, 2008 | Sheet 39 of 45




UMA

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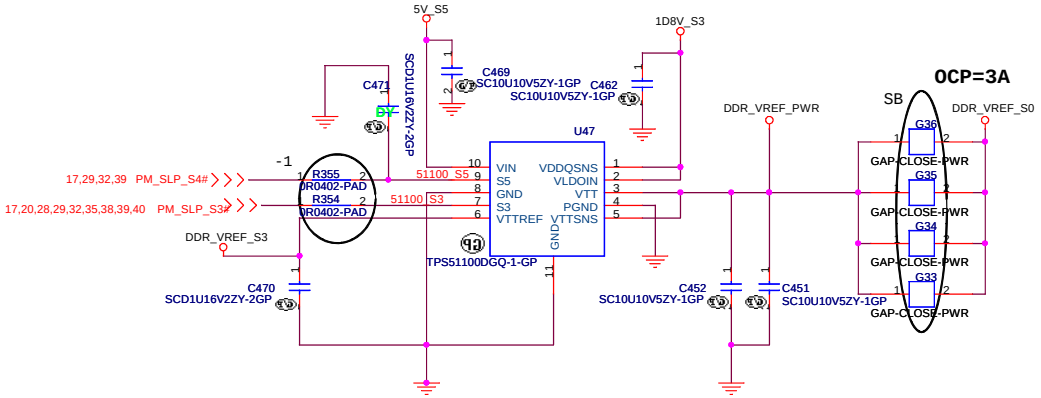
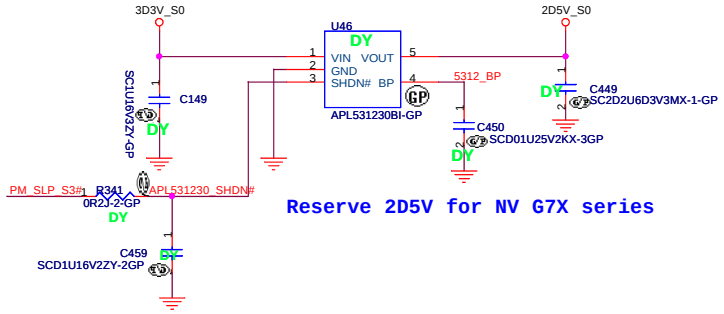
| | | |
|---|---|---|
| Title | ***APW5912_1D5V*** | |
| Size | Document Number **Columbia/Tangiz** | Rev -1M |
| Date: Monday, January 14, 2008 | Sheet 40 of 45 | |

## 0D9V_S3
## Iomax=1.2A

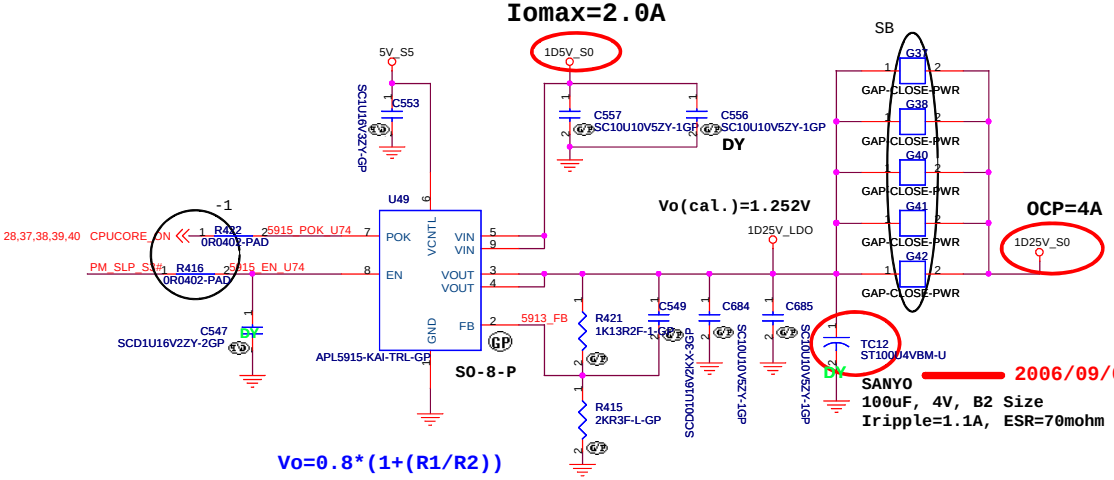



## 2D5V
## Iomax=130mA




**Reserve 2D5V for NV G7X series**

## 1D25V_S0
## Iomax=2.0A

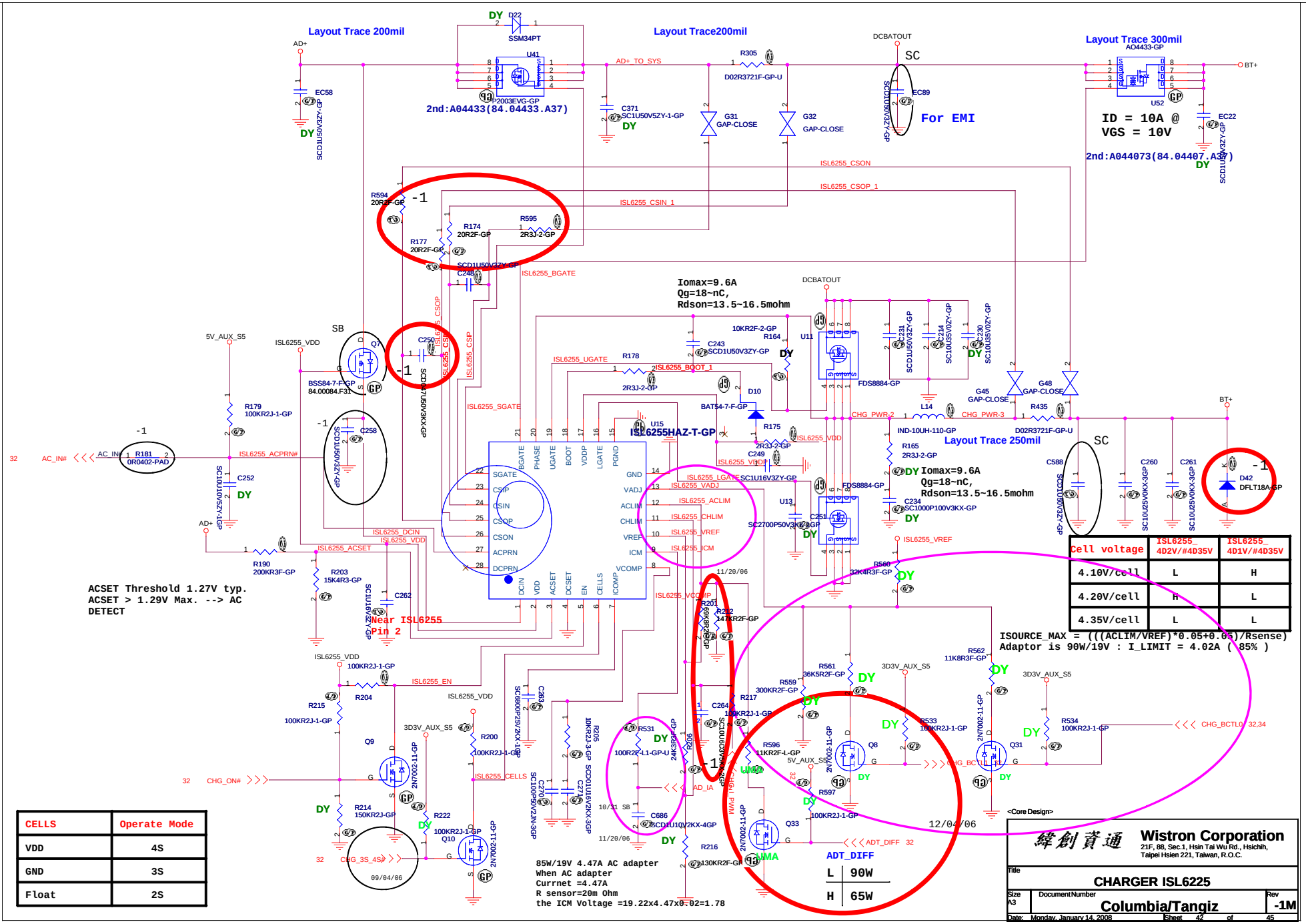



**2006/09/05 Modified**

**Vo=0.8*(1+(R1/R2))**

UMA

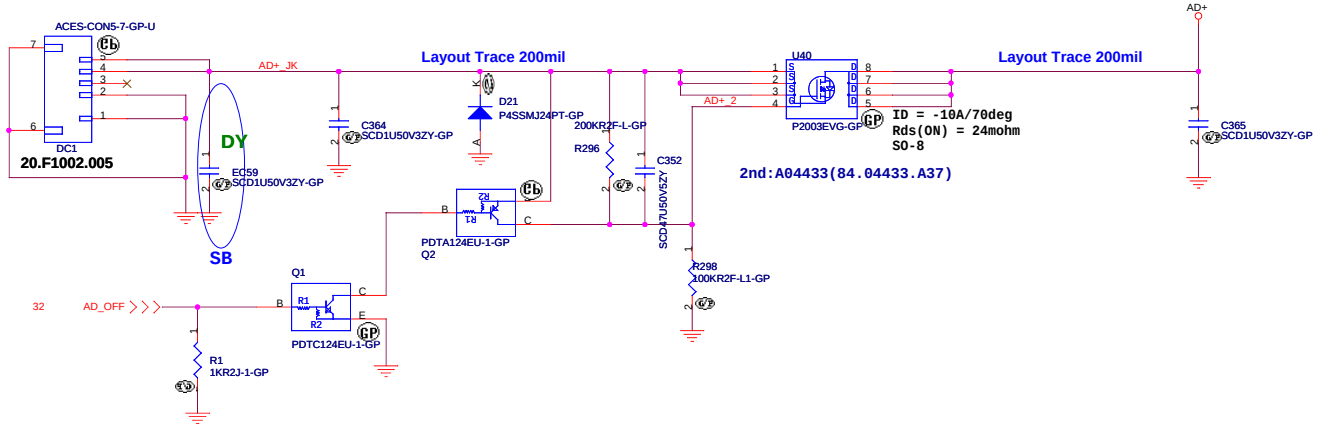
| | |
|---|---|
| 緯創資通 Wistron Corporation | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | 1D25V/2D5V//1D05V/0D9V |
| Size: B | Document Number: Columbia/Tangiz |
| Rev | -1M |
| Date: Monday, January 14, 2008 | Sheet 41 of 45 |



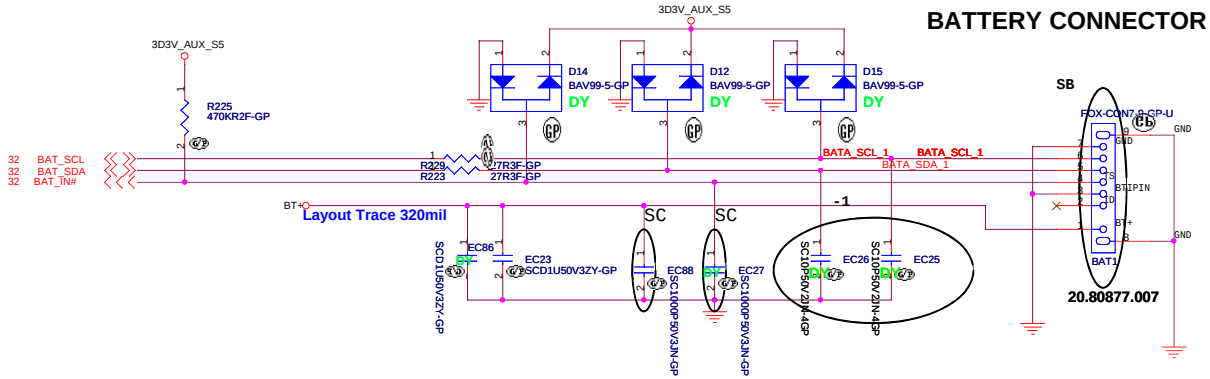

| Cell voltage | ISL6255_ 4D2V/#4D35V | ISL6255_ 4D1V/#4D35V |
|---|---|---|
| 4.10V/cell | L | H |
| 4.20V/cell | H | L |
| 4.35V/cell | L | L |

| CELLS | Operate Mode |
|---|---|
| VDD | 4S |
| GND | 3S |
| Float | 2S |

# Adaptor in to generate DCBATOUT

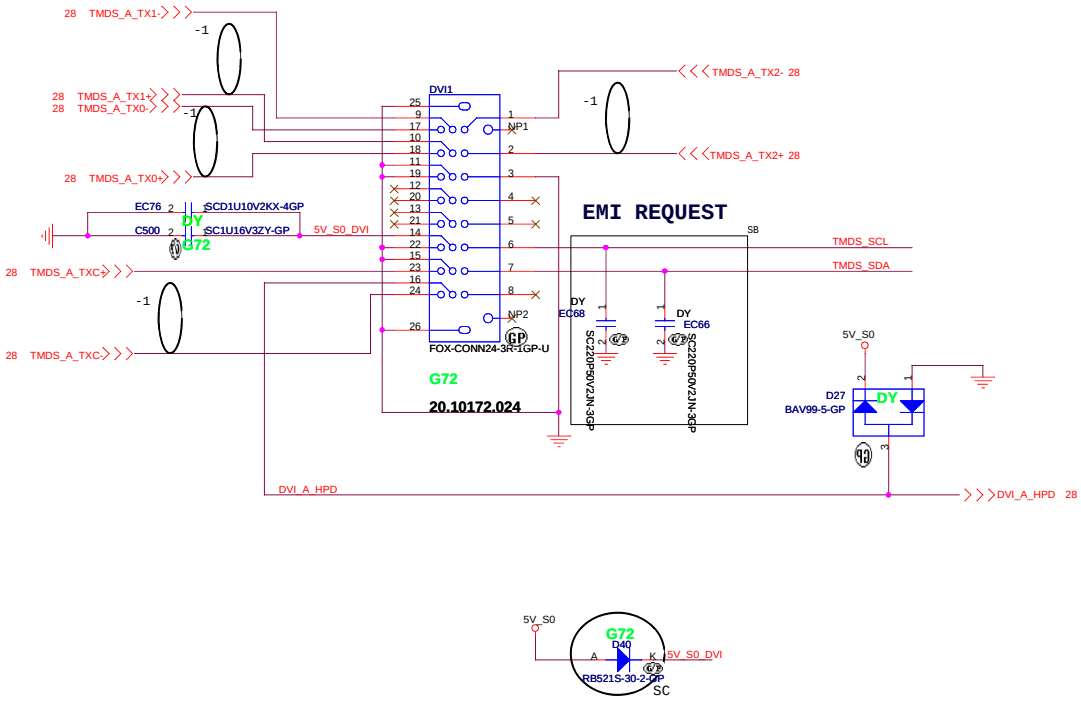



## BATTERY CONNECTOR



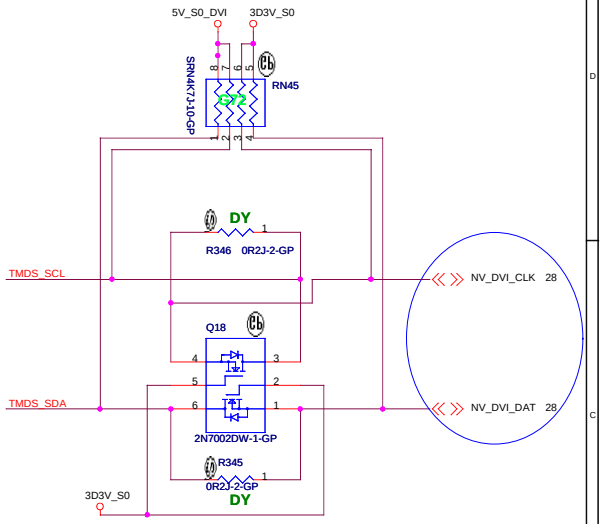

<VariantName>

| | |
|---|---|
| 緯創資通 | Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |
| Title | AD/BATT CONN |
| Size: A3 | Document Number: Columbia/Tangiz |
| Rev: -1M | |
| Date: Monday, January 14, 2008 | Sheet 43 of 45 |



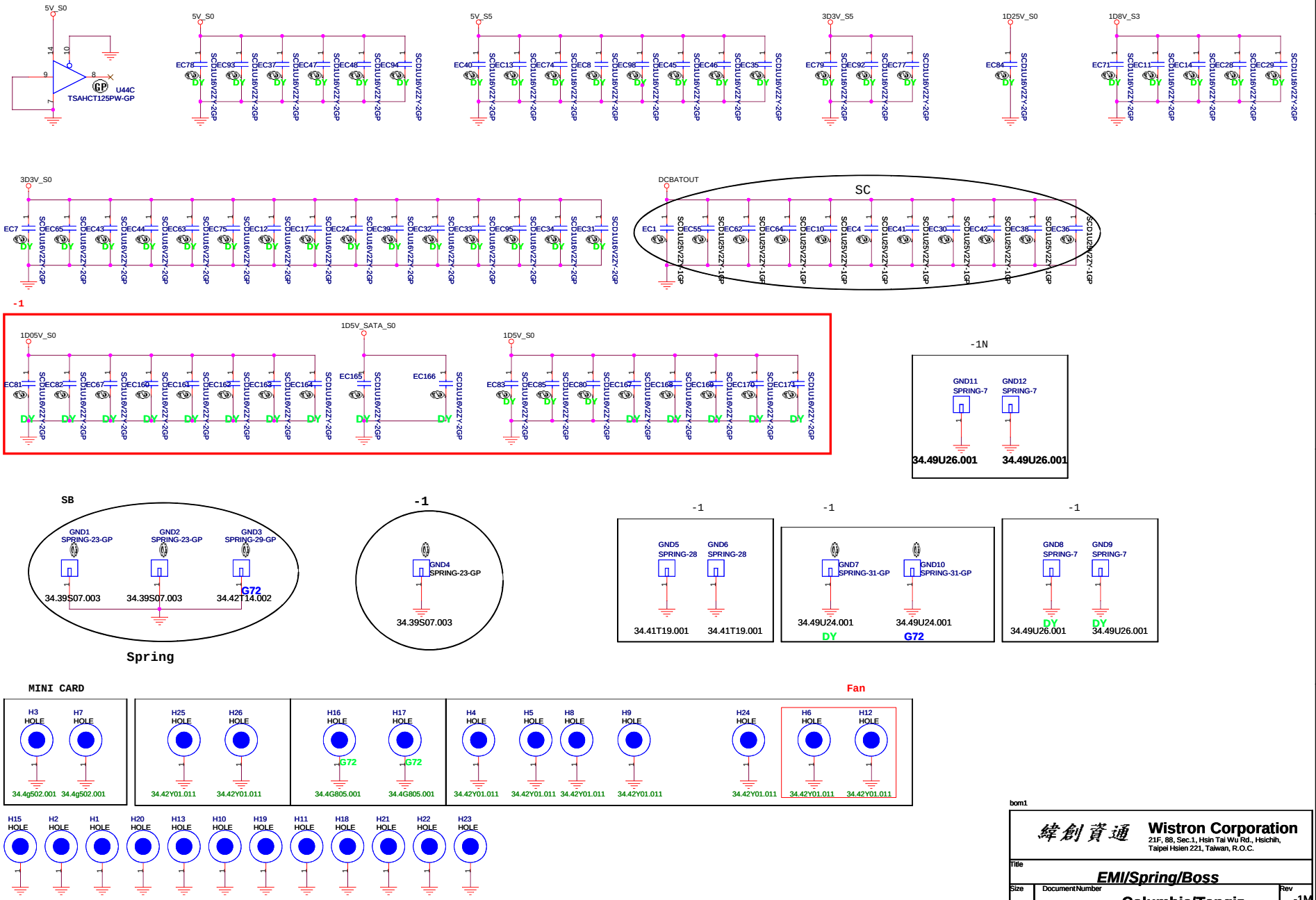







<variant_name>

| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | **DVI CONNECTOR** | |
| Size A3 | Document Number **Columbia/Tangiz** | Rev **-1M** |
| Date: Monday, January 14, 2008 | Sheet 44 of 45 | |




bom1

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size | Document Number: **Columbia/Tangiz** | Rev: -1M

Date: Monday, January 14, 2008 | Sheet 45 of 45