BOM MARK
SA@ SATA 要打
PA@ PATA 要打
3@ 3G 要打

ZH3

ZH3 ASSY P/N :31ZH3MB0008
ZH3 MB C/S ASSY P/N: 41ZH3CS0001
ZH3 MB S/S ASSY P/N: 51ZH3SS0003

AMD S1
Turion 64 Rev.F Dual-Core/
Sempron Rev.F Single-Core
Dual-Core 35W / Single-Core 25W
(638 S1g1 socket)
PG 3,4,5,6

DDRII-SODIMM1 PG 7,8
DDRII-SODIMM2 PG 7,8
533/ 667 MHZ DDR II

CPU THERMAL SENSOR Page 5

HT_LINK

RS485
465 FCBGA
PG 9,10,11,12

Mini Card (WLAN) PCIE3 & USB4
PCI Express Mini Card PG 19
PCI-E, 1X

Express Card PCIE2 & USB5
NEW CARD PG 31
PCI-E, 1X
USB 2.0 * 1(USB5)

DVO → DVI TI TFP513PAP Page : 29 → DVI → Docking Page : 30
TVOUT → EXT_CRT → Docking Page : 30
RGB → CRT Switch SN74CBTLV3257PWR Page : 16 → INT_CRT → CRT Page : 16
LVDS → LVDS Page : 16

A_LINK

SB460
549 BGA
PG 14,15,16,17

SATA - HDD PG 23
PATA - HDD PG 23
SATA0
PATA 100

USB2.0 (P0~P7)
Bluetooth USB7 PG 20
USB2.0 I/O Port X3 USB0 & USB1& USB2 PG 20
DSC USB I/F USB6 PG 16

HOST 133/166MHz
PCIE 100MHz
VGA 96MHz
USB 48MHz
REF 14MHz
CLOCK GENERATOR
ICS951462
PG 2

PCI Bus 33MHz

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7412	AD25	REQ0# / GNT0#	INT E/F/G#
5788M	AD20	REQ2# / GNT2#	INT G#

BROADCOM 10/100/1G LAN
5788M PG 17
BOTHHAND TRANSFORMER PG 18
RJ45 PG 18

AD25
REQ0# / GNT0#
INT E/F/G#
OSC 48MHZ
TI PCMCIA+1394 +6 IN 1
PCI7412
Page :21~22
1394 Page: 21
5 IN 1 Page: 22
PCMCIA Page: 22

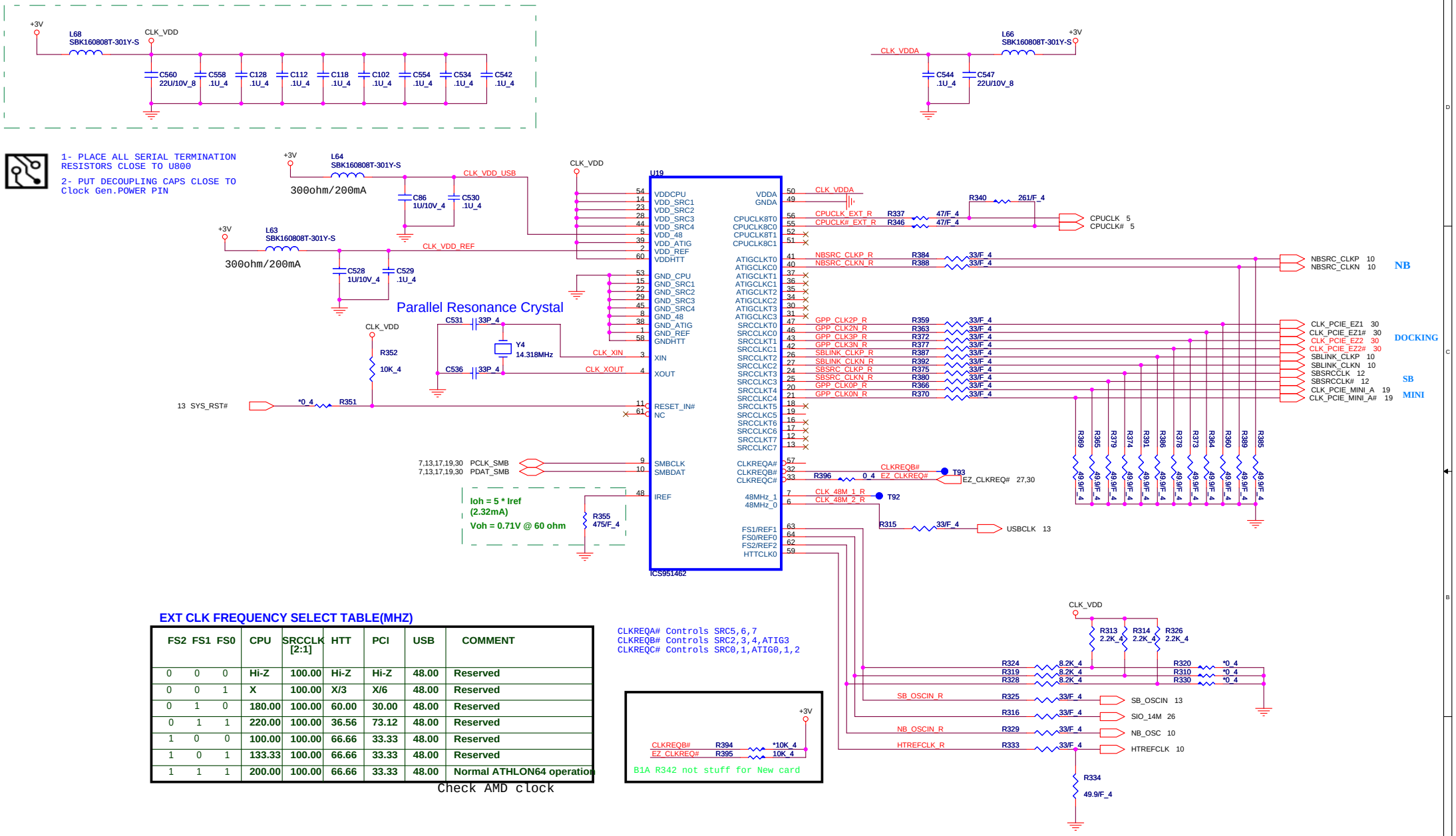
Azalia
Azalia Audio PG 24
Amplifier MAX4411 PG 25
Amplifier MAX9755A PG 25
Azalia MDC PG 24
MIC. PG 25
H.P/SPDIF PG 25
INT. S.P. PG 25
MODEM RJ 11 PG 18

LPC
G-SENSOR KXP84-0200 Page : 23
KBC NS97551 PG 27
NS SIO (87383) Page : 26
X-Bus
K/B CONN. PG 28
Touch Pad PG 28
Flash ROM PG 27
FIR Page : 26

VCC_CORE → CPU VR PG 30
+1.2V, +VCCP → +1.2V +VCCP PG 31
+1.8VSUS, +1.8V, SMDDR_VTERM → +1.8VSUS SMDDR VTERM PG 32
+3VPCU, +3V_S5, +3VSUS, +5VSUS, +5V, +12V → 3V/5V PG 33
VIN → CHARGER PG 34

PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	D
Date: Tuesday, June 27, 2006	Sheet 1 of 36	



EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Check AMD clock

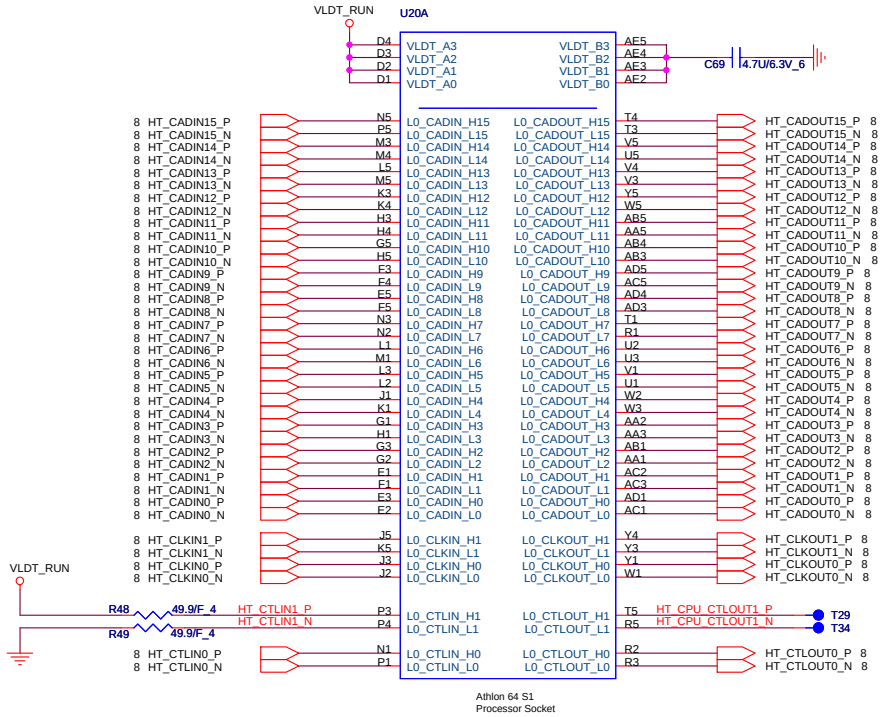
CLKREQA# Controls SRC5,6,7
CLKREQB# Controls SRC2,3,4,ATIG3
CLKREQC# Controls SRC0,1,ATIG0,1,2

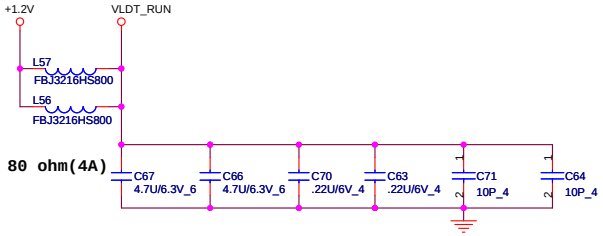
PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR	D
Date: Tuesday, June 27, 2006	Sheet 2 of 36	

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE





LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 HT I/F	D

Date: Tuesday, June 27, 2006 Sheet 3 of 36

Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

PLACE THEM CLOSE TO CPU WITHIN 1"

U20B

DDR II: CMD/CTRL/CLK

Athlon 64 S1
Processor Socket

U20C

DDR: DATA

Athlon 64 S1
Processor Socket

To SODIMM socket B (Far)

To SODIMM socket A (near)

PROJECT :ZH3		
Quanta Computer Inc.		
Size	Document Number: ATHLON64 DDRII MEMORY I/F	Rev: D
Date: Tuesday, June 27, 2006	Sheet 4 of 36	

ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

+2.5V
CPU_VDDA_RUN
L65 BLM18PG330SN1D
C532 4.7U/6.3V_6
C98 22U/6V_4
C88 3900p/25V_4
C533 100U/6.3V_3528

2 CPUCLK C541 3900p/25V_4 CPU_CLKIN_SC_P
R345 169F
2 CPUCLK# C537 3900p/25V_4 CPU_CLKIN_SC_N

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

+1.8V R308 *300 R309 *300
R311 300_4
CPU_SIC_R
CPU_SID_R

VLDT_RUN
place them to CPU within 1"
R47 44.2F_4
R46 44.2F_4
CPU_HTREF1
CPU_HTREF0

31 COREFB+V
31 COREFB-
To Power

T20 VDD_FB_H
T11 VDD_FB_L
T36 CPU_VDDIO_SUS_FB_H
T28 CPU_VDDIO_SUS_FB_L
VDDIO_FB_H
VDDIO_FB_L

CPU_CLKIN_SC_P
CPU_CLKIN_SC_N
CLKIN_H
CLKIN_L

U20D

CPU_VDDA_RUN F8 VDDA2, F9 VDDA1
T88 CPU_HT_RESET# B7
T89 CPU_ALL_PWROK A7
T38 CPU_LDTSTOP# F10
RESET_L, PWROK, LDTSTOP_L
CPU_SIC_R AF4 SIC
CPU_SID_R AE5 SID
CPU_HTREF1 P6 HT_REF1
CPU_HTREF0 R6 HT_REF0
F6 VDD_FB_H
E6 VDD_FB_L
W9 VDDIO_FB_H
Y9 VDDIO_FB_L
A9 CLKIN_H
A8 CLKIN_L

THERMTRIP_L AF6 H_THERMTRIP#
PROCHOT_L AC7 H_PROCHOT#
VID5 A5 31
VID4 C6 31
VID3 A6 31
VID2 A4 31
VID1 C5 31
VID0 B5 31
CPU_PRESENT_L AC6 CPU_PRESENT#
PSI_L A3 PSI_L
T22

PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

+1.8VSUS
R52 300_4

CPU_DBRDY G10 DBRDY
CPU_TMS AA9 TMS
CPU_TCK AC9 TCK
CPU_TRST# AD9 TRST_L
CPU_TDI AF9 TDI
DBREQ_L E10 CPU_DBREQ#
TDO AF9 CPU_TDO

TEST29_H C9 CPU_TEST29_H_FBCLKOUT_P R59 80.6F
TEST29_L C8 CPU_TEST29_L_FBCLKOUT_N
ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

CPU_TEST25_H_BYPASSCLK_H E9
CPU_TEST25_L_BYPASSCLK_L E8
CPU_TEST19_PLLTEST0 G9
CPU_TEST18_PLLTEST1 H10
AA7
C2
T12 CPU_TEST17_BP3 D7
T19 CPU_TEST16_BP2 E7
CPU_TEST15_BP1 F7
CPU_TEST14_BP0 C7
CPU_TEST12_SCANSHIFTENB AC8
T17 CPU_TEST07_ANALOG_T C3
T32 CPU_TEST6_DIECRACKMON AA6
CPU_TEST5_THERMDC W7
CPU_TEST4_THERMDA W8
T14 CPU_TEST3_GATE0 Y6
T13 CPU_TEST2_DRAIN0 AB6
TEST25_H, TEST25_L, TEST19, TEST18, TEST13, TEST9, TEST17, TEST16, TEST15, TEST14, TEST12, TEST7, TEST6, TEST5, TEST4, TEST3, TEST2

TEST24 AE7 CPU_TEST24_SCANCLK1
TEST23 AD7 CPU_TEST23_TSTUPD T90
TEST22 AE8 CPU_TEST22_SCANSHIFTEN
TEST21 AB8 CPU_TEST21_SCANEN
TEST20 AE7 CPU_TEST20_SCANCLK2
TEST28_H J7 CPU_TEST28_H_PLLCHRZ_P T16
TEST28_L H8 CPU_TEST28_L_PLLCHRZ_N T30
TEST27 AF8 CPU_TEST27_SINGLECHAIN
TEST26 AE6 CPU_TEST26_BURNIN#
TEST10 K8 CPU_TEST10_ANALOGOUT T31
TEST8 C4 CPU_TEST08_DIG_T T18

T44 CPU_RSVD_MA0_CLK3_P P20
T41 CPU_RSVD_MA0_CLK3_N P19
T45 CPU_RSVD_MA0_CLK0_P N20
T42 CPU_RSVD_MA0_CLK0_N N19
RSVD0, RSVD1, RSVD2, RSVD3

RSVD8 H16 CPU_MA_RESET# T40
RSVD9 B18 CPU_MB_RESET# T43
RSVD10 B3 CPU_RSVD_VIDSTRB1 T21
RSVD11 C1 CPU_RSVD_VIDSTRB0 T15
RSVD12 H6 CPU_RSVD_VDDNB_FB_P T9
RSVD13 G6 CPU_RSVD_VDDNB_FB_N T10
RSVD14 D5 CPU_RSVD_CORE_TYPE T24
MISC
RSVD15 R24
RSVD16 W18
RSVD17 R23
RSVD18 AA8
RSVD19 R18
RSVD20 R19

T96 CPU_RSVD_MB0_CLK3_P R26
T50 CPU_RSVD_MB0_CLK3_N R25
T46 CPU_RSVD_MB0_CLK0_P P22
T47 CPU_RSVD_MB0_CLK0_N R22
RSVD4, RSVD5, RSVD6, RSVD7

AMD NPT S1 SOCKET
Processor Socket

B2A:ATI suggestion to avoid hynix ram s3 issue stuff R303,R299 del R298

+1.8V R307 300_4
+3V +1.8VSUS R303 4.7K/F_4 C522 .1U_4
12,13 CPU_PWRGD
U17 NC7SZ08P5X_NL CPU_ALL_PWROK

+1.8V R51 300_4
+1.8VSUS C75 .1U_4
10,12,13 LDT_STOP#
U3 NC7SZ08P5X_NL CPU_LDTSTOP#

+1.8V R302 300_4
+1.8VSUS C519 .1U_4
12 LDT_RST#
12,13,27 EC_PWRGD R299 0_4
10,27 NB_PWRGD R298 *0_4
U15 NC7SZ08P5X_NL CPU_HT_RESET#

+1.8VSUS +3V
R586 10K_4 R587 10K_4
Q41 MMBT3904
PSI_L
PSI# PSI# 31
B1A :Change P/N for ROHS

+1.8V R39 330_4
+1.8VSUS
Q3 MMBT3904
R41 300_4
B1A :Change P/N for ROHS
CPU_EC_PROCHOT# 27
H_PROCHOT#
R42 *0_4
CPU_PROCHOT# 13

SB_THERMTRIP# 13
separated input voltage 0104
+1.8V R45 *330_4 Q4 *MMBT3904
R43 4.7K/F_4 EC_PWRGD
R44 4.7K/F_4
+1.8VSUS R40 300_4 H_THERMTRIP#
Q5 MMBT3904
THERM_SYS_PWR 34
B1A :Change P/N for ROHS

+1.8VSUS
CPU_TEST27_SINGLECHAIN R336 *300_4
CPU_TEST26_BURNIN# R312 300_4
CPU_PRESENT# R322 1K/F_4
CPU_TEST25_H_BYPASSCLK_H R56 510/F_4
CPU_TEST21_SCANEN R331 300_4
CPU_TEST20_SCANCLK2 R318 300_4
CPU_TEST24_SCANCLK1 R323 300_4
CPU_TEST22_SCANSHIFTEN R332 300_4
CPU_TEST12_SCANSHIFTENB R335 300_4
CPU_TEST15_BP1 R50 300_4
CPU_TEST14_BP0 R57 300_4
CPU_TEST25_L_BYPASSCLK_L R53 510/F_4
CPU_TEST19_PLLTEST0 R62 300_4
CPU_TEST18_PLLTEST1 R60 300_4

IF no use which Net need pull-up or down

+1.8VSUS
R349 220_4
R339 220_4
R338 220_4
R342 220_4
R54 220_4
CPU_DBREQ# T39
CPU_DBRDY T37
CPU_TCK T25
CPU_TMS T33
CPU_TDI T91
CPU_TRST# T27
CPU_TDO T26
LDT_RST# T87

HDT CONNECTOR
PUT CLOSE ON LAYOUT

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

CPU H/W MONITOR

+3V R348 47/F_6 3V_THM
C535 .1U_4
15 MIL
Address 98H
U18 G781
VCC, DXN, DXP, -OVT, -ALT, SMDATA, SMCLK, GND
CPU_TEST5_THERMDC
C539 2200P/50V_4
CPU_TEST4_THERMDA
10 mil trace / 10 mil space

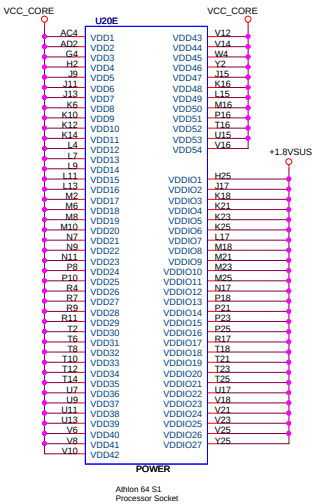
+3V R306 10K_4 Q28 2N7002E-LF
To SB GPIO
MAX6648_AL# 13
KBSMDAT
KBSMCLK

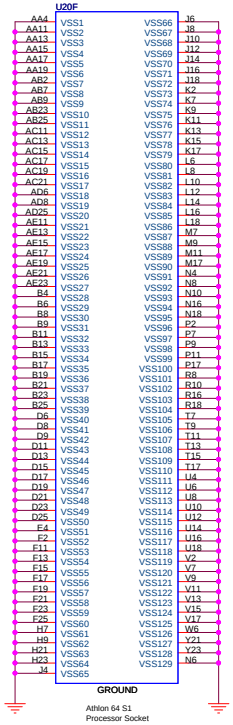
+3V R327 10K_4 Q28 2N7002E-LF
MBDATA 27,35
+3V R317 10K_4 Q27 2N7002E-LF
MBCLK 27,35

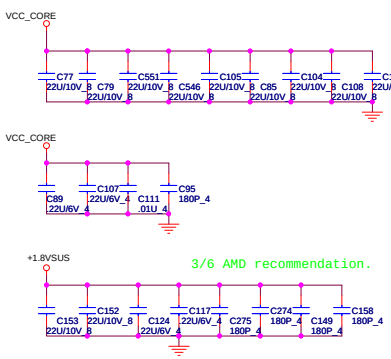
+3V R347 10K_4
To FAN
MAX6648_OV# 28

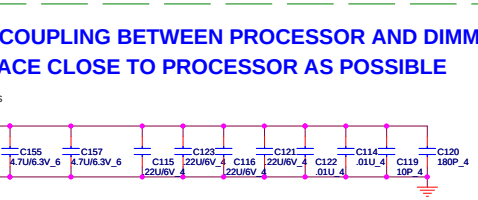
PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 CTRL & DEBUG	D
Date: Tuesday, June 27, 2006	Sheet 5 of 36	

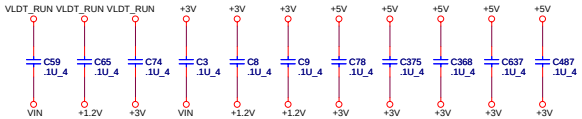




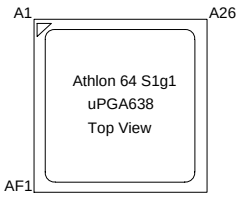




PROCESSOR POWER AND GROUND



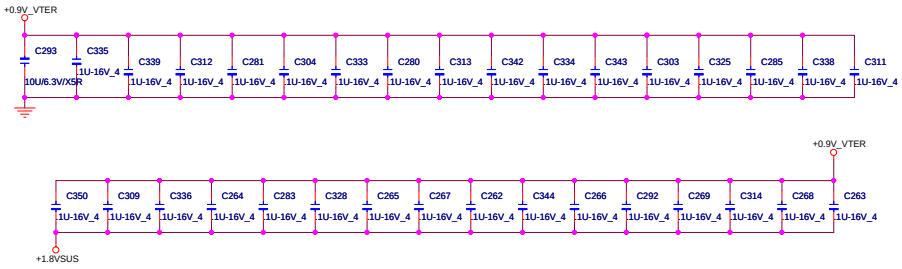
3/6 :ADD 0.1U CAPACITOR TO CROSS POWER PLANE.



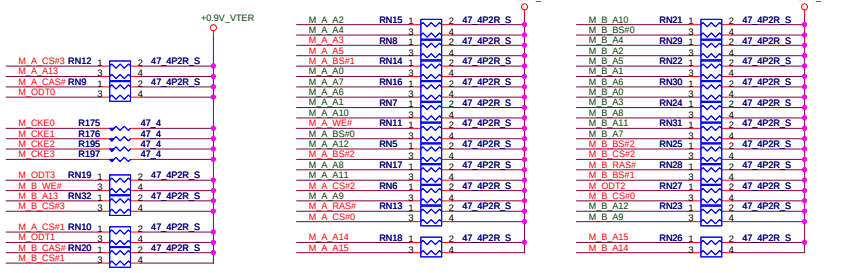
PROJECT :ZH3
Quanta Computer Inc.

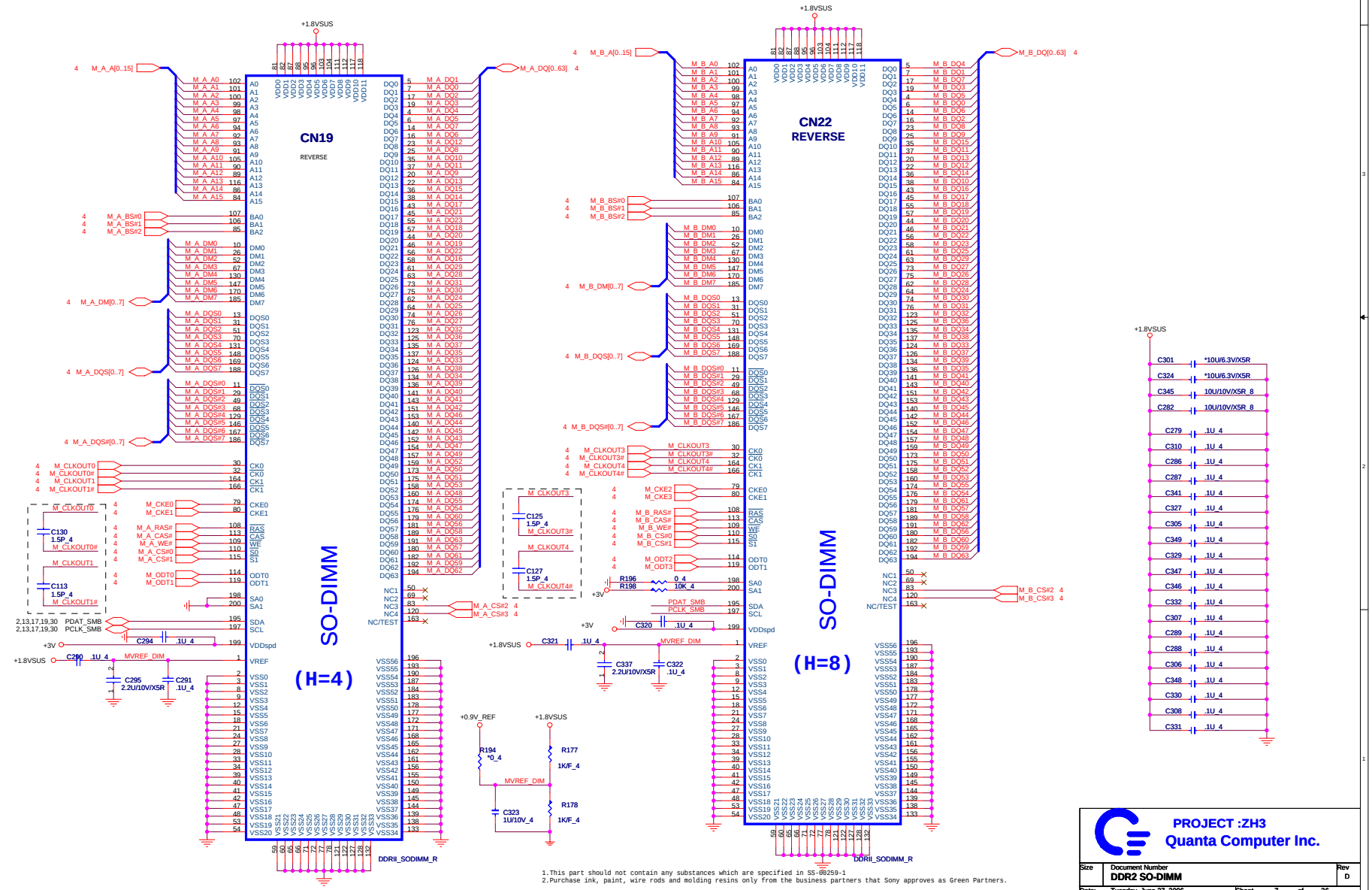
Size	Document Number	Rev
	ATHLON64 PWR & GND	D
Date: Tuesday, June 27, 2006	Sheet 6 of 36	

TERMINATOR DECOUPLING CAPACITOR



DDR2 TERMINATOR

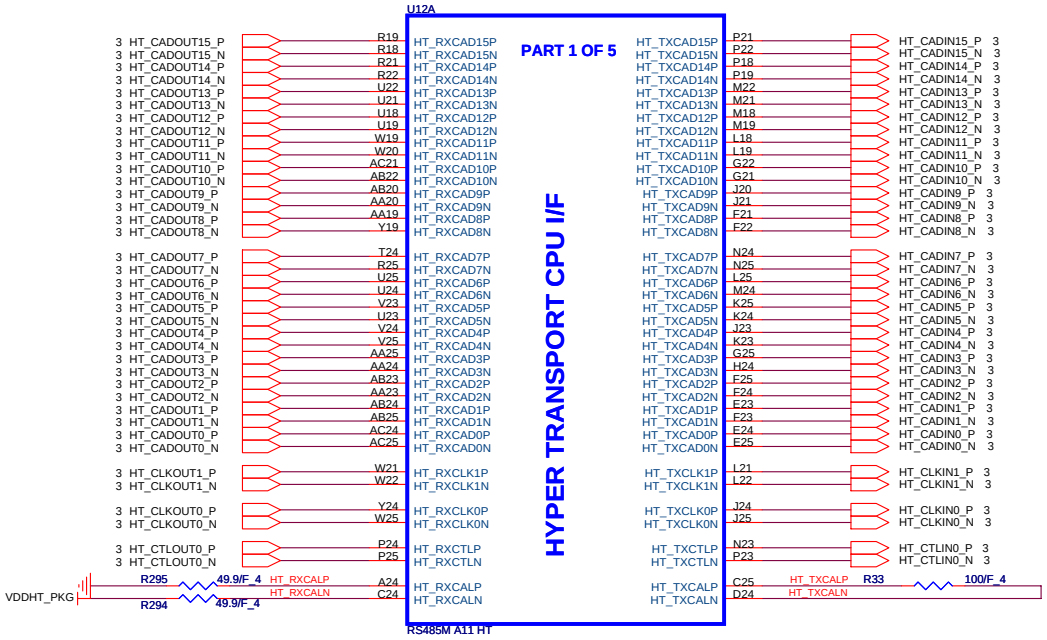




1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

PROJECT :ZH3
Quanta Computer Inc.

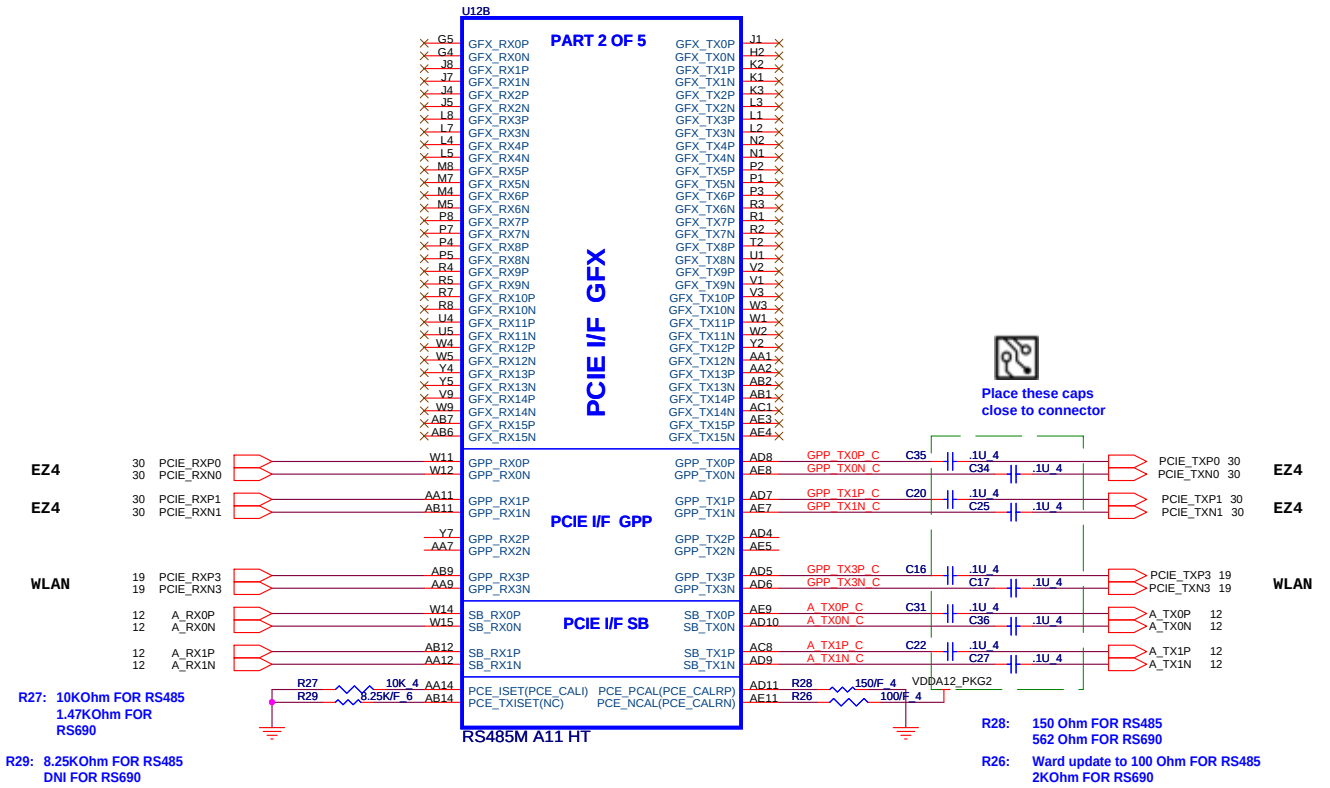
Size	Document Number	Rev
	DDR2 SO-DIMM	D
Date: Tuesday, June 27, 2006	Sheet 7 of 36	



PROJECT :ZH3

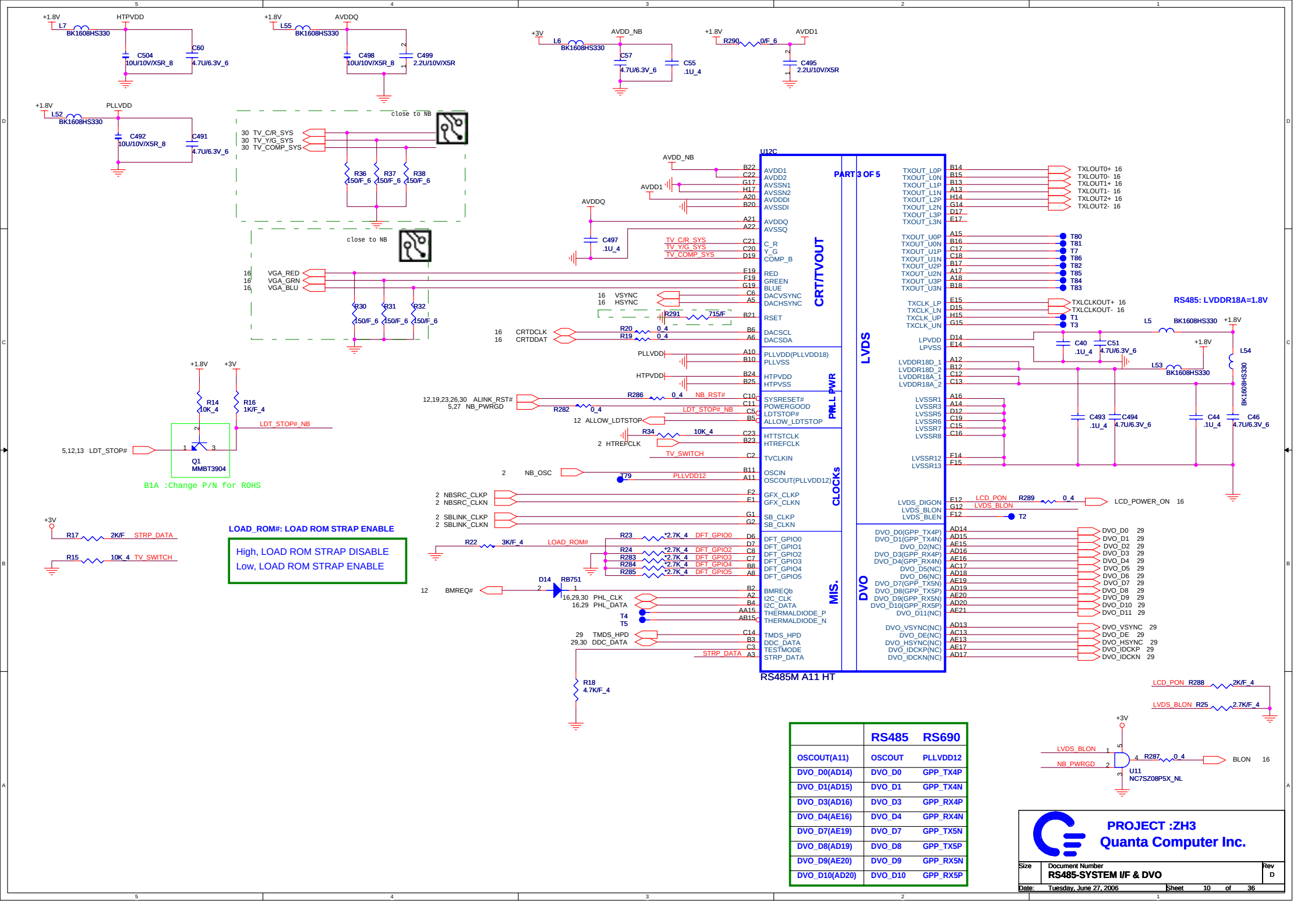
Quanta Computer Inc.

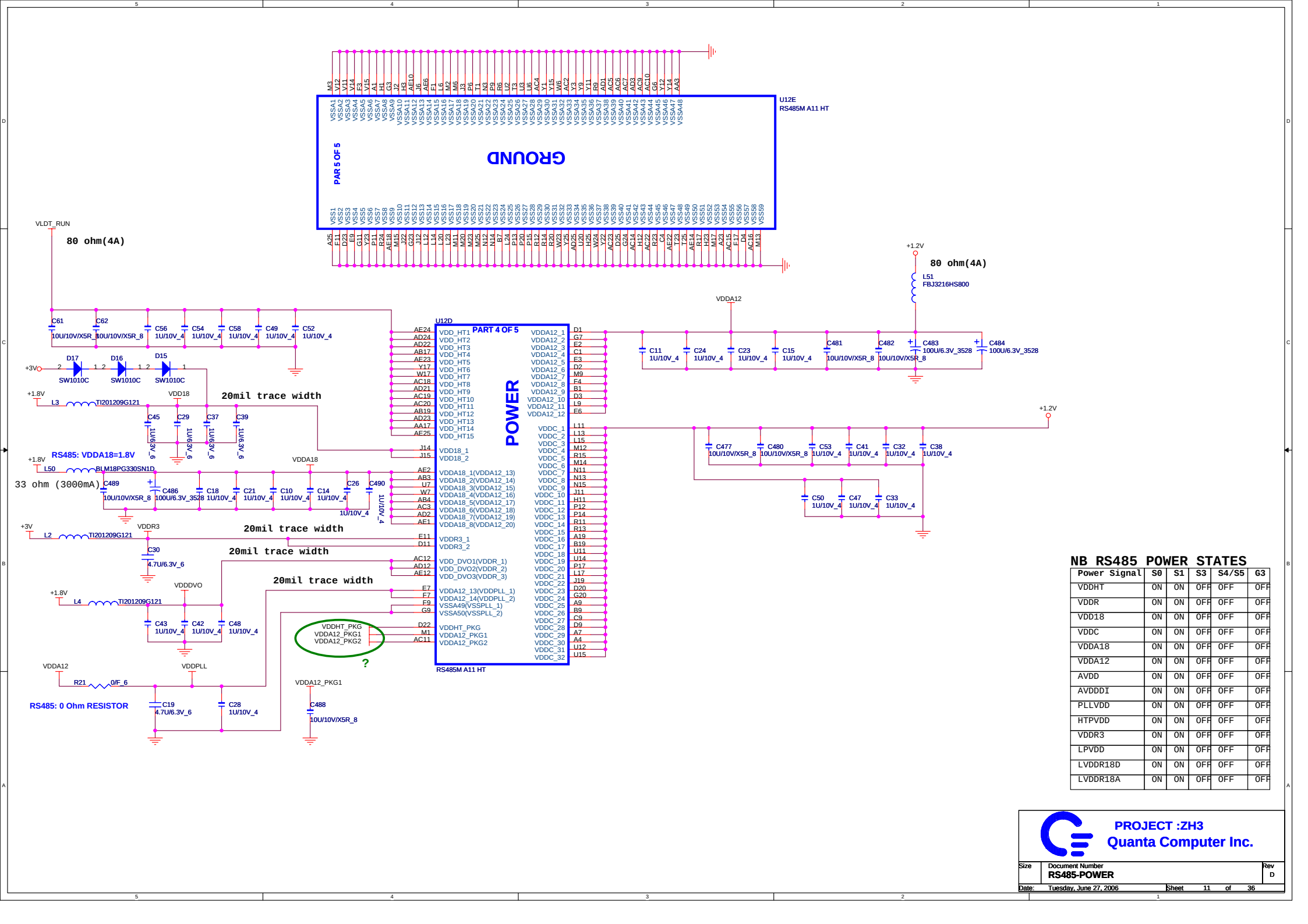
Size	Document Number	Rev
	RS485-HT LINK0 I/F	D
Date: Tuesday, June 27, 2006	Sheet 8 of 36	

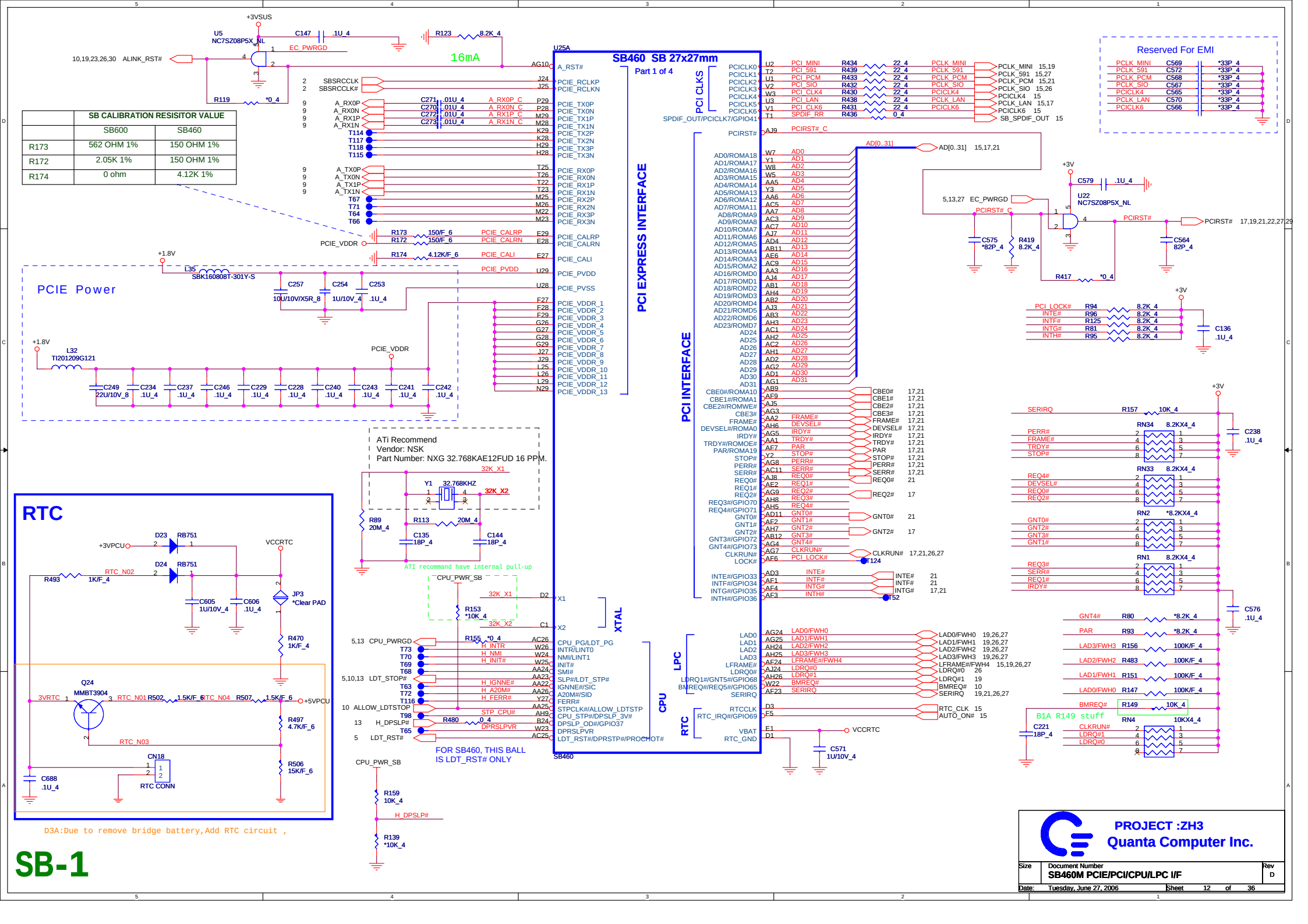


PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	RS485-PCIE LINK I/F	D
Date: Tuesday, June 27, 2006	Sheet 9 of 36	


+1.8V
L7
BK1608HS330
HTPVDD
C504
10U/10V/X5R_8
C60
4.7U/6.3V_6
+1.8V
L55
BK1608HS330
AVDDQ
C498
10U/10V/X5R_8
C499
2.2U/10V/X5R
+3V
L6
BK1608HS330
AVDD_NB
C57
4.7U/6.3V_6
C55
.1U_4
+1.8V
R290
0/F_6
AVDD1
C495
2.2U/10V/X5R
+1.8V
L52
BK1608HS330
PLLVDD
C492
10U/10V/X5R_8
C491
4.7U/6.3V_6
close to NB
30 TV_C/R_SYS
30 TV_Y/G_SYS
30 TV_COMP_SYS
R36
150/F_6
R37
150/F_6
R38
150/F_6
close to NB
16 VGA_RED
16 VGA_GRN
16 VGA_BLU
R30
150/F_6
R31
150/F_6
R32
150/F_6
+1.8V
+3V
R14
10K_4
R16
1K/F_4
LDT_STOP#_NB
5,12,13 LDT_STOP#
Q1
MMBT3904
B1A :Change P/N for ROHS
+3V
R17
2K/F
STRP_DATA
R15
10K_4
TV_SWITCH
LOAD_ROM#: LOAD ROM STRAP ENABLE
High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE
U12C
PART 3 OF 5
AVDD_NB
AVDD1
AVDDQ
AVDD1
AVDD2
AVSSN1
AVSSN2
AVDDDI
AVSSDI
AVDDQ
AVSSQ
C497
.1U_4
C_R
Y_G
COMP_B
TV_C/R_SYS
TV_Y/G_SYS
TV_COMP_SYS
RED
GREEN
BLUE
DACVSYNC
DACHSYNC
16 VSYNC
16 HSYNC
RSET
R291
715/F
DACSCL
DACSDA
R20
0_4
R19
0_4
16 CRTDCLK
16 CRTDDAT
CRT/TVOUT
PLLVDD
PLLVDD(PLLVDD18)
PLLVSS
HTPVDD
HTPVSS
PLL_PWR
12,19,23,26,30 ALINK_RST#
5,27 NB_PWRGD
R286
0_4
NB_RST#
R282
0_4
LDT_STOP#_NB
12 ALLOW_LDTSTOP
SYSRESET#
POWERGOOD
LDTSTOP#
ALLOW_LDTSTOP
R34
10K_4
2 HTREFCLK
HTTSTCLK
HTREFCLK
TVCLKIN
TV_SWITCH
2 NB_OSC
OSCIN
OSCOUT(PLLVDD12)
T79
PLLVDD12
2 NBSRC_CLKP
2 NBSRC_CLKN
GFX_CLKP
GFX_CLKN
2 SBLINK_CLKP
2 SBLINK_CLKN
SB_CLKP
SB_CLKN
CLOCKs
R22
3K/F_4
LOAD_ROM#
R23
*2.7K_4
DFT_GPIO0
R24
*2.7K_4
DFT_GPIO2
R283
*2.7K_4
DFT_GPIO3
R284
*2.7K_4
DFT_GPIO4
R285
*2.7K_4
DFT_GPIO5
DFT_GPIO0
DFT_GPIO1
DFT_GPIO2
DFT_GPIO3
DFT_GPIO4
DFT_GPIO5
D14
RB751
12 BMREQ#
BMREQb
I2C_CLK
I2C_DATA
16,29,30 PHL_CLK
16,29 PHL_DATA
THERMALDIODE_P
THERMALDIODE_N
T4
T5
MIS.
29 TMDS_HPD
29,30 DDC_DATA
TMDS_HPD
DDC_DATA
TESTMODE
STRP_DATA
R18
4.7K/F_4
RS485M A11 HT
LVDS
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXCLK_LP
TXCLK_LN
TXCLK_UP
TXCLK_UN
LVDDR18D_1
LVDDR18D_2
LVDDR18A_1
LVDDR18A_2
LVSSR1
LVSSR3
LVSSR5
LVSSR6
LVSSR7
LVSSR8
LVSSR12
LVSSR13
LVDS_DIGON
LVDS_BLON
LVDS_BLEN
TXLOUT0+ 16
TXLOUT0- 16
TXLOUT1+ 16
TXLOUT1- 16
TXLOUT2+ 16
TXLOUT2- 16
T80
T81
T7
T86
T82
T85
T84
T83
TXLCLKOUT+ 16
TXLCLKOUT- 16
T1
T3
RS485: LVDDR18A=1.8V
L5
BK1608HS330
+1.8V
L54
BK1608HS330
C40
.1U_4
C51
4.7U/6.3V_6
L53
BK1608HS330
C493
.1U_4
C494
4.7U/6.3V_6
C44
.1U_4
C46
4.7U/6.3V_6
LCD_PON
R289
0_4
LCD_POWER_ON 16
LVDS_BLON
T2
DVO
DVO_D0(GPP_TX4P)
DVO_D1(GPP_TX4N)
DVO_D2(NC)
DVO_D3(GPP_RX4P)
DVO_D4(GPP_RX4N)
DVO_D5(NC)
DVO_D6(NC)
DVO_D7(GPP_TX5N)
DVO_D8(GPP_TX5P)
DVO_D9(GPP_RX5N)
DVO_D10(GPP_RX5P)
DVO_D11(NC)
DVO_VSYNC(NC)
DVO_DE(NC)
DVO_HSYNC(NC)
DVO_IDCKP(NC)
DVO_IDCKN(NC)
DVO_D0 29
DVO_D1 29
DVO_D2 29
DVO_D3 29
DVO_D4 29
DVO_D5 29
DVO_D6 29
DVO_D7 29
DVO_D8 29
DVO_D9 29
DVO_D10 29
DVO_D11 29
DVO_VSYNC 29
DVO_DE 29
DVO_HSYNC 29
DVO_IDCKP 29
DVO_IDCKN 29
LCD_PON R288 2K/F_4
LVDS_BLON R25 2.7K/F_4
+3V
LVDS_BLON
NB_PWRGD
R287
0_4
BLON 16
U11
NC7SZ08P5X_NL
RS485
RS690
OSCOUT(A11)
OSCOUT
PLLVDD12
DVO_D0(AD14)
DVO_D0
GPP_TX4P
DVO_D1(AD15)
DVO_D1
GPP_TX4N
DVO_D3(AD16)
DVO_D3
GPP_RX4P
DVO_D4(AE16)
DVO_D4
GPP_RX4N
DVO_D7(AE19)
DVO_D7
GPP_TX5N
DVO_D8(AD19)
DVO_D8
GPP_TX5P
DVO_D9(AE20)
DVO_D9
GPP_RX5N
DVO_D10(AD20)
DVO_D10
GPP_RX5P
PROJECT :ZH3
Quanta Computer Inc.
Size
Document Number
RS485-SYSTEM I/F & DVO
Rev
D
Date: Tuesday, June 27, 2006
Sheet 10 of 36


U12E
RS485M A11 HT
PAR 5 OF 5
GROUND
U12D
PART 4 OF 5
POWER
RS485M A11 HT
VLDT_RUN
80 ohm(4A)
+1.2V
80 ohm(4A)
L51
FBJ3216HS800
VDDA12
+3V
+1.8V
VDD18
20mil trace width
RS485: VDDA18=1.8V
VDDA18
33 ohm (3000mA)
VDDR3
20mil trace width
20mil trace width
VDDDVO
20mil trace width
VDDA12
VDDPLL
RS485: 0 Ohm RESISTOR
VDDA12_PKG1
?
VDDHT_PKG
VDDA12_PKG1
VDDA12_PKG2
D17
D16
D15
SW1010C
L3
TI201209G121
L50
BLM18PG330SN1D
L2
L4
R21
0/F_6
C61
C62
C56
C54
C58
C49
C52
C45
C29
C37
C39
C489
C486
C18
C21
C10
C14
C26
C490
C30
C43
C42
C48
C19
C28
C488
C11
C24
C23
C15
C481
C482
C483
C484
C477
C480
C53
C41
C32
C38
C50
C47
C33
NB RS485 POWER STATES
Power Signal | S0 | S1 | S3 | S4/S5 | G3
VDDHT | ON | ON | OFF | OFF | OFF
VDDR | ON | ON | OFF | OFF | OFF
VDD18 | ON | ON | OFF | OFF | OFF
VDDC | ON | ON | OFF | OFF | OFF
VDDA18 | ON | ON | OFF | OFF | OFF
VDDA12 | ON | ON | OFF | OFF | OFF
AVDD | ON | ON | OFF | OFF | OFF
AVDDDI | ON | ON | OFF | OFF | OFF
PLLVDD | ON | ON | OFF | OFF | OFF
HTPVDD | ON | ON | OFF | OFF | OFF
VDDR3 | ON | ON | OFF | OFF | OFF
LPVDD | ON | ON | OFF | OFF | OFF
LVDDR18D | ON | ON | OFF | OFF | OFF
LVDDR18A | ON | ON | OFF | OFF | OFF
PROJECT :ZH3
Quanta Computer Inc.
Size
Document Number
RS485-POWER
Rev
D
Date: Tuesday, June 27, 2006
Sheet 11 of 36


SB460 SB 27x27mm
Part 1 of 4
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
CPU
LPC
RTC
SB460
PCIE Power
RTC
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.
ATI recommand have internal pull-up
FOR SB460, THIS BALL
IS LDT_RST# ONLY
SB CALIBRATION RESISITOR VALUE
SB600
SB460
R173 150/F_6 150/F_6
R172 150/F_6 150/F_6
R174 4.12K/F_6 4.12K/F_6
R119 *0_4 *0_4
R123 8.2K_4 8.2K_4
16mA
Reserved For EMI
D3A:Due to remove bridge battery,Add RTC circuit ,
B1A R149 stuff
SB-1
PROJECT :ZH3
Quanta Computer Inc.
SB460M PCIE/PCI/CPU/LPC I/F
Rev D
Tuesday, June 27, 2006
Sheet 12 of 36

USB power use S3 power,But Over current signal datasheet is S5 only,But ATI FAE say use S3 is ok

SB460 SB 27x27mm

Part 4 of 4

ACPI / WAKE UP EVENTS

USB INTERFACE

GPIO

USB OC

AZALIA

AC97

USB PWR

OSC / RST

USB0: M/B IO
USB1: M/B IO
USB2: M/B IO
USB4: MINI CARD(3G)
USB5: NEW CARD
USB6: CCD
USB7: BLUETOOTH

B1A: SB600 ONLY(NC for SB460)

D3A : Remove RP1

USB power

Delay 20ms after S5 powerOK

D3A:Modify NET of HIGHT_G_INT & LOW_G_INT contact to GPM3 & 4, Add net of USB_OCP3 &USB_OCP4 contact to location :RN3

If throttling from SM remore R264

B2A:ATI suggestion ,The signal should be pull down to ground through 10k resistor.

B1A:Change from +3V_SUS to +3V_S5

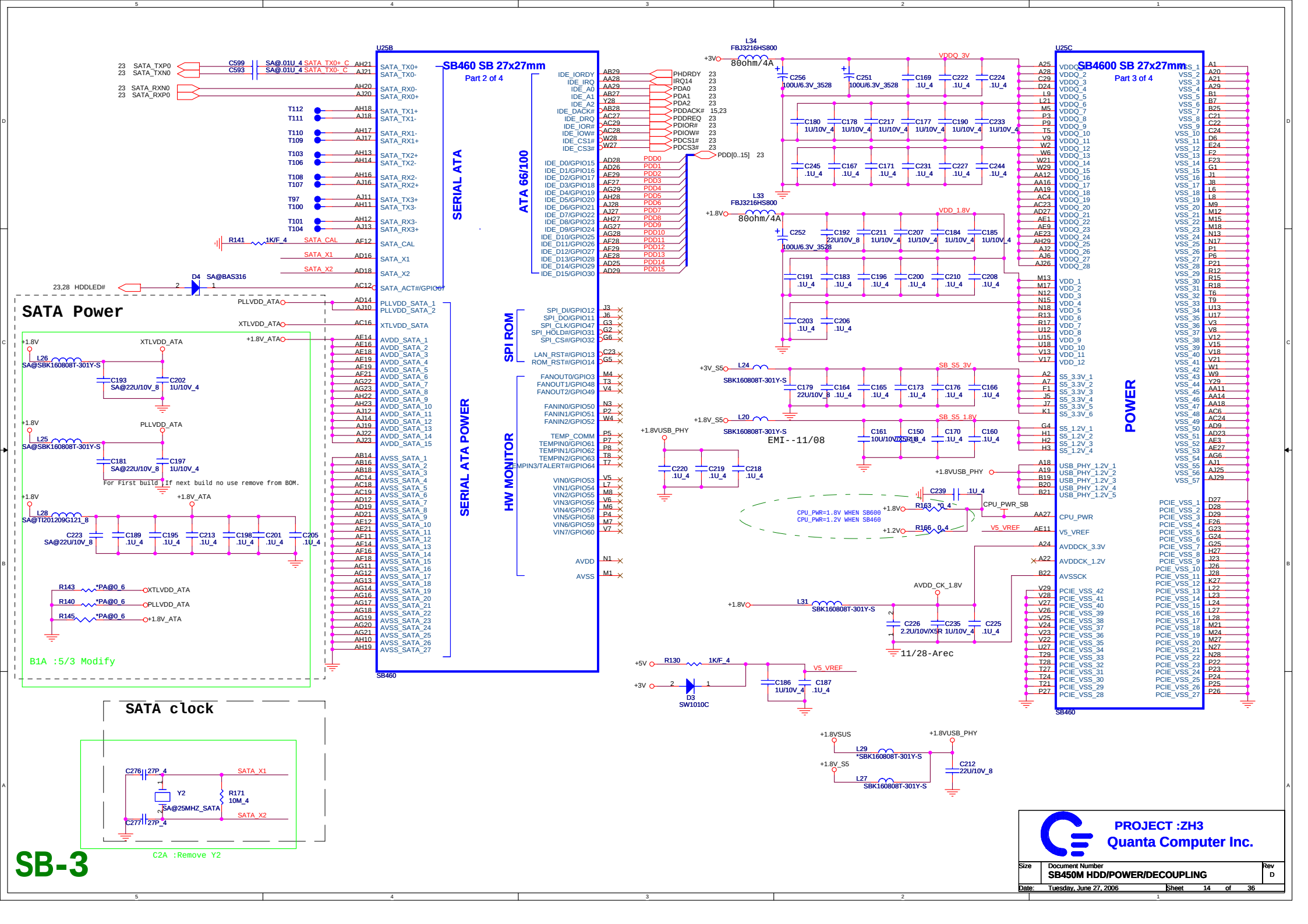
B1A :ADD MB ID

Board ID	ID1	ID0	
00			SATA
01			PATA
10			
11			

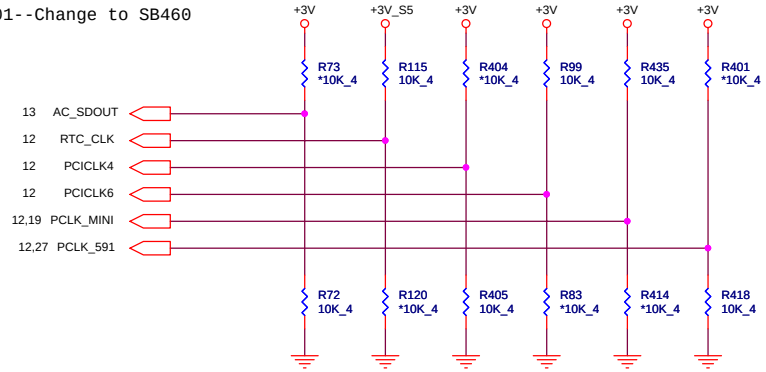
SB-2

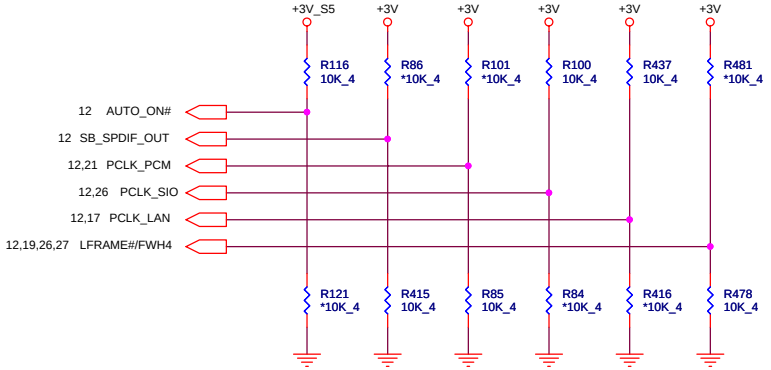
PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	SB460M ACPI/GPIO/USB/AC97	D
Date: Tuesday, June 27, 2006	Sheet 13 of 36	


SB460 SB 27x27mm
Part 2 of 4
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
SATA Power
SATA clock
B1A :5/3 Modify
C2A :Remove Y2
SB-3
SB4600 SB 27x27mm
Part 3 of 4
POWER
EMI--11/08
11/28-Arec
PROJECT :ZH3
Quanta Computer Inc.
SB450M HDD/POWER/DECOUPLING
Tuesday, June 27, 2006

Edison-11/01--Change to SB460



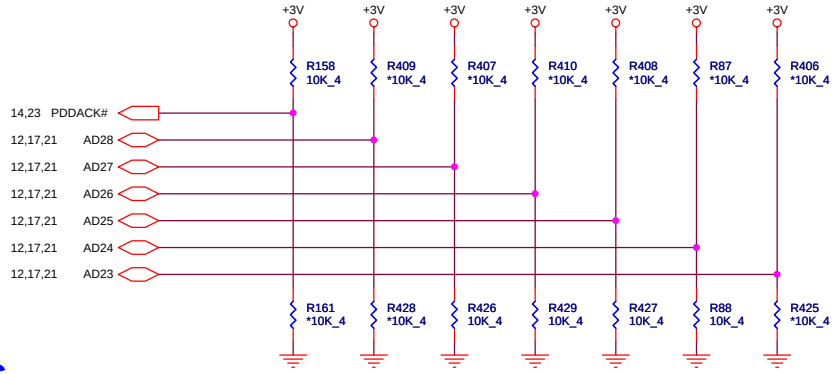


REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI PCLK_591
					PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM DEFAULT L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT	NOTE:FOR SB460,PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]

	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

BIOS ENABLE AFTER STARTUP



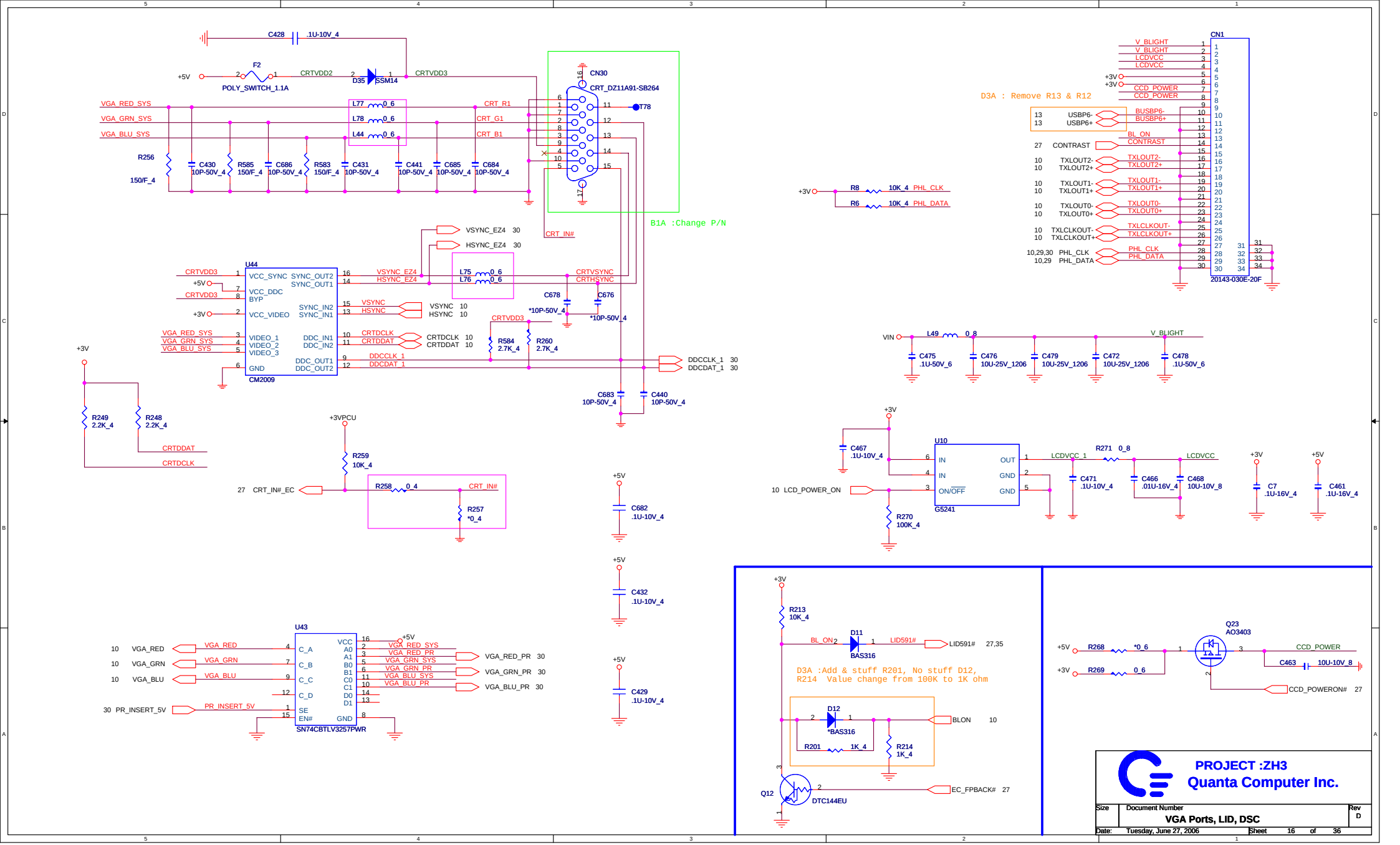
DEBUG STRAPS

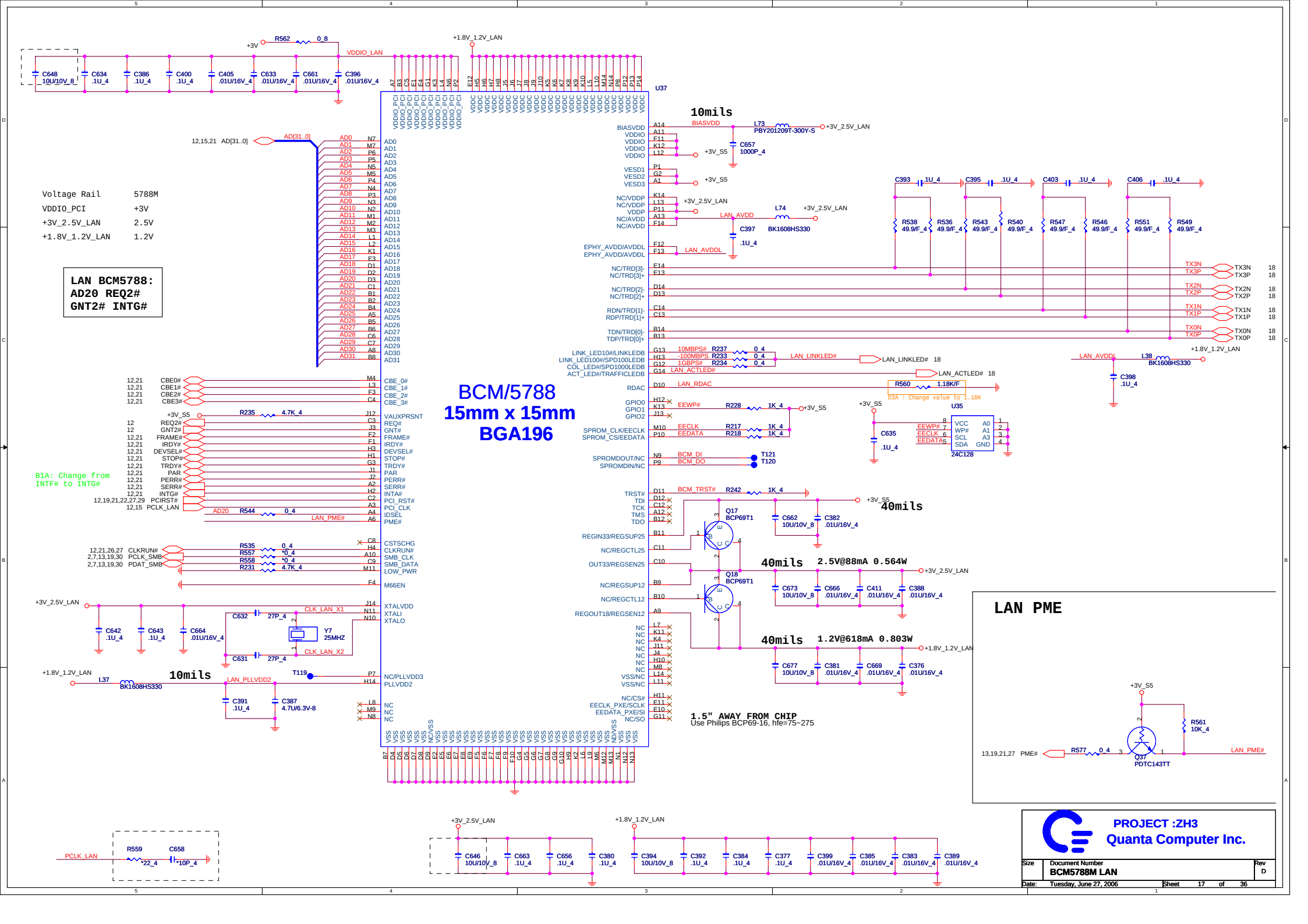
	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

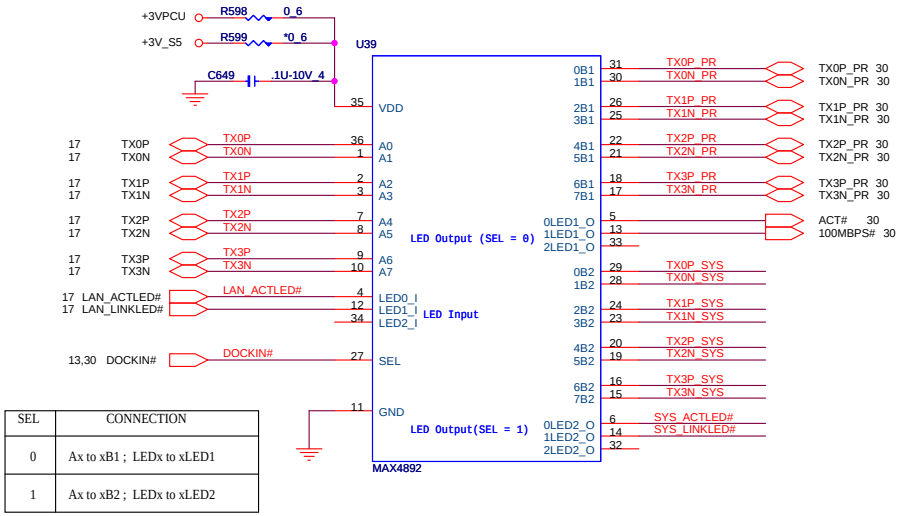
SB-4

PROJECT :ZH3
Quanta Computer Inc.

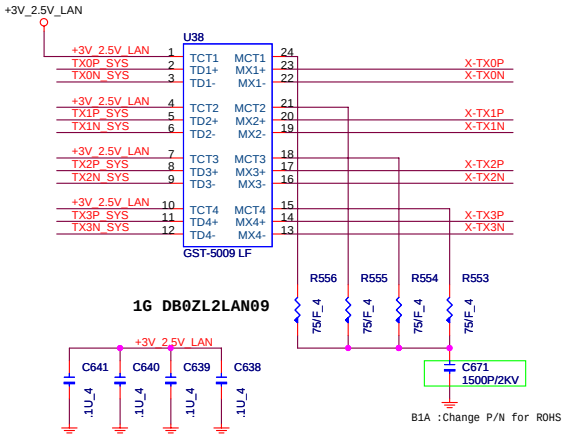
Size	Document Number	Rev
	SB460M STRAPS	D
Date: Tuesday, June 27, 2006	Sheet 15 of 36	

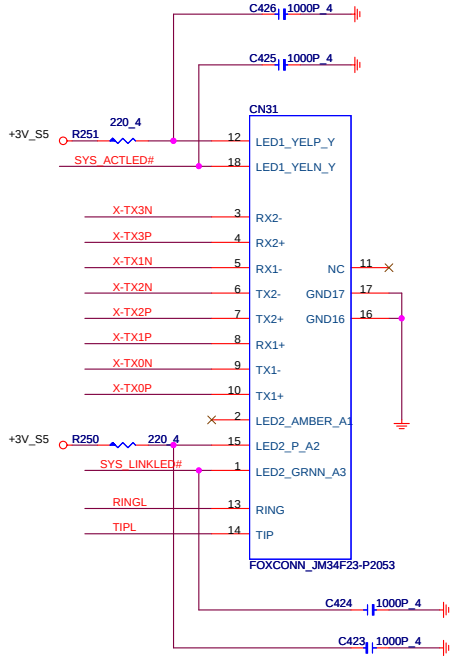

C428 .1U-10V_4
F2
POLY_SWITCH_1.1A
D35 SSM14
CRTVDD2
CRTVDD3
CN30
CRT_DZ11A91-SB264
VGA_RED_SYS
VGA_GRN_SYS
VGA_BLU_SYS
L77 0_6
L78 0_6
L44 0_6
CRT_R1
CRT_G1
CRT_B1
R256 150/F_4
C430 10P-50V_4
R585 150/F_4
C686 10P-50V_4
R583 150/F_4
C431 10P-50V_4
C441 10P-50V_4
C685 10P-50V_4
C684 10P-50V_4
T78
CRT_IN#
B1A :Change P/N
VSYNC_EZ4 30
HSYNC_EZ4 30
U44
CM2009
L75 0_6
L76 0_6
C678 *10P-50V_4
C676 *10P-50V_4
R584 2.7K_4
R260 2.7K_4
DDCCLK_1 30
DDCDAT_1 30
C683 10P-50V_4
C440 10P-50V_4
R249 2.2K_4
R248 2.2K_4
CRTDDAT
CRTDCLK
+3VPCU
R259 10K_4
R258 0_4
R257 *0_4
CRT_IN#_EC
C682 .1U-10V_4
C432 .1U-10V_4
C429 .1U-10V_4
U43
SN74CBTLV3257PWR
VGA_RED_PR 30
VGA_GRN_PR 30
VGA_BLU_PR 30
PR_INSERT_5V
CN1
20143-030E-20F
D3A : Remove R13 & R12
R8 10K_4 PHL_CLK
R6 10K_4 PHL_DATA
L49 0_8
C475 .1U-50V_6
C476 10U-25V_1206
C479 10U-25V_1206
C472 10U-25V_1206
C478 .1U-50V_6
U10
G5241
C467 .1U-10V_4
R271 0_8
C471 .1U-10V_4
C466 .01U-16V_4
C468 10U-10V_8
C7 .1U-16V_4
C461 .1U-16V_4
R270 100K_4
LCD_POWER_ON
D3A :Add & stuff R201, No stuff D12,
R214 Value change from 100K to 1K ohm
R213 10K_4
D11 BAS316
D12 *BAS316
R201 1K_4
R214 1K_4
Q12 DTC144EU
Q23 AO3403
R268 *0_6
R269 0_6
C463 10U-10V_8
CCD_POWERON# 27
PROJECT :ZH3
Quanta Computer Inc.
VGA Ports, LID, DSC
Size
Document Number
Rev D
Date: Tuesday, June 27, 2006
Sheet 16 of 36

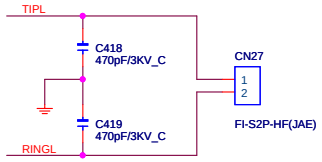

Voltage Rail 5788M
VDDIO_PCI +3V
+3V_2.5V_LAN 2.5V
+1.8V_1.2V_LAN 1.2V
LAN BCM5788:
AD20 REQ2#
GNT2# INTG#
B1A: Change from INTF# to INTG#
BCM/5788
15mm x 15mm
BGA196
U37
10mils
40mils
2.5V@88mA 0.564W
1.2V@618mA 0.803W
1.5" AWAY FROM CHIP
Use Philips BCP69-16, hfe=75~275
LAN PME
PROJECT :ZH3
Quanta Computer Inc.
BCM5788M LAN
Tuesday, June 27, 2006
Sheet 17 of 36



SEL	CONNECTION
0	Ax to xB1 ; LEDx to xLED1
1	Ax to xB2 ; LEDx to xLED2







PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	TRANSFORMER/RJ45-11	D
Date: Tuesday, June 27, 2006	Sheet 18 of 36	

WLAN MINI CARD

B1A:These signals of reserve have be used by wileless module of Foxconn BG. These signals impact LPC. I remove signal line in order to solve the WLAN issue.

C2A :add RC in PCIK_MINI (R=22ohm,C=15P)
D3A :Modify circuit

C687 *15P_4 R341 *22_4 PCLK_MINI_IN

Reserved for debug only

12,21,26,27 SERIRQ R226 0_4
12 LDRQ#1 R227 0_4
12,17,21,22,27,29 PCIRST# R229 0_4
12,15 PCLK_MINI R593 0_4 PCLK_MINI_IN

CN25
MINIPCI EXP_50P_H9

51	Reserved	+3.3V	52		
49	Reserved	GND	50		
47	Reserved	+1.5V	48		
45	Reserved	LED_WPAN#	46		
43	Reserved	LED_WLAN#	44	WLAN_LED	R221 0_4 WIRELESS_LED → WIRELESS_LED 28
41	Reserved	LED_WWAN#	42		
39	Reserved	GND	40		
37	Reserved	USB_D+	38		
35	GND	USB_D-	36		
33	PETp0	GND	34		
31	PETn0	SMB_DATA	32	PDAT_SMB_WLAN	R230 0_4 → PDAT_SMB 2,7,13,17,30
29	GND	SMB_CLK	30	PCLK_SMB_WLAN	R232 0_4 → PCLK_SMB 2,7,13,17,30
27	GND	+1.5V	28		
25	PERp0	GND	26		
23	PERn0	+3.3Vaux	24		
21	GND	PERST#	22		
19	Reserved	Reserved	20		R238 0_4 RF_EN → ALINK_RST# 10,12,23,26,30 / RF_EN 27
17	Reserved	GND	18		
15	GND	Reserved	16		
13	REFCLK+	Reserved	14		
11	REFCLK-	Reserved	12		
9	GND	Reserved	10		
7	CLKREQ#	Reserved	8		
5	Reserved	+1.5V	6		
3	Reserved	GND	4		
1	WAKE#	+3.3V	2		
		GND 53			
		GND 54			

+1.5V +3V_WL_VDD +3VSUS

NO SUPPORT USB

9 PCIE_TXP3
9 PCIE_TXN3
9 PCIE_RXP3
9 PCIE_RXN3
2 CLK_PCIE_MINI_A
2 CLK_PCIE_MINI_A#

T122

13 PCIE_WAKE# R245 *0_4
13,17,21,27 PME# R244 *0_4
+3VSUS
Q16 *DTC144EUA
MINI_A_WAKE#

Reserved for debug only

0_4 R216 LFRAME# → LFRAME#/FWH4 12,15,26,27
0_4 R219 LAD3 → LAD3/FWH3 12,26,27
0_4 R220 LAD2 → LAD2/FWH2 12,26,27
0_4 R222 LAD1 → LAD1/FWH1 12,26,27
0_4 R225 LAD0 → LAD0/FWH0 12,26,27

C2A :Add L79

+3V L79 FBJ3216HS800 +3V_WL_VDD
C373 10U/10V/X5R_8 C410 .1U_4 C412 .1U_4 C369 .1U_4
+1.5V +3VSUS
C409 .1U_4 C372 .1U_4 C390 .1U_4

3G MINI CARD

+3G_VDD +1.5V +3G_VDD +3G_VDD

CN23 *3@MINIPCI EXP_50P_H9

51	Reserved	+3.3V	52		
49	Reserved	GND	50		
47	Reserved	+1.5V	48		
45	Reserved	LED_WPAN#	46		
43	Reserved	LED_WLAN#	44		
41	Reserved	LED_WWAN#	42	3G_LED	R202 *3@0_4 → 3G MINI_LED 28
39	Reserved	GND	40		
37	Reserved	USB_D+	38		R516 *3@0_4 → USBP4+ 13
35	GND	USB_D-	36		R517 *3@0_4 → USBP4- 13
33	PETp0	GND	34		
31	PETn0	SMB_DATA	32	PDAT_SMB_3G	R204 *3@0_4 PDAT_SMB
29	GND	SMB_CLK	30	PCLK_SMB_3G	R206 *3@0_4 PCLK_SMB
27	GND	+1.5V	28		
25	PERp0	GND	26		
23	PERn0	+3.3Vaux	24		
21	GND	PERST#	22	ALINK_RST#	
19	UIM_C4	W_DISABLE#	20	WWAN_DIS#	WWAN_DIS# 27
17	UIM_C8	GND	18		
15	GND	UIM_VPP	16	UIM_VPP	
13	REFCLK+	UIM_RST	14	UIM_RST	
11	REFCLK-	UIM_CLK	12	UIM_CLK	
9	GND	UIM_DATA	10	UIM_DATA	
7	CLKREQ#	UIM_PWR	8	UIM_PWR	
5	Reserved	+1.5V	6		
3	Reserved	GND	4		
1	WAKE#	+3.3V	2		
		GND 53			
		GND 54			

R207 *0_6

D3A: No stuff material of 3G function.

+3V L36 *3@FBJ3216HS800 +3G_VDD
C366 *3@10U/10V/X5R_8 C365 *3@10U/10V/X5R_8 C354 *3@.1U_4 C352 *3@.1U_4 PC34 *3@.47u/X7R/10V_6 C626 *3@10P-50V_4
+1.5V C360 .1U_4

SIM CARD

B1A: Change footprint
C2A: Change footprint & modify SIM card PIN define

JSIM1

UIM_DATA	C7	VCC	GND	C3	UIM_CLK
UIM_VPP	C6	RST	VPP	C2	UIM_RST
	C5	CLK	DATA	C1	UIM_PWR
			GND	1	
			GND	2	
			GND	3	

*3@FOX_WL618E2-U05-7F

UIM_PWR C357 *3@1U/10V

+3V ESD1 *3@CM1293-04SO

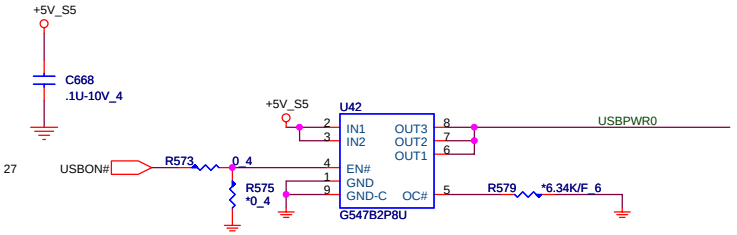
UIM_RESET	1 CH1	CH4 6	UIM_VPP
	2 VN	VP 5	
UIM_CLK	3 CH2	CH3 4	UIM_DATA

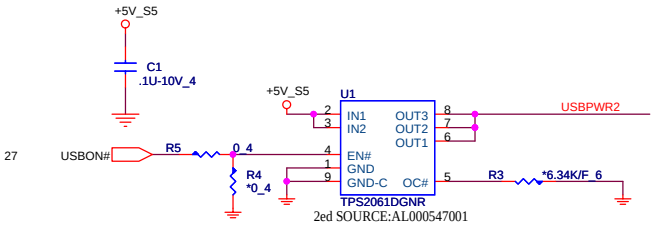
C362 *3@33P/50V_4 C361 *3@33P/50V_4 C364 *3@33P/50V_4 C363 *3@33P/50V_4

PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	MINI CARD (WLAN AND 3G)	D
Date: Tuesday, June 27, 2006	Sheet 19 of 36	

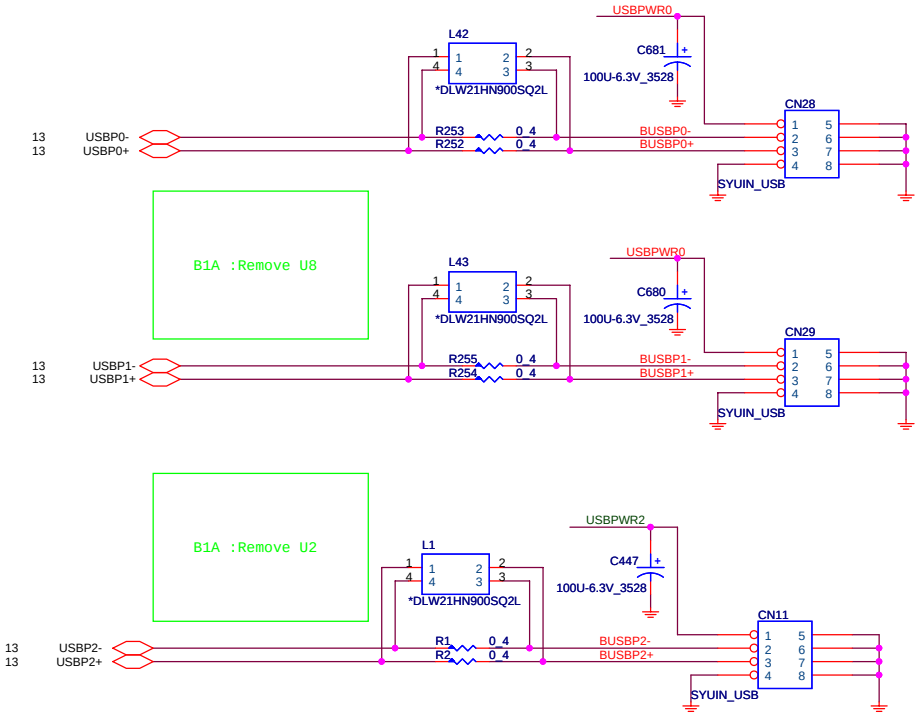
USB POWER SUPPLY



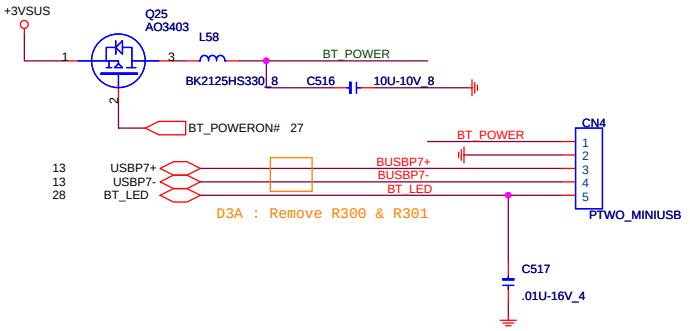


2ed SOURCE:AL000547001

USB

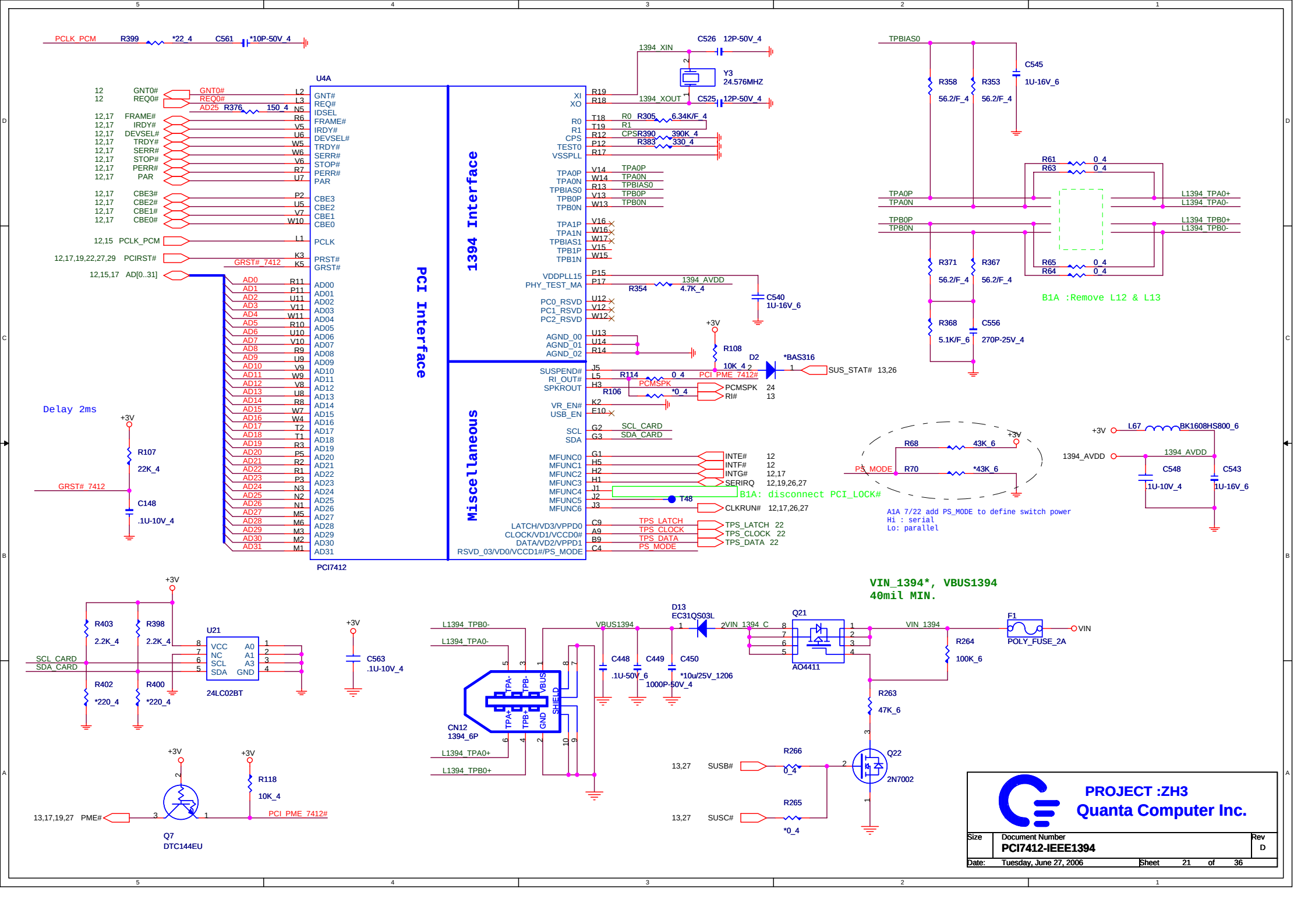


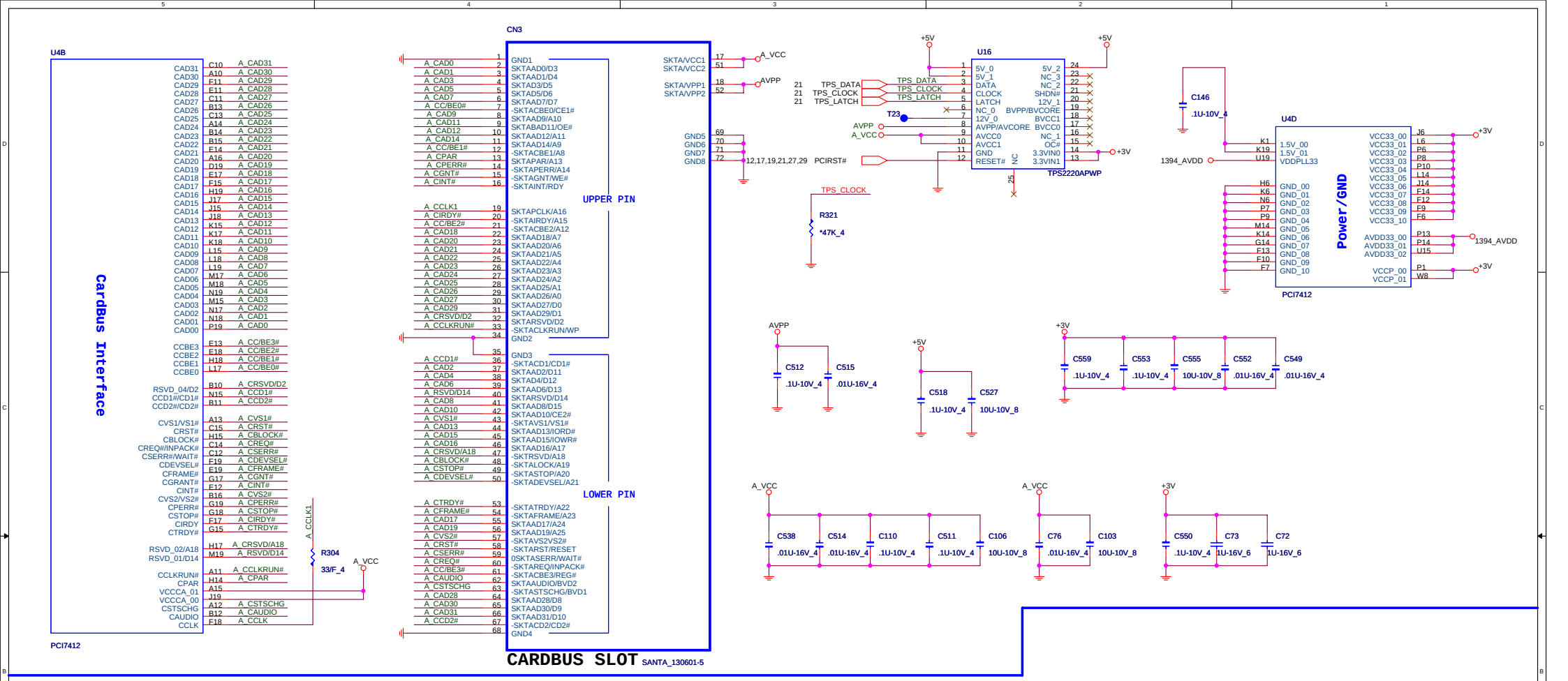
BLUETOOTH MODULE CONNECTOR



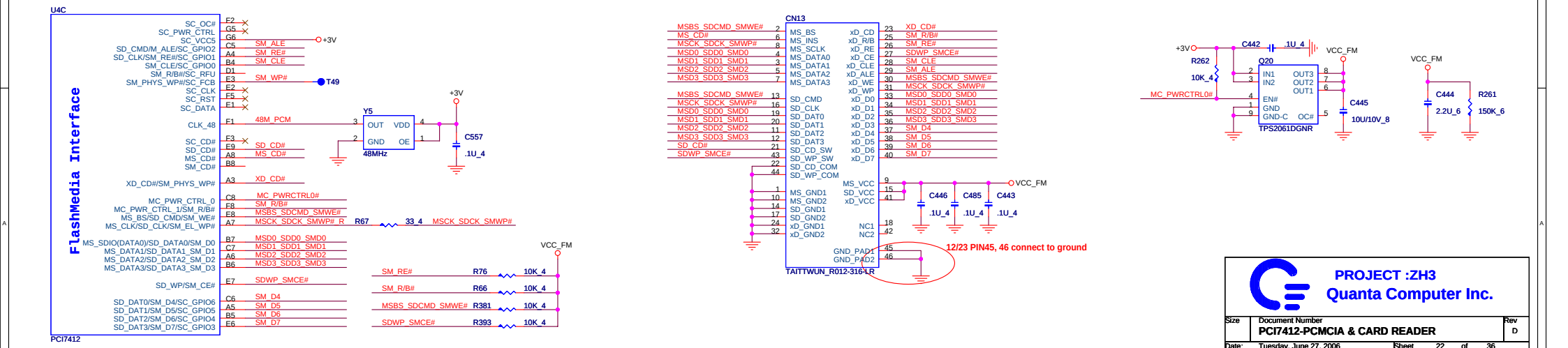
PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	BLUETOOTH , USB	D
Date: Tuesday, June 27, 2006	Sheet 20 of 36	


PCLK_PCM R399 *22_4 C561 *10P-50V_4
U4A
PCI Interface
1394 Interface
Miscellaneous
PCI7412
GNT0# REQ0# AD25 R376 150_4
FRAME# IRDY# DEVSEL# TRDY# SERR# STOP# PERR# PAR
CBE3# CBE2# CBE1# CBE0#
PCLK_PCM
PCIRST#
GRST# 7412
AD[0..31]
1394_XIN C526 12P-50V_4
Y3 24.576MHZ
1394_XOUT C525 12P-50V_4
R0 R305 6.34K/F_4
R1
CPS R390 390K_4
R383 330_4
TPA0P TPA0N TPBIAS0 TPB0P TPB0N
TPA1P TPA1N TPBIAS1 TPB1P TPB1N
VDDPLL15 PHY_TEST_MA
1394_AVDD
R354 4.7K_4
C540 1U-16V_6
PC0_RSVD PC1_RSVD PC2_RSVD
AGND_00 AGND_01 AGND_02
+3V
R108 10K_4
D2 *BAS316
SUS_STAT# 13,26
SUSPEND# RI_OUT# SPKROUT
R114 0_4 PCI_PME_7412#
PCMSPK
R106 *0_4
RI#
VR_EN# USB_EN
SCL SDA
SCL_CARD SDA_CARD
MFUNC0 MFUNC1 MFUNC2 MFUNC3 MFUNC4 MFUNC5 MFUNC6
INTE# INTF# INTG# SERIRQ
T48
B1A: disconnect PCI_LOCK#
CLKRUN#
LATCH/VD3/VPPD0
CLOCK/VD1/VCCD0#
DATA/VD2/VPPD1
RSVD_03/VD0/VCCD1#/PS_MODE
TPS_LATCH TPS_CLOCK TPS_DATA
Delay 2ms
R107 22K_4
C148 .1U-10V_4
TPBIAS0
R358 56.2/F_4
R353 56.2/F_4
C545 1U-16V_6
R61 0_4
R63 0_4
TPA0P TPA0N
TPB0P TPB0N
L1394_TPA0+ L1394_TPA0-
L1394_TPB0+ L1394_TPB0-
R371 56.2/F_4
R367 56.2/F_4
R65 0_4
R64 0_4
R368 5.1K/F_6
C556 270P-25V_4
B1A :Remove L12 & L13
PS_MODE
R68 43K_6
R70 *43K_6
A1A 7/22 add PS_MODE to define switch power
Hi : serial
Lo: parallel
L67 BK1608HS800_6
C548 .1U-10V_4
C543 1U-16V_6
R403 2.2K_4
R398 2.2K_4
R402 *220_4
R400 *220_4
U21
24LC02BT
C563 .1U-10V_4
VIN_1394*, VBUS1394
40mil MIN.
D13 EC31QS03L
Q21 AO4411
F1 POLY_FUSE_2A
VIN
R264 100K_6
R263 47K_6
C448 .1U-50V_6
C449 1000P-50V_4
C450 *10u/25V_1206
CN12 1394_6P
R266 0_4
R265 *0_4
Q22 2N7002
13,27 SUSB#
13,27 SUSC#
R118 10K_4
13,17,19,27 PME#
Q7 DTC144EU
PROJECT :ZH3
Quanta Computer Inc.
Size
Document Number
PCI7412-IEEE1394
Rev D
Date: Tuesday, June 27, 2006
Sheet 21 of 36

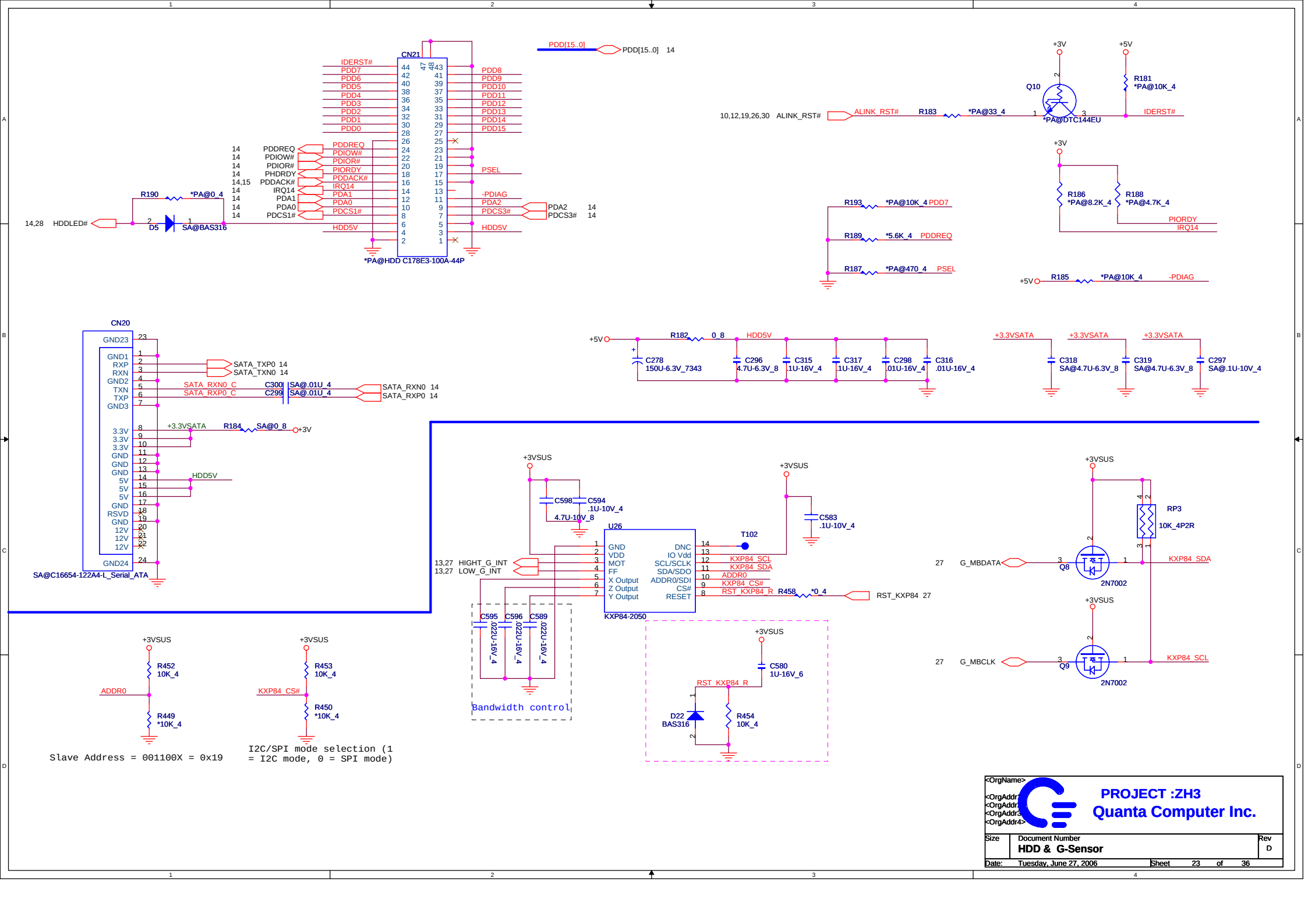


5-IN-1 Card Reader



PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	PCI7412-PCMCIA & CARD READER	D
Date: Tuesday, June 27, 2006	Sheet 22 of 36	

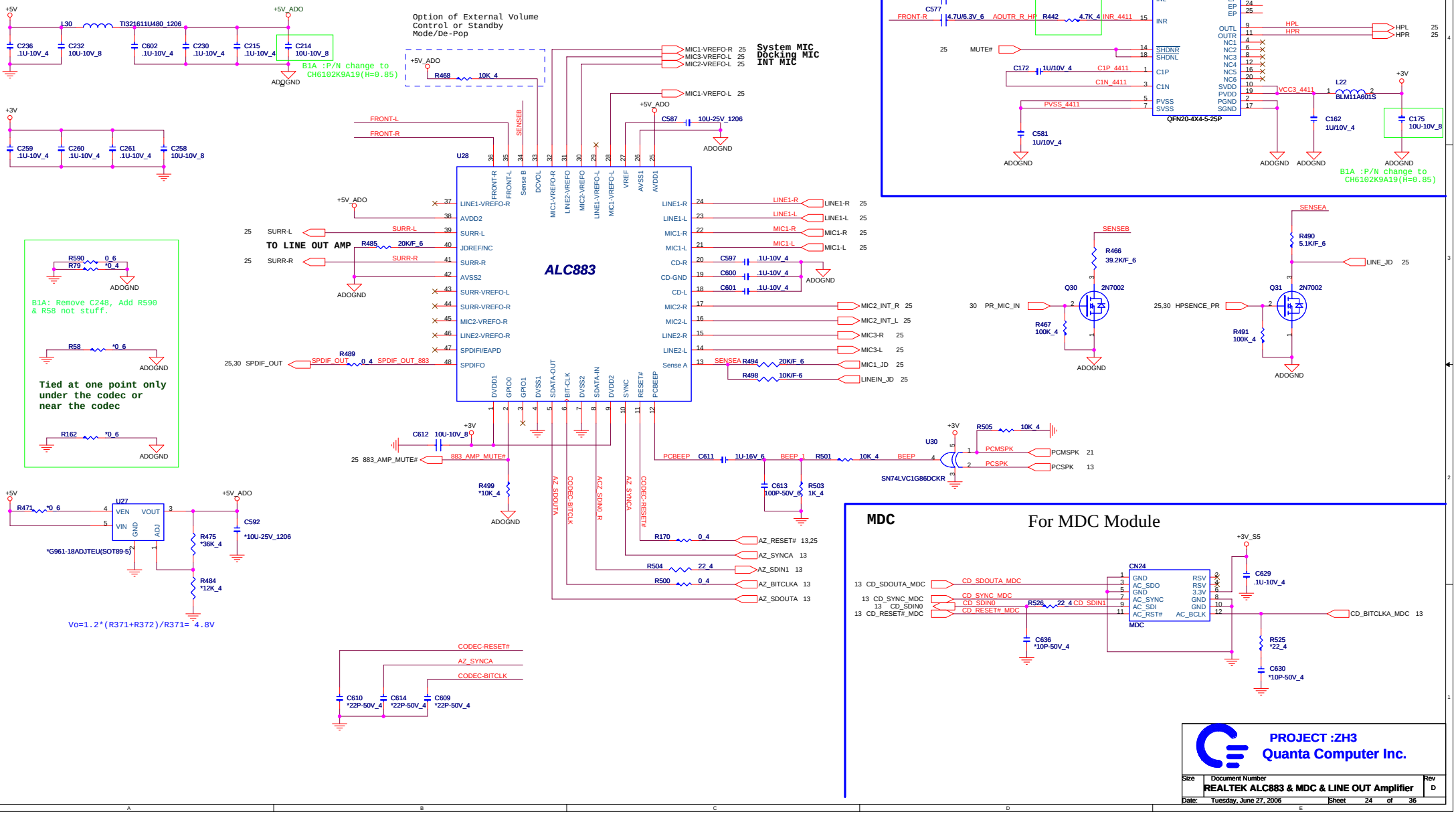


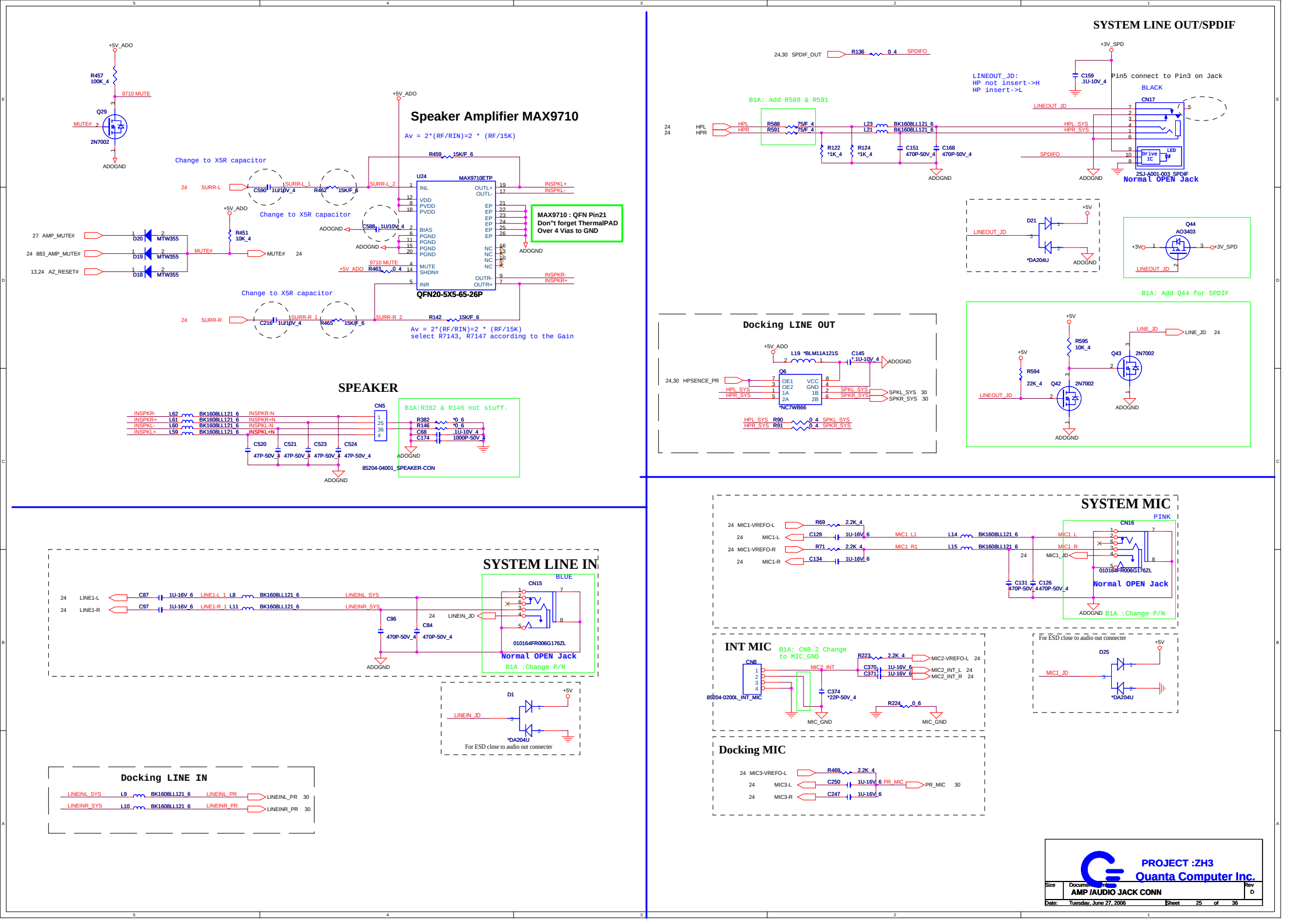
<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

PROJECT :ZH3
Quanta Computer Inc.

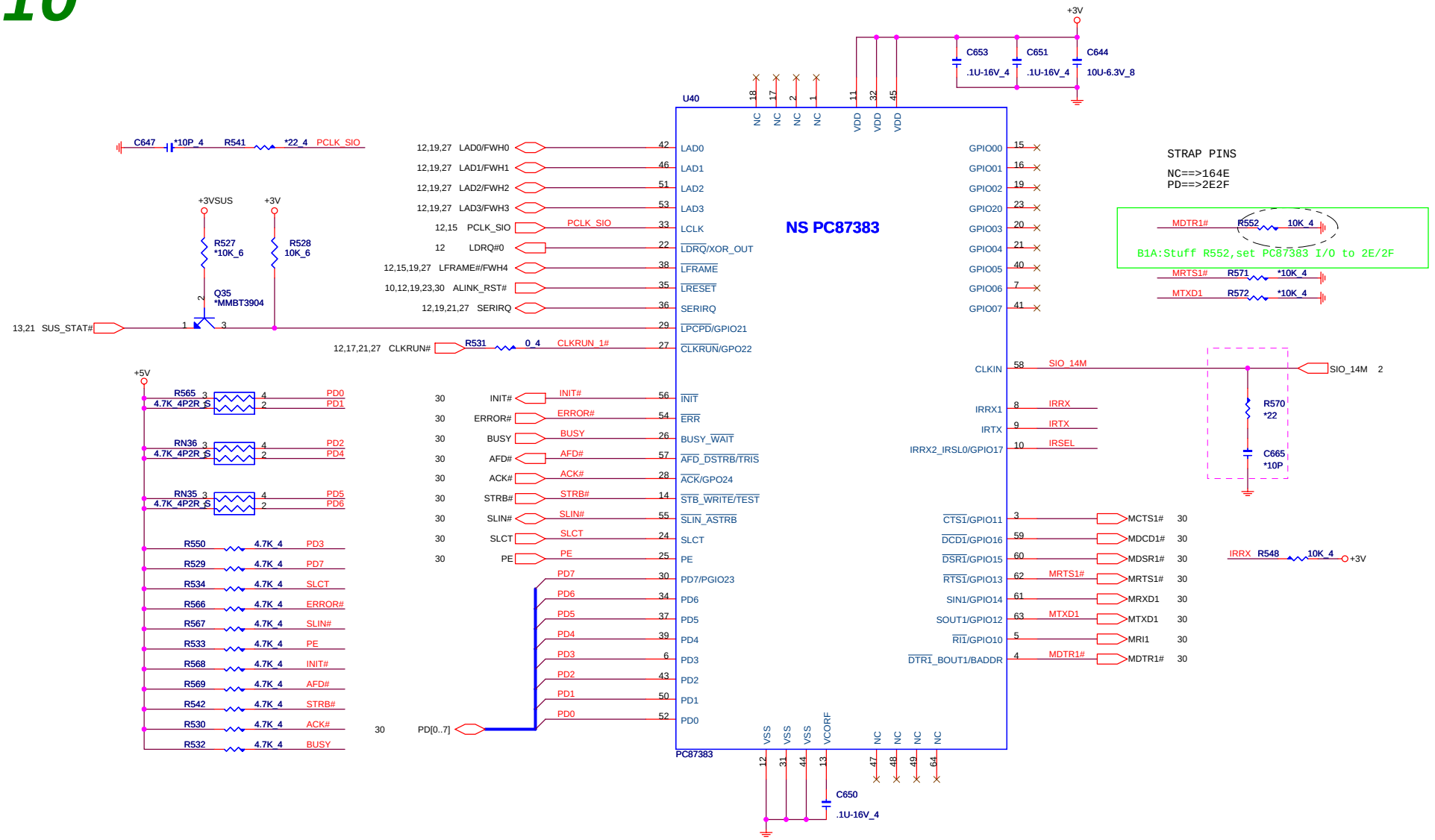
Size	Document Number	Rev
	HDD & G-Sensor	D
Date: Tuesday, June 27, 2006	Sheet 23 of 36	

CODEC(ALC883)

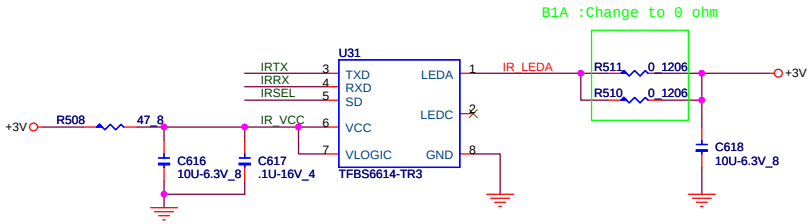



Speaker Amplifier MAX9710
Av = 2*(RF/RIN)=2 * (RF/15K)
Change to X5R capacitor
MAX9710 : QFN Pin21
Don"t forget ThermalPAD
Over 4 Vias to GND
QFN20-5X5-65-26P
Av = 2*(RF/RIN)=2 * (RF/15K)
select R7143, R7147 according to the Gain
SPEAKER
B1A:R382 & R146 not stuff.
85204-04001_SPEAKER-CON
SYSTEM LINE OUT/SPDIF
B1A: Add R588 & R591
LINEOUT_JD:
HP not insert->H
HP insert->L
Pin5 connect to Pin3 on Jack
BLACK
Normal OPEN Jack
2SJ-A001-003_SPDIF
B1A: Add Q44 for SPDIF
Docking LINE OUT
*NC7WB66
SYSTEM LINE IN
BLUE
Normal OPEN Jack
B1A :Change P/N
For ESD close to audio out connecter
Docking LINE IN
SYSTEM MIC
PINK
Normal OPEN Jack
B1A :Change P/N
INT MIC
B1A: CN8.2 Change
to MIC_GND
85204-0200L_INT_MIC
Docking MIC
PROJECT :ZH3
Quanta Computer Inc.
AMP /AUDIO JACK CONN
Tuesday, June 27, 2006
Sheet 25 of 36

SIO



FIR



PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SIO (87383) & FIR	D
Date: Tuesday, June 27, 2006	Sheet 26 of 36	

C2A: Add GPIO for new card (docking side)

INTERNAL PULLUP IN SB

+3V
+3VPCU
Q45 *PDTC143TT
R596 4.7K_4
2,30 EZ_CLKREQ#
EZ_CLKREQ_R#

B1A:Stuff R209,set EC I/O to 4E/4F

BADDR1-0	I/O Address	
	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)(HCFGBAH, HCFGBAL)+1	
1 1	Reserved	

ENV1 R208 10K_4
BADDR0 R209 10K_4
BADDR1 R210 *10K_4
SHBM R212 10K_4
MBCLK R520 4.7K_4
MBDATA R521 4.7K_4
G_MBCLK R518 *4.7K_4
G_MBDATA R519 *4.7K_4

C623 10U-10V_8
C356 .1U-10V_4
C622 .1U-10V_4
C620 .1U-10V_4
C619 .1U-10V_4

VCCRTC
R522 0_4
R200 0_4
C359 .1U-10V_4
C351 .1U-10V_4
C624 *.1U-10V_4
C621 .1U-10V_4

U7
PC97551
VDD VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 AVCC VBAT
591 AVCC

Host interface
SERIRQ
LDRQ
LFRAME
LAD0
LAD1
LAD2
LAD3
LCLK
LRESET
SMI
PWUREQ
IOPD3/ECSCI
GA20/IOPB5
KBRST/IOPB6

AD Input
AD0 TEMP_MBAT T75 TEMP_MBAT 35
AD1 TEMP_ABAT T74
AD2
AD3 WIRELESS_SW# WIRELESS_SW# 28
IOPE0/AD4 BLUETOOTH_SW# BLUETOOTH_SW# 28
IOPE1/AD5 SUSC# SUSC# 13,21
IOPE2/AD6
IOPE3/AD7
DP/AD8
DN/AD9

DA output
DA0 CC-SET CC-SET 35
DA1 LED-SET LED-SET 28
DA2 CONTRAST CONTRAST 16
DA3 VFAN VFAN 28

PWM or PORTA
IOPA0/PWM0 HIGHT_G_INT HIGHT_G_INT 13,23
IOPA1/PWM1 LOW_G_INT LOW_G_INT 13,23
IOPA2/PWM2 CCD_POWERON# CCD_POWERON# 16
IOPA3/PWM3 AMP_MUTE# AMP_MUTE# 25
IOPA4/PWM4 BT1# EMAIL_BTN# 28
IOPA5/PWM5 BT2# WWW_BTN# 28
IOPA6/PWM6 BT3# P1_BTN# 28
IOPA7/PWM7 BT4# P2_BTN# 28

PORTB
IOPB0/URXD CRT_IN# EC CRT_IN# EC 16
IOPB1/UTXD CPU_EC_PROCHOT# CPU_EC_PROCHOT# 5
IOPB2/USCLK RST_KXP84 RST_KXP84 23
IOPB3/SCL1 MBCLK MBCLK 5,35
IOPB4/SDA1 MBDATA MBDATA 5,35
IOPB7/RING/PFAIL PCIRST# PCIRST# 12,17,19,21,22,29

PORTC
IOPC0 EC_FPBACK# EC_FPBACK# 16
IOPC1/SCL2 G_MBCLK G_MBCLK 23
IOPC2/SDA2 G_MBDATA G_MBDATA 23
IOPC3/TA1
IOPC4/TB1/EXWINT22 FANSIG FANSIG 28
IOPC5/TA2 BUZZER
IOPC6/TB2/EXWINT23 LID591# LID591# 16,35
IOPC7/CLKOUT PWROK_1 R211 0_4 EC_PWRGD 5,12,13

PORTD-1
IOPD0/RI1/EXWINT20 WWAN_DIS# WWAN_DIS# 19
IOPD1/RI2/EXWINT21 ACIN ACIN 35
IOPD2/EXWINT24 591_PME#

PORTE
IOPE4/SWIN NBSWON# NBSWON# 28
IOPE5/EXWINT40 SUSB# SUSB# 13,21
IOPE6/LPCPD/EXWIN45 EZ_CLKREQ_R#
IOPE7/CLKRUN/EXWINT46 CLKRUN# CLKRUN# 12,17,21,26

PORTH
IOPH0/A0/ENV0 ENV0
IOPH1/A1/ENV1 ENV1
IOPH2/A2/BADDR0 BADDR0
IOPH3/A3/BADDR1 BADDR1
IOPH4/A4/TRIS TRIS
IOPH5/A5/SHBM SHBM
IOPH6/A6 A6
IOPH7/A7 A7

PORTI
IOPI0/D0 D0
IOPI1/D1 D1
IOPI2/D2 D2
IOPI3/D3 D3
IOPI4/D4 D4
IOPI5/D5 D5
IOPI6/D6 D6
IOPI7/D7 D7

PORTJ-1
IOPJ0/RD RD#
IOPJ1/WR0 WR#

SELIO

PORTD-2
IOPD4 1.2V_ON T126 1.2V_ON 32
IOPD5 D/C# D/C- 35
IOPD6 BLC# T123
IOPD7

PORTK
IOPK0/A8 A8
IOPK1/A9 A9
IOPK2/A10 A10
IOPK3/A11 A11
IOPK4/A12 A12
IOPK5/A13/BE0 A13
IOPK6/A14/BE1 A14
IOPK7/A15/CBRD A15

PORTL
IOPL0/A16 A16
IOPL1/A17 A17
IOPL2/A18 A18
IOPL3/A19 A19
IOPL4/WR1 T125

JTAG debug port
TINT
TCK
TDO
TDI
TMS

PS2 interface
PSCLK1/IOPF0 MSCLK
PSDAT1/IOPF1 MSDATA
PSCLK2/IOPF2 KPCLK
PSDAT2/IOPF3 KPDATA
PSCLK3/IOPF4 TBCLK
PSDAT3/IOPF5 TBDATA
PSCLK4/IOPF6 CAPSLED#
PSDAT4/IOPF7 NUMLED#

PORTM
IOPM0/D8 RF_EN
IOPM1/D9 BT_POWERON#
IOPM2/D10 RSMRST#
IOPM3/D11 NB_PWRGD
IOPM4/D12 VRON
IOPM5/D13 MAINON
IOPM6/D14 SUSON
IOPM7/D15 S5_ON

SEL0
SEL1
CLK

32KX1/32KCLKOUT
32KX2
591_32KX1
591_32KX2
R524 20M_6
R523 62K/F_6
Y6 32.768KHZ
C628 10P-50V_4
C627 10P-50V_4

PR_STS
BT_POWERON#
NB_PWRGD
VRON
MAINON
SUSON
S5_ON
CS#

GND1 GND2 GND3 GND4 GND5 GND6 GND7 AGND
NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10
C353 1U-16V_6

B1A: Second source 87541

+3VPCU
R203 470K_4
12,19,21,26 SERIRQ
12,15,19,26 LFRAME#/FWH4
12,19,26 LAD0/FWH0
12,19,26 LAD1/FWH1
12,19,26 LAD2/FWH2
12,19,26 LAD3/FWH3
12,15 PCLK_591
13 KBSMI#
13 SWI#
13 SCI#
13 GATEA20
13 RCIN#
D30 D29 BAS316 *MTW355
D10 BAS316
D33 BAS316
D31 BAS316

U34
24LC08
MBCLK MBDATA
C625 .1U-10V_4

PCLK_591
R205 *22_4
C355 *10P-50V_4

+5V
RP2 4.7K_8P4R
MSCLK MSDATA KPCLK KPDATA TBCLK TBDATA CAPSLED# NUMLED#

MX0 MX1 MX2 MX3 MX4 MX5 MX6 MX7
KBSIN0 KBSIN1 KBSIN2 KBSIN3 KBSIN4 KBSIN5 KBSIN6 KBSIN7
MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15
KBSOUT0 KBSOUT1 KBSOUT2 KBSOUT3 KBSOUT4 KBSOUT5 KBSOUT6 KBSOUT7 KBSOUT8 KBSOUT9 KBSOUT10 KBSOUT11 KBSOUT12 KBSOUT13 KBSOUT14 KBSOUT15

+3V
R199 10K_4
HWPG

+3VPCU
R512 WIRELESS_SW# 4.7K_4
R513 BLUETOOTH_SW# 4.7K_4

U33
ST Micro M29W008AB/AMD-29LV081B/SST39VF080
ENV0 ENV1 BADDR0 BADDR1 TRIS SHBM A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 CS# RD# WR#
D0 D1 D2 D3 D4 D5 D6 D7
RESET#/NC RY/BY#/NC NC1 NC2 NC3 VCC VCC GND GND CE# OE# WE#
VCC1_PWROK T77 +3VPCU

D32 BAS316 DNBSWON# 13

D3A: EZ_CLKREQ_R# Change from PIN 32 to PIN24

+3VPCU
R215 *10K_4
VCC1_PWROK
C367 .1U-10V_4

D3A :Remove NET (3G_SW#) PIN41

C2A:Remove location:U32(512M BIOS)

BIU configuration should match flash speed used

31,32 CPU_COREPG CPU_COREPG D6 MTW355 HWPG
34 HWPG_SYS HWPG_SYS D7 MTW355
32 HWPG_1.2V HWPG_DDR D8 MTW355
33 HWPG_1.8V 1V5_PGD D9 MTW355

+3V_S5 +3V_S5 +3VPCU
R514 *4.7K_4
Q34 PDTC143TT
R515 *4.7K_4
13,17,19,21 PME# 591_PME#

+5V_S5
BZ1 KCVG084B16_BUZZER
R247 0_6
BUZZER R246 330_4
Q19 MMBT3904
C422 .022U-16V_4

B1A :Change P/N for ROHS

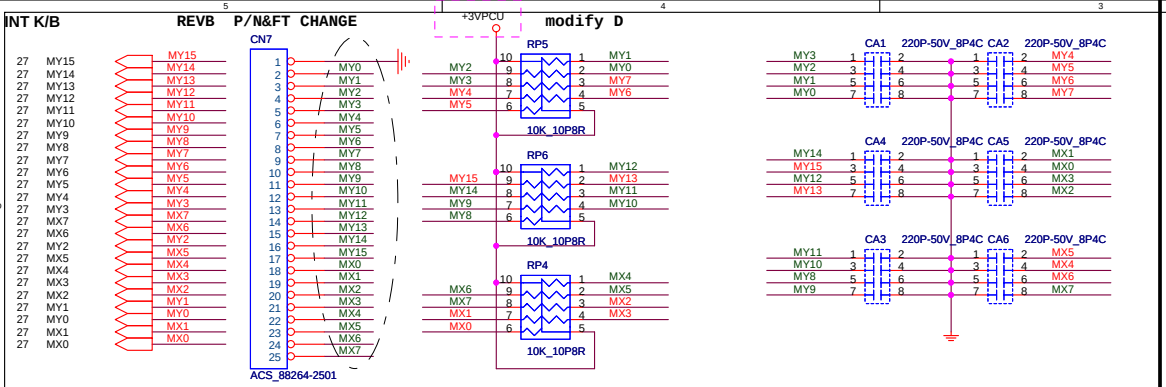
PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	97551 & FLASH	D
Date: Tuesday, June 27, 2006	Sheet 27 of 36	

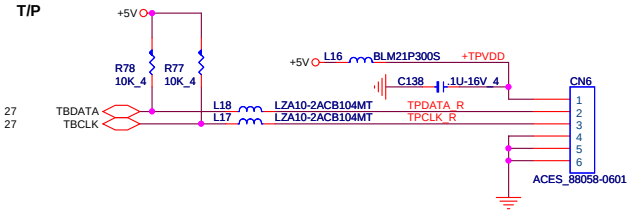
INT K/B

REVB P/N&FT CHANGE

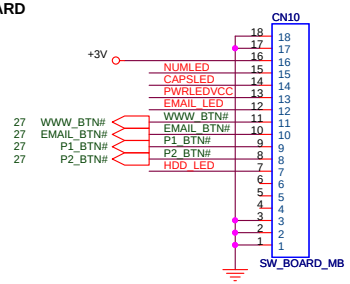
modify D



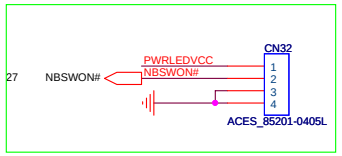
T/P



SW BOARD



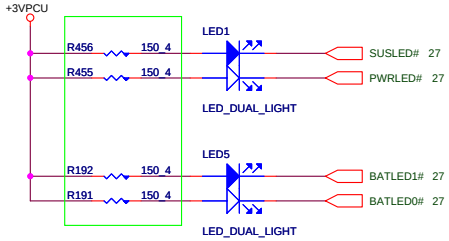
LED conn



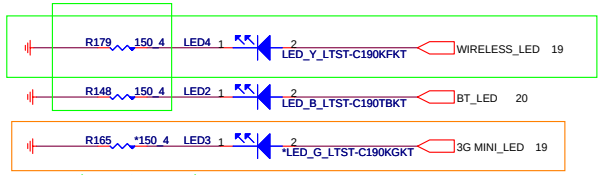
B1A: Move to MB for ME request.
Change P/N

PWR & BT & W/L & BATT LED

B1A:Change to 150 ohm



B1A:T60H921, ABG card, pin44 (LED) is high active



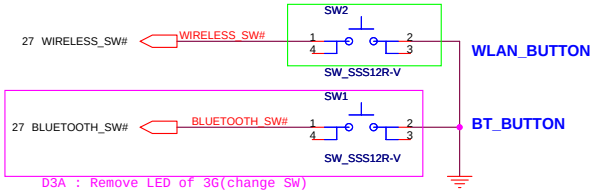
B1A:Change to 150 ohm

D3A : No stuff LED3 & R165

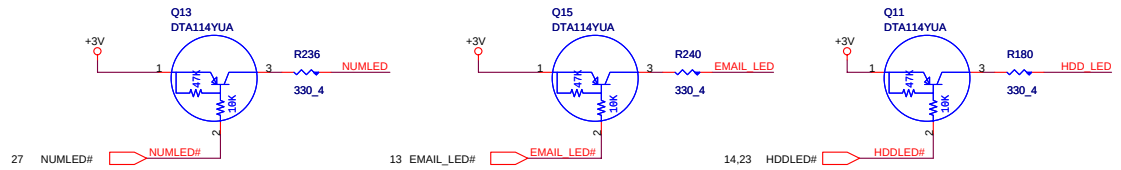
WL/BT BUTTON

B1A: Modify, Solve issue of LED.
Change PIN3 to WIRELESS_SW#
Change PIN4 to float

B1A :Change vendor

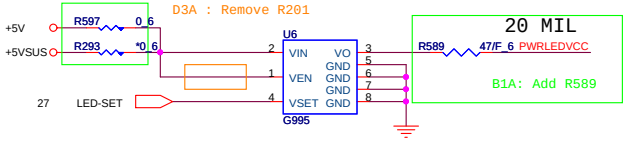


D3A : Remove LED of 3G(change SW)



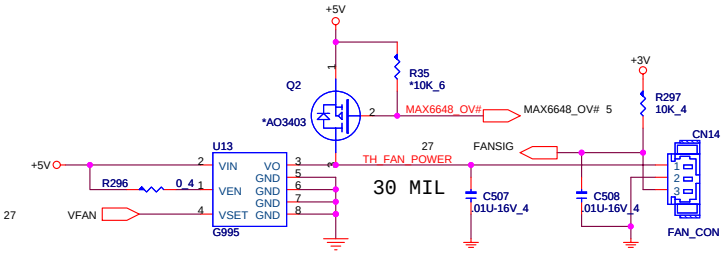
B1A:Change from +5V to +5V_S5
C2A:Change from +5V_S5 to +5VSUS

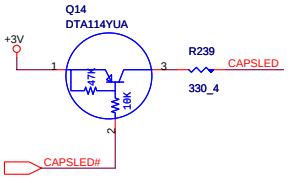
D3A : Remove R201



B1A: Add R589

FAN

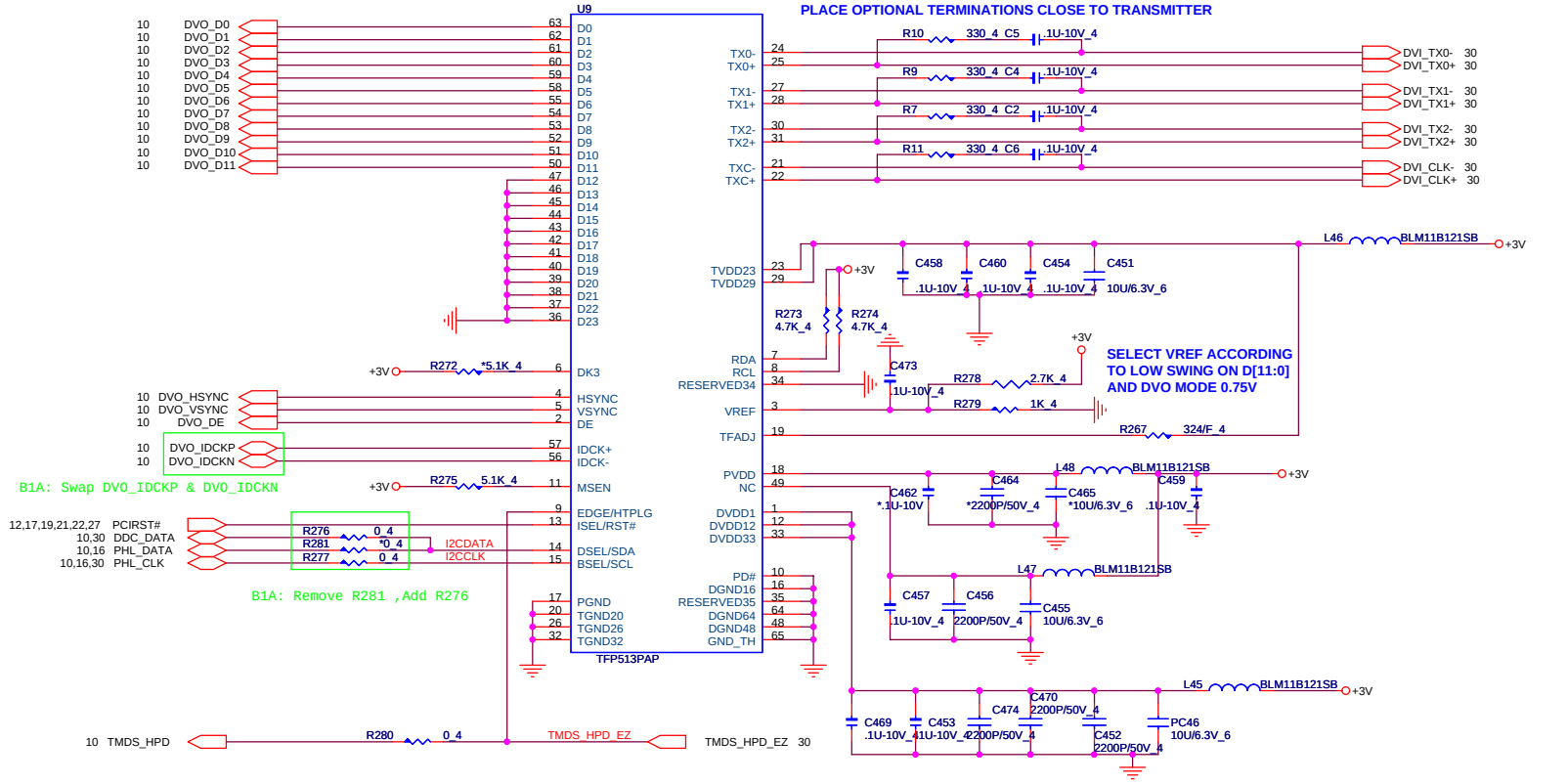




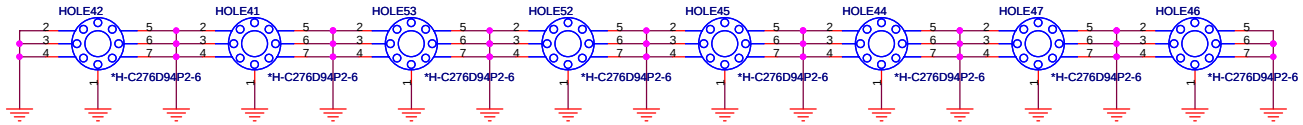
PROJECT :ZH3
Quanta Computer Inc.

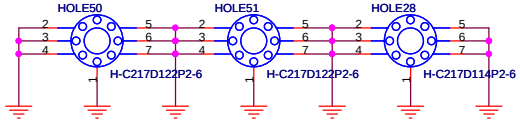
Size	Document Number	Rev
	LED & SW & KB & TP & FAN	D

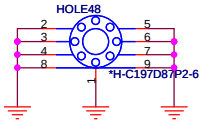
Date: Tuesday, June 27, 2006 Sheet 28 of 36

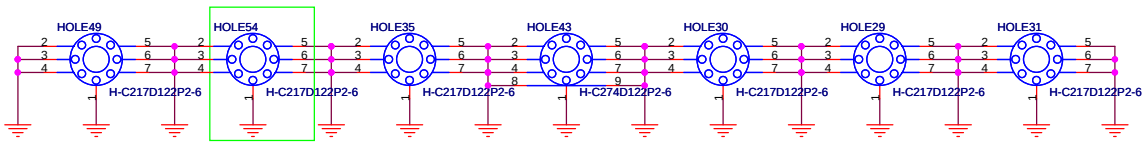


HOLE



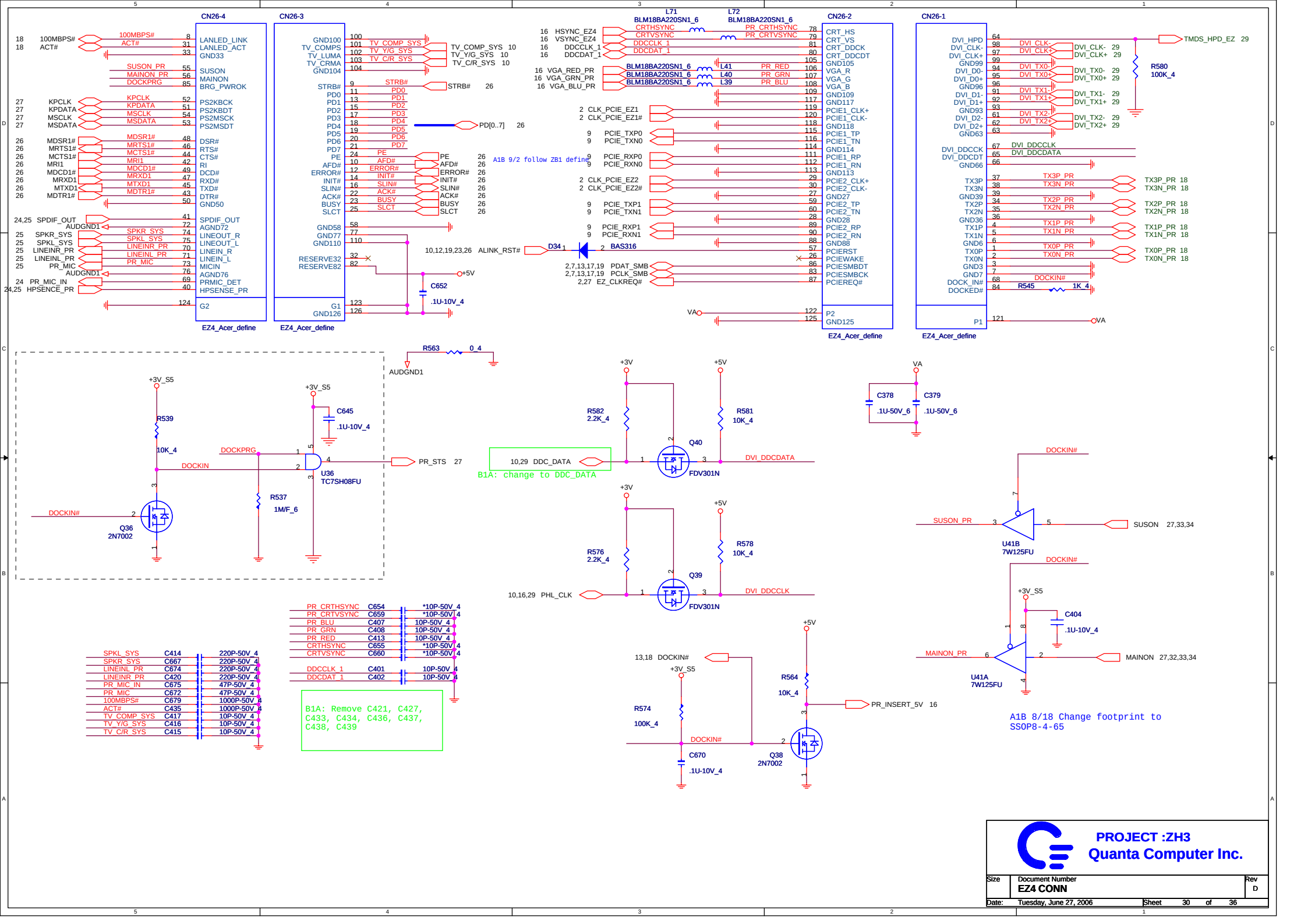


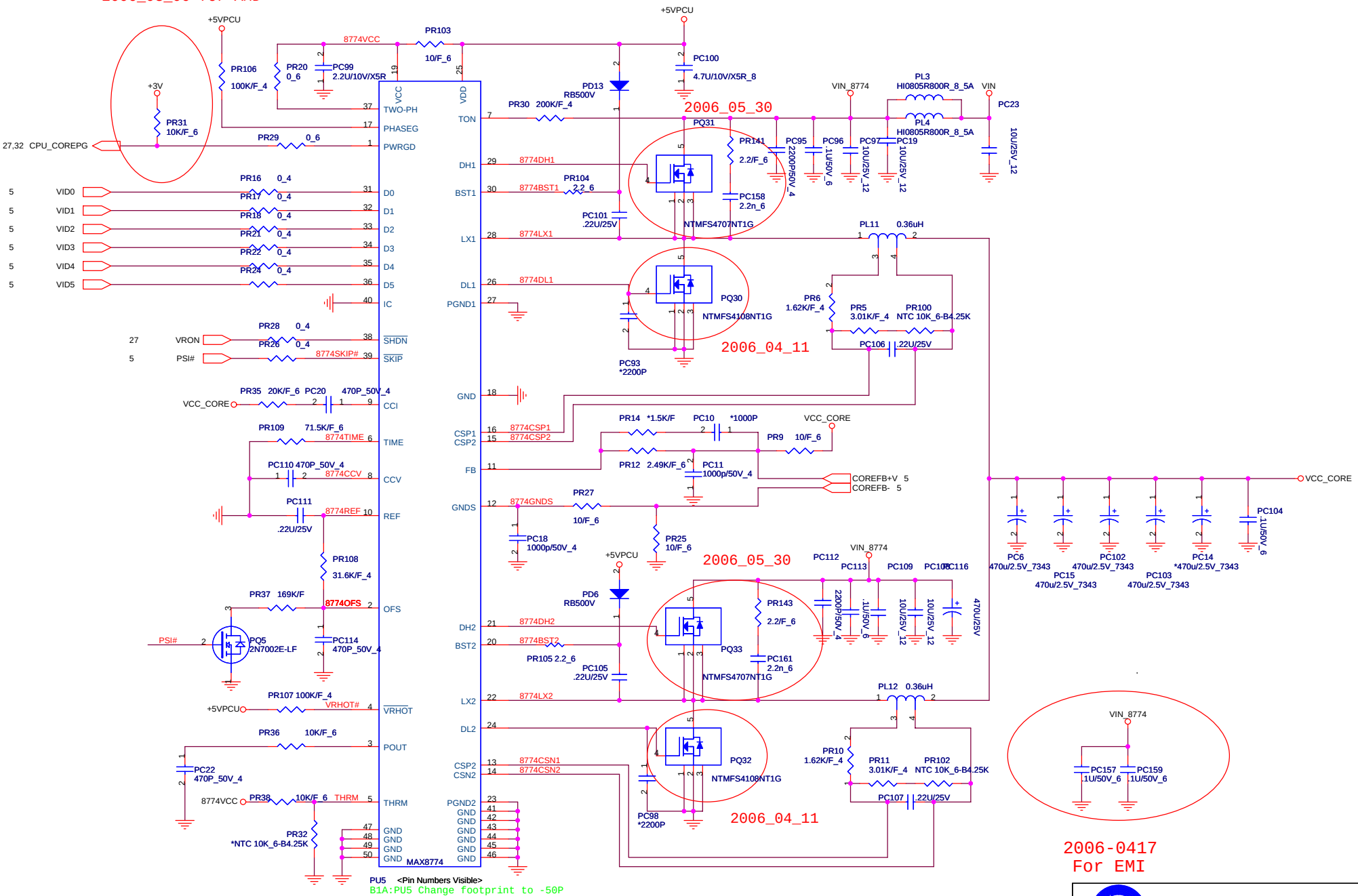




PROJECT :ZH3
Quanta Computer Inc.

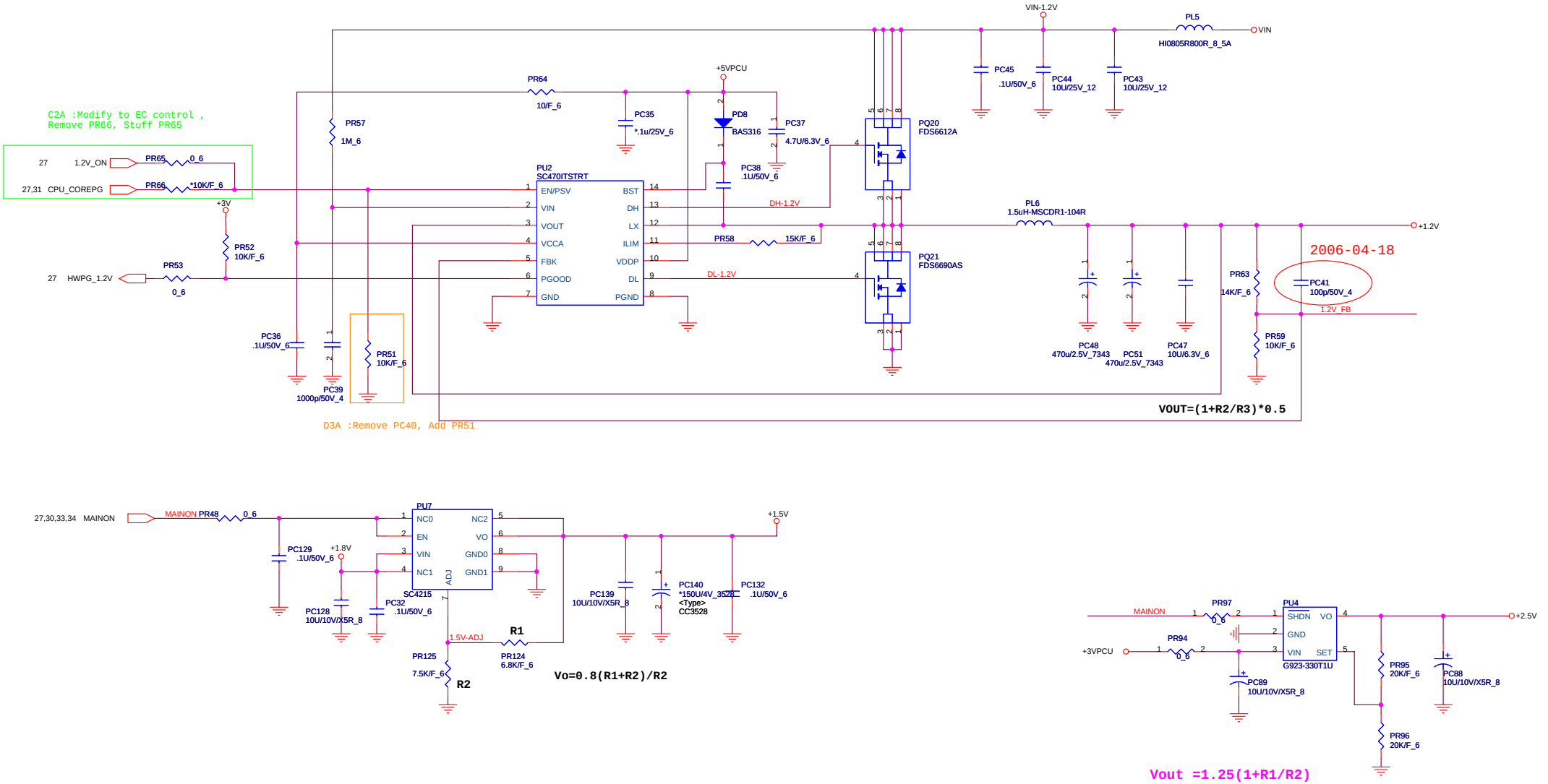
Size	Document Number	Rev
	CH7307& HOLE	D
Date: Tuesday, June 27, 2006	Sheet 29 of 36	


CN26-4
CN26-3
CN26-2
CN26-1
L71
L72
BLM18BA220SN1_6
EZ4_Acer_define
LANLED_LINK
LANLED_ACT
GND33
SUSON
MAINON
BRG_PWROK
PS2KBCK
PS2KBDT
PS2MSCK
PS2MSDT
DSR#
RTS#
CTS#
RI
DCD#
RXD#
TXD#
DTR#
GND50
SPDIF_OUT
AGND72
LINEOUT_R
LINEOUT_L
LINEIN_R
LINEIN_L
MICIN
AGND76
PRMIC_DET
HPSENSE_PR
G2
G1
GND126
GND100
TV_COMPS
TV_LUMA
TV_CRMA
GND104
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
AFD#
ERROR#
INIT#
SLIN#
ACK#
BUSY
SLCT
GND58
GND77
GND110
RESERVE32
RESERVE82
HSYNC_EZ4
VSYNC_EZ4
DDCCLK_1
DDCDAT_1
VGA_RED_PR
VGA_GRN_PR
VGA_BLU_PR
PR_CRTHSYNC
PR_CRTVSYNC
PR_RED
PR_GRN
PR_BLU
CRT_HS
CRT_VS
CRT_DDCK
CRT_DDCDT
GND105
VGA_R
VGA_G
VGA_B
GND109
GND117
PCIE1_CLK+
PCIE1_CLK-
GND118
PCIE1_TP
PCIE1_TN
GND114
PCIE1_RP
PCIE1_RN
GND113
PCIE2_CLK+
PCIE2_CLK-
GND27
PCIE2_TP
PCIE2_TN
GND28
PCIE2_RP
PCIE2_RN
GND88
PCIERST
PCIEWAKE
PCIESMBDT
PCIESMBCK
PCIEREQ#
P2
GND125
P1
DVI_HPD
DVI_CLK-
DVI_CLK+
GND99
DVI_D0-
DVI_D0+
GND96
DVI_D1-
DVI_D1+
GND93
DVI_D2-
DVI_D2+
GND63
DVI_DDCCK
DVI_DDCDT
GND66
TX3P
TX3N
GND39
TX2P
TX2N
GND36
TX1P
TX1N
GND6
TX0P
TX0N
GND3
GND7
DOCK_IN#
DOCKED#
R580
100K_4
TMDS_HPD_EZ
DVI_CLK-
DVI_CLK+
DVI_TX0-
DVI_TX0+
DVI_TX1-
DVI_TX1+
DVI_TX2-
DVI_TX2+
DVI_DDCCLK
DVI_DDCDATA
TX3P_PR
TX3N_PR
TX2P_PR
TX2N_PR
TX1P_PR
TX1N_PR
TX0P_PR
TX0N_PR
DOCKIN#
R545
1K_4
VA
D34
BAS316
ALINK_RST#
C652
.1U-10V_4
+5V
A1B 9/2 follow ZB1 define
R563
0_4
AUDGND1
R539
10K_4
C645
.1U-10V_4
DOCKPRG
DOCKIN
U36
TC7SH08FU
R537
1M/F_6
Q36
2N7002
PR_STS
R582
2.2K_4
R581
10K_4
Q40
FDV301N
DDC_DATA
B1A: change to DDC_DATA
C378
C379
.1U-50V_6
R576
2.2K_4
R578
10K_4
Q39
PHL_CLK
U41B
7W125FU
SUSON_PR
SUSON
U41A
MAINON_PR
MAINON
C404
R564
10K_4
R574
100K_4
C670
Q38
PR_INSERT_5V
A1B 8/18 Change footprint to SSOP8-4-65
SPKL_SYS C414 220P-50V_4
SPKR_SYS C667 220P-50V_4
LINEINL_PR C674 220P-50V_4
LINEINR_PR C420 220P-50V_4
PR_MIC_IN C675 47P-50V_4
PR_MIC C672 47P-50V_4
100MBPS# C679 1000P-50V_4
ACT# C435 1000P-50V_4
TV_COMP_SYS C417 10P-50V_4
TV_Y/G_SYS C416 10P-50V_4
TV_C/R_SYS C415 10P-50V_4
PR_CRTHSYNC C654 *10P-50V_4
PR_CRTVSYNC C659 *10P-50V_4
PR_BLU C407 10P-50V_4
PR_GRN C408 10P-50V_4
PR_RED C413 10P-50V_4
CRTHSYNC C655 *10P-50V_4
CRTVSYNC C660 *10P-50V_4
DDCCLK_1 C401 10P-50V_4
DDCDAT_1 C402 10P-50V_4
B1A: Remove C421, C427, C433, C434, C436, C437, C438, C439
PROJECT :ZH3
Quanta Computer Inc.
Size
Document Number
EZ4 CONN
Rev
D
Date: Tuesday, June 27, 2006
Sheet 30 of 36



PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	CPU CORE MAX8760	D
Date: Tuesday, June 27, 2006	Sheet 31 of 36	

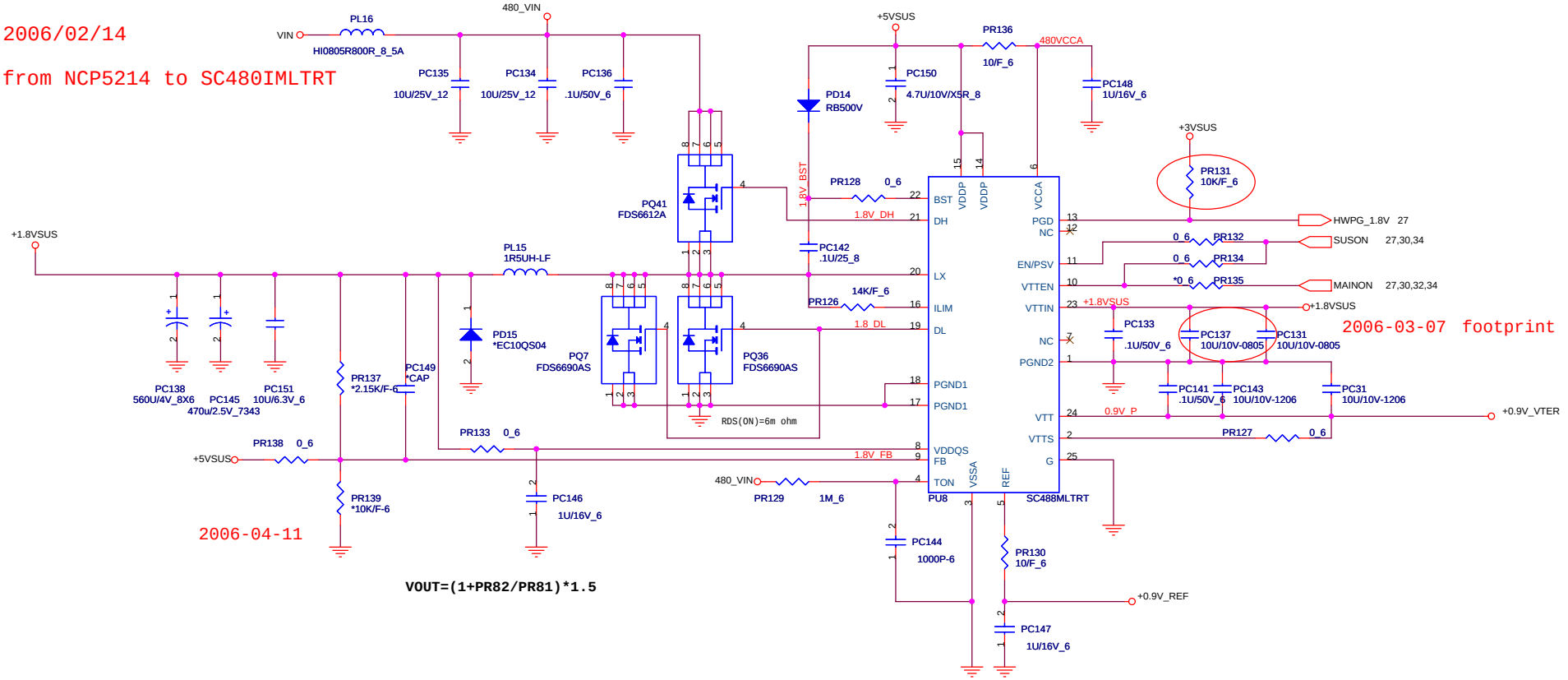


PROJECT :ZH3
Quanta Computer Inc.

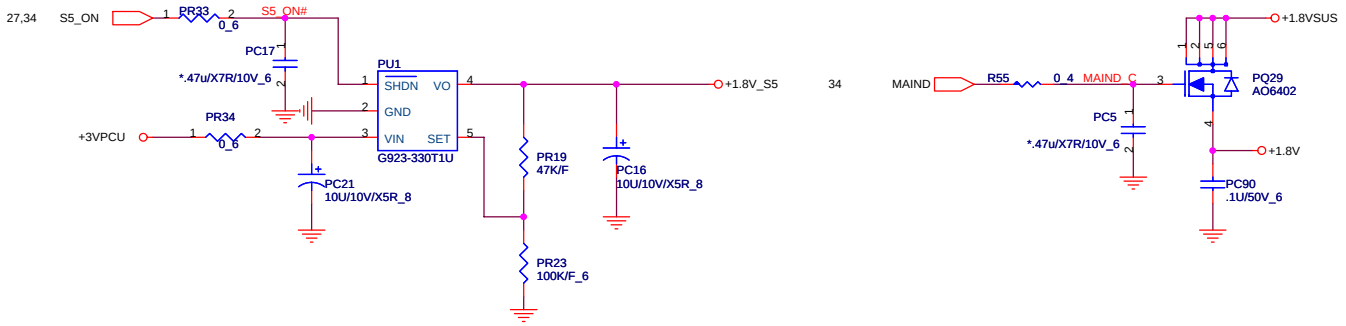
Size	Document Number	Rev
Custom	+1.2V & NBRUN	D
Date: Tuesday, June 27, 2006	Sheet 32 of 36	

2006/02/14

change from NCP5214 to SC480IMLTRT



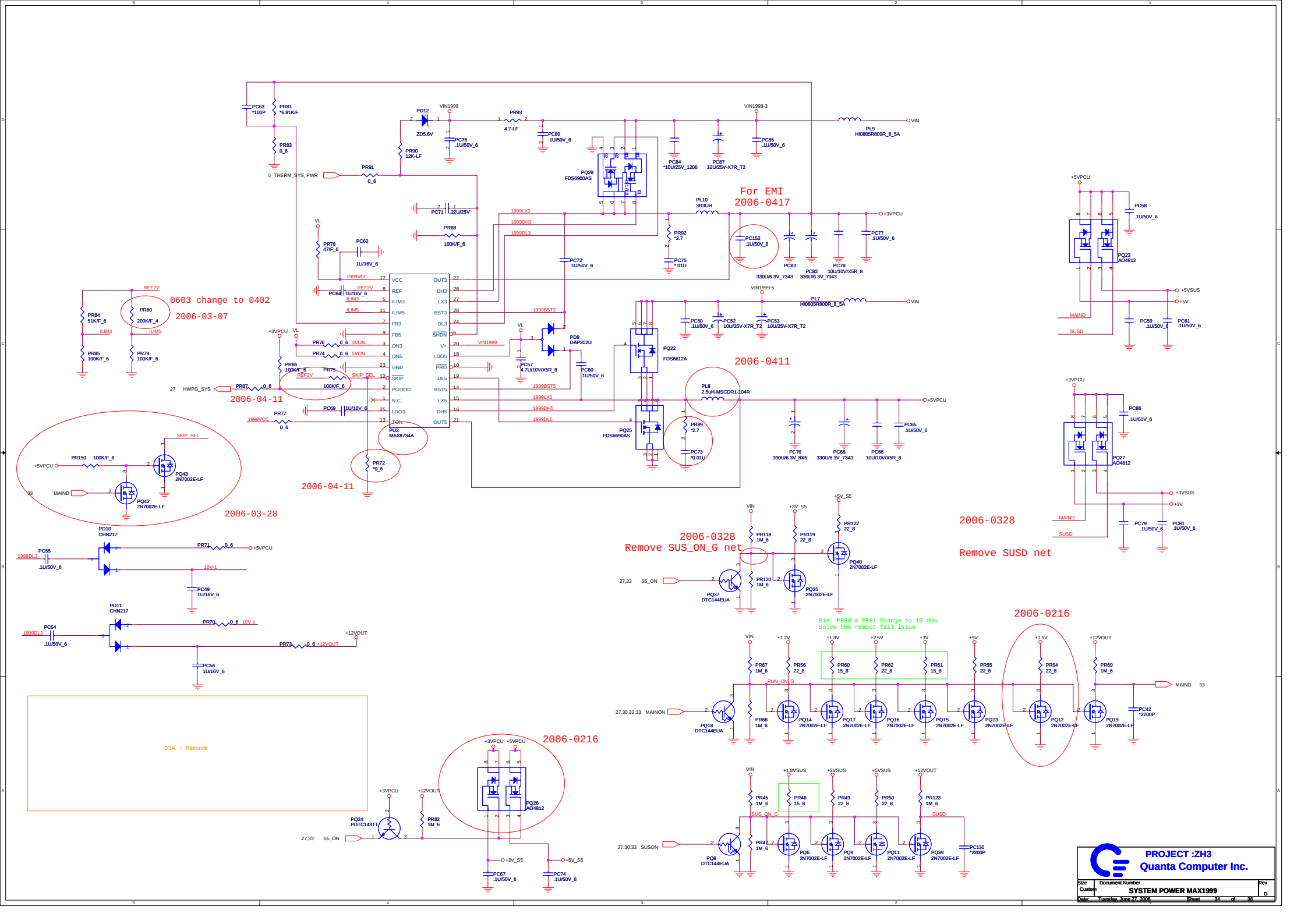
VOUT=(1+PR82/PR81)*1.5

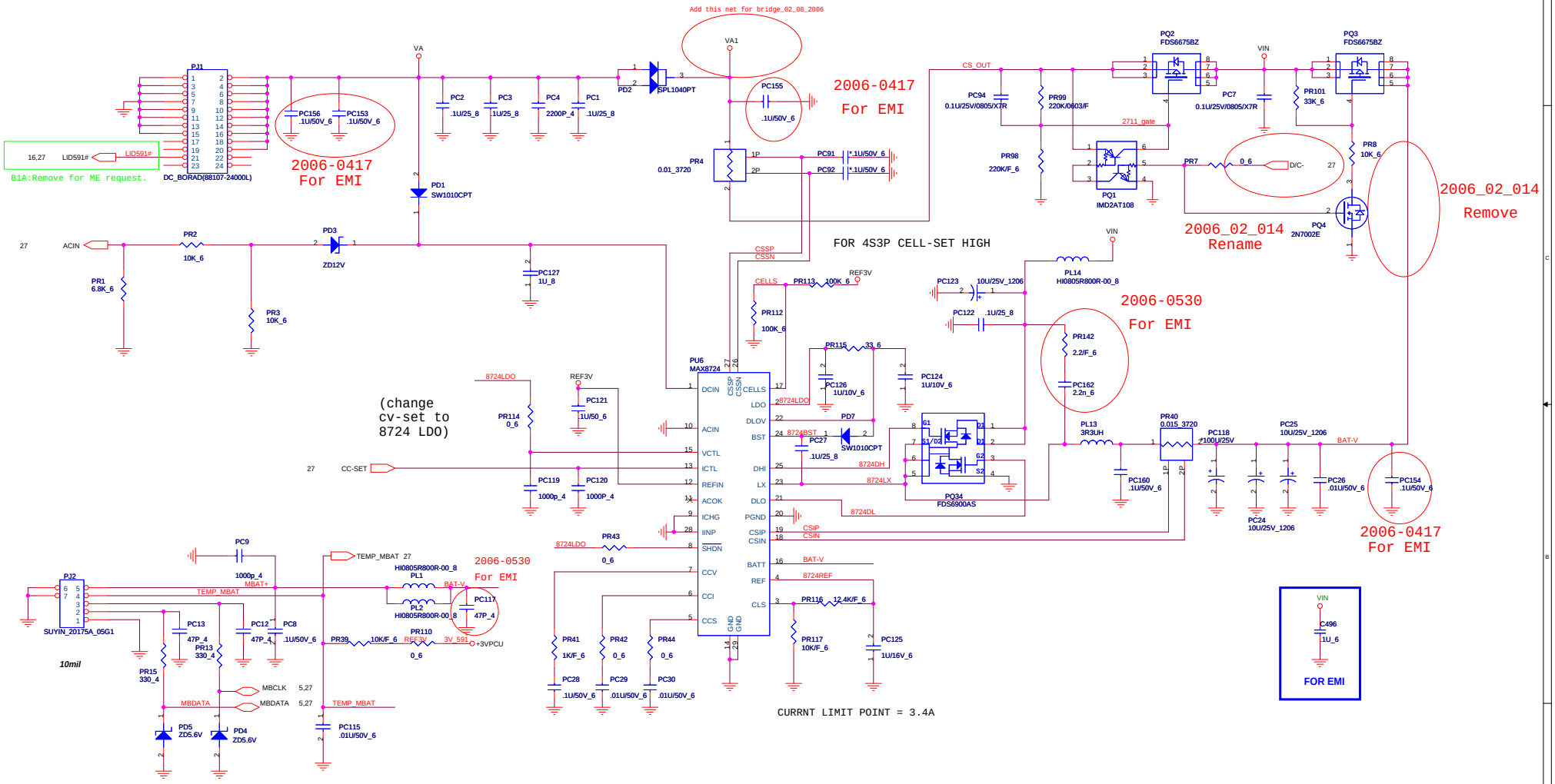


Vout =1.25(1+R1/R2)
= 1.25 (1+44K/100K)
= 1.8V

PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.8V&DDR	D
Date: Tuesday, June 27, 2006	Sheet 33 of 36	


For EMI
2006-0417
2006-0411
2006-04-11
2006-04-11
0603 change to 0402
2006-03-07
2006-03-28
2006-0328
Remove SUS_ON_G net
2006-0328
Remove SUSD net
2006-0216
2006-0216
B1A: PR60 & PR61 Change to 15 Ohm
Solve the reboot fail issue
D3A : Remove
PU3
MAX8734A
PROJECT :ZH3
Quanta Computer Inc.
SYSTEM POWER MAX1999
Size: Custom
Document Number
Rev: D
Date: Tuesday, June 27, 2006
Sheet 34 of 36


Add this net for bridge_02_08_2006
2006-0417
For EMI
2006-0417
For EMI
B1A:Remove for ME request.
DC_BORAD(88107-24000L)
FOR 4S3P CELL-SET HIGH
2006_02_014
Rename
2006_02_014
Remove
2006-0530
For EMI
(change
cv-set to
8724 LDO)
2006-0530
For EMI
2006-0417
For EMI
CURRNT LIMIT POINT = 3.4A
FOR EMI
10mil
PROJECT :ZH3
Quanta Computer Inc.
BATTERY CHARGER
Tuesday, June 27, 2006
Sheet 35 of 36

Change list

Item	Fixed Issue	Modify List	Schematic Rev.	PG#
1	New card issue.	NC_EN# connect the PIN4 & PIN17 of CN2 and PIN11 & PIN12 of CN14	B	13,31
2	New card issue.	Change from USB8 to USB5 for new card,	B	13,31
3	Lan issue.	Signal change from INTF to INTG	B	12,17
4	INT MIC issue.	CN8.2 change from MIC2_INT to MIC_GND	B	25
5	Wireless LED issue.	SW2.1 change from GND to wireless_sw#, SW2.2 change from wireless_sw# to GND.PIN3,4 is float	B	28
6	DVI issue	Q40.1 change from PHL_DATA to DDC_DATA	B	29,30
7	RAMP test			
8				
9				
10				
1				
2				
3				
4				
5				
6				
7				
8				
1				
2				
3				

PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	BATTERY CHARGER	D

Date: Tuesday, June 27, 2006 Sheet 36 of 36