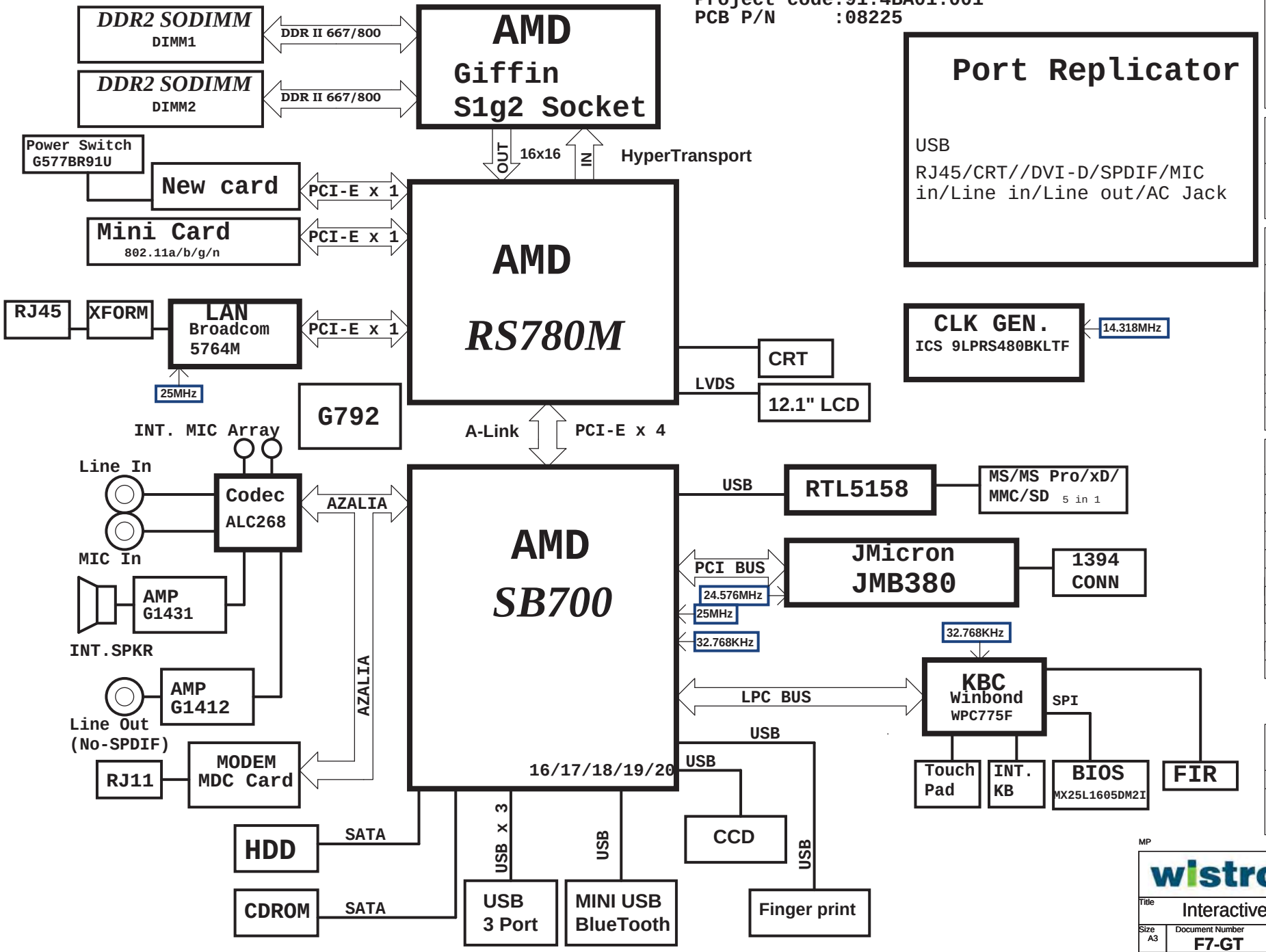
Ferrari 7 GT Block Diagram

2008/10/01

Project code:91.4BA01.001
PCB P/N :08225



PCB Layer Stackup

- L1: Component
- L2: GND
- L3: Signal
- L4: VCC
- L5: GND
- L6: Signal
- L7: GND
- L8: Component

CPU V_CORE — ISL6265HR — 37

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC — TPS51124 — 38

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D1V_S0

TPS51120 — 40

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

TPS51117 — 39

INPUT	OUTPUT
DCBATOUT	1D8V_S3

SYSTEM LDO — G2997 — 41

INPUT	OUTPUT
1D8V_S3	0D9V_S3

G9161

INPUT	OUTPUT
3D3V_S5	1D2V_S5

G9166

INPUT	OUTPUT
3D3V_S0	2D5V_S0

G957

INPUT	OUTPUT
3D3V_S0	1D5V_S0

Battery Charger — MAX8371 — 43

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

MP

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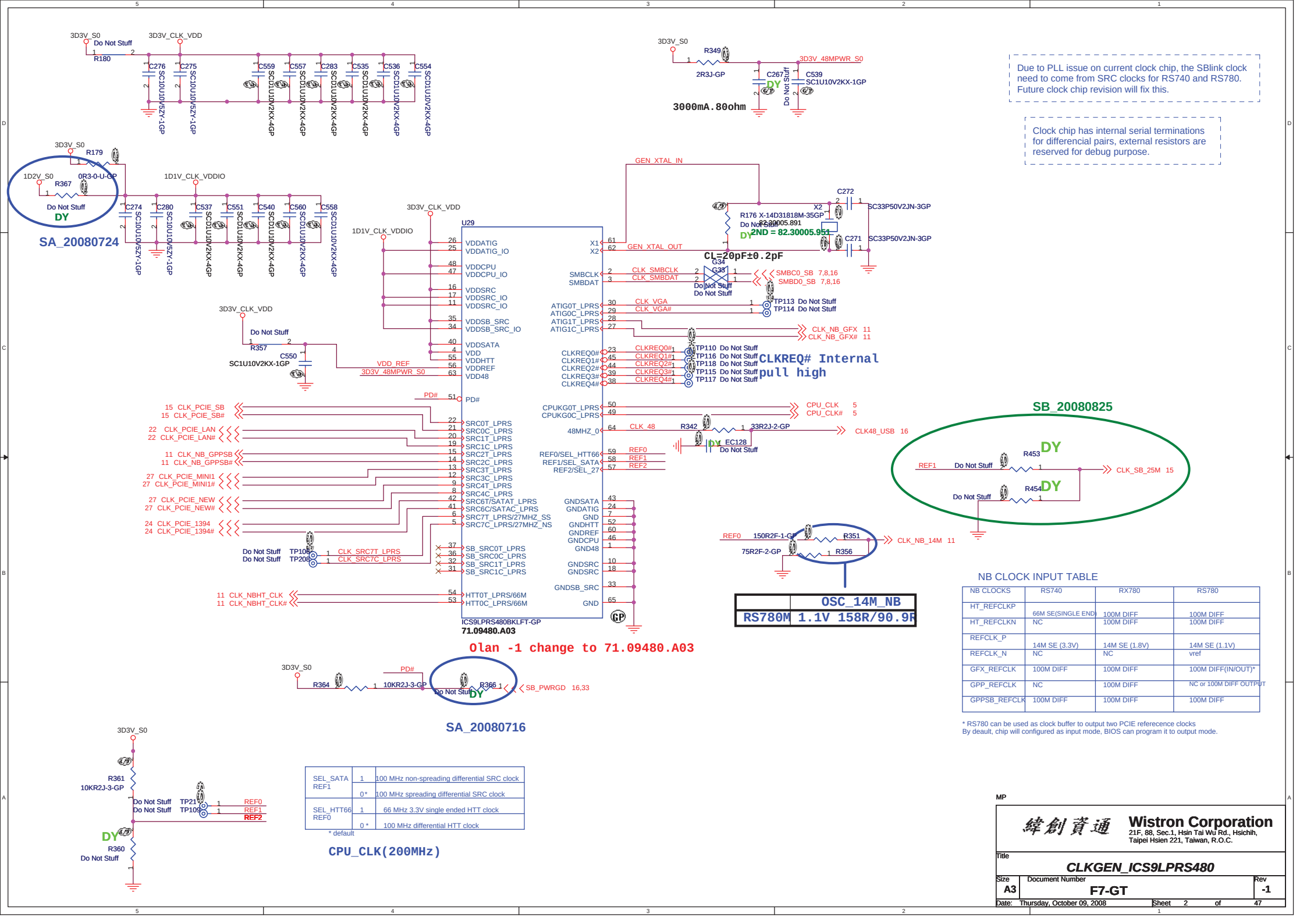
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Interactive Circuit Map

Size: A3 | Document Number: F7-GT | Rev: -1

Date: Wednesday, October 01, 2008 | Sheet 1 of 47


3D3V_S0
Do Not Stuff
R180
3D3V_CLK_VDD
C276 SC10U10V5ZY-1GP
C275 SC10U10V5ZY-1GP
C559 SC1U10V2KX-4GP
C557 SC1U10V2KX-4GP
C283 SC1U10V2KX-4GP
C535 SC1U10V2KX-4GP
C536 SC1U10V2KX-4GP
C554 SC1U10V2KX-4GP
3D3V_S0
R349
2R3J-GP
3D3V_48MPWR_S0
C267 DY
C539 SC1U10V2KX-1GP
3000mA.80ohm
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.
3D3V_S0
R179
1D2V_S0
0R3-0-U-GP
R367
Do Not Stuff
DY
SA_20080724
1D1V_CLK_VDDIO
C274 SC10U10V5ZY-1GP
C280 SC10U10V5ZY-1GP
C537 SC1U10V2KX-4GP
C551 SC1U10V2KX-4GP
C540 SC1U10V2KX-4GP
C560 SC1U10V2KX-4GP
C558 SC1U10V2KX-4GP
GEN_XTAL_IN
C272 SC33P50V2JN-3GP
X2
R176 X-14D31818M-35GP
82.30005.891
2ND = 82.30005.951
C271 SC33P50V2JN-3GP
CL=20pF±0.2pF
GEN_XTAL_OUT
3D3V_CLK_VDD
U29
VDDATIG
VDDATIG_IO
VDDCPU
VDDCPU_IO
VDDSRC
VDDSRC_IO
VDDSRC_IO
VDDSB_SRC
VDDSB_SRC_IO
VDDSATA
VDD
VDDHTT
VDDREF
VDD48
X1
X2
SMBCLK
SMBDAT
CLK_SMBCLK
CLK_SMBDAT
G34
G33
SMBC0_SB 7,8,16
SMBD0_SB 7,8,16
ATIG0T_LPRS
ATIG0C_LPRS
ATIG1T_LPRS
ATIG1C_LPRS
CLK_VGA
CLK_VGA#
TP113 Do Not Stuff
TP114 Do Not Stuff
CLK_NB_GFX 11
CLK_NB_GFX# 11
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
TP110 Do Not Stuff
TP116 Do Not Stuff
TP118 Do Not Stuff
TP115 Do Not Stuff
TP117 Do Not Stuff
CLKREQ# Internal pull high
3D3V_CLK_VDD
Do Not Stuff
R357
C550 SC1U10V2KX-1GP
VDD_REF
3D3V_48MPWR_S0
PD#
SRC0T_LPRS
SRC0C_LPRS
SRC1T_LPRS
SRC1C_LPRS
SRC2T_LPRS
SRC2C_LPRS
SRC3T_LPRS
SRC3C_LPRS
SRC4T_LPRS
SRC4C_LPRS
SRC6T/SATAT_LPRS
SRC6C/SATAC_LPRS
SRC7T_LPRS/27MHZ_SS
SRC7C_LPRS/27MHZ_NS
CPUKG0T_LPRS
CPUKG0C_LPRS
CPU_CLK 5
CPU_CLK# 5
48MHZ_0
CLK_48
R342
33R2J-2-GP
CLK48_USB 16
EC128
Do Not Stuff
REF0/SEL_HTT66
REF1/SEL_SATA
REF2/SEL_27
REF0
REF1
REF2
GNDSATA
GNDATIG
GND
GNDHTT
GNDREF
GNDCPU
GND48
GNDSRC
GNDSRC
GNDSB_SRC
GND
HTT0T_LPRS/66M
HTT0C_LPRS/66M
SB_SRC0T_LPRS
SB_SRC0C_LPRS
SB_SRC1T_LPRS
SB_SRC1C_LPRS
CLK_SRC7T_LPRS
CLK_SRC7C_LPRS
TP108 Do Not Stuff
TP208 Do Not Stuff
CLK_PCIE_SB
CLK_PCIE_SB#
CLK_PCIE_LAN
CLK_PCIE_LAN#
CLK_NB_GPPSB
CLK_NB_GPPSB#
CLK_PCIE_MINI1
CLK_PCIE_MINI1#
CLK_PCIE_NEW
CLK_PCIE_NEW#
CLK_PCIE_1394
CLK_PCIE_1394#
CLK_NBHT_CLK
CLK_NBHT_CLK#
ICS9LPRS480BKLFT-GP
71.09480.A03
Olan -1 change to 71.09480.A03
SB_20080825
DY
R453
R454
REF1
Do Not Stuff
CLK_SB_25M 15
REF0
150R2F-1-GP
75R2F-2-GP
R351
R356
CLK_NB_14M 11
OSC_14M_NB
RS780M 1.1V 158R/90.9F
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
3D3V_S0
R364
10KR2J-3-GP
PD#
R366
Do Not Stuff
DY
SB_PWRGD 16,33
SA_20080716
3D3V_S0
R361
10KR2J-3-GP
Do Not Stuff
Do Not Stuff
TP21
TP109
REF0
REF1
REF2
DY
R360
Do Not Stuff
SEL_SATA REF1
1 100 MHz non-spreading differential SRC clock
0* 100 MHz spreading differential SRC clock
SEL_HTT66 REF0
1 66 MHz 3.3V single ended HTT clock
0* 100 MHz differential HTT clock
* default
CPU_CLK(200MHz)
MP
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CLKGEN_ICS9LPRS480
Size A3
Document Number F7-GT
Rev -1
Date: Thursday, October 09, 2008
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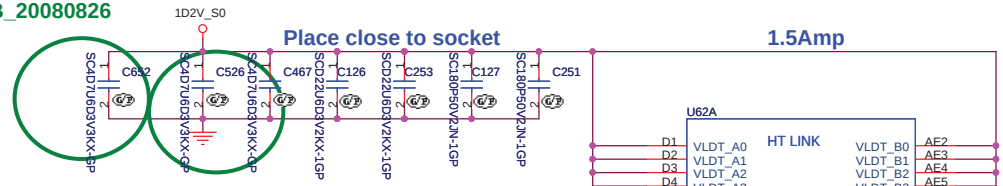
SB_20080826



SA_20080723

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

U62A

HT LINK

D1	VLDT_A0	VLDT_B0	AE2
D2	VLDT_A1	VLDT_B1	AE3
D3	VLDT_A2	VLDT_B2	AE4
D4	VLDT_A3	VLDT_B3	AE5

10 HT_NB_CPU_CAD_H0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	HT_CPU_NB_CAD_H0 10
10 HT_NB_CPU_CAD_L0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	HT_CPU_NB_CAD_L0 10
10 HT_NB_CPU_CAD_H1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	HT_CPU_NB_CAD_H1 10
10 HT_NB_CPU_CAD_L1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	HT_CPU_NB_CAD_L1 10
10 HT_NB_CPU_CAD_H2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	HT_CPU_NB_CAD_H2 10
10 HT_NB_CPU_CAD_L2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	HT_CPU_NB_CAD_L2 10
10 HT_NB_CPU_CAD_H3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	HT_CPU_NB_CAD_H3 10
10 HT_NB_CPU_CAD_L3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	HT_CPU_NB_CAD_L3 10
10 HT_NB_CPU_CAD_H4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	HT_CPU_NB_CAD_H4 10
10 HT_NB_CPU_CAD_L4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	HT_CPU_NB_CAD_L4 10
10 HT_NB_CPU_CAD_H5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	HT_CPU_NB_CAD_H5 10
10 HT_NB_CPU_CAD_L5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	HT_CPU_NB_CAD_L5 10
10 HT_NB_CPU_CAD_H6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	HT_CPU_NB_CAD_H6 10
10 HT_NB_CPU_CAD_L6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	HT_CPU_NB_CAD_L6 10
10 HT_NB_CPU_CAD_H7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	HT_CPU_NB_CAD_H7 10
10 HT_NB_CPU_CAD_L7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	HT_CPU_NB_CAD_L7 10
10 HT_NB_CPU_CAD_H8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	HT_CPU_NB_CAD_H8 10
10 HT_NB_CPU_CAD_L8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	HT_CPU_NB_CAD_L8 10
10 HT_NB_CPU_CAD_H9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	HT_CPU_NB_CAD_H9 10
10 HT_NB_CPU_CAD_L9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	HT_CPU_NB_CAD_L9 10
10 HT_NB_CPU_CAD_H10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	HT_CPU_NB_CAD_H10 10
10 HT_NB_CPU_CAD_L10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	HT_CPU_NB_CAD_L10 10
10 HT_NB_CPU_CAD_H11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	HT_CPU_NB_CAD_H11 10
10 HT_NB_CPU_CAD_L11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	HT_CPU_NB_CAD_L11 10
10 HT_NB_CPU_CAD_H12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	HT_CPU_NB_CAD_H12 10
10 HT_NB_CPU_CAD_L12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	HT_CPU_NB_CAD_L12 10
10 HT_NB_CPU_CAD_H13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	HT_CPU_NB_CAD_H13 10
10 HT_NB_CPU_CAD_L13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	HT_CPU_NB_CAD_L13 10
10 HT_NB_CPU_CAD_H14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	HT_CPU_NB_CAD_H14 10
10 HT_NB_CPU_CAD_L14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	HT_CPU_NB_CAD_L14 10
10 HT_NB_CPU_CAD_H15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	HT_CPU_NB_CAD_H15 10
10 HT_NB_CPU_CAD_L15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	HT_CPU_NB_CAD_L15 10
10 HT_NB_CPU_CLK_H0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	HT_CPU_NB_CLK_H0 10
10 HT_NB_CPU_CLK_L0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	HT_CPU_NB_CLK_L0 10
10 HT_NB_CPU_CLK_H1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	HT_CPU_NB_CLK_H1 10
10 HT_NB_CPU_CLK_L1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	HT_CPU_NB_CLK_L1 10
10 HT_NB_CPU_CTL_H0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	HT_CPU_NB_CTL_H0 10
10 HT_NB_CPU_CTL_L0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	HT_CPU_NB_CTL_L0 10
10 HT_NB_CPU_CTL_H1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	HT_CPU_NB_CTL_H1 10
10 HT_NB_CPU_CTL_L1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	HT_CPU_NB_CTL_L1 10

SKT-CPU638P-GP-U2

62.10055.111 2ND = 62.10055.251

SKT - BGA638H176

MP

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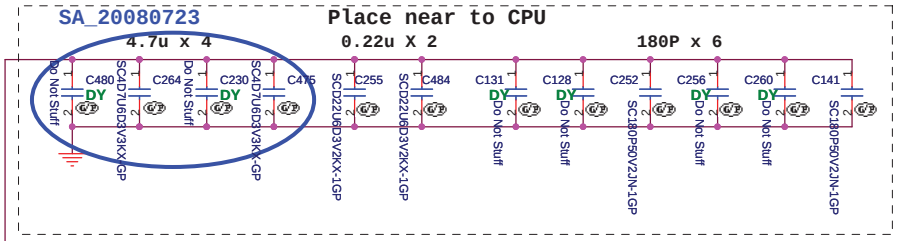
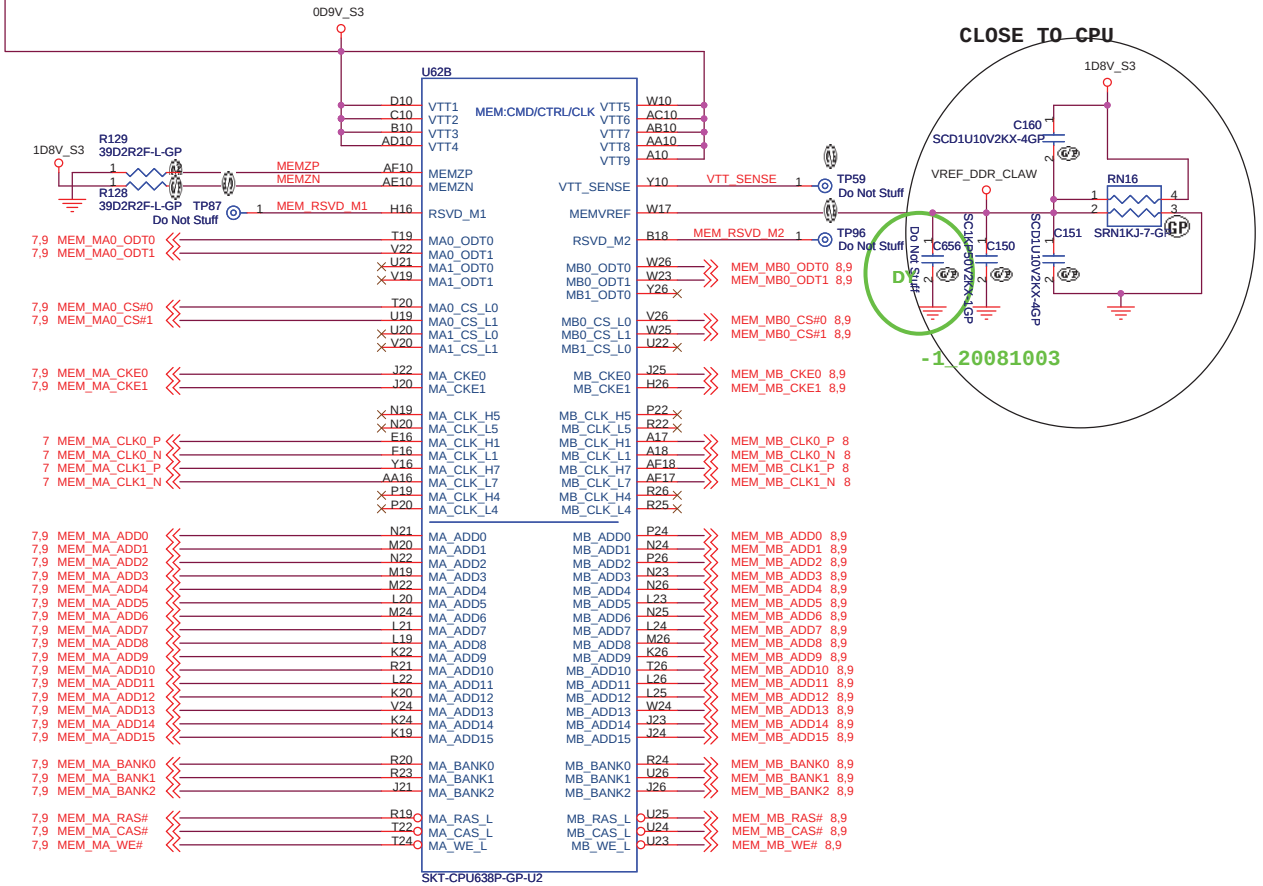
Taipei Hsien 221, Taiwan, R.O.C.

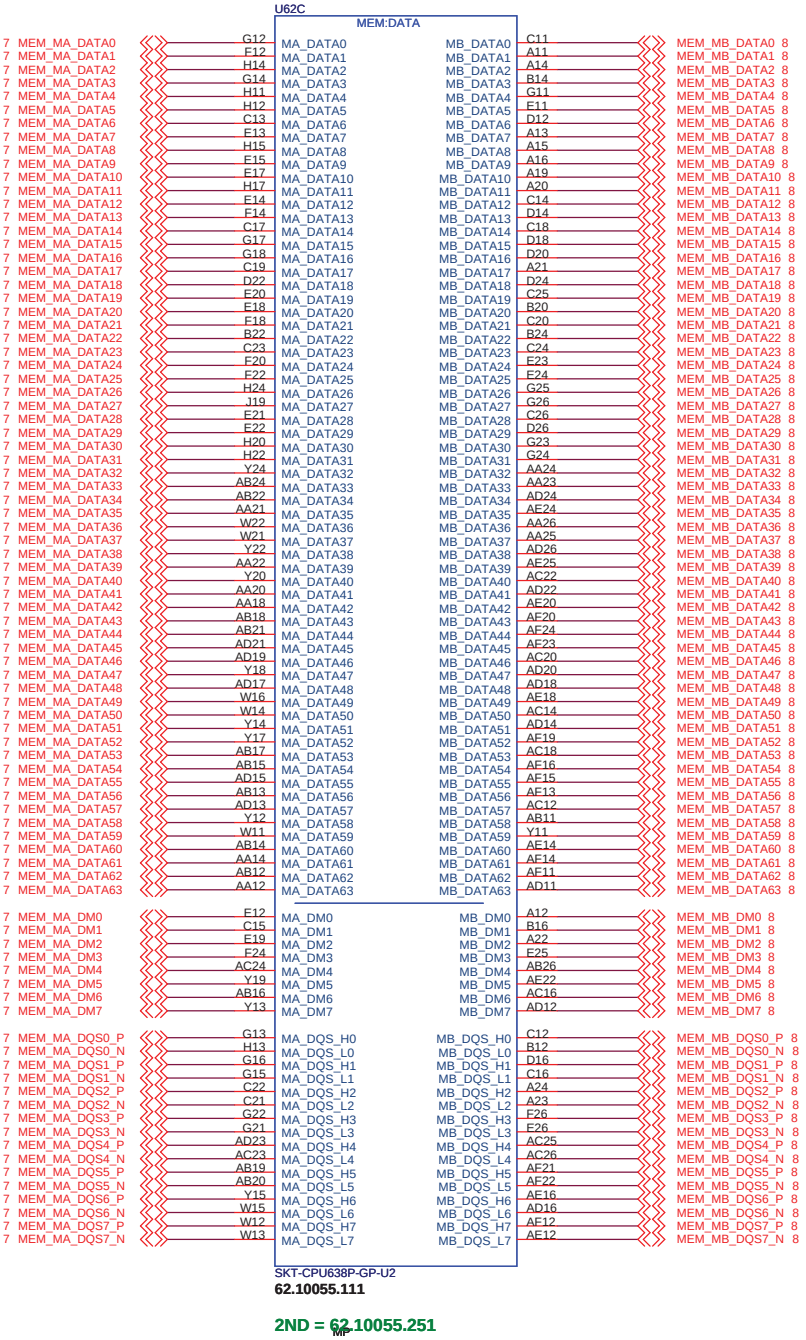
Title: CPU_HT_LINK I/F_(1/4)

Size	Document Number	Rev
A3	F7-GT	-1

Date: Thursday, October 09, 2008 Sheet 3 of 47







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Title: CPU_DDR_(2/4)

Size	Document Number	Rev
A3	F7-GT	-1

Date: Thursday, October 09, 2008 Sheet 4 of 47

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU

For HDT DBG

SA_20080721

internal pull high 300 ohm

20080723

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

Near CPU PIN

CPU exceeds to 125℃

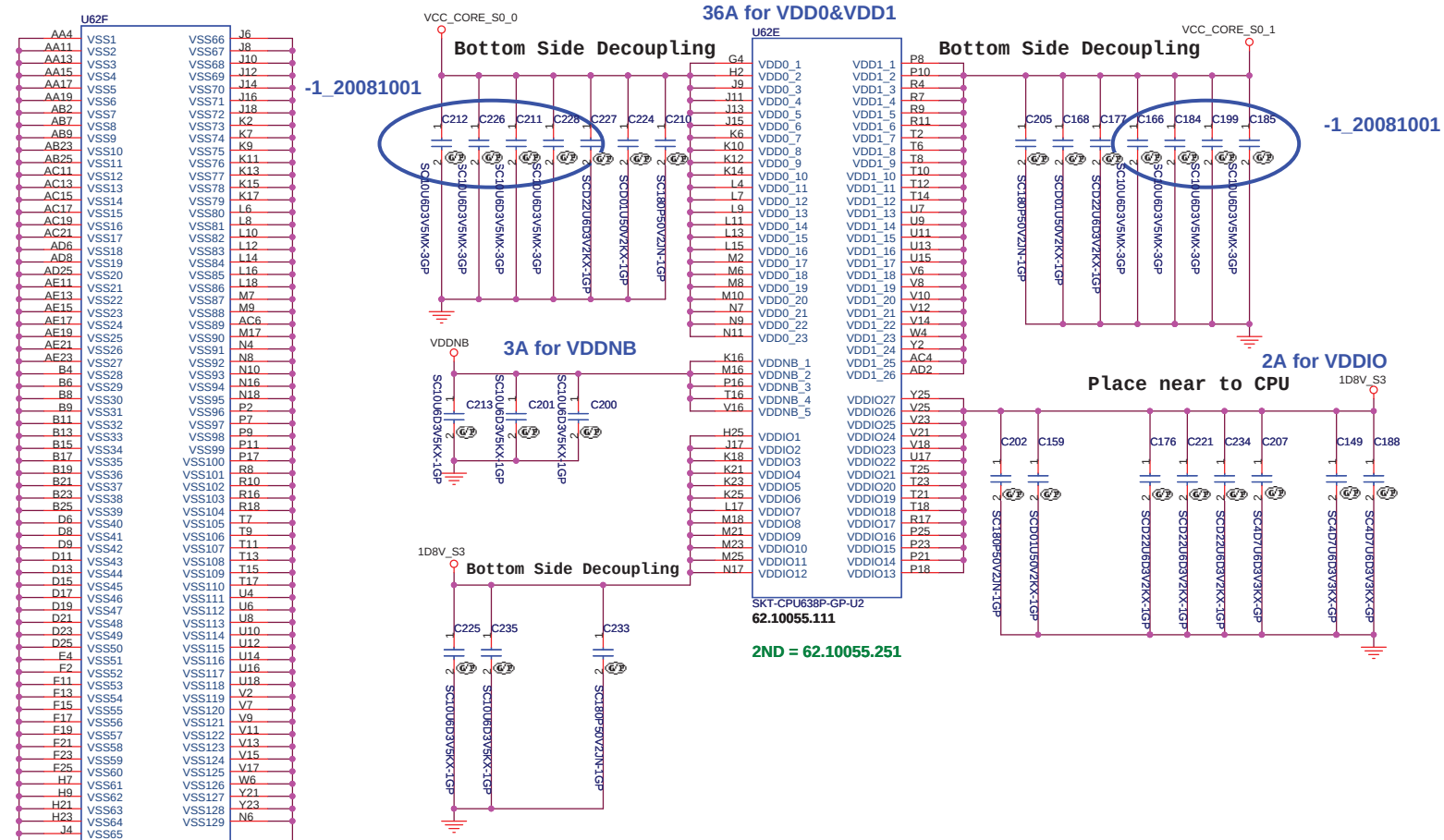
HDT Connectors

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)

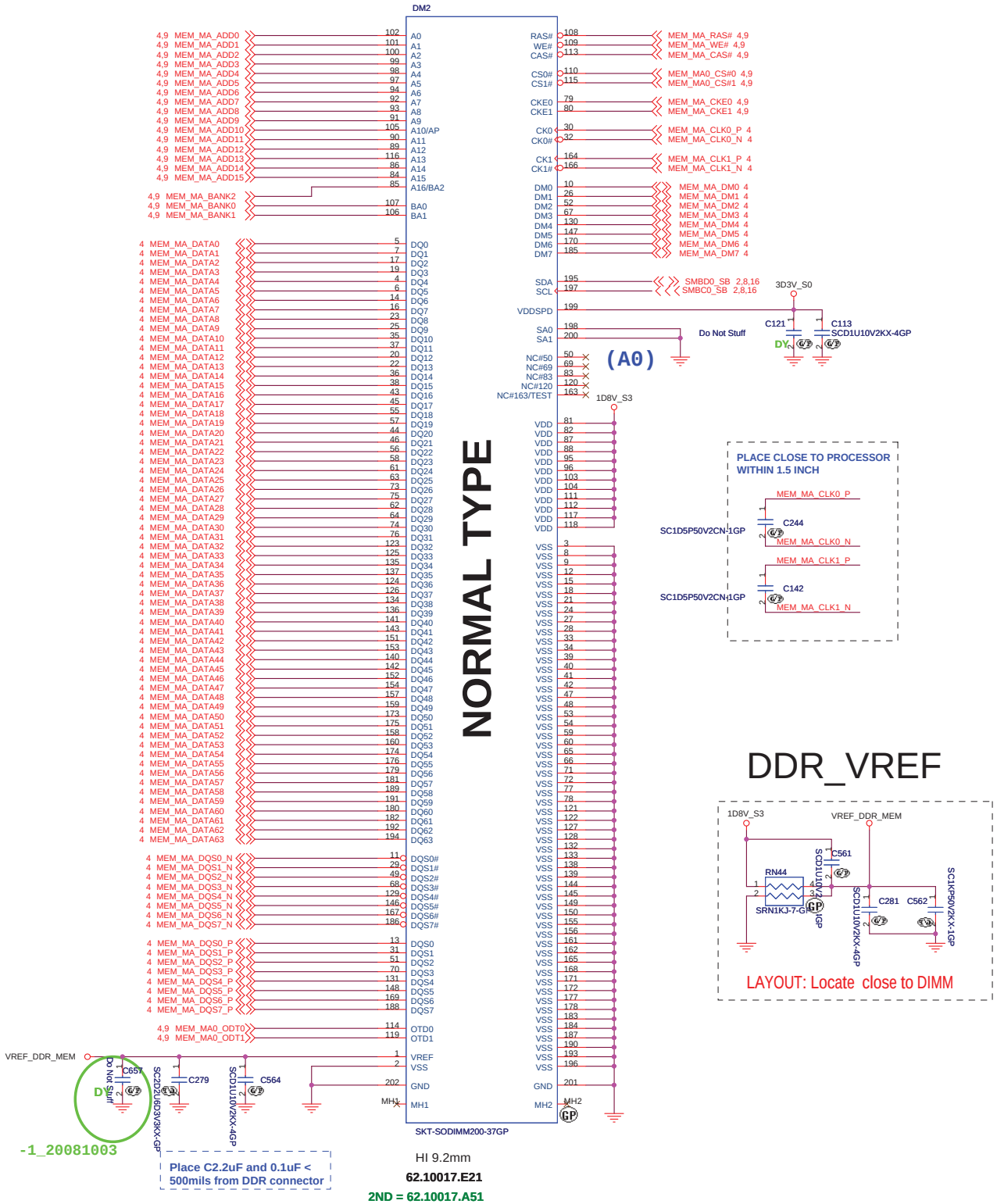
Size: A3 | Document Number: F7-GT | Rev: -1

Date: Thursday, October 09, 2008 | Sheet 5 of 47



MP

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU_Power_(4/4)***	
Size A3	Document Number **F7-GT**	Rev -1
Date: Wednesday, October 01, 2008	Sheet 6 of 47	



MP

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size	Document Number	Rev
Custom	F7-GT	-1

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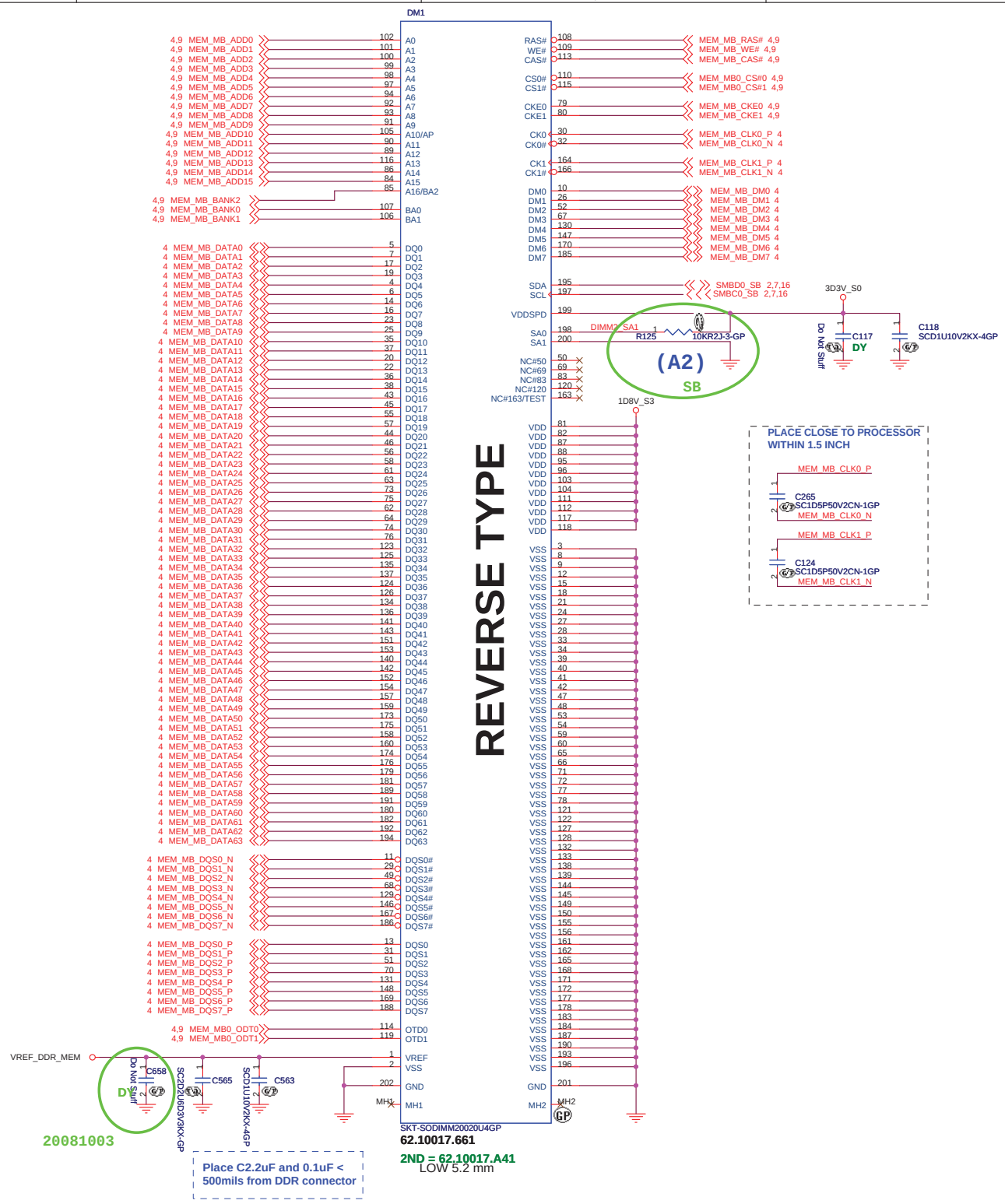

MP

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR_SO-DIMM SKT_2*

Size	Document Number	Rev
Custom	F7-GT	-1

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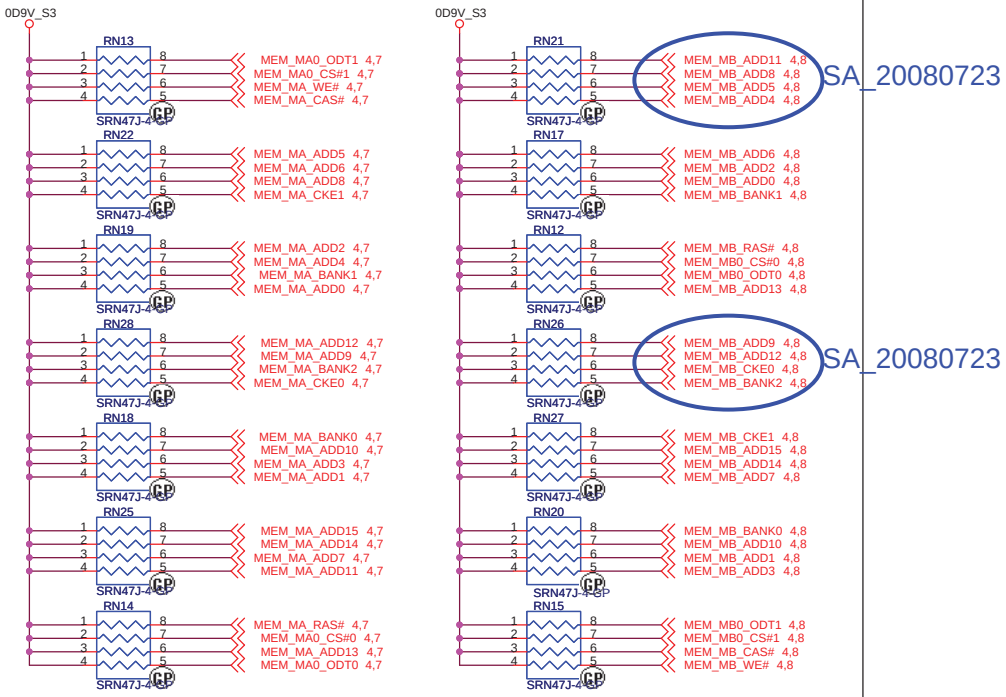
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



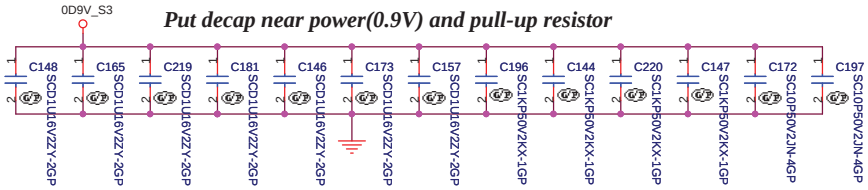
SA_20080723

SA_20080723

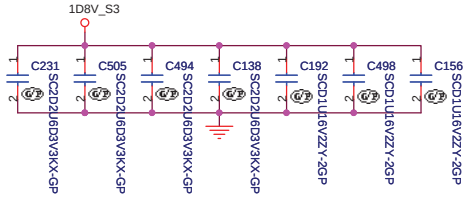
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

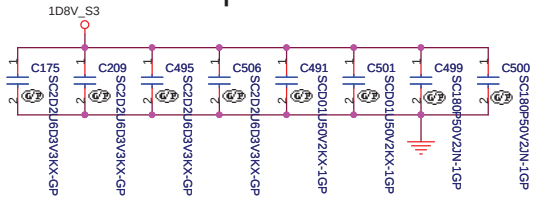


Place these Caps near DM1



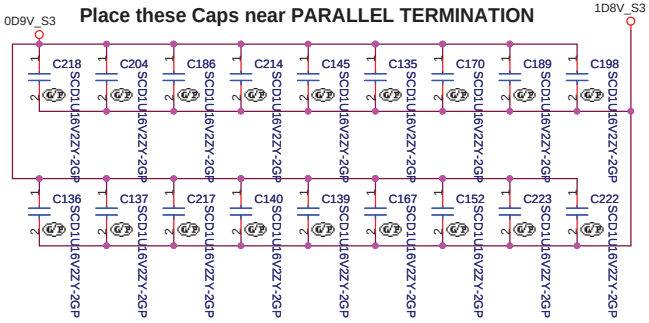
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



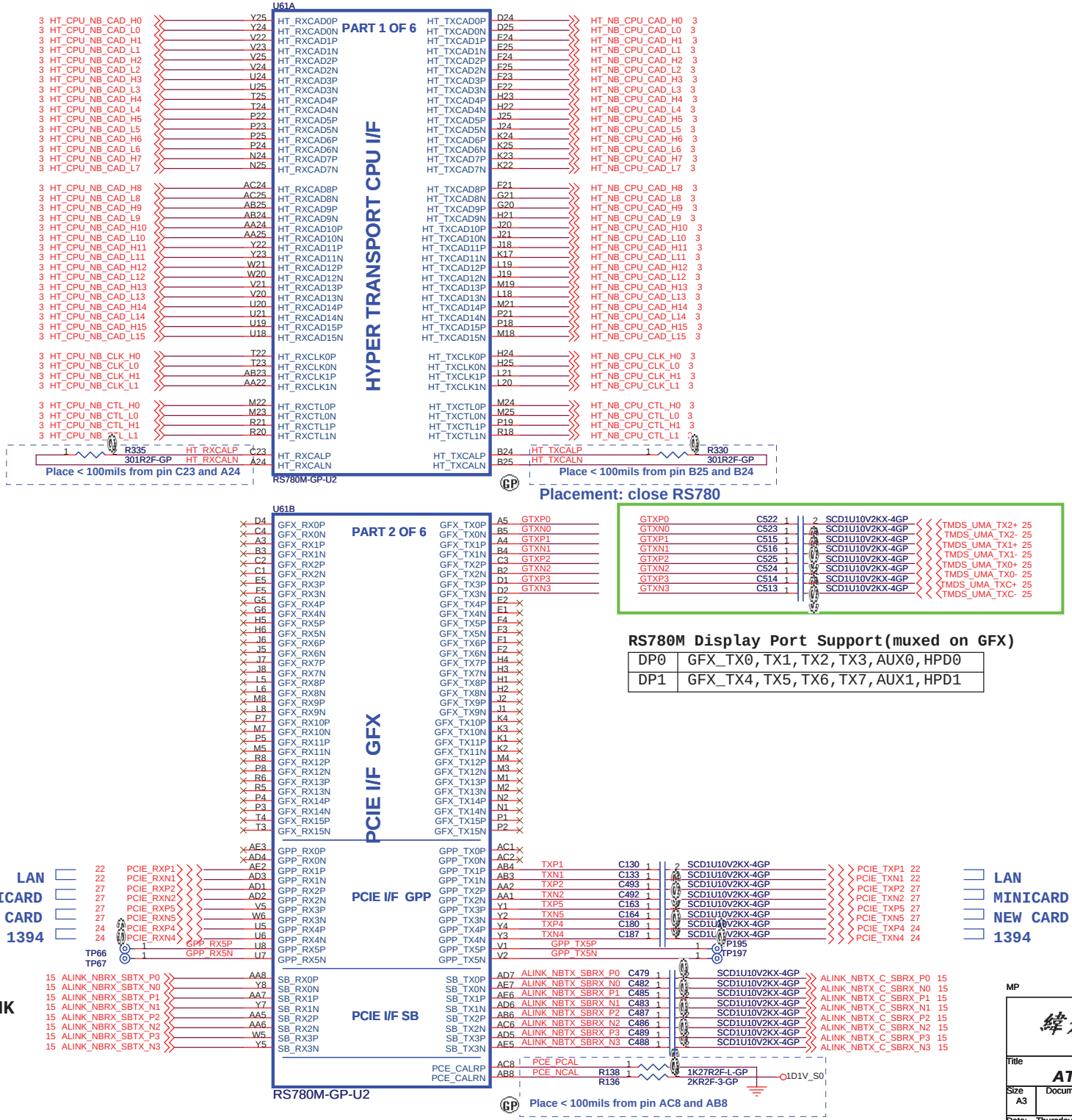
MP

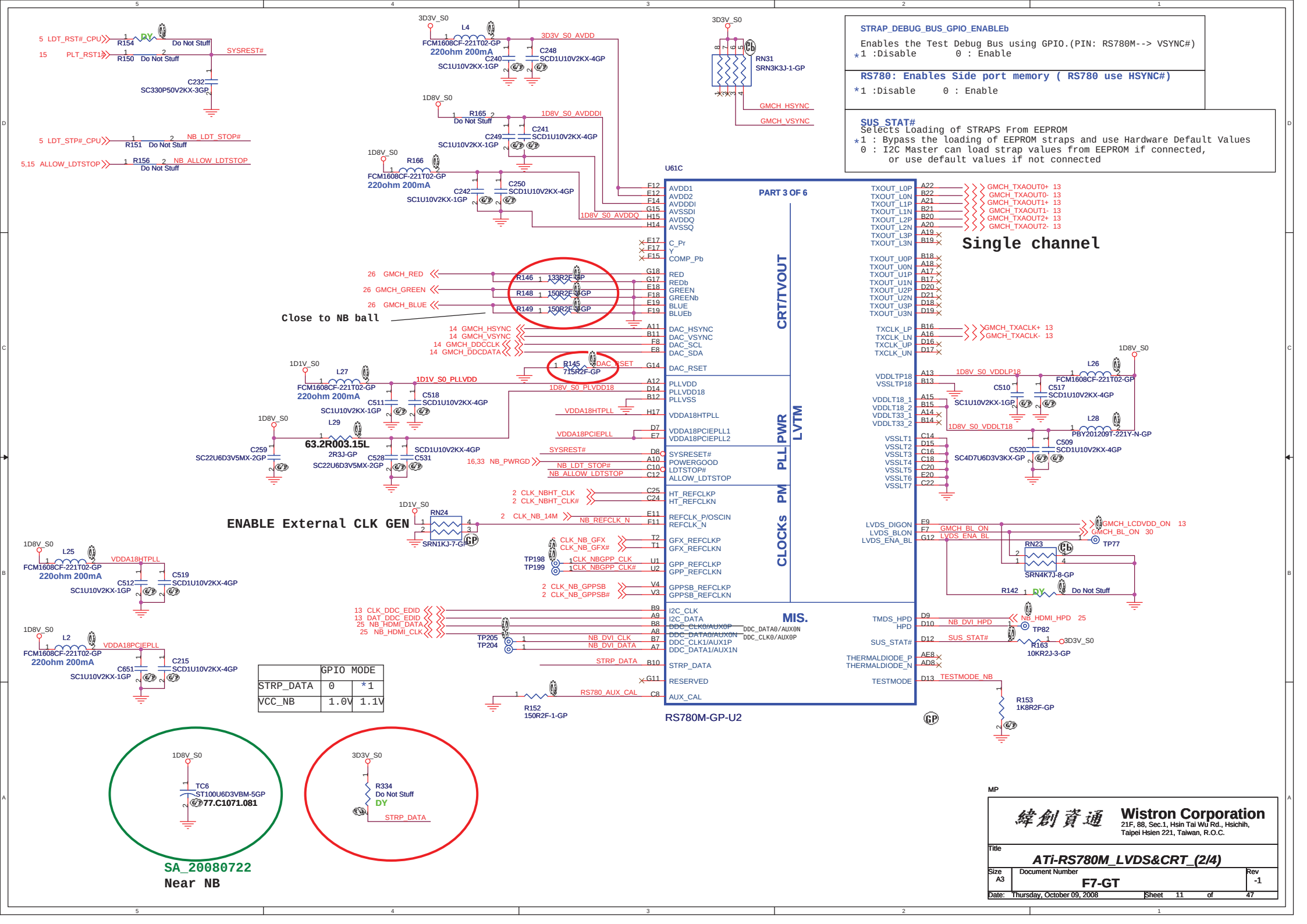
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

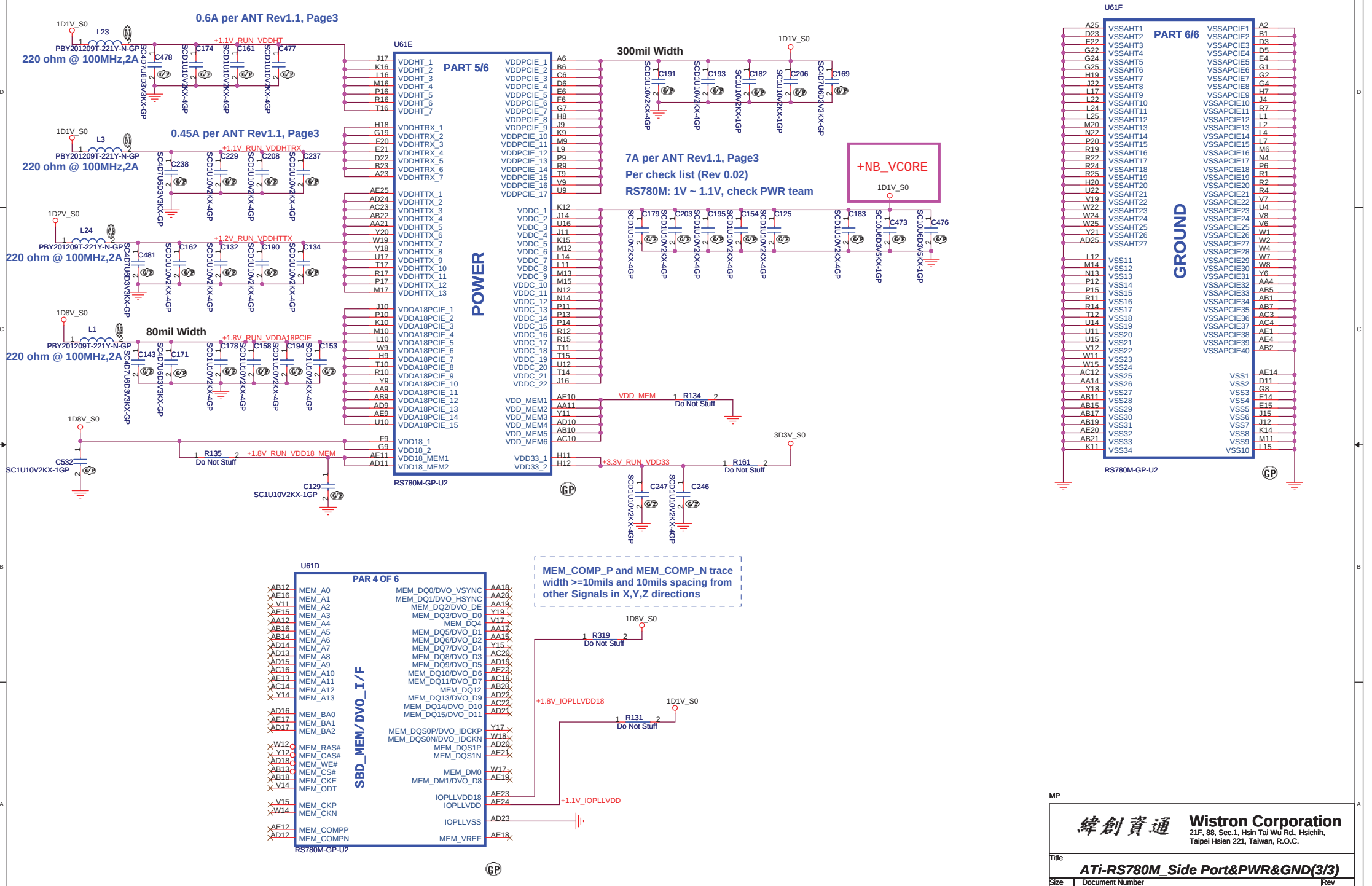
Title: ***DDR_DAMPING & TERMINATION***

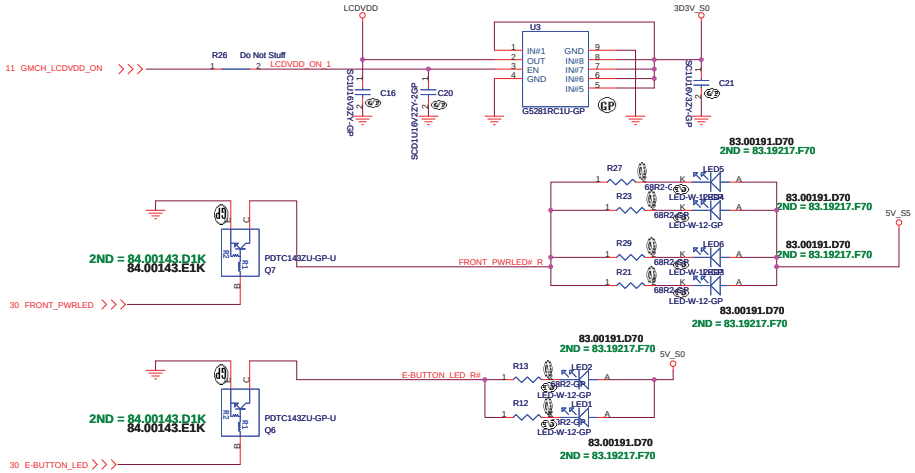
Size	Document Number	Rev
A3	F7-GT	-1

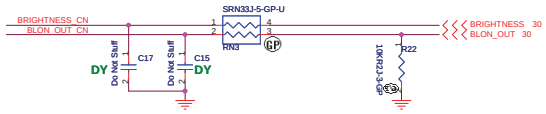
Date: Thursday, October 09, 2008 Sheet 9 of 47


U61A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
Placement: close RS780
U61B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
Place < 100mils from pin AC8 and AB8
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
LAN
MINICARD
NEW CARD
1394
A-LINK
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M_HT LINK&PCIe(1/3)
Size A3
Document Number F7-GT
Rev -1
Date: Thursday, October 09, 2008
Sheet 10 of 47


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
U61C
PART 3 OF 6
RS780M-GP-U2
CRT/TVOUT
LVTM
PLL PWR
CLOCKs PM
MIS.
Single channel
Close to NB ball
ENABLE External CLK GEN
SA_20080722
Near NB
GPIO MODE
STRP_DATA 0 *1
VCC_NB 1.0V 1.1V
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS780M_LVDS&CRT_(2/4)
F7-GT
Date: Thursday, October 09, 2008
Sheet 11 of 47

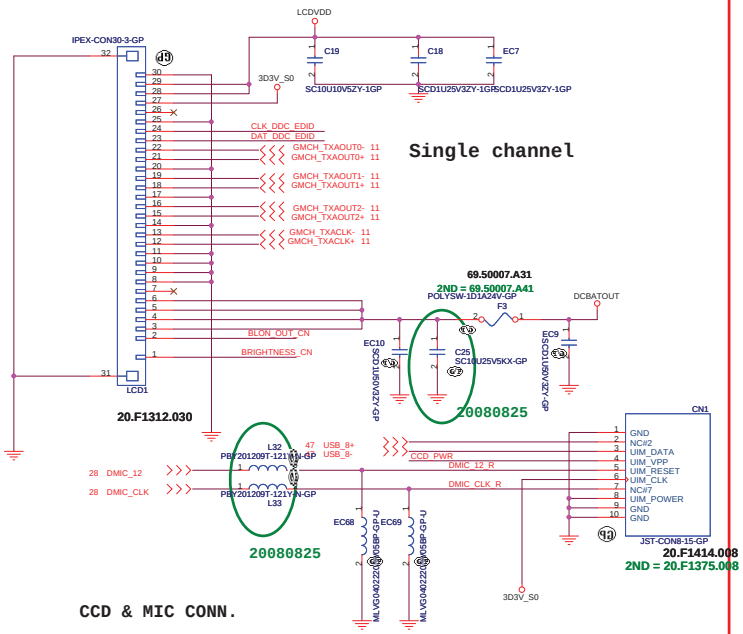

0.6A per ANT Rev1.1, Page3
0.45A per ANT Rev1.1, Page3
80mil Width
300mil Width
7A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
220 ohm @ 100MHz,2A
PART 5/6
POWER
PART 6/6
GROUND
PAR 4 OF 6
SBD_MEM/DVO_I/F
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
RS780M-GP-U2
Do Not Stuff
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS780M_Side Port&PWR&GND(3/3)
F7-GT
Wednesday, October 01, 2008

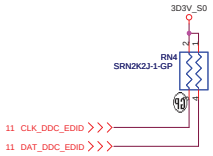


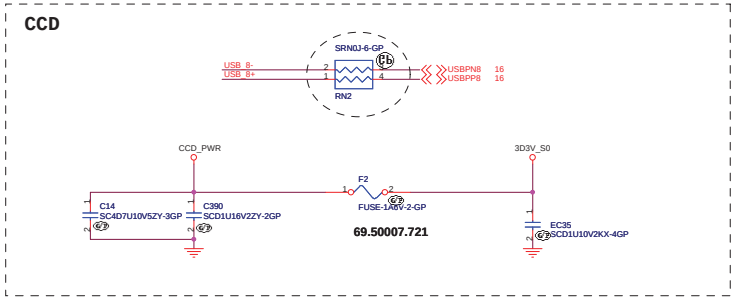


SA_20080731 change connect

LCD CONN

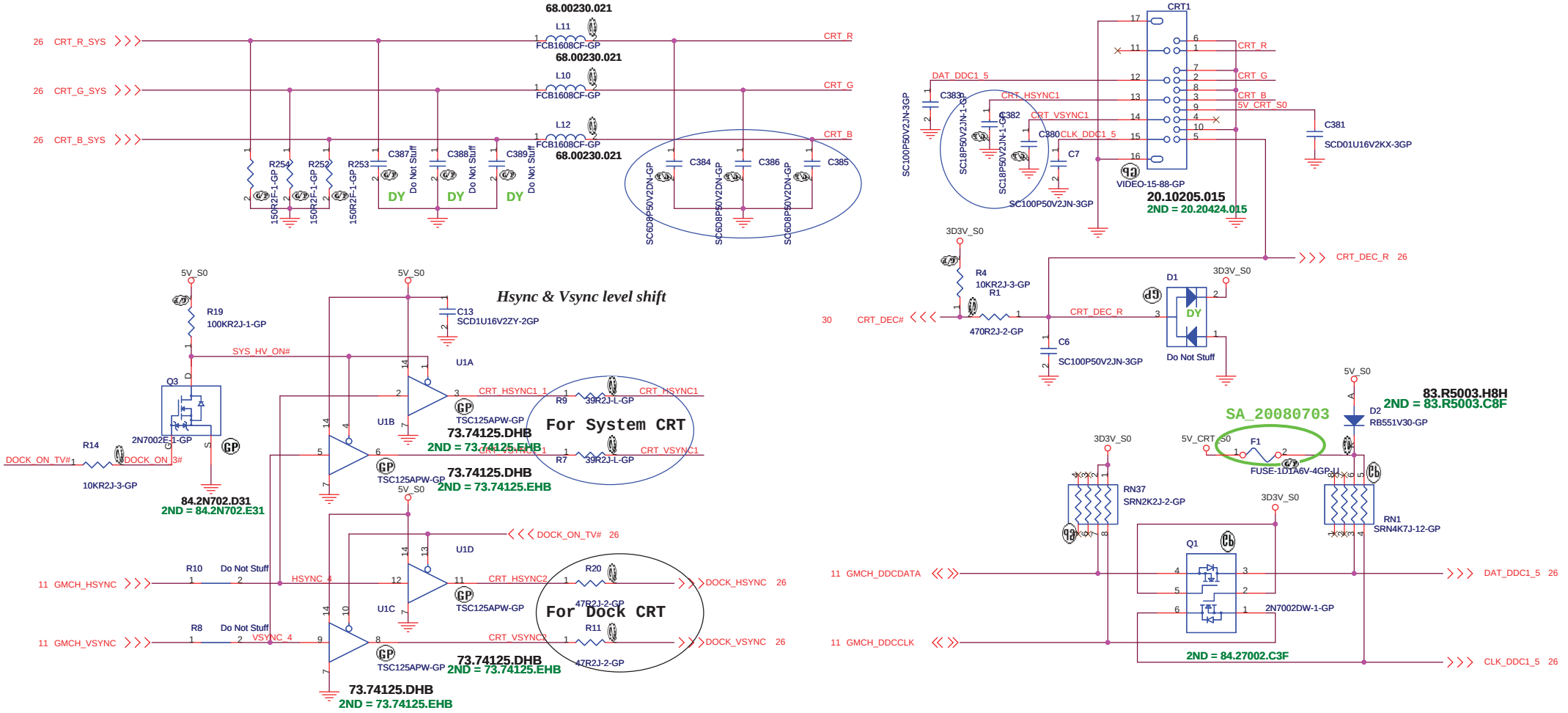




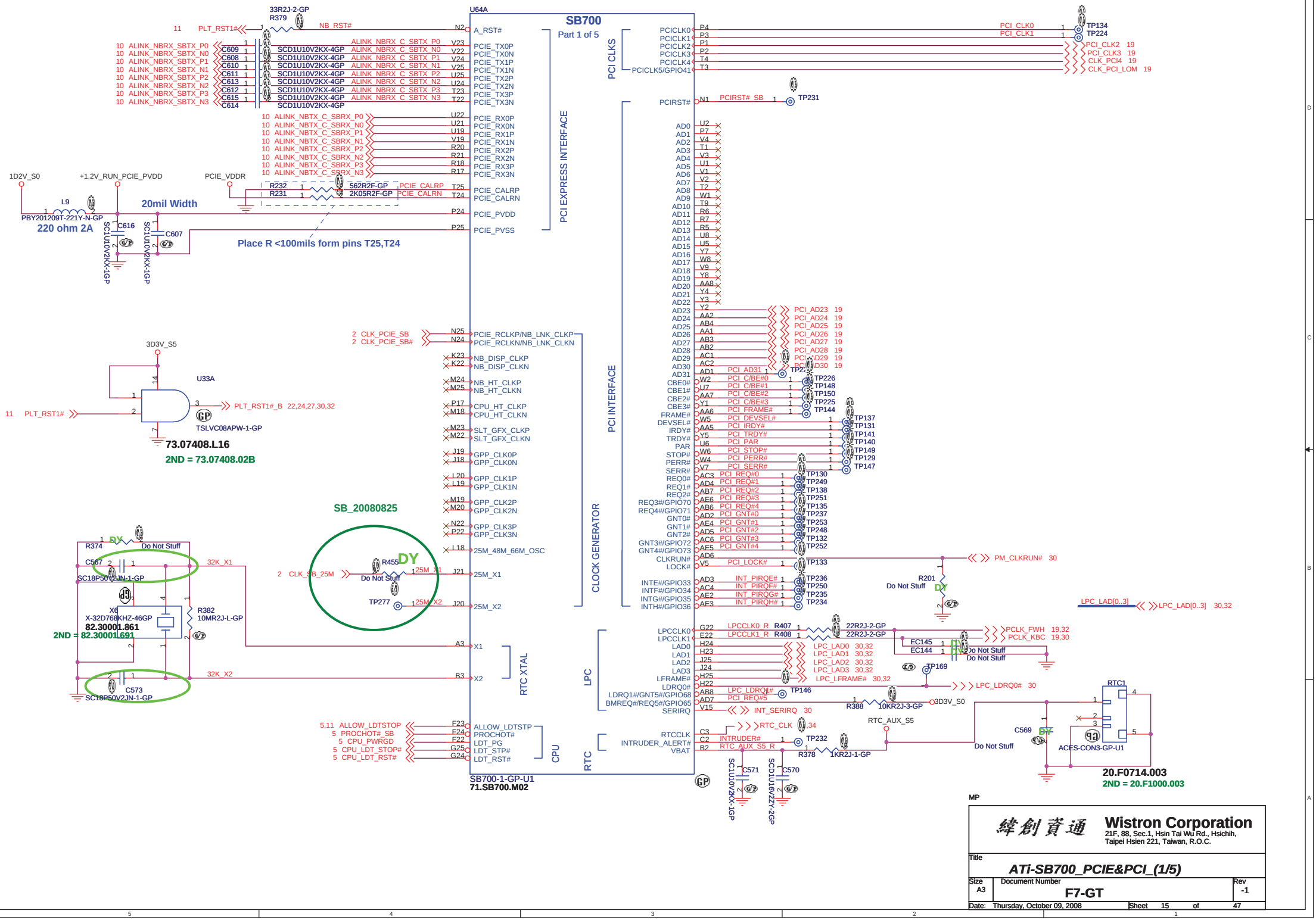


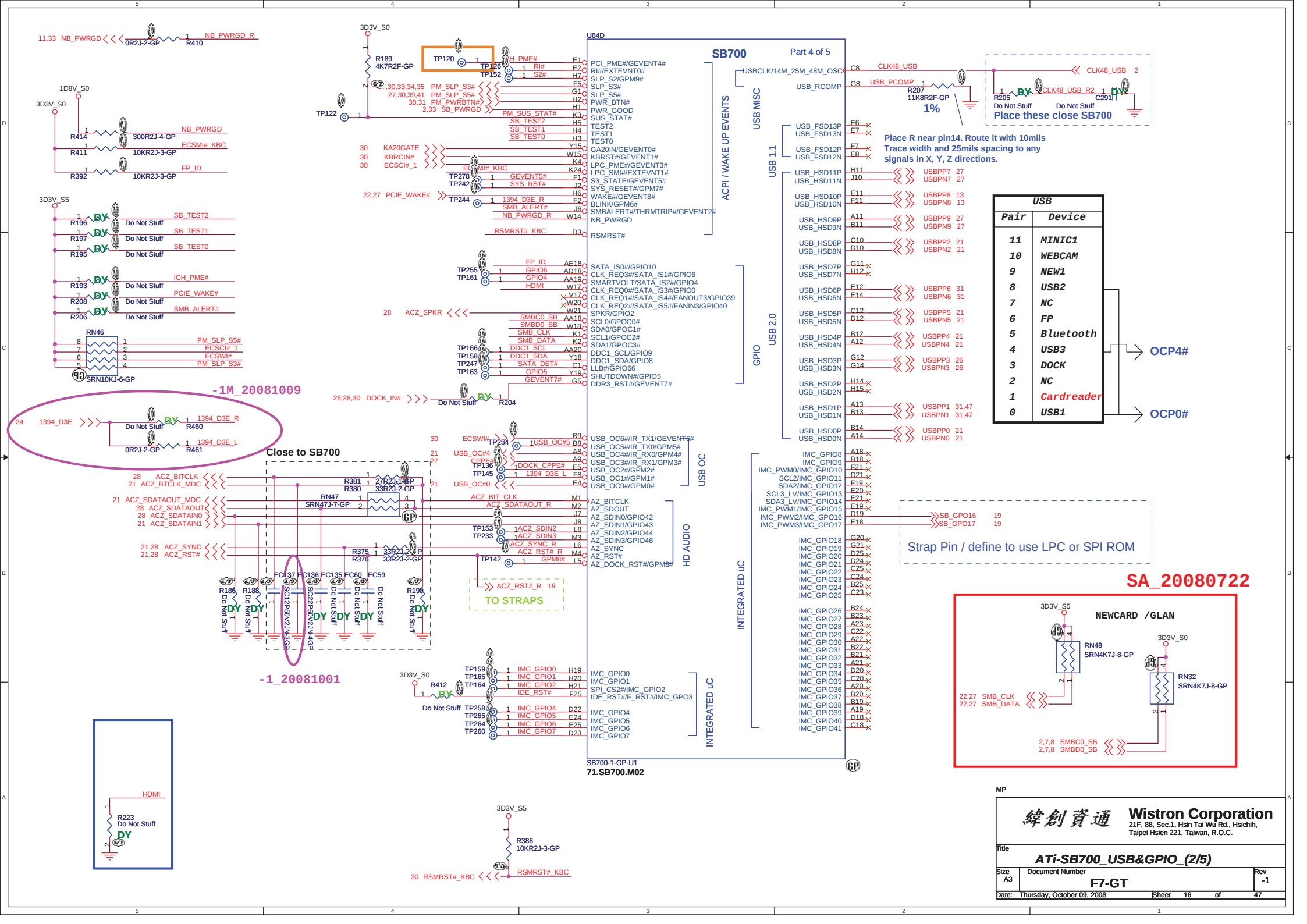
MP

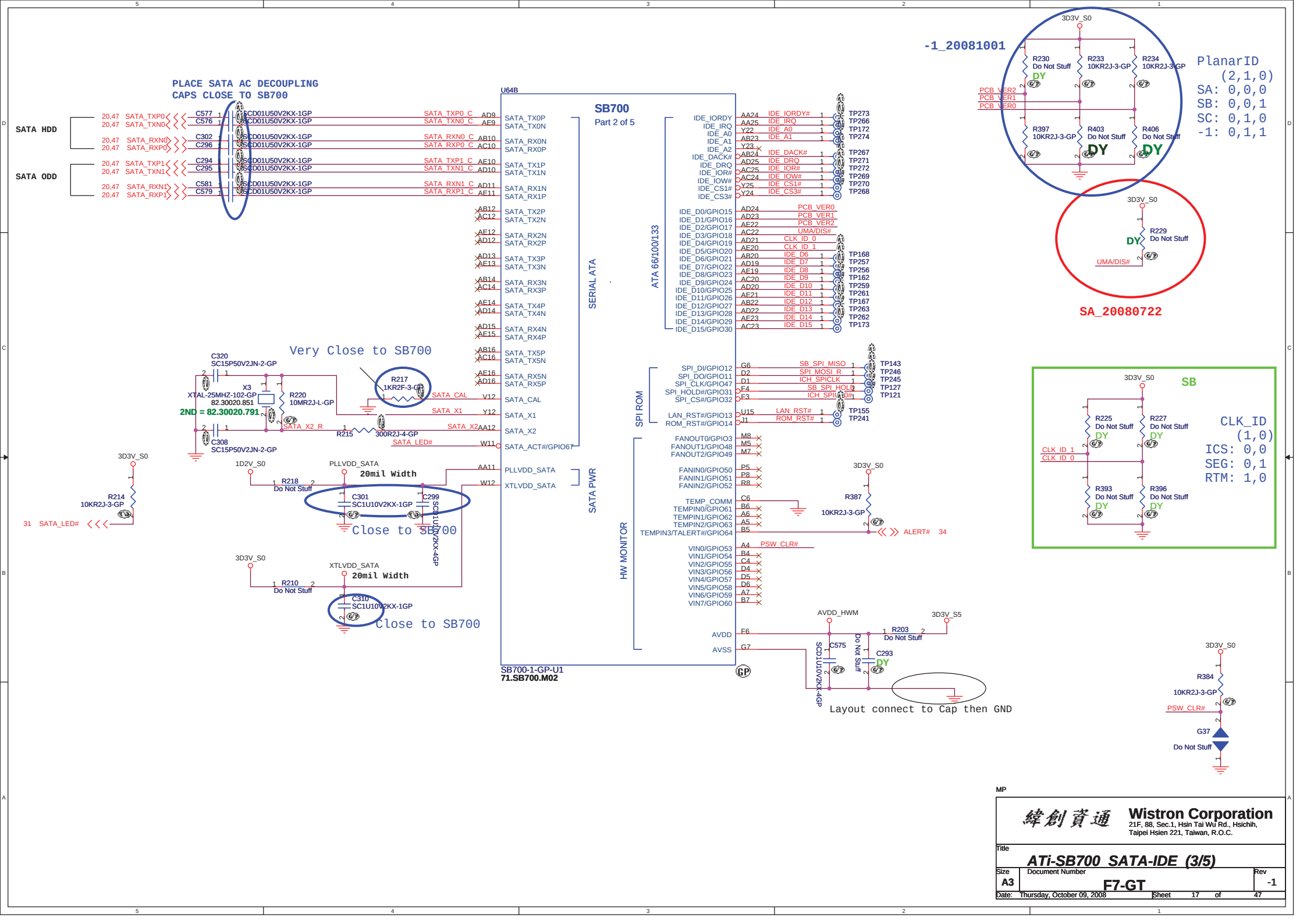
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD CONN & LED		
Size	Document Number: F7-GT	Rev: -1
Date: Wednesday, October 29, 2008	Sheet 13 of 47	

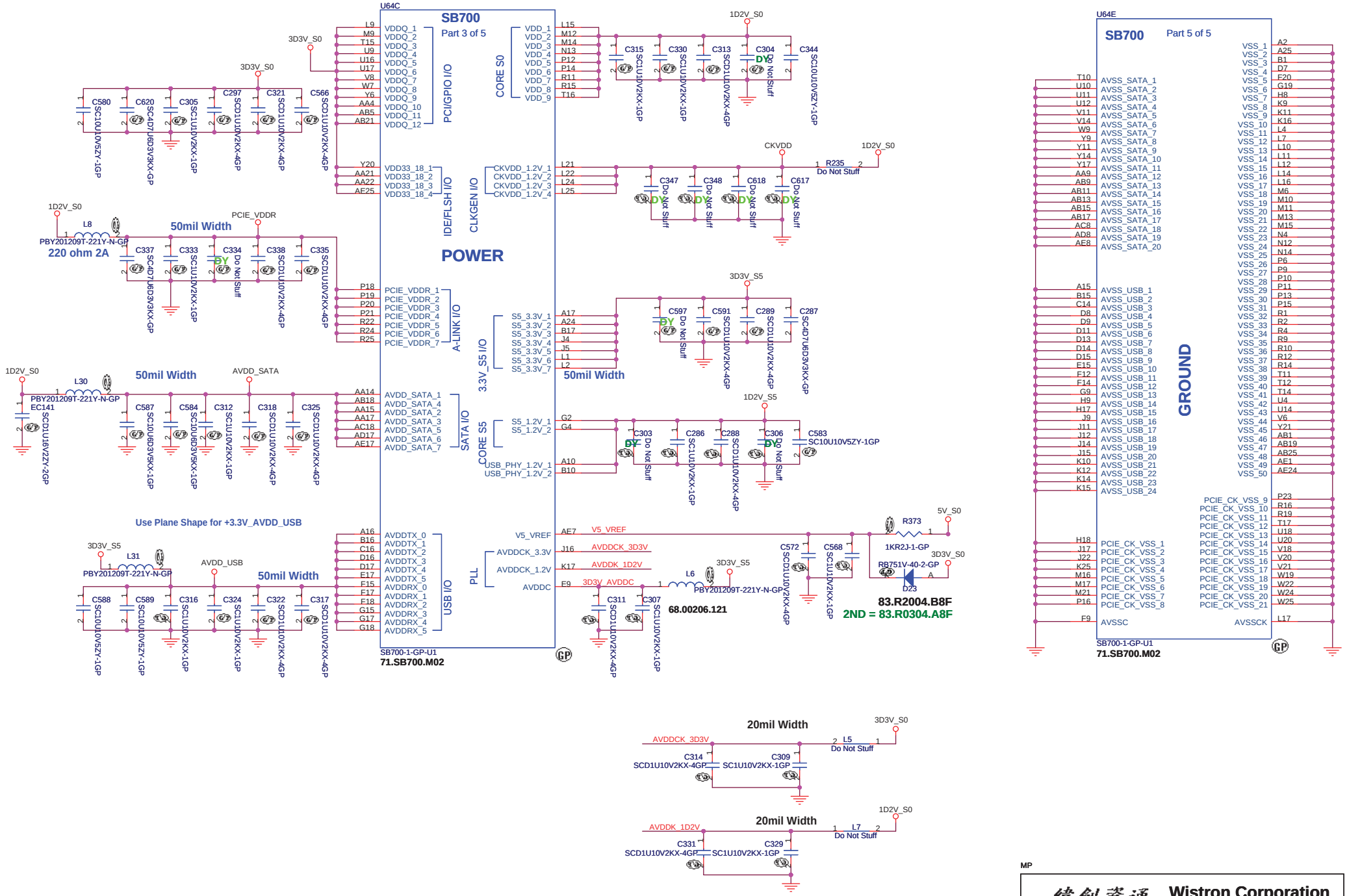


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*CRT/TV Connector*	
Size	Document Number F7-GT	Rev -1
Date: Thursday, October 09, 2008	Sheet 14 of 47	


SB700
Part 1 of 5
U64A
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
SB700-1-GP-U1
71.SB700.M02
20mil Width
Place R <100mils form pins T25,T24
220 ohm 2A
PBY201209T-221Y-N-GP
73.07408.L16
2ND = 73.07408.02B
TSLVC08APW-1-GP
SB_20080825
X6
X-32D768KHZ-46GP
82.30001.861
2ND = 82.30001.691
SC18P50V2JN-1-GP
10MR2J-L-GP
ACES-CON3-GP-U1
20.F0714.003
2ND = 20.F1000.003
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB700_PCIE&PCI_(1/5)
F7-GT
Size A3
Rev -1
Date: Thursday, October 09, 2008
Sheet 15 of 47


SB700
Part 4 of 5
U64D
SB700-1-GP-U1
71.SB700.M02
-1M_20081009
-1_20081001
SA_20080722
Close to SB700
Place these close SB700
Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.
Strap Pin / define to use LPC or SPI ROM
TO STRAPS
NEWCARD /GLAN
USB
Pair Device
11 MINIC1
10 WEBCAM
9 NEW1
8 USB2
7 NC
6 FP
5 Bluetooth
4 USB3
3 DOCK
2 NC
1 Cardreader
0 USB1
OCP4#
OCP0#
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB700_USB&GPIO_(2/5)
F7-GT
Size A3
Rev -1
Date: Thursday, October 09, 2008
Sheet 16 of 47


-1_20081001
PlanarID
(2,1,0)
SA: 0,0,0
SB: 0,1,0
SC: 0,1,0
-1: 0,1,1
SA_20080722
SB
CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0
PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700
SATA HDD
SATA ODD
SB700
Part 2 of 5
SB700-1-GP-U1
71.SB700.M02
SERIAL ATA
SATA PWR
ATA 66/100/133
SPI ROM
HW MONITOR
Very Close to SB700
Close to SB700
Close to SB700
20mil Width
20mil Width
2ND = 82.30020.791
Do Not Stuff
DY
Layout connect to Cap then GND
MP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700 SATA-IDE (3/5)
Size
A3
Document Number
F7-GT
Rev
-1
Date: Thursday, October 09, 2008
Sheet 17 of 47



MP

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700 POWER&GND (4/5)

Size	Document Number	Rev
A3	F7-GT	-1

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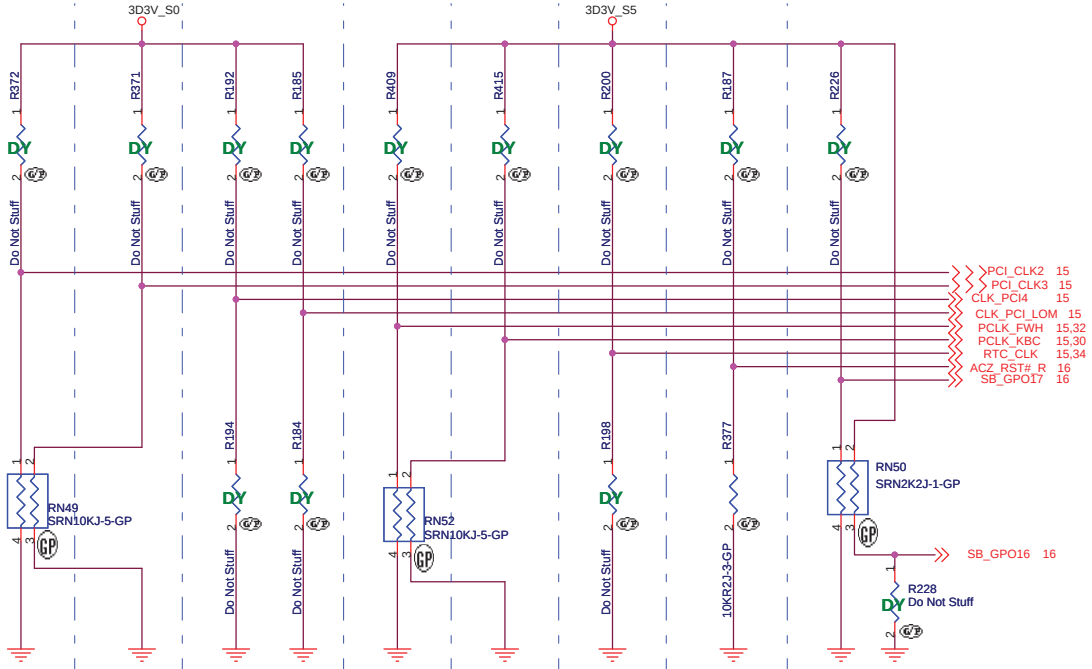
REQUIRED STRAPS

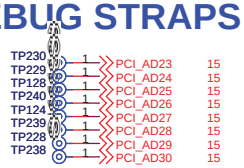
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved; H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM; L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

MP

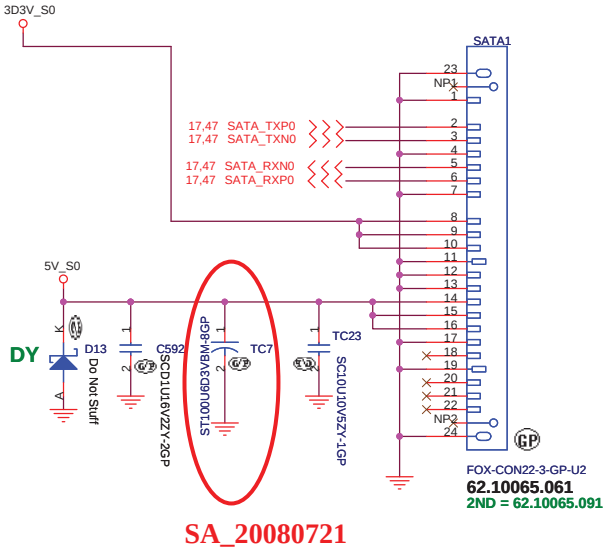
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: F7-GT | Rev: -1

Date: Thursday, October 09, 2008 | Sheet 19 of 47

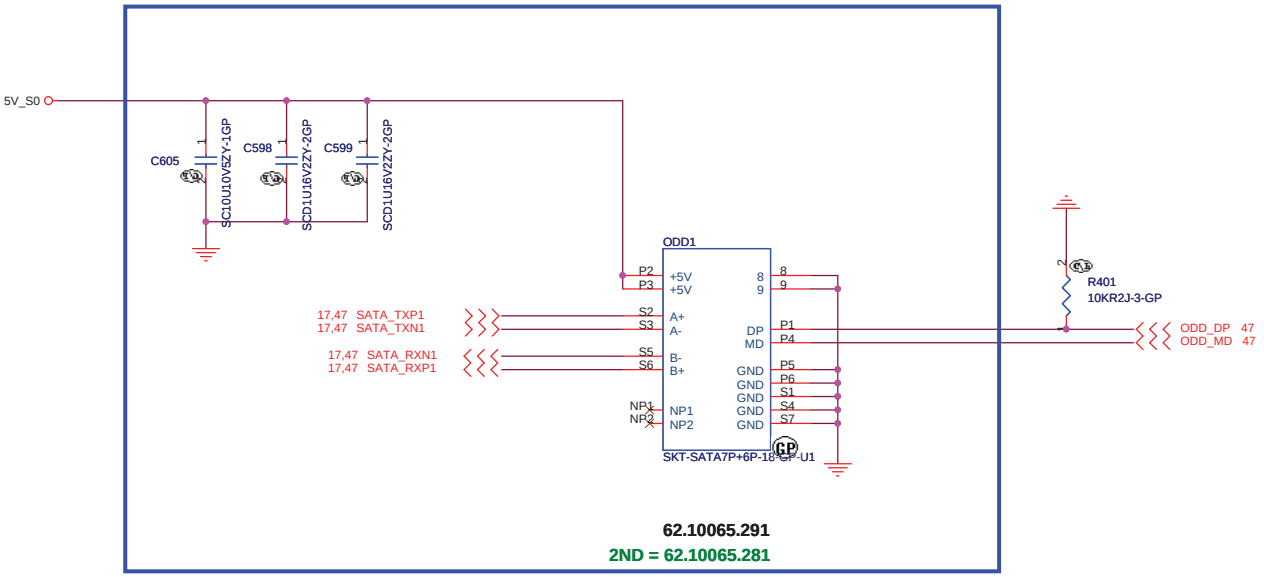
SATA HDD Connector



SA_20080721

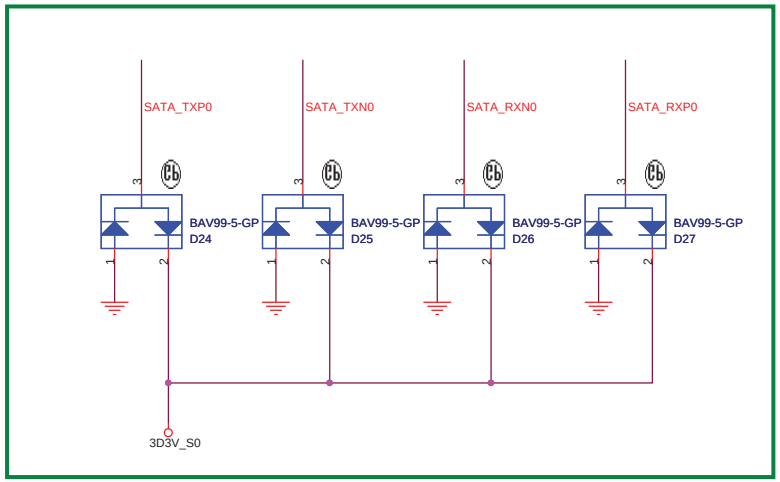
SA_20080714

SATA ODD Connector

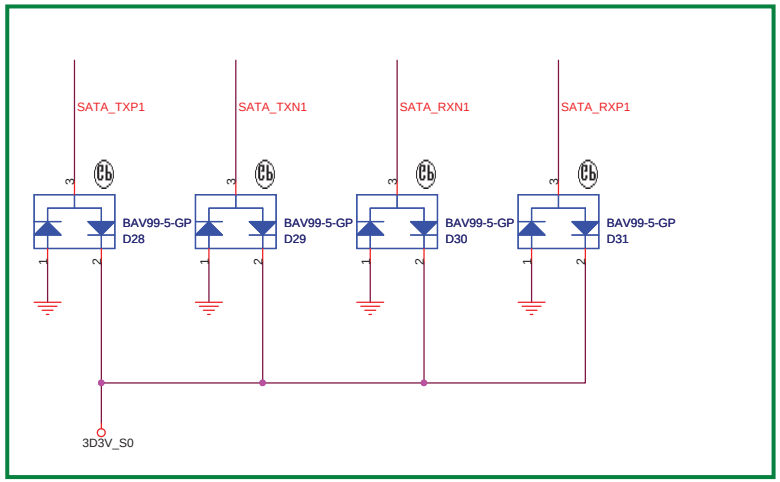


SB_20080825

For HDD



For ODD



MP

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD and CDROM

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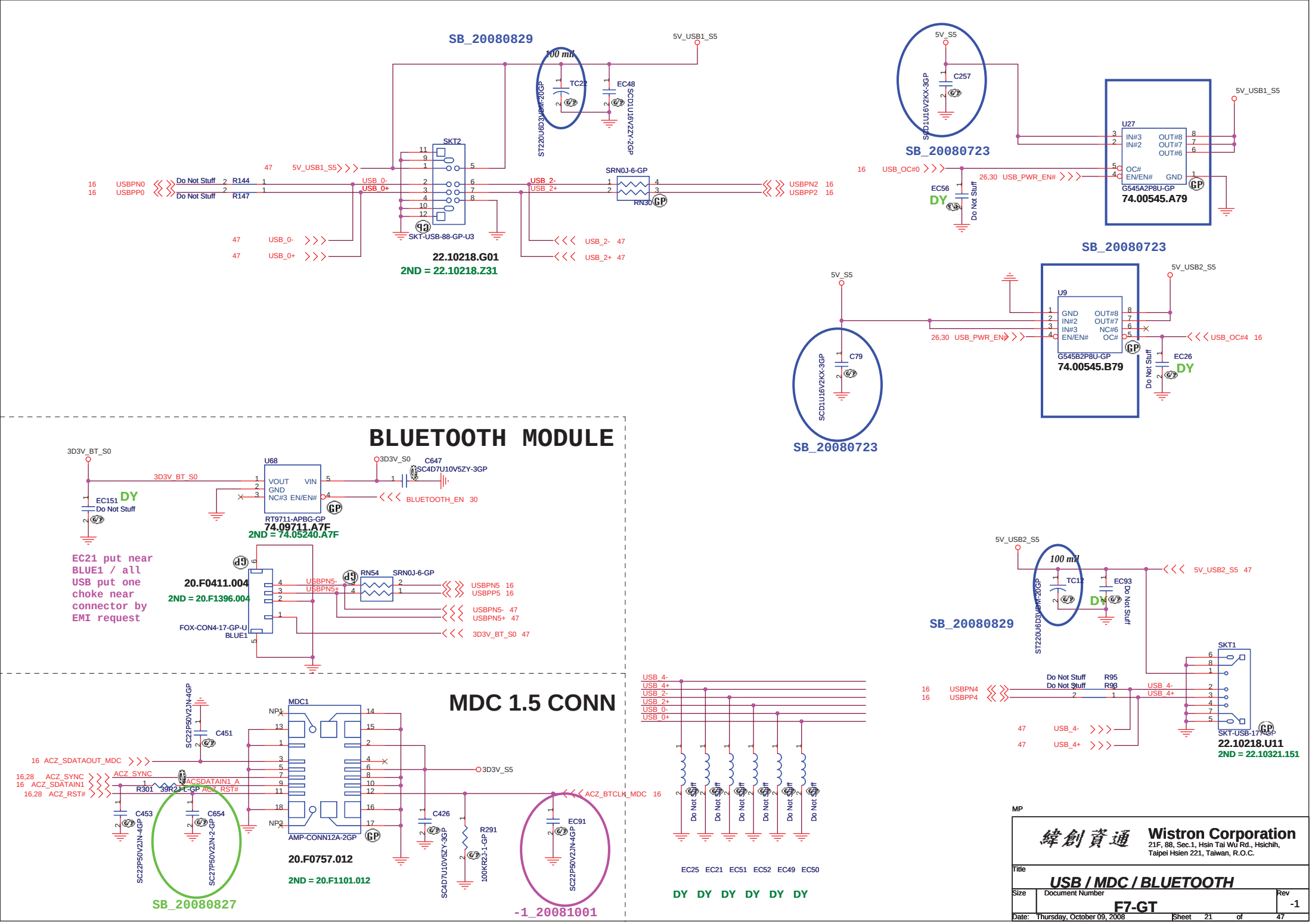
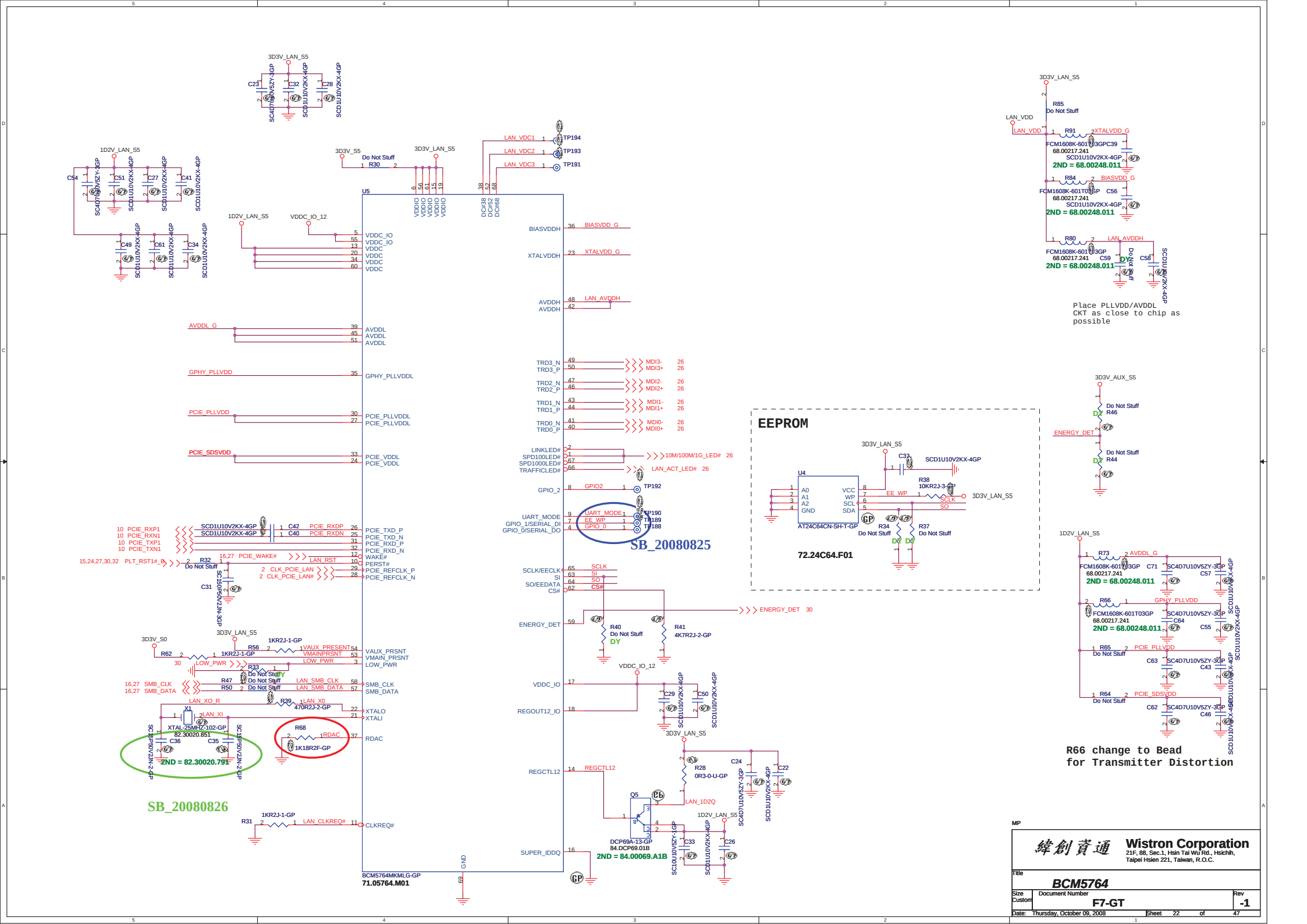

SB_20080829
5V_USB1_S5
100 mil
TC22
EC48
ST220U6D3VMF-2DGP
SCD1U16V2ZY-2GP
SKT2
SKT-USB-88-GP-U3
SRN0J-6-GP
RN30
USBPN0
USBPP0
USBPN2
USBPP2
R144
R147
Do Not Stuff
USB_0-
USB_0+
USB_2-
USB_2+
22.10218.G01
2ND = 22.10218.Z31
SB_20080723
C257
SCD1U16V2KX-3GP
U27
IN#3
IN#2
OUT#8
OUT#7
OUT#6
OC#
EN/EN#
GND
G545A2P8U-GP
74.00545.A79
USB_OC#0
26,30 USB_PWR_EN#
EC56
DY
SB_20080723
U9
GND
IN#2
IN#3
EN/EN#
OUT#8
OUT#7
NC#6
OC#
G545B2P8U-GP
74.00545.B79
5V_USB2_S5
USB_OC#4
C79
EC26
SB_20080723
BLUETOOTH MODULE
3D3V_BT_S0
U68
VOUT
GND
NC#3
VIN
EN/EN#
RT9711-APBG-GP
74.09711.A7F
2ND = 74.05240.A7F
C647
SC4D7U10V5ZY-3GP
BLUETOOTH_EN
EC151
DY
Do Not Stuff
EC21 put near BLUE1 / all USB put one choke near connector by EMI request
20.F0411.004
2ND = 20.F1396.004
RN54
SRN0J-6-GP
USBPN5-
USBPN5+
USBPN5
USBPP5
FOX-CON4-17-GP-U
BLUE1
3D3V_BT_S0
MDC 1.5 CONN
MDC1
AMP-CONN12A-2GP
20.F0757.012
2ND = 20.F1101.012
SB_20080827
C451
C453
C654
C426
R291
R301
39R2J-L-GP
SC22P50V2JN-4GP
SC27P50V2JN-2GP
SC4D7U10V5ZY-3GP
100KR2J-1-GP
16 ACZ_SDATAOUT_MDC
16,28 ACZ_SYNC
16 ACZ_SDATAIN1
16,28 ACZ_RST#
ACSDATAIN1_A
ACZ_RST#
3D3V_S5
ACZ_BTCLK_MDC
-1_20081001
EC91
USB_4-
USB_4+
USB_2-
USB_2+
USB_0-
USB_0+
EC25 EC21 EC51 EC52 EC49 EC50
DY DY DY DY DY DY
SB_20080829
TC12
EC93
SKT1
SKT-USB-17-GP
USBPN4
USBPP4
R95
R93
22.10218.U11
2ND = 22.10321.151
MP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
USB / MDC / BLUETOOTH
Size
Document Number
F7-GT
Rev
-1
Date: Thursday, October 09, 2008
Sheet 21 of 47


U5
BCM5764MKMLG-GP
71.05764.M01
EEPROM
AT24C64CN-SH-T-GP
72.24C64.F01
SB_20080825
SB_20080826
2ND = 82.30020.791
2ND = 84.00069.A1B
2ND = 68.00248.011
Place PLLVDD/AVDDL CKT as close to chip as possible
R66 change to Bead for Transmitter Distortion
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
BCM5764
F7-GT
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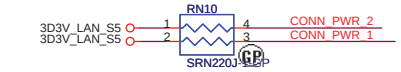
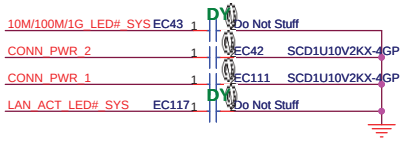
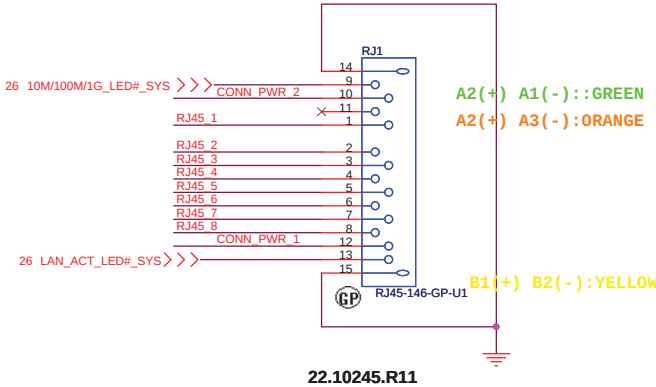
22
47

LAN Connector



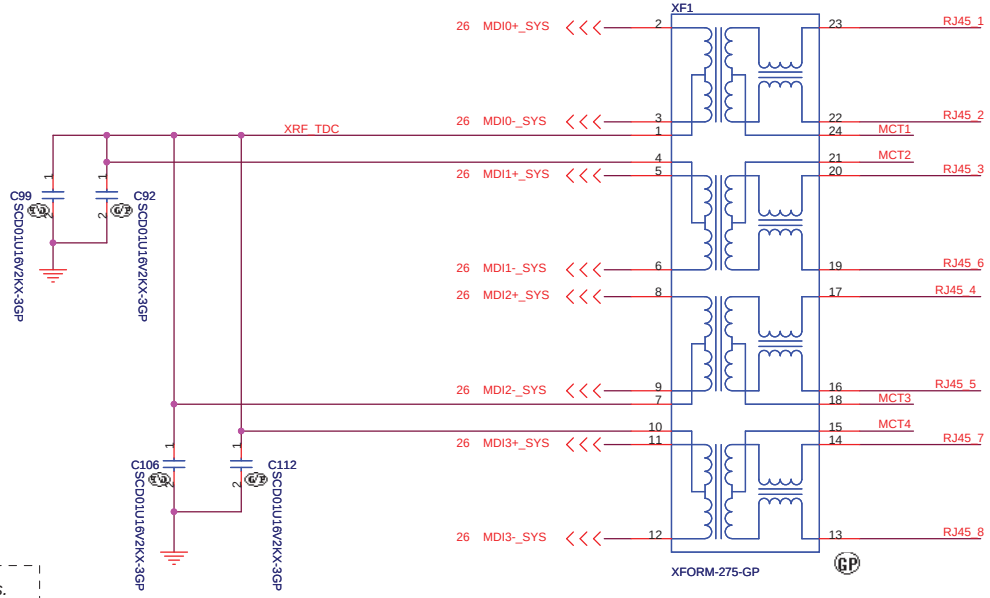




22.10245.R11

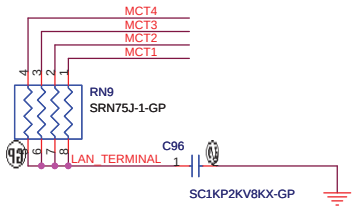
2ND = 22.10245.X61

GIGA Lan Transformer



68.89240.30A

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

MP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector

Size	Document Number	Rev
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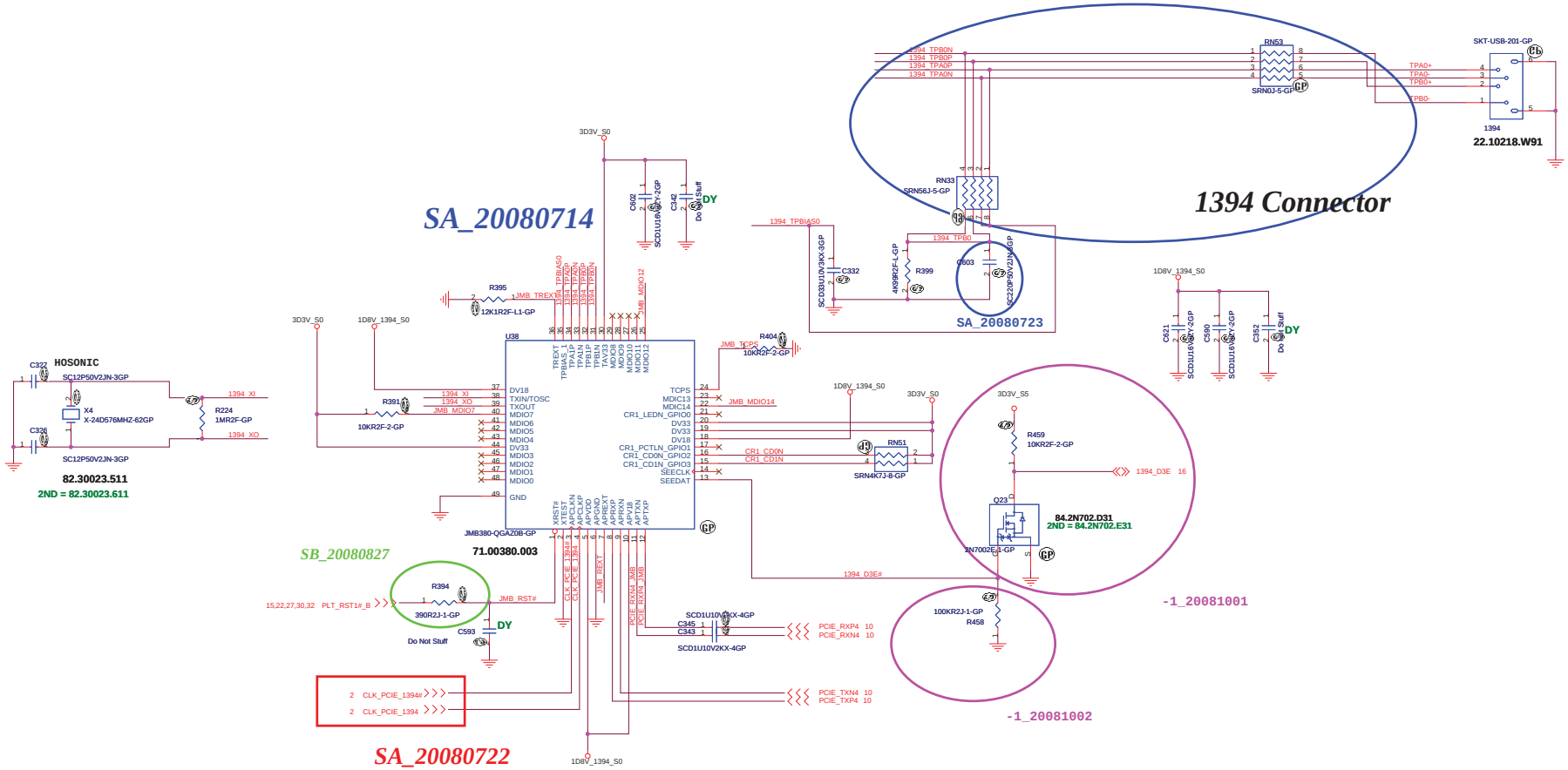


H:on-board, L:on Add-in card
H:CR1_LEDN high active,L:CR1_LEDN low active
H:CR1_PCTLN high active,L:CR1_PCTLN low active
(MDIO12 is no use in MP version IC)

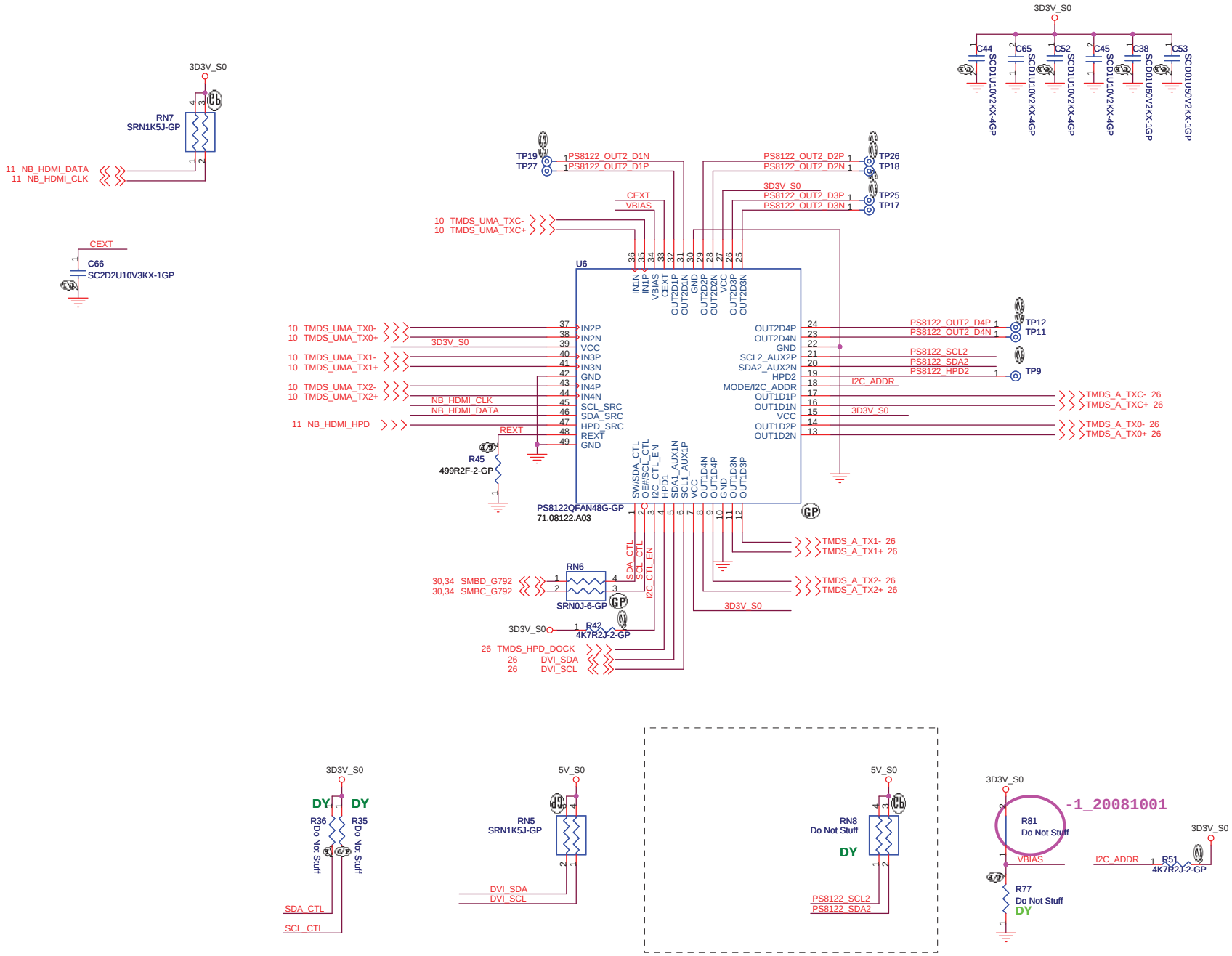
MP

綽創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1394-JMB380

Size | Document Number: F7-GT | Rev: -1

Date: Thursday, October 09, 2008 | Sheet 24 of 47

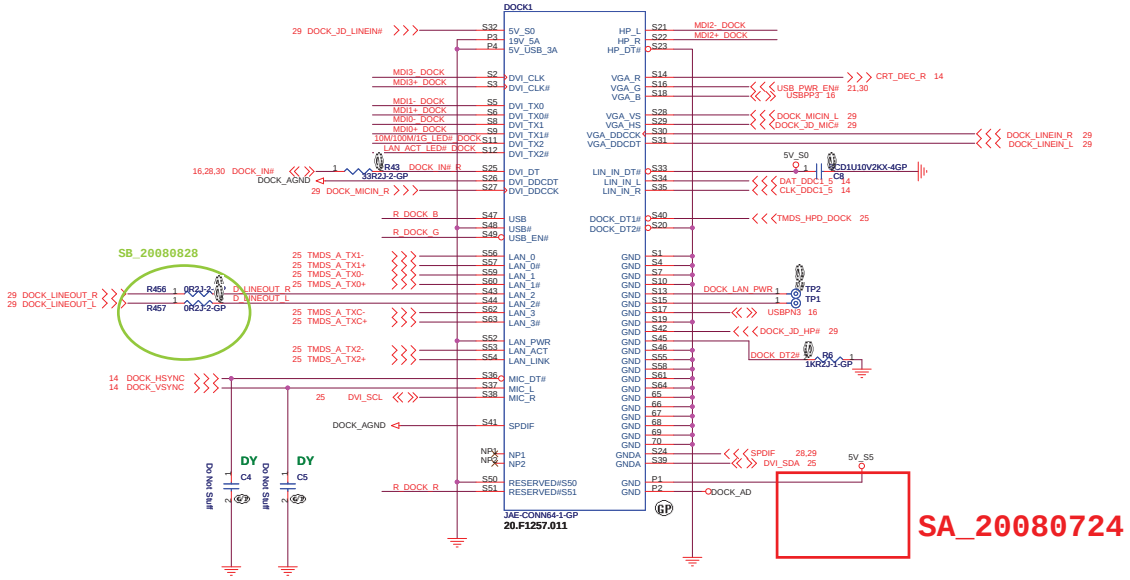


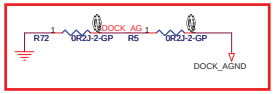
MP

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*PS8122*	
Size	Document Number: F7-GT	Rev: -1
Date: Thursday, October 09, 2008	Sheet 25 of 47	

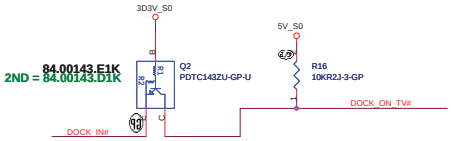
SA_20080709 change to Port Replicator

DOCK

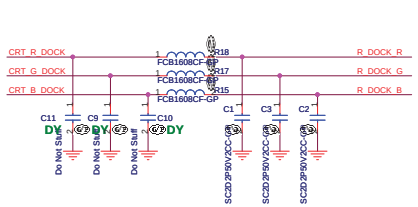


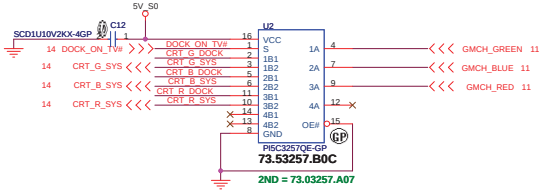


CRT SWITCH

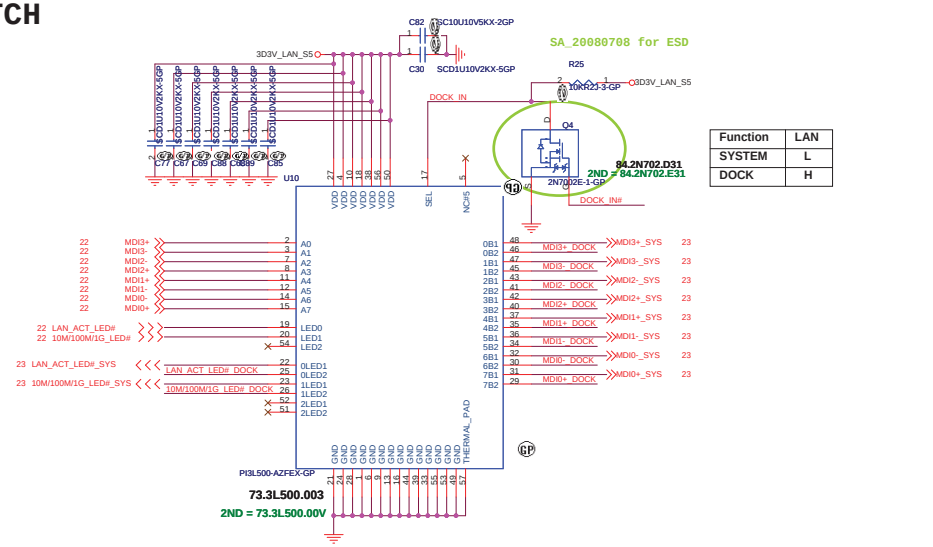


Function	CRT	TV
SYSTEM	H	H
DOCK	L	L





LAN SWITCH



Function	LAN
SYSTEM	L
DOCK	H

MP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DOCK

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NEWCARD Connector

Mini Card Connector

Reserve the symbol for bottom side connector

SK1 — 21.H0168.001 — 2ND = 21.H0182.001 — CARDBUS-SKT-GP

NEW1 — FCI-CON26-7-GP — 20.F1336.026 — 2ND = 62.10081.131

EC140 (DY, Do Not Stuff) — 3D3V_NEW_LAN_S5 — EC139 (DY, Do Not Stuff)

TPS2231_PERST# — R216 (DY, Do Not Stuff) — 1D5V_NEW_S0

3D3V_NEW_S0 — CLK_PCIE_NEW / CLK_PCIE_NEW# — CPPE# — CPUTSB# — USBPP9 / USBPN9

PCIE_TXP5 / PCIE_TXN5 — PCIE_RXP5 / PCIE_RXN5

SA_20080722 — SB_20080827

15,22,24,30,32 PLT_RST1#_B — R202 390R2J-1-GP — NEW_PLT_RST1# — C292 (DY) — A_RST — Do Not Stuff

WHEN DUMMY U19,R702 MUST STUFF

3D3V_S5 — R383 / R385 (DY, Do Not Stuff) — CPPE# — CPUTSB# — TPS2231_PERST# — 16,30,39,41 PM_SLP_S5#

U34 — G577BR91U-GP

SYSRST# / CPPE# / CPUSB# / PERST# / SHDN#

3_3VIN / 3_3VOUT / 1_5VIN / 1_5VOUT / AUXIN / AUXOUT

STBY# / RCLKEN / OC# / GND / GND

3D3V_NEW_S0 — 3D3V_S0 — 1D5V_S0 — 1D5V_NEW_S0 — 3D3V_S5 — 3D3V_NEW_LAN_S5

16,30,33,34,35 PM_SLP_S3#

74.00577.A73 — 2ND = 74.02231.A73

CHECK /POWER PIN

SB

MINIC1 — SKT-MINI52P-15-GP

3D3V_S0_MINI — MINI_WAKE# — TP184

CLK_PCIE_MINI1# 2 / CLK_PCIE_MINI1 2

PCIE_RXP2 10 / PCIE_RXN2 10 / PCIE_TXP2 10 / PCIE_TXN2 10

E51_RxD 30 / E51_TxD 30

USBPN7 16 / USBPP7 16

LED_WPAN# — LED_WPAN# 1D5V_S0

WLAN_LED# 31,47

SA_20080722

30 WIRELESS_EN — 15,22,24,30,32 PLT_RST1#_B — R426 150R2F-1-GP — A_RST

R425 / R416 (DY, Do Not Stuff) — 3D3V_P24 — R427 (DY, Do Not Stuff)

C630 SC120P50V3JN-GP (Do Not Stuff) — 16,22 SMB_CLK / SMB_DATA — R423 / R424 (DY, Do Not Stuff) — SMB_CLK_MINI / SMB_DATA_MINI

R440 / R442 0R3-0-U-GP

R418 10KR2J-3-GP — 3D3V_S0

SA_20080723

R241 0R3-0-U-GP — 5V_S5

20.F1049.052 — 2ND = 62.10043.461

CHECK WITH COLUMBIA

Place them Near to Chip: C328, C285 (SC1U16V3ZY-GP)

Place them Near to Connector: C323, C585, C300, C578, C582 (SC1U16V2ZY-2GP)

Place near MINIC1: R422, R417 (0R5J-5-GP, DY, Do Not Stuff); TC24, C367, C629, C633, C627, C628, C631, C632, C626 (SC1U16V3ZY-GP / SC1U16V2ZY-2GP, DY, Do Not Stuff)

MP

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD / NEW CARD

Size | Document Number: F7-GT | Rev: -1

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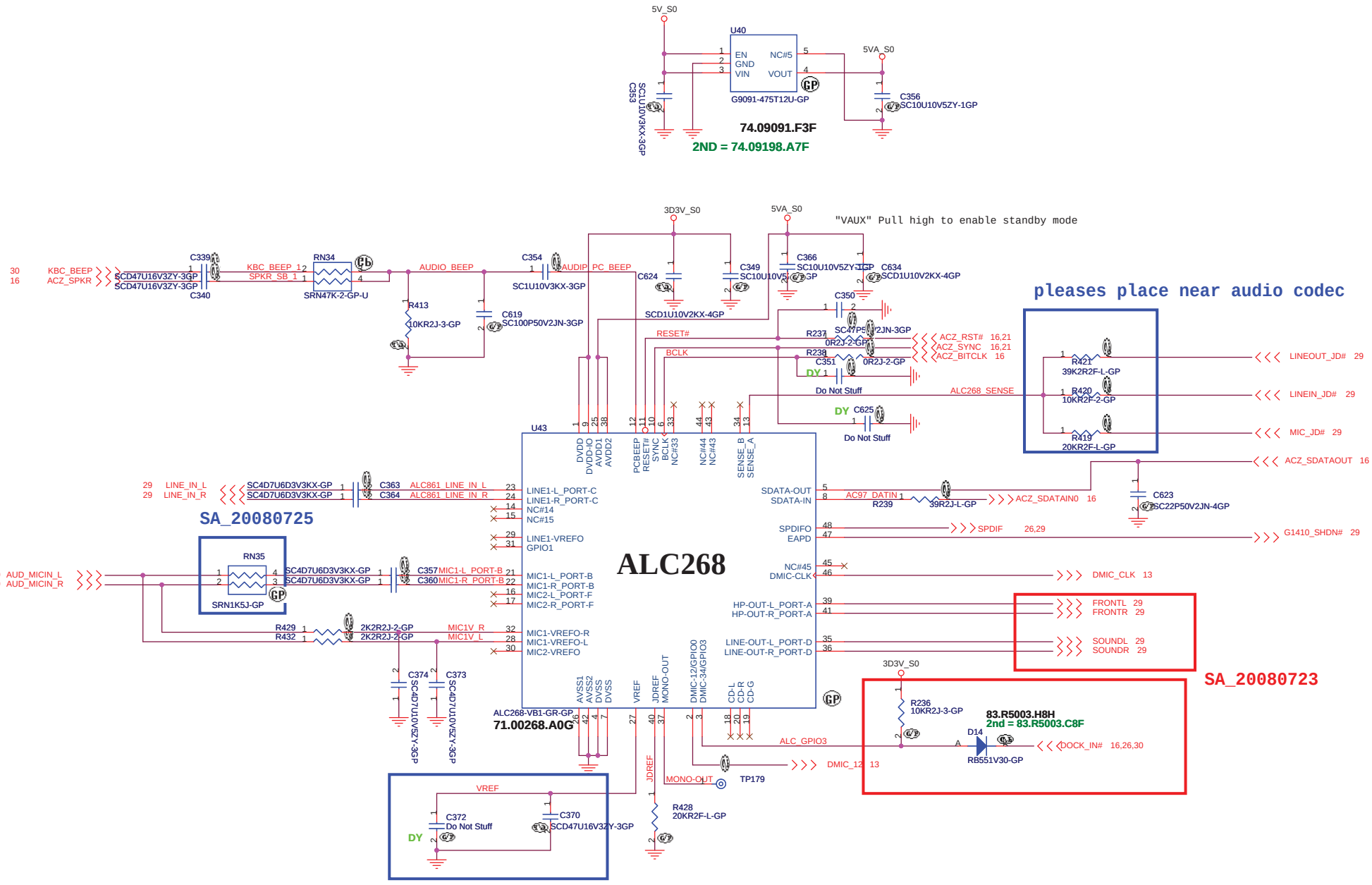
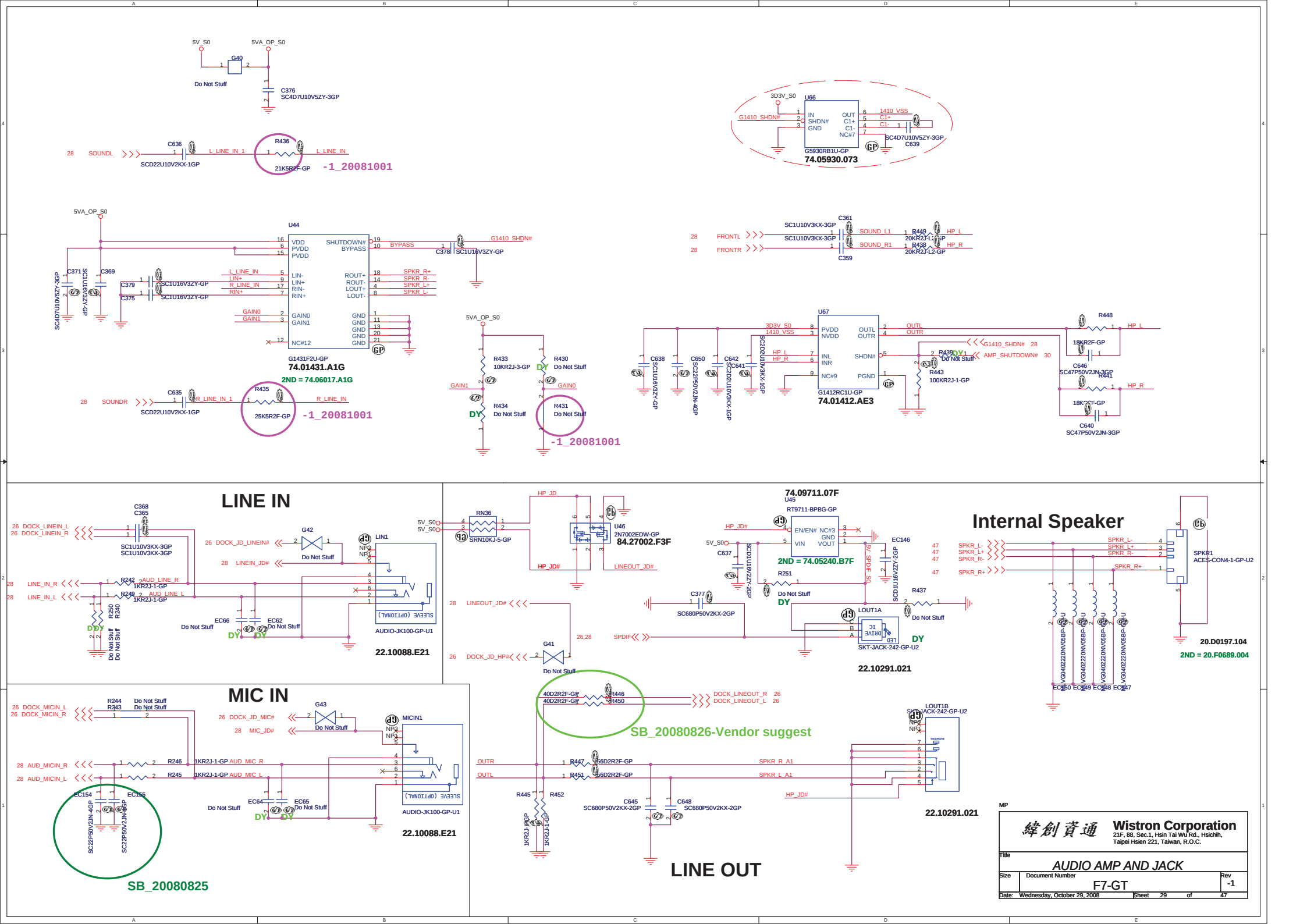


MP

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*AZALIA CODEC - ALC268*
Size	Document Number: F7-GT — Rev: -1
Date: Thursday, October 09, 2008	Sheet 28 of 47


5V_S0
5VA_OP_S0
G40
Do Not Stuff
C376
SC4D7U10V5ZY-3GP
28 SOUNDL
C636
L_LINE_IN_1
R436
L_LINE_IN
SCD22U10V2KX-1GP
21K5R2F-GP
-1_20081001
3D3V_S0
U66
G1410_SHDN#
IN
SHDN#
GND
OUT
C1+
C1-
NC#7
1410_VSS
G5930RB1U-GP
74.05930.073
C639
SC4D7U10V5ZY-3GP
U44
VDD
PVDD
SHUTDOWN#
BYPASS
LIN-
LIN+
RIN-
RIN+
ROUT+
ROUT-
LOUT+
LOUT-
GAIN0
GAIN1
NC#12
GND
SPKR_R+
SPKR_R-
SPKR_L+
SPKR_L-
C371
C369
C379
C375
SC1U16V3ZY-GP
C378
SC1U16V3ZY-GP
G1431F2U-GP
74.01431.A1G
2ND = 74.06017.A1G
28 SOUNDR
C635
R_LINE_IN_1
R_LINE_IN
R435
25K5R2F-GP
-1_20081001
R433
10KR2J-3-GP
R430
Do Not Stuff
R434
Do Not Stuff
R431
Do Not Stuff
-1_20081001
28 FRONTL
28 FRONTR
C361
C359
SC1U10V3KX-3GP
SOUND_L1
SOUND_R1
R449
R438
20KR2J-L1-GP
20KR2J-L2-GP
HP_L
HP_R
U67
PVDD
NVDD
INL
INR
NC#9
OUTL
OUTR
SHDN#
PGND
3D3V_S0
1410_VSS
HP_L
HP_R
G1412RC1U-GP
74.01412.AE3
C638
C650
C642
C641
SC1U16V3ZY-GP
SC22P50V2JN-4GP
SC2D2U10V3KX-1GP
G1410_SHDN# 28
AMP_SHUTDOWN# 30
R439
Do Not Stuff
R443
100KR2J-1-GP
R448
18KR2F-GP
R441
18KR2F-GP
C646
SC47P50V2JN-3GP
C640
SC47P50V2JN-3GP
LINE IN
26 DOCK_LINEIN_L
26 DOCK_LINEIN_R
C368
C365
SC1U10V3KX-3GP
SC1U10V3KX-3GP
G42
Do Not Stuff
26 DOCK_JD_LINEIN#
28 LINEIN_JD#
LIN1
28 LINE_IN_R
28 LINE_IN_L
R242
R249
1KR2J-1-GP
AUD_LINE_R
AUD_LINE_L
R250
R240
Do Not Stuff
Do Not Stuff
EC66
Do Not Stuff
EC62
Do Not Stuff
AUDIO-JK100-GP-U1
22.10088.E21
RN36
SRN10KJ-5-GP
HP_JD
HP_JD#
U46
2N7002EDW-GP
84.27002.F3F
LINEOUT_JD#
28 LINEOUT_JD#
26 DOCK_JD_HP#
G41
Do Not Stuff
26,28 SPDIF
74.09711.07F
U45
RT9711-BPBG-GP
EN/EN#
NC#3
GND
VIN
VOUT
2ND = 74.05240.B7F
C637
SCD1U16V2ZY-2GP
EC146
SV_SPDIF_SO
R251
Do Not Stuff
DY
C377
SC680P50V2KX-2GP
R437
Do Not Stuff
LOUT1A
SKT-JACK-242-GP-U2
DY
22.10291.021
Internal Speaker
SPKR_L-
SPKR_L+
SPKR_R-
SPKR_R+
47
SPKR1
ACES-CON4-1-GP-U2
20.D0197.104
2ND = 20.F0689.004
VG0402200NV05BP-U
EC150
EC149
EC148
EC147
MIC IN
26 DOCK_MICIN_L
26 DOCK_MICIN_R
R244
R243
Do Not Stuff
Do Not Stuff
G43
Do Not Stuff
26 DOCK_JD_MIC#
28 MIC_JD#
MICIN1
28 AUD_MICIN_R
28 AUD_MICIN_L
R246
R245
1KR2J-1-GP
AUD_MIC_R
AUD_MIC_L
EC154
EC155
SC22P50V2JN-4GP
SC22P50V2JN-4GP
Do Not Stuff
EC64
EC65
Do Not Stuff
AUDIO-JK100-GP-U1
22.10088.E21
SB_20080825
40D2R2F-GP
R446
R450
DOCK_LINEOUT_R 26
DOCK_LINEOUT_L 26
SB_20080826-Vendor suggest
OUTR
OUTL
R447
R451
56D2R2F-GP
SPKR_R_A1
SPKR_L_A1
HP_JD#
LOUT1B
SKT-JACK-242-GP-U2
R445
R452
1KR2J-1-GP
C645
C648
SC680P50V2KX-2GP
LINE OUT
22.10291.021
MP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO AMP AND JACK
Size
Document Number
F7-GT
Rev
-1
Date: Wednesday, October 29, 2008
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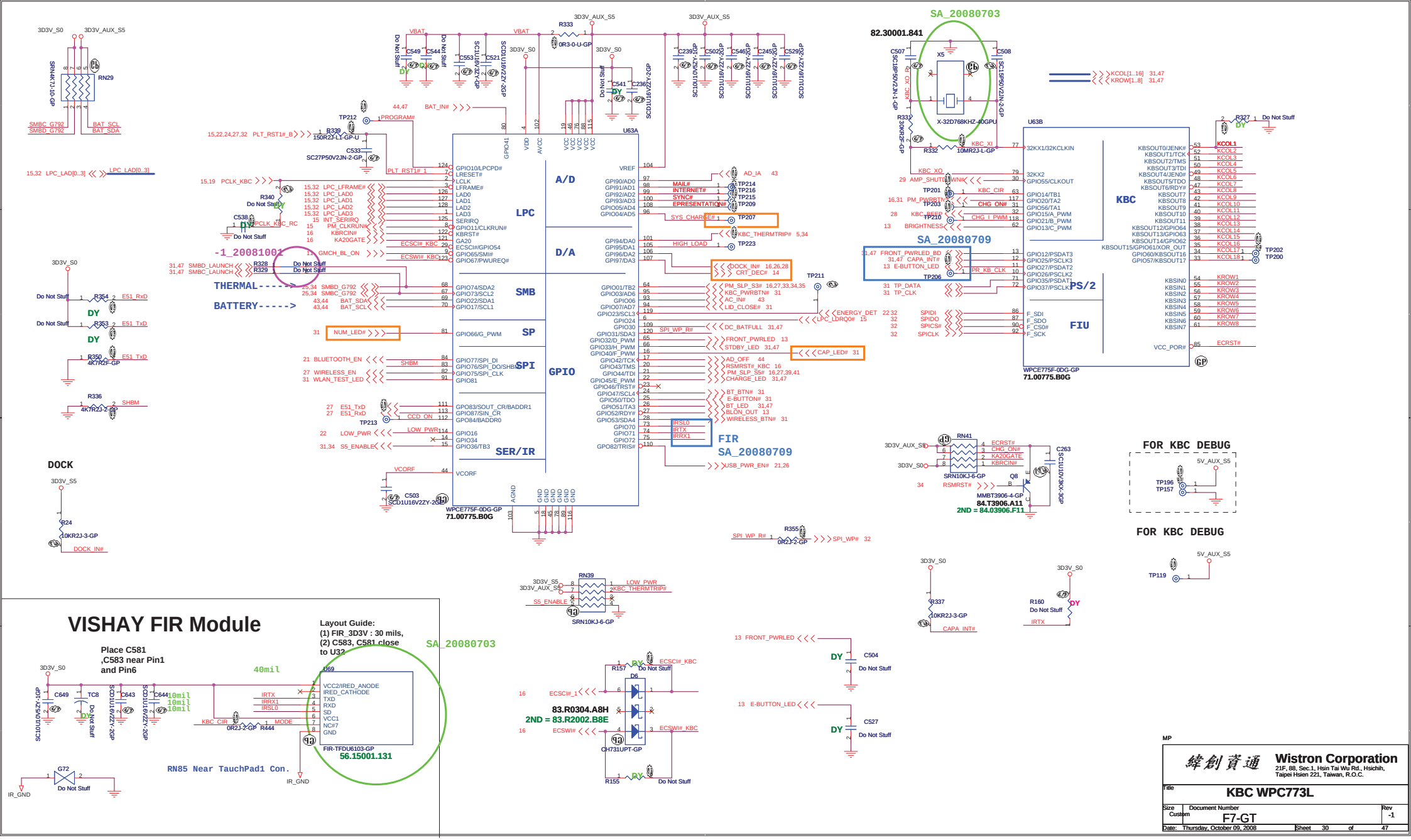
SA_20080703
82.30001.841
SA_20080709
-1_20081001
THERMAL------>
BATTERY----->
DOCK
VISHAY FIR Module
Place C581 ,C583 near Pin1 and Pin6
Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32
RN85 Near TauchPad1 Con.
83.R0304.A8H
2ND = 83.R2002.B8E
56.15001.131
FIR
SA_20080709
FOR KBC DEBUG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773L
F7-GT
Date: Thursday, October 09, 2008
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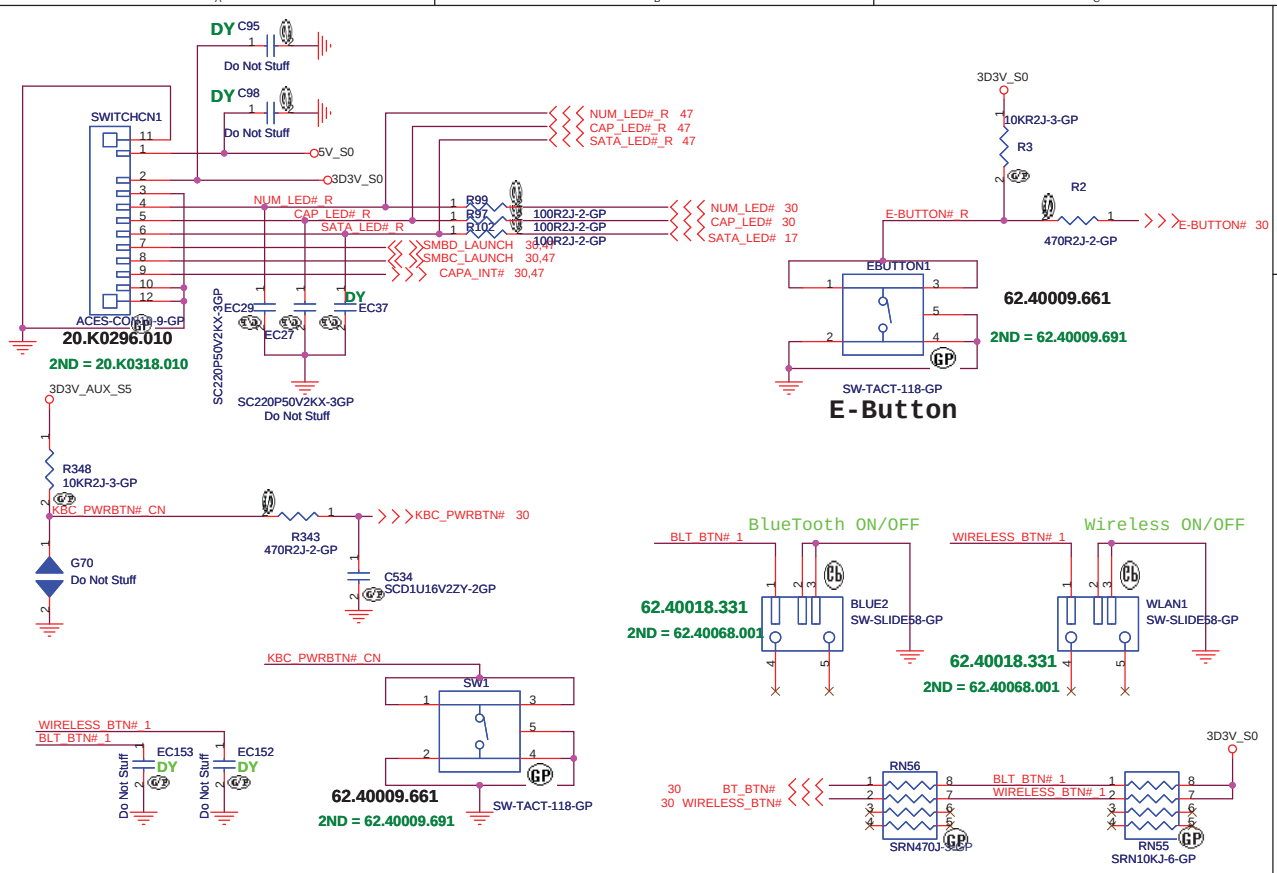

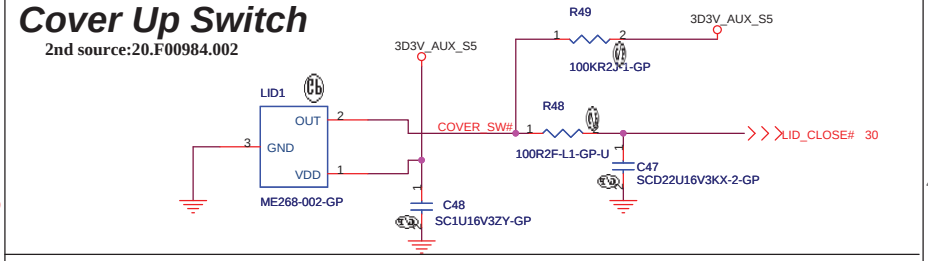

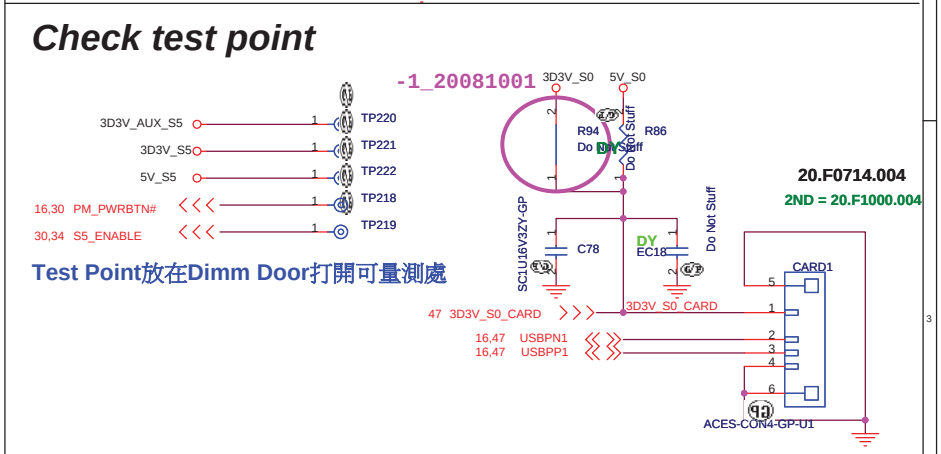

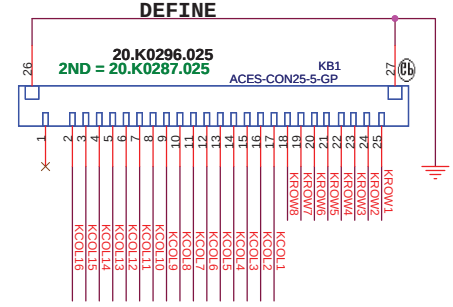

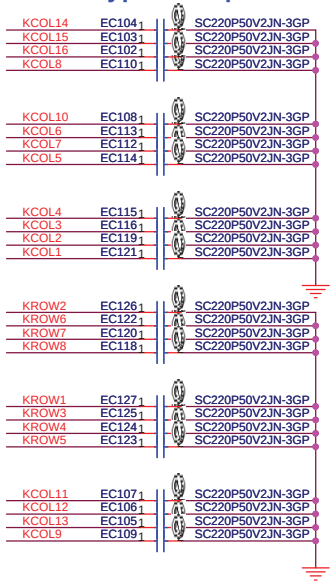

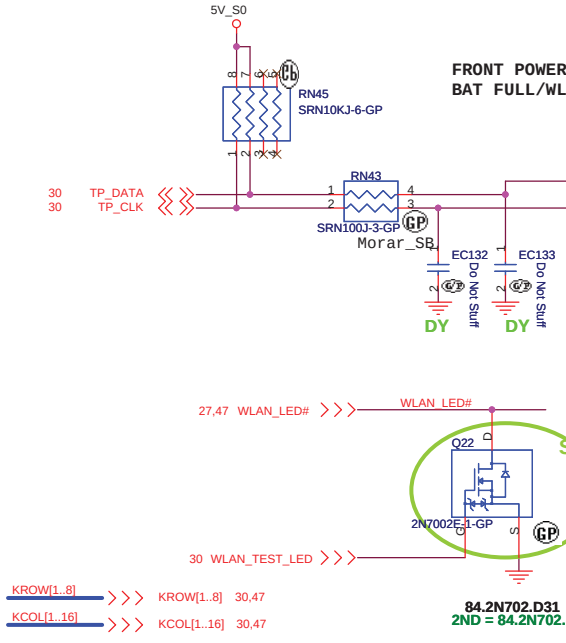

CHECK PIN DEFINE

MP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BUTTONs / KB / TOUCHPAD

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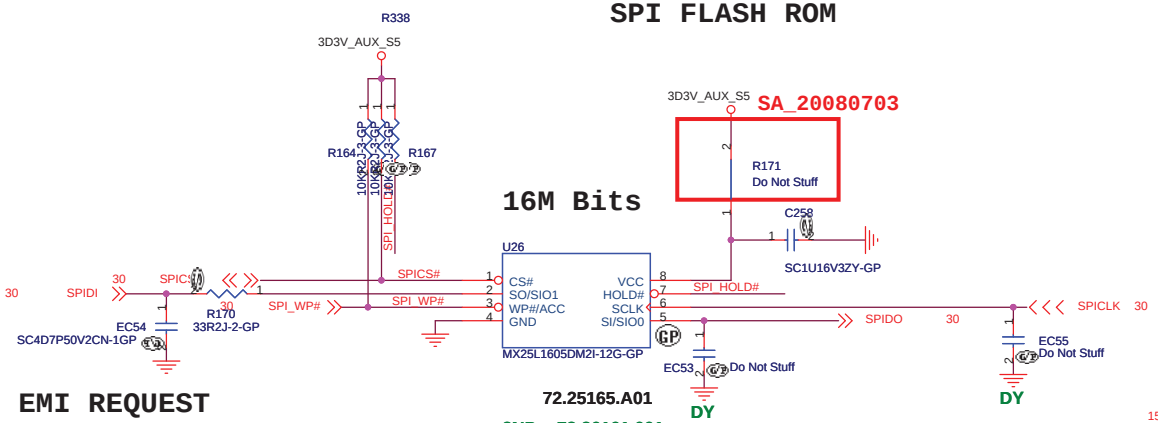
SPI FLASH ROM



EMI REQUEST

72.25165.A01

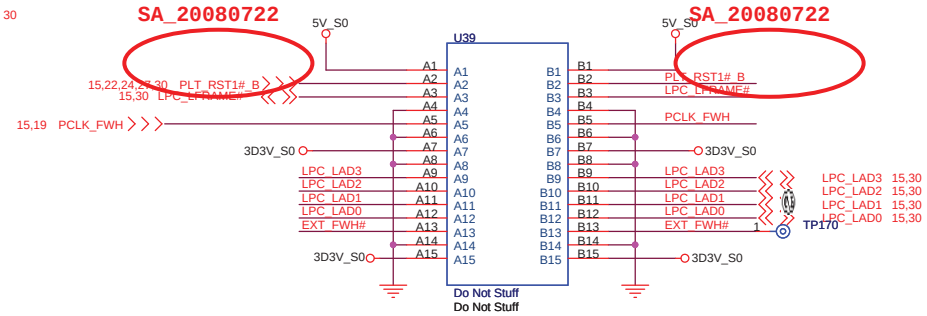
2ND = 72.26161.001

TOP VIEW

A15 (B1)
A14 (B2)
⋮ ⋮
A2 (B14)
A1 (B15)

(BOTTOM VIEW)

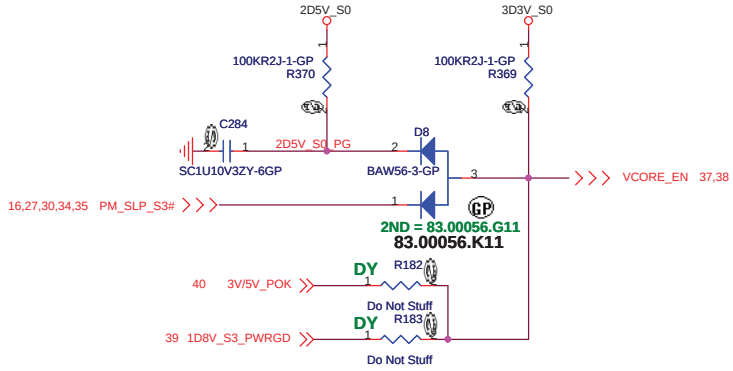
GOLDEN FINGER FOR DEBUG BOARD



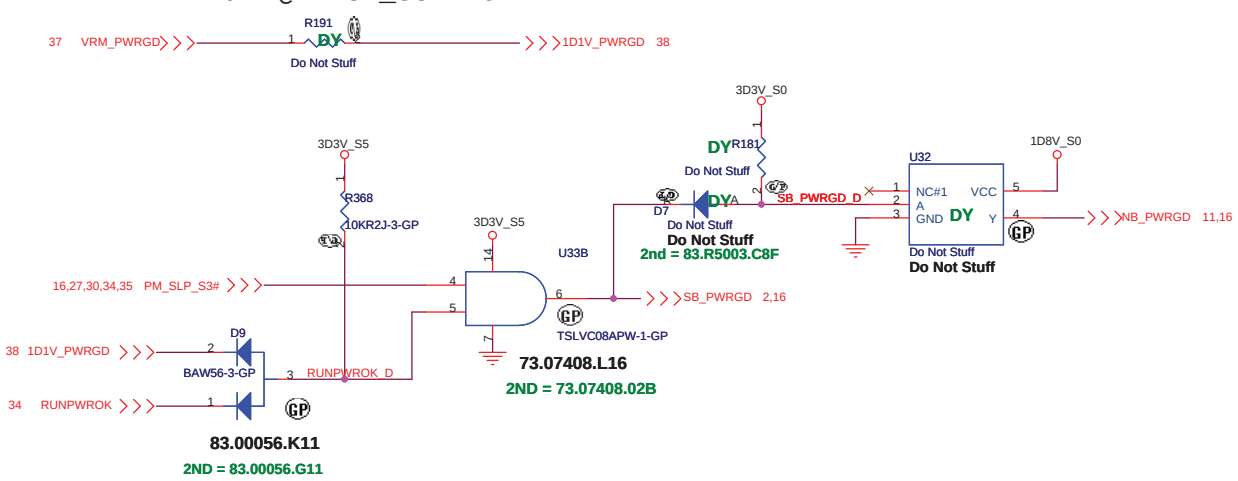
MP

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
BIOS			
Size: A3	Document Number: F7-GT		Rev: -1
Date: Thursday, October 09, 2008	Sheet 32 of 47		

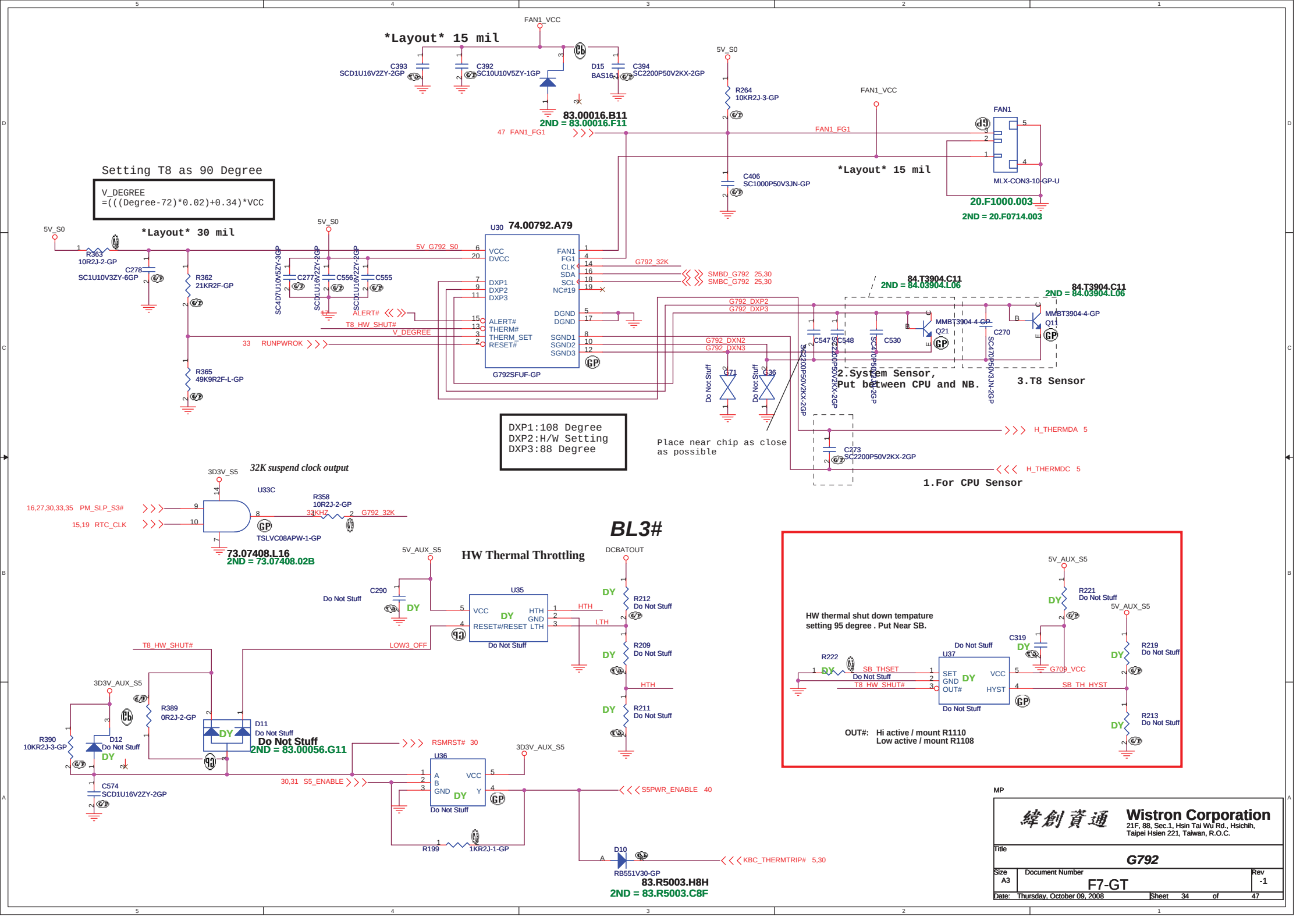


P/H @ 1D8V_S3 PAGE



MP

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: POWERGOOD&ENABLES		
Size: A3	Document Number: F7-GT	Rev: -1
Date: Thursday, October 09, 2008	Sheet 33 of 47	



MP

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: G792

Size	Document Number	Rev
A3	F7-GT	-1

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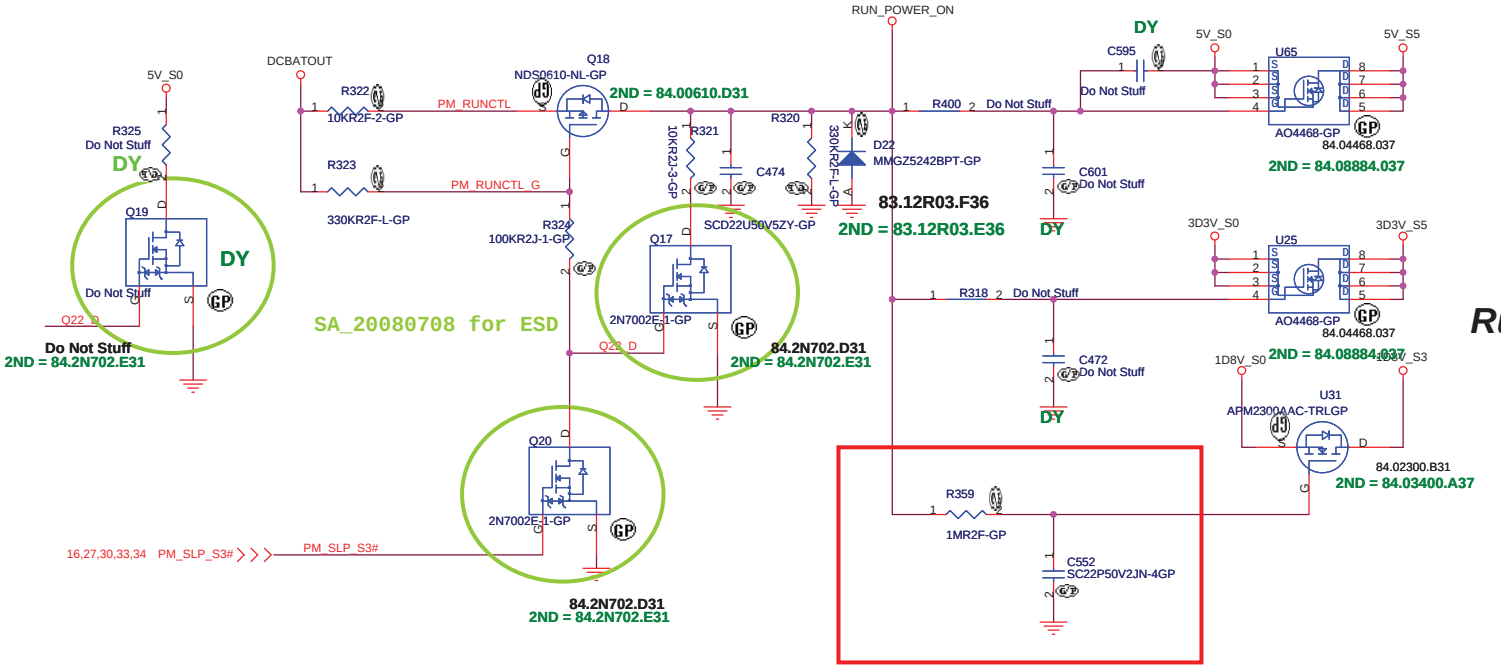

Run Power

MP

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***PWR CTL LOGIC / PWR PLANE***
Size: A3	Document Number: F7-GT
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Date: Thursday, October 09, 2008	Sheet 35 of 47

CPU_CORE
ISL6264CRZ

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

COREFB
COREFB#

Input Power
VCC(I)
VCC(I)
VCC(I)

DCBATOUT
5V_S0
3D3V_S0

TI TPS51120
3D3V/5V

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

DCBATOUT_51120

Input Power
VIN
REG5V_IN(I / 5V)

DCBATOUT_51120

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

APL5913

1D8V_S5

3D3V_S5 → INPUT / OUT → 1D2V_S5

APL5332KAC-TRLGP

Adapter

Input Signal
(I)

AD_OFF

Output Signal
(O)

AD_IN

Input Power
AD_JK
VCC(I)
5V_AUX_S5
VCC(I)

Output Power
VCC(O)

AD+

Charger_ISL6255

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

AD_IN
CHARGE_LED#
BL2#

Input Power
DCIN (I)

AD+

Output Power
VCC (O)
VCC (O)

DCBATOUT
BT+

TI TPS51116
1.8V / 0.9V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
DCBATOUT
VCC(I)
5V_S5
VCC(I)

Output Power
VCC(O)
VCC(O)

1.8V_S3
0.9V_S3

ISL6268_1D2V

1D2V_S0_EN

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Output Power
1D2V_PWR

1D2V (6.5A)

5V_S5
DCBATOUT

Input Power
VCC
VIN

ISL6268_VGA_CORE

VGA_CORE_EN

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Output Power
1D2V_PWR

VGA_CORE_S0 (15A)

5V_S5
DCBATOUT

Input Power
VCC
VIN

MP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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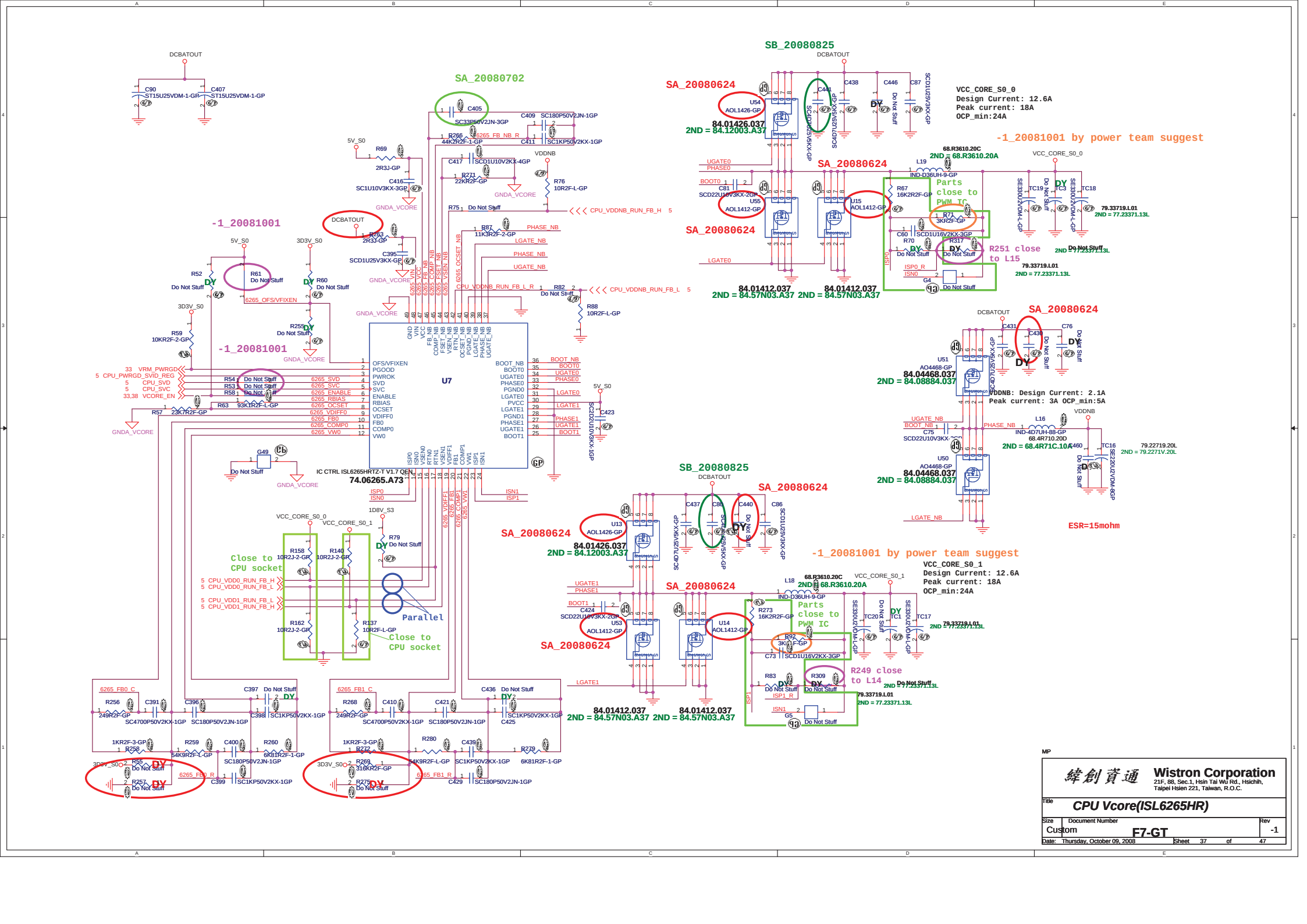
SA_20080825
SA_20080702
SA_20080624
-1_20081001
-1_20081001 by power team suggest
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
Parts close to PWM IC
R251 close to L15
R249 close to L14
Close to CPU socket
Parallel
ESR=15mohm
IC CTRL ISL6265HRTZ-T V1.7 QFN
74.06265.A73
U7
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
F7-GT
Custom
Date: Thursday, October 09, 2008
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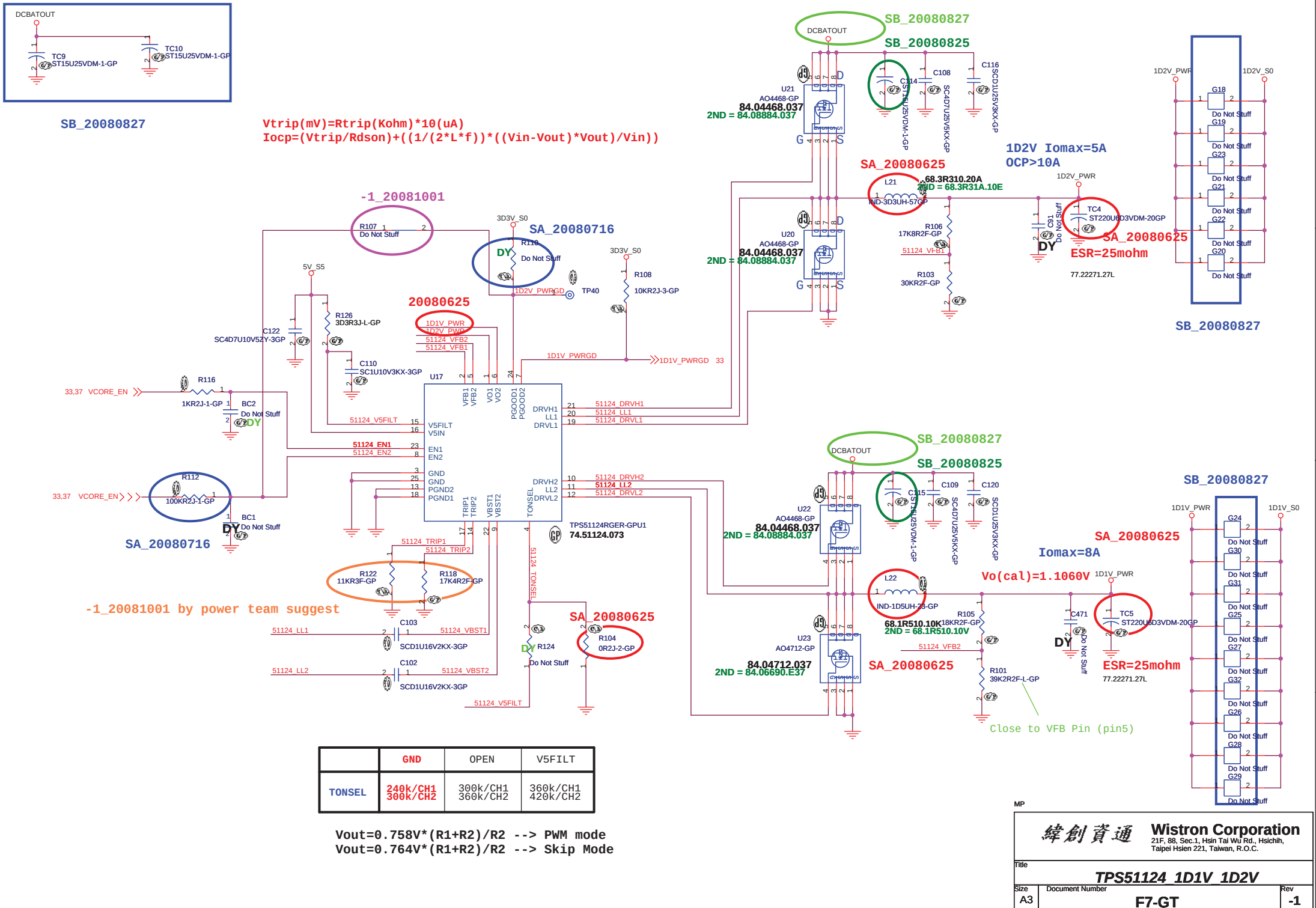
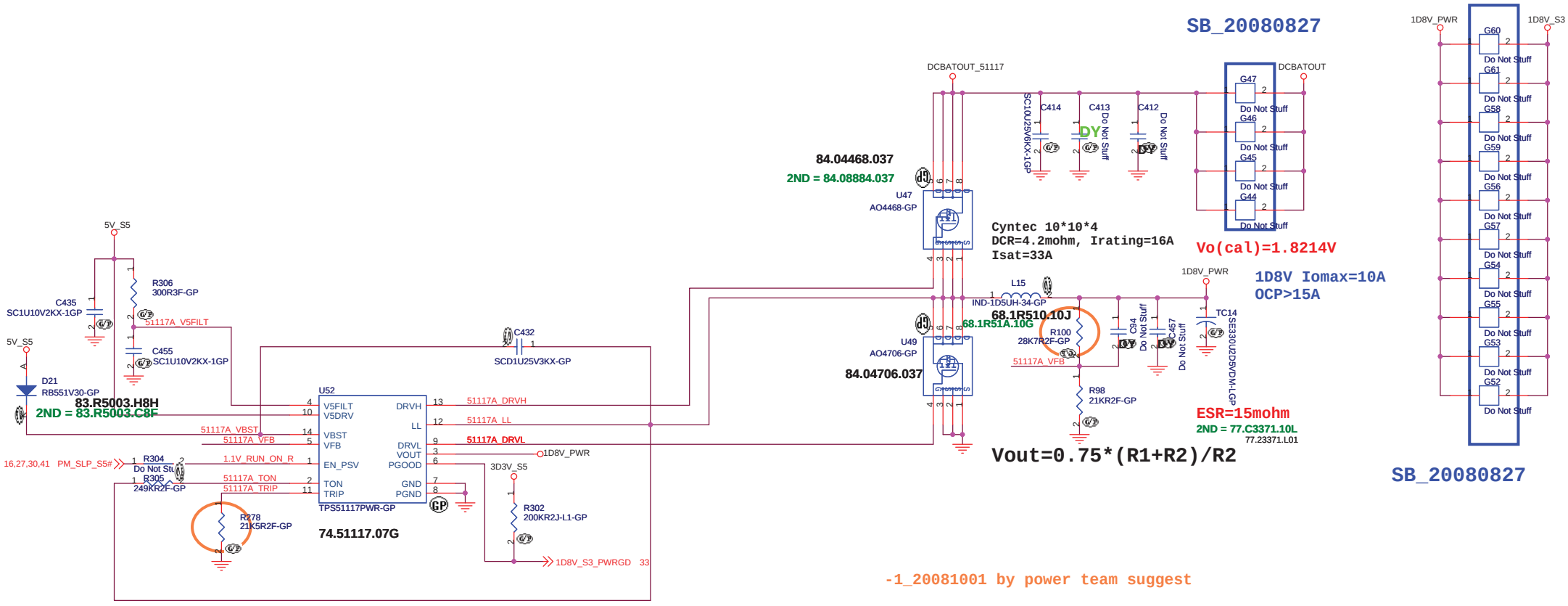


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2



MP

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Title: 1D8V(TPS5117)		
Size: A3	Document Number: F7-GT	Rev: -1
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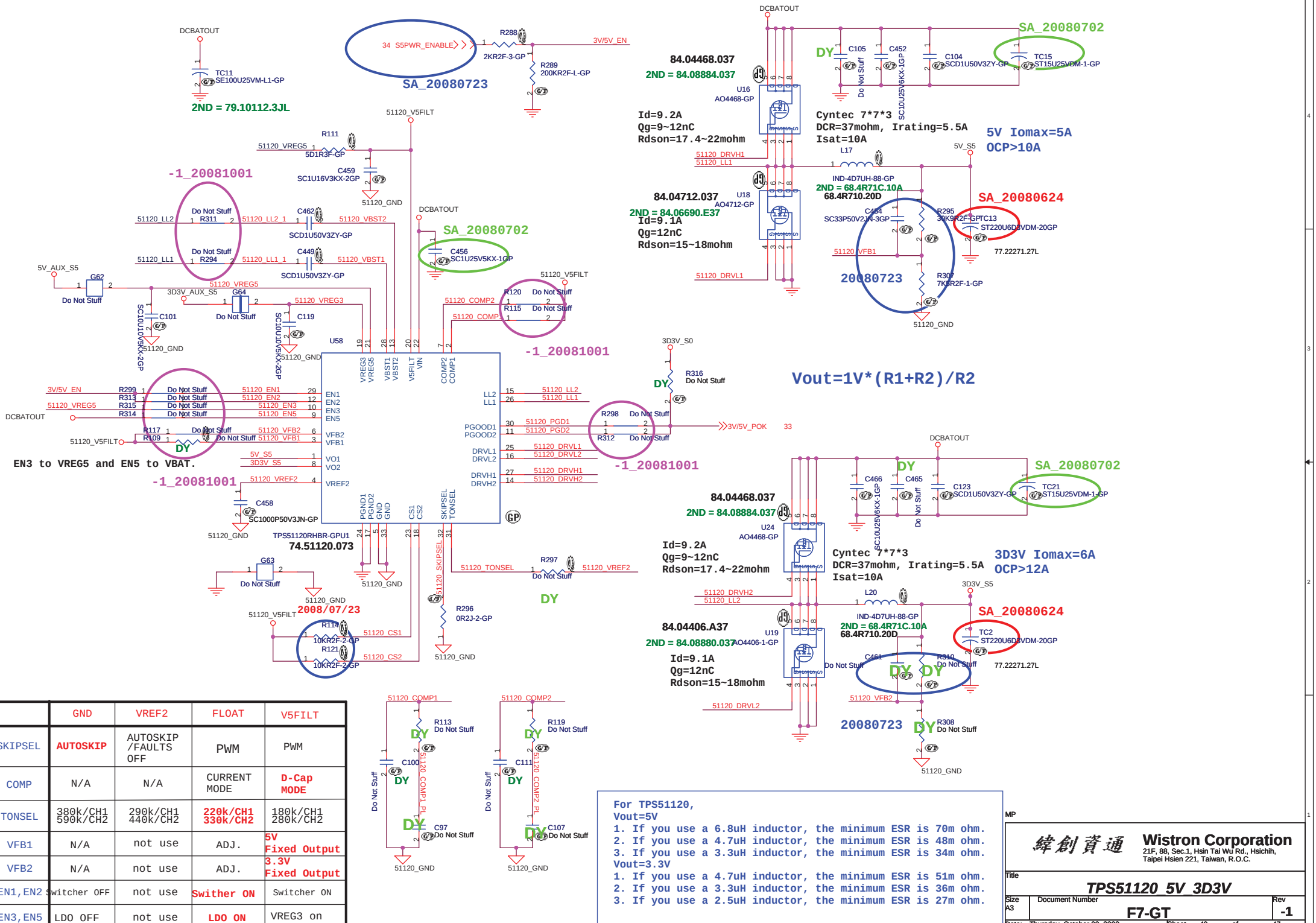

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swither ON**	Switcher ON
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

MP

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51120_5V_3D3V**

Size: A3 | Document Number: **F7-GT** | Rev: **-1**

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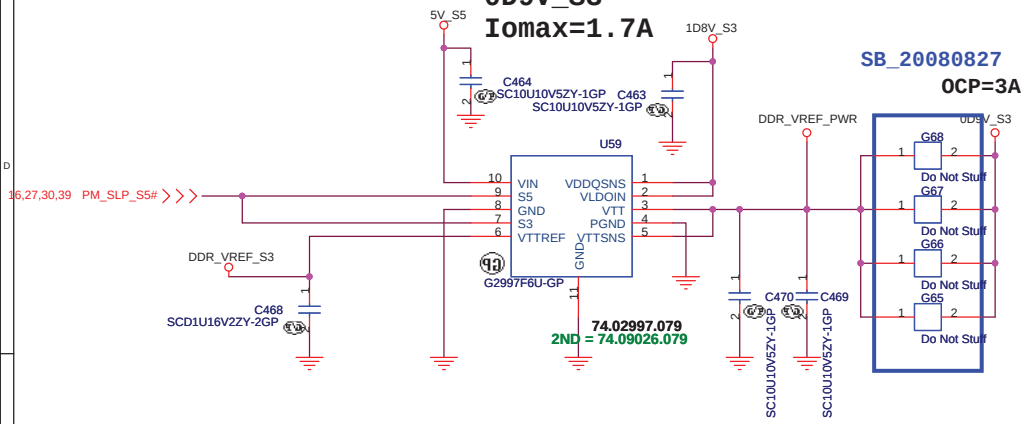
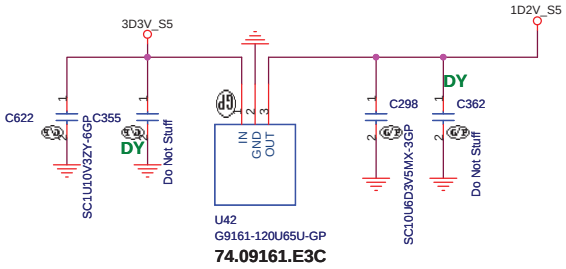
0D9V_S3
Iomax=1.7A



SB_20080827

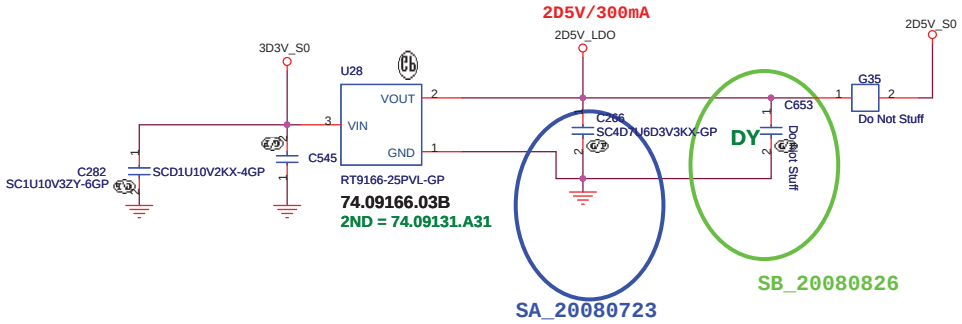
OCP=3A

1D2V_S5 for SB
Iomax=400mA



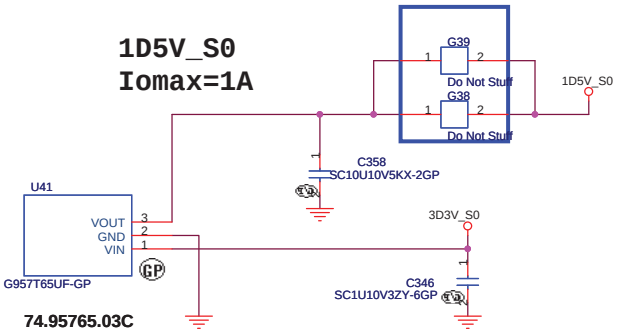
Place near to SB700

2D5V_S0 for CPU
Iomax=0.3A



SB_20080827

1D5V_S0
Iomax=1A



MP

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *2D5V/1D5V/0D9V*		
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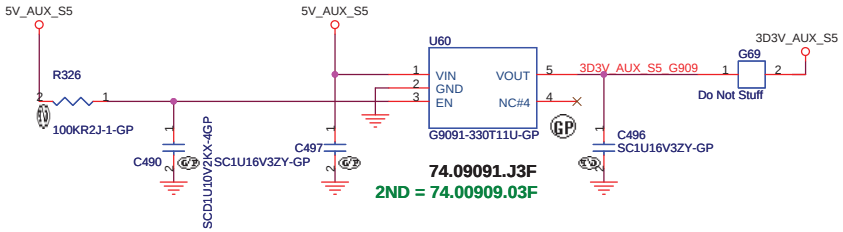
Aux Power 3D3V_AUX_S5



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緯創資通 **Wistron Corporation**
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Title		
3D3V_AUX		
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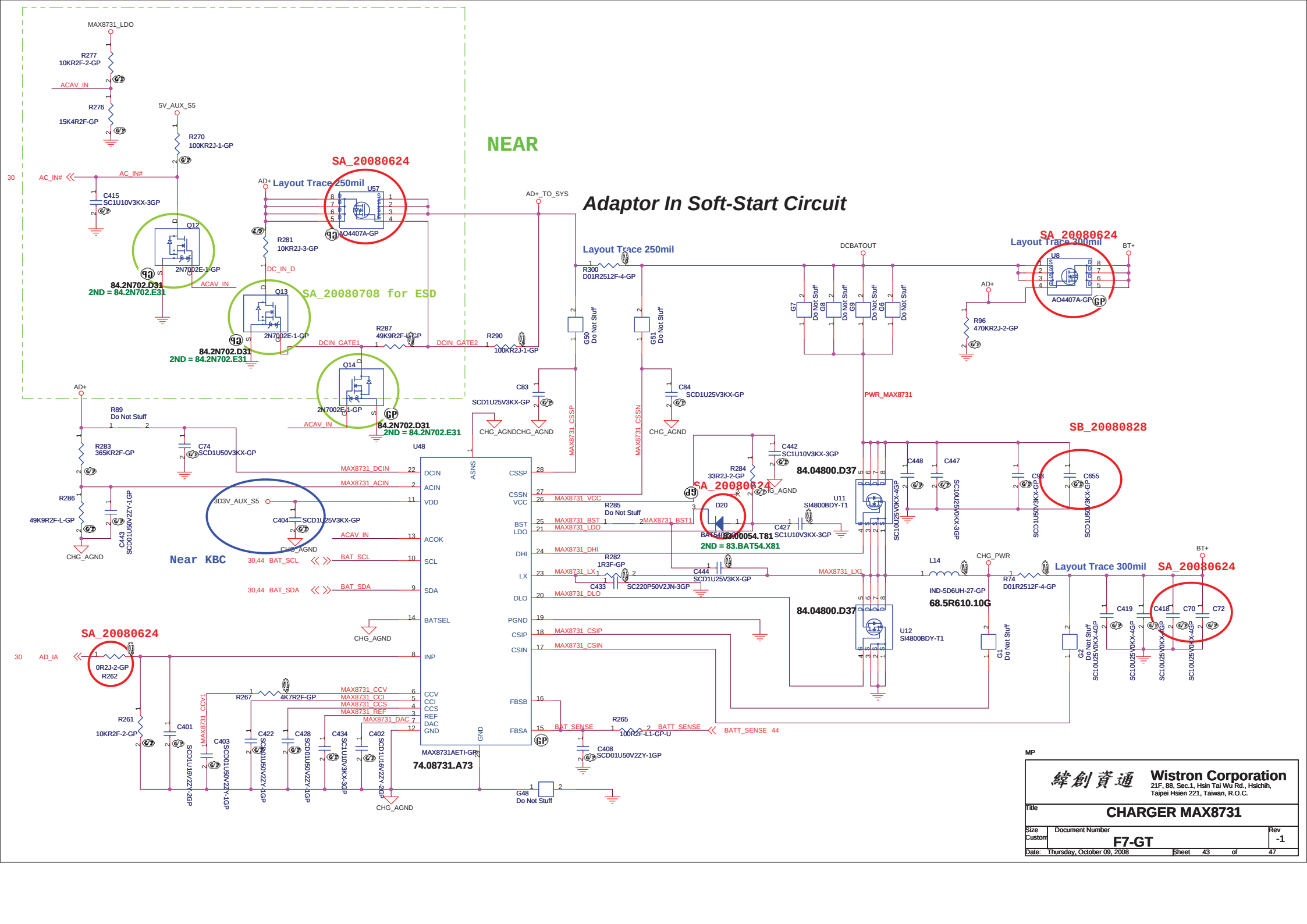
NEAR
Adaptor In Soft-Start Circuit
SA_20080624
SA_20080708 for ESD
SB_20080828
Near KBC
Layout Trace 250mil
Layout Trace 300mil
MAX8731_LDO
ACAV_IN
5V_AUX_S5
AC_IN#
AD+
AD+_TO_SYS
DCBATOUT
BT+
PWR_MAX8731
CHG_PWR
DC_IN_D
DCIN_GATE1
DCIN_GATE2
MAX8731AETI-GP
74.08731.A73
84.2N702.D31
2ND = 84.2N702.E31
84.04800.D37
2ND = 83.BAT54.X81
68.5R610.10G
MP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER MAX8731
Size
Custom
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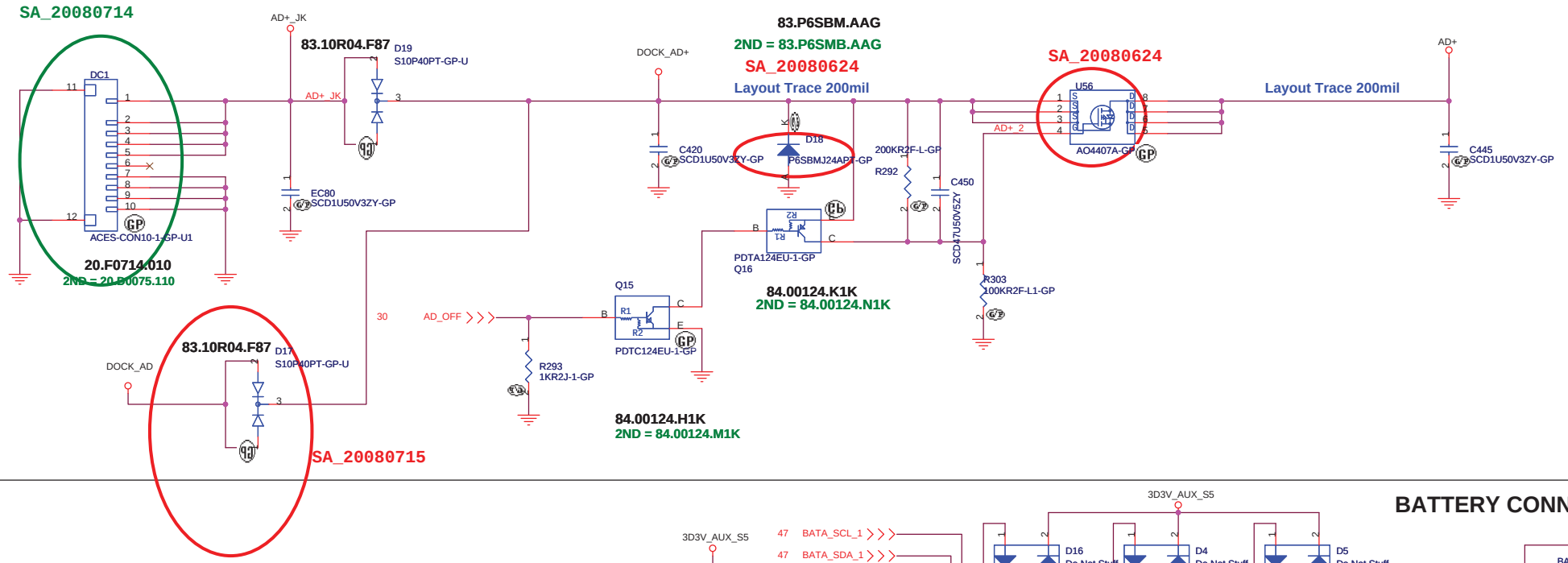
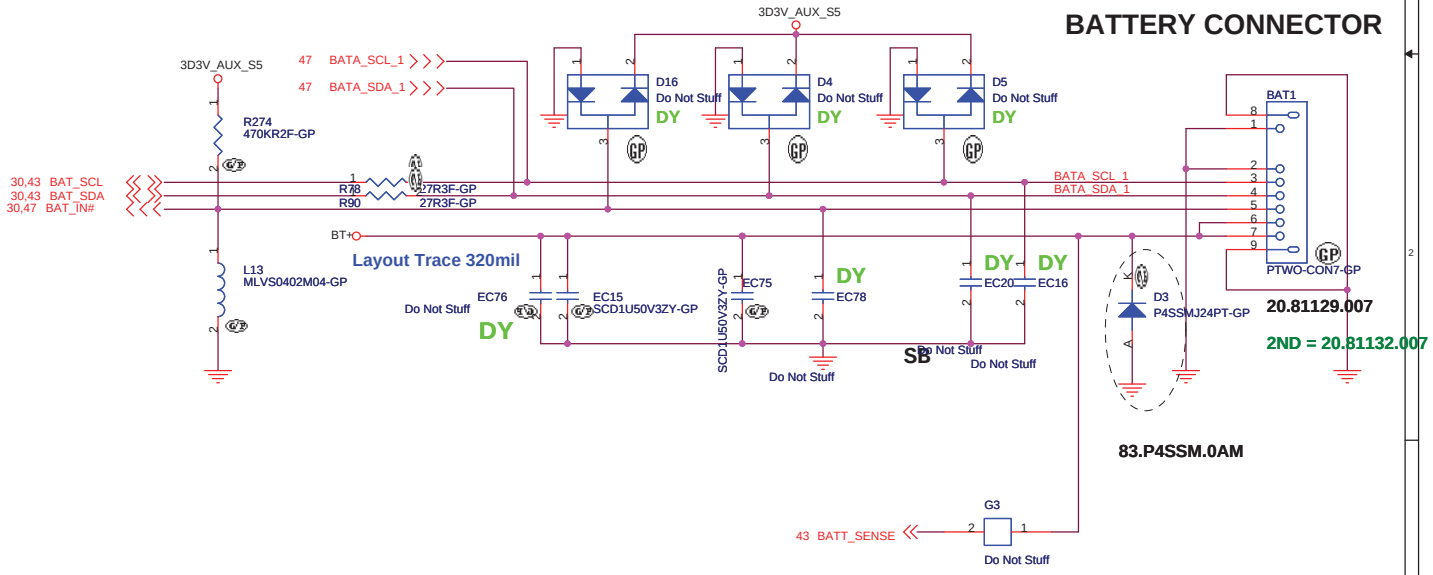
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



MP

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**AD/BATT CONN**
Size: A3	Document Number: **F7-GT**
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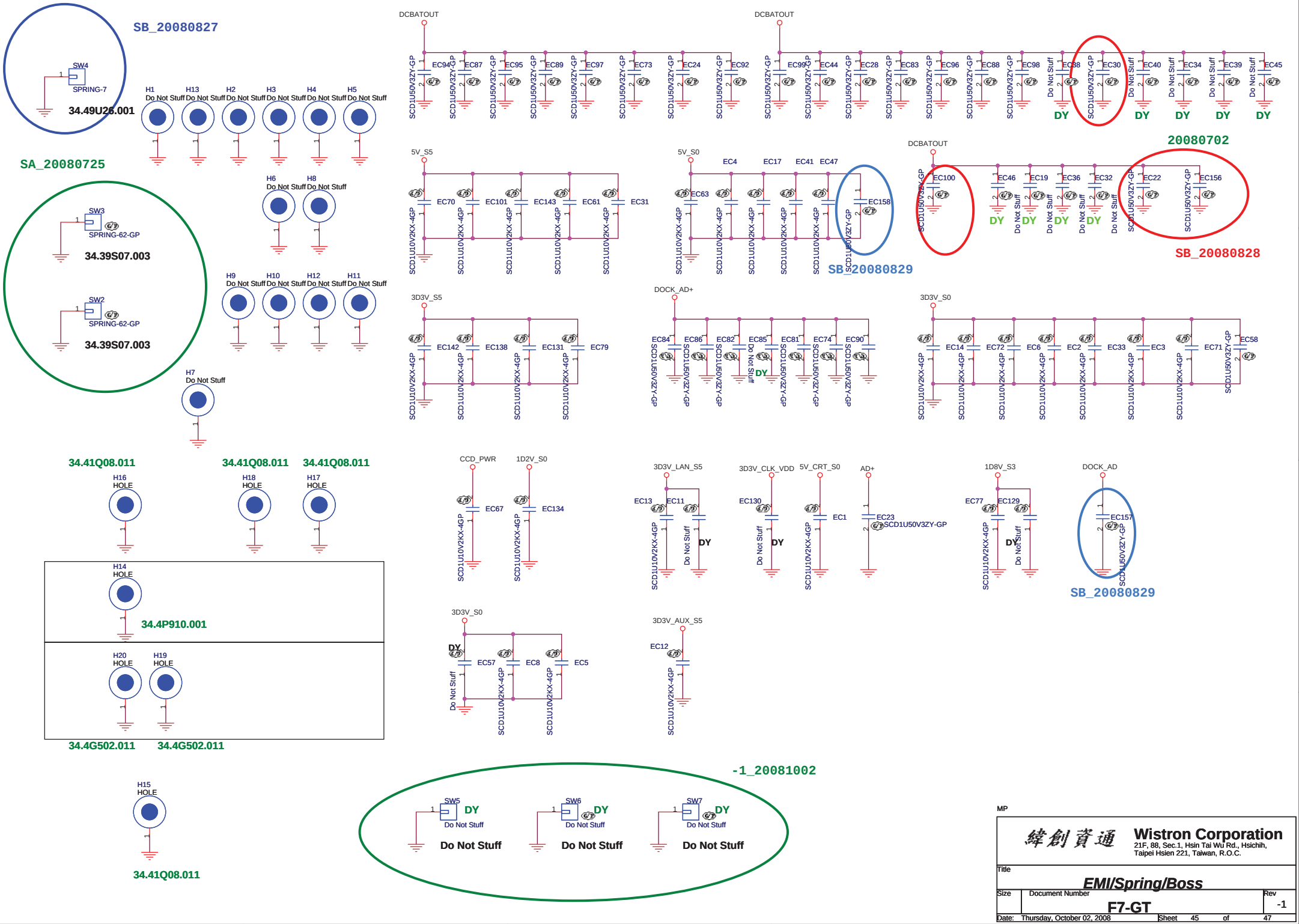

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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI/Spring/Boss**

Size	Document Number	Rev
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MP

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Change List

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CCD Test Point

	CCD_PWR	1	TP7	Do Not Stuff
13	USB_8+	1	5	Do Not Stuff
13	USB_8-	1	TP6	Do Not Stuff

RTC1 CN Test Point

	RTC_AUX_S5	1	TP154	Do Not Stuff

ODD1 Conn. Test Point

17,20	SATA_TXP1	1	TP178	Do Not Stuff
17,20	SATA_TXN1	1	TP177	Do Not Stuff
17,20	SATA_RXN1	1	TP176	Do Not Stuff
17,20	SATA_RXP1	1	TP174	Do Not Stuff
	5V_S0	1	TP4	Do Not Stuff
	5V_S0	1	TP3	Do Not Stuff
20	ODD_DP	1	TP171	Do Not Stuff
20	ODD_MD	1	TP160	Do Not Stuff

HDD Conn. Test Point

17,20	SATA_TXP0	1	123	Do Not Stuff
17,20	SATA_TXN0	1	TP125	Do Not Stuff
17,20	SATA_RXN0	1	139	Do Not Stuff
17,20	SATA_RXP0	1	TP151	Do Not Stuff
	5V_S0	1	175	Do Not Stuff
	3D3V_S0	1	TP156	Do Not Stuff

FAN1 Conn. Test Point

34	FAN1_FG1	1	TP10	Do Not Stuff
	FAN1_VCC	1	TP8	Do Not Stuff

CARD1 Conn. Test Point

31	3D3V_S0_CARD	1	28	Do Not Stuff
16,31	USBPN1	1	29	Do Not Stuff
16,31	USBPP1	1	TP33	Do Not Stuff

BT Conn. Test Point

21	USBPN5-	1	TP187	Do Not Stuff
21	USBPN5+	1	TP186	Do Not Stuff
21	3D3V_BT_S0	1	TP185	Do Not Stuff

USB Conn2. Test Point

21	5V_USB1_S5	1	72	Do Not Stuff
21	USB_0-	1	78	Do Not Stuff
21	USB_0+	1	81	Do Not Stuff
21	USB_2-	1	84	Do Not Stuff
21	USB_2+	1	TP88	Do Not Stuff

USB Conn1. Test Point

21	5V_USB2_S5	1	39	Do Not Stuff
21	USB_4-	1	38	Do Not Stuff
21	USB_4+	1	TP30	Do Not Stuff

KB Conn1. Test Point

30,31	KROW1	1	79	Do Not Stuff
30,31	KROW2	1	80	Do Not Stuff
30,31	KROW3	1	75	Do Not Stuff
30,31	KROW4	1	76	Do Not Stuff
30,31	KROW5	1	73	Do Not Stuff
30,31	KROW6	1	74	Do Not Stuff
30,31	KROW7	1	TP70	Do Not Stuff
30,31	KROW8	1	71	Do Not Stuff
30,31	KCOL1	1	68	Do Not Stuff
30,31	KCOL2	1	69	Do Not Stuff
30,31	KCOL3	1	TP64	Do Not Stuff
30,31	KCOL4	1	65	Do Not Stuff
30,31	KCOL5	1	61	Do Not Stuff
30,31	KCOL6	1	62	Do Not Stuff
30,31	KCOL7	1	57	Do Not Stuff
30,31	KCOL8	1	58	Do Not Stuff
30,31	KCOL9	1	55	Do Not Stuff
30,31	KCOL10	1	56	Do Not Stuff
30,31	KCOL11	1	TP52	Do Not Stuff
30,31	KCOL12	1	53	Do Not Stuff
30,31	KCOL13	1	48	Do Not Stuff
30,31	KCOL14	1	49	Do Not Stuff
30,31	KCOL15	1	43	Do Not Stuff
30,31	KCOL16	1	TP44	Do Not Stuff

TPAD1 Conn. Test Point

	3D3V_S0	1	107	Do Not Stuff
	3D3V_S5	1	TP108	Do Not Stuff
31	TP_DATA_1	1	98	Do Not Stuff
	5V_S0	1	99	Do Not Stuff
31	TP_CLK_1	1	100	Do Not Stuff
30,31	FRONT_PWRLED_BD	1	101	Do Not Stuff
30,31	STDBY_LED	1	97	Do Not Stuff
30,31	DC_BATFULL	1	TP102	Do Not Stuff
30,31	CHARGE_LED	1	103	Do Not Stuff
30,31	BT_LED	1	104	Do Not Stuff
27,31	WLAN_LED#	1	105	Do Not Stuff
31	USB_6+	1	111	Do Not Stuff
31	USB_6-	1	TP112	Do Not Stuff

SWITCH Conn. Test Point

	5V_S0	1	42	Do Not Stuff
	3D3V_S0	1	41	Do Not Stuff
31	NUM_LED#_R	1	37	Do Not Stuff
31	CAP_LED#_R	1	TP32	Do Not Stuff
31	SATA_LED#_R	1	31	Do Not Stuff
30,31	SMBD_LAUNCH	1	36	Do Not Stuff
30,31	SMBC_LAUNCH	1	35	Do Not Stuff
30,31	CAPA_INT#	1	TP34	Do Not Stuff

SPKR1 Conn. Test Point

29	SPKR_L-	1	181	Do Not Stuff
29	SPKR_L+	1	180	Do Not Stuff
29	SPKR_R-	1	182	Do Not Stuff
29	SPKR_R+	1	TP183	Do Not Stuff

DC1 Conn. Test Point

	AD+_JK	1	16	Do Not Stuff
	AD+_JK	1	15	Do Not Stuff
	AD+_JK	1	TP14	Do Not Stuff

BAT1 Conn. Test Point

44	BATA_SCL_1	1	24	Do Not Stuff
44	BATA_SDA_1	1	23	Do Not Stuff
30,44	BAT_IN#	1	22	Do Not Stuff
	BT+	1	21	Do Not Stuff
	BT+	1	20	Do Not Stuff
	BT+	1	TP13	Do Not Stuff

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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Change List

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