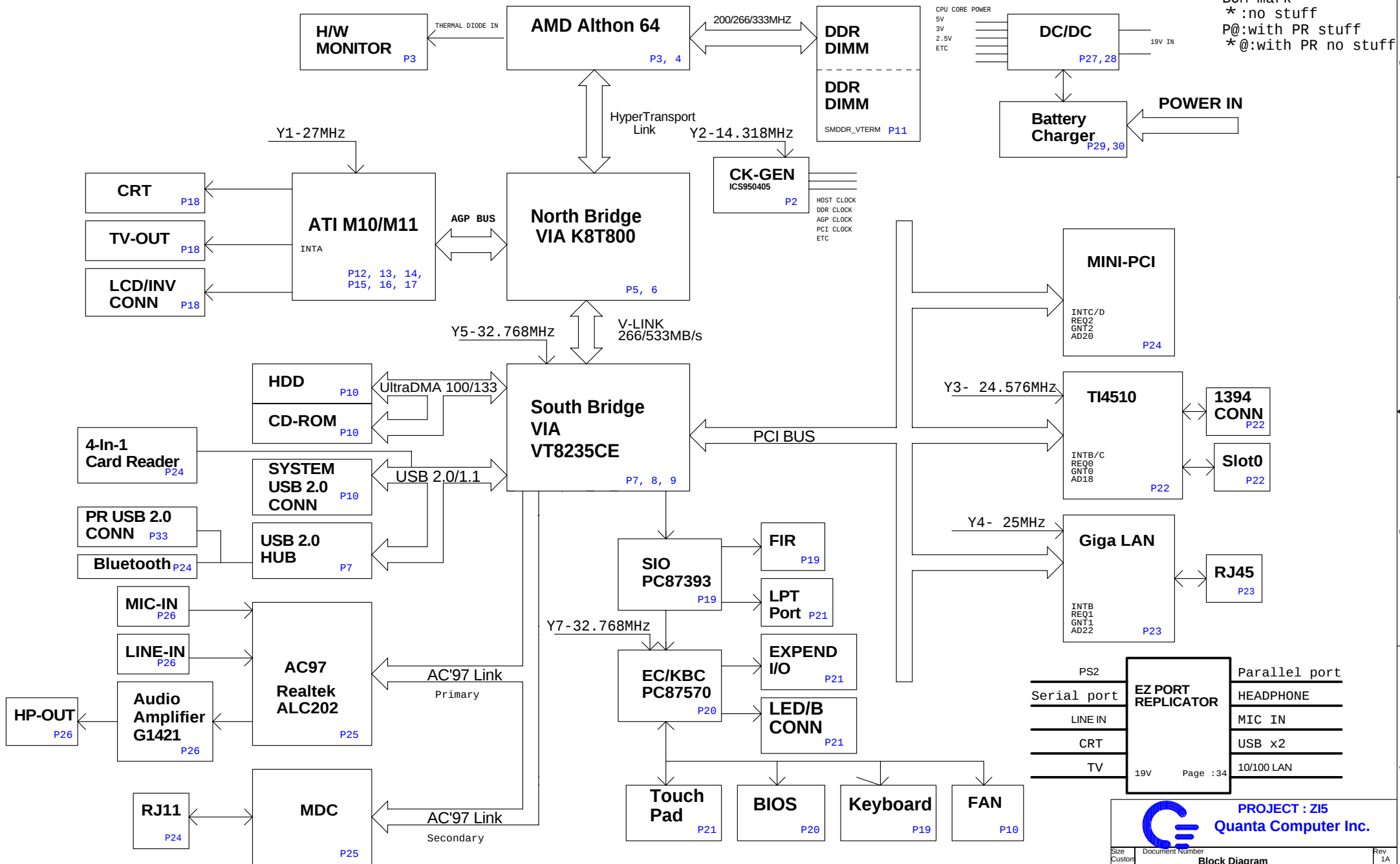
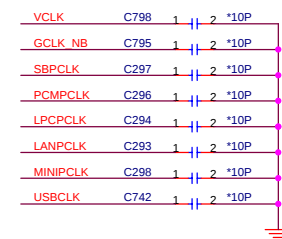
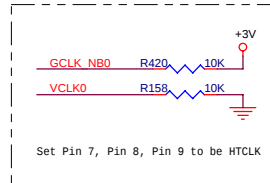
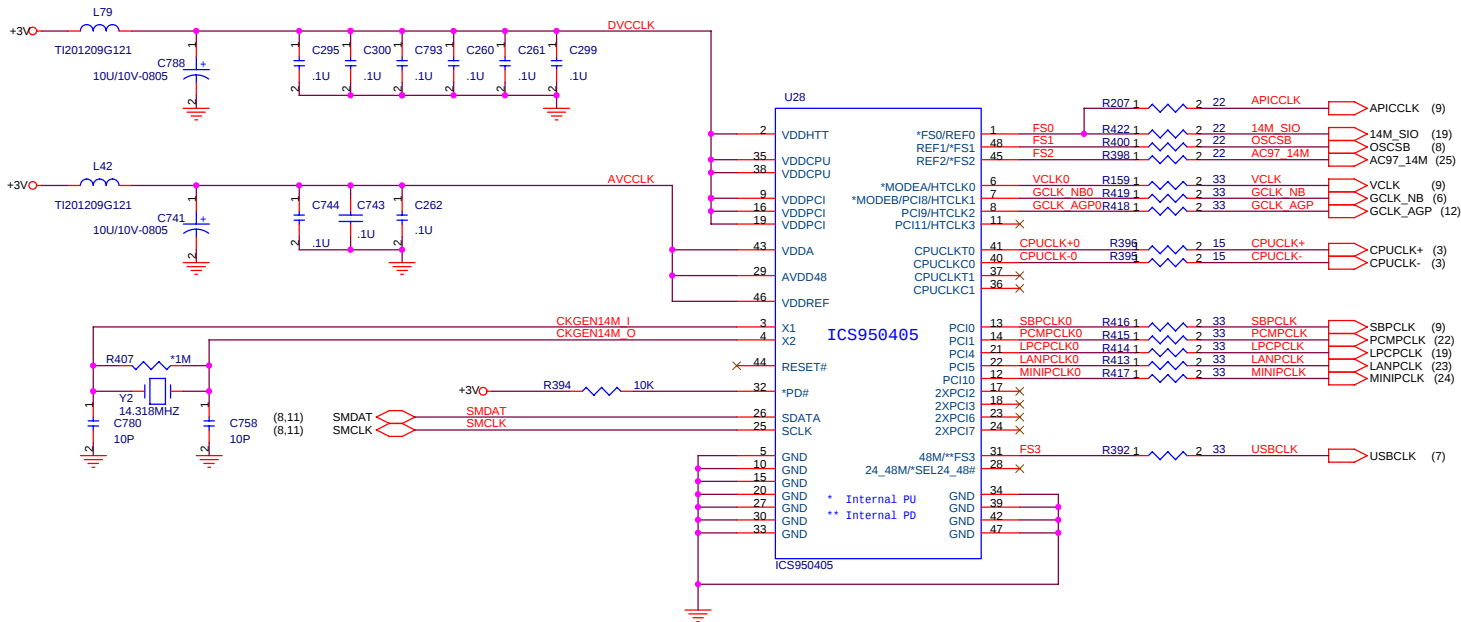
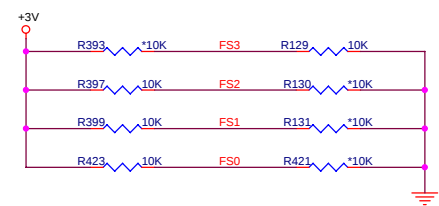


ZI5 SYSTEM BLOCK DIAGRAM

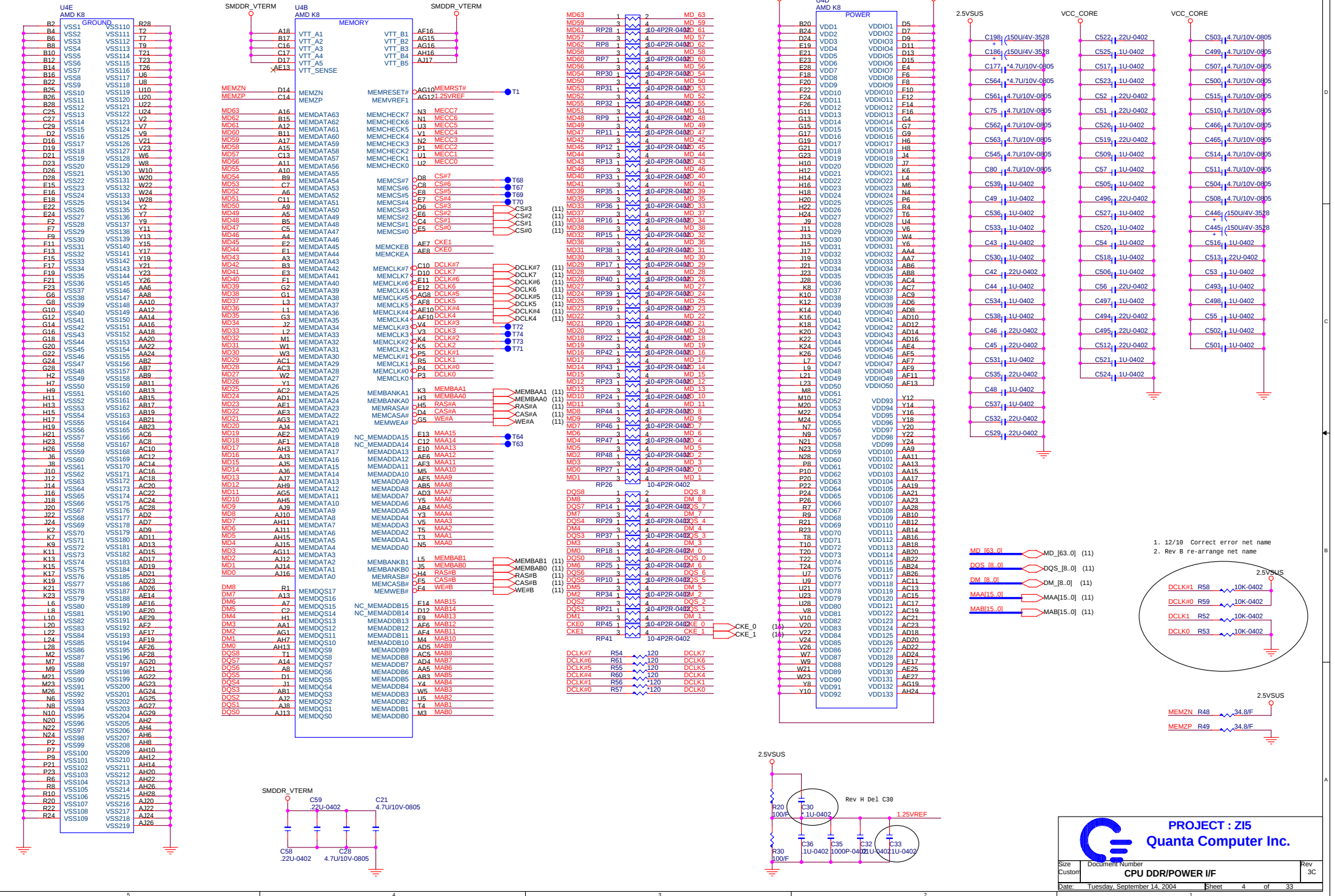


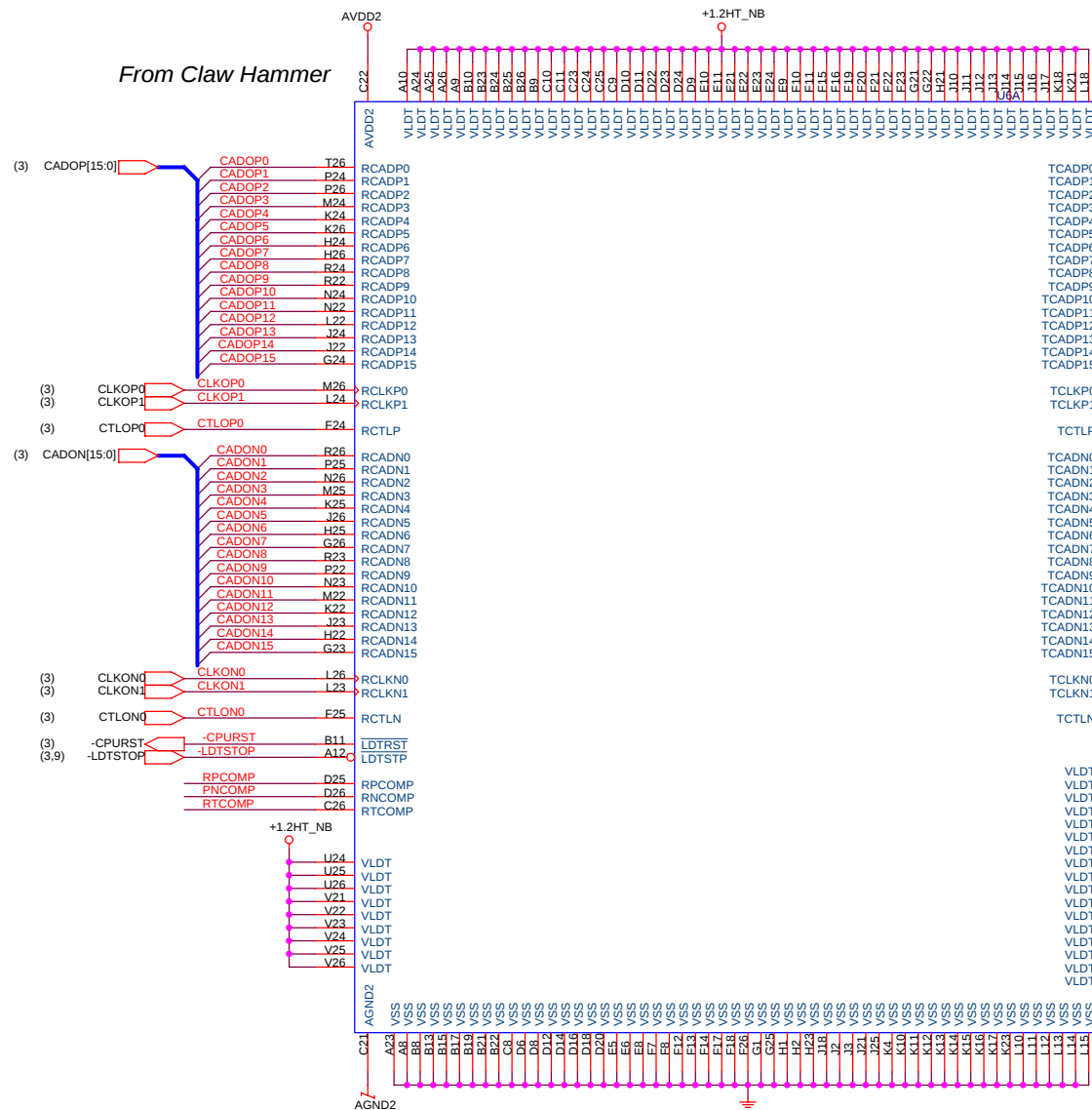


FS3	FS2	FS1	FS0	CPUCLK MHZ	HTT MHZ	PCICLK MHZ
0	0	0	0	100.00	67.27	33.63
0	0	0	1	133.33	89.59	44.88
0	0	1	0	166.67	112.77	56.60
0	0	1	1	200.00	140.00	69.55
0	1	0	0	266.67	177.78	92.77
0	1	0	1	333.33	222.22	116.67
0	1	1	0	400.00	266.67	140.00
0	1	1	1	466.67	311.11	163.33
1	0	0	0	500.00	333.33	177.78
1	0	0	1	600.00	400.00	213.33
1	0	1	0	750.00	500.00	266.67
1	0	1	1	1000.00	666.67	355.56
1	1	0	0	1333.33	888.89	466.67
1	1	0	1	1666.67	1111.11	577.78
1	1	1	0	2000.00	1333.33	694.44
1	1	1	1	2666.67	1777.78	927.78

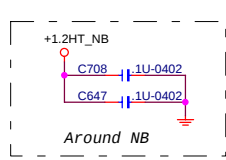
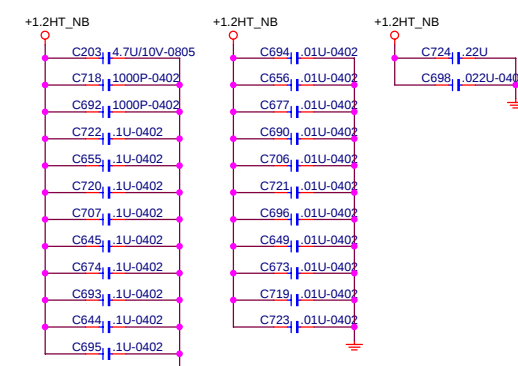
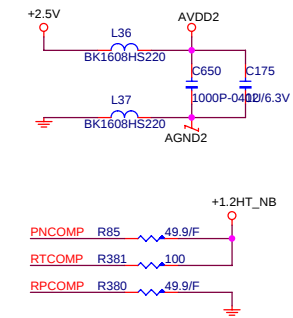
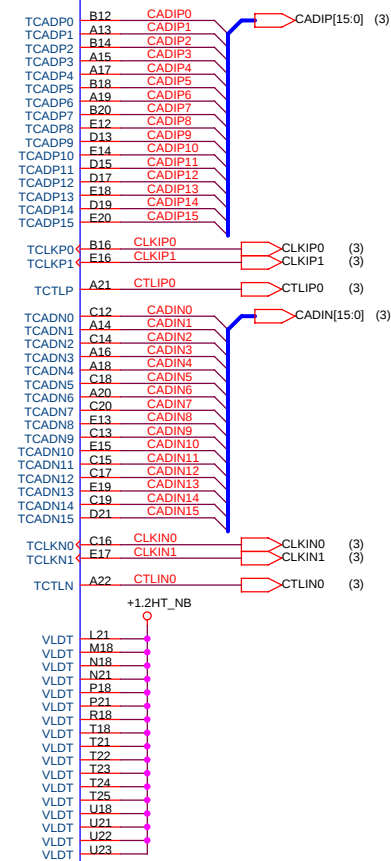


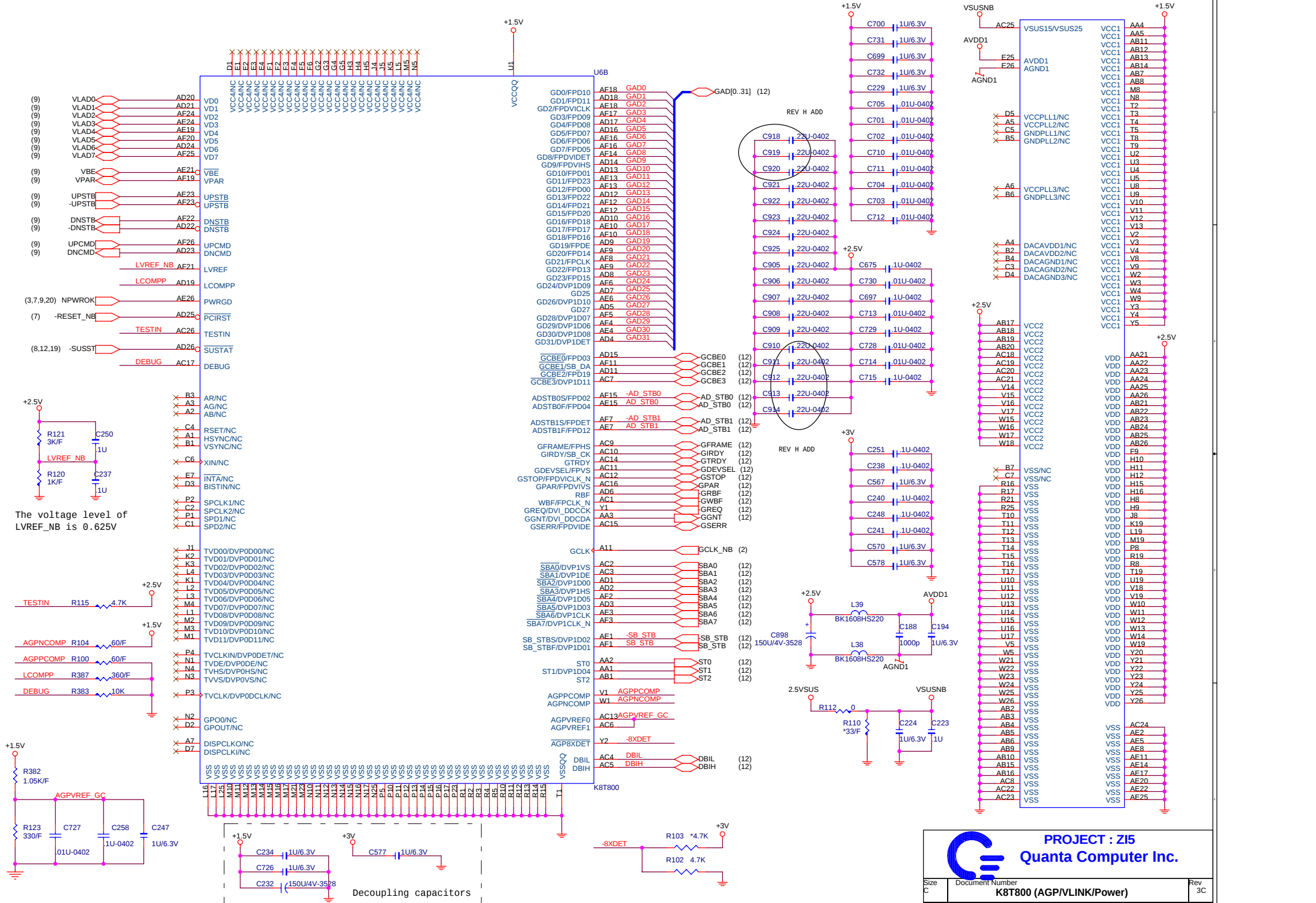
CPU DDR/POWER I/F



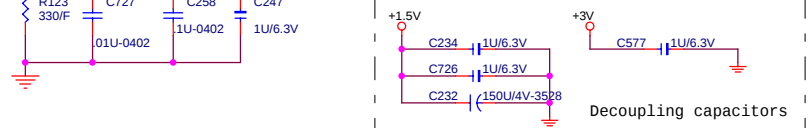


To Claw Hammer





The voltage level of LVREF_NB is 0.625V





PROJECT : Z15
Quanta Computer Inc.

Size C	Document Number K8T800 (AGP/VLINK/Power)	Rev 3C
Date:	Tuesday, September 14, 2004	Sheet 6 of 33

(22,23,24) AD[0..31]

AD0 G2
AD1 J4
AD2 J3
AD3 H3
AD4 F1
AD5 A5
AD6 G1
AD7 E2
AD8 E1
AD9 A8
AD10 G3
AD11 E3
AD12 D1
AD13 G4
AD14 D2
AD15 D3
AD16 F3
AD17 K3
AD18 K2
AD19 K1
AD20 M4
AD21 L2
AD22 N4
AD23 I1
AD24 M2
AD25 M1
AD26 P4
AD27 N3
AD28 N2
AD29 N1
AD30 P1
AD31 P2

(22,23,24) -CBE0
(22,23,24) -CBE1
(22,23,24) -CBE2
(22,23,24) -CBE3

(22,23,24) -FRAME
(22,23,24) -DEVSEL
(22,23,24) -IRDY
(22,23,24) -TRDY
(22,23,24) -STOP
(22,23,24) -SERR
(22,23,24) -PAR
(22,23,24) -PERR

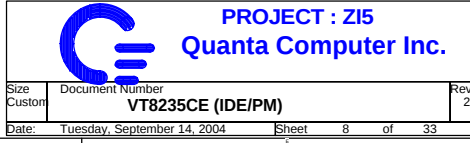
(12) -INTA
(22,23) -INTB
(22,24) -INTC
(24) -INTD

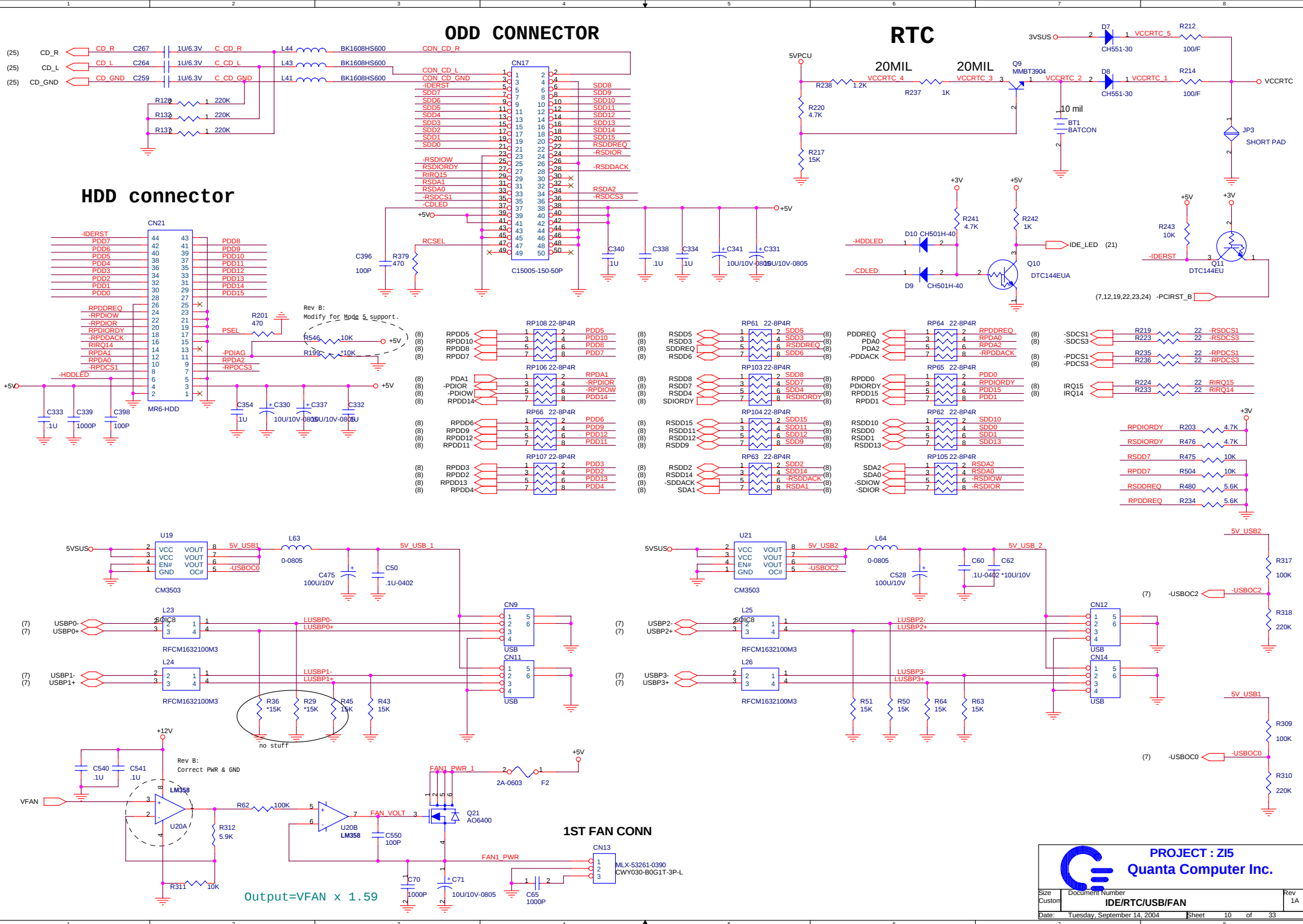
(22) -REQ0
(23) -REQ1
(24) -REQ2

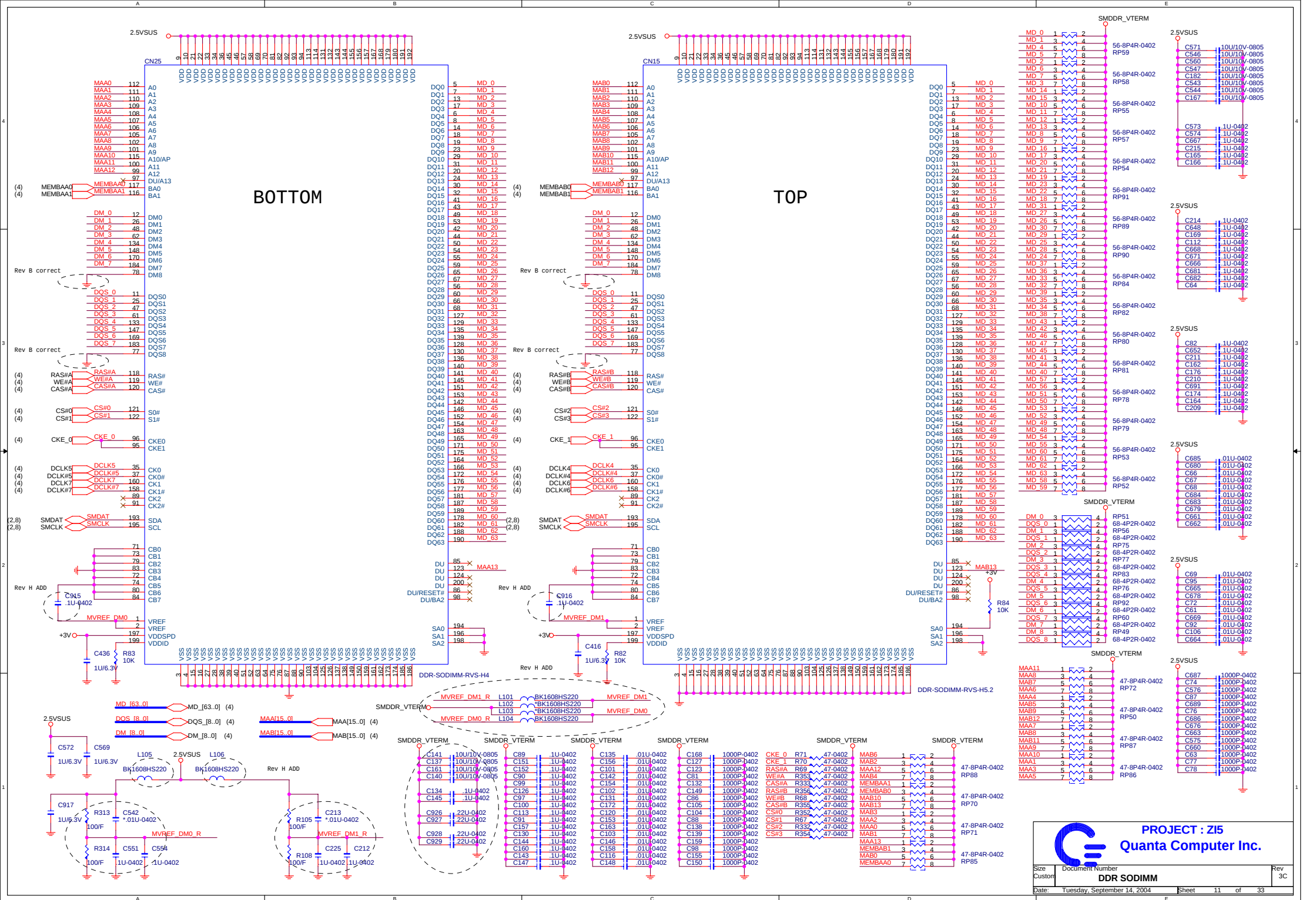
(22) -GNT0
(23) -GNT1
(24) -GNT2

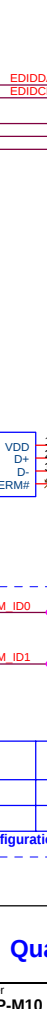
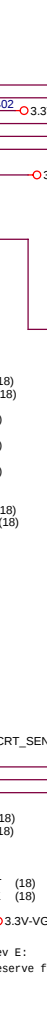
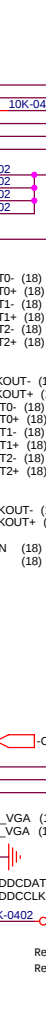
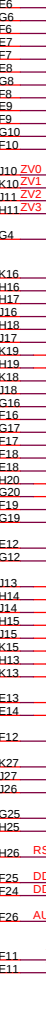
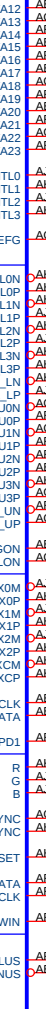
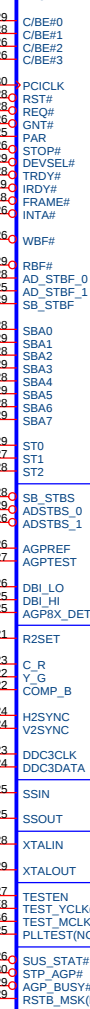
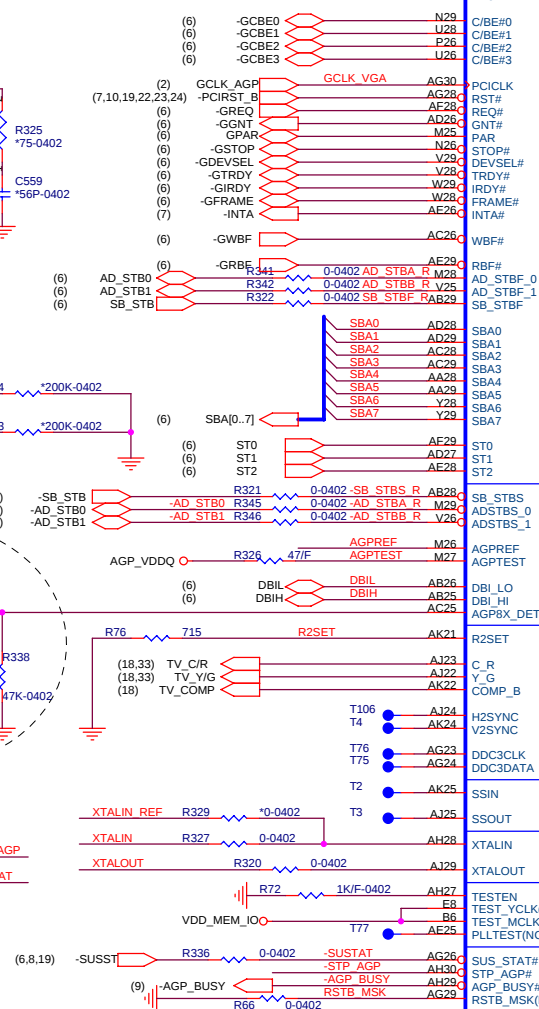
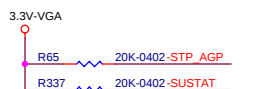
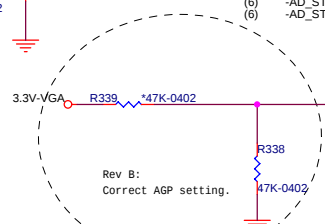
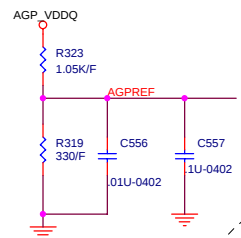
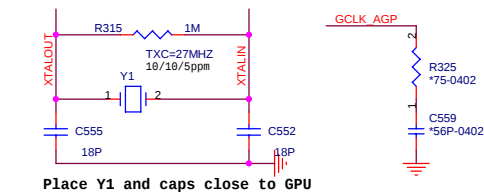
(18) DISPON

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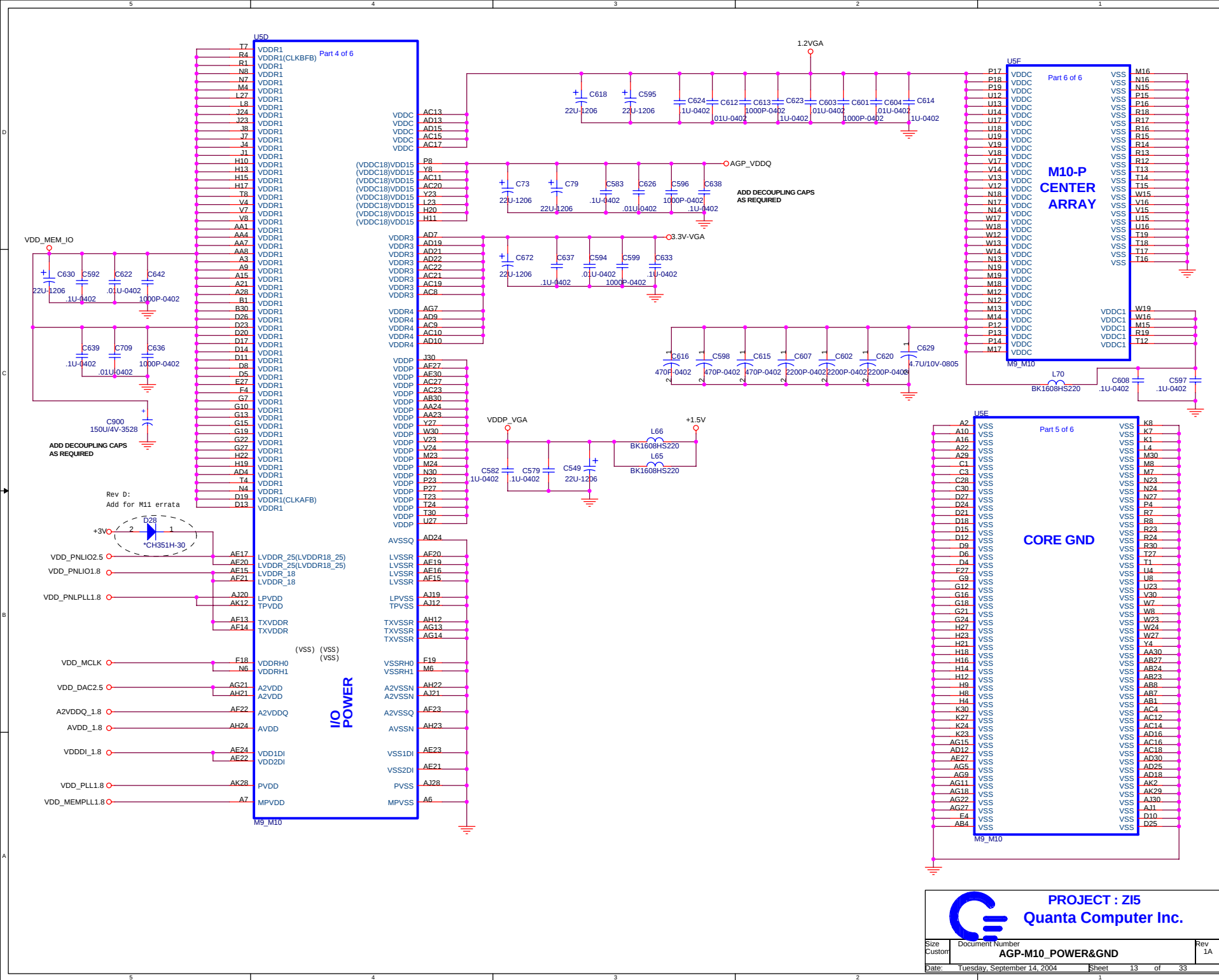




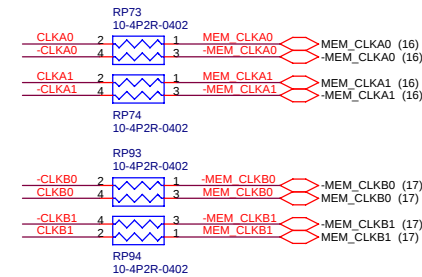
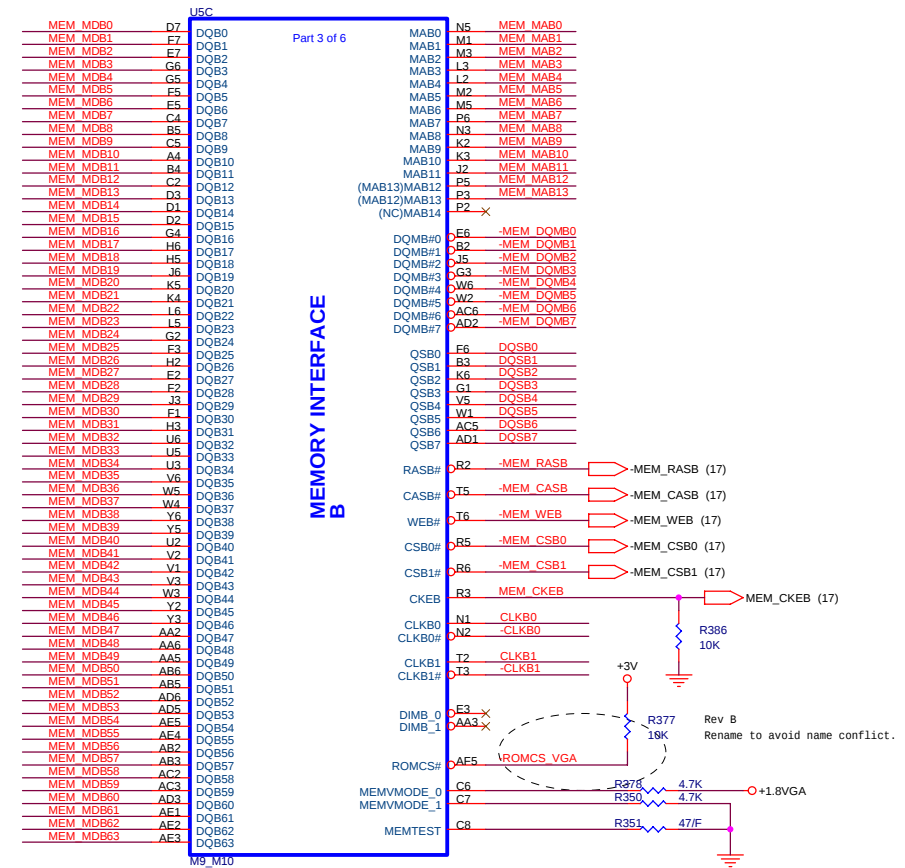


		Hynix 128MB		
ID1		0		
ID0		1		

VRAM configuration

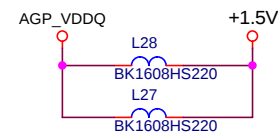
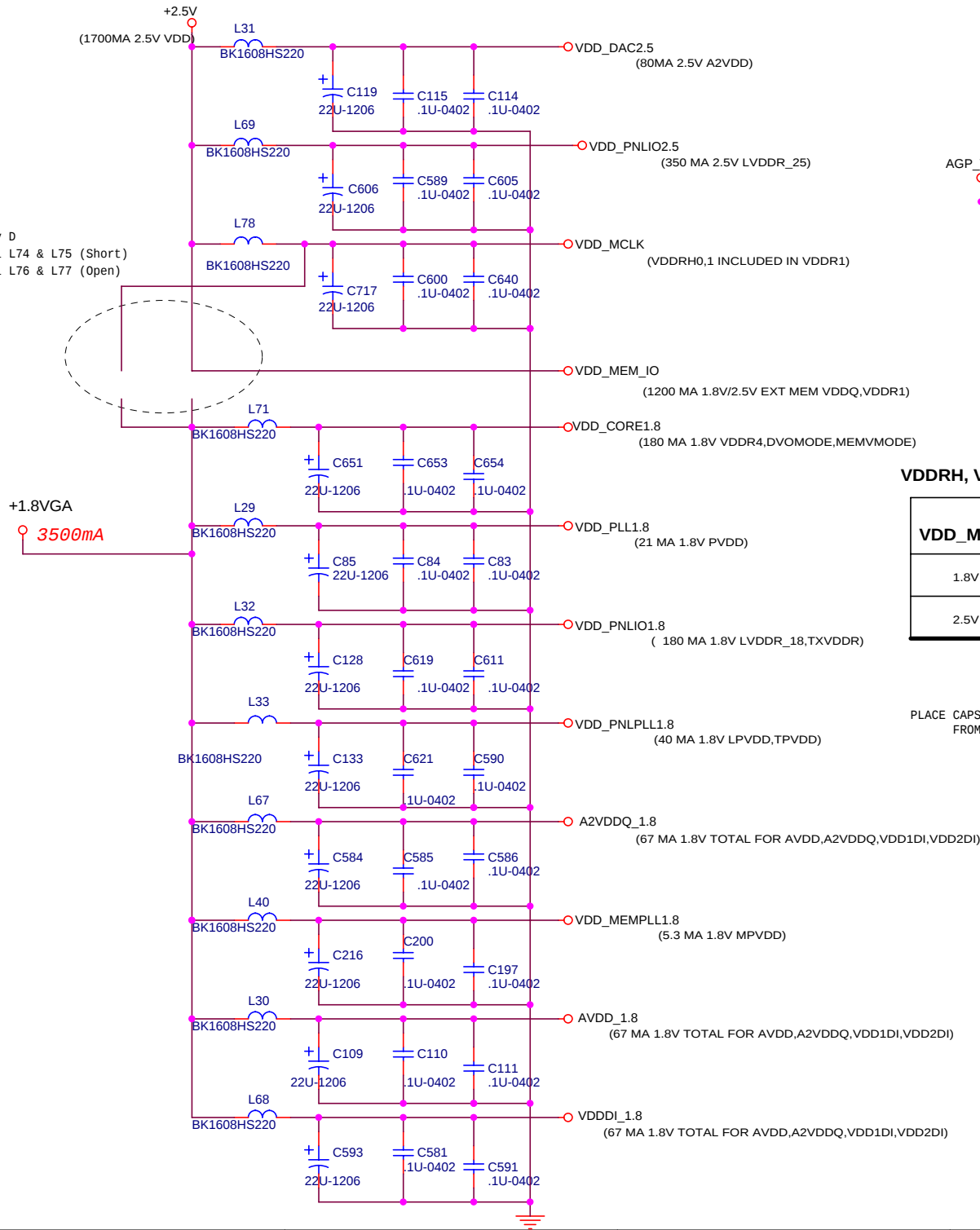


MEMORY CHANNEL B



MEMMODE[1:0]	MEMORY I/O VOLTAGE
0 1	2.5V (DDR)
1 0	1.8V (DDR)
1 1	3.3V (SDR)

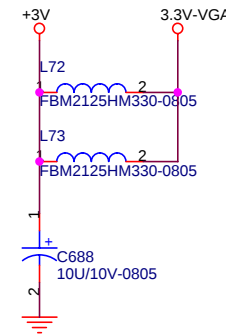
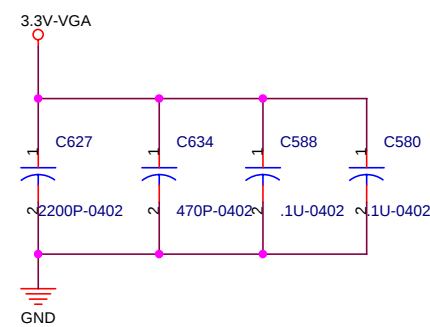
Rev D
Del L74 & L75 (Short)
Del L76 & L77 (Open)



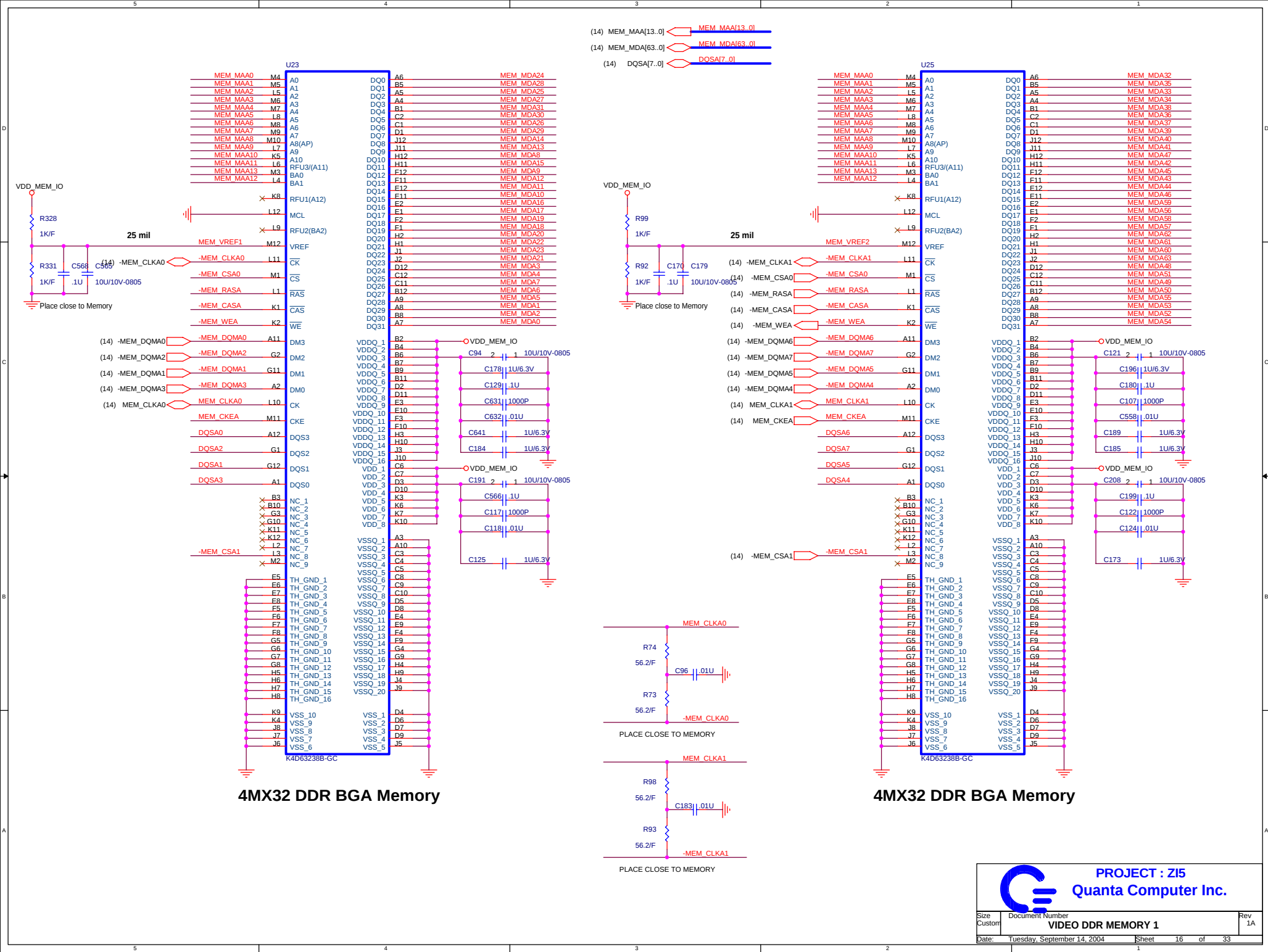
VDDRH, VDDQ AND VDDR1 VOLTAGE SELECTION

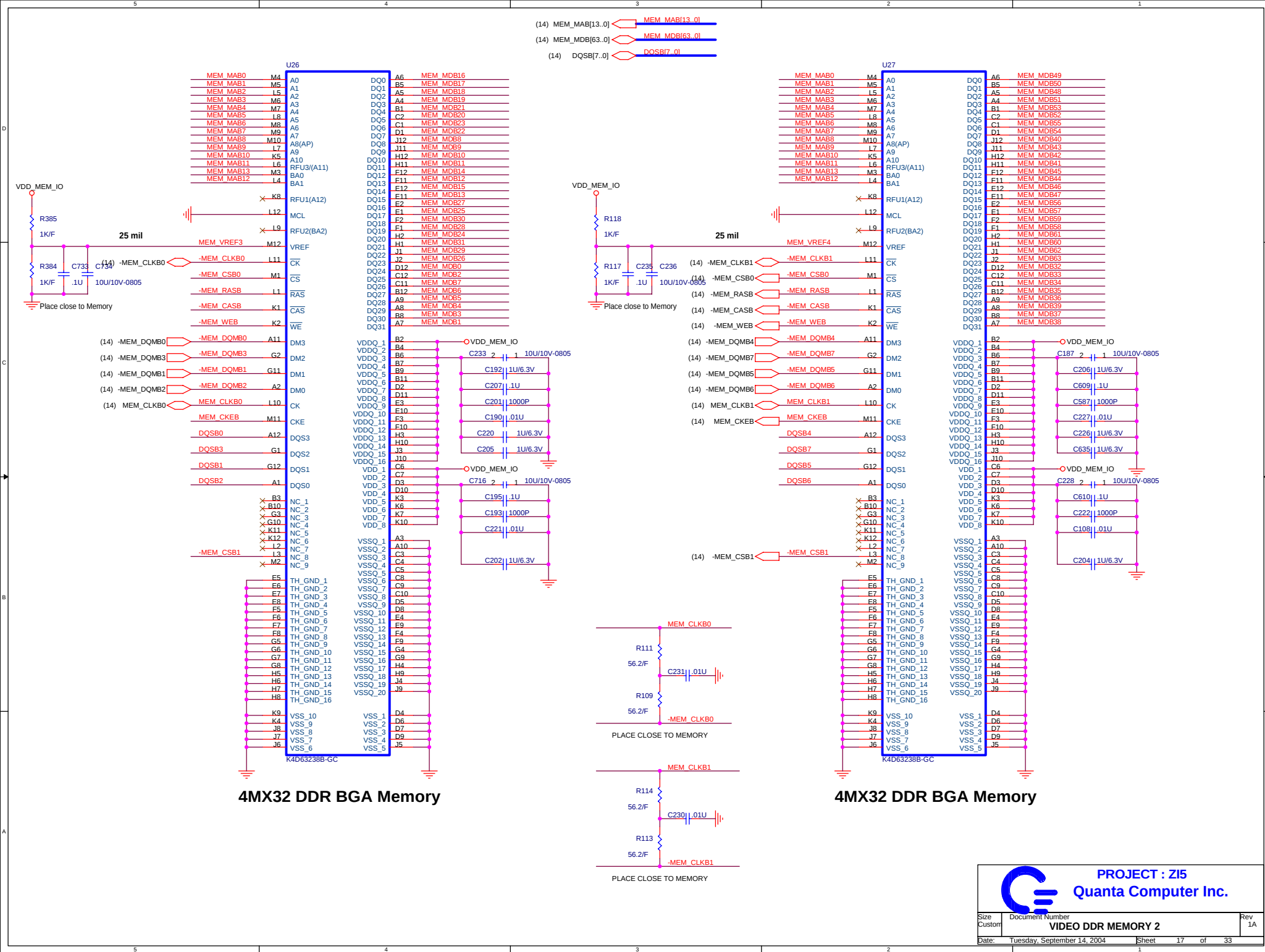
VDD_MEM_IO	FBa	FBb	FBc	FBd
1.8V (ELPIDA)	IN	OUT	OUT	IN
2.5V	OUT	IN	IN	OUT

PLACE CAPS FOR THESE GROUNDS CLOSE TO ASIC AND RUN DEDICATED TRACES FROM PINS THAT JOIN TO GROUND PLANE WITH ONE VIA AT CAP

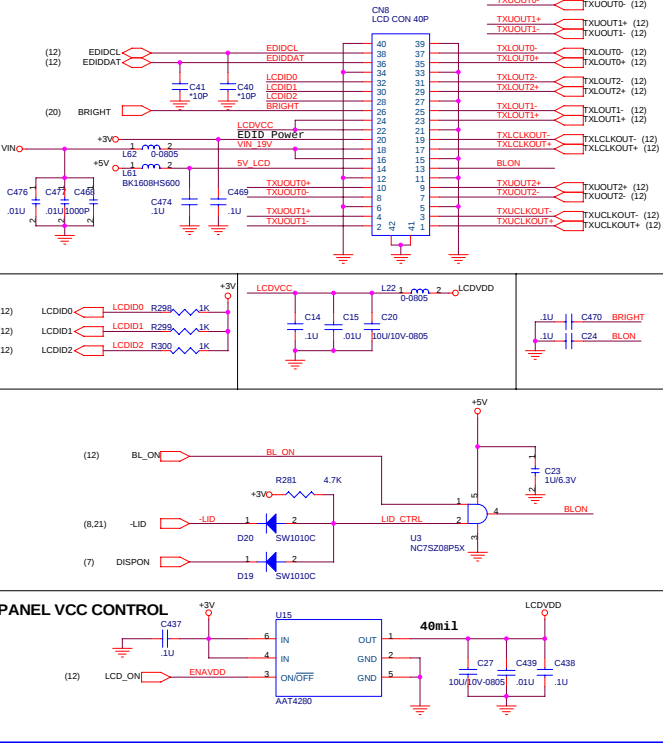


PROJECT : ZI5
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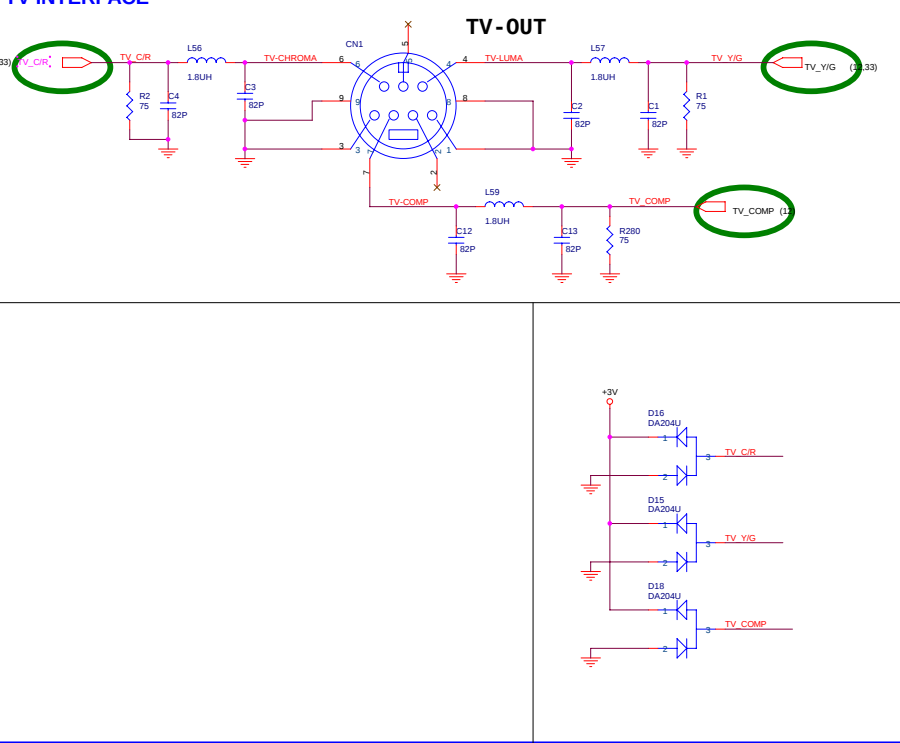




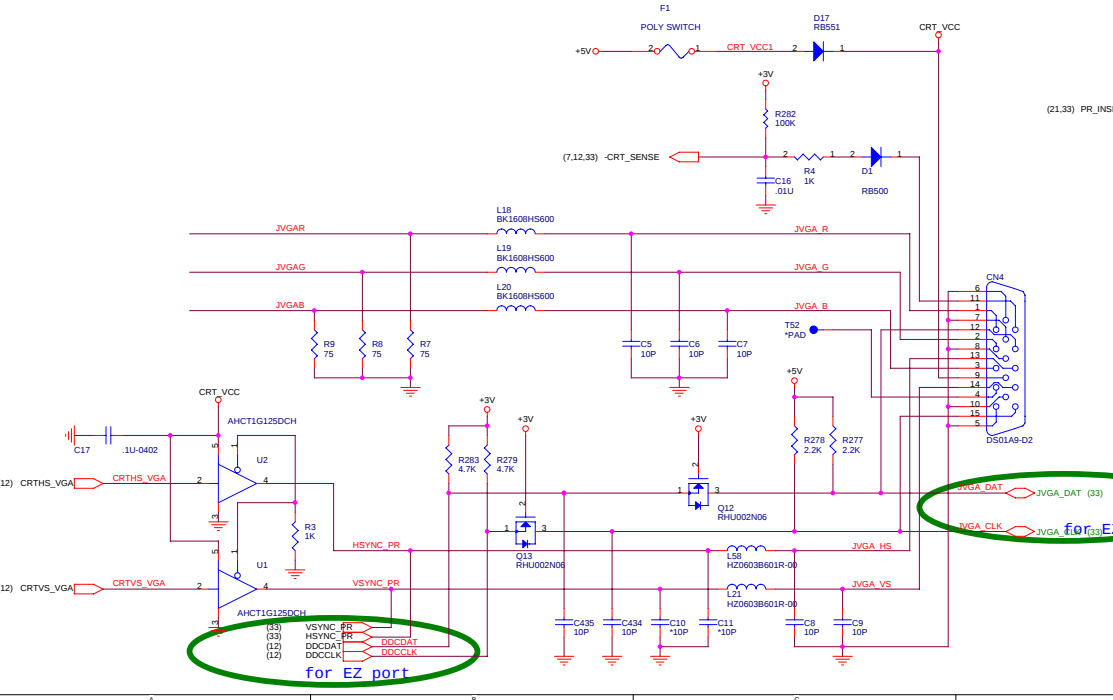
LCD INTERFACE



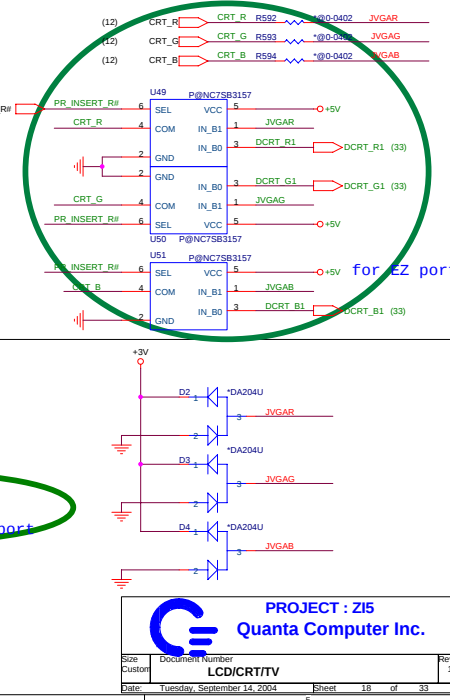
TV INTERFACE

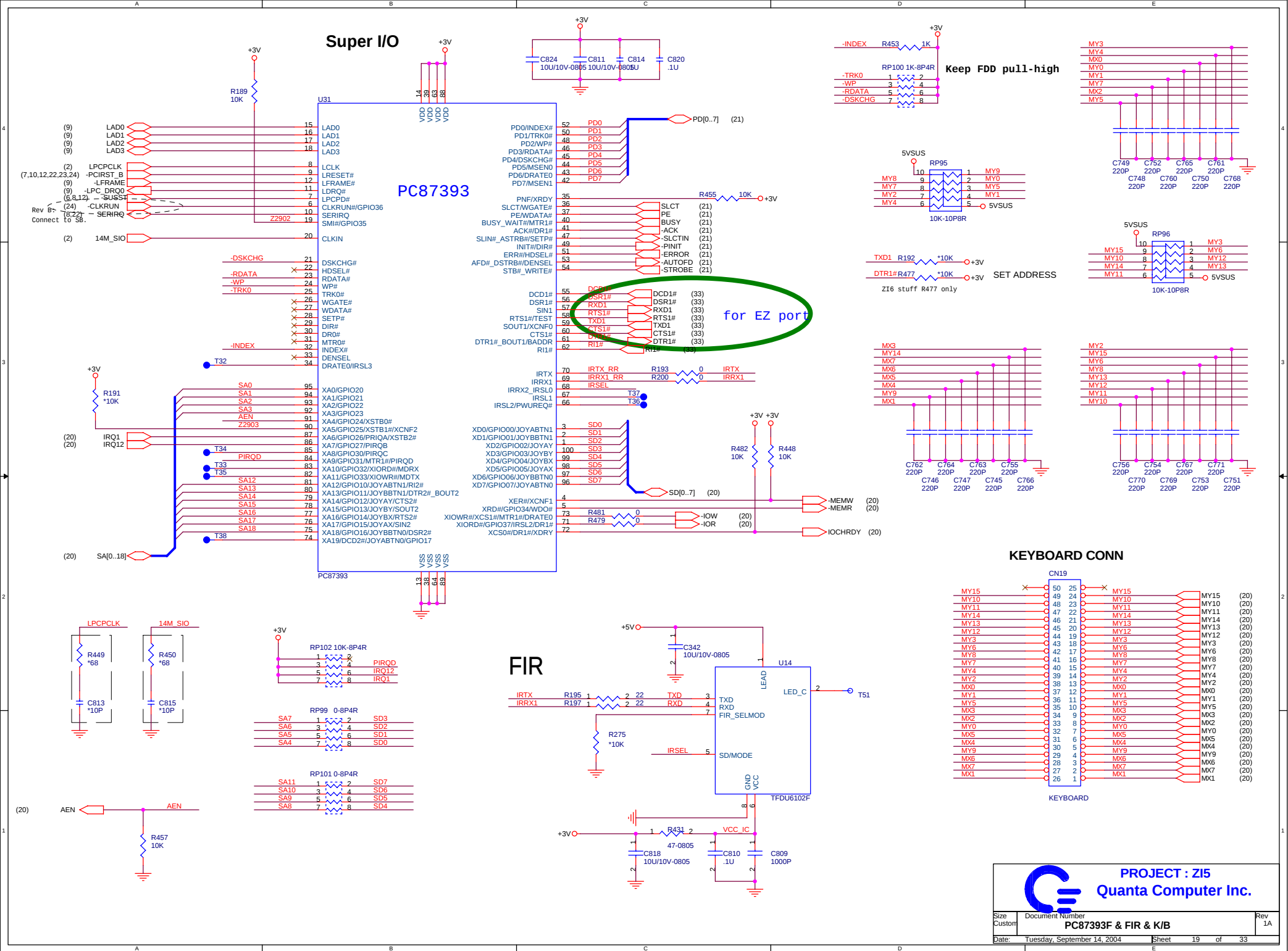


CRT INTERFACE



stuff R for ZI5





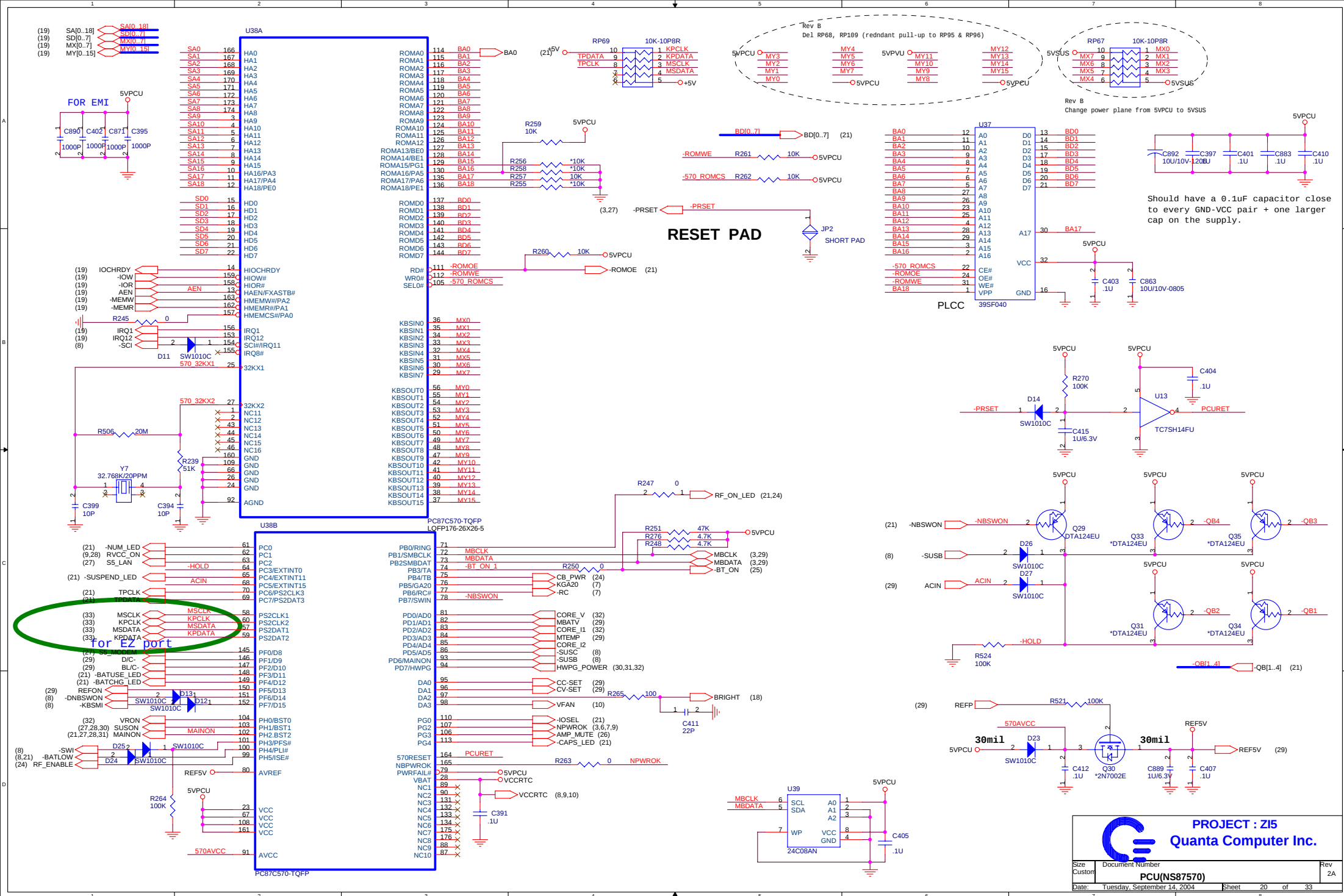


Figure 10 is a detailed schematic of the PE test board. It shows the connection of various components including LEDs (BATCHG_LED, BATUSE_LED, RF_ON_LED, SUSPEND_LED, BATLOW), resistors (R381, R390, R38, R136, R135), capacitors (C277, C278, C266, C265), and a 74VHC04 inverter (U42). It also shows the connection of the ACES-87126-2002 connector (CN18) and the TPDATA/TPCLK signals. The board is powered by +5V and +3V sources. The schematic is labeled "Rev D: Reserve for PE test requirement."

The schematic diagram shows the internal connections of the SN74AHC244PW buffer. Key components and connections include:

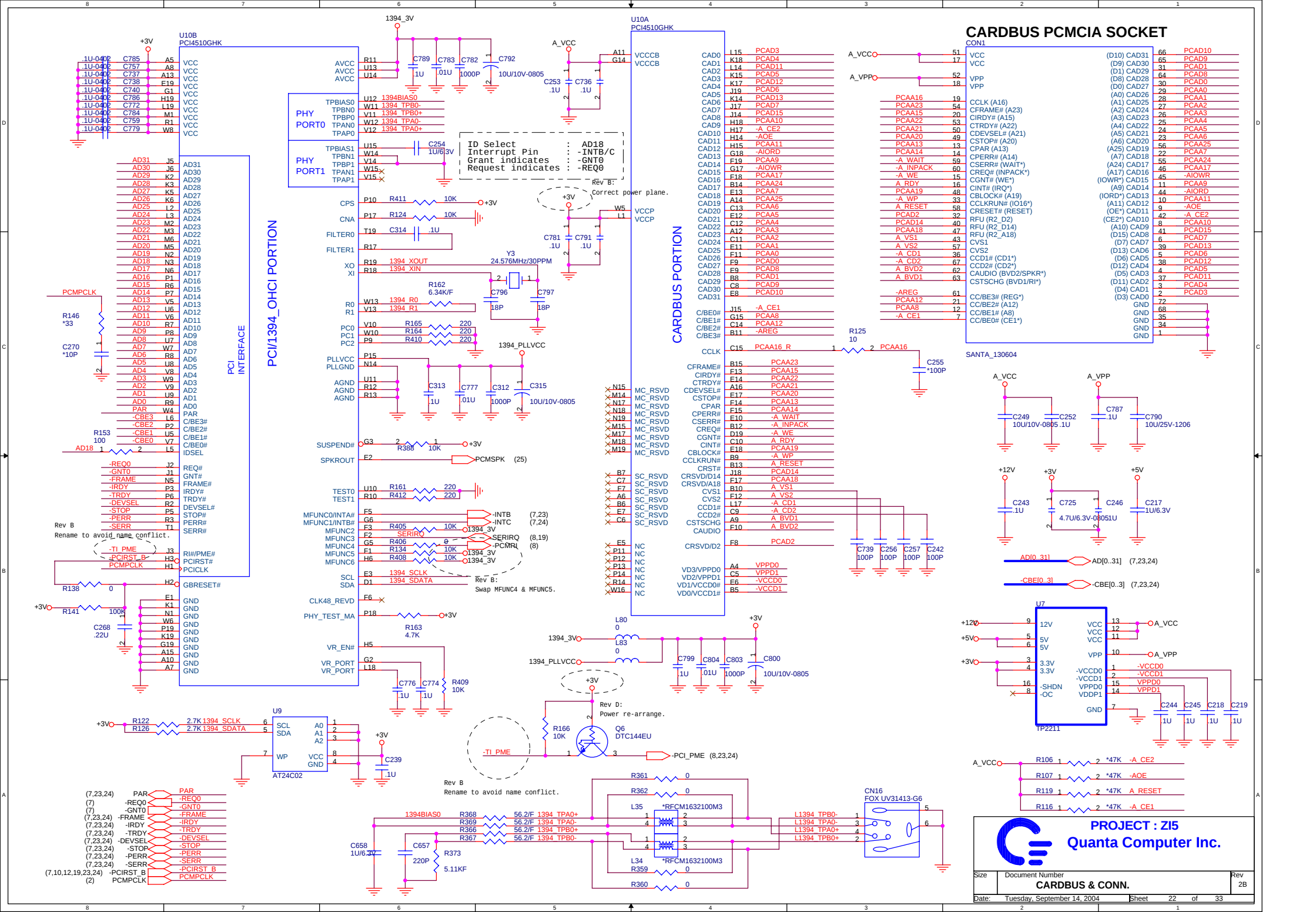
- Power and Ground:** Two 5VPCU pins are connected to the VCC pins of the buffers. A 10k resistor (R274) is connected to the 5VPCU pin. A 1uF capacitor (C413) is connected to the ground pin.
- Buffer U41A:** Inputs include -ROMOE, -IOSEL, and 5VPCU. Outputs are BA0 and BA1.
- Buffer U41B:** Inputs include -Q84, -Q83, -Q82, -Q81, -BT_SW, -PR_INSERT#_EC, -SHDN, and -WL_SW. Outputs are BD0[0..7].
- Resistors:** R274 (10k) and R269 (10k) are shown.
- Capacitors:** C413 (1uF) and C414 (1uF) are shown.
- Annotations:** A green circle highlights the PR_INSERT#_EC pin and its connection to P@0. A red circle highlights the BD0[0..7] output and its connection to BD0[7].

The diagram illustrates the LPT1 and PRINT PORT connections for the FCMI608K301 microcontroller. The LPT1 port (pins 19-25) is connected to a 5V_PR supply via a resistor network (C418-C425) and a 4.7K-10PBR resistor (RP1). The PRINT PORT (pins 14-25) is connected to a 5V_PR supply via a resistor network (C427-C434) and a 4.7K-10PBR resistor (RP2). The diagram also shows the connection of the LPT1 port to a 5V_PR supply via a resistor network (C418-C425) and a 4.7K-10PBR resistor (RP1). The PRINT PORT is connected to a 5V_PR supply via a resistor network (C427-C434) and a 4.7K-10PBR resistor (RP2).

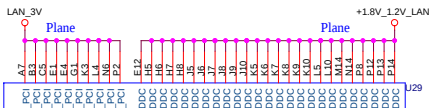
[illegible]

The schematic diagram illustrates the LED driver circuit for the device. It features a 5V supply connected to four LEDs: NUMLED, CAPSLED, EMAIL_LED, and IDE_LED. Each LED is connected to the 5V supply through a 1K resistor (R18, R19, R35, and R36 respectively). The LEDs are also connected to ground through a common ground connection. The circuit includes a 5V supply, a 1K resistor (R35), and a 1K resistor (R36). The LEDs are connected to a 5V supply through resistors. The circuit also includes a 5V supply, a 1K resistor (R35), and a 1K resistor (R36). The LEDs are connected to a 5V supply through resistors.

The figure consists of two rows of circuit diagrams, each representing a 12-bit ripple-carry adder. Each diagram shows a sequence of 12 full adders connected in a chain. The top row shows the carry propagation from the least significant bit (LSB) to the most significant bit (MSB). The bottom row shows the carry propagation from the MSB back to the LSB, indicating a full adder configuration.



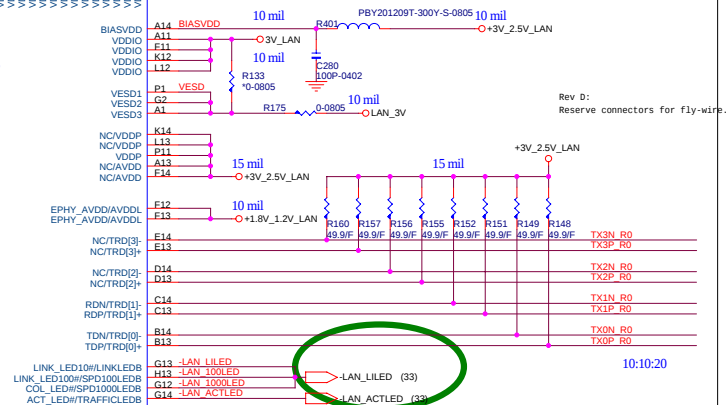
3V_LAN & +3V are from system power



BCM5788M

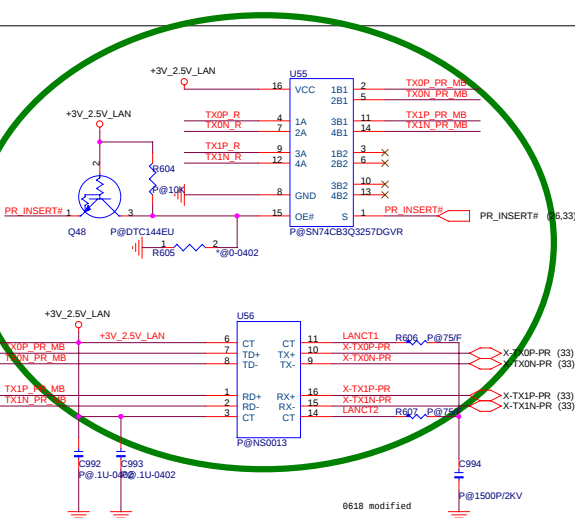
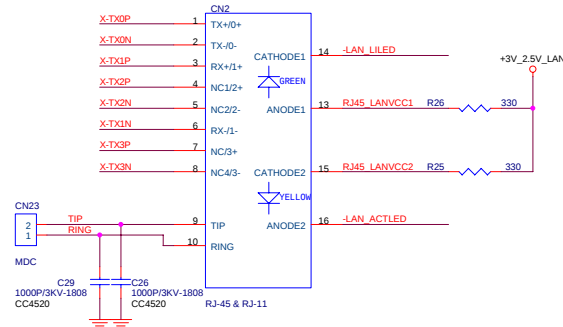
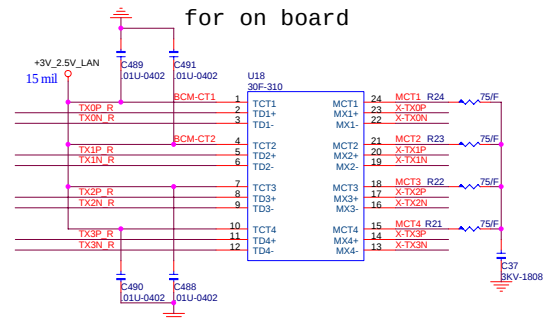
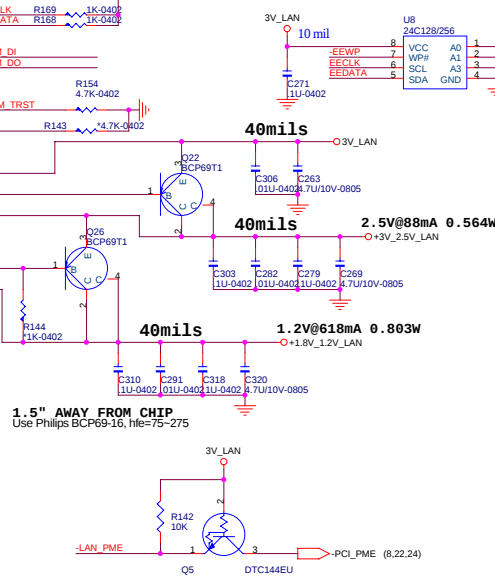
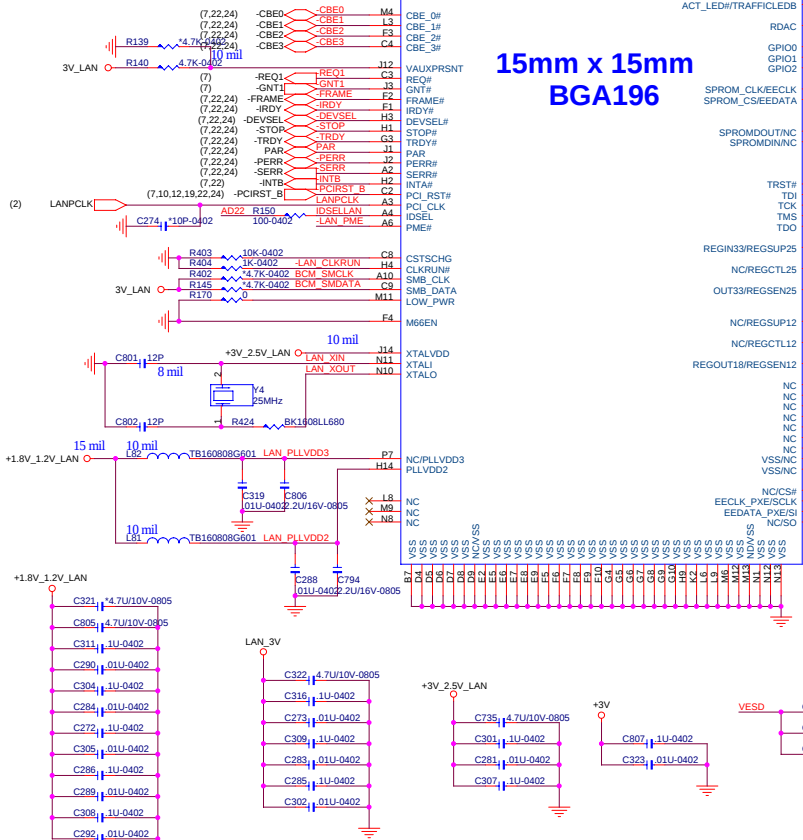
BCM5788M LAN

```
| ID Select      : AD22
| Interrupt Pin  : -INTB
| Request indicates : -REQ1
| Grant indicates : -GNT1
```



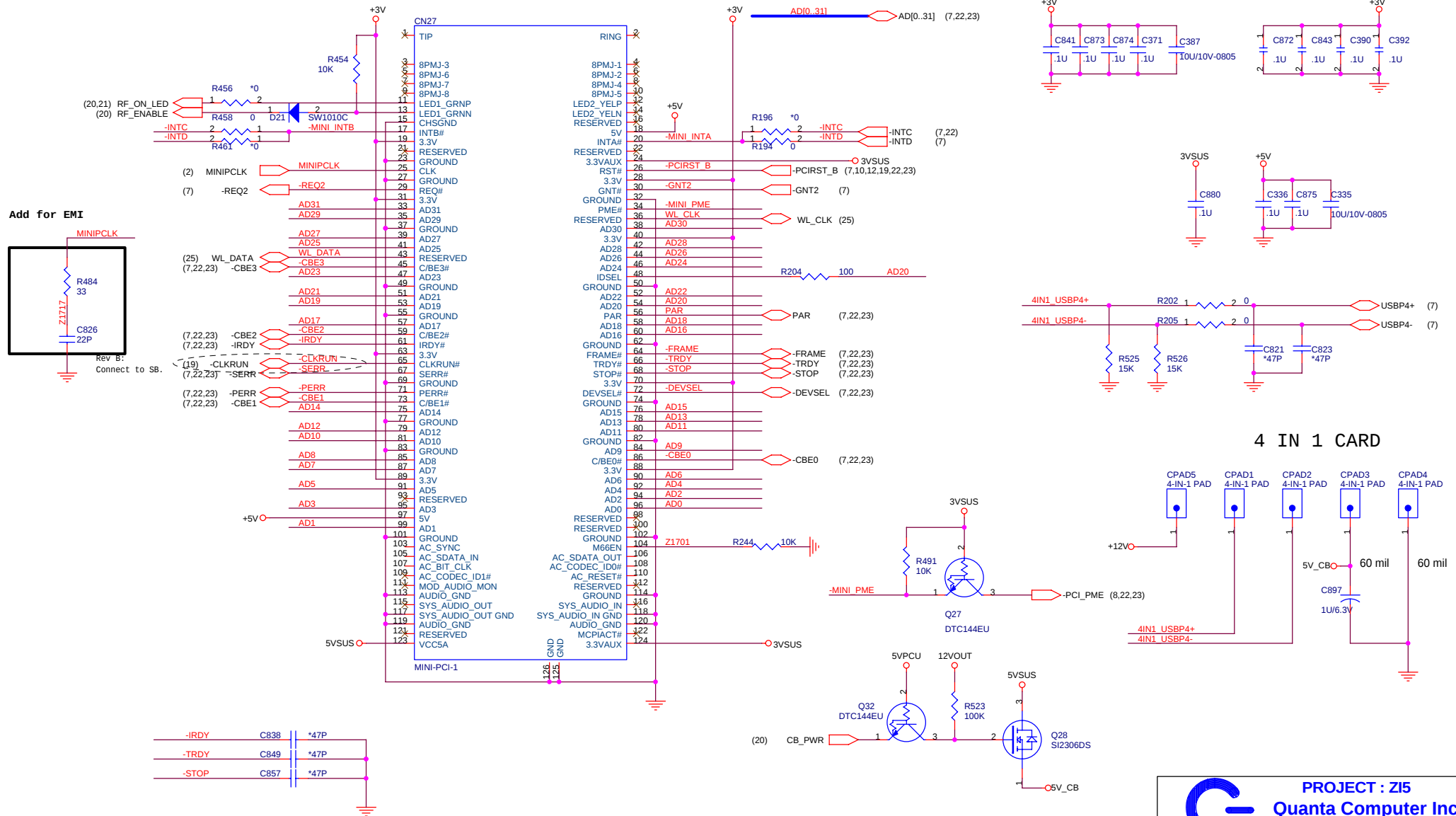
Rev D:
Reserve connectors for fly-wire.

15mm x 15mm
BGA196

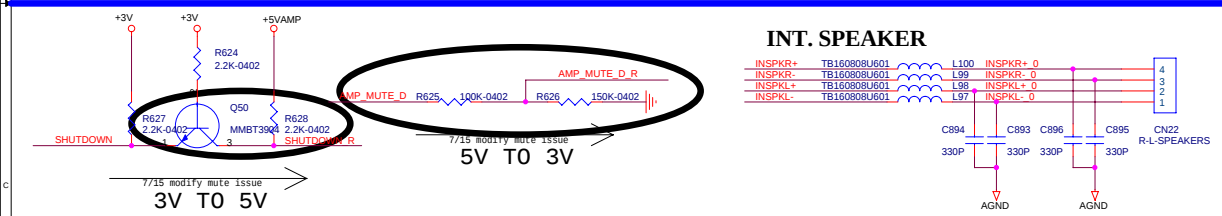
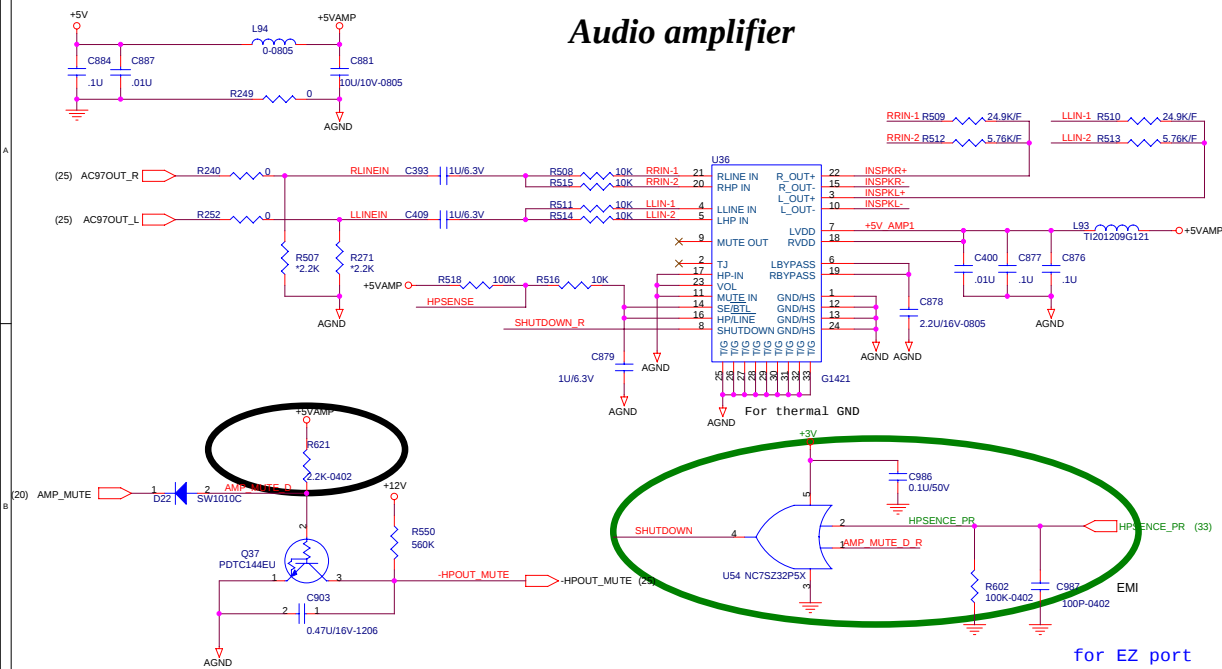


ID Select : AD20
Interrupt Pin : -INTC/D
Grant indicates : -GNT2
Request indicates : -REQ2

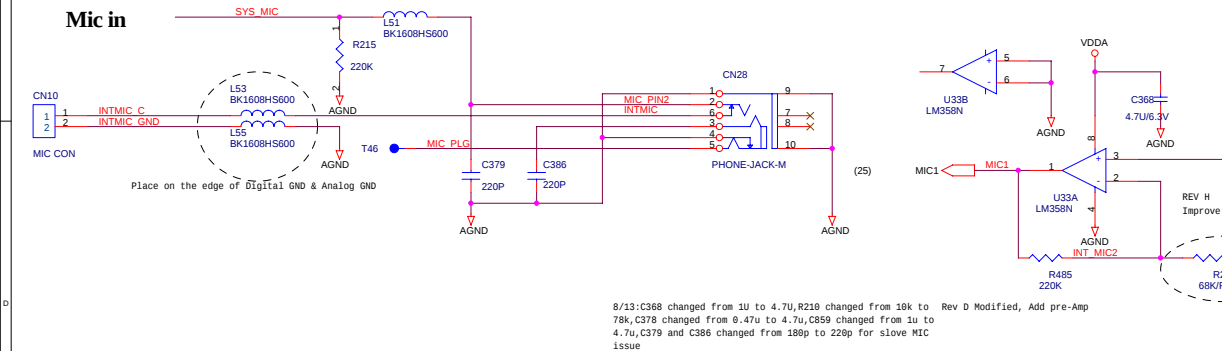
TYPE III MINI PCI SOCKET



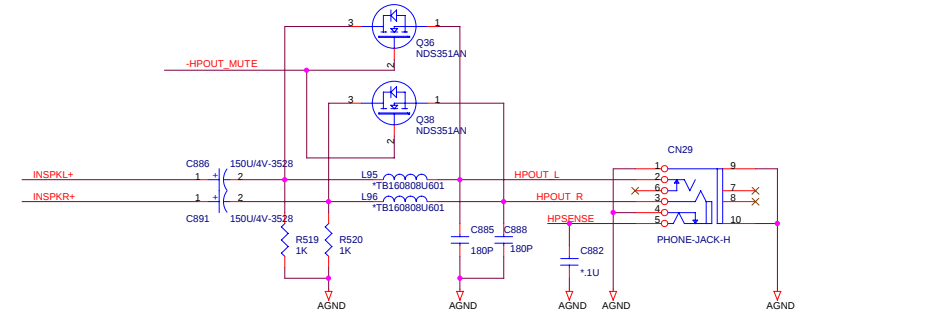
Audio amplifier



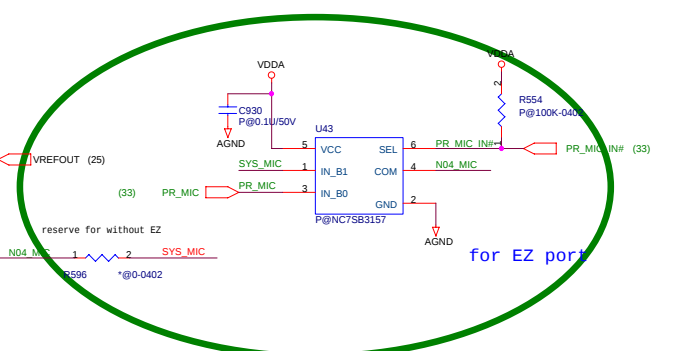
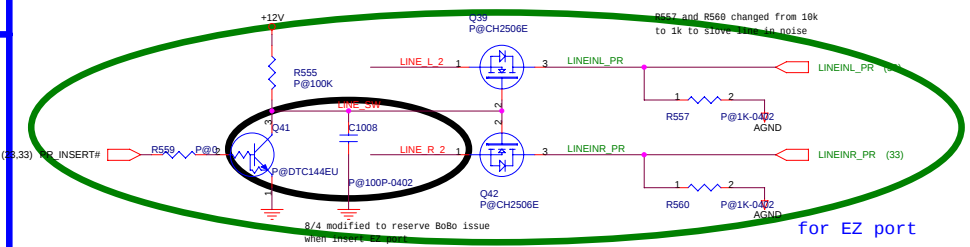
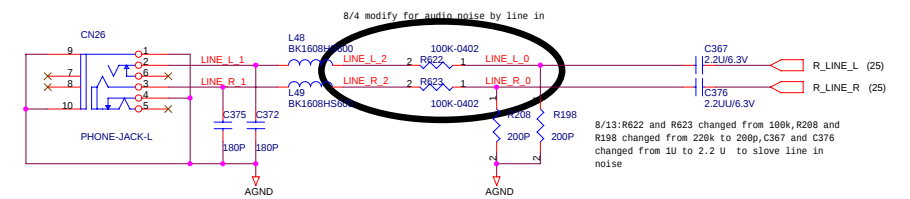
Mic in

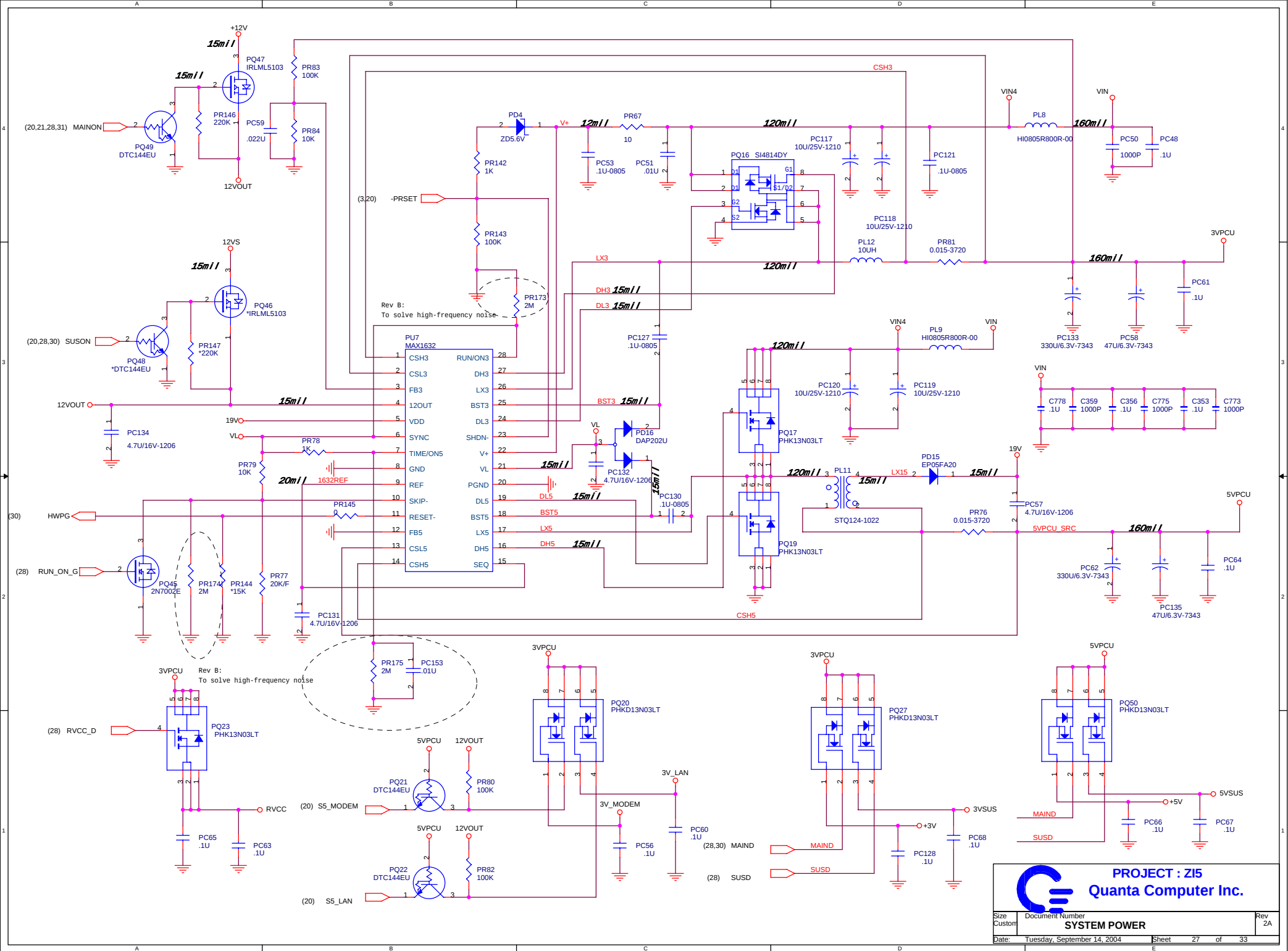


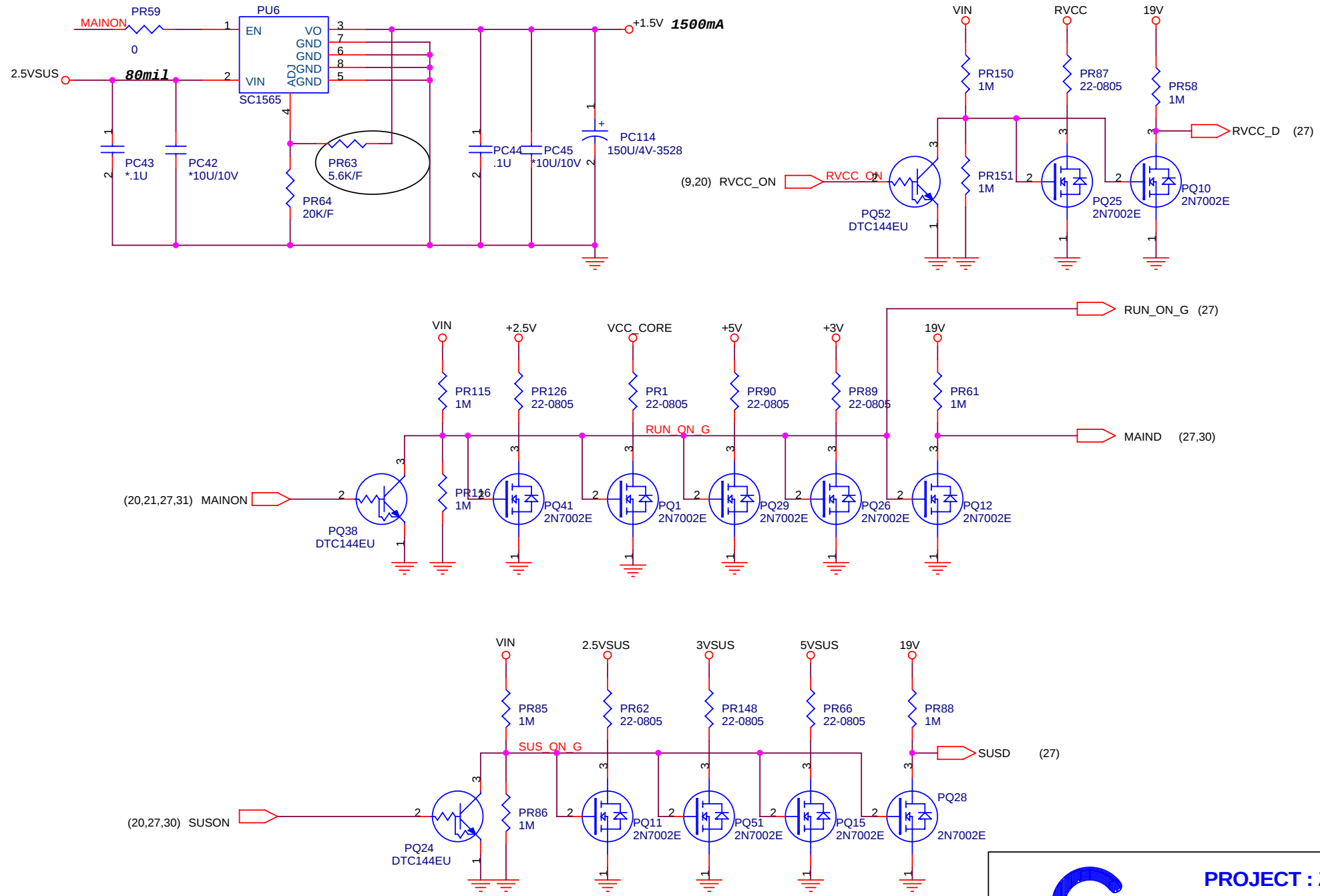
Headphone out

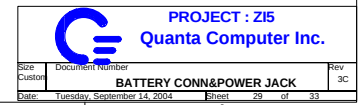


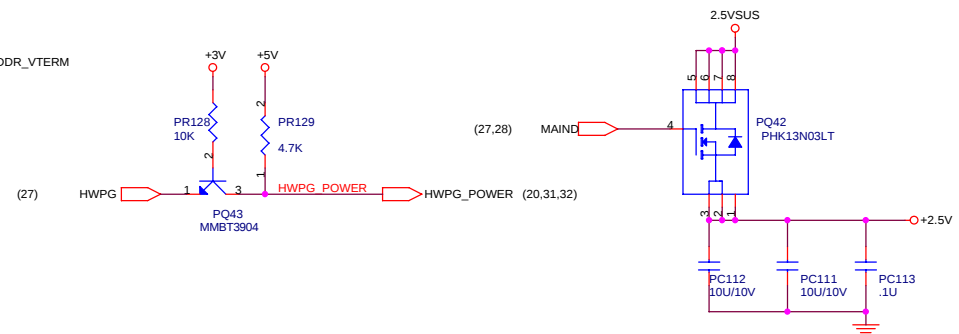
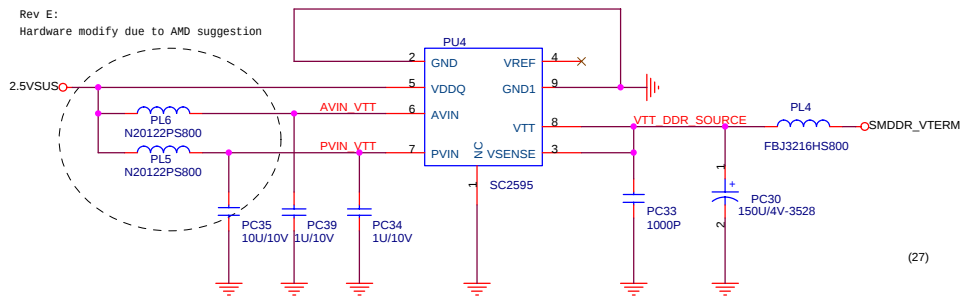
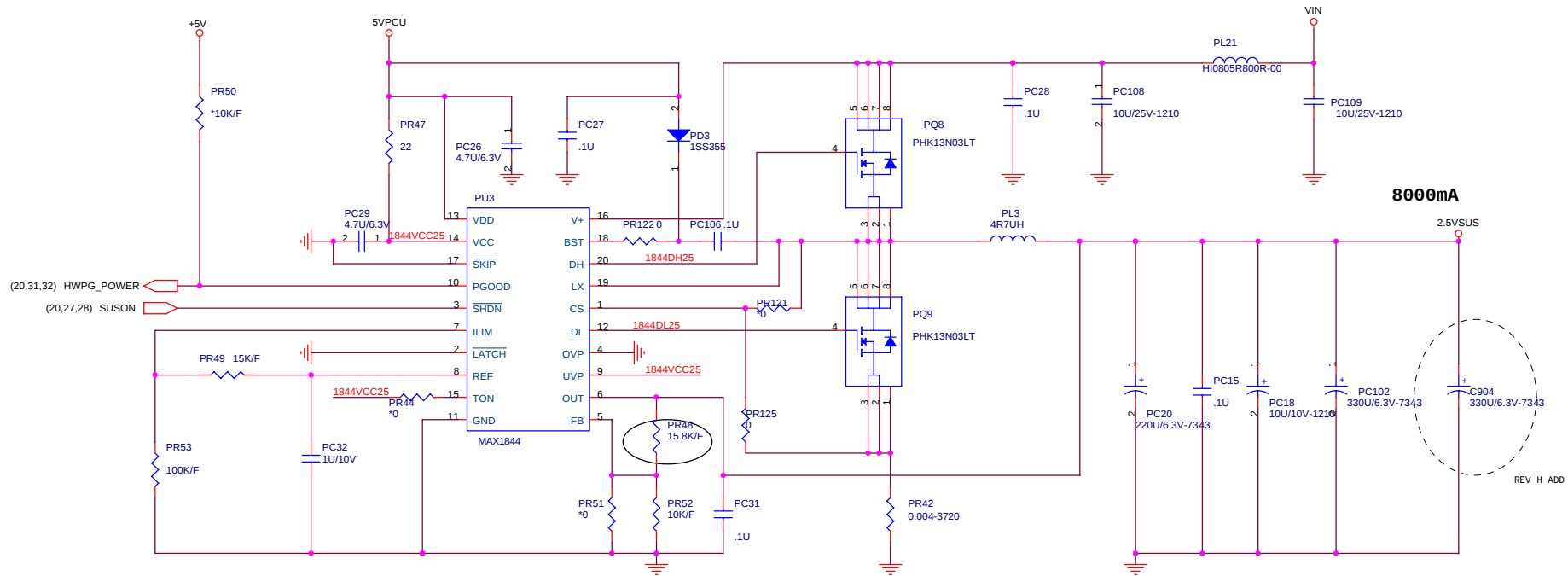
Line in











PROJECT : Z15
Quanta Computer Inc.

