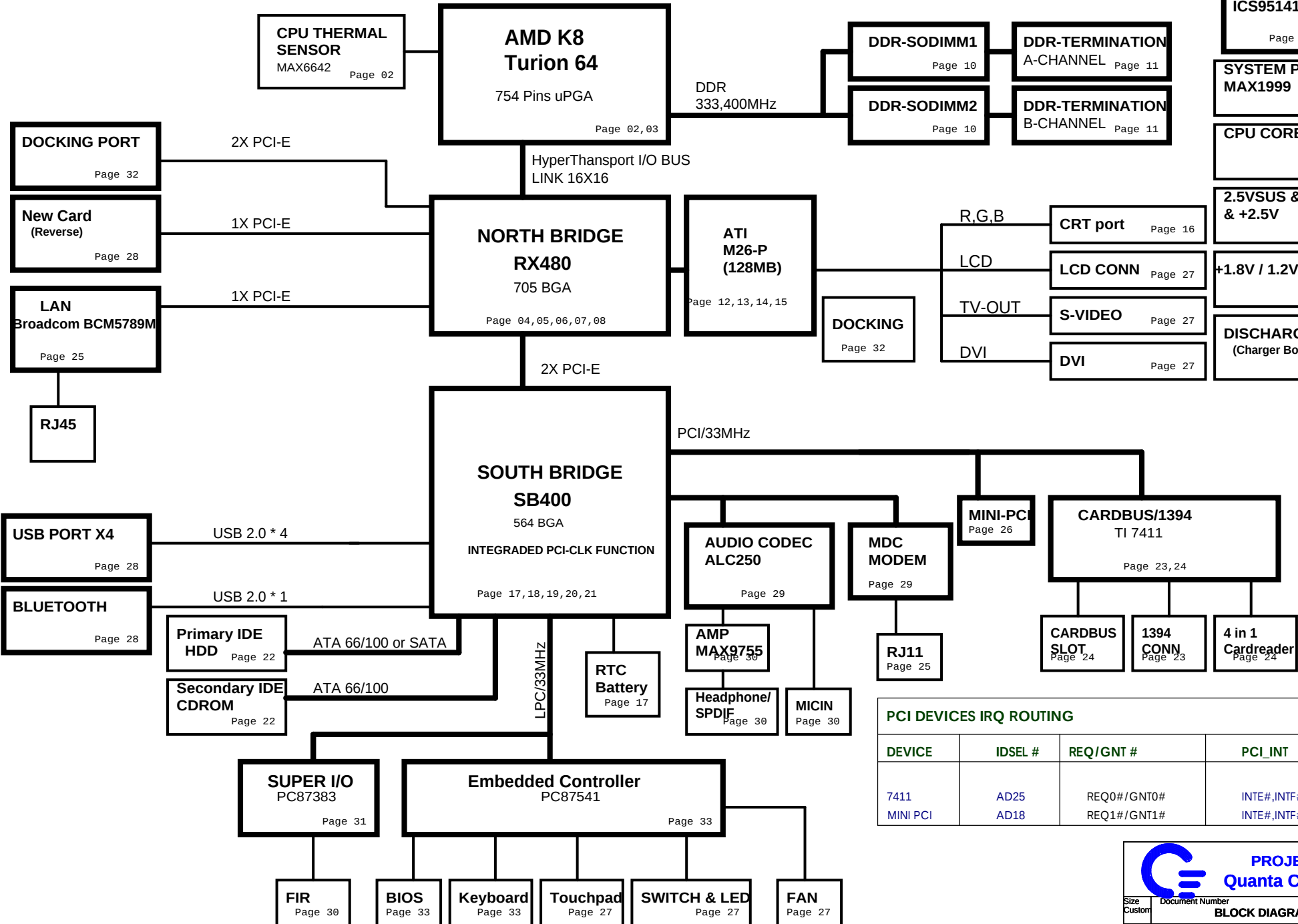
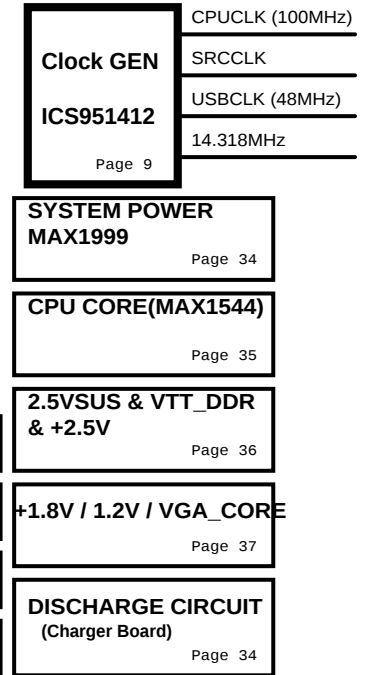


ZF3 BLOCK DIAGRAM

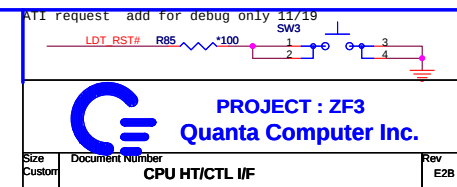
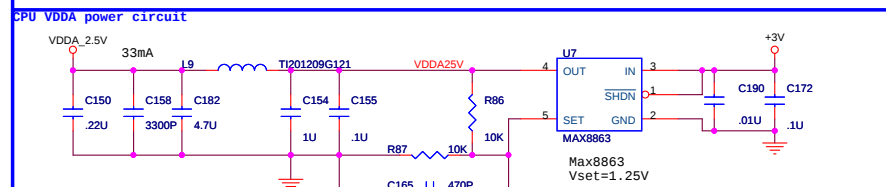
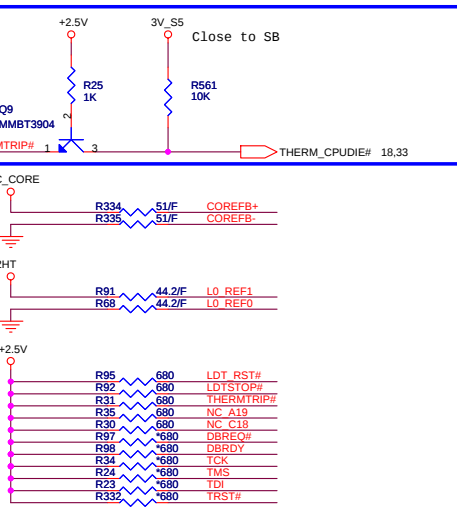
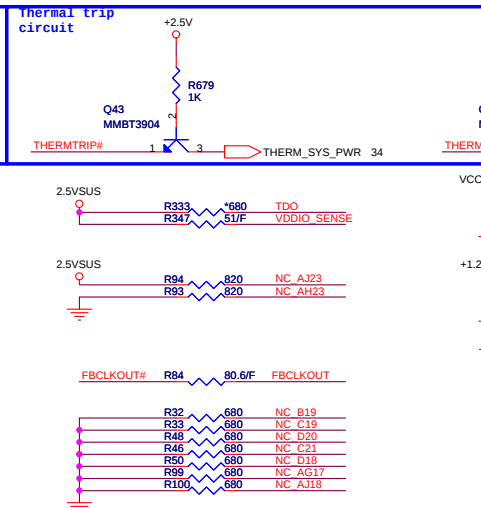
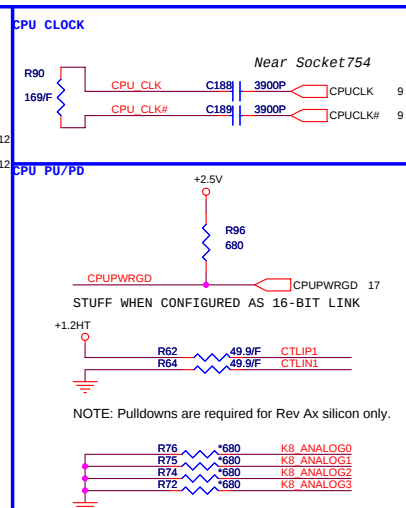
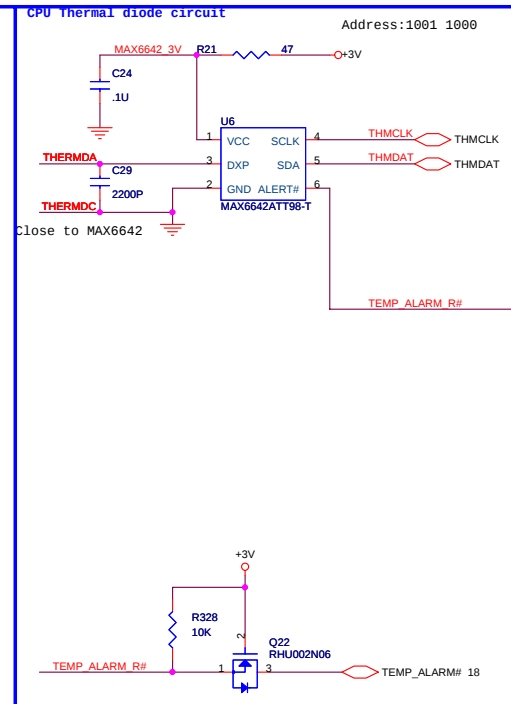
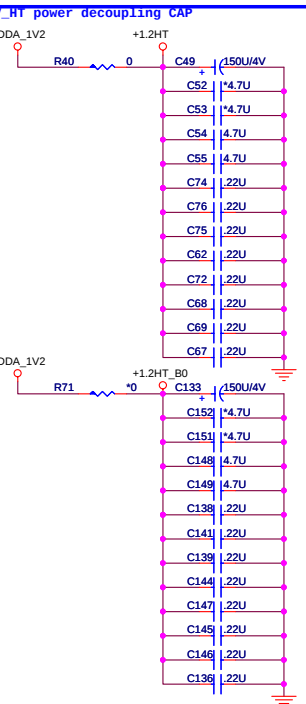
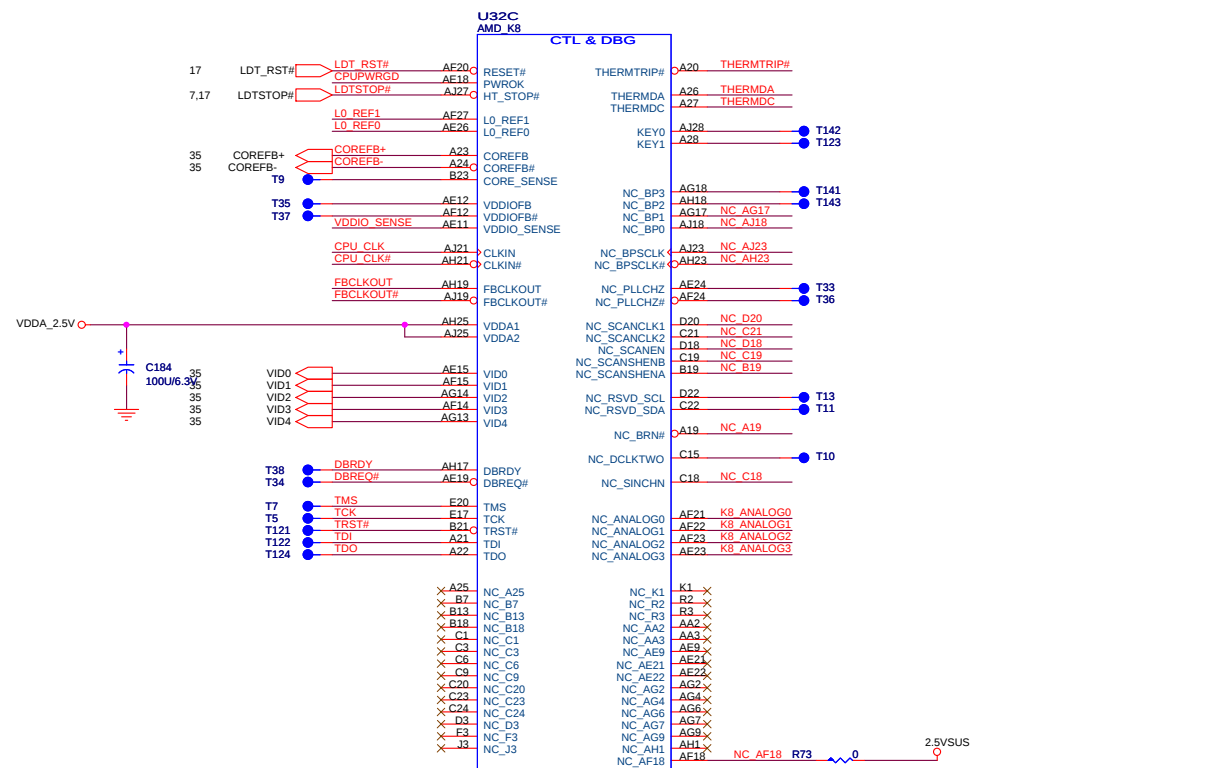
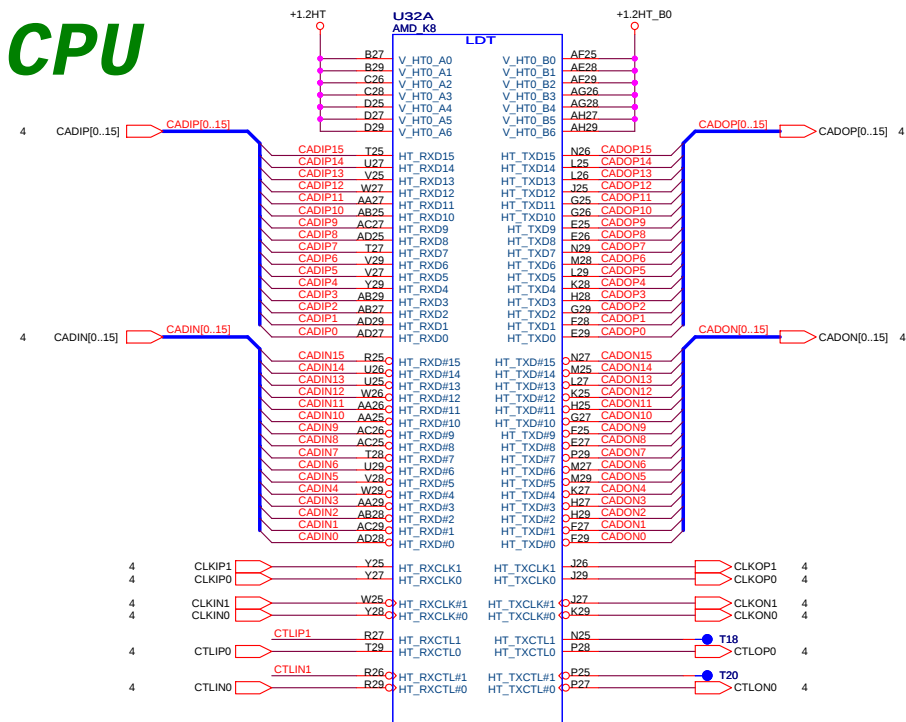
AMD K8/RX480/SB400

REV: G3A

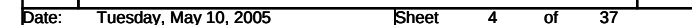


PCI DEVICES IRQ ROUTING			
DEVICE	IDSEL #	REQ/GNT #	PCI_INT
7411 MINI PCI	AD25 AD18	REQ0#/GNT0# REQ1#/GNT1#	INTE#,INTF#,INTH# INTE#,INTF#

CPU



A



NB



PROJECT : ZF3
Quanta Computer Inc.

Size Custom	Document Number RS480M SIDE-PORT MEM I/F	Rev E2B
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NB

U36B

PART 2 OF 6

PCIE I/F TO VIDEO

12 PEG_RXN15 D8 GFX_RX0P GFX_TX0P A7 GFX_TX0P_C GFX_TX0P_C .1U C342 PEG_TXP_C0 GFX_TX0N_C .1U C343 PEG_TXN_C0

12 PEG_RXP15 D7 GFX_RX0N GFX_TX0N B7 GFX_TX0N_C

12 PEG_RXN14 D5 GFX_RX1P GFX_TX1P B6 GFX_TX1P_C GFX_TX1P_C .1U C735 PEG_TXP_C1 GFX_TX1N_C .1U C738 PEG_TXN_C1

12 PEG_RXP14 D4 GFX_RX1N GFX_TX1N B5 GFX_TX1N_C

12 PEG_RXN13 E4 GFX_RX2P GFX_TX2P A4 GFX_TX2P_C GFX_TX2P_C .1U C739 PEG_TXP_C2 GFX_TX2N_C .1U C740 PEG_TXN_C2

12 PEG_RXP13 G5 GFX_RX2N GFX_TX2N B3 GFX_TX2N_C

12 PEG_RXN12 G4 GFX_RX3P GFX_TX3P B2 GFX_TX3N_C GFX_TX3P_C .1U C741 PEG_TXP_C3 GFX_TX3N_C .1U C742 PEG_TXN_C3

12 PEG_RXP12 H4 GFX_RX3N GFX_TX3N C1 GFX_TX4P_C

12 PEG_RXN11 J4 GFX_RX4P GFX_TX4P D1 GFX_TX4N_C GFX_TX4P_C .1U C747 PEG_TXP_C4 GFX_TX4N_C .1U C748 PEG_TXN_C4

12 PEG_RXP11 H5 GFX_RX4N GFX_TX4N D2 GFX_TX5P_C

12 PEG_RXN10 H6 GFX_RX5P GFX_TX5P E2 GFX_TX5N_C GFX_TX5P_C .1U C769 PEG_TXP_C5 GFX_TX5N_C .1U C770 PEG_TXN_C5

12 PEG_RXP10 G1 GFX_RX5N GFX_TX5N E2 GFX_TX6P_C

12 PEG_RXN9 G2 GFX_RX6P GFX_TX6P F1 GFX_TX6N_C GFX_TX6P_C .1U C749 PEG_TXP_C6 GFX_TX6N_C .1U C750 PEG_TXN_C6

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12 PEG_RXP8 L4 GFX_RX7N GFX_TX7N J1 GFX_TX8P_C

12 PEG_RXN7 M4 GFX_RX8P GFX_TX8P K1 GFX_TX8N_C GFX_TX8P_C .1U C771 PEG_TXP_C8 GFX_TX8N_C .1U C772 PEG_TXN_C8

12 PEG_RXP7 N5 GFX_RX8N GFX_TX8N K2 GFX_TX9P_C

12 PEG_RXN6 N4 GFX_RX9P GFX_TX9P L2 GFX_TX9N_C GFX_TX9P_C .1U C753 PEG_TXP_C9 GFX_TX9N_C .1U C754 PEG_TXN_C9

12 PEG_RXP6 P4 GFX_RX9N GFX_TX9N M2 GFX_TX10P_C

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12 PEG_RXP5 P5 GFX_RX10N GFX_TX10N N1 GFX_TX11P_C

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12 PEG_RXP4 R2 GFX_RX11N GFX_TX11N R1 GFX_TX12P_C

12 PEG_RXN3 R2 GFX_RX12P GFX_TX12P T1 GFX_TX12N_C

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12 PEG_RXN2 T4 GFX_RX13P GFX_TX13P U2 GFX_TX13N_C

12 PEG_RXP2 U4 GFX_RX13N GFX_TX13N V2 GFX_TX14P_C

12 PEG_RXN1 V4 GFX_RX14P GFX_TX14P V1 GFX_TX14N_C

12 PEG_RXP1 W1 GFX_RX14N GFX_TX14N Y2 GFX_TX15P_C

12 PEG_RXN0 W2 GFX_RX15P GFX_TX15P Y2 GFX_TX15P_C

12 PEG_RXP0 W2 GFX_RX15N GFX_TX15N AA2 GFX_TX15N_C

12 PEG_RXN0 W2 GFX_RX15N GFX_TX15N AA2 GFX_TX15N_C

32 PCIE_RXP0 AE1 GPP_RX0P GPP_TX0P AD2 GPP_TX0P_C C1175 .1U PCIE_TXP0 32

32 PCIE_RXN0 AE2 GPP_RX0N GPP_TX0N AD1 GPP_TX0N_C C1176 .1U PCIE_TXN0 32

32 PCIE_RXP1 AB2 GPP_RX1P GPP_TX1P AA1 GPP_TX1P_C C763 .1U PCIE_TXP1 32

32 PCIE_RXN1 AC2 GPP_RX1N GPP_TX1N AB1 GPP_TX1N_C C764 .1U PCIE_TXN1 32

25 PCIE_RXP2 AB5 GPP_RX2P GPP_TX2P Y5 GPP_TX2P_C C782 .1U PCIE_TXP2 25

25 PCIE_RXN2 AB4 GPP_RX2N GPP_TX2N Y6 GPP_TX2N_C C781 .1U PCIE_TXN2 25

28 PCIE_RXP3 Y4 GPP_RX3P GPP_TX3P W5 GPP_TX3P_C C762 *.1U PCIE_TXP3 28

28 PCIE_RXN3 AA4 GPP_RX3N GPP_TX3N W4 GPP_TX3N_C C761 *.1U PCIE_TXN3 28

17 A_RX0P AG1 SB_RX0P SB_TX0P AF2 A_TX0P_C C765 .1U A_TX0P 17

17 A_RX0N AH1 SB_RX0N SB_TX0N AG2 A_TX0N_C C766 .1U A_TX0N 17

17 A_RX1P AC5 SB_RX1P SB_TX1P AC4 A_TX1P_C C783 .1U A_TX1P 17

17 A_RX1N AC6 SB_RX1N SB_TX1N AD4 A_TX1N_C C784 .1U A_TX1N 17

R138 10K/F NB_PCE_ISET AH3 PCE_ISET AH2 NB_PCE_PCAL R415 150/F

R414 8.25K/FNB_PCE_TXISET AJ3 PCE_TXISET AJ2

RX480

NB_PCE_NCAL R413 82.5/F VDDA_1V2

PROJECT : ZF3

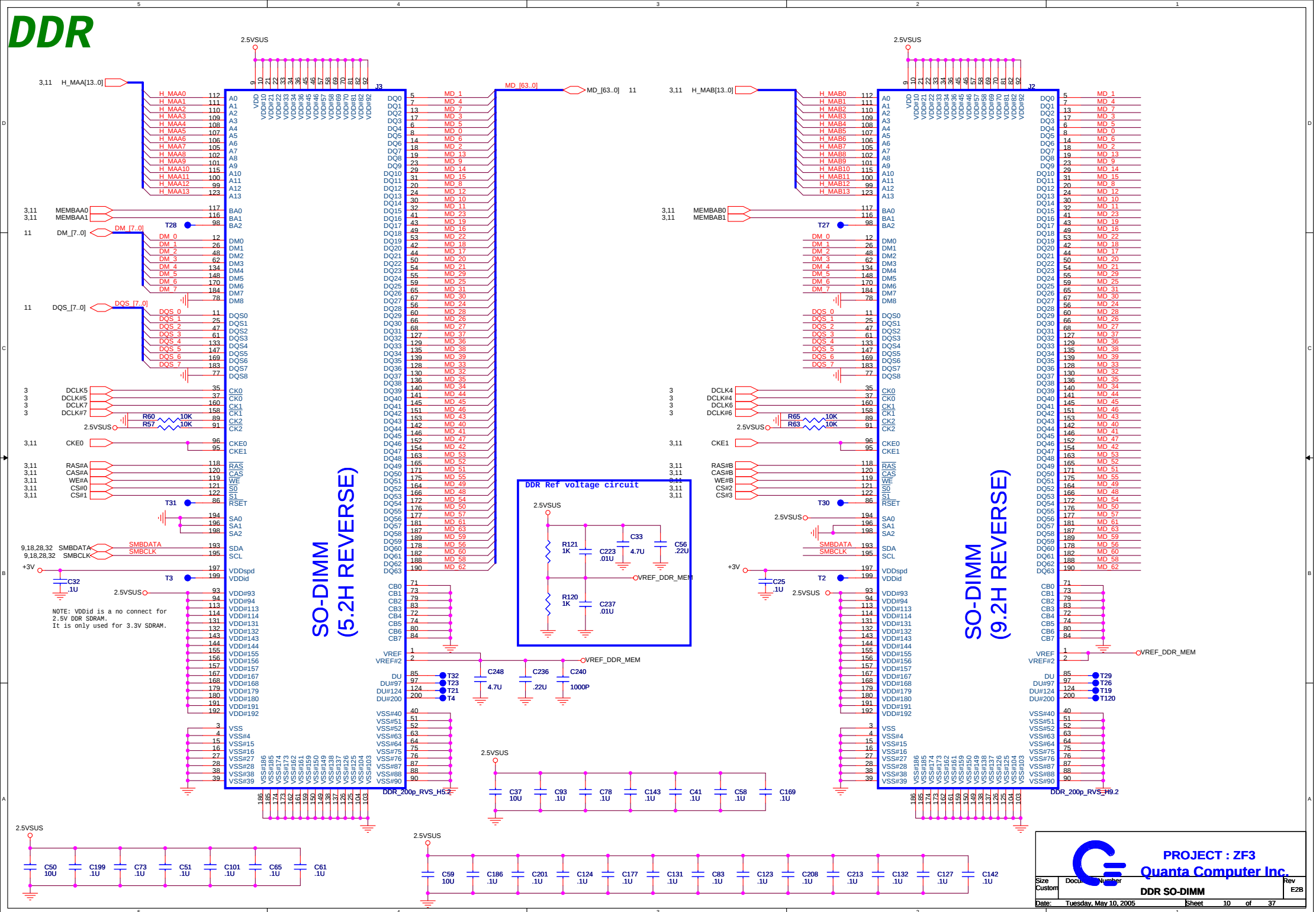
Quanta Computer Inc.

Size Document Number Rev

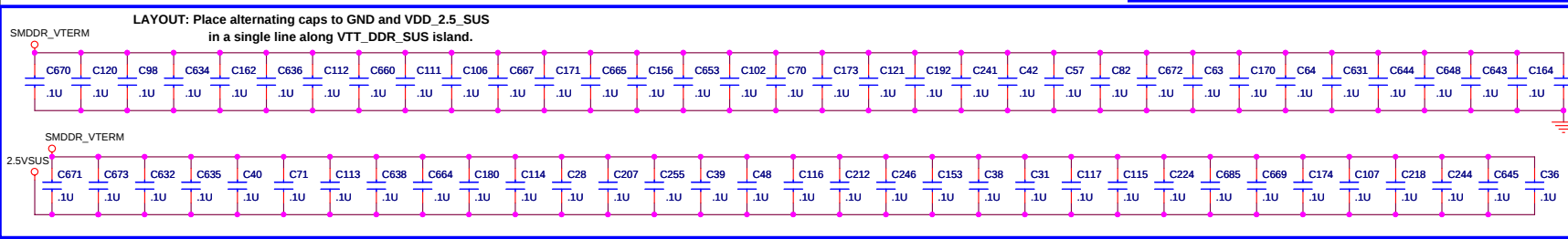
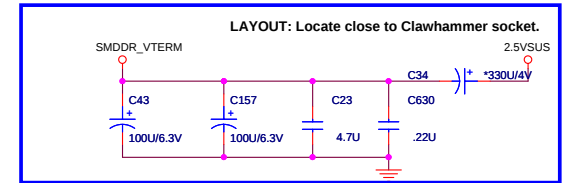
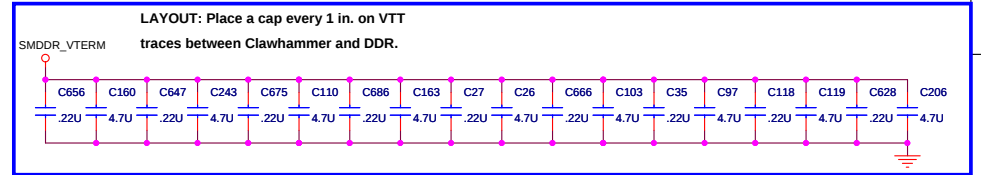
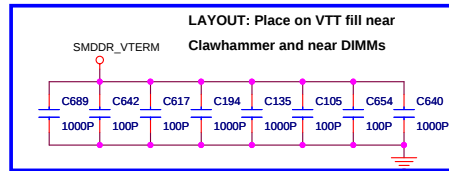
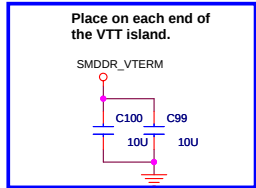
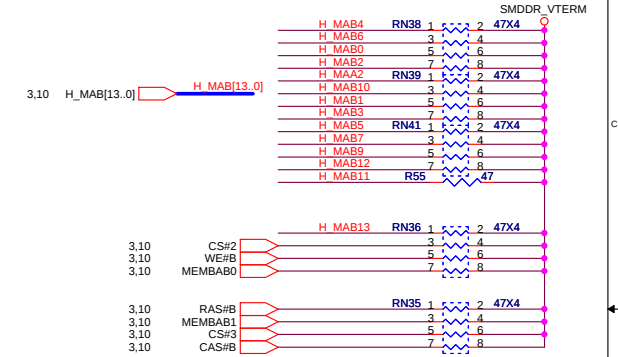
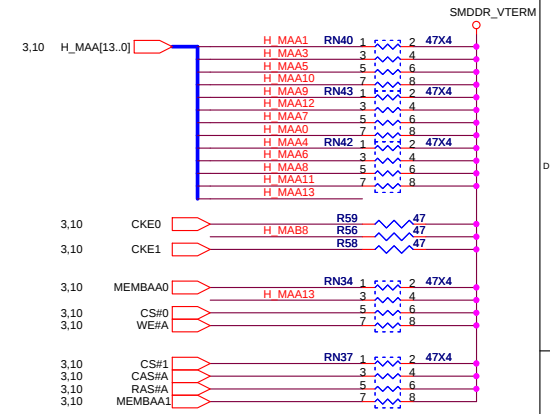
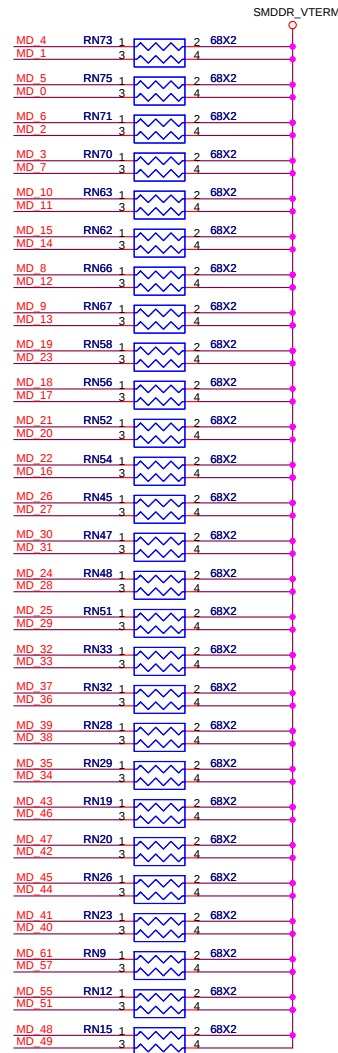
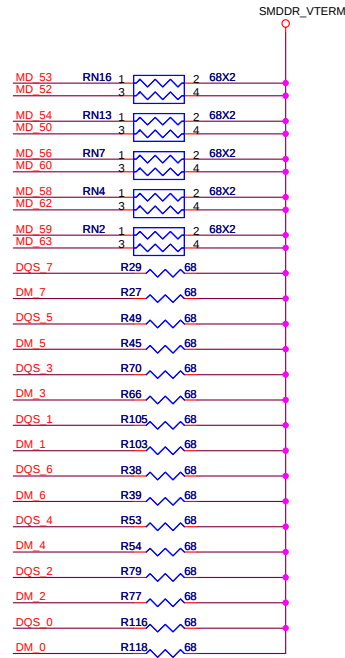
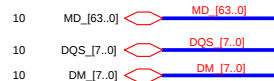
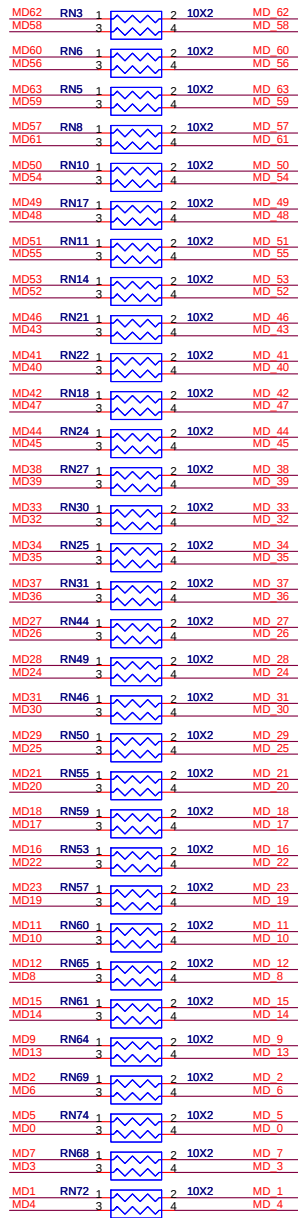
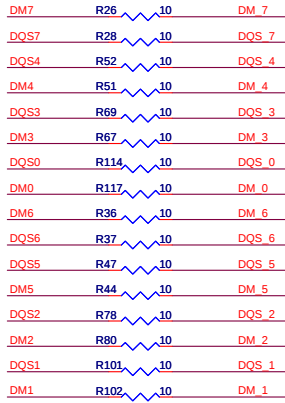
Custom E2B

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Size	Docu	Rev	
Custom	Number	E2B	
RS480M POWER			
Date:	Tuesday, May 10, 2005	Sheet	8 of 37



DDR



VGA

6 PEG_TXP_C[0..15]

6 PEG_TXN_C[0..15]

6 PEG_RXP[0..15]

6 PEG_RXN[0..15]

9 CLK_PCIE_VGA

VGA_1.2V

+3V

R166

C804

C805

+3V

7.17.22.25.28.31.32.33

5

U40A

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PEG_TXP_C15 AG30
PEG_TXN_C14 AG29
PEG_TXP_C14 AE29
PEG_TXN_C13 AE29
PEG_TXP_C13 AE30
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PEG_TXP_C12 AD30
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PEG_TXP_C11 AB29
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PEG_TXN_C9 AA29
PEG_TXP_C9 Y29
PEG_TXN_C8 W29
PEG_TXP_C8 W30
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PEG_TXP_C7 V29
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PEG_TXP_C6 U30
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PEG_TXP_C5 T30
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PEG_TXP_C4 R30
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PEG_TXP_C3 N30
PEG_TXN_C2 M29
PEG_TXP_C2 M30
PEG_TXN_C1 L29
PEG_TXP_C1 K29
PEG_TXN_C0 K30
PEG_TXP_C0 J30

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PCIE_RX0N AG30
PCIE_RX1P AG29
PCIE_RX1N AE29
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PCIE_TX14N K27
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PCIE_RX2N C432
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PCIE_RX14N C347
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PCIE_TX15N K26

PCIE EXPRESS

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PCIE_TX0N AE26
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PCIE_TX14P K27
PCIE_TX14N K27
PCIE_TX15P L26
PCIE_TX15N K26

PCIE REFCLKP AE27
PCIE REFCLKN AE27

PCIE_CALRP AC23
PCIE_CALRN AB24
PCIE_CALI AB23
PCIE_TESTIN AE25

PCIE_RST# M26 A_RST# AD25
VPCIE_RST# AD24

TV_Y/G AK21
TV_C/R AJ22
TV_COMP AK22

H2SYNC V2SYNC
V2SYNC

DDC3CLK DDC3DATA
DDC3DATA

SSIN SSOUT
SSOUT

XTALIN XTALOUT
XTALOUT

TESTEN TEST_YCLK
TEST_YCLK
TEST_YCLK
PLLTEST AE25

STEREOSYNC
STEREOSYNC

SS

CLK

THERM

SSIN SSOUT
SSOUT

XTALIN XTALOUT
XTALOUT

TESTEN TEST_YCLK
TEST_YCLK
TEST_YCLK
PLLTEST AE25

STEREOSYNC
STEREOSYNC

SS

CLK

THERM

SSIN SSOUT
SSOUT

XTALIN XTALOUT
XTALOUT

TESTEN TEST_YCLK
TEST_YCLK
TEST_YCLK
PLLTEST AE25

STEREOSYNC
STEREOSYNC

GPIO0 AJ5
GPIO1 AH5
GPIO2 AJ4
GPIO3 AK4
GPIO4 AE4
GPIO5 AE4
GPIO6 AJ3
GPIO7 AK3
GPIO8 AH3
GPIO9 AJ2
GPIO10 AH2
GPIO11 AH1
GPIO12 AG3
GPIO13 AG1
GPIO14 AG2
GPIO15 AE3

ROMIDCFG0 14
C794 10P

DVOMODE AE10
DVOMODE R153

DVPDATA_0 AH6
DVPDATA_1 AJ6
DVPDATA_2 AK6
DVPDATA_3 AH7
DVPDATA_4 AK7
DVPDATA_5 AJ7
DVPDATA_6 AH8
DVPDATA_7 AJ8
DVPDATA_8 AH9
DVPDATA_9 AJ9
DVPDATA_10 AK9
DVPDATA_11 AH10
DVPDATA_12 AJ10
DVPDATA_13 AK6
DVPDATA_14 AE7
DVPDATA_15 AE8
DVPDATA_16 AE9
DVPDATA_17 AE8
DVPDATA_18 AE9
DVPDATA_19 AE9
DVPDATA_20 AE9
DVPDATA_21 AE9
DVPDATA_22 AG10
DVPDATA_23 AE10

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EDIDCLK 27
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DVPDATA_22 14
DVPDATA_23 14

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DVPDATA_17 14
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EDIDCLK 27
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DVPDATA_22 14
DVPDATA_23 14

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DVPDATA_16 14
DVPDATA_17 14
EDIDCLK 27
EDIDCLK 27
DVPDATA_20 20
DVPDATA_21 14
DVPDATA_22 14
DVPDATA_23 14

DVPDATA_16 14
DVPDATA_17 14
EDIDCLK 27
EDIDCLK 27
DVPDATA_20 20
DVPDATA_21 14
DVPDATA_22 14
DVPDATA_23 14

DVPDATA_16 14
DVPDATA_17 14
EDIDCLK 27
EDIDCLK 27
DVPDATA_20 20
DVPDATA_21 14
DVPDATA_22 14
DVPDATA_23 14

LVDS

TXOUT_L0N
TXOUT_L0P
TXOUT_L1N
TXOUT_L1P
TXOUT_L2N
TXOUT_L2P
TXOUT_L3N
TXOUT_L3P
TXCLK_LN
TXCLK_LP
TXOUT_U0N
TXOUT_U0P
TXOUT_U1N
TXOUT_U1P
TXOUT_U2N
TXOUT_U2P
TXOUT_U3N
TXOUT_U3P
TXCLK_UN
TXCLK_UP

TXOUT0- 27
TXOUT0+ 27
TXOUT1- 27
TXOUT1+ 27
TXOUT2- 27
TXOUT2+ 27
TXOUT3- 27
TXOUT3+ 27
TXCLKOUT- 27
TXCLKOUT+ 27
TXOUT0- 27
TXOUT0+ 27
TXOUT1- 27
TXOUT1+ 27
TXOUT2- 27
TXOUT2+ 27
TXCLKOUT- 27
TXCLKOUT+ 27

TXOUT0- 27
TXOUT0+ 27
TXOUT1- 27
TXOUT1+ 27
TXOUT2- 27
TXOUT2+ 27
TXOUT3- 27
TXOUT3+ 27
TXCLKOUT- 27
TXCLKOUT+ 27

TMDS

TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TXCM
TXCP

TMDS_TX0M
TMDS_TX0P
TMDS_TX1M
TMDS_TX1P
TMDS_TX2M
TMDS_TX2P
TMDS_TXCM
TMDS_TXCP

TMDS_TX0M
TMDS_TX0P
TMDS_TX1M
TMDS_TX1P
TMDS_TX2M
TMDS_TX2P
TMDS_TXCM
TMDS_TXCP

DAC1

DDC2CLK DDC2DATA
DDC2DATA

HPD1
HPD1

R VGA_RED
G VGA_GRN
B VGA_BLU

HSYNC VSYNC
VSYNC

RSET
RSET

DDC1DATA DDC1CLK
DDC1CLK

GPIO_AUXWIN
GPIO_AUXWIN

DPLUS DMINUS
DPLUS

U10 *7SH08
U10

SS

CLK

THERM

SSIN SSOUT
SSOUT

XTALIN XTALOUT
XTALOUT

TESTEN TEST_YCLK
TEST_YCLK
TEST_YCLK
PLLTEST AE25

STEREOSYNC
STEREOSYNC

VGA clock spectrum

MEMORY CLOCK SPREAD SPECTRUM

SRS= 1 DOWN -2.5%
0 DOWN -1.8%
M DOWN -0.6%

U45
CY25619
MK1726-8

XT_IN 1
XIN 2
VSS 3
SRS 4
SSCLK 5
XT_OUT 8
MK1726 VDD 7
MK PD 6
MK 27M 5
REF 4

1726_S0
1726_CK0

R485 *10K
R483 *10K
R491 *10K

33F
27MOUT
C822 .1U
C819 22U/10V

27M_IN R493
27M_O R449

Place Close to VGA

R500 71.5F

Thermal circuit

Q15 RHU002N06
Q16 RHU002N06

VTHM_CLK R170
VTHM_DAT R171
DVPDATA_20 R162

6.8K/F
6.8K/F
10K

3V THM1 47
C474 1U

MAX6647MUA
MSOP8-4_9-65

SMCLK VDD
SMDATA DXP
ALERT DXP
OVERT

3V THM1 47
C474 1U

TV_OUT

TV_Y/G
TV_C/R
TV_COMP

Place Close to VGA

R441 150F
R442 150F
R443 150F

TMDS

Place Close to VGA

TMDS_TX0M
TMDS_TX0P
TMDS_TX1M
TMDS_TX1P
TMDS_TX2M
TMDS_TX2P
TMDS_TXCM
TMDS_TXCP

TMDS_TX0M 16
TMDS_TX0P 16
TMDS_TX1M 16
TMDS_TX1P 16
TMDS_TX2M 16
TMDS_TX2P 16
TMDS_TXCM 16
TMDS_TXCP 16

RGB

Place Close to VGA

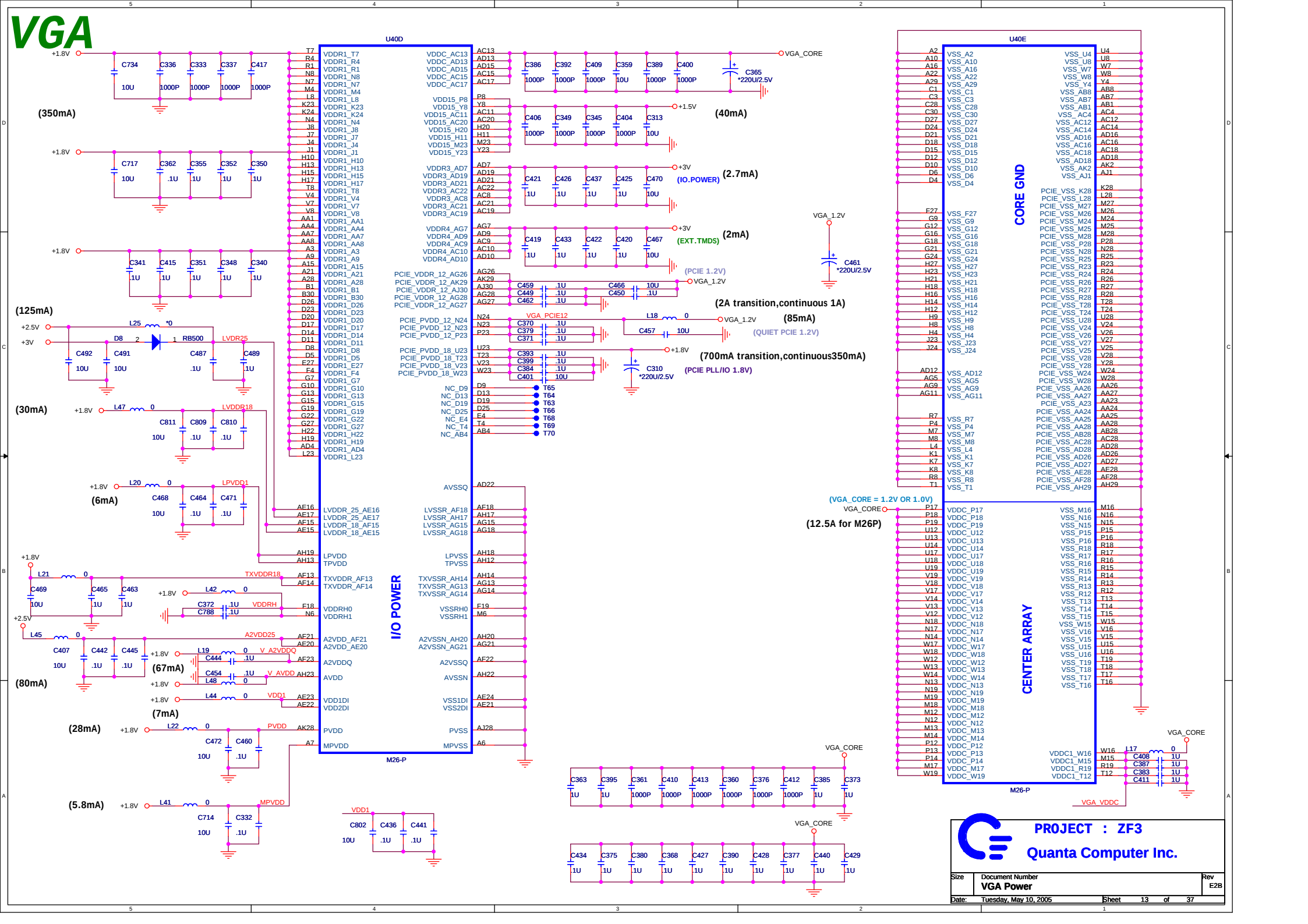
VGA_RED R447
VGA_GRN R446
VGA_BLU R445

150F
150F
150F

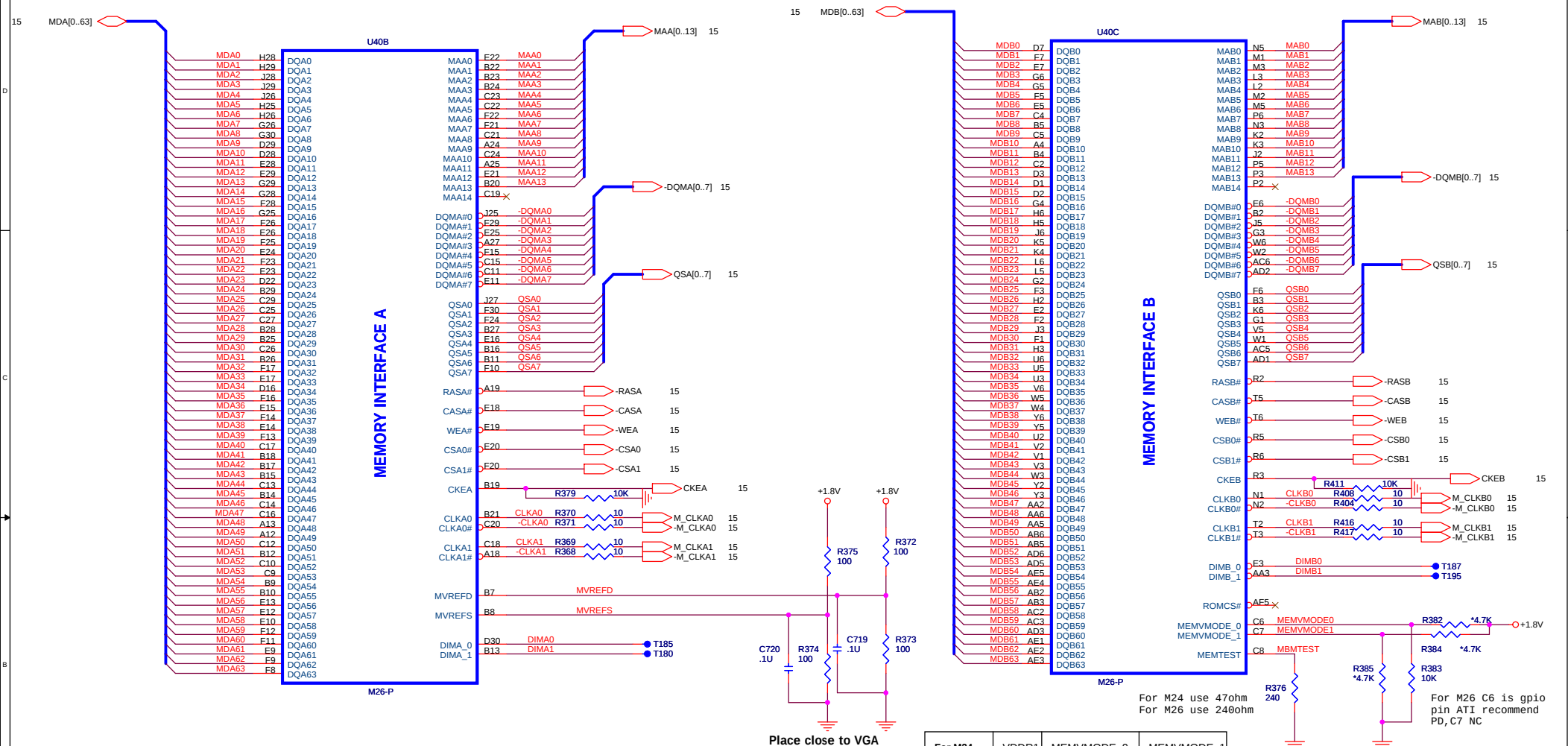
PROJECT : ZF3
Quanta Computer Inc.

Size Document Number
VGA Host

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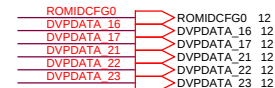
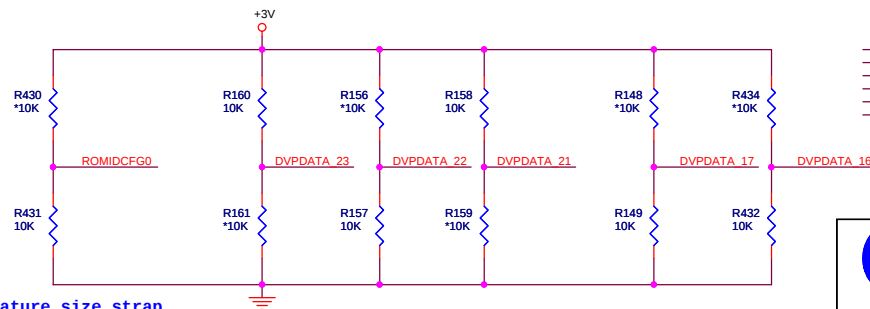
VGA



STRAPS PIN

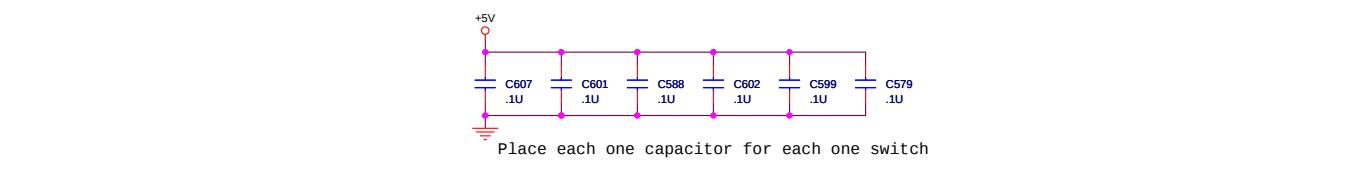
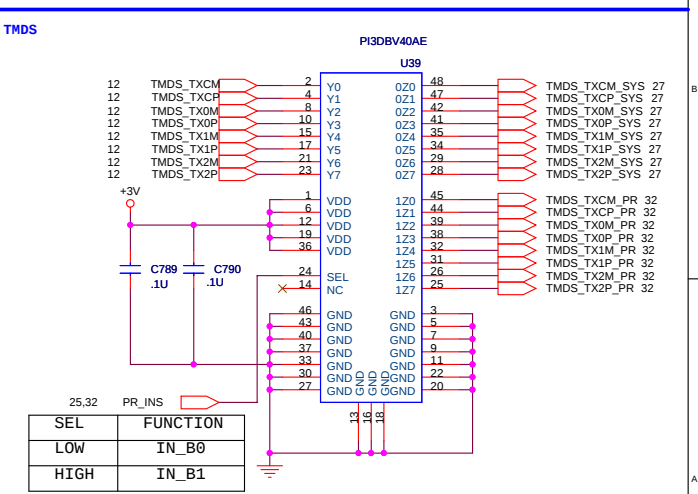
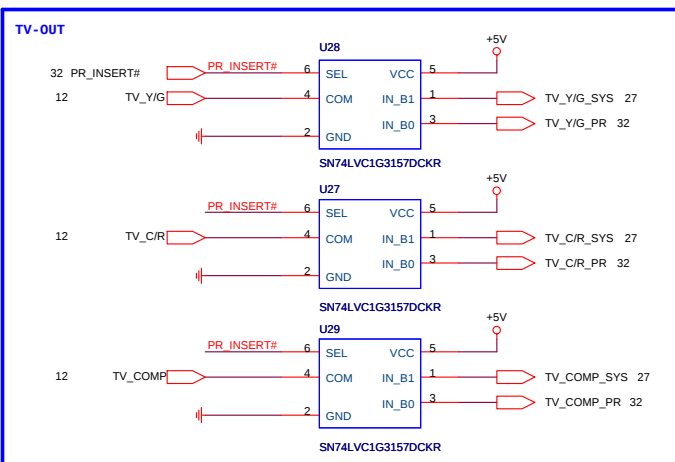
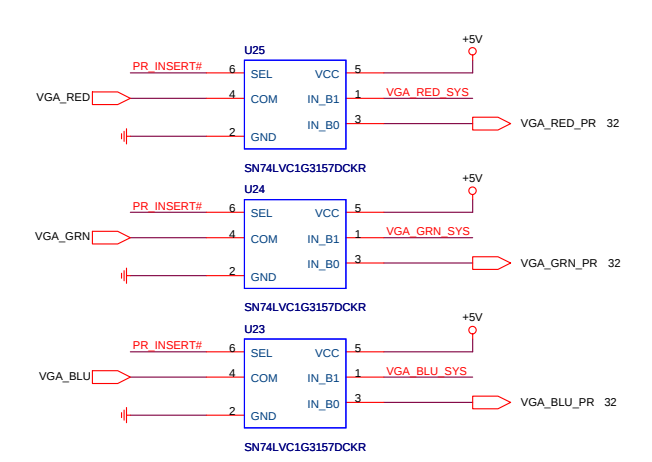
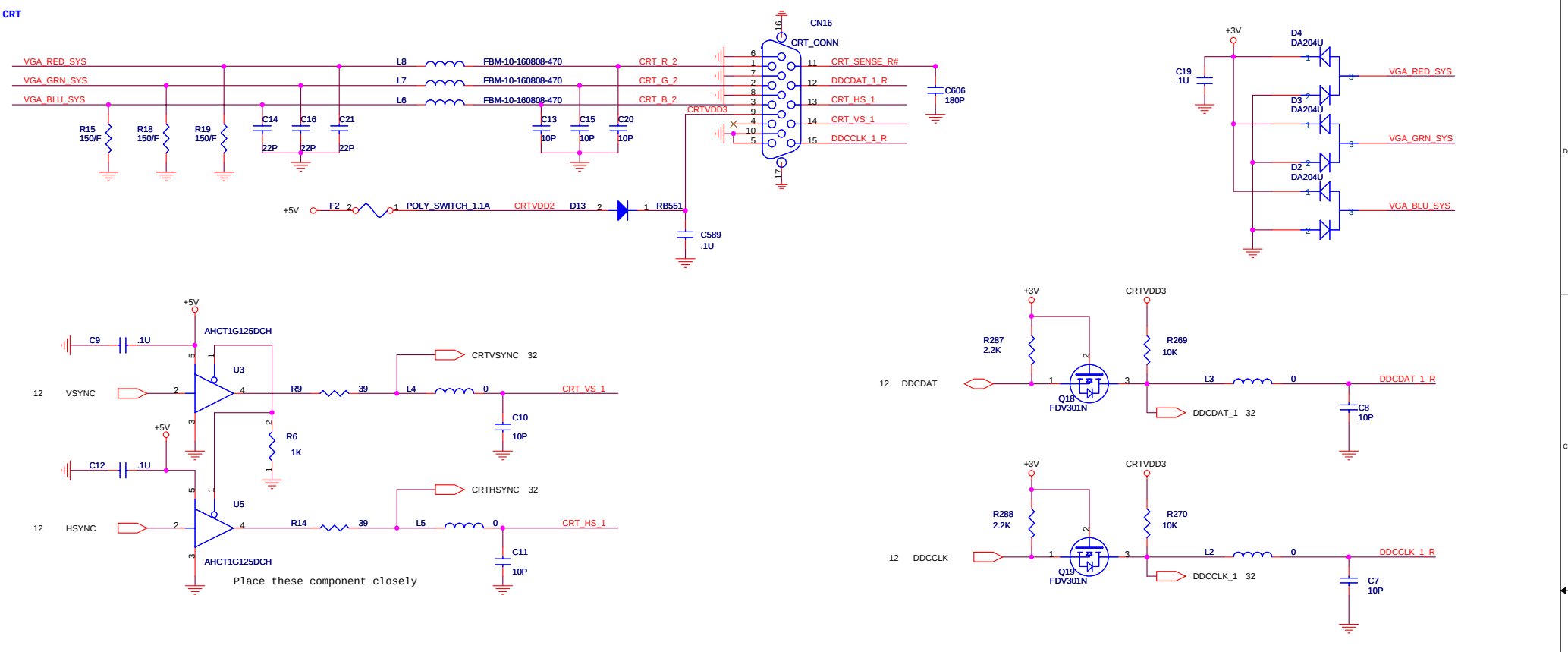
GPIO(9,13:11) INT P/D	ROMIDCFG
	0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 1000: Parallel ROM, Chip ID'S from ROM 1000: Parallel ROM, Chip ID'S from ROM
DVPDATA_21-23 MEM TYPE	DVPDATA_21: 0=4Mx32 1=8Mx32 DVPDATA_22: 0=128M 1=64M DVPDATA_23: 0=Hynix 1=Samsung Default Samsung 128M

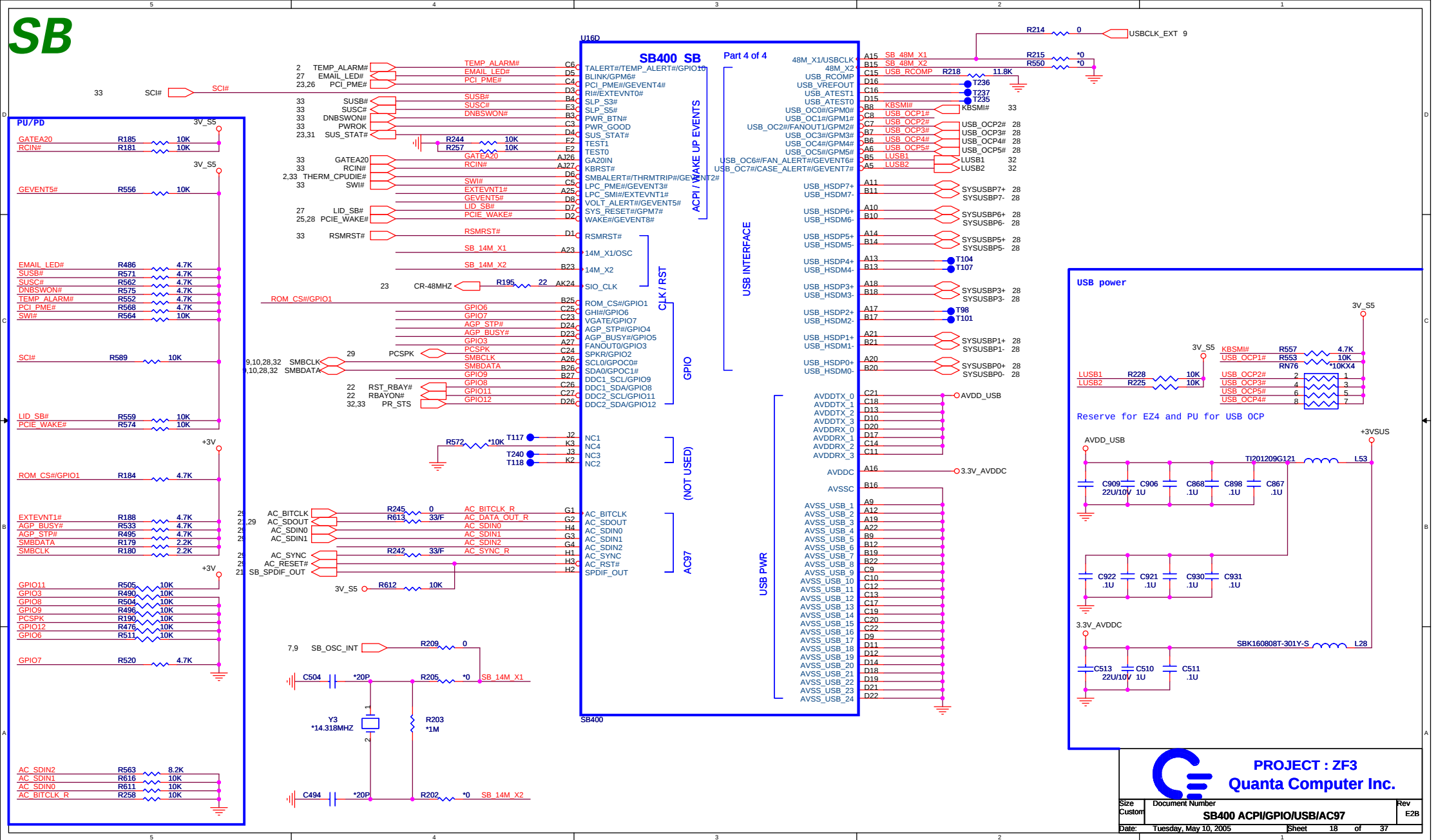
ROMID1 is aperture size strap
0: 128M
1: 256M

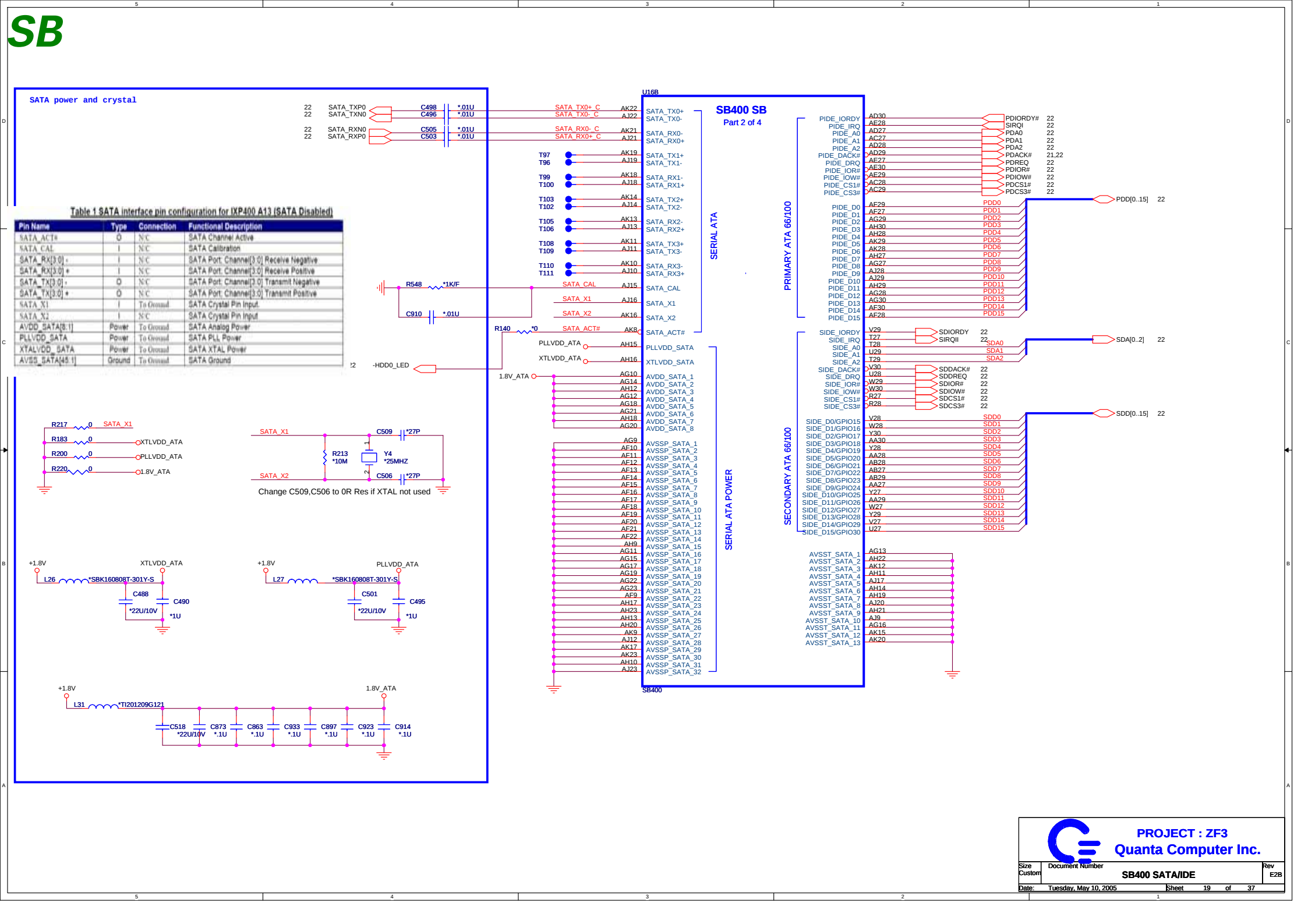


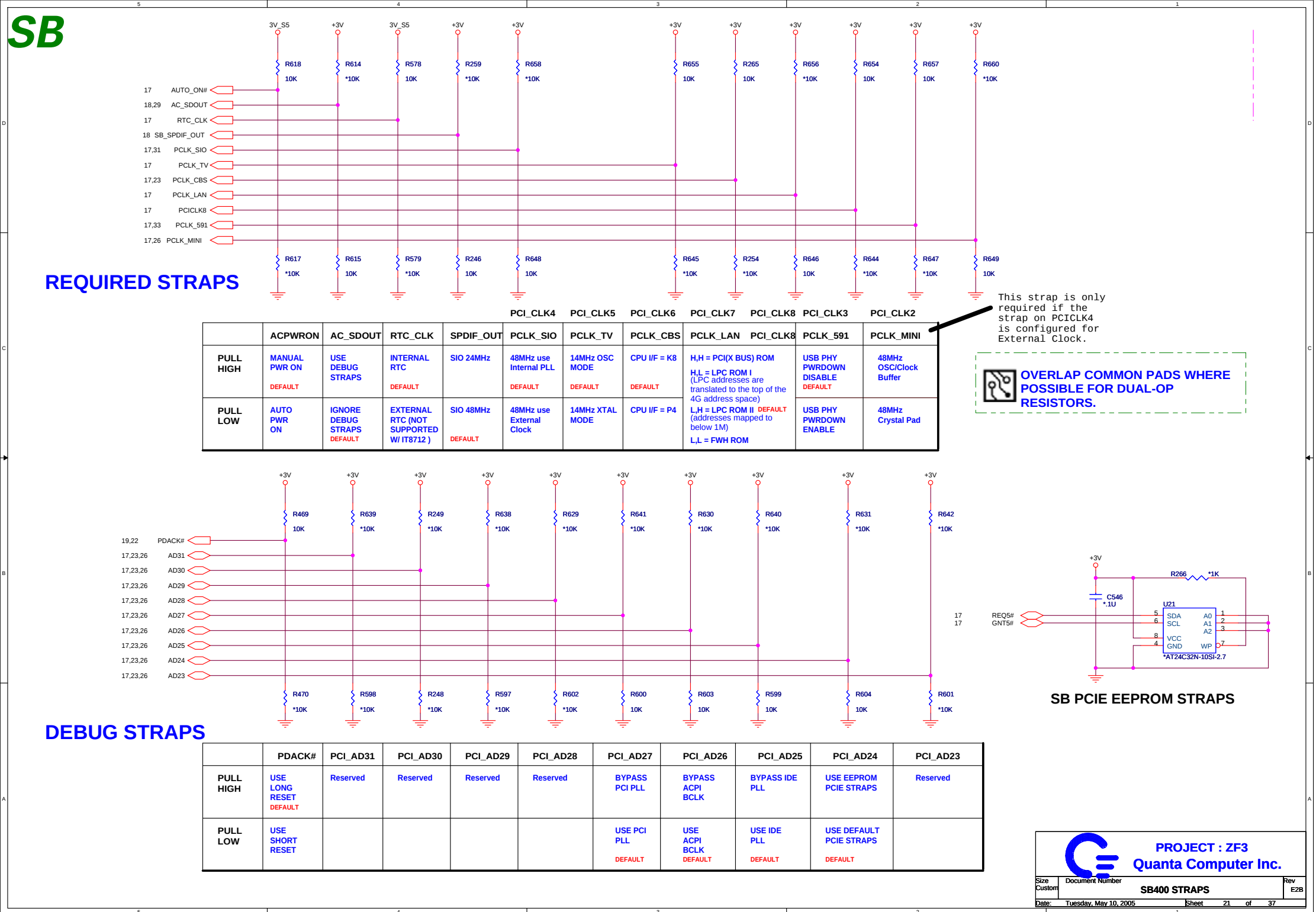
**PROJECT : ZF3**
Quanta Computer Inc.

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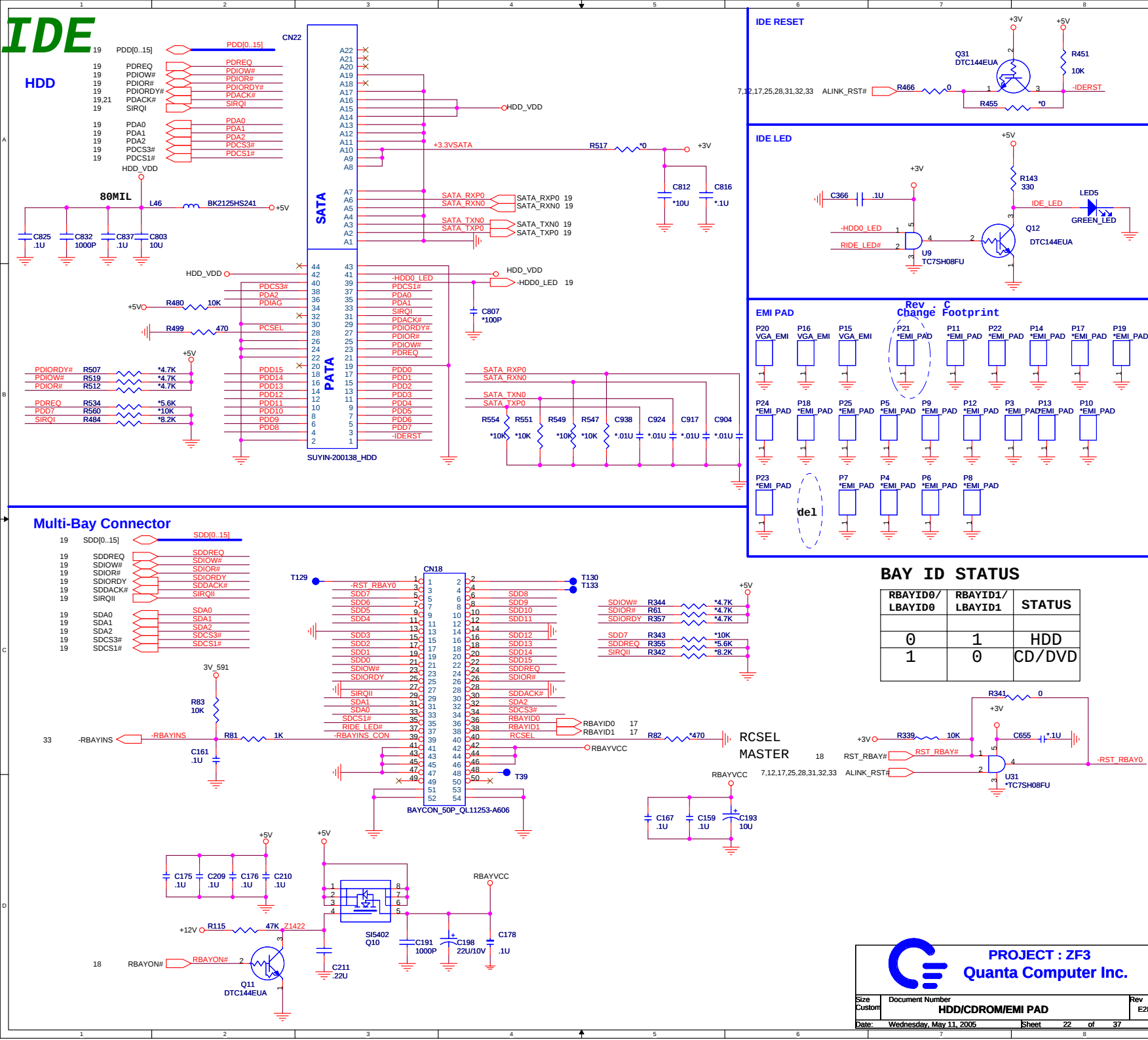




This strap is only required if the strap on PCI_CLK4 is configured for External Clock.

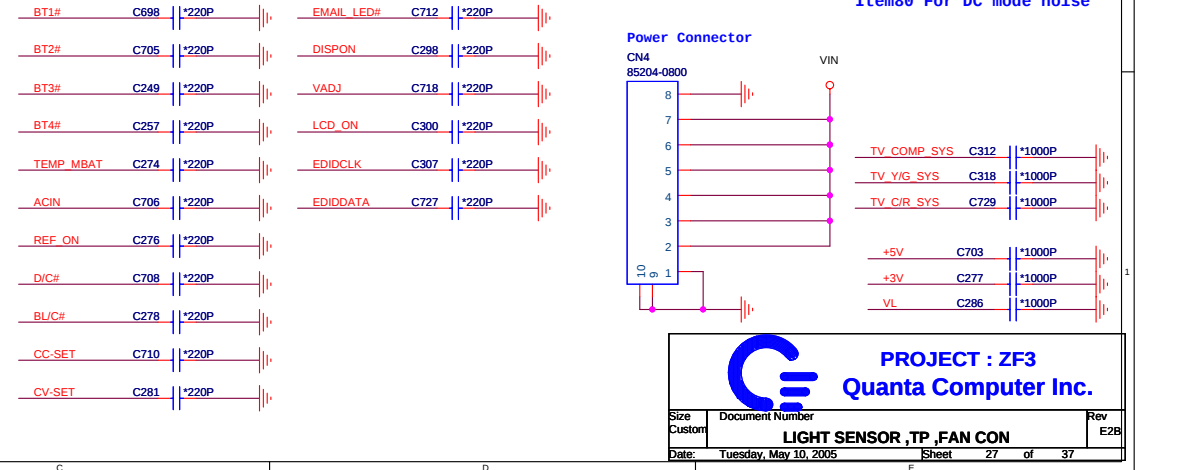
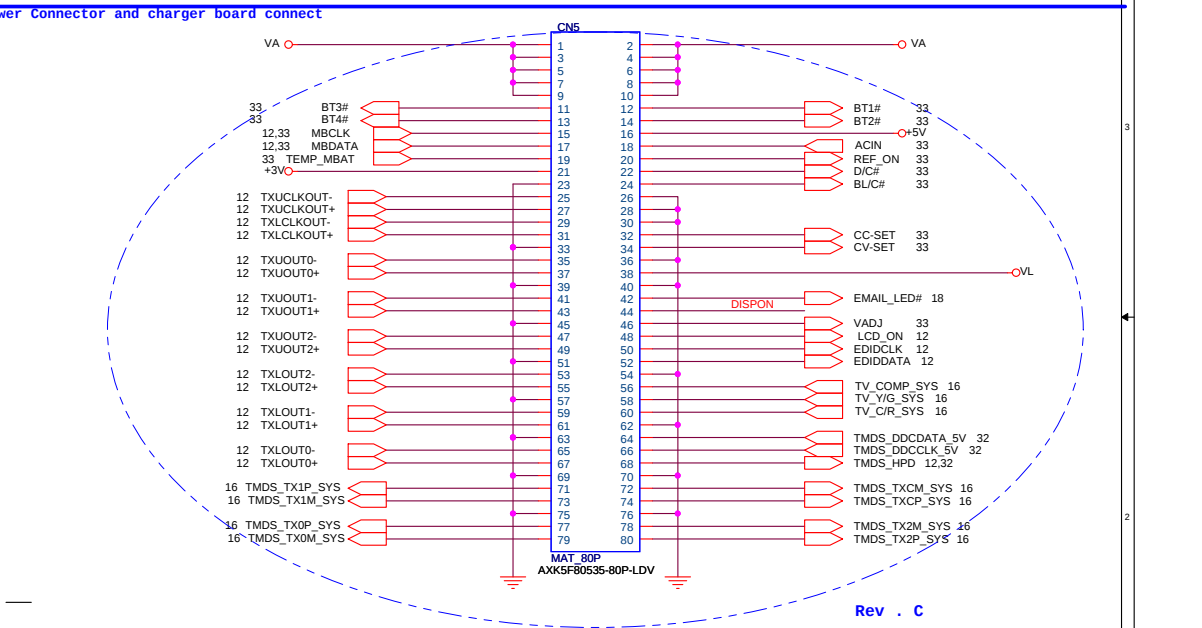
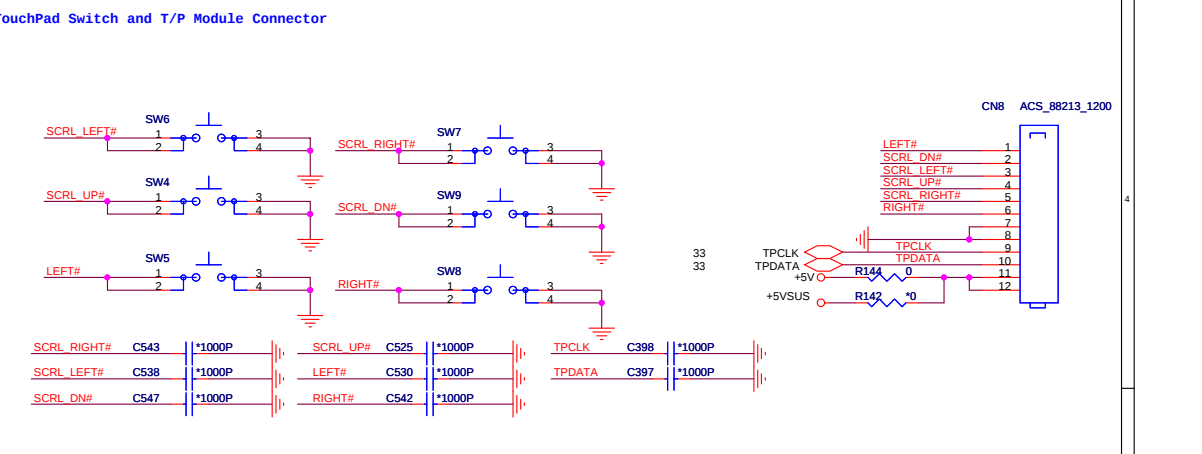
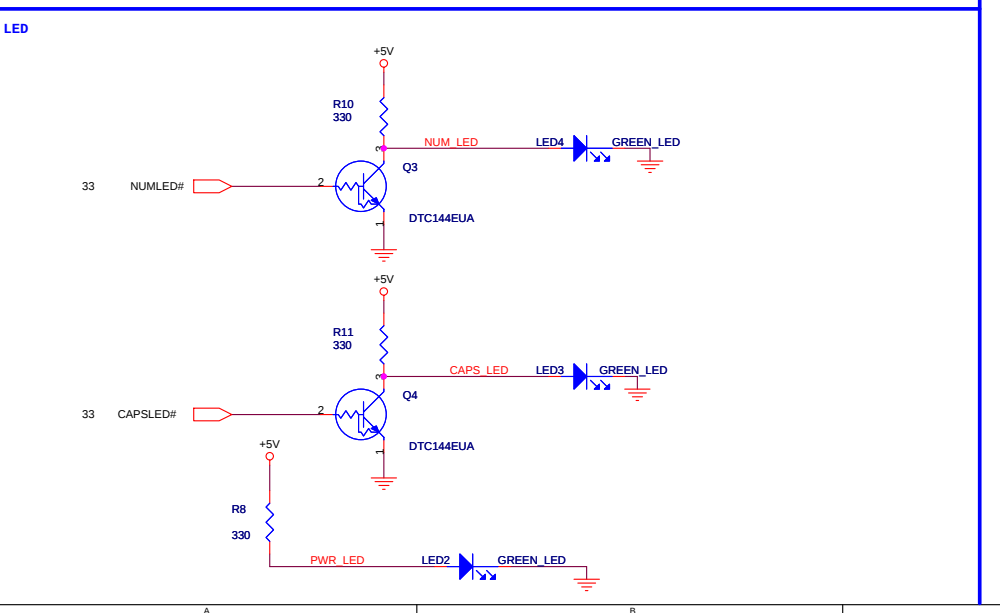
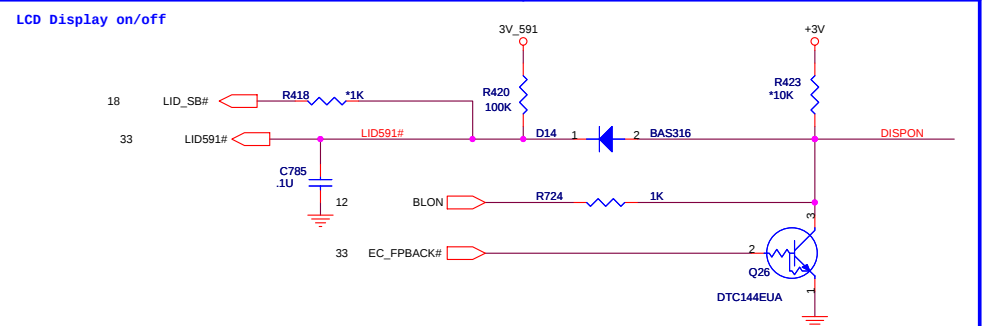
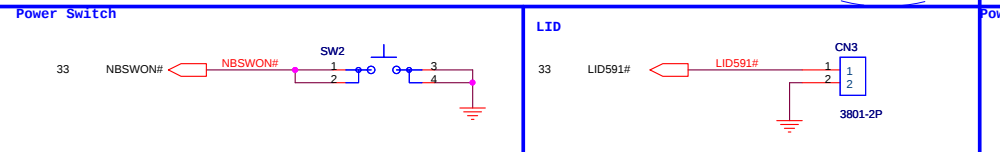
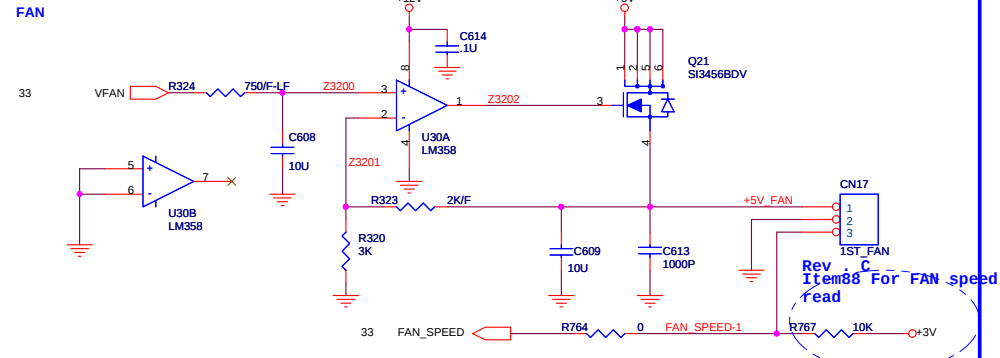


OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



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MISC



[illegible]

SPDIF

32 SPDIF_OUT_PR

30 SPDIF_OUT_HP

R240 0

R237 0

SPDIF_OUT

BEEP

+3V

+3V

U19
SN74LVC1G86DCKR

23 PCMSPK

18 PCSPK

U17
SN74LVC1G08DCKR

33 SYSSPKOFF#

C520 .1U

C514 .1U

R223 10K

R224 10K

PCBEEP

[illegible]

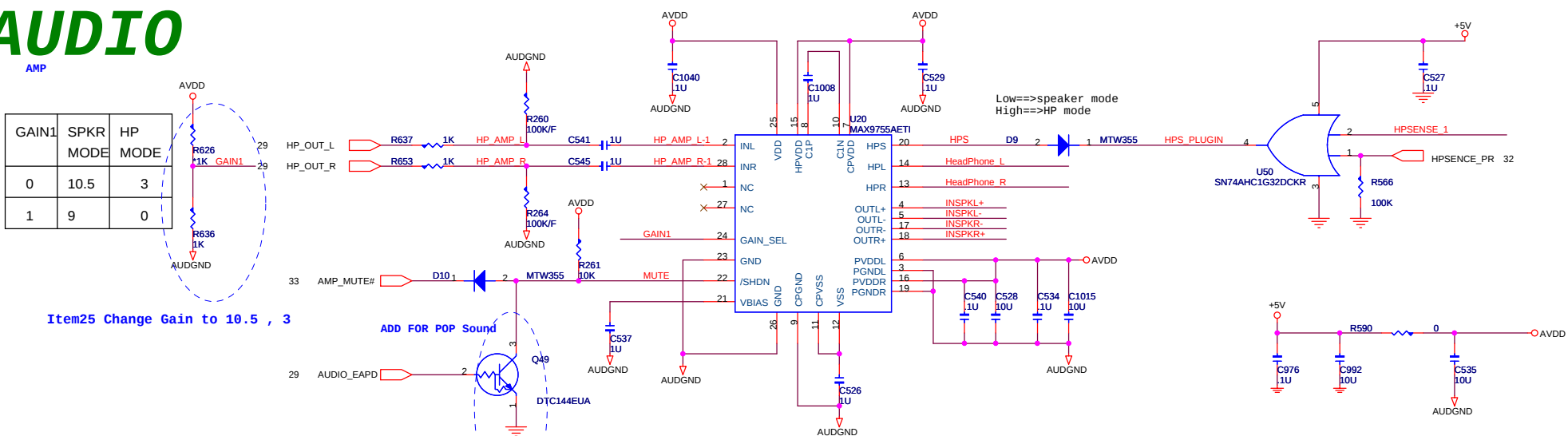
AUDIO

AMP

GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0

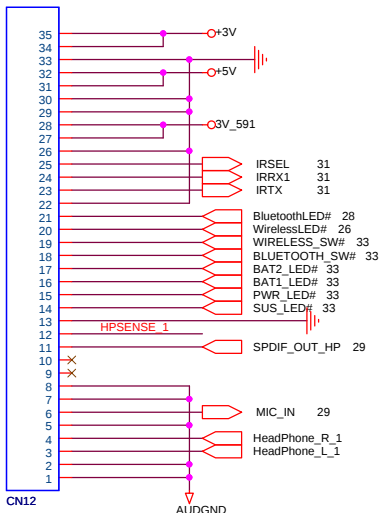
Item25 Change Gain to 10.5 , 3

ADD FOR POP Sound

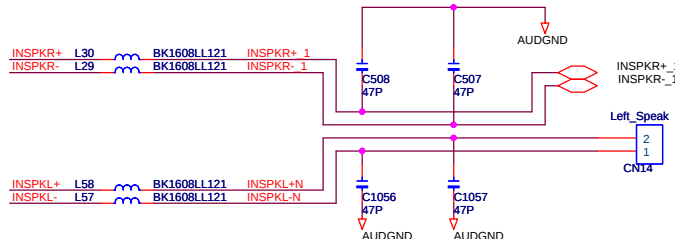


Audio conn

ACES_88060_3500



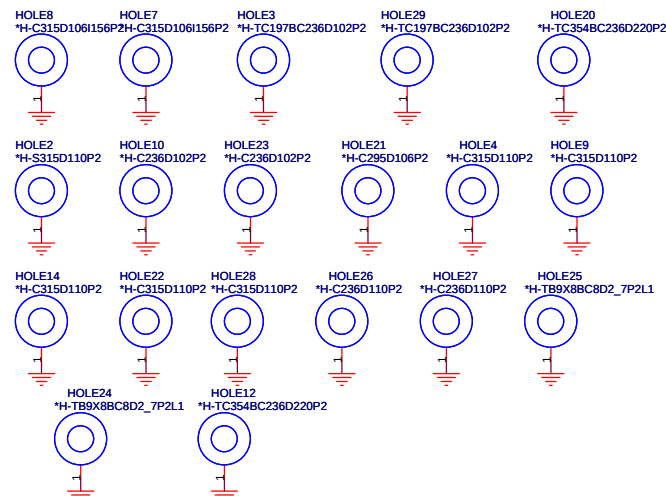
Internal speaker



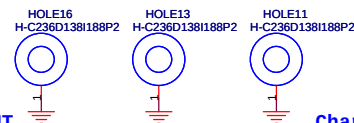
Headphone



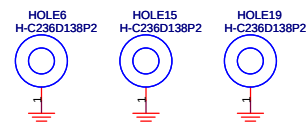
HOLE



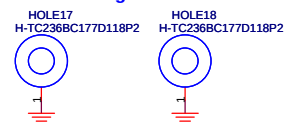
CPU NUT



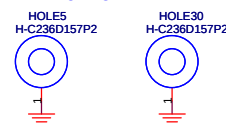
Thermal NUT



Charger board NUT



MDC NUT





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