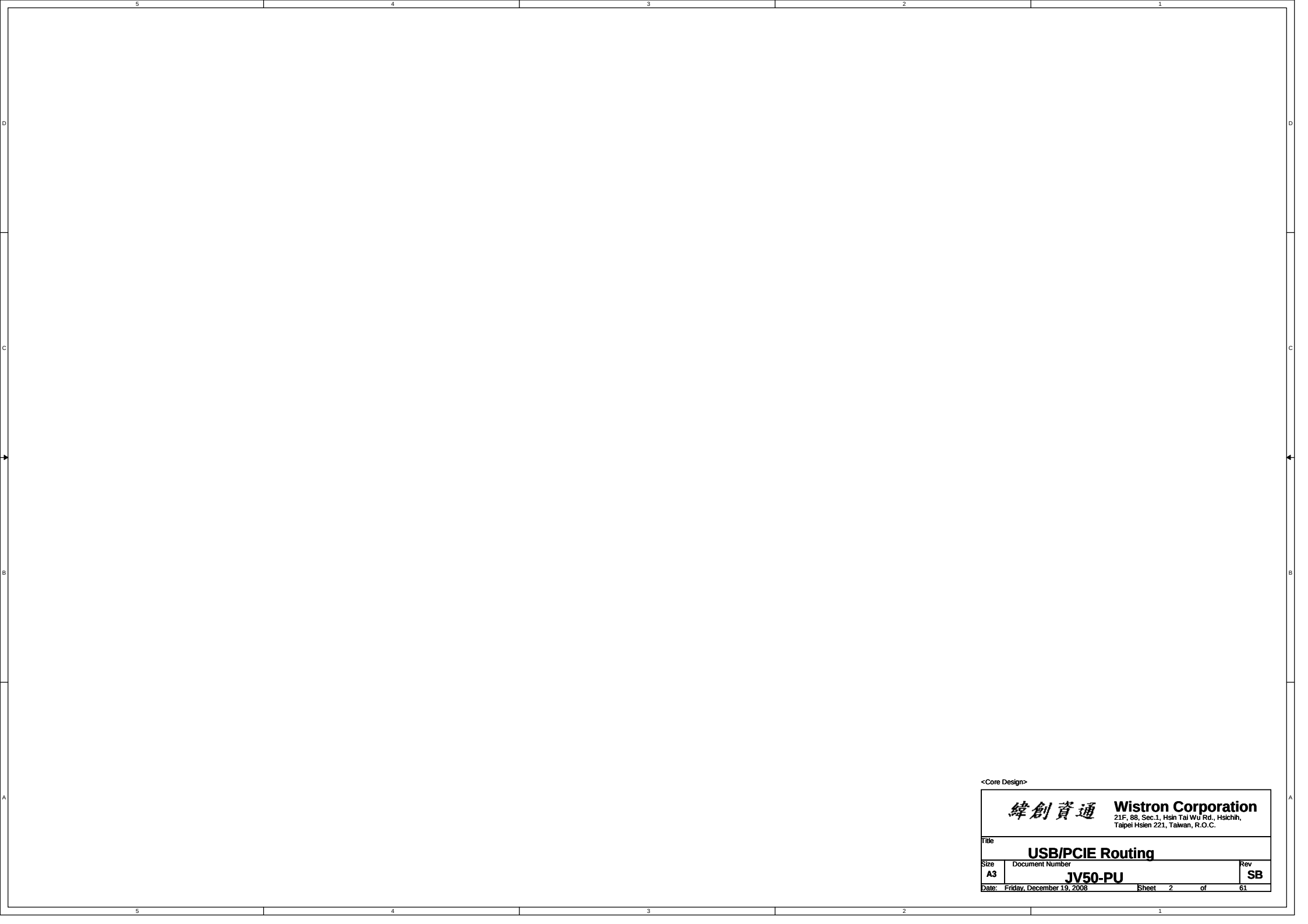
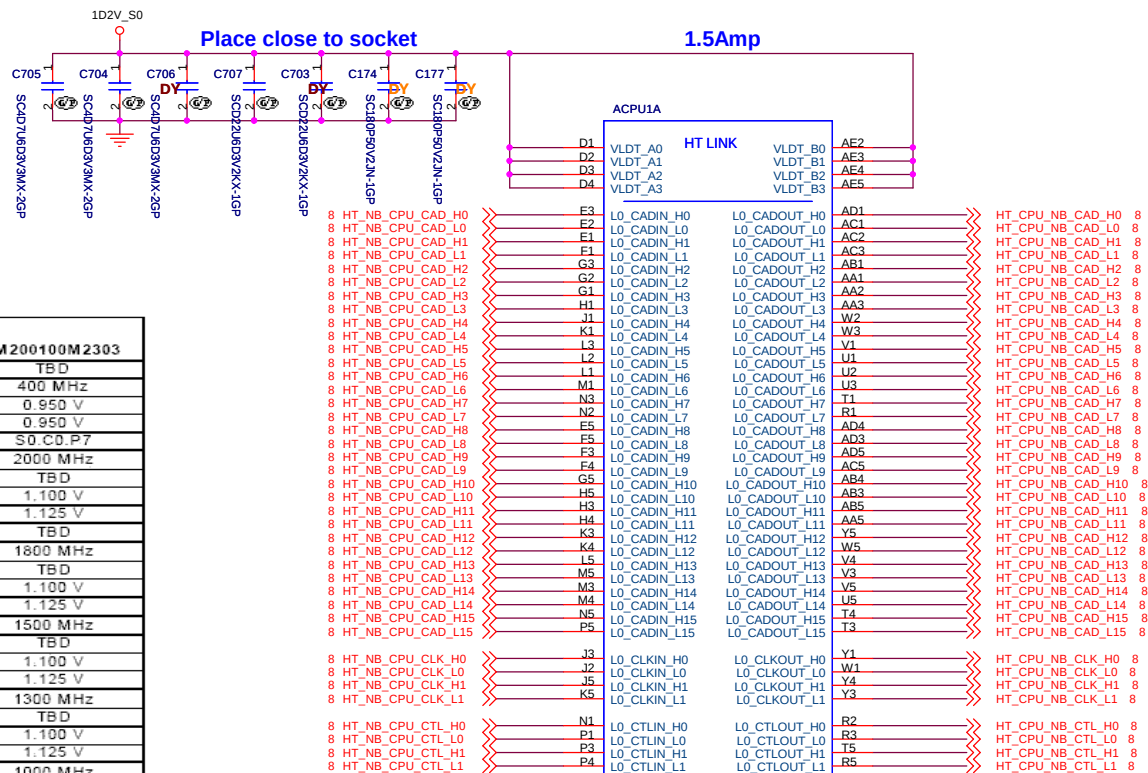


Sheet 1 of 6



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
USB/PCIE Routing		
Size	Document Number	Rev
A3	JV50-PU	SB
Date: Friday, December 19, 2008	Sheet 2 of	61



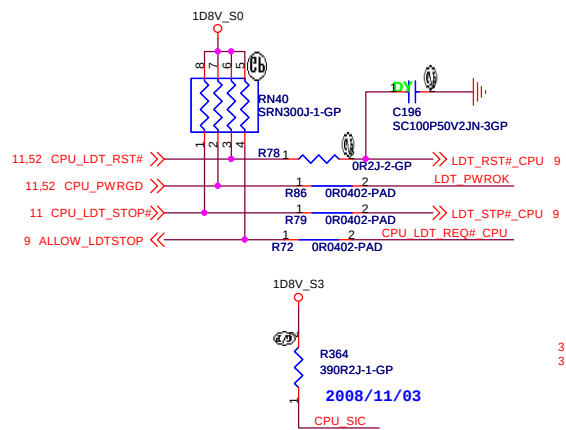
State	Specification	Notes	ZM200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V

SKT-CPU638P-GP-U2
62.10055.111
2ND = 62.10040.471 3RD = 62.10040.501
SKT - BGA638H176

<Core Design>

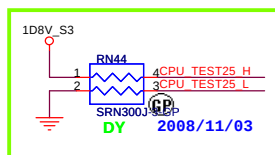
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU HT LINK I/F (1/4)		
Size A3	Document Number JV50-PU	Rev SB
Date: Friday, December 19, 2008 Sheet 4 of 61		

The Processor has reached a preset maximum operating temperature. 100°C
I=Active HTC
O=FAN

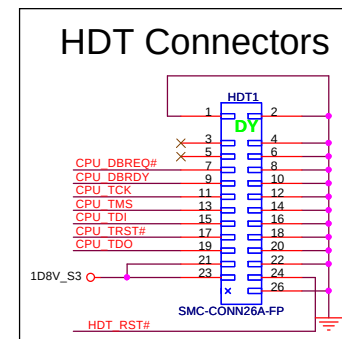
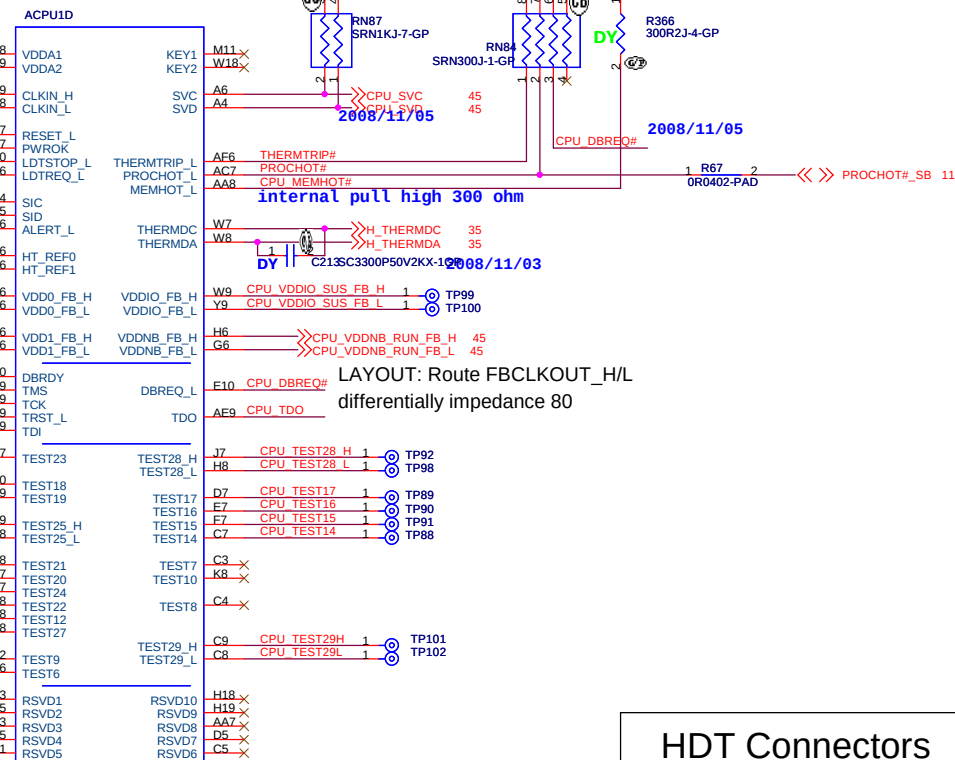
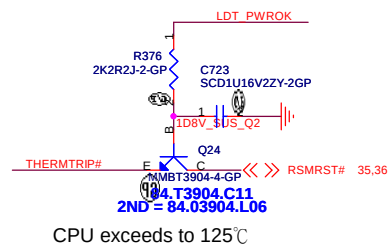
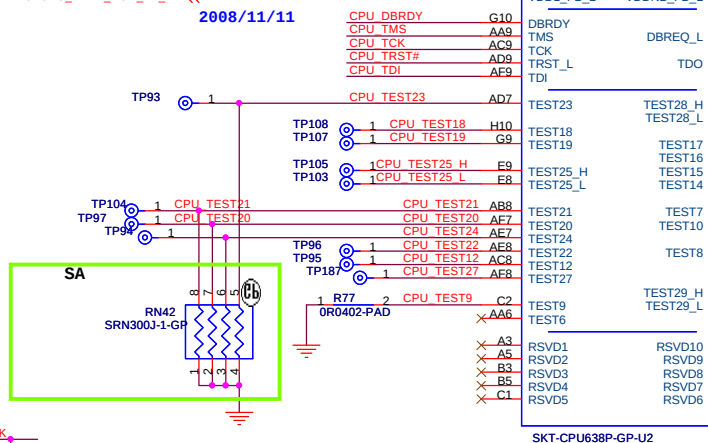
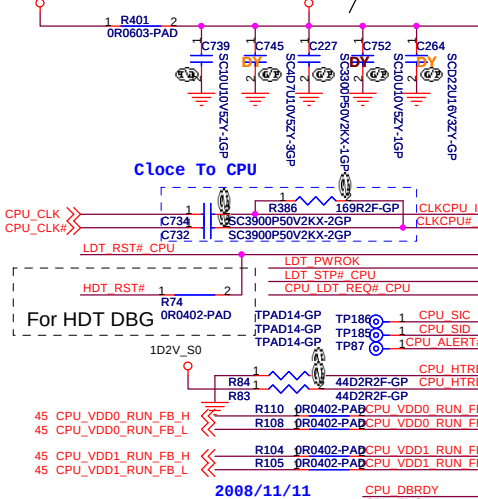
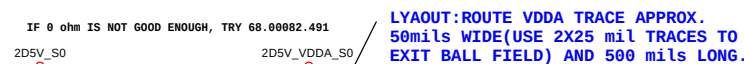
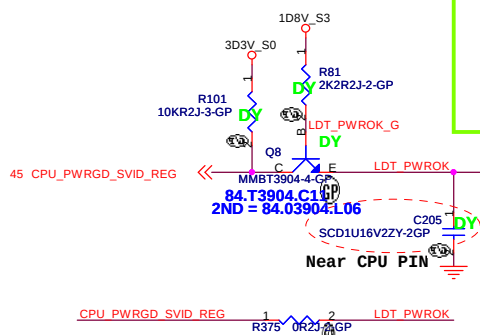
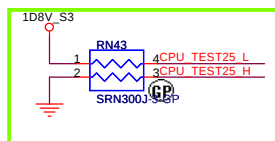


For leverage S1g3, please reserve 300 ohm resistor pullup to VDDIO.

For leverage S1g3, please reserve
300 ohm resistor pulldown to VSS



SA

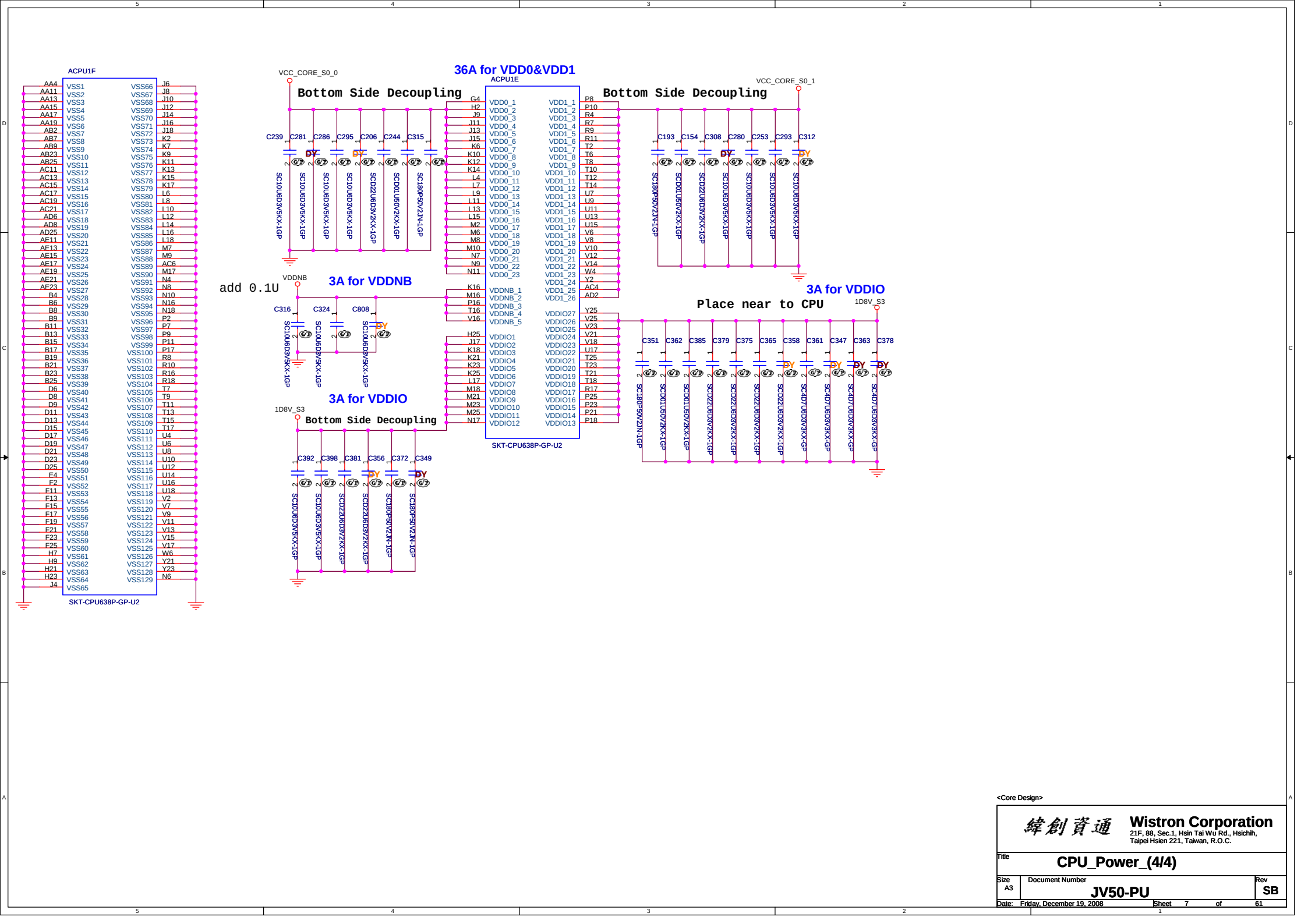


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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_Control&Debug_(3/4)
-------	------------------------------------

Size A3	Document Number JV50-PU	Rev SE
Date: Friday, December 19, 2008		Sheet 6 of 61

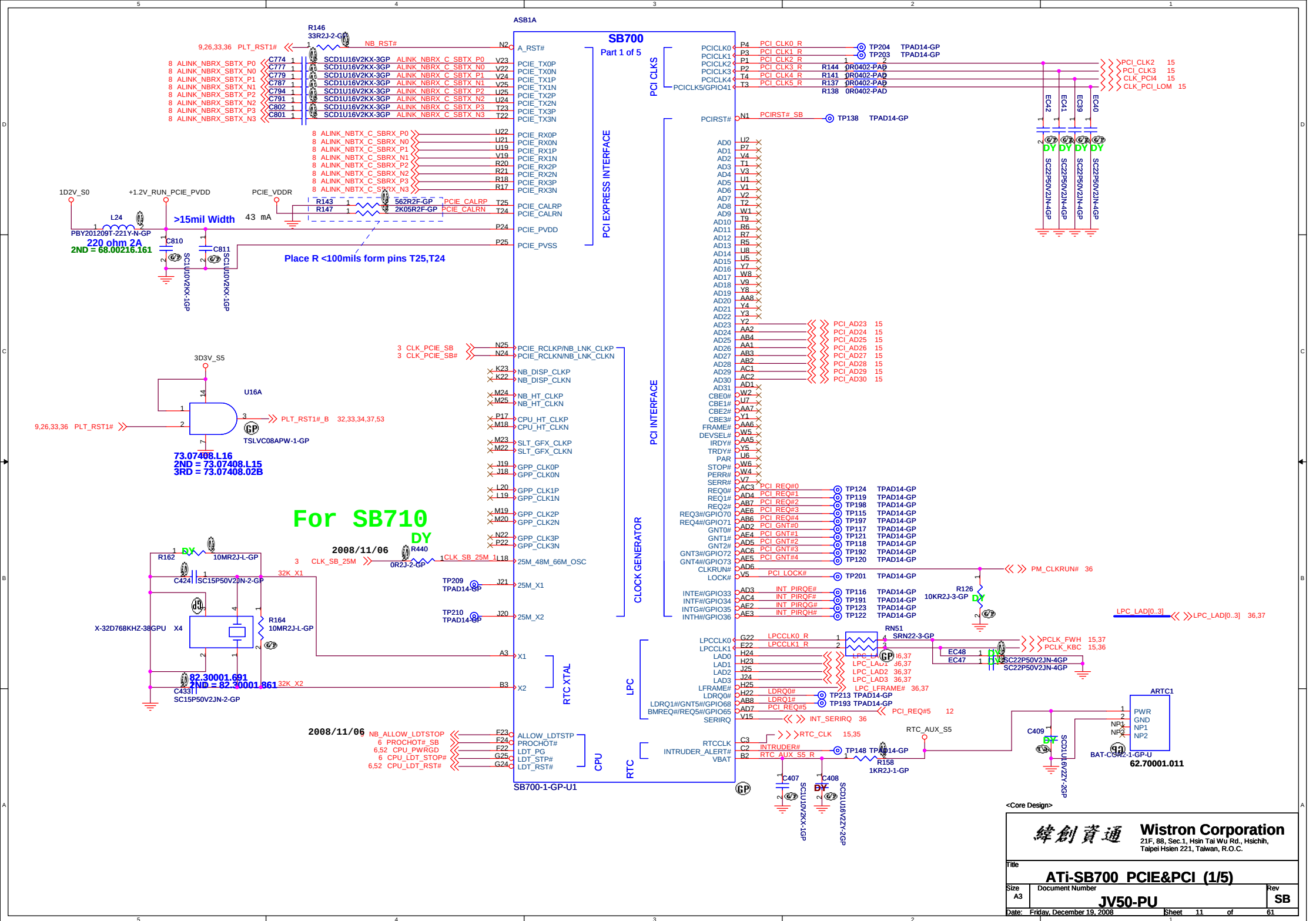


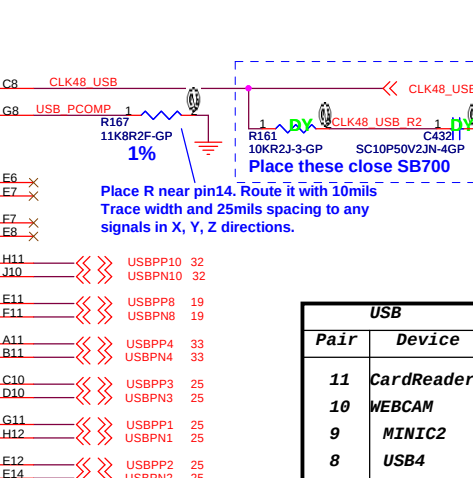
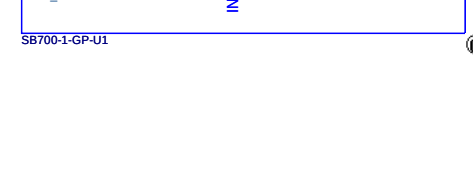
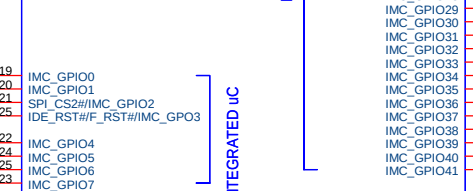
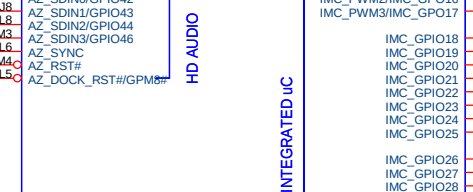
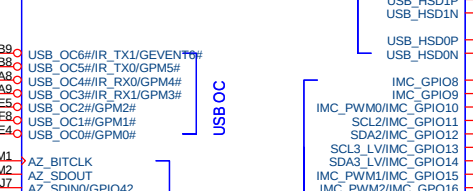
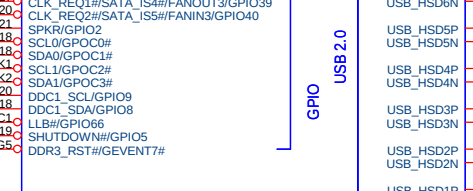
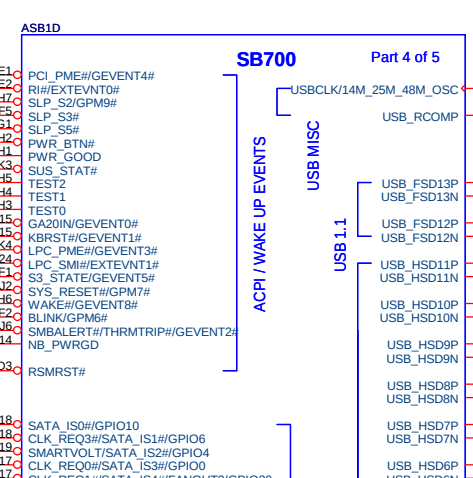
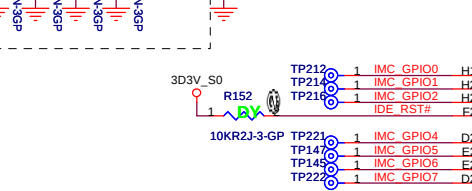
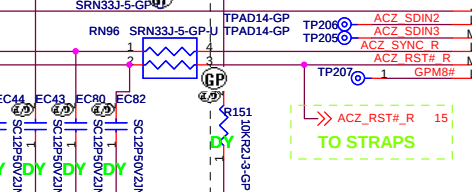
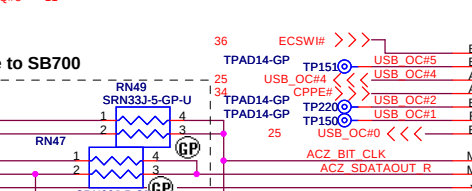
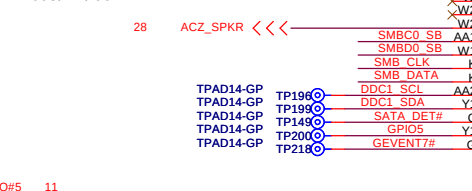
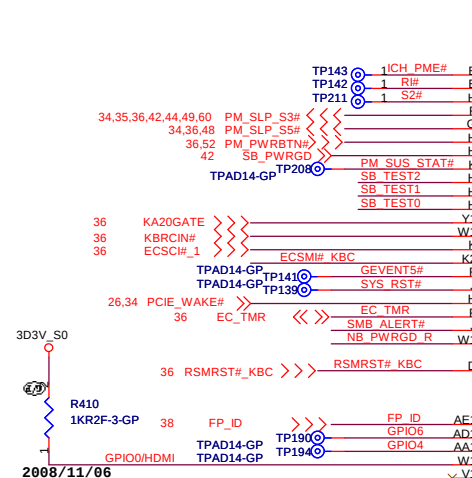
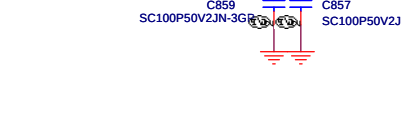
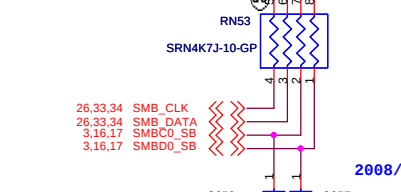
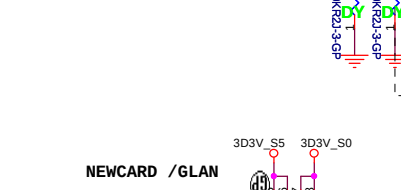
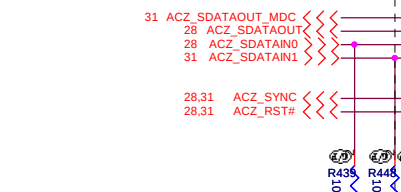
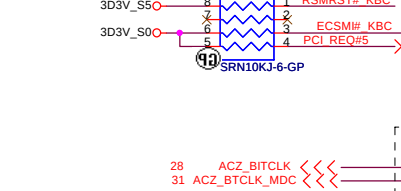
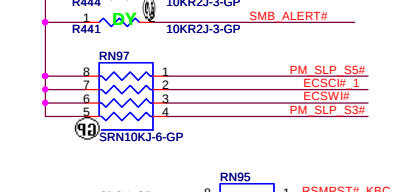
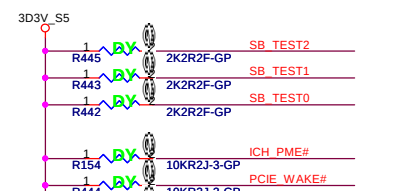
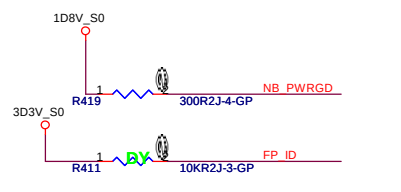
<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

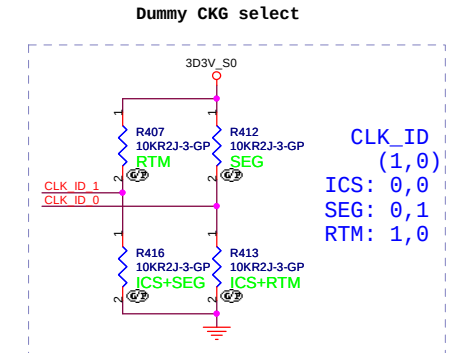
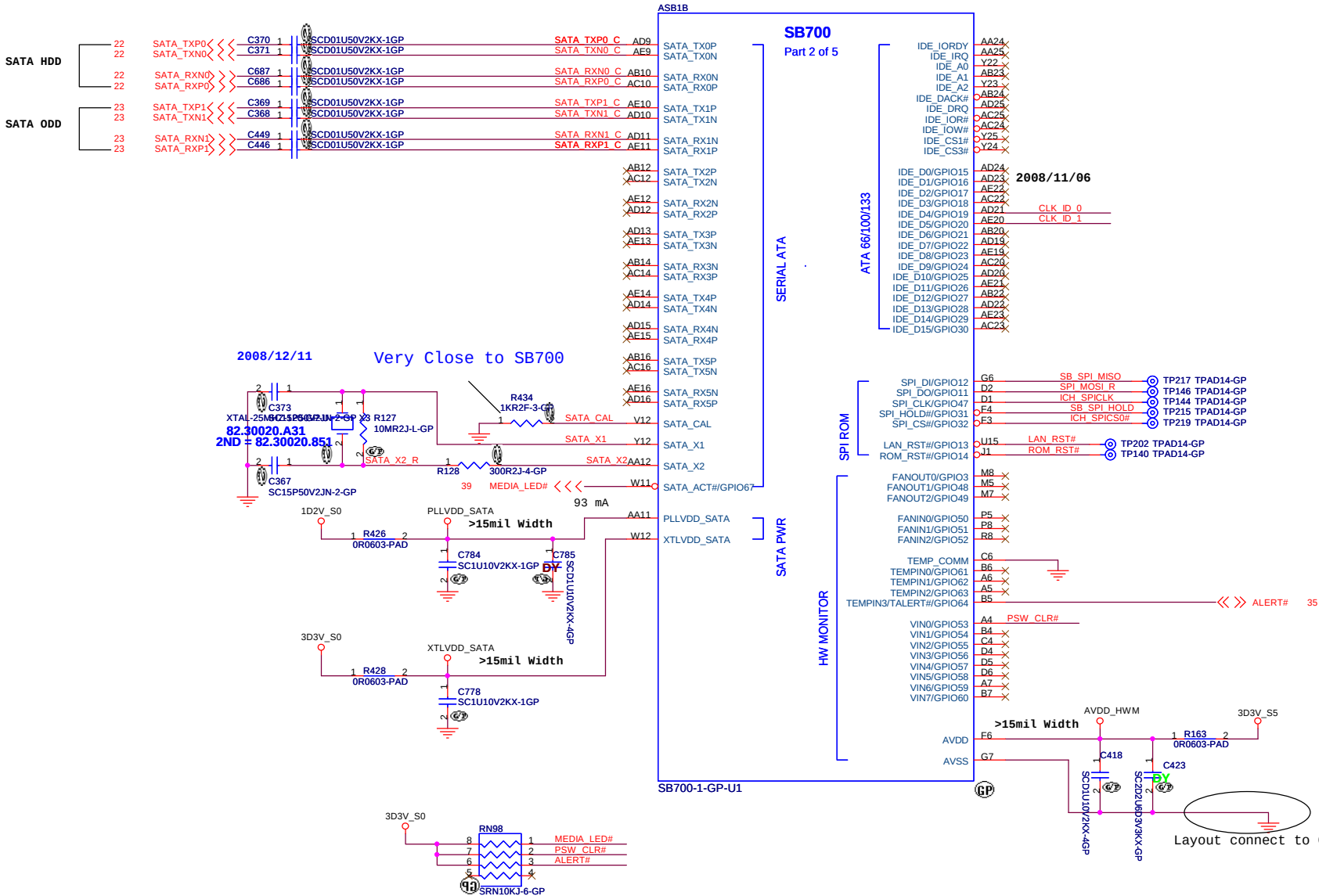
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Size	Document Number	Rev	
A3	JV50-PU	SB	
Date:	Friday, December 19, 2008	Sheet	7 of 61





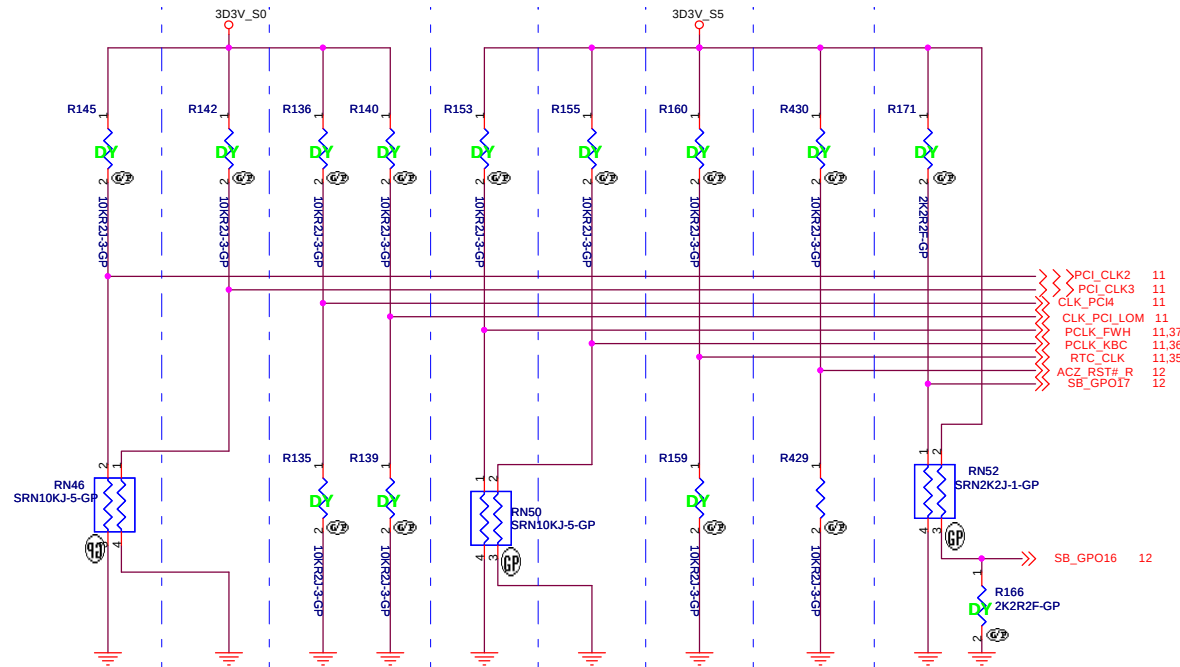


PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700



REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



DEBUG STRAPS

TPAD14-GP137	PCI_AD23	11
TPAD14-GP136	PCI_AD24	11
TPAD14-GP195	PCI_AD25	11
TPAD14-GP135	PCI_AD26	11
TPAD14-GP134	PCI_AD27	11
TPAD14-GP133	PCI_AD28	11
TPAD14-GP130	PCI_AD29	11
TPAD14-GP129	PCI_AD30	11

	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	RQM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

<Core Design>

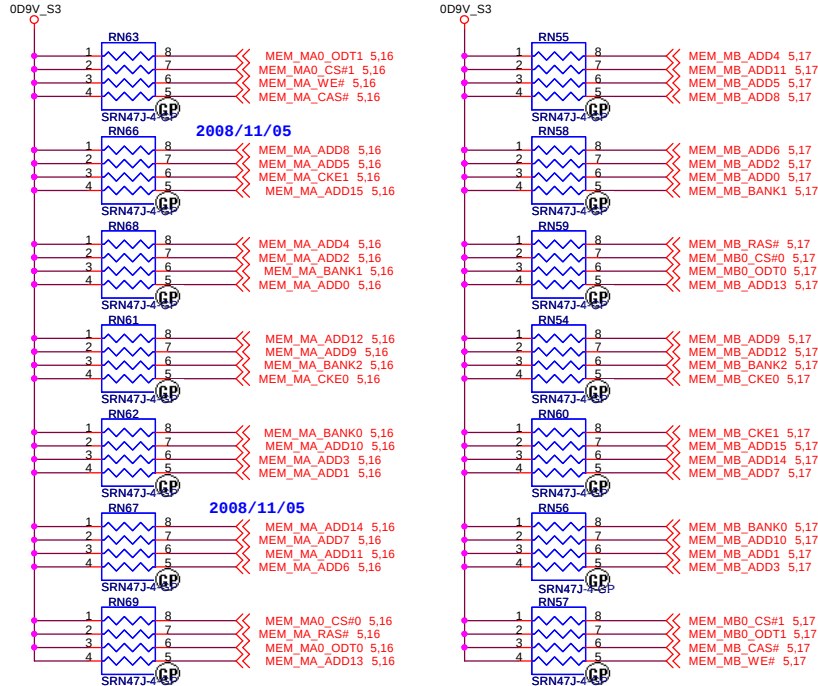
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			ATi-SB700 STRAPPING (5/5)		
Size	Document Number				Rev
A3	JV50-PU				SB
Date:	Friday, December 19, 2008	Sheet	15	of	61



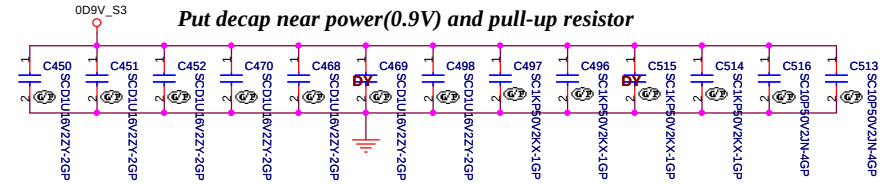
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

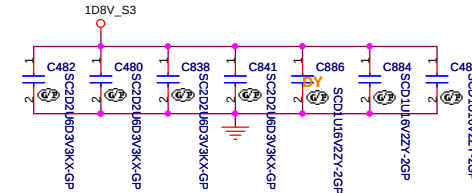


Do not share the Term resistor between the DDR address and Control Signals.

Decoupling Capacitor

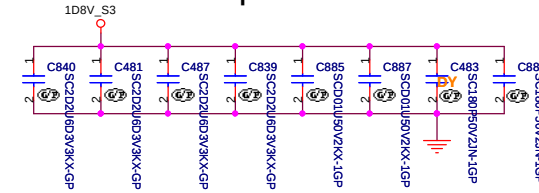


Place these Caps near DM1

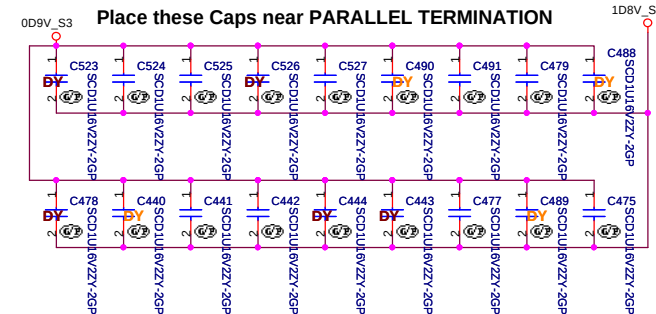


Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

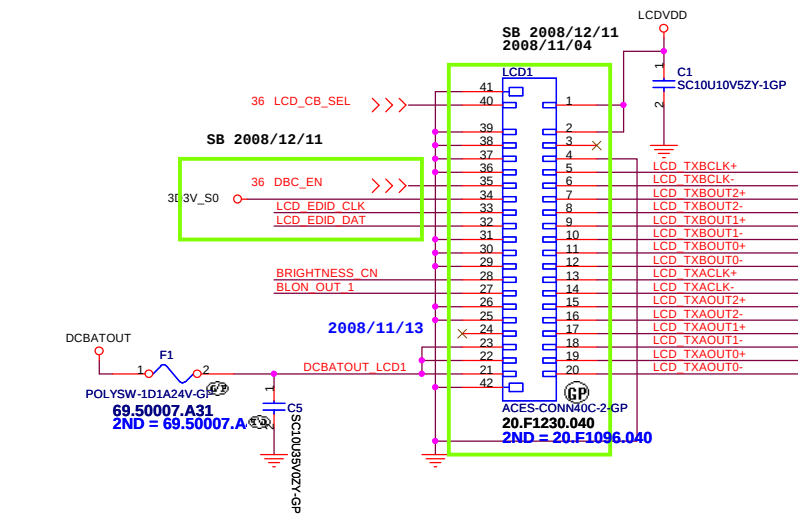


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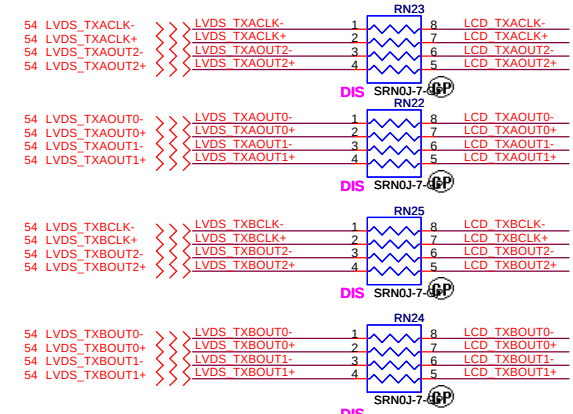
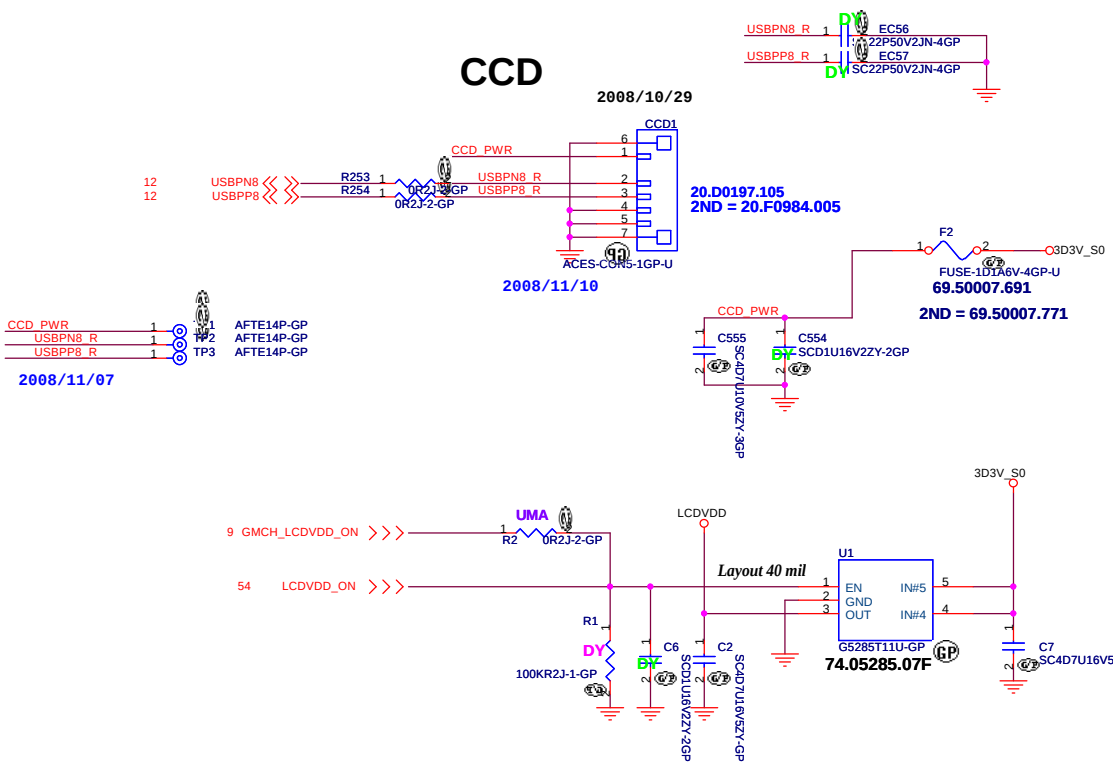
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			DDR DAMPING & TERMINATION
Size	Document Number	Rev	
A3	JV50-PU	SB	
Date:	Friday, December 19, 2008	Sheet	18 of 61

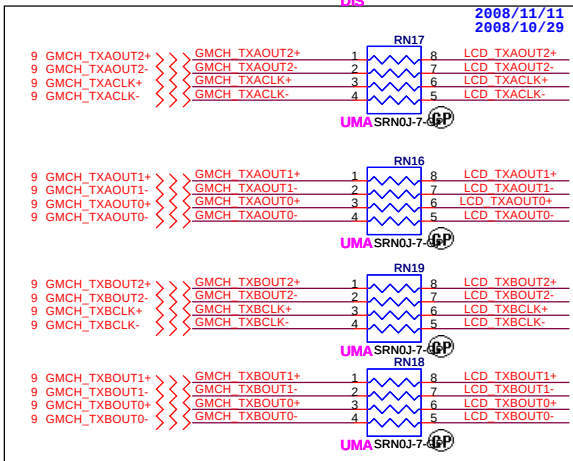
LCD/INVERTER/CCD CONN



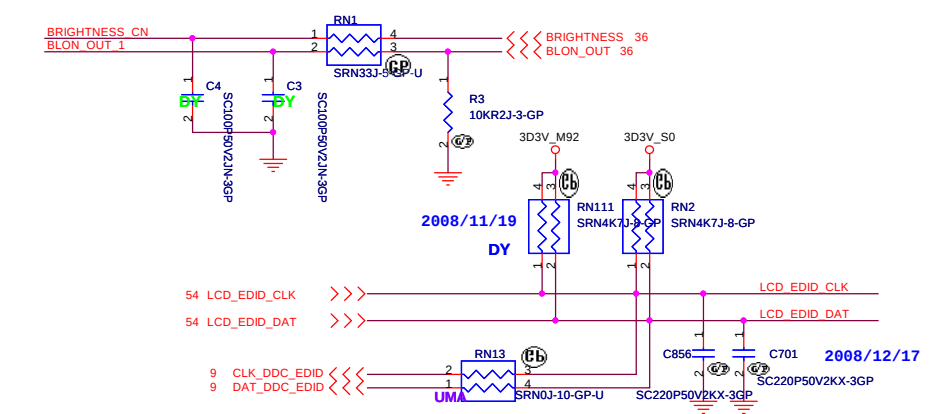
CCD



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND



CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



<Core Design>

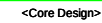
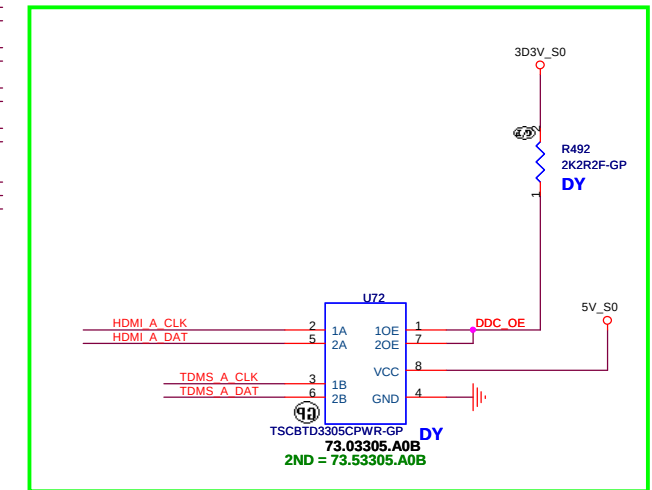
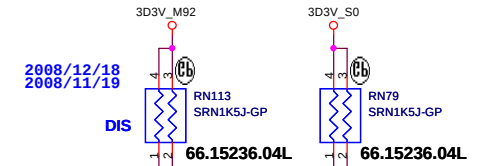
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
LCD CONN

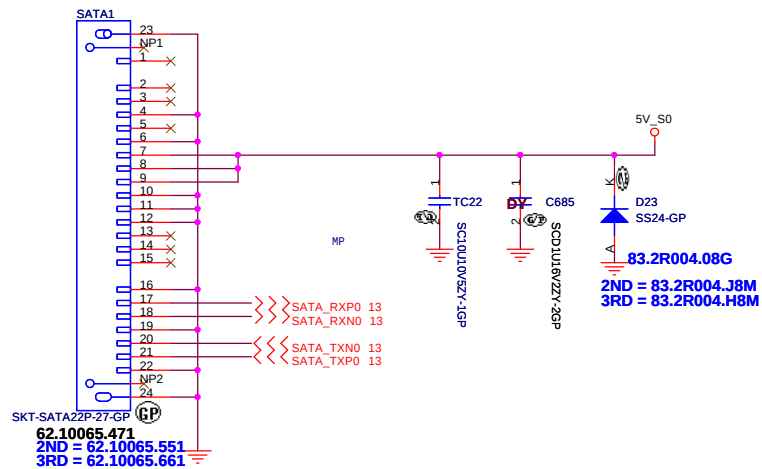
Size A3 Document Number
JV50-PU

Date: Friday, December 19, 2008 Sheet 19 of 61

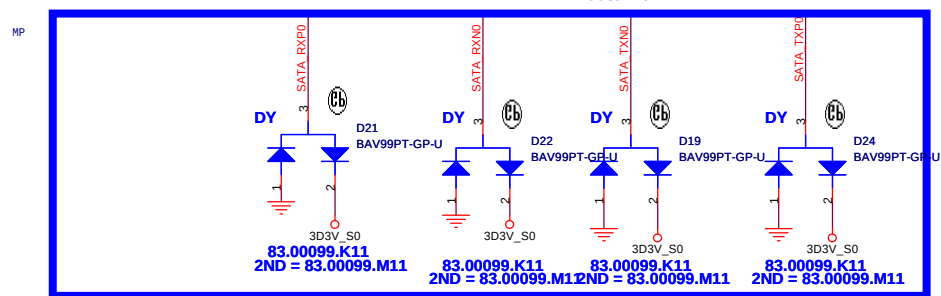
Rev SB



SATA Connector



2008/12/17



<Core Design>

緯創資通

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Date	Location	Notes
Title	Author	Date	Location	Notes

HDD

Size	Document Number
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JV50-PU

Date: Friday, December 19, 2008

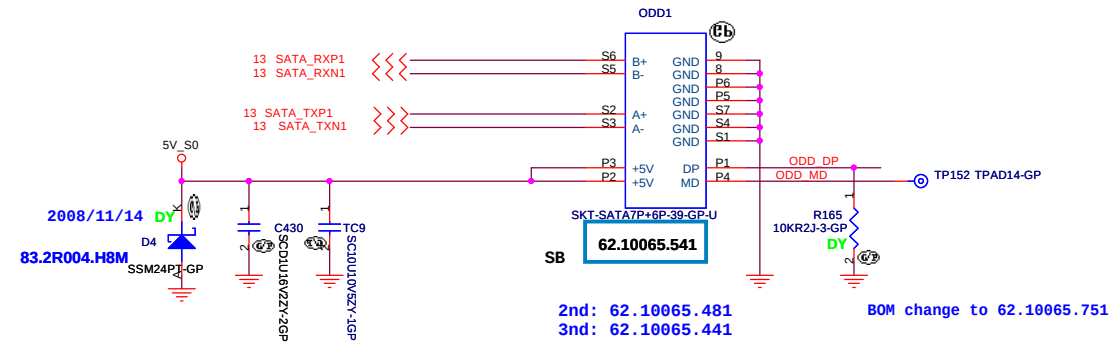
Sheet 22

of

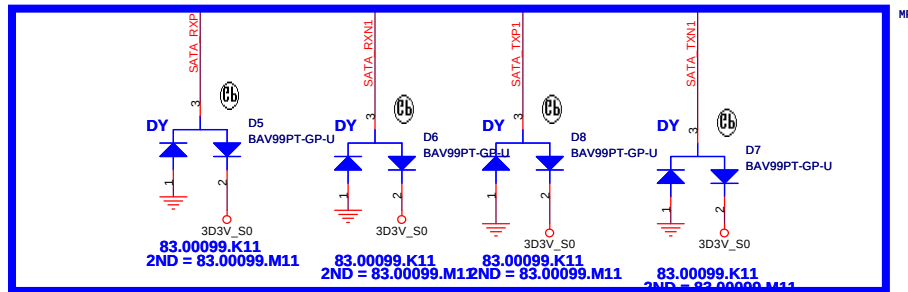
Rev	SB
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SATA ODD Connector

2008/11/12



2008/12/17



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

ODD

Size

Document Number

JV50-PU

Rev

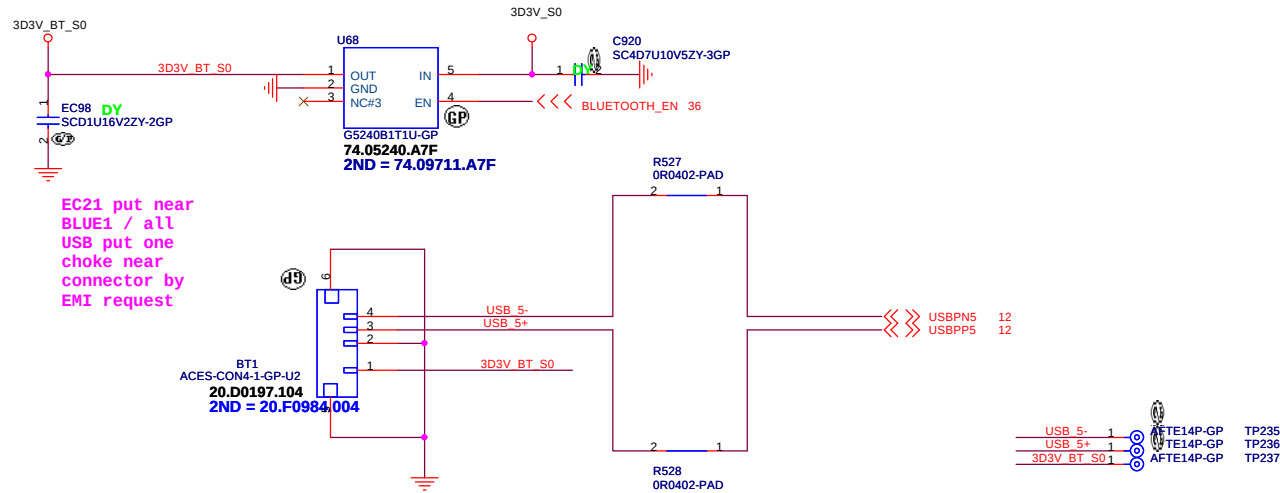
SB

Date: Friday, December 19, 2008

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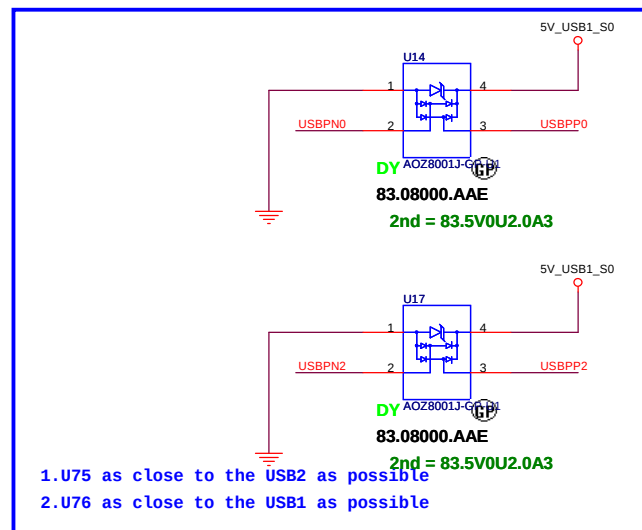
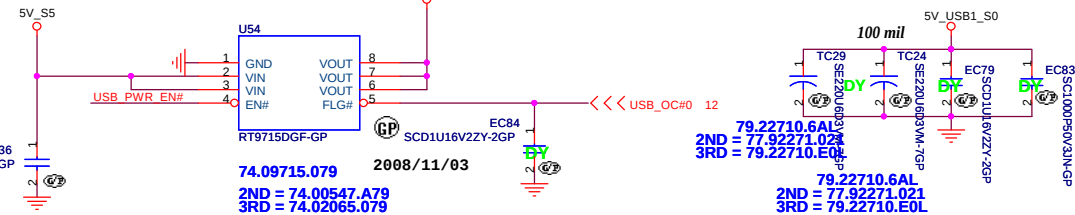
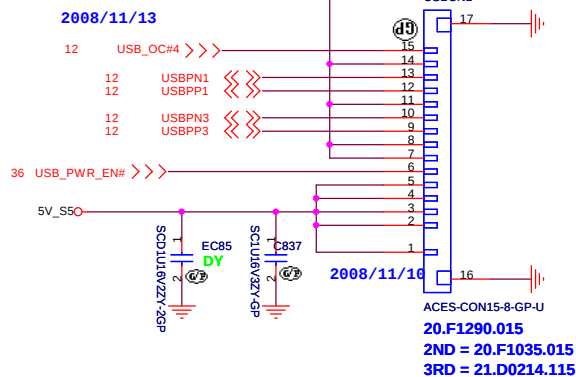
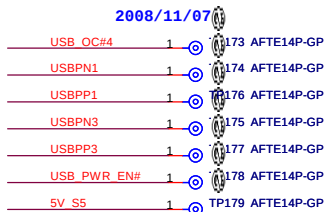
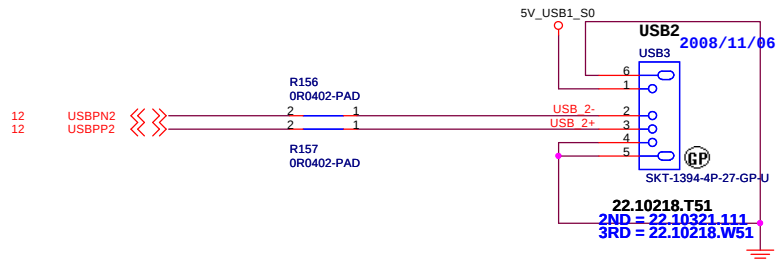
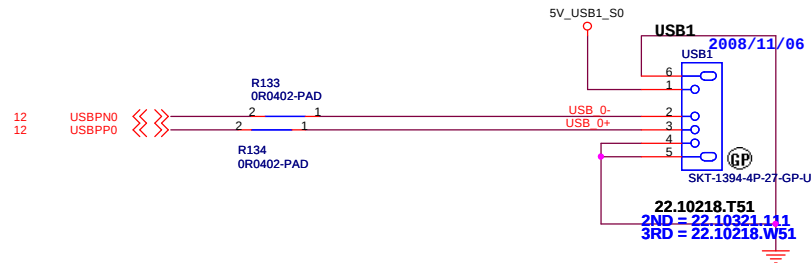
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			BLUETOOTH		
Size	Document Number				Rev
	JV50-PU				SB
Date:	Friday, December 19, 2008		Sheet	24	of 61



CO-Layout BCM5764 and BCM5784
modify BOM :71.05784.003

2008/10/28

2008/11/13

84.00069.B1B
2ND = 84.DCP69.01B
3RD = 84.00069.A1B

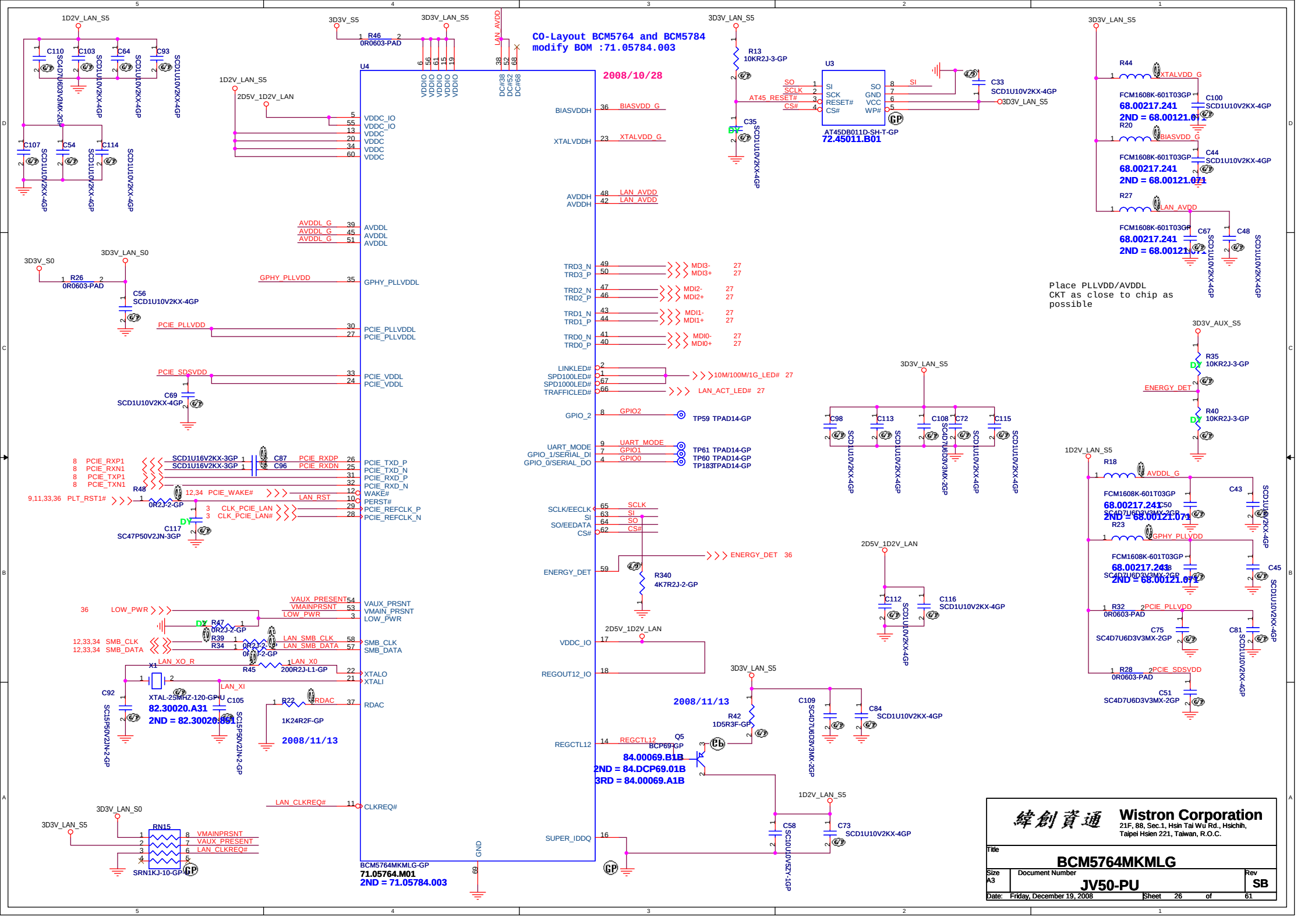
Place PLLVDD/AVDDL
CKT as close to chip as
possible

緯創資通

Wistron Corporation

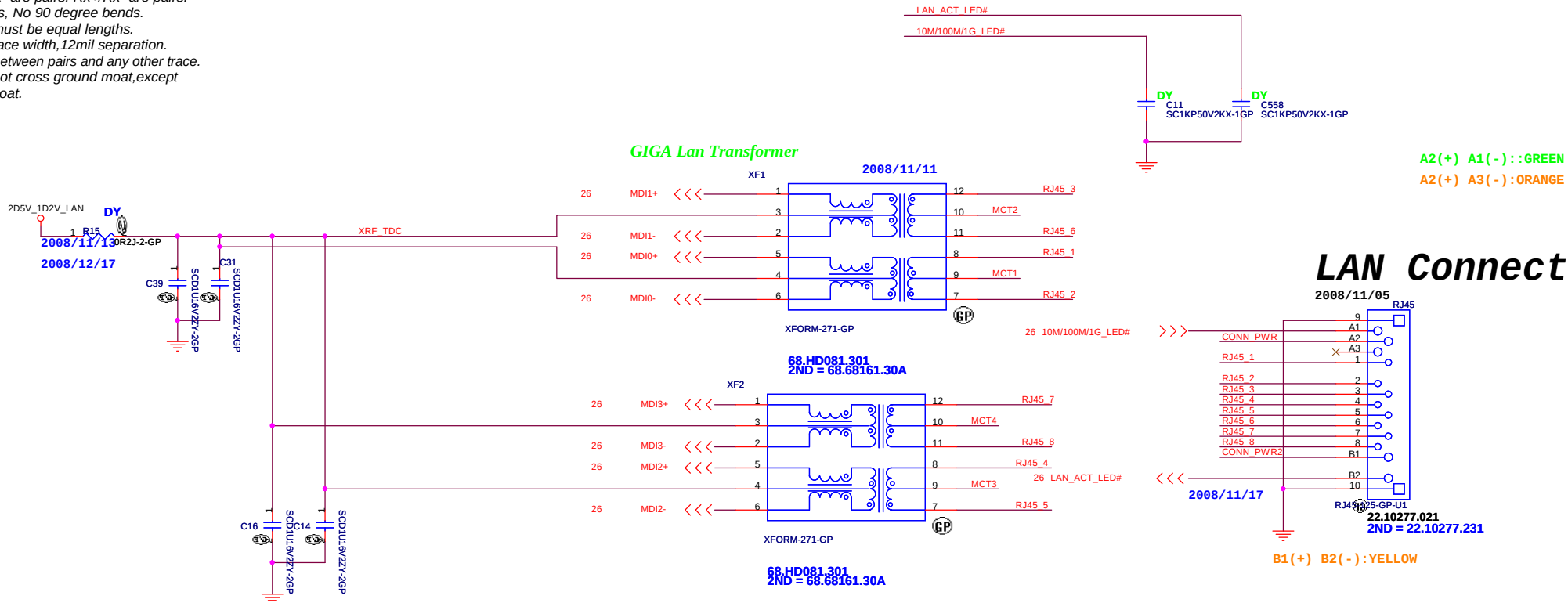
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			BCM5764MKMLG		
Size	Document Number			Rev	
A3	JV50-PU			SB	
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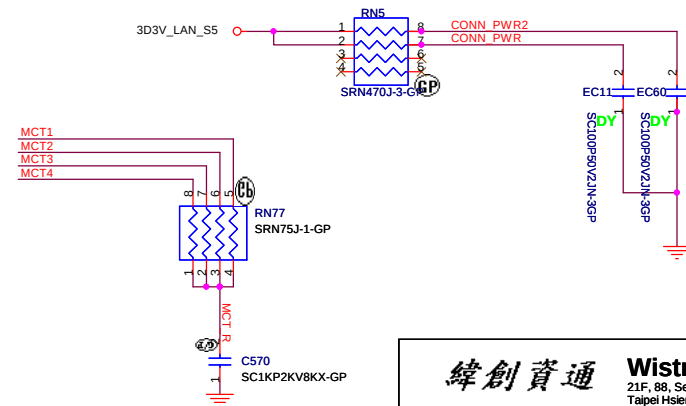


LAN Connector

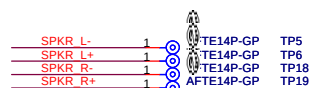
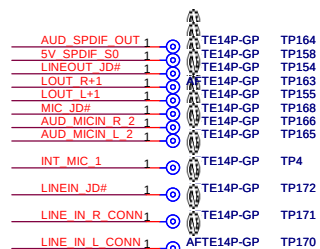
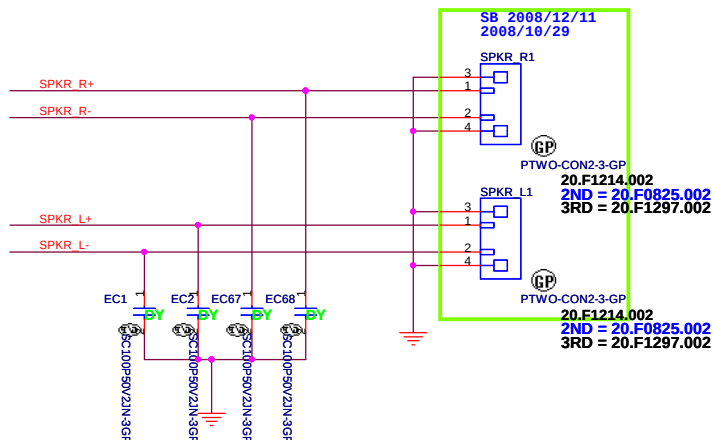
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.



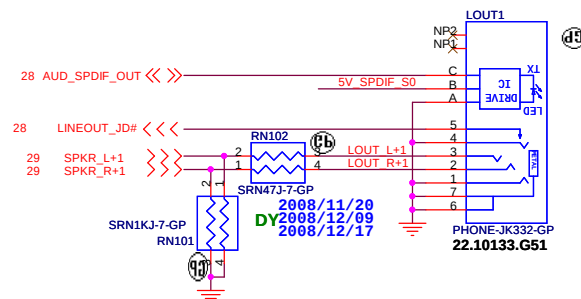
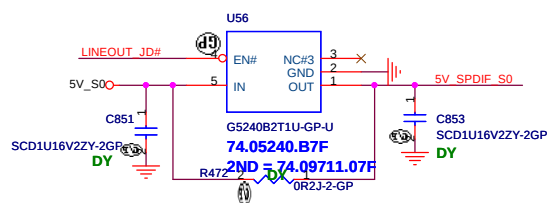
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



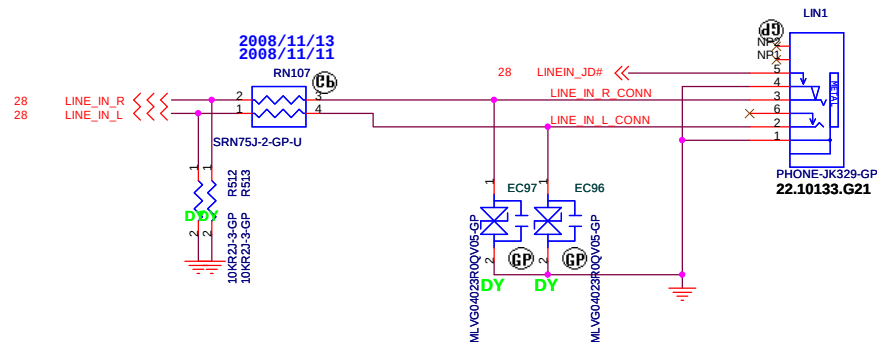
Internal Speaker



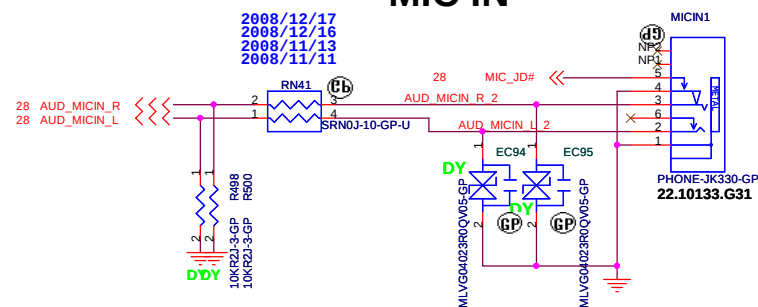
LINE OUT



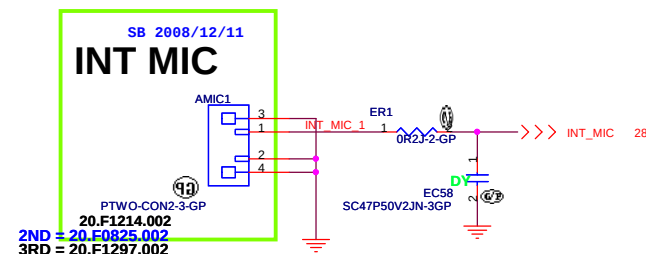
LINE IN



MIC IN



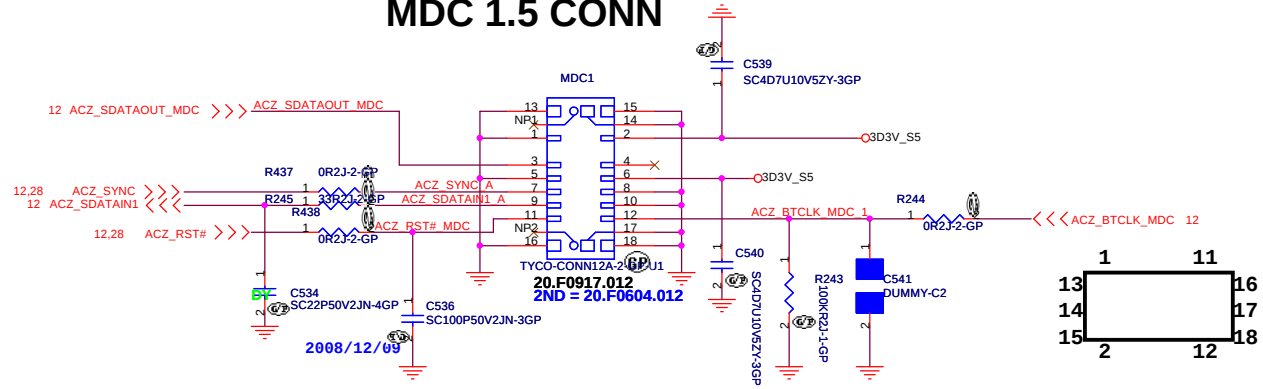
INT MIC



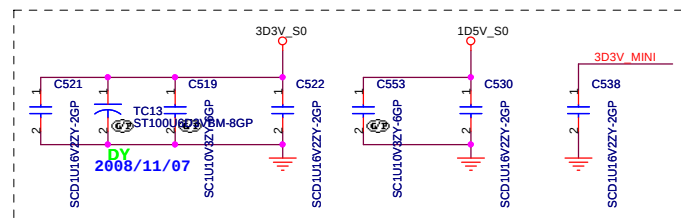
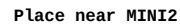
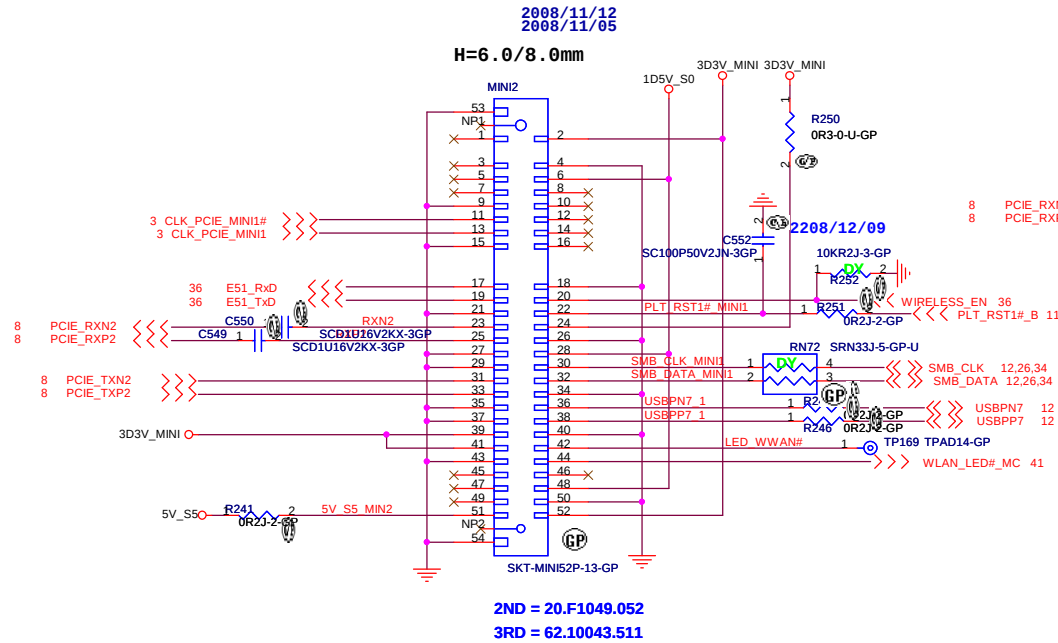
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 Taipei Hsien 221, Taiwan, R.O.C.

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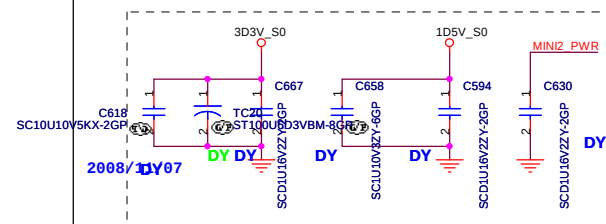
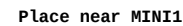
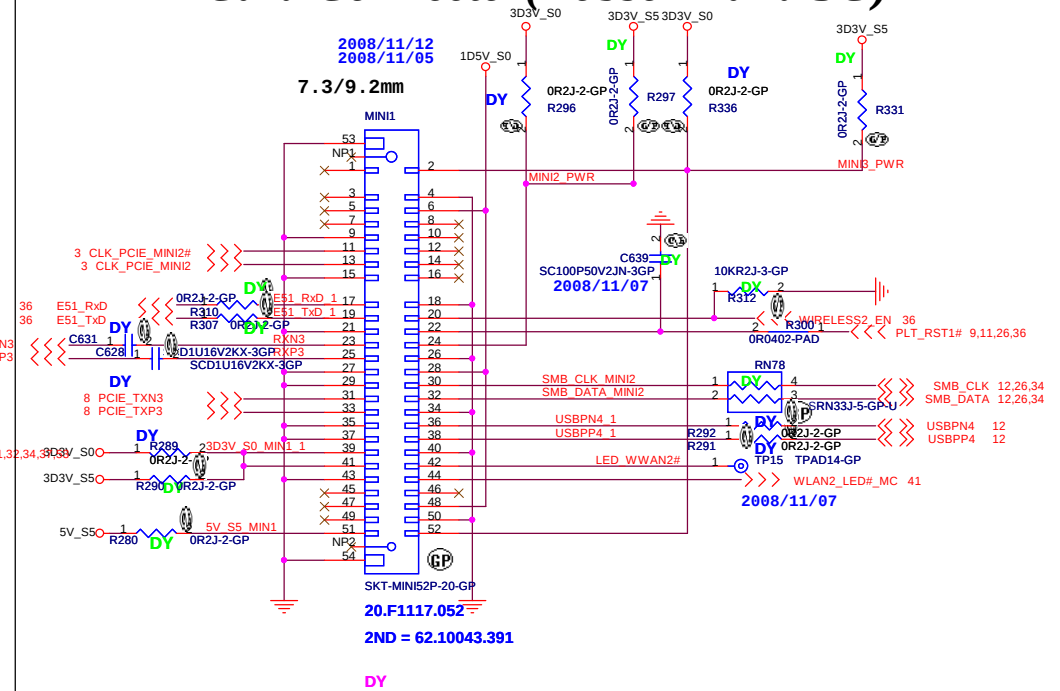
MDC 1.5 CONN

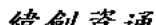


Mini Card Connector(WLAN)

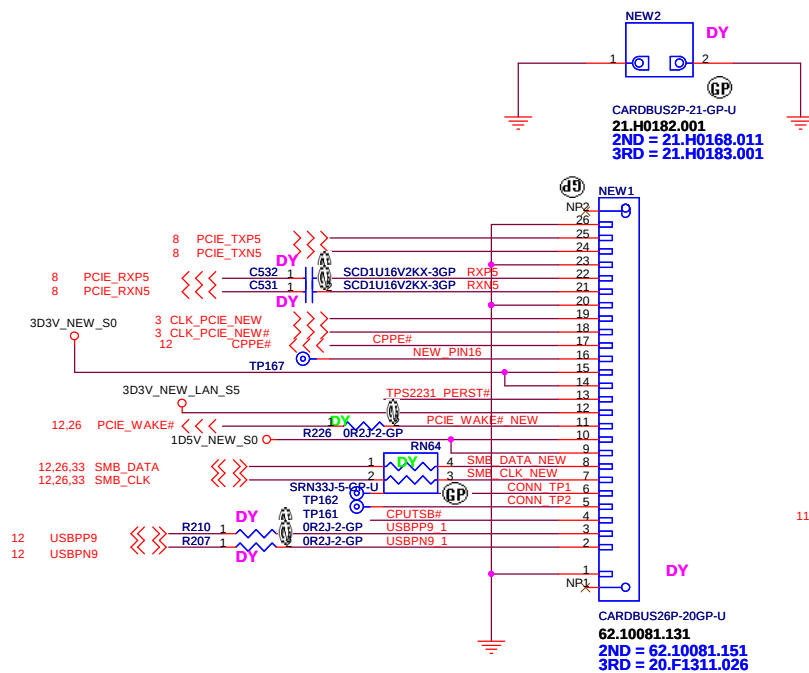


Mini Card Connector(Robson2 and 3G)

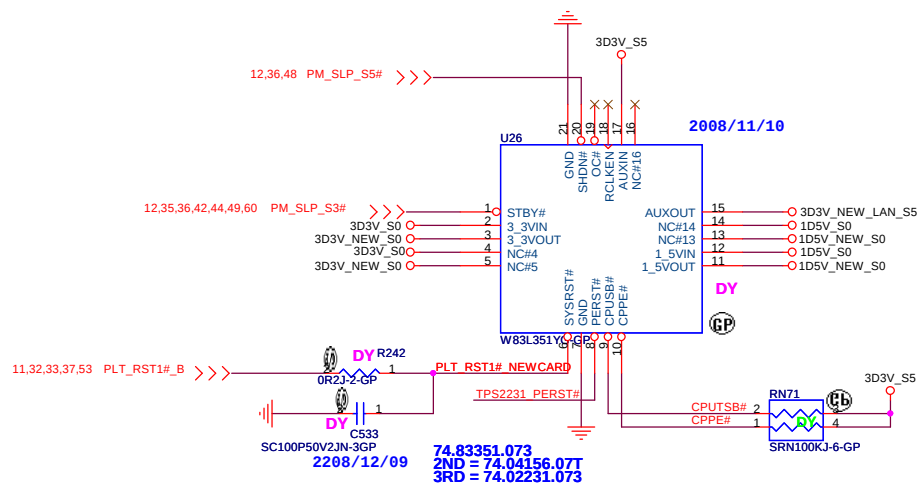
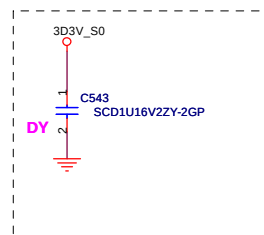


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MINI CARD			
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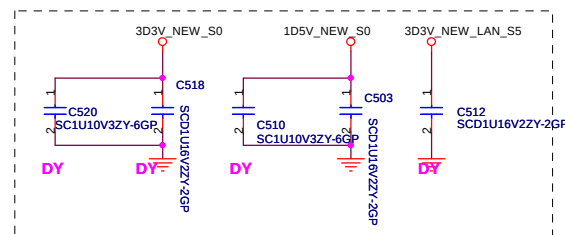
NEWCARD Connector

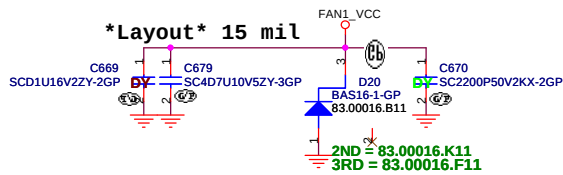


Place them Near to Chip

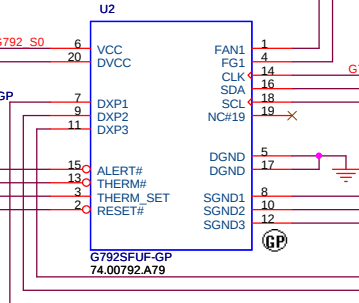
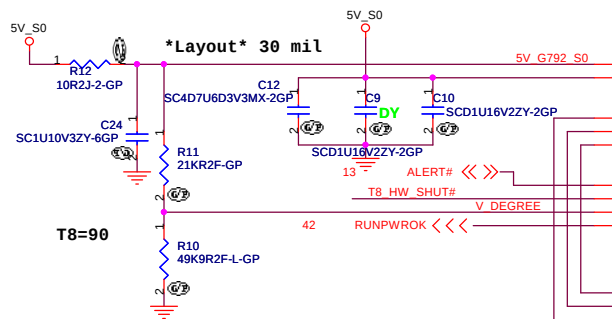
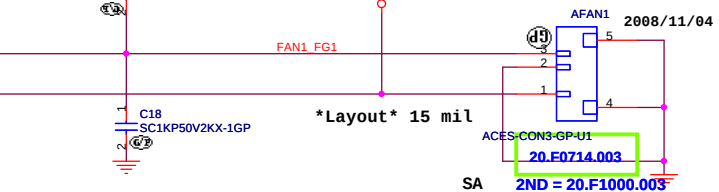
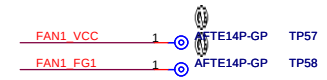


Place them Near to Connector

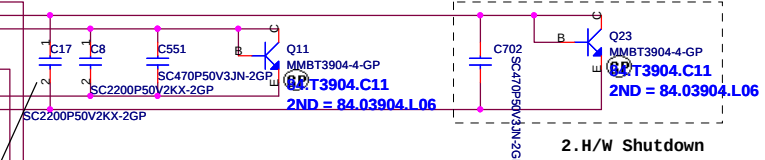




2008/12/8

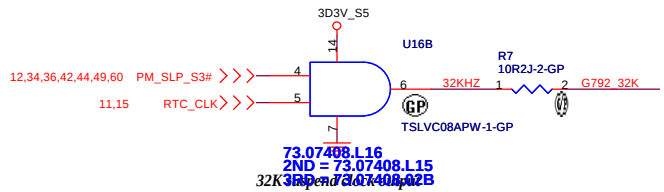


3.System Sensor, Put Plamrest.



DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

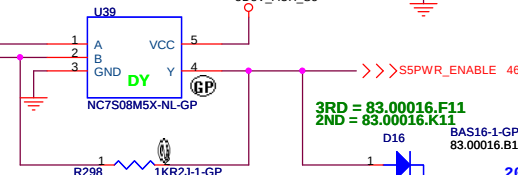
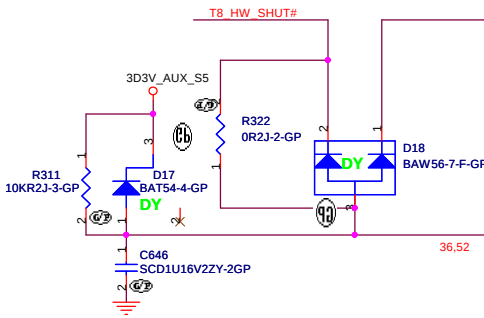
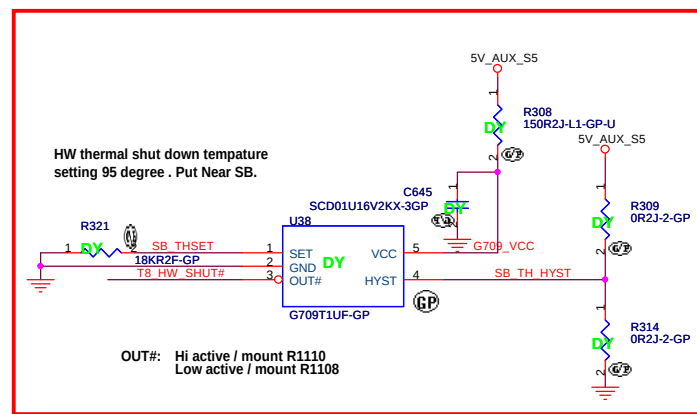
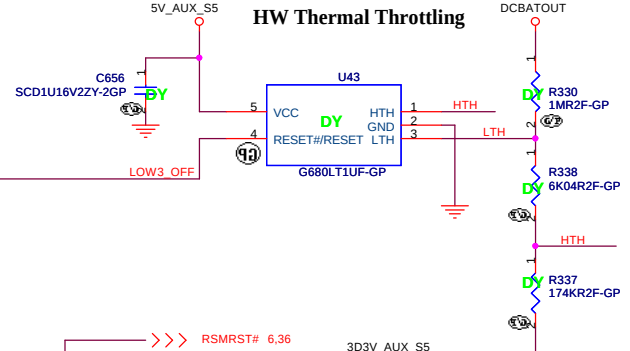
Place near chip as close as possible



1.For CPU Sensor

BL3#

HW Thermal Throttling

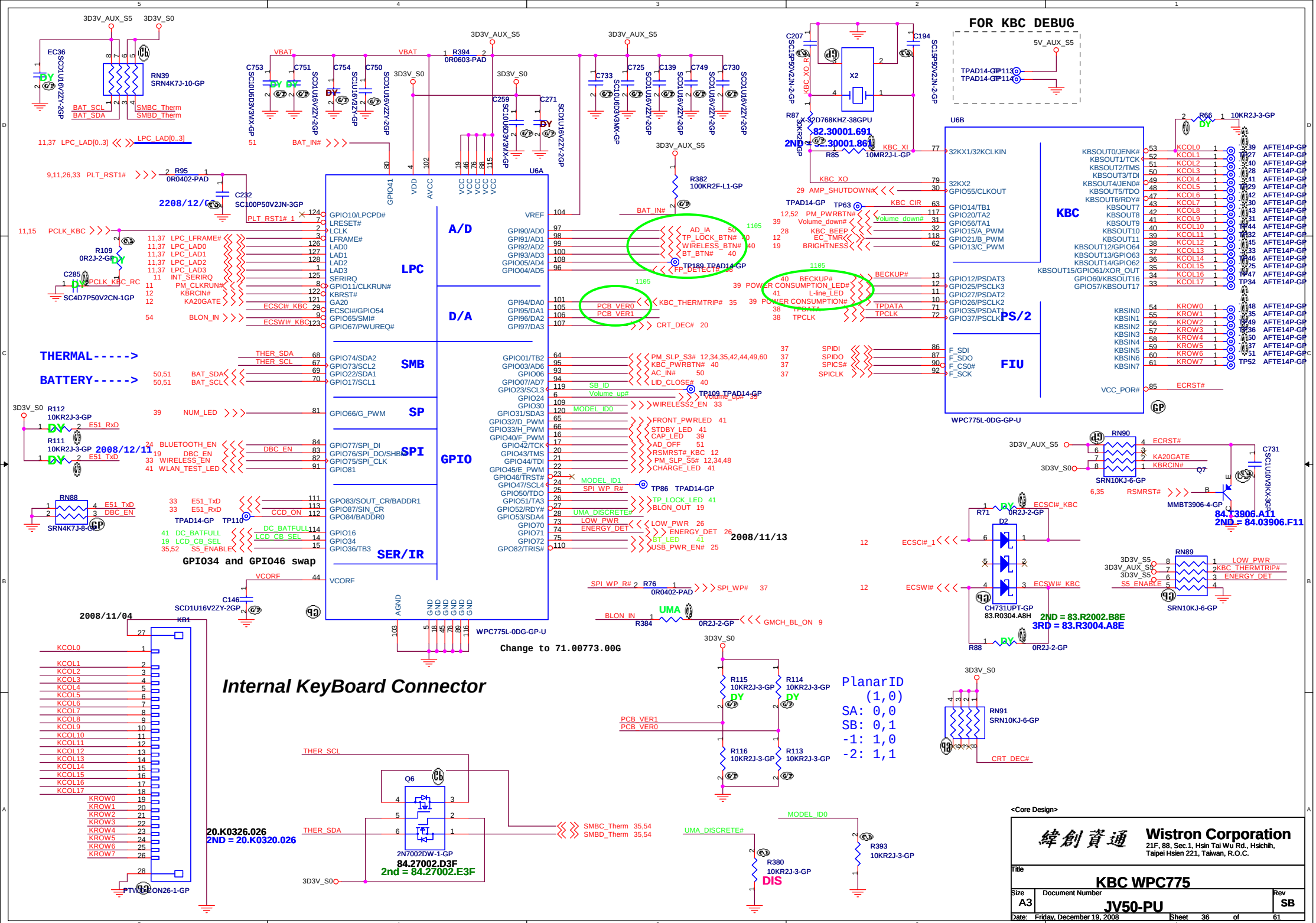


3RD = 83.00016.F11
2ND = 83.00016.K11

2008/11/07

<Core Design>

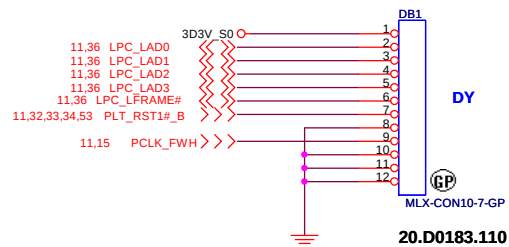
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
G792			
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16M Bits SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD

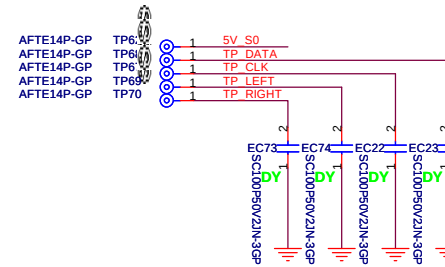
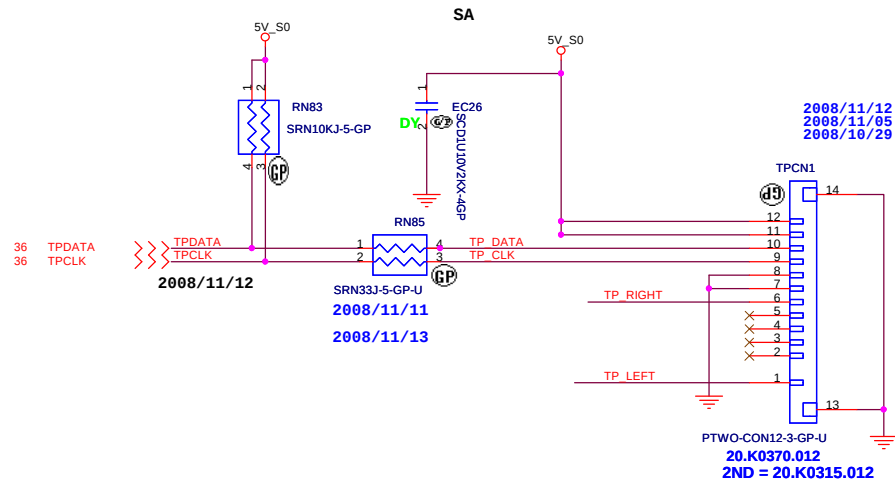
11.36 LPC_LAD[0..3] <<< LPC_LAD[0..3]



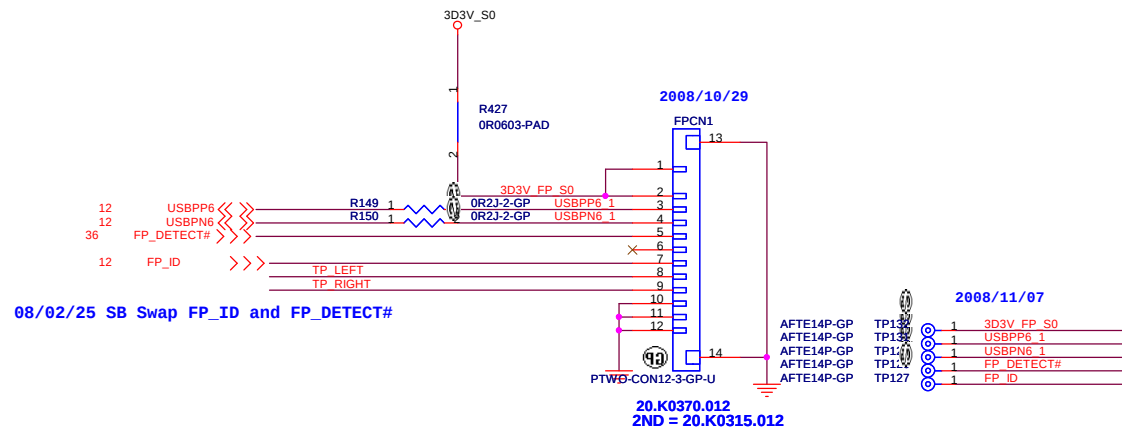
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Title		BIOS	
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TOUCH PAD

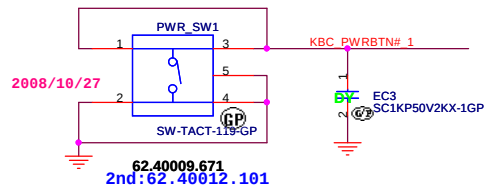


Finger printer

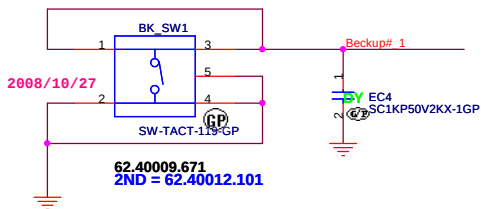




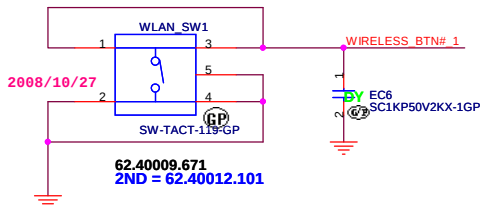
Power Button



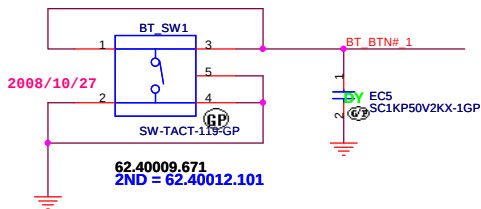
Beckup Button



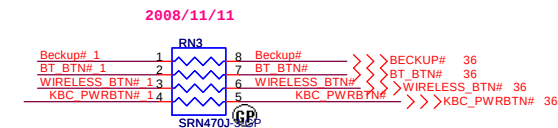
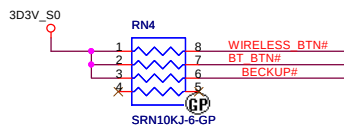
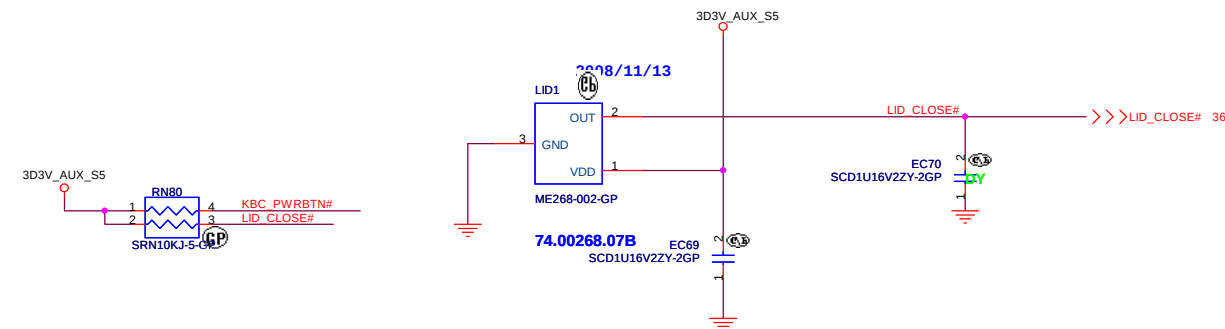
WIRELESS Button



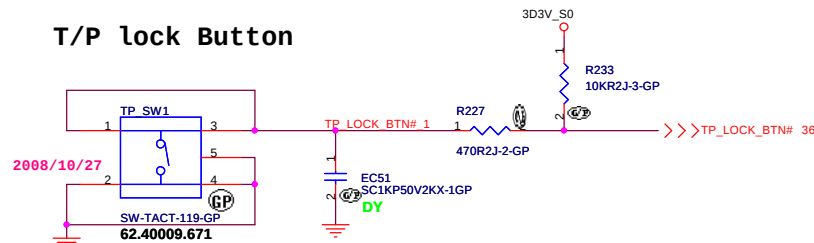
BT/3G Button



Cover Up Switch

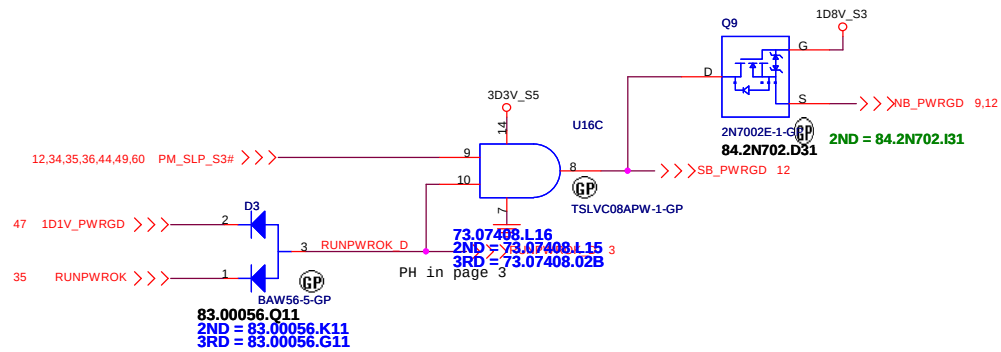


T/P lock Button



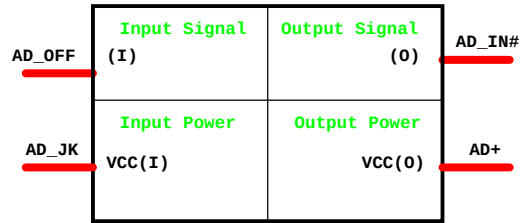
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			SWITCH
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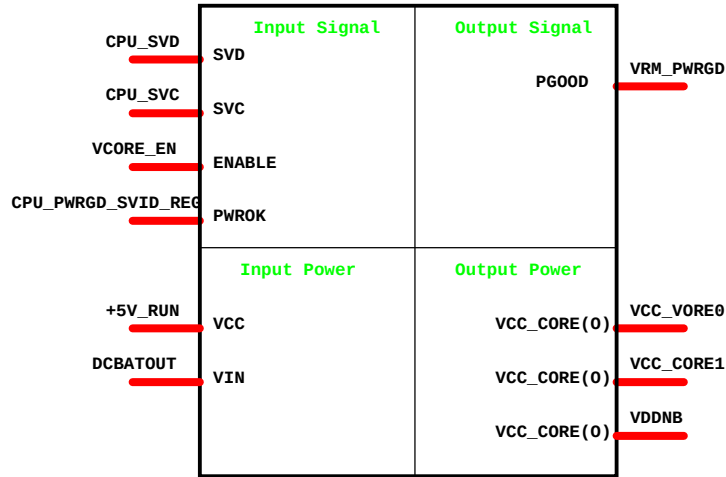


Title			
POWER ON LOGIC			
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A3	JV50-PU	SB	
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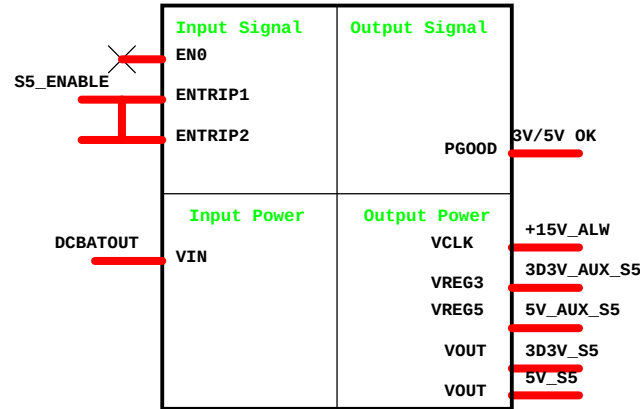
Adapter



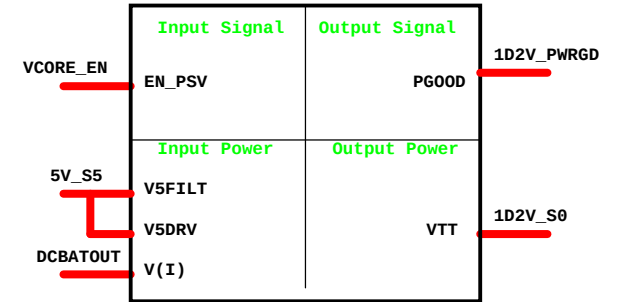
CPU_CORE ISL6265HRTZ



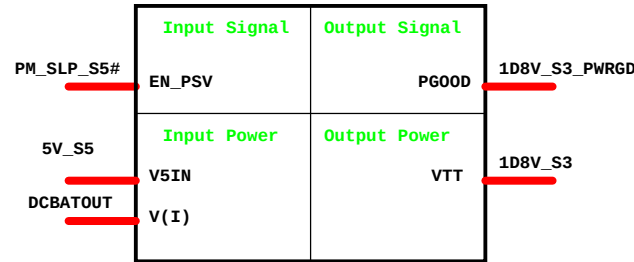
DCDC 5V/3D3V(TPS51125)



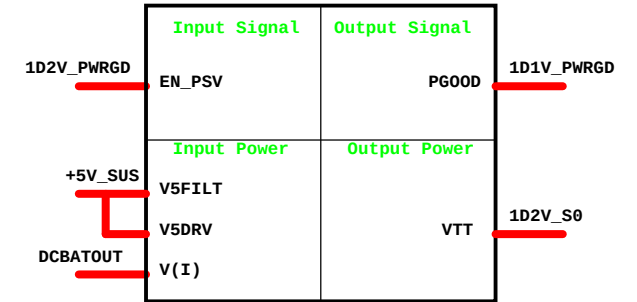
DCDC 1D2V(RT8202)



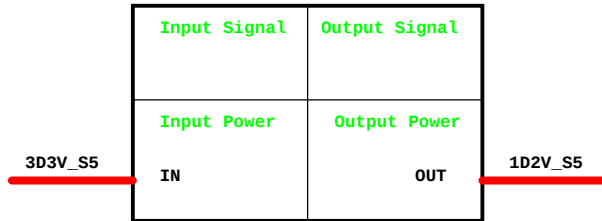
DCDC 1D8V(RT8202)



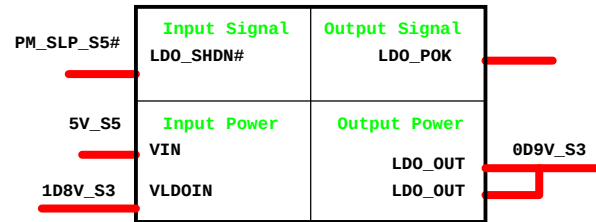
DCDC 1D1V(RT8202)



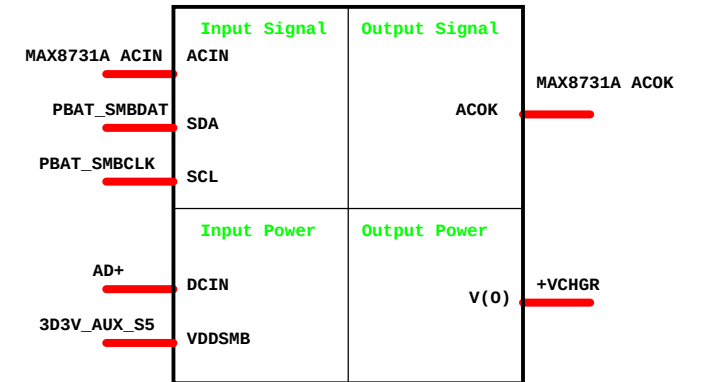
1D2V LDO G9161



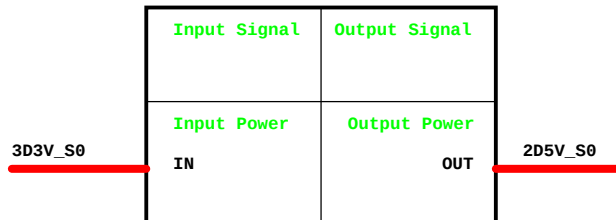
0D9V LDO RT9026



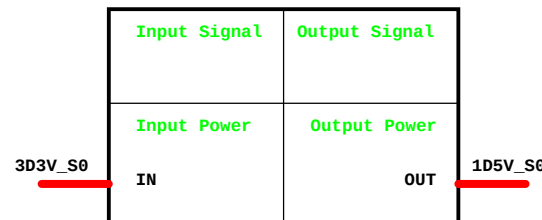
CHARGER MAX8731



2D5V LDO R9161



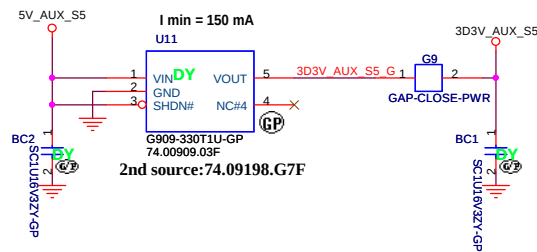
1D5V LDO G9571



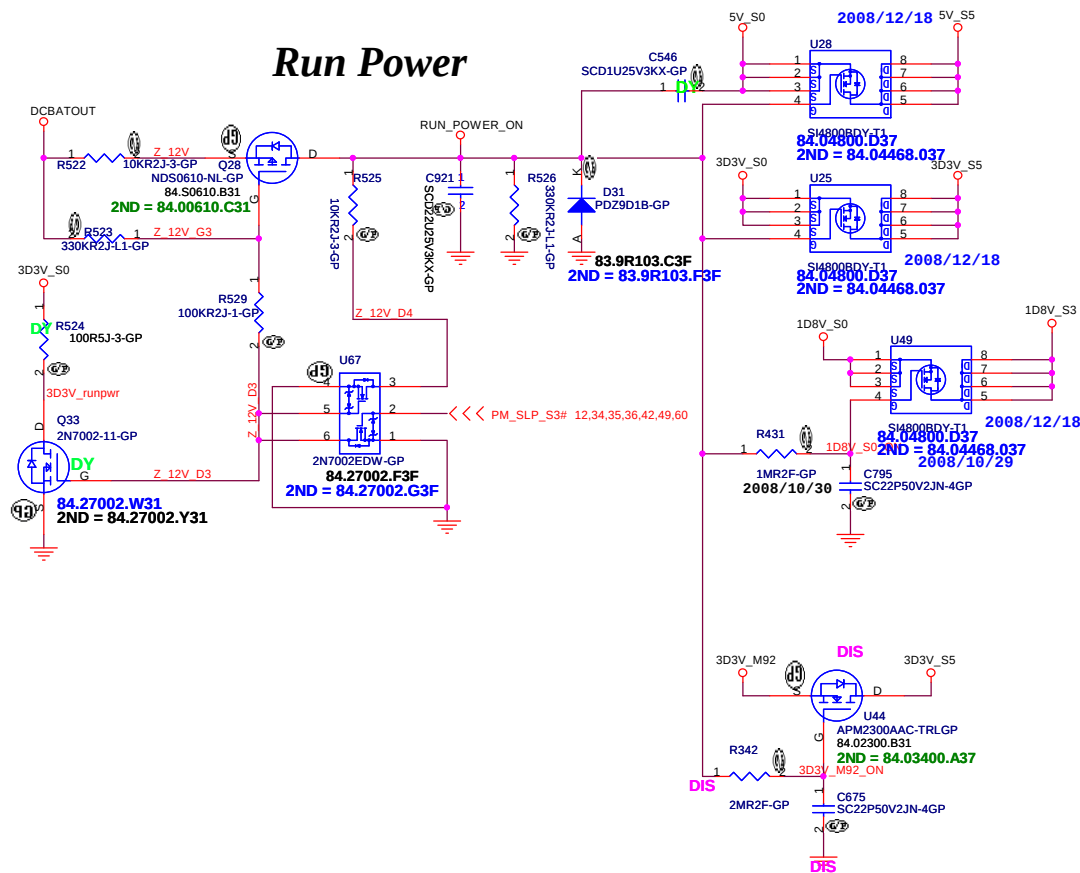
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Power Block Diagram	
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Aux Power 3D3V_AUX_S5



Run Power



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Title																													

RUN AND AUX POWER

Size	A3
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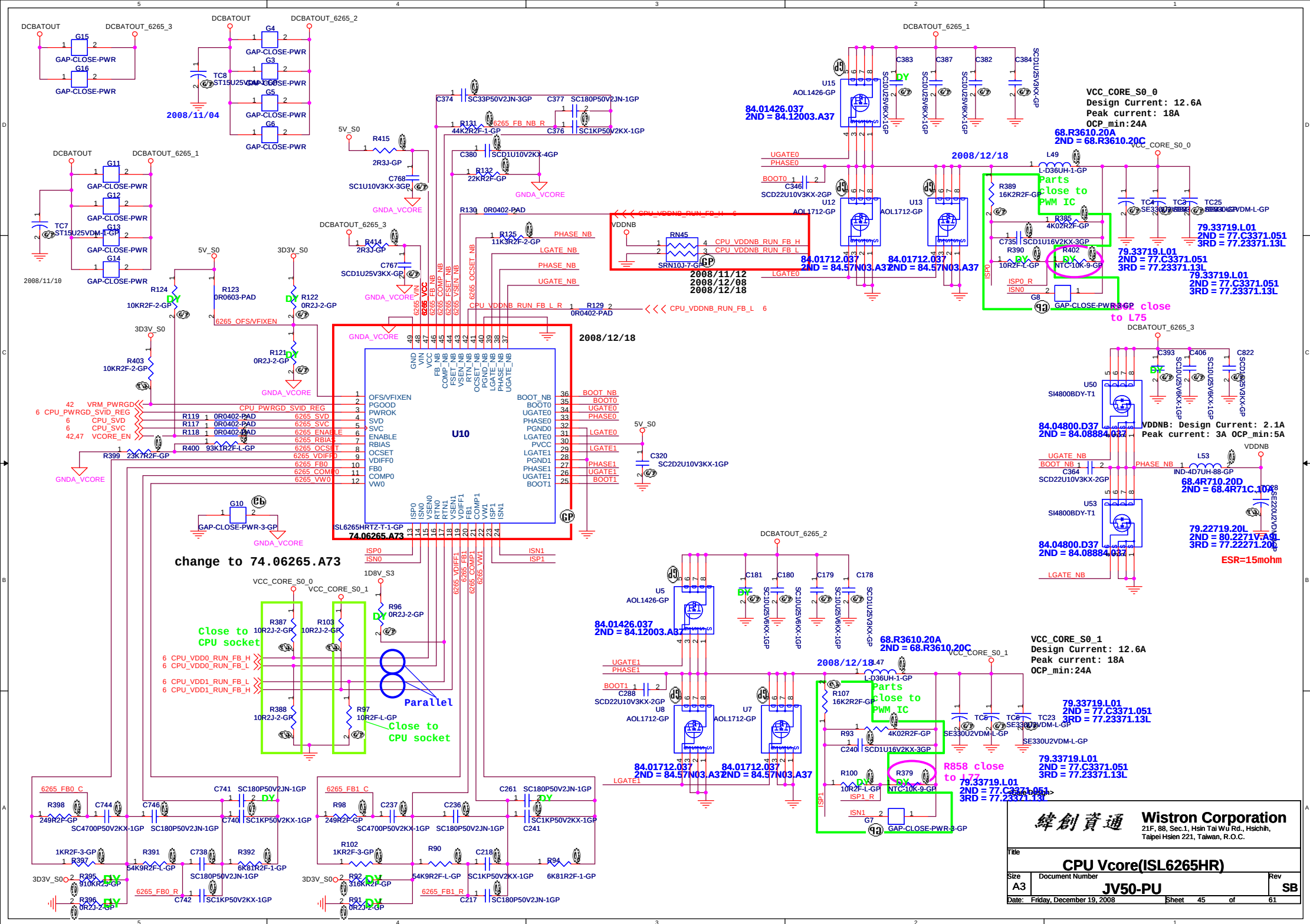
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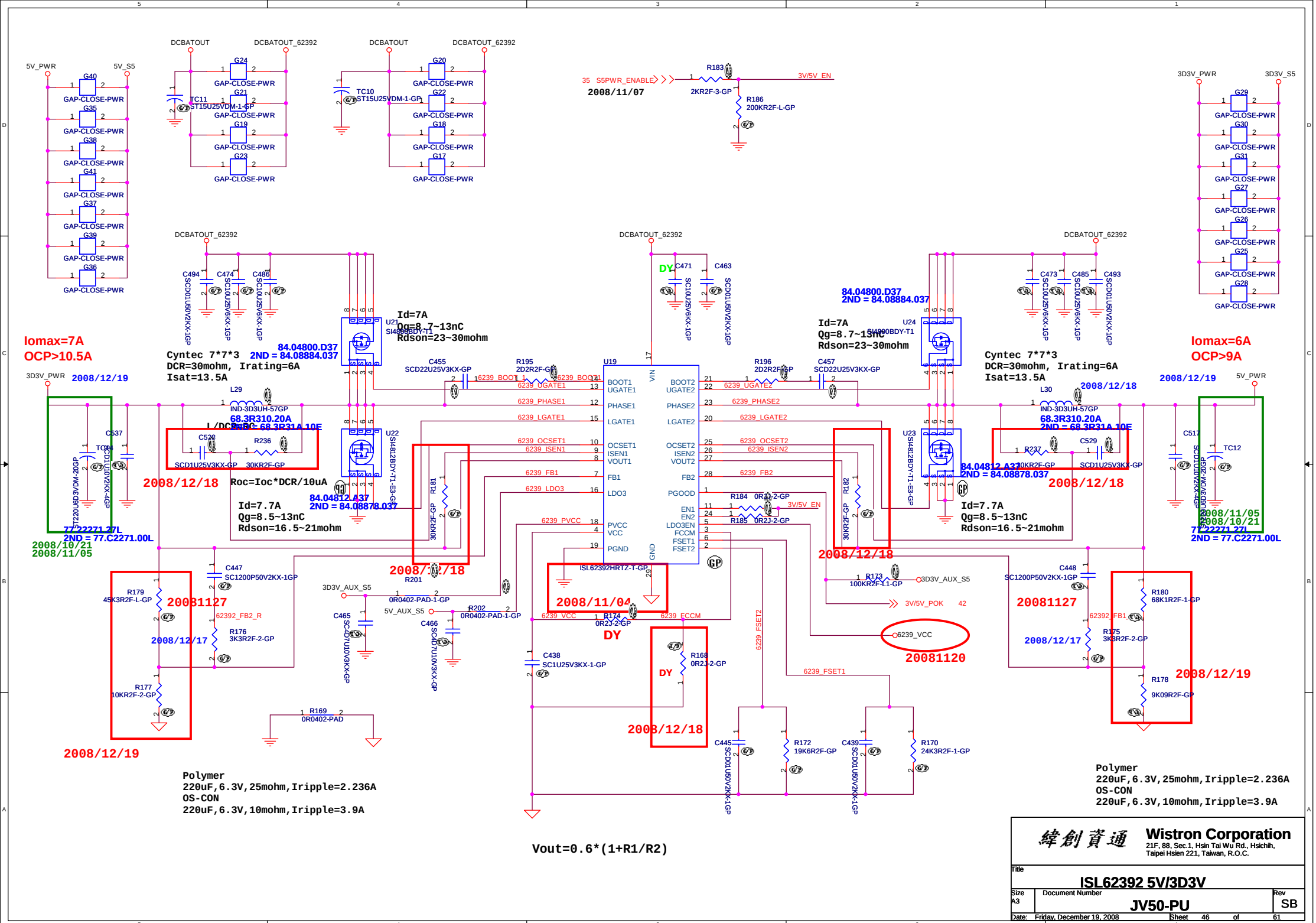
JV50-PU

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79.10712.L02
2ND = 79.10712.6JL
3RD = 79.10112.3JL

79.10712.L02
2ND = 79.10712.6JL
3RD = 79.10112.3JL

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2 * L * f)) * ((V_{in} - V_{out}) * V_{out})/V_{in}))$$

DCBATOUT_51124_1

U37

SM4800BDY-T1

84.04800.D37

2ND = 84.08884.037

C633

SC10J25V6KX-10P

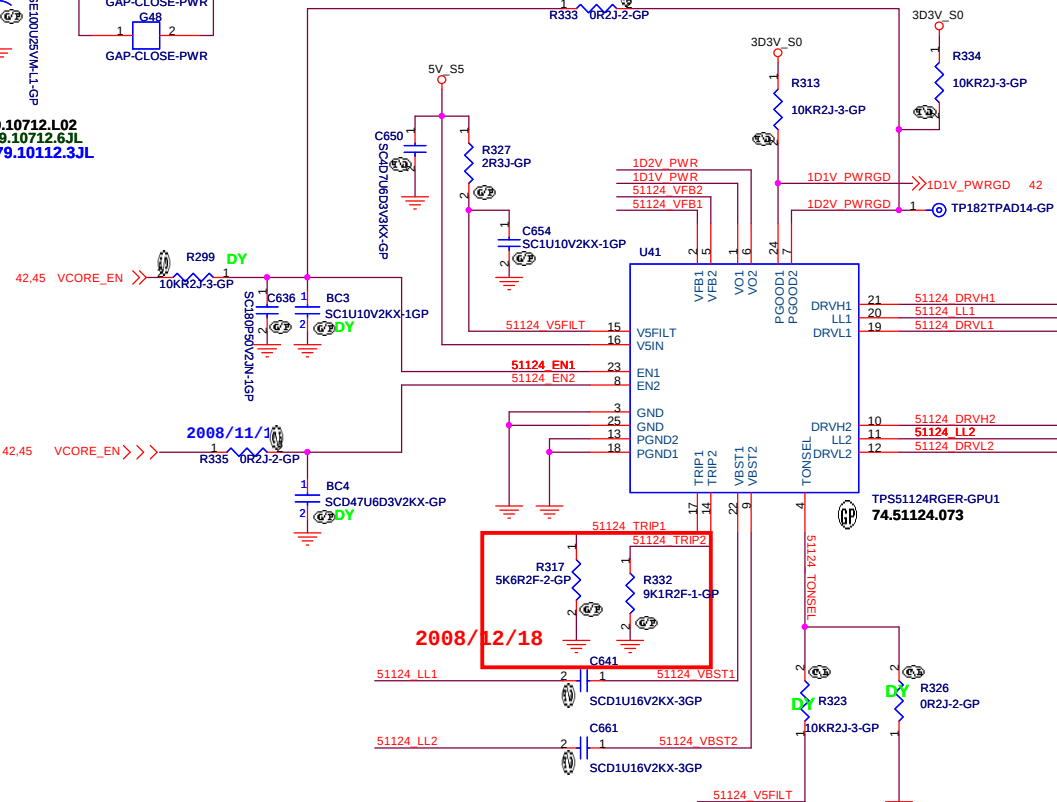
C634

SC10J25V6KX-10P

C635

SC10J25V6KX-10P

1.2V



20080307_Modify by
Brian
ACOUSTIC NIOSE

DCBATOUT_51124

C664
SC10U25V6X-X-10P

U45
S4800BDY-T1
84.04800.D37
2ND = 84.08884.037

12VDC

100uF 25V

100k

10k

U42 6N12BDY-T1-E3-GP

17K8R2

68.1R5 10W

30K2R2

51124

30K2R2

30K2R2

CP

12V Iomax=5A
OCP>10A

12V_PWR

12V_S0

G66

1 2

GAP-CLOSE-PWR

G67

1 2

GAP-CLOSE-PWR

G68

1 2

GAP-CLOSE-PWR

G69

1 2

GAP-CLOSE-PWR

G70

1 2

GAP-CLOSE-PWR

G71

1 2

GAP-CLOSE-PWR

G72

1 2

GAP-CLOSE-PWR

G73

1 2

GAP-CLOSE-PWR

G74

1 2

GAP-CLOSE-PWR

G75

1 2

GAP-CLOSE-PWR

G76

1 2

GAP-CLOSE-PWR

G77

1 2

GAP-CLOSE-PWR

G78

1 2

GAP-CLOSE-PWR

G79

1 2

GAP-CLOSE-PWR

G80

1 2

GAP-CLOSE-PWR

G81

1 2

GAP-CLOSE-PWR

G82

1 2

GAP-CLOSE-PWR

G83

1 2

GAP-CLOSE-PWR

G84

1 2

GAP-CLOSE-PWR

G85

1 2

GAP-CLOSE-PWR

G86

1 2

GAP-CLOSE-PWR

G87

1 2

GAP-CLOSE-PWR

G88

1 2

GAP-CLOSE-PWR

G89

1 2

GAP-CLOSE-PWR

G90

1 2

GAP-CLOSE-PWR

G91

1 2

GAP-CLOSE-PWR

G92

1 2

GAP-CLOSE-PWR

G93

1 2

GAP-CLOSE-PWR

G94

1 2

GAP-CLOSE-PWR

G95

1 2

GAP-CLOSE-PWR

G96

1 2

GAP-CLOSE-PWR

G97

1 2

GAP-CLOSE-PWR

G98

1 2

GAP-CLOSE-PWR

G99

1 2

GAP-CLOSE-PWR

G100

1 2

GAP-CLOSE-PWR

G101

1 2

GAP-CLOSE-PWR

G102

1 2

GAP-CLOSE-PWR

G103

1 2

GAP-CLOSE-PWR

G104

1 2

GAP-CLOSE-PWR

G105

1 2

GAP-CLOSE-PWR

G106

1 2

GAP-CLOSE-PWR

G107

1 2

GAP-CLOSE-PWR

G108

1 2

GAP-CLOSE-PWR

G109

1 2

GAP-CLOSE-PWR

G110

1 2

GAP-CLOSE-PWR

G111

1 2

GAP-CLOSE-PWR

G112

1 2

GAP-CLOSE-PWR

G113

1 2

GAP-CLOSE-PWR

G114

1 2

GAP-CLOSE-PWR

G115

1 2

GAP-CLOSE-PWR

G116

1 2

GAP-CLOSE-PWR

G117

1 2

GAP-CLOSE-PWR

G118

1 2

GAP-CLOSE-PWR

G119

1 2

GAP-CLOSE-PWR

G120

1 2

GAP-CLOSE-PWR

G121

1 2

GAP-CLOSE-PWR

G122

1 2

GAP-CLOSE-PWR

G123

1 2

GAP-CLOSE-PWR

G124

1 2

GAP-CLOSE-PWR

G125

1 2

GAP-CLOSE-PWR

G126

1 2

GAP-CLOSE-PWR

G127

1 2

GAP-CLOSE-PWR

G128

1 2

GAP-CLOSE-PWR

G129

1 2

GAP-CLOSE-PWR

G130

1 2

GAP-CLOSE-PWR

G131

1 2

GAP-CLOSE-PWR

G132

1 2

GAP-CLOSE-PWR

G133

1 2

GAP-CLOSE-PWR

G134

1 2

GAP-CLOSE-PWR

G135

1 2

GAP-CLOSE-PWR

G136

1 2

GAP-CLOSE-PWR

G137

1 2

GAP-CLOSE-PWR

G138

1 2

GAP-CLOSE-PWR

G139

1 2

GAP-CLOSE-PWR

G140

1 2

GAP-CLOSE-PWR

G141

1 2

GAP-CLOSE-PWR

G142

1 2

GAP-CLOSE-PWR

G143

1 2

GAP-CLOSE-PWR

G144

1 2

GAP-CLOSE-PWR

G145

1 2

GAP-CLOSE-PWR

G146

1 2

GAP-CLOSE-PWR

G147

1 2

GAP-CLOSE-PWR

G148

1 2

GAP-CLOSE-PWR

G149

1 2

GAP-CLOSE-PWR

G150

1 2

GAP-CLOSE-PWR

G151

1 2

GAP-CLOSE-PWR

G152

1 2

GAP-CLOSE-PWR

G153

1 2

GAP-CLOSE-PWR

G154

1 2

GAP-CLOSE-PWR

G155

1 2

GAP-CLOSE-PWR

G156

1 2

GAP-CLOSE-PWR

G157

1 2

GAP-CLOSE-PWR

G158

1 2

GAP-CLOSE-PWR

G159

1 2

GAP-CLOSE-PWR

G160

1 2

GAP-CLOSE-PWR

G161

1 2

GAP-CLOSE-PWR

G162

1 2

GAP-CLOSE-PWR

G163

1 2

GAP-CLOSE-PWR

G164

1 2

GAP-CLOSE-PWR

G165

1 2

GAP-CLOSE-PWR

G166

1 2

GAP-CLOSE-PWR

G167

1 2

GAP-CLOSE-PWR

G168

1 2

GAP-CLOSE-PWR

G169

1 2

GAP-CLOSE-PWR

G170

1 2

GAP-CLOSE-PWR

G171

1 2

GAP-CLOSE-PWR

G172

1 2

GAP-CLOSE-PWR

G173

1 2

GAP-CLOSE-PWR

G174

1 2

GAP-CLOSE-PWR

G175

1 2

GAP-CLOSE-PWR

G176

1 2

GAP-CLOSE-PWR

G177

1 2

GAP-CLOSE-PWR

G178

1 2

GAP-CLOSE-PWR

G179

1 2

GAP-CLOSE-PWR

G180

1 2

GAP-CLOSE-PWR

G181

1 2

GAP-CLOSE-PWR

G182

1 2

GAP-CLOSE-PWR

G183

1 2

GAP-CLOSE-PWR

G184

1 2

GAP-CLOSE-PWR

G185

1 2

GAP-CLOSE-PWR

G186

1 2

GAP-CLOSE-PWR

G187

1 2

GAP-CLOSE-PWR

G188

1 2

GAP-CLOSE-PWR

G189

1 2

GAP-CLOSE-PWR

G190

1 2

GAP-CLOSE-PWR

G191

1 2

GAP-CLOSE-PWR

G192

1 2

GAP-CLOSE-PWR

G193

1 2

GAP-CLOSE-PWR

G194

1 2

GAP-CLOSE-PWR

G195

1 2

GAP-CLOSE-PWR

G196

1 2

GAP-CLOSE-PWR

G197

1 2

GAP-CLOSE-PWR

G198

1 2

GAP-CLOSE-PWR

G199

1 2

GAP-CLOSE-PWR

G200

1 2

GAP-CLOSE-PWR

G201

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

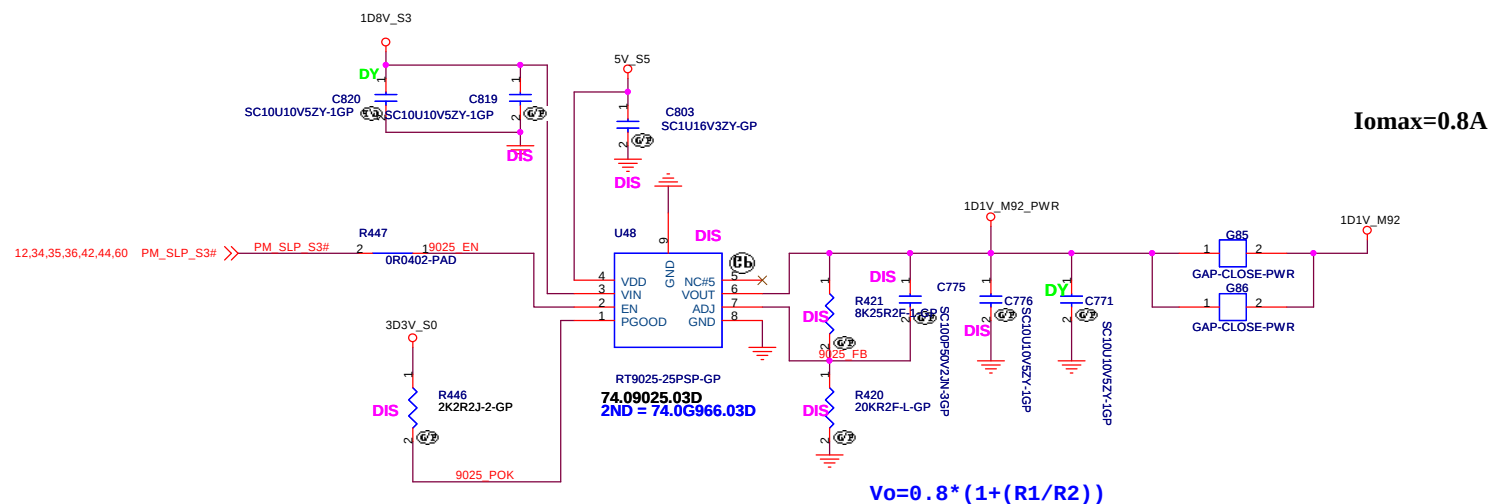
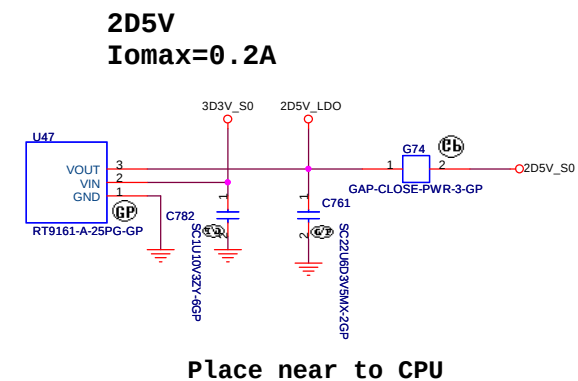
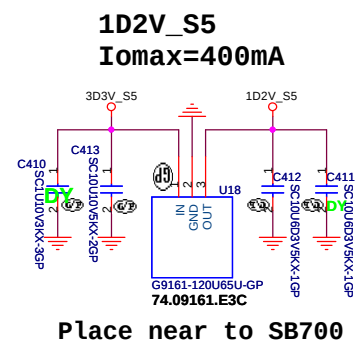
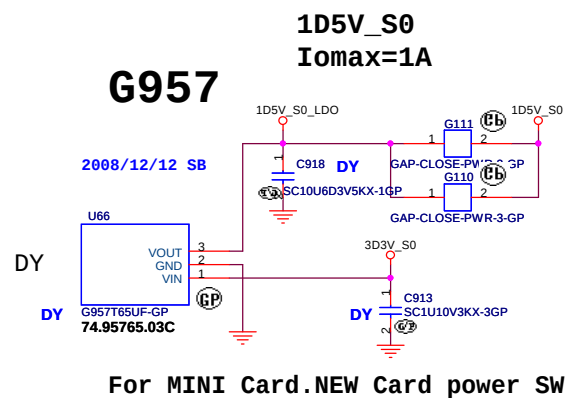
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DCIN1

6 GND

5

4

1

2

3

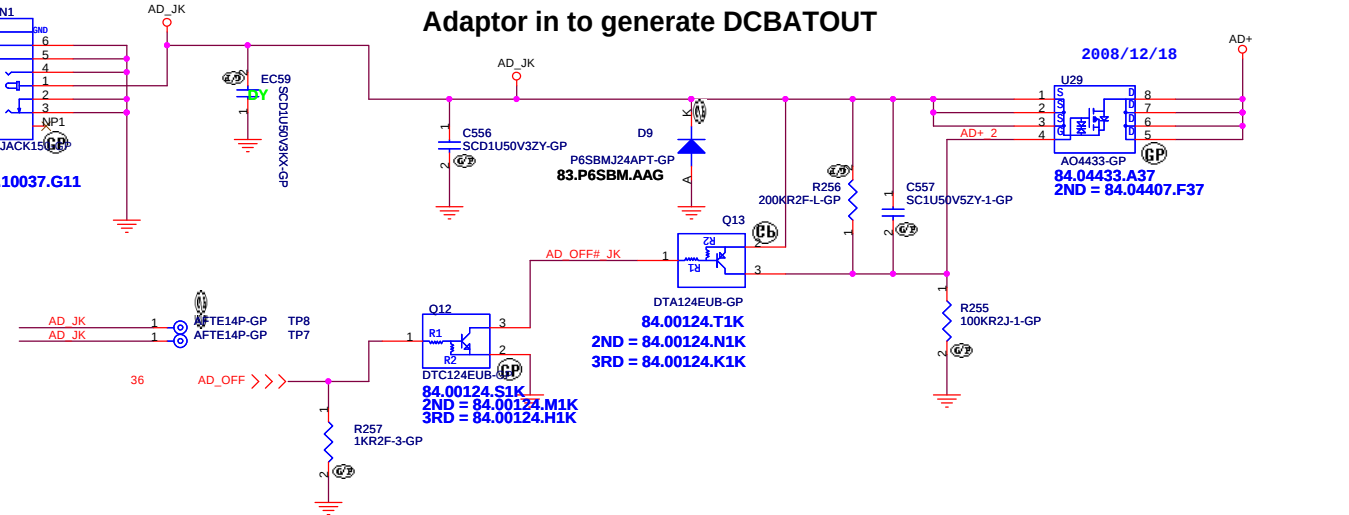
NP1

DC-JACK15V

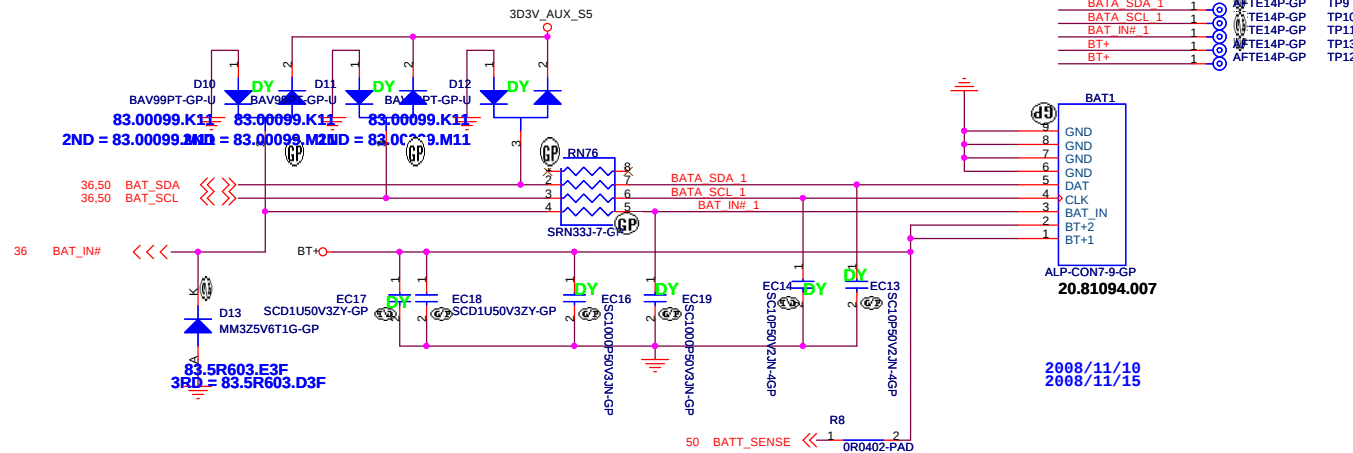
22.10037.G11

Adaptor in to generate DCBATOUT

U29
1 S 8
2 S 7
3 S 6
4 G 5
AO4433-GP
84.04433.A37
2ND = 84.04407.F37

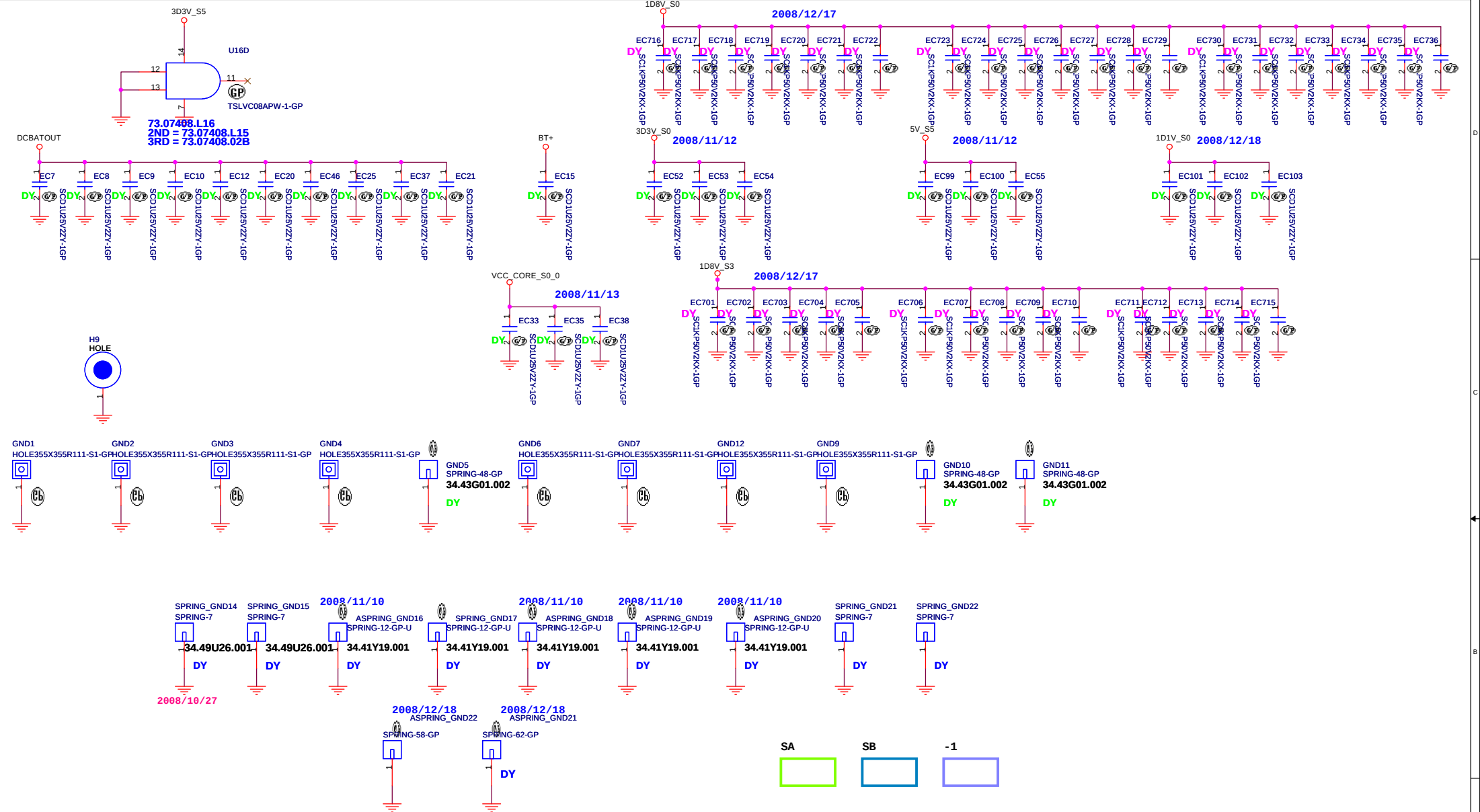


BATTERY CONNECTOR

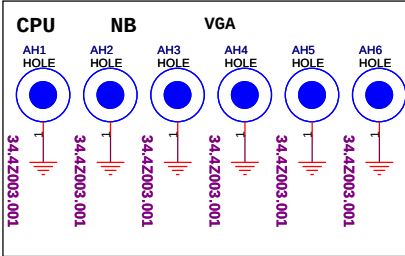


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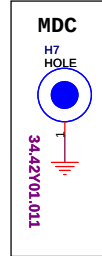
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AD/BATT CONN			
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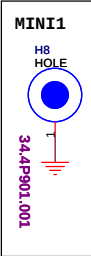
TOP



TOP



BOT



Check test point

3D3V_S0	TP233	TPAD14-GP
3D3V_AUX_S5	TP232	TPAD14-GP
3D3V_S5	TP231	TPAD14-GP
5V_S5	TP230	TPAD14-GP
12.36 PM_PWRBTN# <<<	TP229	TPAD14-GP
6.11 CPU_PWRGD <<<	TP228	TPAD14-GP
35.36 SS_ENABLE <<<	TP227	TPAD14-GP
6.11 CPU_LDT_RST# <<<	TP226	TPAD14-GP

Test Point放在Dimm Door打開可量測處

緯創資通

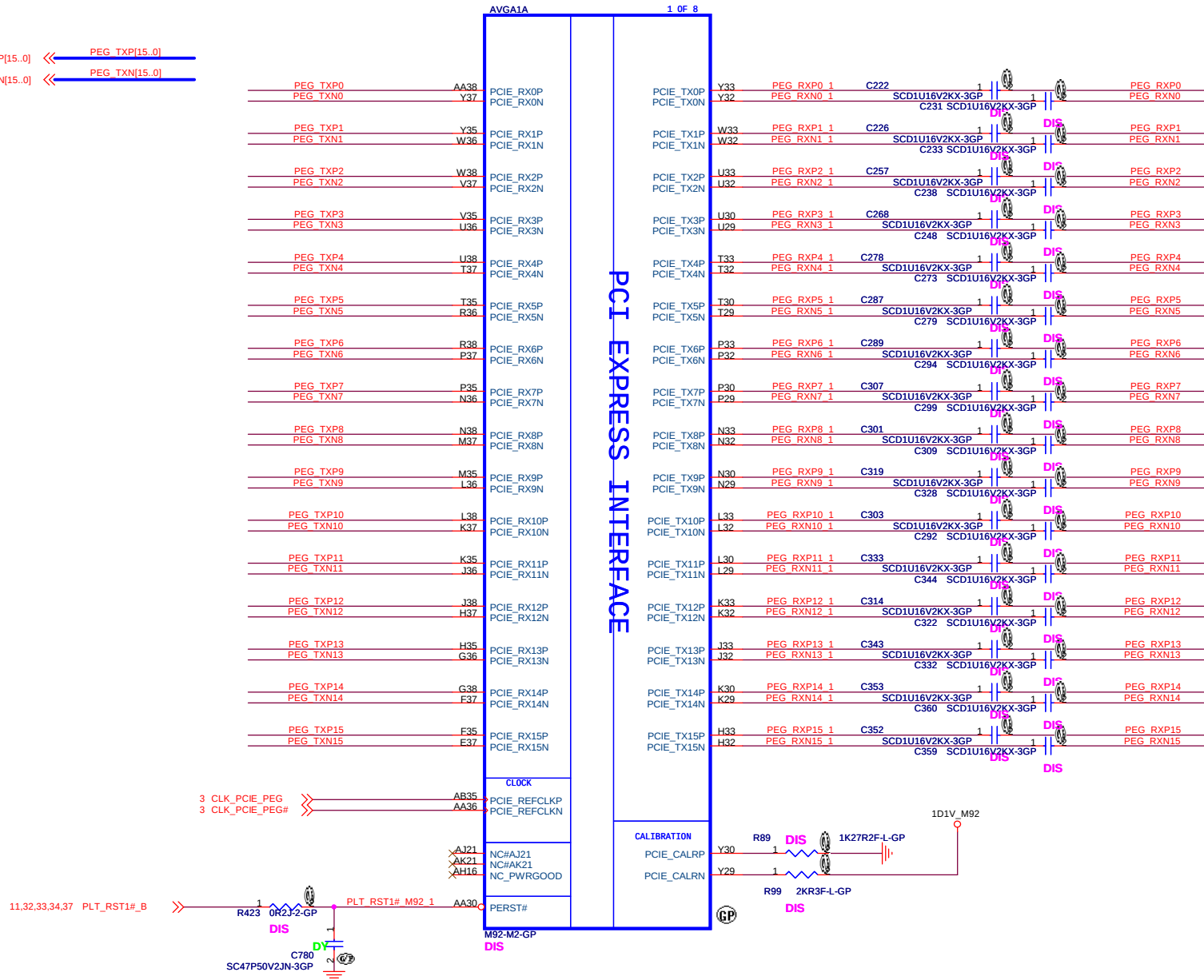
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File			EMI/Spring/Boss		
Size	Document Number				Rev
	JV50-PU				SB
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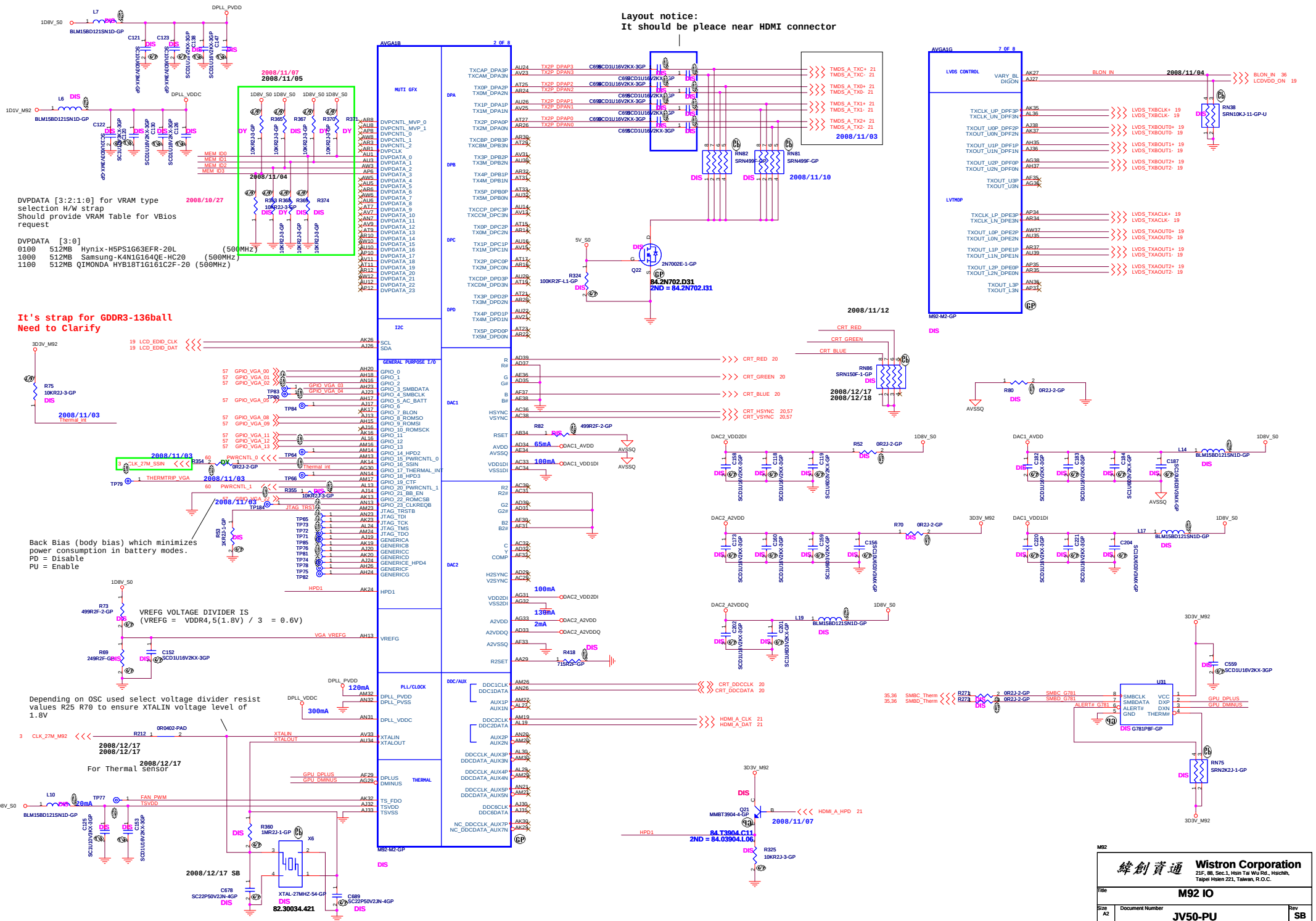
8 PEG_TXP[15..0] << PEG_TXP[15..0]
8 PEG_TXN[15..0] << PEG_TXN[15..0]

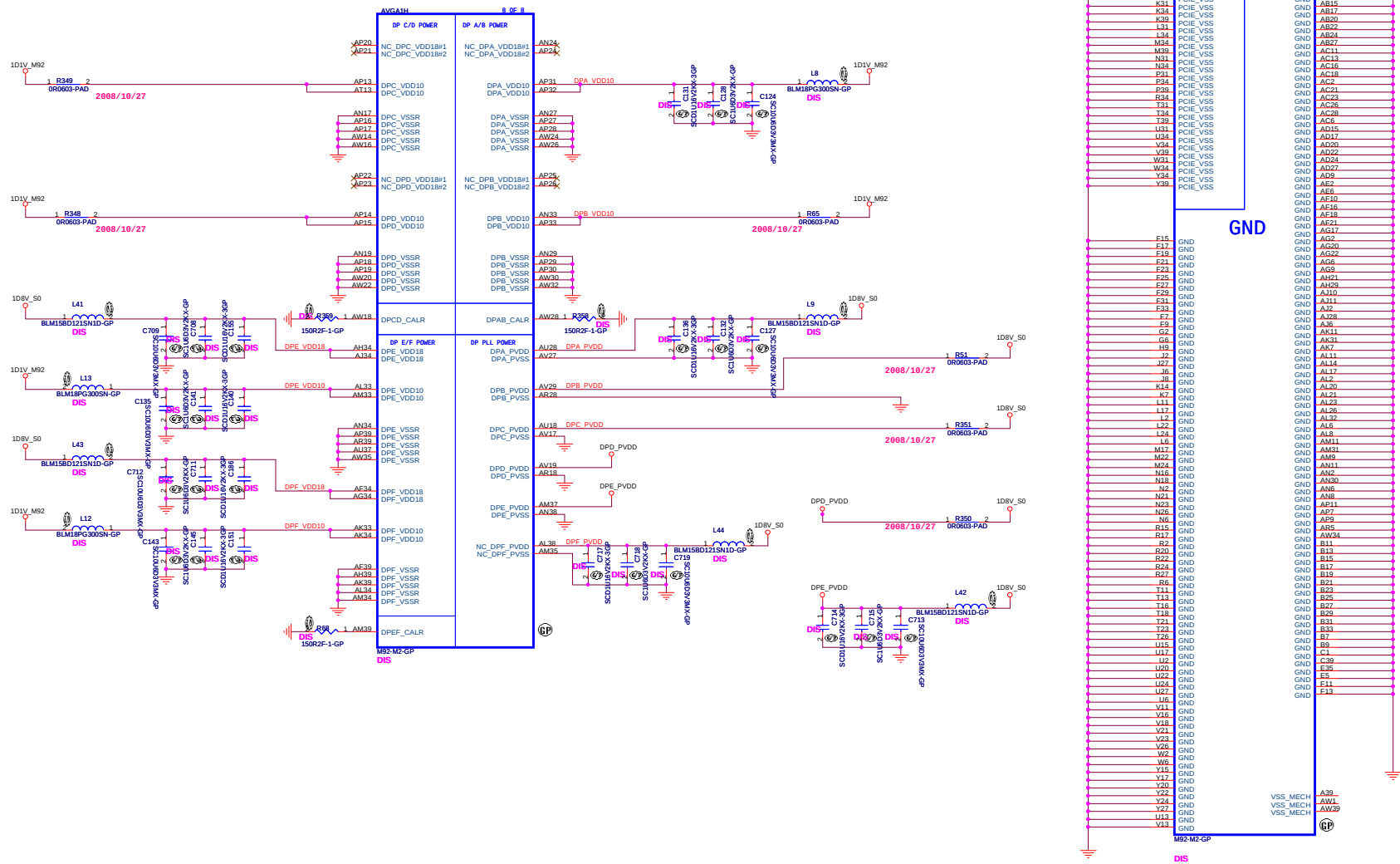
8 PEG_RXP[15..0] << PEG_RXP[15..0]
8 PEG_RXN[15..0] << PEG_RXN[15..0]



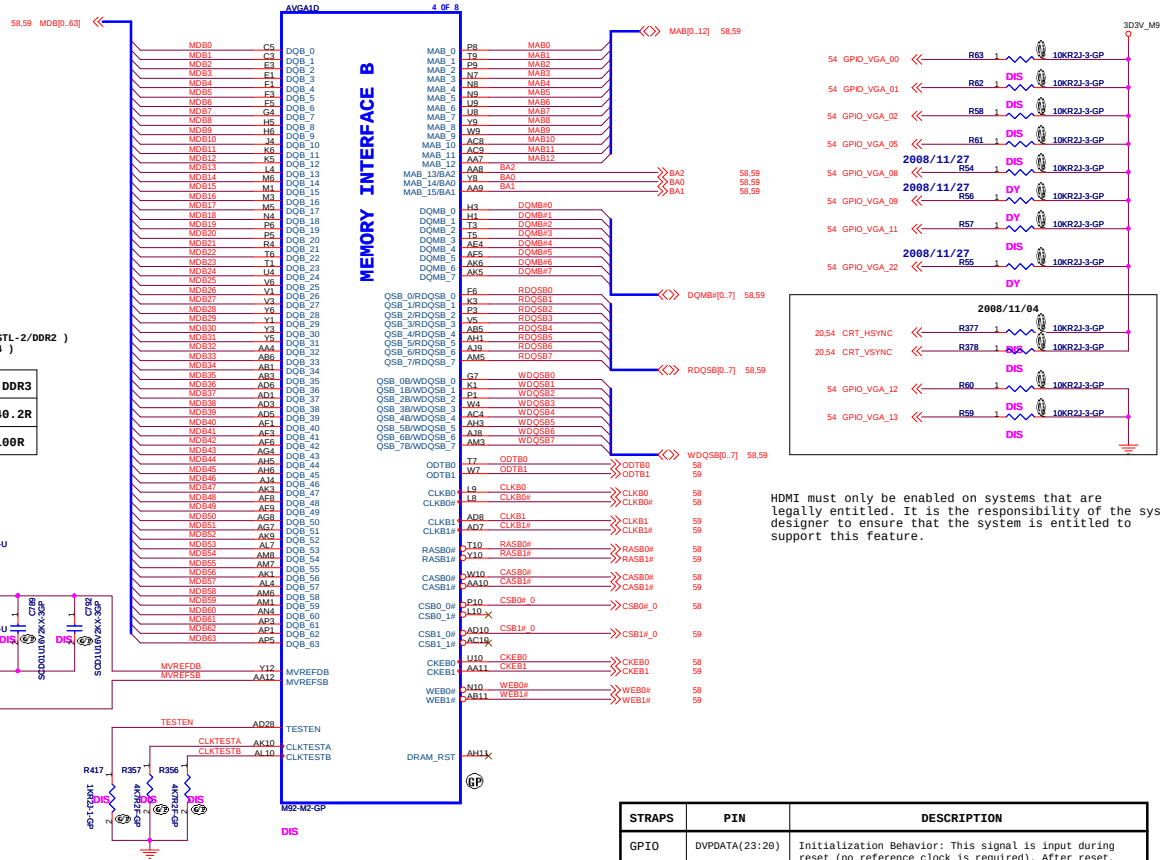
M92

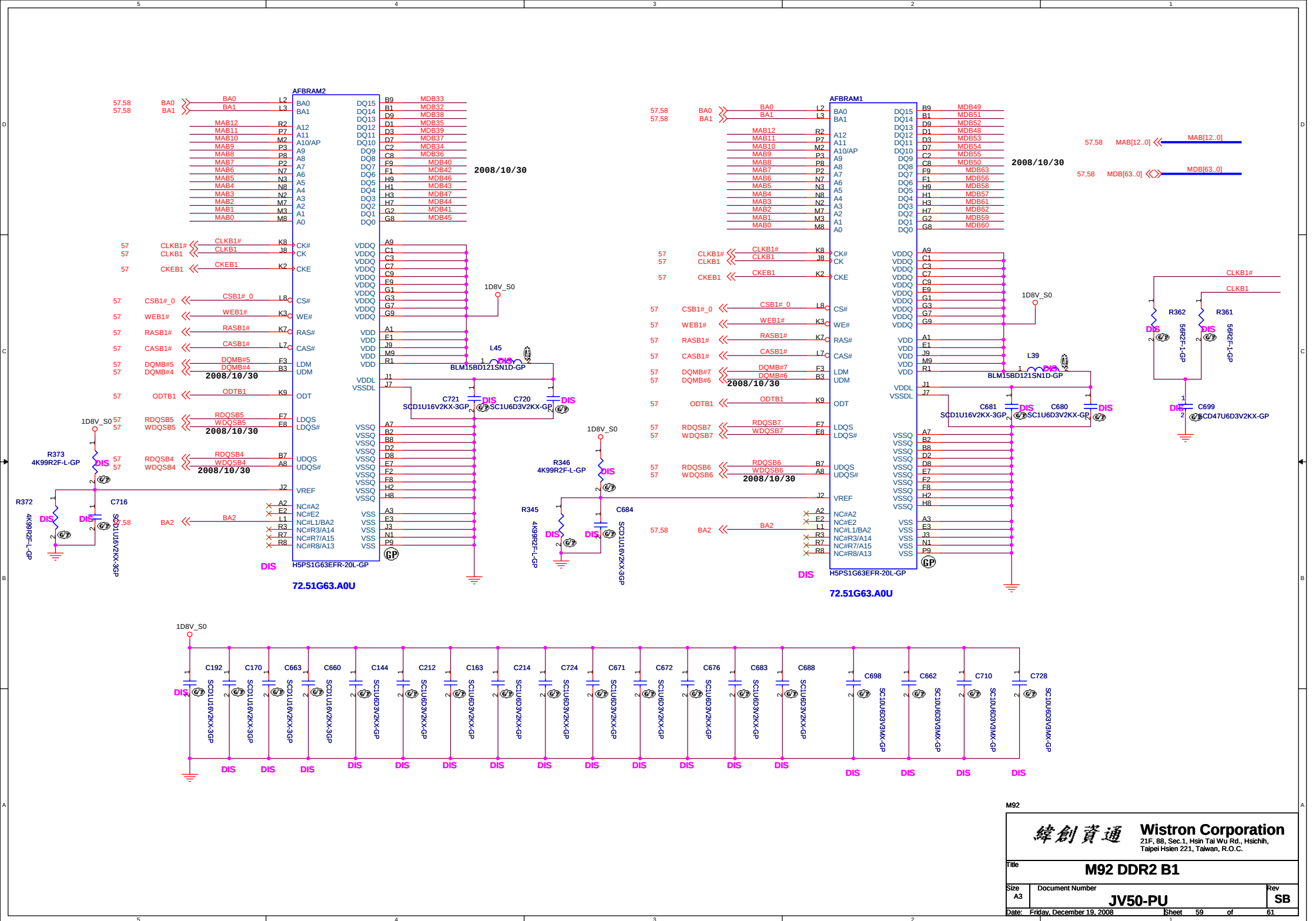
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Title M92 PCIE	
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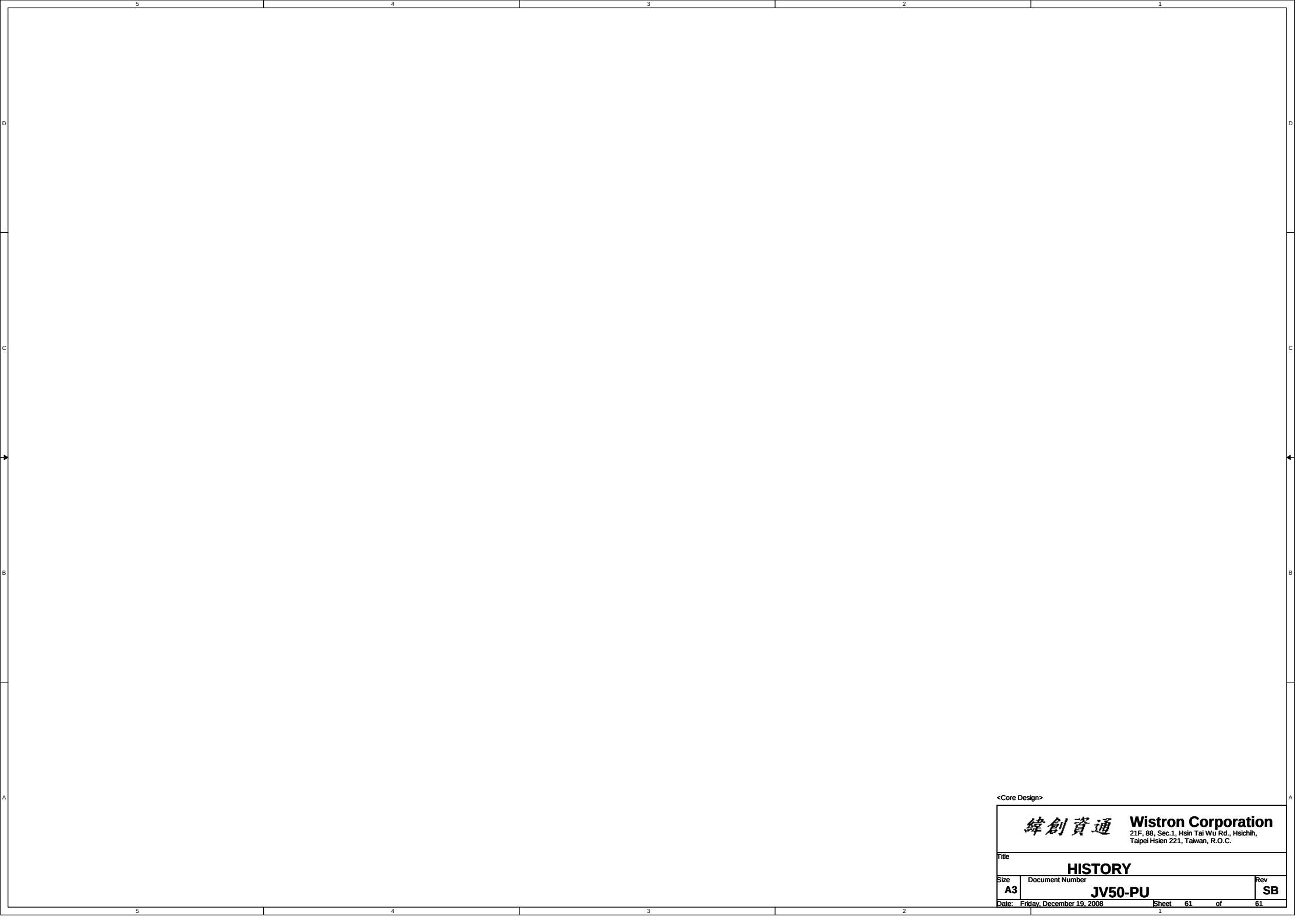




M92-M2 uses memory group B only







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