

PCB STACK UP

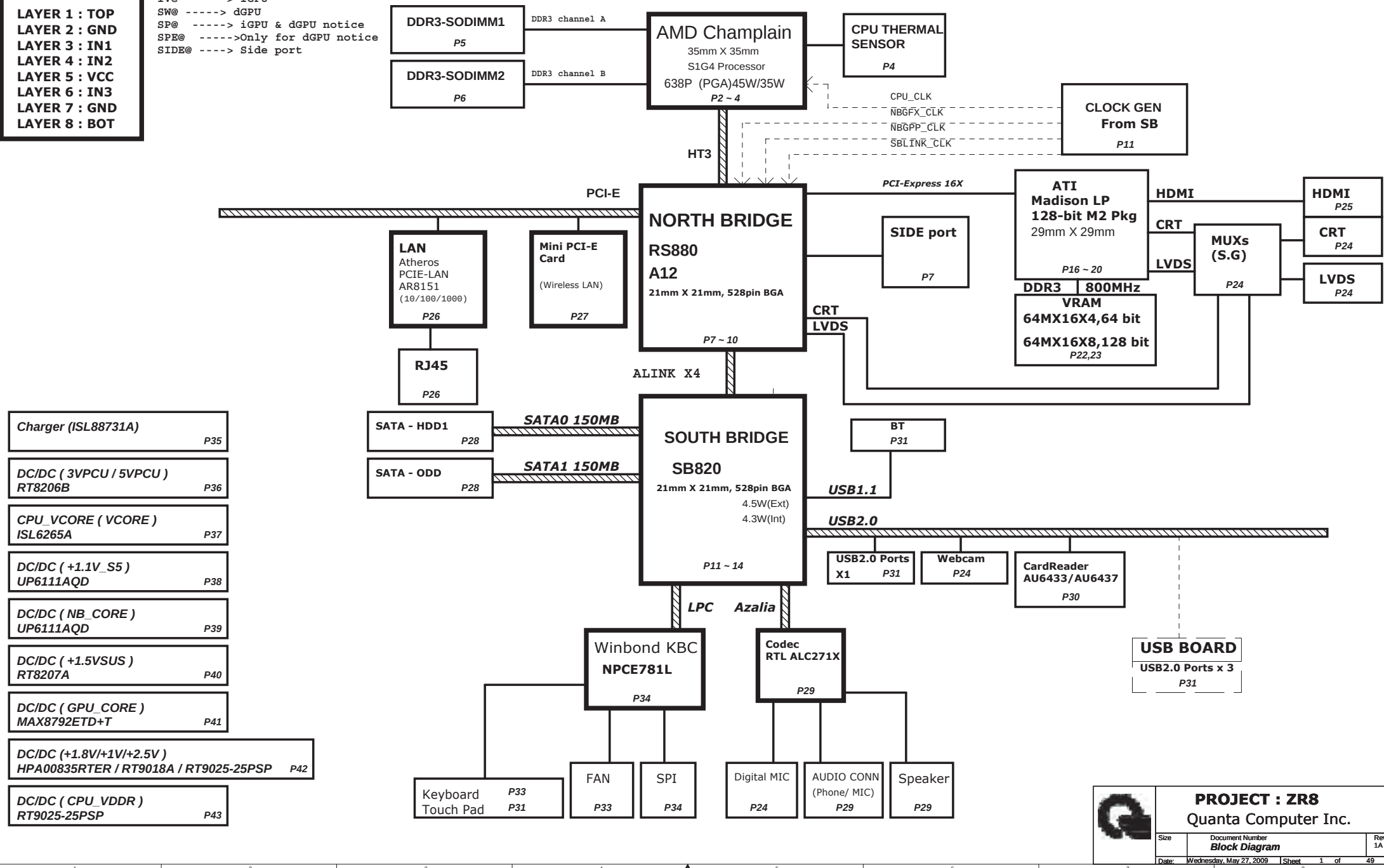
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

SGN@----->Internal CLK GEN.
GN@ ----->External CLK GEN.
IV@ -----> iGPU
SW@ -----> dGPU
SP@ -----> iGPU & dGPU notice
SPE@ ----->Only for dGPU notice
SIDE@ -----> Side port

ZR8 SYSTEM DIAGRAM



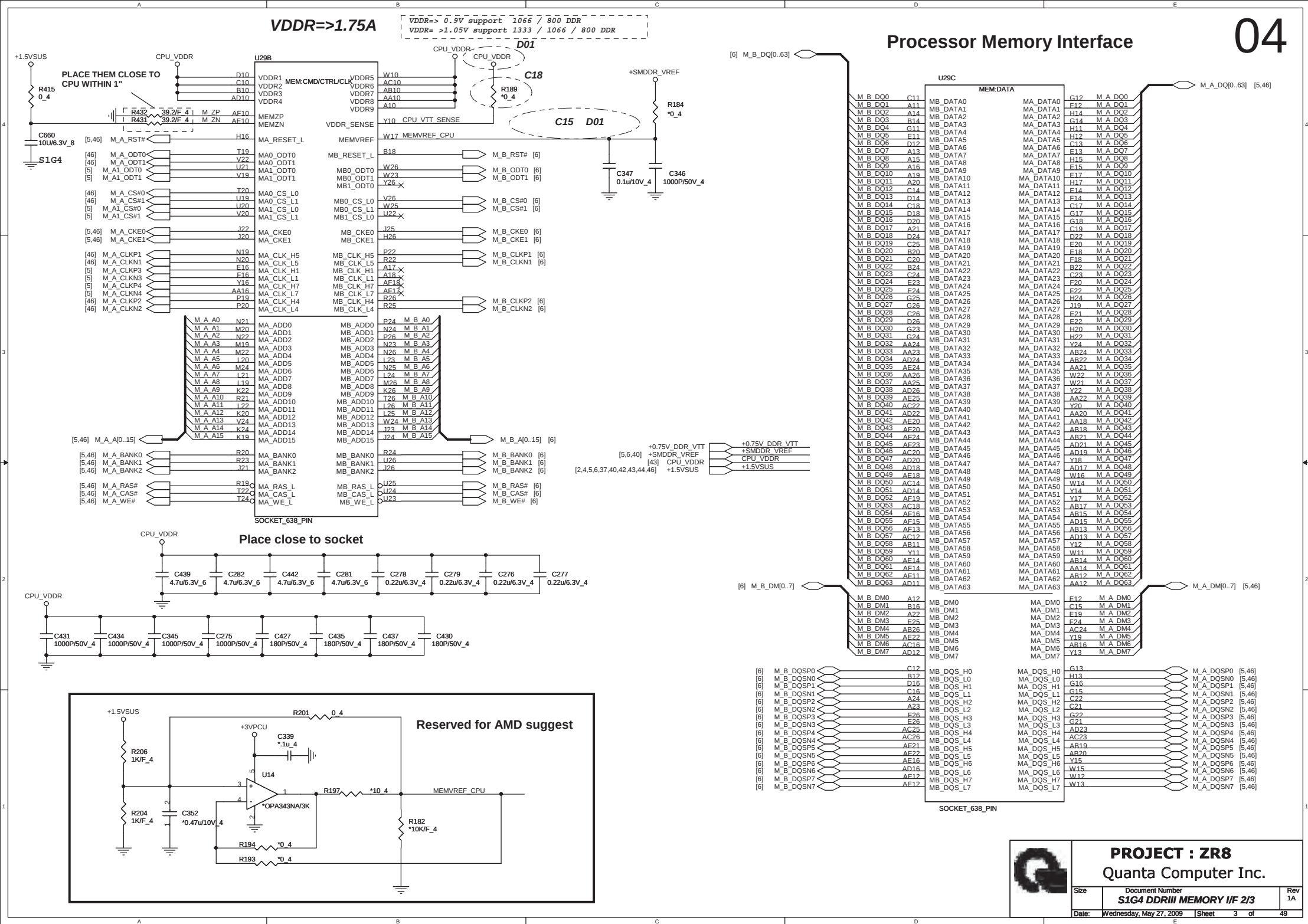
RAMP

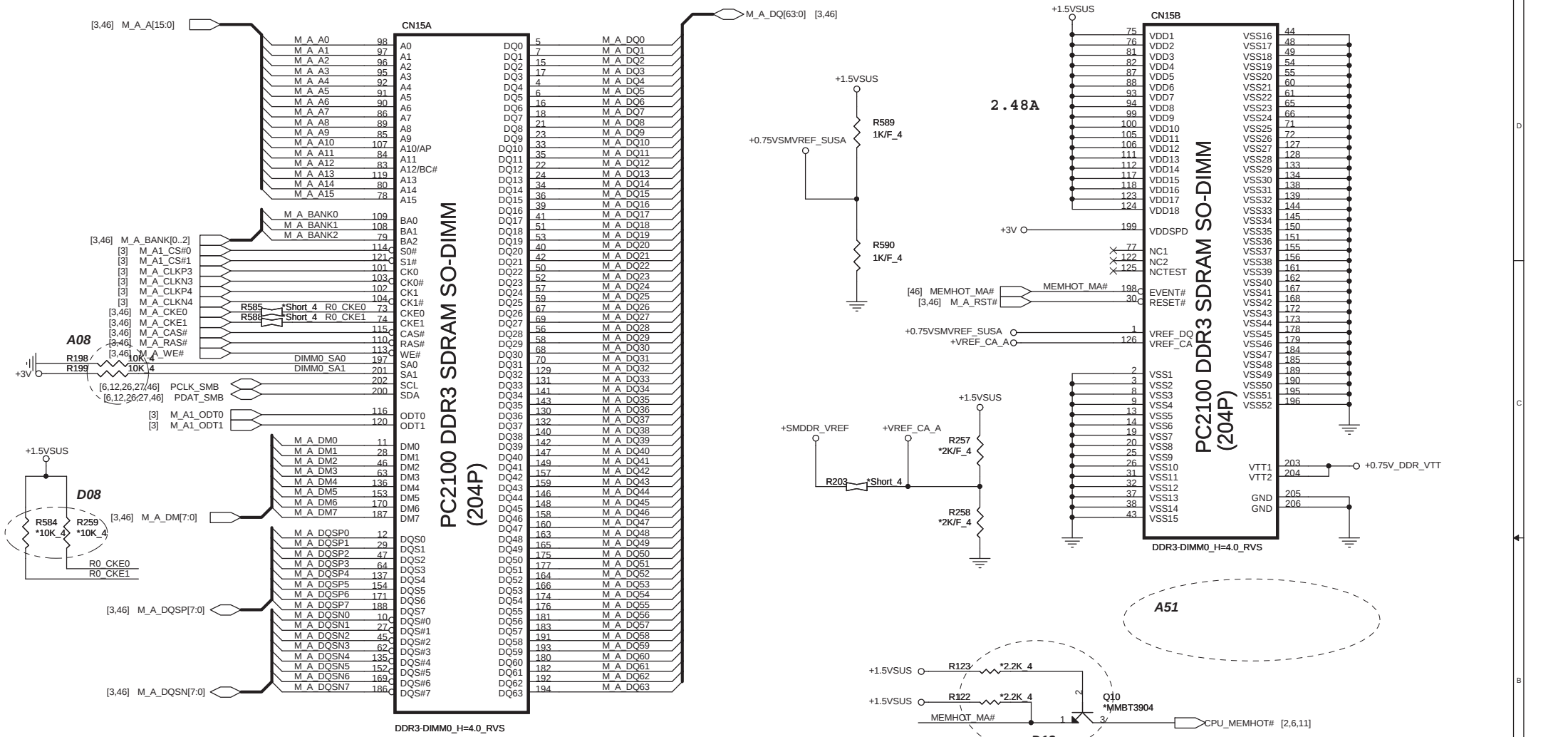


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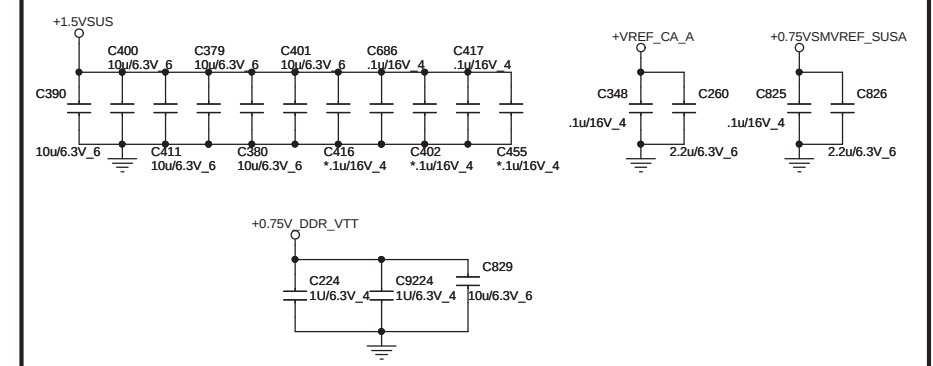
Size	Document Number	Rev
	Block Diagram	1A
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Processor Memory Interface





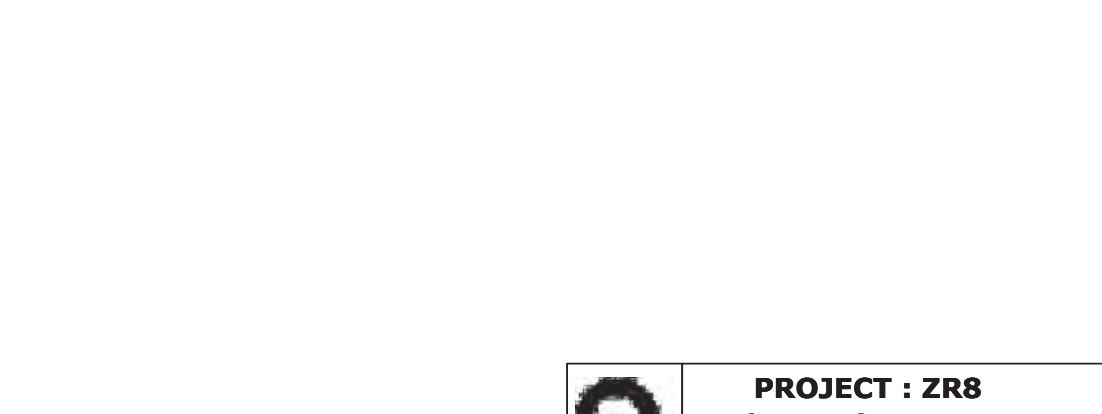
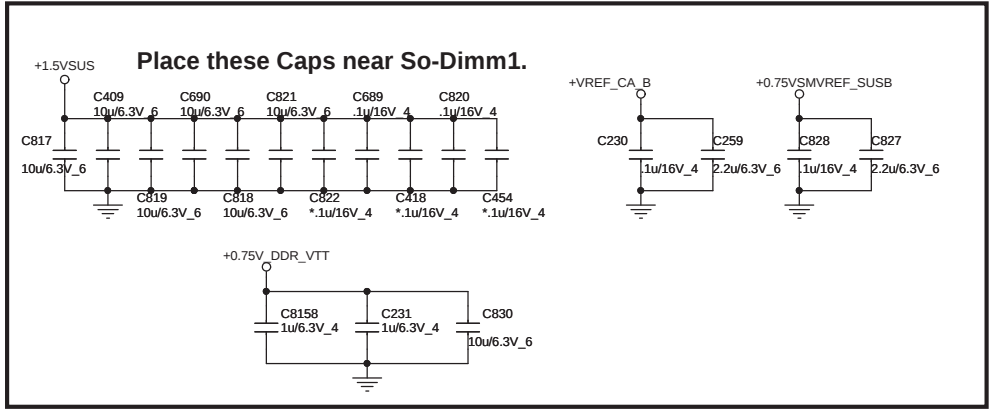
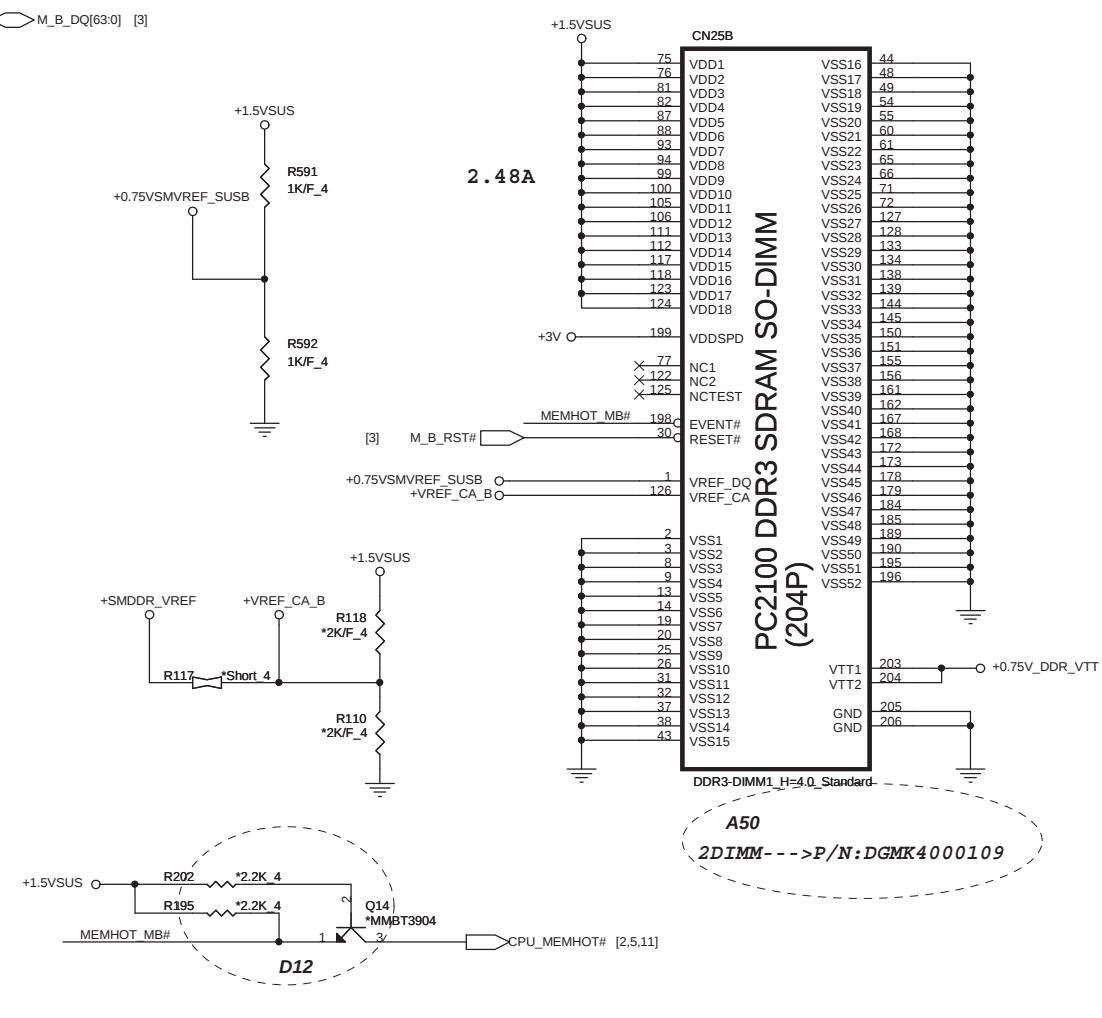
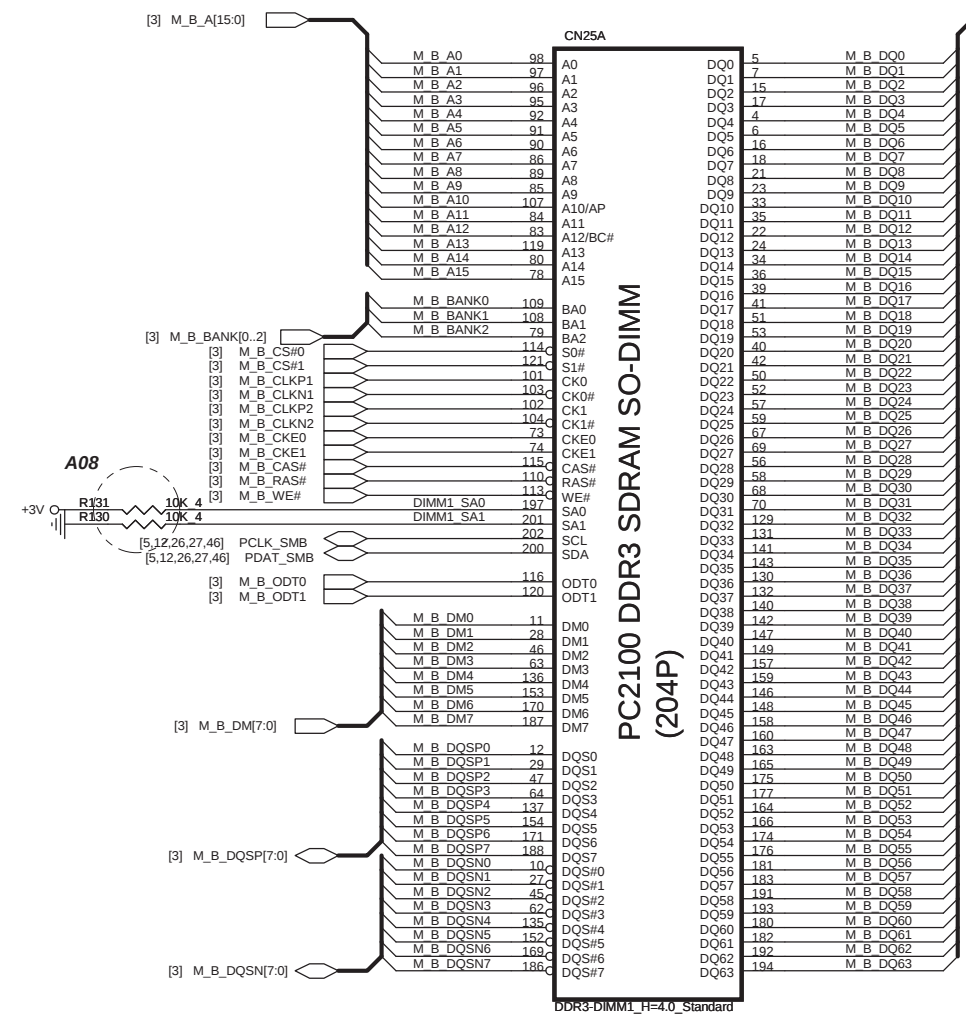
Place these Caps near So-Dimm0.



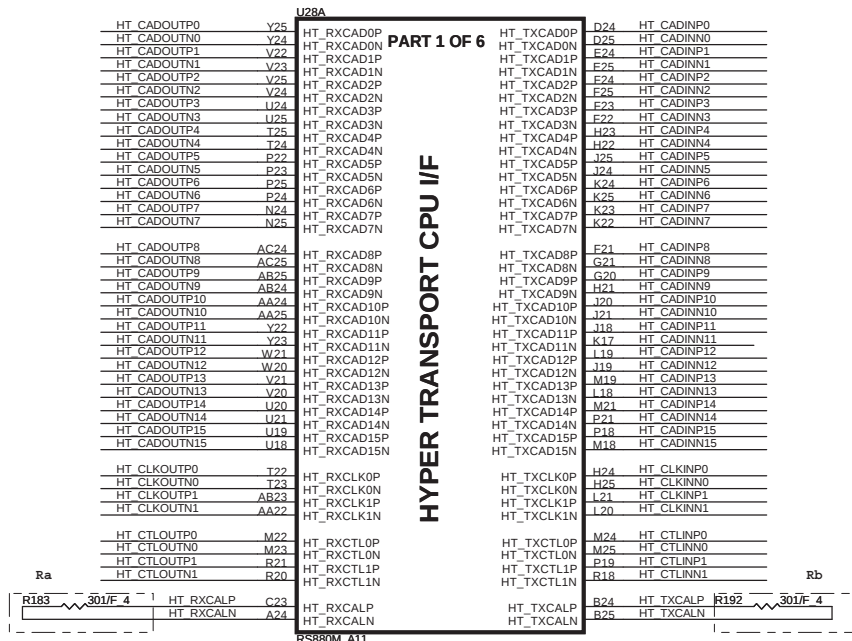
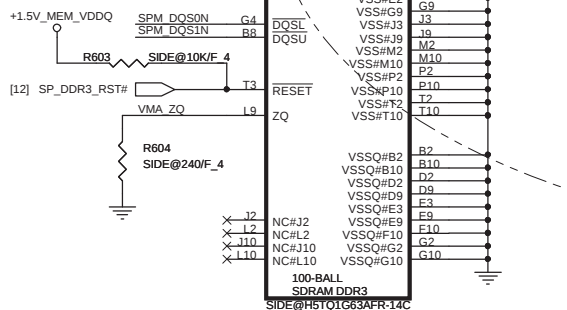
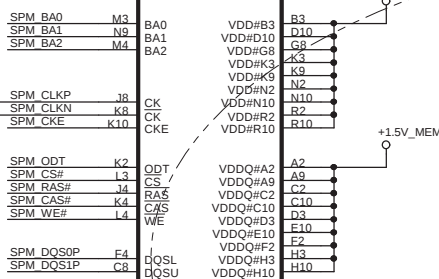
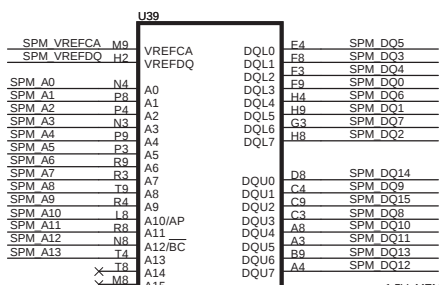
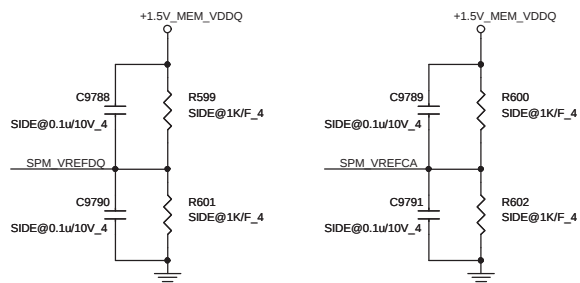


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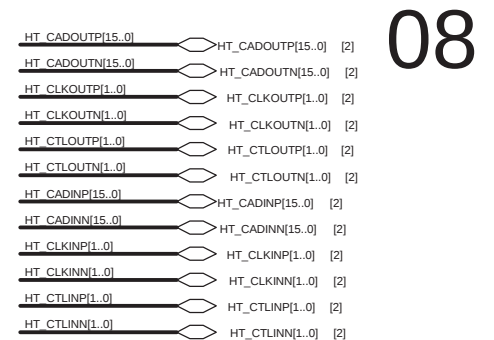
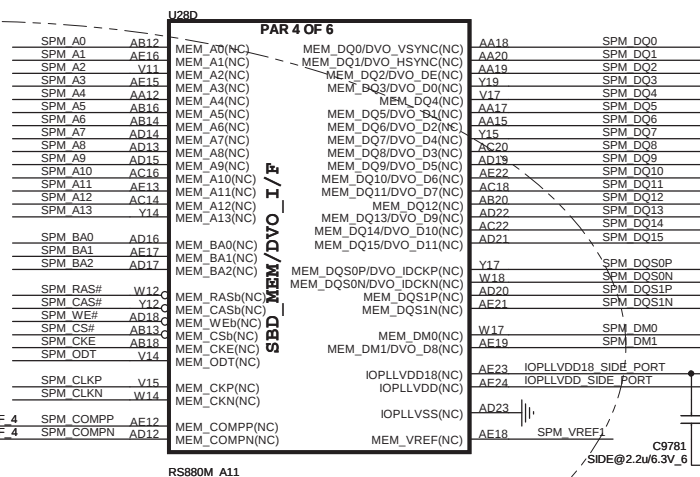
Size	Document Number DDR2 SODIMMS: A/B CHANNEL	Rev 1A
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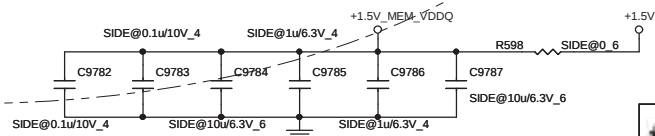
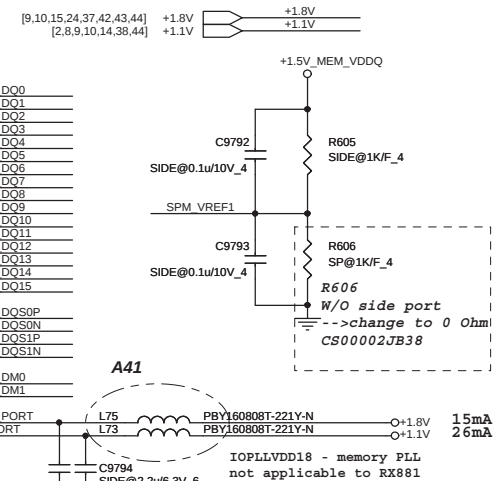


This block is for UMA only , Discrete can remove all component



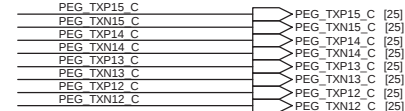
signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

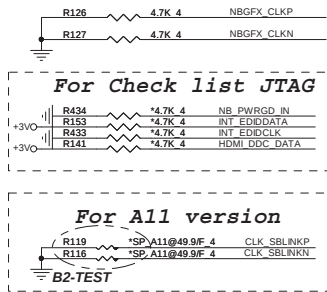


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Size	Document Number RS880M-HT LINK I/F 1/5	Rev 1A
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RS880 Display Port Support (muxed on GFX)

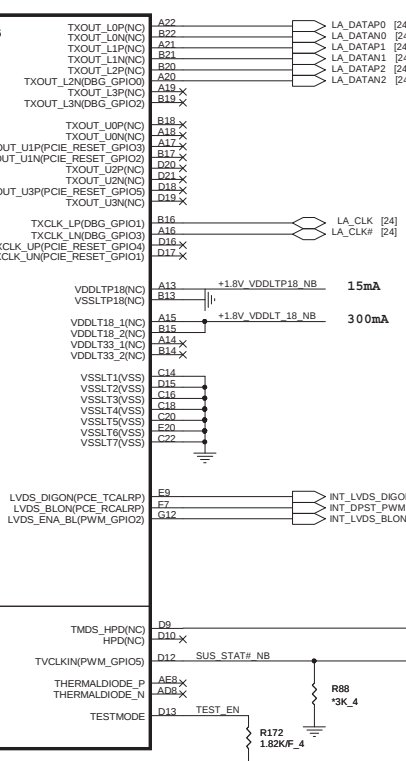
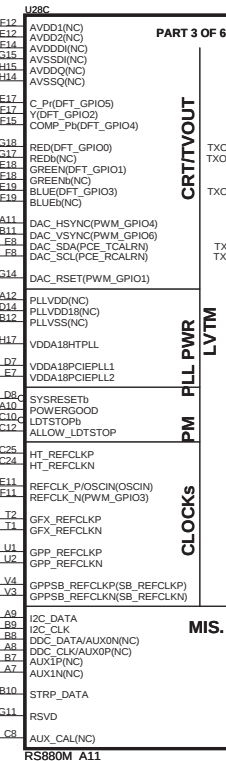
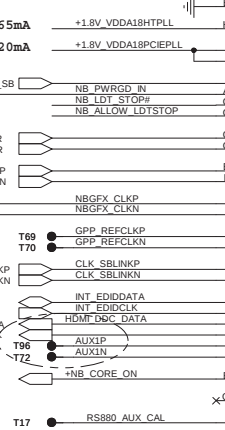
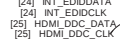
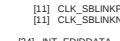
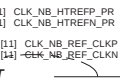


UMA use 140 ohm 1%.
Discrete use 133 ohm 1%.
Note: Only for RS880 series A11 ASIC errata.

Only for UMA
VGA (Not
applicable to
RX881)



B2-TEST
D06



STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO.

RS880M
1 Disable
0 Enable



RS880M: Enables Side port memory

RS880M:INT_CRT_HSYNC

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

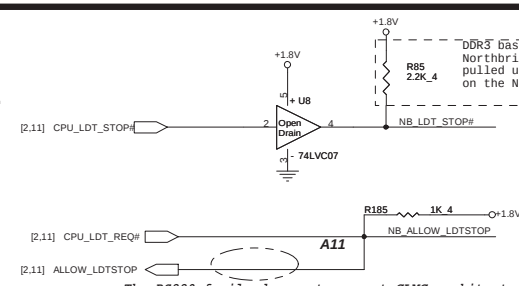
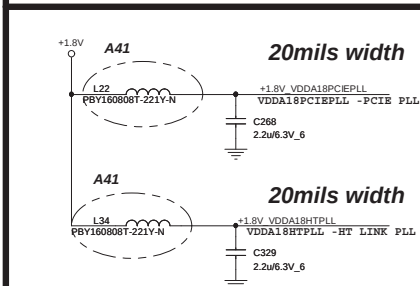
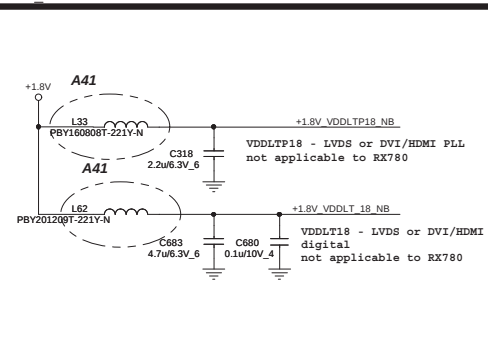
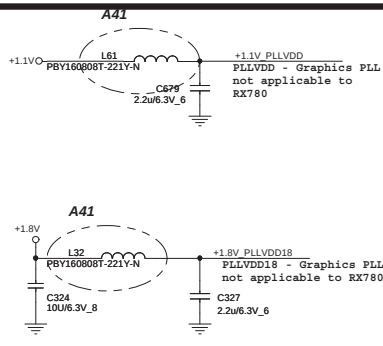
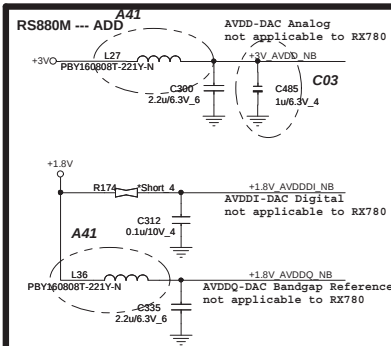


For external EEPROM Debug only

RS780/RX780/RS880



Display Port interface from PCIeGraphics (RS880/rs880M only)



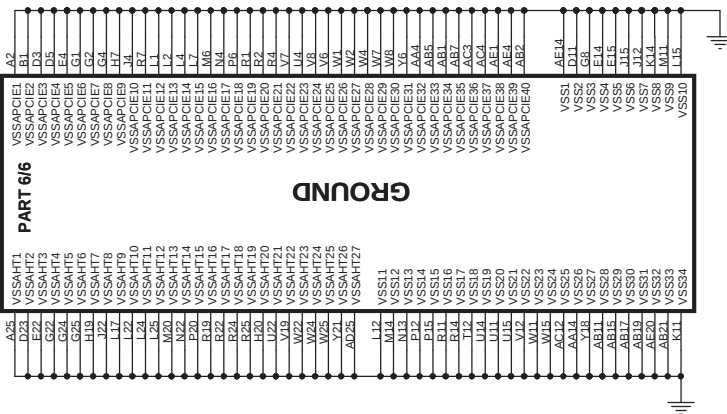
The RS880 family does not support CLMC architecture
The LDTREQ# connection from the CPU to
ALLOW_LDTSTOP of the Northbridge is no longer
required.



PROJECT : ZR8
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Size	Document Number	Rev
	RS880M-SYSTEM I/F 3/5	1A
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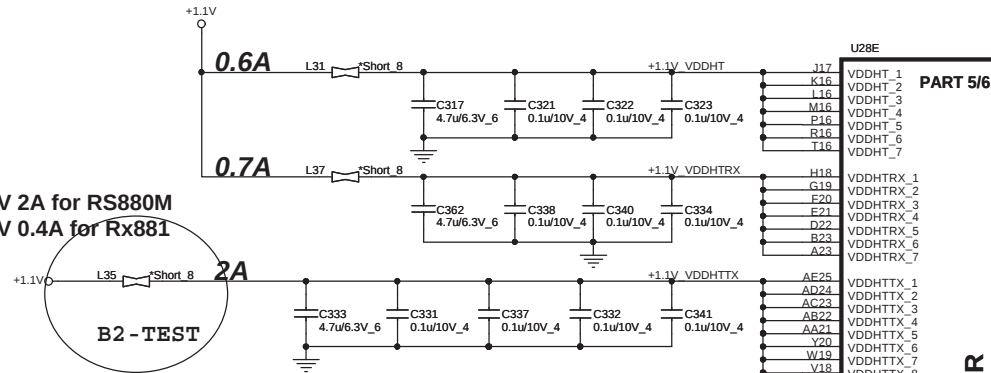
U28F



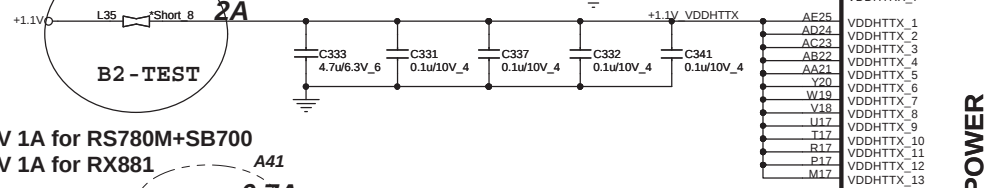
RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDL18	GND	+1.8V
IOPLLVD18	+1.8V	+1.8V	VDDL18	NC	NC

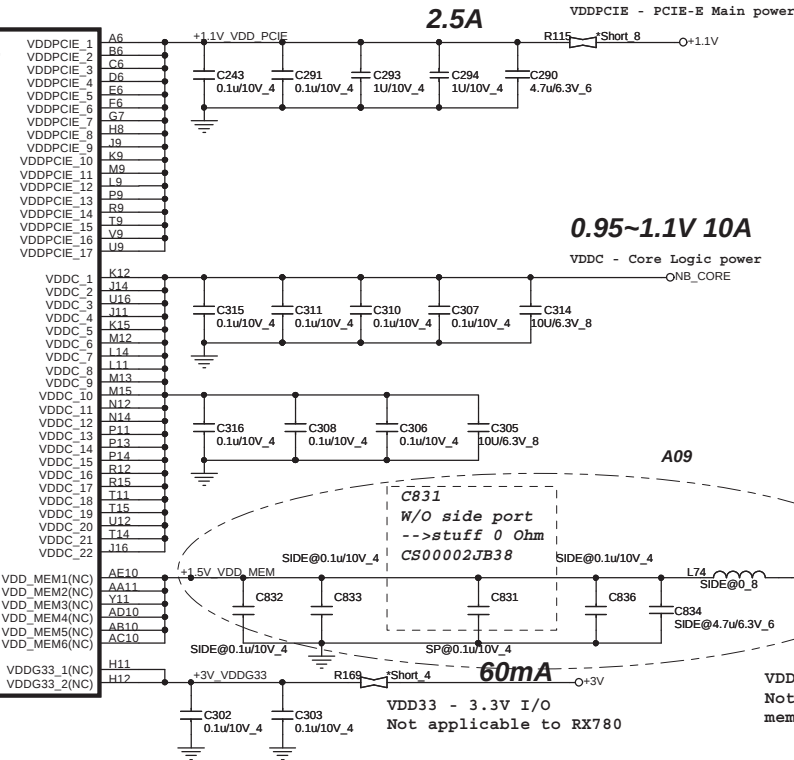
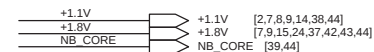
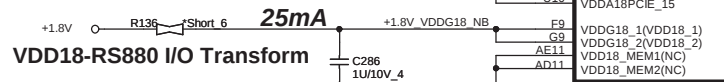
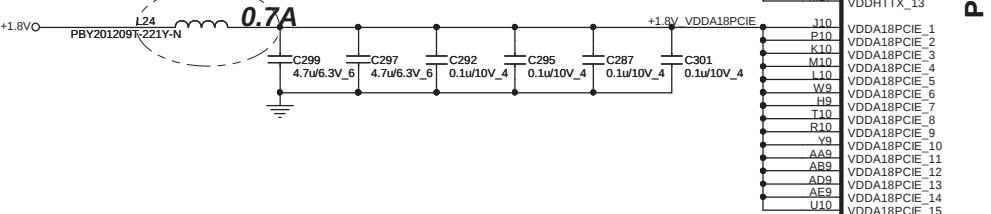
+1.1V 2A for RS880M
+1.1V 1.3A for RX881



+1.1V 2A for RS880M
+1.2V 0.4A for Rx881



+1.8V 1A for RS780M+SB700
+1.8V 1A for RX881

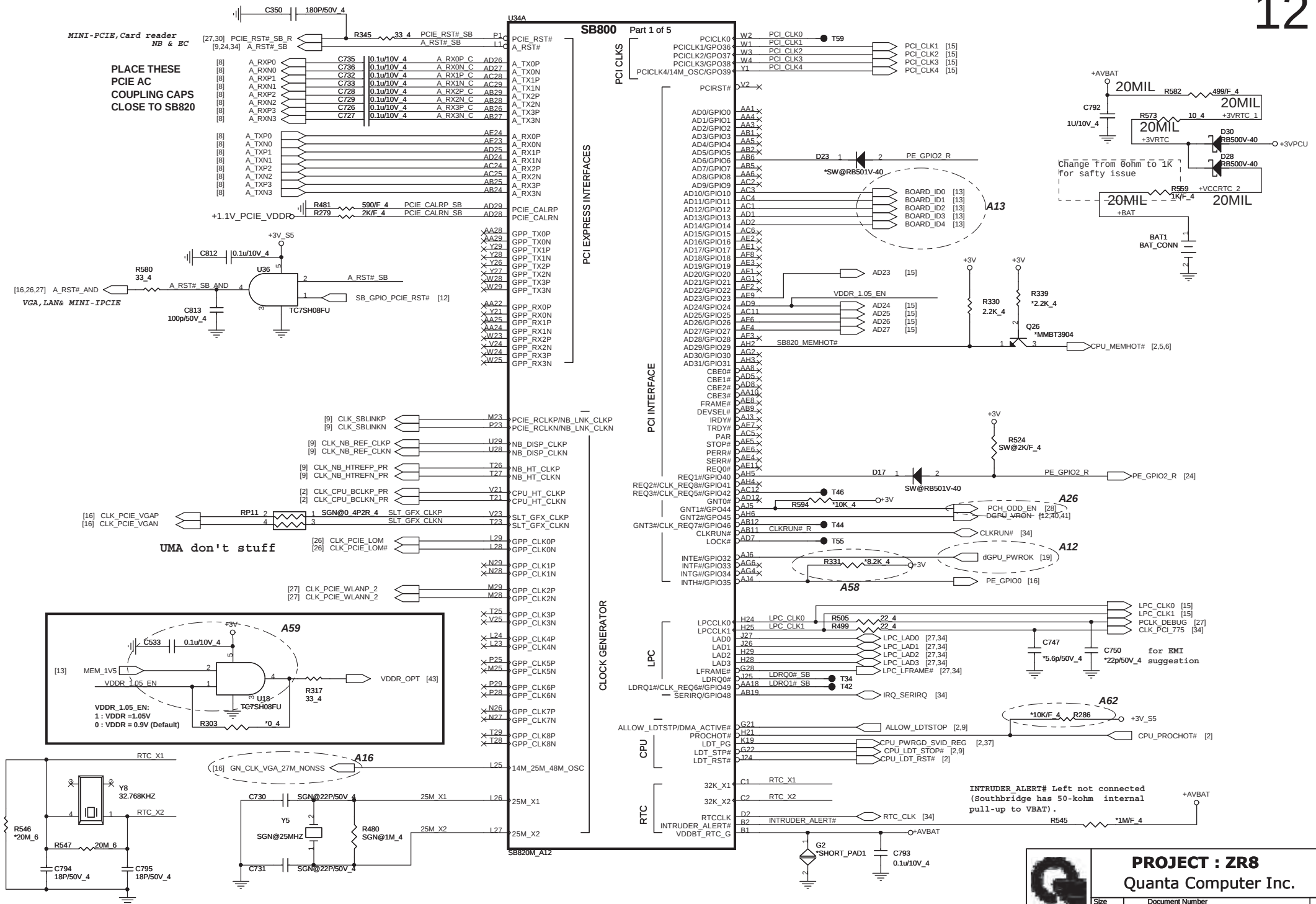


VDD MEM For UMA RS780 only
 Not applicable to RX780
 memory I/O transform



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Size	Document Number	Rev 1A
	RS880M-POWER5/5	
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NC only ,Can't be install

R352 *2.2K 4 SB TEST0
R350 *2.2K 4 SB TEST1
R347 *2.2K 4 SB TEST2

SCL0/SDATA0 is 3V tolerance
AMD datasheet define it

R288 2.2K 4 PCLK SMB
R287 2.2K 4 PDAT SMB

Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

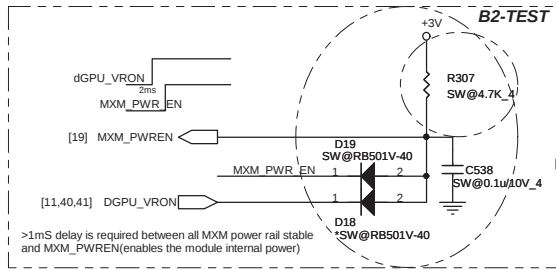
SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it

R348 10K 4 SB SMBCLK1
R346 10K 4 SB SMBDATA1

SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it

R290 10K 4 SB SCLK2
R283 10K 4 SB SDATA2

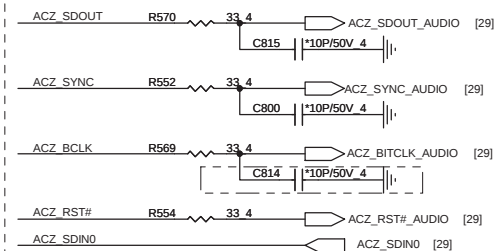
R338 4.7K 4 SUS_STAT#



A14

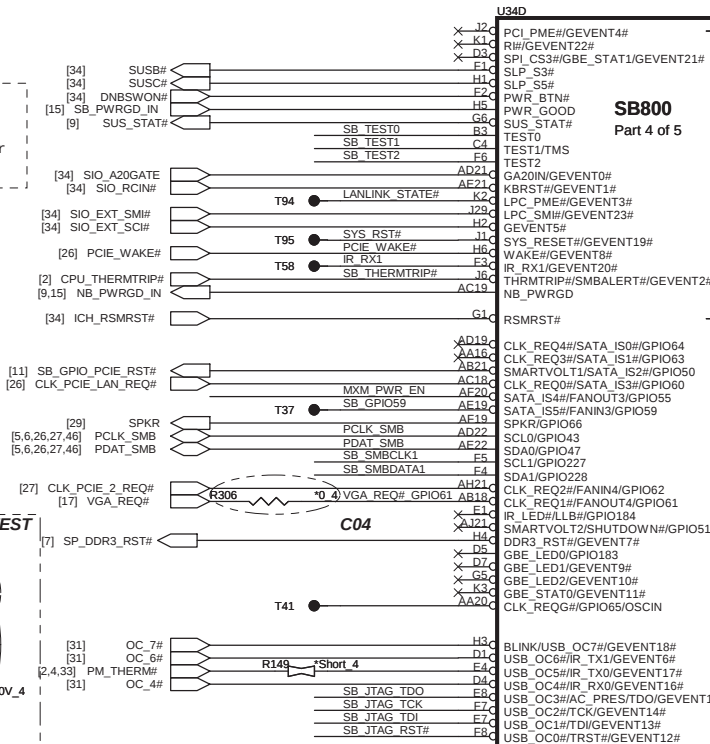
A61

R474 8.2K 4 CLK_PCIE_LAN_REQ#
R498 8.2K 4 CLK_PCIE_2_REQ#



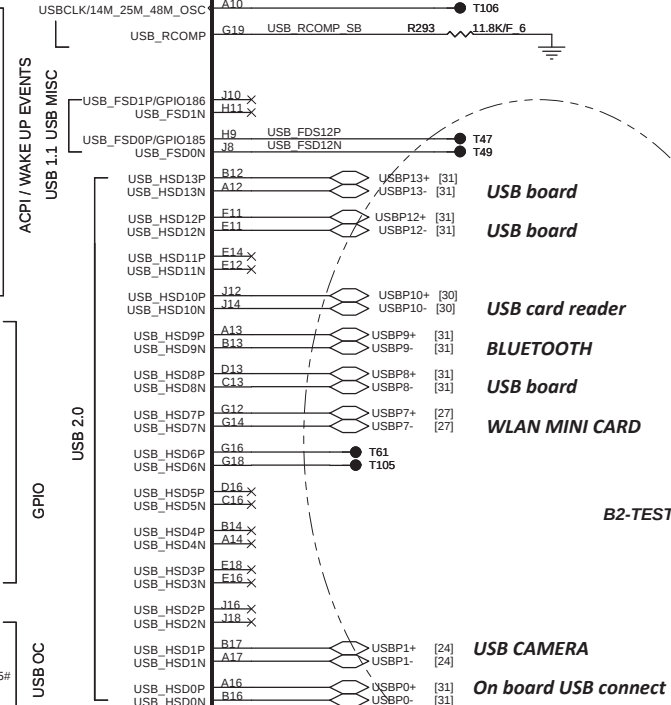
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDI0[3:0] can not be connected to 3.3-V devices.

[11,13,14,15,24,26,31,32,36,44]
[2,4,5,6,9,10,11,13,14,15,19,24,25,27,29,30,32,33,34,36,37,38,39,41,42,43,44,46]



+3V_S5
+3V

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT_CLKGEN mode.
It is output CLK source when INT_CLKGEN mode.



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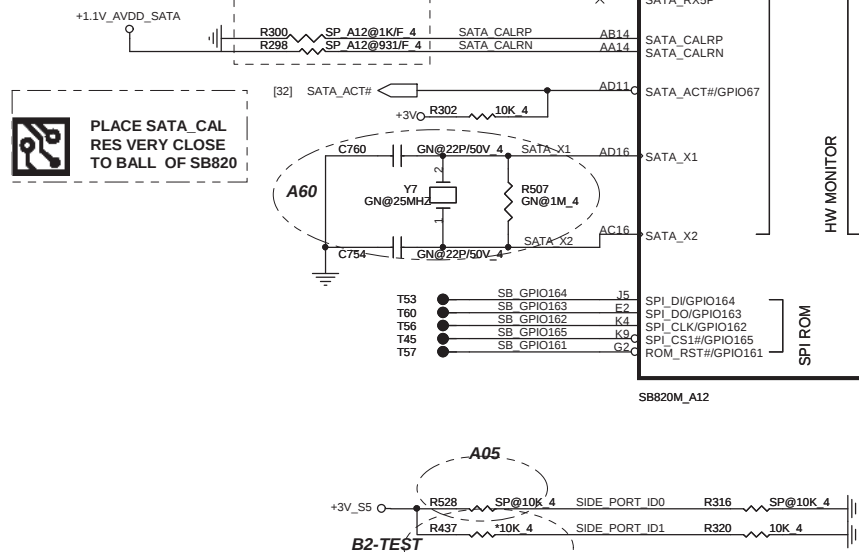
Size	Document Number	Rev
	SB820-ACPI/GPIO/USB 2/4	1A
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SATA PORT 0,1,2,3
can support AHCI
mode

SATA1

SATA ODD

Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. P/N:CS18062FB00(806 Ohm)
SATA_CALRN	SB800 A12: 1k ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931-? 1% resistor to VDDAN_11_SATA.
SATA_CALRN	SB800 A12: TBD-? 1% resistor to VDDAN_11_SATA.



DDR3 Sideport Memory Device

Vendor	Vendor P/N	STN B/S P/N	Size	BOARD_ID2 GPIO12	SIDE_PORT_ID1 GPIO178	SIDE_PORT_ID0 GPIO177
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	0 (WO/Sideport)	0	0
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	1 (W/Sideport)	0	1

	ID1	ID0
HYX	0	0
SAM	0	1
ATI	1	0

[14] +1.1V AVDD_SATA
[11,12,14,15,24,26,31,32,36,44] +3V_S5

14

SB800
Part 2 of 5

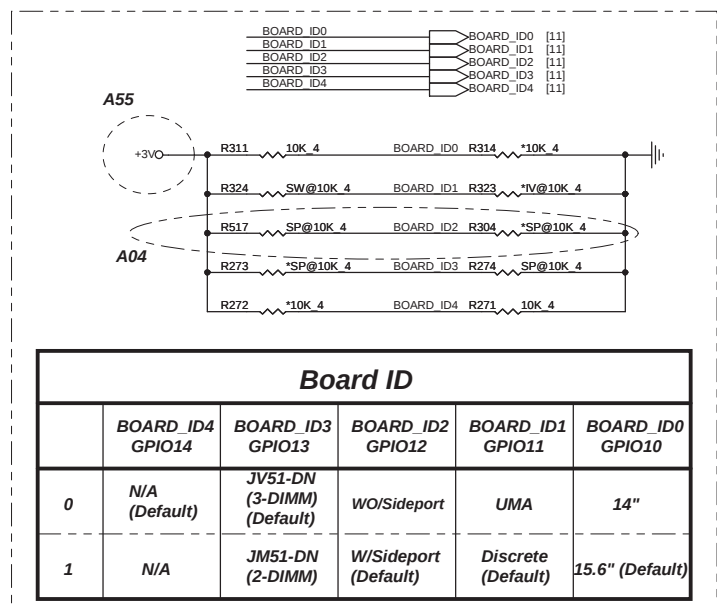
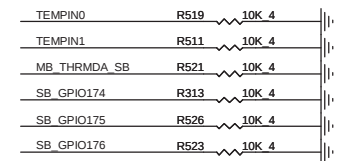
FLASH

SERIAL ATA

HW MONITOR

SPI ROM

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY



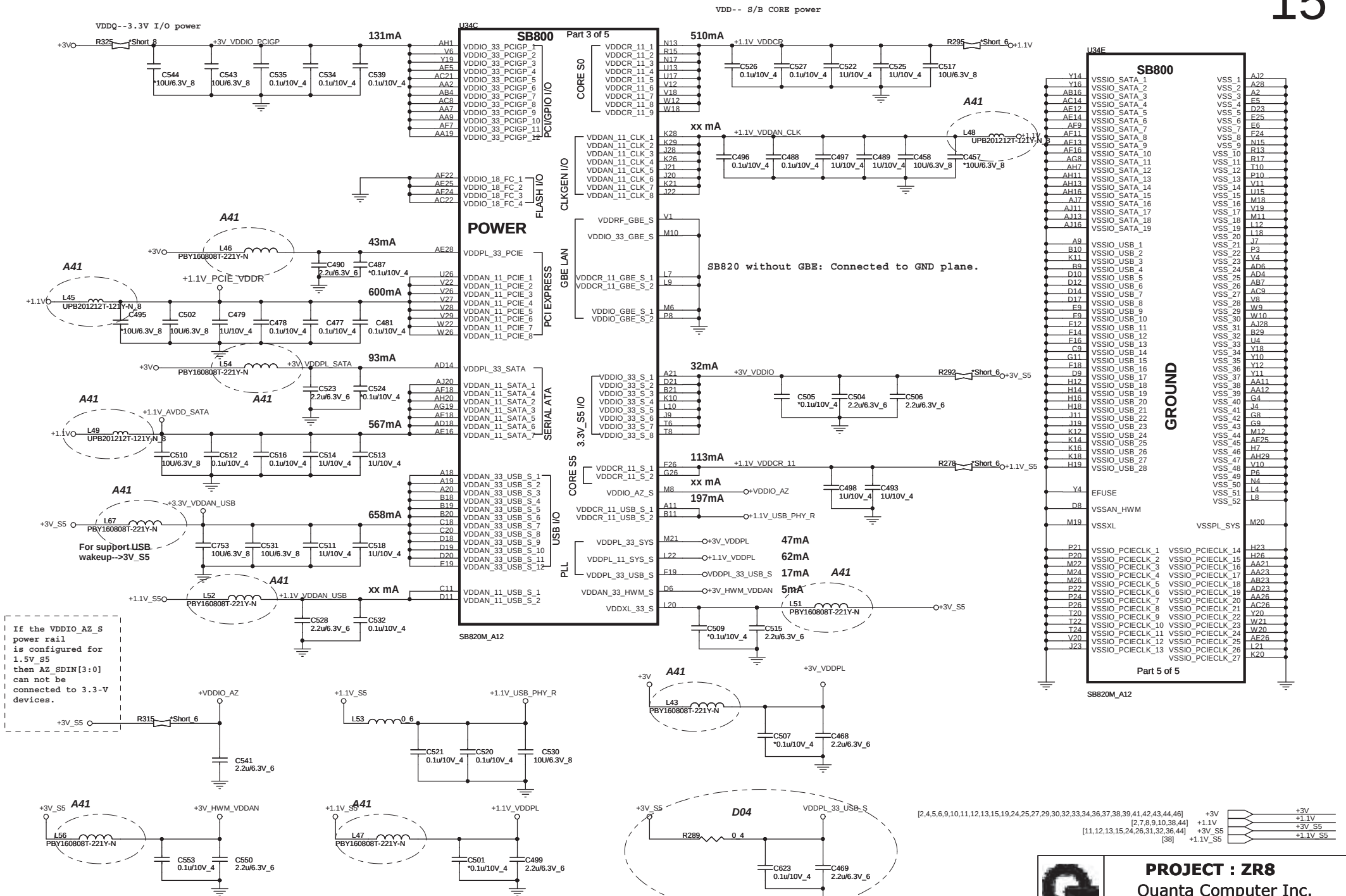
Board ID

	BOARD_ID4 GPIO14	BOARD_ID3 GPIO13	BOARD_ID2 GPIO12	BOARD_ID1 GPIO11	BOARD_ID0 GPIO10
0	N/A (Default)	JV51-DN (3-DIMM) (Default)	WO/Sideport	UMA	14"
1	N/A	JM51-DN (2-DIMM)	W/Sideport (Default)	Discrete (Default)	15.6" (Default)

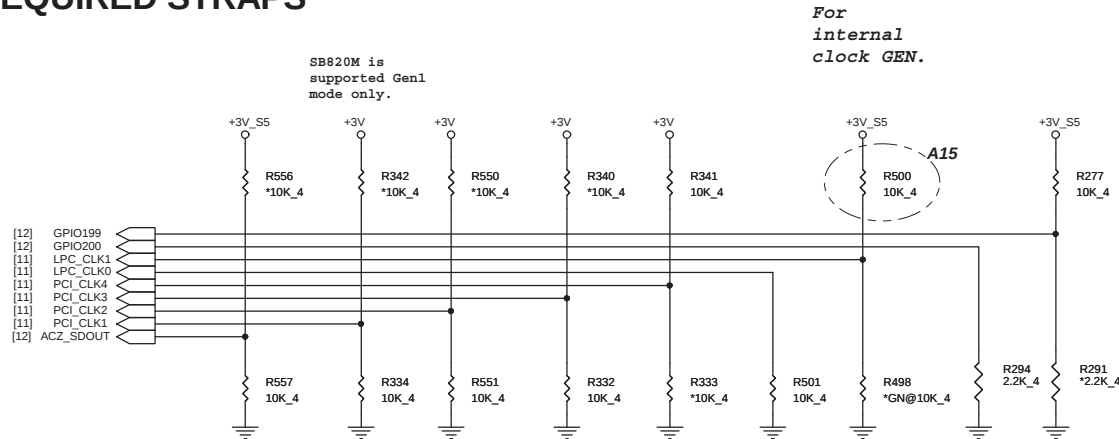


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PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE



REQUIRED STRAPS

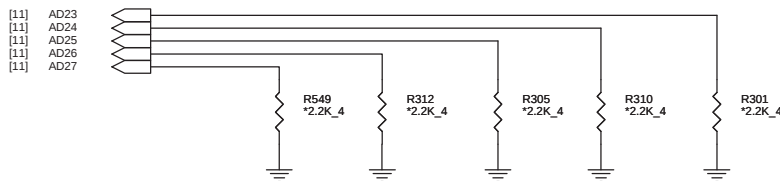


D02	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	This is required as the low power mode is not supported on the SB8xx	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	INT. CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	EXT. CLKGEN ENABLE	L, H=LPC ROM L, L=FWH ROM	DEFAULT

internal have
pull Hi 10K

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

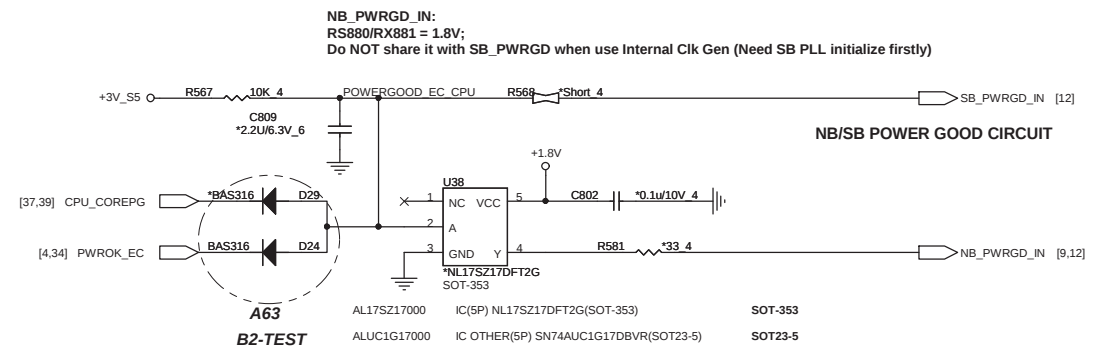


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE I2C ROM DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL	ENABLE PCI MEM BOOT



OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

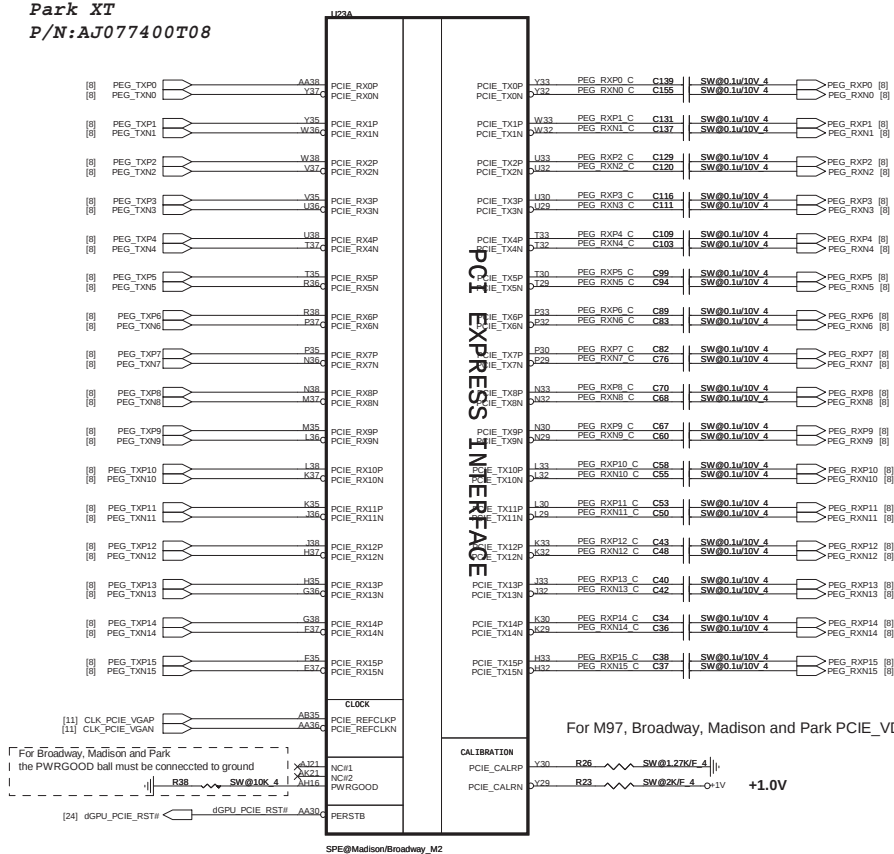
16

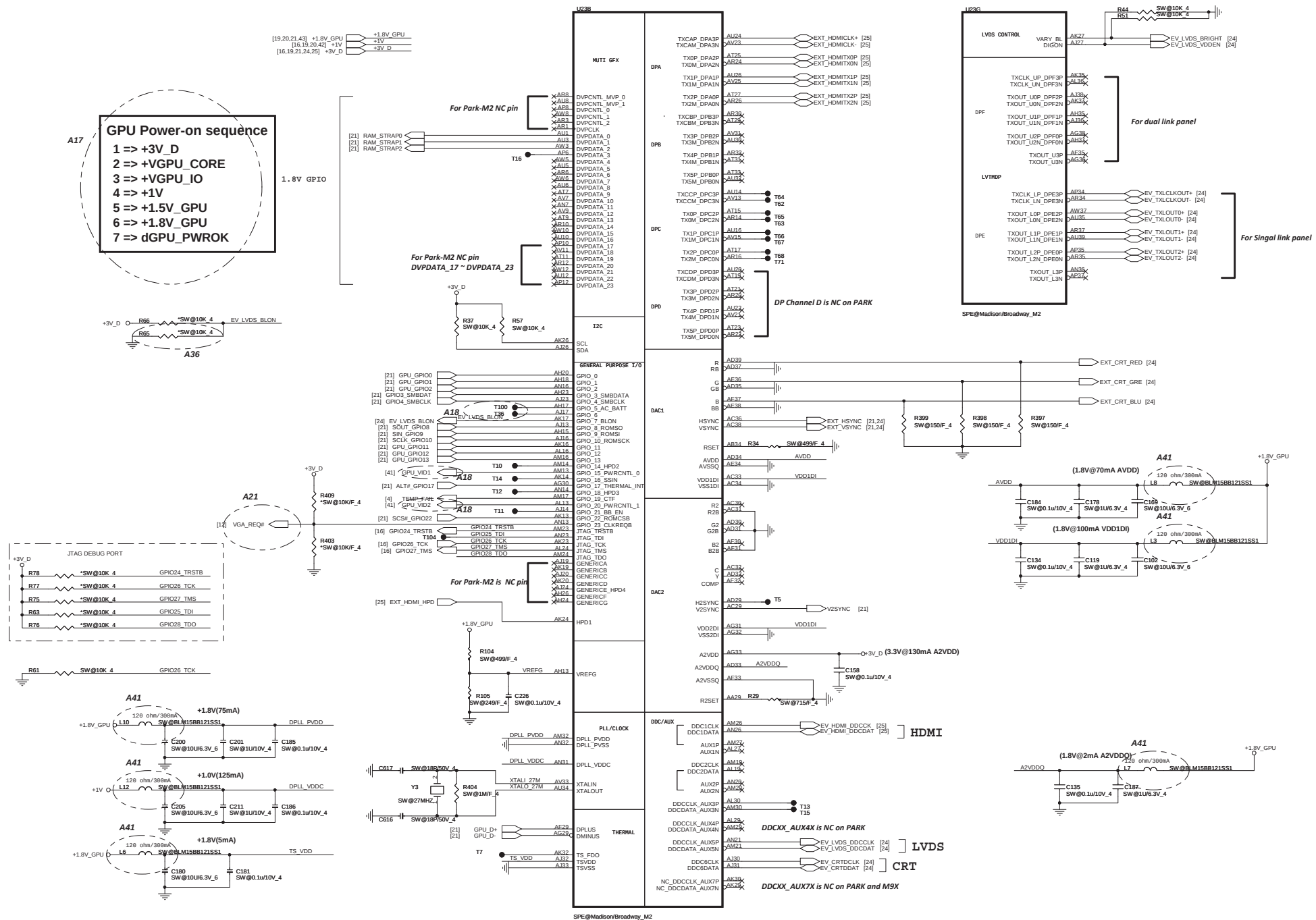


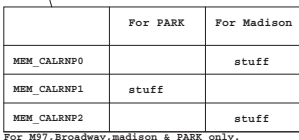
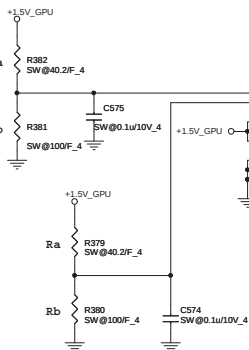
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Park XT
P/N: AJ077400T08

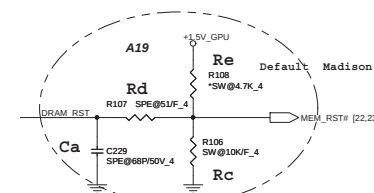
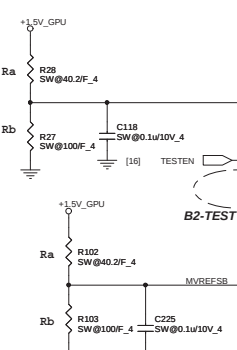






	GDDR5	GDDR3	DDR3(Default)
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

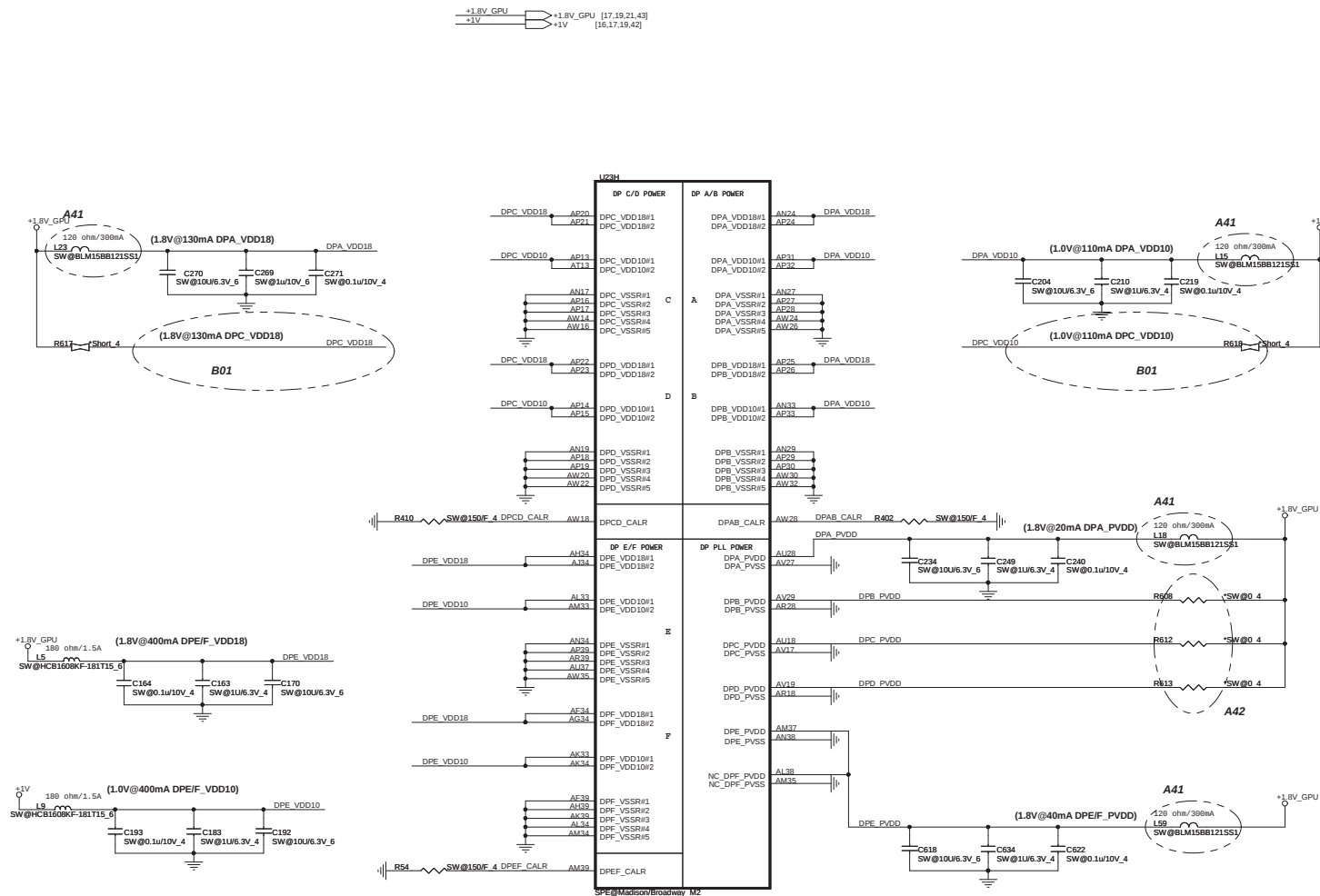
Broadway no dual rank support for GDDR5



This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.

Size	Document Number Madison/Broadway-MEM I/F	Re 1A
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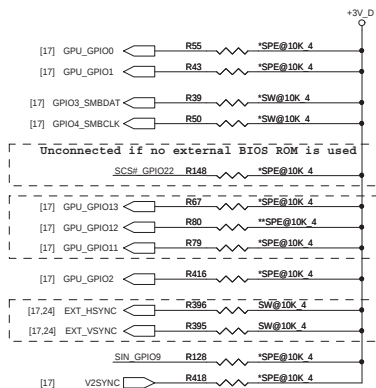




PROJECT : ZR8
Quantia Computer Inc.

Size	Document Number	Rev
	Madison/Broadway (DP_PWR/GND)	1A
DATE:	Wednesday, May 27, 2020, 15:00	of 49

PIN STRAPS



Memory Aperture size

GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

Function Table

EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

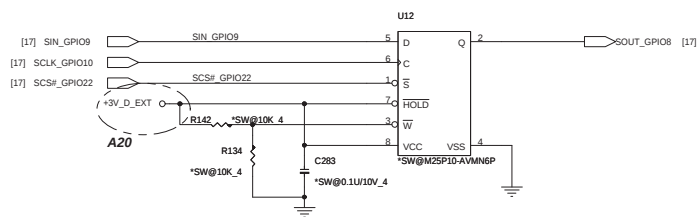
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

Z88

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
BIOS_ROM_EN	GPIO_22_ROMCSB		0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX_M25P10A:101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	(Recommended setting as 5.0GT/s capability will be controlled by software.)
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable 1 = VGA controller capacity disable (The device will not be recognized as the system's VGA controller.)	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET. 1 = DRIVER would use the value sample on VHAD_0 during RESET.	0	

SERIAL ROM

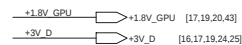
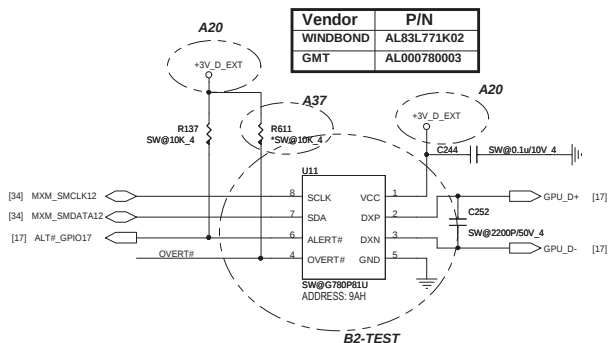


DDR3 Memory Aperture size

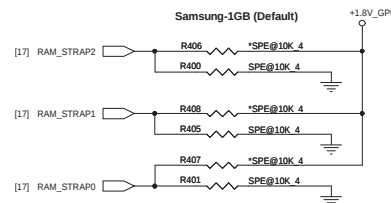
DDR3 Memory Aperture size

Vendor	Vendor P/N	STN B/S P/N	GPU	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	Park	1	1	0
			Madison	1	0	0
			2Gb	1	1	1
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	Park	0	1	0
			Madison	0	0	0
			2Gb	0	0	1
AMD	23EY2387MA12-SZ	AKD5LGGT700	Park	0	1	1
			Madison	1	0	1

Thermal Sensor



Samsung-1GB (Default)

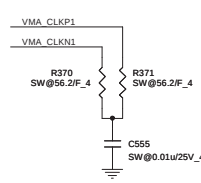
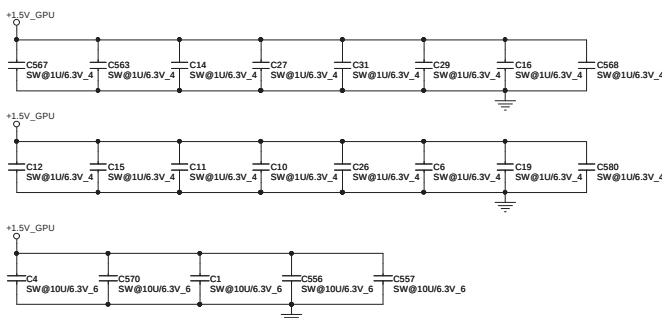
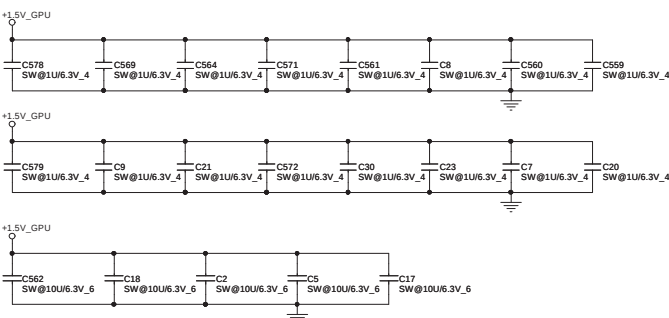
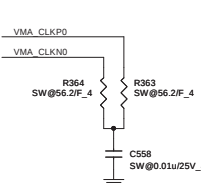
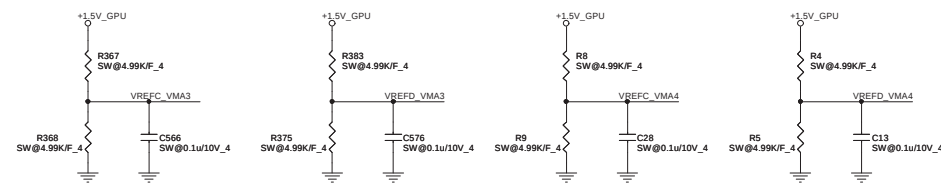
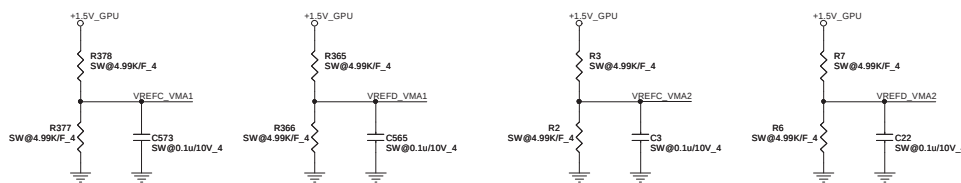


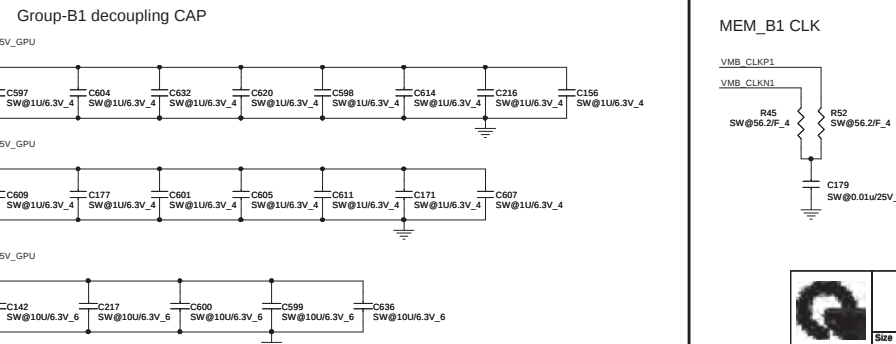
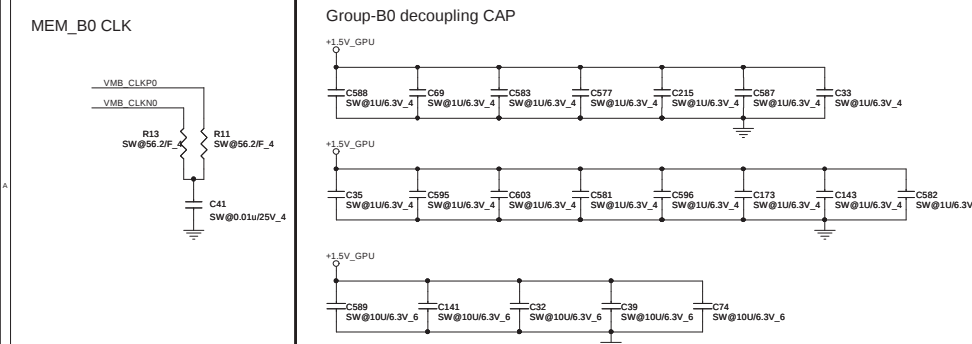
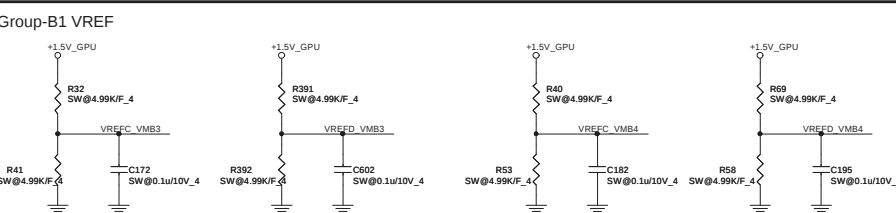
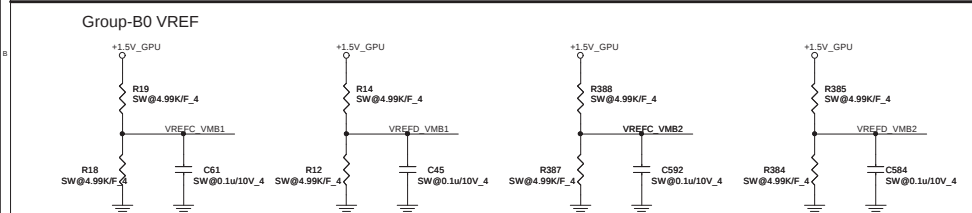
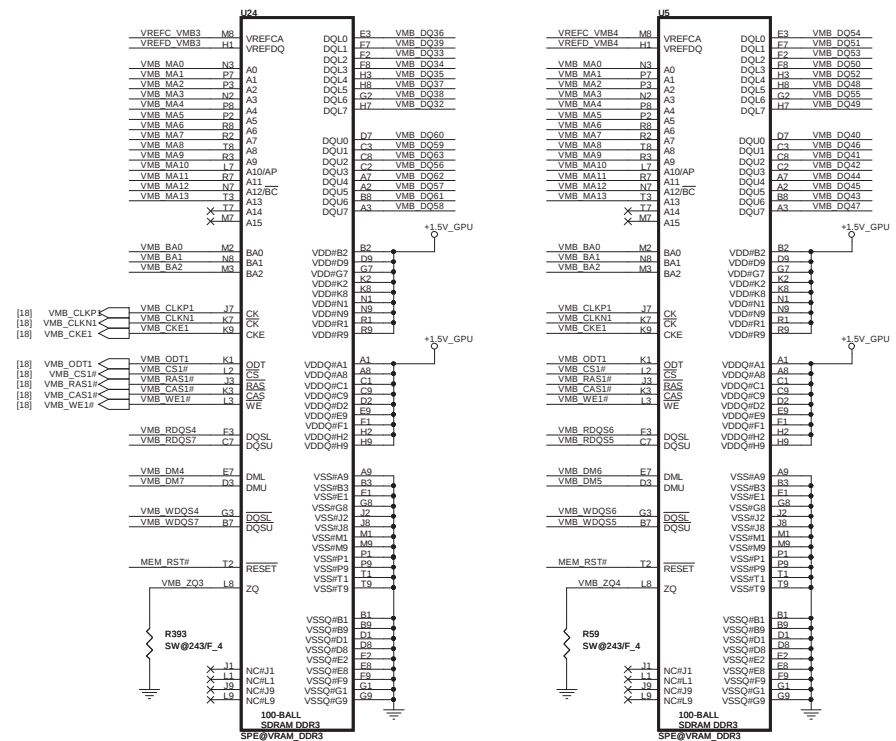
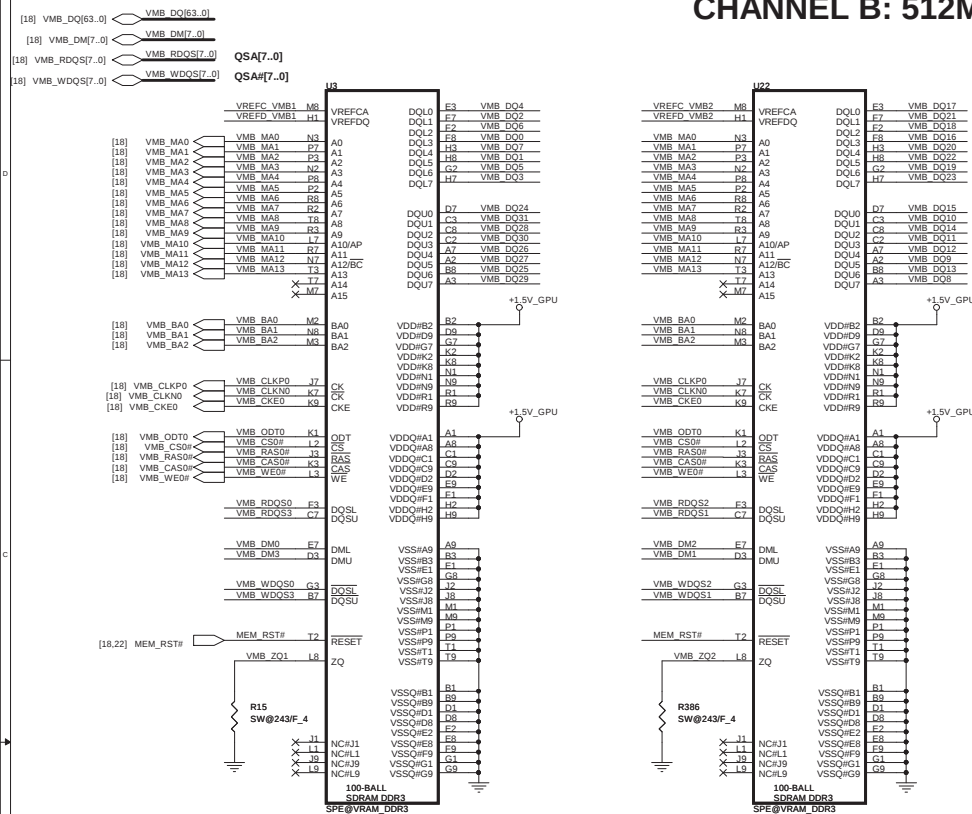
RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

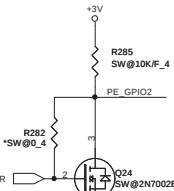
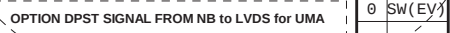


PROJECT : Z88
Quanta Computer Inc.

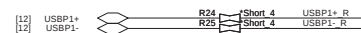
Size Document Number
Strip/Thermal
Date: Wednesday, May 27, 2009 Sheet 21 of 49





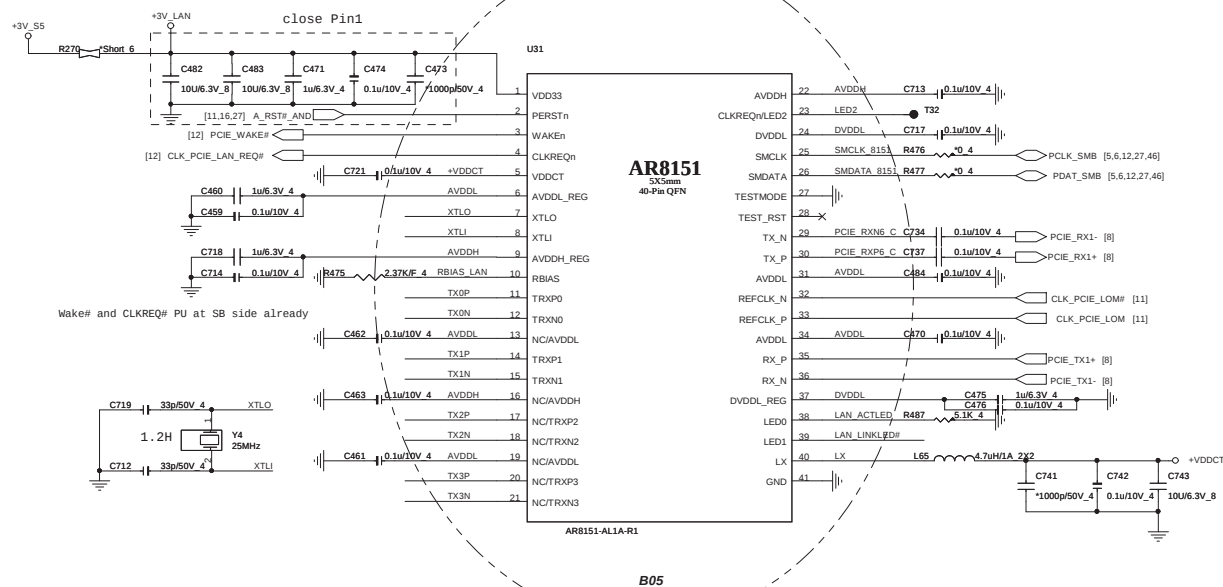


OPTION SIGNAL FROM NB to LVDS for UMA					
LA_CLK#	RP5	1		2	*IV@0 4P2R 4 T
LA_CLK	3		4		
LA_DATAN0	RP4	1		2	*IV@0 4P2R 4 T
LA_DATA0	3		4		
LA_DATAN1	RP3	1		2	*IV@0 4P2R 4 T
LA_DATA1	3		4		
LA_DATAN2	RP2	1		2	*IV@0 4P2R 4 T
LA_DATA2	3		4		

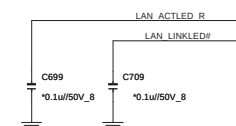
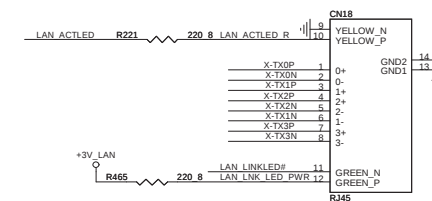


Size	Document Number	P
	CRT/LVDS/LID	1
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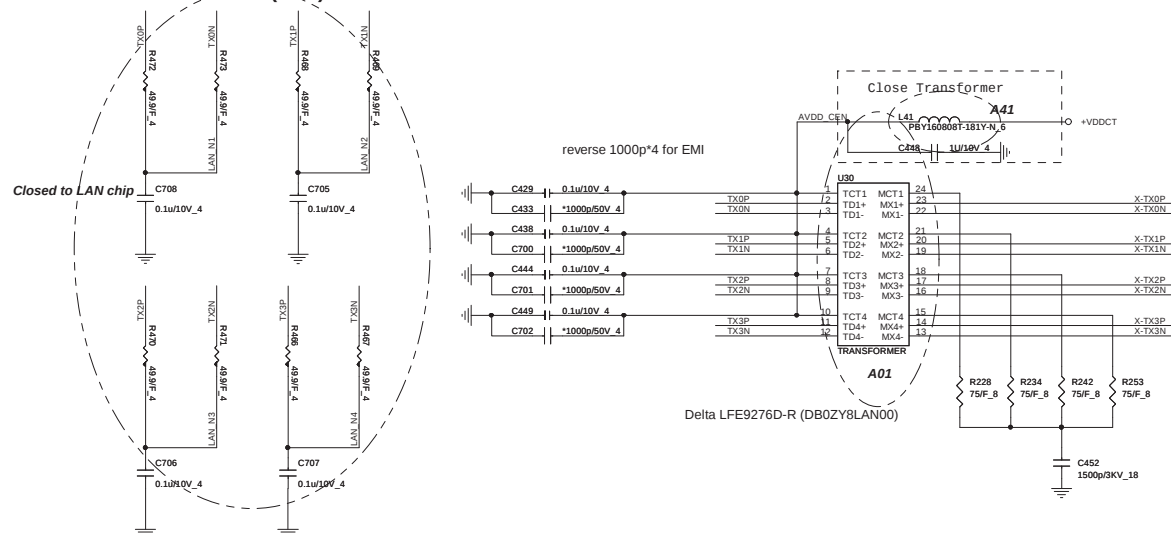
Giga-LAN AR8151



RJ45(LAN)



TRANSFORMER(LAN)

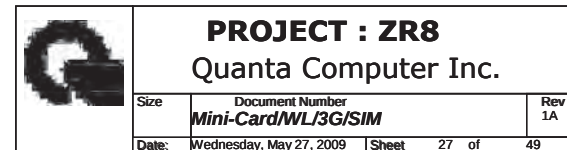


PROJECT : ZR8
Quanta Computer Inc.

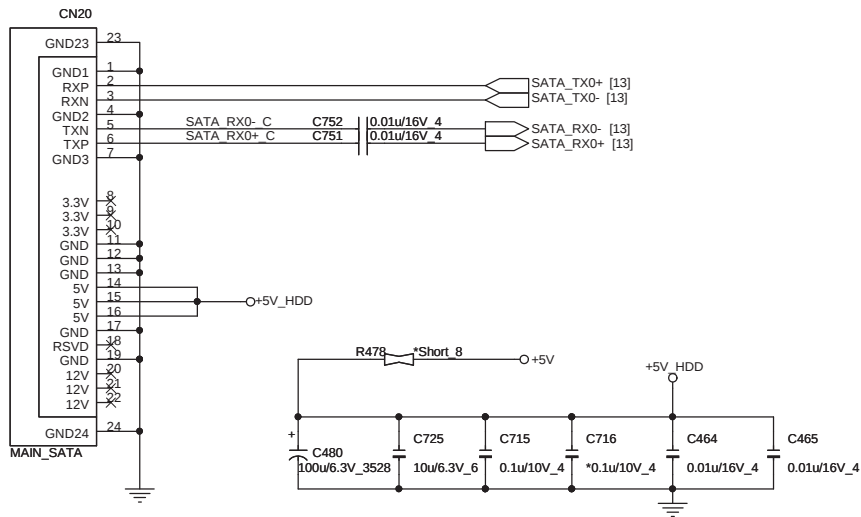
Size Document Number
LAN (AR8151)
 Date: Wednesday, May 27, 2009 Sheet 26 of 49

Rev
 1A

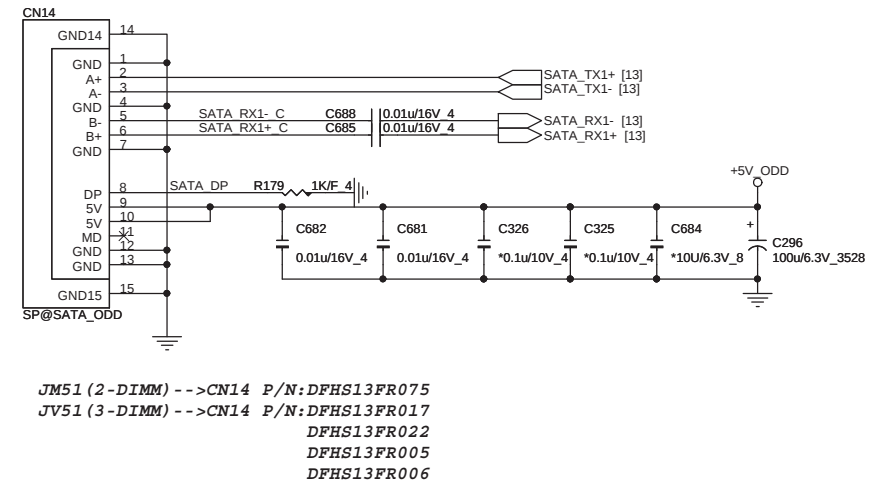
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



SATA HDD(HDD)

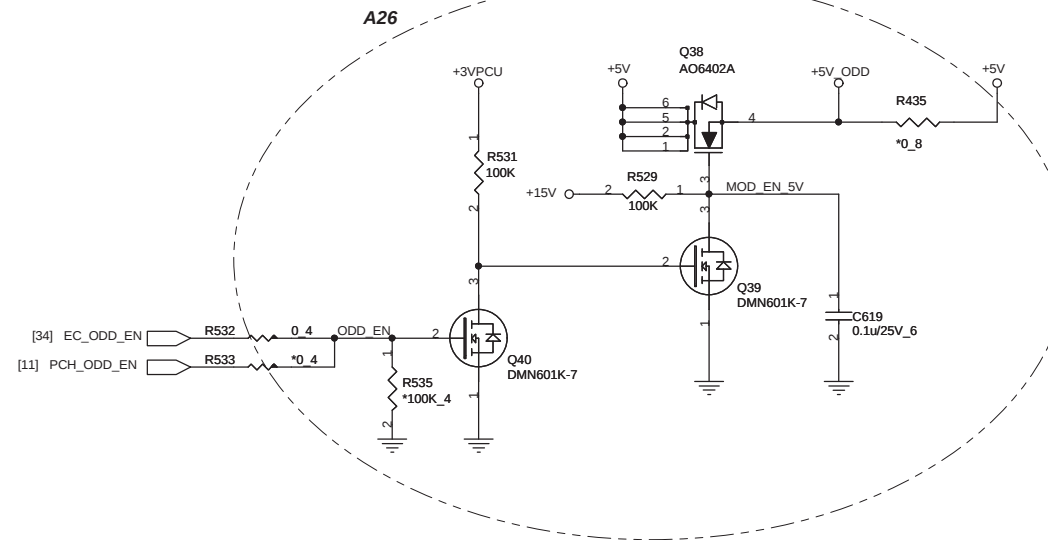


SATA ODD (ODD)



HOLE(OTH)

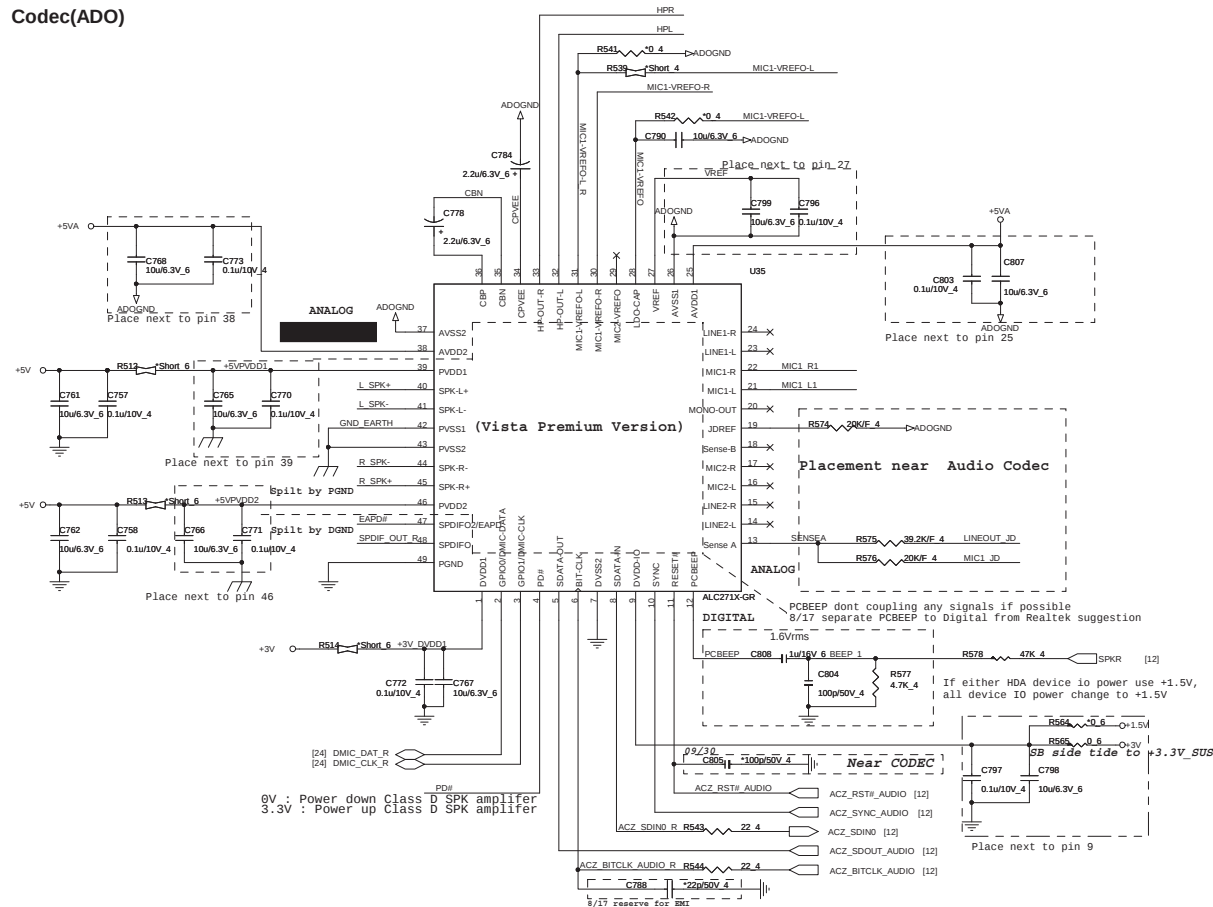
ODD POWER(ODD)



PROJECT : ZR8
Quanta Computer Inc.

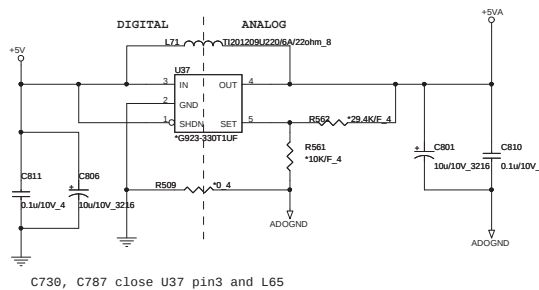
Size	Document Number	Rev
	SATA-HDD/ODD	1A
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Codec(ADO)

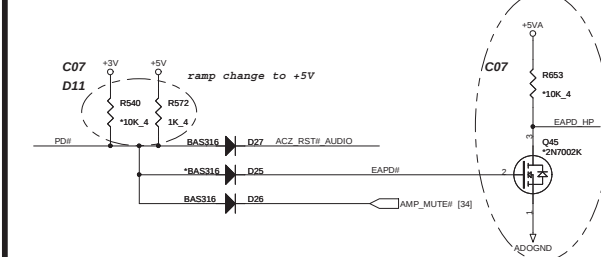


Power (ADO)

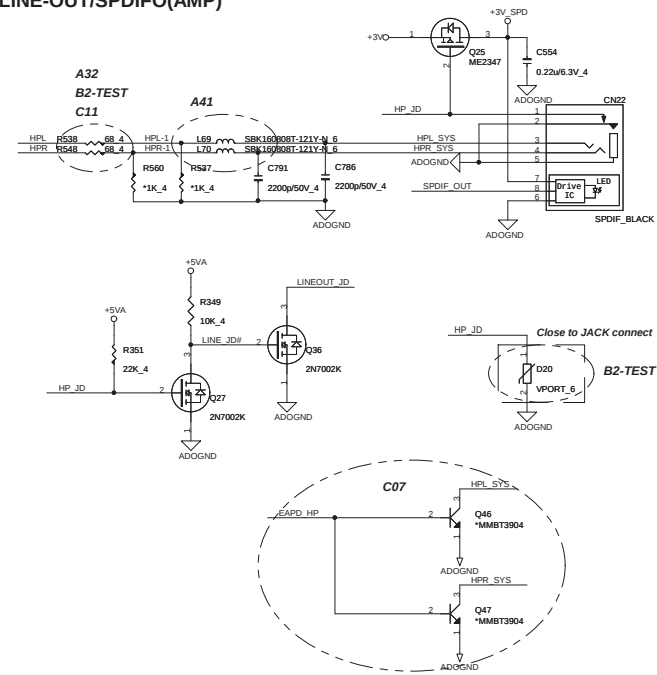
Demodulation Filter L65 Place close to Codec


$$V_{out} = V_{set} [1 + AR(1, 2) / AR(2, GND)]$$

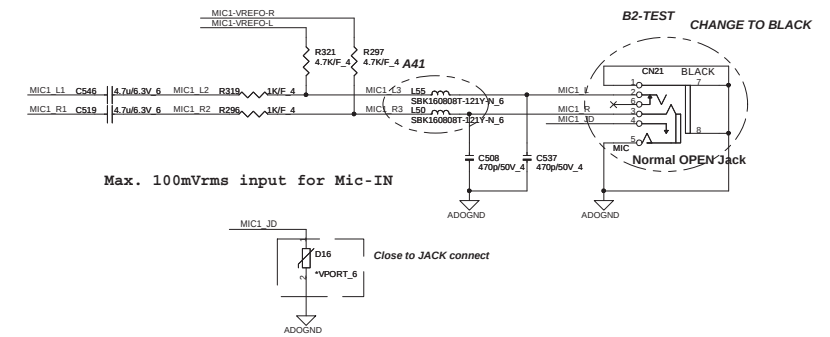
Mute(ADO)



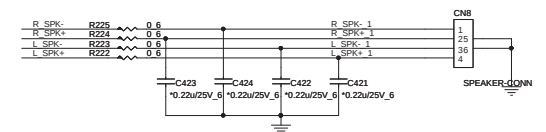
LINE-OUT/SPDIFO(AMP)



MIC(AMP)



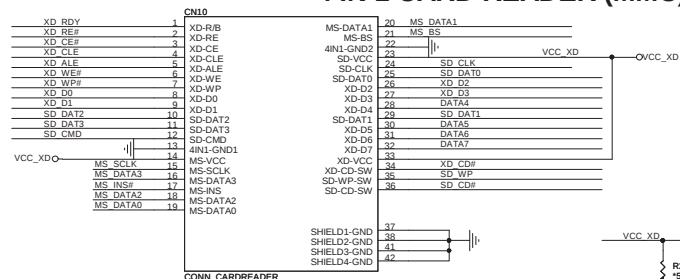
Internal Speaker(AMP)



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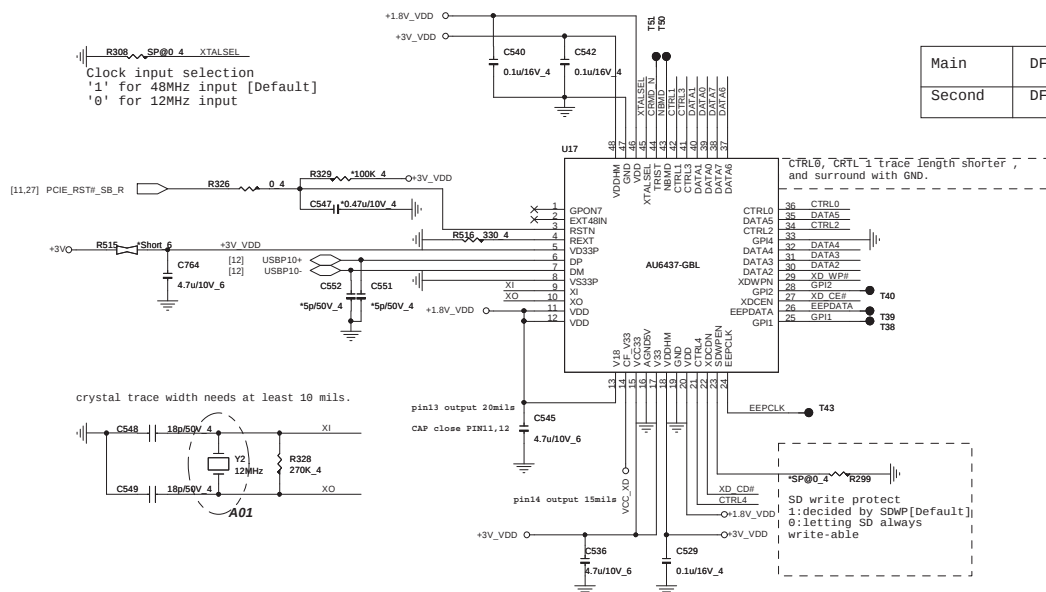
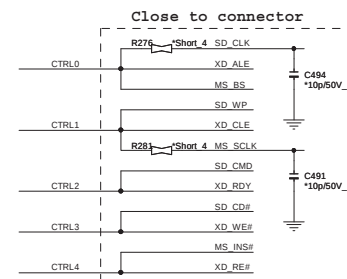
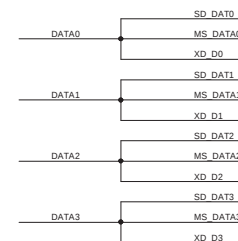
Size	Document Number ALC271X / AMP / SPK	Rev 1A
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4 IN 1 CARD READER (MMC)



Close to Connect pin 14 & pin23
4.7u CAP close to pin23

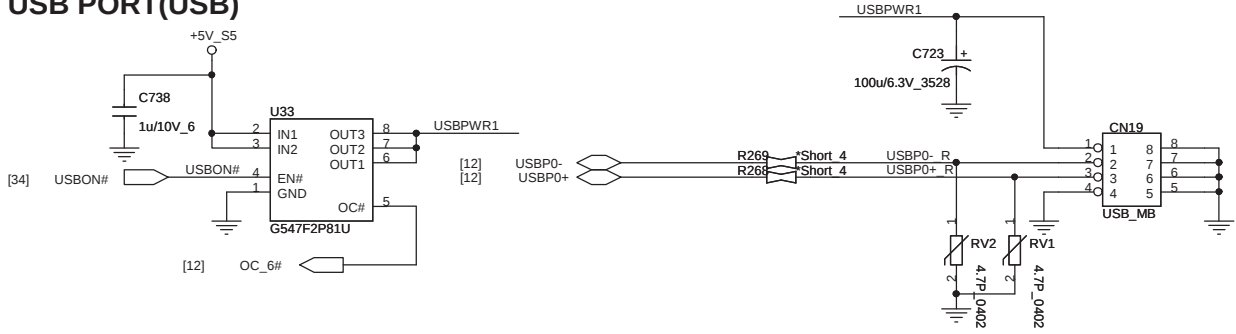
Main	DFHD36MS006
Second	DFHD36MS012



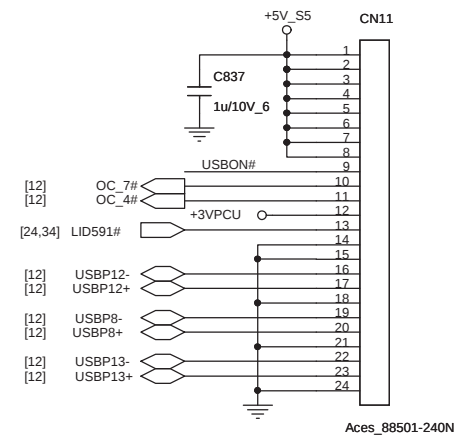
PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	AU6437 CardReader	1A
Date:	Wednesday, May 27, 2009	Sheet 30 of 49

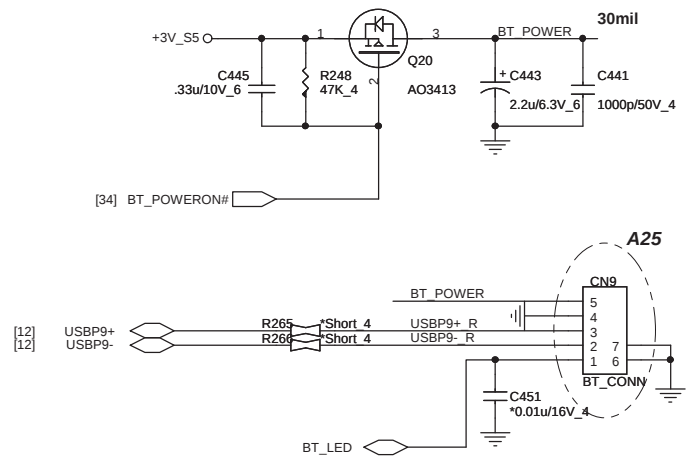
USB PORT(USB)



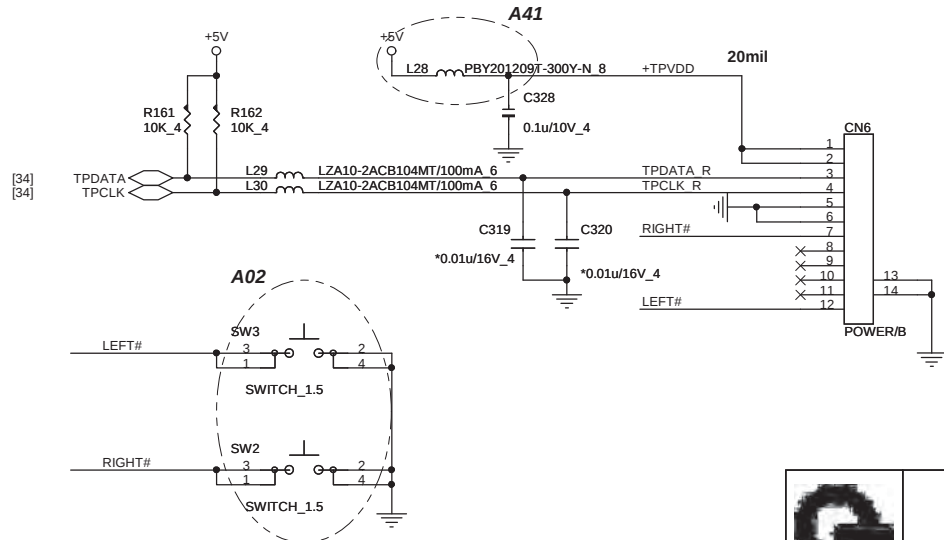
USB BOARD CONN(USB)



BLUETOOTH CONN(BTM)



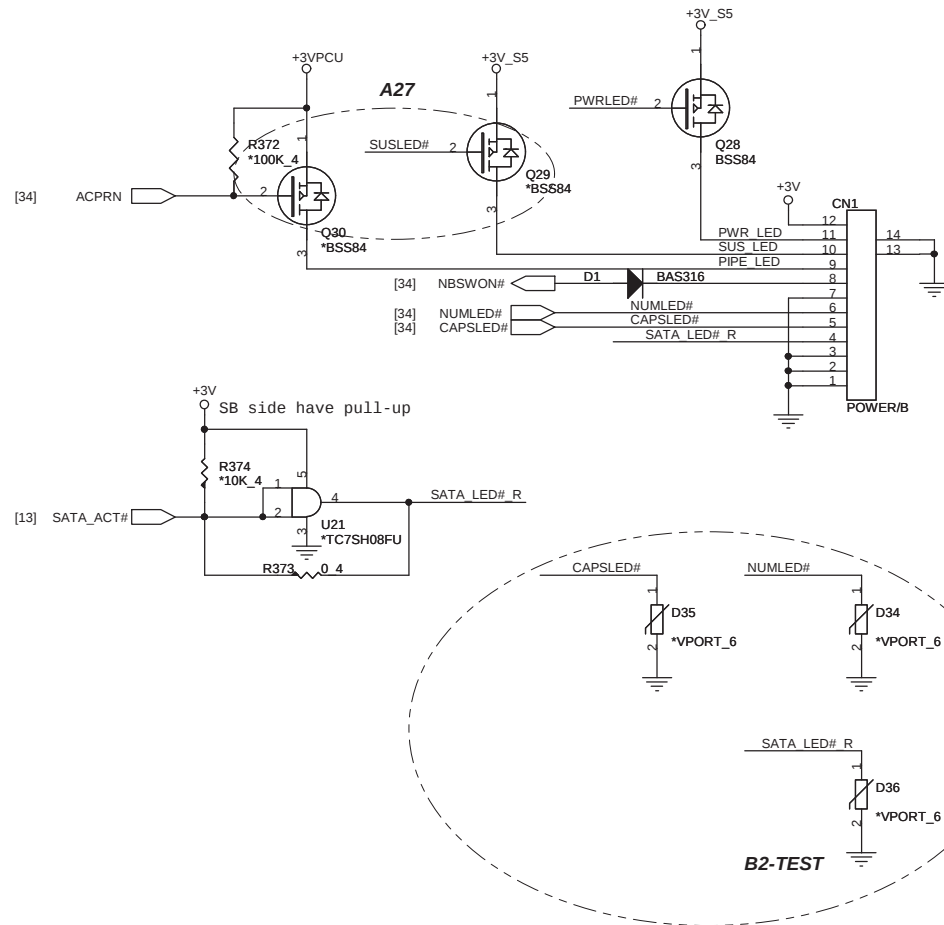
TOUCHPAD BOARD CONN(TPD)



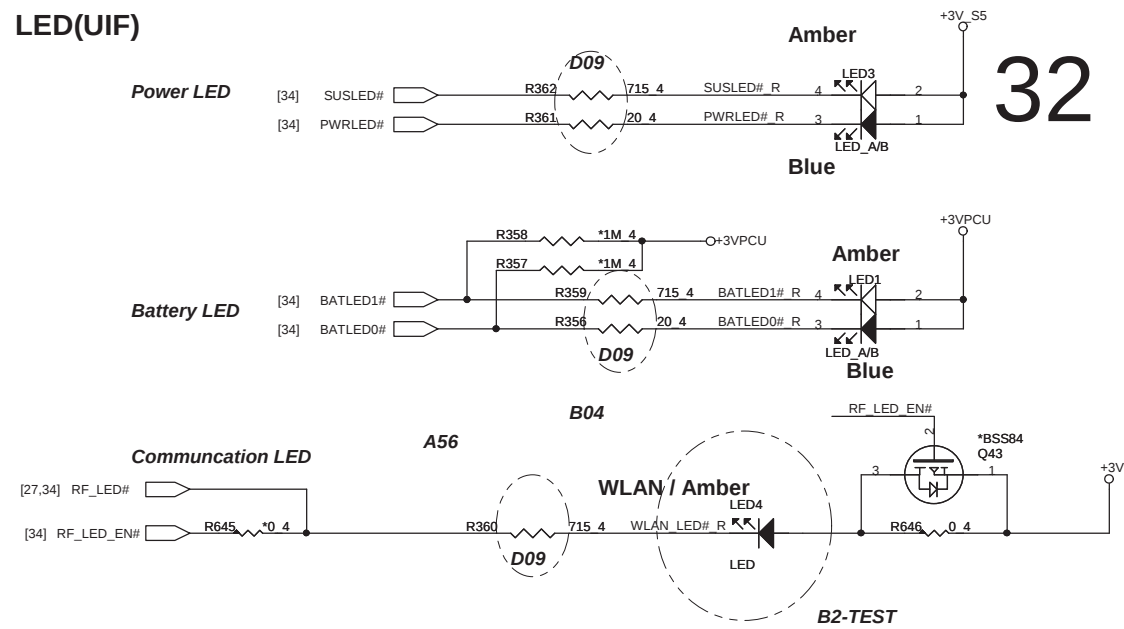
PROJECT : ZR8
Quanta Computer Inc.

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	eSATA/USB	1A
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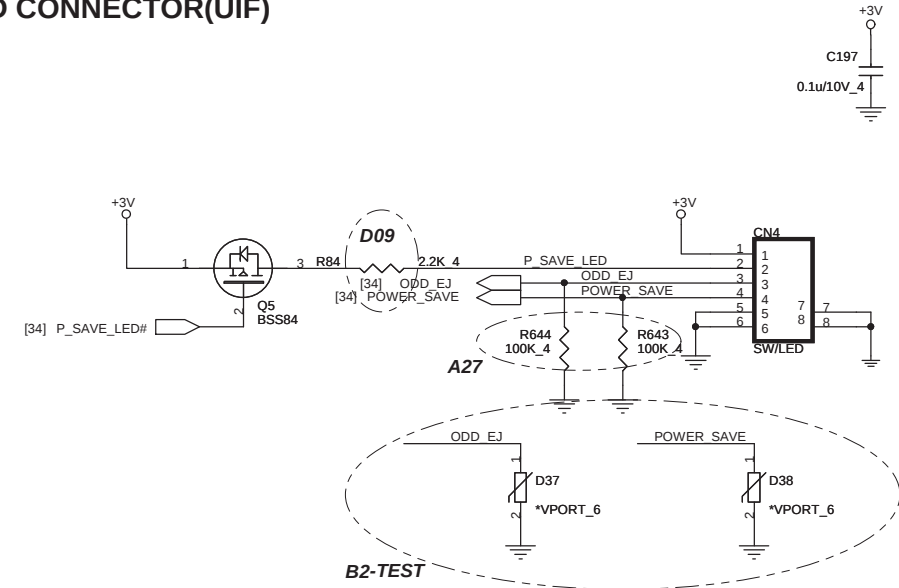
POWER BOARD CONN(UIF)



LED(UIF)



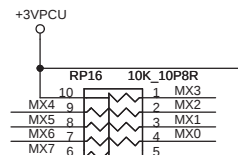
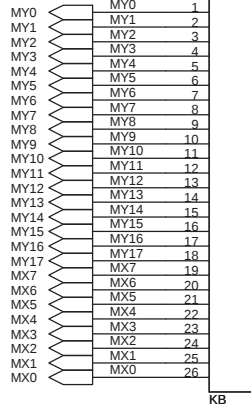
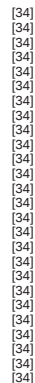
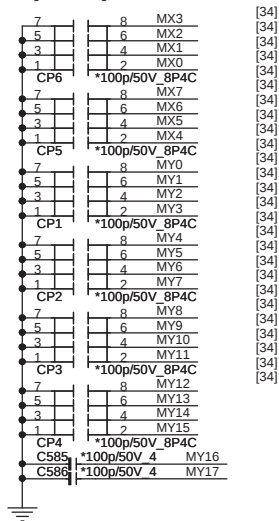
LED BOARD CONNECTOR(UIF)



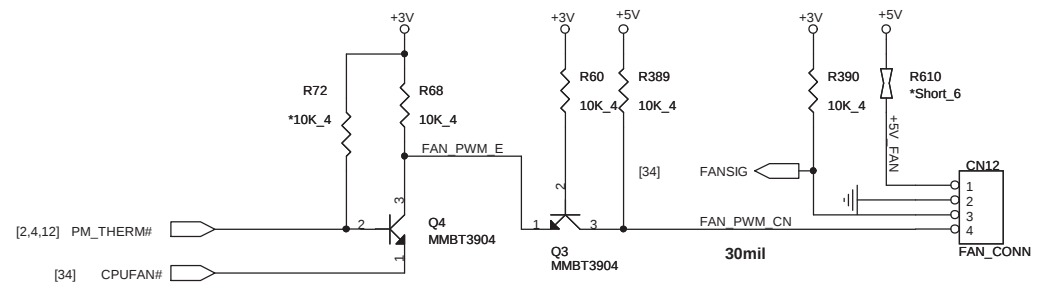
PROJECT : ZR8
Quanta Computer Inc.

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	POWER/USB/BT/TP/MDC	1A
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K/B(KBC)



CPU FAN(THM)

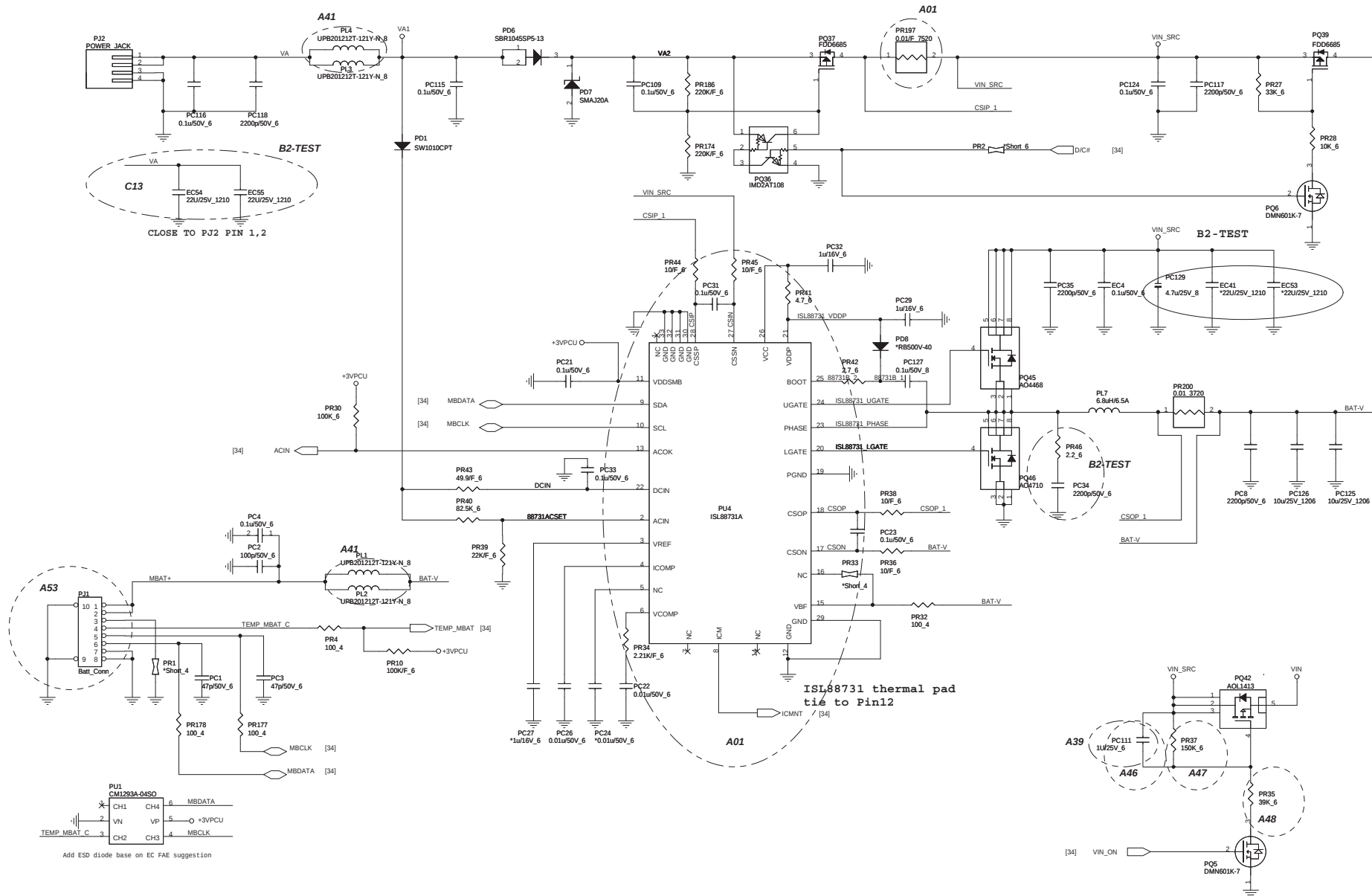


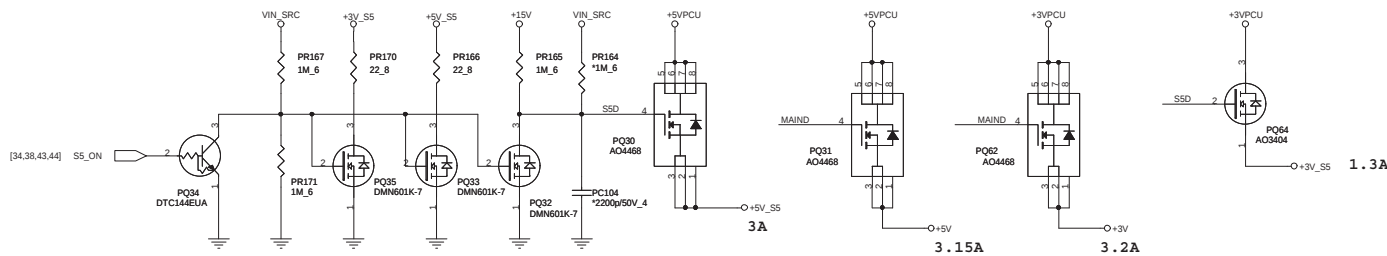
33



PROJECT : ZR8
Quanta Computer Inc.

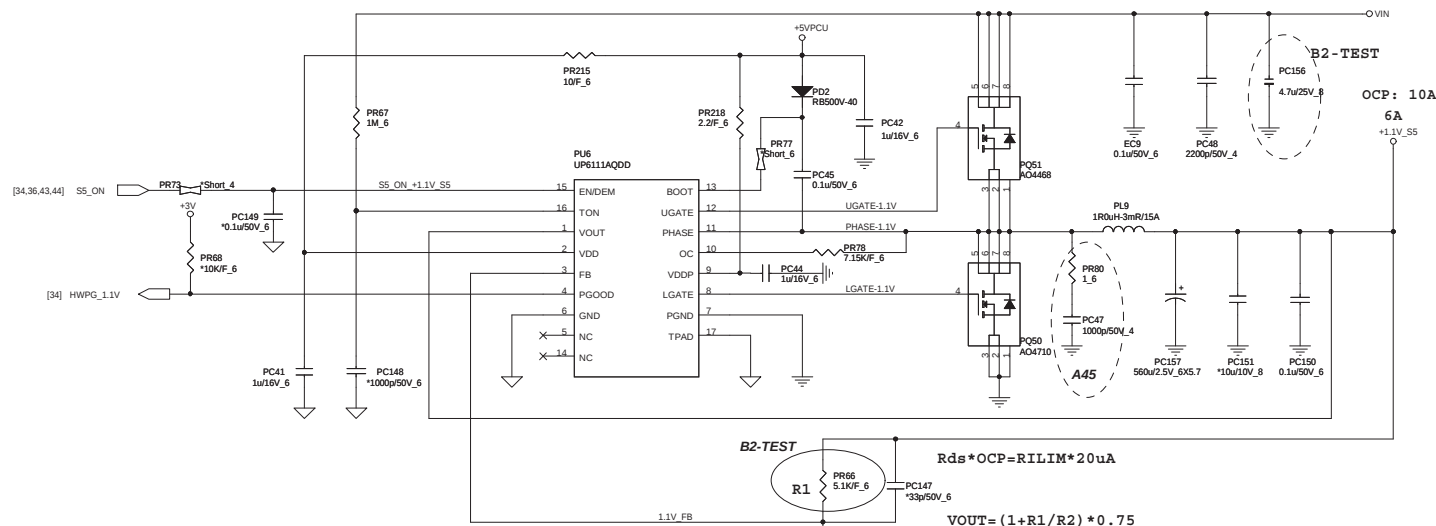
Size	Document Number			Rev
	KB/FAN/EE RETURN CAP			1A
Date:	Wednesday, May 27, 2009	Sheet	33 of	49





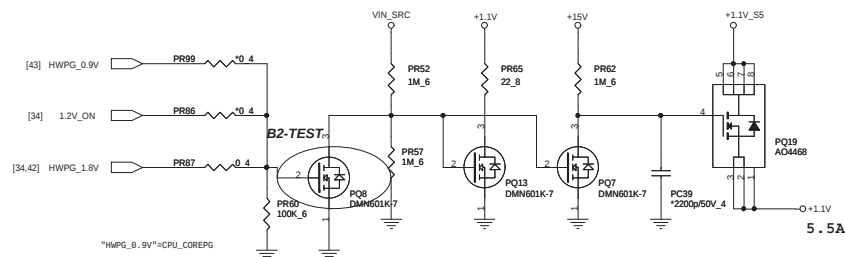
PROJECT : ZR8
Quanta Computer Inc.

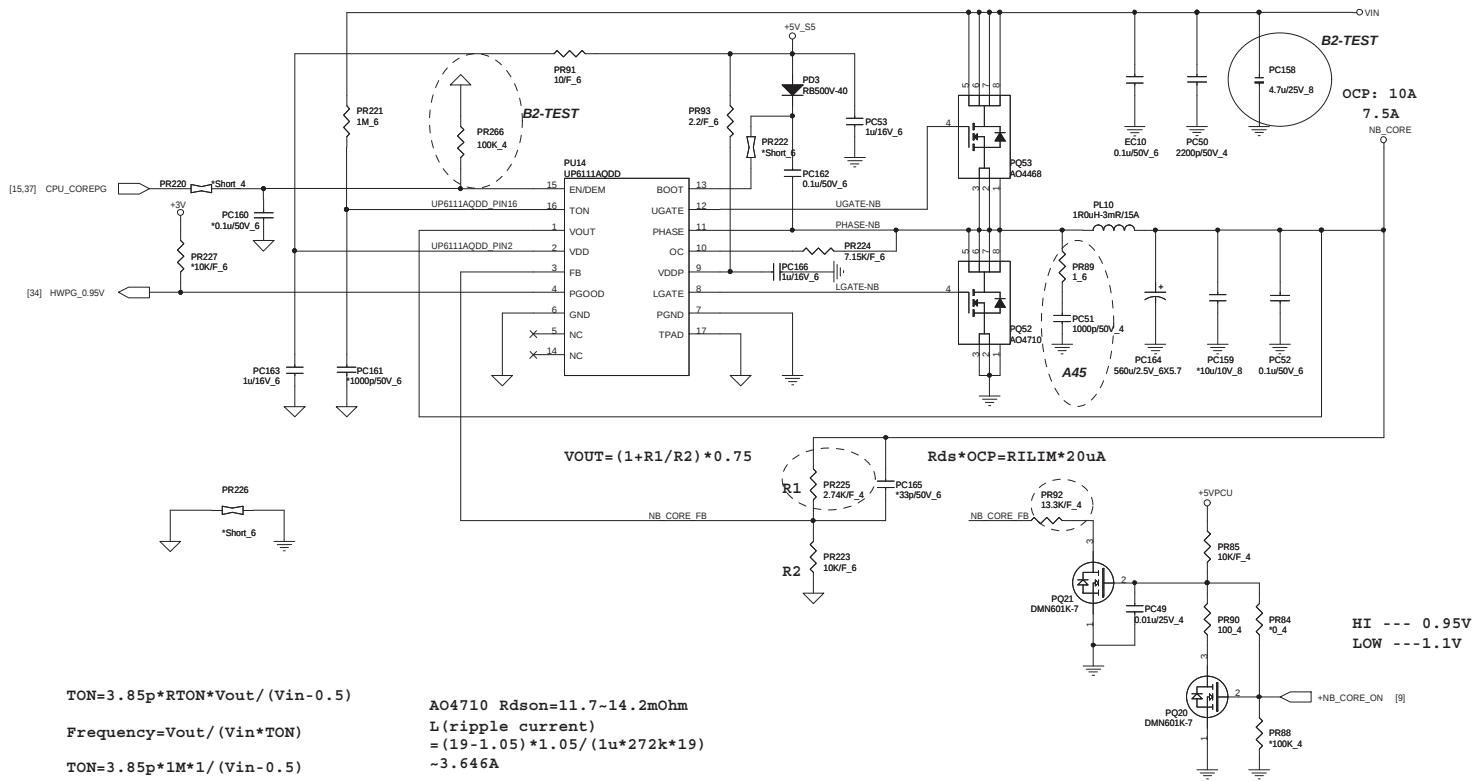
Size	Document Number		
	SYSTEM 5V/3V (RT8206)		
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$$\begin{aligned} \text{TON} &= 3.85p * \text{RTON} * \text{Vout} / (\text{Vin} - 0.5) \\ \text{Frequency} &= \text{Vout} / (\text{Vin} * \text{TON}) \\ \text{TON} &= 3.85p * 1M * 1 / (\text{Vin} - 0.5) \\ \text{Frequency} &= 1 / (0.0036767) = 272K \end{aligned}$$

$$\begin{aligned} \text{AO4710 } R_{\text{ds(on)}} &= 11.7 \sim 14.2 \text{m}\Omega \\ L(\text{ripple current}) &= (19 - 1.1) * 1.1 / (1u * 272k * 19) \\ &\sim 3.81\mu\text{H} \\ 14.2\text{m} * 10 &= \text{RILIM} * 20\mu\text{A} \\ \text{RILIM} &= 7.1K \sim 7.15K \end{aligned}$$





$$TON = 3.85p \cdot RTON \cdot Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin \cdot TON)$$

$$TON = 3.85p \cdot 1M \cdot 1 / (Vin - 0.5)$$

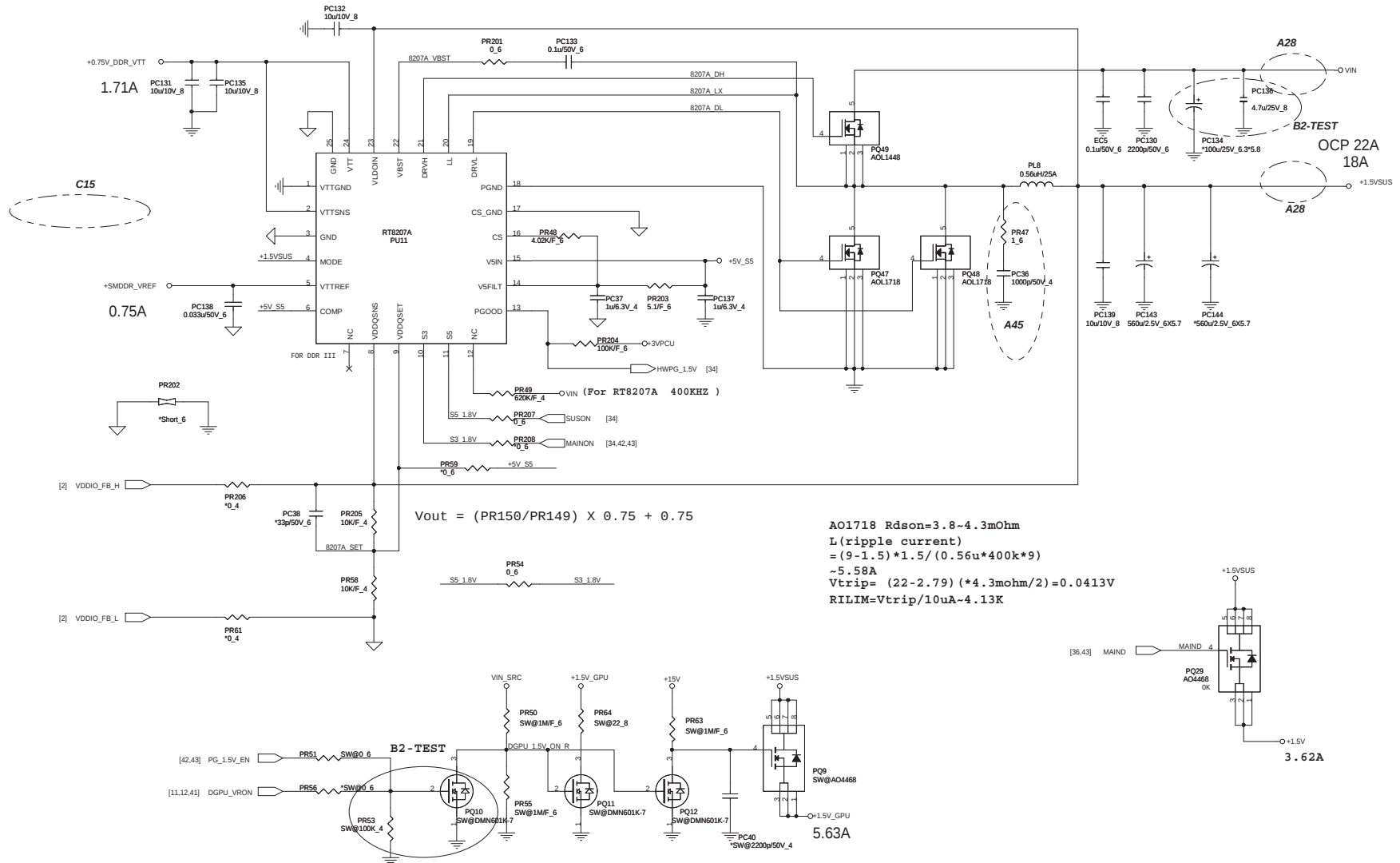
$$Frequency = 1 / (0.0036767) = 272K$$

$$AO4710 \text{ } Rdson = 11.7 \sim 14.2m\Omega$$

$$L(\text{ripple current}) = (19 - 1.05) \cdot 1.05 / (1u \cdot 272k \cdot 19) \sim 3.646A$$

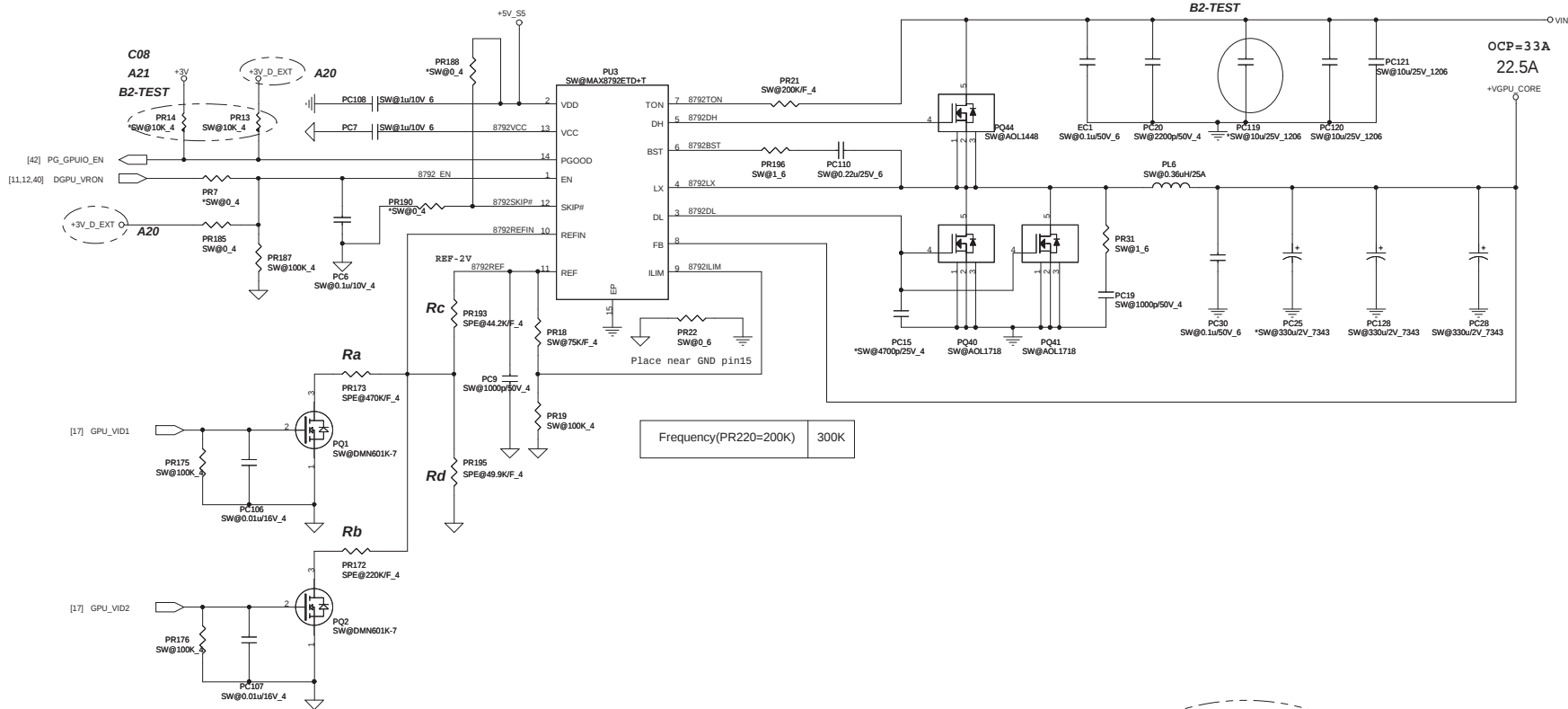
$$14.2m \cdot 10 = RILIM \cdot 20uA$$

$$RILIM = 7.1K \sim 7.15K$$



PROJECT : ZR8
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	DDR 1.5V(TPSS1116)	1A
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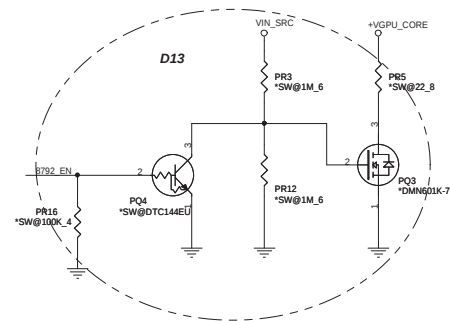


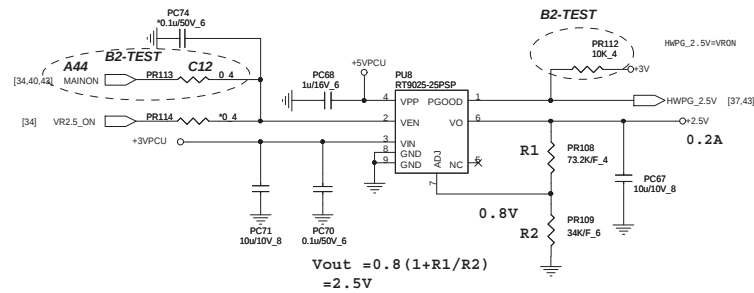
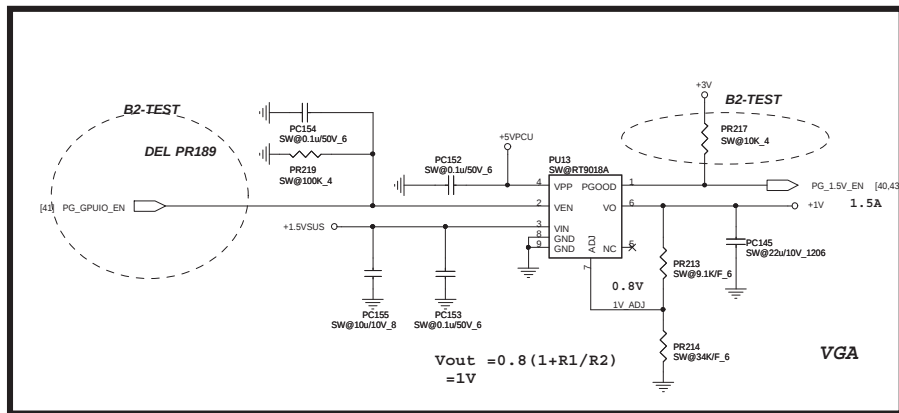
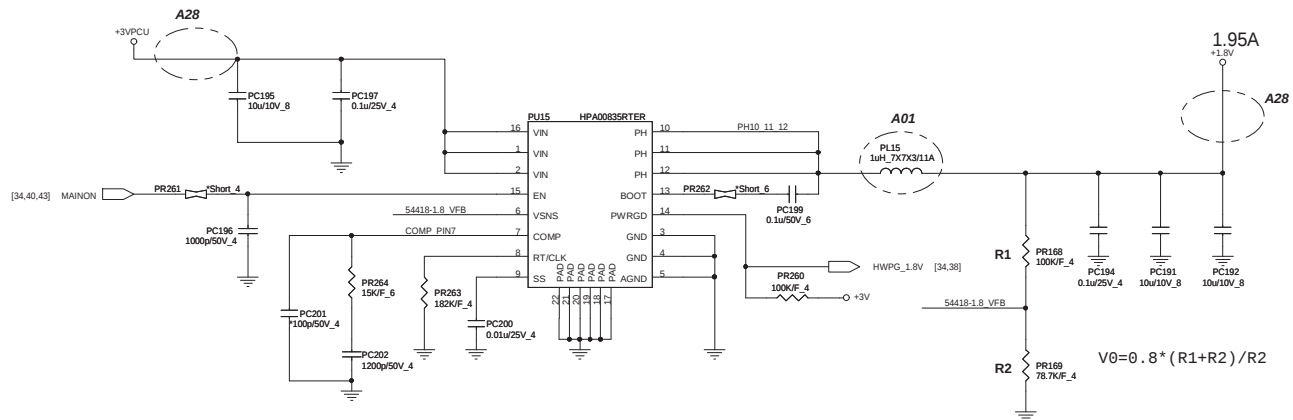
Frequency(PR220=200K) 300K

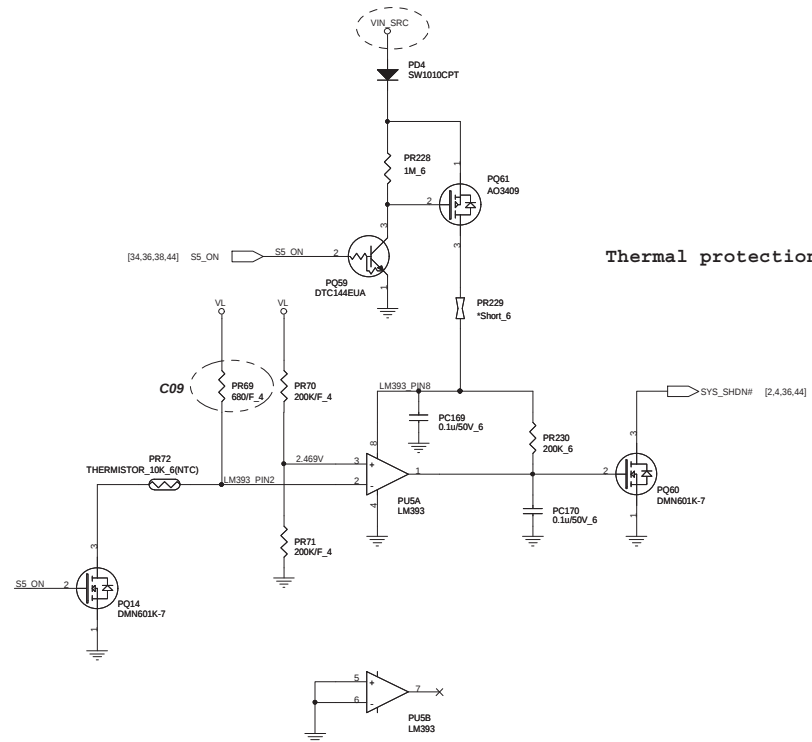
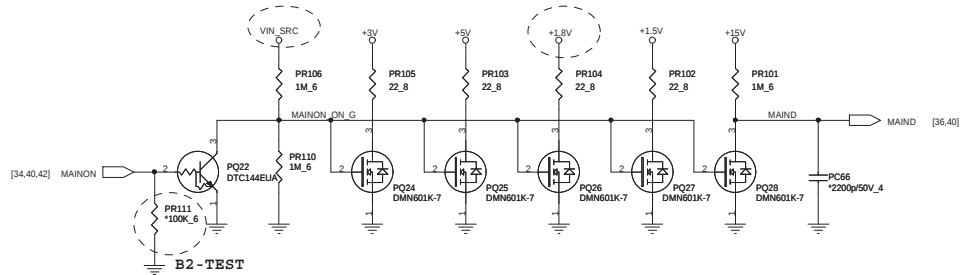
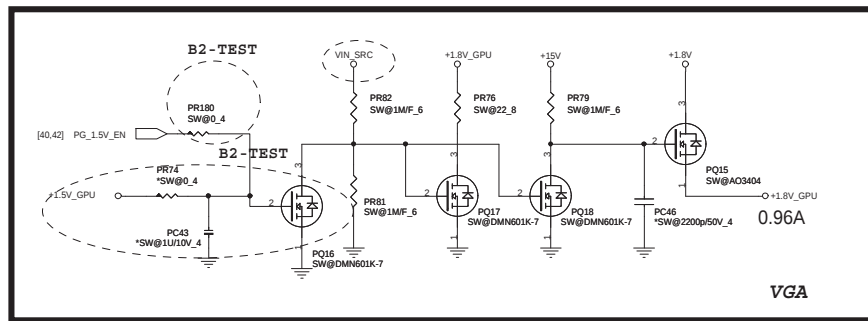
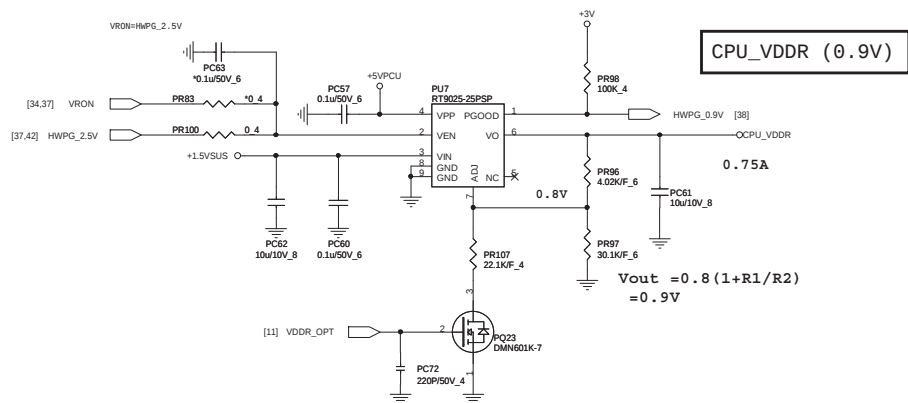
Madison-Pro		
GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
1	1	0.9V

Ra	Rb	Rc	Rd	VREF
470K	220K	44.2K	49.9K	2V

Rc --> 39.2K/F_4 (CS33922FB15)
Ra --> 332K/F_4 (CS43322FB15)
Rb --> 130K/F_4 (CS41302FB00)

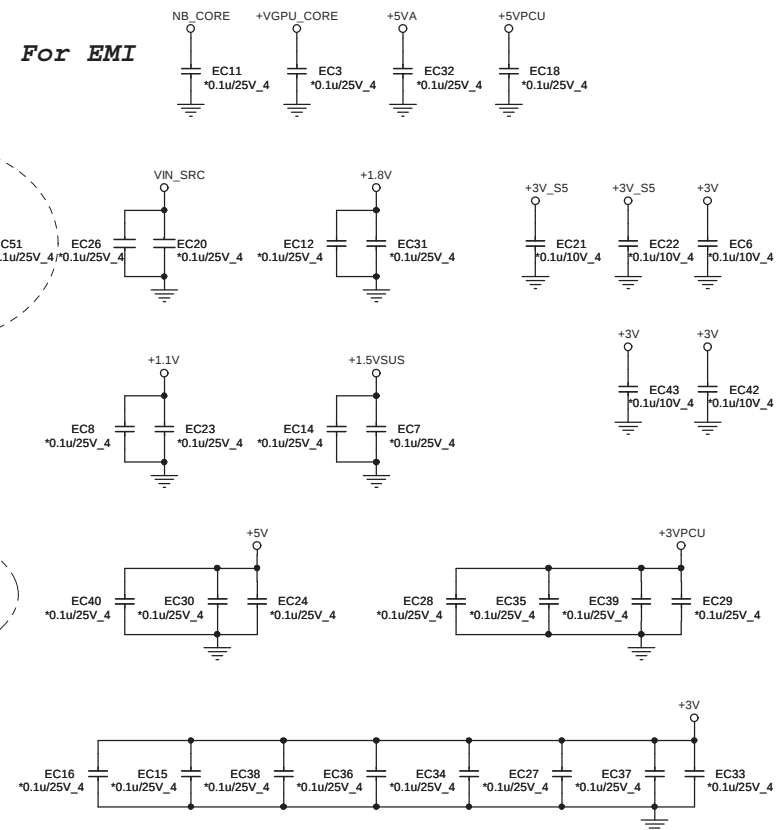
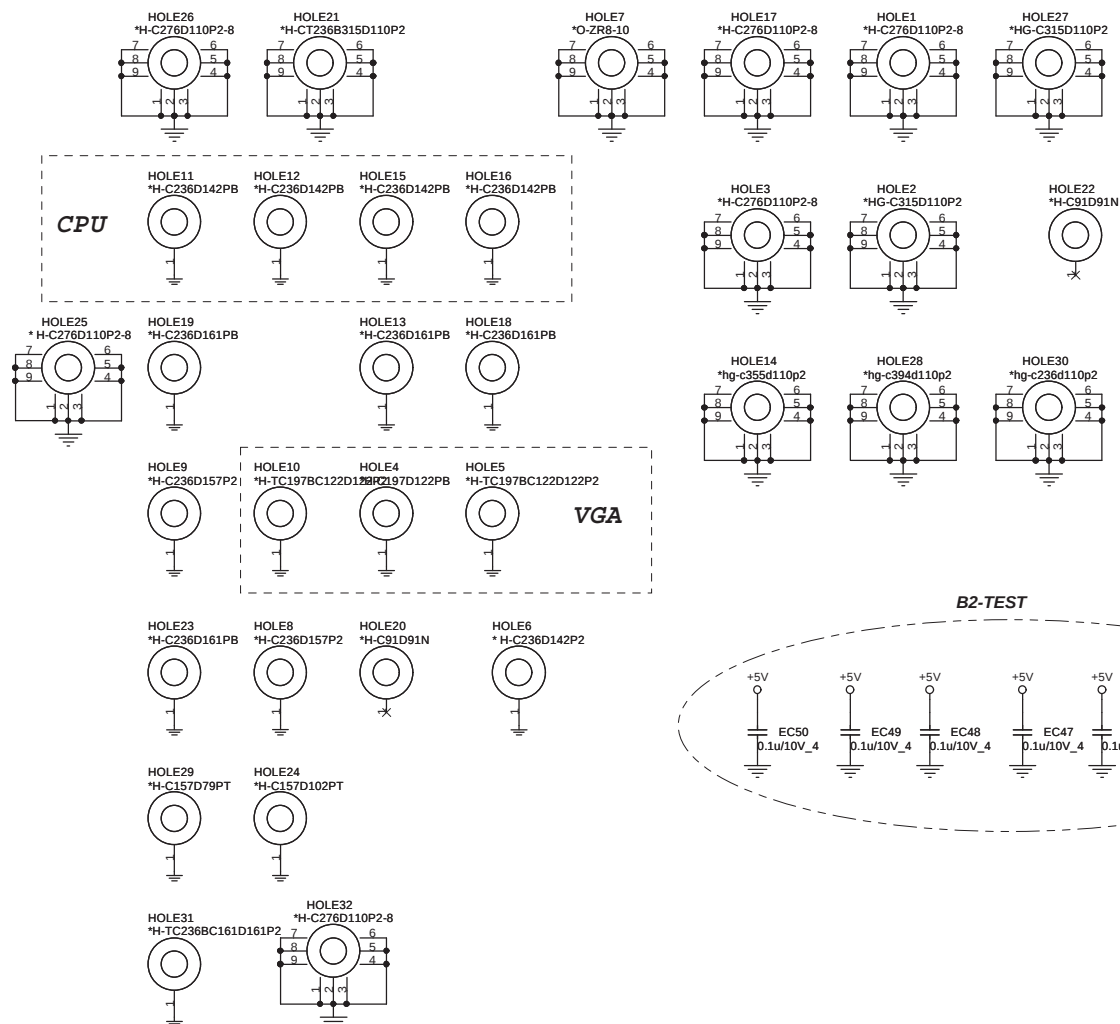




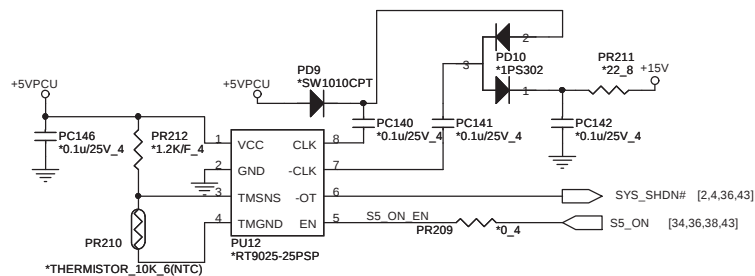


For EC control thermal protection (output 3.3V)

For EMI

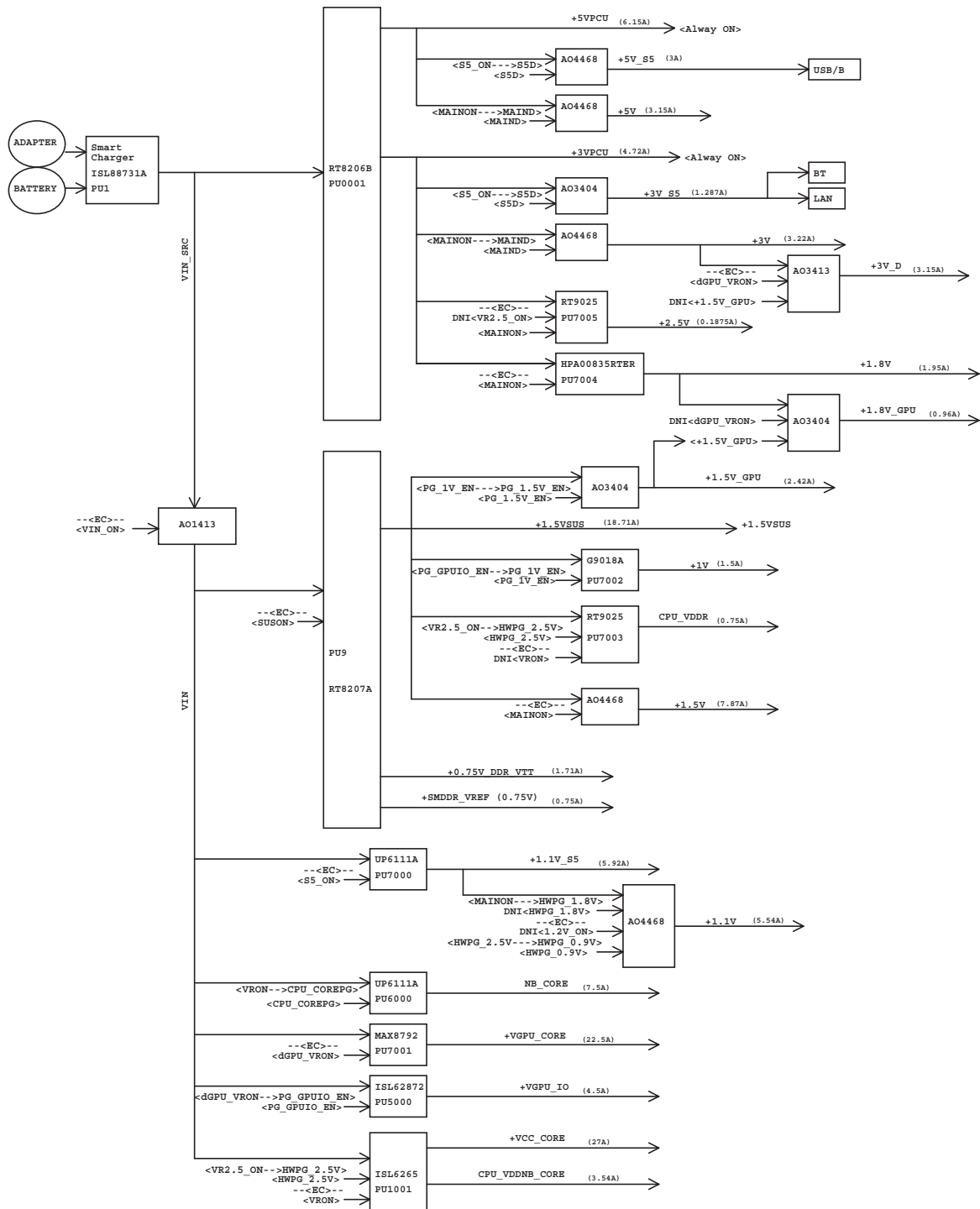


POWER TEST

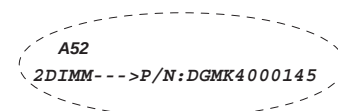


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Size	Document Number DDR3 DIMM-1(H=9.2)	Rev 1A
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A01	Page25/27/28/31/32/36/38/44	Change footprint , due to SMT open issue highlight.
A02	Page32	Change T/P switch P/N, due to SMT open issue highlight.
A03	Page42	Modify Madison-Pro & Park-XT VID table.
A04	Page14	Modify board ID table and R517,R304 support Side-port function.
A05	Page14	Add R528 support different Side-port VRAM type.
A06	Page44	Support CPU 45W solution.
A07	Page02	Change clock gen to no stuff, due to use internal clock source.
A08	Page06/07/48	Change SO-DIMM SMBUS address.
A09	Page08/10/11	Add Side-port function.
A10	Page10	Chane HDMI DDC CLK/DATA port.
A11	Page10	Stuff R190.
A12	Page12	Change dGPU_PWROK from GPIO1 to GPIO32.
A13	Page12	Change board ID GPIO pin.
A14	Page13	1. Stuff D19,R307,C538 and no stuff D18. 2. Change pull high power rail from +3V_D to +3V.
A15	Page16	Change R500 from 0ohm to 10k.
A16	Page12	Connect 25Mhz for GPU workaround design.
A17	Page18	Modify GPU Power-on sequence table.
A18	Page18	Remove GPU_IO VID contron pin and change GPU_CORE GPIO pin to GPIO15/20.
A19	Page19	Change R107 from 680ohm to 51 ohm and modify design of MEM_RST#. Also change R30 to no stuff.
A20	Page20/22/35/42	Reserve +3V_D_ZR8 power rail for GPU leakage issue.
A21	Page18	Reserve VGA_REQ# pin.
A22	Page25	Delete brightness switch IC control and change to 0ohm solution.
A23	Page25	Stuff R135,R144 ,due to some CRT monitor can't display.
A24	Page25	Stuff C776,C787 for EMI request.
A25	Page25/32	Change connect footprint and P/N.
A26	Page29/35	Add ODD power switch design and stuff R170.
A27	Page33	Change Q29,Q30 to no stuff.
A28	Page37/41/44	Remove jmuper.
A29	Page37	Change PC193 P/N to low highlimit, due to ME thermal door impact.
A30	Page38	Change PC179,PC180 from 22uF/25V to 100uF/25V.
A31	Page38	Change CPU_CORE enable from VRON to HWPG_2.5V.
A32	Page30	Change R538,R548 from 48ohm to 68ohm for audio performance.
A33	Page28	Change R572,R563 to short pad for debug use.
A34	Page20	Change +VGPU_IO power rail to +VGPU_CORE.
A35	Page25	Connect CN5 LCD connect shielding pin to GND for ESD issue.
A36	Page18	Change R65 to no stuff.
A37	Page22	Reserve OVERT# pull high resistor prevent noise.
A38	Page33	Add pull low 100k ohm for ODD_EJ,POWER_SAVE signal.
A39	Page36	Reserve cap for power team request.
A40	Page30	Stuff 0 ohm resistor for ESD protect use.
A41	Page02/03/10/11/15/18/20/21/27/30/32/35/36	Change bead P/N for EMI request, the reason is cost down and not STD parts.
A42	Page21	Reserve 0 ohm for PLL power use.
A43	Page38	Remove PR153 & change to 0402 package
A44	Page44	Change PR113 from 0 to 10K Ohm & Change enable source to +3V
A45	Page38/39/40/41	Stuff PR80,PR89,PR94,PR95,PR47 to 1 Ohm & PC47,PC51,PC64,PC65,PC36 of value to 1000p for EMI request
A46	Page36	Change PC111 of value to 1U/25V
A47	Page36	Change PR37 of value, from 33K to 150K
A48	Page36	Change PR35 of value, from 10K to 39K
A49	Page26	Change HDMI connector PN
A50	Page7	Change P/N for 3-DIMM H=4.0 STD
A51	Page6	Change P/N for 3-DIMM H=4.0 RVS
A52	Page48	Change P/N for 3-DIMM H=8.0 RVS
A53	Page36	Change battery connector P/N to DFHD08MR099
A54	Page26	Modify HDMI's I2C for DIS.



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ZR8 Schematic EC Tracking Record A (For A TEST) Nov.17 , 2009
EC / Page / Item / Description

- A55 Page14 Change board ID power rail from +3V_S5 to +3V.
- A56 Page33/35 Modify WLAN RF_LED control design.
- A57
- A58 Page12 Remove R331 only for A11 version.
- A59 Page12 Add U18,C533 & remove R303 for power sequence.
- A60 Page14 Remove C760,C754,R507& Y7, due to it's for external clock use.
- A61 Page2 Stuff R474,R486 for LAN & WLAN of REQ#.
- A62 Page3/12 Stuff R424 and no stuff R286, due to CPU_PRPCHOT# is +1.5VSUS level.
- A63 Page16 Change D29 package & Add D24.

Note : Change 0ohm to short pad
R276,R281,R415,R443,R445,R531,R532,R533,R534,R535,R539,R566,R174,R512,R513,R263,R437,R439,R441,R99

ZR8 Schematic EC Tracking Record B1 (For B1 TEST) Dec.09 , 2009
EC / Page / Item / Description

- B01 Page21 Remove DP/TMDS Output Driver Analog Supply from port C&D. Due to it's don't to use.
- B02 Page25 Stuff R48 for Discrete platform use.
- B03 Page/10/25 Modify R signal pull low resistor value to 140ohm, due to keep 70 ohm trace impedance.
- B04 Page33 Modify WLAN LED design and change from GPIO82 to GPIO84.
- B05 Page27 Change LAN layout footprint for "SAW" new package.
- B06 Page13/25 Reserve CCD USB host from for Port2, due to CCD issue.
- B07 Page33 Reserve blue LED power source to 5V, due to White/Blue LED max Vf is more than Green/Orange LED.

ZR8 Schematic EC Tracking Record C (For C TEST) Jan.28 , 2010
EC / Page / Item / Description

- C01 Page02/34 Remove "CPU_THERMTRIP#" control from SB820, due to BIOS don't support this function. Add another "SYS_SHDN#" for H/W shutdown function and add HWPG shutdown design.
- C02 Page04 No stuff Q21,D14,R255 for thermal sensor Alert frnction and change to EC or H/W shutdown function.
- C03 Page09 Add 1uF for monitor test noise issue.
- C04 Page12 Add 0ohm to separate VGA_REQ function, due to it's don't support the function and cause by leakage current concern.
- C05 Page24 Modify VGA note text for R signal impedance control.
- C06 Page24 Add brightness switch control by iGPU switch mode. Due to BIOS for C test already support.
- C07 Page29 Reserve EAPD# audio design for "Bo" sound.
- C08 Page41 Change PG_GPUIO_EN pull high power rail from +3V to +3V_D_EXT. For Park GPU SG mode hang up issue.
- C09 Page43 Change PR69 FROM 1.2K to 680ohm , the reason is for SDA high temperature (40 degree/20% humidity) auto shutdown issue.
- C10 Page27 Short LPC signal for debug card use.
- C11 Page29 Change R538,R548 from 56ohm to 68ohm for audio performance test FSOV spec requirement.
- C12 Page42 Change PR113 from 10k to 0ohm.
- C13 Page35 Change EC54,EC55 to stuff for ISN issue.
- C14 Page21 Modify DDR3 Memory Aperture size table.
- C15 Page03/40 Reserve VDDR_SENSE signal to controller IC.
- C16 Page27 Change RP32 to no stuff.
- C17 Page04 Modify CPU thermal control design from EC or BIOS control and change U16,R254 to no stuff ,Q17,Q18,Q19 to stuff.
- C18 Page03 No stuff R189.

Note : Change 0ohm to short pad
R124,R121,R174,L31,L37,L35,R136,R115,R169,R325,R315,R295,R292,R278,R31,R90,R21,R112,R24,R25,R270,R530,R99,R478,R512,R513,R514,R326,R269,R268,R265,R266,R610,PR73,PR220,PR261,PR229



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ZR8 Schematic EC Tracking Record A (For Ramp) Feb.25 , 2010
EC / Page / Item / Description

- D01 Page03 Change CPU VDDR_SENSE pull high power rail to CPU_VDDR and remove trace connect to controller IC.
- D02 Page15 Modify text note.
- D03 Page12 Change "GBE_COL" ,"GBE_CRS" ,"GBE_RXERR" to GND follow SCL V1.04 version.
- D04 Page14 Change USB PLL power rail source to separate VDDPL_33_USB_S follow SCL V1.04 version.
- D05 Page04 No stuff R267,C450,C344.
- D06 Page09 Delete R149,R152 layout pad.
- D07 Page36 No stuff PD12 and add PR181, change PR257 from 1k to 390k. The purpose is for panasonic battery low power protect issue.
- D08 Page05/46 No stuff R584,R259,R583,R586 for CKE signal.
- D09 Page32 Change LED current sense resistor value for LED light measure requirement. (Follow ZR7B)
- D10 Page21 Modify VRAM table.
- D11 Page05/06 Change R123,R122,Q10,R202,R195,Q14 to no stuff, due to S1g4 don't support MEMHOT function.
- D12 Page02 Reserve prochot# for FAN control.
- D13 Page41 No stuff PR16,PQ4,PR3,PR12,PR5,PQ3. Due to MAX8792 had integrate discharge design.
- D14 Page37 Change some component to no stuff, dut to for S1g4 use the same VDD power don't need to compensation difference voltage.

Note : Change 0ohm to hort pad.
R203,117,R585,R588,R260,R587,PR1,PR2,PR33,PR241,PR147,PR146,PR160,PR256,PR133,PR233,PR152,PR155,PR128,PR142,PR143,PR144,PR145,PR130,PR131,PR115,PR120,PR77,PR226,PR222,PR202,PR262.