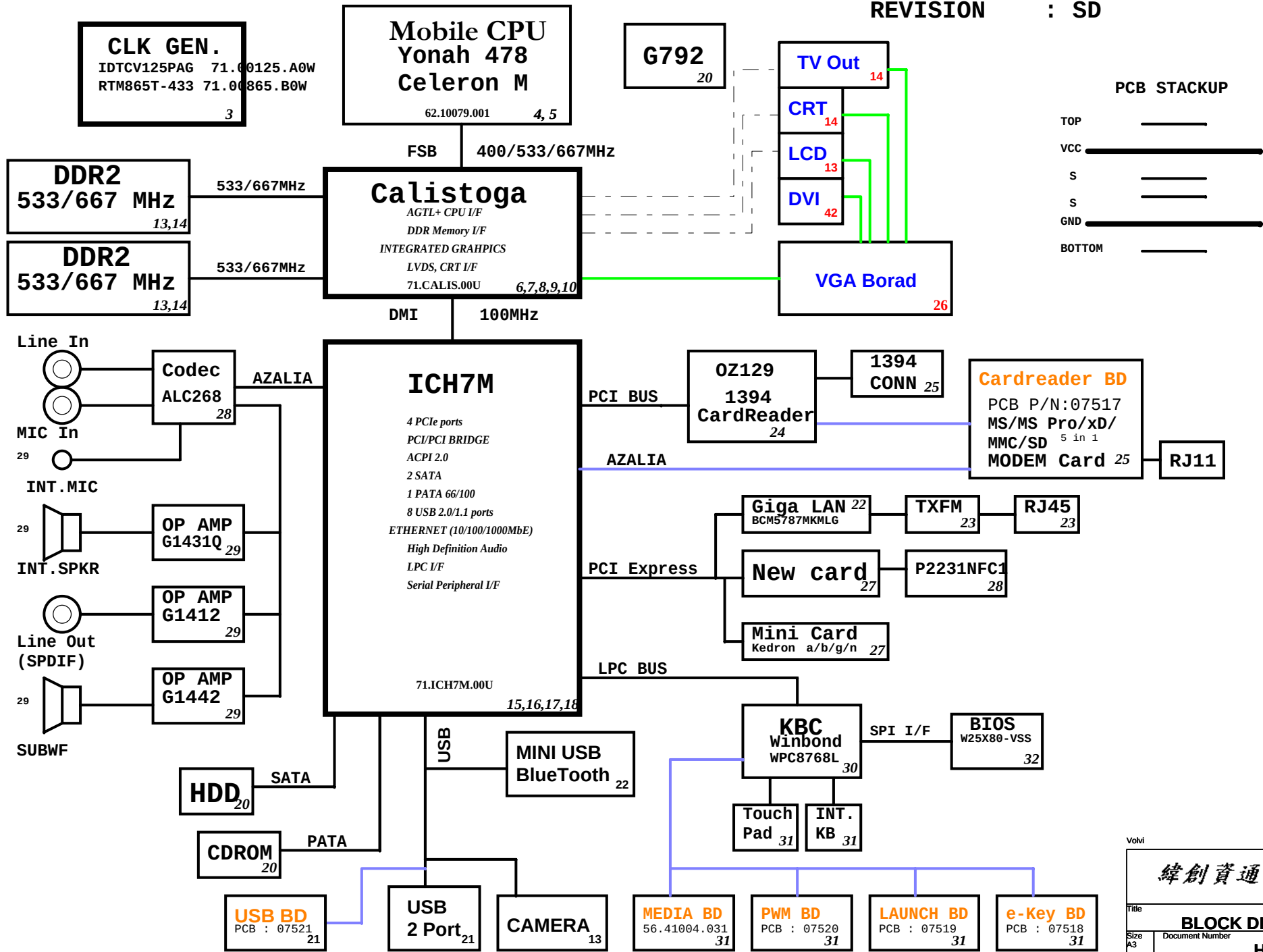


# Huron Block Diagram



Project code: 91.4V301.001  
PCB P/N : 07205  
REVISION : SD

| SYSTEM DC/DC<br>TPS51120 37    |                                      |
|--------------------------------|--------------------------------------|
| INPUTS                         | OUTPUTS                              |
| DCBATOUT                       | 5V_S5<br>3V_S5                       |
| SYSTEM DC/DC<br>TPS51124 38    |                                      |
| INPUTS                         | OUTPUTS                              |
| DCBATOUT                       | 1D8V_S3<br>1D05V_S0                  |
| TPS51100 40                    |                                      |
| 1D8V_S3                        | DDR_VREF                             |
| APL5308 40                     |                                      |
| 3D3V_S0                        | 2D5V_S0                              |
| APL5912 39                     |                                      |
| 1D8V_S3                        | 1D5V_S0                              |
| Intersil CHARGER<br>MAX8731 41 |                                      |
| INPUTS                         | OUTPUTS                              |
| DCBATOUT                       | BT+<br>18V 4.0A<br>UP+5V<br>5V 100mA |
| CPU DC/DC<br>ISL6262 35        |                                      |
| INPUTS                         | OUTPUTS                              |
| DCBATOUT                       | VCC_CORE<br>0~1.3V<br>48A            |

ICH7M Integrated Pull-up and Pull-down Resistors

|                                                                                                                                                                      |                                |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| EE_DIN,EE_DOUT, GNT[3:0], GPIO[25],<br>GNT[4]#/GPIO48, GNT[5]#/GP017, PME#,<br>LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0]<br><br>LDRQ[0], LDRQ[1]/GPIO[41],<br>PWRBTN#, TP[3] | ICH7 internal 20K pull-ups     |
| DD[7], DDREQ                                                                                                                                                         | ICH7 internal 11.5K pull-downs |
| ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0],<br>ACZ_SDOUT,ACZ_SYNC, DPRSLPVR/GPIO16,<br>EE_CS,SPI_ARB, SPI_CLK, SPKR,                                                       | ICH7 internal 20K pull-downs   |
| USB[7:0][P,N]                                                                                                                                                        | ICH7 internal 15K pull-downs   |
| SATALED#                                                                                                                                                             | ICH7 internal 15K pull-up      |
| LAN_CLK                                                                                                                                                              | ICH7 internal 100K pull-down   |

ICH7M IDE Integrated Series Termination Resistors

|                                                                                  |                      |
|----------------------------------------------------------------------------------|----------------------|
| DD[15:0], DIOW#, DIOR#, DREQ,<br>DDACK#, IORDY, DA[2:0], DCS1#,<br>DCS3#, IDEIRQ | approximately 33 ohm |
|----------------------------------------------------------------------------------|----------------------|

ICH7M Functional Strap Definitions

| Signal                                 | Usage/When Sampled                                                    | Comment                                                                                                                                                                                                          |
|----------------------------------------|-----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ACZ_SDOUT                              | XOR Chain Entrance/<br>PCIE Port Config bit1,<br>Rising Edge of PWROK | Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)                                                      |
| ACZ_SYNC                               | PCIE bit0,<br>Rising Edge of PWROK.                                   | Sets bit0 of RPC.PC(Config Registers:Offset 224h)                                                                                                                                                                |
| EE_CS                                  | Reserved                                                              | This signal should not be pull high.                                                                                                                                                                             |
| EE_DOUT                                | Reserved                                                              | This signal should not be pull low.                                                                                                                                                                              |
| GNT2#                                  | Reserved                                                              | This signal should not be pull low.                                                                                                                                                                              |
| GNT3#                                  | Top-Block<br>Swap Override.<br>Rising Edge of PWROK.                  | Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space).<br>Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down. |
| GNT5#/<br>GPIO17#,<br>GNT4#/<br>GPIO48 | Boot BIOS Destination<br>Selection.<br>Rising Edge of PWROK.          | Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10).<br>GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.                                                                                   |
| DPRSLPVR                               | Reserved                                                              | This signal should not be pull high.                                                                                                                                                                             |
| GPIO25                                 | Reserved.<br>Rising Edge of RSMRST#.                                  | This signal should not be pull low.                                                                                                                                                                              |
| INTVRMEN                               | Integrated VccSusi_05<br>VRM Enable/Disable.<br>Always sampled.       | Enables integrated VccSusi_05 VRM when sampled high                                                                                                                                                              |
| LINKALERT#                             | Reserved                                                              | Requires an external pull-up resistor.                                                                                                                                                                           |
| REQ[4:1]#                              | XOR Chain Selection.<br>Rising Edge of PWROK.                         | TBD, Chapter 8.                                                                                                                                                                                                  |
| SATALED#                               | Reserved                                                              | This signal should not be pull low.                                                                                                                                                                              |
| SPKR                                   | No Reboot.<br>Rising Edge of PWROK.                                   | If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.                                            |
| TP3                                    | XOR Chain Entrance.<br>Rising Edge of PWROK.                          | This signal should not be pull low unless using XOR Chain testing.                                                                                                                                               |

RTM865T-433 100Mhz/LCDCLK Spread and Frequency Selection Table

| SS3<br>Byte9<br>bit 7 | SS2<br>bit6 | SS1<br>bit5 | SS0<br>bit4 | Spread Amount% |
|-----------------------|-------------|-------------|-------------|----------------|
| 0                     | 0           | 0           | 0           | 0.8% Down      |
| 0                     | 0           | 0           | 1           | 1.0% Down      |
| 0                     | 0           | 1           | 0           | 1.25% Down     |
| 0                     | 0           | 1           | 1           | 1.50% Down     |
| 0                     | 1           | 0           | 0           | 1.75% Down     |
| 0                     | 1           | 0           | 1           | 2.0% Down      |
| 0                     | 1           | 1           | 0           | 2.5% Down      |
| 0                     | 1           | 1           | 1           | 3.0% Down      |
| 1                     | 0           | 0           | 0           | +0.3% Center   |
| 1                     | 0           | 0           | 1           | +0.4% Center   |
| 1                     | 0           | 1           | 0           | +0.5% Center   |
| 1                     | 0           | 1           | 1           | +0.6% Center   |
| 1                     | 1           | 0           | 0           | +0.8% Center   |
| 1                     | 1           | 0           | 1           | +1.0% Center   |
| 1                     | 1           | 1           | 0           | +1.25% Center  |
| 1                     | 1           | 1           | 1           | +1.5% Center   |

PCI Routing

|         | IDSEL | INT -> PIRQ | REQ/GNT     |
|---------|-------|-------------|-------------|
| OZ129TZ | AD22  | A..G        | REQ# ->REQ# |

PCIE Routing

|       |               |
|-------|---------------|
| LANE1 | LAN BCM5787M  |
| LANE2 | MiniCard WLAN |
| LANE3 | NewCard WLAN  |

USB Table

| USB ports definition |           |
|----------------------|-----------|
| Pair                 | Device    |
| 0                    | USB1      |
| 1                    | USB3      |
| 2                    | USB2      |
| 3                    | USB4      |
| 4                    | MINICARD  |
| 5                    | BlueTooth |
| 6                    | CCD       |
| 7                    | NewCard   |

Calistoga Strapping Signals and Configuration

| Pin Name          | Strap Description                      | Configuration                                                                                                                |
|-------------------|----------------------------------------|------------------------------------------------------------------------------------------------------------------------------|
| CFG[2:0]          | FSB Frequency Select                   | 001 = FSB533<br>011 = FSB667<br>others = Reserved                                                                            |
| CFG[4:3]          | Reserved                               |                                                                                                                              |
| CFG5              | DMI x2 Select                          | 0 = DMI x2<br>1 = DMI x4 (Default)                                                                                           |
| CFG6              | Reserved                               |                                                                                                                              |
| CFG7              | CPU Strap                              | 0 = Reserved<br>1 =Mobile CPU(Default)                                                                                       |
| CFG8              | Reserved                               |                                                                                                                              |
| CFG9              | PCI Express Graphics<br>Lane Reversal  | 0 = Reverse Lanes,15->0,14->1 ect..<br>1= Normal operation(Default):Lane<br>Numbered in order                                |
| CFG[11:10]        | Reserved                               |                                                                                                                              |
| CFG[13:12]        | XOR/ALL Z test<br>straps               | 00 = Reserved<br>01 = XOR mode enabled<br>10 = All Z mode enabled<br>11 = Normal operation<br>(Default)                      |
| CFG[15:14]        | Reserved                               | Reserved                                                                                                                     |
| CFG16             | FSB Dynamic ODT                        | 0 = Dynamic ODT Disabled<br>1 = Dynamic ODT Enabled (Default)                                                                |
| CFG17             | Global R-comp Disable<br>(All R-comps) | 0 = All R-comp Disable<br>1 = Normal Operation (Default)                                                                     |
| CFG18             | VCC Select                             | 0 = 1.05V (Default)<br>1 = 1.5V                                                                                              |
| CFG19             | DMI Lane Reversal                      | 0 = Normal operation (Default):lane<br>Numbered in order<br>1 =Reverse Lane,4->0,3->1 ect...                                 |
| CFG20             | SDVO/PCIE<br>Concurrent                | 0 = Only SDVO or PCIE x1 is<br>operational (Default)<br>1 =SDVO and PCIE x1 are operating<br>simultaneously via the PEG port |
| SDV0CTRL<br>_DATA | SDVO Present                           | 0 = No SDVO Card present<br>(Default)<br>1= SDVO Card present                                                                |

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

<Core Design>

緯創資通

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Title

Reference

Size

Document Number

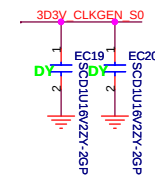
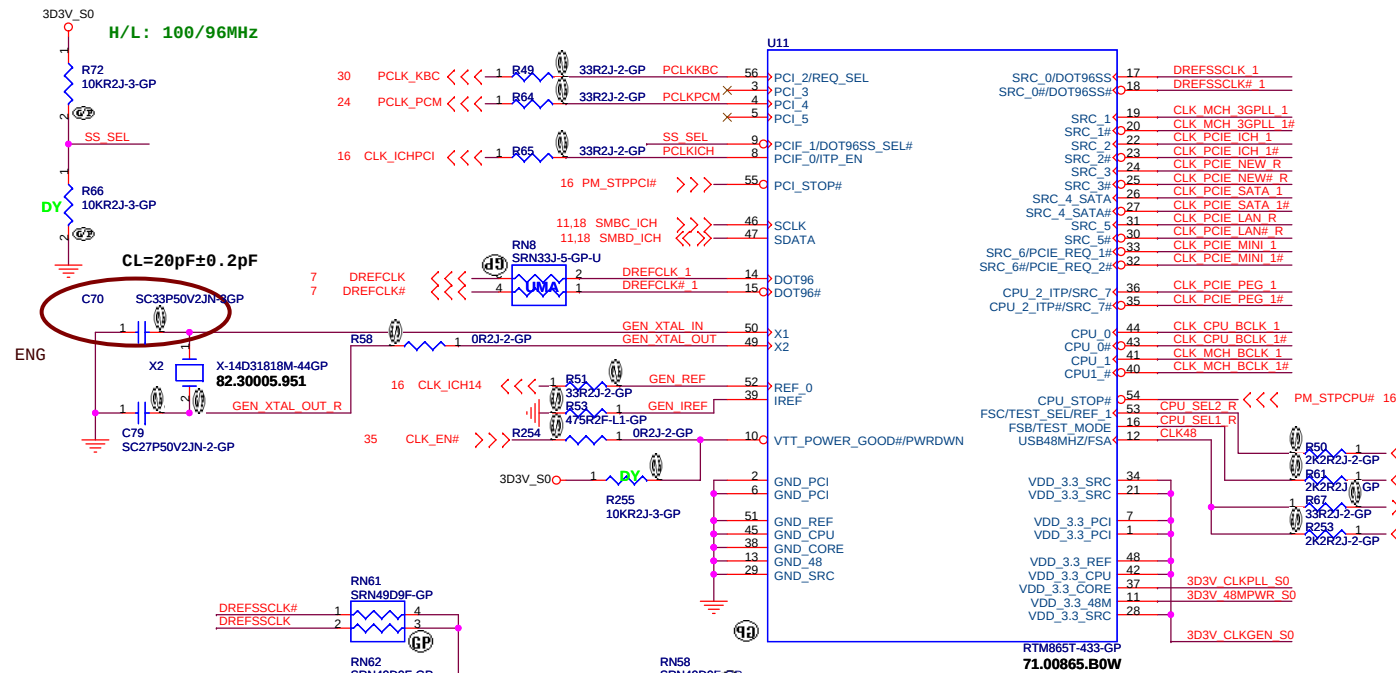
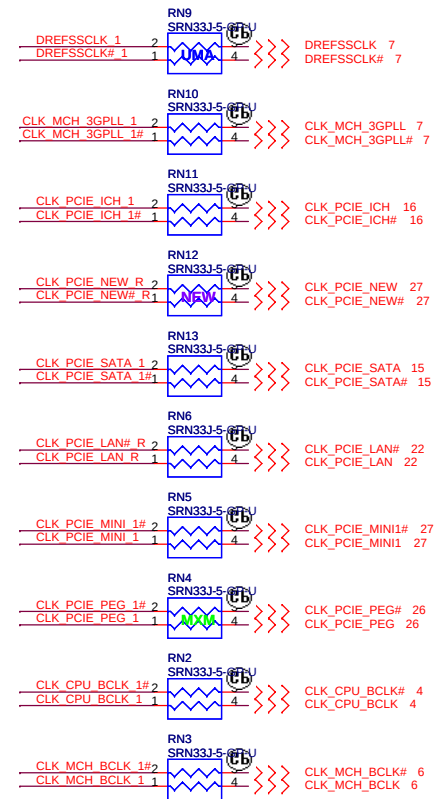
Rev

HURON

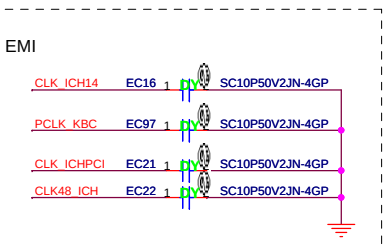
SD

Date: Monday, March 12, 2007

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| FSC | FSB | FSA | CPU      | FSB  |
|-----|-----|-----|----------|------|
| 0   | 0   | 0   | 266M     | X    |
| 0   | 0   | 1   | 133M     | 533M |
| 0   | 1   | 0   | 200M     | X    |
| 0   | 1   | 1   | 166M     | 667M |
| 1   | 0   | 0   | 333M     | X    |
| 1   | 0   | 1   | 100M     | X    |
| 1   | 1   | 0   | 400M     | X    |
| 1   | 1   | 1   | Reserved | X    |



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Title

CPU (1 of 2)

Size

|                 |
|-----------------|
| Document Number |
|-----------------|

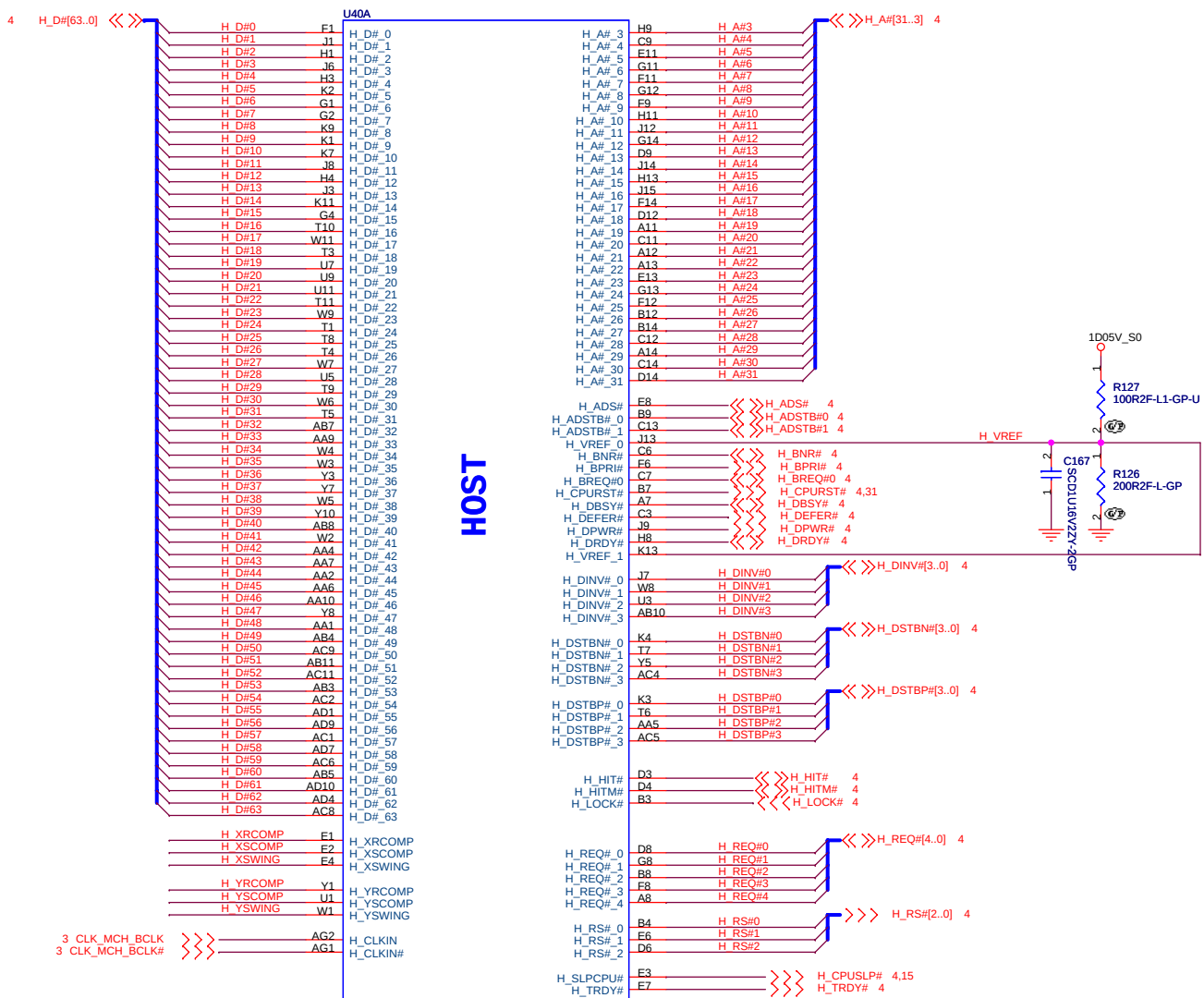
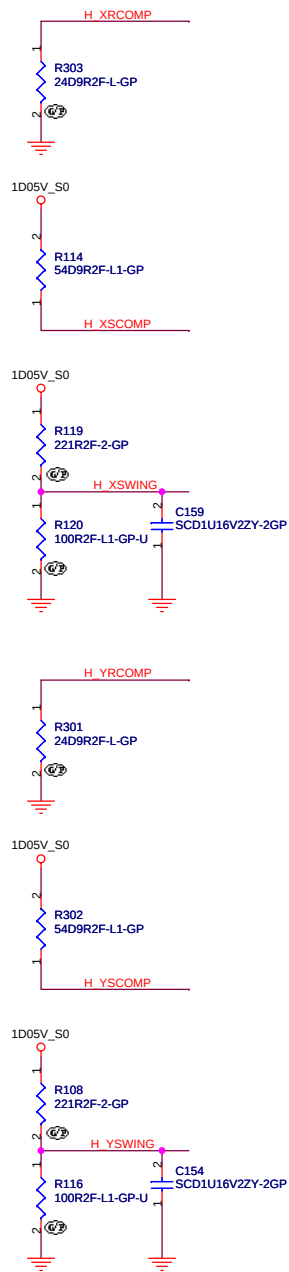
Rev

## HURON

Date: Monday, March 12, 2007

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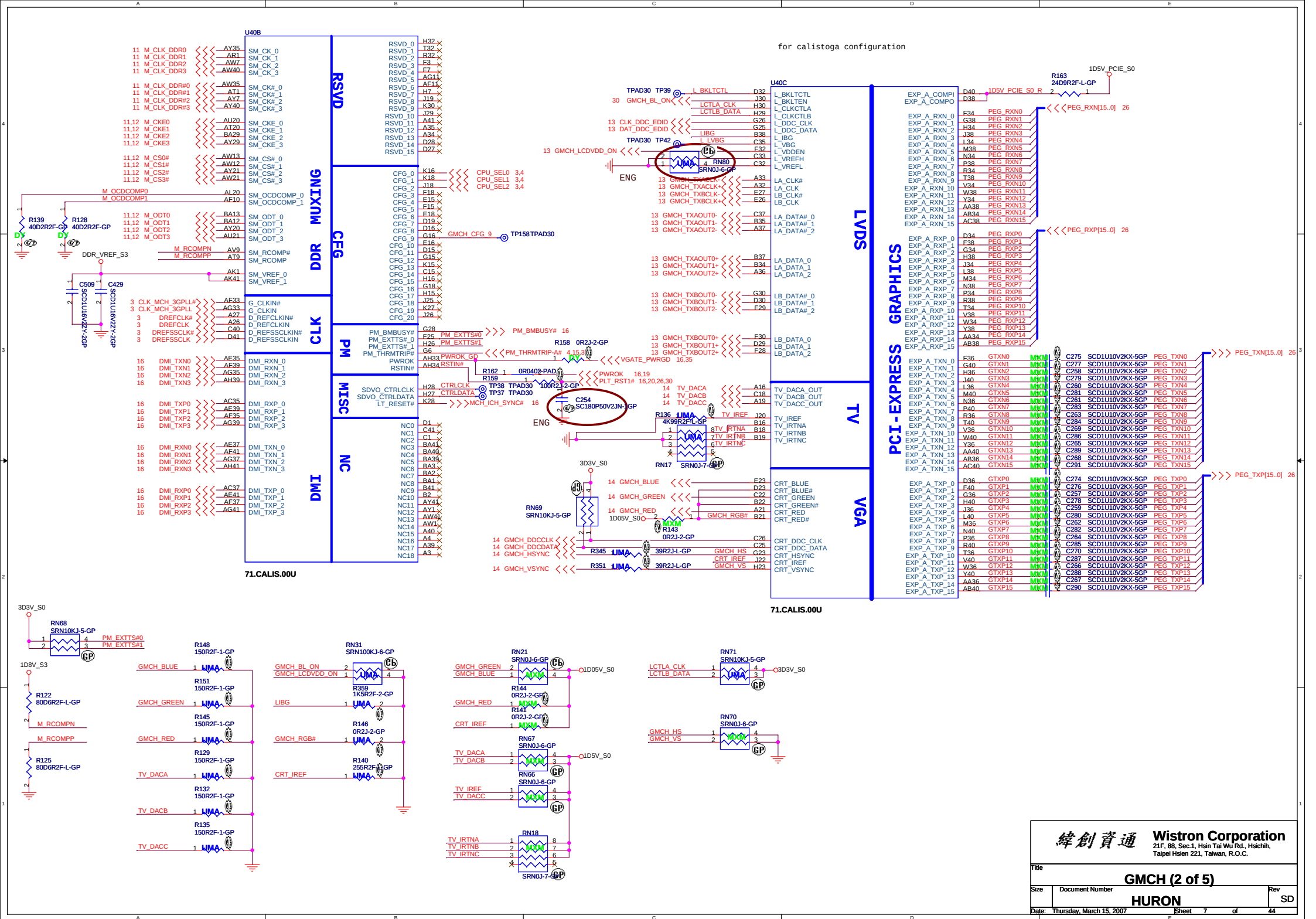


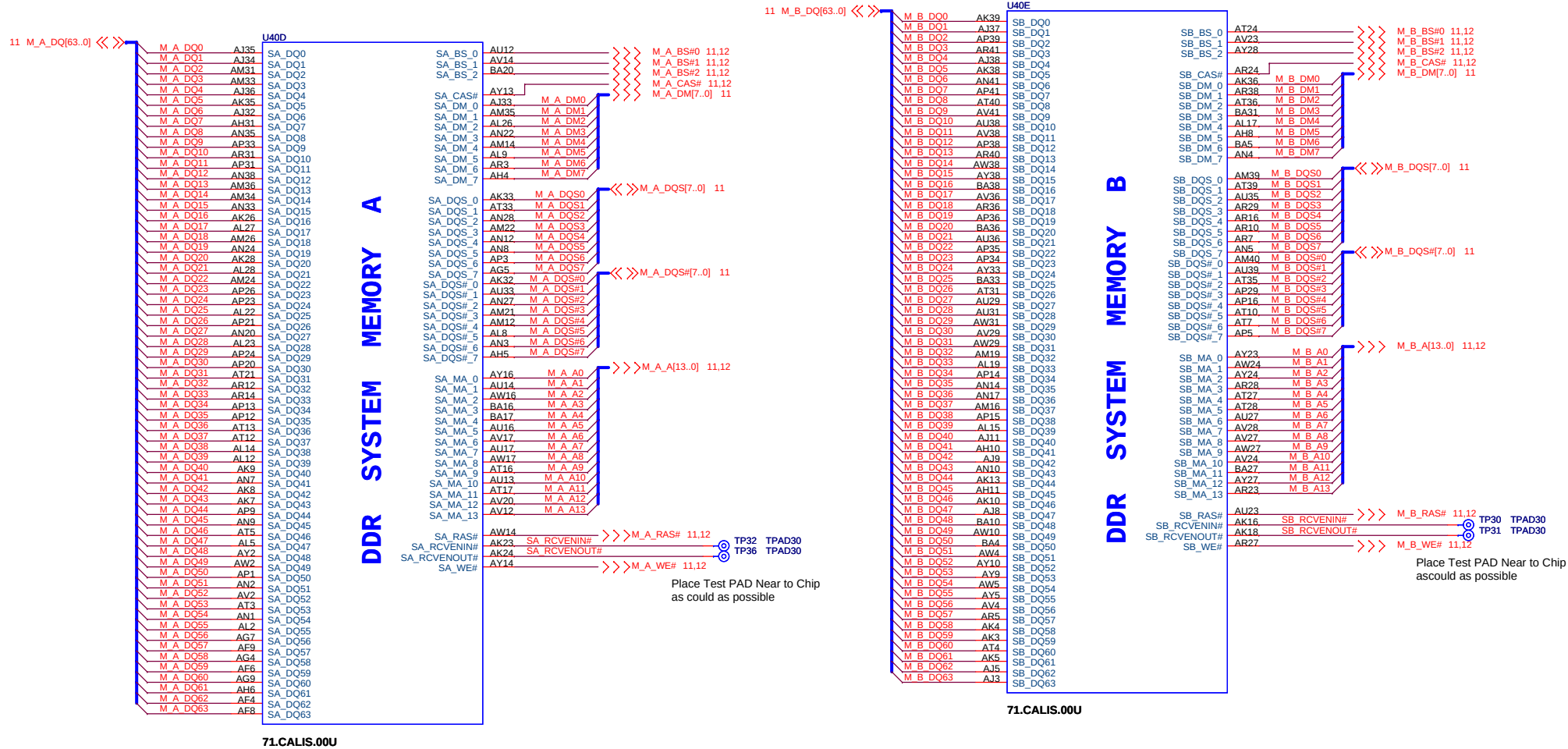


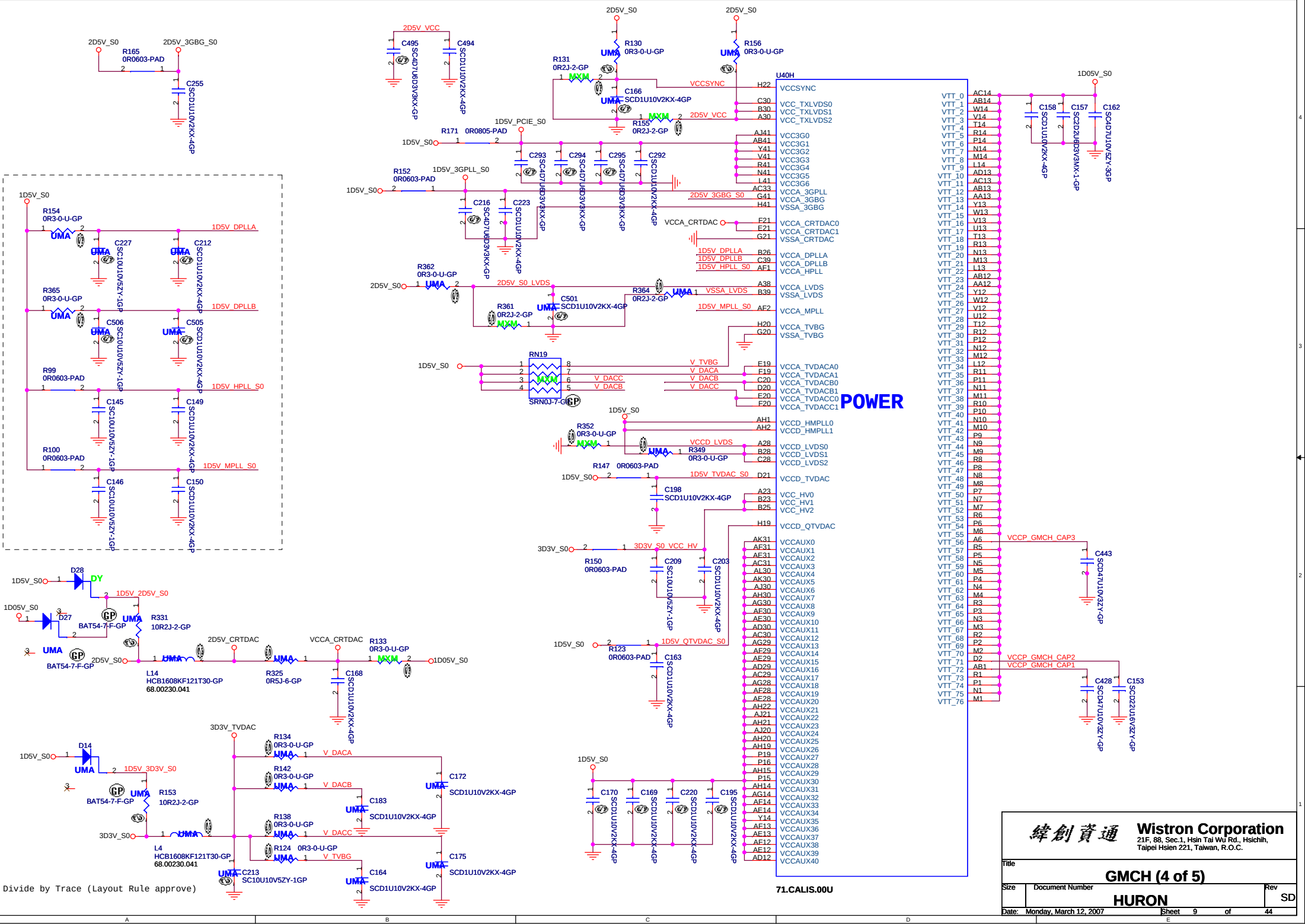
71.CALIS.00U

DIS : 945PN P/N is KI.94501.006  
UMA : 945GM P/N is KI.94501.005

Place them near to the chip ( < 0.5")







POWER

緯創資通 Wistron Corporation  
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|       |                        |               |    |
|-------|------------------------|---------------|----|
| Title |                        | GMCH (4 of 5) |    |
| Size  | Document Number        | Rev           | SD |
| Date: | Monday, March 12, 2007 | Sheet 9 of 44 |    |

Divide by Trace (Layout Rule approve)

71.CALIS.00U

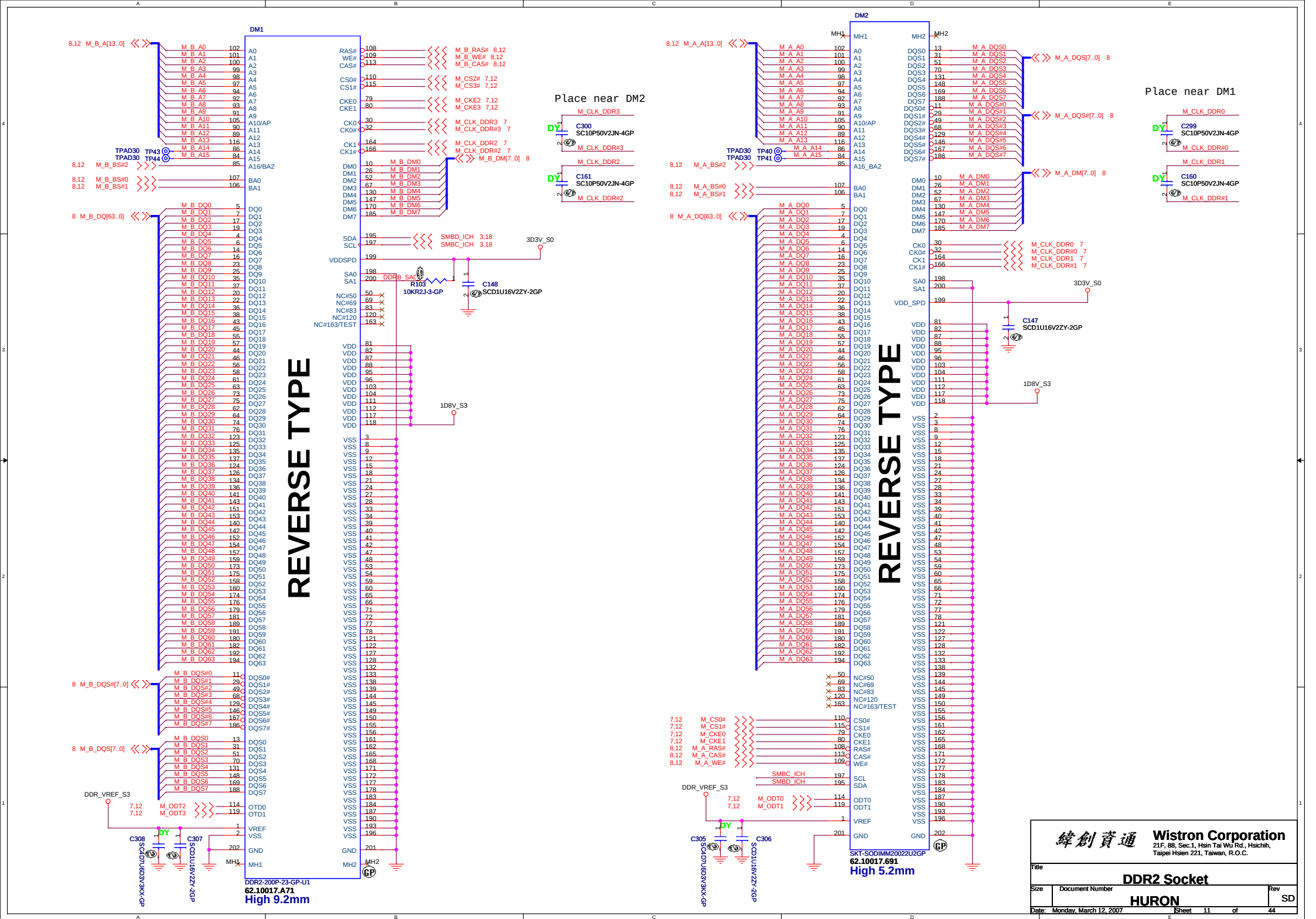
|          |      |         |      |
|----------|------|---------|------|
| 1D05V_S0 | AA33 | VCC_0   | U40G |
|          | W33  | VCC_1   |      |
|          | P33  | VCC_2   |      |
|          | M33  | VCC_3   |      |
|          | L33  | VCC_4   |      |
|          | J33  | VCC_5   |      |
|          | AA32 | VCC_6   |      |
|          | V32  | VCC_7   |      |
|          | W32  | VCC_8   |      |
|          | P32  | VCC_9   |      |
|          | M32  | VCC_10  |      |
|          | L32  | VCC_11  |      |
|          | J32  | VCC_12  |      |
|          | AA31 | VCC_13  |      |
|          | W31  | VCC_14  |      |
|          | P31  | VCC_15  |      |
|          | M31  | VCC_16  |      |
|          | L31  | VCC_17  |      |
|          | J31  | VCC_18  |      |
|          | AA30 | VCC_19  |      |
|          | W30  | VCC_20  |      |
|          | P30  | VCC_21  |      |
|          | M30  | VCC_22  |      |
|          | L30  | VCC_23  |      |
|          | J30  | VCC_24  |      |
|          | AA29 | VCC_25  |      |
|          | W29  | VCC_26  |      |
|          | P29  | VCC_27  |      |
|          | M29  | VCC_28  |      |
|          | L29  | VCC_29  |      |
|          | J29  | VCC_30  |      |
|          | AA28 | VCC_31  |      |
|          | W28  | VCC_32  |      |
|          | P28  | VCC_33  |      |
|          | M28  | VCC_34  |      |
|          | L28  | VCC_35  |      |
|          | J28  | VCC_36  |      |
|          | AA27 | VCC_37  |      |
|          | W27  | VCC_38  |      |
|          | P27  | VCC_39  |      |
|          | M27  | VCC_40  |      |
|          | L27  | VCC_41  |      |
|          | J27  | VCC_42  |      |
|          | AA26 | VCC_43  |      |
|          | W26  | VCC_44  |      |
|          | P26  | VCC_45  |      |
|          | M26  | VCC_46  |      |
|          | L26  | VCC_47  |      |
|          | J26  | VCC_48  |      |
|          | AA25 | VCC_49  |      |
|          | W25  | VCC_50  |      |
|          | P25  | VCC_51  |      |
|          | M25  | VCC_52  |      |
|          | L25  | VCC_53  |      |
|          | J25  | VCC_54  |      |
|          | AA24 | VCC_55  |      |
|          | W24  | VCC_56  |      |
|          | P24  | VCC_57  |      |
|          | M24  | VCC_58  |      |
|          | L24  | VCC_59  |      |
|          | J24  | VCC_60  |      |
|          | AA23 | VCC_61  |      |
|          | W23  | VCC_62  |      |
|          | P23  | VCC_63  |      |
|          | M23  | VCC_64  |      |
|          | L23  | VCC_65  |      |
|          | J23  | VCC_66  |      |
|          | AA22 | VCC_67  |      |
|          | W22  | VCC_68  |      |
|          | P22  | VCC_69  |      |
|          | M22  | VCC_70  |      |
|          | L22  | VCC_71  |      |
|          | J22  | VCC_72  |      |
|          | AA21 | VCC_73  |      |
|          | W21  | VCC_74  |      |
|          | P21  | VCC_75  |      |
|          | M21  | VCC_76  |      |
|          | L21  | VCC_77  |      |
|          | J21  | VCC_78  |      |
|          | AA20 | VCC_79  |      |
|          | W20  | VCC_80  |      |
|          | P20  | VCC_81  |      |
|          | M20  | VCC_82  |      |
|          | L20  | VCC_83  |      |
|          | J20  | VCC_84  |      |
|          | AA19 | VCC_85  |      |
|          | W19  | VCC_86  |      |
|          | P19  | VCC_87  |      |
|          | M19  | VCC_88  |      |
|          | L19  | VCC_89  |      |
|          | J19  | VCC_90  |      |
|          | AA18 | VCC_91  |      |
|          | W18  | VCC_92  |      |
|          | P18  | VCC_93  |      |
|          | M18  | VCC_94  |      |
|          | L18  | VCC_95  |      |
|          | J18  | VCC_96  |      |
|          | AA17 | VCC_97  |      |
|          | W17  | VCC_98  |      |
|          | P17  | VCC_99  |      |
|          | M17  | VCC_100 |      |
|          | L17  | VCC_101 |      |
|          | J17  | VCC_102 |      |
|          | AA16 | VCC_103 |      |
|          | W16  | VCC_104 |      |
|          | P16  | VCC_105 |      |
|          | M16  | VCC_106 |      |
|          | L16  | VCC_107 |      |
|          | J16  | VCC_108 |      |
|          | AA15 | VCC_109 |      |
|          | W15  | VCC_110 |      |
|          | P15  | VCC_111 |      |
|          | M15  | VCC_112 |      |
|          | L15  | VCC_113 |      |
|          | J15  | VCC_114 |      |
|          | AA14 | VCC_115 |      |
|          | W14  | VCC_116 |      |
|          | P14  | VCC_117 |      |
|          | M14  | VCC_118 |      |
|          | L14  | VCC_119 |      |
|          | J14  | VCC_120 |      |
|          | AA13 | VCC_121 |      |
|          | W13  | VCC_122 |      |
|          | P13  | VCC_123 |      |
|          | M13  | VCC_124 |      |
|          | L13  | VCC_125 |      |
|          | J13  | VCC_126 |      |
|          | AA12 | VCC_127 |      |
|          | W12  | VCC_128 |      |
|          | P12  | VCC_129 |      |
|          | M12  | VCC_130 |      |
|          | L12  | VCC_131 |      |
|          | J12  | VCC_132 |      |
|          | AA11 | VCC_133 |      |
|          | W11  | VCC_134 |      |
|          | P11  | VCC_135 |      |
|          | M11  | VCC_136 |      |
|          | L11  | VCC_137 |      |
|          | J11  | VCC_138 |      |
|          | AA10 | VCC_139 |      |
|          | W10  | VCC_140 |      |
|          | P10  | VCC_141 |      |
|          | M10  | VCC_142 |      |
|          | L10  | VCC_143 |      |
|          | J10  | VCC_144 |      |
|          | AA9  | VCC_145 |      |
|          | W9   | VCC_146 |      |
|          | P9   | VCC_147 |      |
|          | M9   | VCC_148 |      |
|          | L9   | VCC_149 |      |
|          | J9   | VCC_150 |      |
|          | AA8  | VCC_151 |      |
|          | W8   | VCC_152 |      |
|          | P8   | VCC_153 |      |
|          | M8   | VCC_154 |      |
|          | L8   | VCC_155 |      |
|          | J8   | VCC_156 |      |
|          | AA7  | VCC_157 |      |
|          | W7   | VCC_158 |      |
|          | P7   | VCC_159 |      |
|          | M7   | VCC_160 |      |
|          | L7   | VCC_161 |      |
|          | J7   | VCC_162 |      |
|          | AA6  | VCC_163 |      |
|          | W6   | VCC_164 |      |
|          | P6   | VCC_165 |      |
|          | M6   | VCC_166 |      |
|          | L6   | VCC_167 |      |
|          | J6   | VCC_168 |      |
|          | AA5  | VCC_169 |      |
|          | W5   | VCC_170 |      |
|          | P5   | VCC_171 |      |
|          | M5   | VCC_172 |      |
|          | L5   | VCC_173 |      |
|          | J5   | VCC_174 |      |
|          | AA4  | VCC_175 |      |
|          | W4   | VCC_176 |      |
|          | P4   | VCC_177 |      |
|          | M4   | VCC_178 |      |
|          | L4   | VCC_179 |      |
|          | J4   | VCC_180 |      |
|          | AA3  | VCC_181 |      |
|          | W3   | VCC_182 |      |
|          | P3   | VCC_183 |      |
|          | M3   | VCC_184 |      |
|          | L3   | VCC_185 |      |
|          | J3   | VCC_186 |      |
|          | AA2  | VCC_187 |      |
|          | W2   | VCC_188 |      |
|          | P2   | VCC_189 |      |
|          | M2   | VCC_190 |      |
|          | L2   | VCC_191 |      |
|          | J2   | VCC_192 |      |
|          | AA1  | VCC_193 |      |
|          | W1   | VCC_194 |      |
|          | P1   | VCC_195 |      |
|          | M1   | VCC_196 |      |
|          | L1   | VCC_197 |      |
|          | J1   | VCC_198 |      |
|          | AA0  | VCC_199 |      |
|          | W0   | VCC_200 |      |
|          | P0   | VCC_201 |      |
|          | M0   | VCC_202 |      |
|          | L0   | VCC_203 |      |
|          | J0   | VCC_204 |      |
|          | AA0  | VCC_205 |      |
|          | W0   | VCC_206 |      |
|          | P0   | VCC_207 |      |
|          | M0   | VCC_208 |      |
|          | L0   | VCC_209 |      |
|          | J0   | VCC_210 |      |
|          | AA0  | VCC_211 |      |
|          | W0   | VCC_212 |      |
|          | P0   | VCC_213 |      |
|          | M0   | VCC_214 |      |
|          | L0   | VCC_215 |      |
|          | J0   | VCC_216 |      |
|          | AA0  | VCC_217 |      |
|          | W0   | VCC_218 |      |
|          | P0   | VCC_219 |      |
|          | M0   | VCC_220 |      |
|          | L0   | VCC_221 |      |
|          | J0   | VCC_222 |      |
|          | AA0  | VCC_223 |      |
|          | W0   | VCC_224 |      |
|          | P0   | VCC_225 |      |
|          | M0   | VCC_226 |      |
|          | L0   | VCC_227 |      |
|          | J0   | VCC_228 |      |
|          | AA0  | VCC_229 |      |
|          | W0   | VCC_230 |      |
|          | P0   | VCC_231 |      |
|          | M0   | VCC_232 |      |
|          | L0   | VCC_233 |      |
|          | J0   | VCC_234 |      |
|          | AA0  | VCC_235 |      |
|          | W0   | VCC_236 |      |
|          | P0   | VCC_237 |      |
|          | M0   | VCC_238 |      |
|          | L0   | VCC_239 |      |
|          | J0   | VCC_240 |      |
|          | AA0  | VCC_241 |      |
|          | W0   | VCC_242 |      |
|          | P0   | VCC_243 |      |
|          | M0   | VCC_244 |      |
|          | L0   | VCC_245 |      |
|          | J0   | VCC_246 |      |
|          | AA0  | VCC_247 |      |
|          | W0   | VCC_248 |      |
|          | P0   | VCC_249 |      |
|          | M0   | VCC_250 |      |
|          | L0   | VCC_251 |      |
|          | J0   | VCC_252 |      |
|          | AA0  | VCC_253 |      |
|          | W0   | VCC_254 |      |
|          | P0   | VCC_255 |      |
|          | M0   | VCC_256 |      |
|          | L0   | VCC_257 |      |
|          | J0   | VCC_258 |      |
|          | AA0  | VCC_259 |      |
|          | W0   | VCC_260 |      |
|          | P0   | VCC_261 |      |
|          | M0   | VCC_262 |      |
|          | L0   | VCC_263 |      |
|          | J0   | VCC_264 |      |
|          | AA0  | VCC_265 |      |
|          | W0   | VCC_266 |      |
|          | P0   | VCC_267 |      |
|          | M0   | VCC_268 |      |
|          | L0   | VCC_269 |      |
|          | J0   | VCC_270 |      |
|          | AA0  | VCC_271 |      |
|          | W0   | VCC_272 |      |
|          | P0   | VCC_273 |      |
|          | M0   | VCC_274 |      |
|          | L0   | VCC_275 |      |
|          | J0   | VCC_276 |      |
|          | AA0  | VCC_277 |      |
|          | W0   | VCC_278 |      |
|          | P0   | VCC_279 |      |
|          | M0   | VCC_280 |      |
|          | L0   | VCC_281 |      |
|          | J0   | VCC_282 |      |
|          | AA0  | VCC_283 |      |
|          | W0   | VCC_284 |      |
|          | P0   | VCC_285 |      |
|          | M0   | VCC_286 |      |
|          | L0   | VCC_287 |      |
|          | J0   | VCC_288 |      |
|          | AA0  | VCC_289 |      |
|          | W0   | VCC_290 |      |
|          | P0   | VCC_291 |      |
|          | M0   | VCC_292 |      |
|          | L0   | VCC_293 |      |
|          | J0   | VCC_294 |      |
|          | AA0  | VCC_295 |      |
|          | W0   | VCC_296 |      |
|          | P0   | VCC_297 |      |
|          | M0   | VCC_298 |      |
|          | L0   | VCC_299 |      |
|          | J0   | VCC_300 |      |
|          | AA0  | VCC_301 |      |
|          | W0   | VCC_302 |      |
|          | P0   | VCC_303 |      |
|          | M0   | VCC_304 |      |
|          | L0   | VCC_305 |      |
|          | J0   | VCC_306 |      |
|          | AA0  | VCC_307 |      |
|          | W0   | VCC_308 |      |
|          | P0   | VCC_309 |      |
|          | M0   | VCC_310 |      |
|          | L0   | VCC_311 |      |
|          | J0   | VCC_312 |      |
|          | AA0  | VCC_313 |      |
|          | W0   | VCC_314 |      |
|          | P0   | VCC_315 |      |
|          | M0   | VCC_316 |      |
|          | L0   | VCC_317 |      |
|          | J0   | VCC_318 |      |
|          | AA0  | VCC_319 |      |
|          | W0   | VCC_320 |      |
|          | P0   | VCC_321 |      |
|          | M0   | VCC_322 |      |
|          | L0   | VCC_323 |      |
|          | J0   | VCC_324 |      |
|          | AA0  | VCC_325 |      |
|          | W0   | VCC_326 |      |
|          | P0   | VCC_327 |      |
|          | M0   | VCC_328 |      |
|          | L0   | VCC_329 |      |
|          | J0   | VCC_330 |      |
|          | AA0  | VCC_331 |      |
|          | W0   | VCC_332 |      |
|          | P0   | VCC_333 |      |
|          | M0   | VCC_334 |      |
|          | L0   | VCC_335 |      |
|          | J0   | VCC_336 |      |
|          | AA0  | VCC_337 |      |
|          | W0   | VCC_338 |      |
|          | P0   | VCC_339 |      |
|          | M0   | VCC_340 |      |
|          | L0   | VCC_341 |      |
|          | J0   | VCC_342 |      |
|          | AA0  | VCC_343 |      |
|          | W0   | VCC_344 |      |
|          | P0   | VCC_345 |      |
|          | M0   | VCC_346 |      |
|          | L0   | VCC_347 |      |
|          | J0   | VCC_348 |      |
|          | AA0  | VCC_349 |      |
|          | W0   | VCC_350 |      |
|          | P0   | VCC_351 |      |
|          | M0   | VCC_352 |      |
|          | L0   | VCC_353 |      |
|          | J0   | VCC_354 |      |
|          | AA0  | VCC_355 |      |
|          | W0   | VCC_356 |      |
|          | P0   | VCC_357 |      |
|          | M0   | VCC_358 |      |
|          | L0   | VCC_359 |      |
|          | J0   | VCC_360 |      |

71.CALIS.00U

1D05V\_S0 U40F

71.CALIS.00U

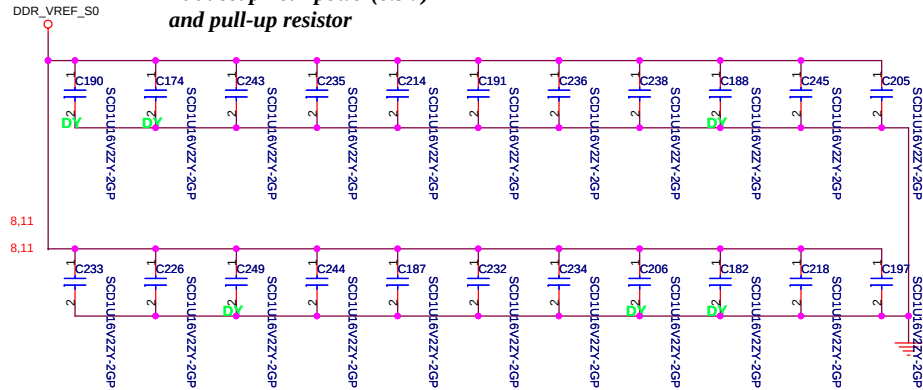
|      |            |            |      |
|------|------------|------------|------|
| AD27 | VCC_NCTF0  | VSS_NCTF0  | AE27 |
| AC27 | VCC_NCTF1  | VSS_NCTF1  | AE26 |
| AB27 | VCC_NCTF2  | VSS_NCTF1  | AE25 |
| AA27 | VCC_NCTF3  | VSS_NCTF2  | AE24 |
| W27  | VCC_NCTF4  | VSS_NCTF3  | AE23 |
| V27  | VCC_NCTF5  | VSS_NCTF4  | AE22 |
| W27  | VCC_NCTF6  | VSS_NCTF5  | AE21 |
| T27  | VCC_NCTF7  | VSS_NCTF6  | AE20 |
| R27  | VCC_NCTF8  | VSS_NCTF7  | AE19 |
| Q27  | VCC_NCTF9  | VSS_NCTF8  | AE18 |
| P27  | VCC_NCTF10 | VSS_NCTF9  | AE17 |
| O27  | VCC_NCTF11 | VSS_NCTF10 | AE16 |
| N27  | VCC_NCTF12 | VSS_NCTF11 | AE15 |
| M27  | VCC_NCTF13 | VSS_NCTF12 | AE14 |
| L27  | VCC_NCTF14 | VSS_NCTF13 | AE13 |
| K27  | VCC_NCTF15 | VSS_NCTF14 | AE12 |
| J27  | VCC_NCTF16 | VSS_NCTF15 | AE11 |
| I27  | VCC_NCTF17 | VSS_NCTF16 | AE10 |
| H27  | VCC_NCTF18 | VSS_NCTF17 | AE09 |
| G27  | VCC_NCTF19 | VSS_NCTF18 | AE08 |
| F27  | VCC_NCTF20 | VSS_NCTF19 | AE07 |
| E27  | VCC_NCTF21 | VSS_NCTF20 | AE06 |
| D27  | VCC_NCTF22 | VSS_NCTF21 | AE05 |
| C27  | VCC_NCTF23 | VSS_NCTF22 | AE04 |
| B27  | VCC_NCTF24 | VSS_NCTF23 | AE03 |
| A27  | VCC_NCTF25 | VSS_NCTF24 | AE02 |
| W27  | VCC_NCTF26 | VSS_NCTF25 | AE01 |
| V27  | VCC_NCTF27 | VSS_NCTF26 | AE00 |
| W27  | VCC_NCTF28 | VSS_NCTF27 | AE00 |
| T27  | VCC_NCTF29 | VSS_NCTF28 | AE00 |
| R27  | VCC_NCTF30 | VSS_NCTF29 | AE00 |
| Q27  | VCC_NCTF31 | VSS_NCTF30 | AE00 |
| P27  | VCC_NCTF32 | VSS_NCTF31 | AE00 |
| O27  | VCC_NCTF33 | VSS_NCTF32 | AE00 |
| N27  | VCC_NCTF34 | VSS_NCTF33 | AE00 |
| M27  | VCC_NCTF35 | VSS_NCTF34 | AE00 |
| L27  | VCC_NCTF36 | VSS_NCTF35 | AE00 |
| K27  | VCC_NCTF37 | VSS_NCTF36 | AE00 |
| J27  | VCC_NCTF38 | VSS_NCTF37 | AE00 |
| I27  | VCC_NCTF39 | VSS_NCTF38 | AE00 |
| H27  | VCC_NCTF40 | VSS_NCTF39 | AE00 |
| G27  | VCC_NCTF41 | VSS_NCTF40 | AE00 |
| F27  | VCC_NCTF42 | VSS_NCTF41 | AE00 |
| E27  | VCC_NCTF43 | VSS_NCTF42 | AE00 |
| D27  | VCC_NCTF44 | VSS_NCTF43 | AE00 |
| C27  | VCC_NCTF45 | VSS_NCTF44 | AE00 |
| B27  | VCC_NCTF46 | VSS_NCTF45 | AE00 |
| A27  | VCC_NCTF47 | VSS_NCTF46 | AE00 |
| W27  | VCC_NCTF48 | VSS_NCTF47 | AE00 |
| V27  | VCC_NCTF49 | VSS_NCTF48 | AE00 |
| W27  | VCC_NCTF50 | VSS_NCTF49 | AE00 |
| T27  | VCC_NCTF51 | VSS_NCTF50 | AE00 |
| R27  | VCC_NCTF52 | VSS_NCTF51 | AE00 |
| Q27  | VCC_NCTF53 | VSS_NCTF52 | AE00 |
| P27  | VCC_NCTF54 | VSS_NCTF53 | AE00 |
| O27  | VCC_NCTF55 | VSS_NCTF54 | AE00 |
| N27  | VCC_NCTF56 | VSS_NCTF55 | AE00 |
| M27  | VCC_NCTF57 | VSS_NCTF56 | AE00 |
| L27  | VCC_NCTF58 | VSS_NCTF57 | AE00 |
| K27  | VCC_NCTF59 | VSS_NCTF58 | AE00 |
| J27  | VCC_NCTF60 | VSS_NCTF59 | AE00 |
| I27  | VCC_NCTF61 | VSS_NCTF60 | AE00 |
| H27  | VCC_NCTF62 | VSS_NCTF61 | AE00 |
| G27  | VCC_NCTF63 | VSS_NCTF62 | AE00 |
| F27  | VCC_NCTF64 | VSS_NCTF63 | AE00 |
| E27  | VCC_NCTF65 | VSS_NCTF64 | AE00 |
| D27  | VCC_NCTF66 | VSS_NCTF65 | AE00 |
| C27  | VCC_NCTF67 | VSS_NCTF66 | AE00 |
| B27  | VCC_NCTF68 | VSS_NCTF67 | AE00 |
| A27  | VCC_NCTF69 | VSS_NCTF68 | AE00 |
| W27  | VCC_NCTF70 | VSS_NCTF69 | AE00 |
| V27  | VCC_NCTF71 | VSS_NCTF70 | AE00 |
| W27  | VCC_NCTF72 | VSS_NCTF71 | AE00 |
| T27  | VCC_NCTF73 | VSS_NCTF72 | AE00 |

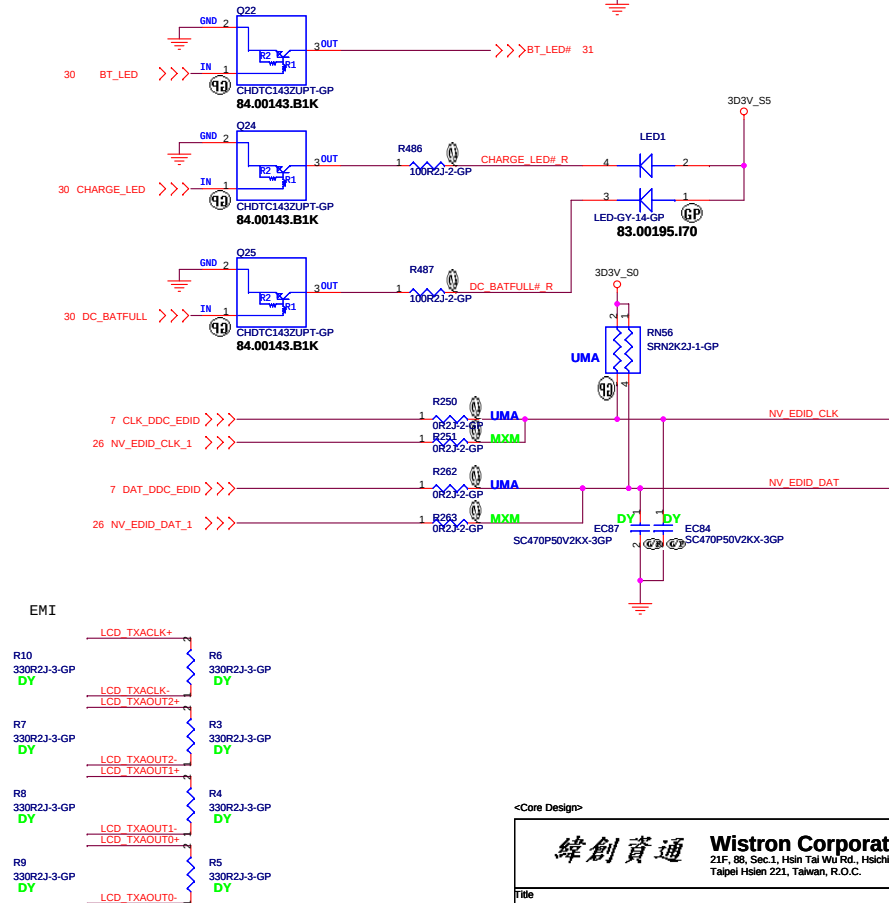
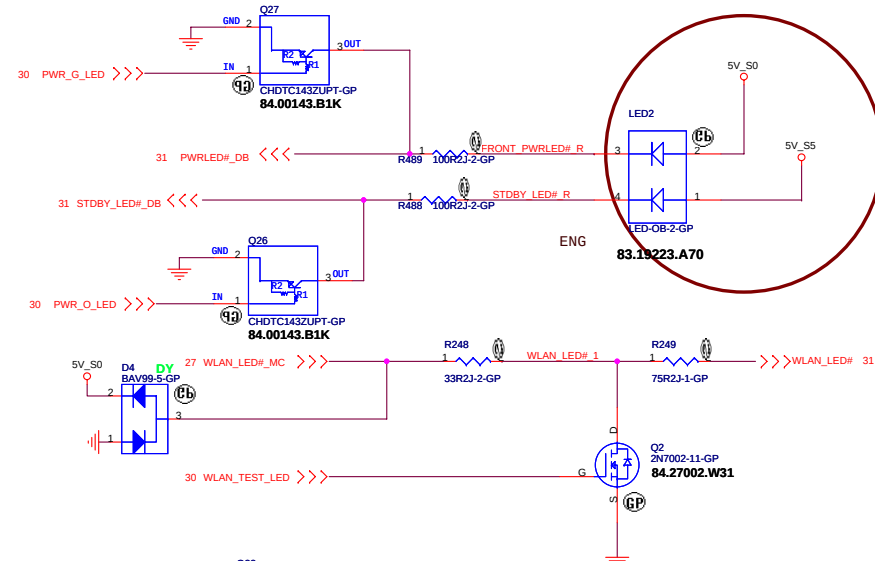


**Put decap near power(0.9V) and pull-up resistor**



**Put decap near power(0.9V)  
and pull-up resistor**

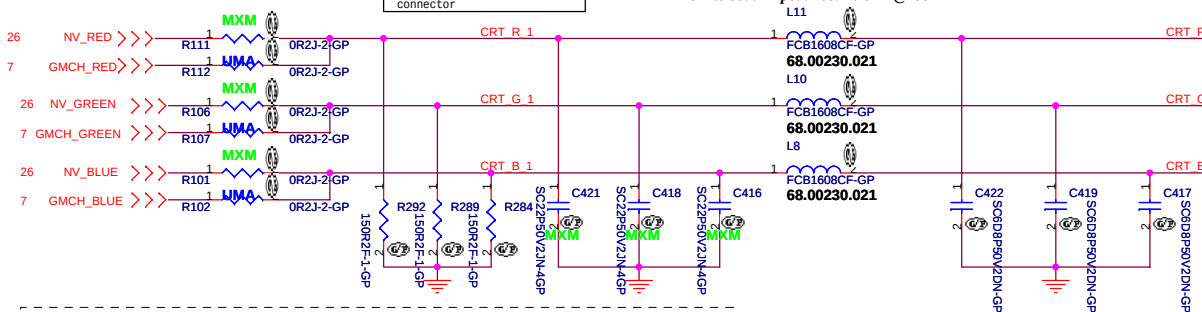
[illegible]



# CRT I/F & CONNECTOR

Layout Note:  
Place these resistors  
close to the CRT-out  
connector

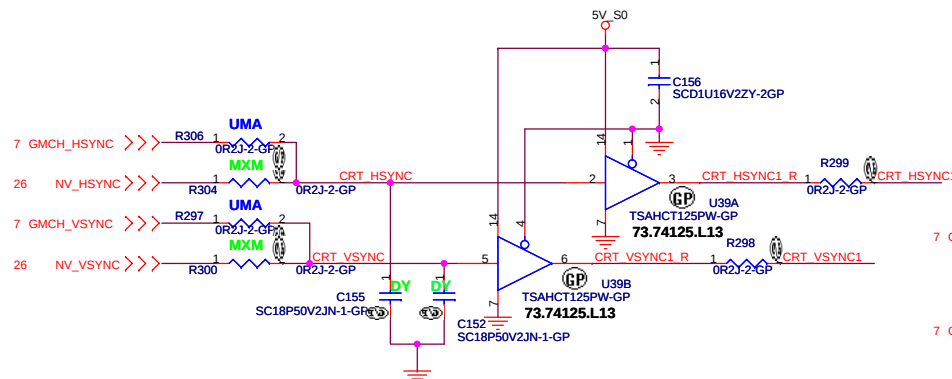
Ferrite bead impedance: 10 ohm@100MHz



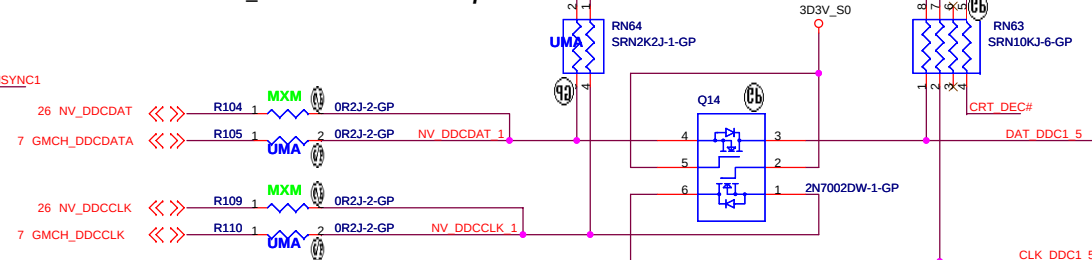
Layout Note:

\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

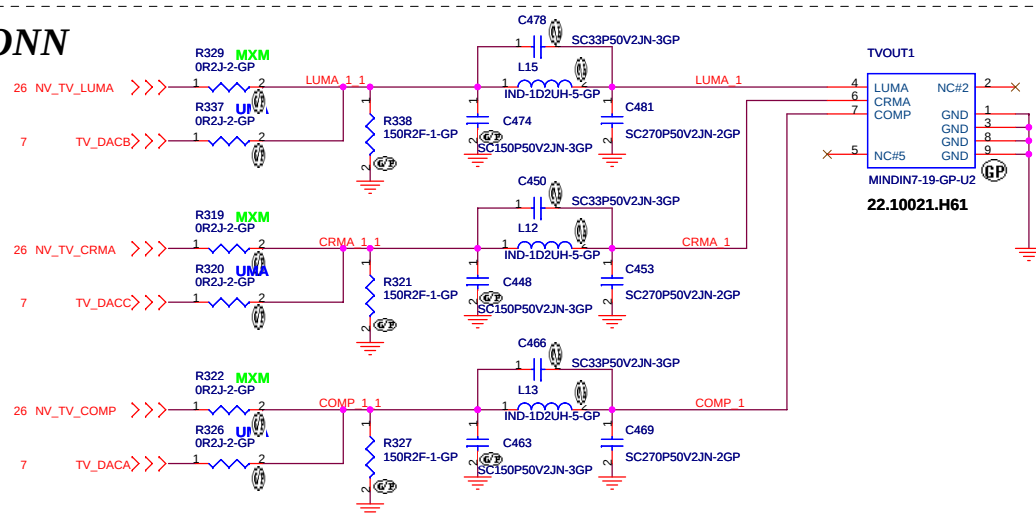
Hsync & Vsync level shift



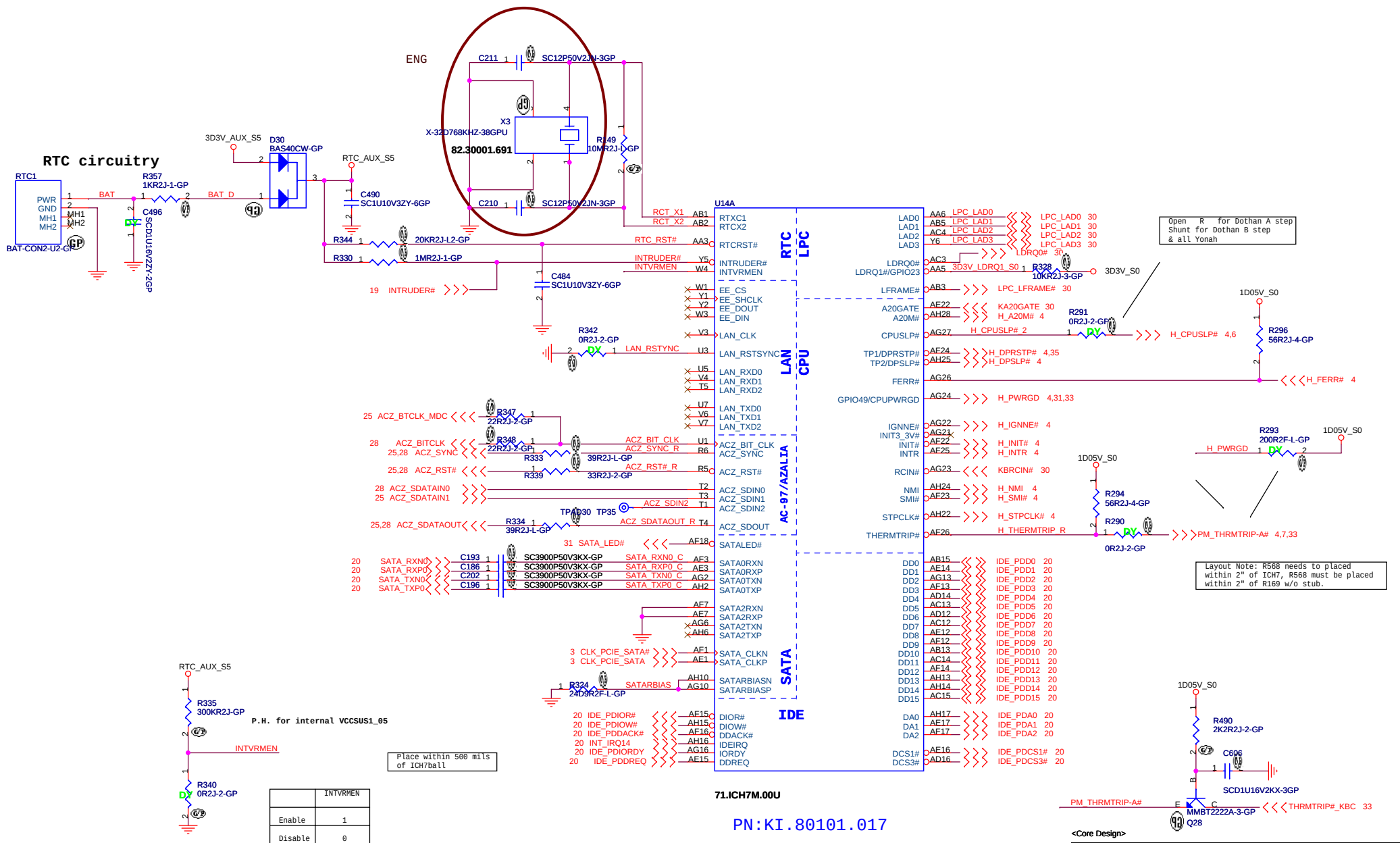
DDC\_CLK & DATA level shift

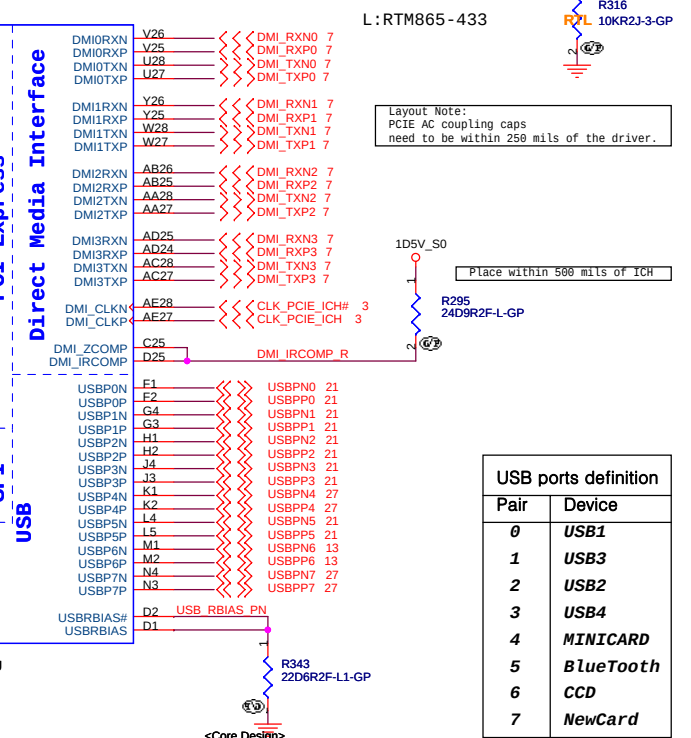
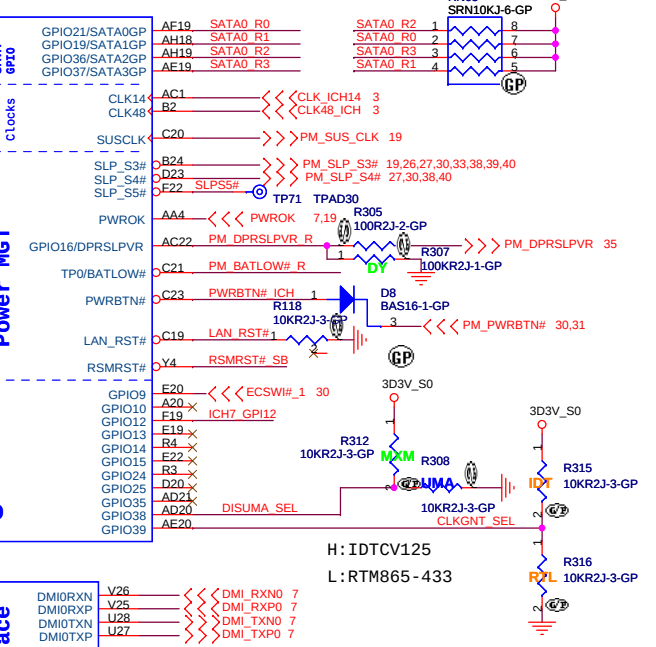


## TV CONN



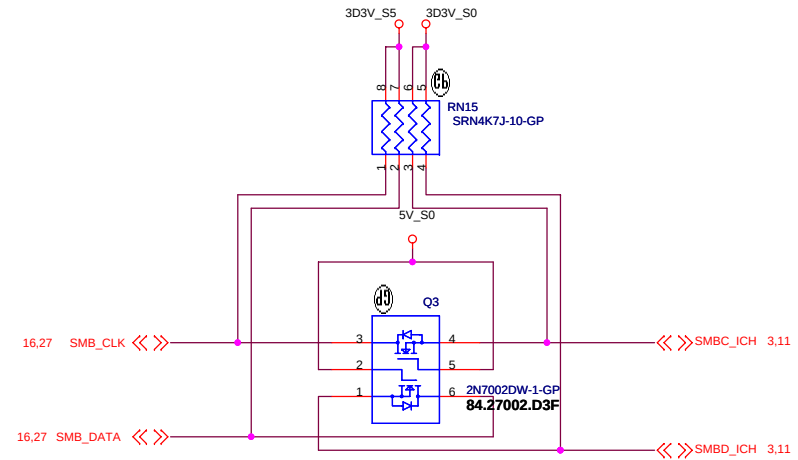
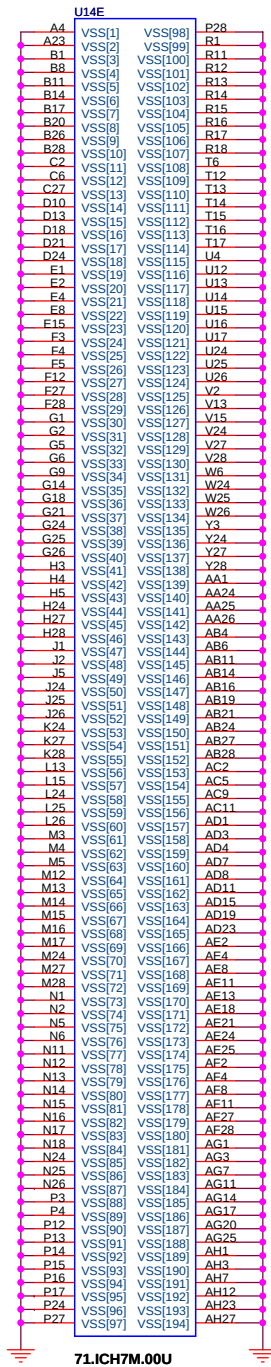
|                         |                        |                                                                               |       |
|-------------------------|------------------------|-------------------------------------------------------------------------------|-------|
| <b>緯創資通</b>             |                        | <b>Wistron Corporation</b>                                                    |       |
|                         |                        | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |       |
| Title                   |                        |                                                                               |       |
| <b>CRT/TV Connector</b> |                        |                                                                               |       |
| Size                    | Document Number        |                                                                               | Rev   |
| <b>HURON</b>            |                        |                                                                               |       |
| Date:                   | Mondav. March 12, 2007 | Sheet 14                                                                      | of 44 |





A circuit diagram showing a diode labeled G55. The diode is oriented with its cathode (marked '1') connected to a signal line labeled PSW\_CLR# and its anode (marked '2') connected to ground. The diode is also labeled GAP-OPEN.



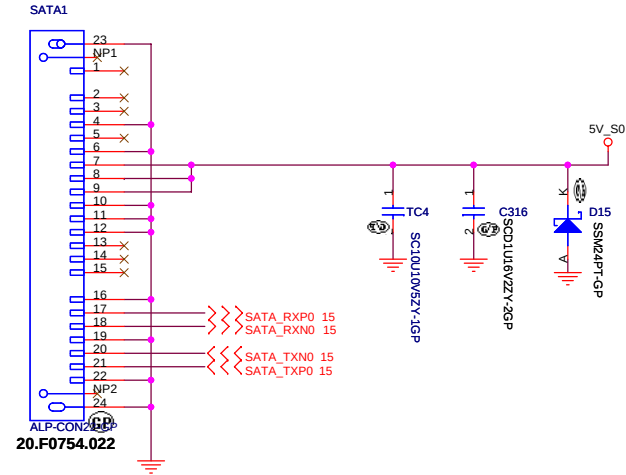


Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

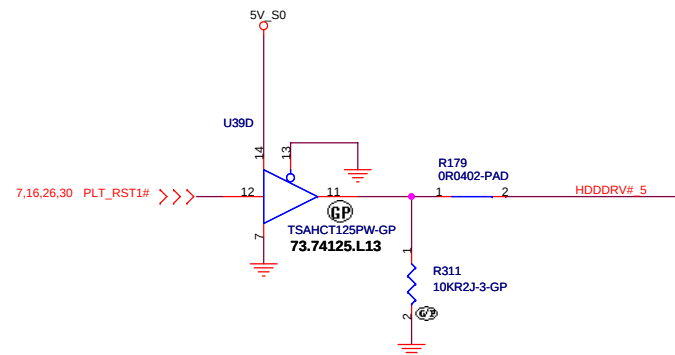
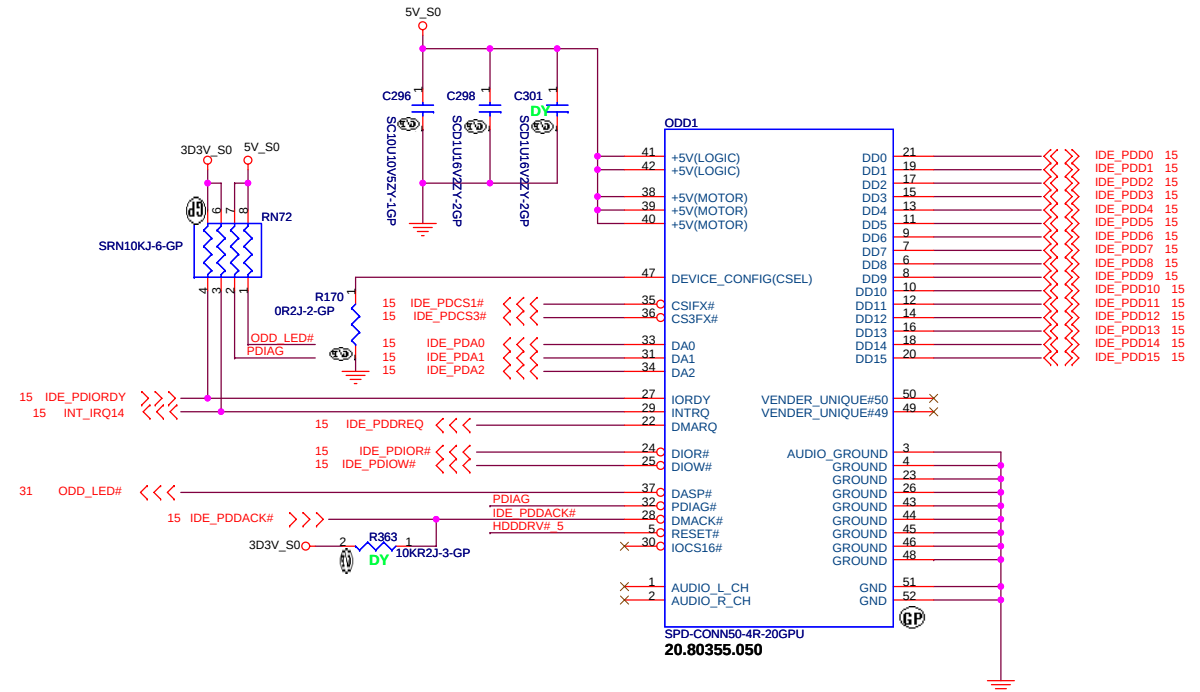
SMBUS



## SATA HD Connector



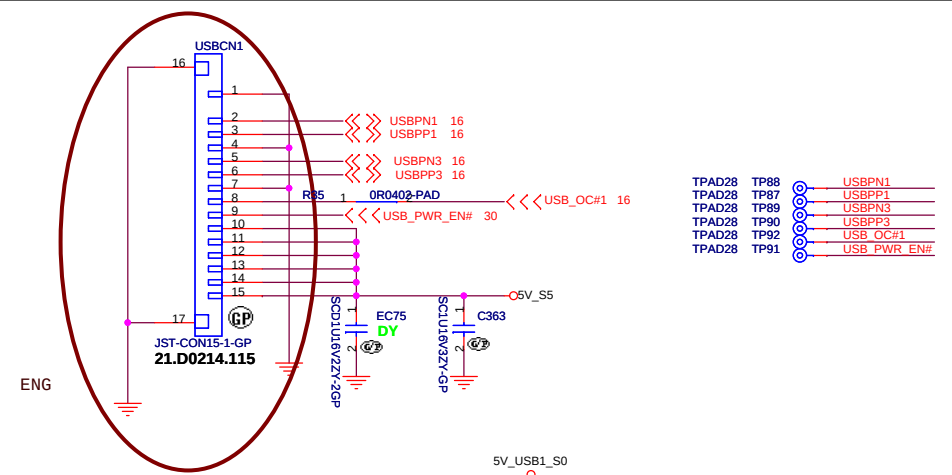
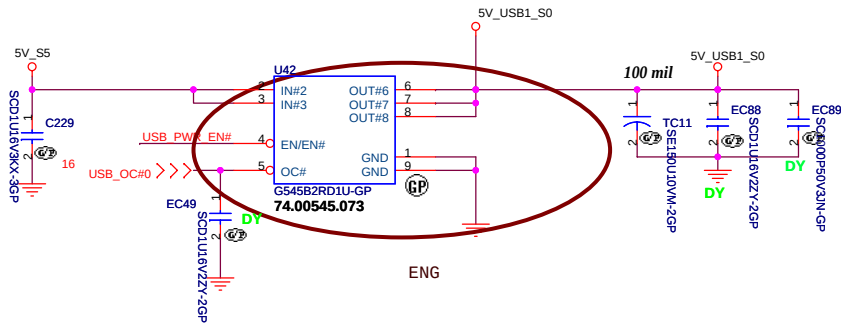
## ODD Connector



<Core Design>

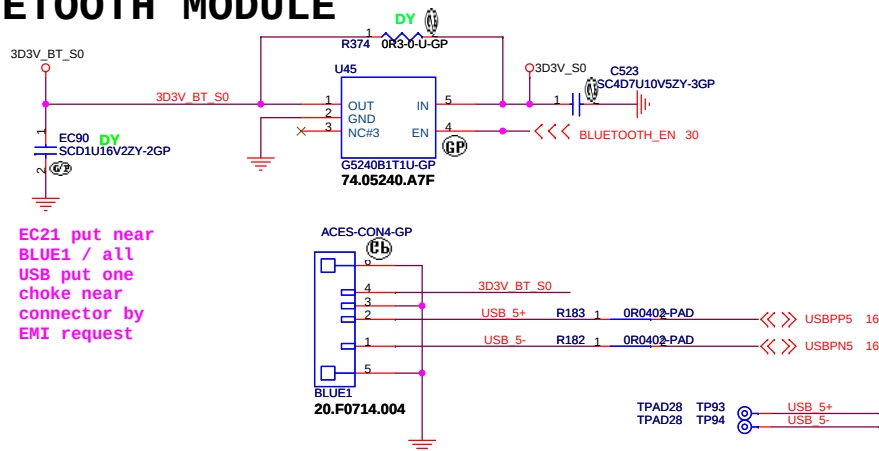
**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

|               |                        |                |     |
|---------------|------------------------|----------------|-----|
| Title         |                        |                |     |
| HDD and CDROM |                        |                |     |
| Size          | Document Number        |                | Rev |
|               | HURON                  |                | SD  |
| Date:         | Monday, March 12, 2007 | Sheet 20 of 44 |     |

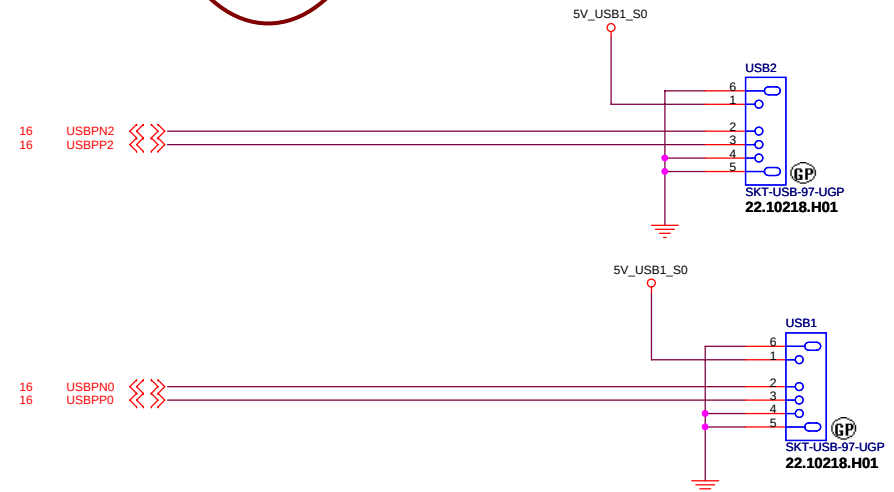
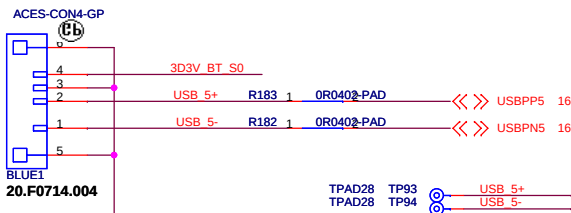


|        |      |             |
|--------|------|-------------|
| TPAD28 | TP88 | USBPN1      |
| TPAD28 | TP87 | USBPP1      |
| TPAD28 | TP89 | USBPN3      |
| TPAD28 | TP90 | USBPP3      |
| TPAD28 | TP92 | USB_OC#1    |
| TPAD28 | TP91 | USB_PWR_EN# |

## BLUETOOTH MODULE



EC21 put near  
BLUE1 / all  
USB put one  
choke near  
connector by  
EMI request



<Core Design>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**USB / BLUETOOTH**

Size

Document Number

**HURON**

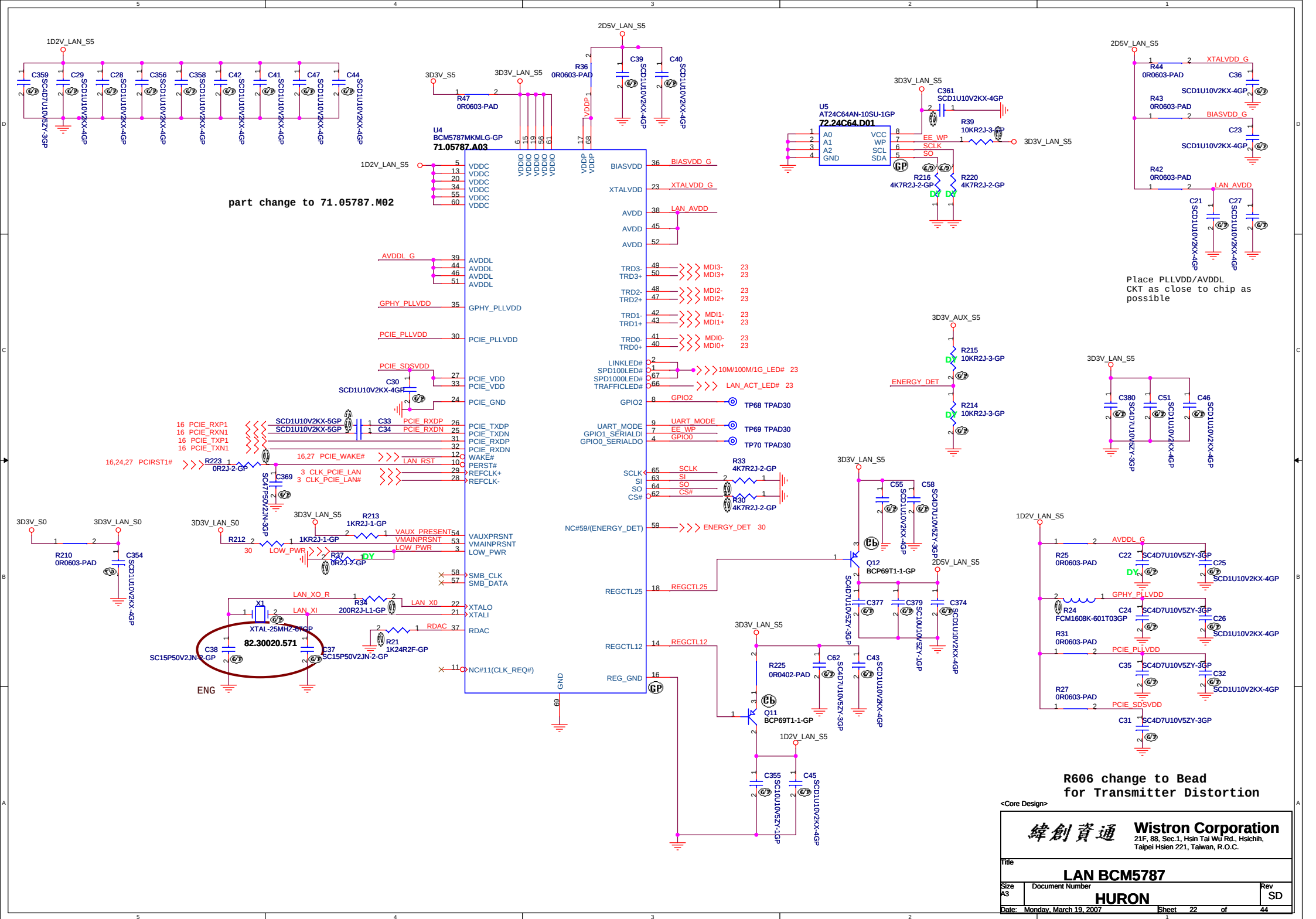
Rev

**SD**

Date: Tuesday, March 13, 2007

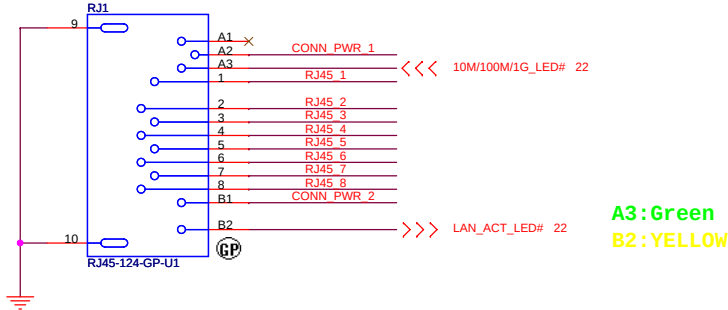
Sheet 21

of 44



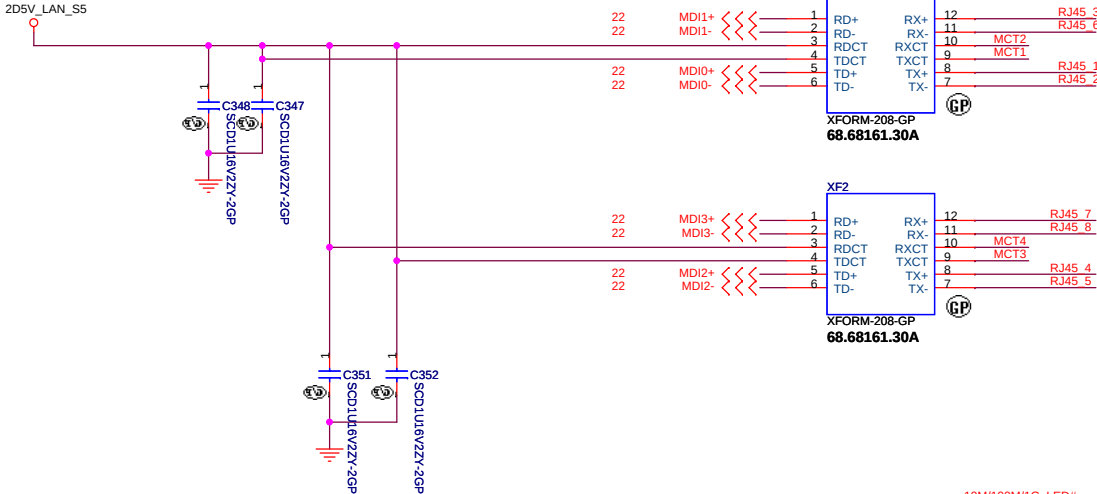
| Voltage Rail | 4401E       | 5789        | 5787       |
|--------------|-------------|-------------|------------|
| VDDIO_PCI    | 3D3V_LAN_S5 | 3D3V_S0     | Don't Care |
| VDDC         | 1D8V_LAN_S5 | 1D2V_LAN_S5 |            |
| VDDIO        | 3D3V_LAN_S5 | 3D3V_LAN_S5 |            |
| VESD         | 3D3V_LAN_S5 | 3D3V_S0     | Don't Care |
| VDDP         | Don't Care  | 2D5V_S5     |            |
| 3D3V_2D5V_S5 | 3D3V_S5     | 2D5V_S5     |            |
| 1D8V_1D2V_S5 | 1D8V_LAN_S5 | 1D2V_S5     |            |

LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits  
LAN Data: Yellow(B2), when LAN is transferring data.

GIGA Lan Transformer

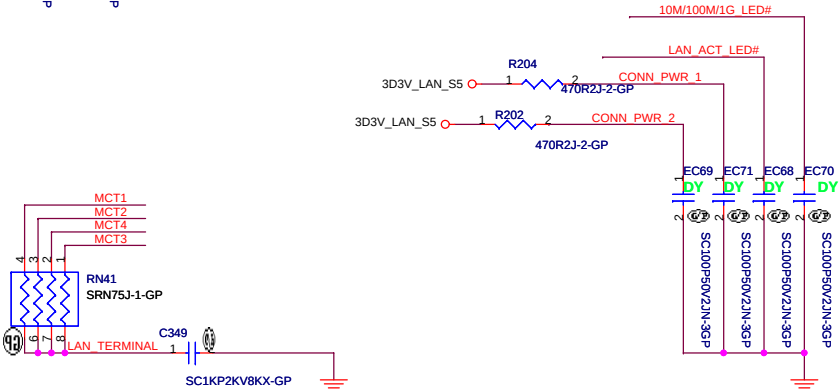


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC\_TIP,DOC\_RING,TIP,RING:  
W/S : 10/100 @ Surface layers  
10/20 @ Inner layers

| 10/100 LAN Transformer | RJ45 PIN |
|------------------------|----------|
| TD+ --> TX+            | RJ45-1   |
| TD- --> TX-            | RJ45-2   |
| RD+ --> RX+            | RJ45-3   |
| RD- --> RX-            | RJ45-6   |

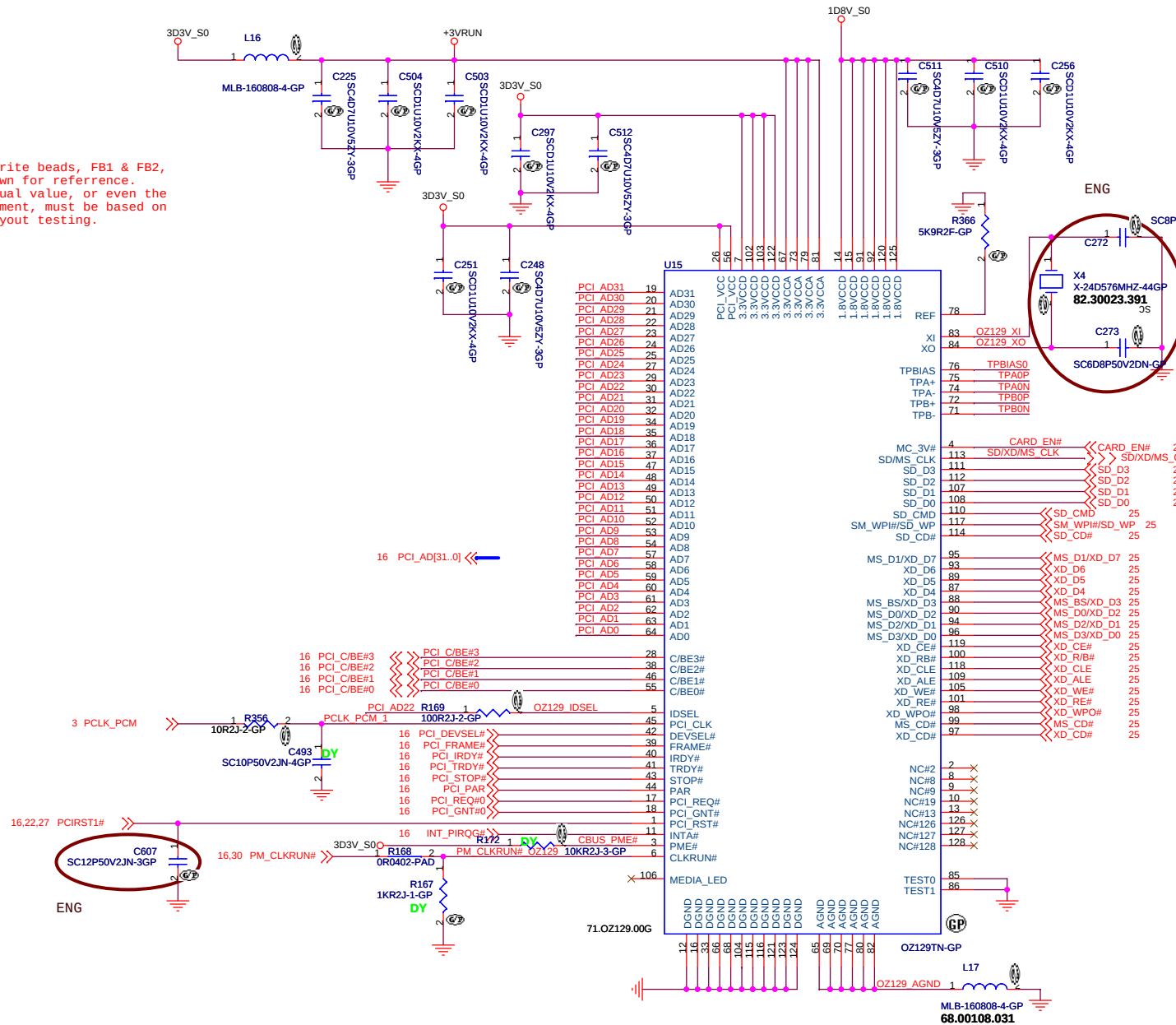


<Core Design>

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Title: **LAN Connector**

|                              |                              |               |
|------------------------------|------------------------------|---------------|
| Size A3                      | Document Number <b>HURON</b> | Rev <b>SD</b> |
| Date: Monday, March 19, 2007 | Sheet 23 of 44               |               |



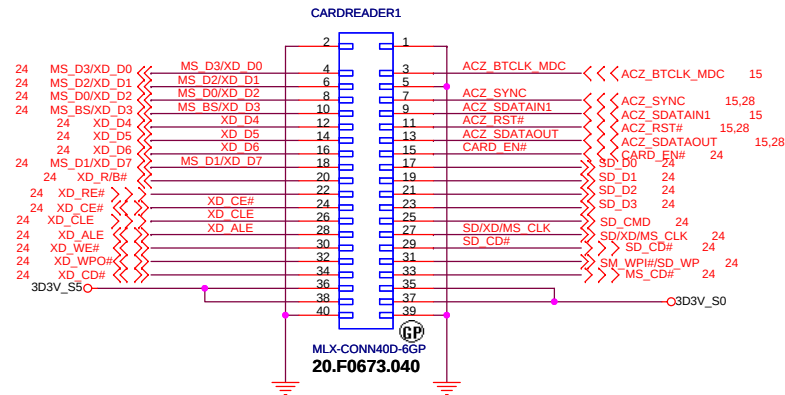
with a differential in  
(Zo) of 110ohms.

TPB1A0  
TPA0P  
TPA0N  
TPB0P  
TPB0N

25  
25  
25  
25  
25

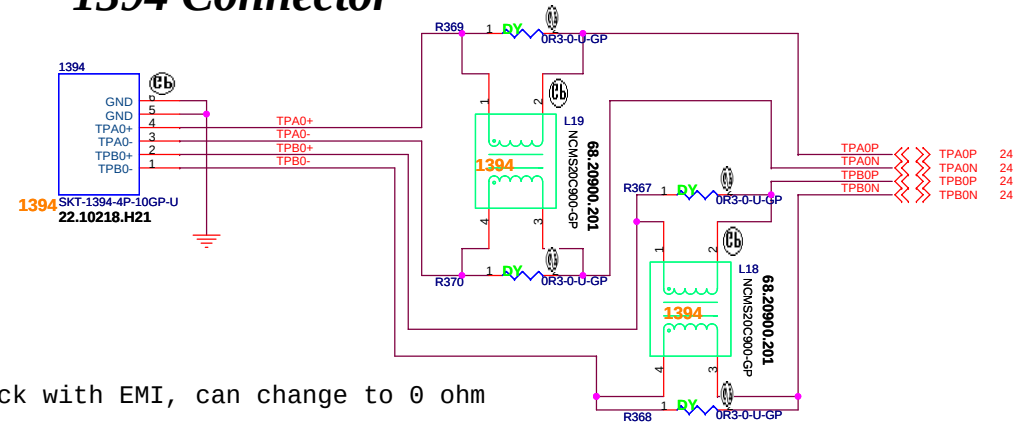
25

|        |                        |  |                |
|--------|------------------------|--|----------------|
| Title  |                        |  |                |
| OZ129T |                        |  |                |
| Size   | Document Number        |  | Rev            |
|        | HURON                  |  | SD             |
| Date:  | Monday, March 19, 2007 |  | Sheet 24 of 44 |



CONN on Bottom side

## 1394 Connector



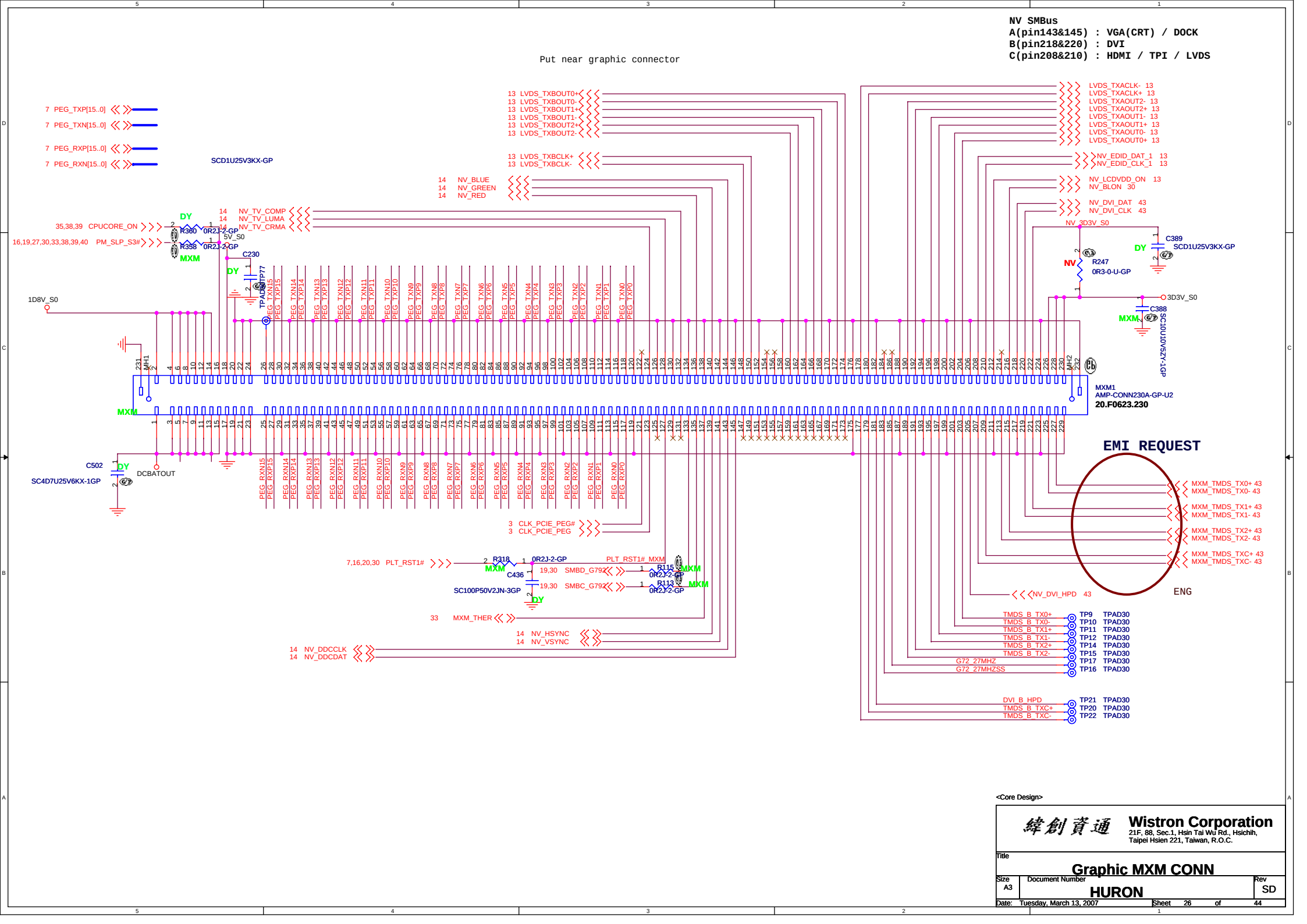
check with EMI, can change to 0 ohm

<Core Design>

緯創資通

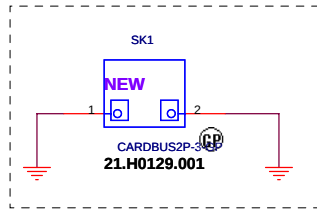
**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

|                               |                 |          |
|-------------------------------|-----------------|----------|
| Title                         |                 |          |
| 1394 / CARD READER BD         |                 |          |
| Size                          | Document Number | Rev      |
|                               | HURON           | SD       |
| Date: Tuesday, March 13, 2007 | Sheet           | 25 of 44 |

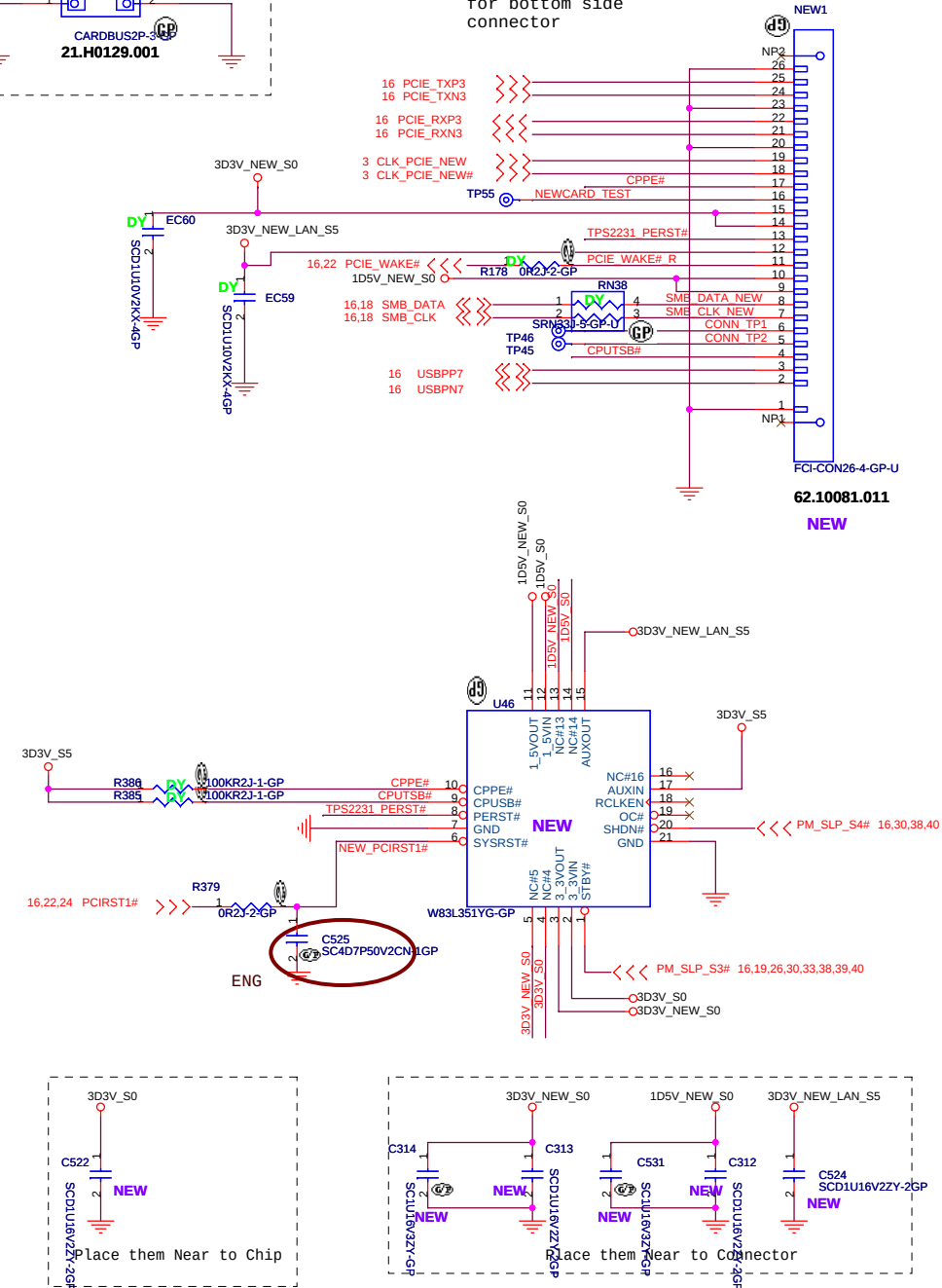


NV SMBus  
A(pin143&145) : VGA(CRT) / DOCK  
B(pin218&220) : DVI  
C(pin208&210) : HDMI / TPI / LVDS

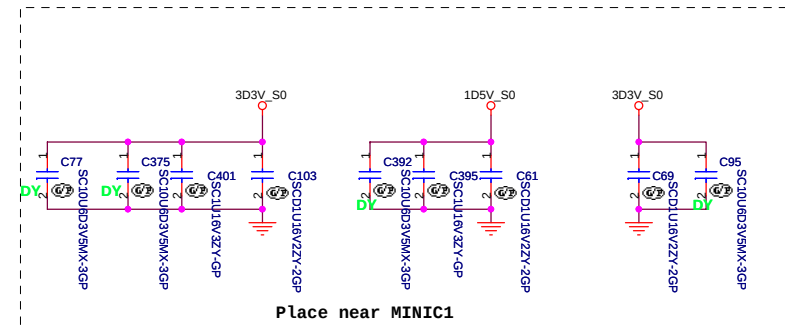
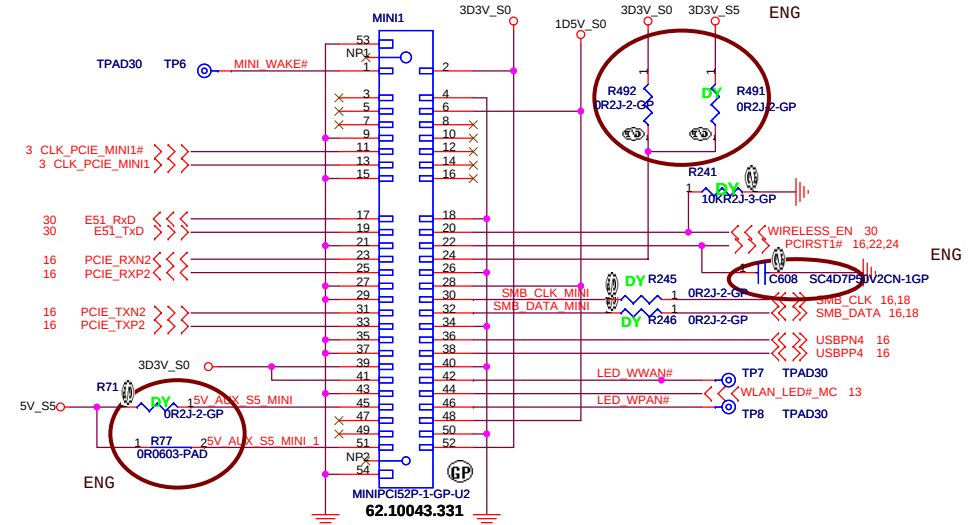
## NEWCARD Connector



Reserve the symbol  
for bottom side  
connector



## Mini Card Connector



<Core Design>

緯創資通

**Wistron Corporation**  
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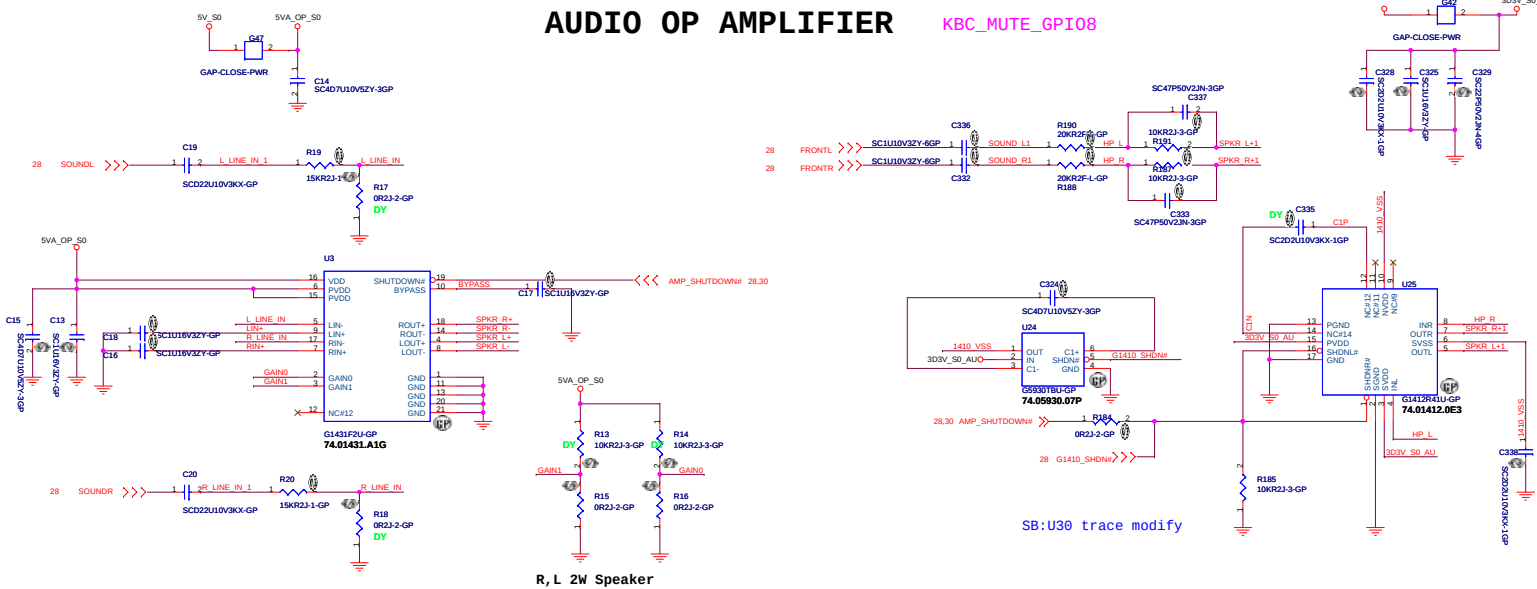
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

|                             |                           |       |           |
|-----------------------------|---------------------------|-------|-----------|
| Title                       |                           |       |           |
| <b>MINI CARD / NEW CARD</b> |                           |       |           |
| Size                        | Document Number           |       | Rev       |
|                             | <b>HURON</b>              |       | <b>SD</b> |
| Date:                       | Wednesday, March 14, 2007 | Sheet | 27 of 44  |



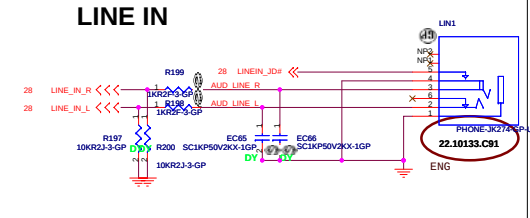
## AUDIO OP AMPLIFIER

KBC\_MUTE\_GPI08

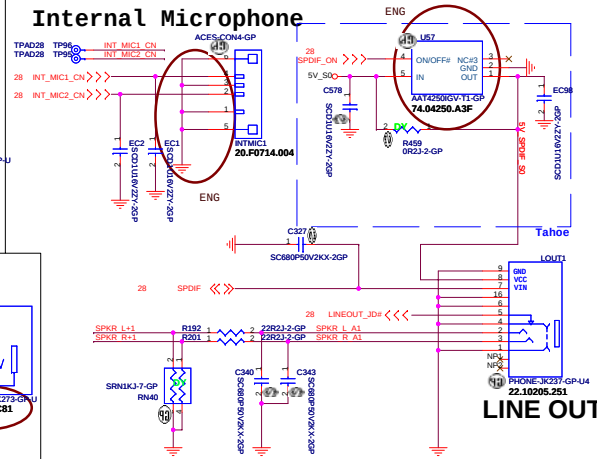


R, L 2W Speaker

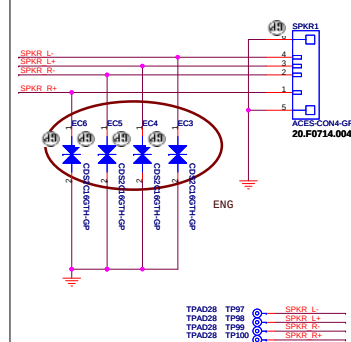
**LINE IN**



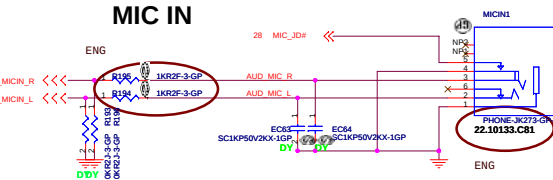
## Internal Microphone



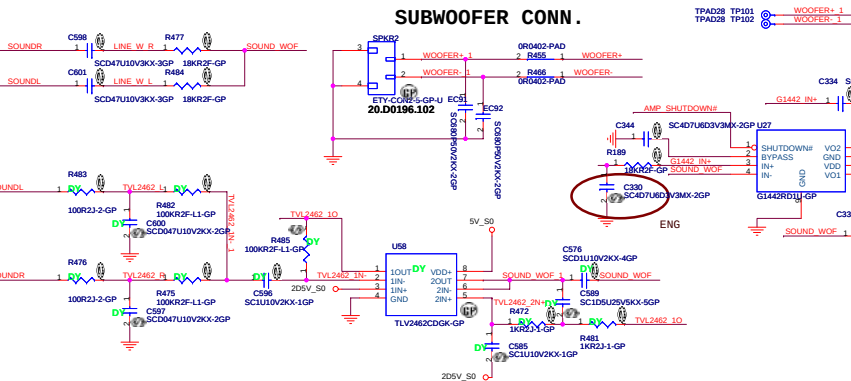
## Internal Speaker



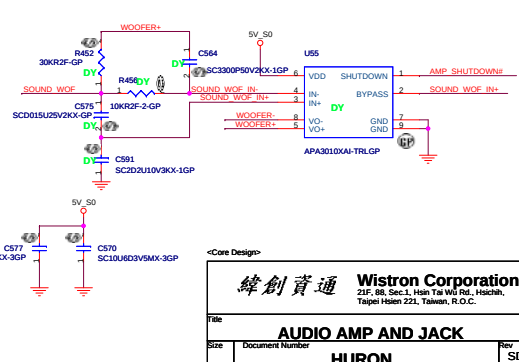
**MIC IN**

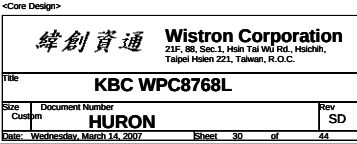


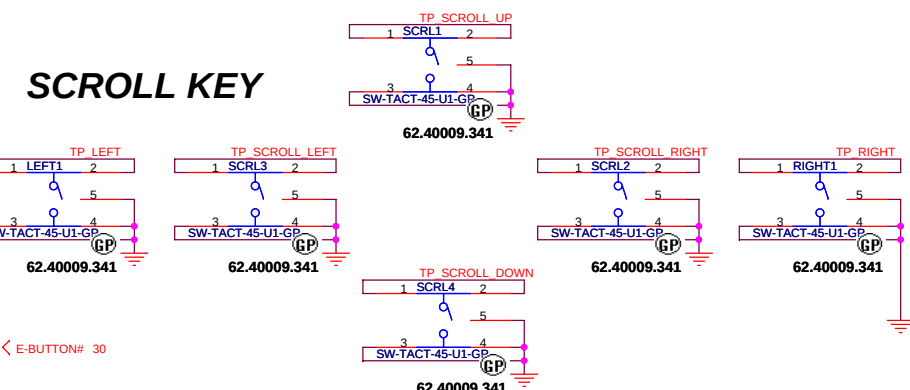
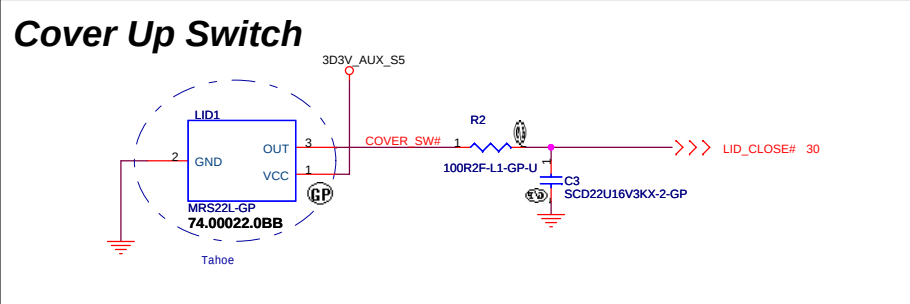
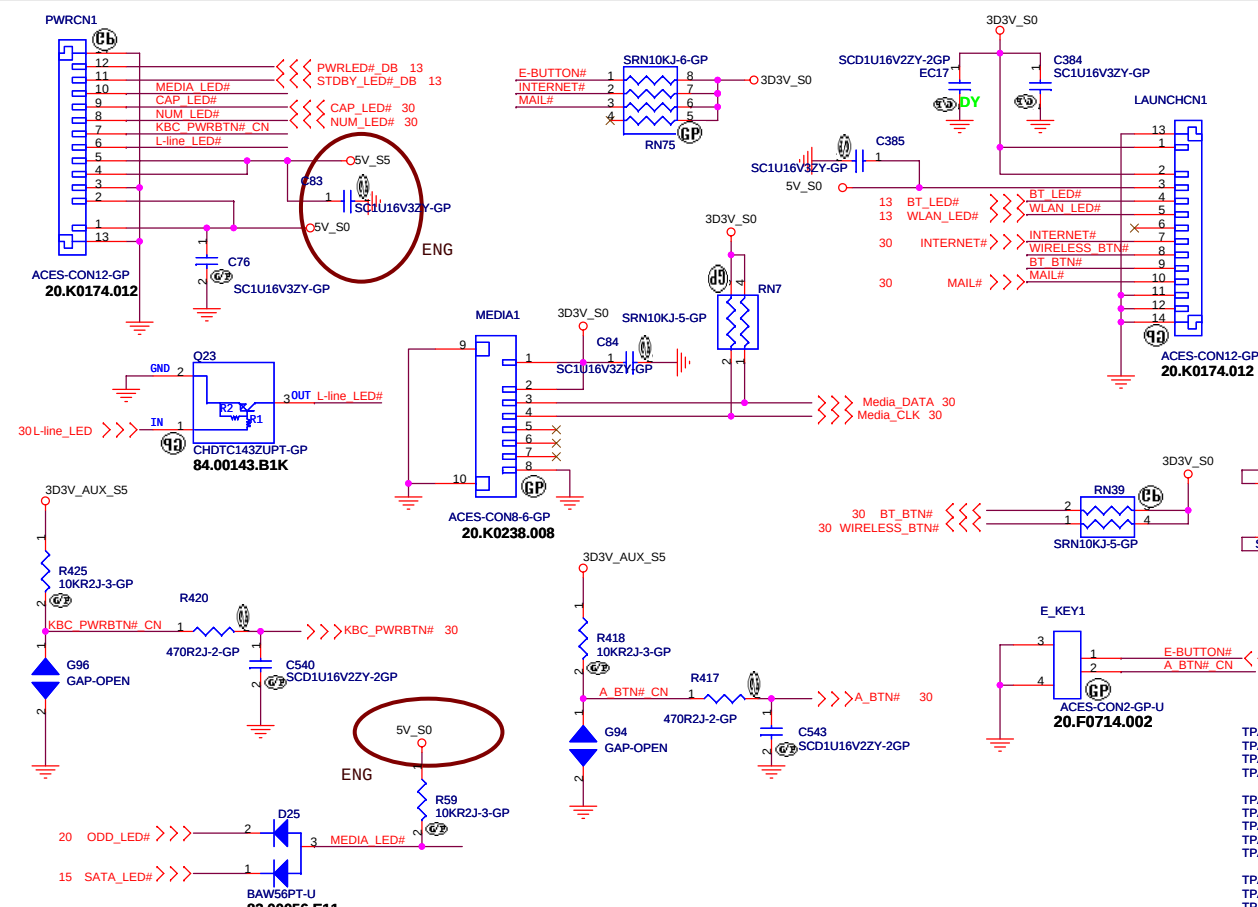
**SUBWOOFER CONN.**



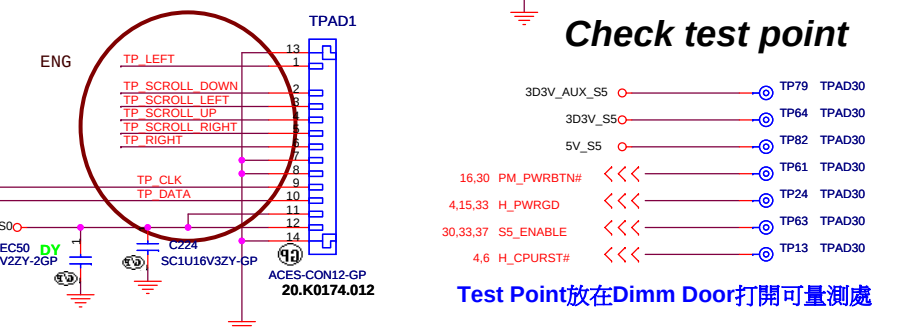
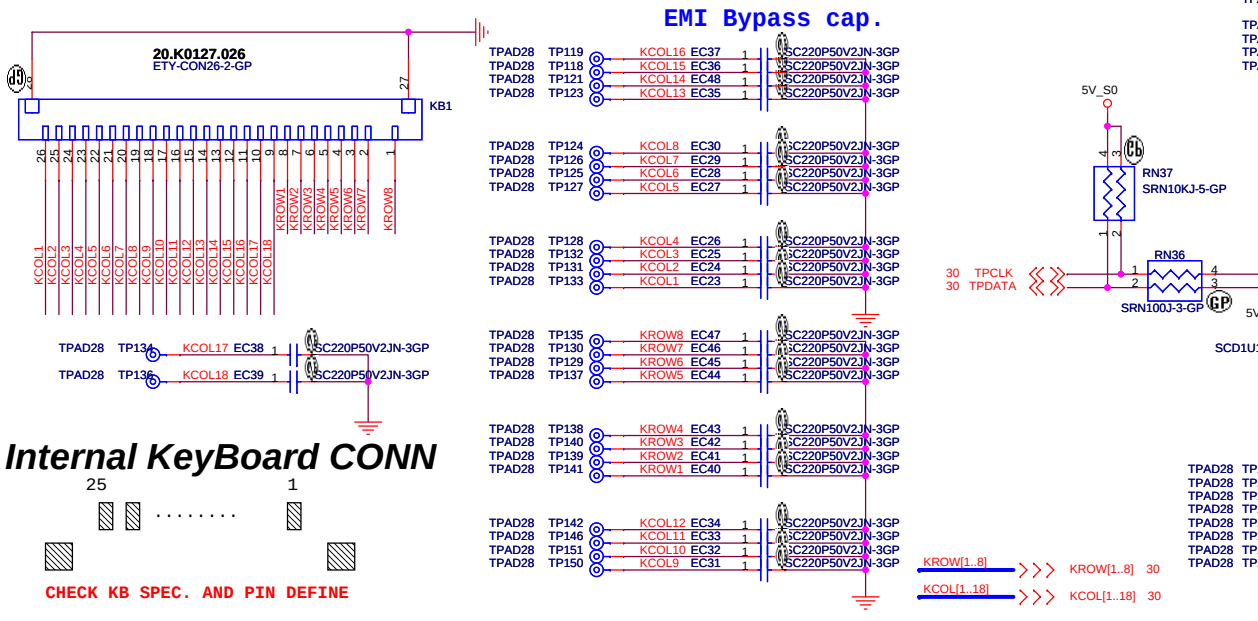
**SUBWOOFER AMP.**







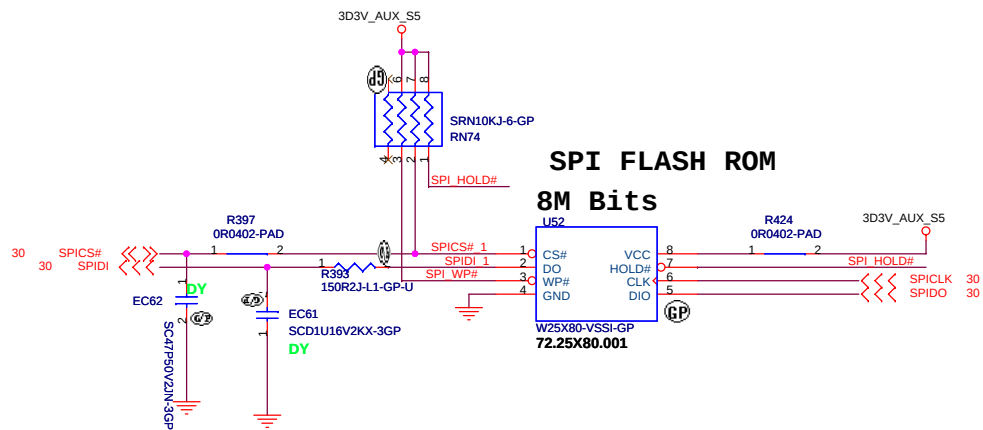
|        |       |                |                  |       |
|--------|-------|----------------|------------------|-------|
| TPAD28 | TP103 | MAIL#          | SC100P50V2JN-3GP | EC86  |
| TPAD28 | TP105 | INTERNET#      | SC100P50V2JN-3GP | EC85  |
| TPAD28 | TP104 | WLAN_LED#      | SC100P50V2JN-3GP | EC82  |
| TPAD28 | TP106 | BT_LED#        | SC100P50V2JN-3GP | EC83  |
| TPAD28 | TP108 | MEDIA_LED#     | SC100P50V2JN-3GP | EC18  |
| TPAD28 | TP110 | STDBY_LED# DB  | SC100P50V2JN-3GP | EC77  |
| TPAD28 | TP109 | A_BTN# CN      | SC100P50V2JN-3GP | EC8   |
| TPAD28 | TP111 | E-BUTTON#      | SC100P50V2JN-3GP | EC7   |
| TPAD28 | TP113 | L-line_LED#    | SC100P50V2JN-3GP | EC81  |
| TPAD28 | TP112 | KBC_PWRBTN# CN | SC100P50V2JN-3GP | EC78  |
| TPAD28 | TP115 | NUM_LED#       | SC100P50V2JN-3GP | EC79  |
| TPAD28 | TP114 | CAP_LED#       | SC100P50V2JN-3GP | EC80  |
| TPAD28 | TP116 | Media_DATA     | SC100P50V2JN-3GP | EC100 |
| TPAD28 | TP117 | Media_CLK      | SC100P50V2JN-3GP | EC99  |
| TPAD28 | TP120 | WIRELESS_BTN#  | SCD1U16V2ZY-2GP  | EC93  |
| TPAD28 | TP122 | BT_BTN#        | SCD1U16V2ZY-2GP  | EC95  |



**Internal Keyboard CONN**

25 1

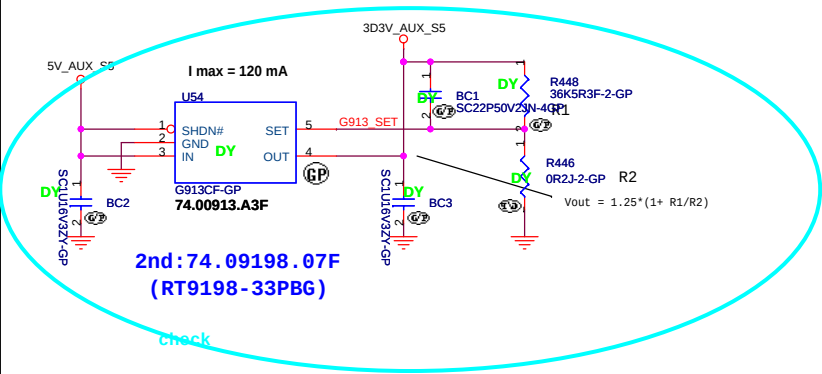
CHECK KB SPEC. AND PIN DEFINE



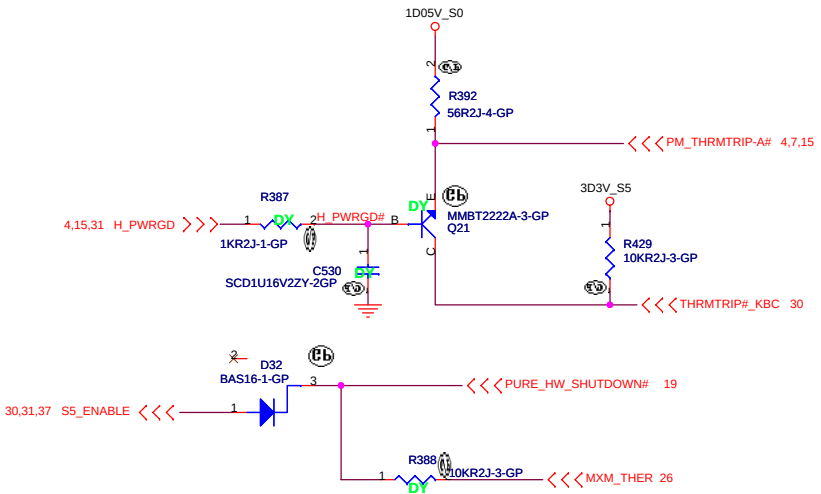
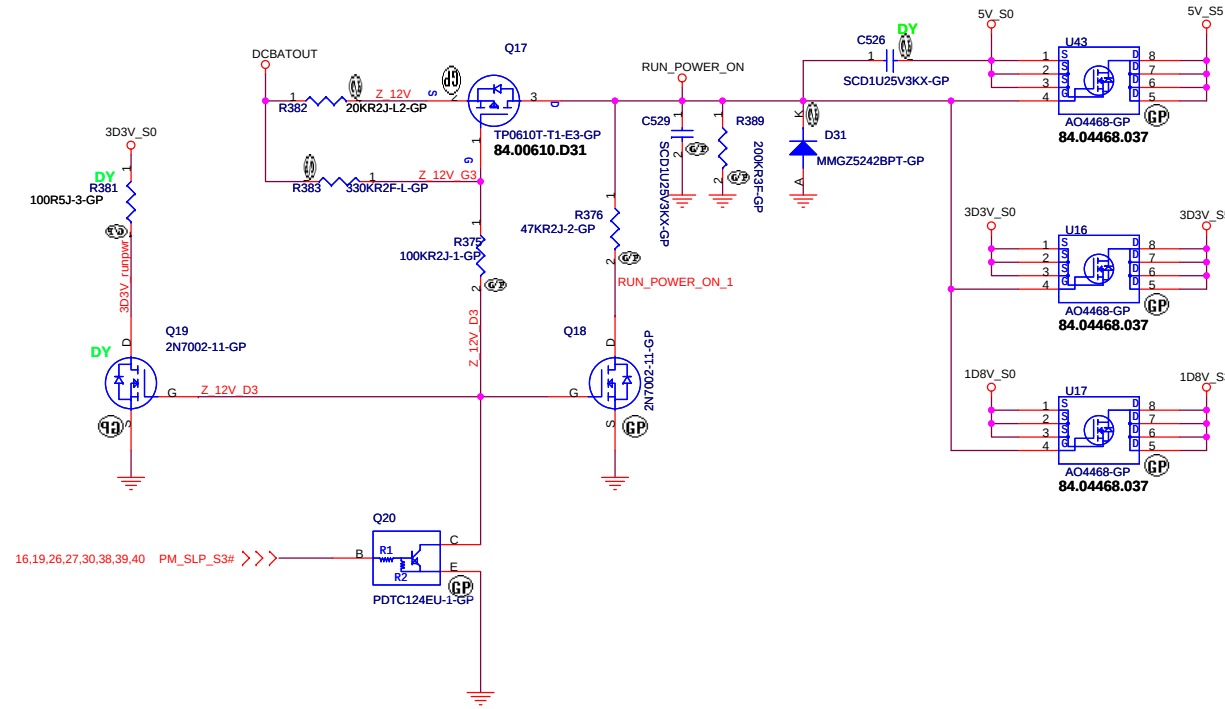
<Core Design>

|                              |                                 |                                                                                                             |           |
|------------------------------|---------------------------------|-------------------------------------------------------------------------------------------------------------|-----------|
| <b>緯創資通</b>                  |                                 | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |           |
| Title                        |                                 |                                                                                                             |           |
| <b>BIOS</b>                  |                                 |                                                                                                             |           |
| Size<br>A3                   | Document Number<br><b>HURON</b> |                                                                                                             | Rev<br>SD |
| Date: Monday, March 12, 2007 | Sheet 32                        | of 44                                                                                                       |           |

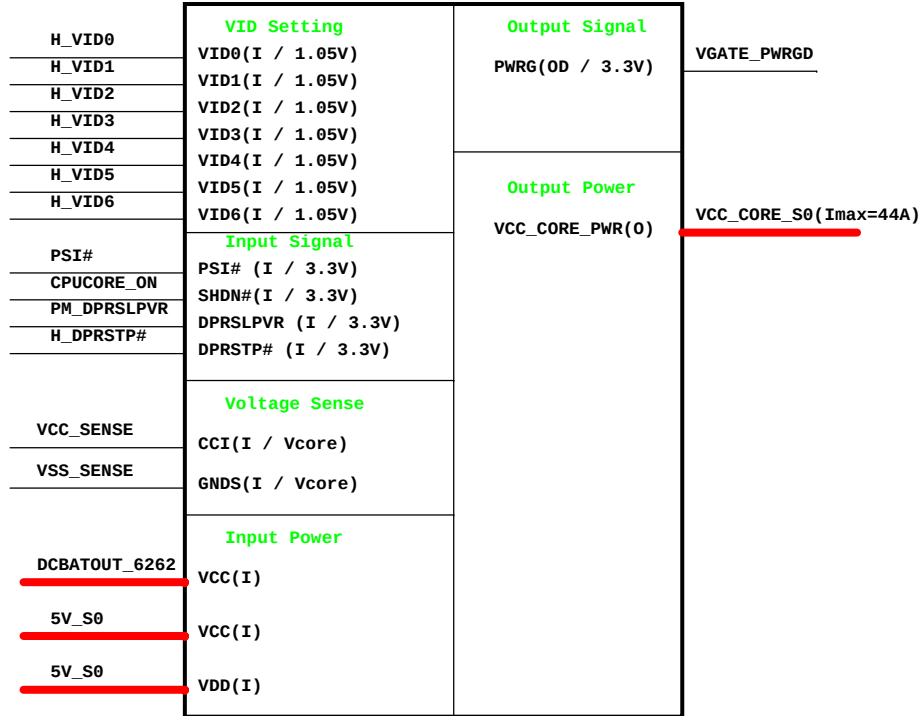
Aux Power 3D3V\_AUX\_S5



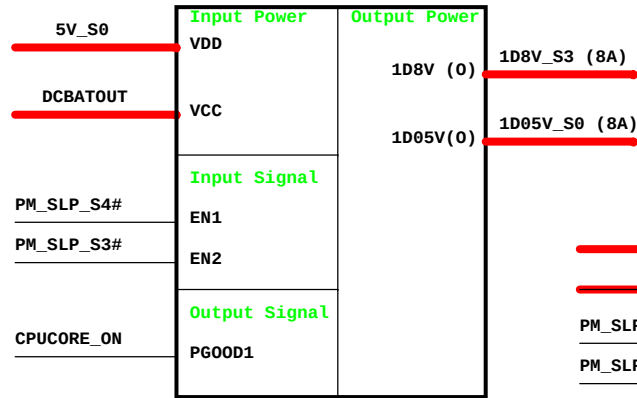
Run Power



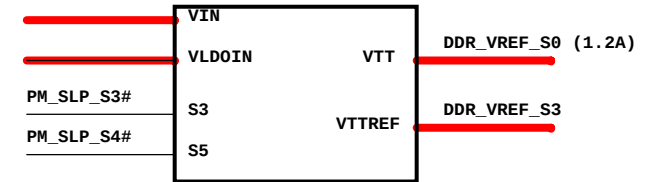
CPU\_CORE  
ISL6262



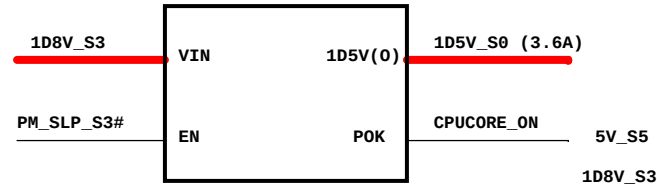
TPS51124  
1D8V\_S3 / 1D05V\_S0



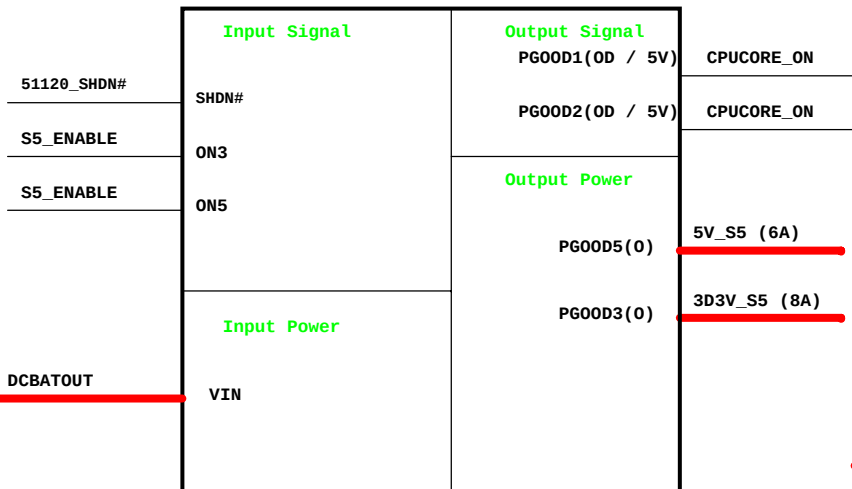
TPS51100  
DDR\_VREF\_S0



API5912  
1D5V\_S0



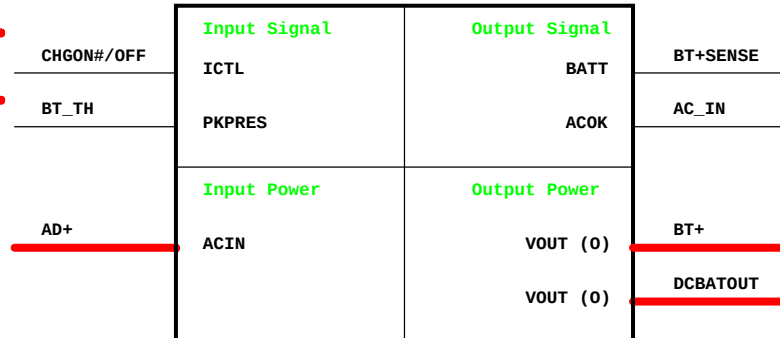
TPS51120  
5V\_S5 / 3D3V\_S5



APL5308  
2D5V\_S0

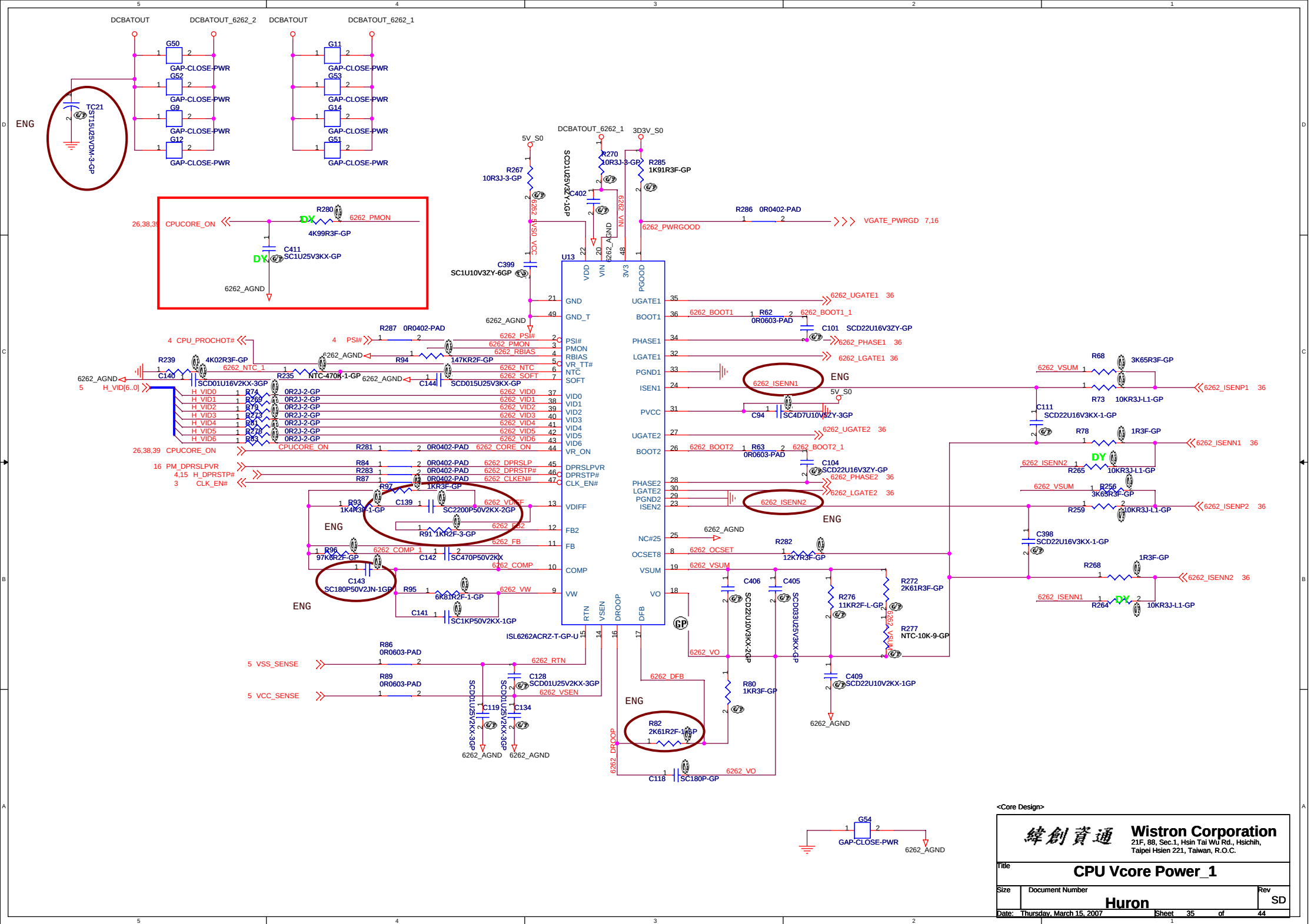


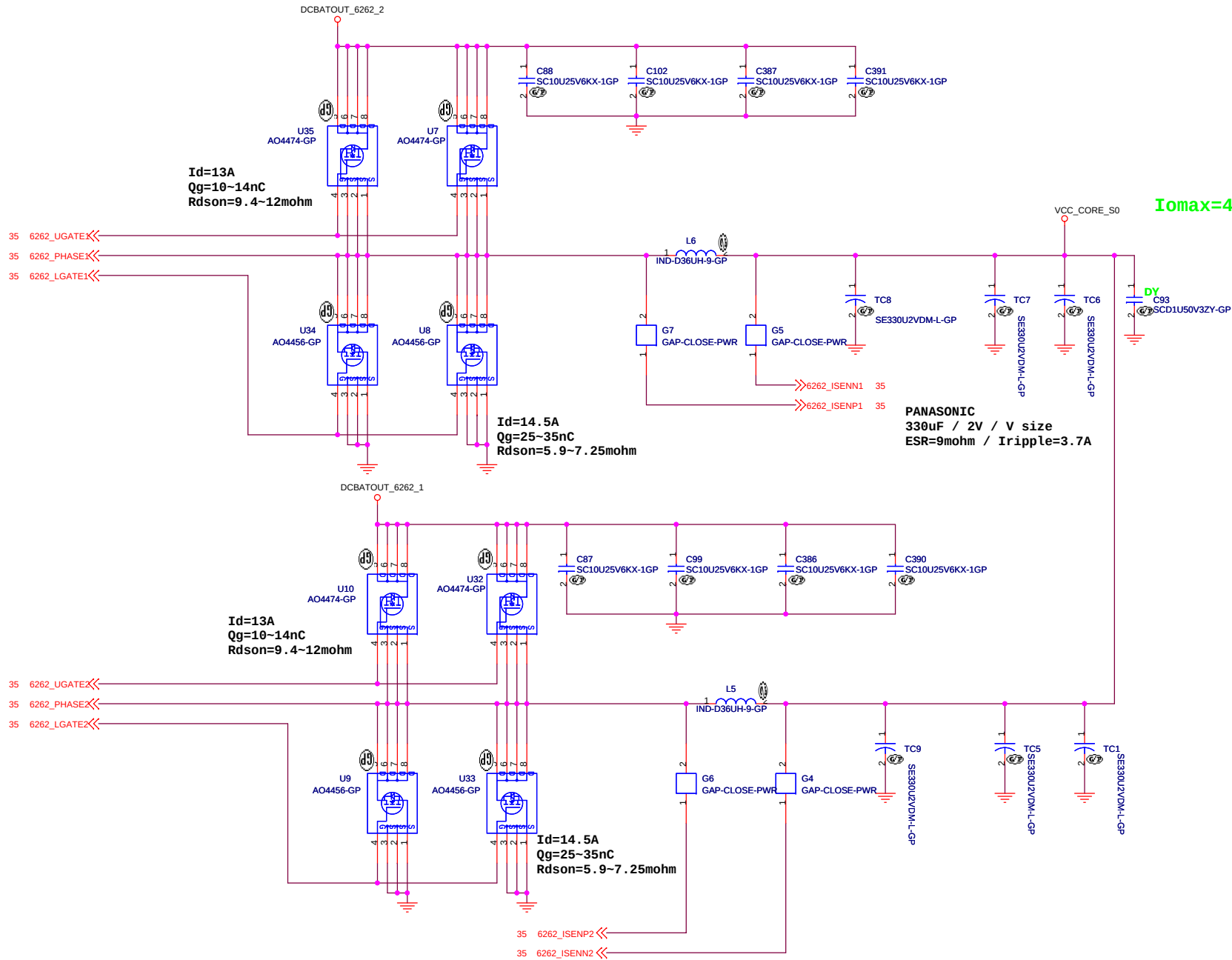
Charger MAX8731A



<Core Design>

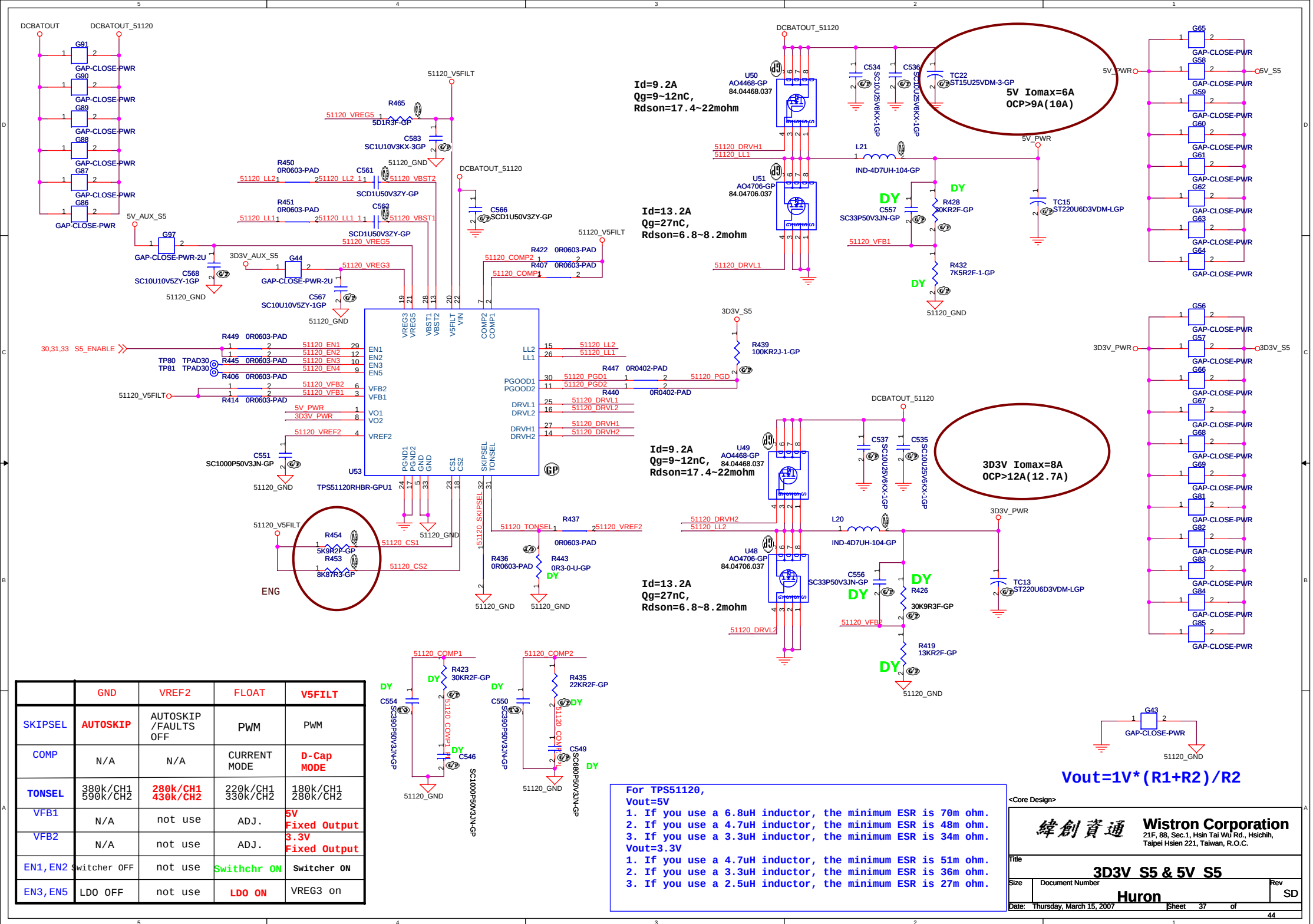
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|----------------------------|------------------------|-------------------------------------------------------------------------------|------------------|
| <b>緯創資通</b>                |                        | <b>Wistron Corporation</b>                                                    |                  |
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| Title                      |                        |                                                                               |                  |
| <b>Power Block Diagram</b> |                        |                                                                               |                  |
| Size<br>A3                 | Document Number        |                                                                               | Rev<br><b>SD</b> |
| <b>Huron</b>               |                        |                                                                               |                  |
| Date:                      | Monday, March 12, 2007 | Sheet 34 of 44                                                                |                  |



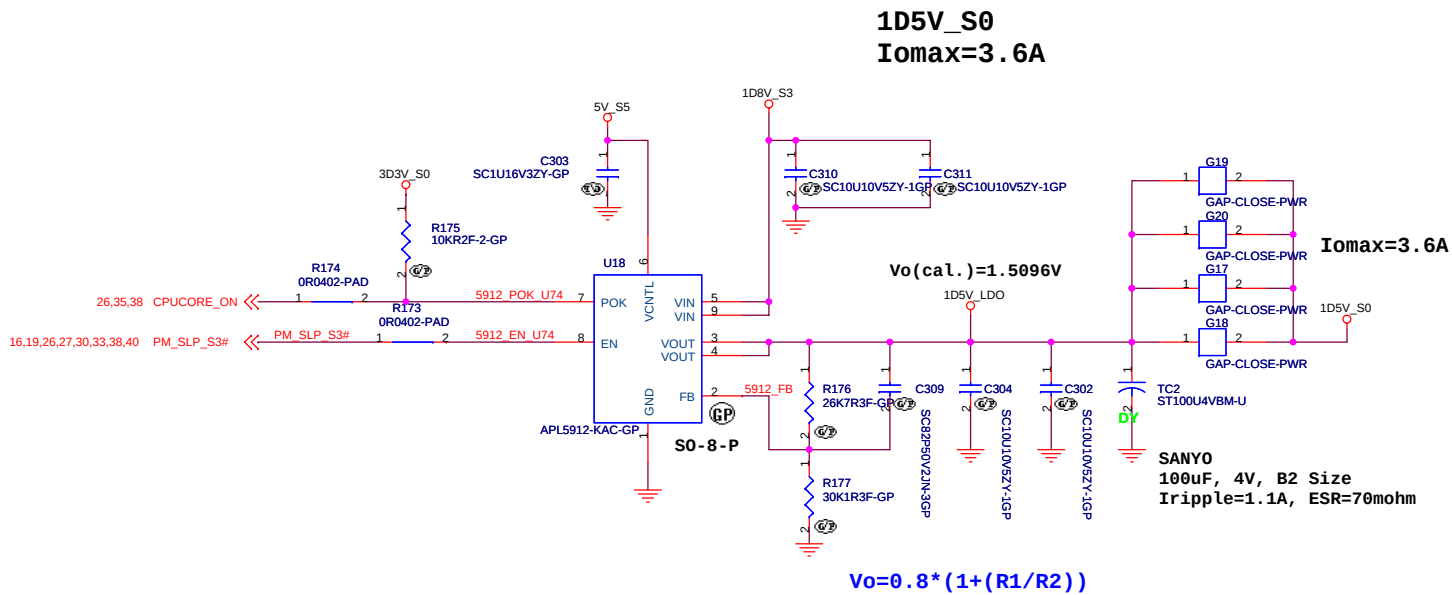


**Iomax=44A**

**PANASONIC**  
**330uF / 2V / V size**  
**ESR=9mohm / Iripple=3.7A**

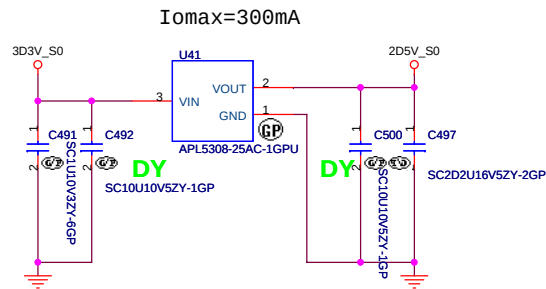
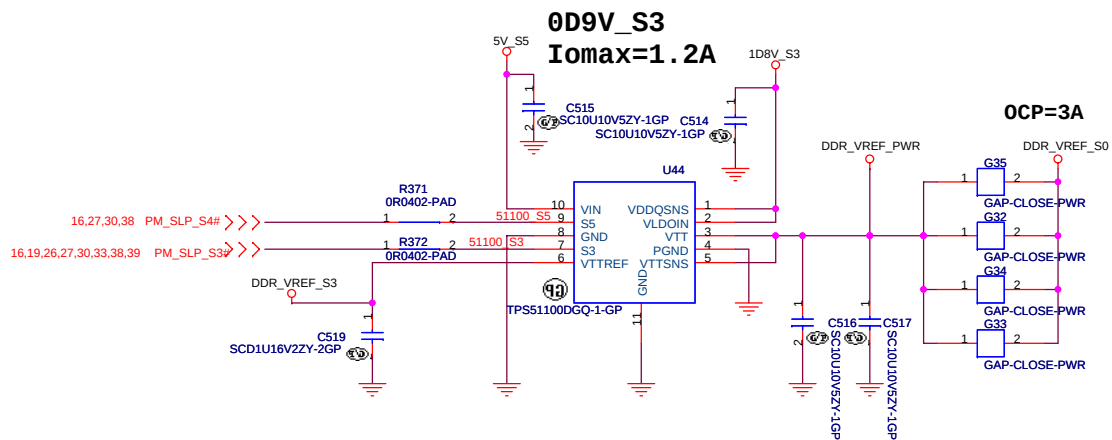






<Core Design>

|                                 |                                 |                                                                                                             |           |
|---------------------------------|---------------------------------|-------------------------------------------------------------------------------------------------------------|-----------|
| <b>緯創資通</b>                     |                                 | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |           |
| Title <b>APL5912_1D5V</b>       |                                 |                                                                                                             |           |
| Size<br>A3                      | Document Number<br><b>Huron</b> |                                                                                                             | Rev<br>SD |
| Date: Wednesday, March 14, 2007 | Sheet 39 of 44                  |                                                                                                             |           |

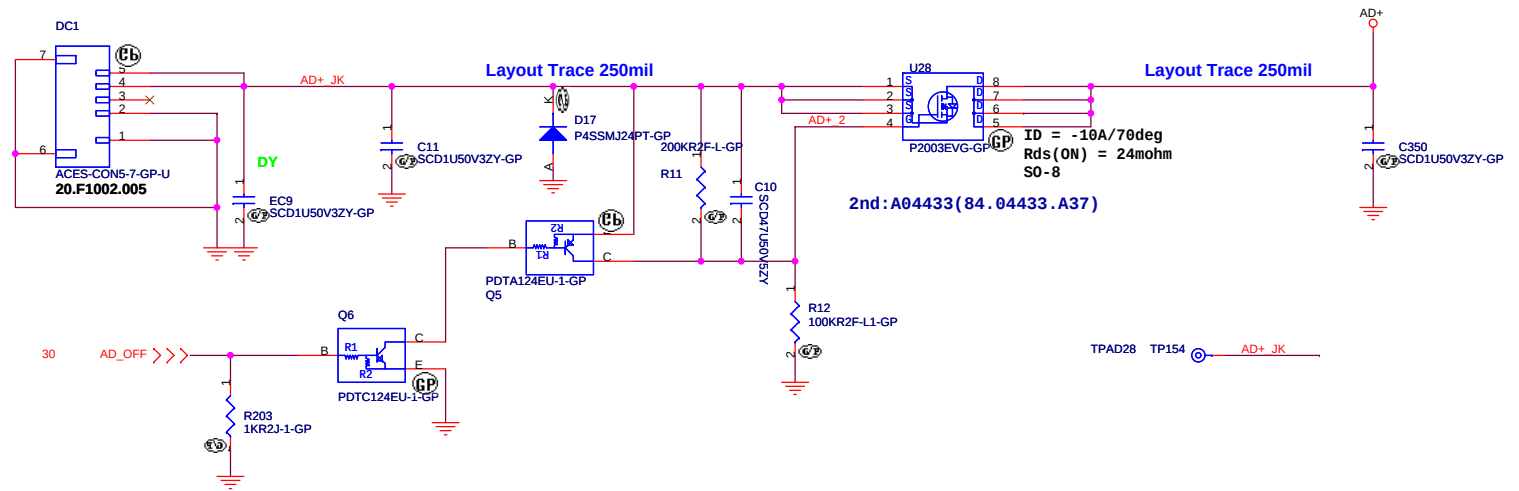


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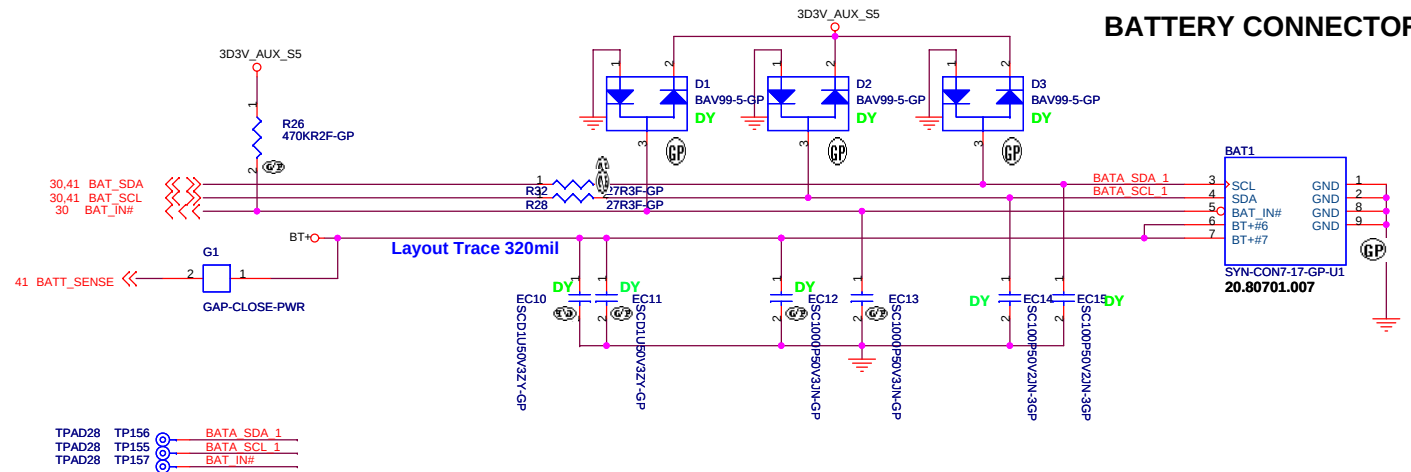
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|------------------------------|---------------------------------|-------------------------------------------------------------------------------------------------------------|-----------|
| <b>緯創資通</b>                  |                                 | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |           |
| Title <b>0D9V/2D5V</b>       |                                 |                                                                                                             |           |
| Size<br>A3                   | Document Number<br><b>Huron</b> |                                                                                                             | Rev<br>SD |
| Date: Monday, March 12, 2007 |                                 | Sheet 40 of 44                                                                                              |           |



## Adaptor in to generate DCBATOUT



## BATTERY CONNECTOR



**<Core Design>**

**緯創資通** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

| Title | Author | Date | Page | Page | Page | Page | Page | Page | Page | Page | Page | Page |
|-------|--------|------|------|------|------|------|------|------|------|------|------|------|
| Title | Author | Date | Page | Page | Page | Page | Page | Page | Page | Page | Page | Page |

### AD/BATT CONN

Size  
A

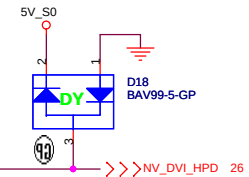
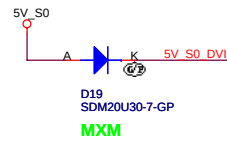
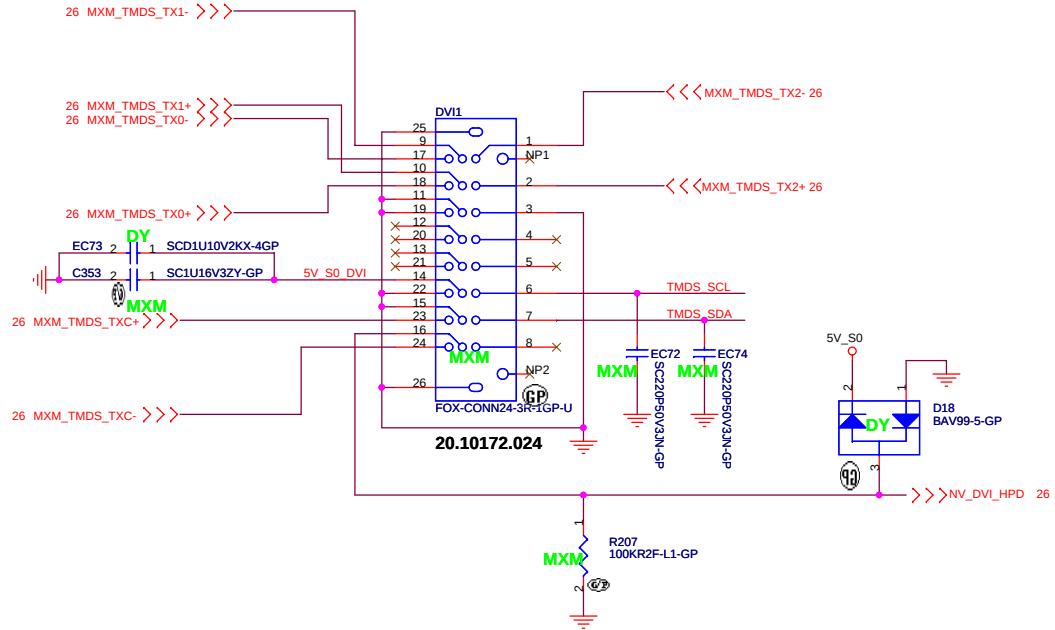
|  |                 |
|--|-----------------|
|  | Document Number |
|--|-----------------|

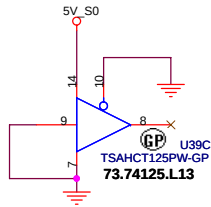
## HURON

Date: Monday, March 12, 2007

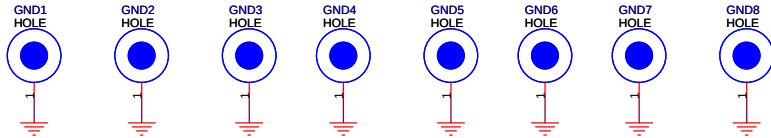
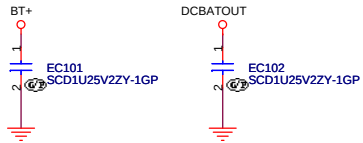
|       |    |    |    |
|-------|----|----|----|
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|-------|----|----|----|

Rev  
SD

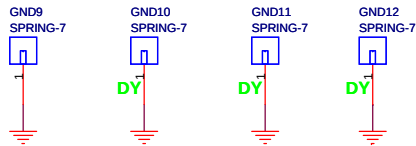




ENG



Spring



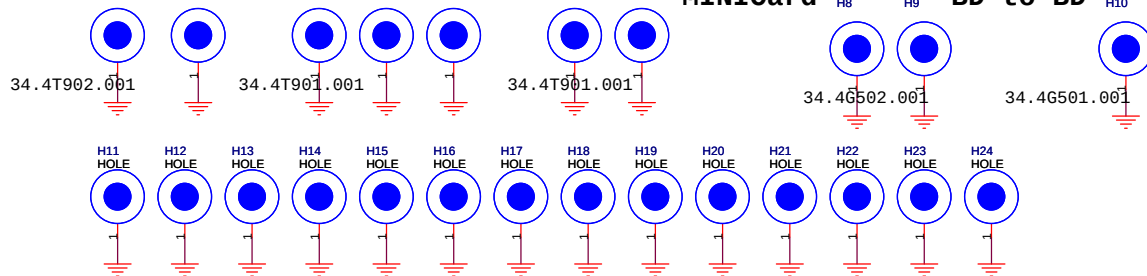
MXM

CPU

NB

MINICard

BD to BD



<Core Design>

|                 |                          |                                                                               |          |
|-----------------|--------------------------|-------------------------------------------------------------------------------|----------|
| 緯創資通            |                          | Wistron Corporation                                                           |          |
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| Title           |                          |                                                                               |          |
| EMI/Spring/Boss |                          |                                                                               |          |
| Size            | Document Number          |                                                                               | Rev      |
|                 | HURON                    |                                                                               | SD       |
| Date:           | Thursday, March 15, 2007 | Sheet                                                                         | 44 of 44 |