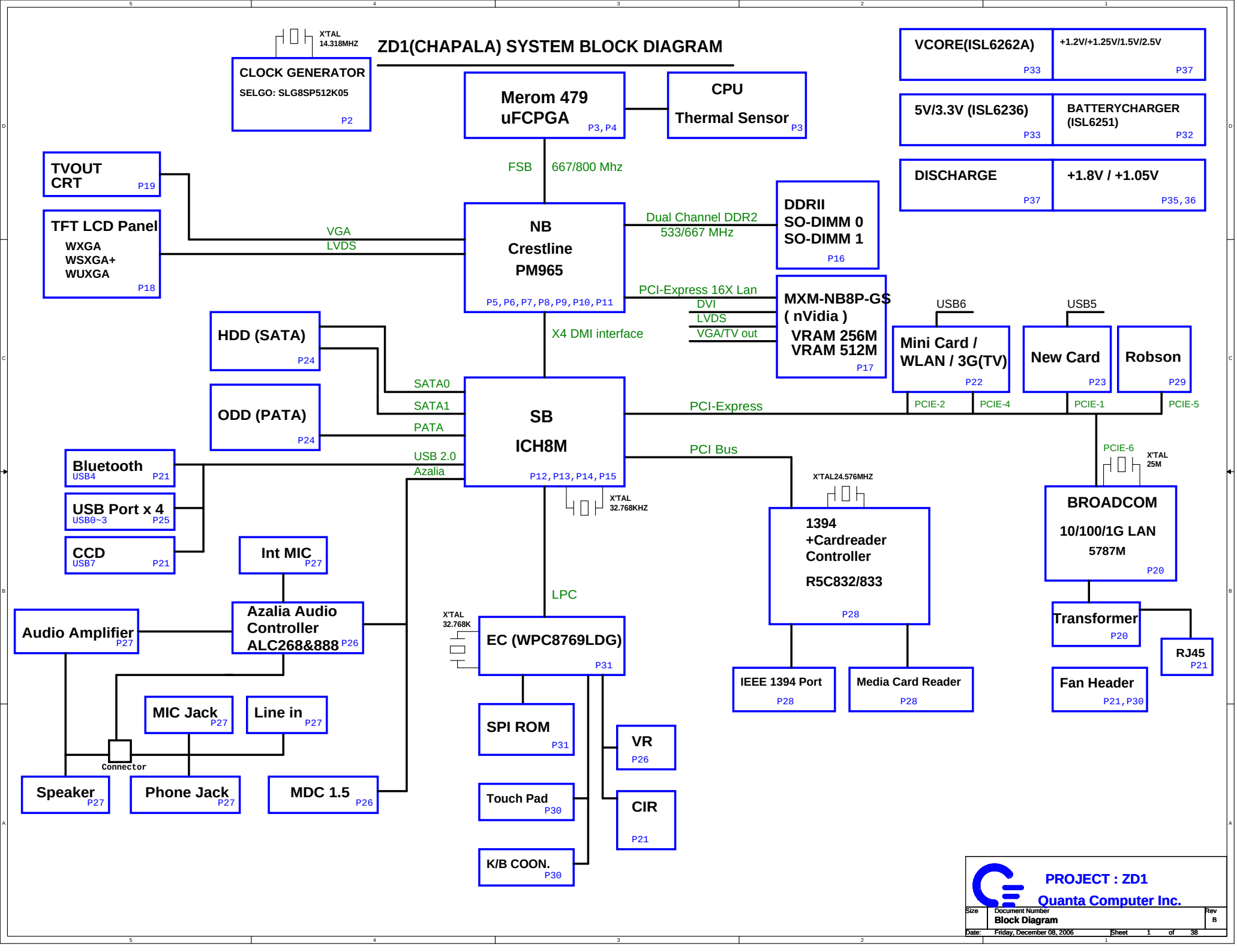
ZD1(CHAPALA) SYSTEM BLOCK DIAGRAM



PROJECT : ZD1

Quanta Computer Inc.

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	Block Diagram	B

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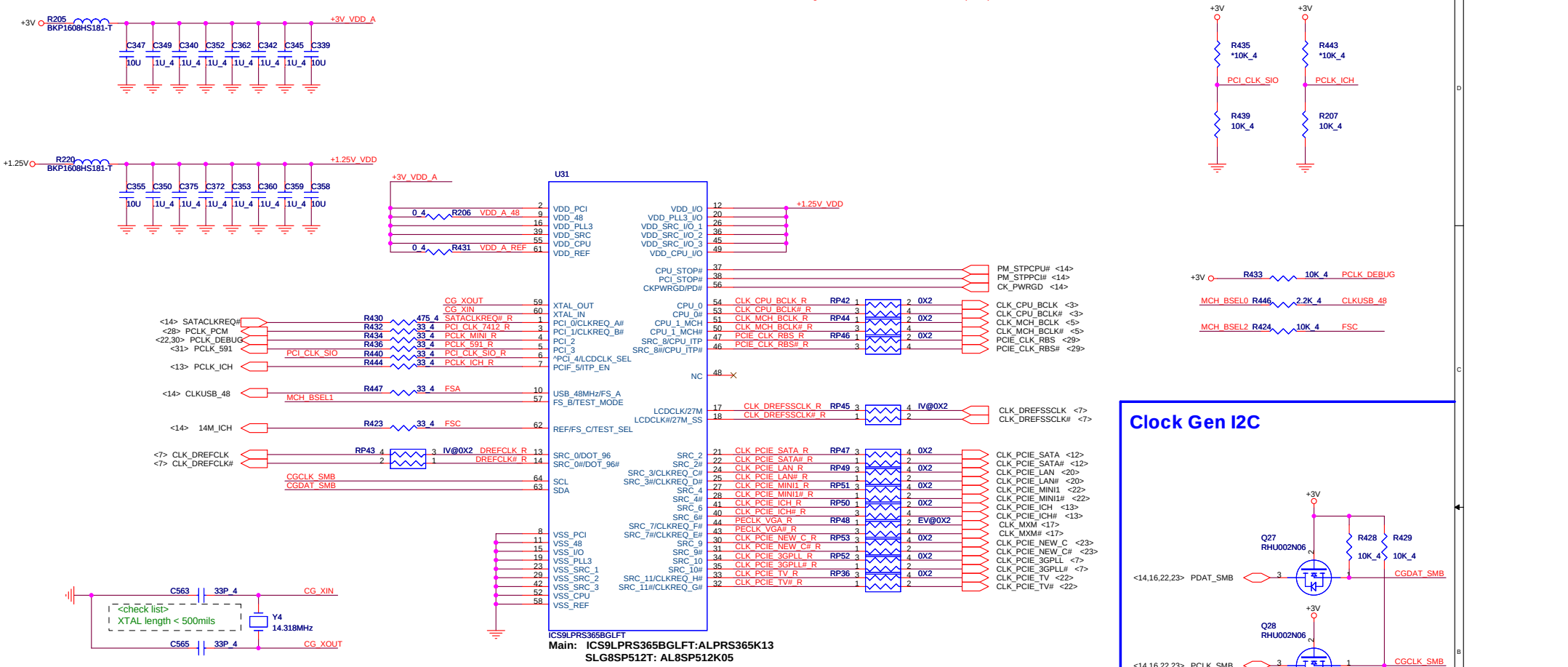
Clock Generator

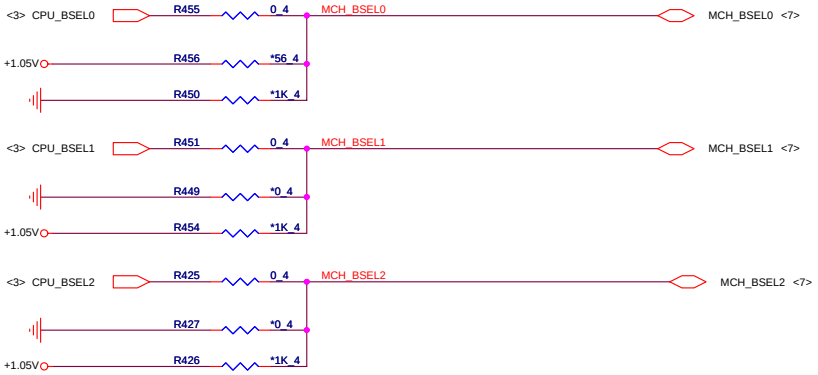
Change list:
B-test
1.Change U31 P/N to ALPRS365K13 (ICS)



Main: ICS9LPRS365BGLFT:ALPRS365K13
SLG8SP512T: AL8SP512K05

Clock Gen I2C

CPU Clock select



BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

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Quanta Computer Inc.

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	CLOCK GENERATOR CK505 W/REGULATOR	B
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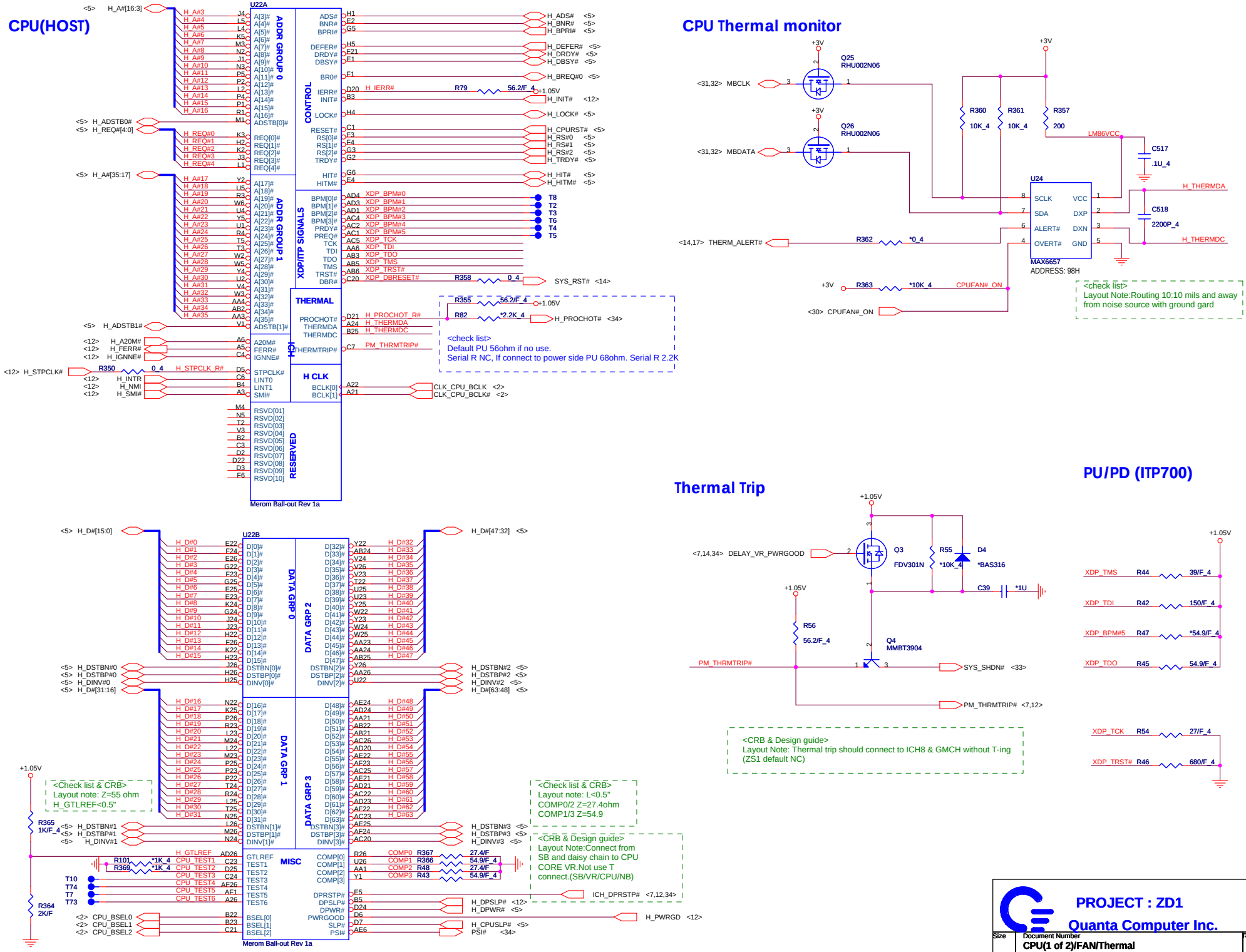
CPU(HOST)
U22A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
Merom Ball-out Rev 1a
<check list>
Default PU 56ohm if no use.
Serial R NC, If connect to power side PU 68ohm. Serial R 2.2K
CPU Thermal monitor
Q25
RHU002N06
Q26
RHU002N06
MAX6657
ADDRESS: 98H
<check list>
Layout Note:Routing 10:10 mils and away from noise source with ground gard
Thermal Trip
Q3
FDV301N
Q4
MMBT3904
<CRB & Design guide>
Layout Note: Thermal trip should connect to ICH8 & GMCH without T-ing (ZS1 default NC)
PU/PD (ITP700)
U22B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
<Check list & CRB>
Layout note: Z=55 ohm
H_GTLREF<0.5"
<Check list & CRB>
Layout note: L<0.5"
COMP0/2 Z=27.4ohm
COMP1/3 Z=54.9
<CRB & Design guide>
Layout Note:Connect from SB and daisy chain to CPU CORE VR.Not use T connect.(SB/VR/CPU/NB)
Merom Ball-out Rev 1a
PROJECT : ZD1
Quanta Computer Inc.
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CPU(1 of 2)/FAN/Thermal
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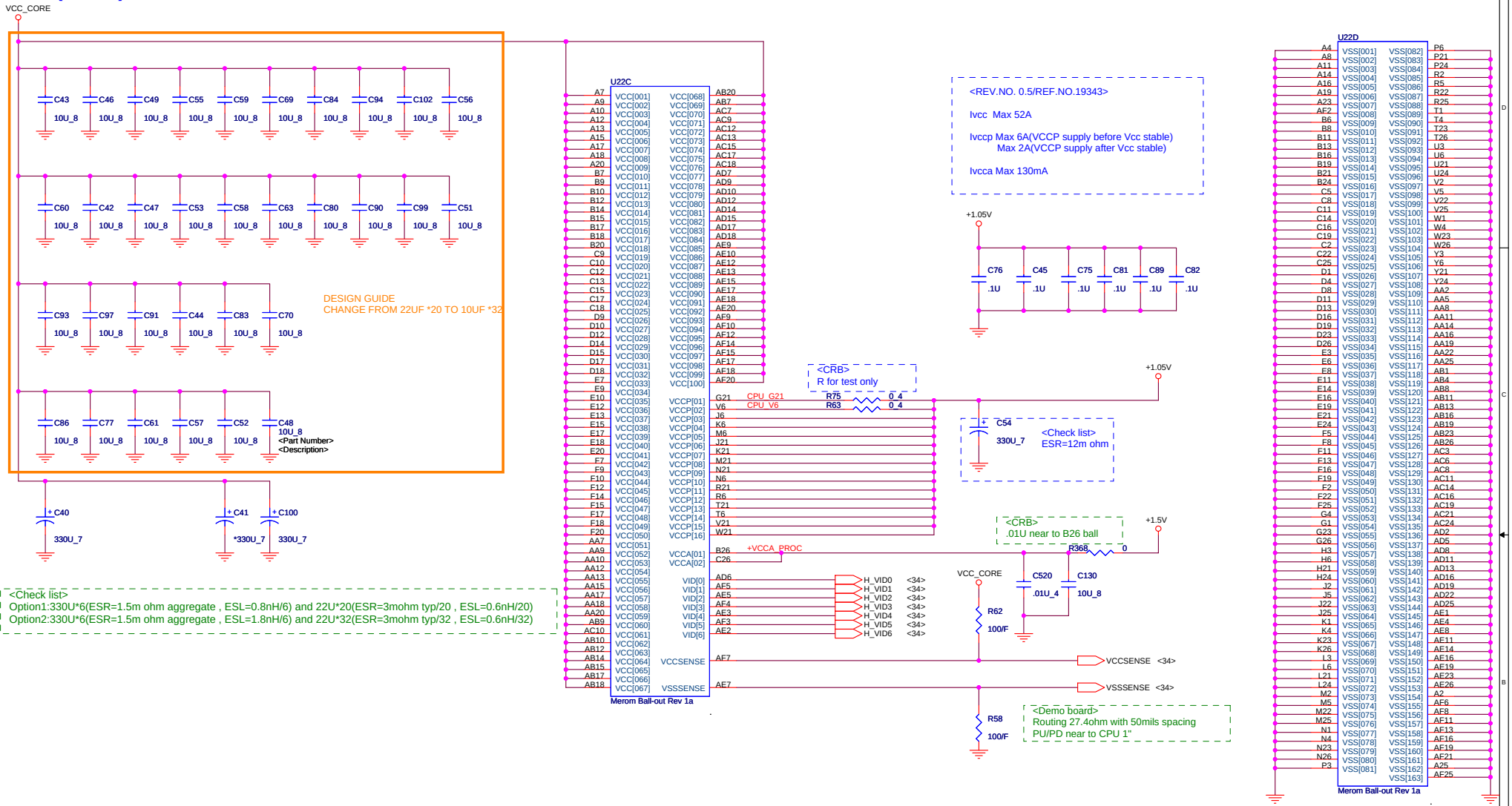
CPU(Power)



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Quanta Computer Inc.

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	CPU(2 of 2)	B

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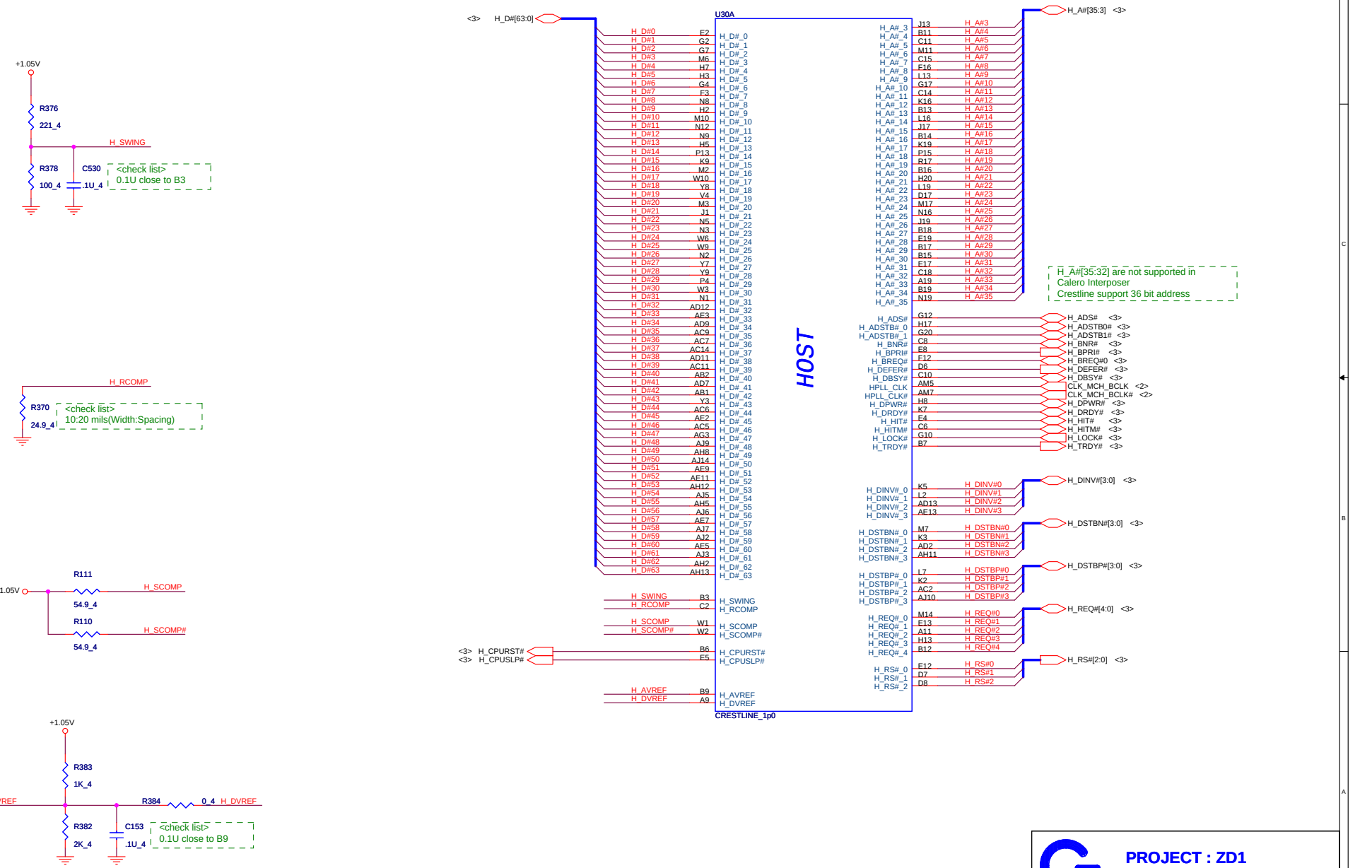
NB(HOST)



PROJECT : ZD1

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	GMCH HOST(1/7)	B

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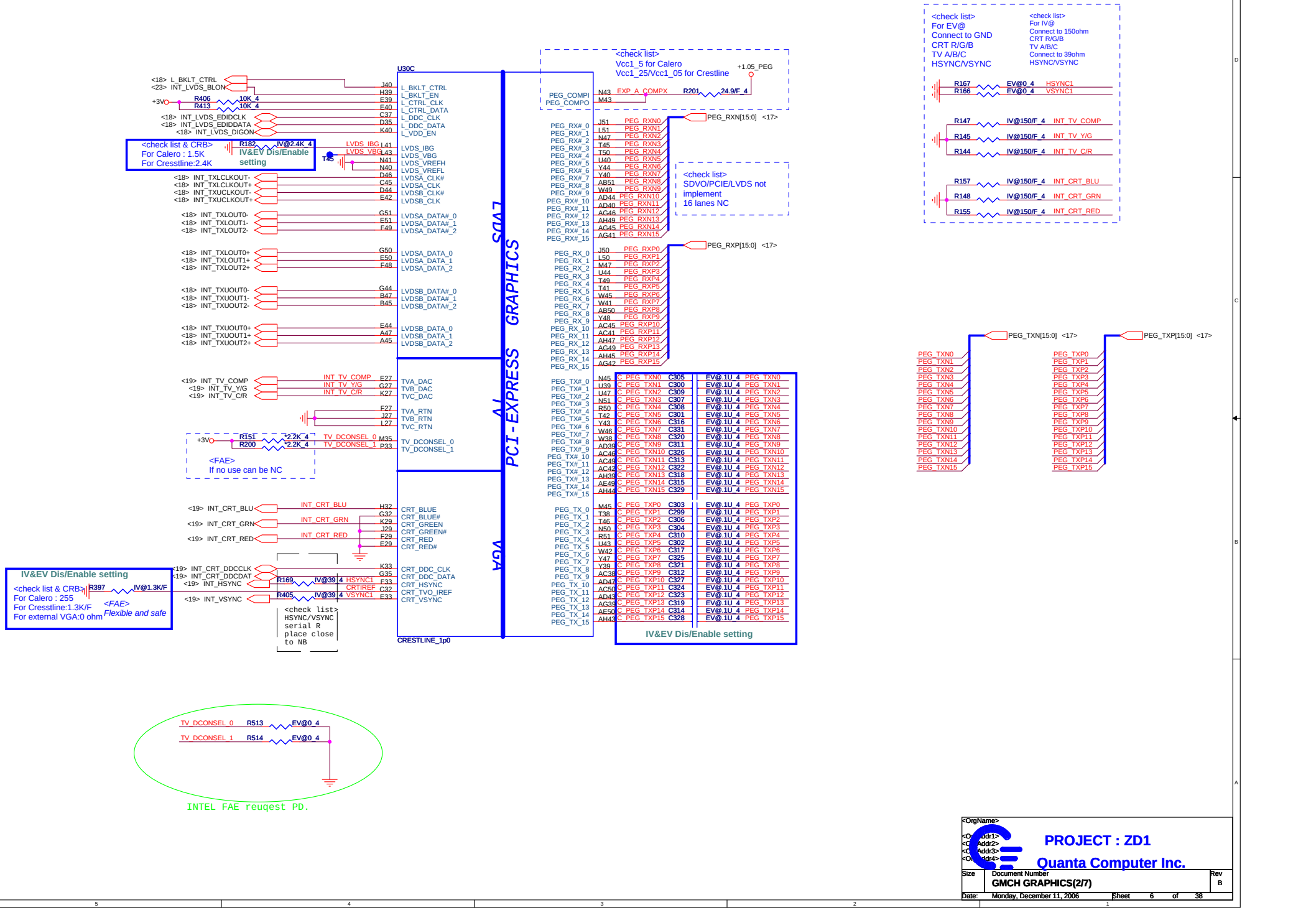

<OrgName>
PROJECT : ZD1
Quanta Computer Inc.

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	GMCH GRAPHICS(2/7)	B

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Strapping table

All strap are sampled with respect to the leading edge of the GMCH power ok signal
CFG[17:3] have internal pull-up
CFG[18:19] have internal pull-down
Any CFG signal strapping option not list below should be left NC pin

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
CFG8	Low Power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reserved Lanes 1 = Normal operation (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ ALLZ/ Clock Un gating	00 = Clock gating disable 01 = ALL-Z Mode Enable 10 = XOR Mode Enable 11 = Normal Cperation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation 1 = Reverse Lanes (Default)
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation (Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card Present

INTEL CRB
CRESSTLINE SHOULD USE 20OHM

<check list & CRB>
R Value select
For Calero : 80.6ohm
For Cresstline:20ohm
But check list use 80.6ohm

M_RCOMP# — R387 20/F_4 — <FAE> 80.6ohm — R388 20/F_4 — +1.8VSUS
M_RCOMP

+3V
R170 10K_4 CLK_MCH_OE#
R395 10K_4 PM_EXTTS#0
R149 10K_4 PM_EXTTS#1

DREFSSCLK R411 EV@4.7K_4 +1.25V
DREFSSCLK# R410 EV@4.7K_4
<FAE>
If no use DREFCLK PU and DREFCLK# PD

IV&EV Dis/Enable setting

DREFCLK R409 EV@4.7K_4 +1.25V
DREFCLK# R408 EV@4.7K_4
<design guide>
If no use DREFCLK PU and DREFCLK# PD

MCH_CFG_5 R138 *4.02K/F_4
MCH_CFG_9 R127 *4.02K/F_4
MCH_CFG_12 R139 *4.02K/F_4
MCH_CFG_13 R137 *4.02K/F_4
MCH_CFG_16 R129 *4.02K/F_4

+3V
MCH_CFG_19 R171 *4.02K/F_4
MCH_CFG_20 R174 *4.02K/F_4

+1.8VSUS — R416 *1K/F_4 — R417 BK1608LL121 — +SMDDR_VREF
+SM_VREF_MCH
R418 *1K/F_4 — C295 .1U_4 — C143 .1U_4

+1.8VSUS — R154 1K/F_4 — SM_RCOMP_VOH
R165 3.01K/F_4 — C241 .01U_4 — C232 2.2U
SM_RCOMP_VOL
R163 1K/F_4 — C250 .01U_4 — C233 2.2U

INTEL CRB
ADD 0.1UF
C165 .1U_4

U30B

RSVD
P36 RSVD1
P37 RSVD2
R35 RSVD3
N35 RSVD4
AR12 RSVD5
AR13 RSVD6
AM12 RSVD7
AN13 RSVD8
J12 RSVD9
AR37 RSVD10
AM36 RSVD11
AL36 RSVD12
AM37 RSVD13
D20 RSVD14

H10 RSVD20
B51 RSVD21
BJ20 RSVD22
BK22 RSVD23
BF19 RSVD24
BH20 RSVD25
BK18 RSVD26
BJ18 RSVD27
BF23 RSVD28
BG23 RSVD29
BC23 RSVD30
BD24 RSVD31

BH39 RSVD32
AW20 RSVD33
BK20 RSVD34
C48 RSVD35
D47 RSVD36
B44 RSVD37
C44 RSVD38
A35 RSVD39
B37 RSVD40
B36 RSVD41
B34 RSVD42
C34 RSVD43

DDR MUXING
SM_CK_0 AV29 M_CLK0 <16>
SM_CK_1 BB23 M_CLK1 <16>
SM_CK_3 BA25 M_CLK2 <16>
SM_CK_4 AV23 M_CLK3 <16>
SM_CK#_0 AW30 M_CLK#0 <16>
SM_CK#_1 BA23 M_CLK#1 <16>
SM_CK#_3 AW25 M_CLK#2 <16>
SM_CK#_4 AW23 M_CLK#3 <16>
SM_CKE_0 BE29 M_CKE0 <16>
SM_CKE_1 AY32 M_CKE1 <16>
SM_CKE_3 BD39 M_CKE2 <16>
SM_CKE_4 BG37 M_CKE3 <16>
SM_CS#_0 BG20 M_CS#0 <16>
SM_CS#_1 BK16 M_CS#1 <16>
SM_CS#_2 BG16 M_CS#2 <16>
SM_CS#_3 BF13 M_CS#3 <16>
SM_ODT_0 BH18 M_ODT0 <16>
SM_ODT_1 BJ15 M_ODT1 <16>
SM_ODT_2 BJ14 M_ODT2 <16>
SM_ODT_3 BE16 M_ODT3 <16>
SM_RCOMP BL15 M_RCOMP
SM_RCOMP# BK14 M_RCOMP#
SM_RCOMP_VOH BK31 SM_RCOMP_VOH
SM_RCOMP_VOL BL31 SM_RCOMP_VOL
SM_VREF_0 AR49 +SM_VREF_MCH
SM_VREF_1 AW4

CLK
DPLL_REF_CLK B42 DREFCLK CLK_DREFCLK <2>
DPLL_REF_CLK# C42 DREFCLK# CLK_DREFCLK# <2>
DPLL_REF_SSCLK H48 DREFSSCLK CLK_DREFSSCLK <2>
DPLL_REF_SSCLK# H47 DREFSSCLK# CLK_DREFSSCLK# <2>
PEG_CLK K44 CLK_PCIE_3GPLL CLK_PCIE_3GPLL <2>
PEG_CLK# K45 CLK_PCIE_3GPLL# CLK_PCIE_3GPLL# <2>

DMI
DMI_RXN_0 AN47 DMI_TXN0
DMI_RXN_1 AJ38 DMI_TXN1
DMI_RXN_2 AN42 DMI_TXN2
DMI_RXN_3 AN46 DMI_TXN3
DMI_TXN[3:0] <13>
DMI_RXP_0 AM47 DMI_TXP0
DMI_RXP_1 AJ39 DMI_TXP1
DMI_RXP_2 AN41 DMI_TXP2
DMI_RXP_3 AN45 DMI_TXP3
DMI_TXP[3:0] <13>
DMI_TXN_0 AJ46 DMI_RXN0
DMI_TXN_1 AJ41 DMI_RXN1
DMI_TXN_2 AM40 DMI_RXN2
DMI_TXN_3 AM44 DMI_RXN3
DMI_RXN[3:0] <13>
DMI_TXP_0 AJ47 DMI_RXP0
DMI_TXP_1 AJ42 DMI_RXP1
DMI_TXP_2 AM39 DMI_RXP2
DMI_TXP_3 AM43 DMI_RXP3
DMI_RXP[3:0] <13>

CFG
<2> MCH_BSEL0 P27 CFG_0
<2> MCH_BSEL1 N27 CFG_1
<2> MCH_BSEL2 N24 CFG_2
CFG_3
CFG_4
CFG_5
T30 MCH_CFG_3 C21 CFG_6
T75 MCH_CFG_4 C23 CFG_7
MCH_CFG_5 F23 CFG_8
T34 MCH_CFG_6 N23 CFG_9
T24 MCH_CFG_7 G23 CFG_10
T29 MCH_CFG_8 J20 CFG_11
MCH_CFG_9 C20 CFG_12
T37 MCH_CFG_10 R24 CFG_13
T28 MCH_CFG_11 L23 CFG_14
MCH_CFG_12 J23 CFG_15
MCH_CFG_13 E23 CFG_16
MCH_CFG_14 E20 CFG_17
T25 MCH_CFG_15 K23 CFG_18
T27 MCH_CFG_16 M20 CFG_19
MCH_CFG_17 M24 CFG_20
T32 MCH_CFG_18 L32
T40 MCH_CFG_19 N33
MCH_CFG_20 L35

PM
<14> PM_BMBUSY# R184 0_4 PM_BMBUSY#_R G41 PM_BM_BUSY#
<3,12,34> ICH_DPRSTP# R177 0_4 ICH_DPRSTP#_R L39 PM_DPRSTP#
<16> PM_EXTTS#0 R401 0_4 PM_EXTTS#0_R L36 PM_EXT_TS#_0
<16> PM_EXTTS#1 R150 0_4 PM_EXTTS#1_R J36 PM_EXT_TS#_1
<3,14,34> DELAY_VR_PWRGOOD AW49 PWROK
<13> PLTRST#_NB R140 100_4 RST_IN#_MCH AV20 RSTIN#
<3,12> PM_THRMTRIP# R130 *0_4 PM_THRMTRIP#_GMCH N20 THERMTRIP#
<14,34> PM_DPRSLPVR R407 0_4 PM_DPRSLPVR_GMCH G36 DPRSLPVR

GRAPHICS VID
GFX_VID_0 E35 MCH_GFX_VID_0 T41
GFX_VID_1 A39 MCH_GFX_VID_1 T42
GFX_VID_2 C38 MCH_GFX_VID_2 T43
GFX_VID_3 B39 MCH_GFX_VID_3 T44
GFX_VR_EN E36 R183 *0_4 SUSB# <14,31>

ME
CL_CLK AM49 CL_CLK0 <14>
CL_DATA AK50 CL_DATA0 <14>
CL_PWROK AT43 MPWROK <14,31>
CL_RST# AN49 CL_RST#0 <14>
CL_VREF AM50 +1.25V_CL_VREF

NC
BJ51 NC_1
BK51 NC_2
BK50 NC_3
BL50 NC_4
BL49 NC_5
BL3 NC_6
BL2 NC_7
BK1 NC_8
BJ1 NC_9
E1 NC_10
A5 NC_11
C51 NC_12
B50 NC_13
A50 NC_14
A49 NC_15
BK2 NC_16

MISC
SDVO_CTRL_CLK H35
SDVO_CTRL_DATA K36
CLK_REQ# G39 CLK_MCH_OE#
ICH_SYNC# G40 MCH_ICH_SYNC# <14>
TEST_1 A37 GMCH_TEST1 R178 0_4
TEST_2 R32 GMCH_TEST2 R168 20K_4

CRESTLINE_1p0

+1.25V
R422 1K/F_4
C559 .1U_4
R420 392/F

DREFCLK R529 EV@0_4
DREFCLK# R531 EV@0_4
DREFSSCLK R532 EV@0_4
DREFSSCLK# R533 EV@0_4
INTEL FAE suggest PD for external graphics

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Quanta Computer Inc.

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	GMCH (STRAPPING/OTHER 3/7)	B
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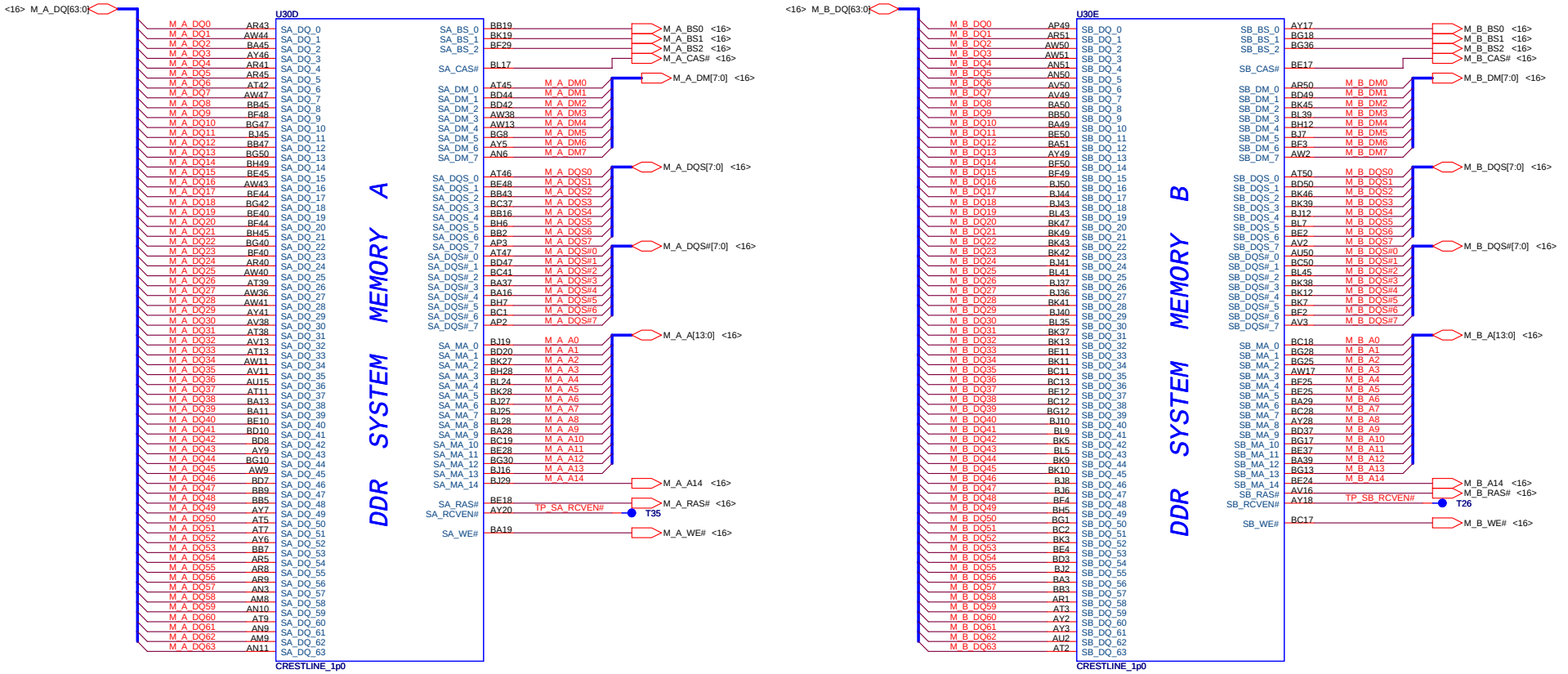
NB(Memory controller)



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	GMCH DDR(4/7)	B
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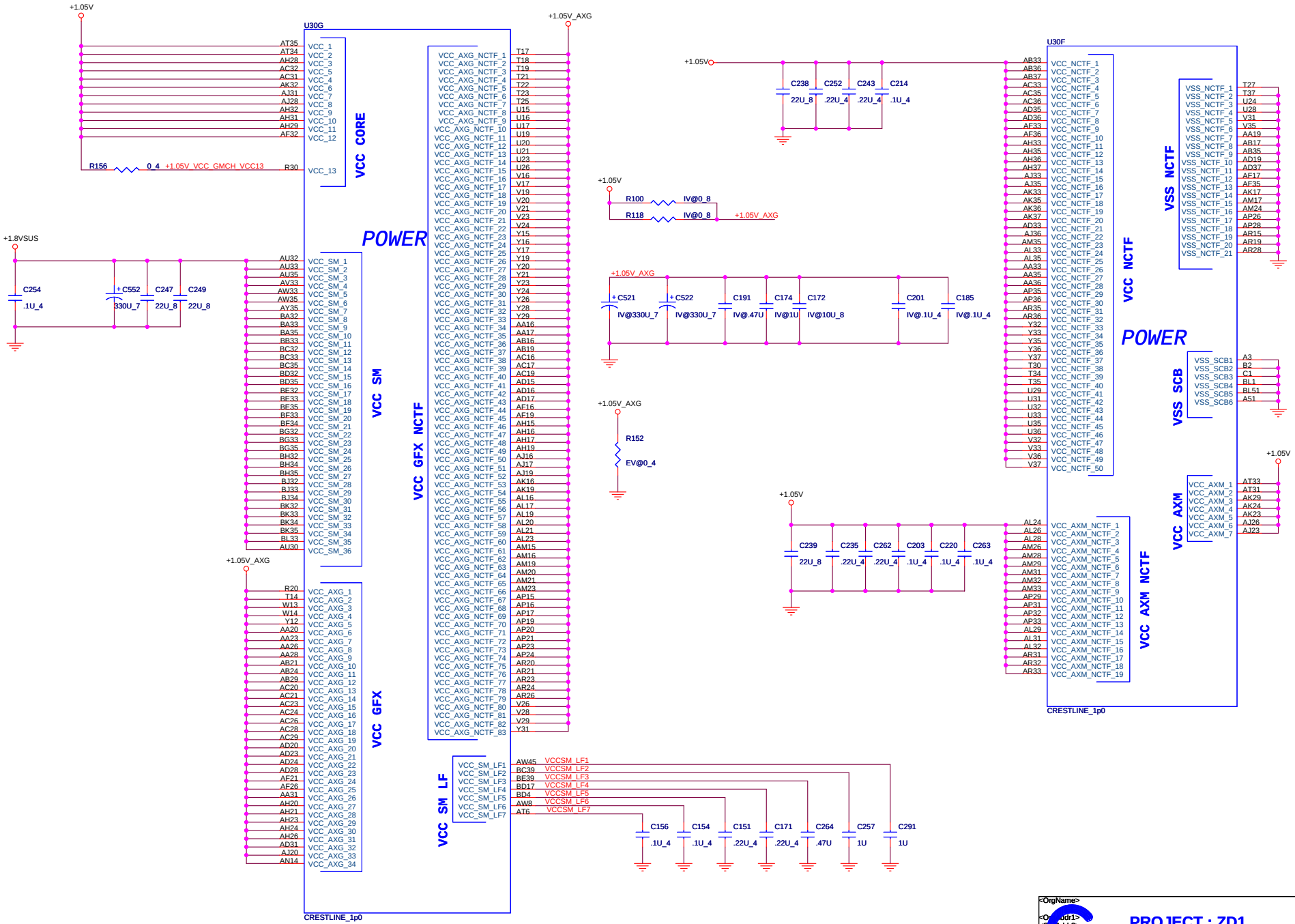
NB(Power-1)



<OrgName>
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	GMCH Power-1(5/7)	B
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NB(Power-2)

CRT/TV Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V

EXTERNAL / INTERNAL

<FAE>
INT VGA disable
VCCSYNC connect to GND

IV&EV Dis/Enable setting

CRB RECOMMEND
180OHM@100MHz
Rdc= 0.09OHM (max)

IV&EV Dis/Enable setting

<FAE>
INT VGA disable
VCCD_TVDAC still +1.5V

Change to
100 ohm Resistor

Use site for filter cap with Gfx enabled CS

IV&EV Dis/Enable setting

<FAE>
VCC_RXR_DMI and VCC_PEG connect to+1.05V

<CRB>
+1.25V AND +1.25M shall be
+1.5V for Calero Interposer

CRESTLINE_1p0

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Quanta Computer Inc.	
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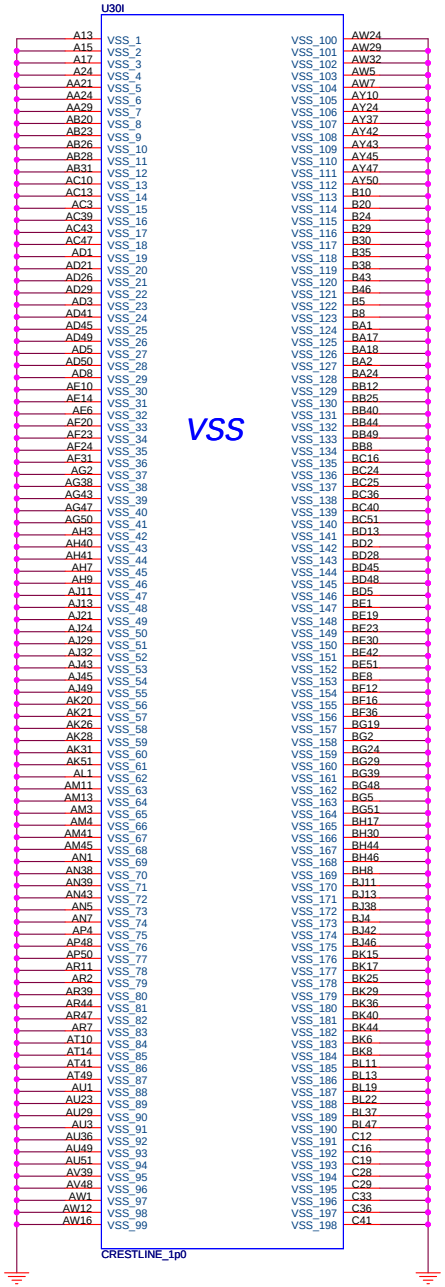
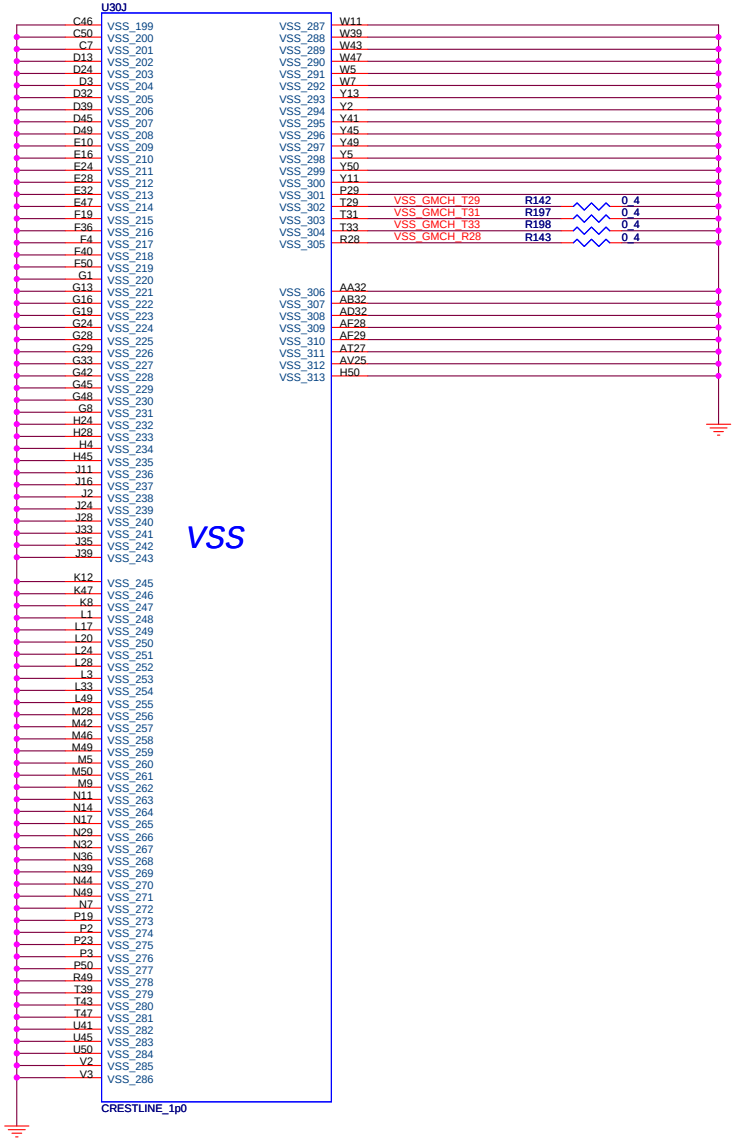
NB(Power-3)





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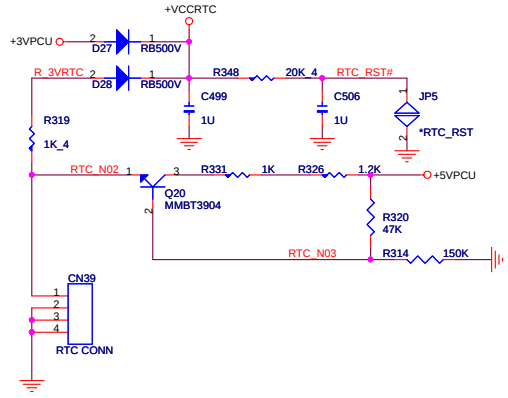
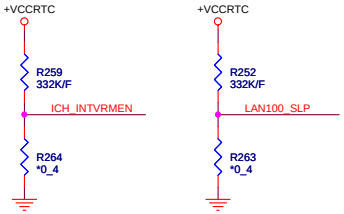
RTC



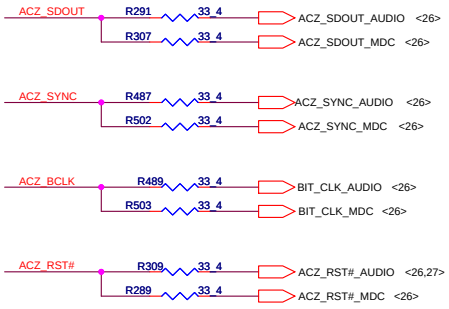
SB Strap

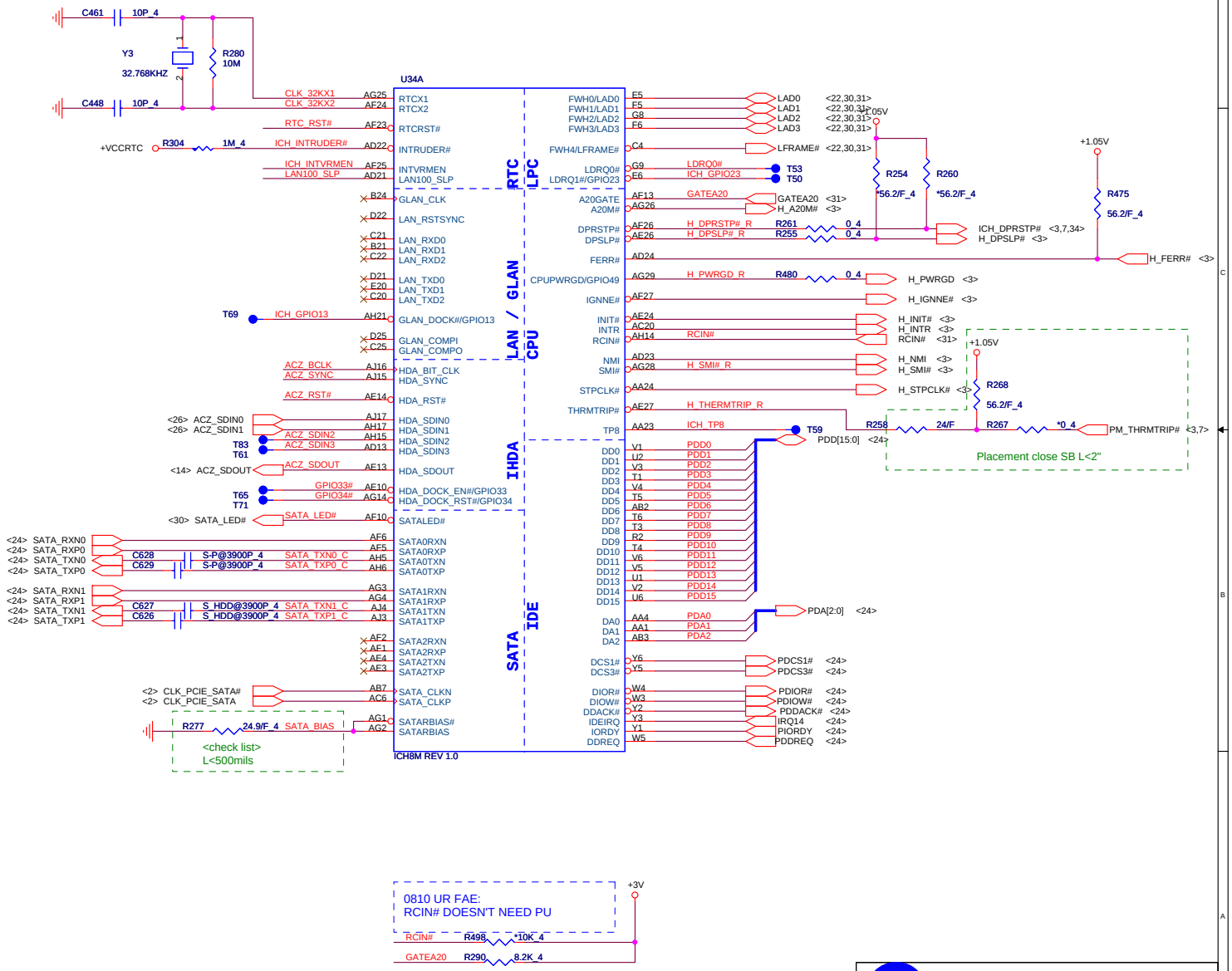
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)



HDA





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	ICH8M HOST(1/4)	B
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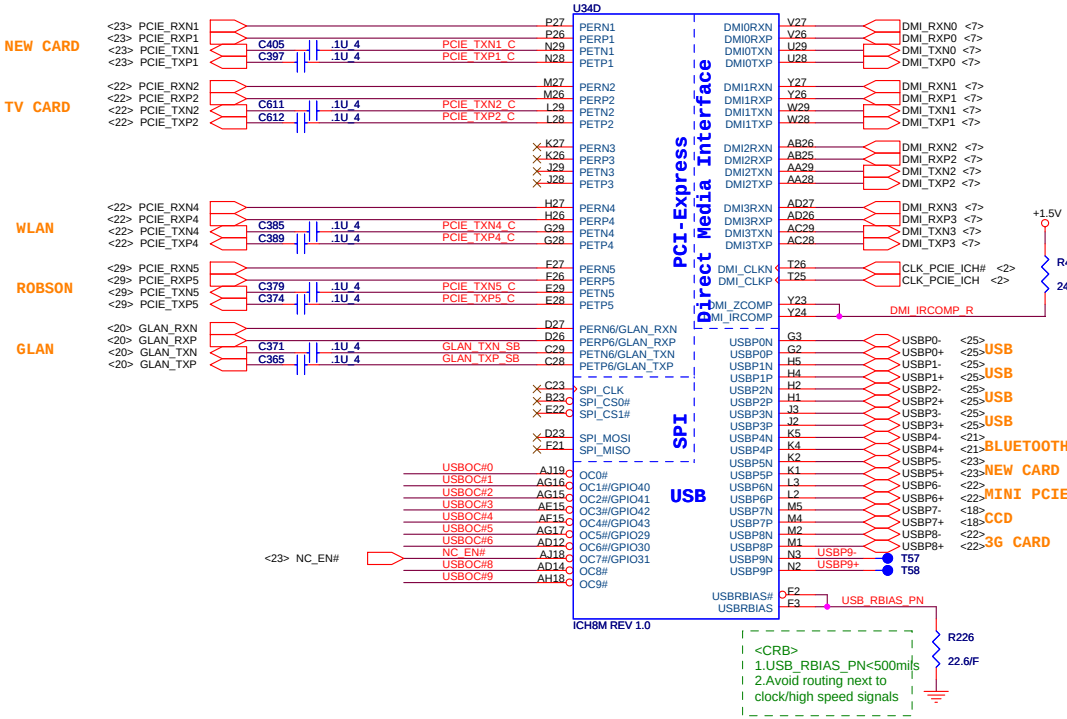
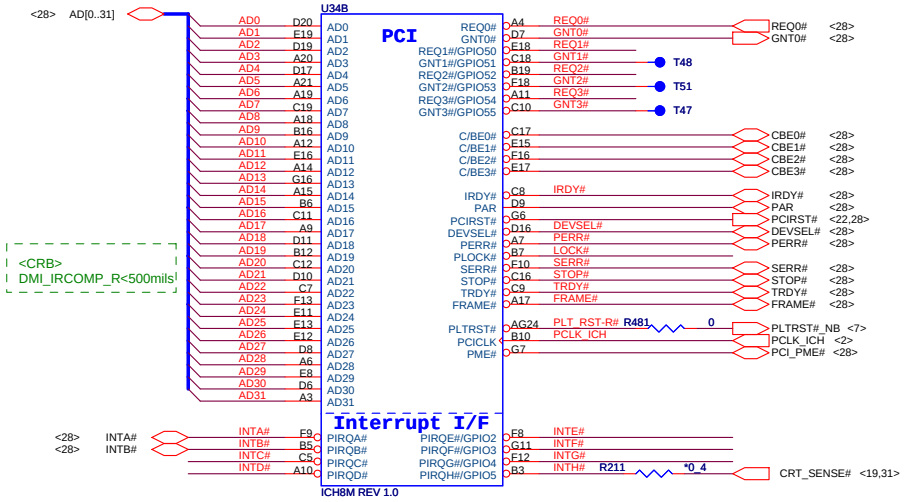
SB-PCIE/USB/DMI

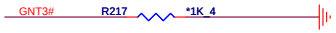


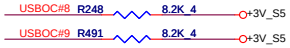
SB-PCI

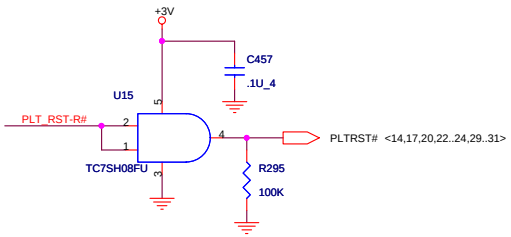


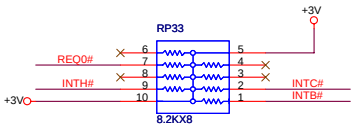
A16 SWAP Override strap

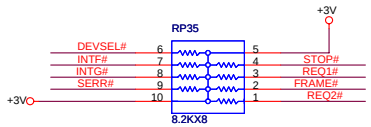
PCI_GNT#3	Low = A16 swap override enabled High = Default

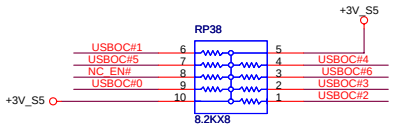


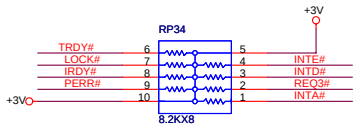












PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M PCIE\PCI\USB(2/4)	B
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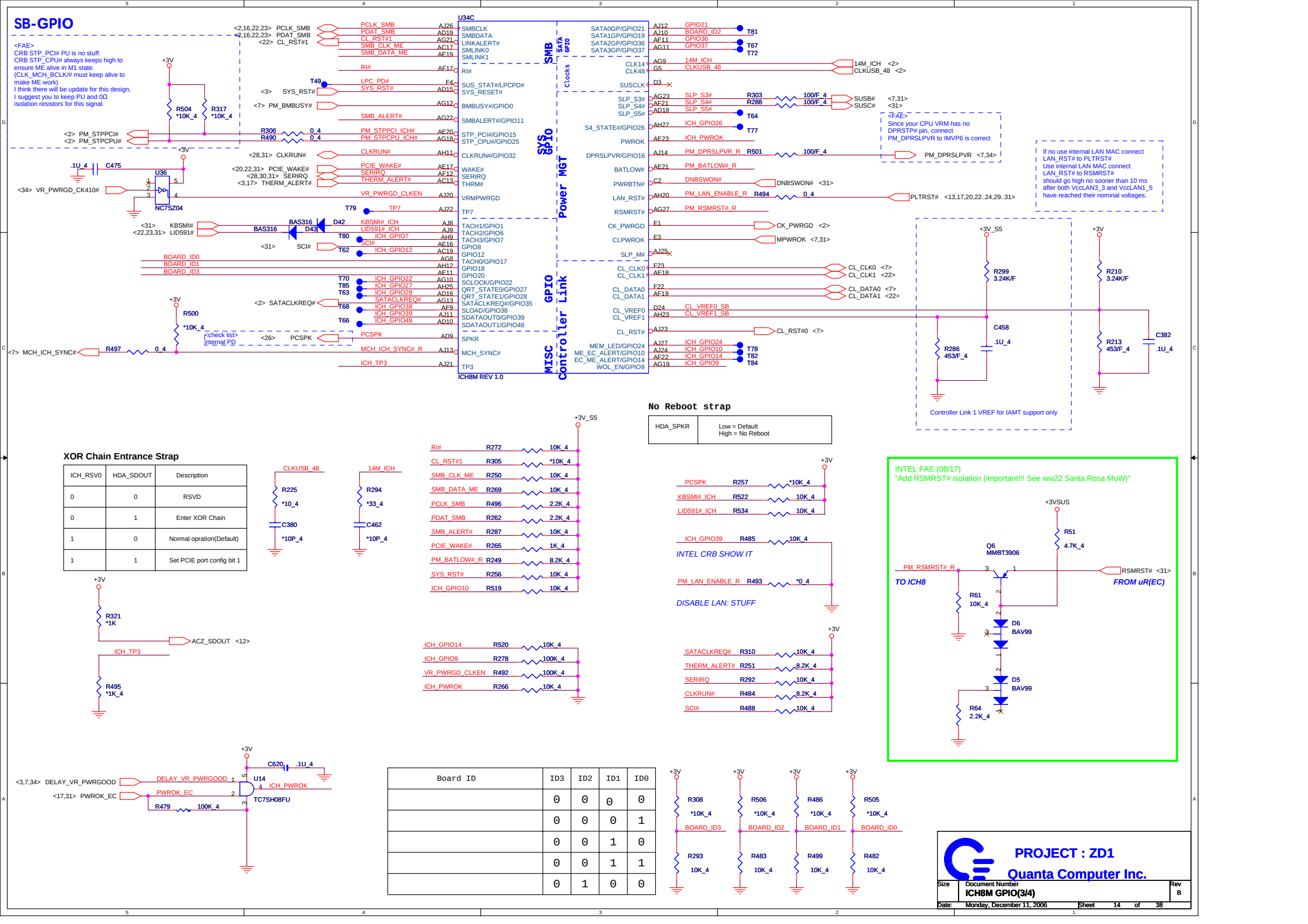
SB-GPIO



No Reboot strap

HDA_SPKR	Low = Default High = No Reboot

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

Board ID	ID3	ID2	ID1	ID0
	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M GPIO(3/4)	B
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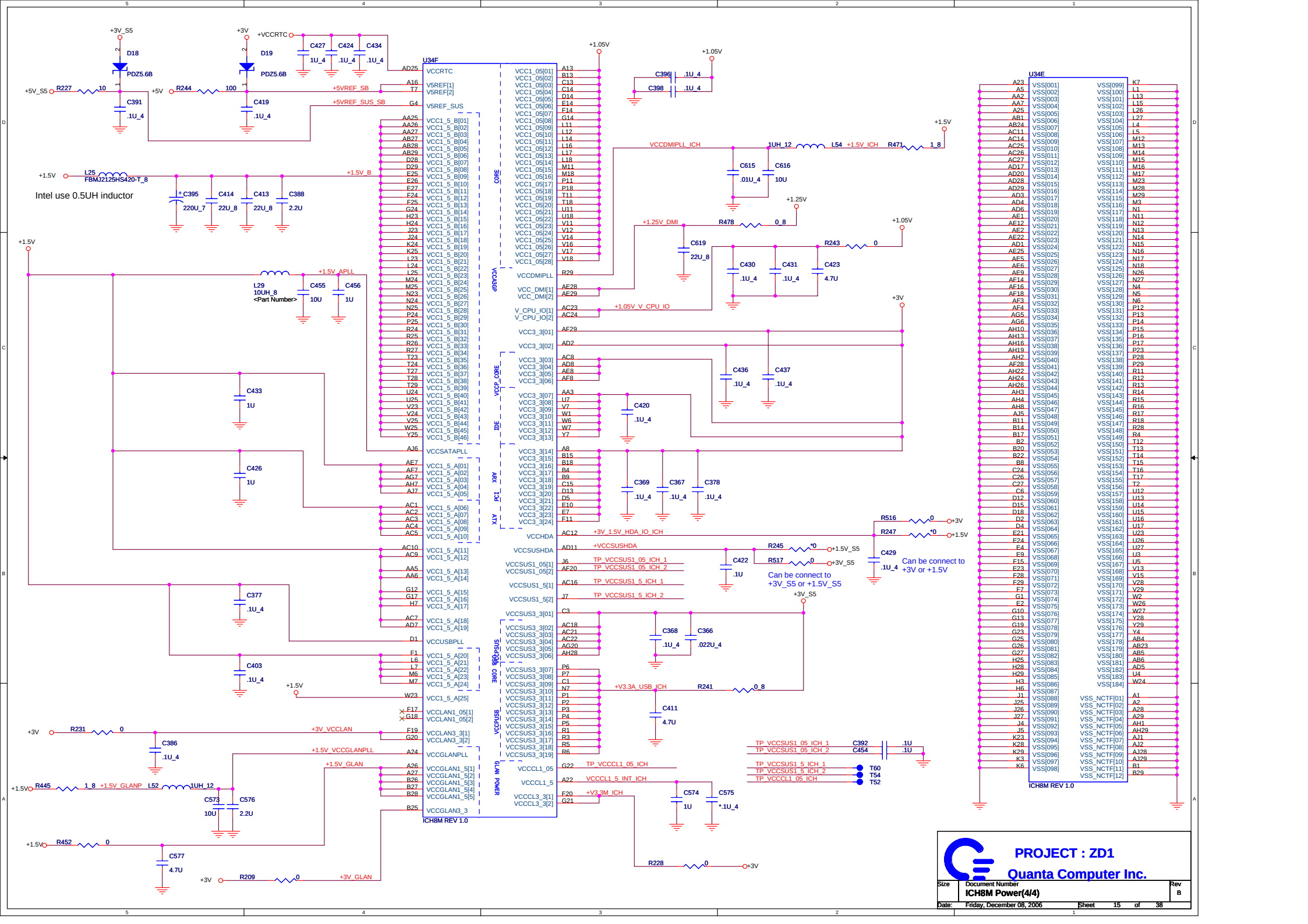
U34F
ICH8M REV 1.0
U34E
ICH8M REV 1.0
Intel use 0.5UH inductor
Can be connect to +3V or +1.5V
Can be connect to +3V_S5 or +1.5V_S5
PROJECT : ZD1
Quanta Computer Inc.
ICH8M Power(4/4)
Rev B
Friday, December 08, 2006
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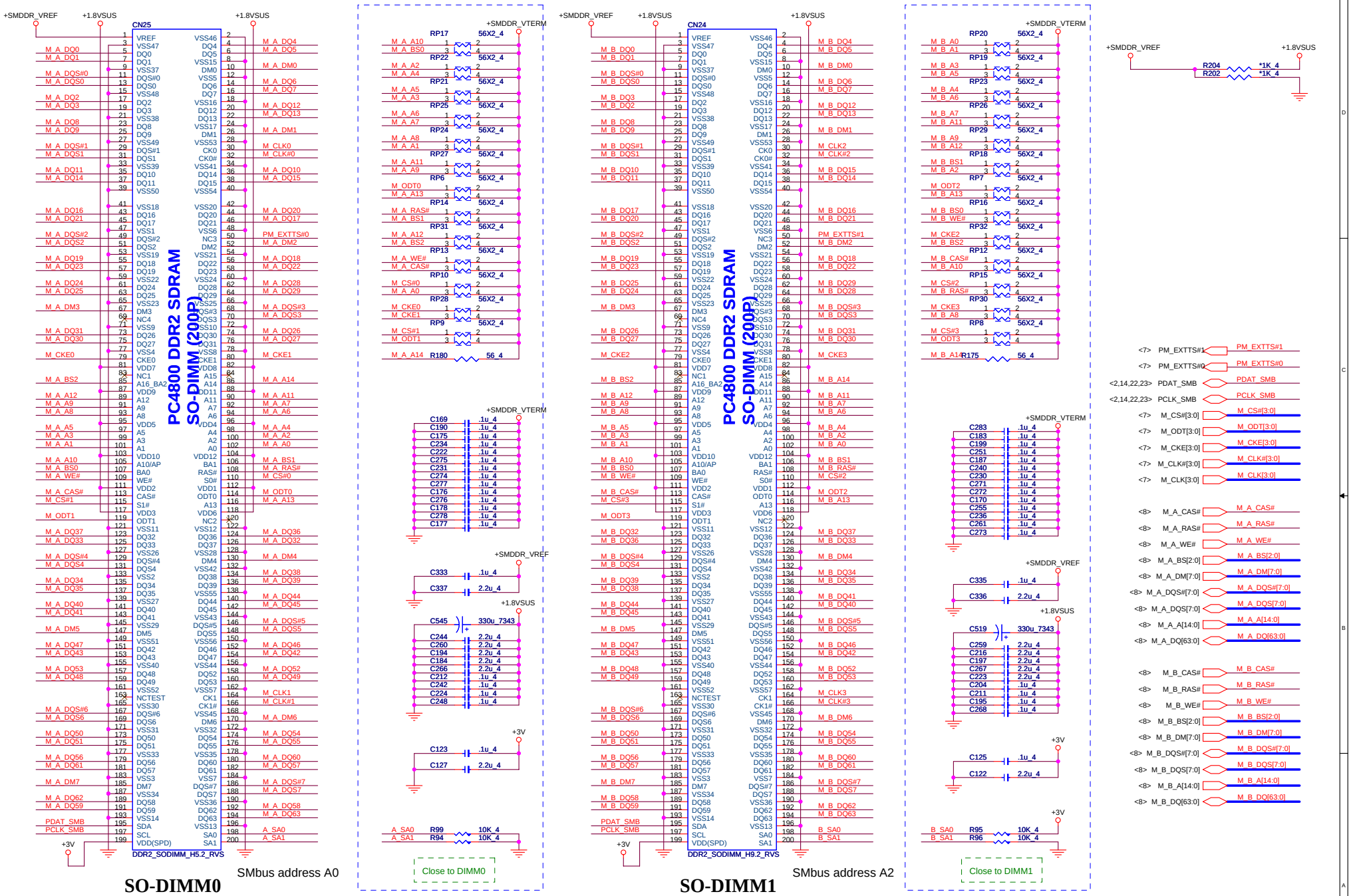

Size	Document Number: DDRII SO-DIMM	Rev: B
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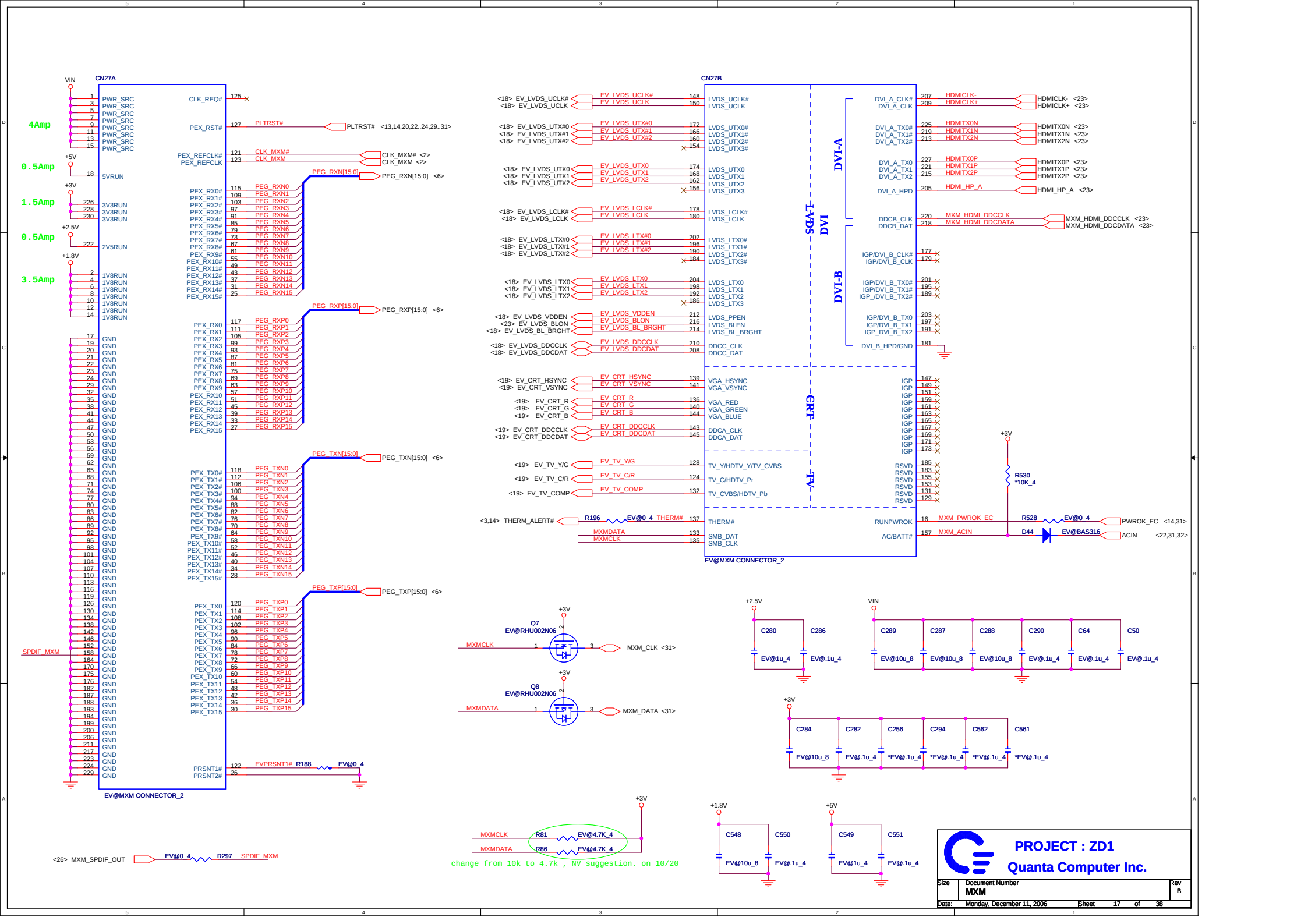
Quanta Computer Inc.


CN27A
CN27B
EV@MXM CONNECTOR_2
4Amp
0.5Amp
1.5Amp
0.5Amp
3.5Amp
VIN
+5V
+3V
+2.5V
+1.8V
PWR_SRC
5VRUN
3V3RUN
2V5RUN
1V8RUN
GND
CLK_REQ#
PEX_RST#
PLTRST#
PEX_REFCLK#
PEX_REFCLK
CLK_MXM#
CLK_MXM
PEG_RXN[15:0]
PEG_RXP[15:0]
PEG_TXN[15:0]
PEG_TXP[15:0]
PEX_RX0#
PEX_RX1#
PEX_RX2#
PEX_RX3#
PEX_RX4#
PEX_RX5#
PEX_RX6#
PEX_RX7#
PEX_RX8#
PEX_RX9#
PEX_RX10#
PEX_RX11#
PEX_RX12#
PEX_RX13#
PEX_RX14#
PEX_RX15#
PEX_RX0
PEX_RX1
PEX_RX2
PEX_RX3
PEX_RX4
PEX_RX5
PEX_RX6
PEX_RX7
PEX_RX8
PEX_RX9
PEX_RX10
PEX_RX11
PEX_RX12
PEX_RX13
PEX_RX14
PEX_RX15
PEX_TX0#
PEX_TX1#
PEX_TX2#
PEX_TX3#
PEX_TX4#
PEX_TX5#
PEX_TX6#
PEX_TX7#
PEX_TX8#
PEX_TX9#
PEX_TX10#
PEX_TX11#
PEX_TX12#
PEX_TX13#
PEX_TX14#
PEX_TX15#
PEX_TX0
PEX_TX1
PEX_TX2
PEX_TX3
PEX_TX4
PEX_TX5
PEX_TX6
PEX_TX7
PEX_TX8
PEX_TX9
PEX_TX10
PEX_TX11
PEX_TX12
PEX_TX13
PEX_TX14
PEX_TX15
PRSNT1#
PRSNT2#
EVPRSNT1#
R188
EV@0_4
SPDIF_MXM
<26> MXM_SPDIF_OUT
R297
LVDS_UCLK#
LVDS_UCLK
LVDS_UTX0#
LVDS_UTX1#
LVDS_UTX2#
LVDS_UTX3#
LVDS_UTX0
LVDS_UTX1
LVDS_UTX2
LVDS_UTX3
LVDS_LCLK#
LVDS_LCLK
LVDS_LTX0#
LVDS_LTX1#
LVDS_LTX2#
LVDS_LTX3#
LVDS_LTX0
LVDS_LTX1
LVDS_LTX2
LVDS_LTX3
LVDS_VDDEN
LVDS_BLON
LVDS_BL_BRGHT
LVDS_PPEN
LVDS_BLEN
DDCC_CLK
DDCC_DAT
DDCA_CLK
DDCA_DAT
VGA_HSYNC
VGA_VSYNC
VGA_RED
VGA_GREEN
VGA_BLUE
TV_Y/HDTV_Y/TV_CVBS
TV_C/HDTV_Pr
TV_CVBS/HDTV_Pb
THERM#
SMB_DAT
SMB_CLK
DVI_A_CLK#
DVI_A_CLK
DVI_A_TX0#
DVI_A_TX1#
DVI_A_TX2#
DVI_A_TX0
DVI_A_TX1
DVI_A_TX2
DVI_A_HPD
DDCB_CLK
DDCB_DAT
IGP/DVI_B_CLK#
IGP/DVI_B_CLK
IGP/DVI_B_TX0#
IGP/DVI_B_TX1#
IGP_/DVI_B_TX2#
IGP/DVI_B_TX0
IGP/DVI_B_TX1
IGP_DVI_B_TX2
DVI_B_HPD/GND
RSVD
RUNPWROK
AC/BATT#
HDMICLK-
HDMICLK+
HDMITX0N
HDMITX1N
HDMITX2N
HDMITX0P
HDMITX1P
HDMITX2P
HDMI_HP_A
MXM_HDMI_DDCCLK
MXM_HDMI_DDCDATA
DVI-A
DVI-B
LVDS
DVI
CRT
TV
EV_LVDS_UCLK#
EV_LVDS_UCLK
EV_LVDS_UTX0#
EV_LVDS_UTX1#
EV_LVDS_UTX2#
EV_LVDS_UTX0
EV_LVDS_UTX1
EV_LVDS_UTX2
EV_LVDS_LCLK#
EV_LVDS_LCLK
EV_LVDS_LTX0#
EV_LVDS_LTX1#
EV_LVDS_LTX2#
EV_LVDS_LTX0
EV_LVDS_LTX1
EV_LVDS_LTX2
EV_LVDS_VDDEN
EV_LVDS_BLON
EV_LVDS_BL_BRGHT
EV_LVDS_DDCCLK
EV_LVDS_DDCDAT
EV_CRT_HSYNC
EV_CRT_VSYNC
EV_CRT_R
EV_CRT_G
EV_CRT_B
EV_CRT_DDCCLK
EV_CRT_DDCDAT
EV_TV_Y/G
EV_TV_C/R
EV_TV_COMP
R196
EV@0_4
THERM#
MXMDATA
MXMCLK
R530
*10K_4
R528
D44
EV@BAS316
MXM_PWROK_EC
MXM_ACIN
PWROK_EC
ACIN
Q7
EV@RHU002N06
Q8
EV@RHU002N06
MXM_CLK
MXM_DATA
C280
C286
C289
C287
C288
C290
C64
C50
C284
C282
C256
C294
C562
C561
R81
R86
EV@4.7K_4
change from 10k to 4.7k , NV suggestion. on 10/20
C548
C550
C549
C551
EV@10u_8
EV@1u_4
EV@.1u_4
*EV@.1u_4
PROJECT : ZD1
Quanta Computer Inc.
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MXM
Rev
B
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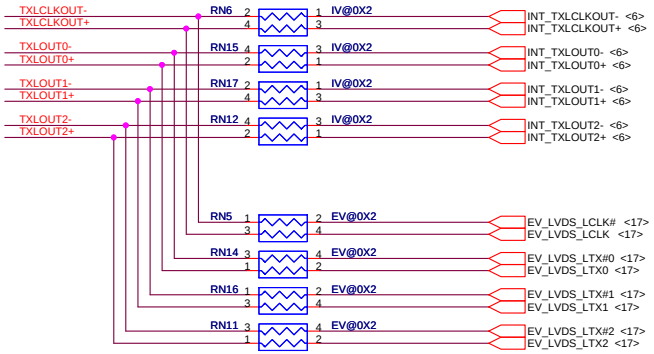
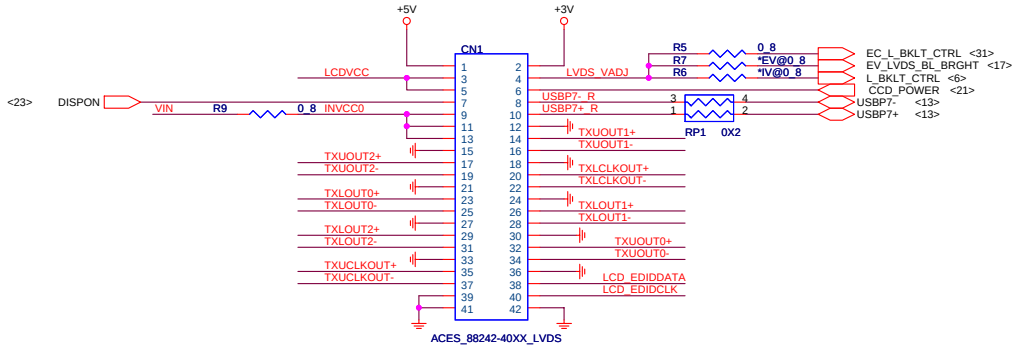
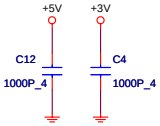
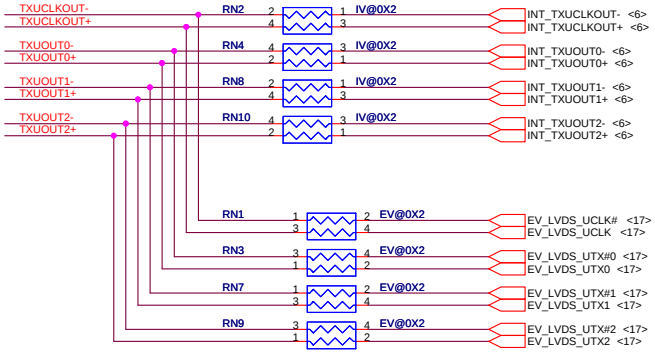
38

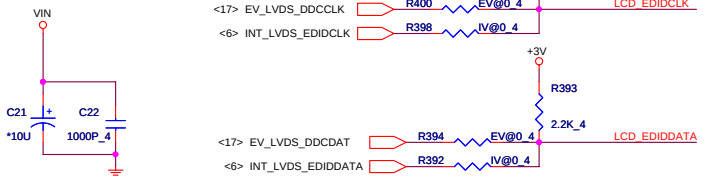
LVDS

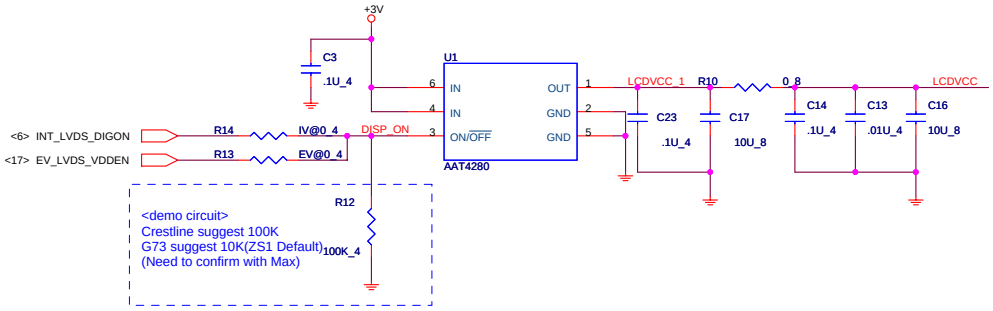












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Quanta Computer Inc.

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	LVDS	B
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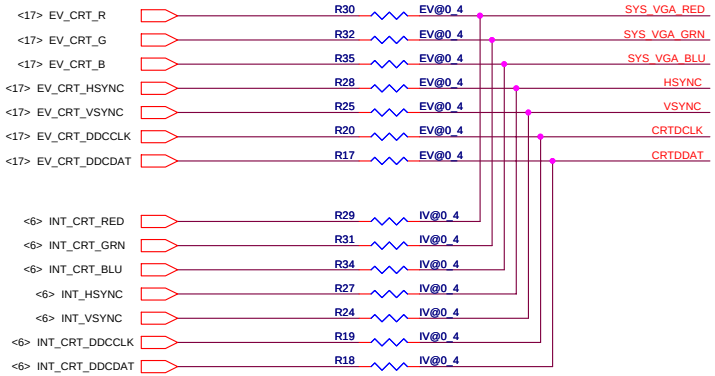
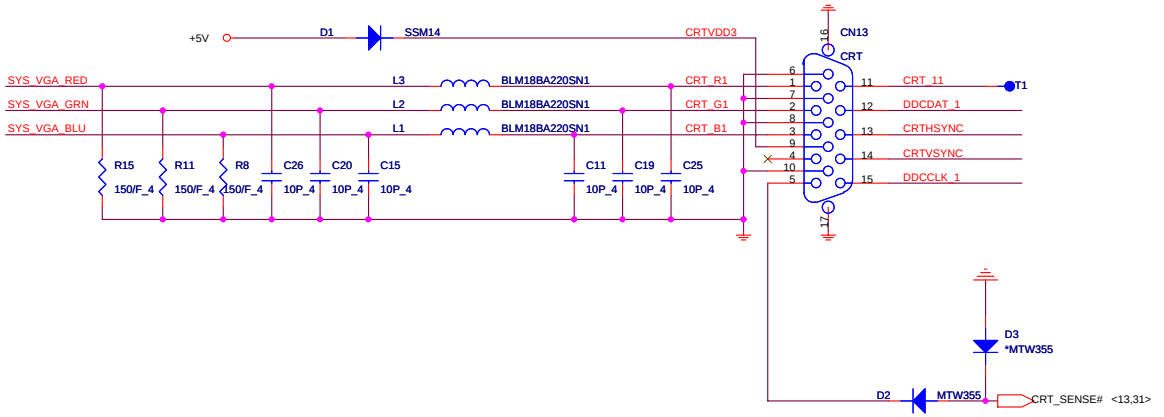
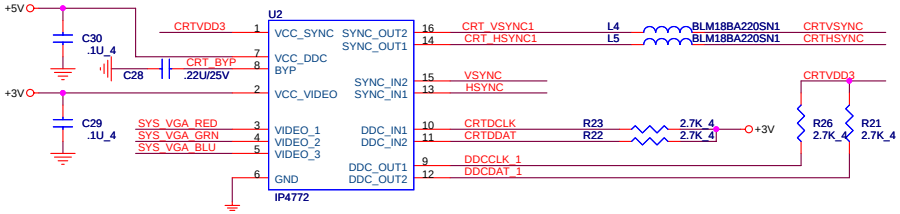
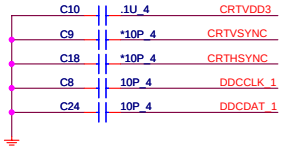
CRT Select



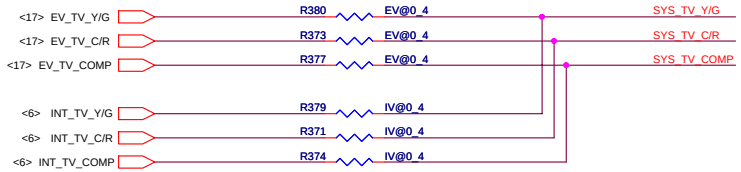
CRT CONNECTOR AND ESD

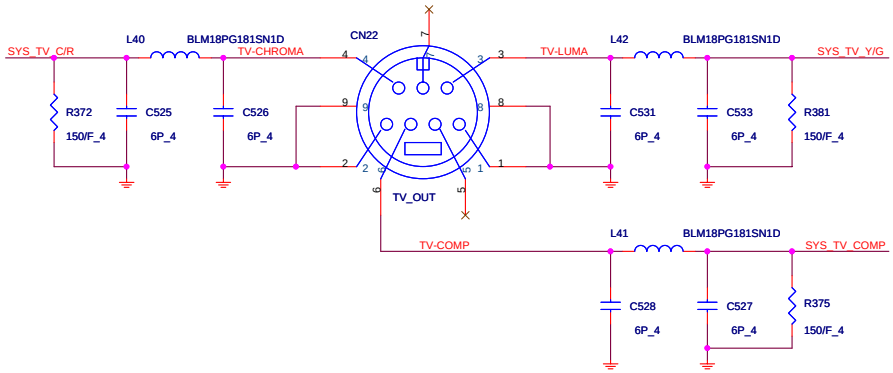


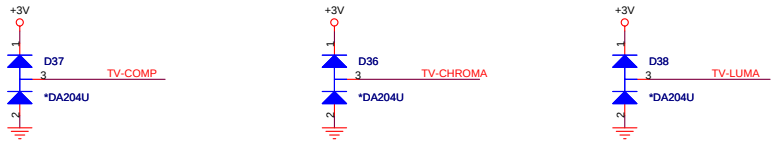




TV Out (SVHS) MiniDIN 7-pin







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Quanta Computer Inc.

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	CRT/TVOUT	B

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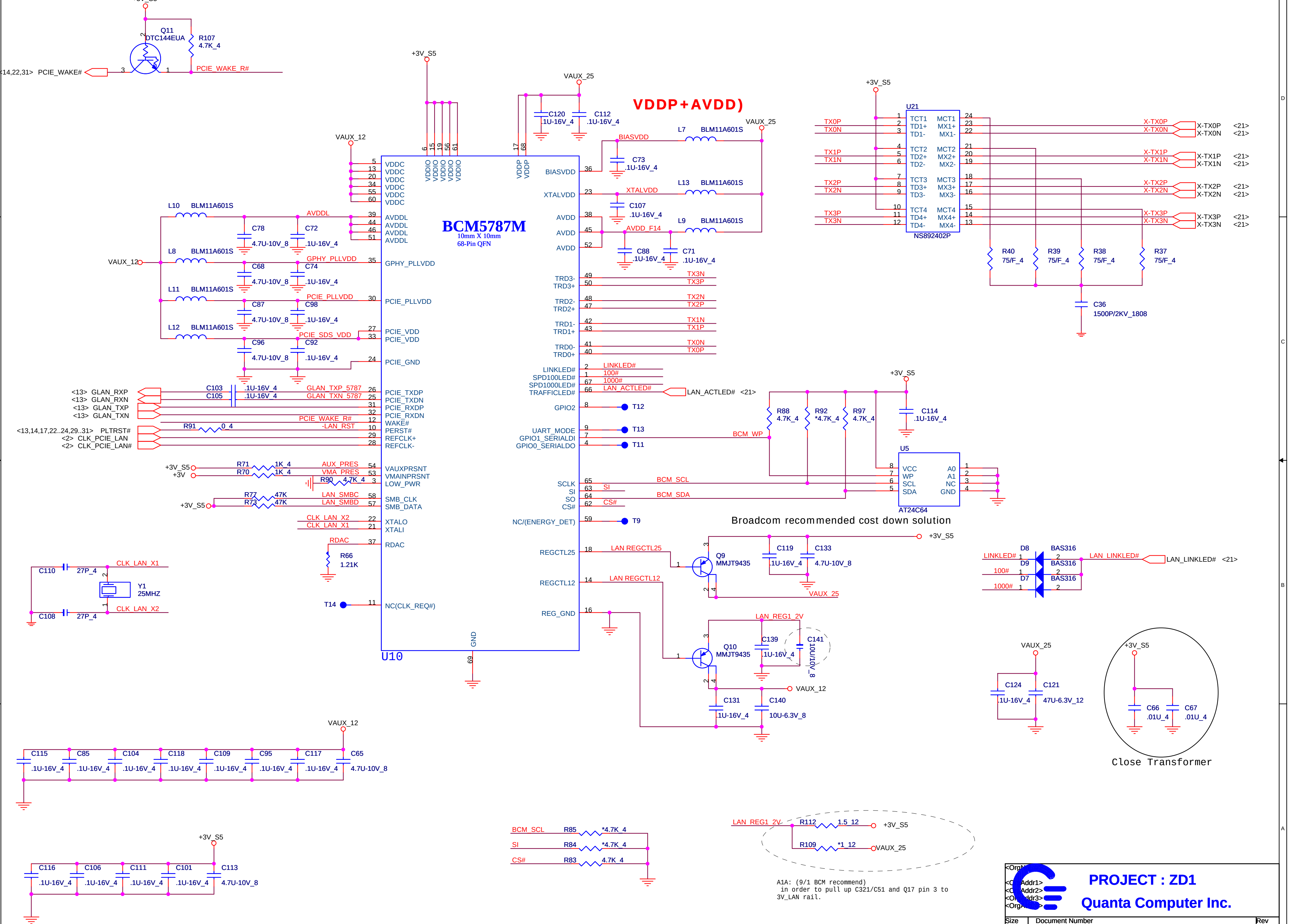
LAN



PROJECT : ZD1

Quanta Computer Inc.

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	BCM5787 LAN/TRANSFORMER	B

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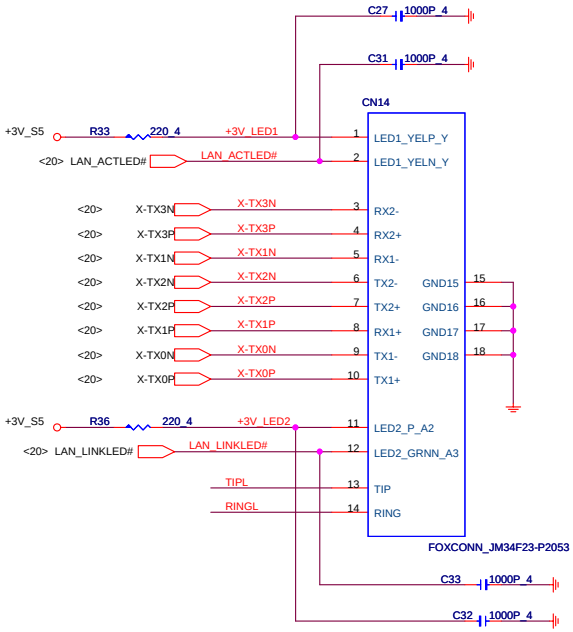
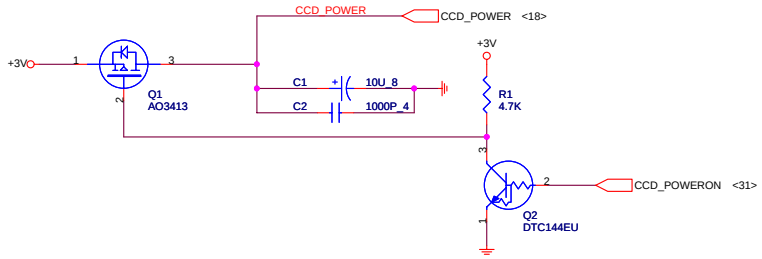
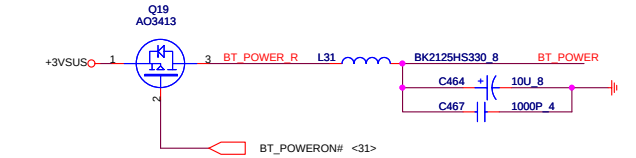
RJ45-11

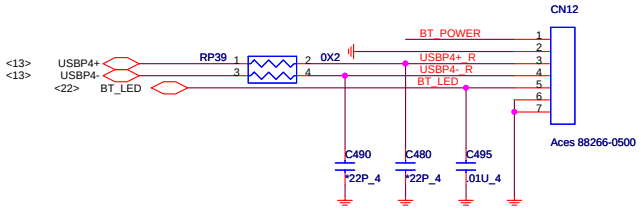


CAMERA MODULE CONNECTOR

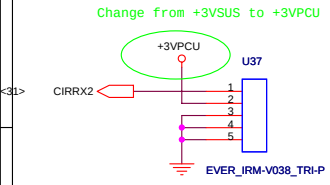


BLUETOOTH MODULE CONNECTOR

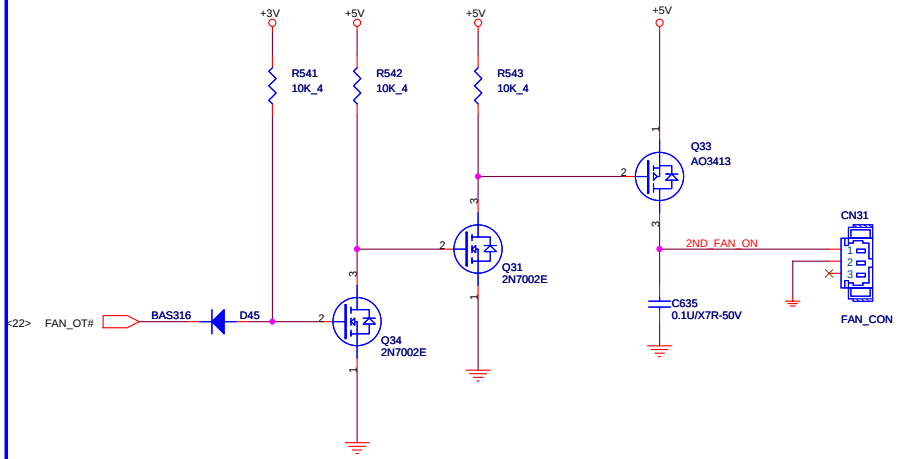




CIR



2nd FAN



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Quanta Computer Inc.

Size	Document Number	Rev
	BT/CCD/RJ45-11/CIR/2nd FAN	B

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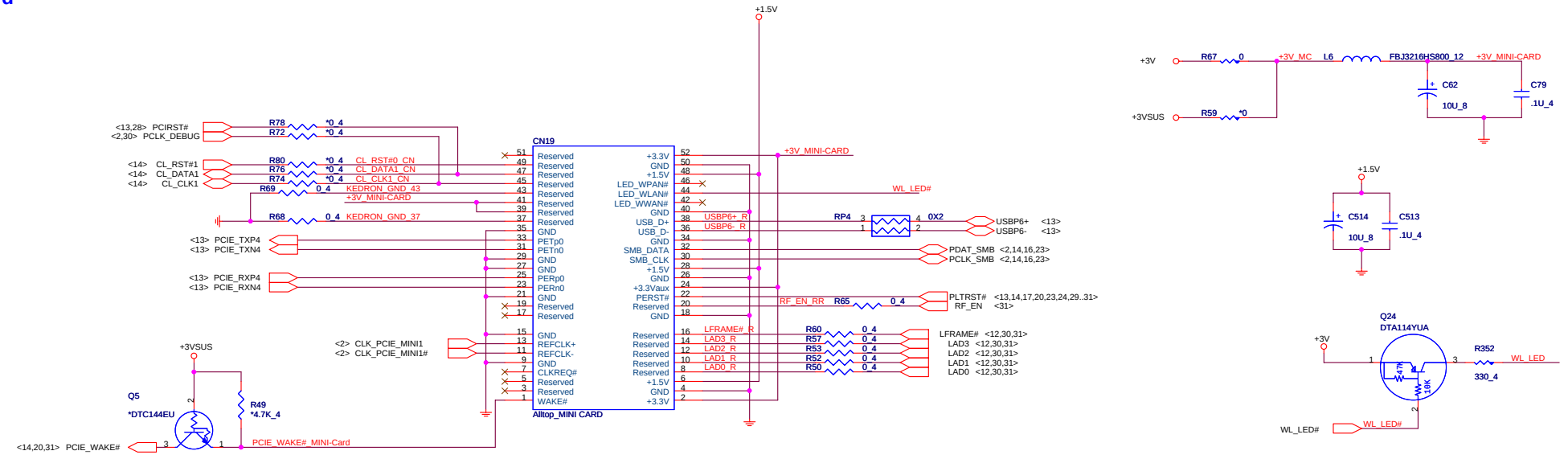
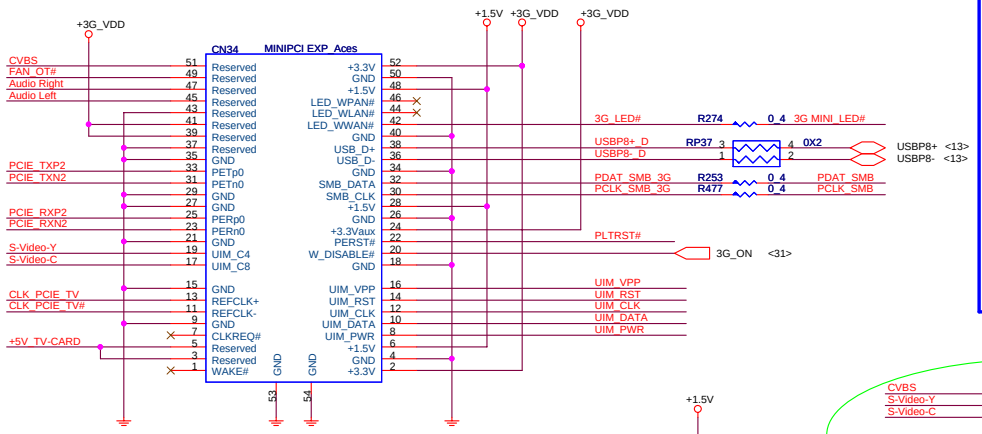
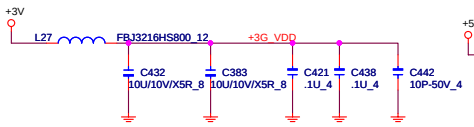
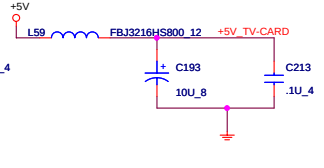
MINI-Card

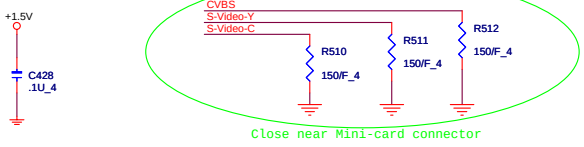


3G/TV MINI CARD

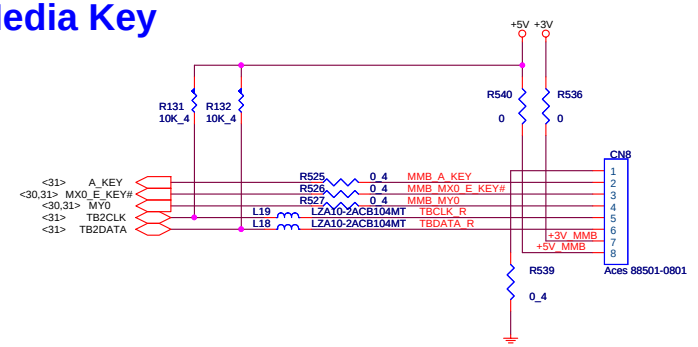


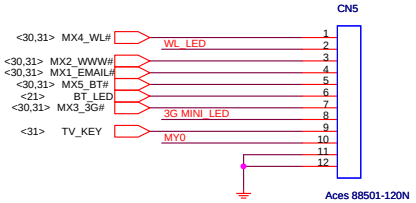


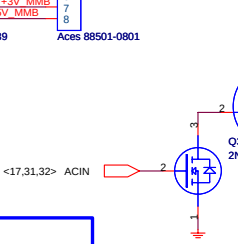


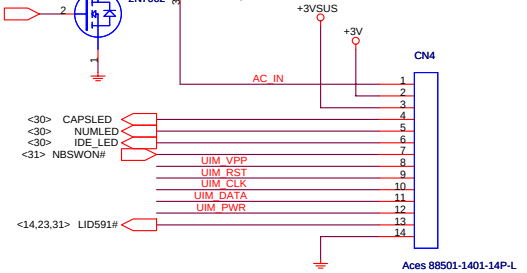


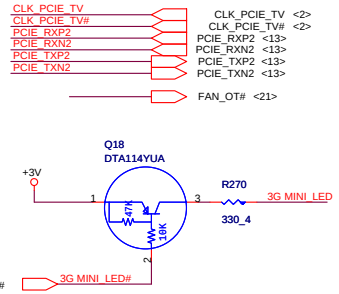
Media Key











PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI-E card/3G/TV/Media Key	B
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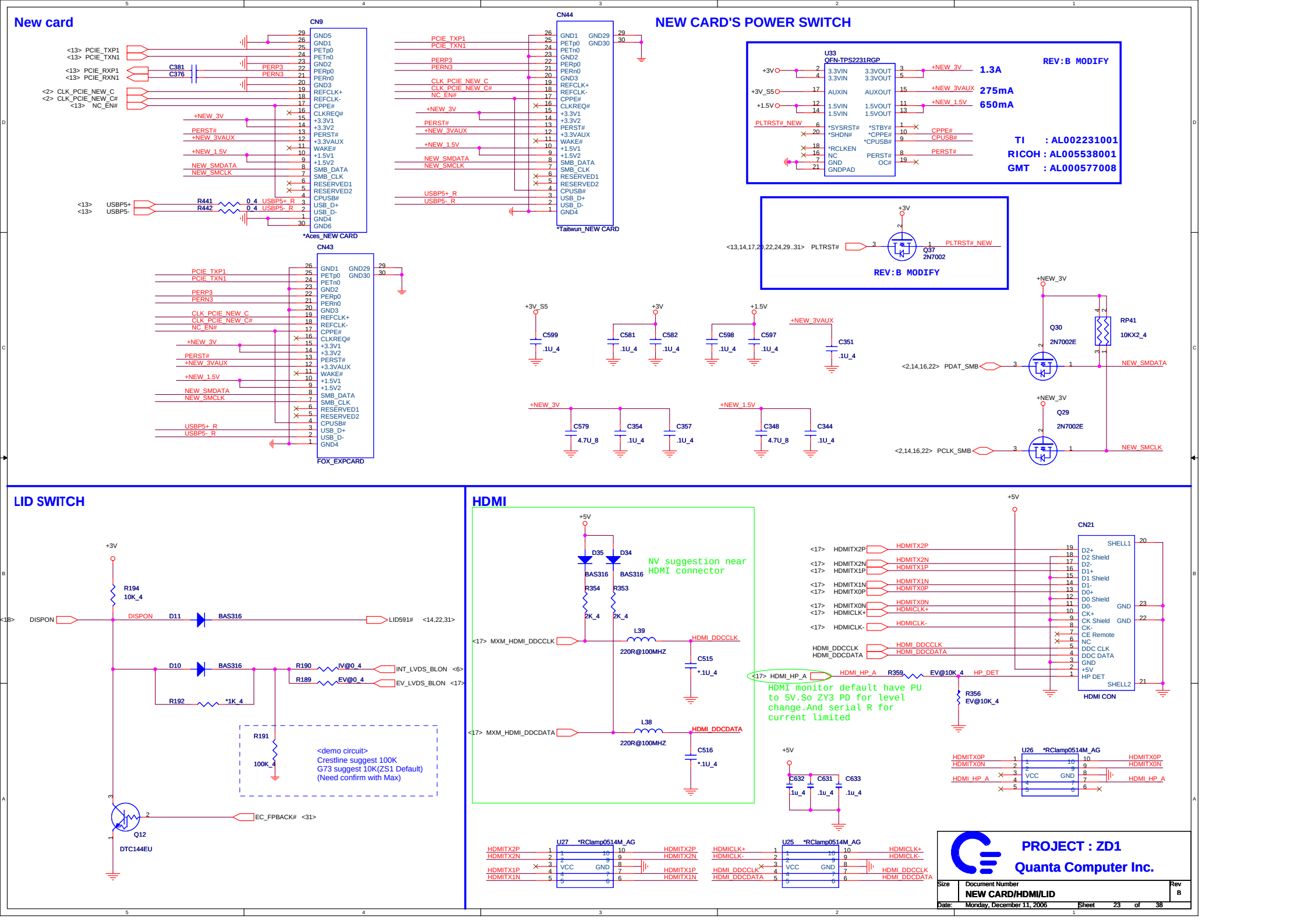
New card
CN9
*Aces_NEW CARD
CN44
*Taitwun_NEW CARD
CN43
FOX_EXPCARD
NEW CARD'S POWER SWITCH
U33
QFN-TPS2231RGP
REV:B MODIFY
1.3A
275mA
650mA
TI : AL002231001
RICOH : AL005538001
GMT : AL000577008
REV:B MODIFY
Q37
2N7002
Q30
2N7002E
Q29
2N7002E
RP41
10KX2_4
LID SWITCH
Q12
DTC144EU
<demo circuit>
Crestline suggest 100K
G73 suggest 10K(ZS1 Default)
(Need confirm with Max)
HDMI
NV suggestion near
HDMI connector
HDMI monitor default have PU
to 5V.So ZY3 PD for level
change.And serial R for
current limited
CN21
HDMI CON
U27 *RClamp0514M_AG
U25 *RClamp0514M_AG
U26 *RClamp0514M_AG
PROJECT : ZD1
Quanta Computer Inc.
Size
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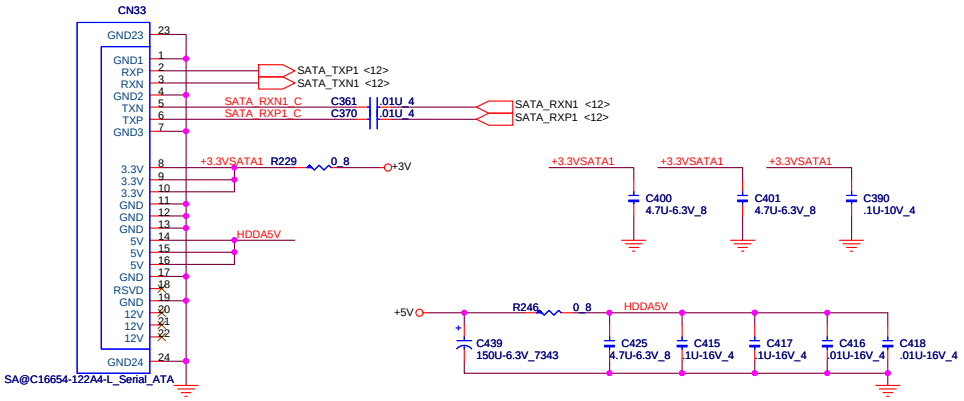
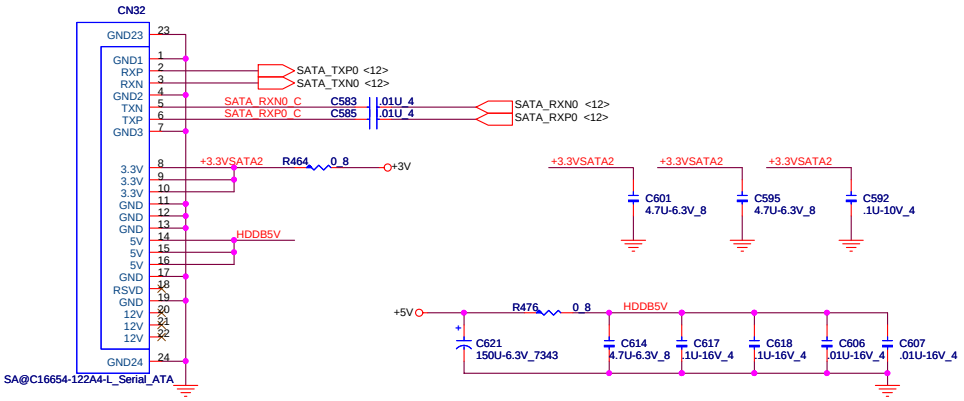
SATA HDD1

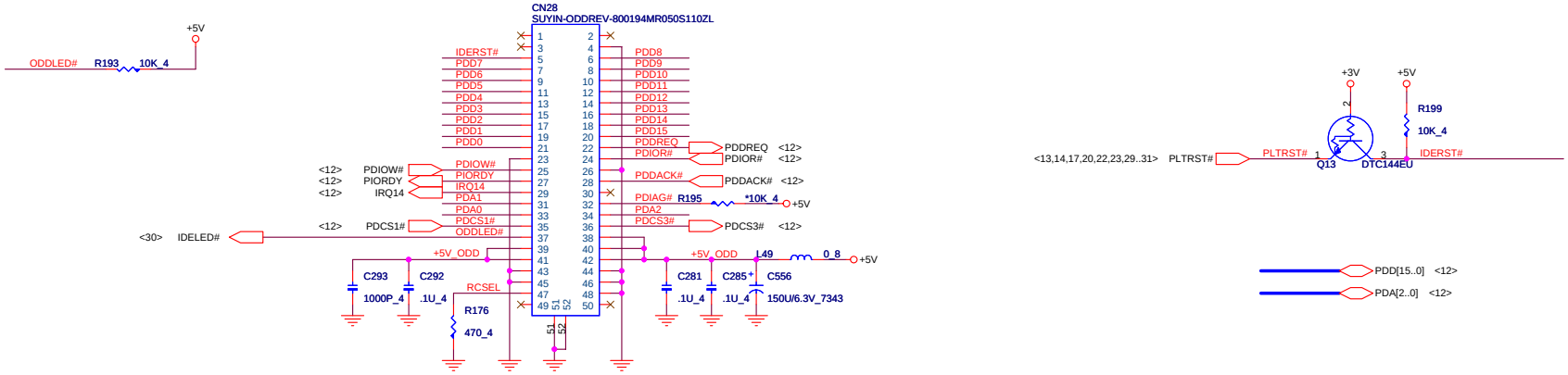


SATA HDD2

Main



ODD (PATA)



<OrgName>

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Quanta Computer Inc.

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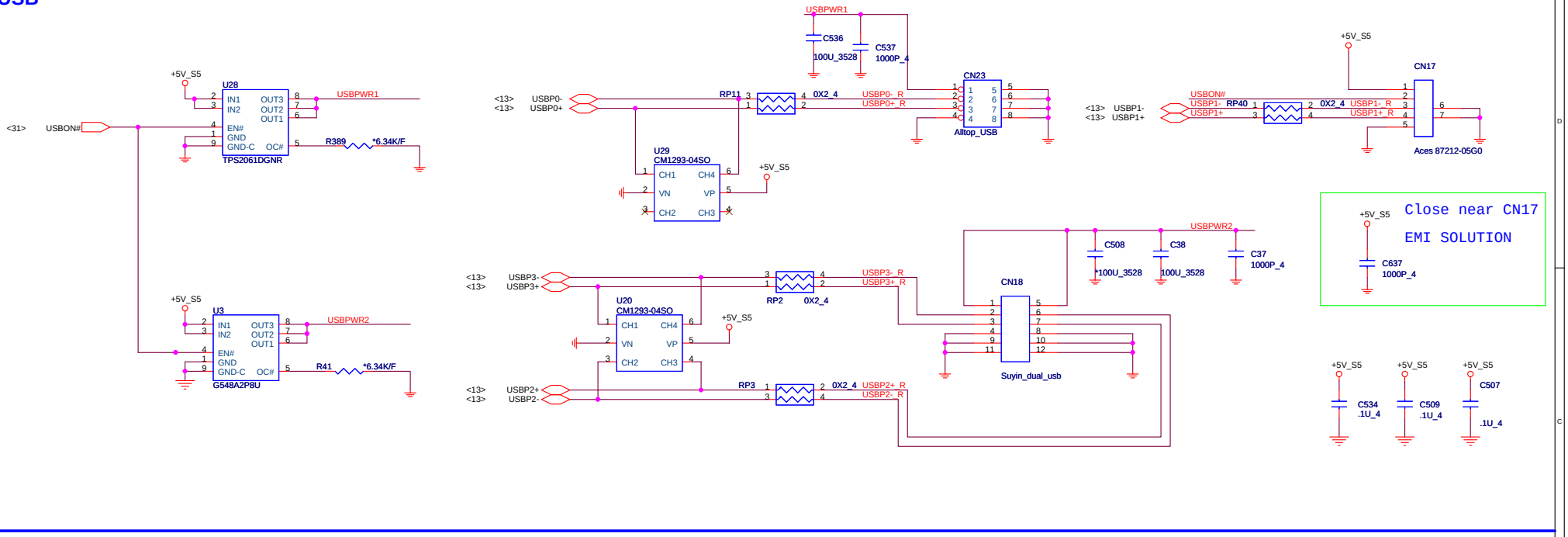
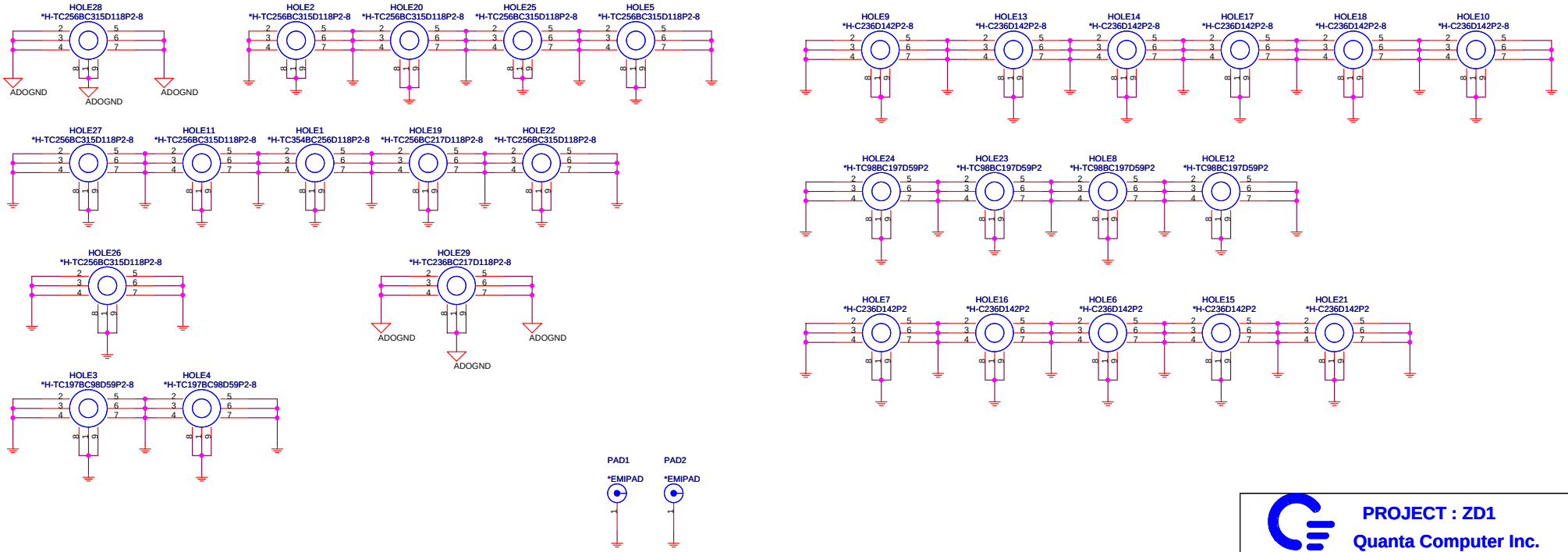
USB



HOLES



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Quanta Computer Inc.

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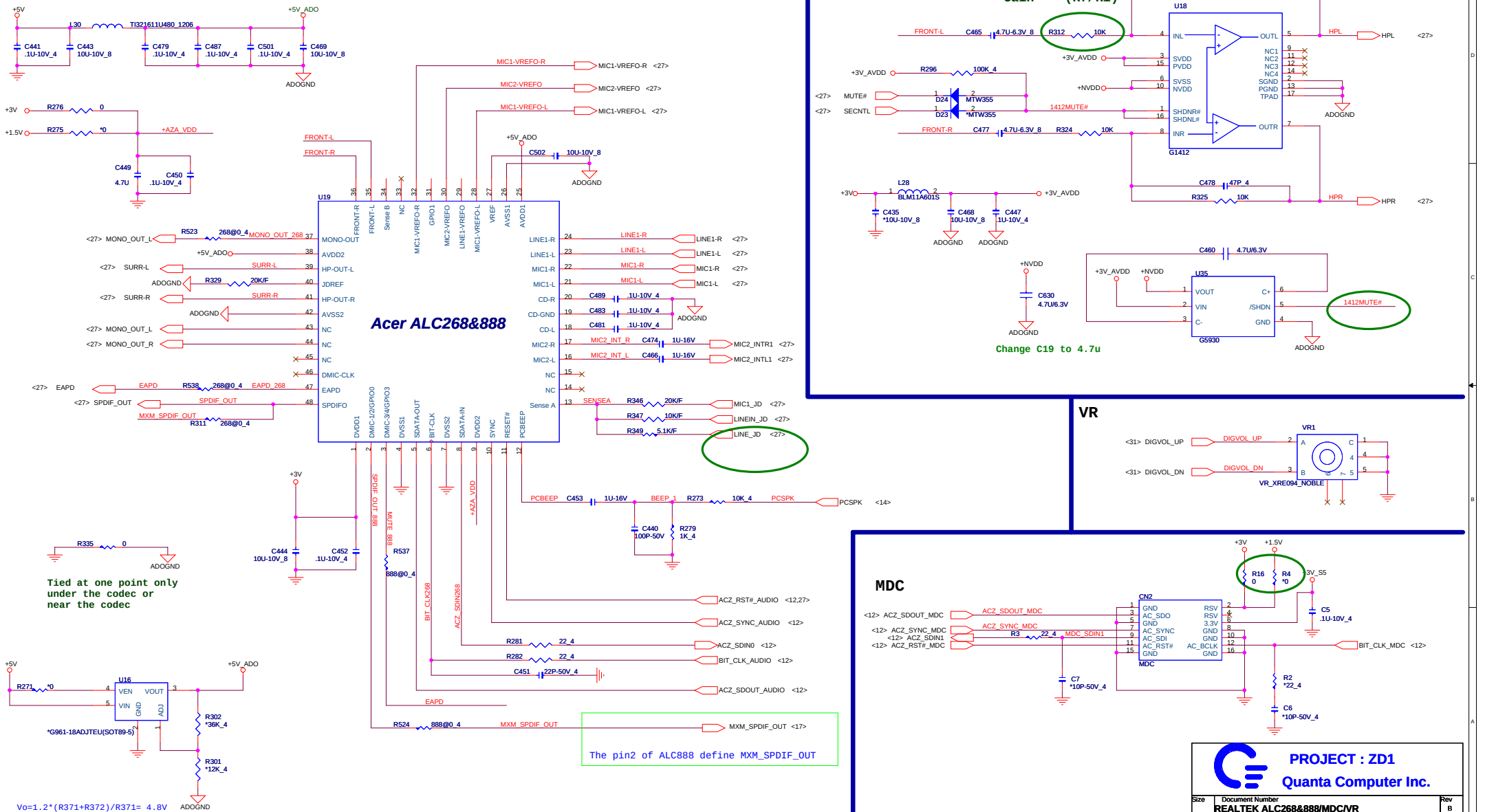
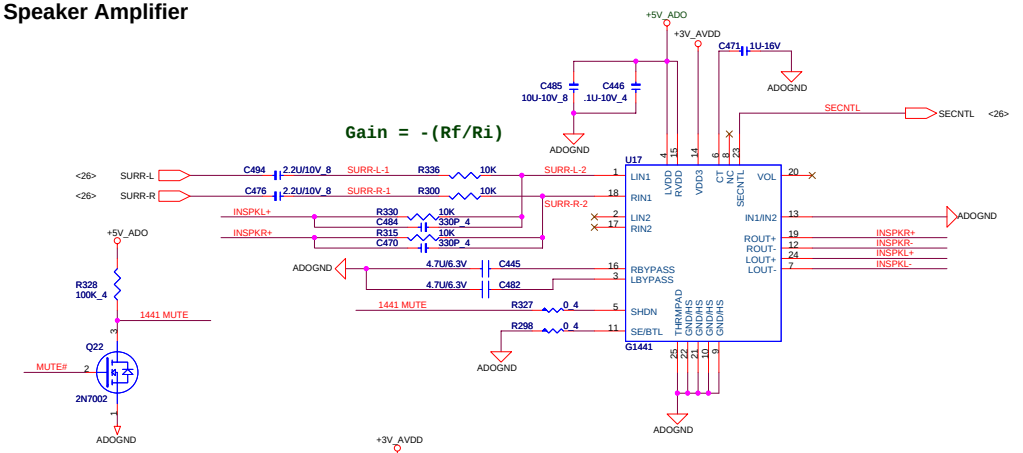
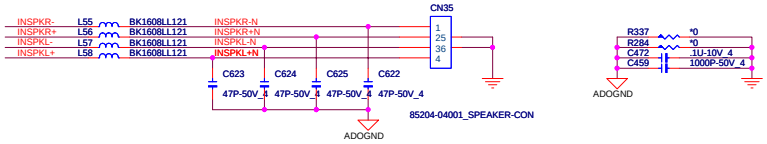
CODEC(ALC268)



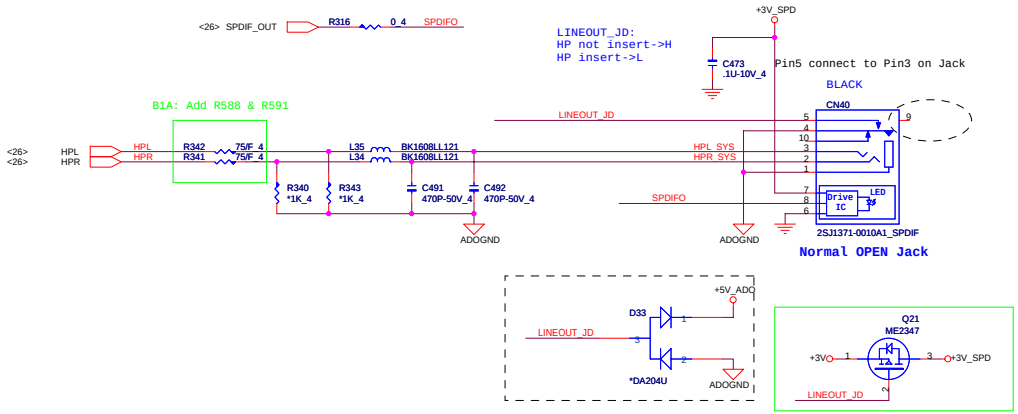
Speaker Amplifier

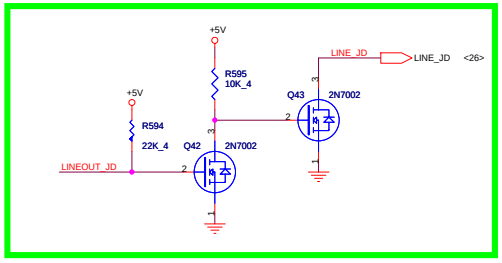


SPEAKER



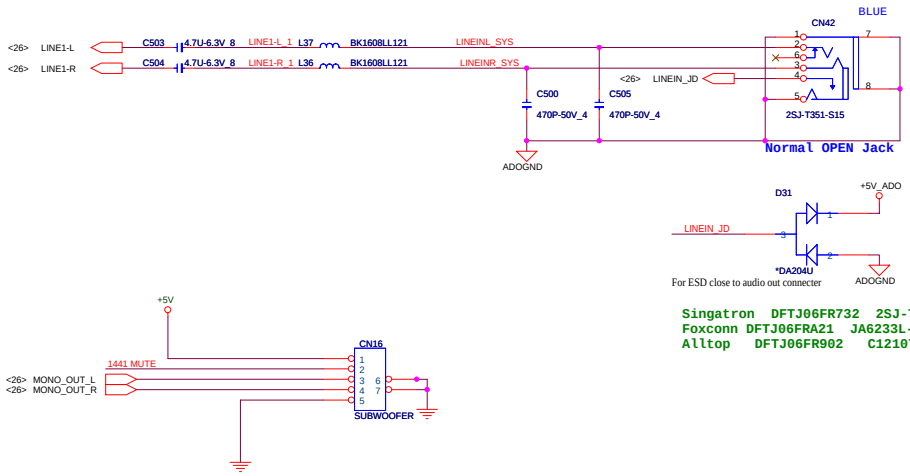
SYSTEM LINE OUT/SPDIF





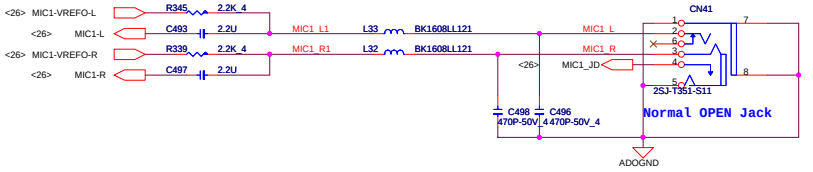
Foxconn DFTJ10FR470 2FB5441-BKMC-7F
Singatron DFTJ10FR437 2SJ1371-0010A1

SYSTEM LINE IN/SUBWOOFER

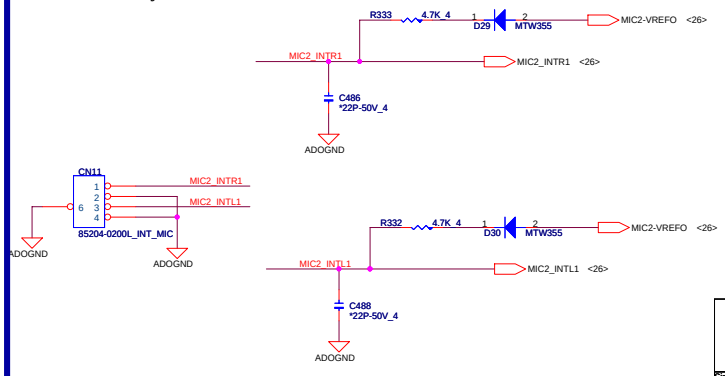


Singatron DFTJ06FR732 2SJ-T351-S15
Foxconn DFTJ06FRA21 JA6233L-U3T4-7F
Alltop DFTJ06FR902 C12107-906A9-L

MIC



INT MIC array



Singatron DFTJ06FR741 2SJ-T351-S11
Foxconn DFTJ06FRA39 JA6233L-P3T4-7F
Alltop DFTJ06FR899 C12107-D06A9-L

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Quanta Computer Inc.
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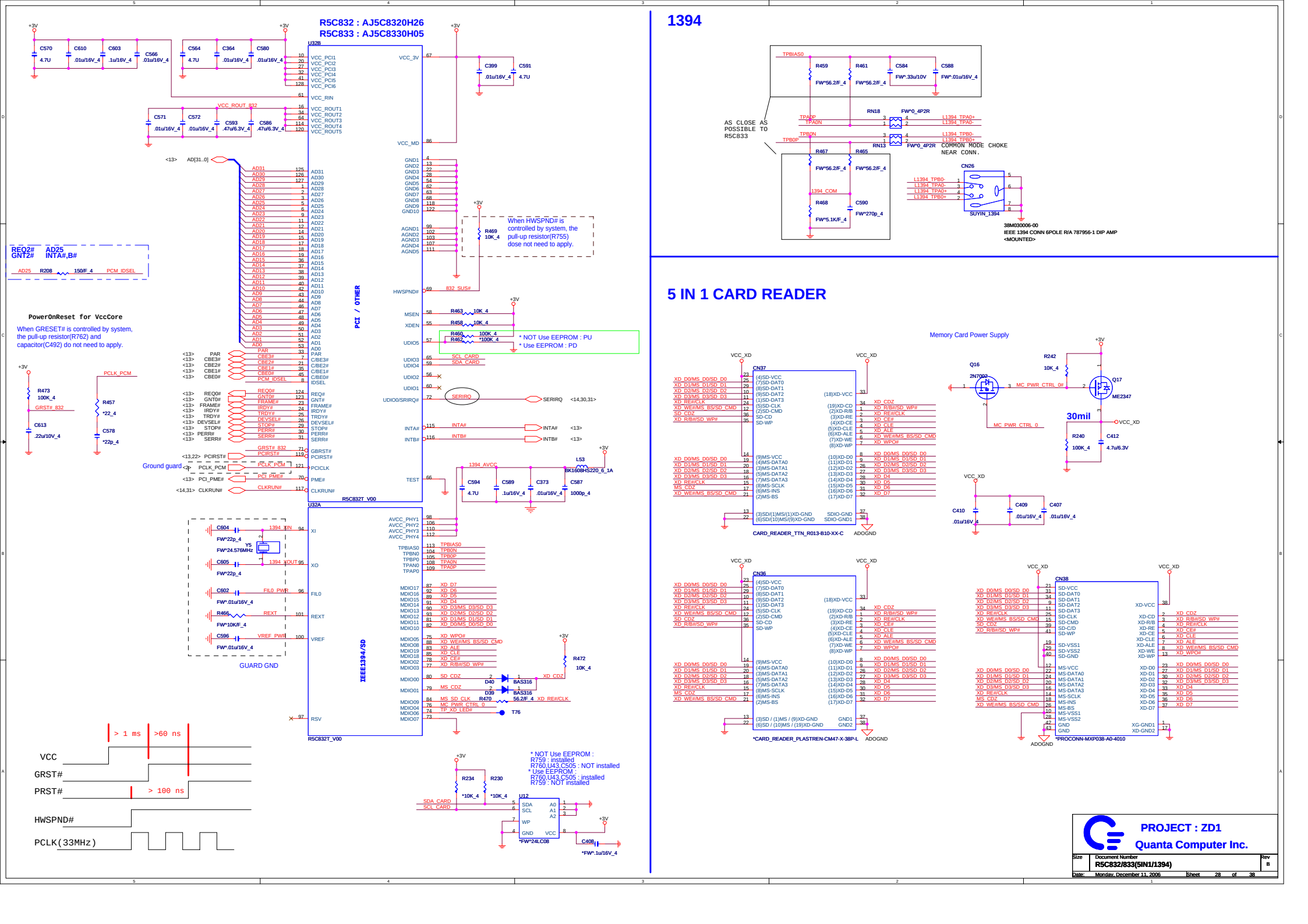
R5C832 : AJ5C8320H26
R5C833 : AJ5C8330H05
U32B
PCI / OTHER
U32A
IEEE1394/SD
R5C832T_V00
1394
TPBIAS0
R459
R461
C584
C588
FW^56.2/F_4
FW^.33u/10V
FW^.01u/16V_4
AS CLOSE AS POSSIBLE TO R5C833
RN18
RN13
FW^0_4P2R
COMMON MODE CHOKE NEAR CONN.
CN26
SUYIN_1394
38M030006-00
IEEE 1394 CONN 6POLE R/A 787956-1 DIP AMP
<MOUNTED>
5 IN 1 CARD READER
Memory Card Power Supply
CN37
CARD_READER_TTN_R013-B10-XX-C
CN36
*CARD_READER_PLASTREN-CM47-X-38P-L
CN38
*PROCONN-MXP038-A0-4010
Q16
2N7002
Q17
ME2347
30mil
PowerOnReset for VccCore
When GRESET# is controlled by system, the pull-up resistor(R762) and capacitor(C492) do not need to apply.
When HWSPND# is controlled by system, the pull-up resistor(R755) dose not need to apply.
* NOT Use EEPROM : PU
* Use EEPROM : PD
Ground guard
GUARD GND
* NOT Use EEPROM : R759 : installed R760,U43,C505 : NOT installed
* Use EEPROM : R760,U43,C505 : installed R759 : NOT installed
> 1 ms
>60 ns
> 100 ns
VCC
GRST#
PRST#
HWSPND#
PCLK(33MHz)
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Quanta Computer Inc.
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R5C832/833(5IN1/1394)
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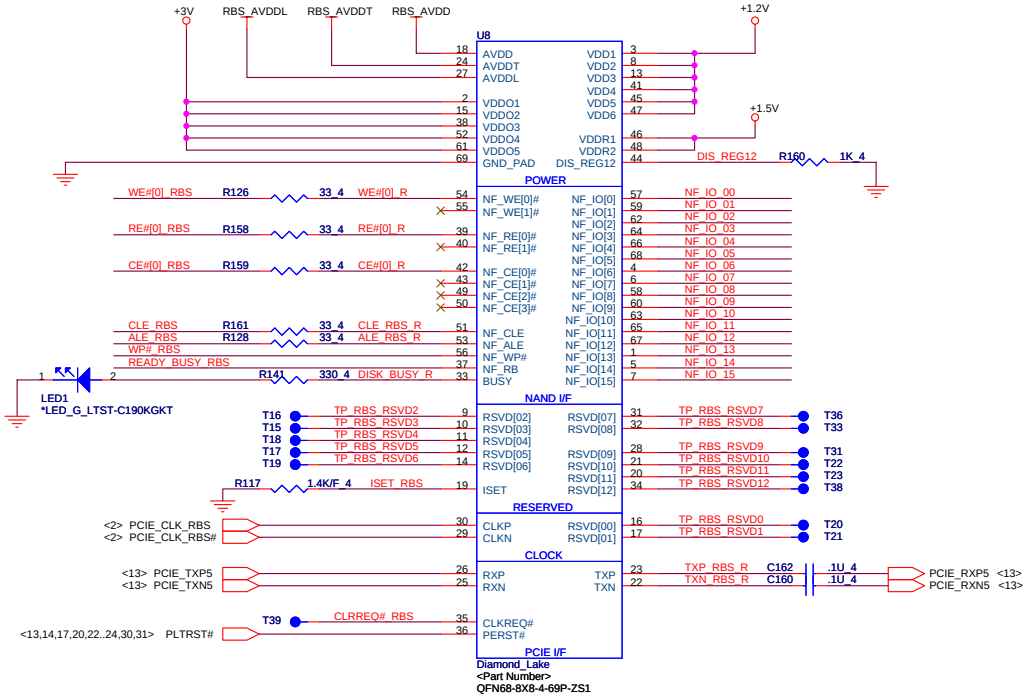
ROBSON

DIAMOND-LAKE ASIC

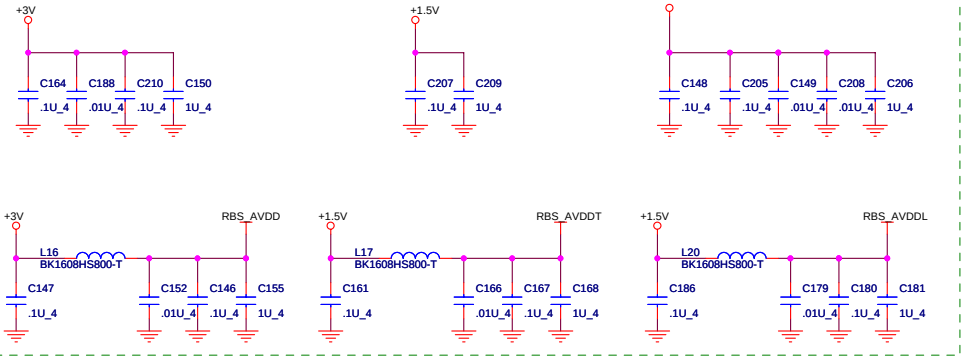


PLACE AS CLOSE AS POSSIBLE TO DIAMOND-LAKE ASIC.

NF_IO_00

R123
*10K_4

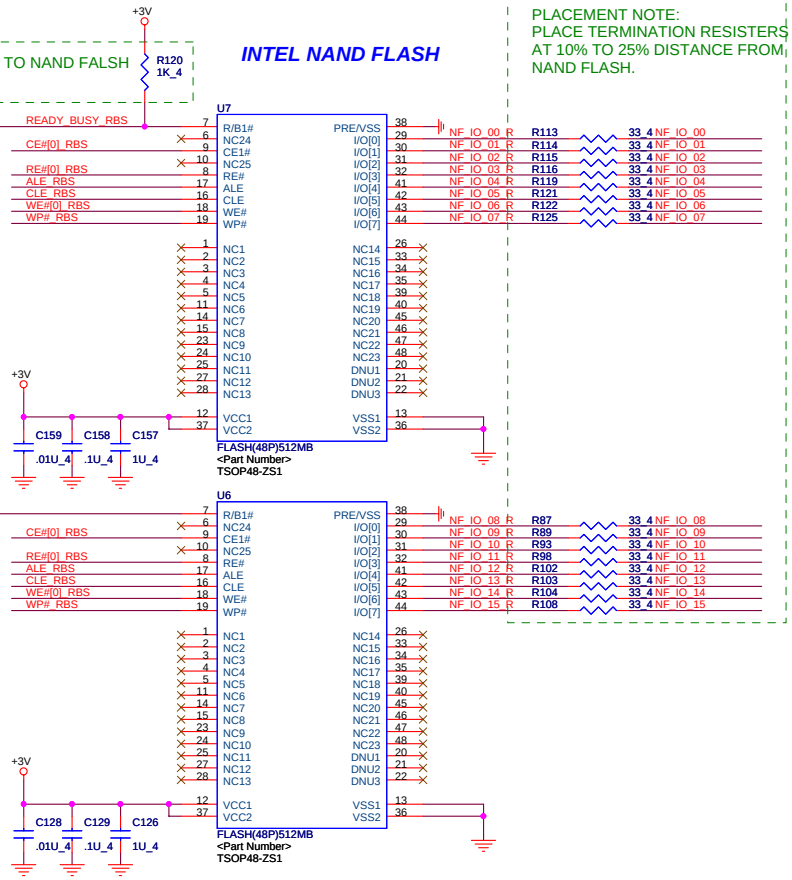
STUFF: INDICATES A 2KB VIRTUAL PAGE. => 256MB
DESTUFF: INDIACTESS A 4KB VIRTUAL PAGE => 512MB & 1024MB



PLACE CLOSE TO NAND FALSH

R120
1K_4

INTEL NAND FLASH



PLACEMENT NOTE:
PLACE TERMINATION RESISTERS AT 10% TO 25% DISTANCE FROM NAND FLASH.

LAYOUT NOTE:
ANY VIA ADDED BENEATH THE NAND FLASH NEEDS TO HAVE A SOLDERMASK ON IT.

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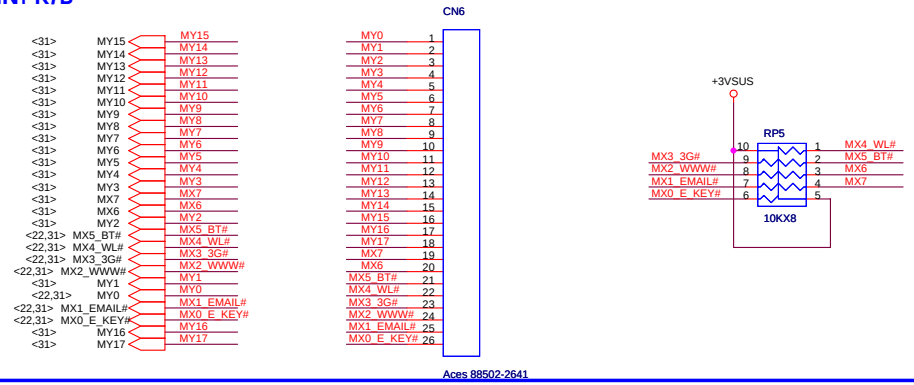
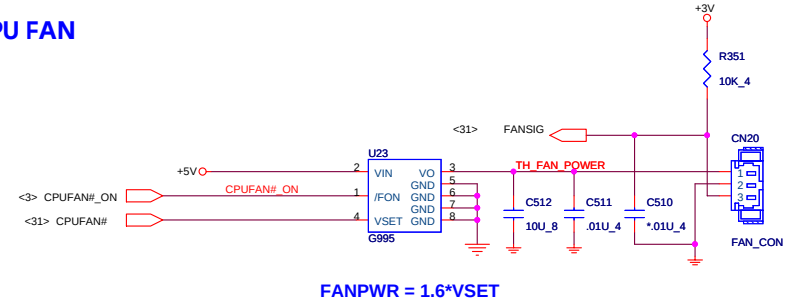
INT K/B

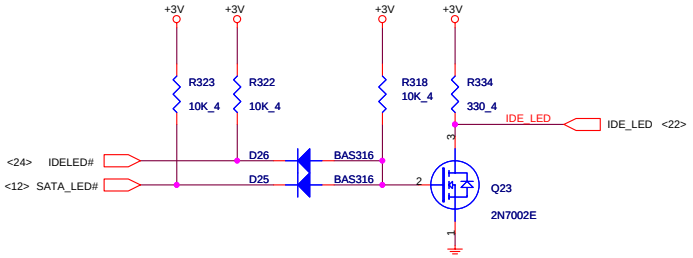


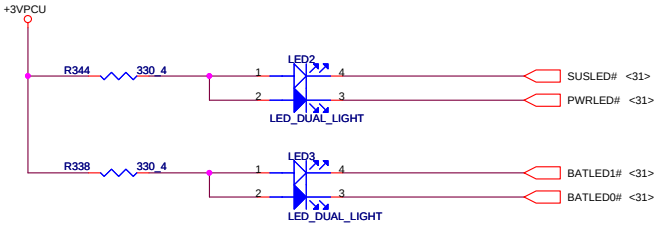
CPU FAN

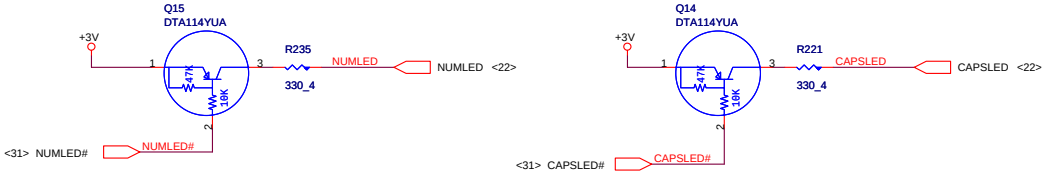


FANPWR = 1.6*VSET

LED

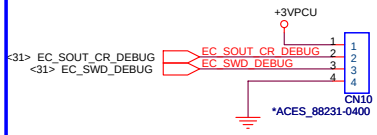




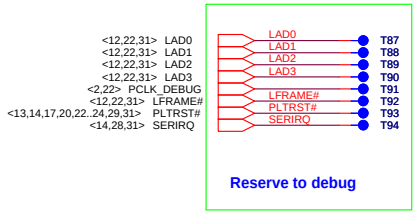


DEBUG PORT

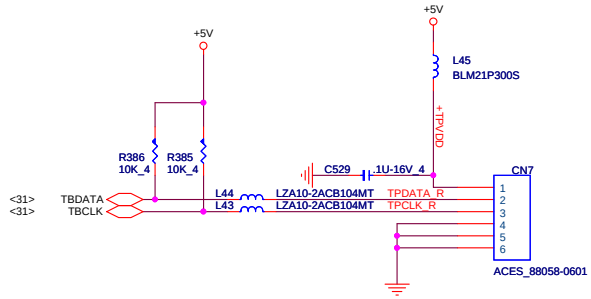
EC Debug Port



Reserved for LPC debug card



T/P



<OrgName>
<OrgAddress>
<OrgAddress>
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Quanta Computer Inc.

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	FAN,LED,KB,DEBUG PORT,TP	B
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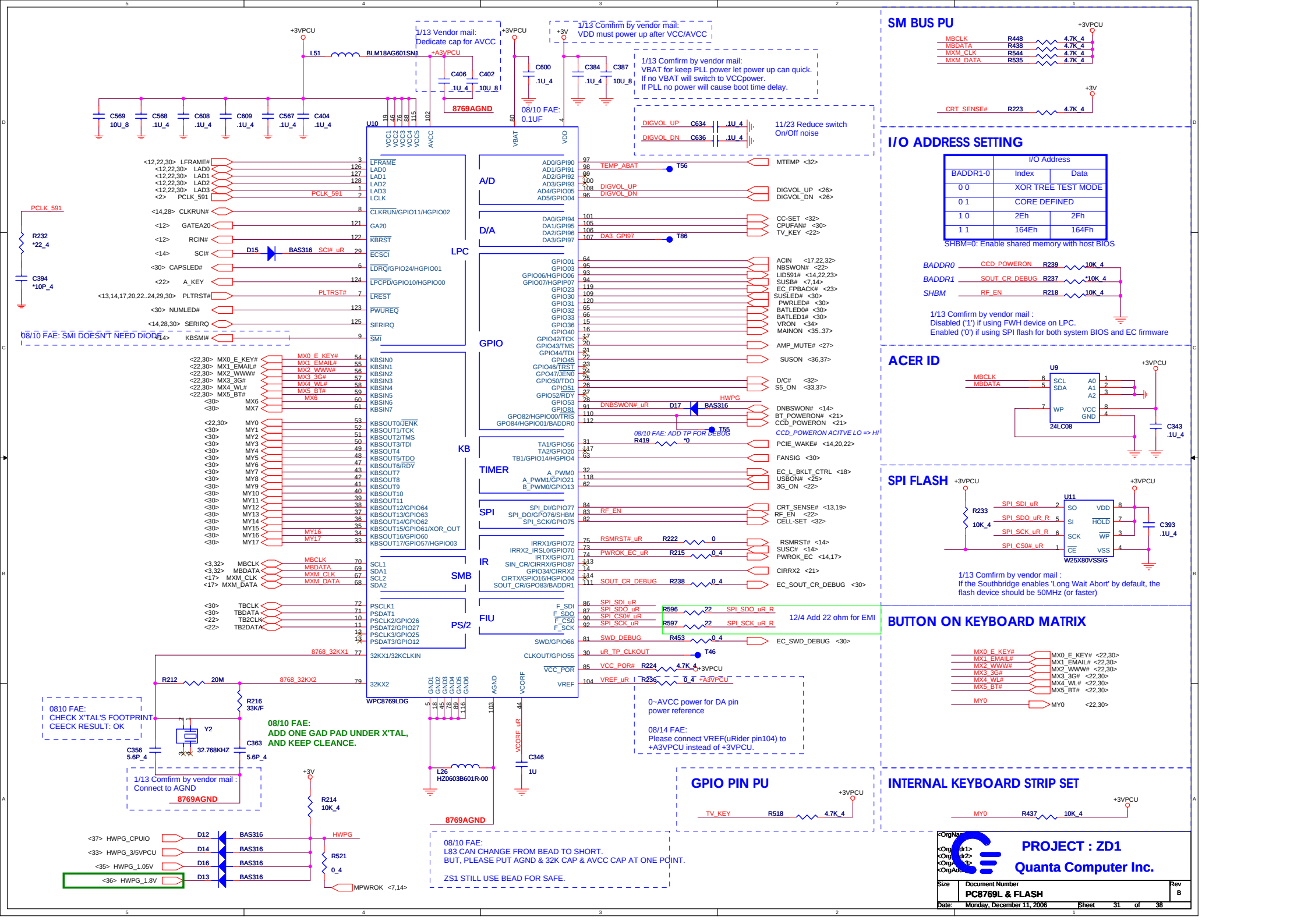
SM BUS PU
MBCLK R448 4.7K_4
MBDATA R438 4.7K_4
MXM_CLK R544 4.7K_4
MXM_DATA R535 4.7K_4
CRT_SENSE# R223 4.7K_4
I/O ADDRESS SETTING
BADDR1-0 | I/O Address: Index | Data
0 0 XOR TREE TEST MODE
0 1 CORE DEFINED
1 0 2Eh 2Fh
1 1 164Eh 164Fh
SHBM=0: Enable shared memory with host BIOS
BADDR0 CCD_POWERON R239 10K_4
BADDR1 SOUT_CR_DEBUG R237 *10K_4
SHBM RF_EN R218 10K_4
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
ACER ID
U9 24LC08 MBCLK MBDATA C343 .1U_4
SPI FLASH
U11 W25X80VSSIG R233 10K_4 C393 .1U_4
SPI_SDI_uR SPI_SDO_uR_R SPI_SCK_uR_R SPI_CS0#_uR
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)
BUTTON ON KEYBOARD MATRIX
MX0_E_KEY# MX1_EMAIL# MX2_WWW# MX3_3G# MX4_WL# MX5_BT# MY0
GPIO PIN PU
TV_KEY R518 4.7K_4
INTERNAL KEYBOARD STRIP SET
MY0 R437 10K_4
1/13 Vendor mail: Dedicate cap for AVCC
1/13 Comfirm by vendor mail: VDD must power up after VCC/AVCC
1/13 Comfirm by vendor mail: VBAT for keep PLL power let power up can quick. If no VBAT will switch to VCCpower. If PLL no power will cause boot time delay.
08/10 FAE: 0.1UF
11/23 Reduce switch On/Off noise
08/10 FAE: SMI DOESN'T NEED DIODE
08/10 FAE: ADD TP FOR DEBUG
CCD_POWERON ACITVE LO => HI
12/4 Add 22 ohm for EMI
0~AVCC power for DA pin power reference
08/14 FAE: Please connect VREF(uRider pin104) to +A3VPCU instead of +3VPCU.
0810 FAE: CHECK X'TAL'S FOOTPRINT CEECK RESULT: OK
08/10 FAE: ADD ONE GAD PAD UNDER X'TAL, AND KEEP CLEANCE.
1/13 Comfirm by vendor mail : Connect to AGND
08/10 FAE: L83 CAN CHANGE FROM BEAD TO SHORT. BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.
U10 WPC8769LDG
LPC A/D D/A GPIO KB TIMER SPI IR SMB PS/2 FIU
8769AGND
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Quanta Computer Inc.
PC8769L & FLASH
Rev B
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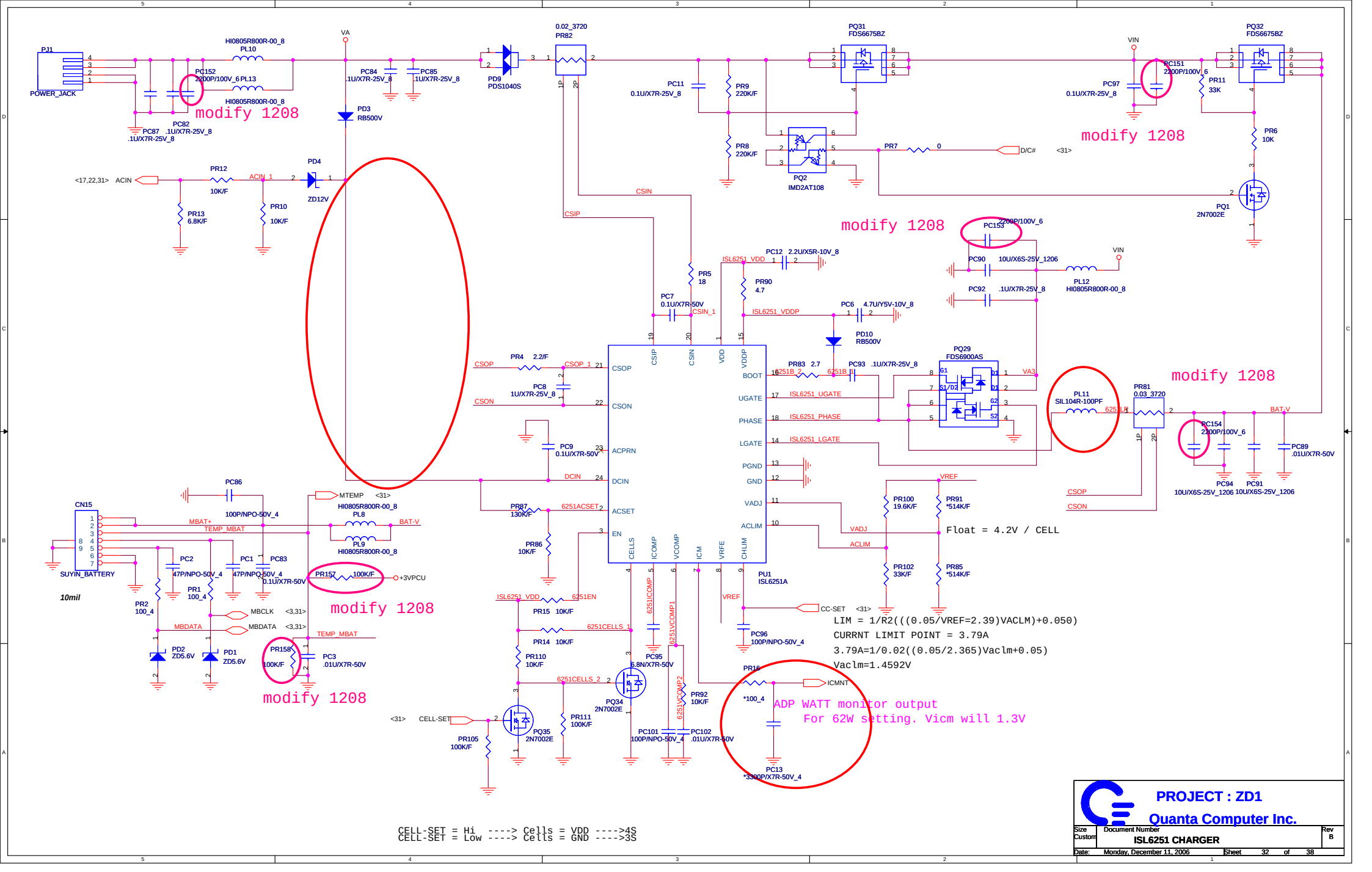
modify 1208
modify 1208
modify 1208
modify 1208
modify 1208
Float = 4.2V / CELL
LIM = 1/R2(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT = 3.79A
3.79A=1/0.02((0.05/2.365)Vaclm+0.05)
Vaclm=1.4592V
ADP WATT monitor output
For 62W setting. Vicm will 1.3V
CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S
PROJECT : ZD1
Quanta Computer Inc.
ISL6251 CHARGER
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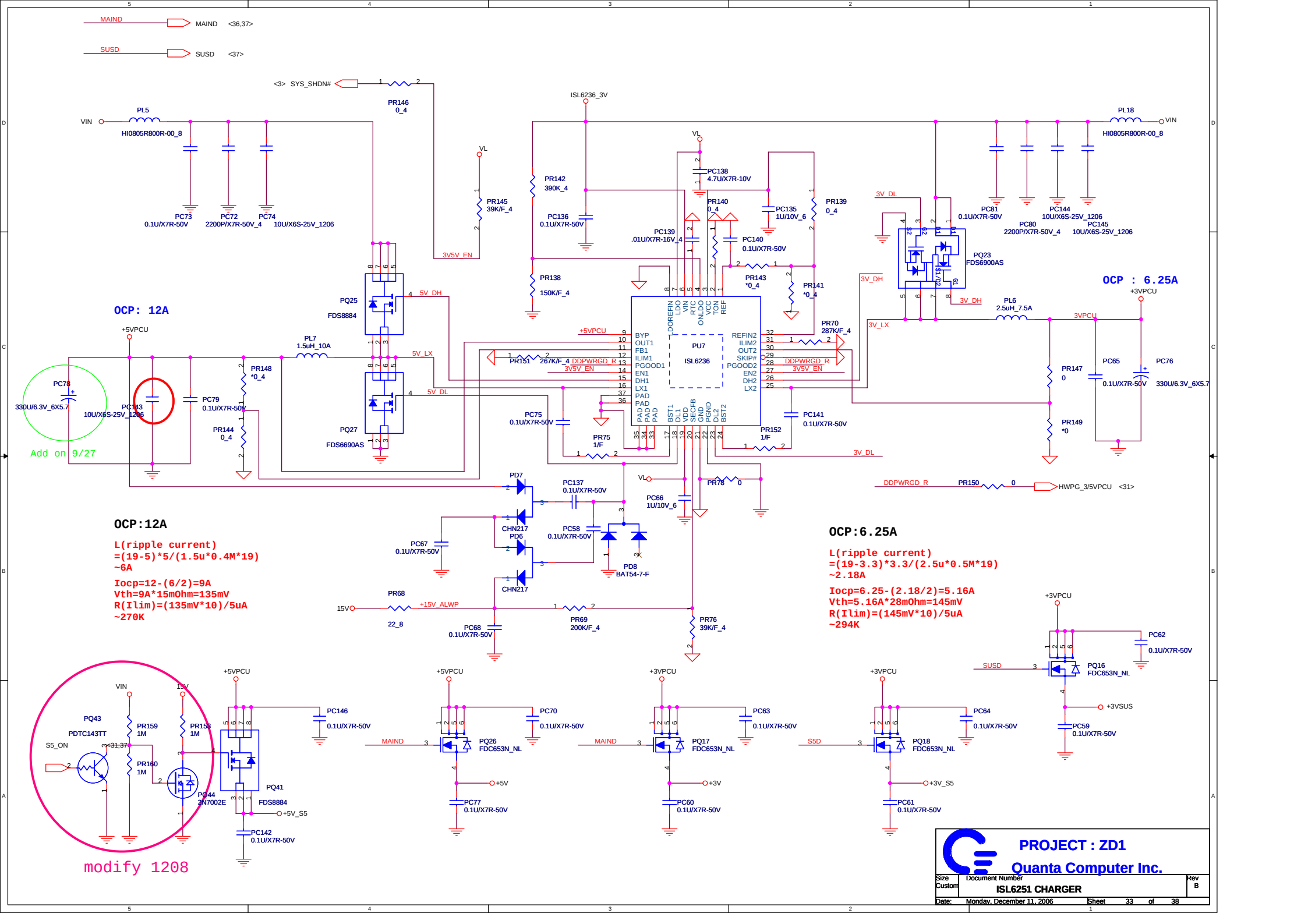
MAIND
MAIND <36,37>
SUSD
SUSD <37>
<3> SYS_SHDN#
ISL6236_3V
VIN
PL5
HI0805R800R-00_8
PR146
0_4
PR142
390K_4
PR145
39K/F_4
3V5V_EN
PR138
150K/F_4
PC73
0.1U/X7R-50V
PC72
2200P/X7R-50V_4
PC74
10U/X6S-25V_1206
PC136
0.1U/X7R-50V
PC138
4.7U/X7R-10V
PR140
0_4
PC135
1U/10V_6
PR139
0_4
PC139
.01U/X7R-16V_4
PC140
0.1U/X7R-50V
PR143
*0_4
PR141
*0_4
PL18
HI0805R800R-00_8
PC81
0.1U/X7R-50V
PC80
2200P/X7R-50V_4
PC144
10U/X6S-25V_1206
PC145
10U/X6S-25V_1206
PQ23
FDS6900AS
3V_DL
3V_DH
3V_LX
OCP : 6.25A
OCP: 12A
+5VPCU
+3VPCU
PL7
1.5uH_10A
PL6
2.5uH_7.5A
PR148
*0_4
PR144
0_4
PC78
330U/6.3V_6X5.7
PC143
10U/X6S-25V_1206
PC79
0.1U/X7R-50V
PQ25
FDS8884
PQ27
FDS6690AS
5V_DH
5V_LX
5V_DL
PR70
287K/F_4
PR151
267K/F_4
DDPWRGD_R
PU7
ISL6236
PC75
0.1U/X7R-50V
PR75
1/F
PR152
1/F
PC141
0.1U/X7R-50V
PR147
0
PR149
*0
PC65
0.1U/X7R-50V
PC76
330U/6.3V_6X5.7
PR150
0
HWPG_3/5VPCU <31>
Add on 9/27
PD7
CHN217
PD6
CHN217
PC137
0.1U/X7R-50V
PC66
1U/10V_6
PR78
0
PC67
0.1U/X7R-50V
PC58
0.1U/X7R-50V
PD8
BAT54-7-F
PR68
22_8
15V
+15V_ALWP
PC68
0.1U/X7R-50V
PR69
200K/F_4
PR76
39K/F_4
OCP:12A
L(ripple current)
=(19-5)*5/(1.5u*0.4M*19)
~6A
Iocp=12-(6/2)=9A
Vth=9A*15mOhm=135mV
R(Ilim)=(135mV*10)/5uA
~270K
OCP:6.25A
L(ripple current)
=(19-3.3)*3.3/(2.5u*0.5M*19)
~2.18A
Iocp=6.25-(2.18/2)=5.16A
Vth=5.16A*28mOhm=145mV
R(Ilim)=(145mV*10)/5uA
~294K
PQ43
PDTC143TT
S5_ON
PR159
1M
PR158
1M
PR160
1M
PQ44
2N7002E
PQ41
FDS8884
+5V_S5
PC142
0.1U/X7R-50V
PC146
0.1U/X7R-50V
PQ26
FDC653N_NL
PC70
0.1U/X7R-50V
+5V
PC77
0.1U/X7R-50V
PQ17
FDC653N_NL
PC63
0.1U/X7R-50V
+3V
PC60
0.1U/X7R-50V
PQ18
FDC653N_NL
PC64
0.1U/X7R-50V
+3V_S5
PC61
0.1U/X7R-50V
PQ16
FDC653N_NL
PC62
0.1U/X7R-50V
+3VSUS
PC59
0.1U/X7R-50V
modify 1208
PROJECT : ZD1
Quanta Computer Inc.
Size
Custom
Document Number
ISL6251 CHARGER
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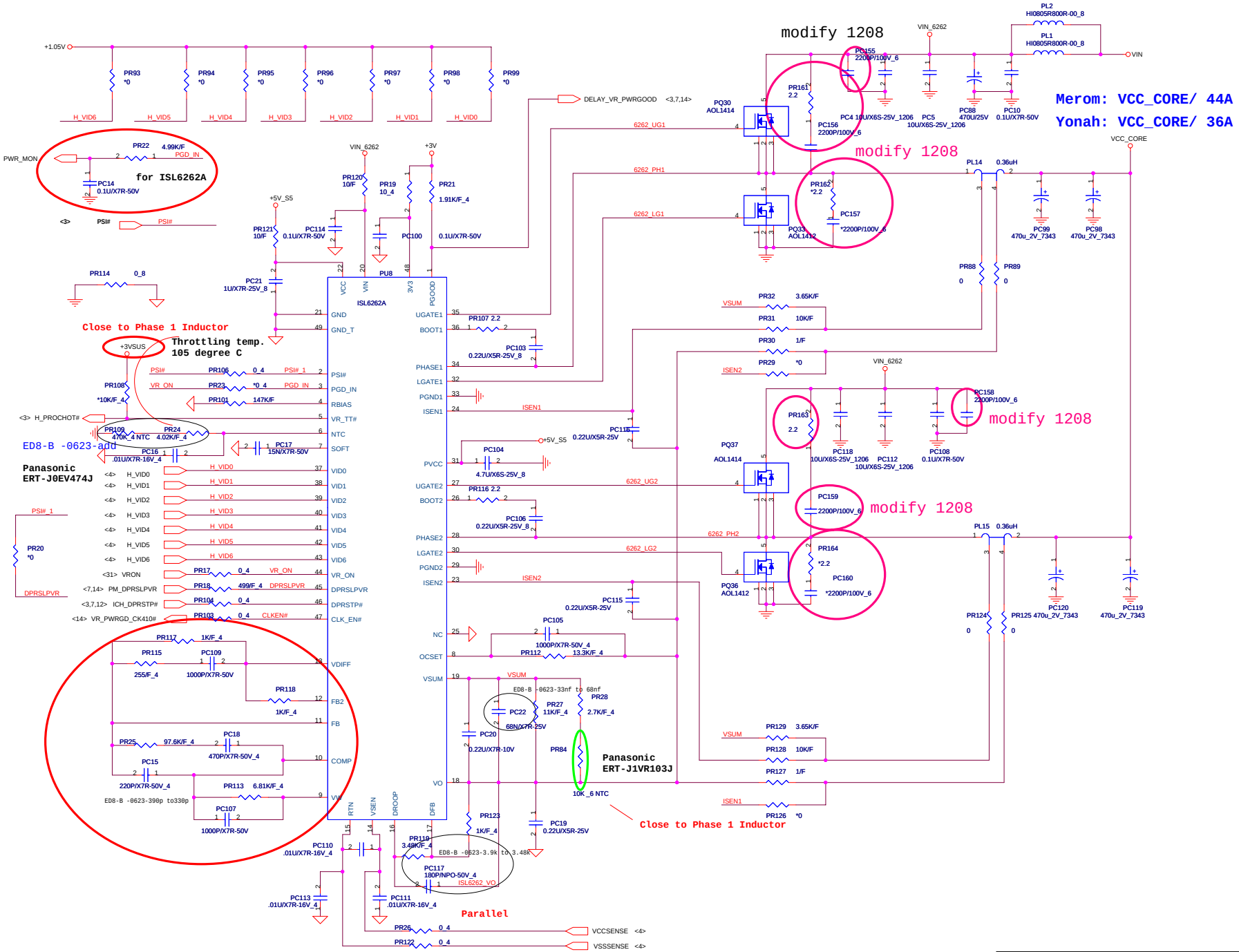
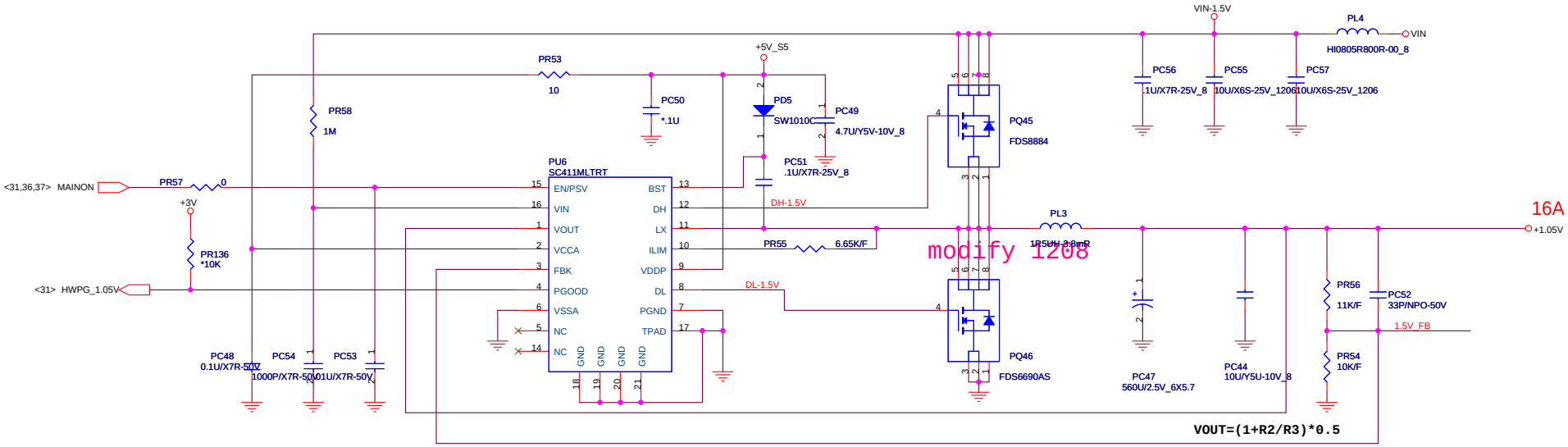

modify 1208
Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A
for ISL6262A
Close to Phase 1 Inductor
Throttling temp.
105 degree C
ED8-B -0623-add
Panasonic
ERT-J0EV474J
Panasonic
ERT-J1VR103J
Parallel
Close to Phase 1 Inductor
ISL6262A
VCC_CORE
VIN_6262
PROJECT : ZD1
Quanta Computer Inc.
CPU CORE(ISL6262)
Monday, December 11, 2006



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Quanta Computer Inc.		
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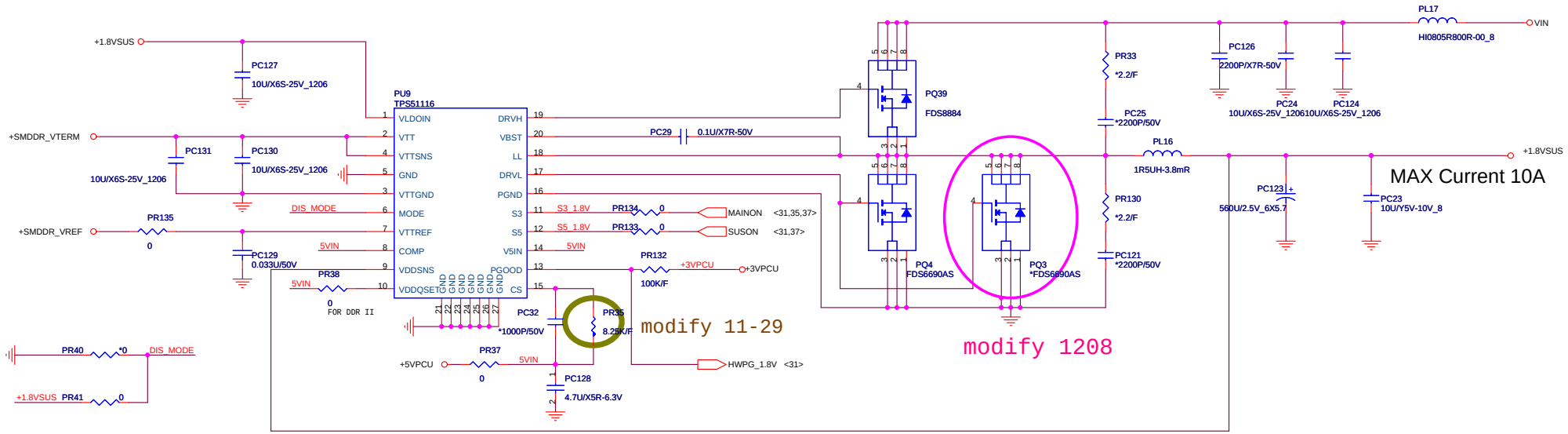

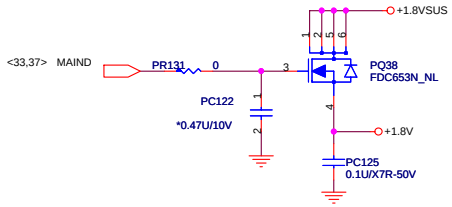

MAX Current 3.5A

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	DDR 1.8V(TPS51116)	B
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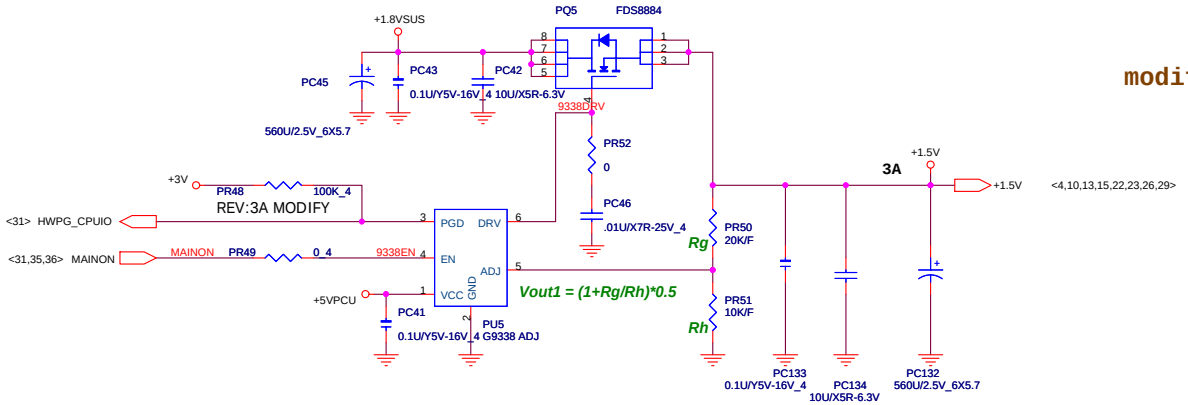
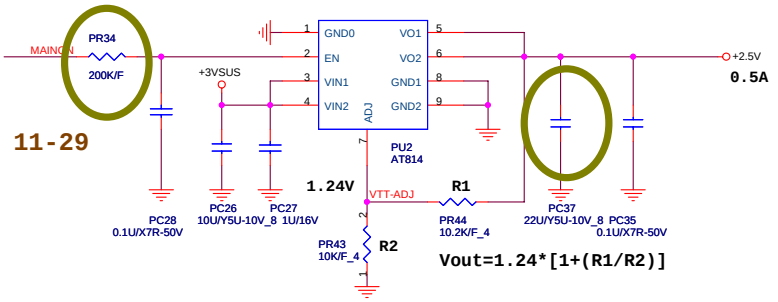
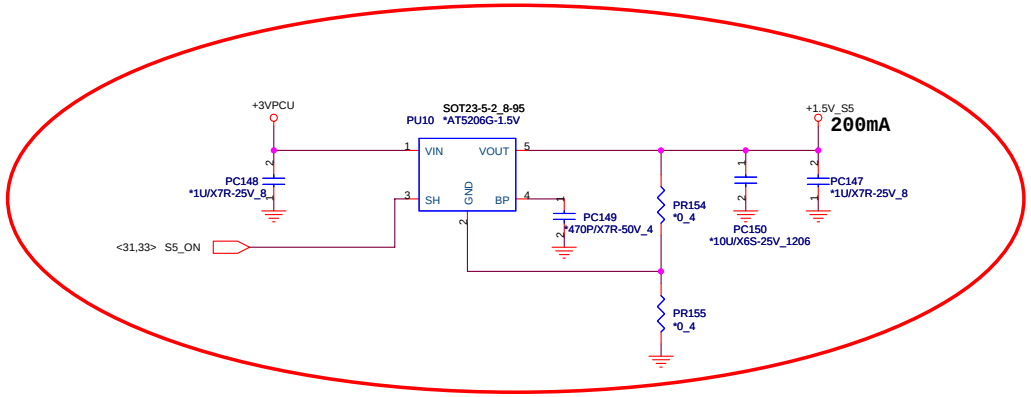
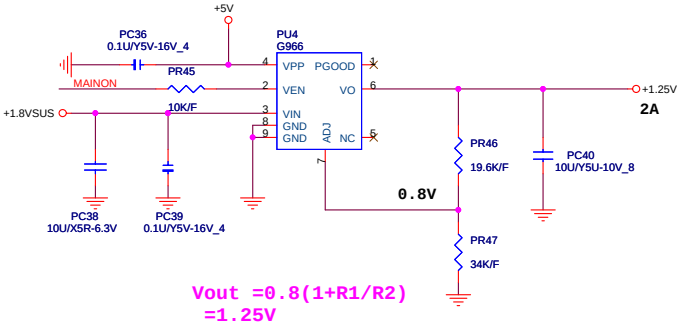
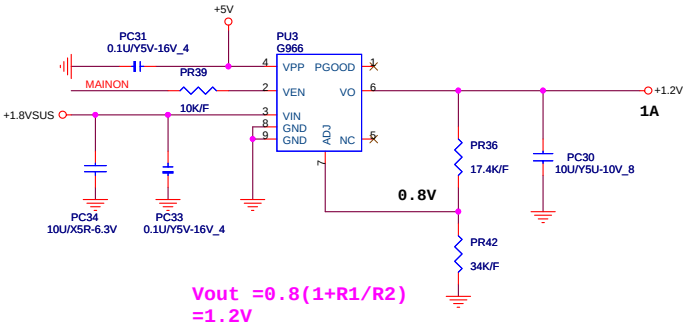


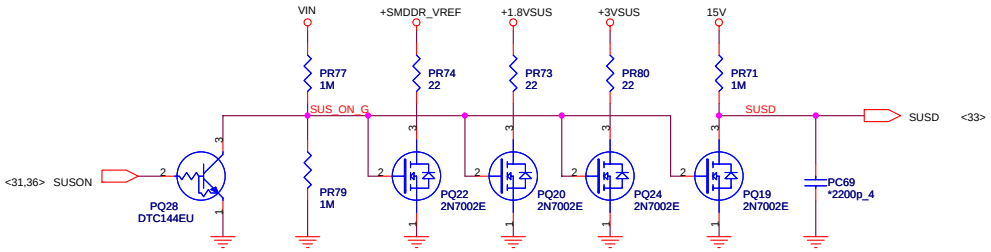
modify 11-29



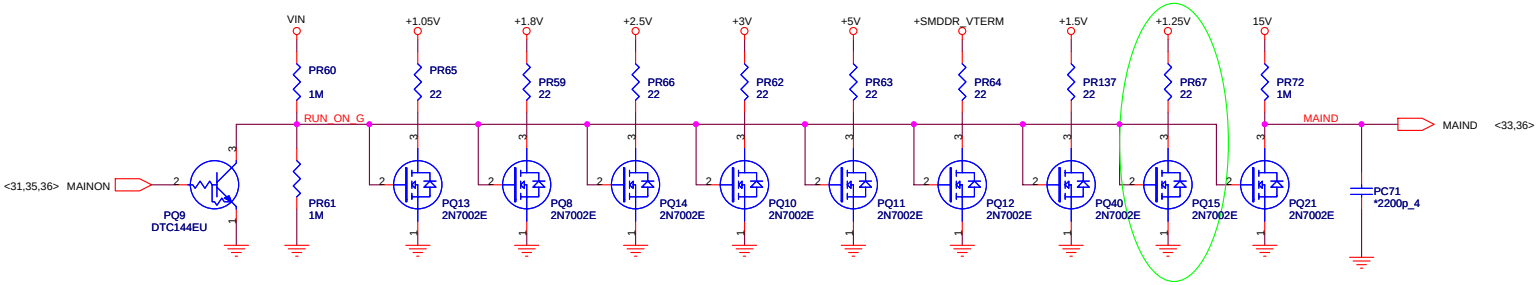








Add by power on 10/19



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	Discharge (1.5V/2.5V)	B
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Change list

Item	Fixed Issue	Reason for change	Schematic Rev.	PG#	Modify List
1	R5C833 SD CARD FAIL	SD CARD NO FUNCTION	B	28	SD card can not be detected , U32(ES2) sample will fix this issue.
2	R5C833 MMC CARD FAIL	MMC CARD NO FUNCTION	B	28	MMC card can not be detected , U32(ES2) sample will fix this issue.
3	TV CARD NO FUNCTION	Add +1.5V,Liteon without +1.5V; Avermedia need +1.5V	B	22	CN34.6 & .28 & .48 connect +1.5V
4	CAN'T BRING UP	power sequence fail	B	14	The CLPWROK pin of ICH8 connect with HWPG signal
5	VOLUME CONTROL ISSUE	VR switch have On/Off noise	B	31	add 2 capacity 0.1uF(C634,C636) in DIGVOL_UP / DIGVOL_DN pins
6	T/P NO FUNCTION	the pin definiton is wrong	B	22	change CN7 pin definition.
7	MMB NO FUNCTION	the pin definiton is wrong	B	22	change CN8 pin definition.
8	NONE	Modem have different interface which is +3V and +1.5V	B	15	reserve +3V and +3V_S5
9	NONE	INTEL request to add for AMT function	B	14	GPIO10: Reserve PU, 10K => It is GPO and OD GPIO14: Reserve PD, 10K => It is GPI as AC present and active high
10	ICH8 ELECTRIC LEAKAGE ISSUE	INTEL request to add for AMT function , ICH8 have electric leadage from EC	B	14	The signal of KBSMI#_ICH add diode , and it PU to +3V_S5 The signal of LID591#_ICH add diode , and it PU to +3V_S5
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					

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	CHANGE LIST	B

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