Eiger Block Diagram

Project code: 91.4Z501.001
PCB P/N : 48.4Z501.001
REVISION : 07246- -1

CLK GEN.
ICS 9LPRS365BKLFT 3

Mobile CPU
Penryn 4, 5

THERMAL EMC2102 23

HOST BUS 667/800/1067MHz@1.05V

DDR2 DIMM1
667/800 MHz 12

DDR2 DIMM2
667/800 MHz 13

667/800MHz

667/800MHz

Cantiga 6,7,8,9,10,11
- AGTL+ CPU I/F
- DDR Memory I/F
- INTEGRATED GRAHPICS
- LVDS, CRT I/F

CRT 17

LCD 15

HDMI 18

PCIex16

MXM CONN 30

X4 DMI 400MHz

C-Link0

ICH9M 19,20,21,22
- 6 PCIe ports
- PCI/PCI BRIDGE
- ACPI 2.0
- 4 SATA
- 12 USB 2.0/1.1 ports
- ETHERNET (10/100/1000MbE)
- High Definition Audio
- LPC I/F
- Serial Peripheral I/F
- Matrix Storage Technology(DO)
- Active Managemnet Technology(DO)

INT.MIC 35

Line In 35

Codec ALC888S VC 33

AZALIA

MIC In 35

OP AMP G1431Q 34

35 INT.SPKR

OP AMP G1412 34

35 Line Out (SPDIF)

RJ11

MODEM MDC Card 25

SPI

BIOS/DASH 2Mb 37

SATA

HDD SATA 24

ODD SATA 24

SATA

Blue Tooth (USB) 25

eSATA 24

USB

Camera (USB) 15

USB 4 Port 26

PCIex1 CardReader JMicro JMB385 27

MS/MS Pro/xD /MMC/SD 5 in 1 27

PCIex1 LAN Giga LAN 88E8071 28

TXFM 29

RJ45 29

PCIex1 New card 31

PWR SW G577BR91U 31

PCIex1 Mini Card Kedron a/b/g/n 32

PCIex1 Mini Card Kedron a/b/g/n 32

LPC BUS

KBC ENE3310 36

BIOS Winbond W25X80 8M Bits 37

Launch Buttom 14

CIR 36

Touch Pad 36

Finger Printer

INT. KB 36

LPC DEBUG CONN 37

Port Replicator 38

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC TPS51125 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

RT9026 44	
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3

RT9018A 44	
1D8V_S3	1D5V_S0

G9131 44	
3D3V_S0	2D5V_S0

GFXCORE DC/DC ISL6263 46	
INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7~1.25V

CPU DC/DC ISL6266A 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER BQ24745 47	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

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Title: BLOCK DIAGRAM

Size: Custom | Document Number: Eiger | Rev: -1

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

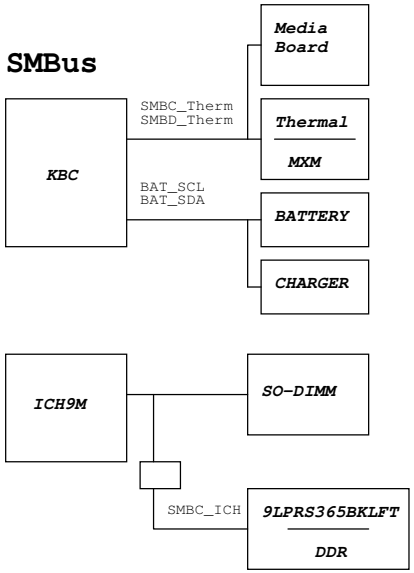
PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN/TV
LANE4	JMB385 Card Reader
LANE5	NewCard
LANE6	*NC*

USB Table

USB	
Pair	*Device*
0	*USB1*
1	*USB4*
2	*USB2*
3	*USB5(DOCK)*
4	*USB3*
5	*Bluetooth*
6	*FP*
7	*MINIC1*
8	*WEBCAM*
9	*NEW1*
10	*MINIC2*
11	*NC*

SMBus



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Title: **Reference**

Size: A3 | Document Number: **Eiger** | Rev: **-1**

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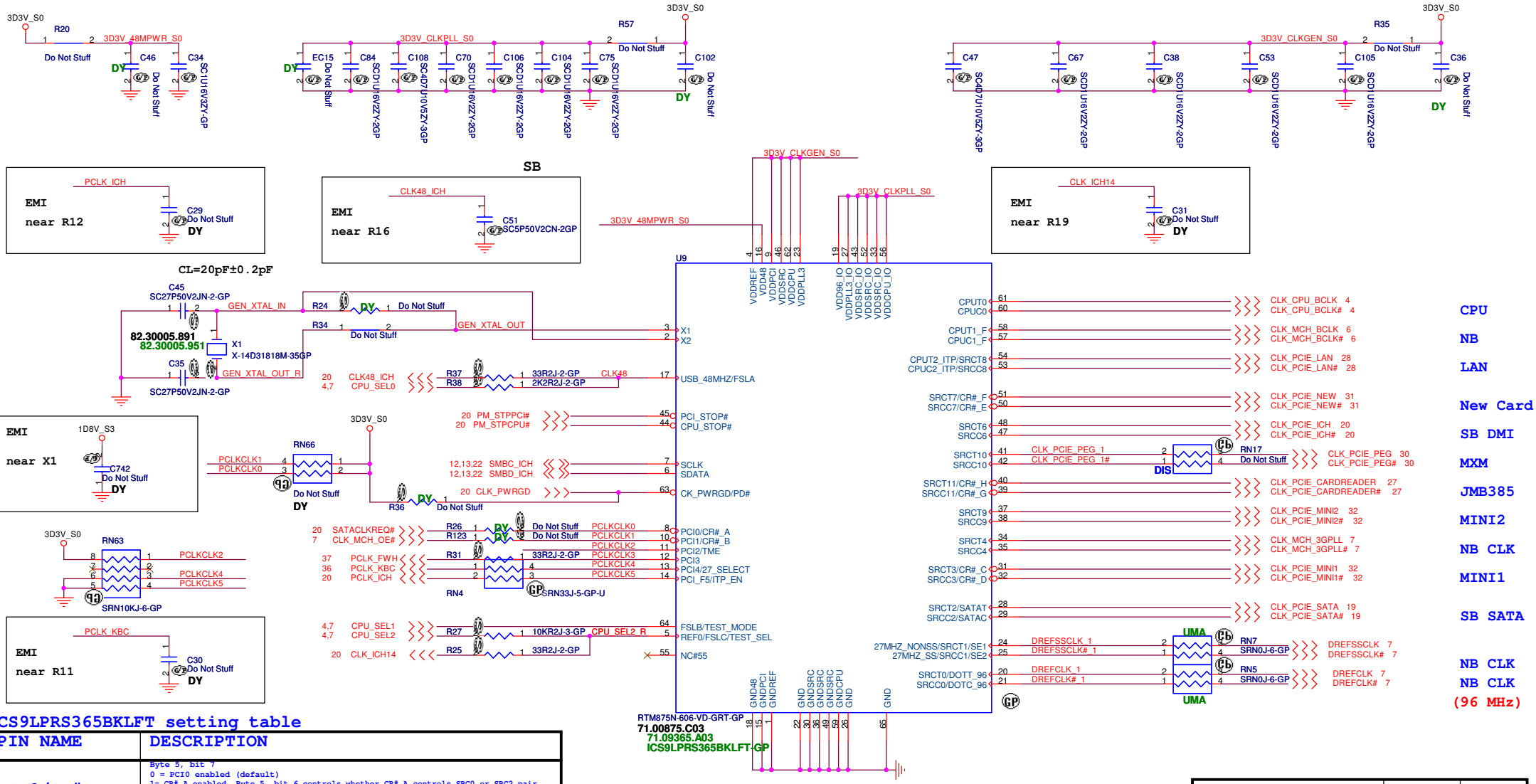

ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

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Title: Clock Generator

Size | Document Number: Eiger | Rev: -1

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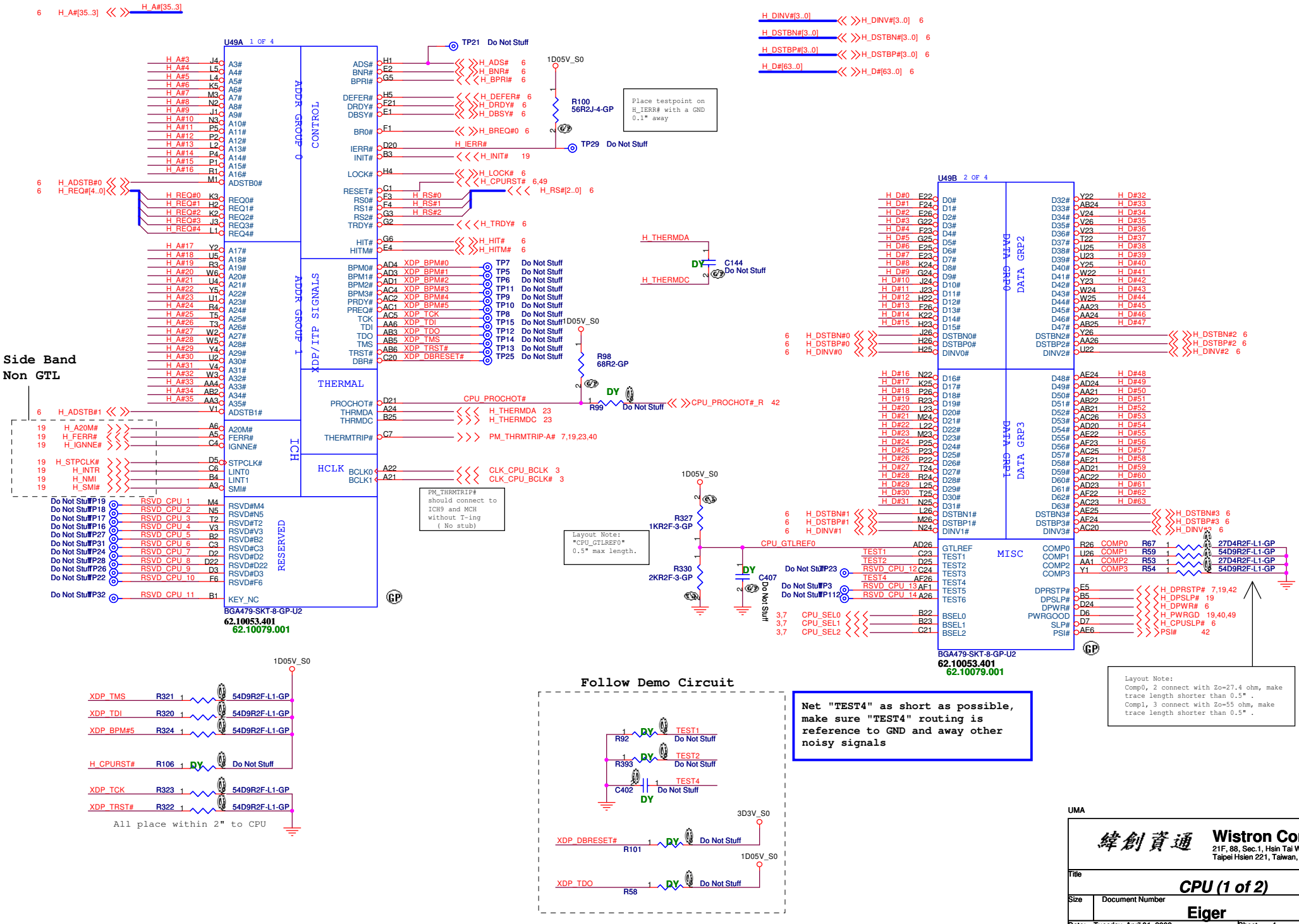
U49A 1 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
RESERVED
MCH
BGA479-SKT-8-GP-U2
62.10053.401
62.10079.001
U49B 2 OF 4
DATA GRP2
DATA GRP0
DATA GRP3
DATA GRP1
MISC
BGA479-SKT-8-GP-U2
62.10053.401
62.10079.001
Side Band
Non GTL
Follow Demo Circuit
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
Layout Note: "CPU_GTLREF0" 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
All place within 2" to CPU
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Title
CPU (1 of 2)
Size
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-1
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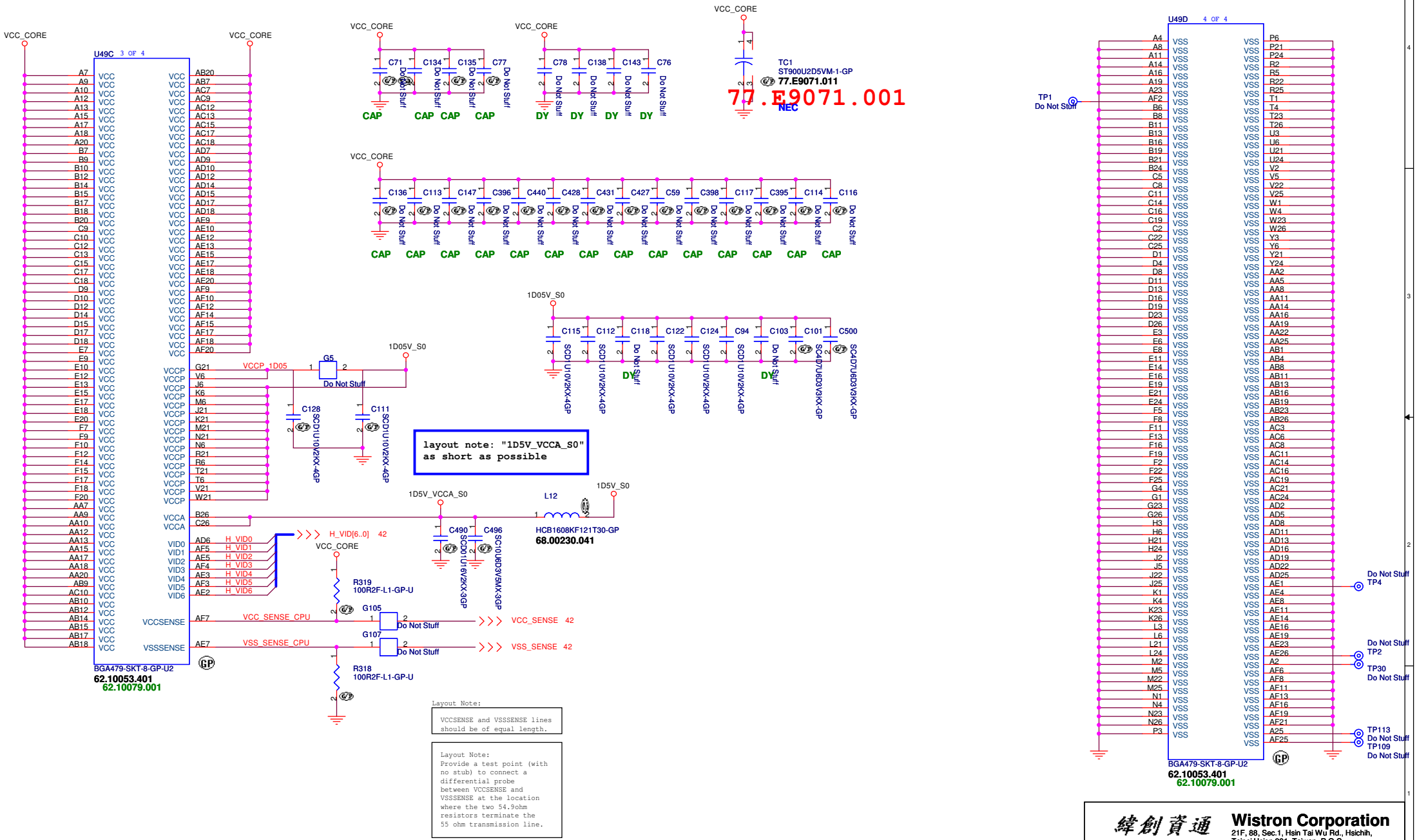

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Title	CPU (2 of 2)	
Size	Document Number: Eiger	Rev: -1
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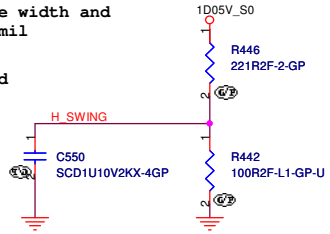
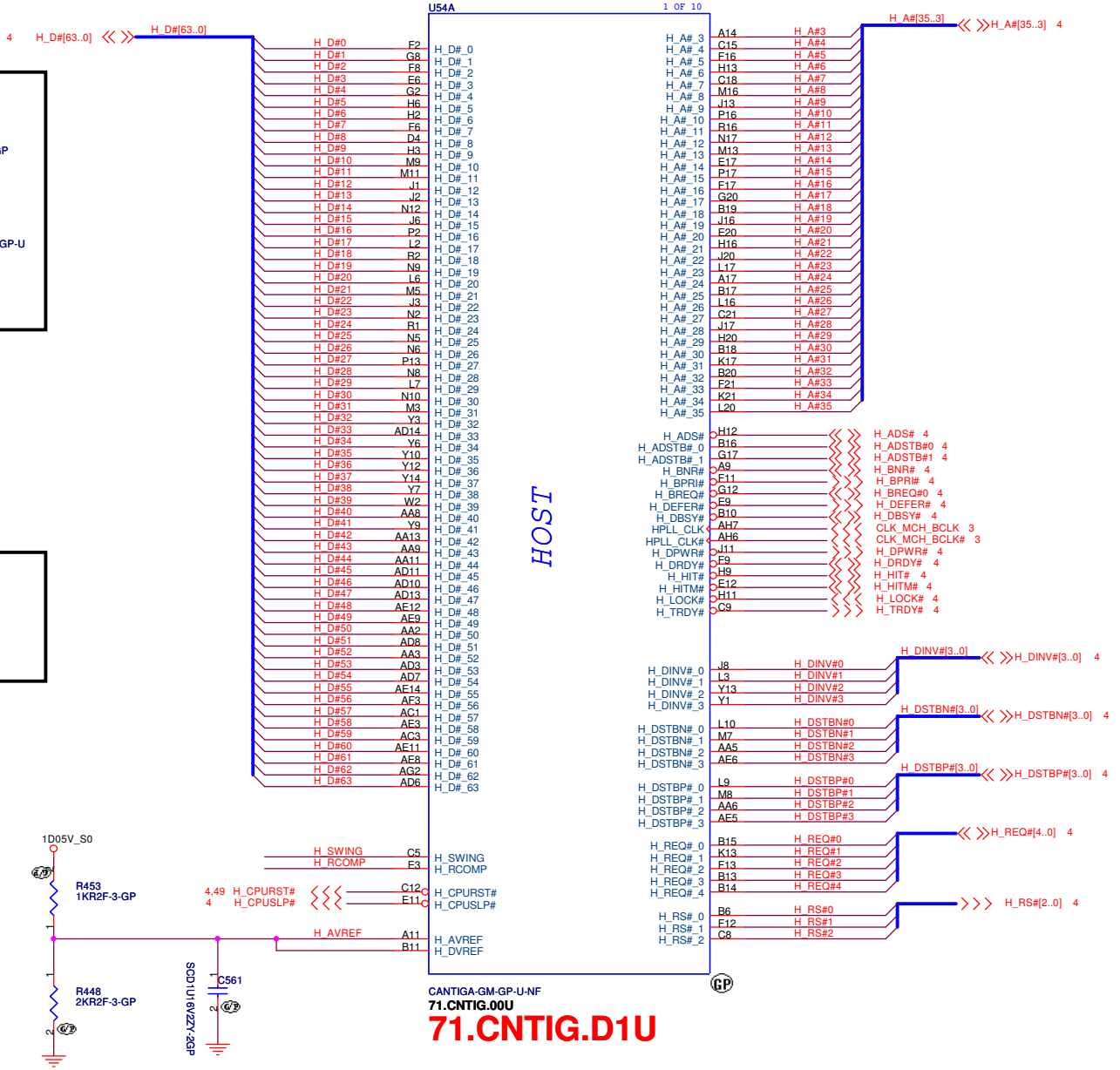
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

Place them near to the chip (< 0.5")



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Title: Cantiga (1 of 6)

Size | Document Number: Eiger | Rev: -1

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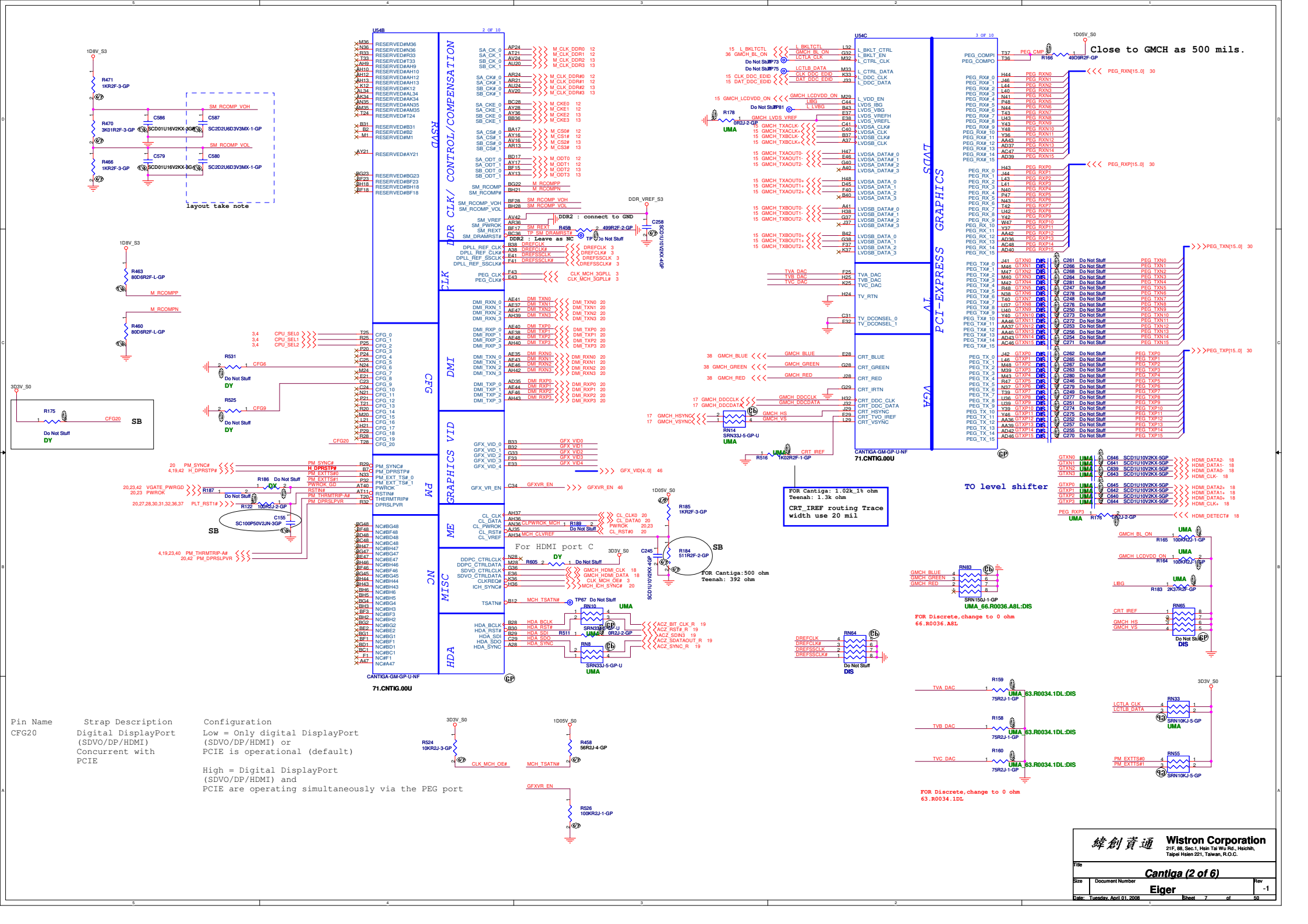
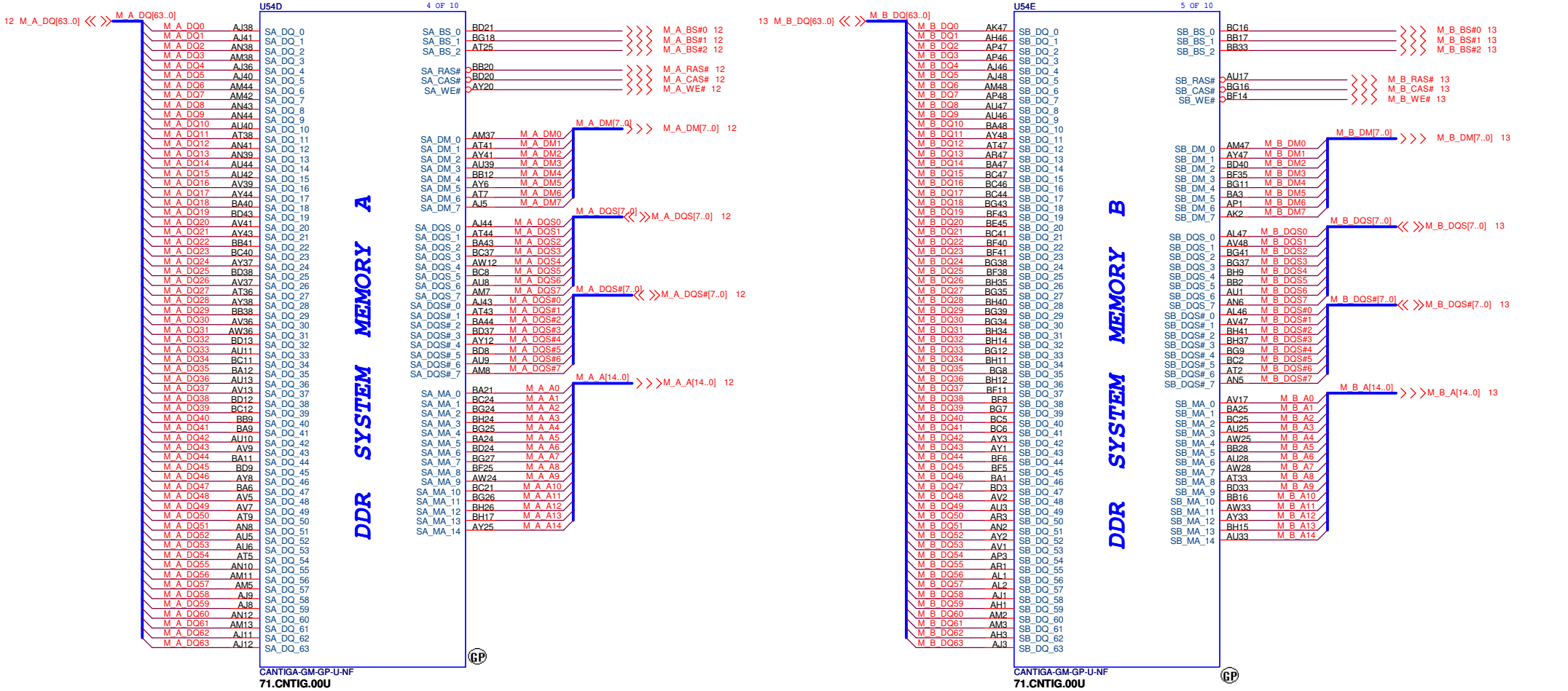


Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIE	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default)
		High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port



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Title: ***Cantiga (3 of 6)***

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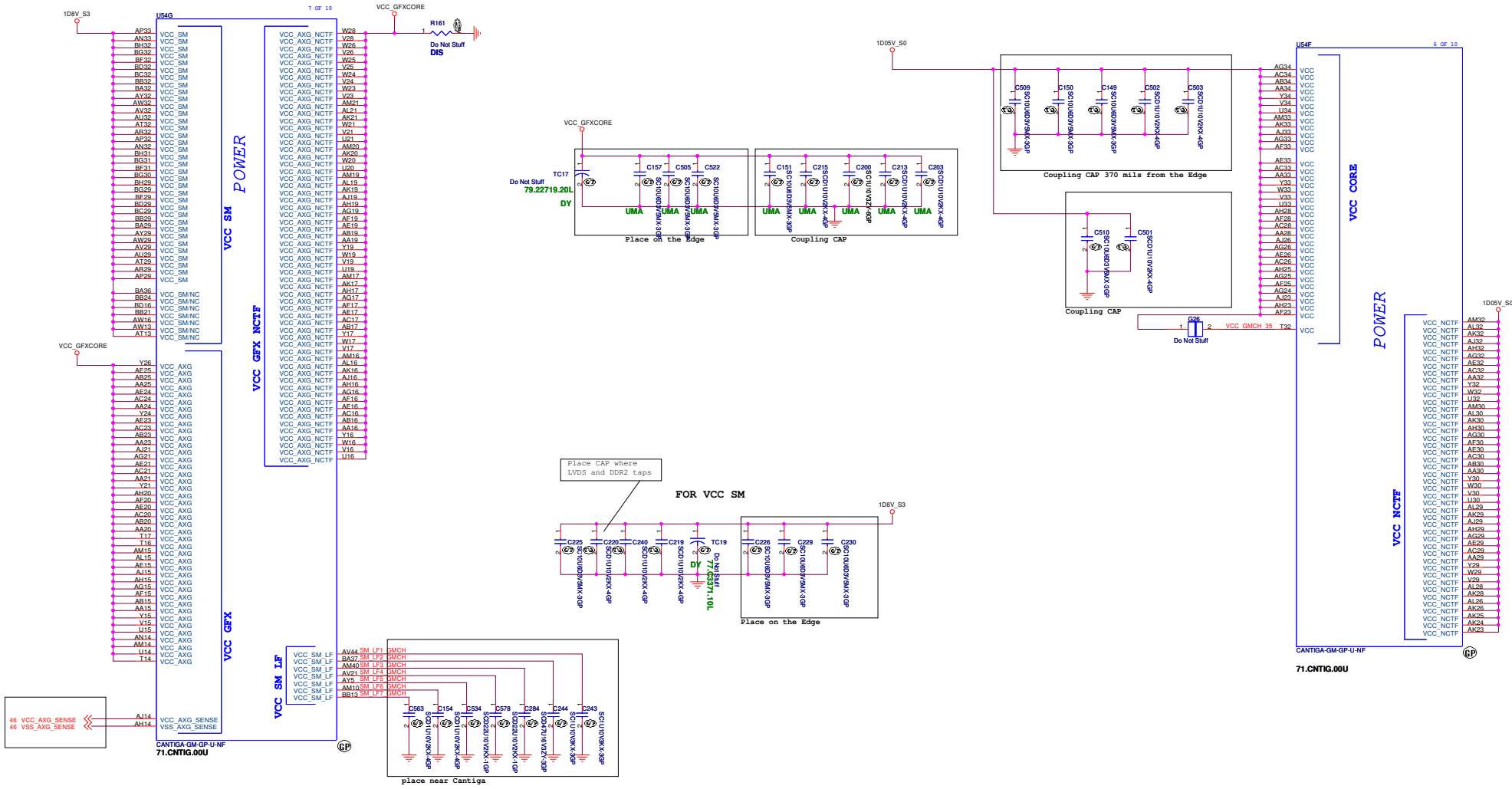

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Title	Cantiga (4 of 6)		
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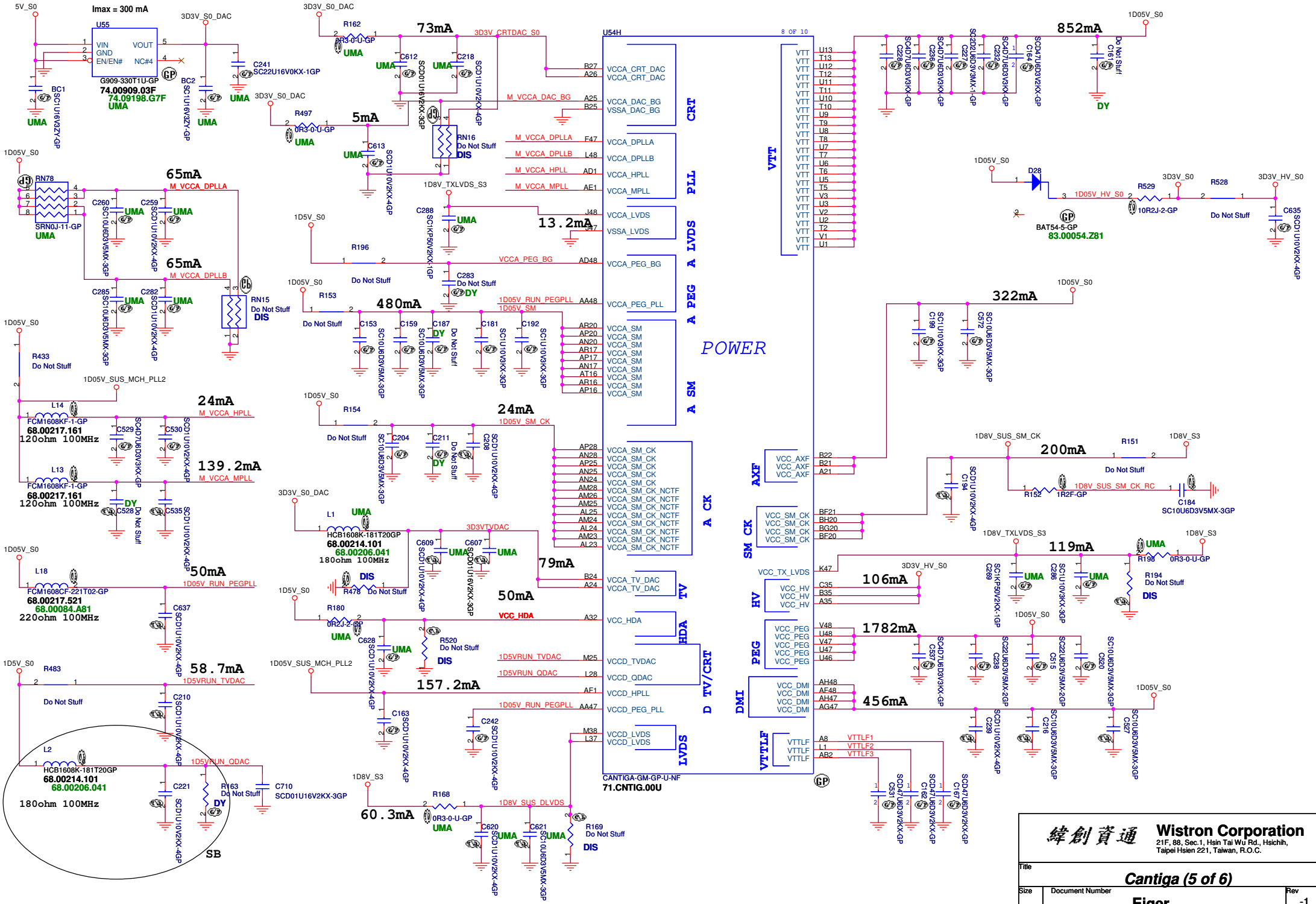
POWER
U54H
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
8 OF 10
Imax = 300 mA
U55
G909-330T1U-GP
74.00909.03F
74.09198.G7F
UMA
73mA
5mA
65mA
M_VCCA_DPLLA
65mA
M_VCCA_DPLLB
480mA
24mA
M_VCCA_HPLL
139.2mA
M_VCCA_MPLL
50mA
58.7mA
1D5VRUN_TVDAC
157.2mA
1D5VRUN_QDAC
60.3mA
13.2mA
24mA
1D05V_SM_CK
79mA
50mA
VCC_HDA
322mA
200mA
119mA
106mA
1782mA
456mA
852mA
DY
DIS
SB
Do Not Stuff
FCM1608KF-1-GP
68.00217.161
120ohm 100MHz
FCM1608CF-221T02-GP
68.00217.521
68.00084.A81
220ohm 100MHz
HCB1608K-181T20GP
68.00214.101
68.00206.041
180ohm 100MHz
BAT54-5-GP
83.00054.Z81
SRN0J-11-GP
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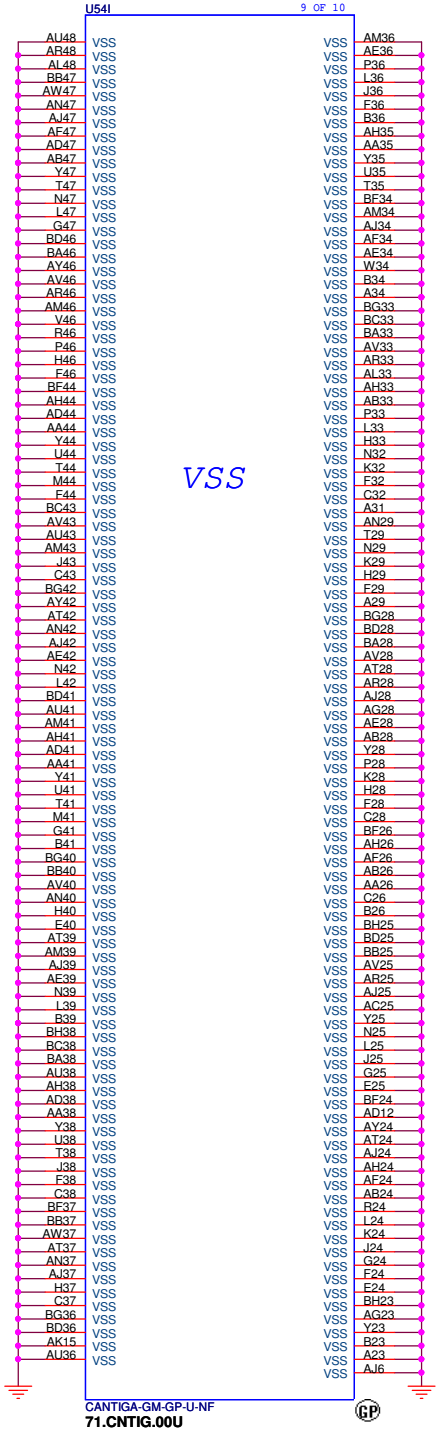

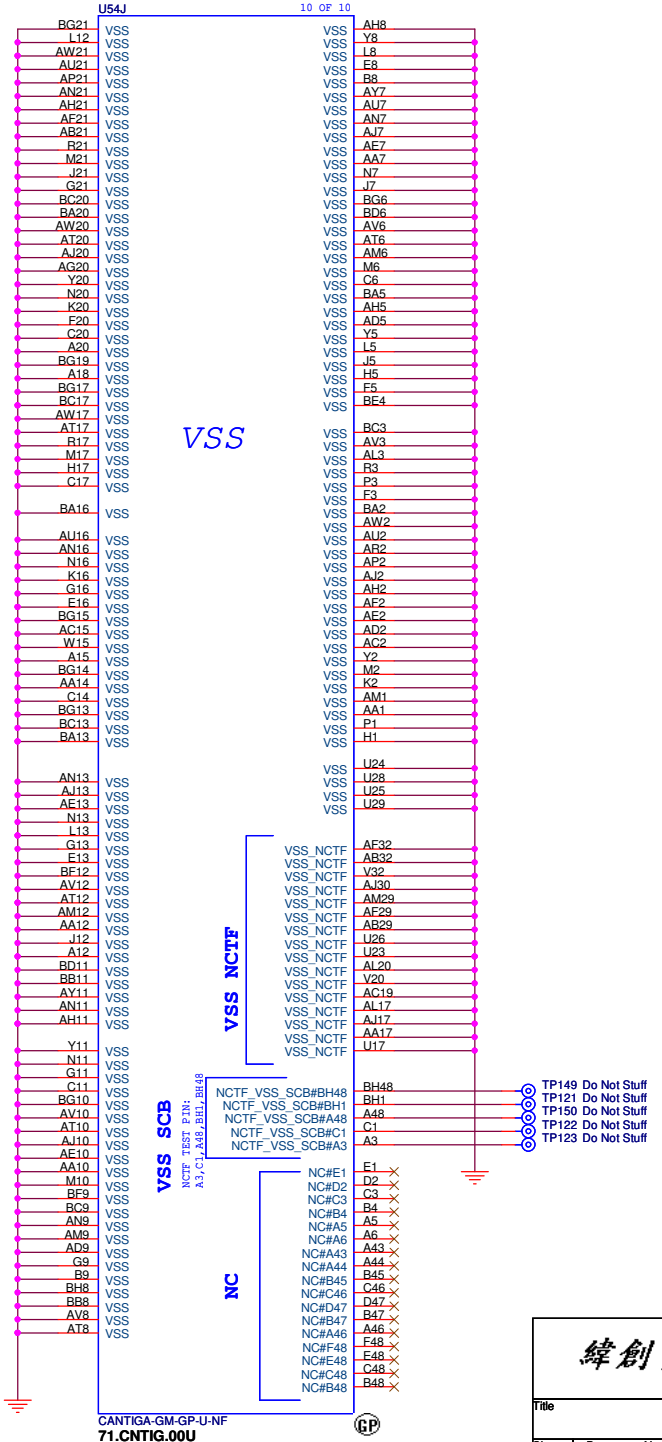

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Size	Document Number: **Eiger**	Rev: -1
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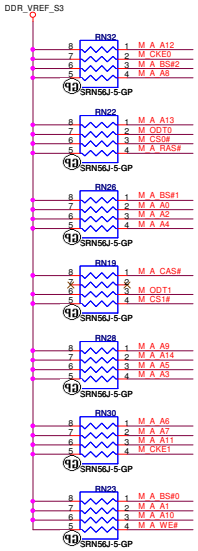
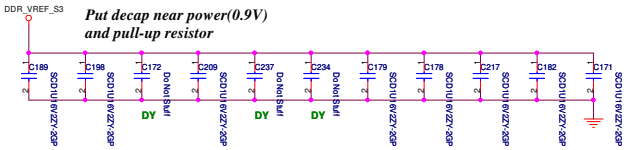
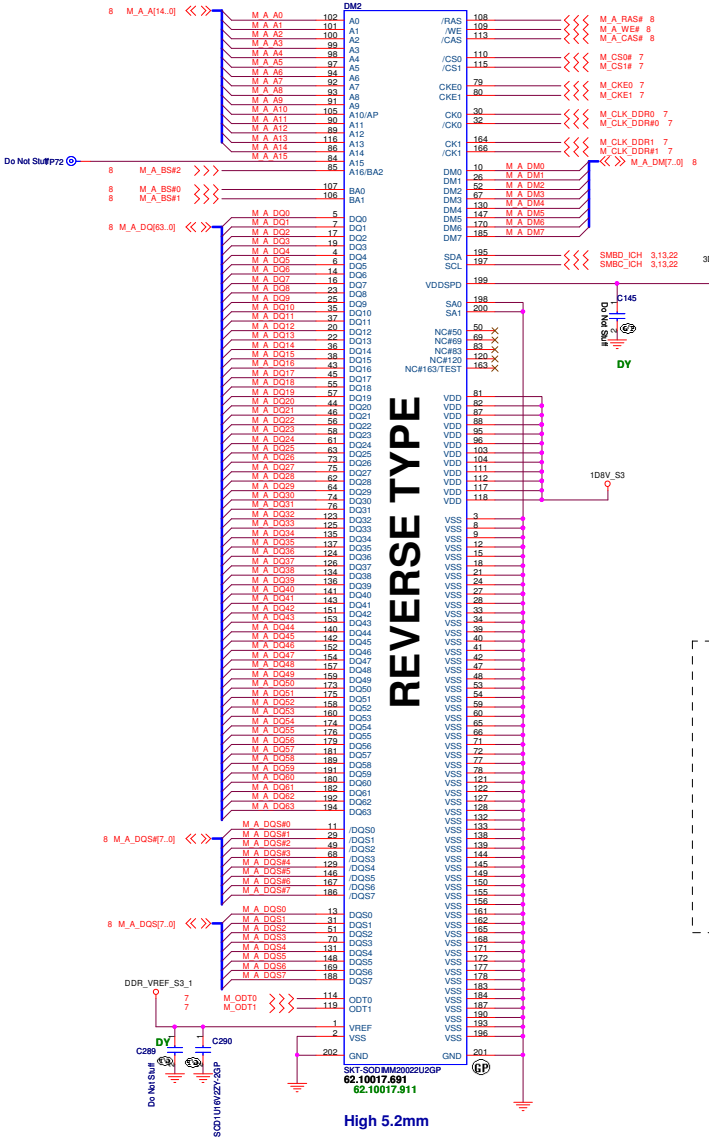
PARALLEL TERMINATION

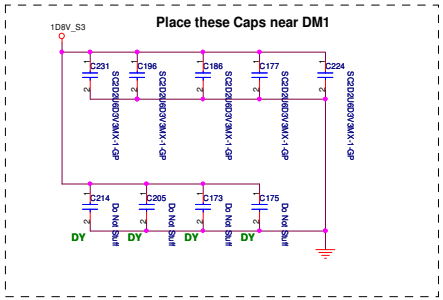
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor







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	Elger	-1

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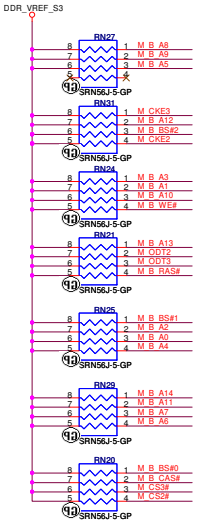
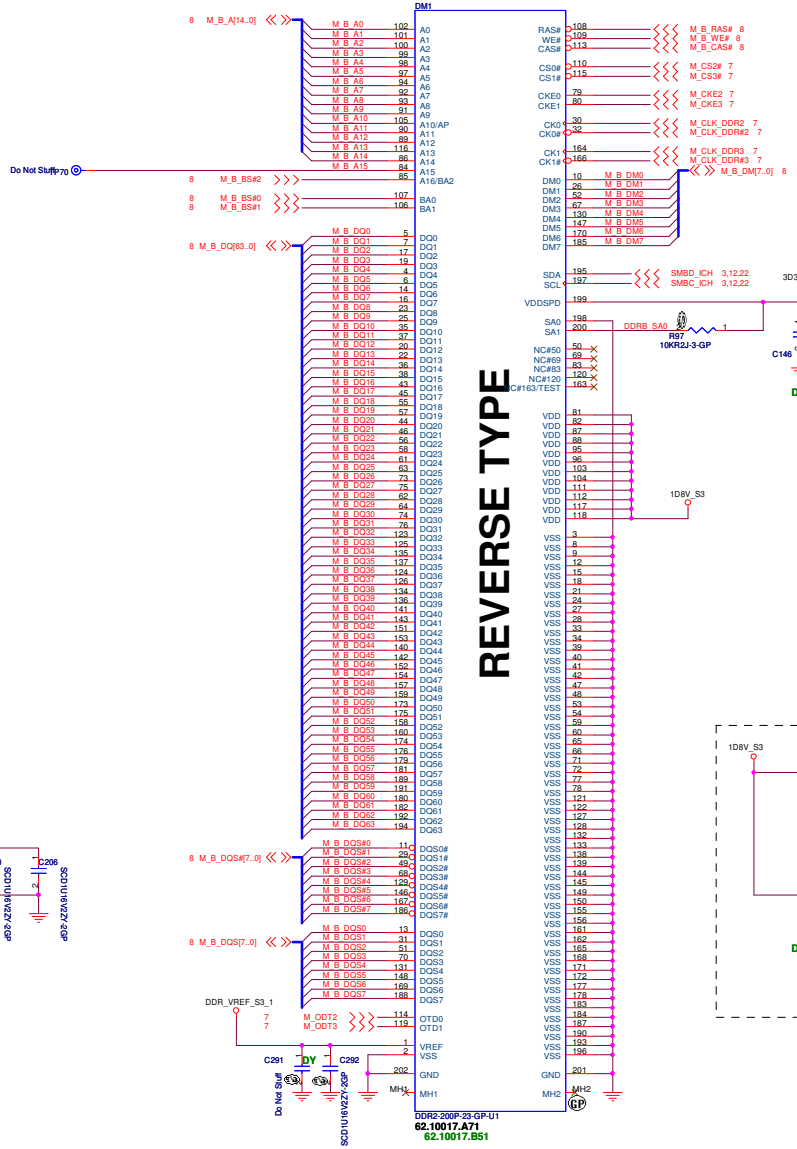
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

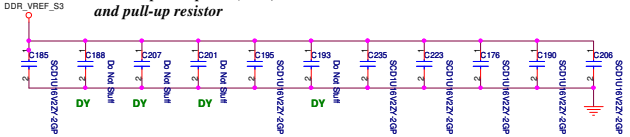


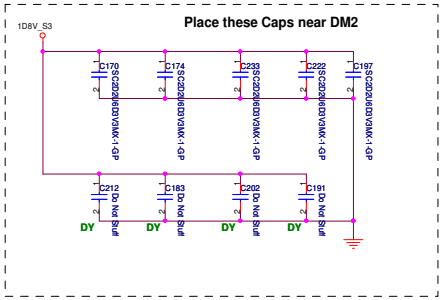
REVERSE TYPE



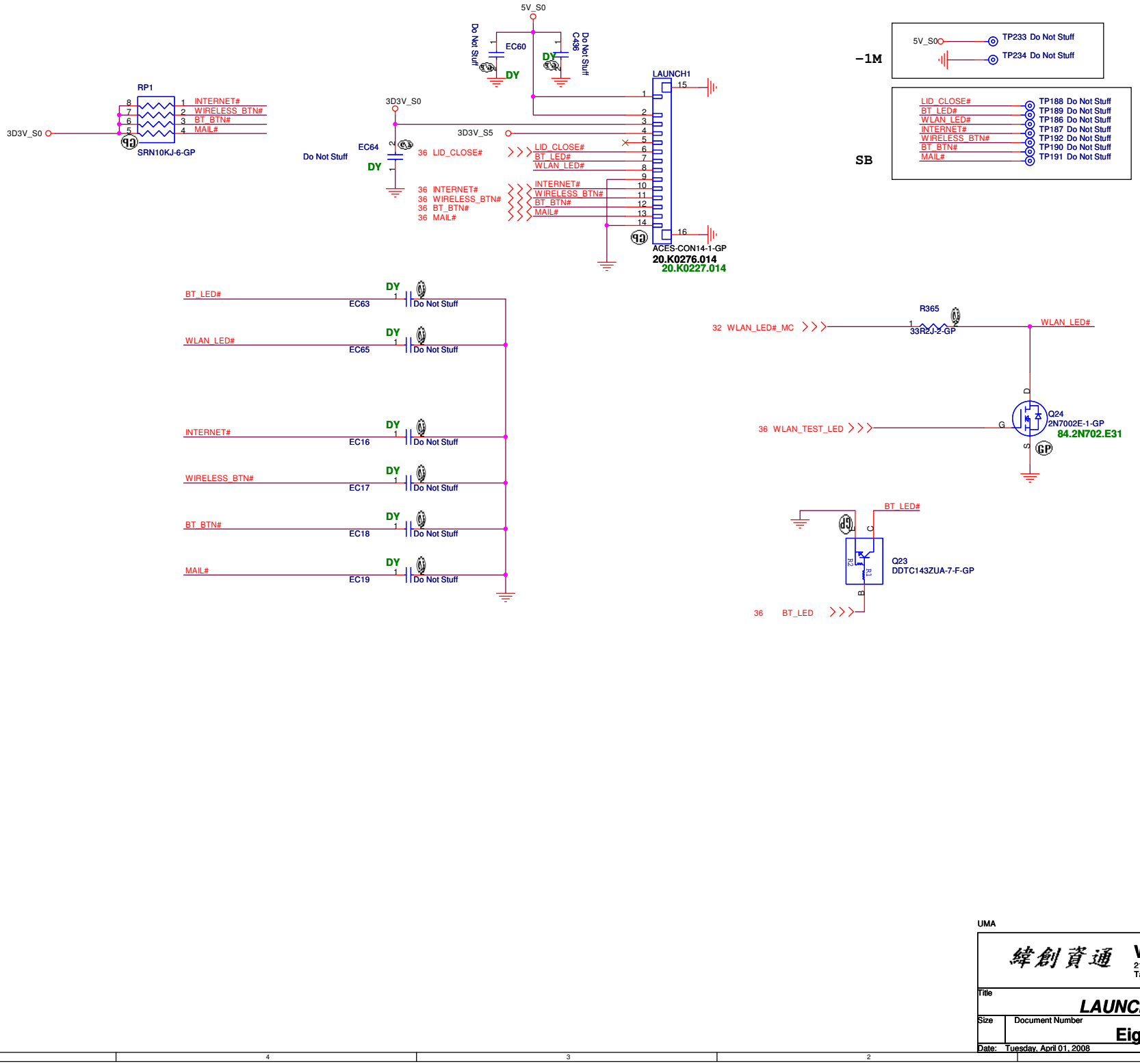
Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor





緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR2 Socket 1 (DM2)		
Size	Document Number: Eiger	Rev: -1
Date: Tuesday, April 01, 2008	Sheet 13 of 50	

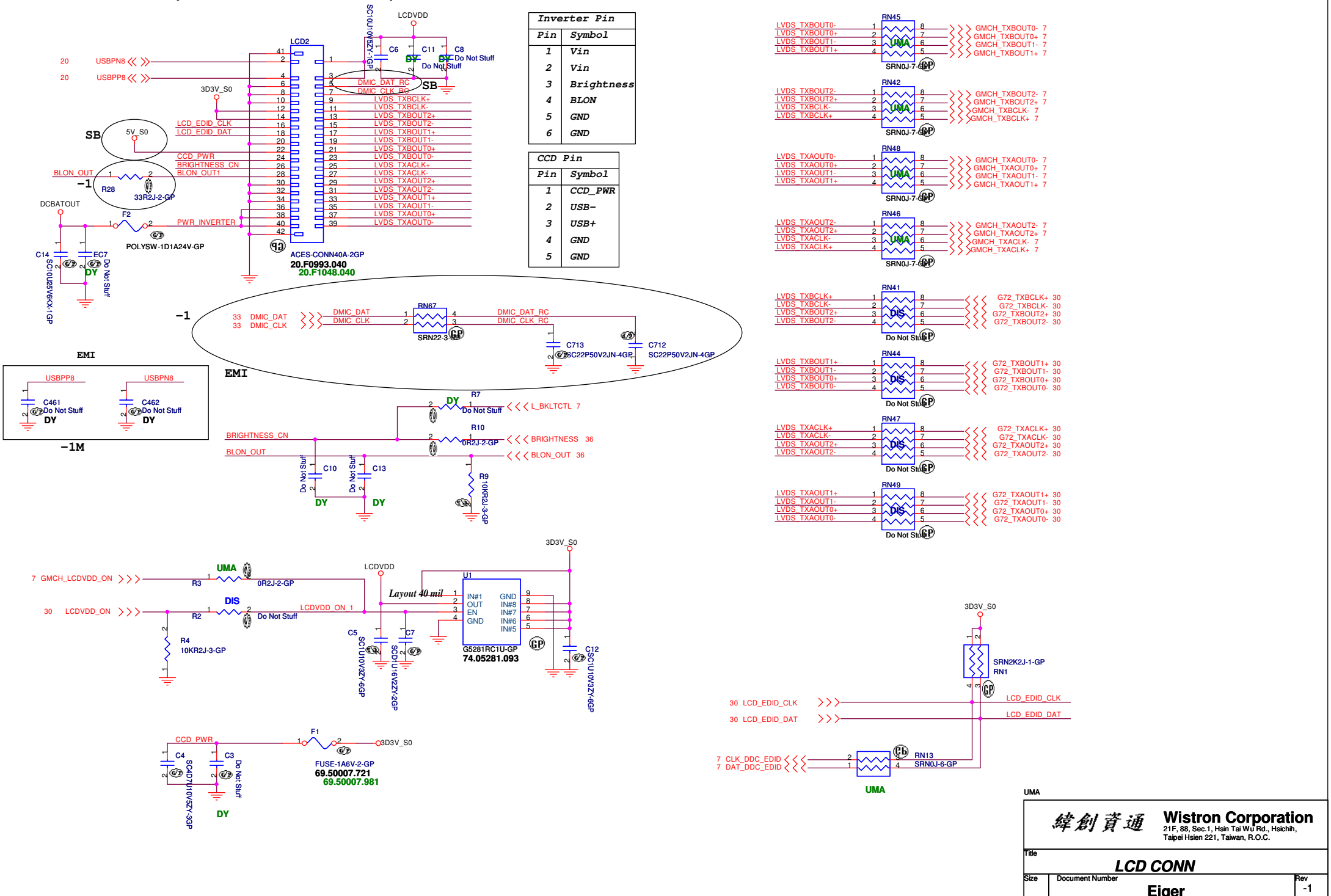


UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**LAUNCH**	
Size	Document Number: **Eiger**	Rev: -1
Date: Tuesday, April 01, 2008	Sheet 14 of 50	

LCD/INVERTER/CCD CONN



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

UMA

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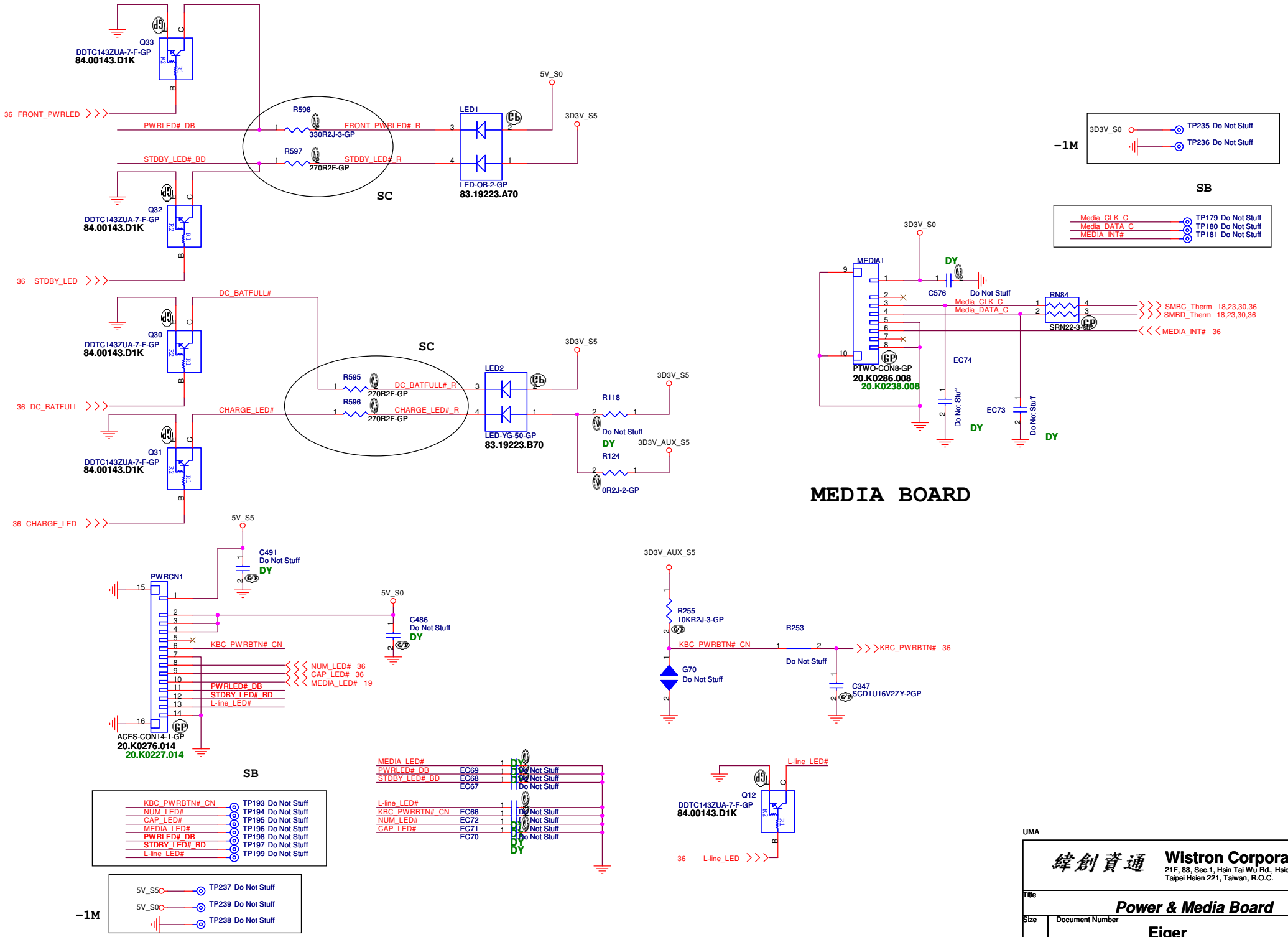
Title	**LCD CONN**	
Size	Document Number **Eiger**	Rev -1
Date: Tuesday, April 01, 2008	Sheet 15 of 50	


Q33
DDTC143ZUA-7-F-GP
84.00143.D1K
36 FRONT_PWRLED
PWRLED# DB
STDBY_LED# BD
R598
330R2J-3-GP
FRONT_PWRLED# R
R597
270R2F-GP
STDBY_LED# R
LED1
LED-OB-2-GP
83.19223.A70
5V_S0
3D3V_S5
SC
Q32
DDTC143ZUA-7-F-GP
84.00143.D1K
36 STDBY_LED
DC_BATFULL#
Q30
DDTC143ZUA-7-F-GP
84.00143.D1K
36 DC_BATFULL
CHARGE_LED#
R595
270R2F-GP
DC_BATFULL# R
R596
270R2F-GP
CHARGE_LED# R
LED2
LED-YG-50-GP
83.19223.B70
R118
Do Not Stuff
DY
R124
0R2J-2-GP
3D3V_AUX_S5
Q31
DDTC143ZUA-7-F-GP
84.00143.D1K
36 CHARGE_LED
-1M
3D3V_S0
TP235 Do Not Stuff
TP236 Do Not Stuff
SB
Media_CLK_C
Media_DATA_C
MEDIA_INT#
TP179 Do Not Stuff
TP180 Do Not Stuff
TP181 Do Not Stuff
MEDIA1
PTWO-CON8-GP
20.K0286.008
20.K0238.008
C576
Do Not Stuff
RN84
SRN22-3-GP
SMBC_Therm 18,23,30,36
SMBD_Therm 18,23,30,36
MEDIA_INT# 36
EC74
EC73
MEDIA BOARD
5V_S5
C491
Do Not Stuff
DY
PWRCN1
ACES-CON14-1-GP
20.K0276.014
20.K0227.014
5V_S0
C486
Do Not Stuff
DY
KBC_PWRBTN# CN
NUM_LED# 36
CAP_LED# 36
MEDIA_LED# 19
PWRLED# DB
STDBY_LED# BD
L-line_LED#
3D3V_AUX_S5
R255
10KR2J-3-GP
KBC_PWRBTN# CN
G70
Do Not Stuff
R253
Do Not Stuff
KBC_PWRBTN# 36
C347
SCD1U16V2ZY-2GP
SB
KBC_PWRBTN# CN
NUM_LED#
CAP_LED#
MEDIA_LED#
PWRLED# DB
STDBY_LED# BD
L-line_LED#
TP193 Do Not Stuff
TP194 Do Not Stuff
TP195 Do Not Stuff
TP196 Do Not Stuff
TP198 Do Not Stuff
TP197 Do Not Stuff
TP199 Do Not Stuff
MEDIA_LED#
PWRLED# DB
STDBY_LED# BD
L-line_LED#
KBC_PWRBTN# CN
NUM_LED#
CAP_LED#
EC69
EC68
EC67
EC66
EC72
EC71
EC70
Do Not Stuff
DY
Q12
DDTC143ZUA-7-F-GP
84.00143.D1K
L-line_LED#
36 L-line_LED
-1M
5V_S5
5V_S0
TP237 Do Not Stuff
TP239 Do Not Stuff
TP238 Do Not Stuff
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power & Media Board
Size
Document Number
Eiger
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Sheet 16 of 50

Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

38 CRT_R_SYS
38 CRT_G_SYS
38 CRT_B_SYS

RN85 SRN150J-1-GP

C484 Do Not Stuff DY
C475 Do Not Stuff DY
C456 Do Not Stuff DY

L11 FCB1608CF-GP 68.00230.021 68.00119.081
L10 FCB1608CF-GP 68.00230.021 68.00119.081
L9 FCB1608CF-GP 68.00230.021 68.00119.081

CRT_R
CRT_G
CRT_B

C485 SC15P50V2JN-2-GP -1
C476 SC6D8P50V2DN-GP
C457 SC6D8P50V2DN-GP

5V_S0

D21 CRT_R Do Not Stuff DY Do Not Stuff 83.00099.K11
D19 CRT_G Do Not Stuff DY Do Not Stuff 83.00099.K11
D17 CRT_B Do Not Stuff DY Do Not Stuff 83.00099.K11

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR

5V_CRT_S0

CRT1
VIDEO-15-78-GP-U1
20.20717.015
20.20722.015

C451 SCD01U16V2KX-3GP

CRT_R
CRT_G
CRT_B
CRT_VSYNC1
CRT_HSYNC1
CLK_DDC1_5
DAT_DDC1_5

C445 SC18P50V2JN-1-GP
C471 SC18P50V2JN-1-GP
C444 SC100P50V2JN-3GP
C419 SC100P50V2JN-3GP

SC EMI
C166 Do Not Stuff DY

36,38 CRT_DEC#

R354 470R2J-2-GP
CRT_IN#_R
C439 Do Not Stuff DY

D15 Do Not Stuff 83.00099.K11

5V_S0

6 1 7 2 8 3 3 9 4 10 5

Hsync & Vsync level shift

5V_S0

SB
38 DOCK_IN_CRT#

30 CRT_HSYNC
30 CRT_VSYNC
7 GMCH_HSYNC
7 GMCH_VSYNC

RN77 Do Not Stuff
RN61 SRN0J-6-GP

HSYNC_4
VSYNC_4

C412 SCD1U16V2ZY-2GP

U46A TSAHCT125PW-GP 73.74125.L12
U46B TSAHCT125PW-GP 73.74125.L12

CRT_HSYNC1
CRT_VSYNC1

C432 Do Not Stuff DY
C423 Do Not Stuff DY

SB

R356 100KR2J-1-GP
DOCK_IN_CRT_2#
DOCK_IN_CRT#
Q20 2N7002E-1-GP 84.2N702.E31

For Dock CRT

HSYNC_4
VSYNC_4

U46C TSAHCT125PW-GP 73.74125.L12
U46D TSAHCT125PW-GP 73.74125.L12

HSYNC_5 38
VSYNC_5 38

DDC_CLK & DATA level shift

3D3V_S0
5V_CRT_S0
5V_S0

D14 CH551H-30PT-GP 83.R5003.H8H

F3 FUSE-1DTA6V-4GP-U 69.50007.691 69.50007.941
5V_CRT_DDC

RN43 SRN2K2J-1-GP
RN40 SRN2KJ-2-GP SB

U45 2N7002KDW-GP 84.00512.03F SD

7 GMCH_DDCDATA
7 GMCH_DDCCLK
30 CRT_DDCDATA
30 CRT_DDCCLK

RN9 SRN0J-6-GP
RN71 Do Not Stuff

DAT_DDC1_5_O
CLK_DDC1_5_O

CRT_IN#_R
DAT_DDC1_5 38
CLK_DDC1_5 38

UMA

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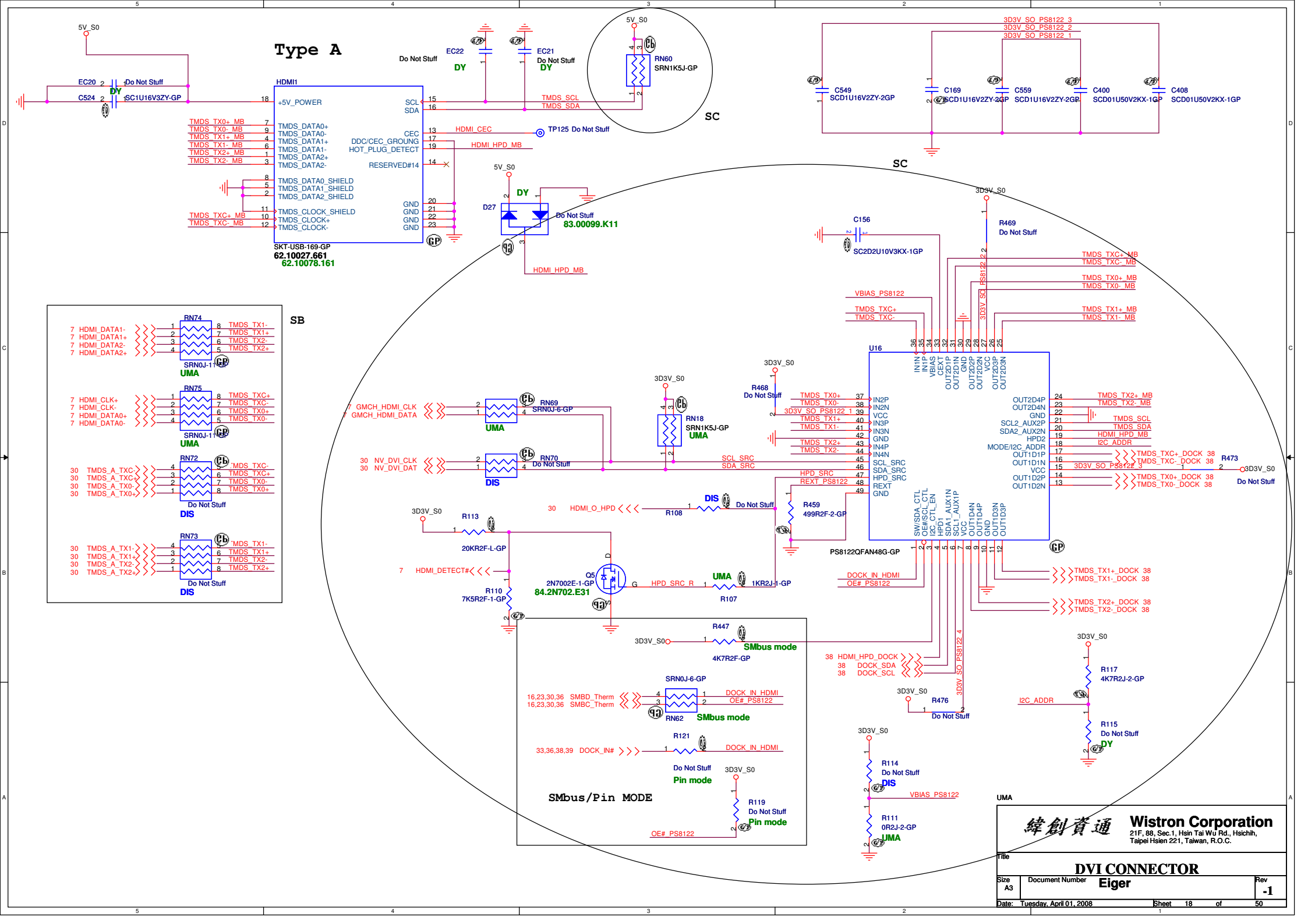
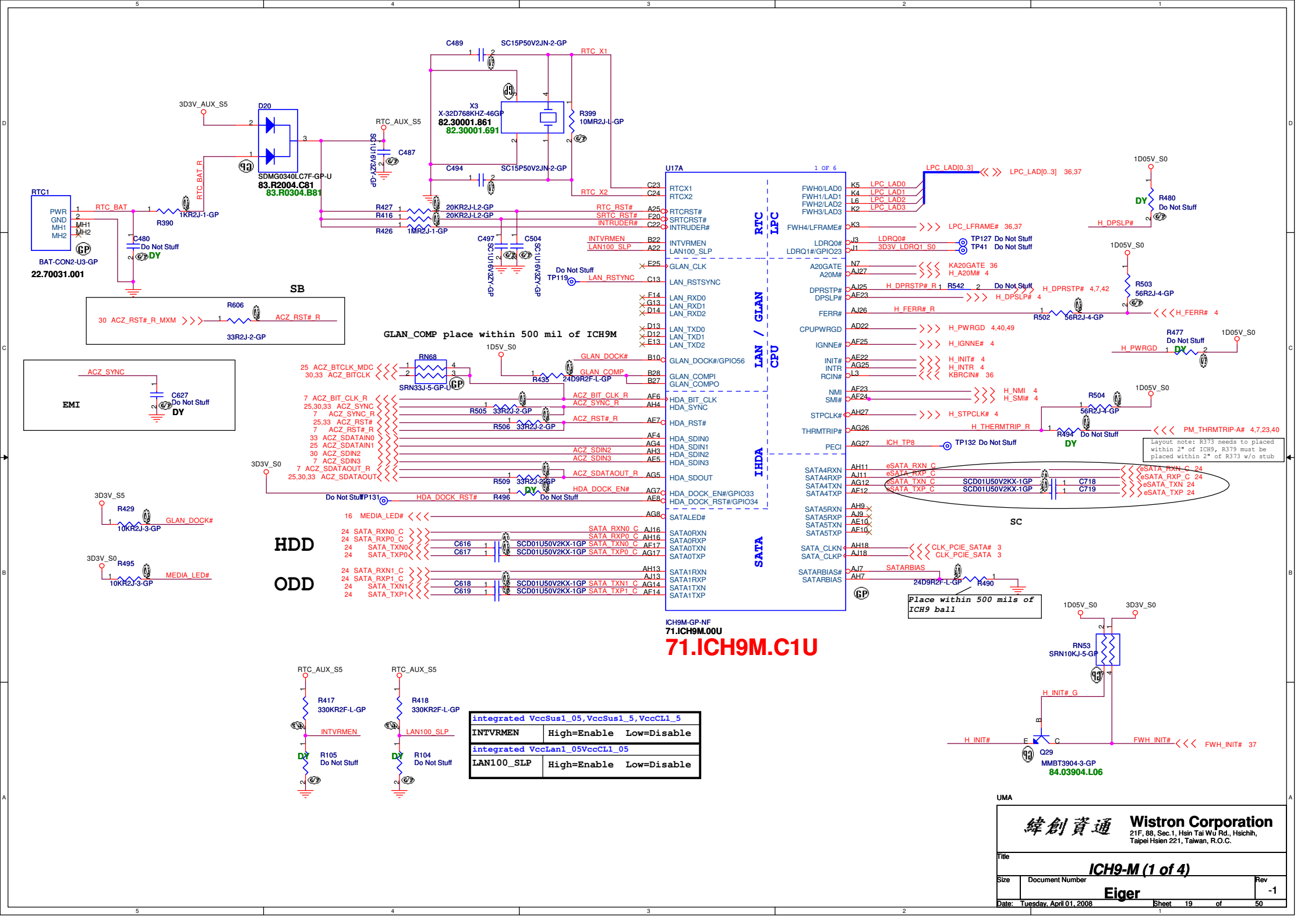
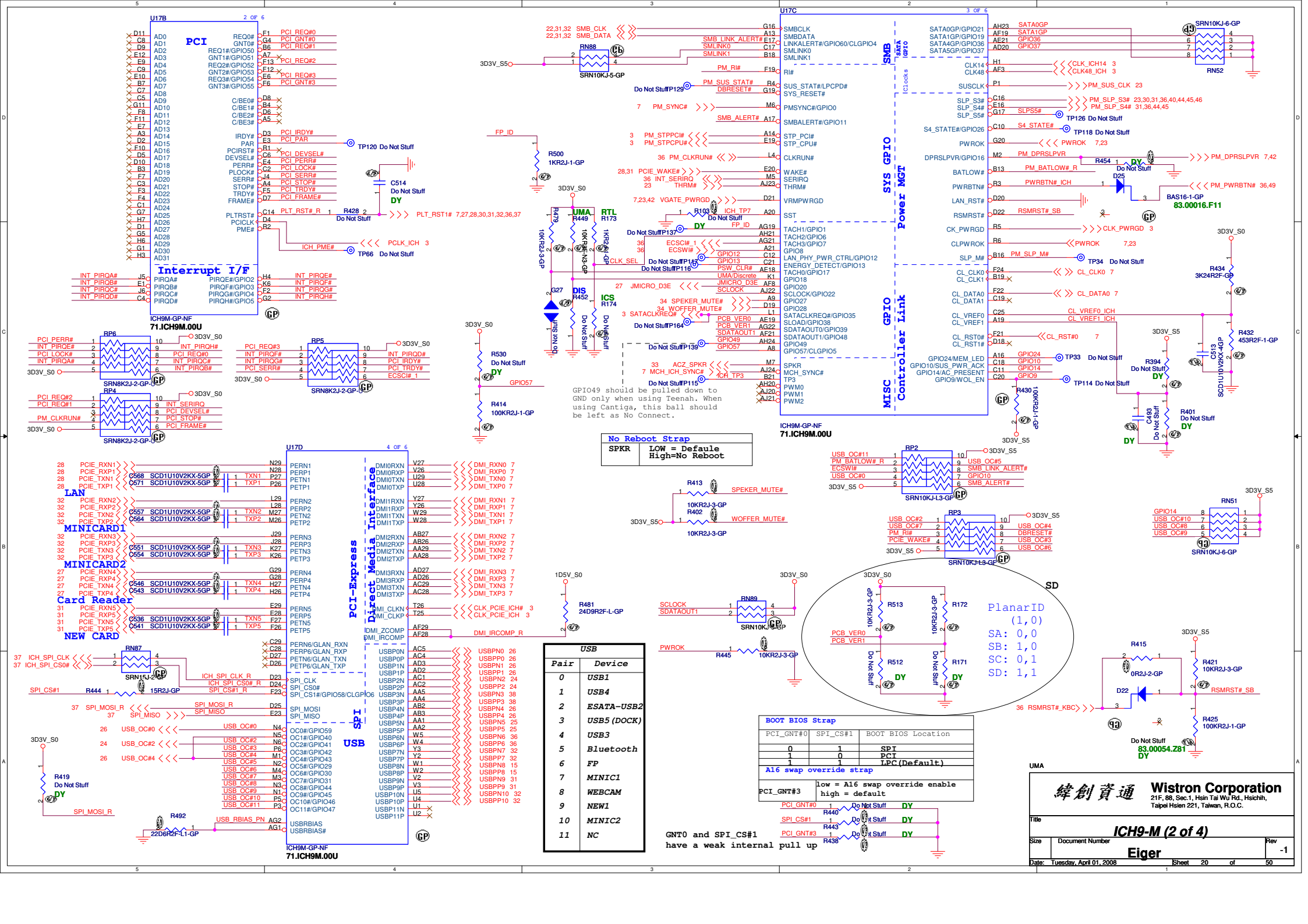
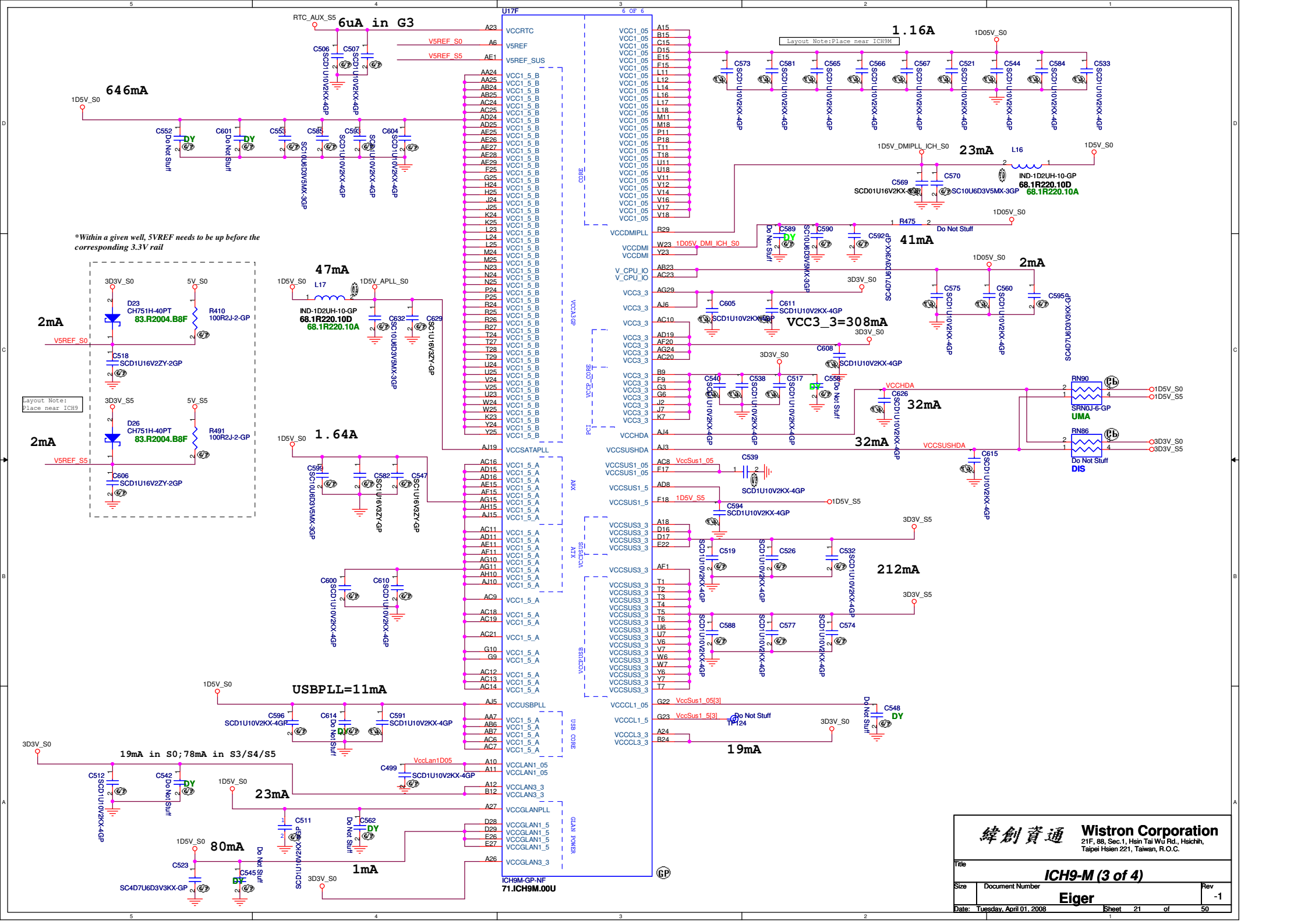
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

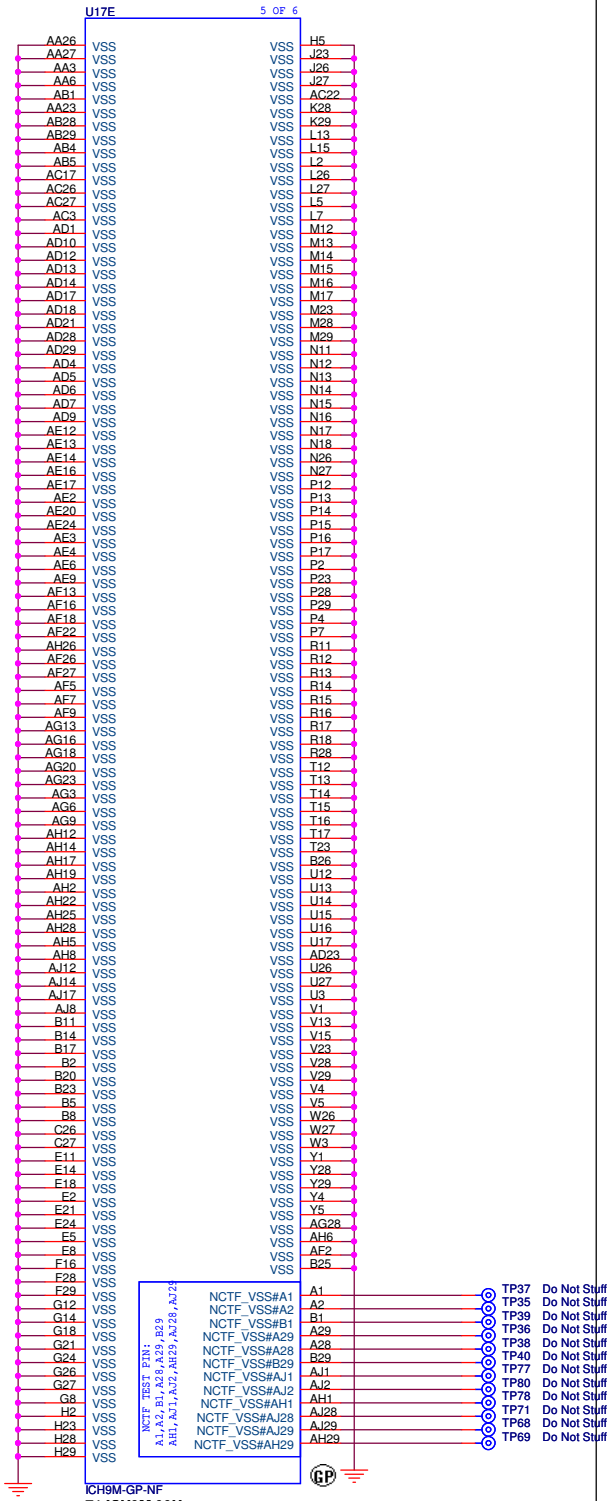
Title: ***CRT Connector***
Size: Document Number: Eiger Rev: -1
Date: Tuesday, April 01, 2008 Sheet 17 of 50

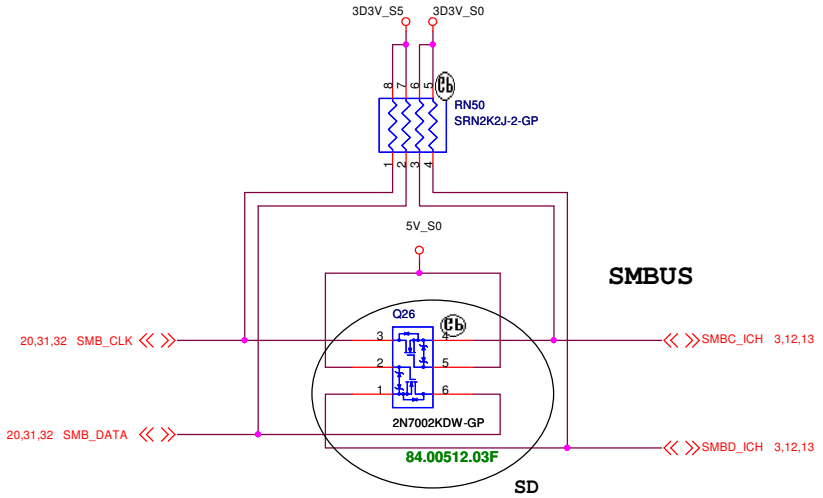

Type A
SC
SB
UMA
DIS
SMbus/Pin MODE
HDMI1
SKT-USB-169-GP
62.10027.661
62.10078.161
U16
PS8122QFAN48G-GP
Q5
2N7002E-1-GP
84.2N702.E31
D27
83.00099.K11
SMbus mode
Pin mode
Do Not Stuff
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DVI CONNECTOR
Eiger
Size A3
Rev -1
Date: Tuesday, April 01, 2008
Sheet 18 of 50


C489 SC15P50V2JN-2-GP
RTC_X1
X3
X-32D768KHZ-46GP
82.30001.861
82.30001.691
R399 10MR2J-L-GP
C494 SC15P50V2JN-2-GP
RTC_X2
3D3V_AUX_S5
D20
SDMG0340LC7F-GP-U
83.R2004.C81
83.R0304.B81
RTC_AUX_S5
SC1U16V2ZY-GP
C487
RTC_BAT_R
RTC1
PWR
GND
MH1
MH2
BAT-CON2-U3-GP
22.70031.001
RTC_BAT
R390 1KR2J-1-GP
C480 Do Not Stuff DY
R427 20KR2J-L2-GP
R416 20KR2J-L2-GP
R426 1MR2J-1-GP
RTC_RST#
SRTC_RST#
INTRUDER#
C497 SC1U16V2ZY-GP
C504 SC1U16V2ZY-GP
INTVRMEN
LAN100_SLP
Do Not Stuff
TP119
LAN_RSTSYNC
SB
R606
30 ACZ_RST#_R_MXM
ACZ_RST# R
33R2J-2-GP
GLAN_COMP place within 500 mil of ICH9M
EMI
ACZ_SYNC
C627 Do Not Stuff DY
RN68
SRN33J-5-GP-U
25 ACZ_BTCLK_MDC
30,33 ACZ_BITCLK
1D5V_S0
R435 24D9R2F-L-GP
GLAN_DOCK#
GLAN_COMP
GLAN_COMPI
GLAN_COMPO
7 ACZ_BIT_CLK_R
25,30,33 ACZ_SYNC
7 ACZ_SYNC_R
25,33 ACZ_RST#
7 ACZ_RST#_R
33 ACZ_SDATAIN0
25 ACZ_SDATAIN1
30 ACZ_SDIN2
7 ACZ_SDIN3
7 ACZ_SDATAOUT_R
25,30,33 ACZ_SDATAOUT
R505 33R2J-2-GP
R506 33R2J-2-GP
R509 33R2J-2-GP DY
Do Not Stuff TP131
HDA_DOCK_RST#
R496 Do Not Stuff
HDA_DOCK_EN#
3D3V_S0
3D3V_S5
R429 10KR2J-3-GP
GLAN_DOCK#
R495 10KR2J-3-GP
MEDIA_LED#
HDD
ODD
16 MEDIA_LED#
24 SATA_RXN0_C
24 SATA_RXP0_C
24 SATA_TXN0
24 SATA_TXP0
C616 C617 SCD01U50V2KX-1GP
24 SATA_RXN1_C
24 SATA_RXP1_C
24 SATA_TXN1
24 SATA_TXP1
C618 C619 SCD01U50V2KX-1GP
U17A
1 OF 6
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH9M-GP-NF
71.ICH9M.00U
71.ICH9M.C1U
LPC_LAD[0..3]
LPC_LFRAME#
TP127 Do Not Stuff
TP41 Do Not Stuff
KA20GATE
H_A20M#
H_DPRSTP#
H_DPSLP#
H_FERR#
H_PWRGD
H_IGNNE#
H_INIT#
H_INTR
KBRCIN#
H_NMI
H_SMI#
H_STPCLK#
H_THERMTRIP_R
PM_THRMTRIP-A#
ICH_TP8
TP132 Do Not Stuff
R480 Do Not Stuff DY
R503 56R2J-4-GP
R502 56R2J-4-GP
R542 Do Not Stuff
R477 Do Not Stuff DY
R504 56R2J-4-GP
R494 Do Not Stuff DY
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
eSATA_RXN_C
eSATA_RXP_C
eSATA_TXN_C
eSATA_TXP_C
SCD01U50V2KX-1GP
C718
C719
SC
CLK_PCIE_SATA#
CLK_PCIE_SATA
SATARBIAS
R490 24D9R2F-L-GP
Place within 500 mils of ICH9 ball
RN53
SRN10KJ-5-GP
H_INIT# G
H_INIT#
FWH_INIT#
Q29
MMBT3904-3-GP
84.03904.L06
R417 330KR2F-L-GP
R105 Do Not Stuff DY
R418 330KR2F-L-GP
R104 Do Not Stuff DY
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
Document Number
Eiger
Rev
-1
Date: Tuesday, April 01, 2008
Sheet 19 of 50


U17B
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
U17C
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
U17D
PCI-Express
Direct Media Interface
SPI
USB
LAN
MINICARD1
MINICARD2
Card Reader
NEW CARD
USB
Pair
Device
0
USB1
1
USB4
2
ESATA-USB2
3
USB5 (DOCK)
4
USB3
5
Bluetooth
6
FP
7
MINIC1
8
WEBCAM
9
NEW1
10
MINIC2
11
NC
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC(Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
GNT0 and SPI_CS#1 have a weak internal pull up
SD
PlanarID
(1,0)
SA: 0,0
SB: 1,0
SC: 0,1
SD: 1,1
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size
Document Number
Eiger
Rev
-1
Date: Tuesday, April 01, 2008
Sheet 20 of 50


U17F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
6uA in G3
646mA
1.16A
Layout Note:Place near ICH9M
23mA
41mA
2mA
47mA
1.64A
VCC3_3=308mA
32mA
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
19mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH9
Do Not Stuff
UMA
DIS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
Eiger
Tuesday, April 01, 2008
Sheet 21 of 50





緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ICH9-M (4 of 4)***

Size	Document Number	Rev
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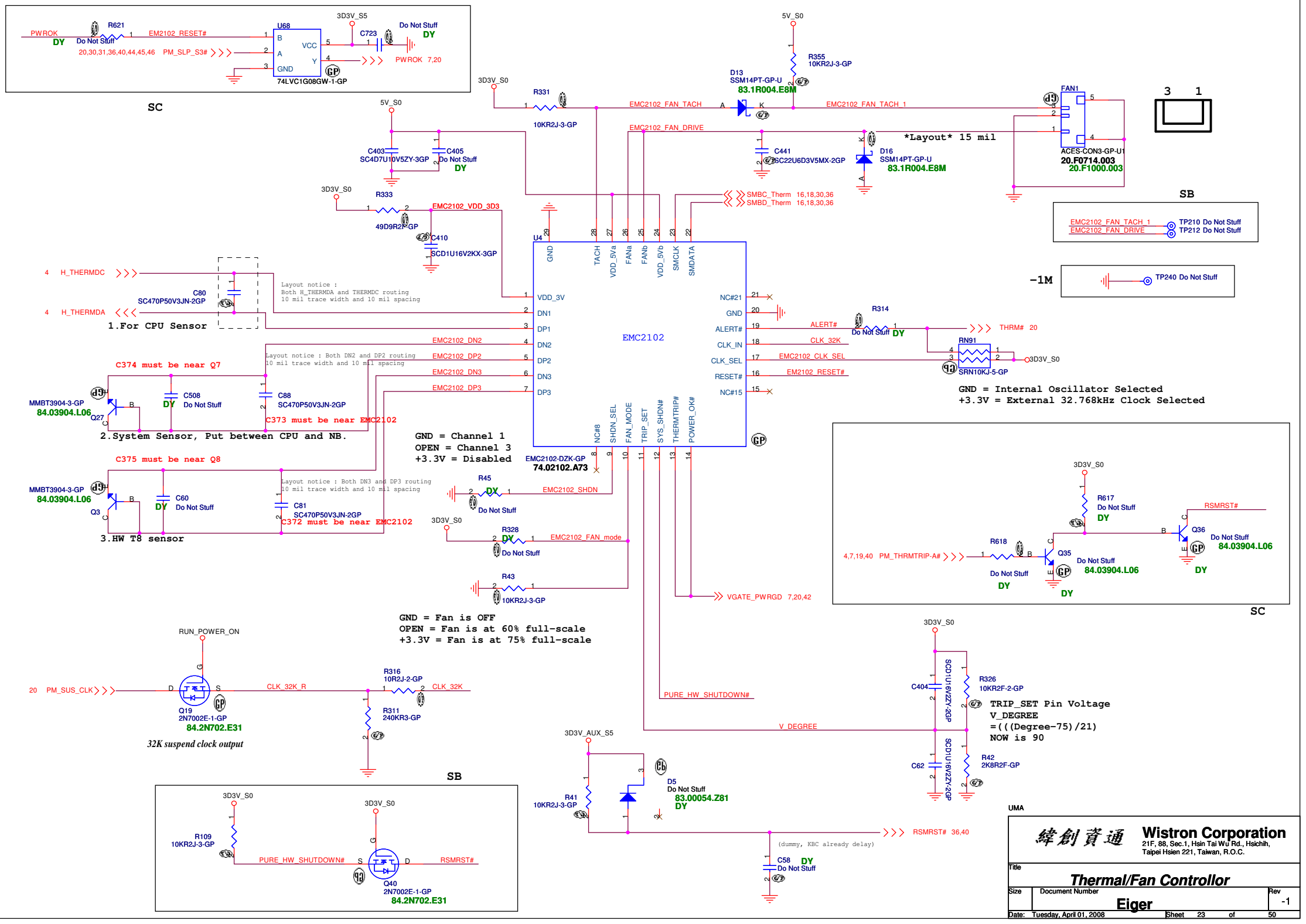
Date: Tuesday, April 01, 2008 Sheet 22 of 50


SC
PWROK
DY
R621
Do Not Stuff
EM2102_RESET#
20,30,31,36,40,44,45,46 PM_SLP_S3#
U68
B
A
GND
VCC
Y
74LVC1G08GW-1-GP
3D3V_S5
C723
Do Not Stuff
DY
PWROK 7,20
5V_S0
R355
10KR2J-3-GP
D13
SSM14PT-GP-U
83.1R004.E8M
3D3V_S0
R331
10KR2J-3-GP
EMC2102_FAN_TACH
EMC2102_FAN_TACH_1
EMC2102_FAN_DRIVE
FAN1
ACES-CON3-GP-U1
20.F0714.003
20.F1000.003
Layout 15 mil
C441
SC22U6D3V5MX-2GP
D16
SSM14PT-GP-U
83.1R004.E8M
C403
SC4D7U10V5ZY-3GP
C405
Do Not Stuff
DY
R333
49D9R2F-GP
EMC2102_VDD_3D3
C410
SCD1U16V2KX-3GP
SMBC_Therm 16,18,30,36
SMBD_Therm 16,18,30,36
SB
EMC2102_FAN_TACH_1
EMC2102_FAN_DRIVE
TP210 Do Not Stuff
TP212 Do Not Stuff
-1M
TP240 Do Not Stuff
U4
GND
TACH
VDD_5Va
FANa
FANb
VDD_5Vb
SMCLK
SMDATA
VDD_3V
DN1
DP1
DN2
DP2
DN3
DP3
NC#21
GND
ALERT#
CLK_IN
CLK_SEL
RESET#
NC#15
NC#8
SHDN_SEL
FAN_MODE
TRIP_SET
SYS_SHDN#
THERMTRIP#
POWER_OK#
EMC2102
EMC2102-DZK-GP
74.02102.A73
4 H_THERMDC
4 H_THERMDA
C80
SC470P50V3JN-2GP
Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing
1.For CPU Sensor
R314
Do Not Stuff
DY
THRM# 20
RN91
SRN10KJ-5-GP
3D3V_S0
ALERT#
CLK_32K
EMC2102_CLK_SEL
EM2102_RESET#
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
C374 must be near Q7
MMBT3904-3-GP
84.03904.L06
Q27
C508
Do Not Stuff
DY
C88
SC470P50V3JN-2GP
C373 must be near EMC2102
Layout notice : Both DN2 and DP2 routing
10 mil trace width and 10 mil spacing
EMC2102_DN2
EMC2102_DP2
EMC2102_DN3
EMC2102_DP3
2.System Sensor, Put between CPU and NB.
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
C375 must be near Q8
MMBT3904-3-GP
84.03904.L06
Q3
C60
Do Not Stuff
DY
C81
SC470P50V3JN-2GP
C372 must be near EMC2102
Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing
3.HW T8 sensor
R45
Do Not Stuff
DY
EMC2102_SHDN
3D3V_S0
R328
Do Not Stuff
DY
EMC2102_FAN_mode
R43
10KR2J-3-GP
VGATE_PWRGD 7,20,42
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
SC
3D3V_S0
R617
Do Not Stuff
DY
RSMRST#
R618
Do Not Stuff
DY
Q35
Do Not Stuff
84.03904.L06
Q36
Do Not Stuff
84.03904.L06
DY
4,7,19,40 PM_THRMTRIP-A#
RUN_POWER_ON
20 PM_SUS_CLK
Q19
2N7002E-1-GP
84.2N702.E31
CLK_32K_R
R316
10R2J-2-GP
CLK_32K
R311
240KR3-GP
32K suspend clock output
PURE_HW_SHUTDOWN#
V_DEGREE
3D3V_S0
C404
SCD1U16V2ZY-2GP
R326
10KR2F-2-GP
C62
SCD1U16V2ZY-2GP
R42
2K8R2F-GP
TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)
NOW is 90
3D3V_AUX_S5
R41
10KR2J-3-GP
D5
Do Not Stuff
83.00054.Z81
DY
RSMRST# 36,40
(dummy, KBC already delay)
C58
Do Not Stuff
DY
SB
3D3V_S0
R109
10KR2J-3-GP
PURE_HW_SHUTDOWN#
Q40
2N7002E-1-GP
84.2N702.E31
RSMRST#
UMA
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Wistron Corporation
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Title
Thermal/Fan Controllor
Size
Document Number
Eiger
Rev
-1
Date: Tuesday, April 01, 2008
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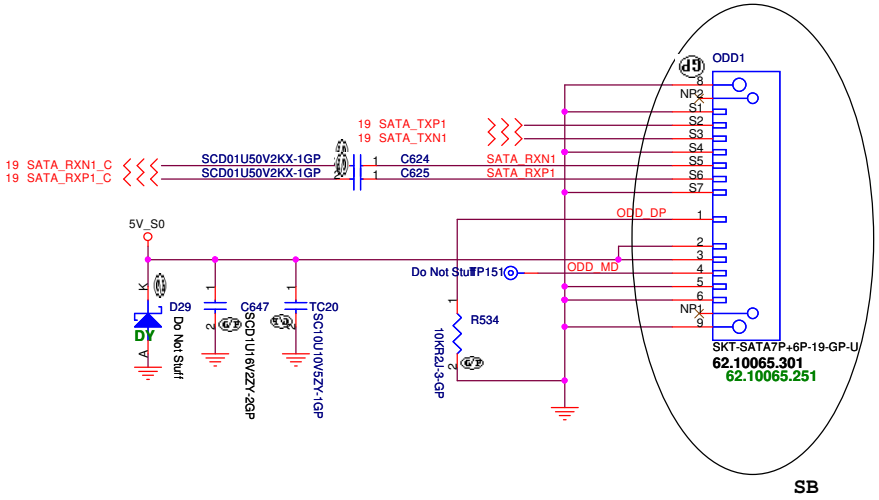
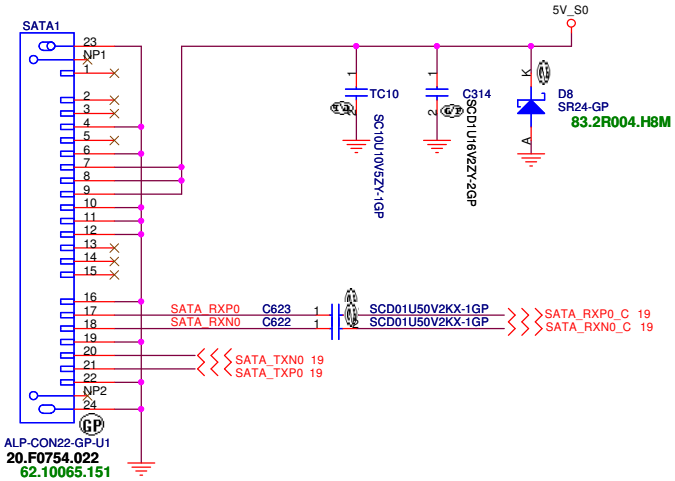
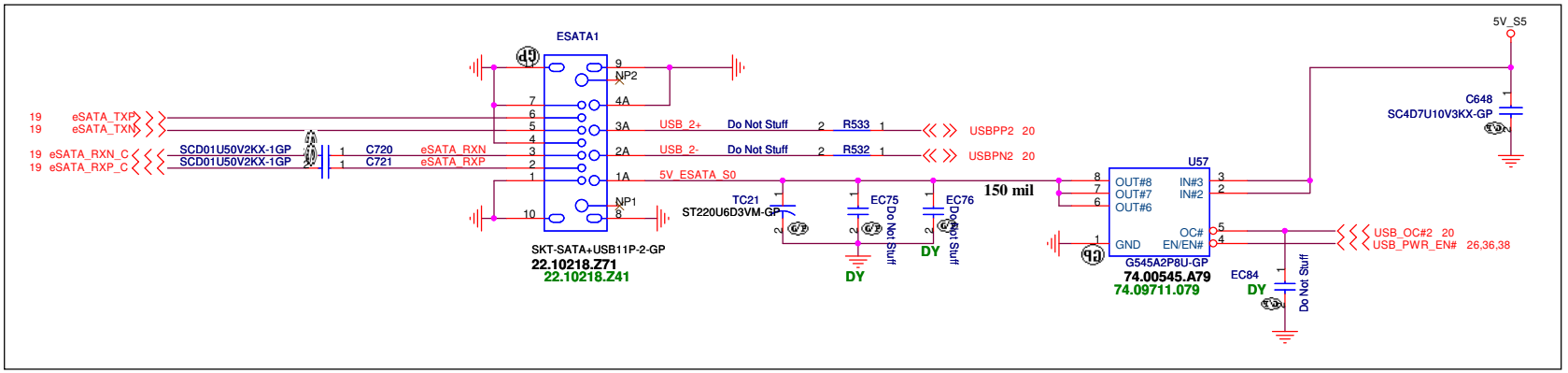
SATA ODD Connector



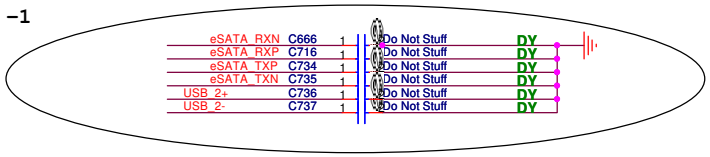
SATA Connector



SC



-1



EMI

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Title: HDD & CDROM & ESATA

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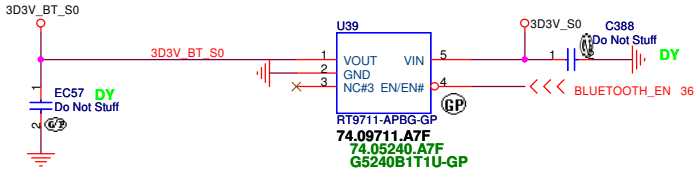
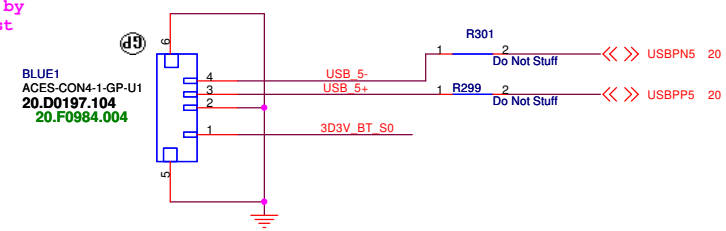
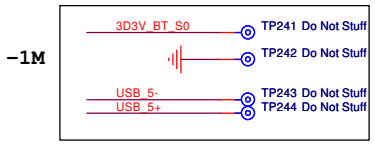
BLUETOOTH MODULE

1.5A / High Active Voltage 2V

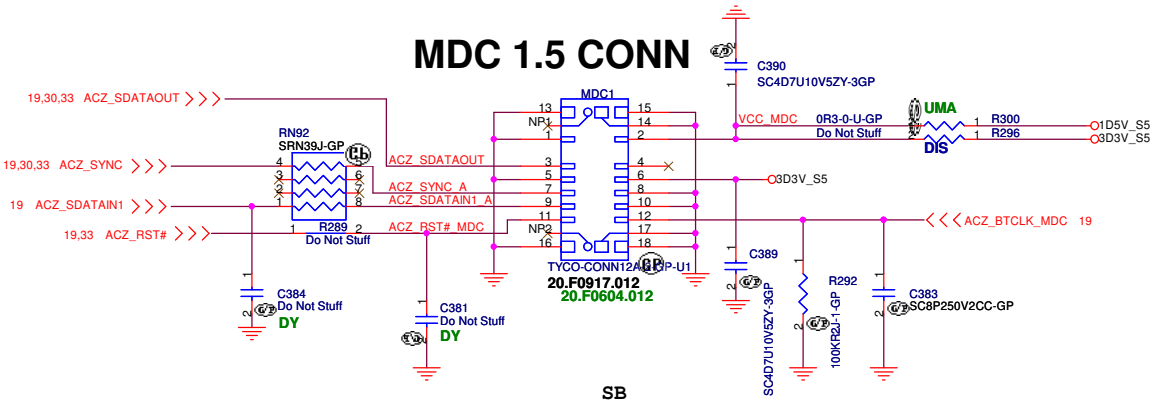


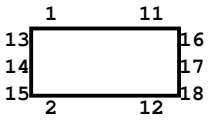
EC21 put near BLUE1 / all USB put one choke near connector by EMI request



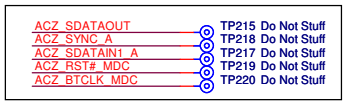


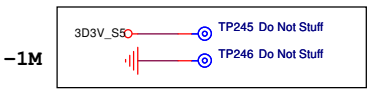
MDC 1.5 CONN





SB





Finger printer

MOVE TO Page 36

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Title: BLUETOOTH MDC Finger printer

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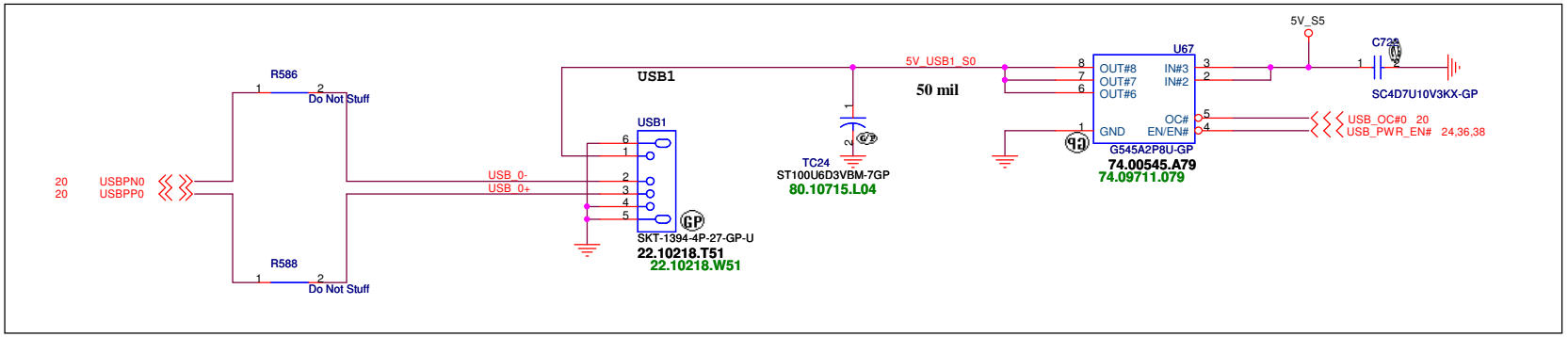
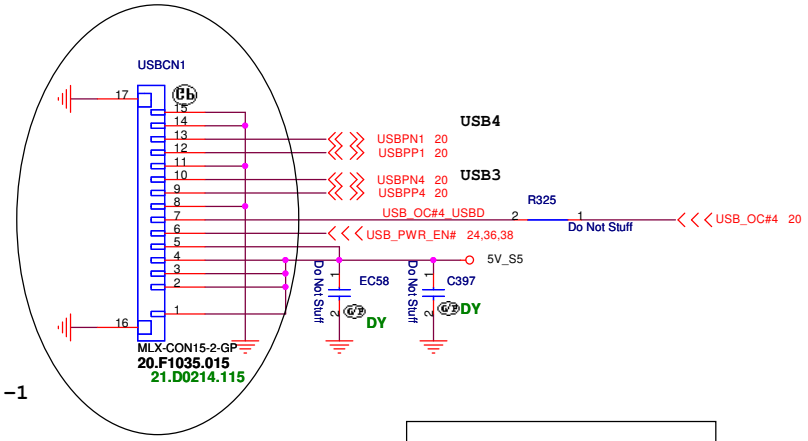
SC

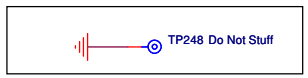




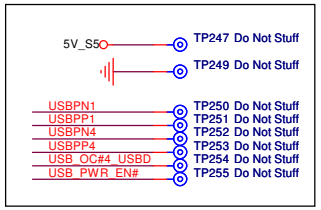
-1

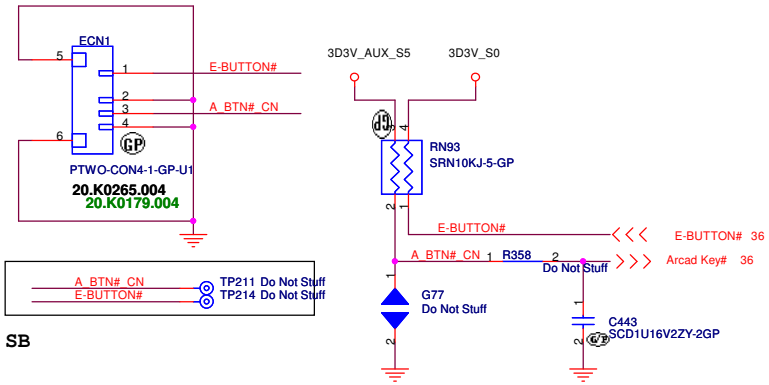
ECN BOARD

-1M



-1M





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Title: USB & ECN

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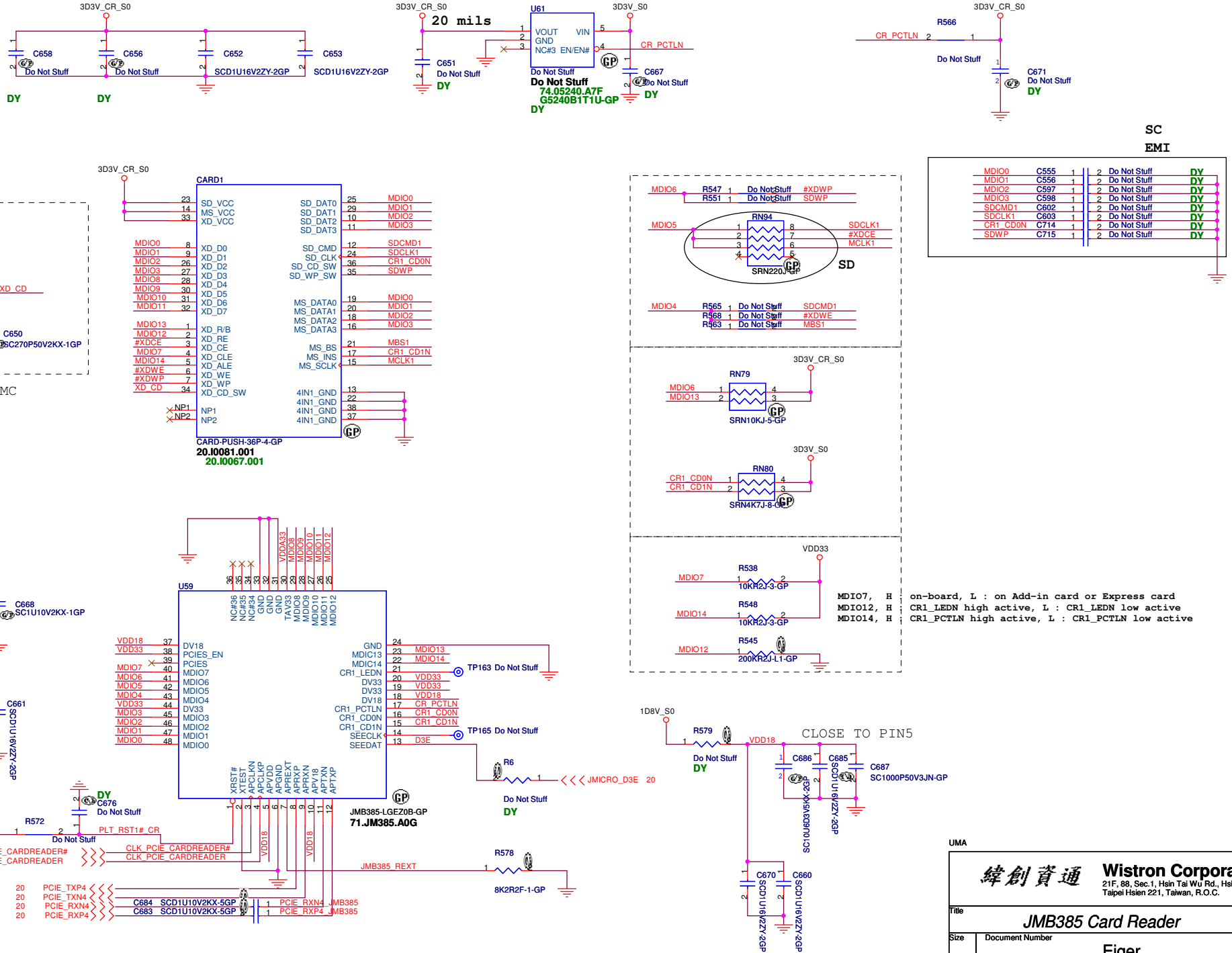
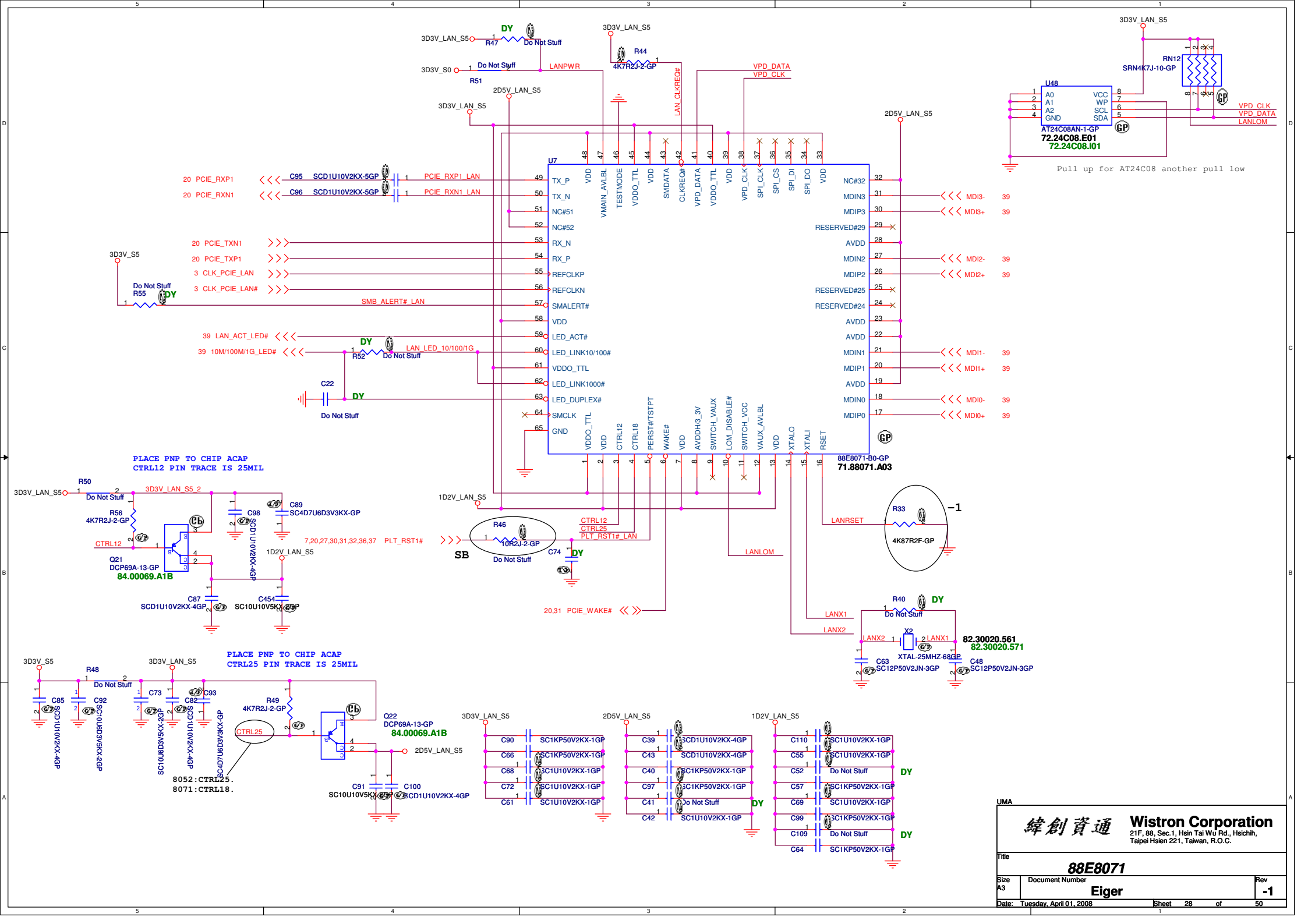
5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)

1.5A / High Active Voltage 2V




U7
88E8071-B0-GP
71.88071.A03
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
8052:CTRL25.
8071:CTRL18.
U48
AT24C08AN-1-GP
72.24C08.E01
72.24C08.I01
Pull up for AT24C08 another pull low
RN12
SRN4K7J-10-GP
XTAL-25MHZ-68GP
82.30020.561
82.30020.571
4K87R2F-GP
Q21
DCP69A-13-GP
84.00069.A1B
Q22
DCP69A-13-GP
84.00069.A1B
UMA
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Title
88E8071
Size
A3
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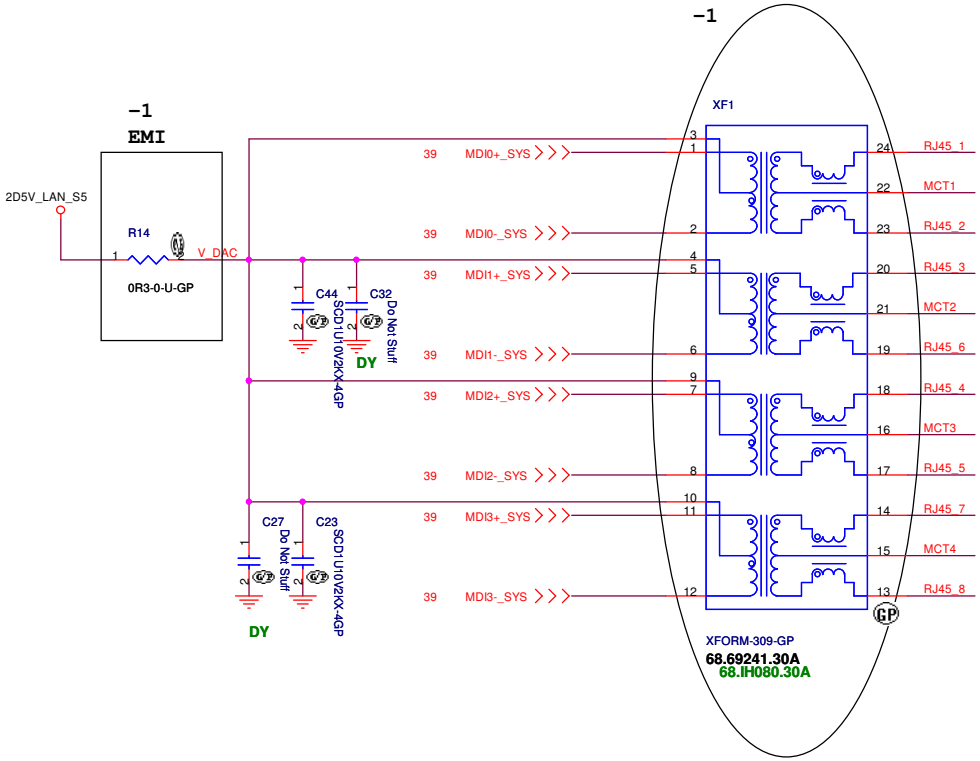
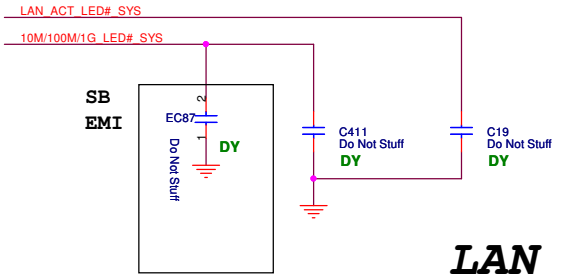
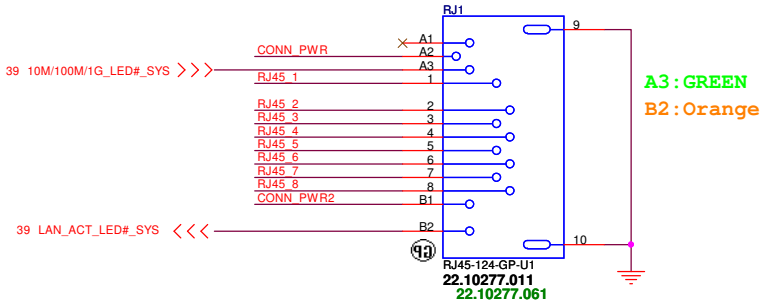
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.





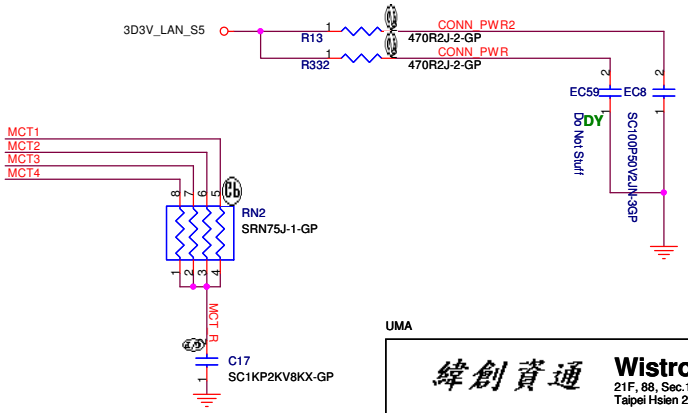
LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



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Title		
LAN CONN		
Size: A3	Document Number	Rev: -1
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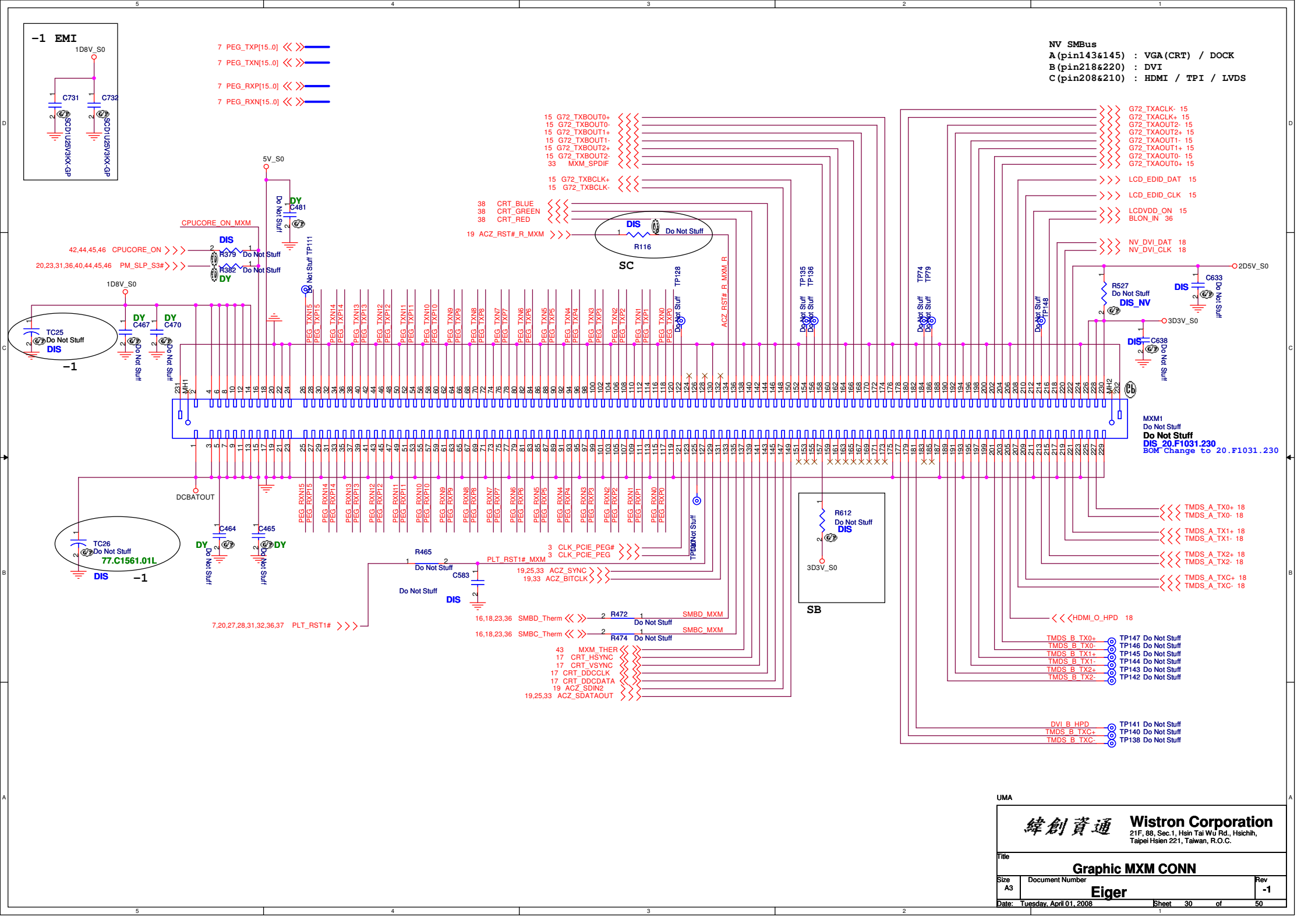
-1 EMI
1D8V_S0
C731
C732
SCD1U25V3KX-GP
7 PEG_TXP[15..0]
7 PEG_TXN[15..0]
7 PEG_RXP[15..0]
7 PEG_RXN[15..0]
NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS
15 G72_TXBOUT0+
15 G72_TXBOUT0-
15 G72_TXBOUT1+
15 G72_TXBOUT1-
15 G72_TXBOUT2+
15 G72_TXBOUT2-
33 MXM_SPDIF
15 G72_TXBCLK+
15 G72_TXBCLK-
38 CRT_BLUE
38 CRT_GREEN
38 CRT_RED
19 ACZ_RST#_R_MXM
R116
SC
G72_TXACLK- 15
G72_TXACLK+ 15
G72_TXAOUT2- 15
G72_TXAOUT2+ 15
G72_TXAOUT1- 15
G72_TXAOUT1+ 15
G72_TXAOUT0- 15
G72_TXAOUT0+ 15
LCD_EDID_DAT 15
LCD_EDID_CLK 15
LCDVDD_ON 15
BLON_IN 36
NV_DVI_DAT 18
NV_DVI_CLK 18
2D5V_S0
3D3V_S0
5V_S0
CPUCORE_ON_MXM
42,44,45,46 CPUCORE_ON
20,23,31,36,40,44,45,46 PM_SLP_S3#
R379
R382
C481
R527
C633
C638
TC25
TC26
77.C1561.01L
C467
C470
C464
C465
DCBATOUT
R465
C583
PLT_RST1# 7,20,27,28,31,32,36,37
PLT_RST1_MXM
3 CLK_PCIE_PEG#
3 CLK_PCIE_PEG
19,25,33 ACZ_SYNC
19,33 ACZ_BITCLK
16,18,23,36 SMBD_Therm
16,18,23,36 SMBC_Therm
R472
R474
SMBD_MXM
SMBC_MXM
43 MXM_THER
17 CRT_HSYNC
17 CRT_VSYNC
17 CRT_DDCCLK
17 CRT_DDCDATA
19 ACZ_SDIN2
19,25,33 ACZ_SDATAOUT
R612
3D3V_S0
SB
TMDS_A_TX0+ 18
TMDS_A_TX0- 18
TMDS_A_TX1+ 18
TMDS_A_TX1- 18
TMDS_A_TX2+ 18
TMDS_A_TX2- 18
TMDS_A_TXC+ 18
TMDS_A_TXC- 18
HDMI_O_HPD 18
TMDS_B_TX0+
TMDS_B_TX0-
TMDS_B_TX1+
TMDS_B_TX1-
TMDS_B_TX2+
TMDS_B_TX2-
TP147 Do Not Stuff
TP146 Do Not Stuff
TP145 Do Not Stuff
TP144 Do Not Stuff
TP143 Do Not Stuff
TP142 Do Not Stuff
DVI_B_HPD
TMDS_B_TXC+
TMDS_B_TXC-
TP141 Do Not Stuff
TP140 Do Not Stuff
TP138 Do Not Stuff
MXM1
Do Not Stuff
DIS_20.F1031.230
BOM Change to 20.F1031.230
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Graphic MXM CONN
Size A3
Document Number
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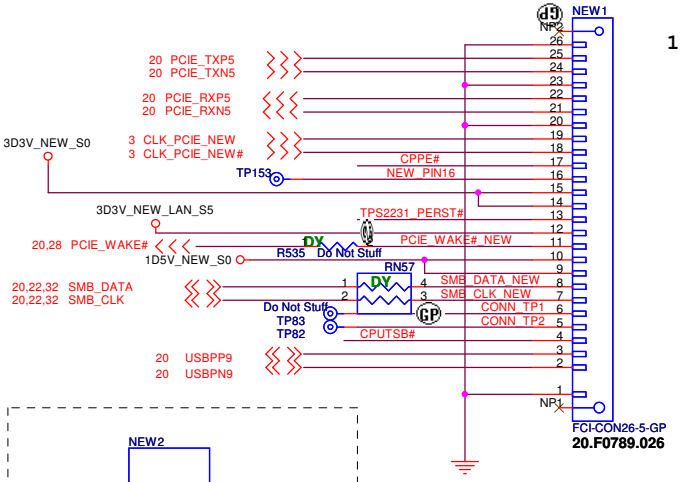
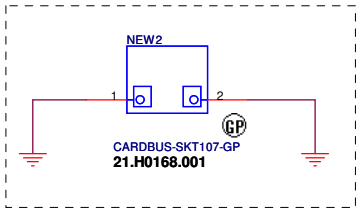
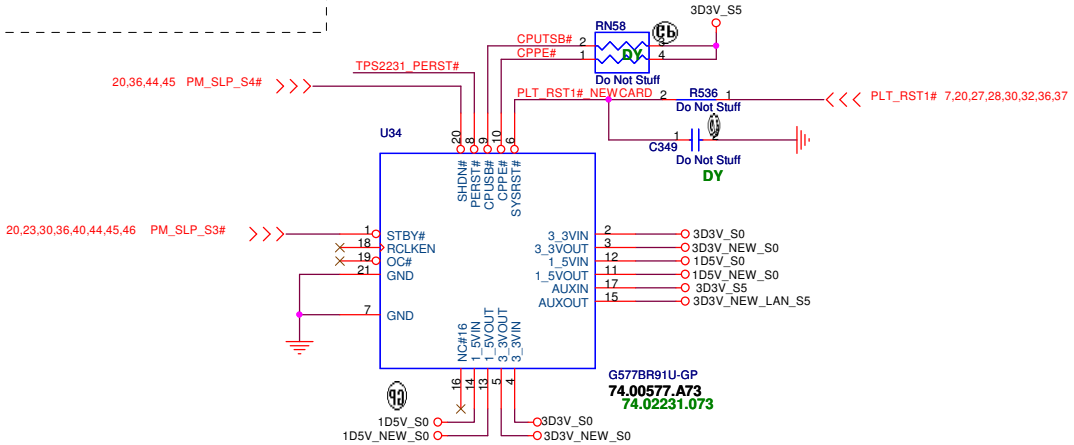
NEWCARD Connector

Reserve the symbol
for bottom side
connector

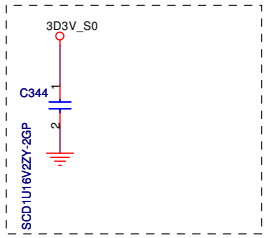
TOP VIEW



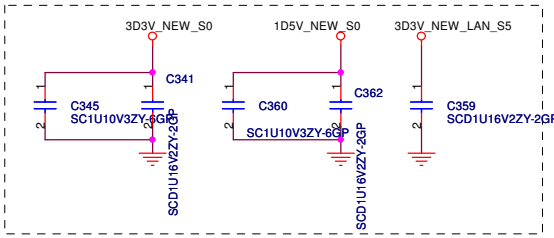




Place them Near to Chip



Place them Near to Connector



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Title: NEW CARD

Size | Document Number: Eiger | Rev: -1

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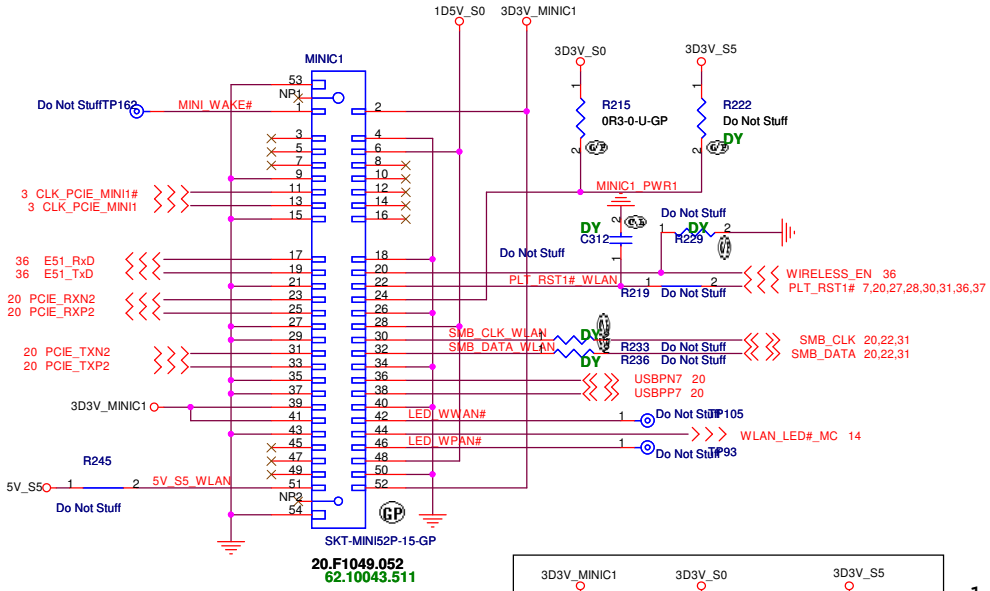
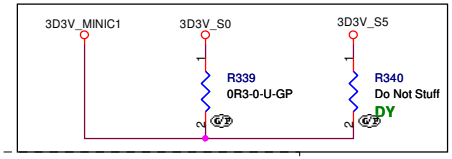
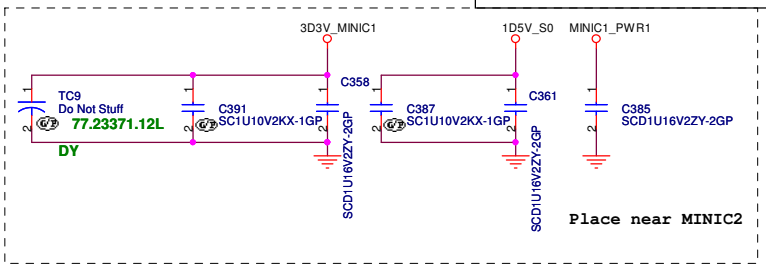
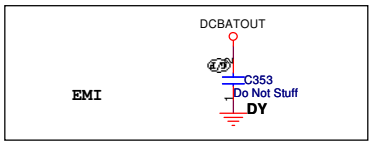
Mini Card Connector(WLAN)



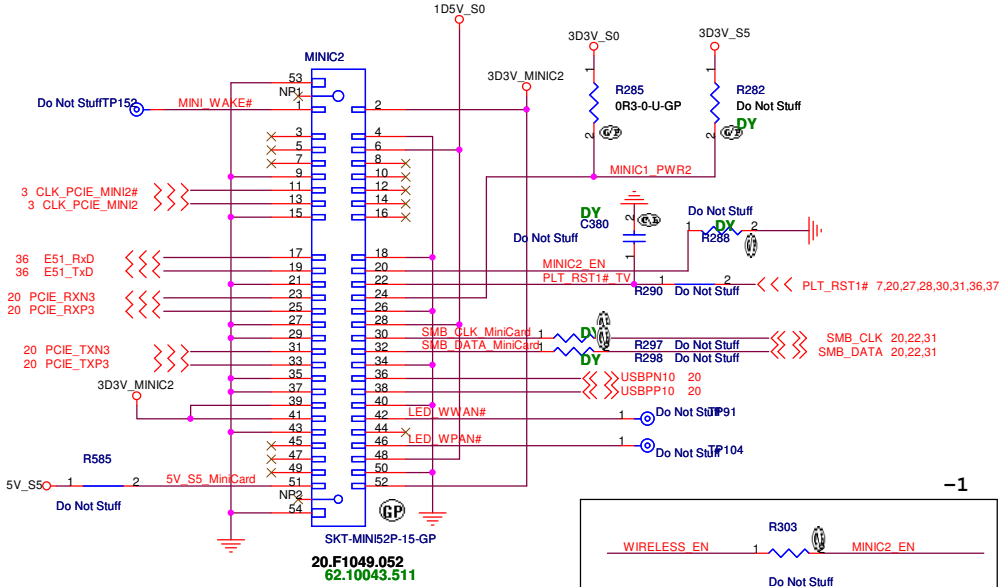
20.F1049.052
62.10043.511



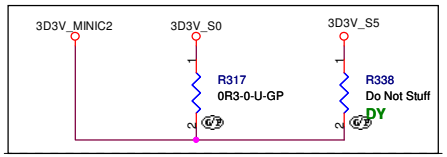


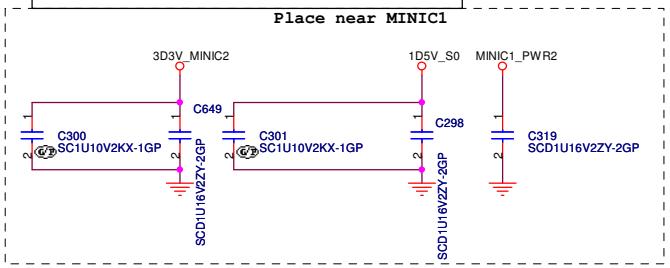


Mini Card Connector(TV)



20.F1049.052
62.10043.511





UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD**

Size	Document Number	Rev
A3	Eiger	-1

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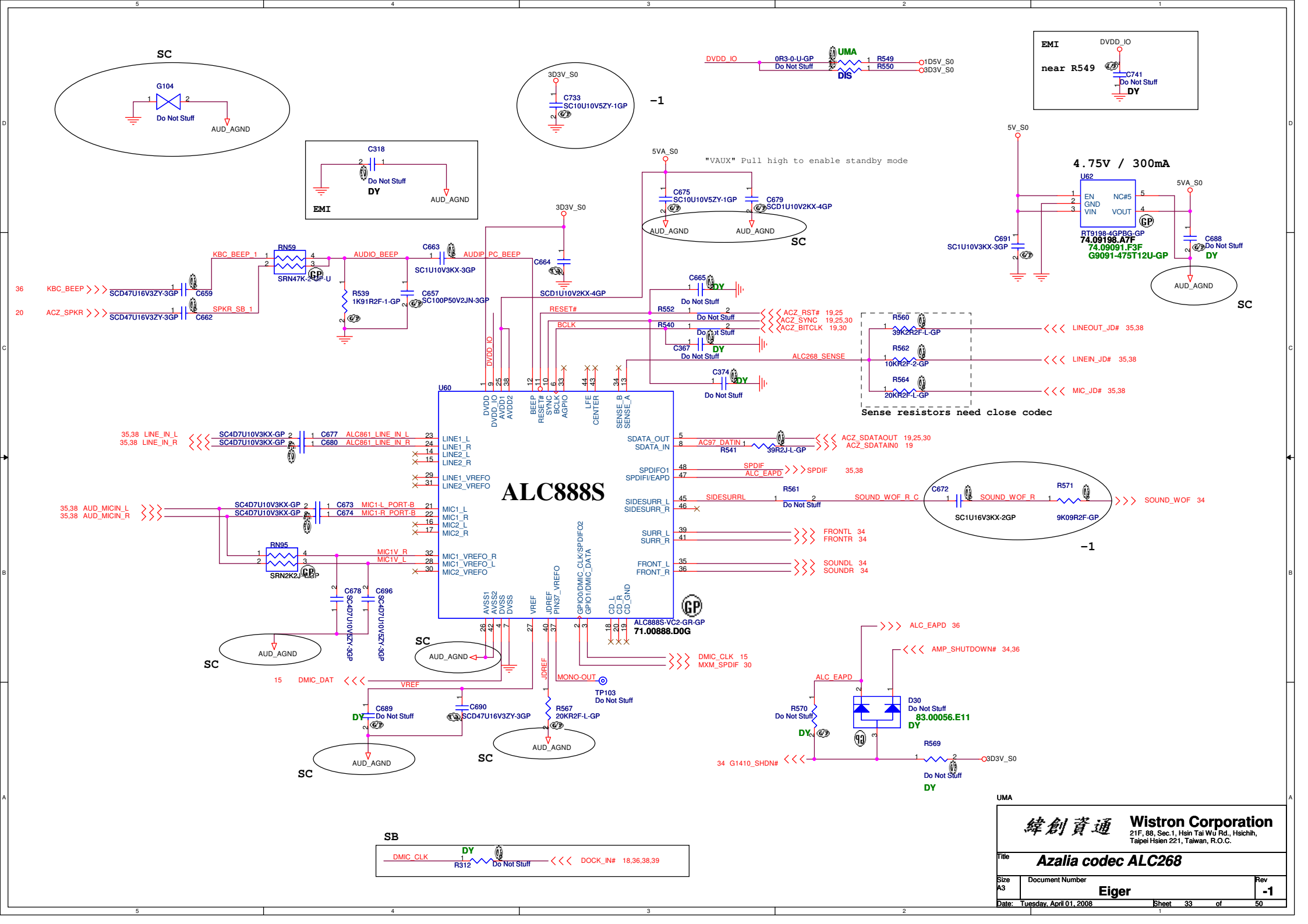
SC
G104
Do Not Stuff
AUD_AGND
3D3V_S0
C733
SC10U10V5ZY-1GP
-1
DVDD_IO
0R3-0-U-GP
Do Not Stuff
UMA
DIS
R549
R550
1D5V_S0
3D3V_S0
EMI
DVDD_IO
near R549
C741
Do Not Stuff
DY
C318
Do Not Stuff
DY
AUD_AGND
EMI
5VA_S0
"VAUX" Pull high to enable standby mode
C675
SC10U10V5ZY-1GP
C679
SCD1U10V2KX-4GP
AUD_AGND
AUD_AGND
SC
5V_S0
4.75V / 300mA
U62
EN
GND
VIN
NC#5
VOUT
RT9198-4GPBG-GP
74.09198.A7F
74.09091.F3F
G9091-475T12U-GP
C691
SC1U10V3KX-3GP
5VA_S0
C688
Do Not Stuff
DY
AUD_AGND
SC
3D3V_S0
KBC_BEEP_1
RN59
SRN47K-2-GP-U
AUDIO_BEEP
C663
SC1U10V3KX-3GP
AUDIP_PC_BEEP
C664
SCD1U10V2KX-4GP
36 KBC_BEEP
SCD47U16V3ZY-3GP
C659
20 ACZ_SPKR
SCD47U16V3ZY-3GP
C662
SPKR_SB_1
R539
1K91R2F-1-GP
C657
SC100P50V2JN-3GP
C665
DY
Do Not Stuff
RESET#
R552
Do Not Stuff
ACZ_RST# 19,25
ACZ_SYNC 19,25,30
ACZ_BITCLK 19,30
BCLK
R540
Do Not Stuff
C367
DY
Do Not Stuff
ALC268_SENSE
C374
DY
Do Not Stuff
R560
39K2R2F-L-GP
R562
10KR2F-2-GP
R564
20KR2F-L-GP
LINEOUT_JD# 35,38
LINEIN_JD# 35,38
MIC_JD# 35,38
Sense resistors need close codec
U60
DVDD
DVDD_IO
AVDD1
AVDD2
BEEP
RESET#
SYNC
BCLK
AGPIO
LFE
CENTER
SENSE_B
SENSE_A
35,38 LINE_IN_L
35,38 LINE_IN_R
SC4D7U10V3KX-GP
C677
ALC861_LINE_IN_L
C680
ALC861_LINE_IN_R
LINE1_L
LINE1_R
LINE2_L
LINE2_R
LINE1_VREFO
LINE2_VREFO
ALC888S
SDATA_OUT
SDATA_IN
AC97_DATIN
R541
39R2J-L-GP
ACZ_SDATAOUT 19,25,30
ACZ_SDATAIN0 19
SPDIFO1
SPDIFI/EAPD
SPDIF
ALC_EAPD
SPDIF 35,38
SIDESURR_L
SIDESURR_R
SIDESURRL
R561
Do Not Stuff
SOUND_WOF_R_C
C672
SOUND_WOF_R
R571
SOUND_WOF
SC1U16V3KX-2GP
9K09R2F-GP
SOUND_WOF 34
-1
35,38 AUD_MICIN_L
35,38 AUD_MICIN_R
SC4D7U10V3KX-GP
C673
MIC1-L_PORT-B
C674
MIC1-R_PORT-B
MIC1_L
MIC1_R
MIC2_L
MIC2_R
RN95
SRN2K2J-GP
MIC1V_R
MIC1V_L
MIC1_VREFO_R
MIC1_VREFO_L
MIC2_VREFO
SURR_L
SURR_R
FRONTL 34
FRONTR 34
FRONT_L
FRONT_R
SOUNDL 34
SOUNDR 34
C678
SC47U10V3ZY-3GP
C696
SC47U10V3ZY-3GP
AVSS1
AVSS2
DVSS
DVSS
VREF
JDREF
PIN37_VREFO
GPIO0/DMIC_CLK/SPDIFO2
GPIO1/DMIC_DATA
CD_L
CD_R
CD_GND
ALC888S-VC2-GR-GP
71.00888.D0G
AUD_AGND
SC
AUD_AGND
SC
DMIC_CLK 15
MXM_SPDIF 30
15 DMIC_DAT
VREF
JDREF
MONO-OUT
TP103
Do Not Stuff
C689
DY
Do Not Stuff
C690
SCD47U16V3ZY-3GP
R567
20KR2F-L-GP
AUD_AGND
SC
AUD_AGND
SC
ALC_EAPD 36
AMP_SHUTDOWN# 34,36
ALC_EAPD
R570
Do Not Stuff
DY
D30
Do Not Stuff
83.00056.E11
DY
R569
34 G1410_SHDN#
3D3V_S0
Do Not Stuff
DY
SB
DMIC_CLK
DY
R312
Do Not Stuff
DOCK_IN# 18,36,38,39
UMA
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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
Azalia codec ALC268
Size
A3
Document Number
Eiger
Rev
-1
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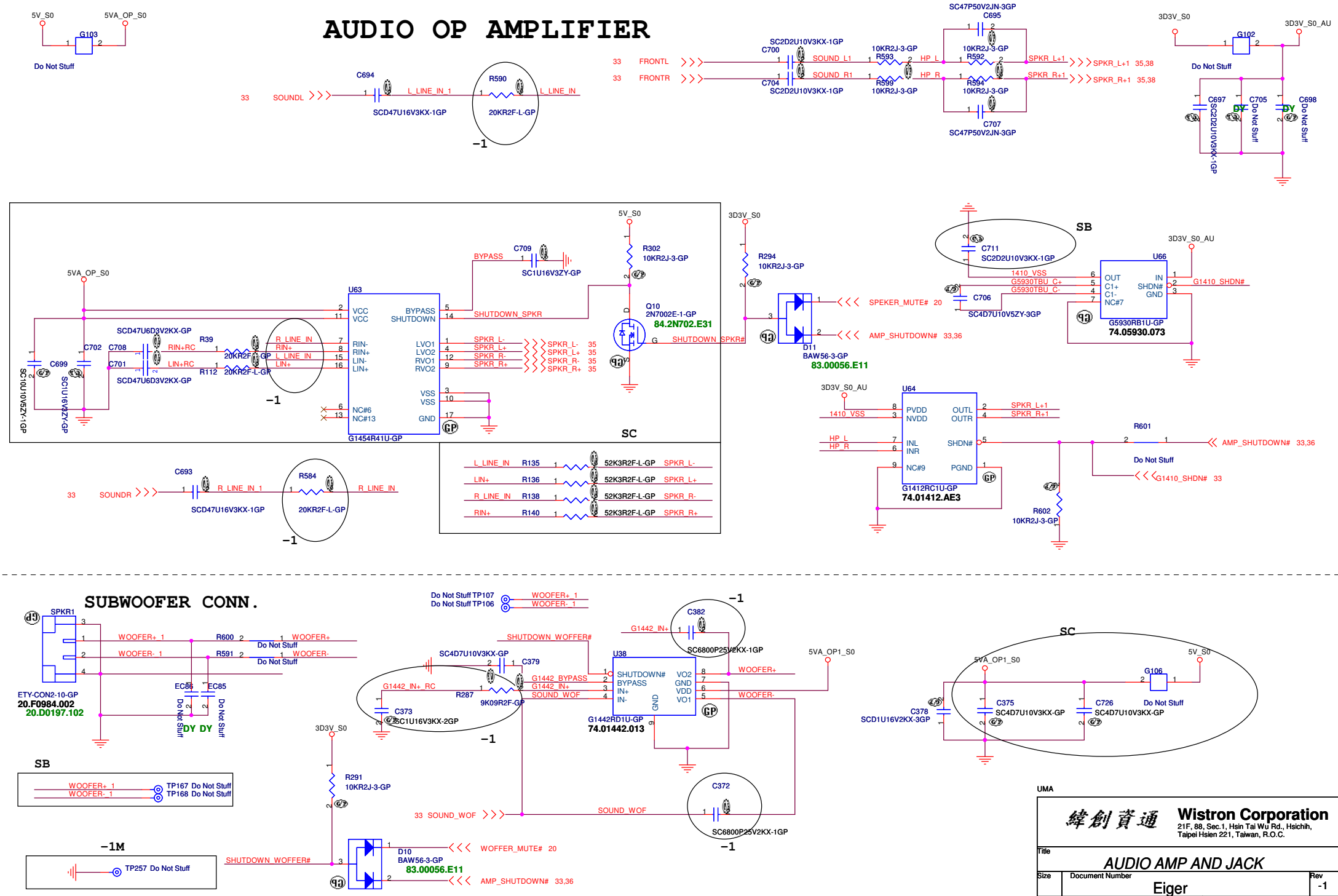
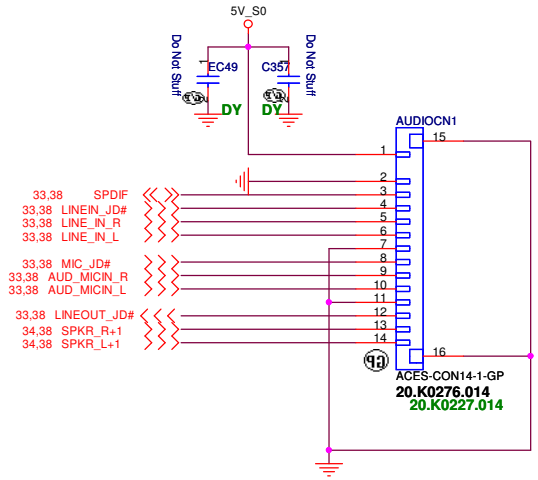
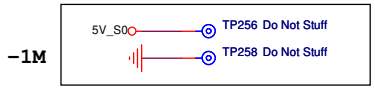
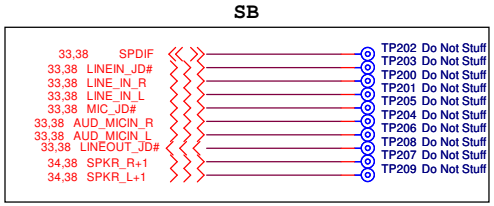
AUDIO OP AMPLIFIER

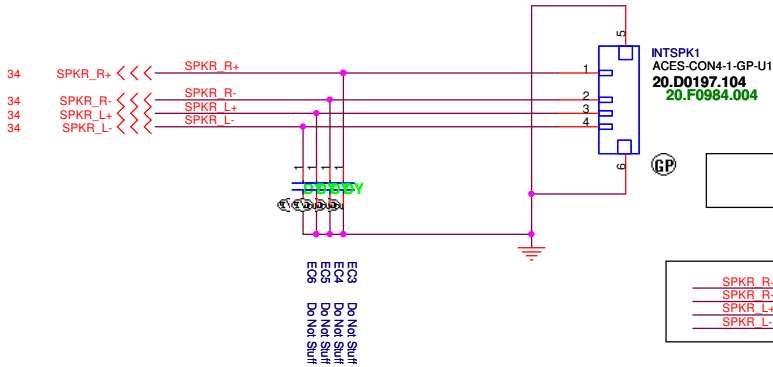


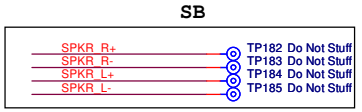






Internal Speaker





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Title	*AUDIO JACK*	
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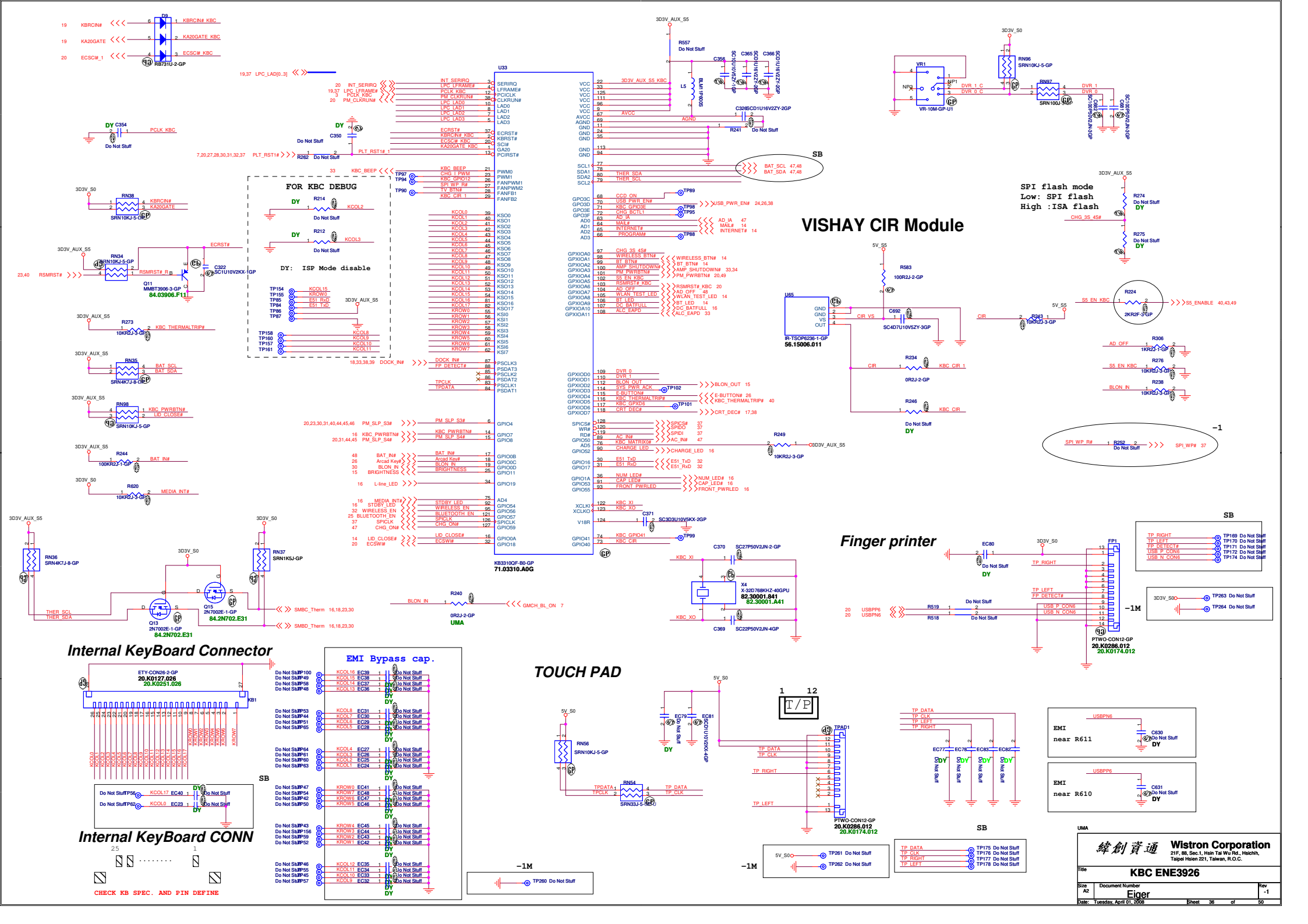
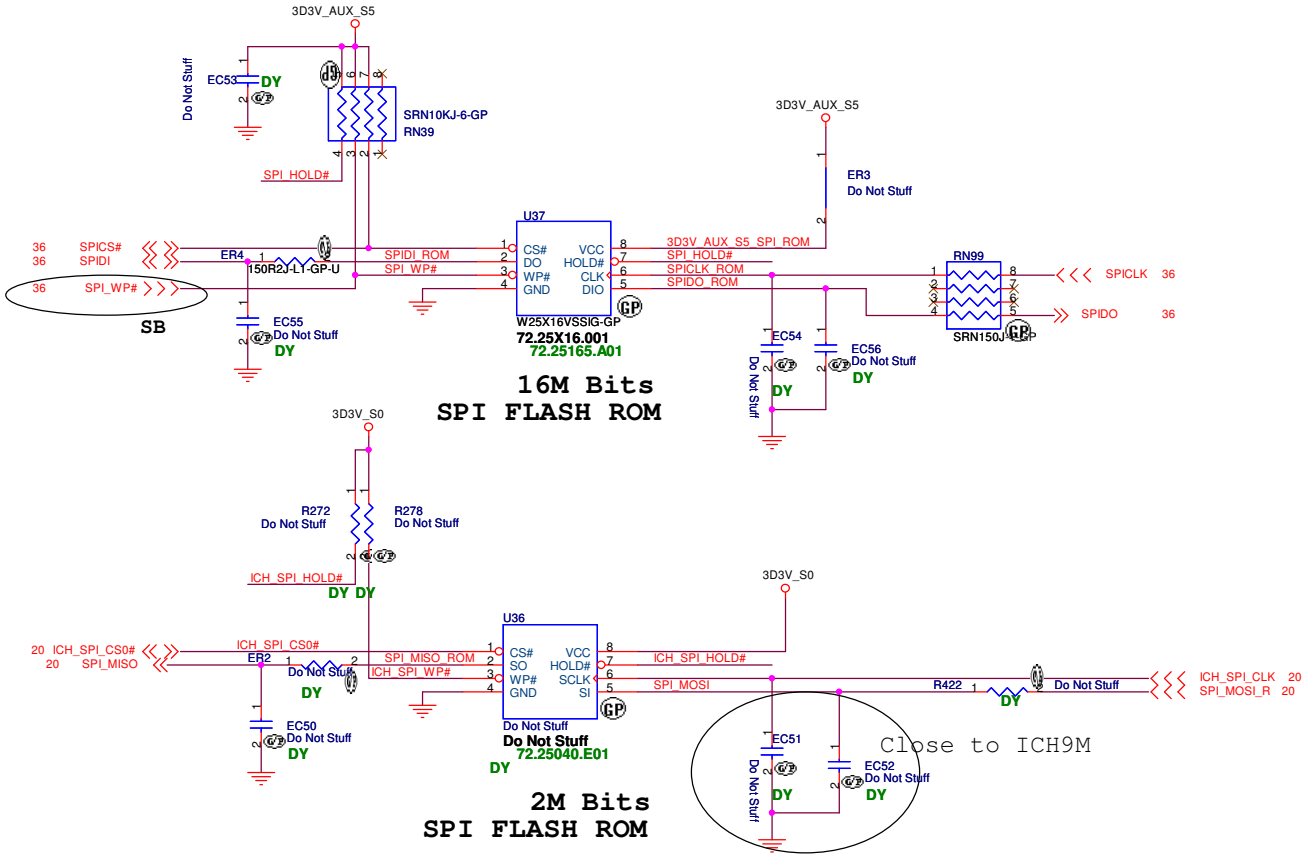
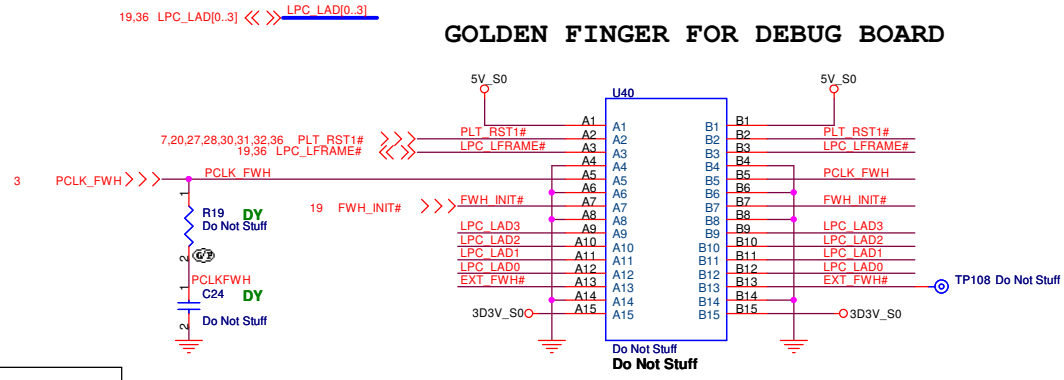

FOR KBC DEBUG
DY: ISP Mode disable
VISHAY CIR Module
SPI flash mode
Low: SPI flash
High :ISA flash
Finger printer
Internal KeyBoard Connector
Internal KeyBoard CONN
TOUCH PAD
EMI Bypass cap.
CHECK KB SPEC. AND PIN DEFINE
KB3310QF-B0-GP
71.03310.A0G
Wistron Corporation
KBC ENE3926
Eiger

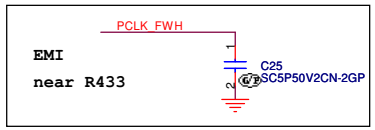


TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)





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Title: ***BIOS***

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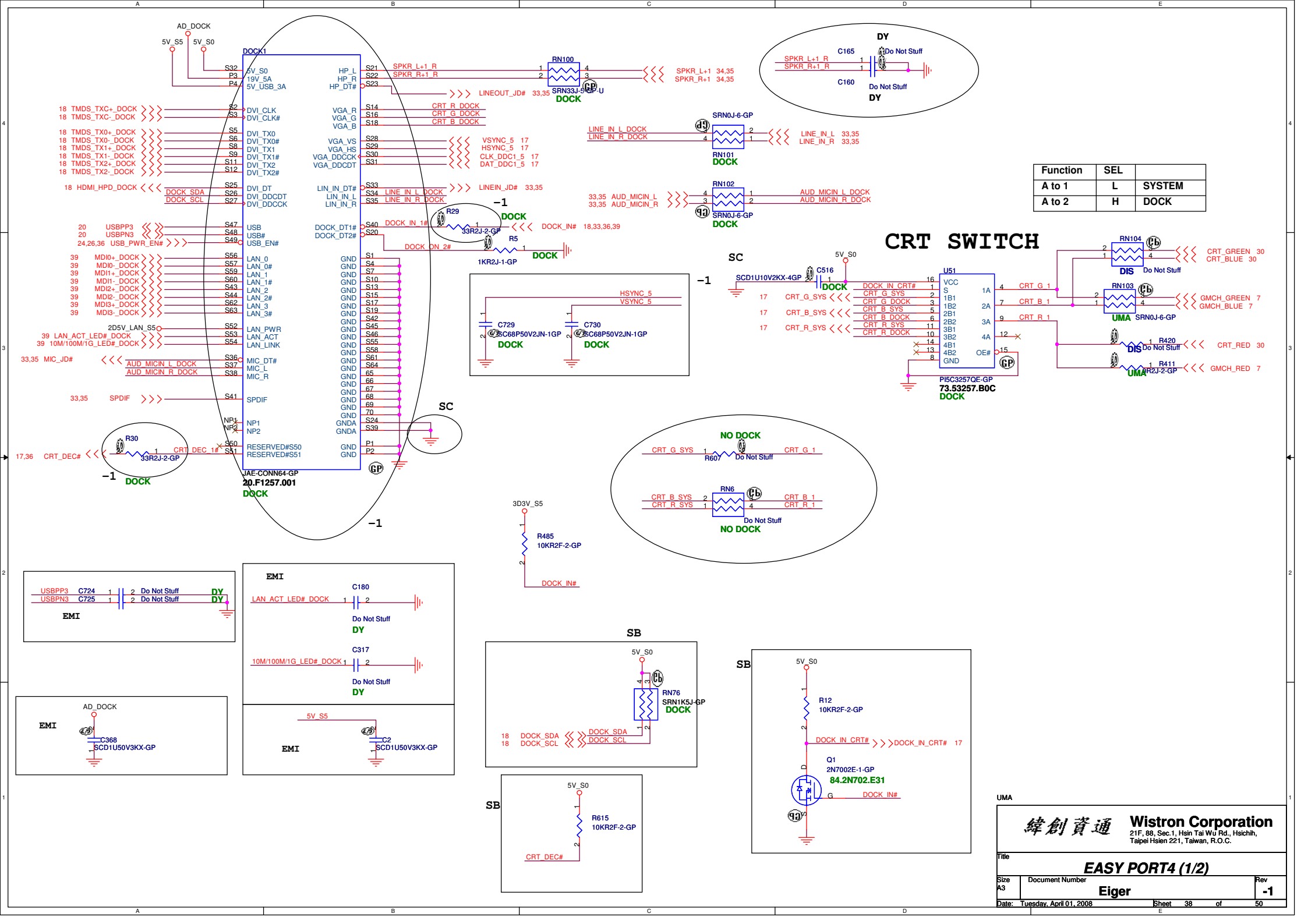

Function	SEL	
A to 1	L	SYSTEM
A to 2	H	DOCK

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Title: **EASY PORT4 (1/2)**

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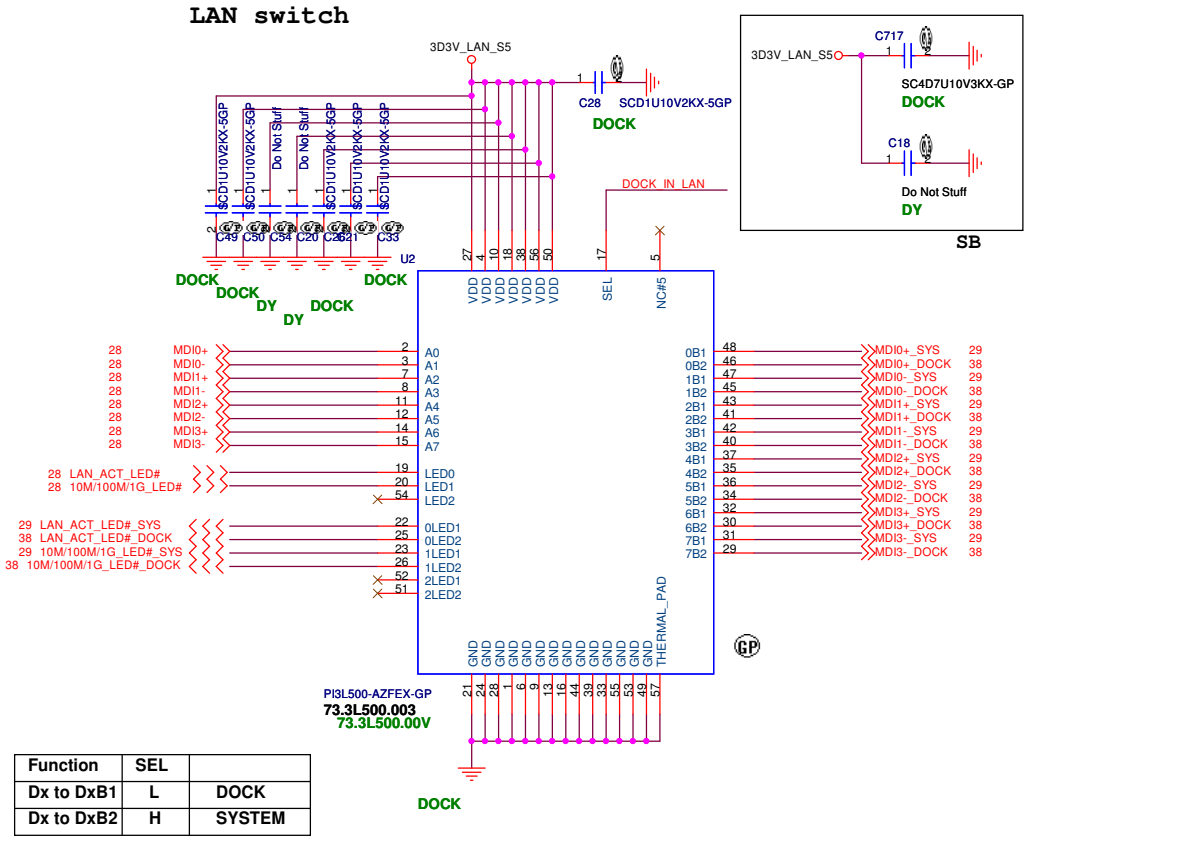
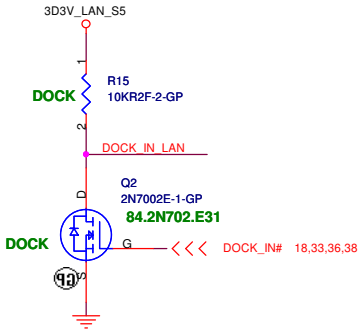
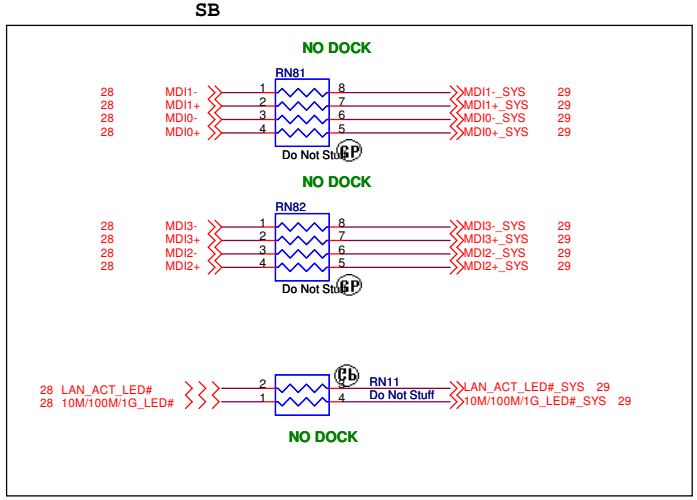
LAN switch



Function	SEL	
Dx to DxB1	L	DOCK
Dx to DxB2	H	SYSTEM





UMA

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Title: EASY PORT4 (2/2)

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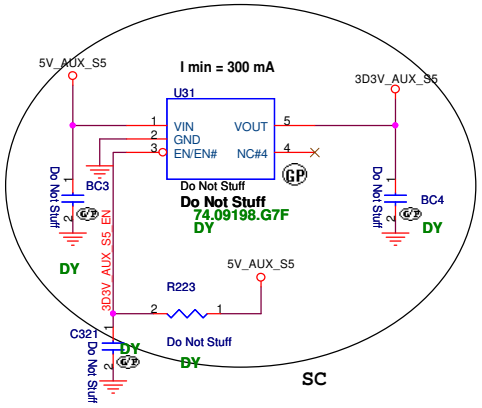
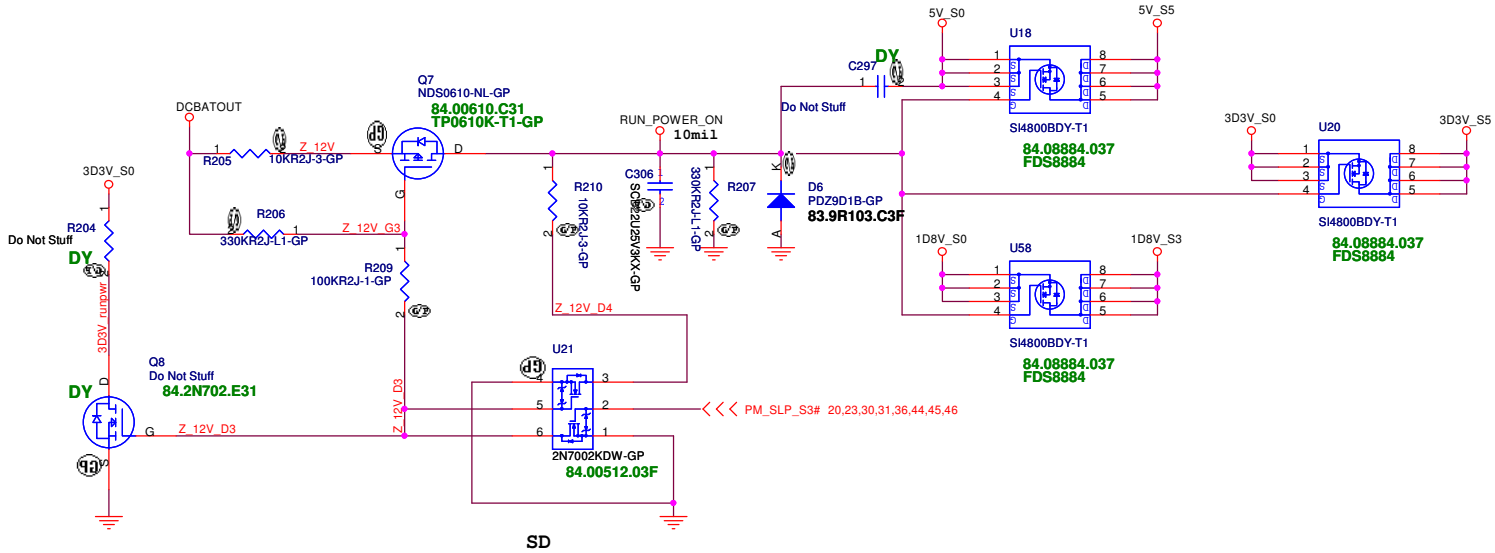
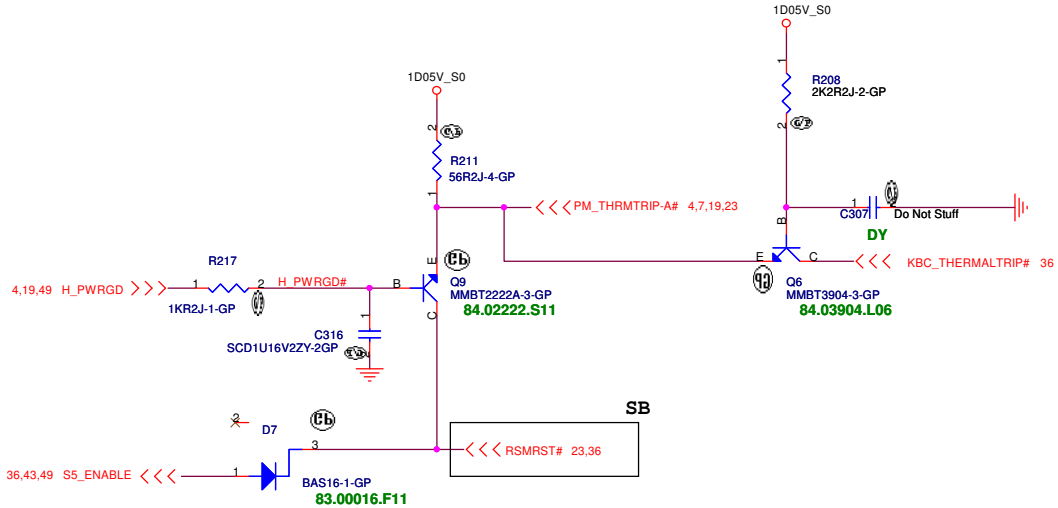
Aux Power 3D3V_AUX_S5



Run Power





UMA

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Title: **RUN POWER and 3D3V_AUX_S5**

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CPU_CORE
ISL6266A

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6266A
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

Output Power
VCC_CORE_PWR(O)

VGATE_PWRGD
VCC_CORE(Imax=38A)

TPS51125
5V/3D3V

DCBATOUT_51125
PM_SLP_S4#
ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (6A)

RT9018A
1D5V_S0

1D8V_S3
PM_SLP_S3#

VIN
EN
1D5V(O)
PGOOD

1D5V_S0 (2.5A)
CPUCORE_ON

RT9026
0D9V_S0

5V_S5
1D8V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D9V_S3 (1A)
0D9V_S3_1

GFX_CORE
ISL6263A

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT

PM_SLP_S3#
GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Input Power
VDD
VIN

Input Signal
VR_ON

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Signal
PGOOD

Output Power
VGFXCORE (O)

CPUCORE_ON
VCC_GFXCORE(5.5A)

G9131
2D5V_S0

3D3V_S0

INPUT
OUT

2D5V_S0(0.3A)

TPS51124
1D8V/1D05V

5V_S5
DCBATOUT_51124

PM_SLP_S4#
PM_SLP_S3#

CPUCORE_ON

Input Power
VDD
VCC

Input Signal
EN1
EN2

Output Signal
PGOOD1
PGOOD2

Output Power
1D8V (O)
1D05V(O)

1D8V_S3 (10A)
1D05V_S0 (15A)

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

Charger BQ24750

CHG_ON#
24750_CELLS

AD+

Input Signal
CHGEN#
CELLS

Input Power
ACN

Output Signal
ACGOOD#
SRSET

Output Power
VOUT (O)
VOUT (O)

AC_IN#
AD_IA
BT+
DCBATOUT

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Sequence Logic**

Size: B | Document Number: **Eiger** | Rev: -1

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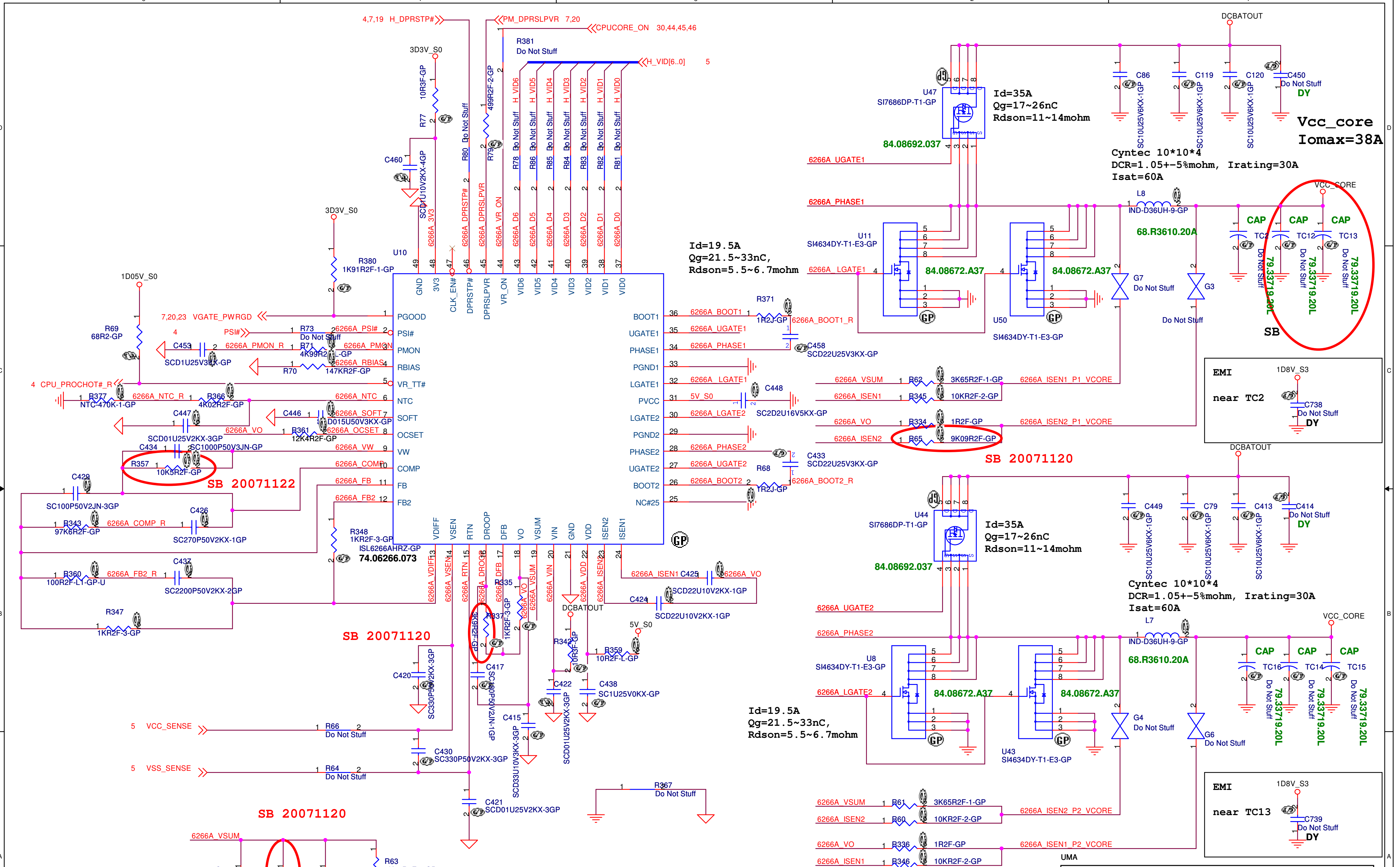

緯創資通 **Wistron Corporation**

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Title		
ISL6266A_CPU_CORE		
Size: A3	Document Number: Eiger	Rev: -1
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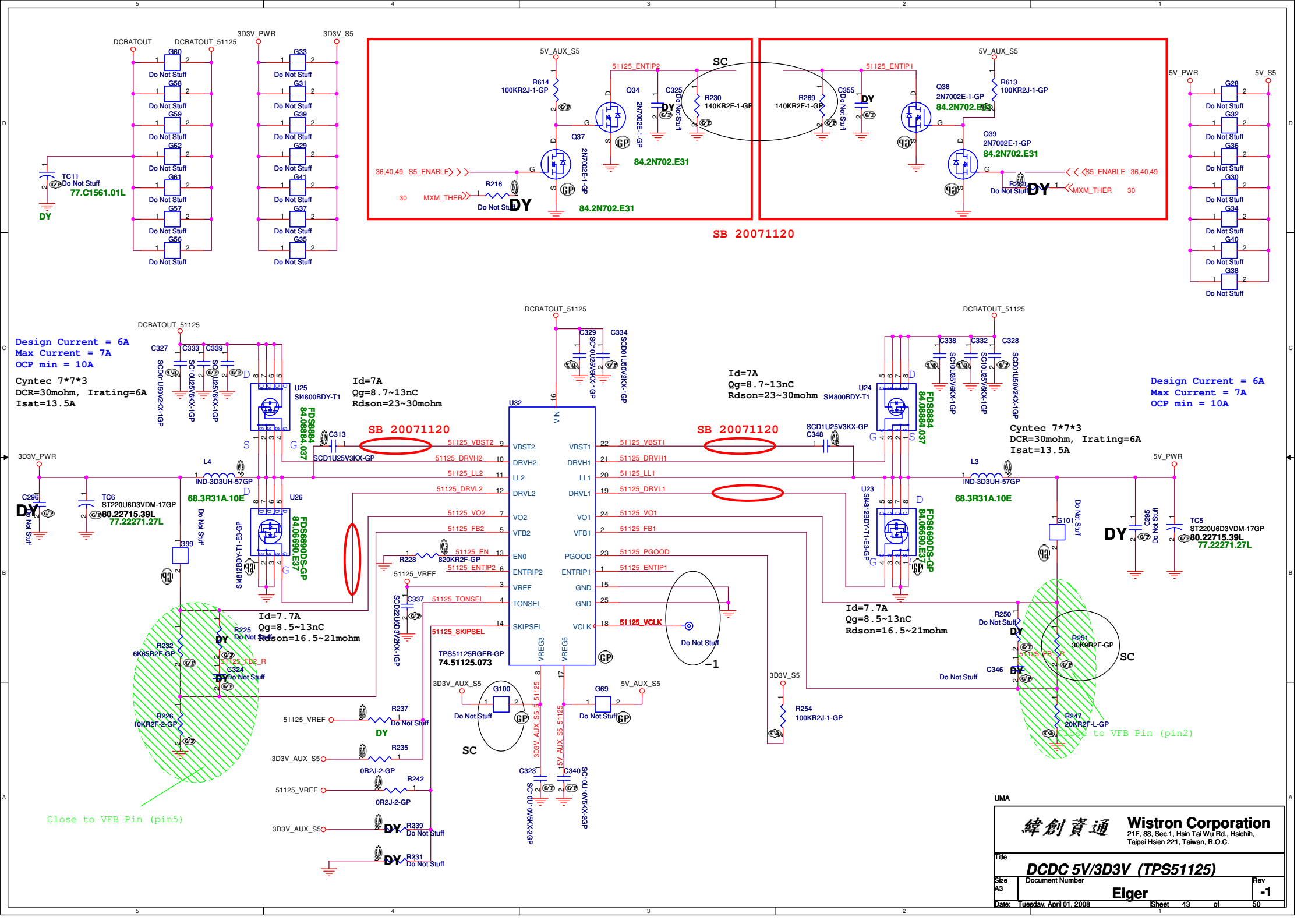
DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_AUX_S5
5V_PWR
5V_S5
SC
DY
SB 20071120
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
TPS51125RGER-GP
74.51125.073
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Eiger
Tuesday, April 01, 2008
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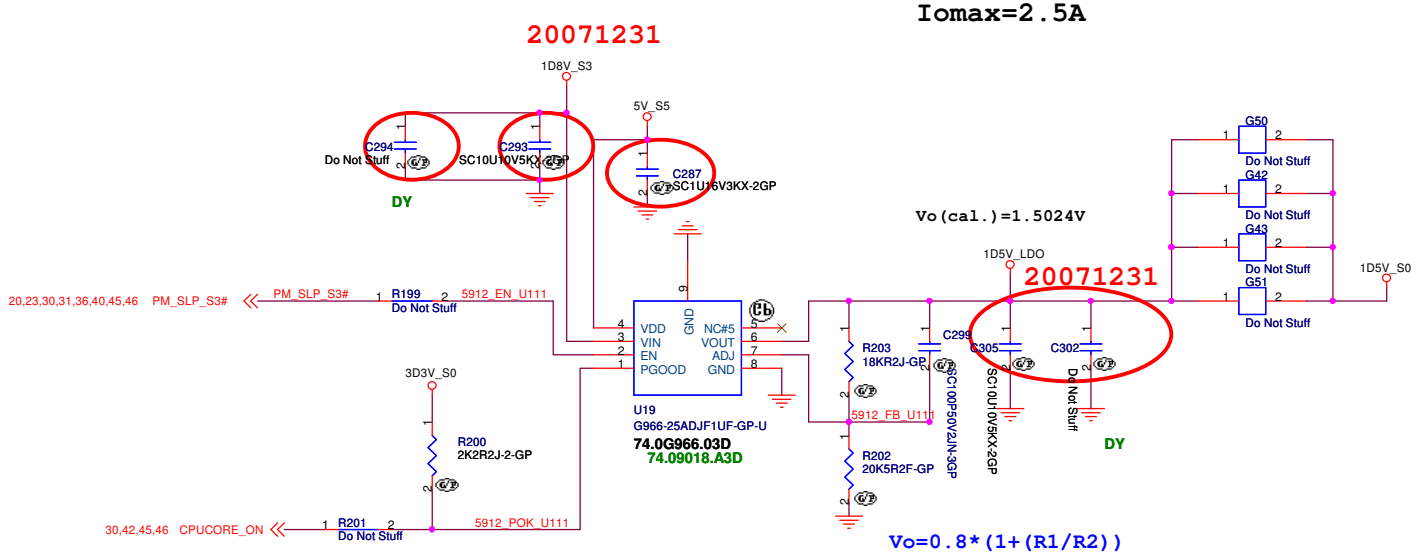
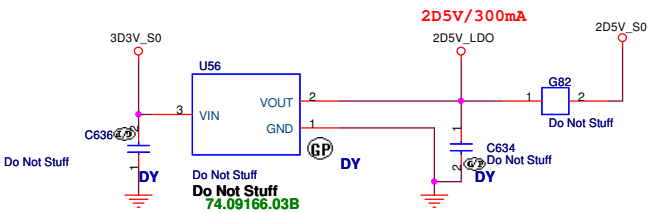
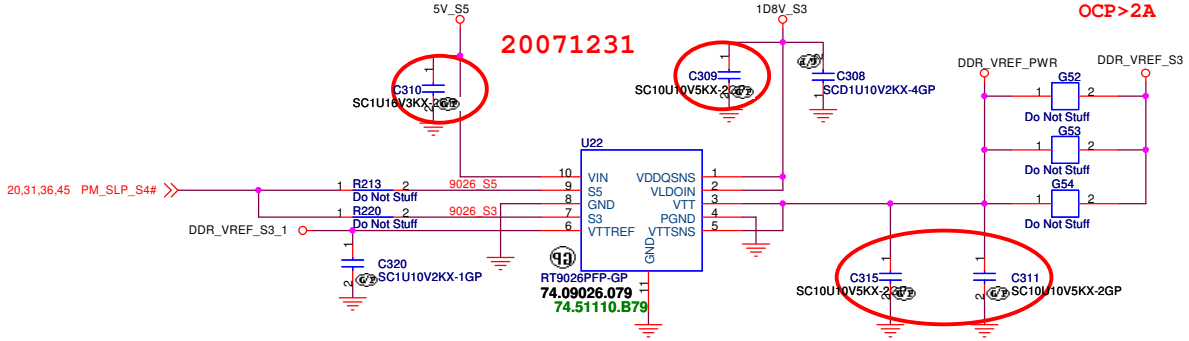
1D5V_S0
Iomax=2.5A



2D5V_S0
Iomax=0.3A



Iomax=1A
OCP>2A



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Title	1D5V & 0D9V & 2D5V	
Size A3	Document Number: Eiger	Rev: -1
Date: Tuesday, April 01, 2008	Sheet 44 of 50	

Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L

SC

DCBATOUT DCBATOUT_51124

TC23 Do Not Stuff 77.C1561.01L DY

G67 G65 G64 G63 G66 G68 Do Not Stuff

1D8V_PWR 1D8V_S3

G97 G94 G47 G48 G45 G46 G44 G95 G98 G96 G93 G49 Do Not Stuff

C655 SC10U25V6KX-1GP C336 SCD1U50V3KX-GP C343 SC10U25V6KX-1GP C331 SC2200P50V2KX-2GP

U29 FDS8880-NL-GP 84.04686.037 SI4686DY

Id=11.6A
Qg=12~16nC,
Rdson=9.6~12mohm

Cyntec 10*10*4
DCR=4.2mohm, Irating=16A
Isat=33A

L19 IND-1D5UH-34-GP 68.1R51A.10A

R261 30KR2F-GP DY C352 Do Not Stuff C304 SCD1U10V2KX-4GP TC8 ST330U2D5VDM-LGP 80.3371V.L01 77.23371.13L

U30 SI4812BDY-T1-E3-GP 84.04812.A37 84.06690.E37 FDS6690DS-GP

Id=10A
Qg=9~13nC,
Rdson=12~15mohm

R259 21K5R3F-GP

1D8V Iomax=10A
OCP>15A

5V_S5

R284 3D3R3J-L-GP C377 SC4D7U10V5KX-1GP C376 SC1U10V3KX-3GP

1D05V_PWR 1D8V_PWR 51124_VFB2 51124_VFB1

R267 R266 Do Not Stuff >>CPUCORE_ON 30,42,44,46

20,31,36,44 PM_SLP_S4# R271 Do Not Stuff DY BC6 Do Not Stuff

20,23,30,31,36,40,44,46 PM_SLP_S3# R270 Do Not Stuff DY BC5 Do Not Stuff

U35 TPS51124RGER-GPU1 74.51124.073

VFB1 VFB2 VO1 VO2 PGOOD1 PGOOD2 V5FILT V5IN EN1 EN2 GND GND PGND2 PGND1 TRIP1 TRIP2 VBST1 VBST2 TONSEL DRVH1 LL1 DRVL1 DRVH2 LL2 DRVL2

51124_PG1 51124_PG2 51124_V5FILT 51124_EN1 51124_EN2 51124_TRIP1 51124_TRIP2 51124_TONSEL

51124_DRVH1 51124_LL1 51124_DRVL1 51124_DRVH2 51124_LL2 51124_DRVL2

SB 20071120

R286 16KR3F-GP R283 11K3R2F-2-GP

C364 SCD1U16V2KX-3GP C363 SCD1U16V2KX-3GP

51124_LL1 R279 51124_LL1_1 51124_VBST1

51124_LL2 R277 51124_LL2_1 51124_VBST2

R258 DY R263 Do Not Stuff

51124_V5FILT

DCBATOUT_51124

C342 SC10U25V6KX-1GP C654 SC10U25V6KX-1GP C335 SCD1U50V3KX-GP C330 SC2200P50V2KX-2GP

U28 FDS8880-NL-GP 84.04686.037 SI4686DY-T1-E3-GP

Id=14.5A
Qg=9.2~14nC,
Rdson=11~14mohm

Cyntec 10*10*4
DCR=4.2mohm, Irating=16A
Isat=33A

L20 IND-D56UH-12-GP 68.R5610.20B

R265 11K8R2F-GP DY C351 Do Not Stuff C303 SCD1U10V2KX-4GP TC7 Do Not Stuff TC22 ST330U2D5VDM-LGP 80.3371V.L01 77.23371.13L

1D05V_PWR 1D05V_S0

G91 G90 G89 G88 G83 G86 G87 G84 G85 G92 Do Not Stuff

84.08672.A37

U27 SI4634DY-T1-E3-GP

Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm

R256 30KR2F-GP

1D05V Iomax=15A
OCP>23A

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

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Title: TPS51124_1D8V_1D05V

Size: A3 | Document Number: Eiger | Rev: -1

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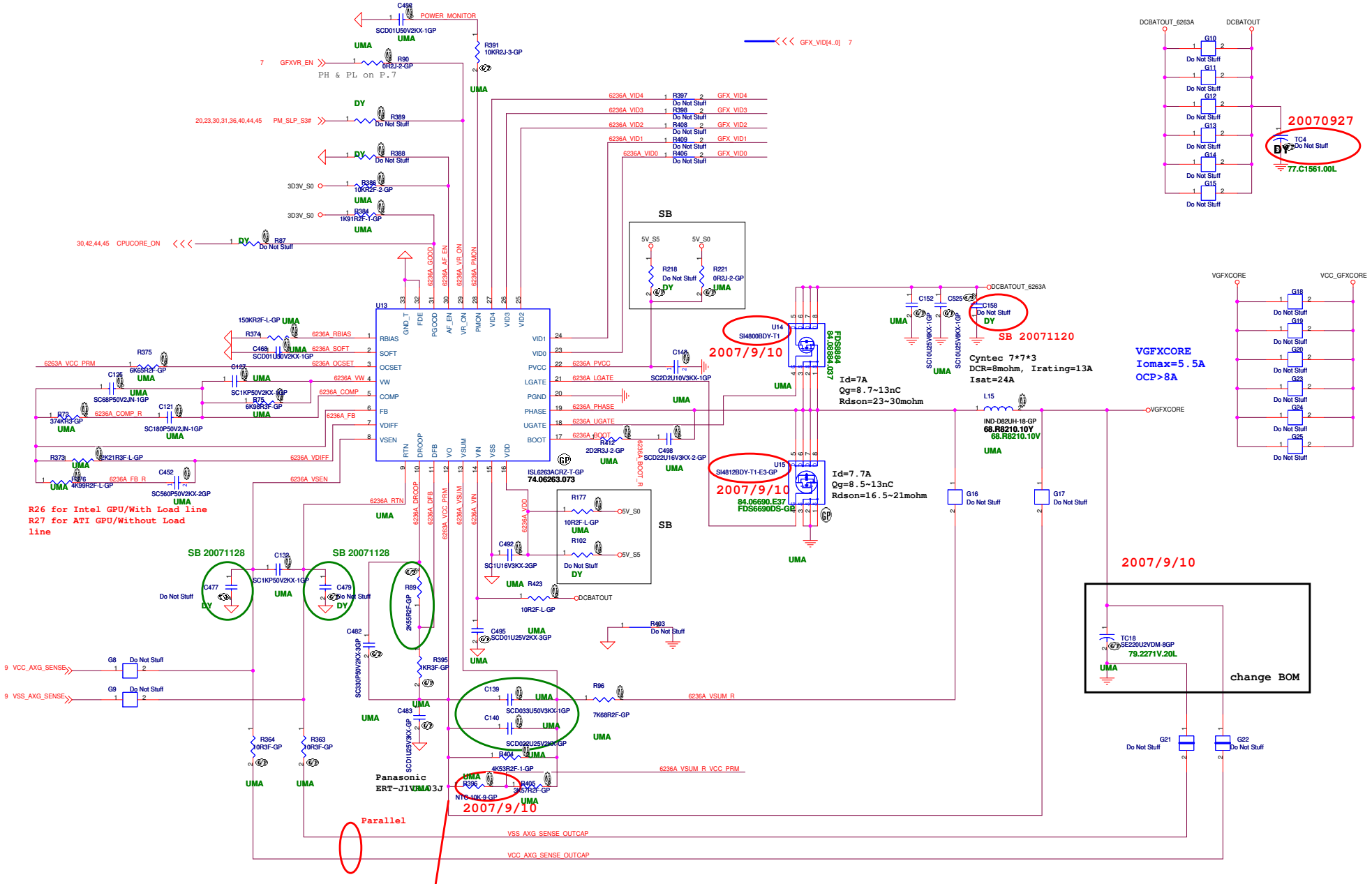

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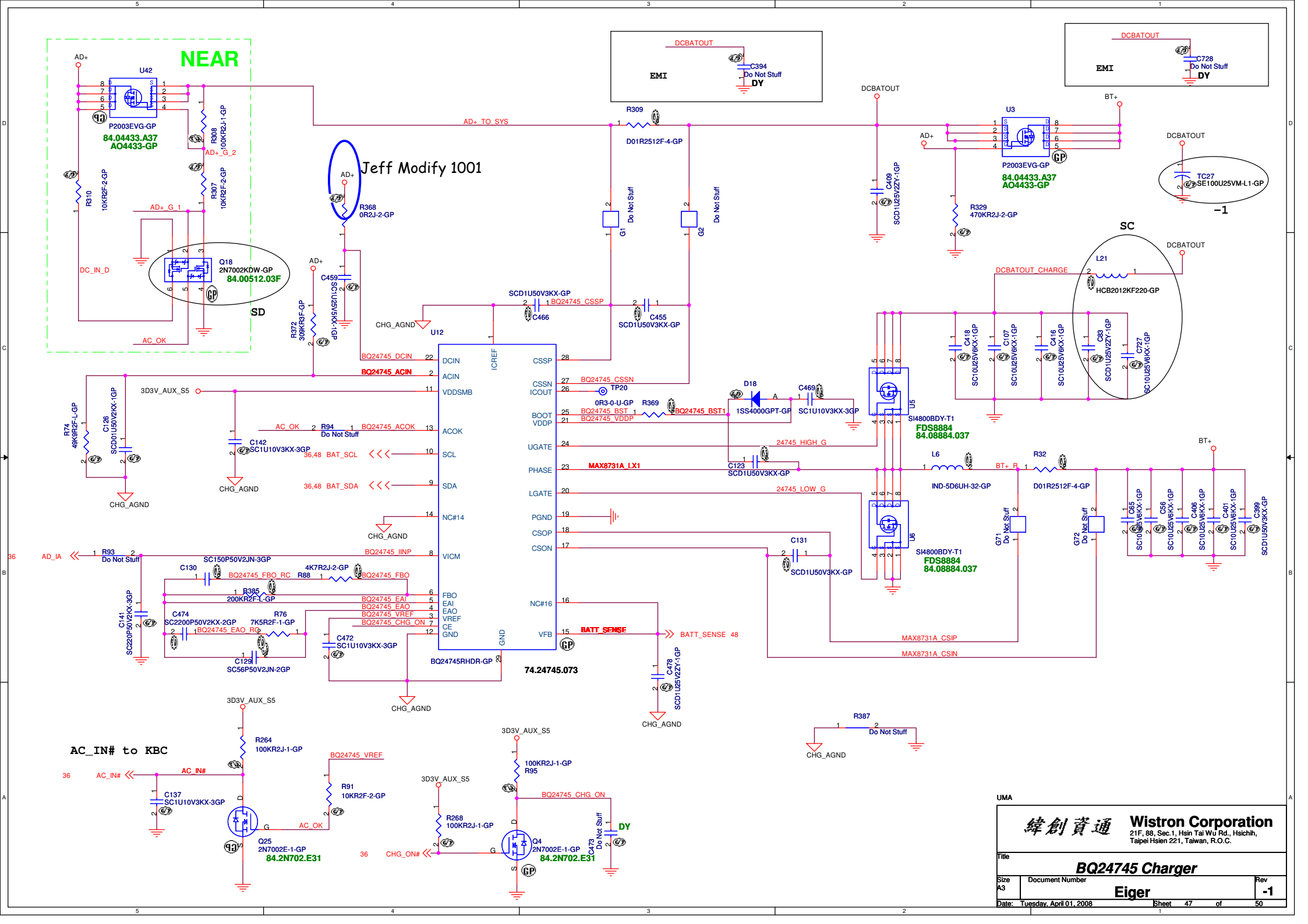
Title	ISL6263A_GFX CORE
Size: C	Document Number: Eiger
Rev: -1	
Date: Tuesday, April 01, 2008	Sheet 46 of 50



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Title: **BQ24745 Charger**

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A3	Eiger	-1

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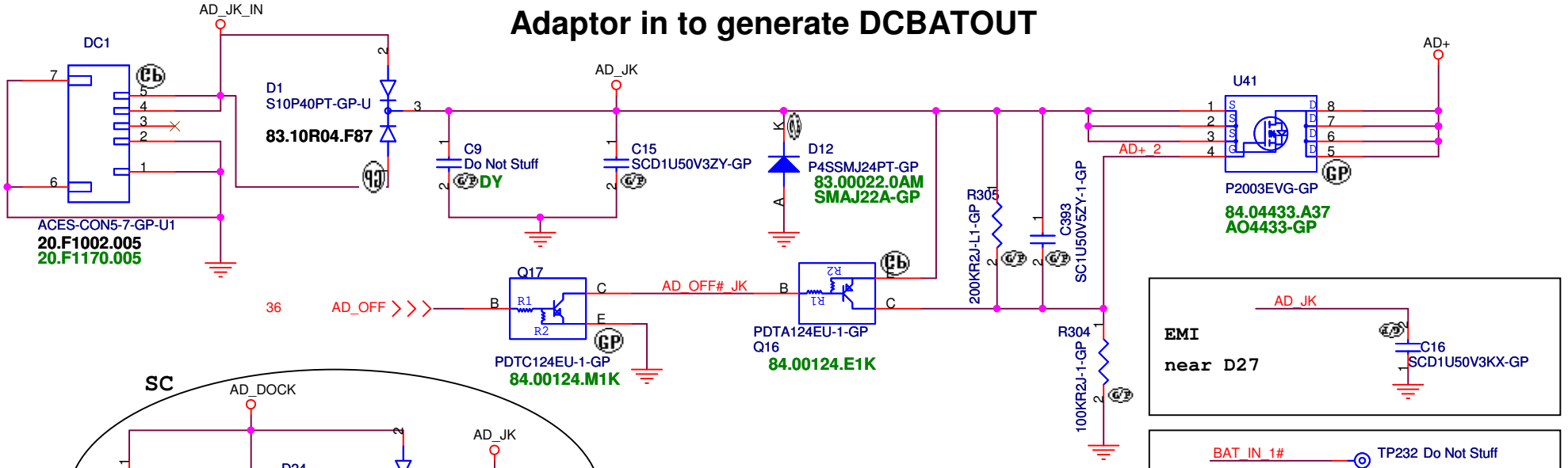
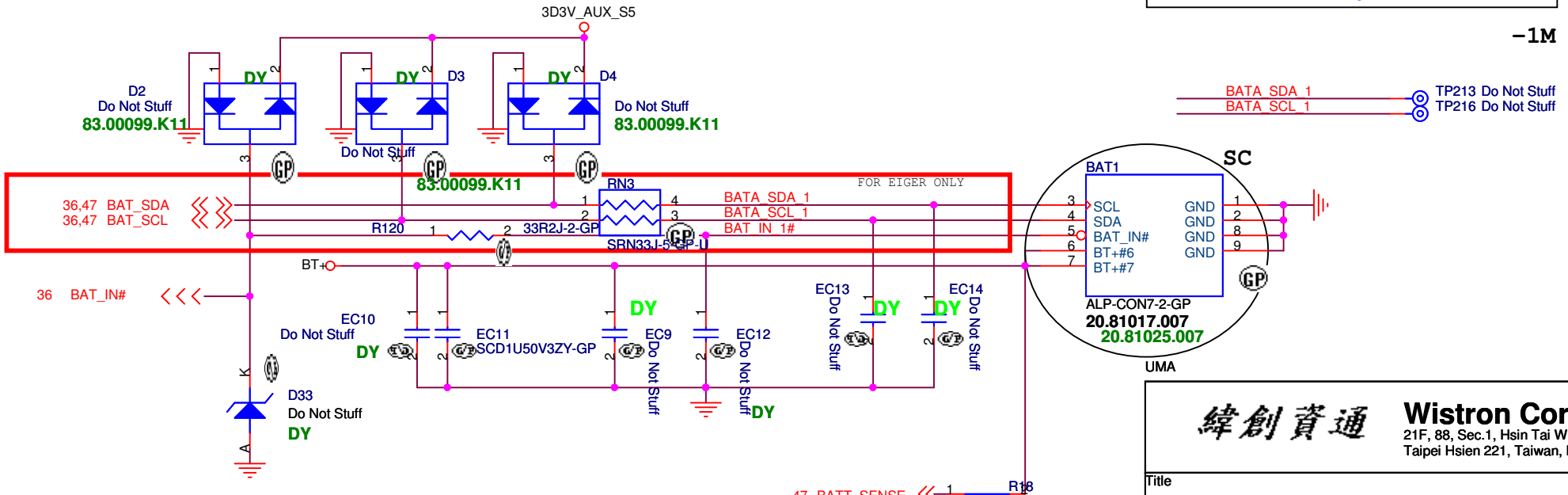
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



-1M

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Title	AD/BATT CONN	
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GND3 Do Not Stuff Do Not Stuff DY
GND4 Do Not Stuff Do Not Stuff DY
GND5 Do Not Stuff Do Not Stuff DY

GND10 Do Not Stuff Do Not Stuff DY
GND9 Do Not Stuff Do Not Stuff DY
GND8 Do Not Stuff Do Not Stuff DY

GND1 Do Not Stuff Do Not Stuff DY
GND6 Do Not Stuff Do Not Stuff DY

SB

H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 Do Not Stuff DY

GND2 Do Not Stuff Do Not Stuff DY
GND7 Do Not Stuff Do Not Stuff DY
GND13 Do Not Stuff Do Not Stuff DY

HDD

H11 H12 H14 H15 H16 H17 H18 Do Not Stuff DY

H28 H29 H30 Do Not Stuff DY
H38 Do Not Stuff

H45 H46 H47 H48 H49 H50 H51 H52 Do Not Stuff DY

EMI near H20
5V_S0
C133 Do Not Stuff DY

EMI
5V_S5
C168 Do Not Stuff DY

EMI near H56
DCBATOUT
C386 Do Not Stuff DY

EMI near H56
5V_S0
C392 Do Not Stuff DY

EMI near H9
1D8V_S3
C740 Do Not Stuff DY

H31 HOLE H33 HOLE H34 HOLE
MS_34.4Z532.001 34.42Y01.011
MS_34.4Z532.001 34.42Y01.011
MS_34.4Z532.001 34.42Y01.011
CPU

H36 HOLE H37 HOLE
MS_34.4Z532.001 34.42Y01.011
MS_34.4Z532.001 34.42Y01.011
MDC

H39 HOLE H40 Do Not Stuff H41 Do Not Stuff H42 HOLE
MS_34.4Z531.001 34.4G502.001
DY_MS_34.4Z531.001 34.4G502.001
DY_MS_34.4Z531.001 34.4G502.001
MS_34.4Z531.001 34.4G502.001
MINIC1

H43 Do Not Stuff H44 HOLE
DY_MS_34.4Z531.001 34.4G502.001
MS_34.4Z531.001 34.4G502.001
MINIC2

H32 HOLE H35 HOLE
MS_34.4Z532.001 34.42Y01.011
MS_34.4Z532.001 34.42Y01.011
NB

GND11 Do Not Stuff Do Not Stuff DIS
GND12 Do Not Stuff Do Not Stuff DIS
GND14 Do Not Stuff Do Not Stuff DIS
GND15 Do Not Stuff Do Not Stuff DIS

H26 Do Not Stuff H27 Do Not Stuff
DIS_34.4Z533.001 34.4F405.001
DIS_34.4Z533.001 34.4F405.001
MXM

SB

Check test point

3D3V_S0	TP92 Do Not Stuff
3D3V_AUX_S5	TP223 Do Not Stuff
3D3V_S5	TP173 Do Not Stuff
5V_S5	TP224 Do Not Stuff
20,36 PM_PWRBTN#	TP222 Do Not Stuff
4,19,40 H_PWRGD	TP221 Do Not Stuff
36,40,43 S5_ENABLE	TP166 Do Not Stuff
4,6 H_CPURST#	TP133 Do Not Stuff

Test Point放在Dimm Door打開可量測處

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Title: EMI/Spring/Boss
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Eiger Schematic EC Tracking Record LAB Dec.10 , 2007
EC #/ Page / Description / Part Affected

EC SB01/07/ DY R175 (fix can not boot)
EC SB02/07/ change R184 (intel spec change)
EC SB03/10/ mount L2,C221 (intel spec change)
EC SB04/15/ modify LCD2 pin define(add dig-MIC,backlight)
EC SB05/17/ DOCK_IN_CRT# logic change
EC SB06/18/ change HDMI level shift IC setting
EC SB07/19/ change R606(meet HDA SPEC)
EC SB08/23/ change PURE_HW_SHUTDOWN# ,PM_THRMTRIP-A# schematic
EC SB09/26/ change C648 ,deltree poly switch
EC SB10/27/ change R555,R557,R559 (vendor request)
EC SB11/30/ change R612 (vendor request)
EC SB12/34/ add C711 (fix audio noise)
EC SB13/36/ add SPI_WP# (BIOS wirte protect)
EC SB14/38/ add CRT_DEC# (Acer change spec)
EC SB15/38/ add dock/no dock option schematic
EC SB16/40/ D7(power sequencing)
EC SC01/16/ R595,R596,R597,R598(LED)
EC SC02/18/ HEMI level shift & switch solution change
EC SC03/19/ ESATA function
EC SC04/23/ H/W Thermal shut down,power off Sequence
EC SC05/24/ Add ESATA circuit
EC SC06/30/ Add R116(MXM aczrst# Acer request)
EC SC07/33/ Add audio gound
EC SC08/34/ Change audio AMP circuit
EC SC09/38/ Add RC circuit to reduce audio noise
EC SC10/40/ 3D3V_AUX_S5 from U32 internal LDO
EC SC11/43/ Change 5V to 5.1V
EC SC12/47/ Isolate Change IC switching high side MOS input power
EC SC13/48/ Isolate AD19V in and Dock19V in

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