

[illegible]

CLK-GEN
ICS 952801

Page 2

HOST 200MHz
ZCLK 133MHz
AGP 66MHz
PCI 33MHz
USB 48MHz
REF 14.318MHz

3V/5V

Page 22

3V_ALWAYS
5VPCU
3V_S5
1.8V_S5
3VSUS
5VSUS
+3V
+5V
15V

2.5V/1.25V

Page 23

2.5VSUS
1.25VREF
+2.5V
DDR_VTT

**1.2V/1.5V
1.8V**

Page 24

+1.2V_HT
+1.5V
+1.8V

CPU CORE

Page 25

VCC_CORE

**BATTERY
CHARGER**

Page 26

DDR SO-DIMM

Page 5

DDR 333

CPU
AMD Athlon64
SMT uPGA754

Page 3,4

HyperTransport
16x16
1600MT/s

Thermal
Thermal sensor & Fan

ZL5
Block Diagram

NB
SIS M760GX
(698 PIN BGA)

Page 6,7,8

MuTIOL(1GB/s)

HDD
Primary Master

Page 19

ATA 66/100

ODD
Secondary Master

Page 19

ATA 66/100

USB
3x connector

Page 15

USB 2.0

MINI USB
(BLUETOOTH)

Page 15

SB
SIS 963L
(371 PIN BGA)

Page 11,12,13

Int. Keyboard
87-Key

Page 21

Touch Pad
6-Button

Page 21

EC
NS PC97551

Page 20

LPC

PCI 2.2 133MB/s (33MHZ)

CardBus
TI PCI1410

Page 14

LAN PHY
RTL8201CP

Page 16

MII

AC'97 2.1

AC97 Codec
ALC203

Page 17

BIOS

Page 20

REQ0#, GNT0#
INTB#, INTC# IDSEL : AD22

Mini PCI
WLAN 802.11A/G

Page 15

Antenna

Transformer

Page 16

MDC1.5
56K MODEM

Page 17

RJ-45

Page 16

RJ-11

Page 16

MIC-In Jack

Line-In Jack

AMP
MAX9755

Page 18

HP-Out Jack

Int. Speaker

CRT
1x D-SUB 15-Pin

Page 10

LCD
15" XGA/WXGA

Page 10

RGB

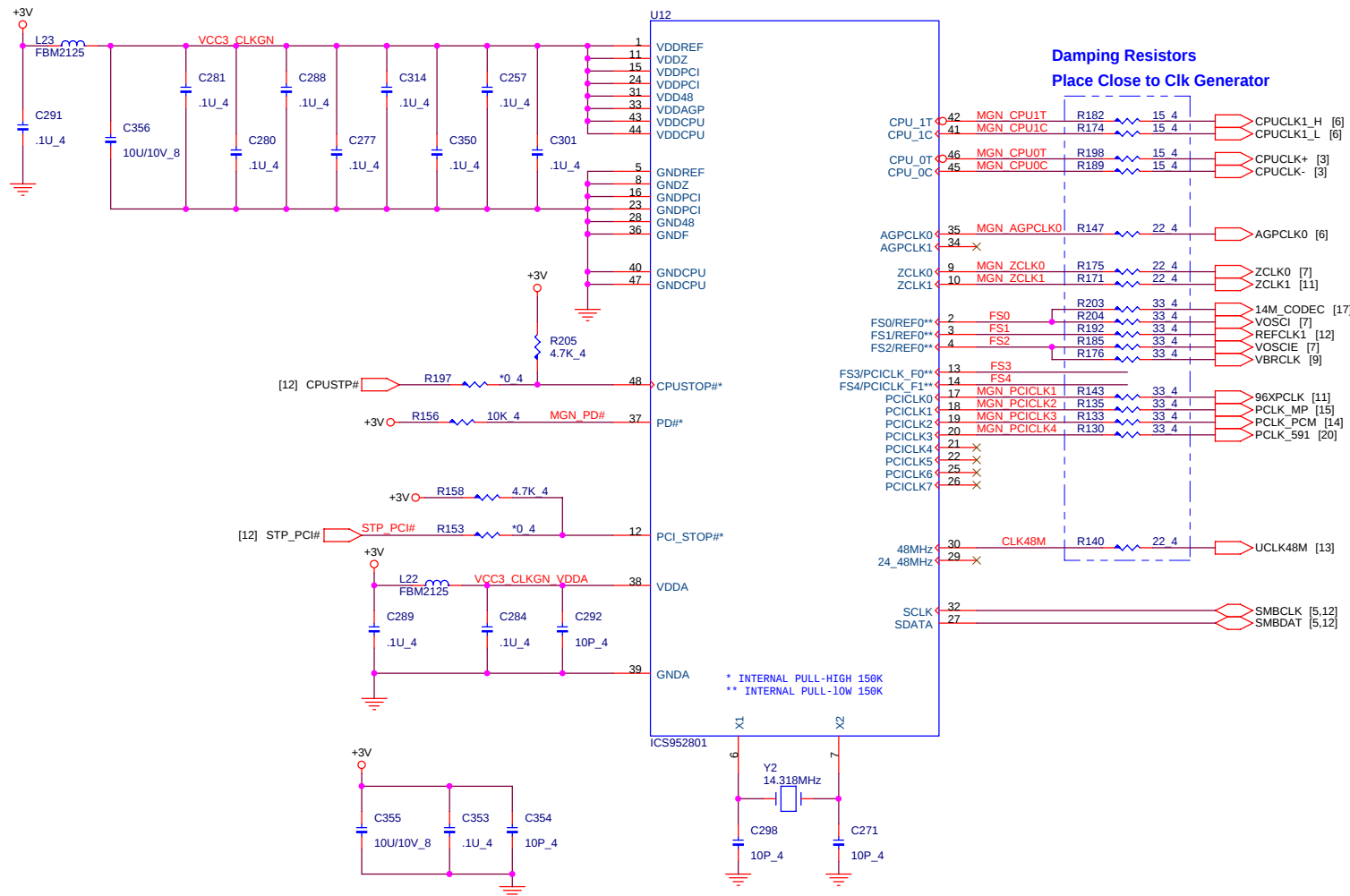
INTA#

DVO

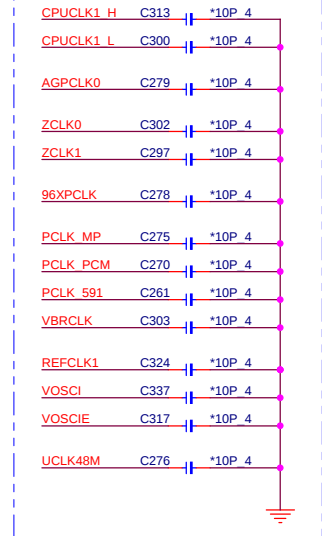
LVDS



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By-Pass Capacitors Place Close to Clock Generator



Frequency Selection



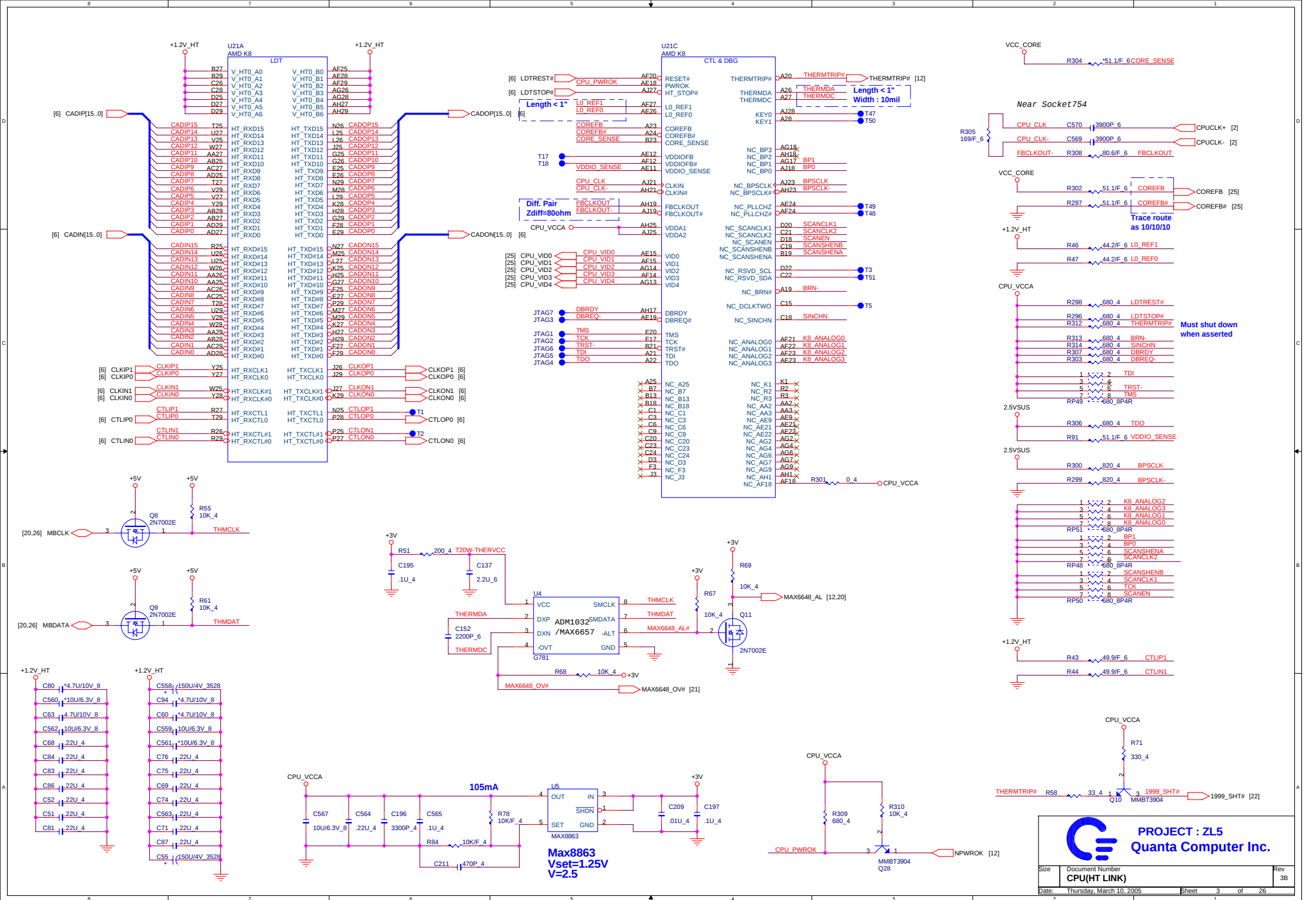
CLK Table for SiS M760 (Not For ICS ICS-952801)

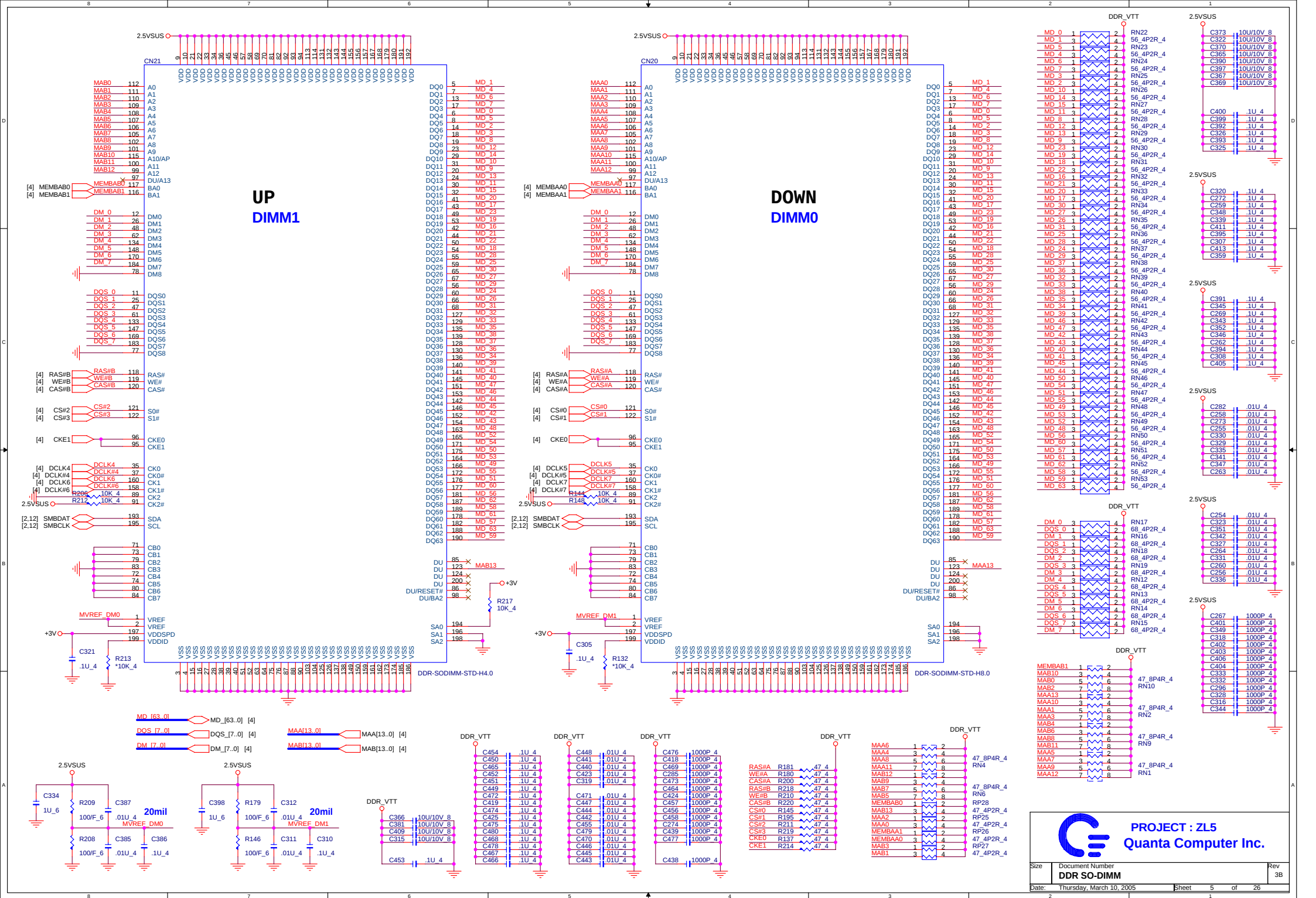
SiS 755/M760 CLOCK									
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)	VCO (MHz)
0	0	0	0	0	200	66.66	66.66	33.33	400
0	0	0	0	1	200	100	66.66	33.33	400
0	0	0	1	0	200	133.33	66.66	33.33	400
0	0	0	1	1	200	166.66	66.66	33.33	1000
0	0	1	0	0	233	66.66	66.66	33.33	466
0	0	1	0	1	233	93.2	66.66	33.33	466
0	0	1	1	0	233	133.28	66.66	33.33	933
0	0	1	1	1	233	139.8	69.9	33.33	699
0	1	0	0	0	266	66.66	66.66	33.33	266
0	1	0	0	1	266	106.4	66.5	33.33	532
0	1	0	1	0	266	133	66.5	33.33	532
0	1	0	1	1	266	159.6	66.5	33.33	798
0	1	1	0	0	200	133	50	33.33	400
0	1	1	0	1	200	114	66.66	33.33	800
0	1	1	1	0	200	142	66.66	33.33	1000
0	1	1	1	1	200	160	66.66	33.33	800

SiS 755/M760 CLOCK									
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)	VCO (MHz)
1	0	0	0	0	180	135	67.5	33.75	
1	0	0	0	1	185	132.14	66.07	33.04	
1	0	0	1	0	190	135.71	67.08	33.93	
1	0	0	1	1	195	130	65	32.5	
1	0	1	0	0	205	136.66	68.33	34.17	
1	0	1	0	1	210	140	70	35	
1	0	1	1	0	215	129	64.5	32.25	
1	0	1	1	1	220	132	66	33	
1	1	0	0	0	66.66	66.66	66.66	33.33	
1	1	0	0	1	66.66	100	66.66	33.33	
1	1	0	1	0	100	100	66.66	33.33	
1	1	0	1	1	100	133.33	66.66	33.33	
1	1	1	0	0	133	100	66.66	33.33	
1	1	1	0	1	133	133.33	66.66	33.33	
1	1	1	1	0	166	100	66.66	33.33	
1	1	1	1	1	166	133.33	66.66	33.33	



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[3] CADIP[15..0] CADIP[15..0]
[3] CADIN[15..0] CADIN[15..0]
[3] CADOP[15..0] CADOP[15..0]
[3] CADON[15..0] CADON[15..0]

CADIP15
CADIP14
CADIP13
CADIP12
CADIP11
CADIP10
CADIP9
CADIP8
CADIP7
CADIP6
CADIP5
CADIP4
CADIP3
CADIP2
CADIP1
CADIP0
CADIN15
CADIN14
CADIN13
CADIN12
CADIN11
CADIN10
CADIN9
CADIN8
CADIN7
CADIN6
CADIN5
CADIN4
CADIN3
CADIN2
CADIN1
CADIN0
CADOP15
CADOP14
CADOP13
CADOP12
CADOP11
CADOP10
CADOP9
CADOP8
CADOP7
CADOP6
CADOP5
CADOP4
CADOP3
CADOP2
CADOP1
CADOP0
CADON15
CADON14
CADON13
CADON12
CADON11
CADON10
CADON9
CADON8
CADON7
CADON6
CADON5
CADON4
CADON3
CADON2
CADON1
CADON0

LRCAD_N0
LRCAD_P0
LRCAD_N1
LRCAD_P1
LRCAD_N2
LRCAD_P2
LRCAD_N3
LRCAD_P3
LRCAD_N4
LRCAD_P4
LRCAD_N5
LRCAD_P5
LRCAD_N6
LRCAD_P6
LRCAD_N7
LRCAD_P7
LRCAD_N8
LRCAD_P8
LRCAD_N9
LRCAD_P9
LRCAD_N10
LRCAD_P10
LRCAD_N11
LRCAD_P11
LRCAD_N12
LRCAD_P12
LRCAD_N13
LRCAD_P13
LRCAD_N14
LRCAD_P14
LRCAD_N15
LRCAD_P15
LRCOMP
C28

LRCLK_N1
LRCLK_P1
LRCLK_N0
LRCLK_P0
LRCTLN
LRCTLP
HTCLKN
HTCLKP
HTAVDD
HTAVSS
HTPHYAVDD
HTPHYAVSS
LDTSTOP#
LDTREQ#
LDTREST#

LDTSTOP#
LDTREQ#
LDTREST#

SBT7
SBT6
SBT5
SBT4
SBT3
SBT2
SBT1
SBT0
ST0
ST1
ST2
AAD0
AAD1
AAD2
AAD3
AAD4
AAD5
AAD6
AAD7
AAD8
AAD9
AAD10
AAD11
AAD12
AAD13
AAD14
AAD15
AAD16
AAD17
AAD18
AAD19
AAD20
AAD21
AAD22
AAD23
AAD24
AAD25
AAD26
AAD27
AAD28
AAD29
AAD30
AAD31

HOST_TX

HOST_RX

M760-1

LVDS/AGP

[9] VBCLK R80 10 4

+1.2V_HT R49 75 4
R50 75 4
CPUCLK1_L C136 3900P 6 755CLK-
CPUCLK1_H C122 3900P 6 755CLK+
R53 169/F_6

AC/BE#3
AC/BE#2
AC/BE#1
AC/BE#0
AREQ#
AGNT#
AFRAME#
AIRDY#
ATRDY#
ADEVSEL#
ASERR#
ASTOP#
APAR
RBF#
WBF#
GC_DET#
PIPE#ADB#
ADBIL
SB_STB
SB_STB#
AD_STB0
AD_STB0#
AD_STB1
AD_STB1#
AGPCLK
AGPCOMP_P
AGPCOMP_N
A1XAVDD
A1XAVSS
A4XAVDD
A4XAVSS
AGPREF
V1
AGPVSSREF
V4

+1.8V
R315 4.7K_4
VBCLK [9]

GCDET-
R319 10 4 VAGCLK
R85 10 4 VBCLK

AGPCLK0 [2]

20mil
+1.8V
R318 124/F_6
R323 124/F_6
R320 *33_4
C606 *22P_4
Near 200mil

[9] VAD[11..0]
[9] VAGCLK
[9] VAHSYNC
[9] VAVSYNC
[9] VADE
[9] VBD[11..0]
[9] VBCLK
[9] VBHSYNC
[9] VBVSYSN
[9] VBDE
[9] VBCTL1
[9] VBCTL0

A1XAVDD R62 0 6
C230 .1U_4
C181 .01U_4
A1XAVSS
A4XAVDD L48 WB201209B121QNT03
C597 .1U_4
C601 .01U_4
C59 10U/10V_8
A4XAVSS
HTAVDD L16 WB201209B121QNT03
C145 .1U_4
C153 .01U_4
C56 10U/10V_8
HTAVSS
HTPHYAVDD L40 WB201209B121QNT03
C566 .1U_4
C568 .01U_4
C47 10U/10V_8
HTPHYAVSS

Place close to chip
+1.8V
AGPRCOMP R90 49.9/F 6
CPU_VCCA
LDTREQ# R52 1K 4
+1.2V_HT
LRCOMP R29 100/F 6
LTCOMP R30 49.9/F 6
LTCOMP R36 49.9/F 6
AGPRCOMP R322 43.2/F 6
VAGCLK C604 *10P 4
VBCLK C227 *10P 4
MVCLK C212 *10P 4

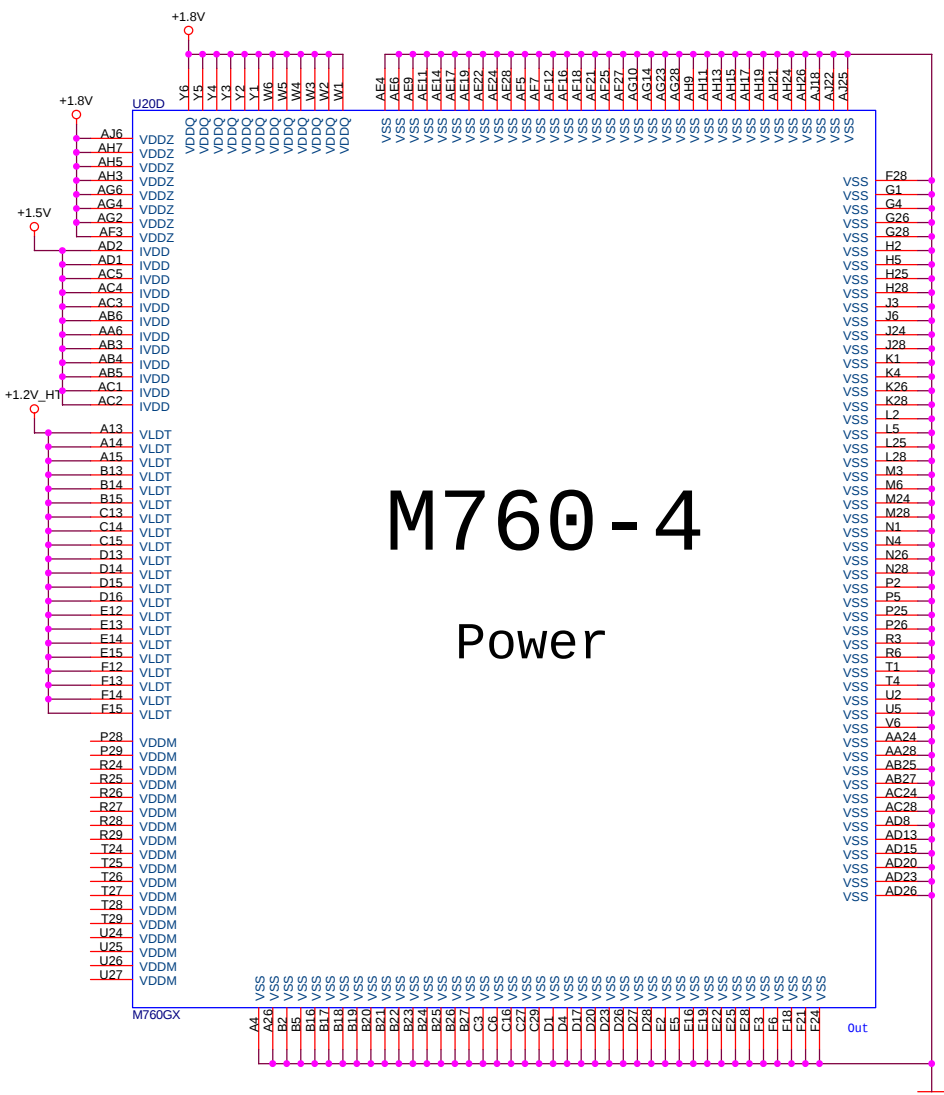


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If Support SiS M760LV IVDD=1.5V

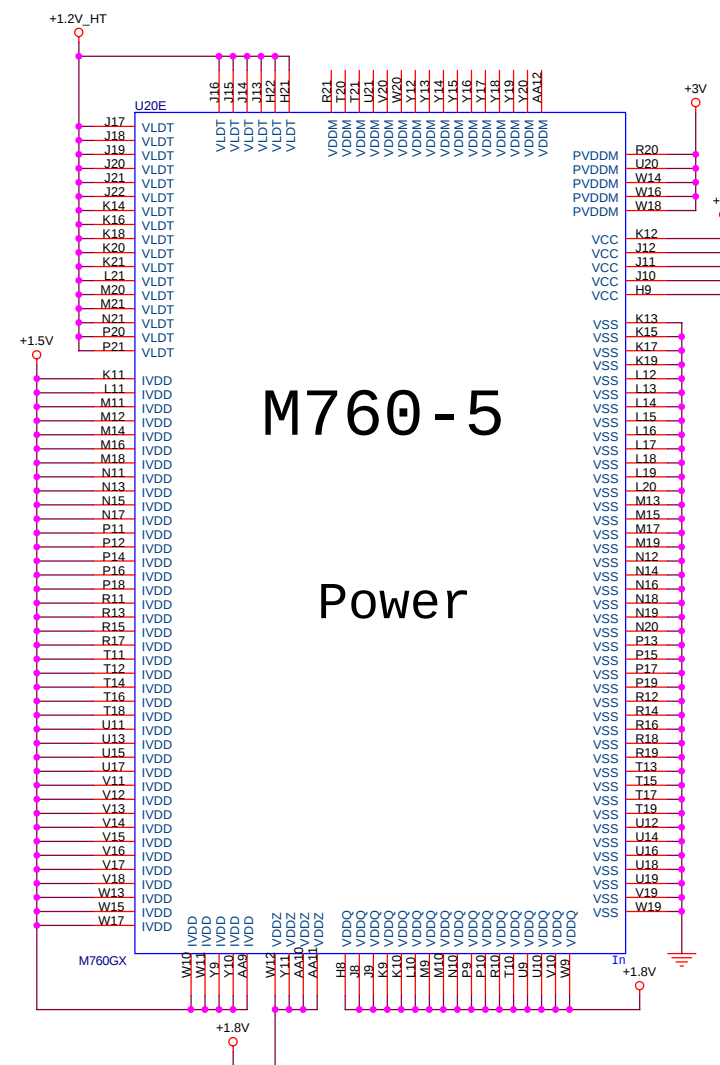
M760-4

Power

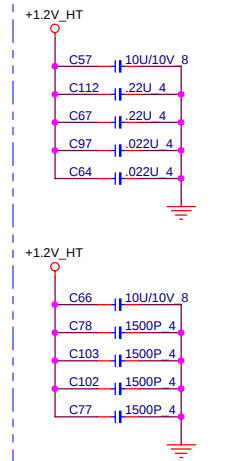


M760-5

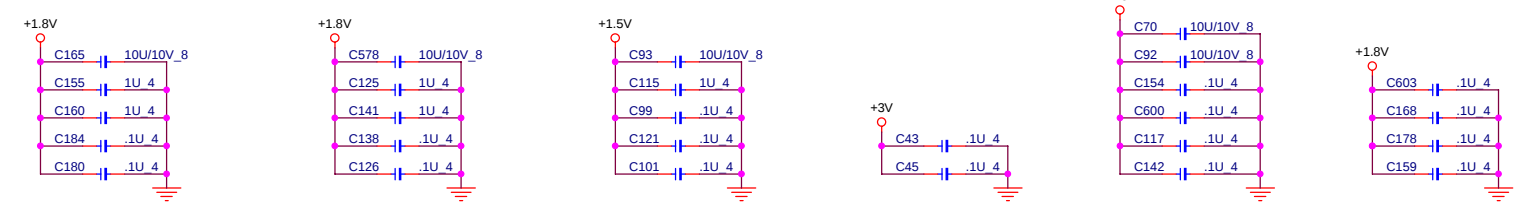
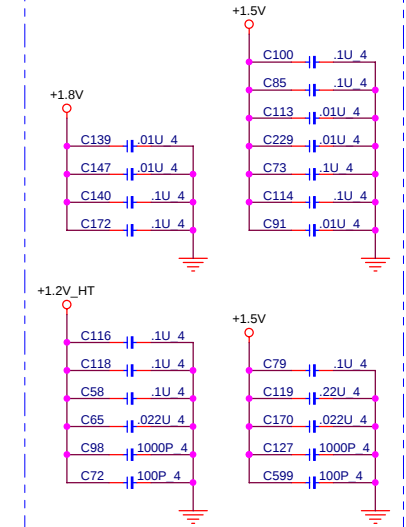
Power



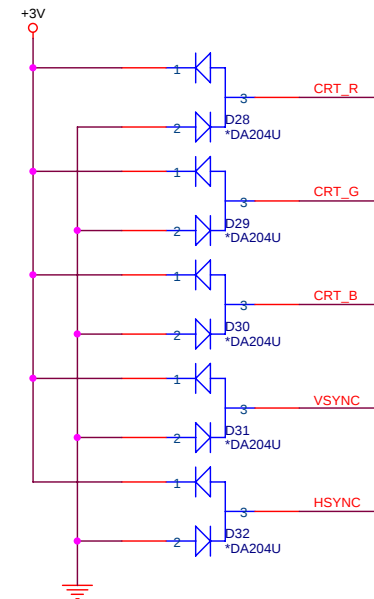
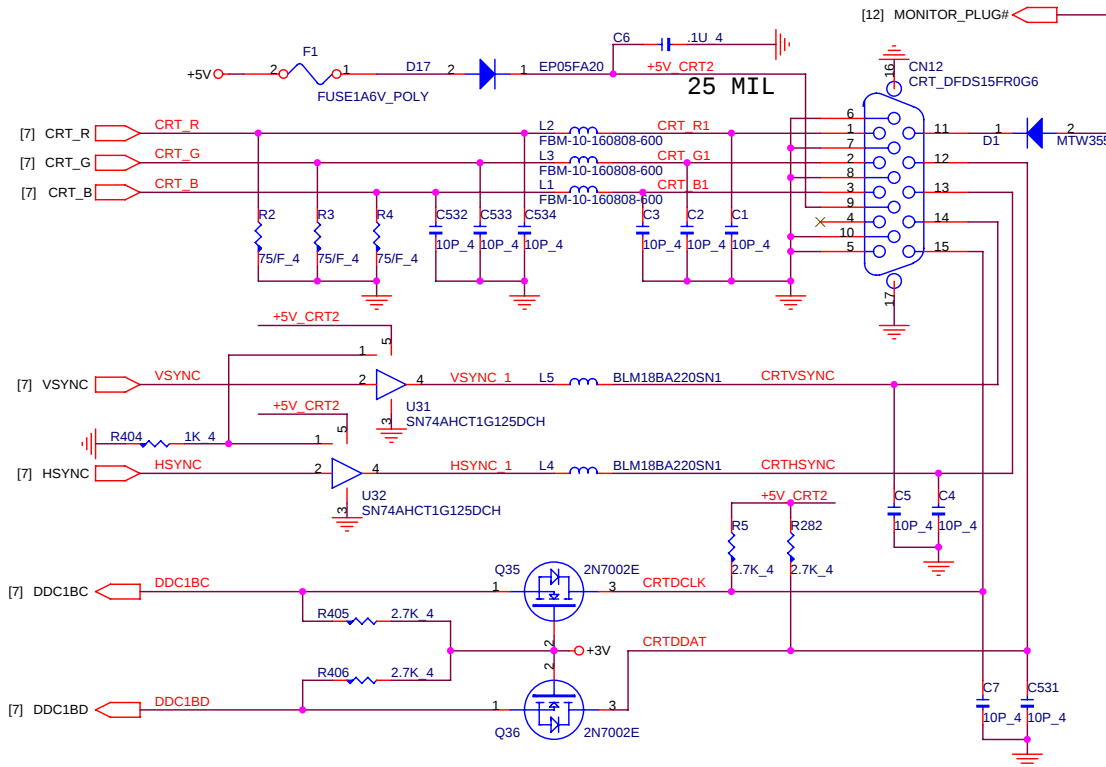
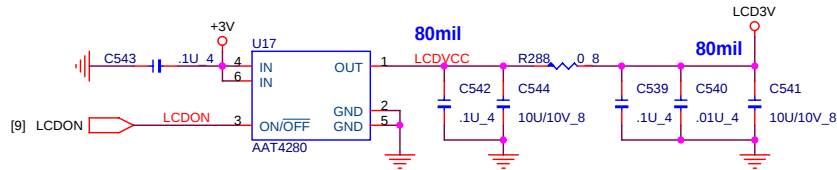
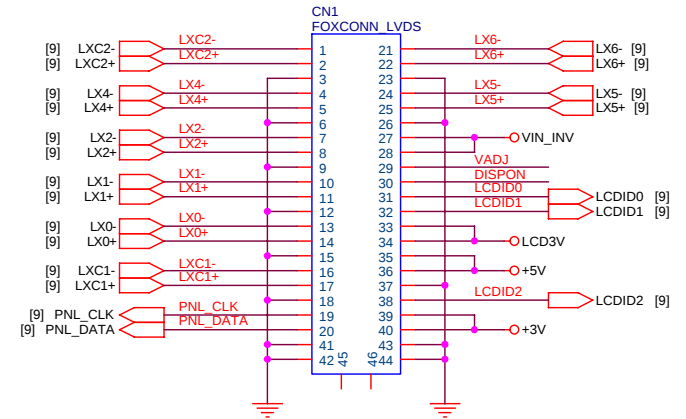
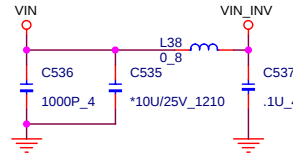
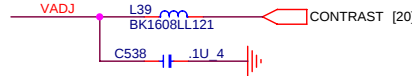
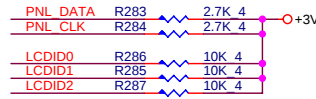
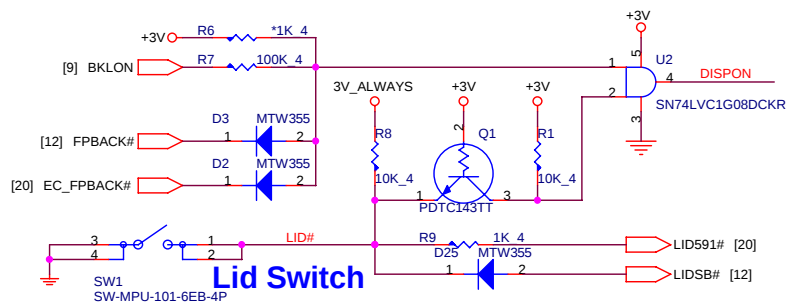
LAYOUT: Place HT bypass caps on topside near connected Lokar HT link.

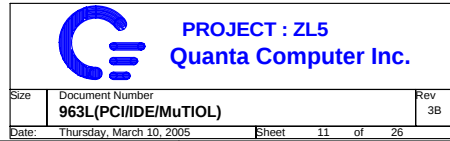


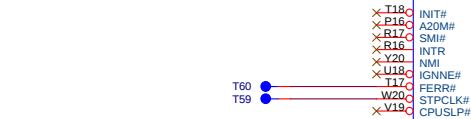
Place these capacitors under 760 solder side.



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CPU_S

APIC

LPC

RTC

963L-2

GPIO

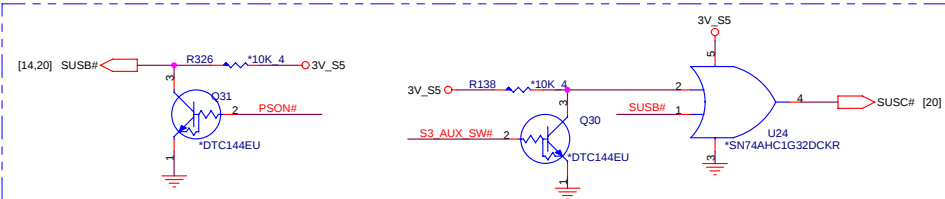
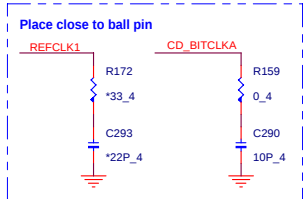
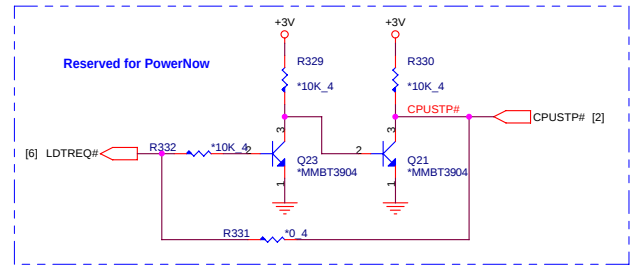
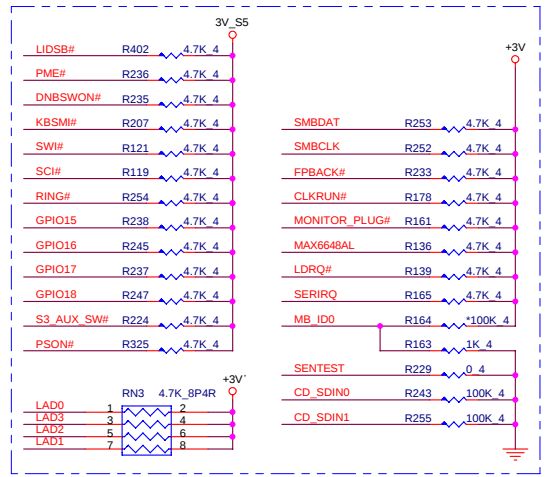
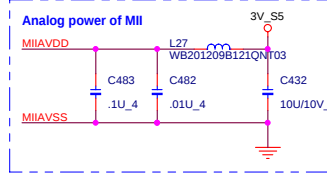
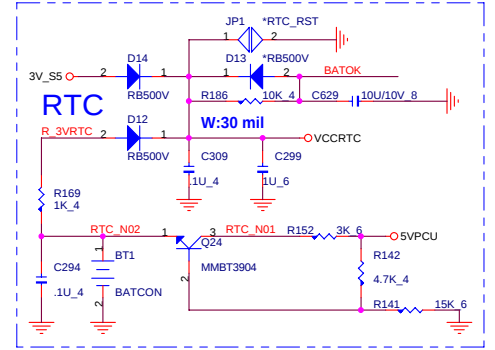
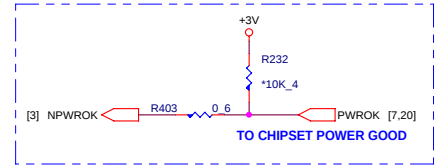
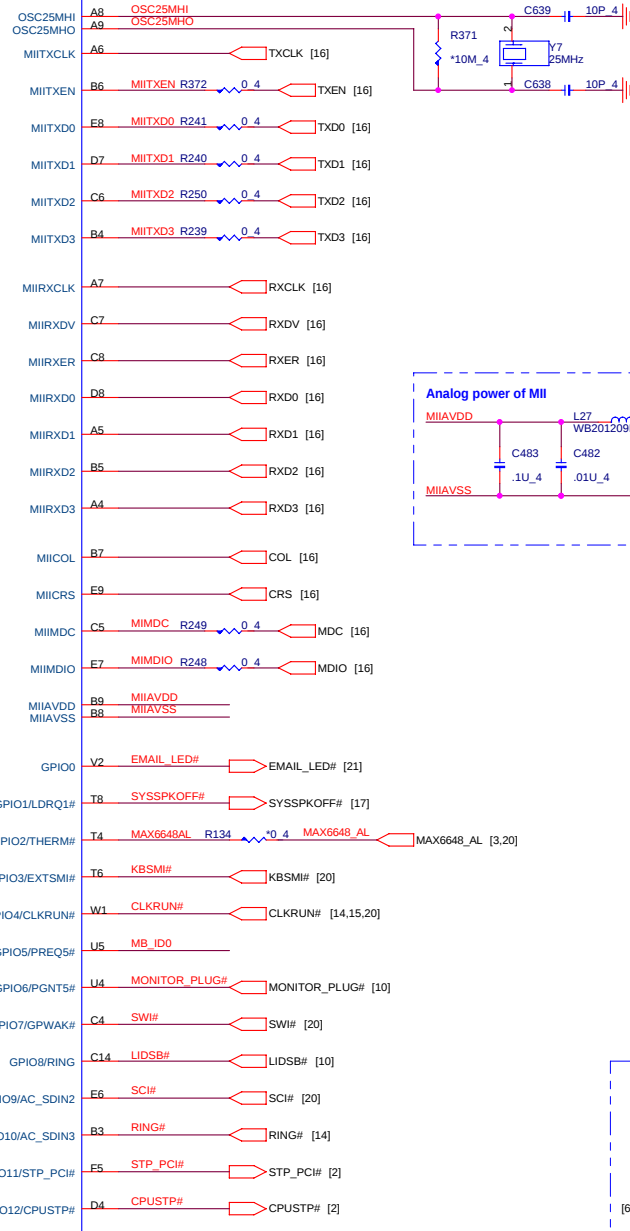
AC97

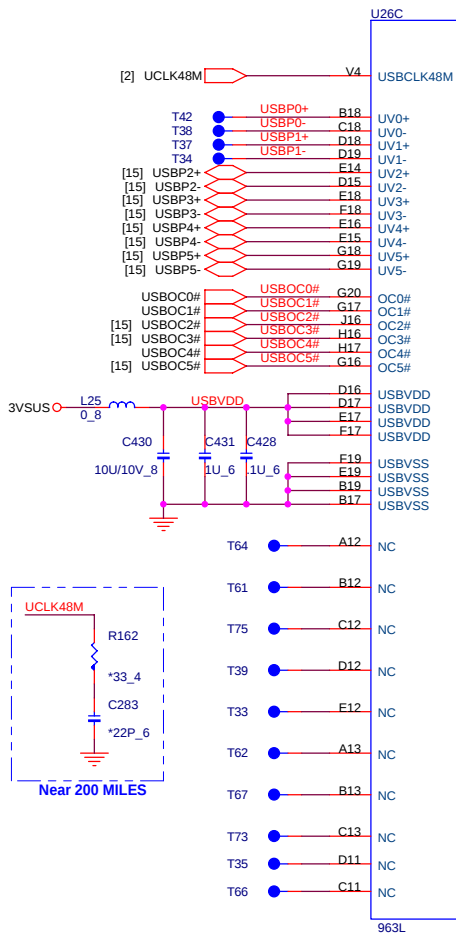
ACPI
/others

GPIO

KBC
SPEEDSTEP

MII

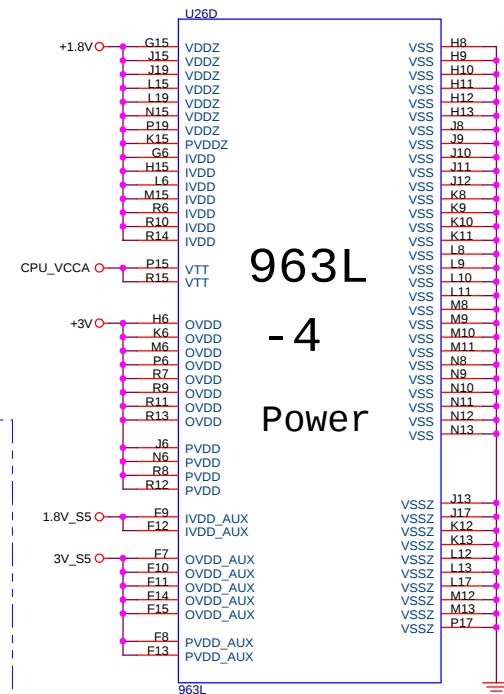
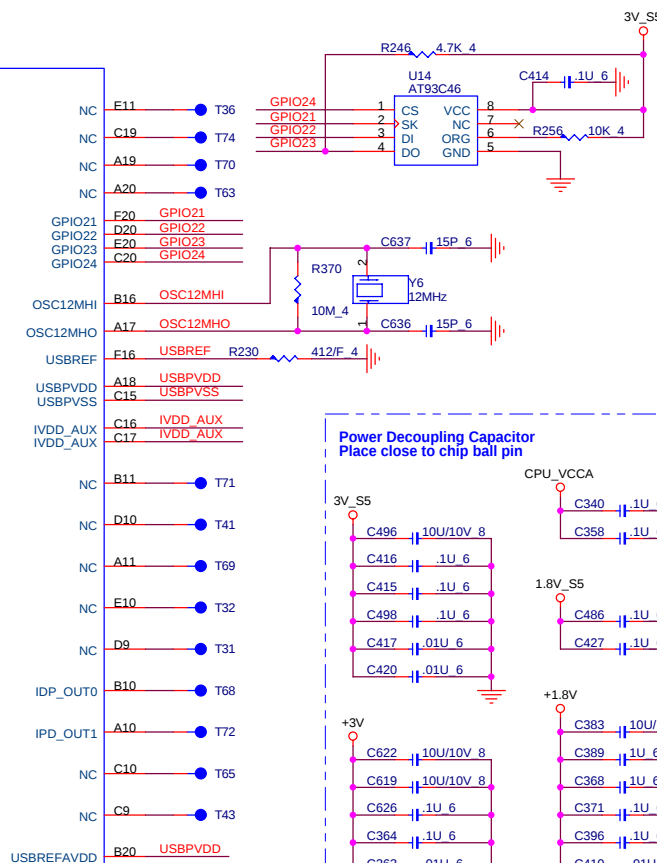
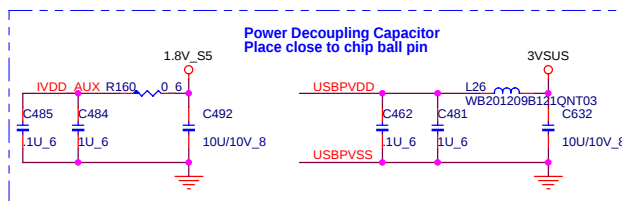
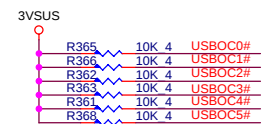




OTHERS

USB

963L - 3



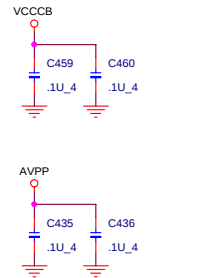
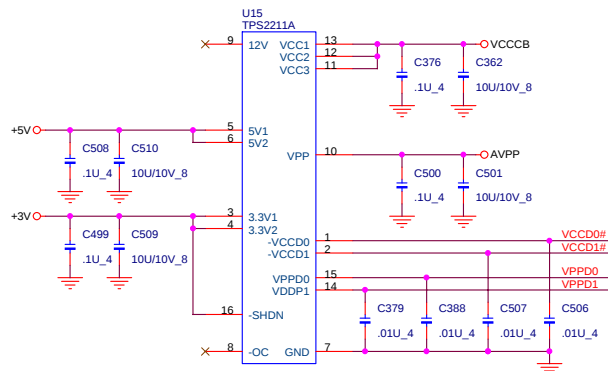
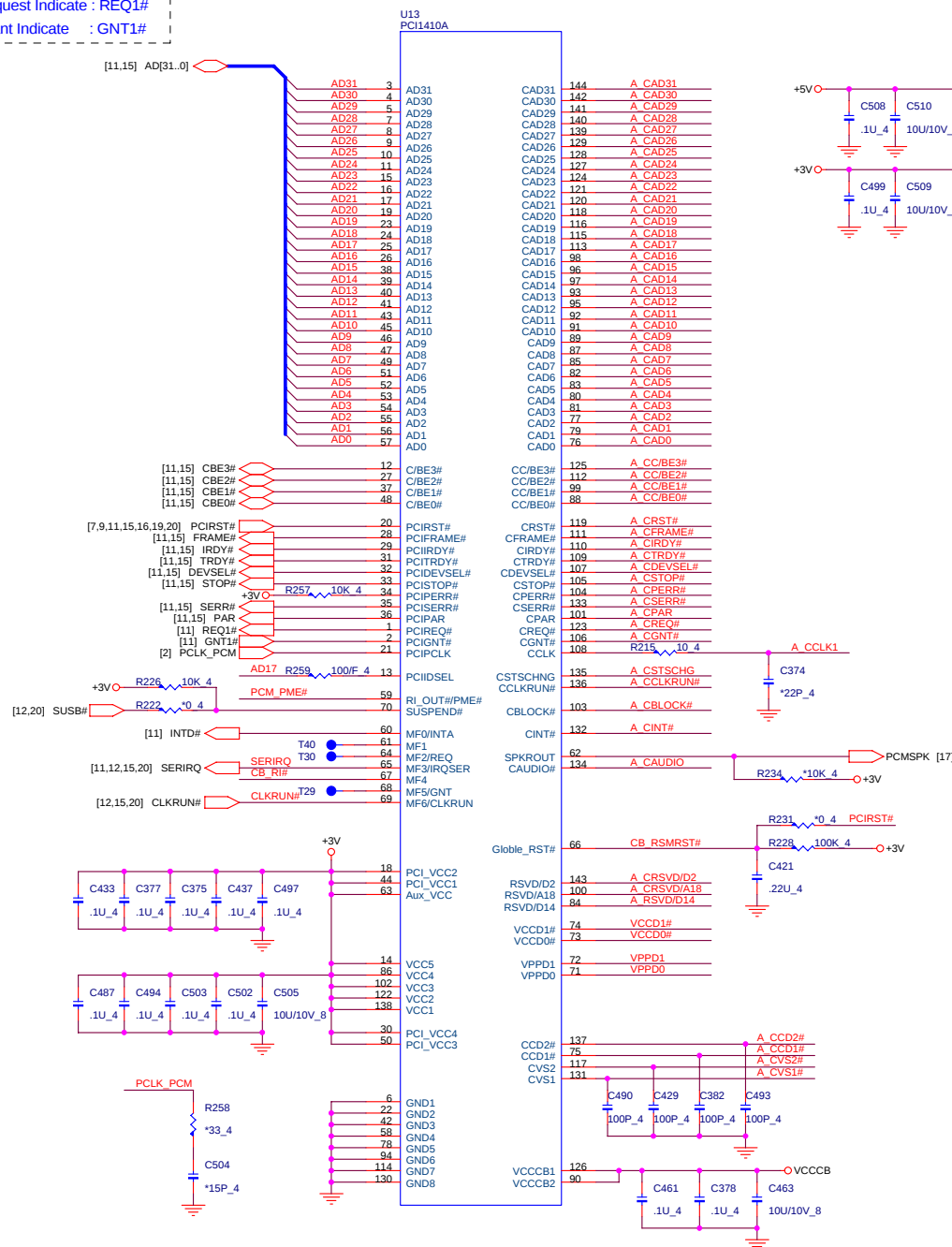
963L
- 4
Power



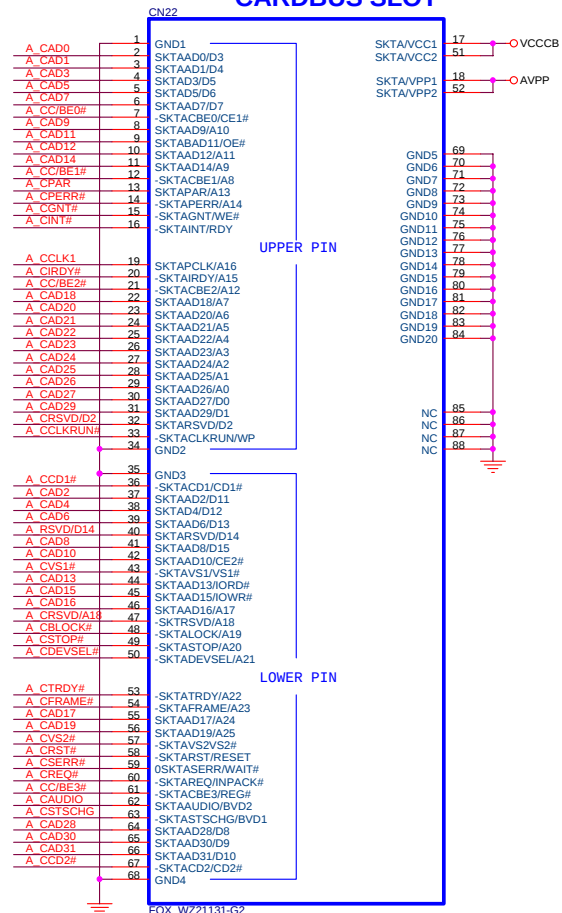
PROJECT : ZL5
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Size	Document Number	Rev
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Date:	Thursday, March 10, 2005	Sheet 13 of 26

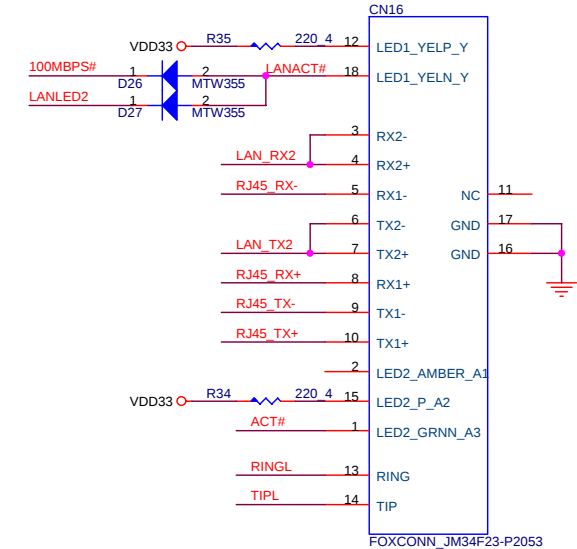
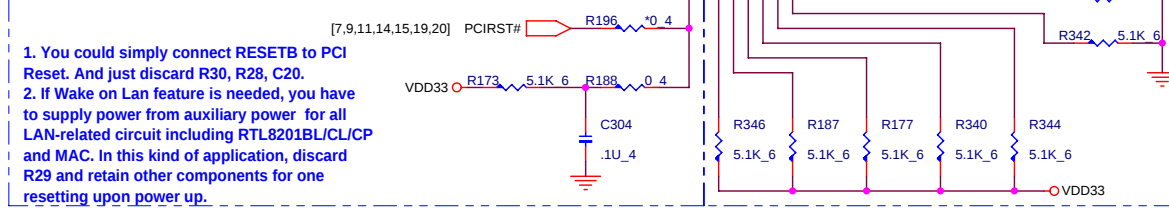
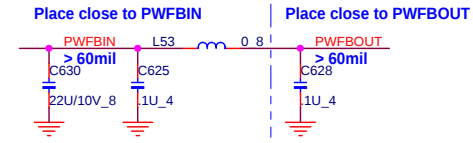
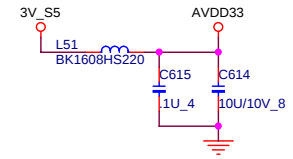
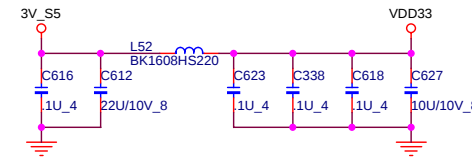
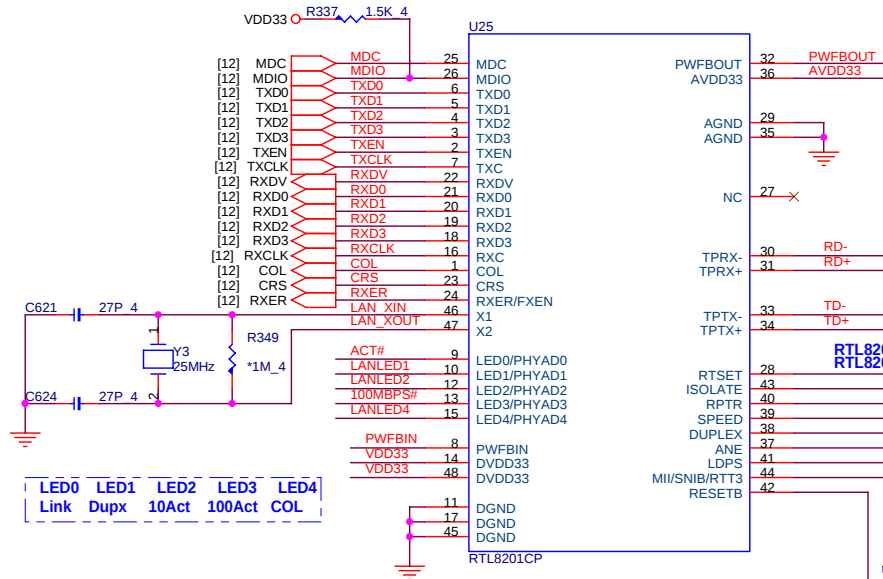
ID Select : AD17
Interrupt Pin : INTD#
Request Indicate : REQ1#
Grant Indicate : GNT1#



CARDBUS SLOT



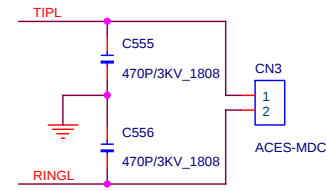
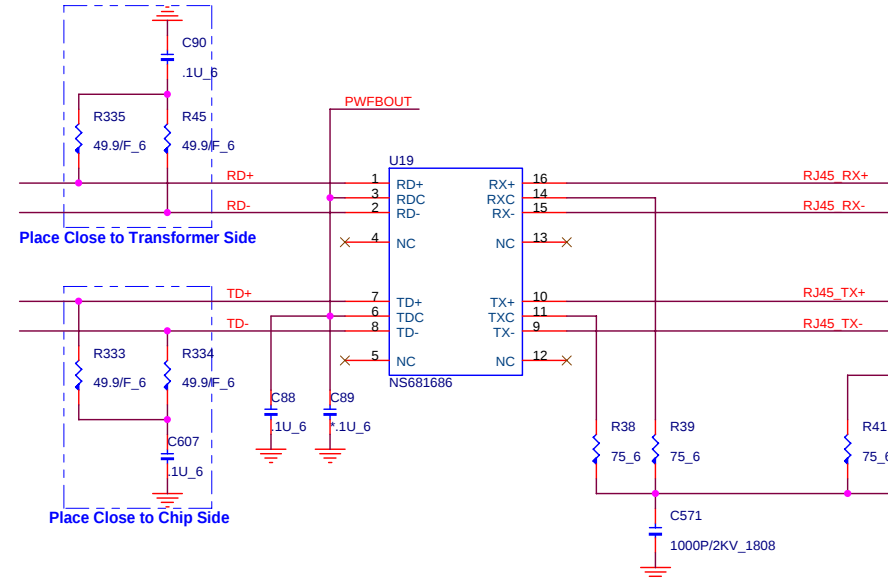
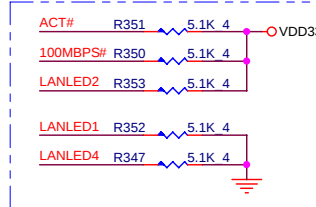
PROJECT : ZL5
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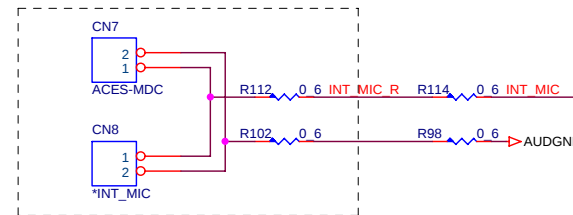
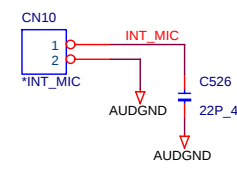
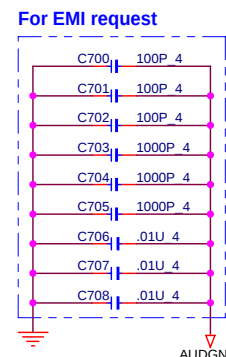
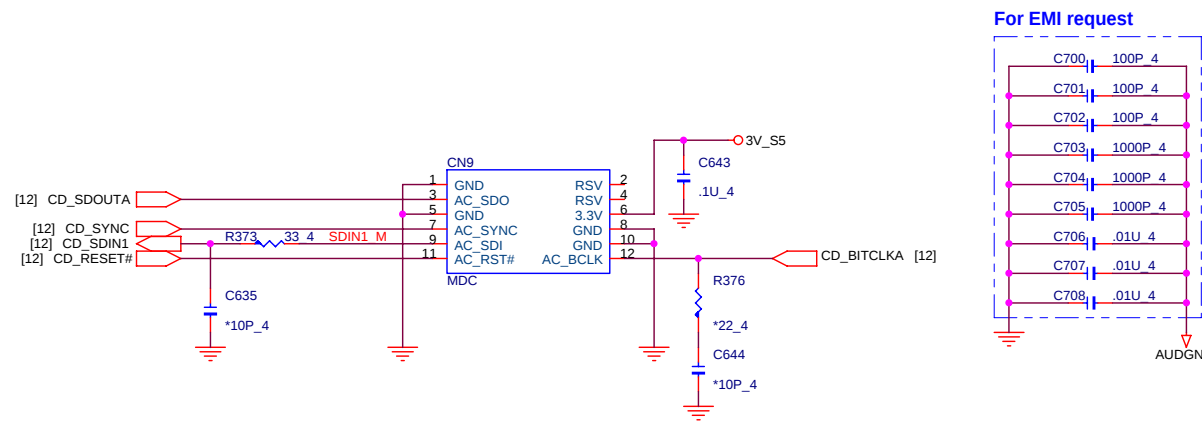
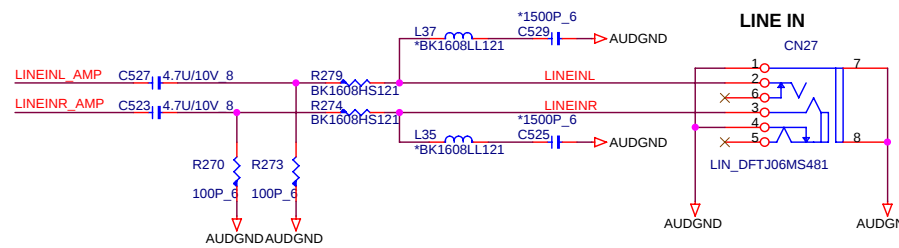
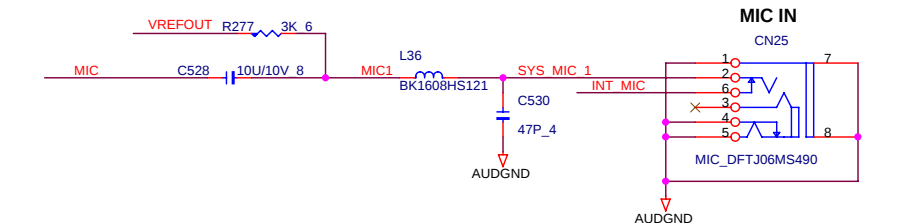
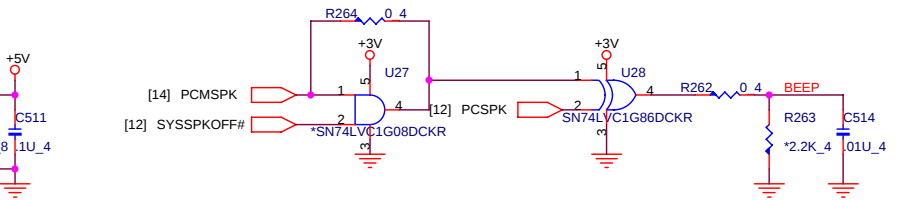
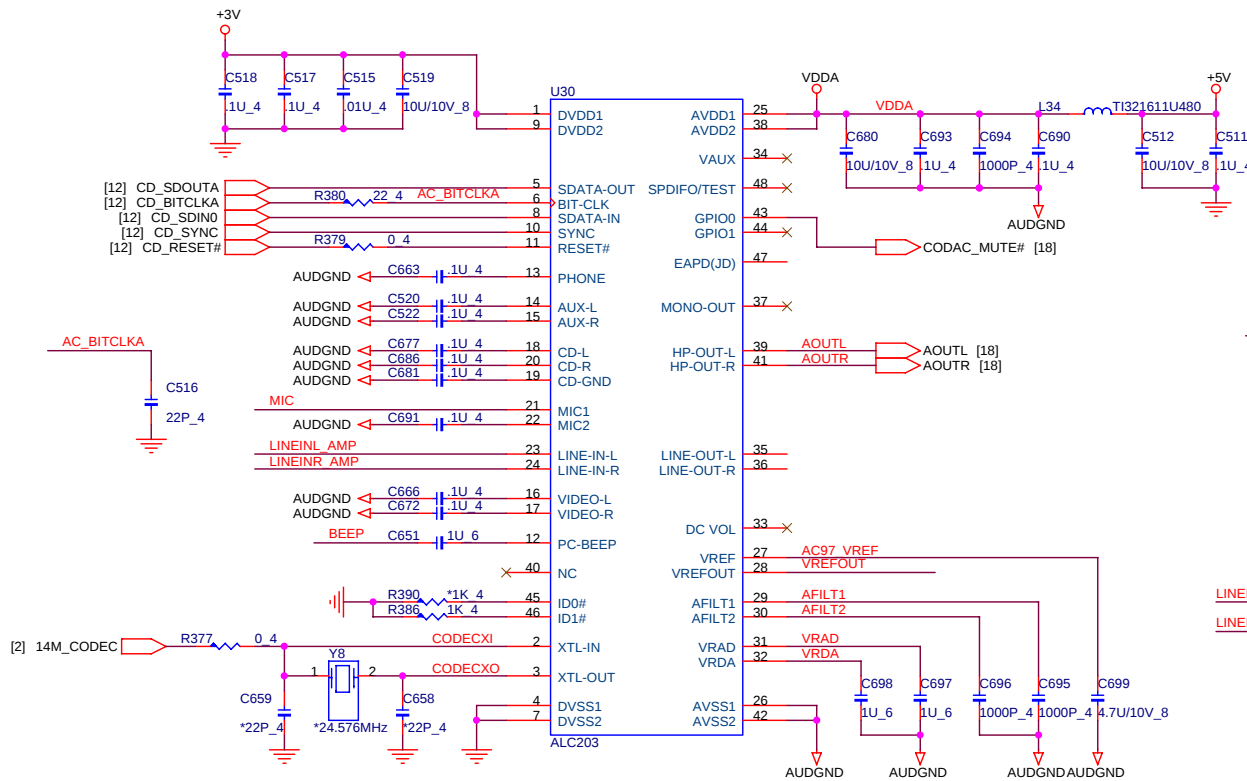


Reserved for 8201CL/CP LED Mode
Change to compatible with BL

Reserved for ensuring
8201BL/CL/CP latch to UTP Mode.

Reserved for ensuring 8201CL/CP
latch to normal operation mode.

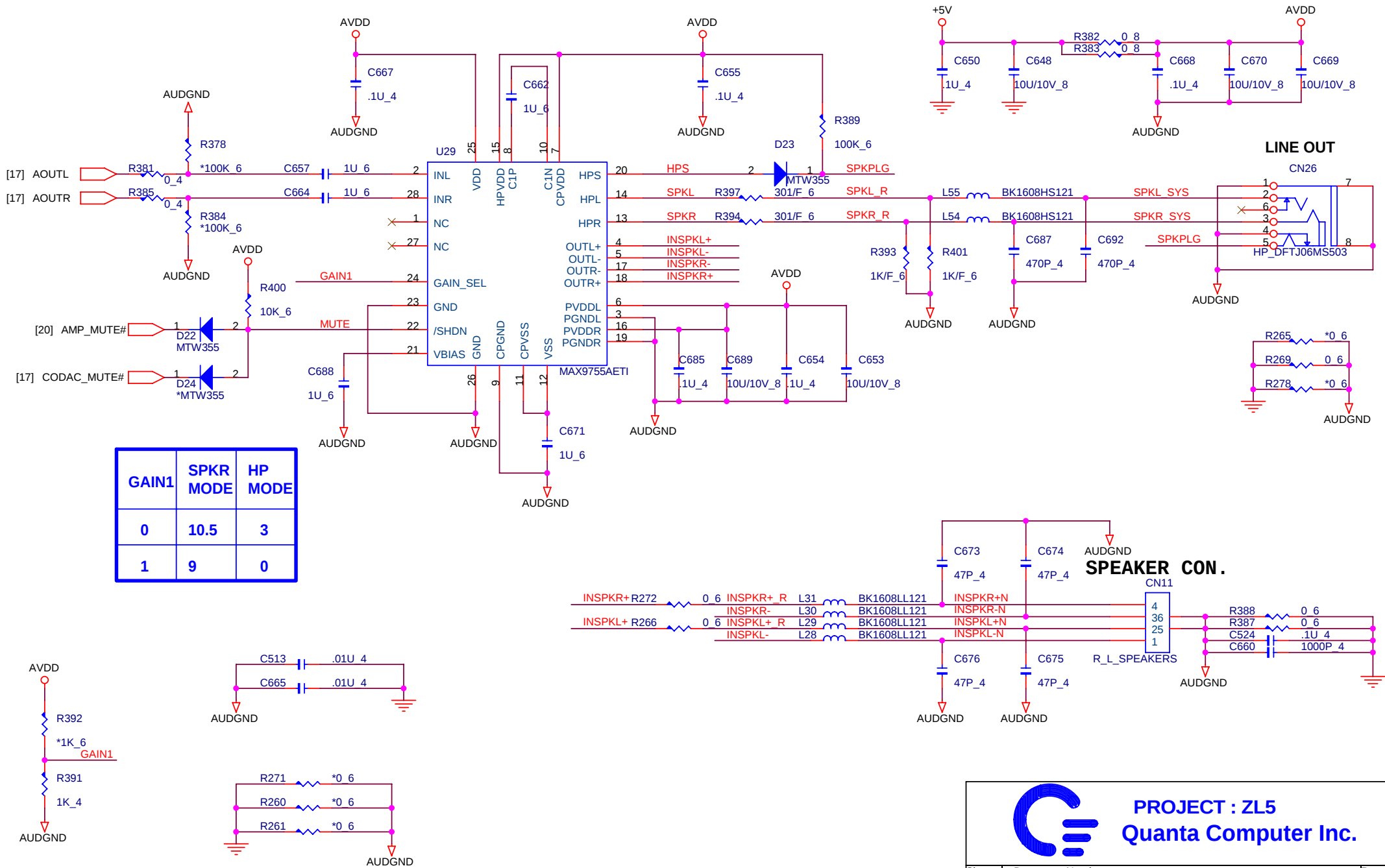


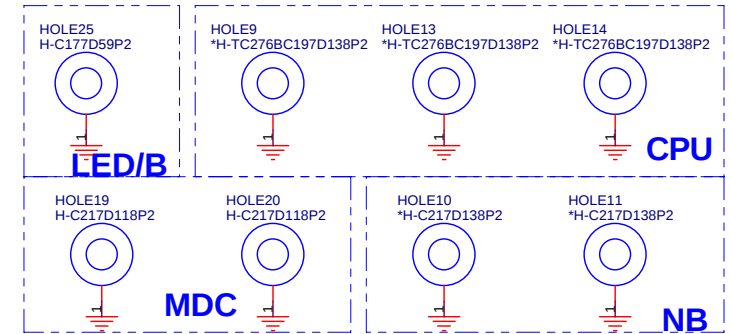
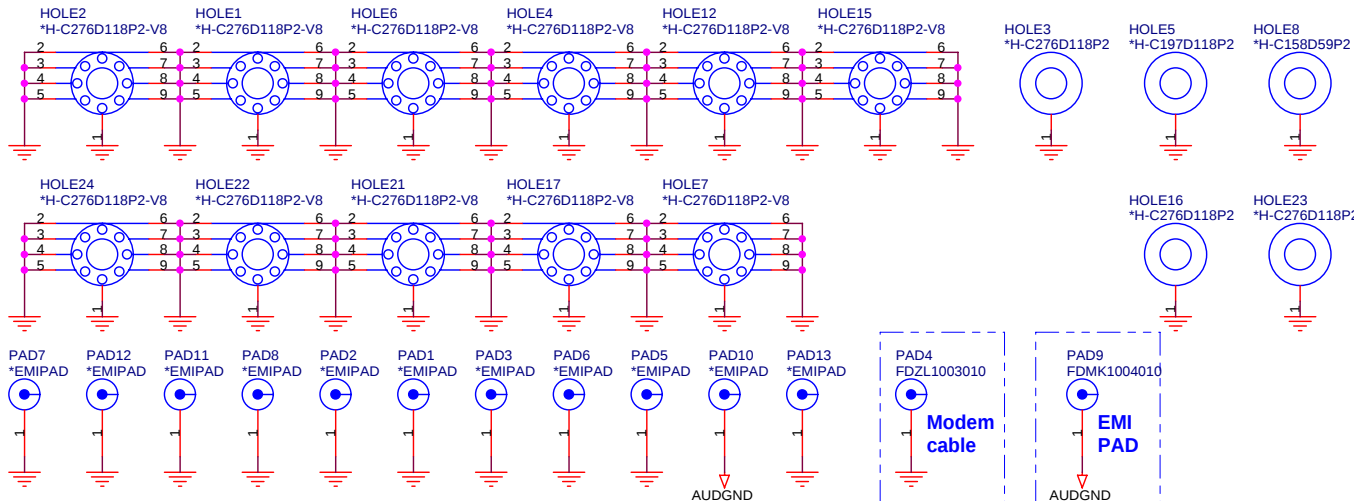
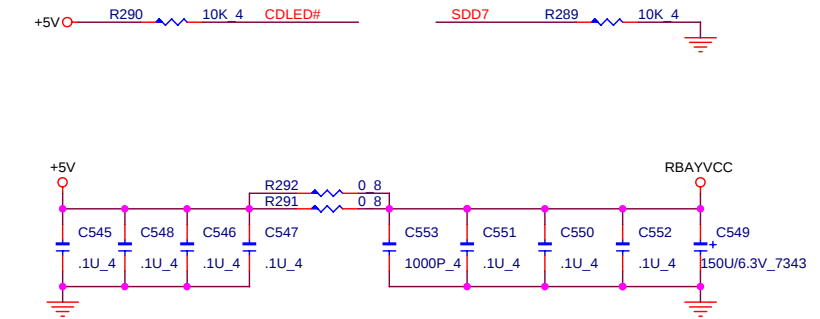
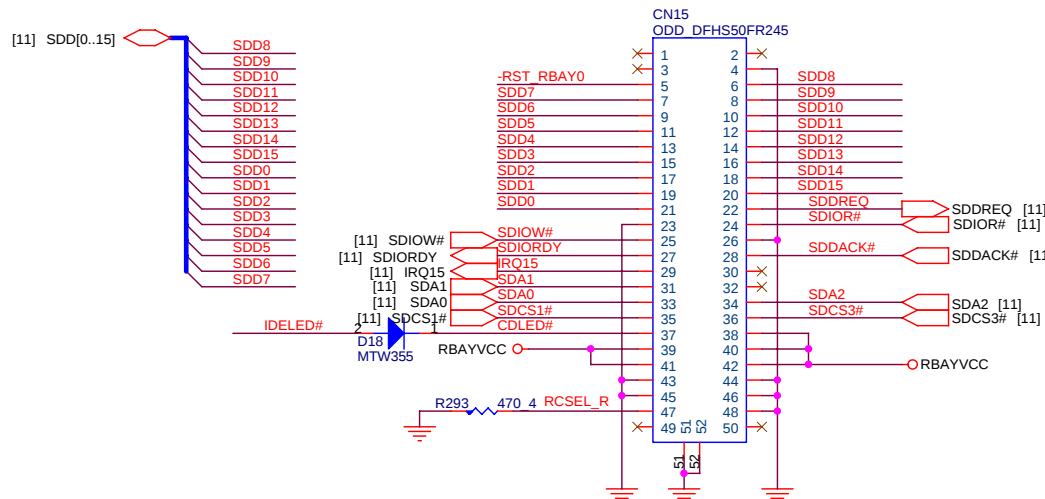
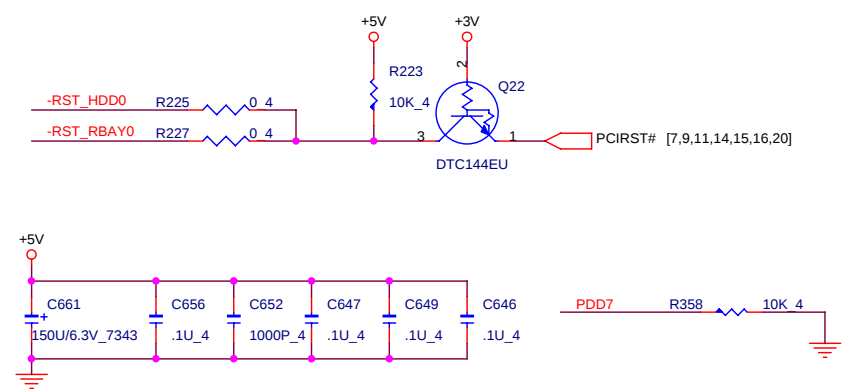
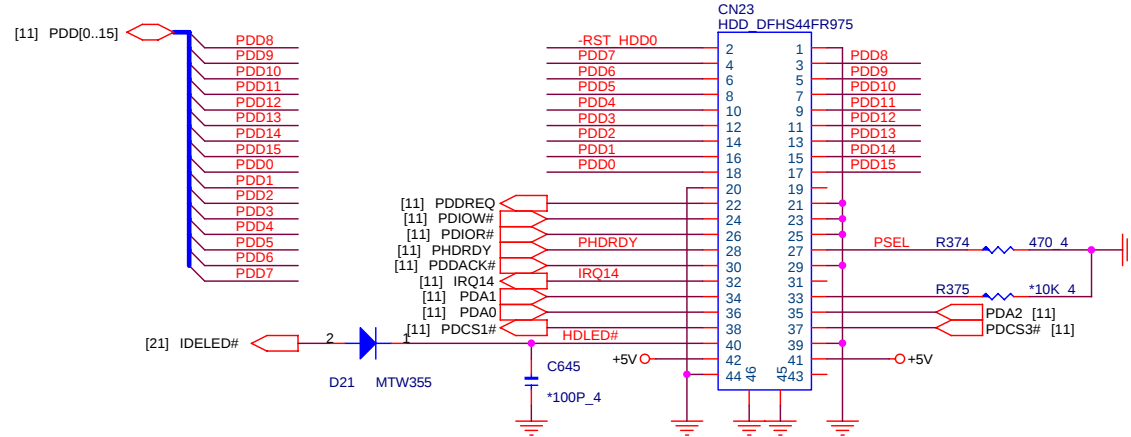




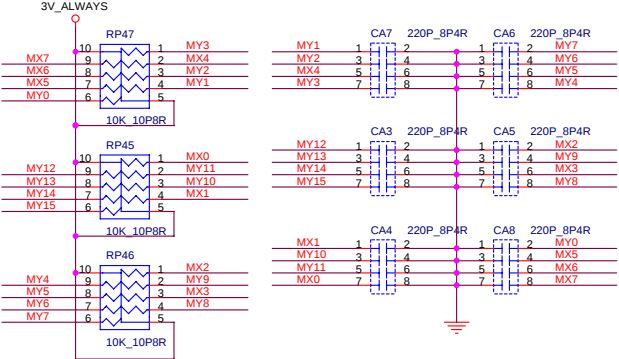
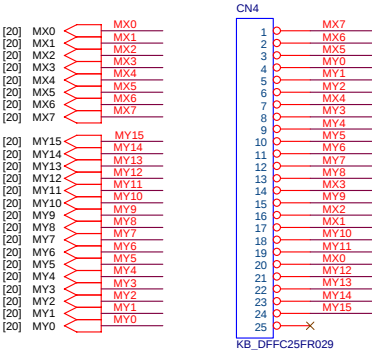
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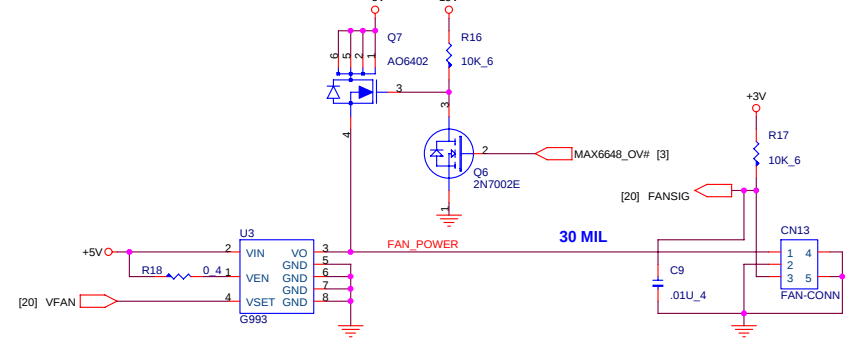




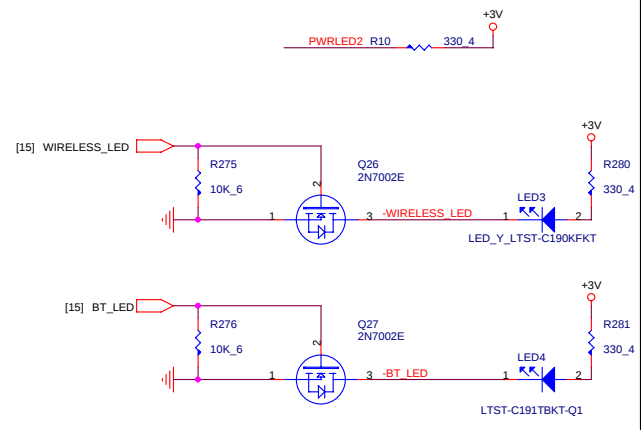
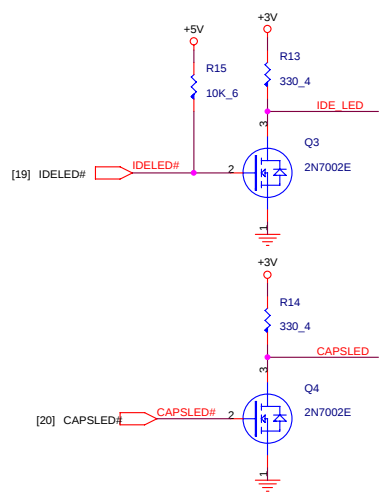
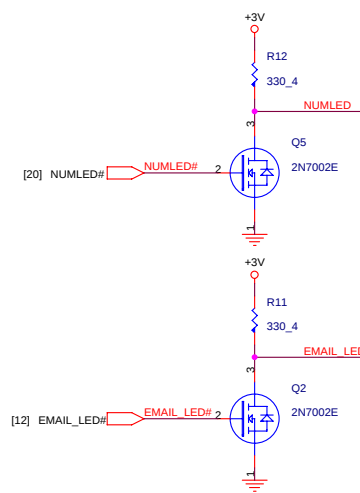
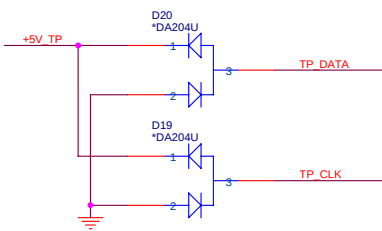
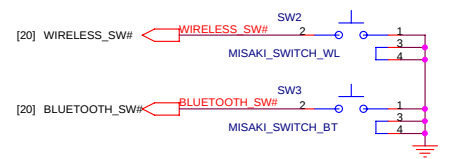
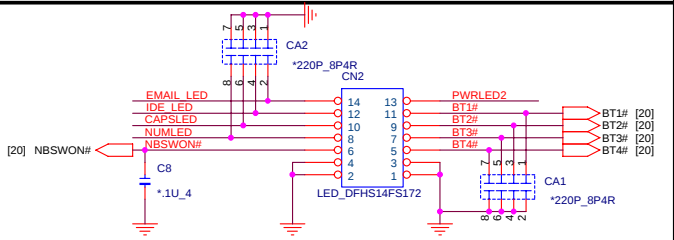
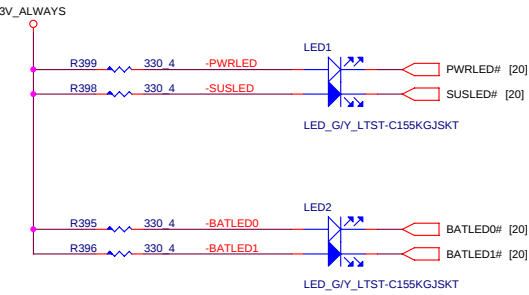
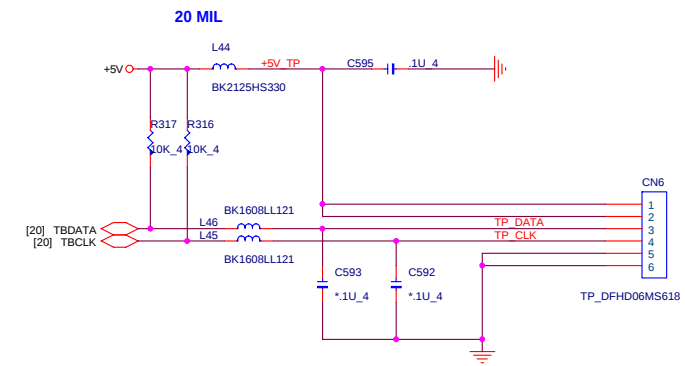
INT K/B

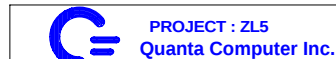


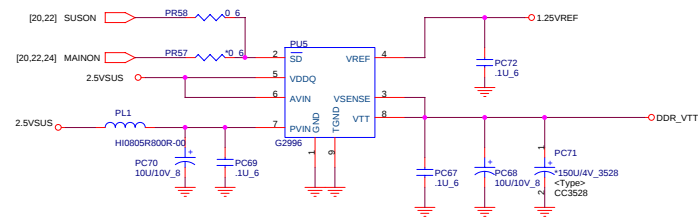
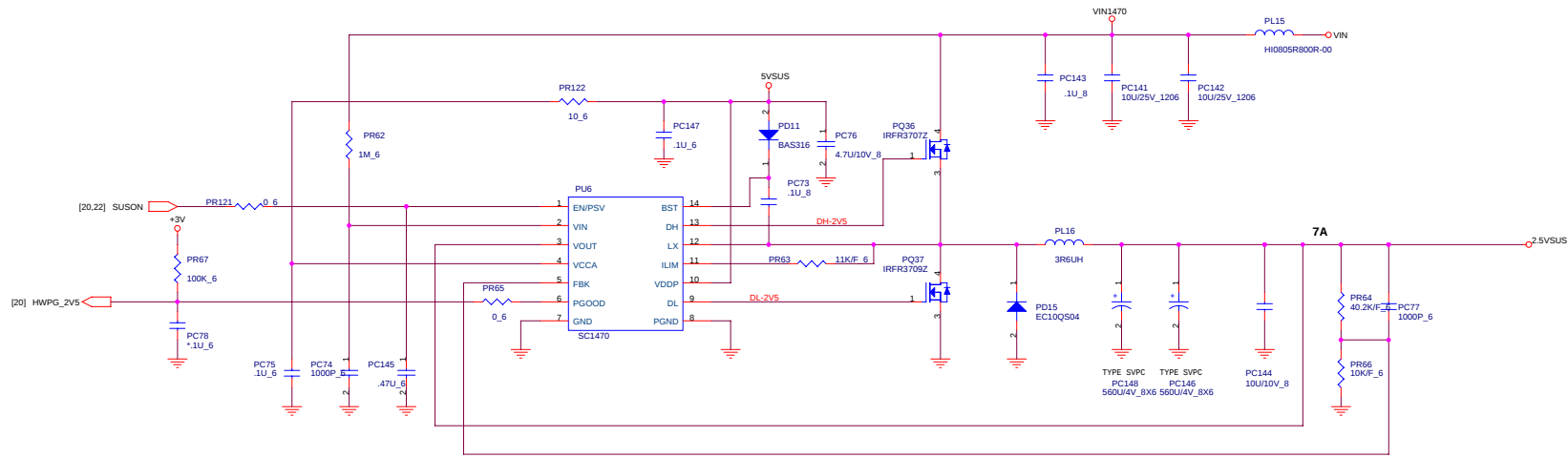
FAN CONTROL



TOUCH PAD

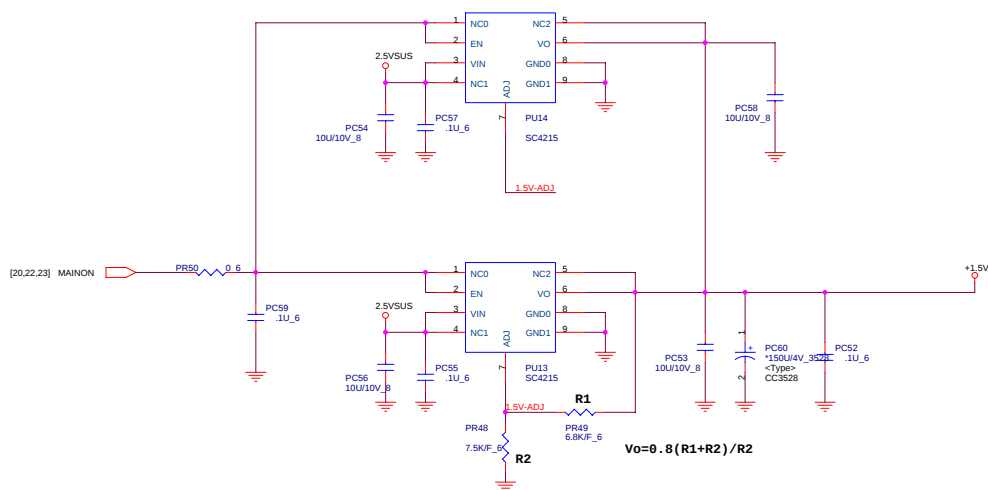
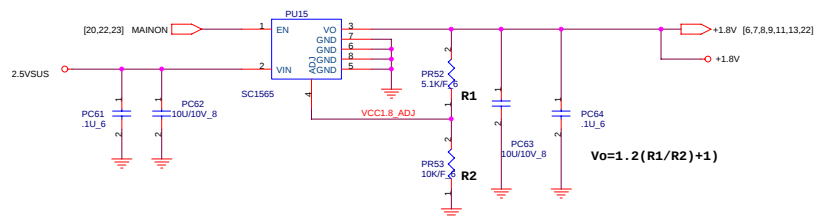
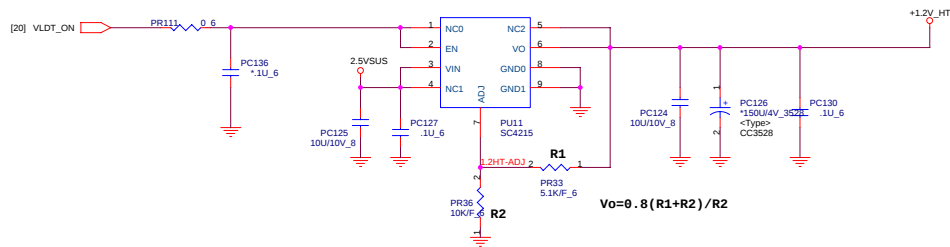






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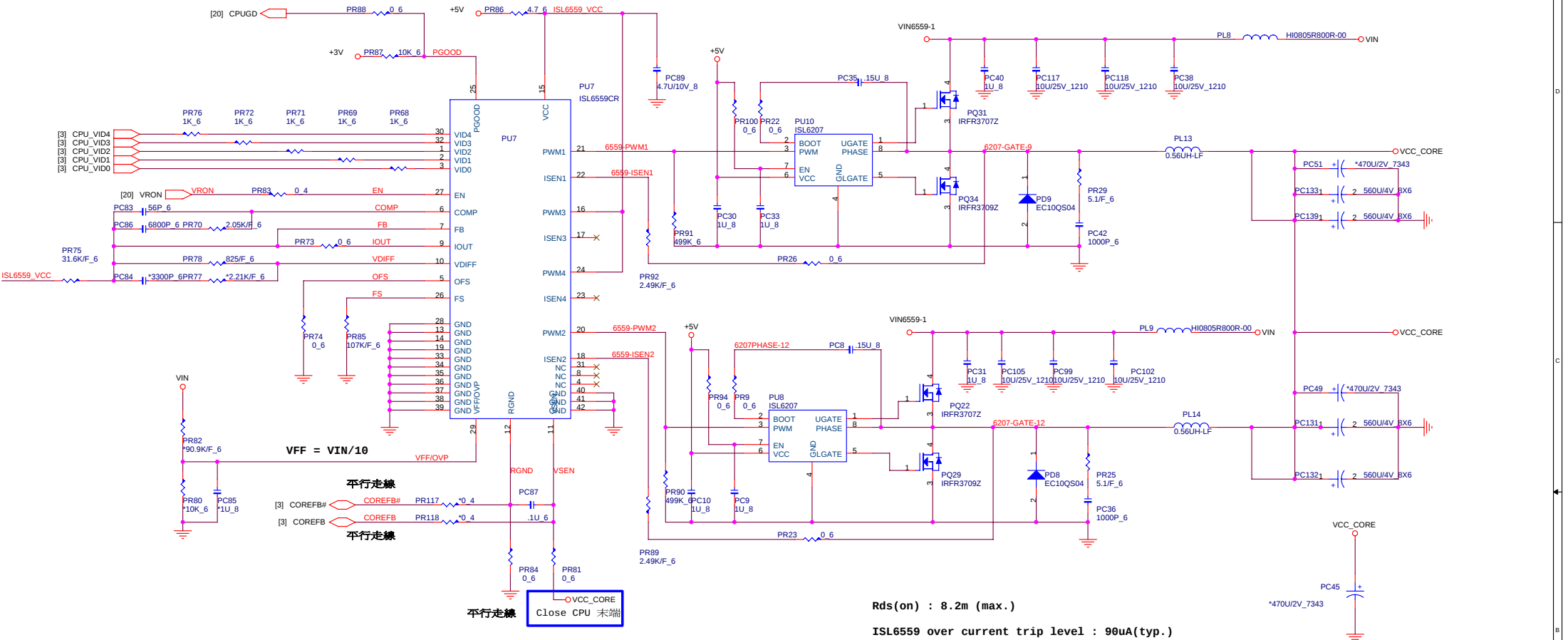
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Vcore



Rds(on) : 8.2m (max.)
ISL6559 over current trip level : 90uA(typ.)
Full load Isen current : 90uA/1.5 ~ 60uA
AMD LPM 35W current 28A
 $Rds(on) * Io(phase) = Rsen * Isen$
 $8.2m * 1.3 * (28A/2) = Rsen * 60uA$
 $Rsen = 2.48K \sim 2.49K$
OCP : $28A * 1.5 = 42A$



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