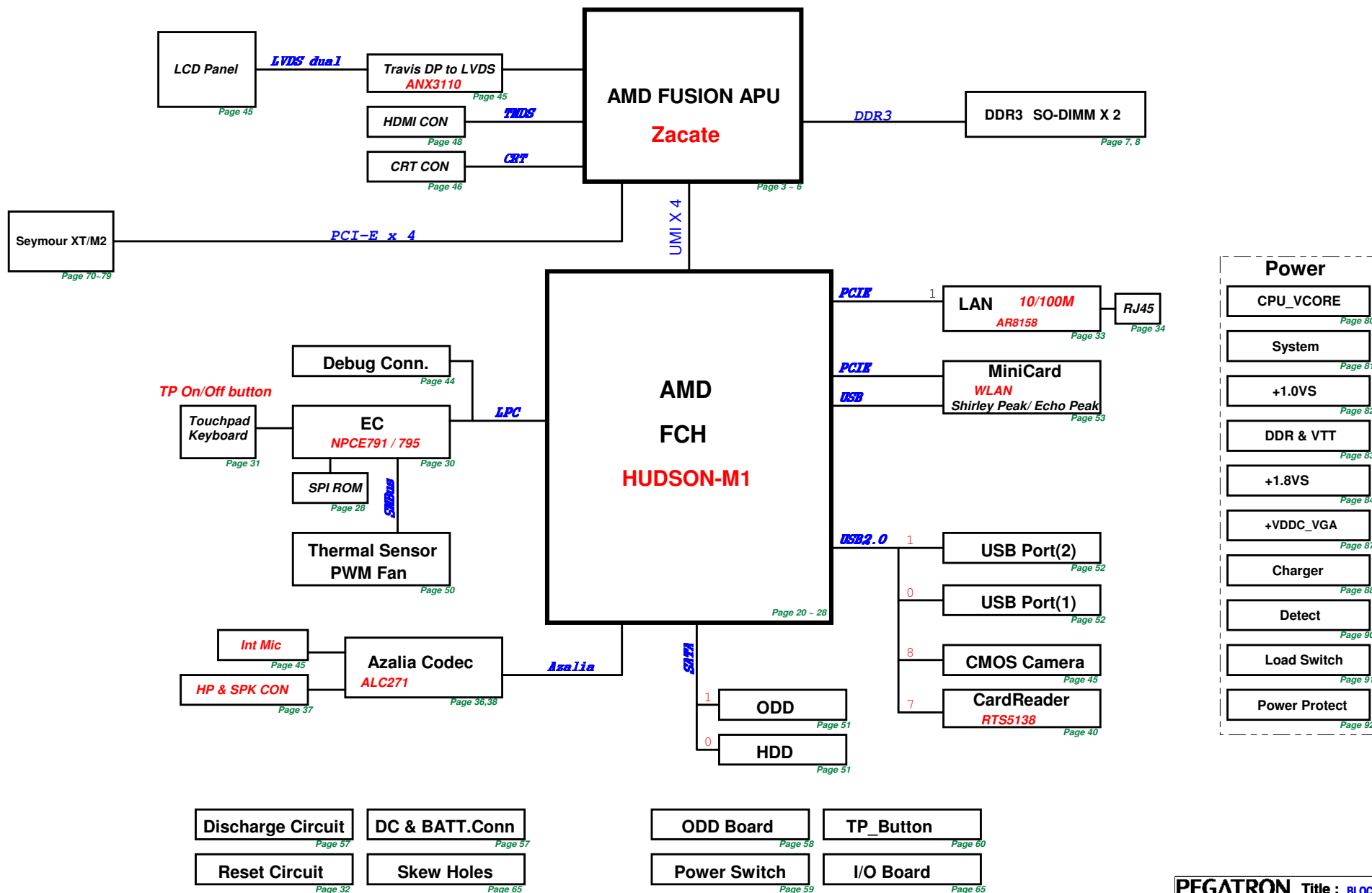


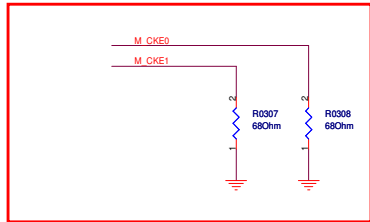
AAB70 AMD Brazos Platform Rev. 2.0

BLOCK DIAGRAM

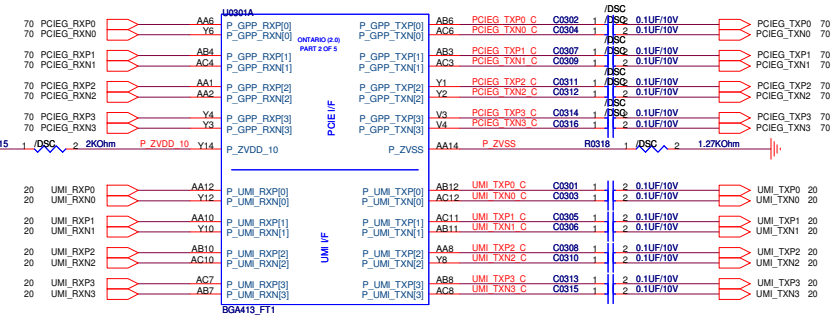
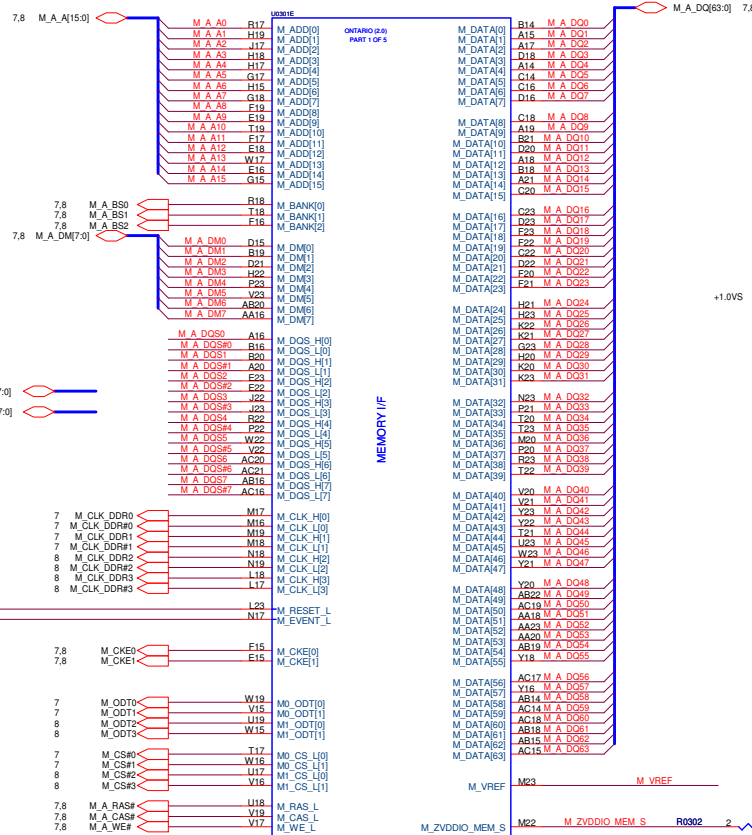
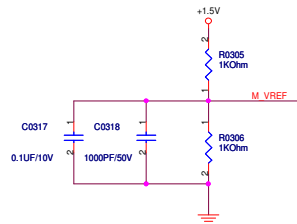
R 1.1 /0301



1228



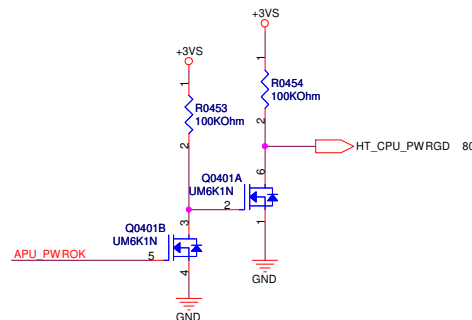
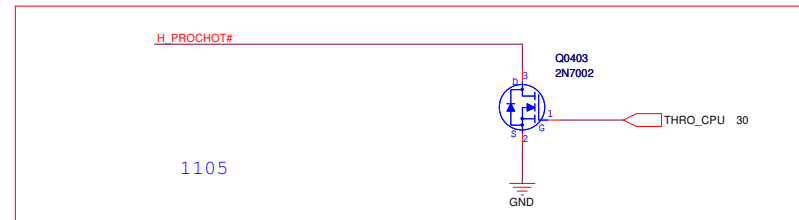
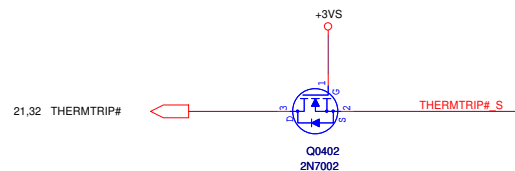
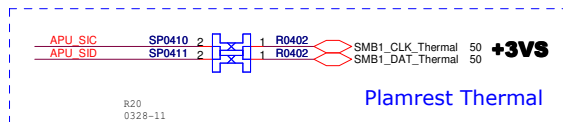
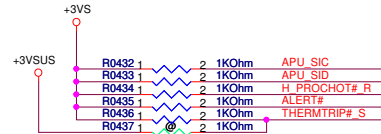
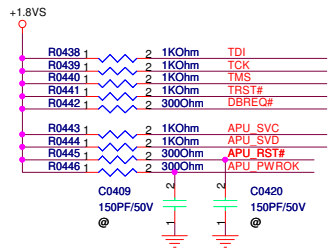
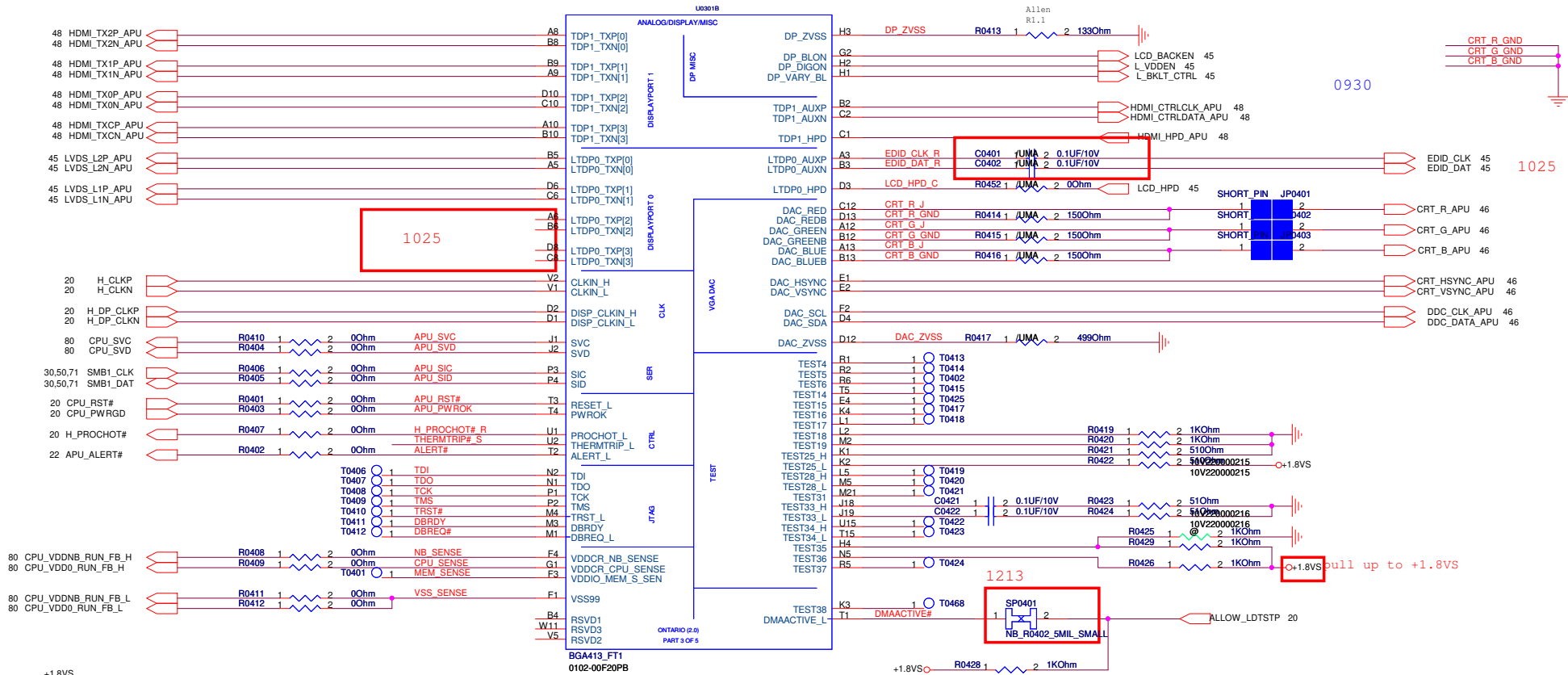
place within 1000mils with APU

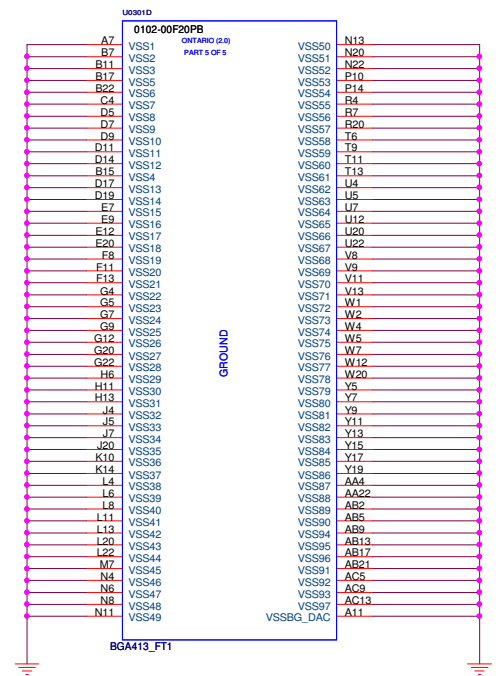
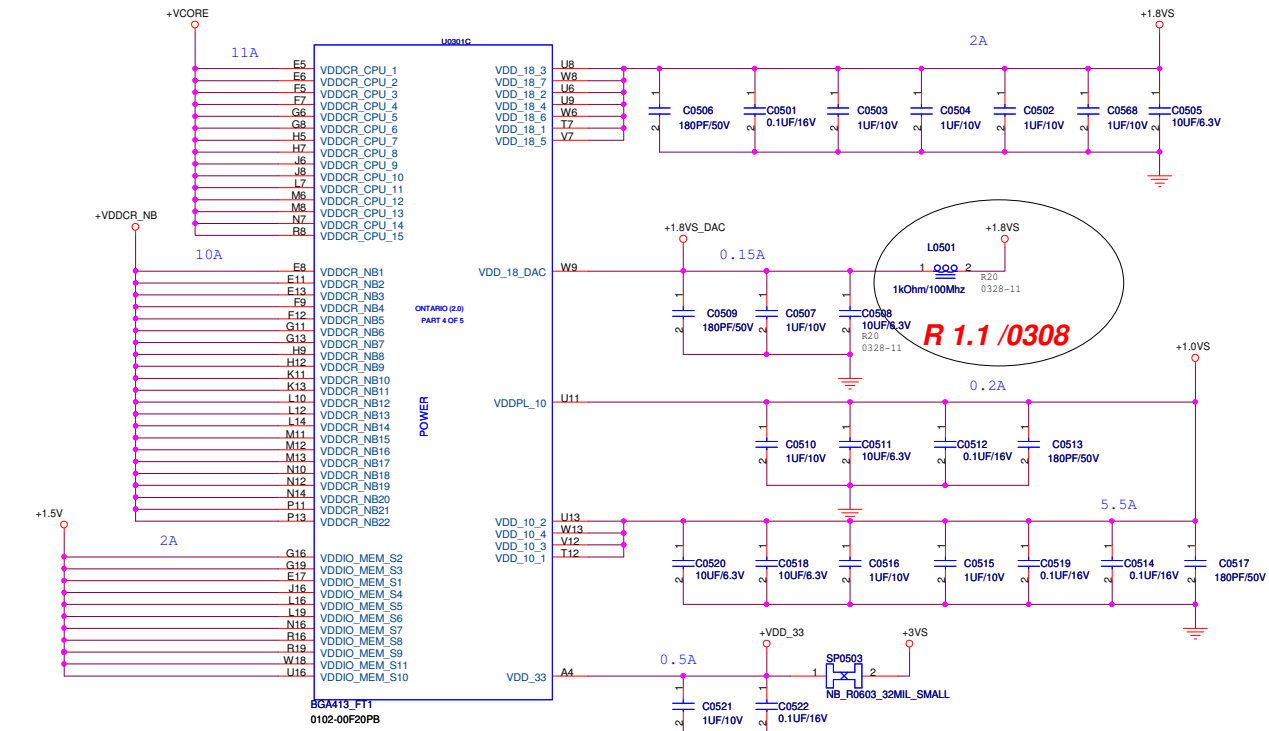


0930

0930

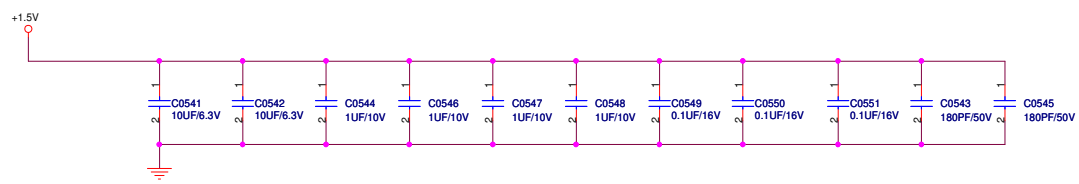
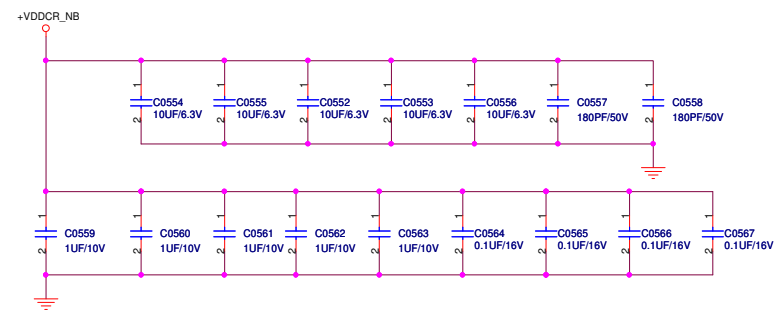
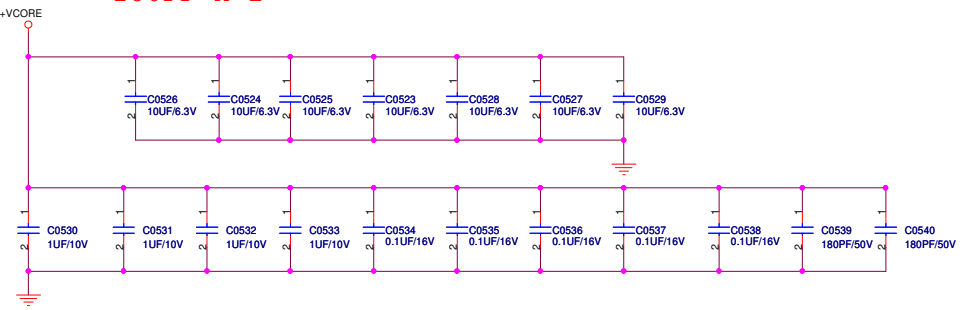
1025

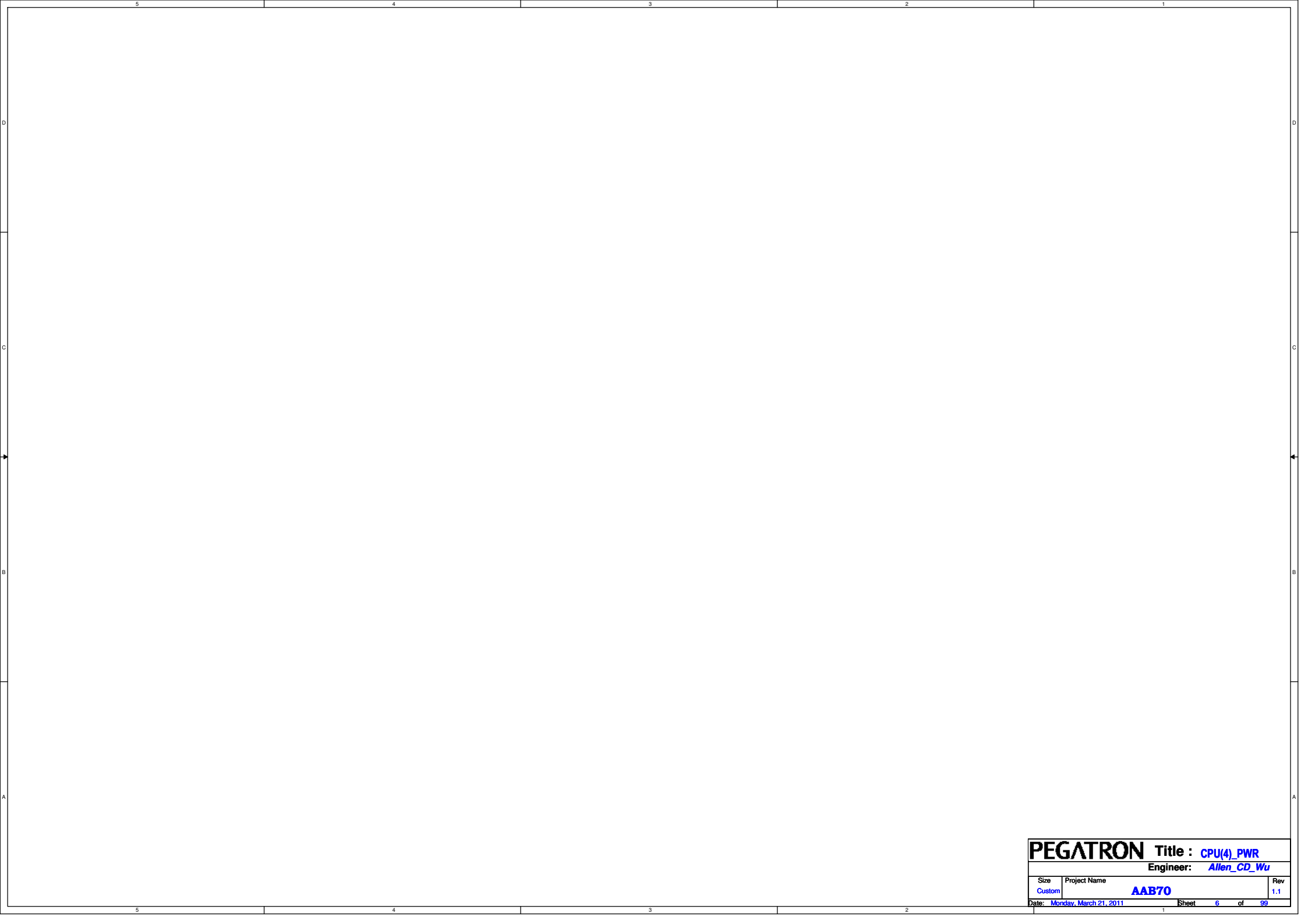




+VCORE
 10UF x 7
 1UF x 4
 0.1UF x 5
 180PF x 2

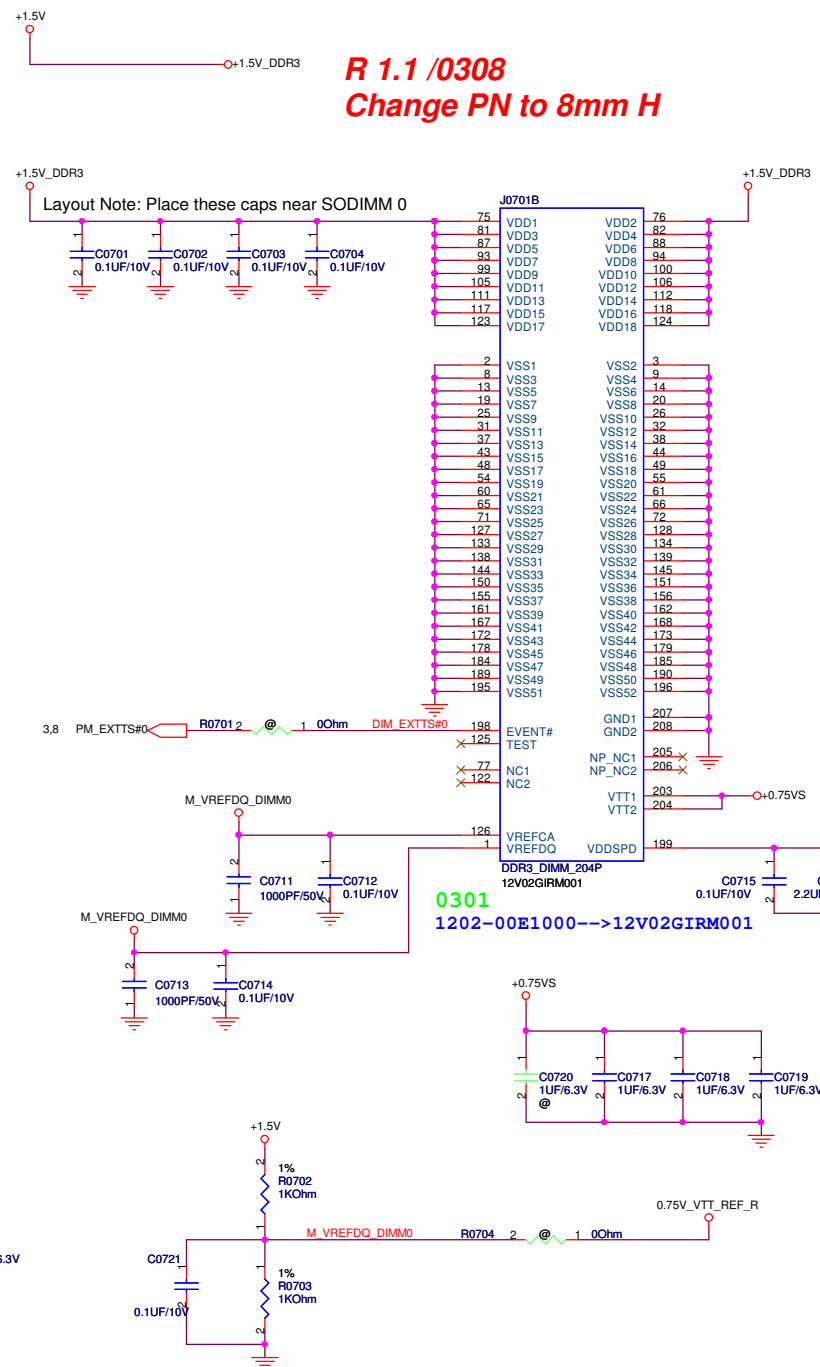
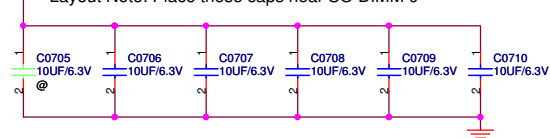
+VDDCR_NB
 10UF x 7
 1UF x 4
 0.1UF x 5
 180PF x 2





PEGATRON		Title : CPU(4)_PWR	
		Engineer: Allen_CD_Wu	
Size	Project Name		Rev
Custom	AAB70		1.1
Date: Monday, March 21, 2011		Sheet	6 of 99

1202-002H000



Engineer: Allen CD Wu

Date: Thursday, April 21, 2011 Sheet 7 of 99

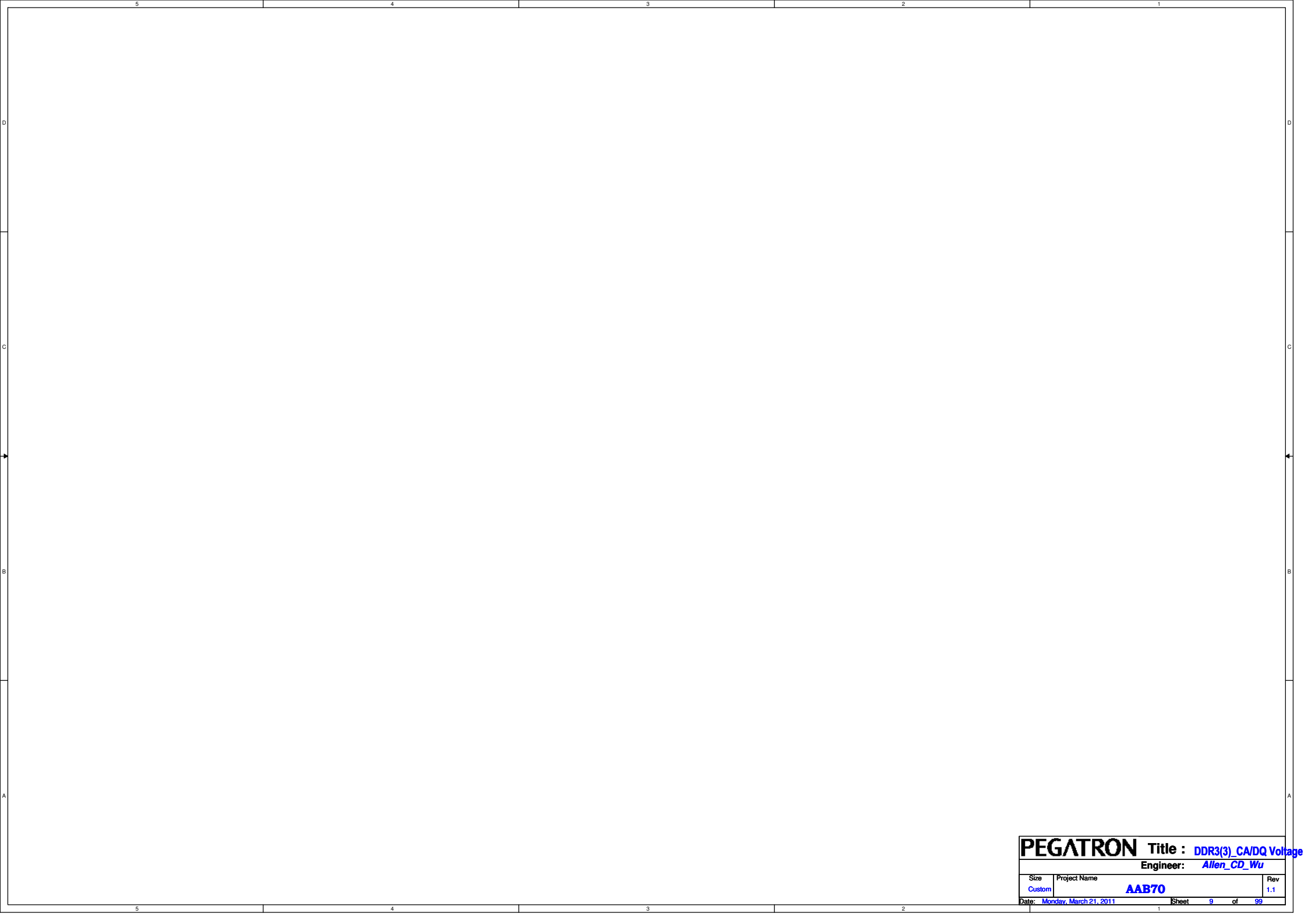
Date: Thursday, April 21, 2011 Sheet 7 of 99

1202-000P000

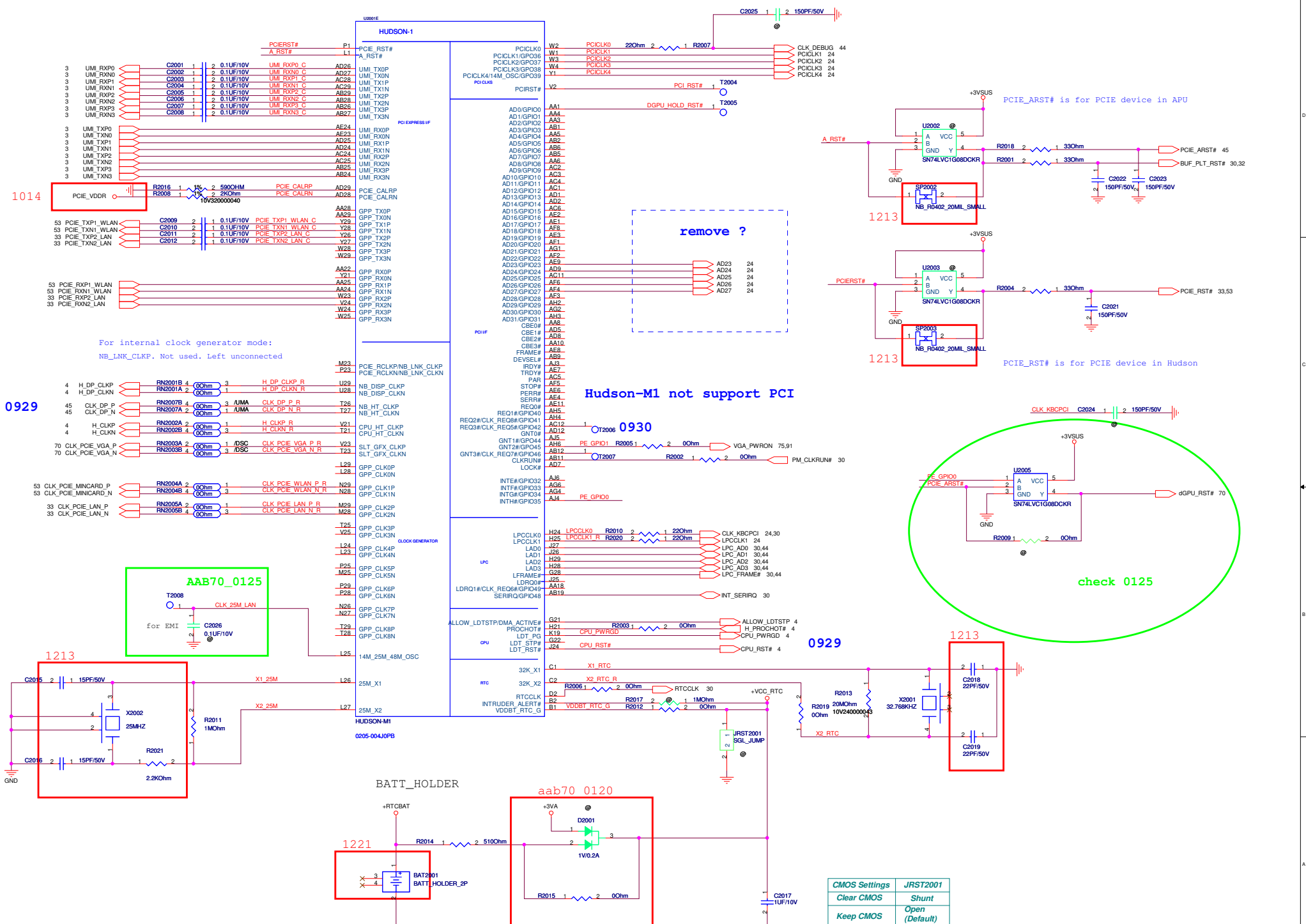
R 1.1 /0308

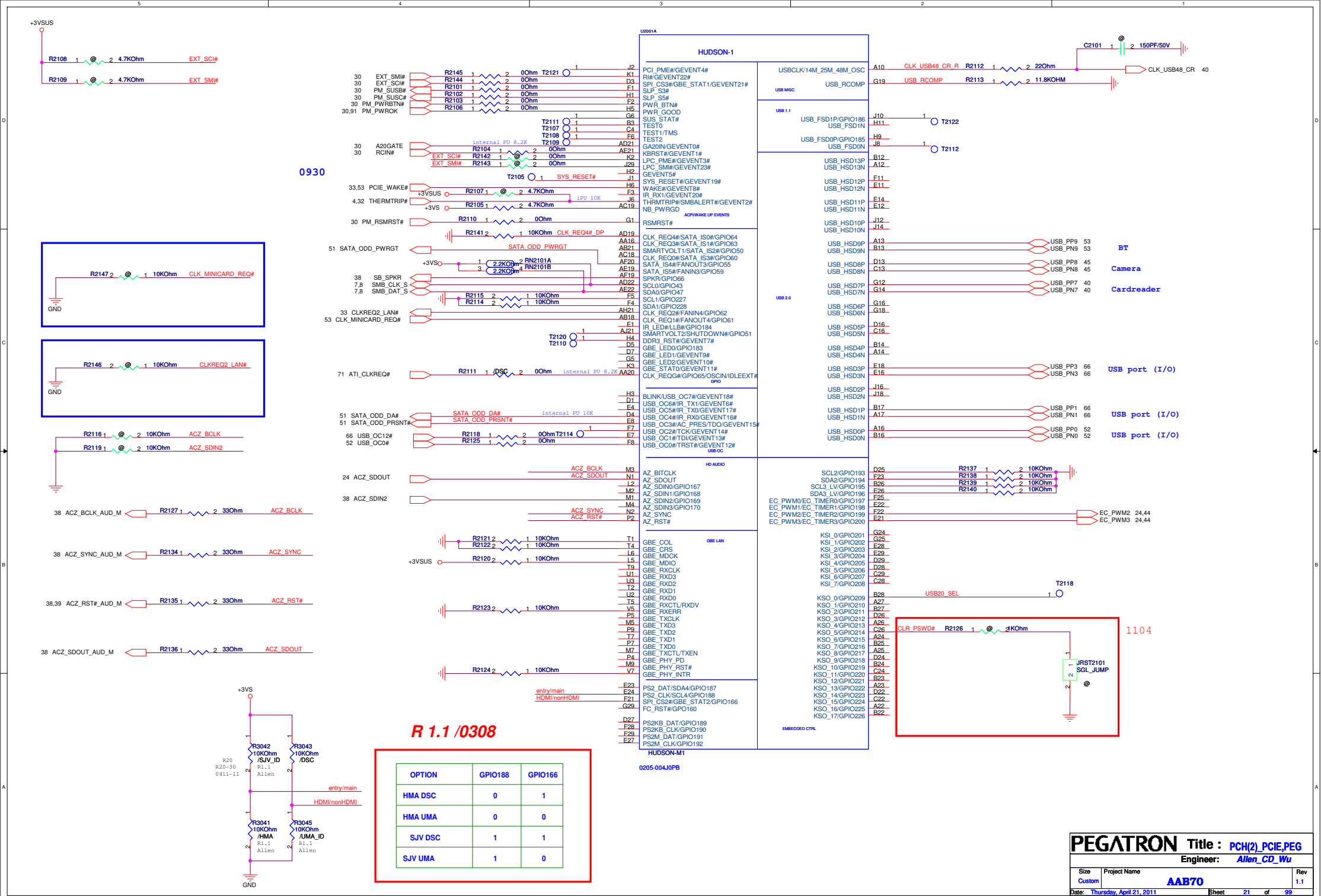
Change PN to 8mm H

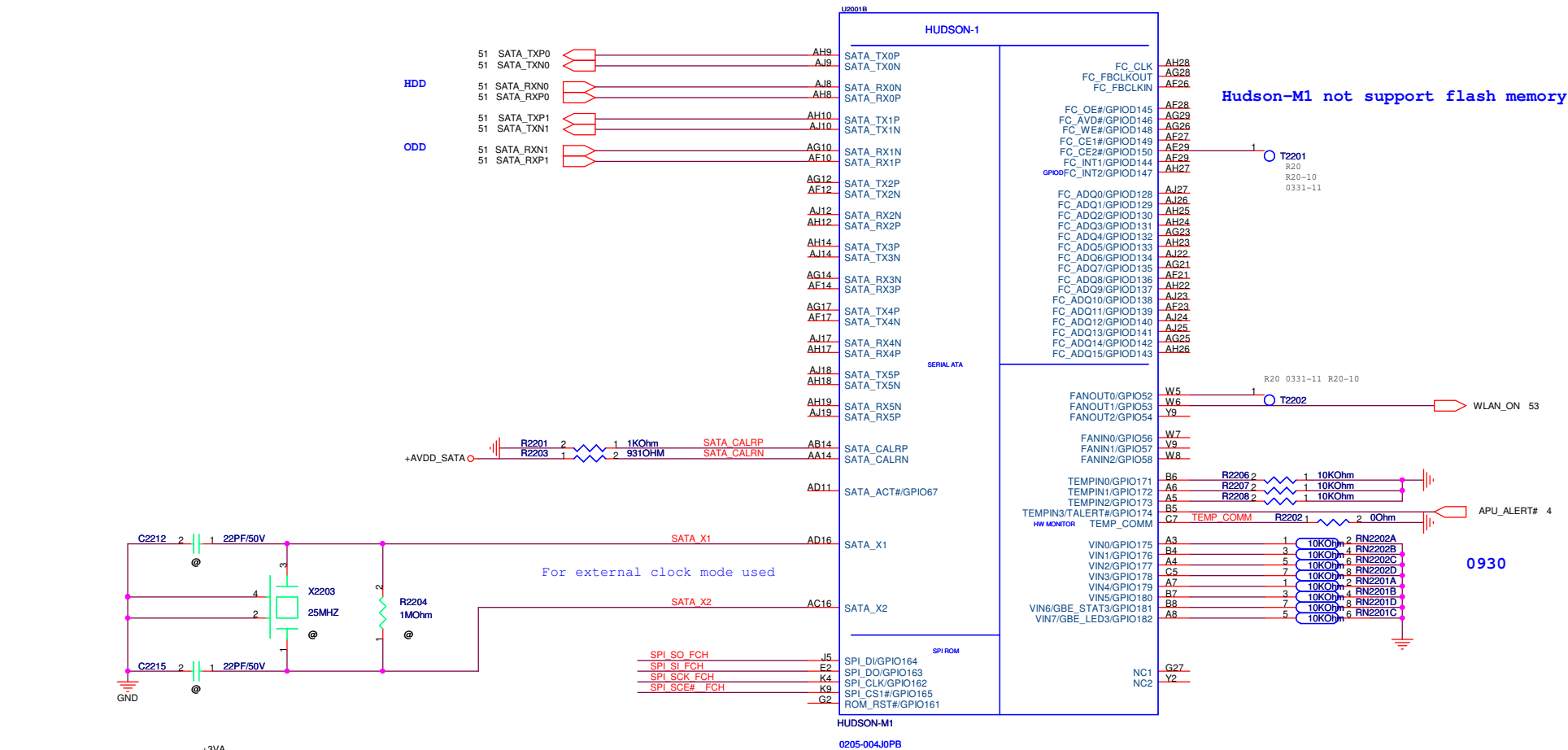




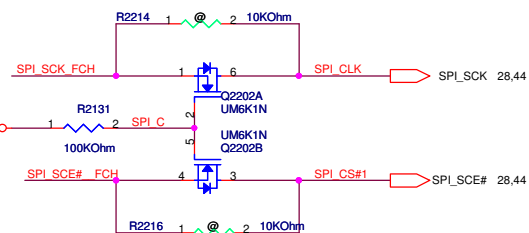
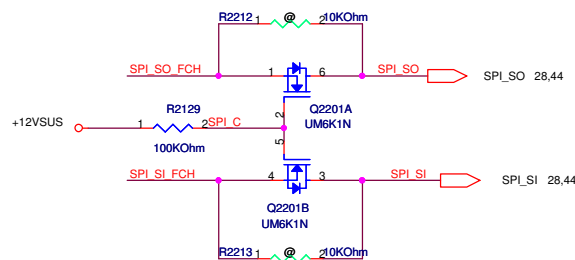
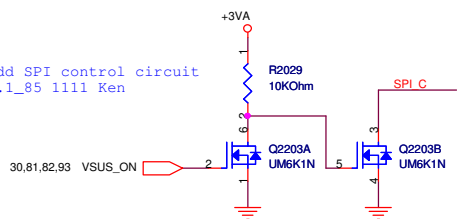
PEGATRON		Title : <i>DDR3(3)_CA/DQ Voltage</i>	
		Engineer: <i>Allen_CD_Wu</i>	
Size	Project Name		Rev
<i>Custom</i>	AAB70		<i>1.1</i>
Date: <i>Monday, March 21, 2011</i>		Sheet <i>9</i> of <i>99</i>	

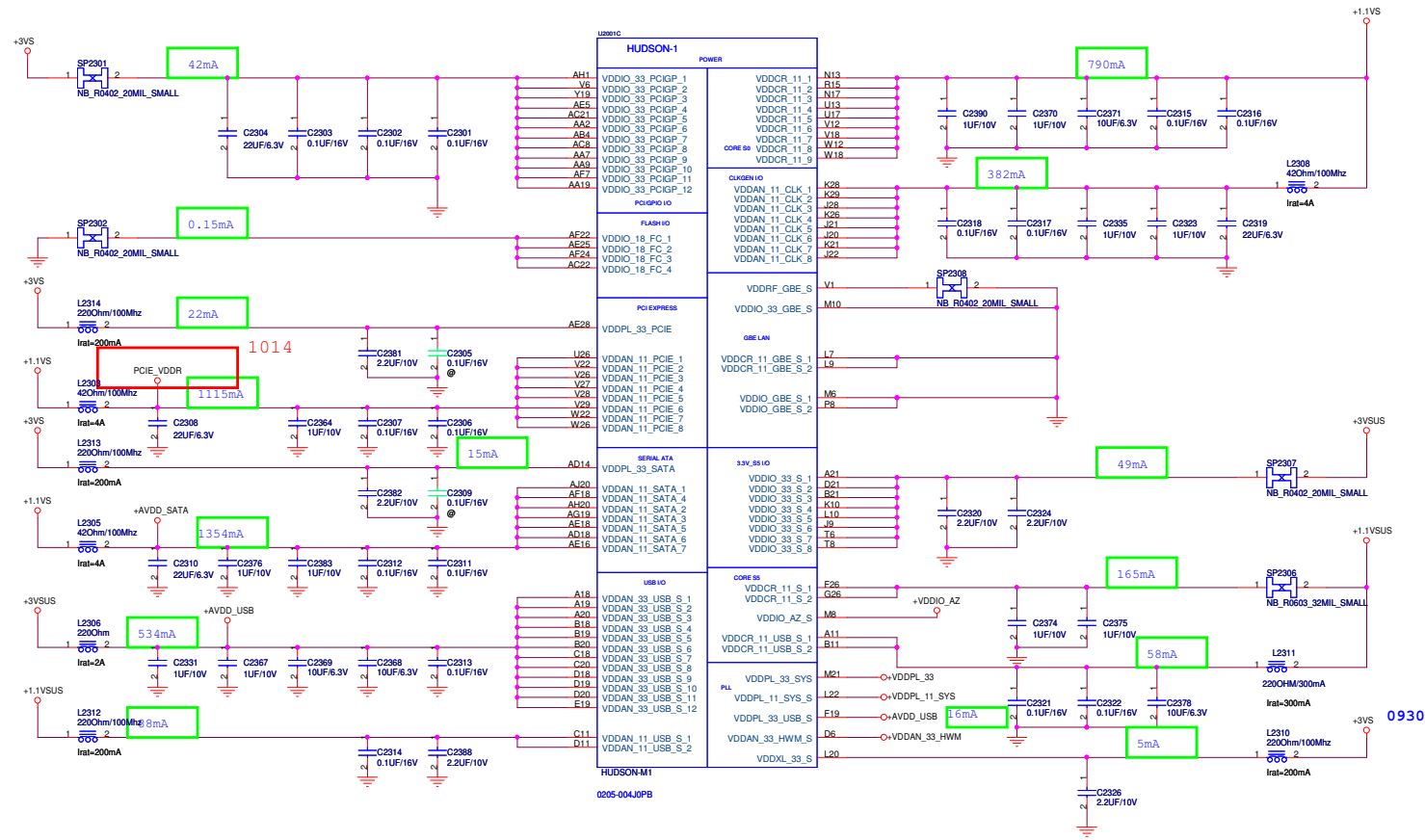






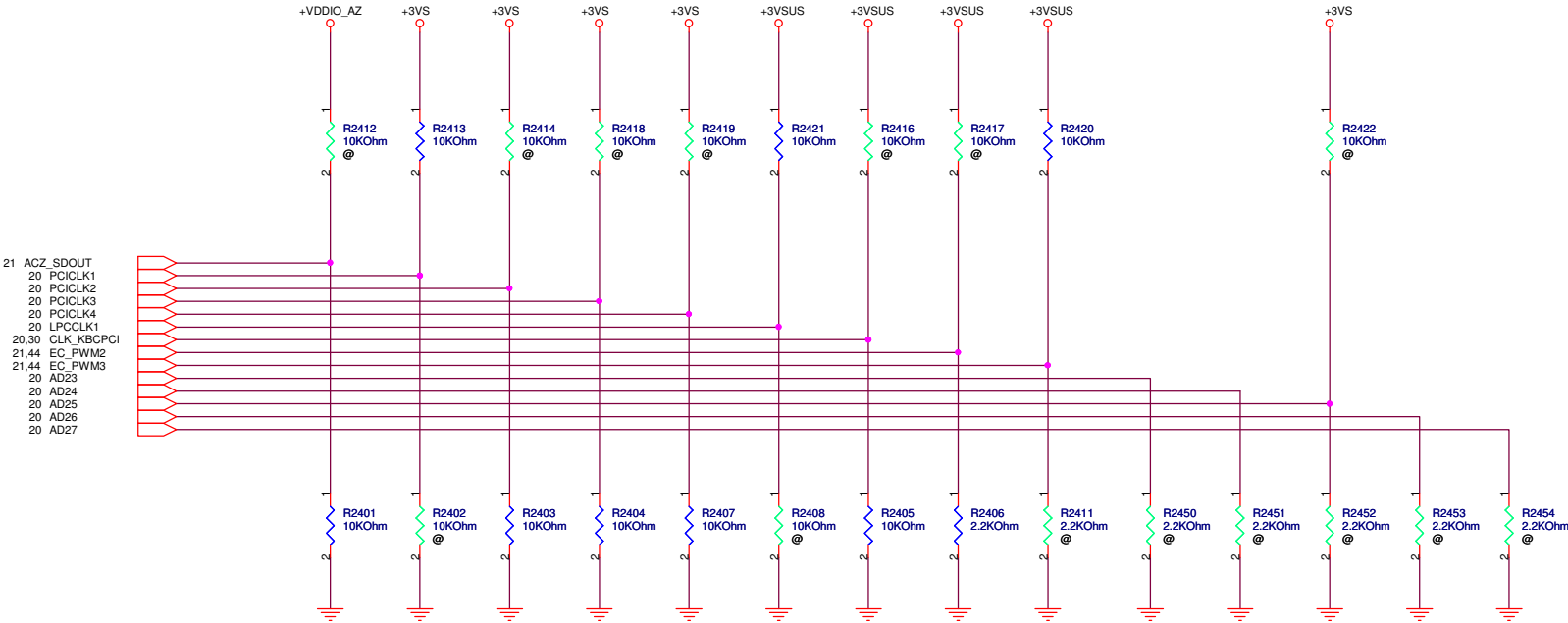
Add SPI control circuit
1.1_85 1111 Ken





HUDSON-1		
Y14	VSSIO SATA_1	VSS_1
Y16	VSSIO SATA_2	VSS_2
AS16	VSSIO SATA_3	VSS_3
AC14	VSSIO SATA_4	VSS_4
AE14	VSSIO SATA_5	VSS_5
AE11	VSSIO SATA_6	VSS_6
AE9	VSSIO SATA_7	VSS_7
AE11	VSSIO SATA_8	VSS_8
AE13	VSSIO SATA_9	VSS_9
AE16	VSSIO SATA_10	VSS_10
AG8	VSSIO SATA_11	VSS_11
AH7	VSSIO SATA_12	VSS_12
AH11	VSSIO SATA_13	VSS_13
AH13	VSSIO SATA_14	VSS_14
AH16	VSSIO SATA_15	VSS_15
AJ7	VSSIO SATA_16	VSS_16
AJ11	VSSIO SATA_17	VSS_17
AJ13	VSSIO SATA_18	VSS_18
AJ16	VSSIO SATA_19	VSS_19
AG	VSSIO USB_1	VSS_20
B10	VSSIO USB_2	VSS_21
K11	VSSIO USB_3	VSS_22
B9	VSSIO USB_4	VSS_23
D10	VSSIO USB_5	VSS_24
D12	VSSIO USB_6	VSS_25
D14	VSSIO USB_7	VSS_26
D17	VSSIO USB_8	VSS_27
E9	VSSIO USB_9	VSS_28
F9	VSSIO USB_10	VSS_29
F12	VSSIO USB_11	VSS_30
F14	VSSIO USB_12	VSS_31
F16	VSSIO USB_13	VSS_32
G11	VSSIO USB_14	VSS_33
G13	VSSIO USB_15	VSS_34
F18	VSSIO USB_16	VSS_35
D9	VSSIO USB_17	VSS_36
H12	VSSIO USB_18	VSS_37
H14	VSSIO USB_19	VSS_38
H16	VSSIO USB_20	VSS_39
J11	VSSIO USB_21	VSS_40
K12	VSSIO USB_22	VSS_41
K14	VSSIO USB_23	VSS_42
K16	VSSIO USB_24	VSS_43
K18	VSSIO USB_25	VSS_44
H19	VSSIO USB_26	VSS_45
Y4	EFUSE	VSS_46
D4	VSSAN_HWM	VSS_47
M19	VSSXL	VSS_48
P21	VSSIO_PCIECLK_1	VSS_49
P20	VSSIO_PCIECLK_2	VSS_50
M22	VSSIO_PCIECLK_3	VSS_51
M24	VSSIO_PCIECLK_4	VSS_52
M26	VSSIO_PCIECLK_5	VSS_53
P22	VSSIO_PCIECLK_6	VSS_54
P24	VSSIO_PCIECLK_7	VSS_55
P26	VSSIO_PCIECLK_8	VSS_56
T20	VSSIO_PCIECLK_9	VSS_57
T22	VSSIO_PCIECLK_10	VSS_58
T24	VSSIO_PCIECLK_11	VSS_59
V20	VSSIO_PCIECLK_12	VSS_60
J23	VSSIO_PCIECLK_13	VSS_61
H23	VSSIO_PCIECLK_14	VSS_62
H26	VSSIO_PCIECLK_15	VSS_63
AA21	VSSIO_PCIECLK_16	VSS_64
AA23	VSSIO_PCIECLK_17	VSS_65
AA25	VSSIO_PCIECLK_18	VSS_66
AA27	VSSIO_PCIECLK_19	VSS_67
AA29	VSSIO_PCIECLK_20	VSS_68
AA31	VSSIO_PCIECLK_21	VSS_69
AA33	VSSIO_PCIECLK_22	VSS_70
AA35	VSSIO_PCIECLK_23	VSS_71
AA37	VSSIO_PCIECLK_24	VSS_72
AA39	VSSIO_PCIECLK_25	VSS_73
AA41	VSSIO_PCIECLK_26	VSS_74
AA43	VSSIO_PCIECLK_27	VSS_75

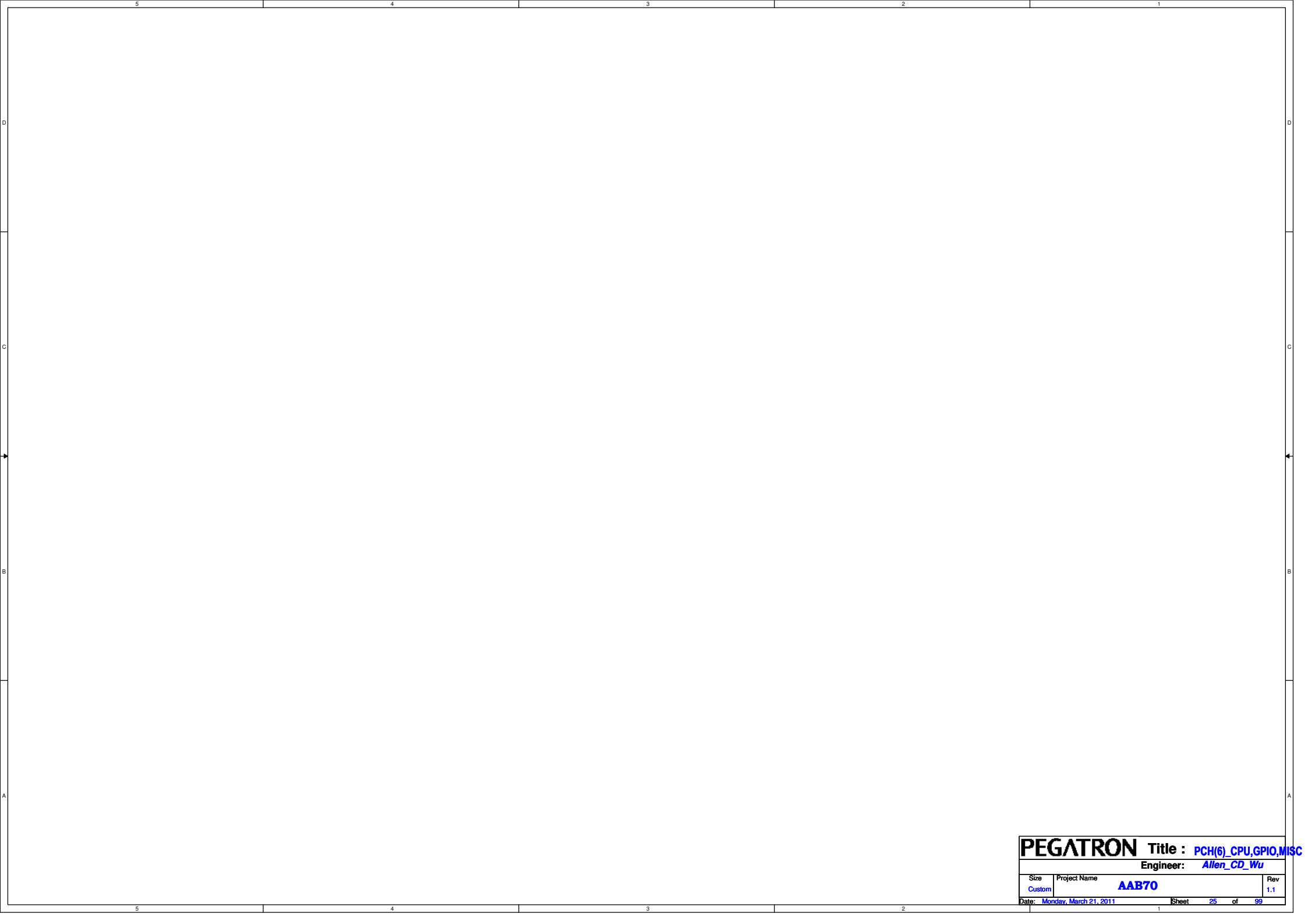
Strap Pins



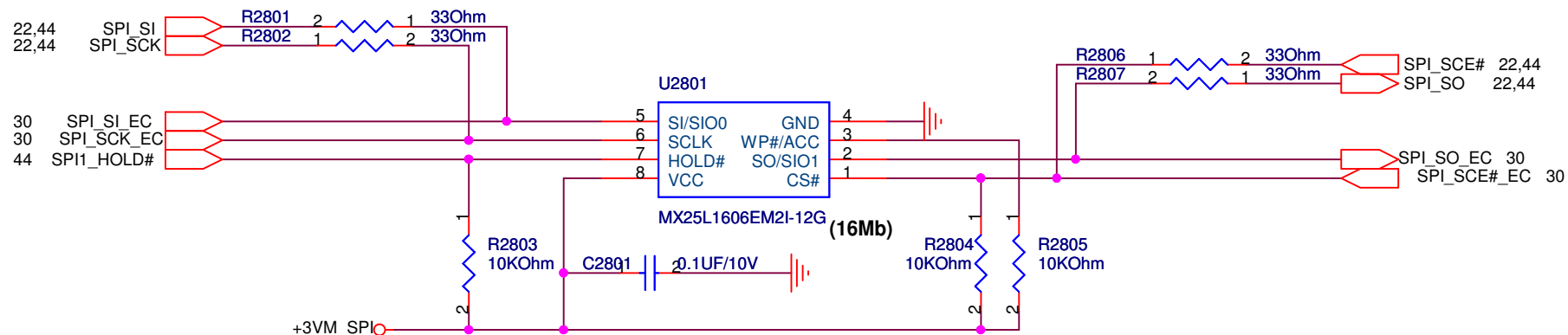
	ACZ_SDOUT_AUD	PCICLK1	PCICLK2	PCICLK3	PCICLK4	LPCCLK0 CLK_KBCPCI	LPCCLK1	EC_PWM2	EC_PWM3	
High	low power mode	PCIE Gen2	watchdog timer enable	debug	no-Fusion clock mode	EC enable	clock gen. enable	H	L	LPC ROM
Low	performance mode	PCIE Gen1	watchdog timer disable	ignore debug	Fusion clock mode	EC disable	clock gen. disable	L	H	SPI ROM

Debug Straps

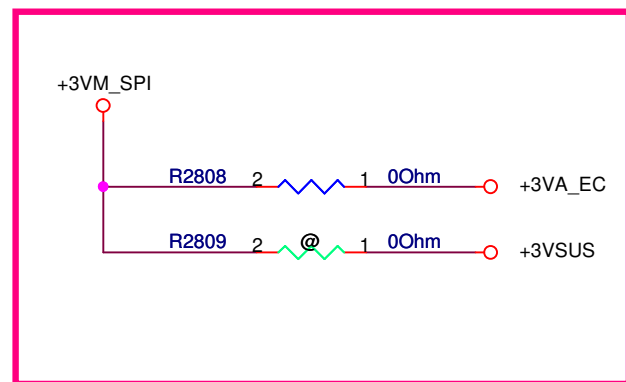
	AD23	AD24	AD25	AD26	AD27
High	disable PCI mem boot	default PCIE straps	use FC PLL	disable ILA autorun	use PCI PLL
Low	enable PCI mem boot	EEPROM PCIE straps	bypass FC PLL	enable ILA autorun	by pass PCI PLL



PEGATRON		Title : PCH(6)_CPU,GPIO,MISC	
		Engineer: Allen_CD_Wu	
Size	Project Name	Rev	
Custom	AAB70	1.1	
Date: Monday, March 21, 2011		Sheet	25 of 99



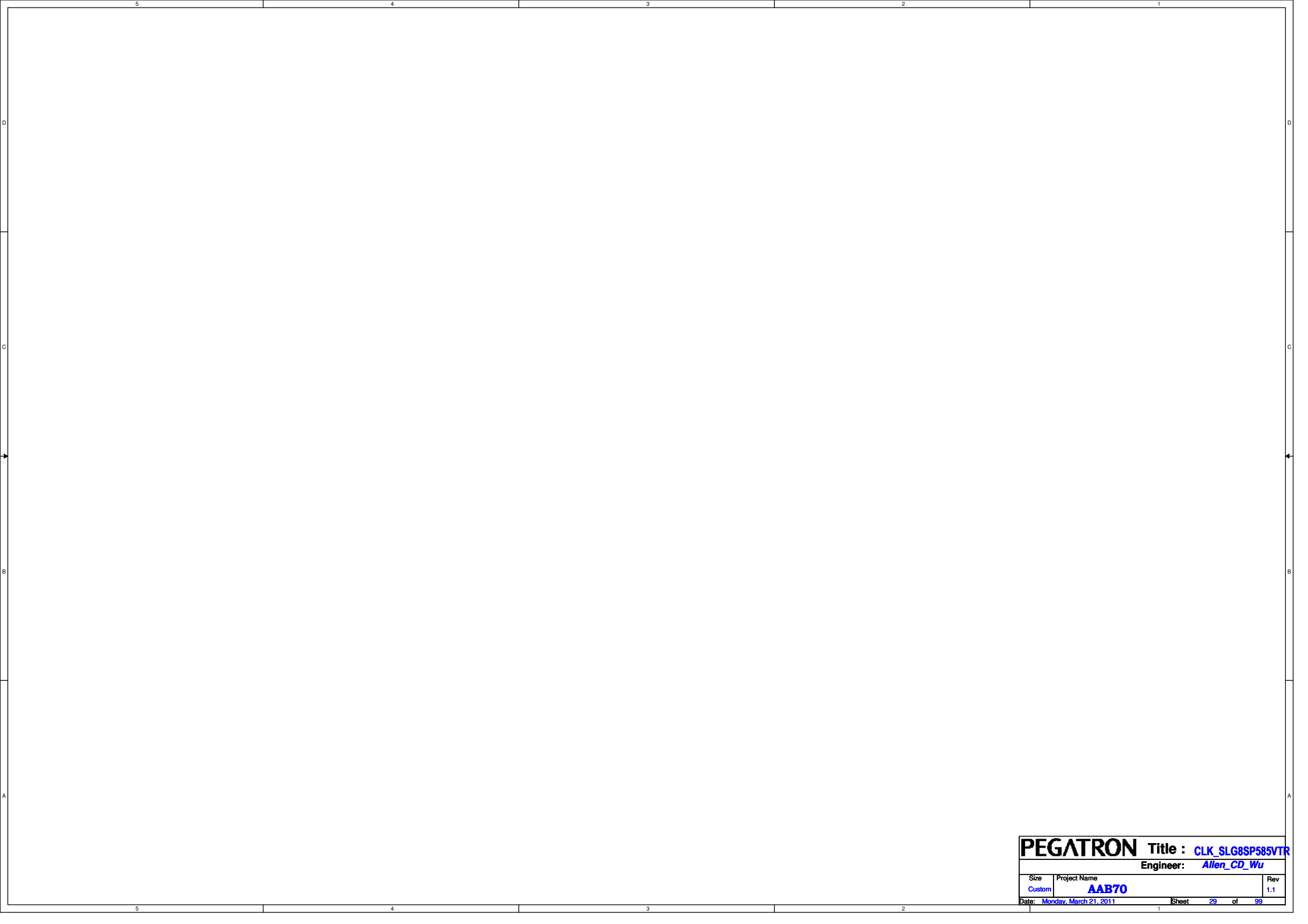
1110



WINBOND: 0500-00P4000
MXIC: 0500-00TY000

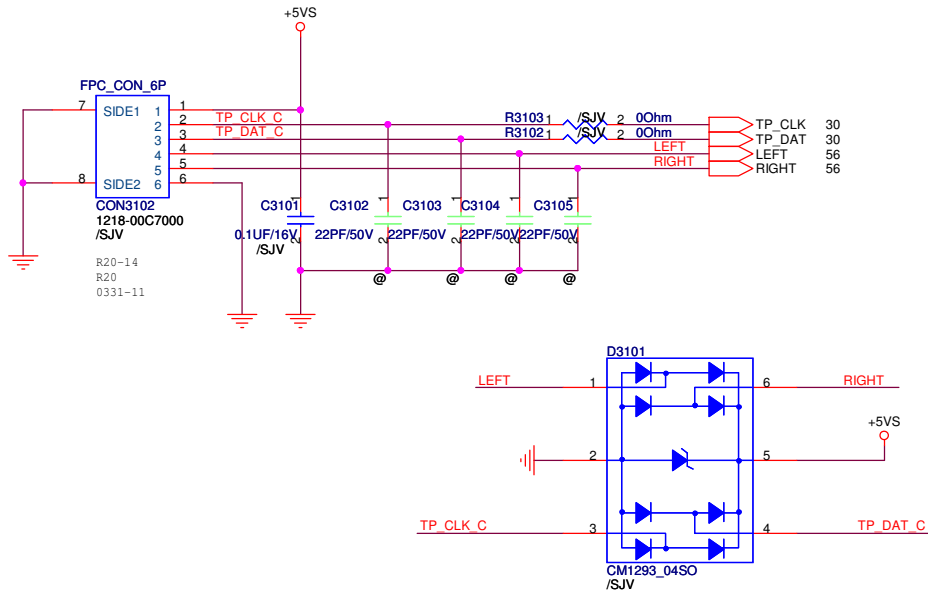
reserved for BIOS testing

PEGATRON		Title : SPI ROM	
		Engineer: Allen_CD_Wu	
Size A	Project Name BS_AB		Rev 1.1
Date: Thursday, April 21, 2011		Sheet	28 of 99

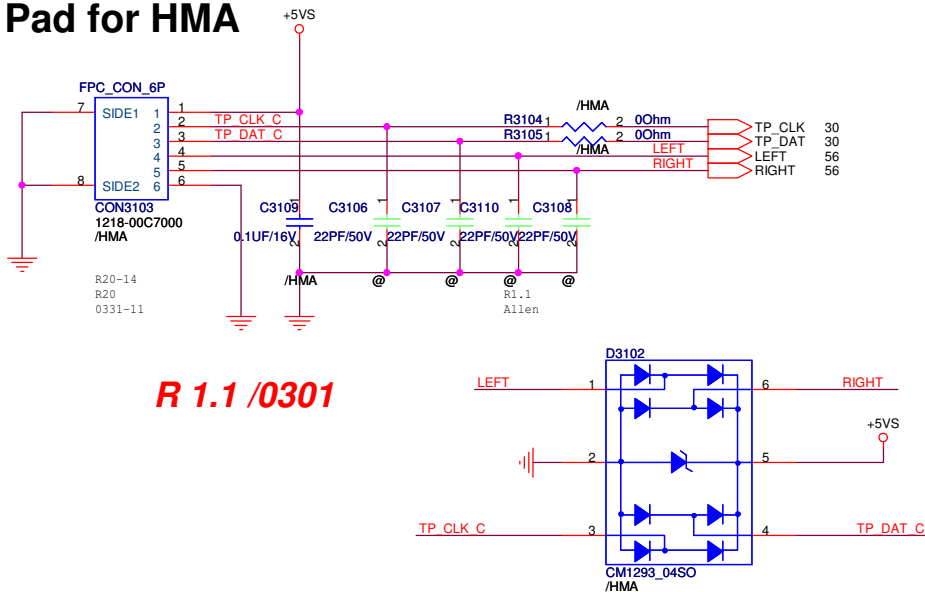


PEGATRON		Title : CLK_SLG8SP585VTR	
		Engineer: Allen_CD_Wu	
Size	Project Name		Rev
Custom	AAB70		1.1
Date: Monday, March 21, 2011		Sheet 29	of 99

Touch Pad for SJV

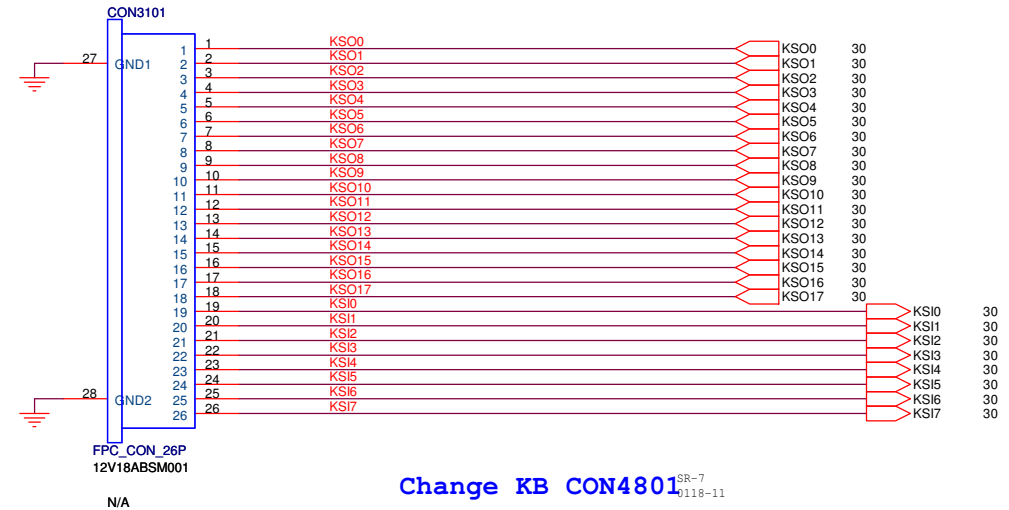


Touch Pad for HMA



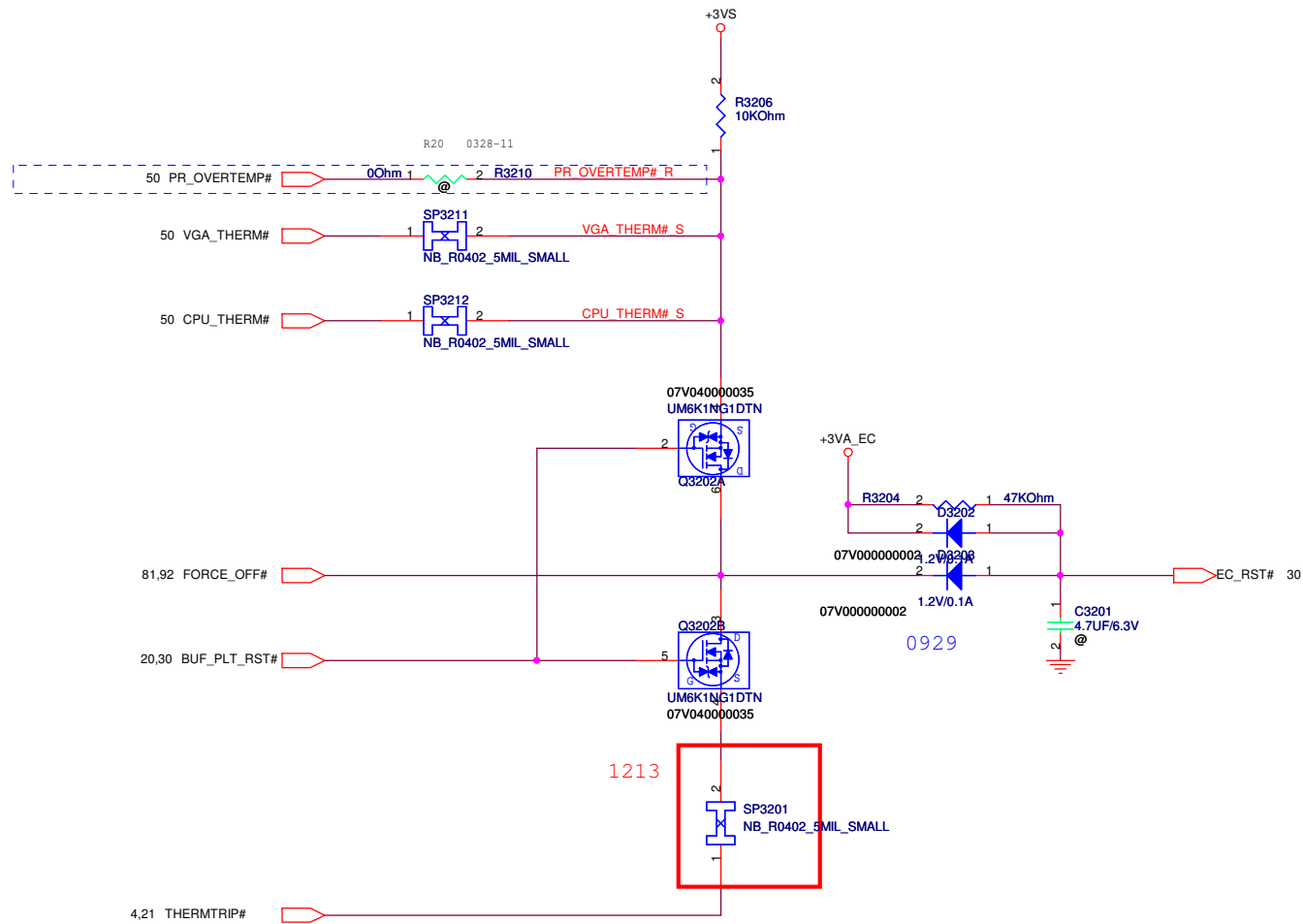
Keyboard FOR 17"

AAB70 0124

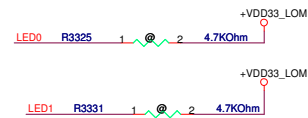


Thermal Policy

NPCE795 has internal power-on reset circuit
Use 47k ohm to make sure that raising time of POR is less than 10us



PEGATRON		Title : RST_Reset Circuit	
		Engineer: Allen_CD_Wu	
Size B	Project Name AAB70		Rev 1.1
Date: Thursday, April 21, 2011		Sheet	32 of 99

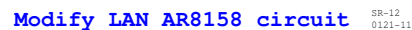


Modify H/W strap setting

SR-41
0125-11

Close to PIN2
within 400 mil

Modify R3311 as VP



SR-12
0121-11

Change U3301 to AR8158 Part and remover SM BUS^{SR-32}
0125-11

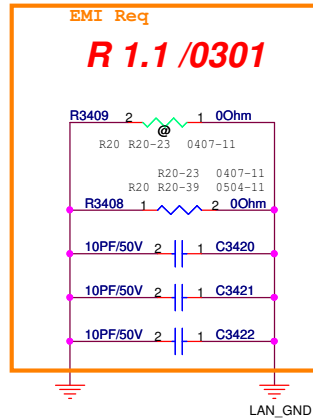
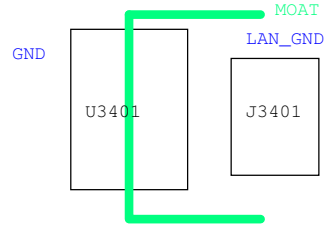
JS SR-32
0125-11

R 1.1 /0308 L3403/L3302 change to PB201209T-152-N

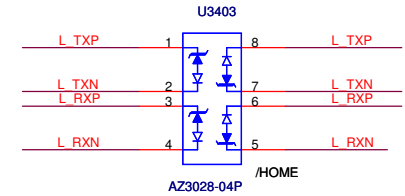
R 1.1 /0308

D3401
AZ2025-01H.R7G

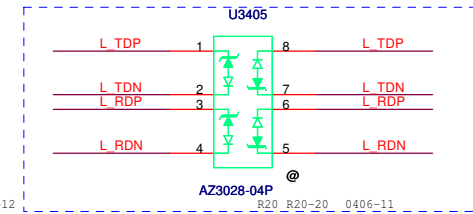
LAN layout note:



**Change RJ45 CON3401
0301
1223-0002000
R 1.1 /0301**



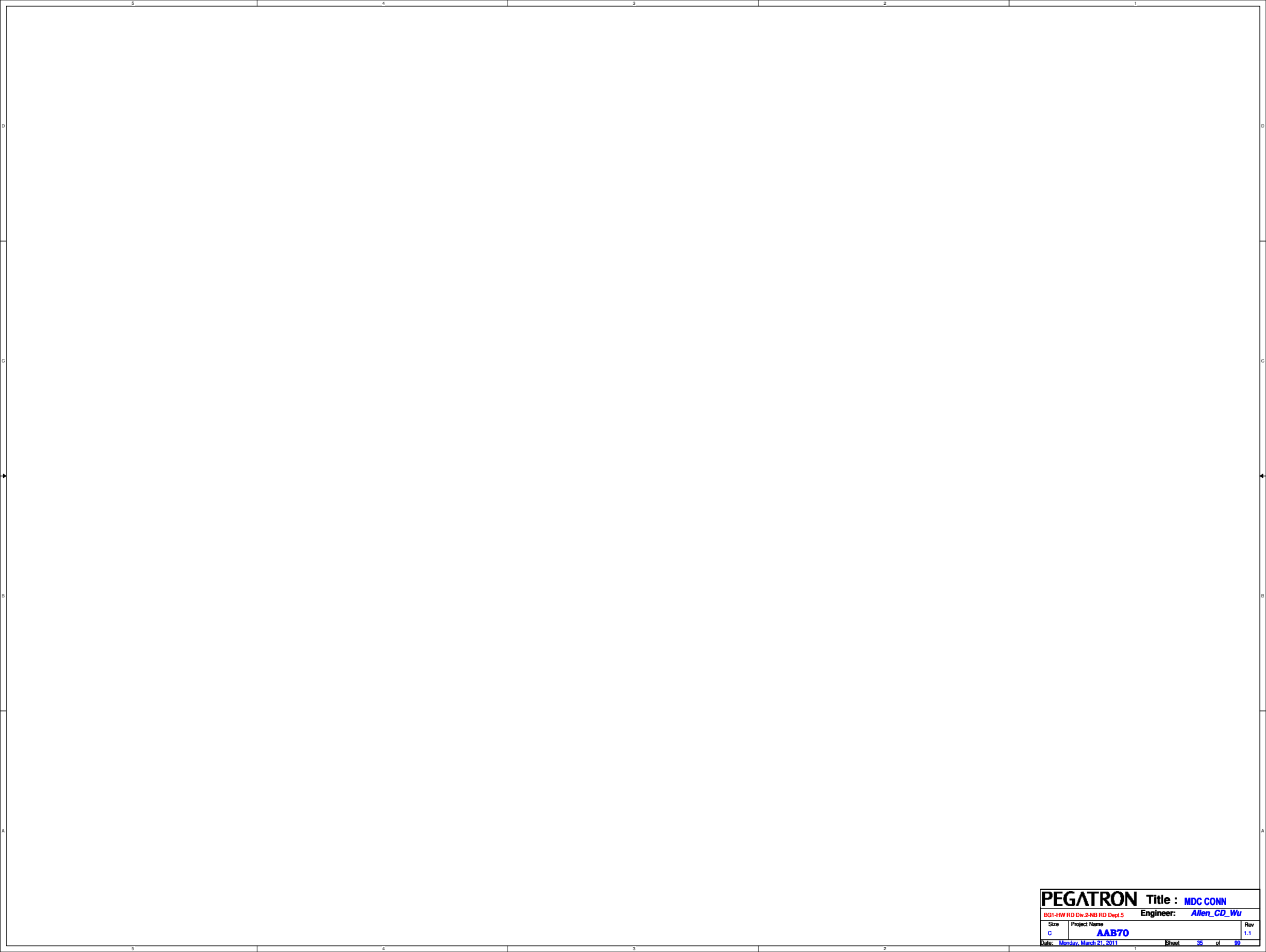
Modify LAN ESD circuit



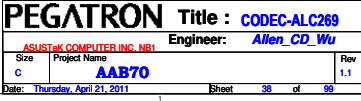
Modify LAN AR8158 circuit

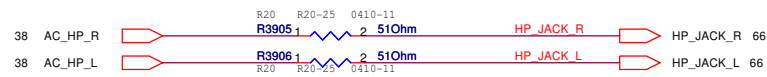
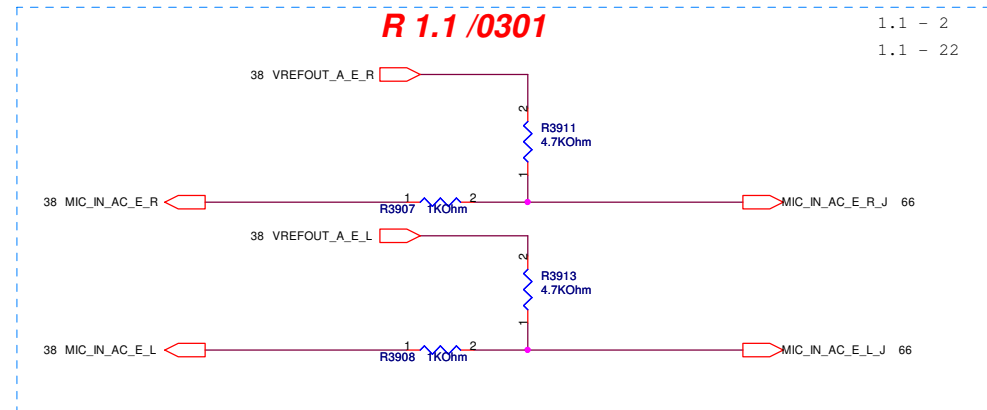
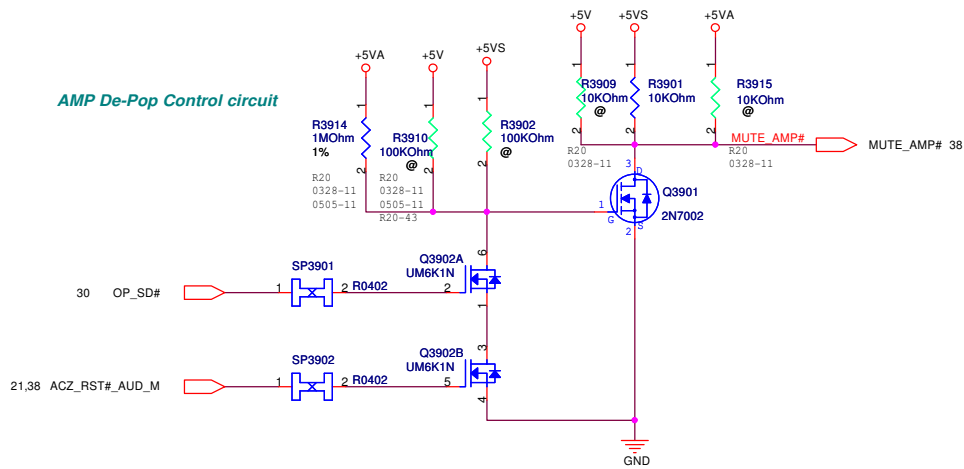
Modify Transformer circuit

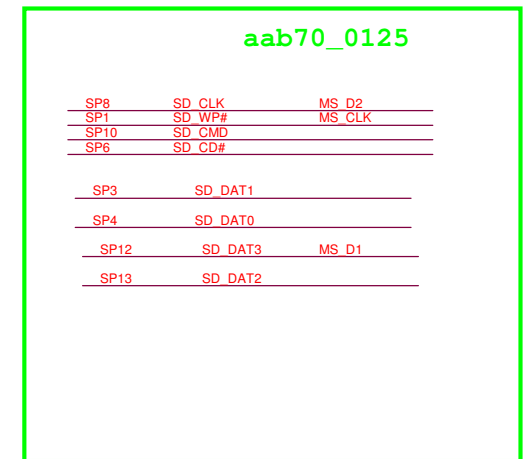
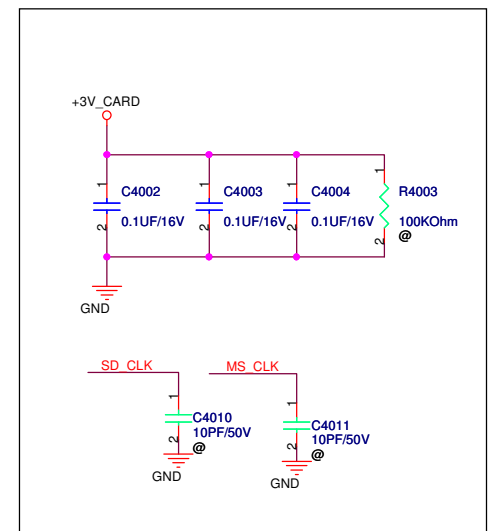
PEGATRON			Title :R.J45
BG1-HW RD Div.2-NB RD Dept.5			Engineer: Allen_CD_Wu
Size B	Project Name AAB70	Rev 1.1	
Date: Wednesday, May 04, 2011		Sheet	34 of 99



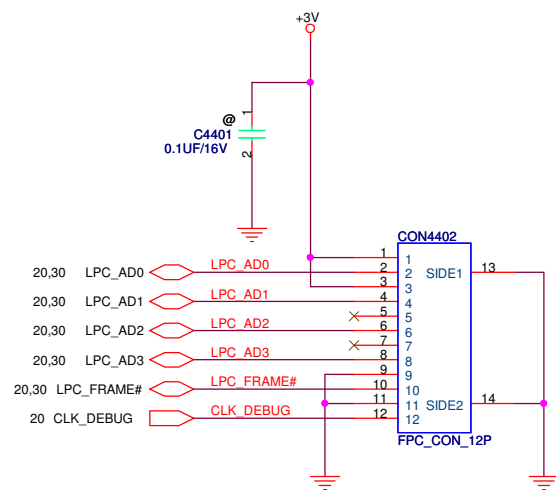
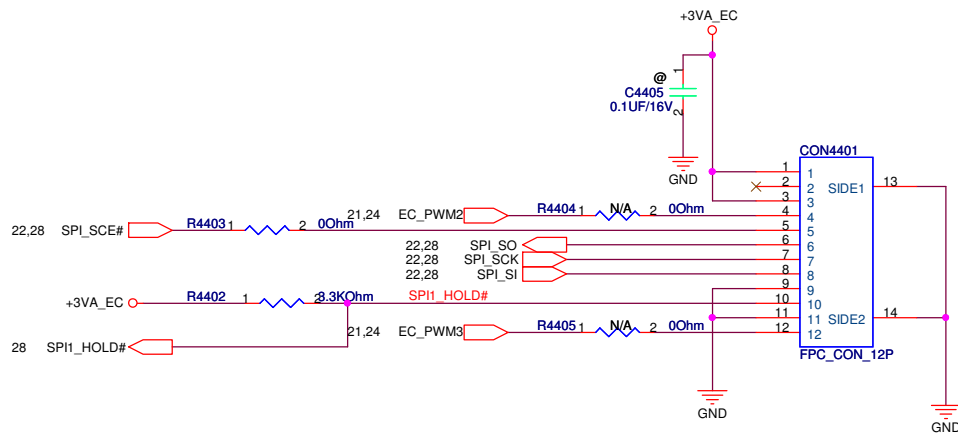
PEGATRON		Title : MDC CONN	
BG1-HW RD Dw.2-NB RD Dept.5		Engineer: Allen_CD_Wu	
Size C	Project Name AAB70	Rev 1.1	
Date: Monday, March 21, 2011		Sheet	35 of 99



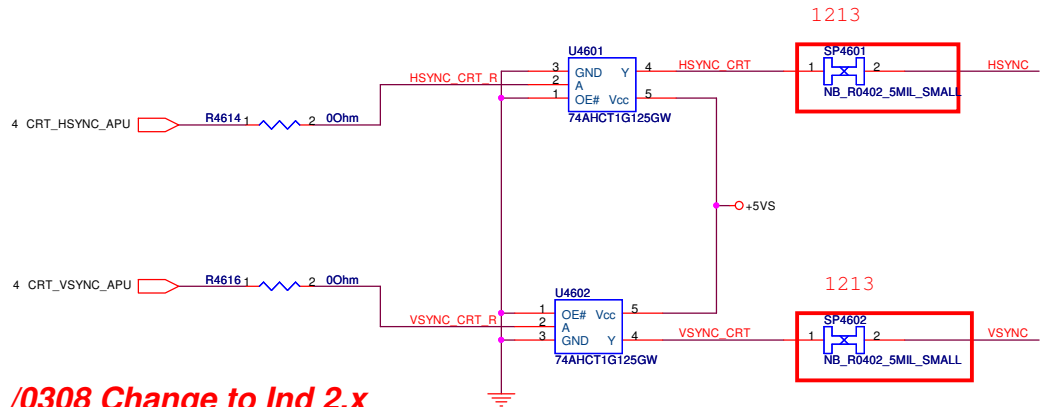
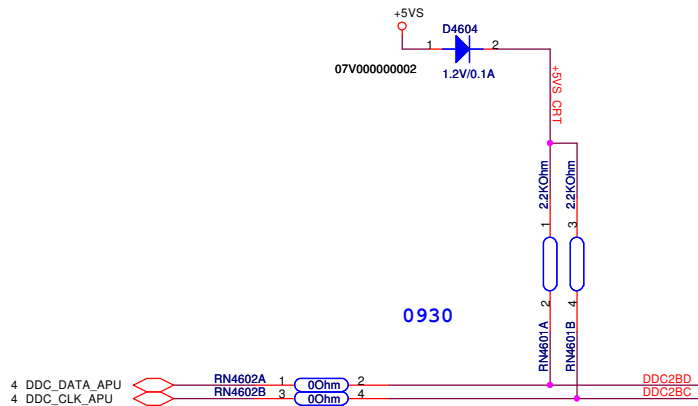




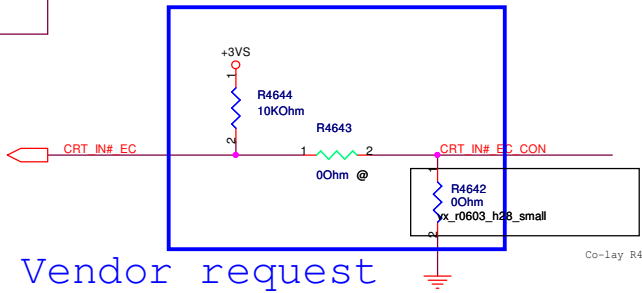
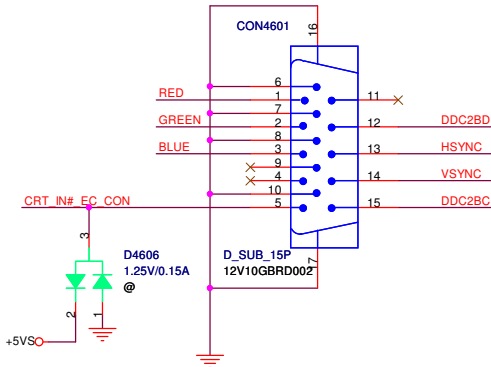
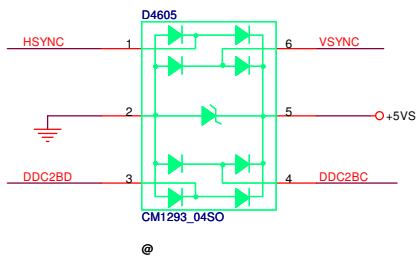
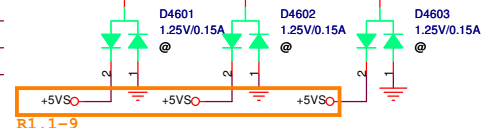
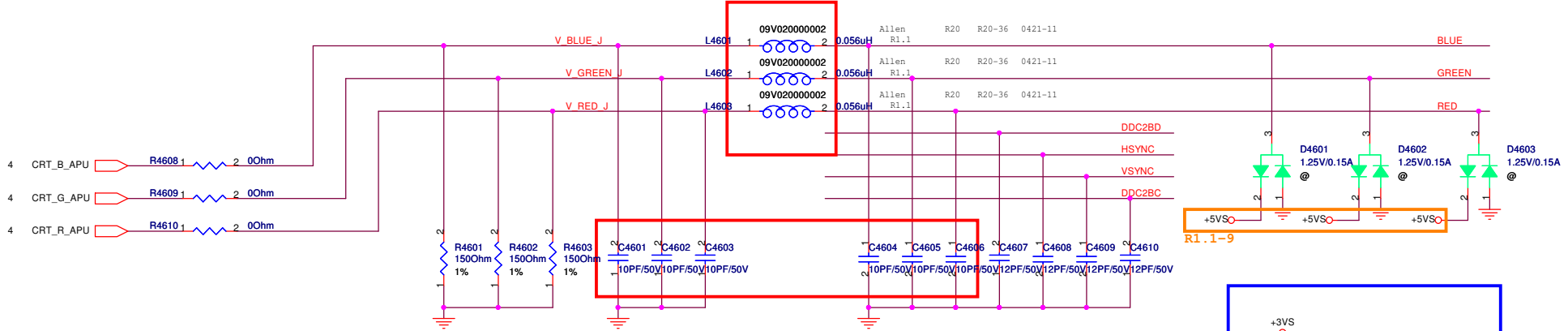
PEGATRON CORPORATION		Engineer:	
Size B	Project Name AAB70		Rev 1.1
Date: Thursday, April 21, 2011		Sheet 40 of 99	



PEGATRON		Title : DEBUG	
BG1/HW2		Engineer: Allen CD Wu	
Size B	Project Name AAB70	Rev 1.1	
Date: Thursday, April 21, 2011		Sheet 44 of 99	



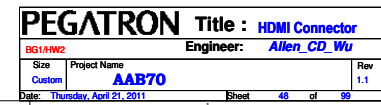
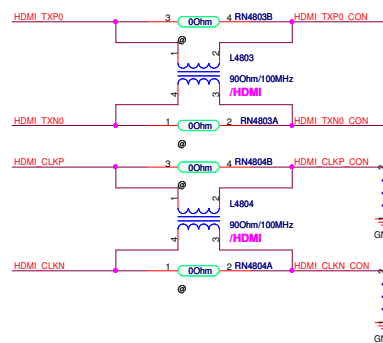
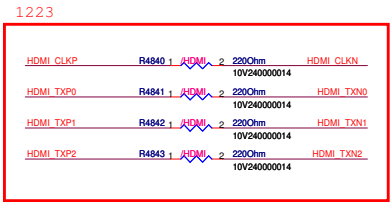
R 1.1 /0308 Change to Ind 2.x

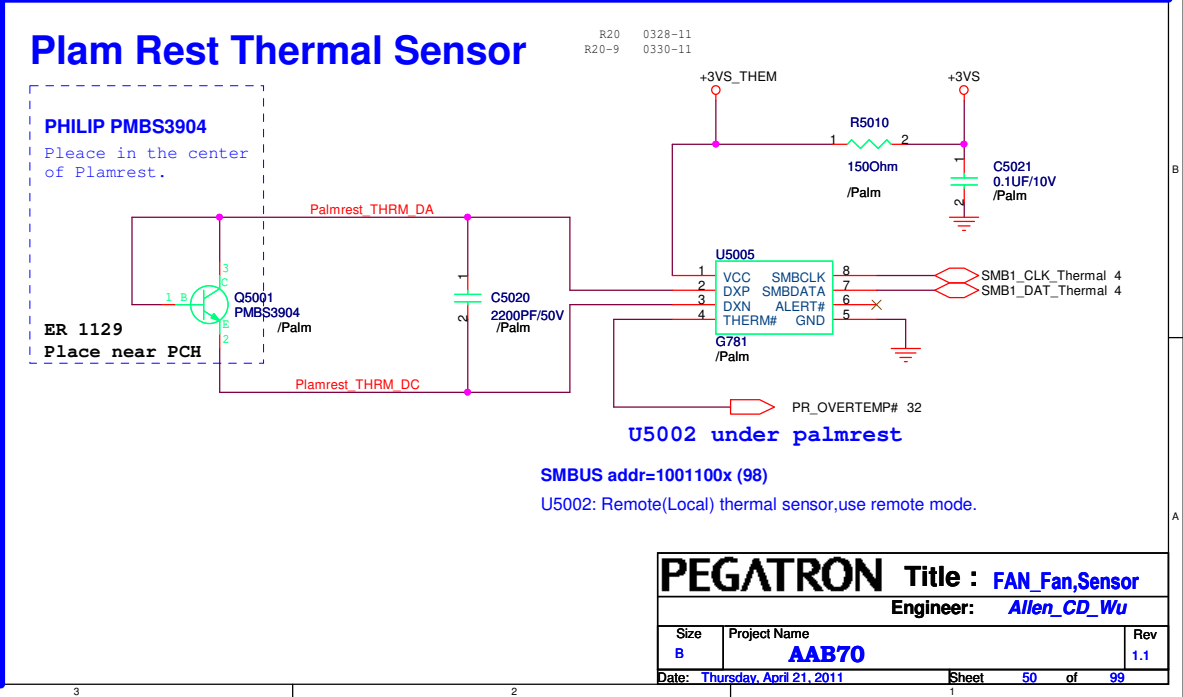
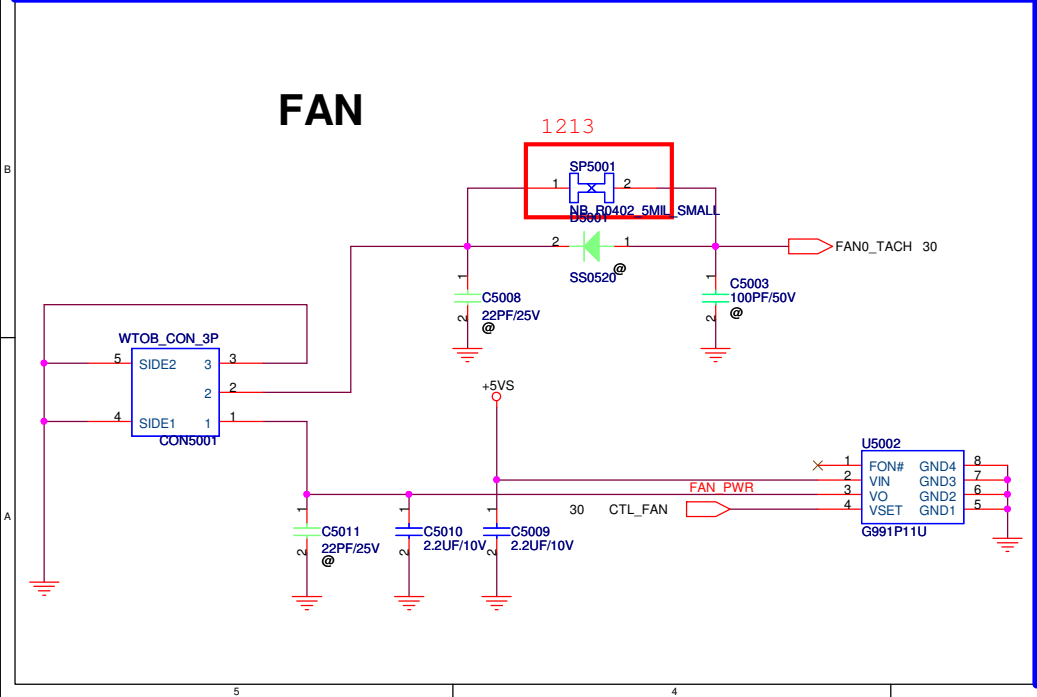
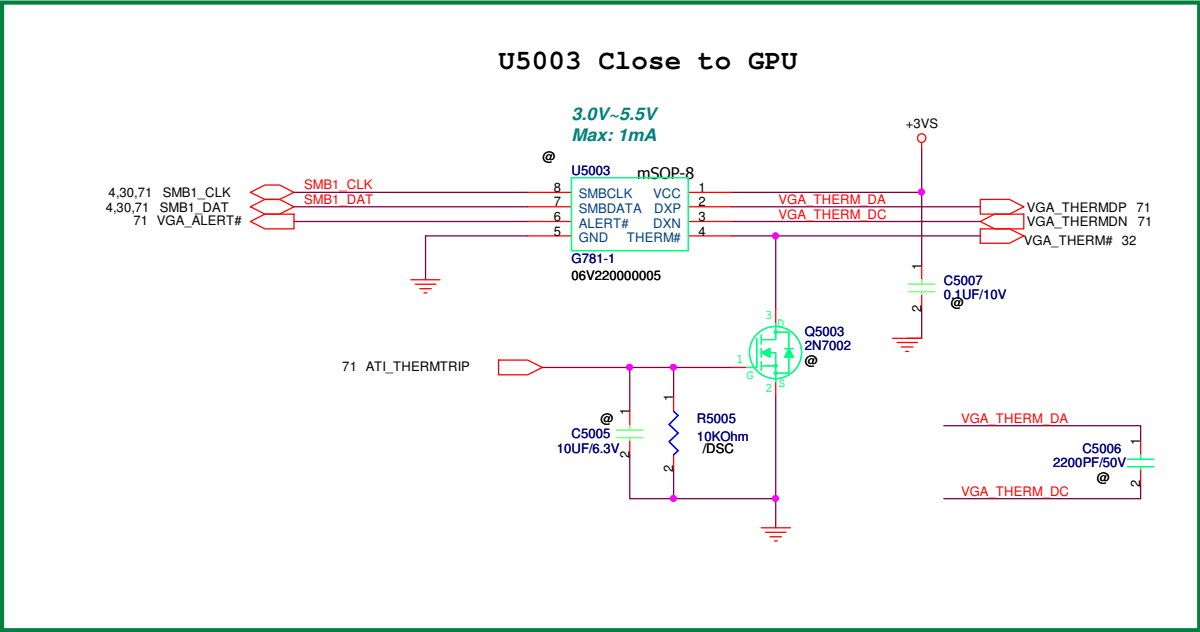
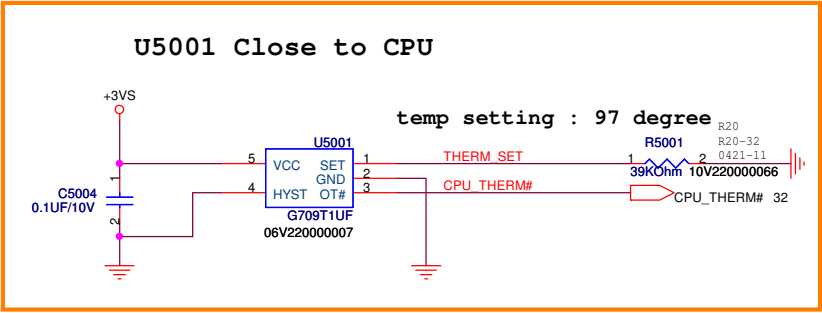


Vendor request

1210-00DY000

PEGATRON		Title : CRT	
BG1/HW2		Engineer: Allen CD Wu	
Size Custom	Project Name AAB70	Rev 1.1	
Date: Thursday, April 21, 2011		Sheet	46 of 99

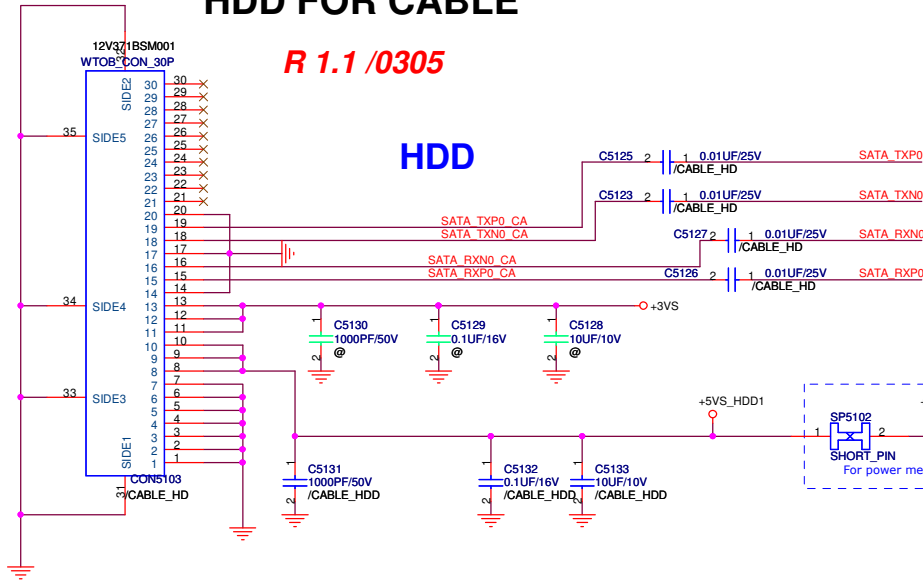




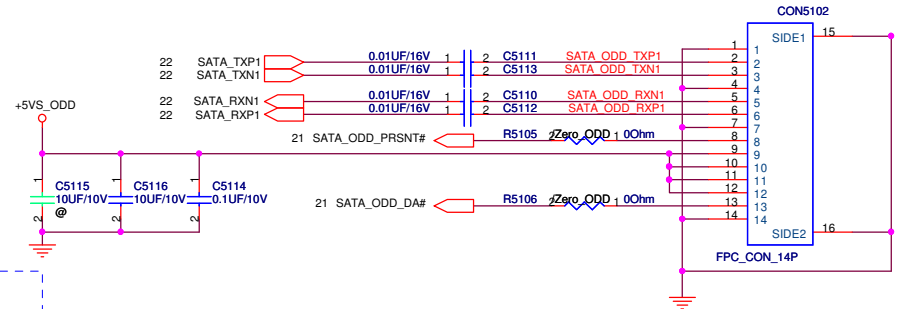
HDD FOR CABLE

R 1.1 /0305

HDD

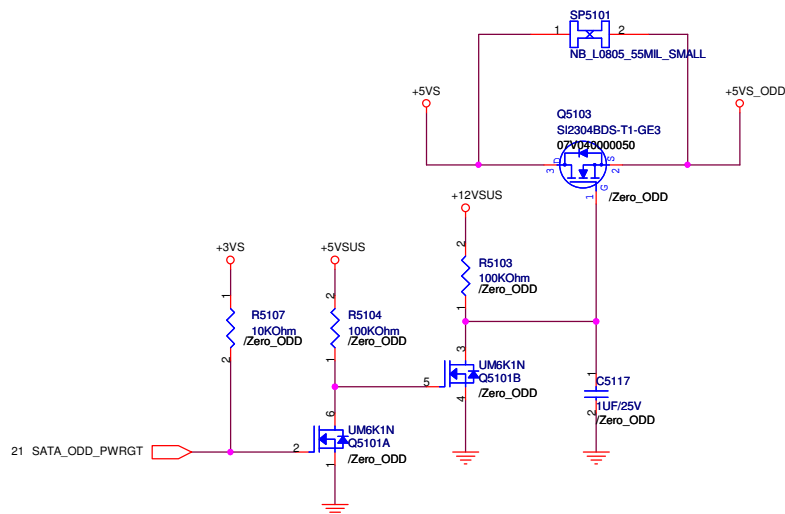


ODD FOR 17"

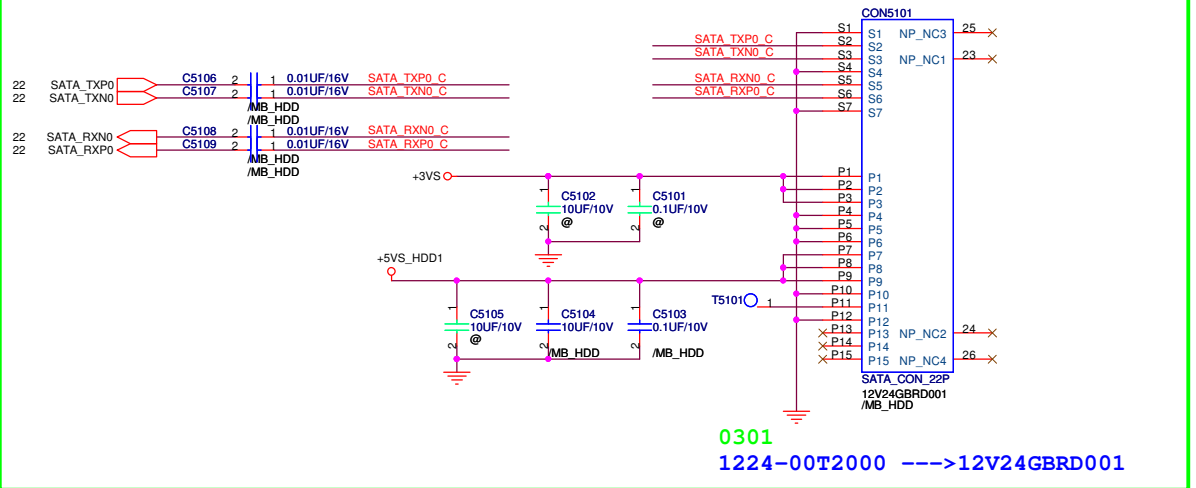


ZERO POWER ODD SUPPORT

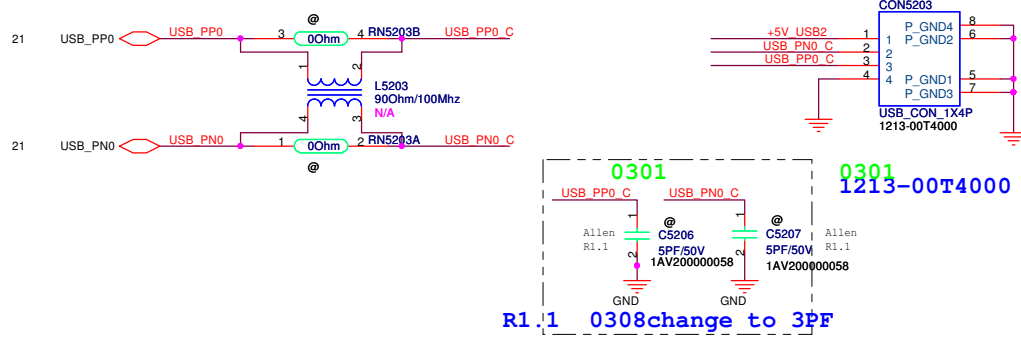
support Hokey turn off ODD power



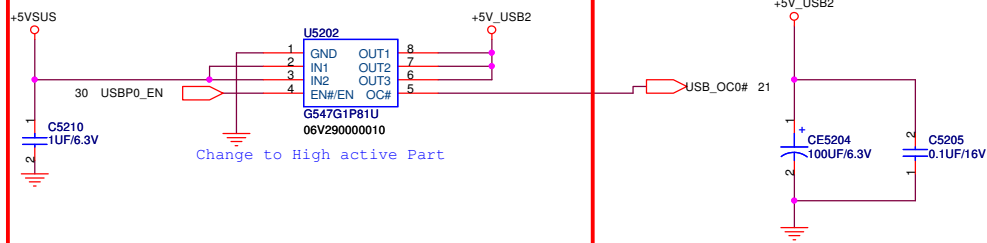
HDD 0129

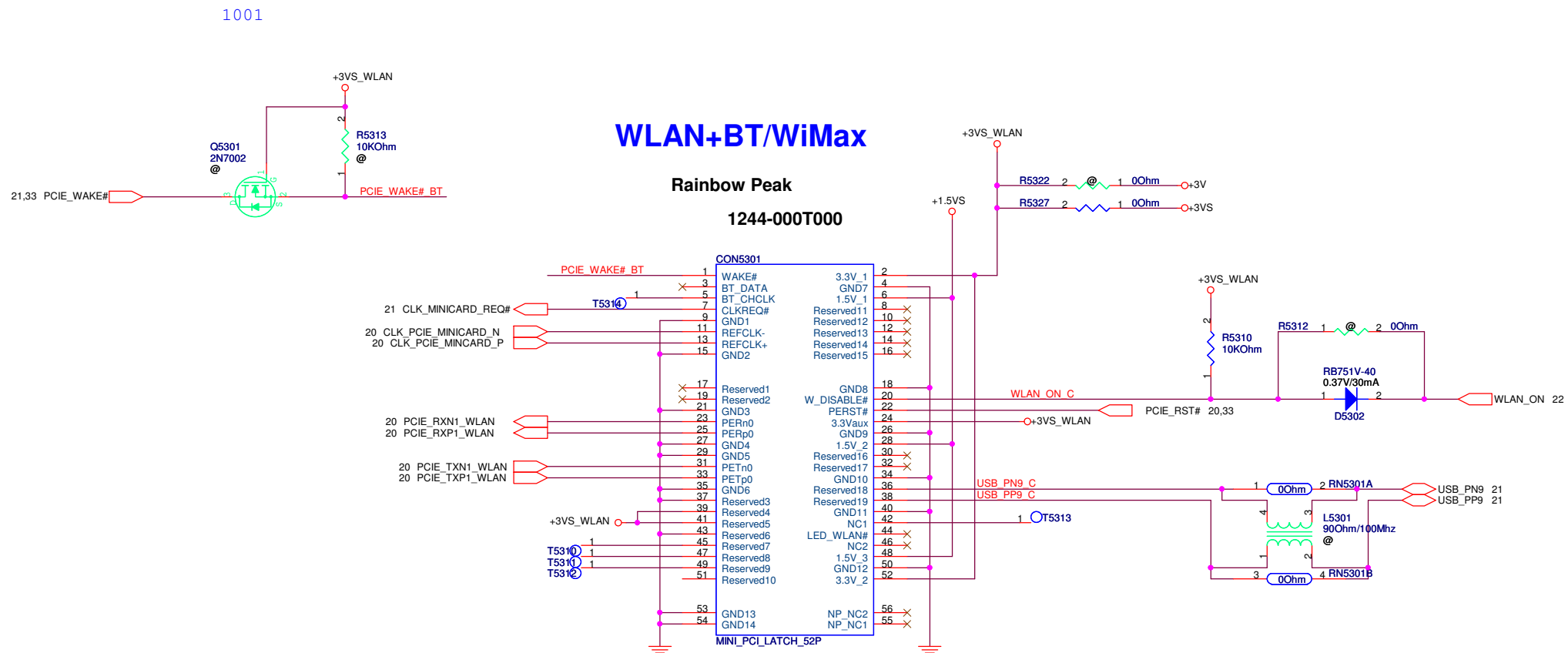


USB 2.0



AAB70



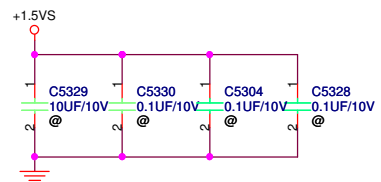


H = 6.5 mm

WLAN +1.5VS bypass capacitor:

Place 0.1uF near pin 6,28,48.

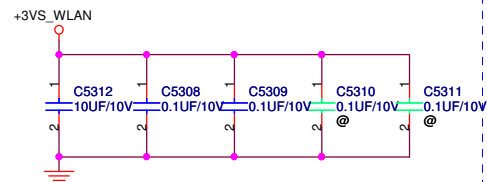
Place 10uF near +1.5VS source side.



WLAN +3VS bypass capacitor:

Place 0.1uF near pin 2,24,52,39 41.

Place 10uF near +3VS_WLAN source side.

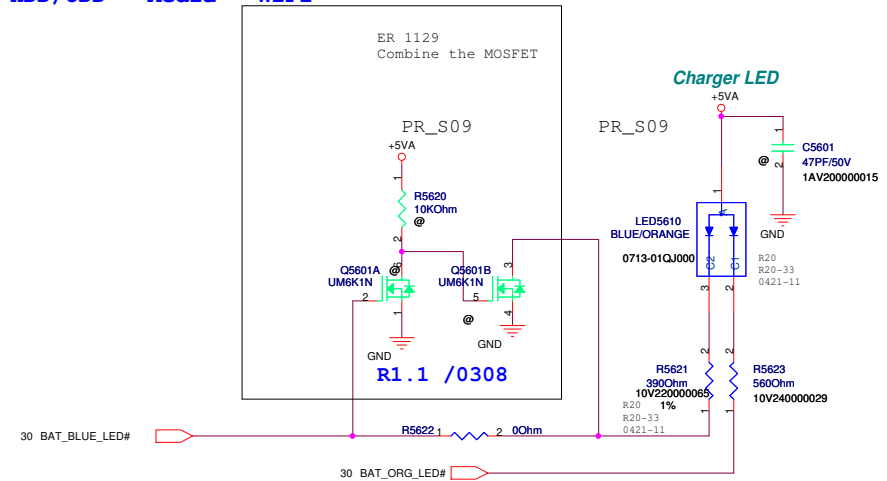


PEGATRON		Title : MINICARD Wireless	
BG1/HW2		Engineer: Allen CD Wu	
Size B	Project Name AAB70	Rev 1.1	
Date: Thursday, April 21, 2011		Sheet 53 of 99	

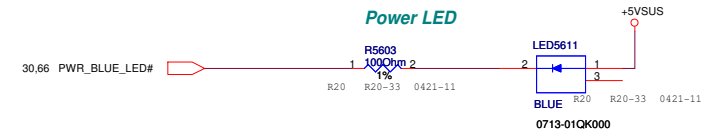


PEGATRON		Title : Mini Card HSDPA	
BG1/HW2		Engineer: Allen_CD_Wu	
Size Custom	Project Name AAB70		Rev 1.1
Date: Monday, March 21, 2011		Sheet	54 of 99

Order of Indicator LEDs
DC-IN Power Battery HDD/ODD Media WiFi



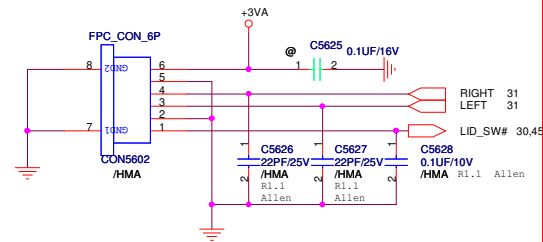
Dual Color



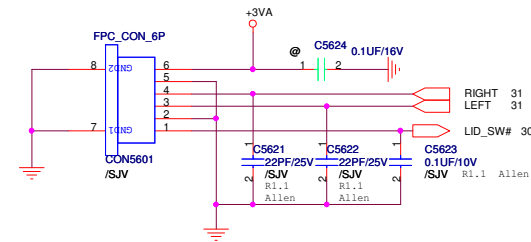
1.1

R 1.1 /0301

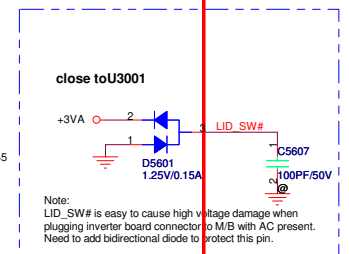
For HMA



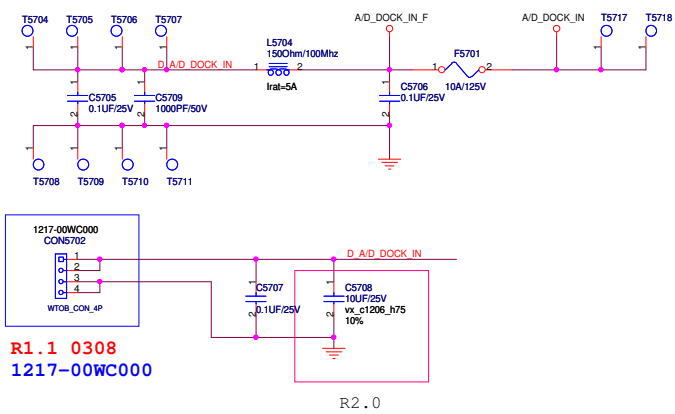
For SJV



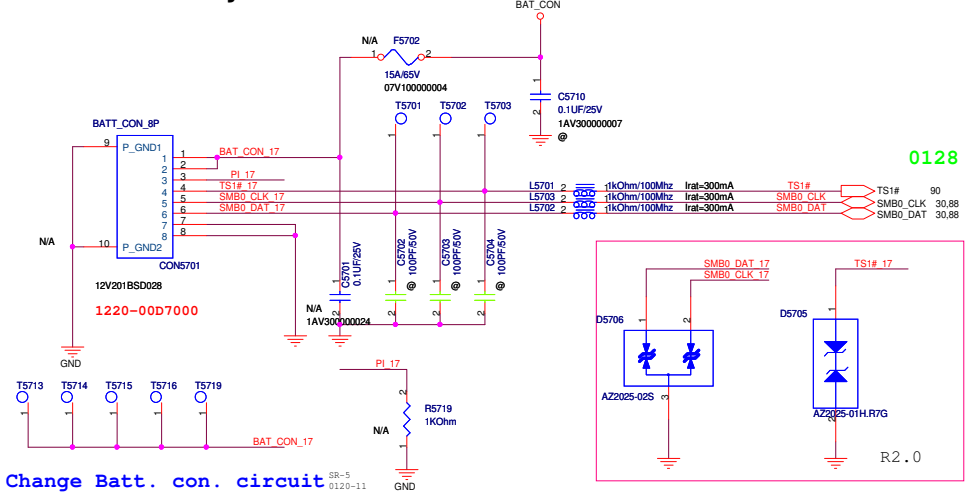
1028



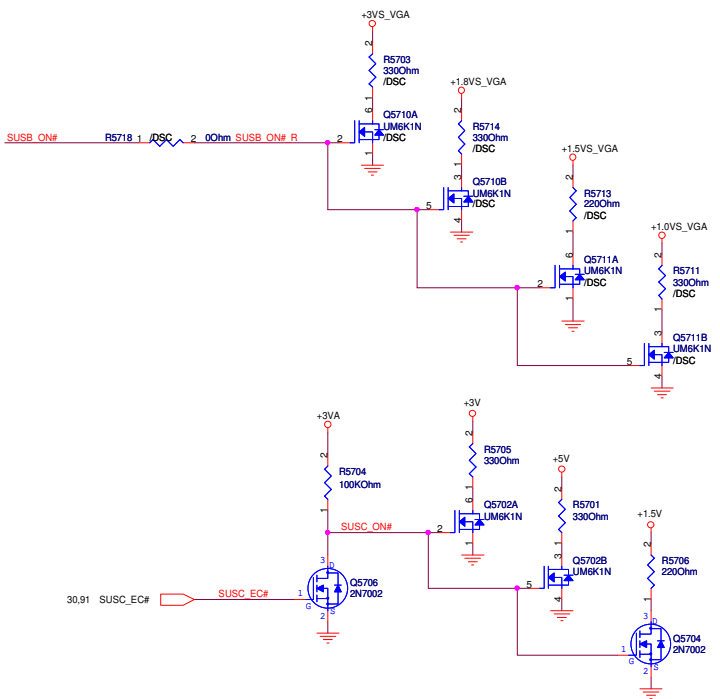
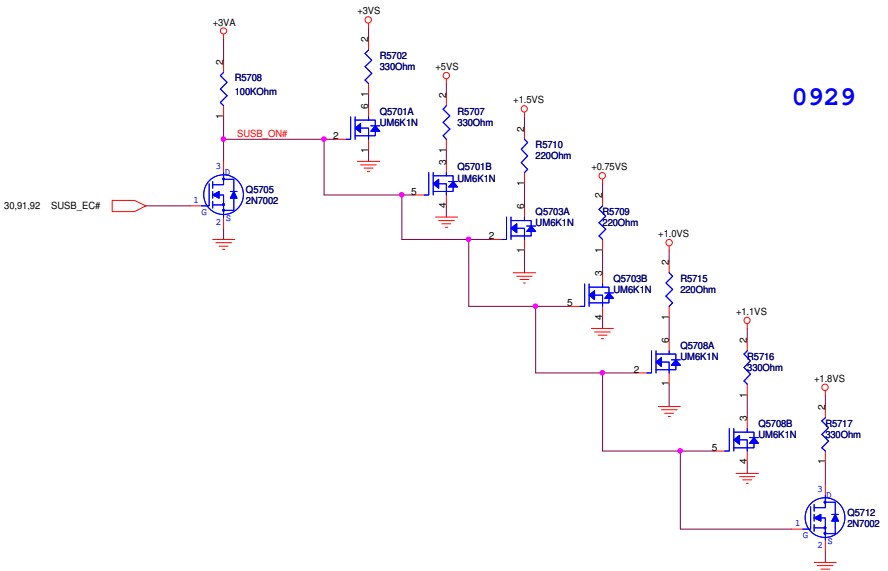
DC IN

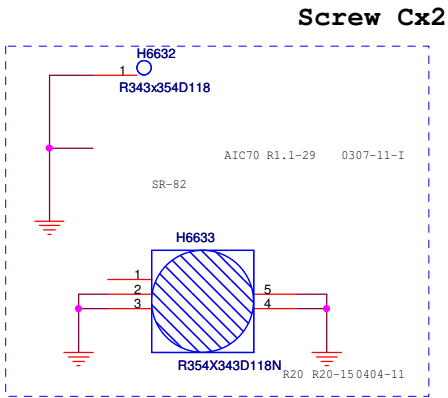
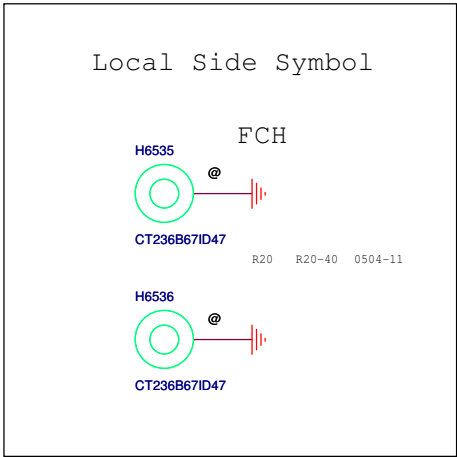
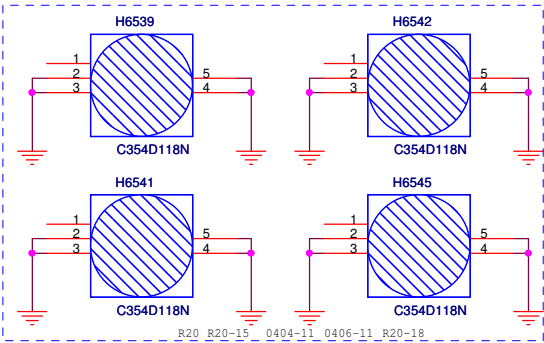
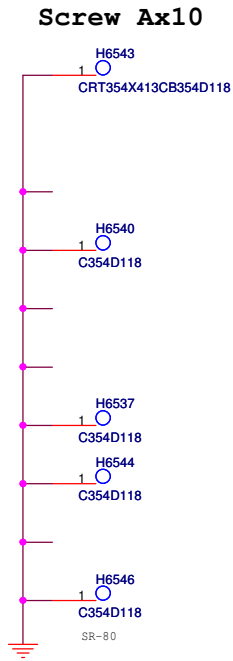
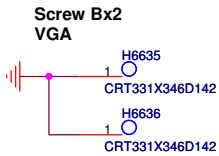
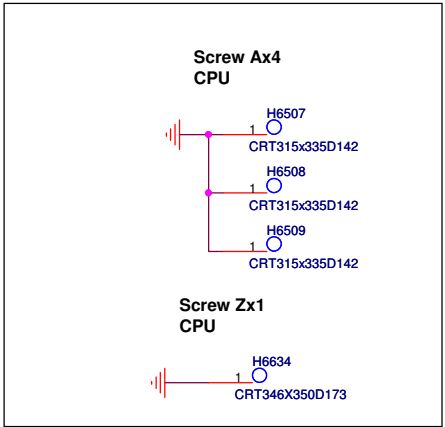
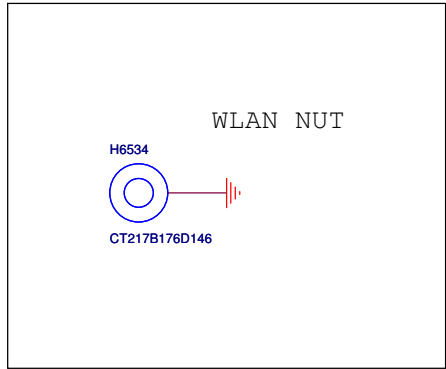


Battery Connector 17"

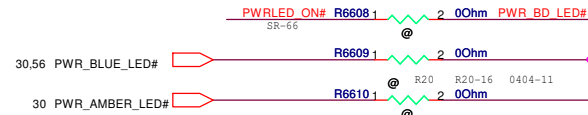
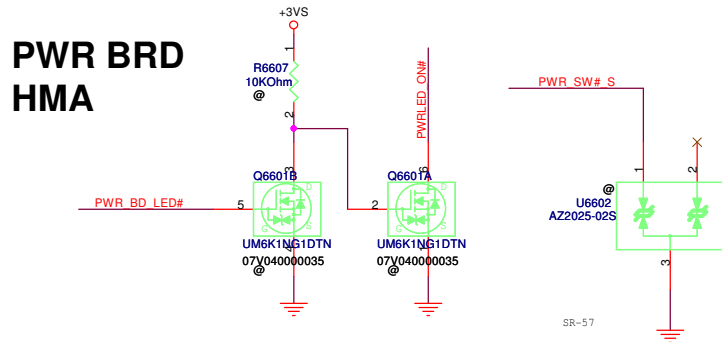


Discharge Circuit



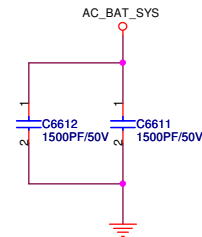


PWR BRD HMA



change PWR LED CON6603 circuit 0129

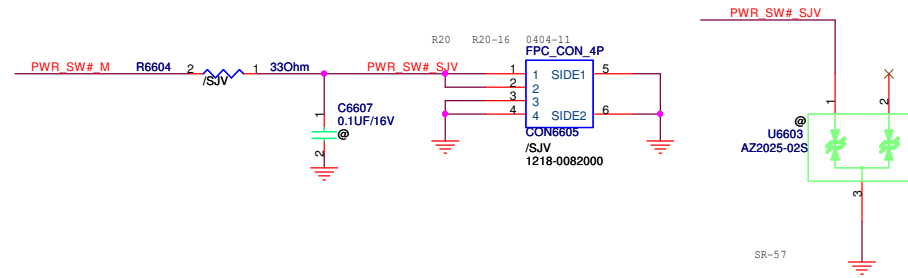
EMI



ADAPTOR VOLTAGE DETECTOR.

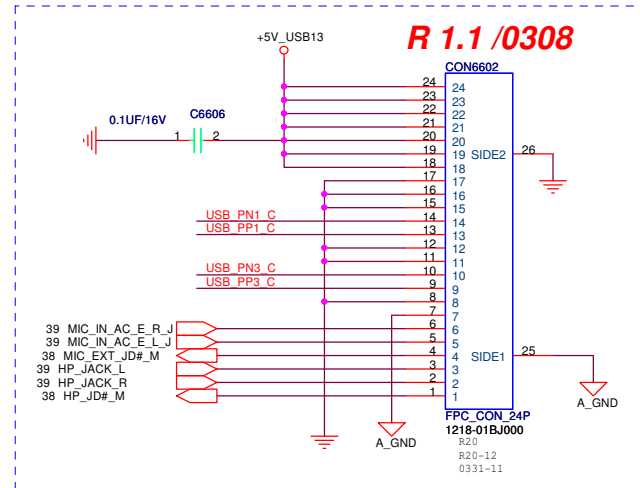
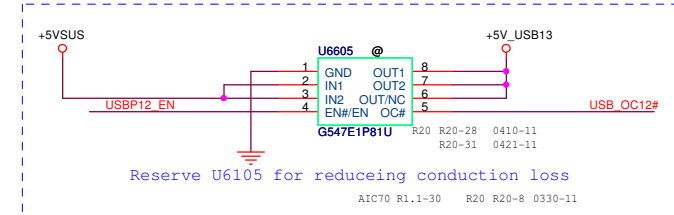
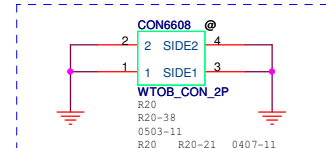
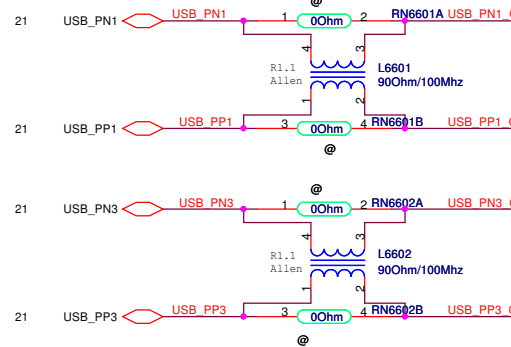
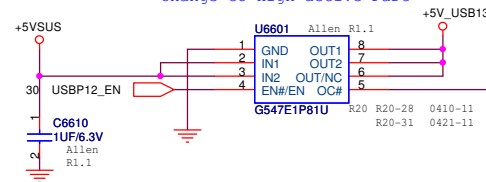
PWR SJV

R 1.1 /0301

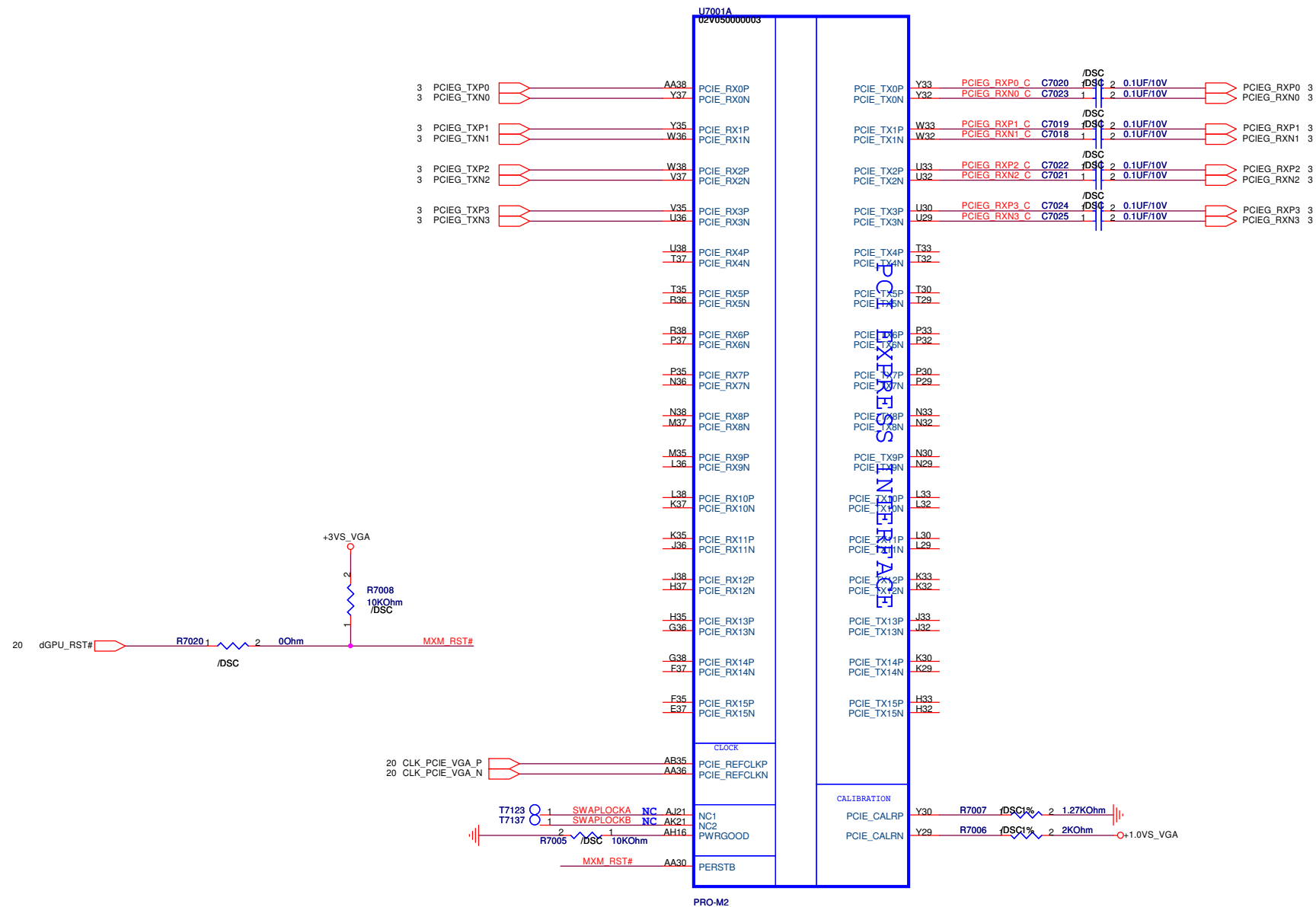


AAB70

Change to High active Part

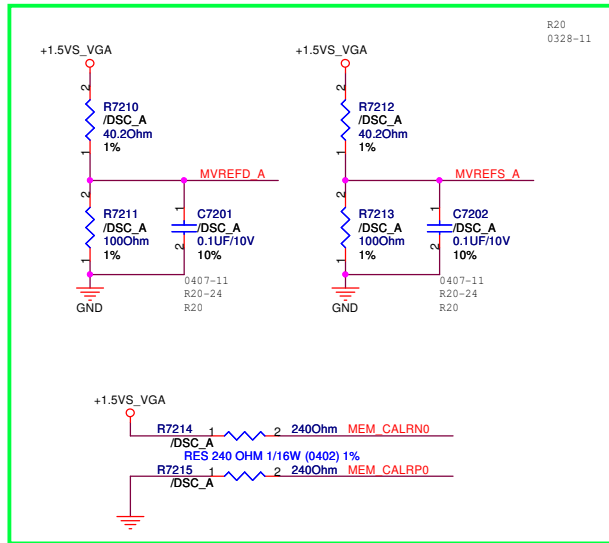


R 1.1 /0301 Seymour XT/M2

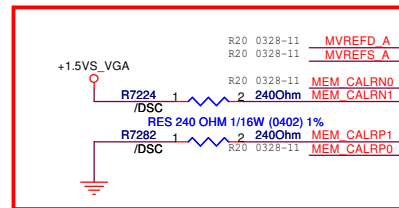


The all balls are NC except N12 /M12 for seymour

Reserve, Unmount

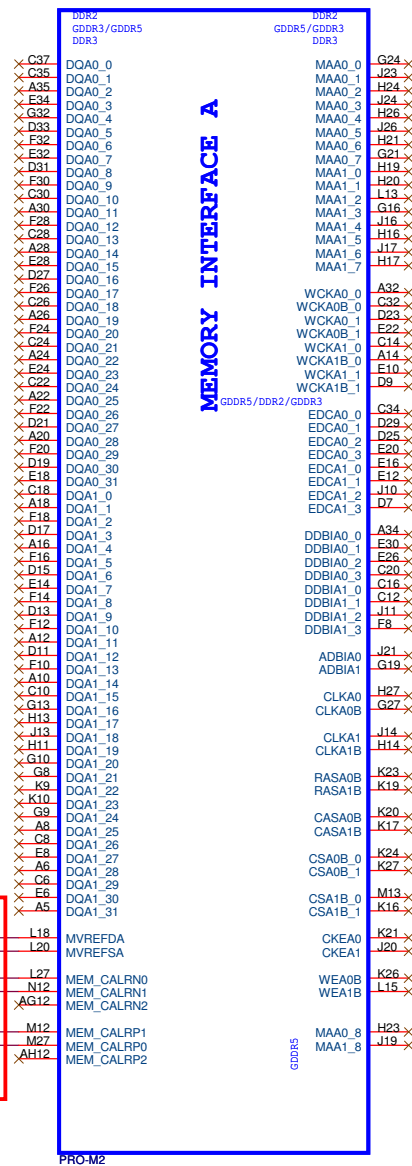


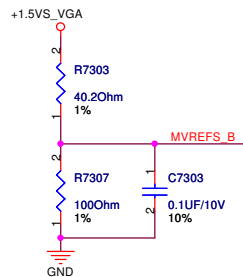
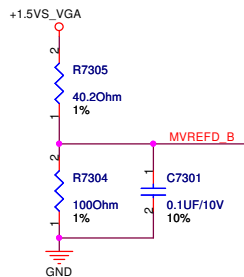
The all balls are NC except N12 /M12 for seymour



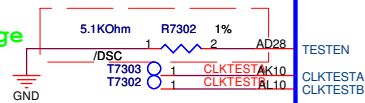
0301-change

U7001C 02V050000003





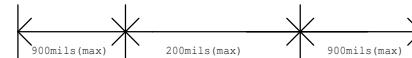
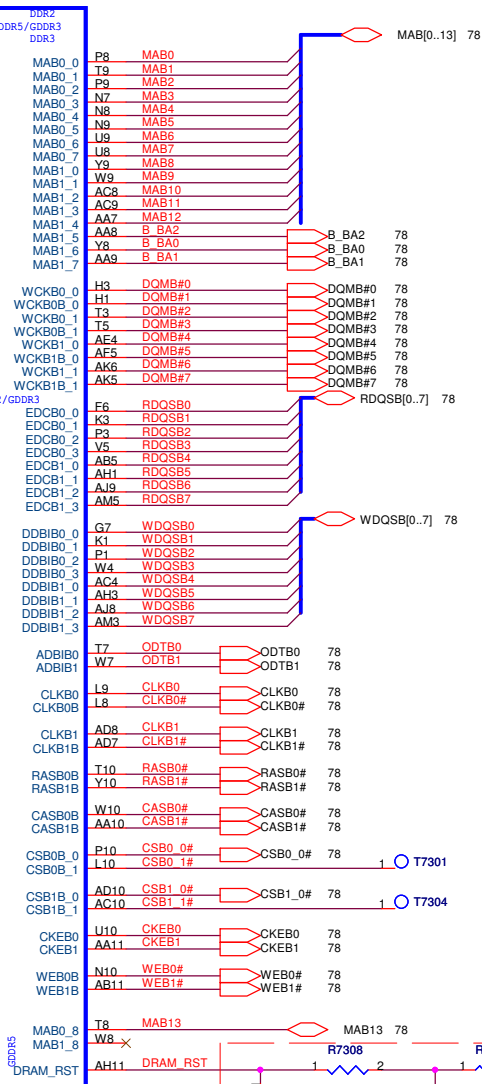
0301-change



U7001D 02V050000003

MEMORY INTERFACE B

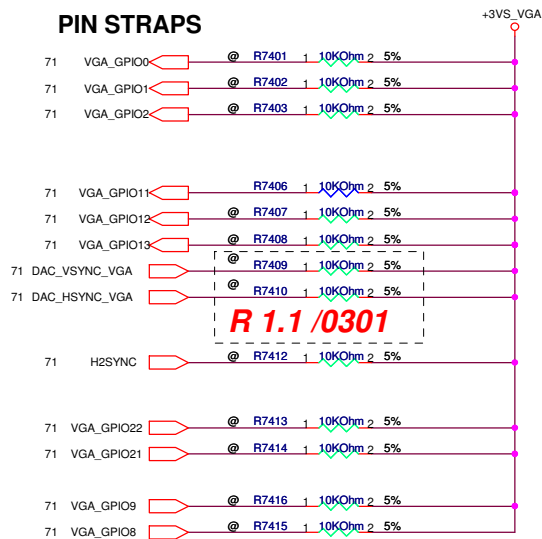
PRO-M2



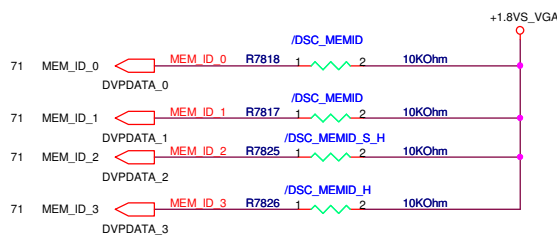
follow up checklist suggestion 0301-change

GPIO21 MUST BE LOW DURING PERSTB WHEN BEING USED TO CONTROL MVDDQ

PIN STRAPS



VRAM size define by VBIOS



Seymour Straps

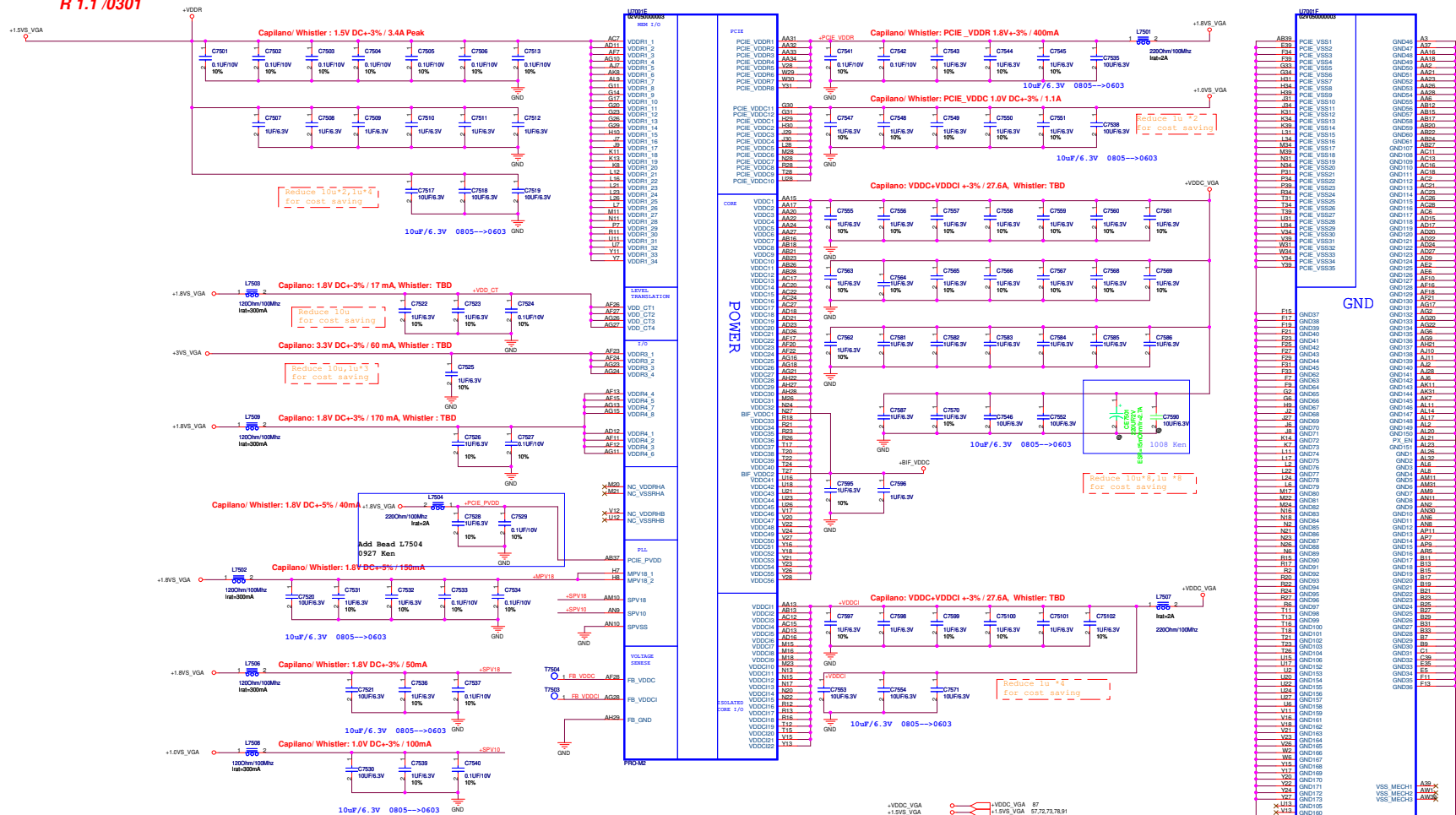
STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing <i>This setting can only be used if the PCIE bus design meets the "Low Loss interconnect" requirements.</i>	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled <i>MXM and add-in boards</i>	0 (internal pull-down)
BIF_GEN2_EN_A	GPIO2	1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on	0
VGA_DIS	GPIO9	0 - VGA Controller capacity enabled 1 - The device will not be recognized as the system's VGA controller	0 (internal pull-down)
ROMIDCFG(2:0)	GPIO(13:11)	If BIOS_ROM_EN=1, then Config[2:0] defines the ROM type. If BIOS_ROM_EN=0, then Config[2:0] defines the primary memory aperture size. 128MB---000 32MB---Not Support 2GB---Not Support 256MB---001 512MB---Not Support 4GB---Not Support 64MB---010 1GB---Not Support	0000 (internal pull-down)
BIOS_ROM_EN	GPIO22_ROMCSB	Enable external BIOS ROM device 0-Disable external BIOS ROM device 1-Enable external BIOS ROM device	0 (internal pull-down)
AUD[1:0] AUD[0]	HSYNC VSYNC	AUD[1:0]: 00: No audio function; 01: Audio for DisplayPort and HDMI if adapter is detected; 10: Audio for DisplayPort only; 11: Audio for both DisplayPort and HDMI.	0 (internal pull-down)
Reserved	GENLK_CLK GPIO_21_BB_EN GPIO8	ATI internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET.	0 (internal pull-down)

Seymour XT:

Memory ID Board Straps

Vendor	DVPDATA(3,2,1,0)	ID	DDR3 Memory Type	VRAM Vendor Part
Hynix	0000	0	64M*16*4 pcs(512MB)	H5TO1G63BFR-12 (1600Mbps)
	0001	1	64M*16*4 pcs(512MB)	H5TO1G63BFR-12C (1600Mbps)
	0010	2	128M*16*4 pcs(1GB)	H5TQ2G63BFR-12C (1600Mbps)
	0011	3	128M*16*4 pcs(1GB)	H5TQ2G63BFR-11C LF (1800Mbps)
	0100	4		
	0101	5		
	0110	6		
	0111	7		
Samsung	1000	8	64M*16*4 pcs(512MB)	K4W1G1646E-HC12 (1600Mbps)
	1001	9	64M*16*4 pcs(512MB)	K4W1G1646G-BC12 (1600Mbps)
	1010	10	128M*16*4 pcs(1GB)	K4W2G1646B-HC12 (1600Mbps)
	1011	11	128M*16*4 pcs(1GB)	K4W2G1646C-HC12 (1600Mbps)
	1100	12		
	1101	13		
	1110	14		
	1111	15		

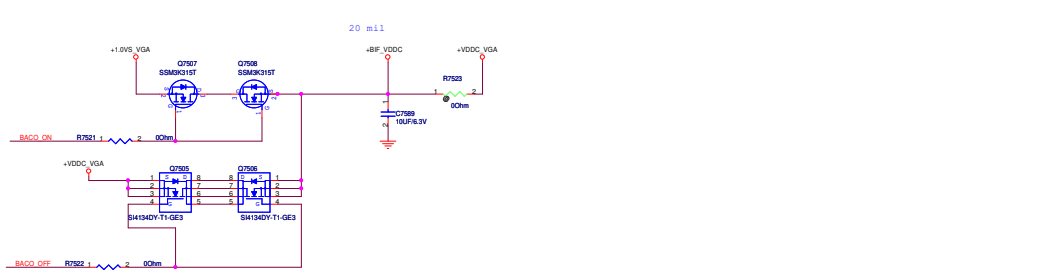
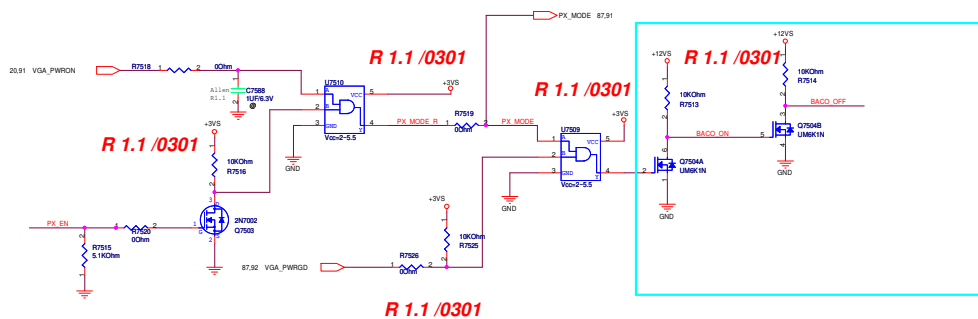
R 1.1 /0301



PX_EN=0: Normal Operation
PX_EN=1: BACO Mode

BIF short with +VDDC_VGA if BACO is not support
BIF_VDDC: I=55mA@BACO MODE (AN_MGEN_R5)

NC for seymour



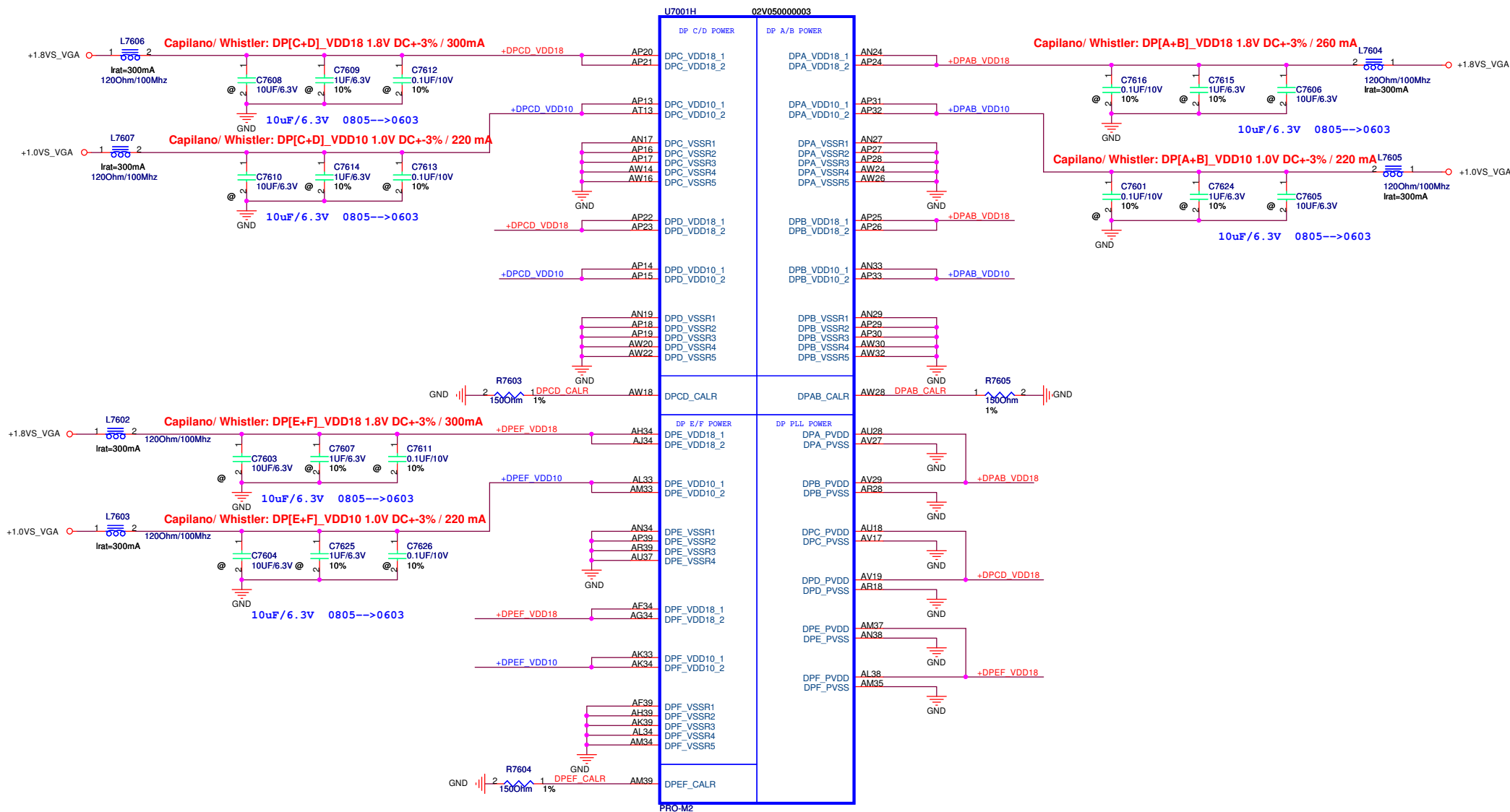
0301-change

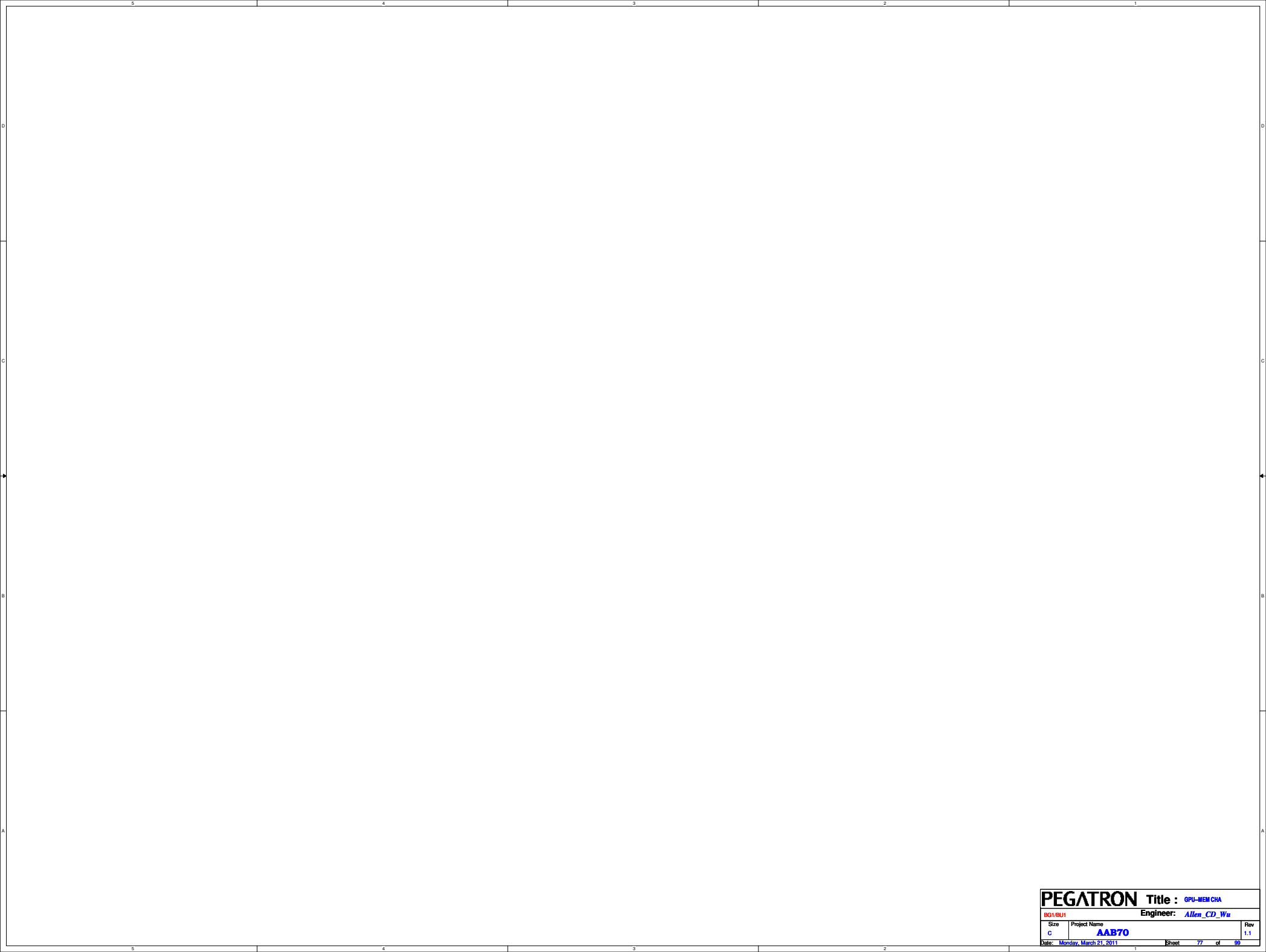
PX with BACO mode all displays are always driven by APU

DPA&DPB share power ;DPC&DPD share power ;DPE&DPF share power

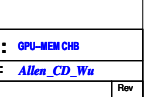
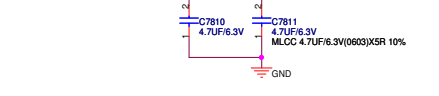
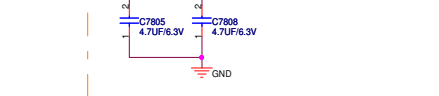
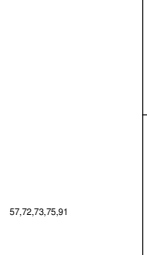
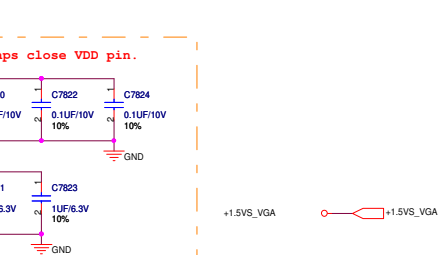
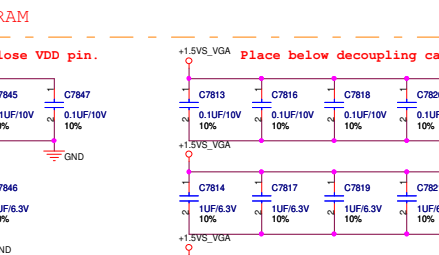
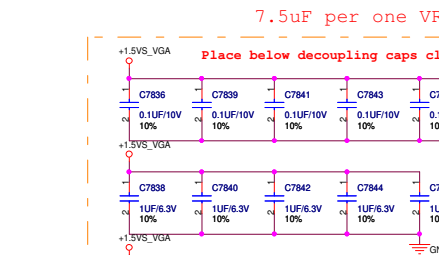
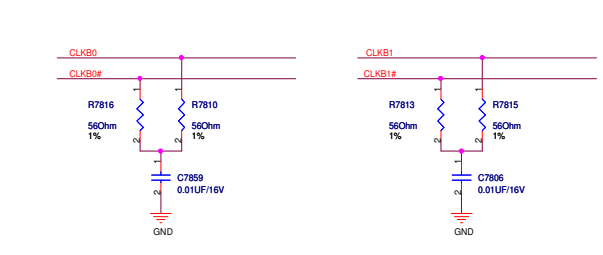
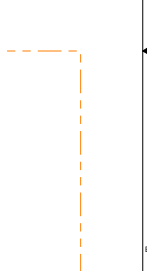
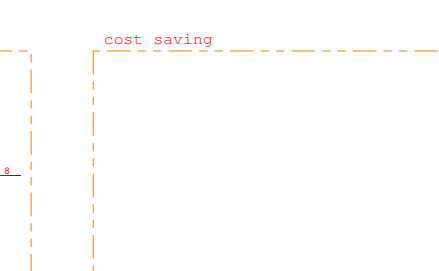
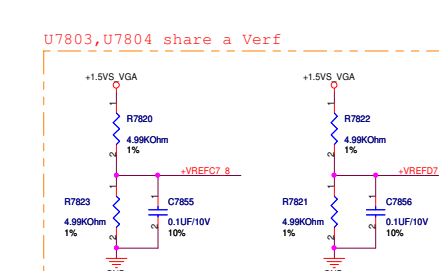
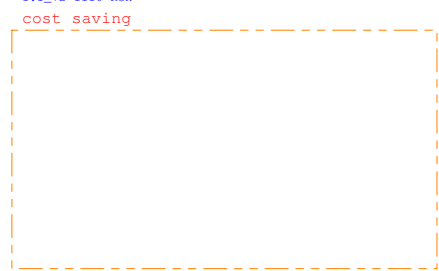
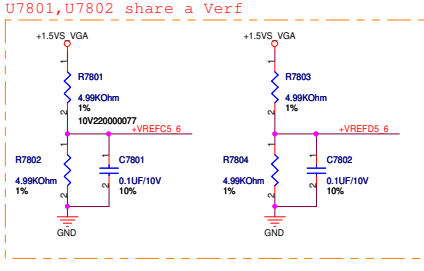
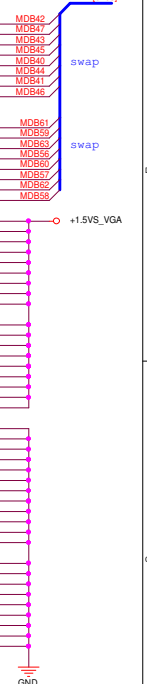
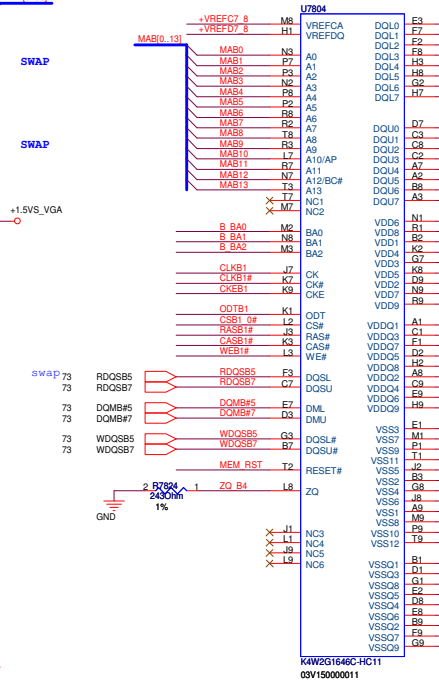
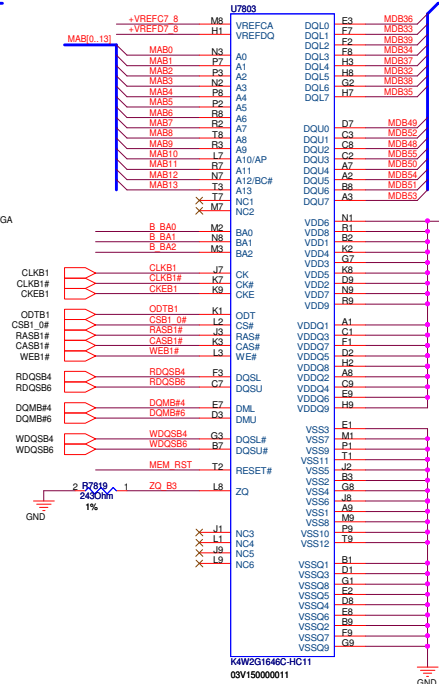
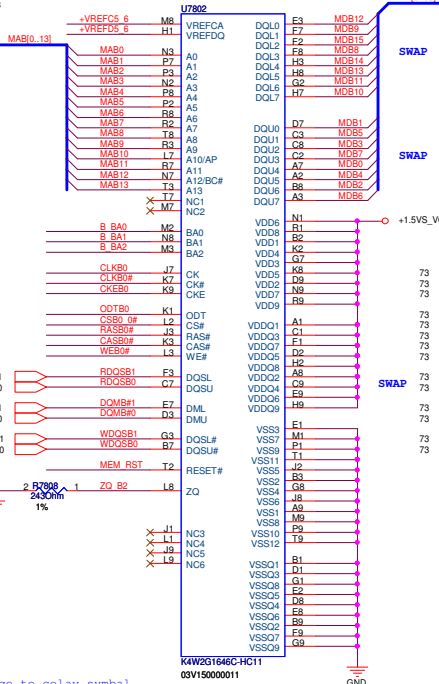
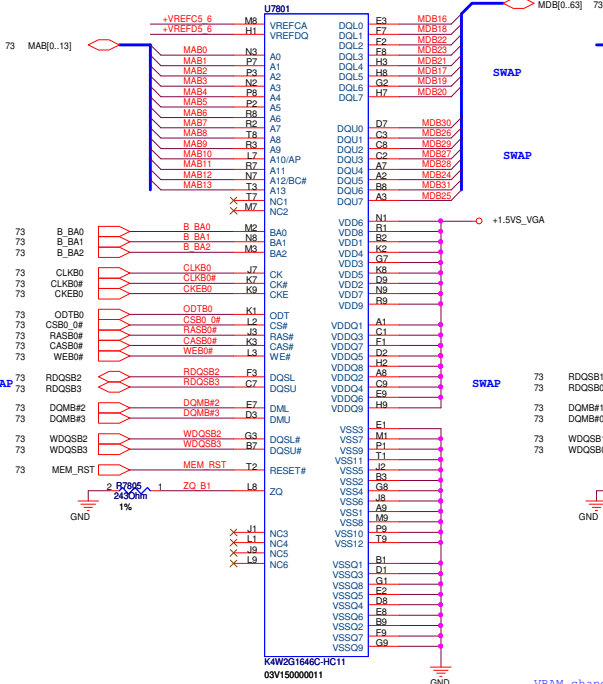
+1.0VS_VGA
+1.8VS_VGA

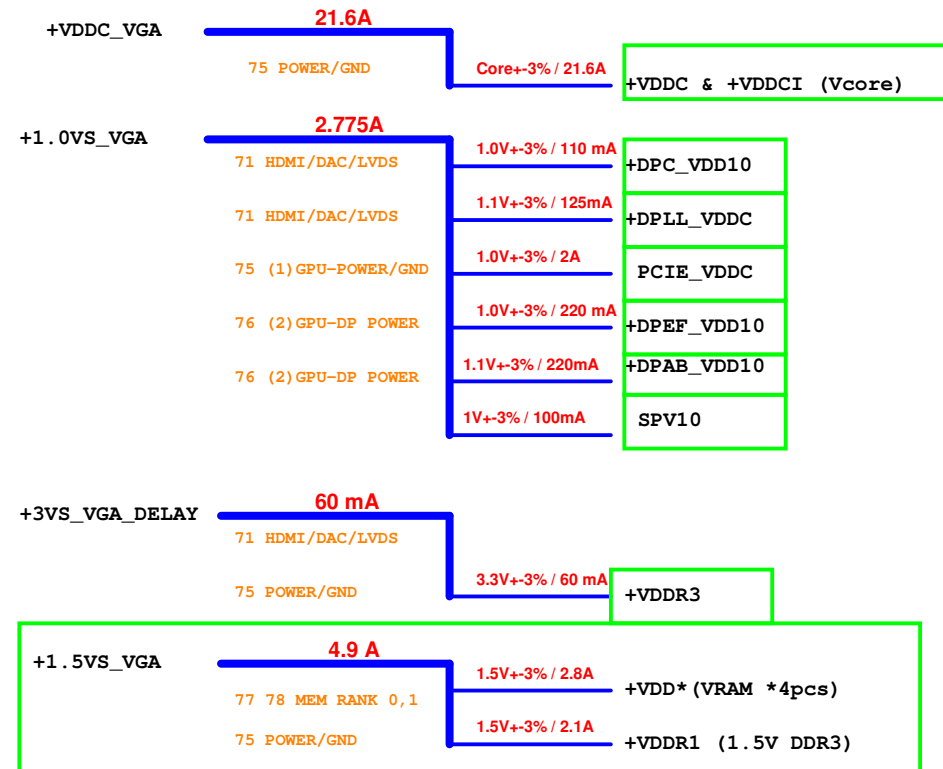
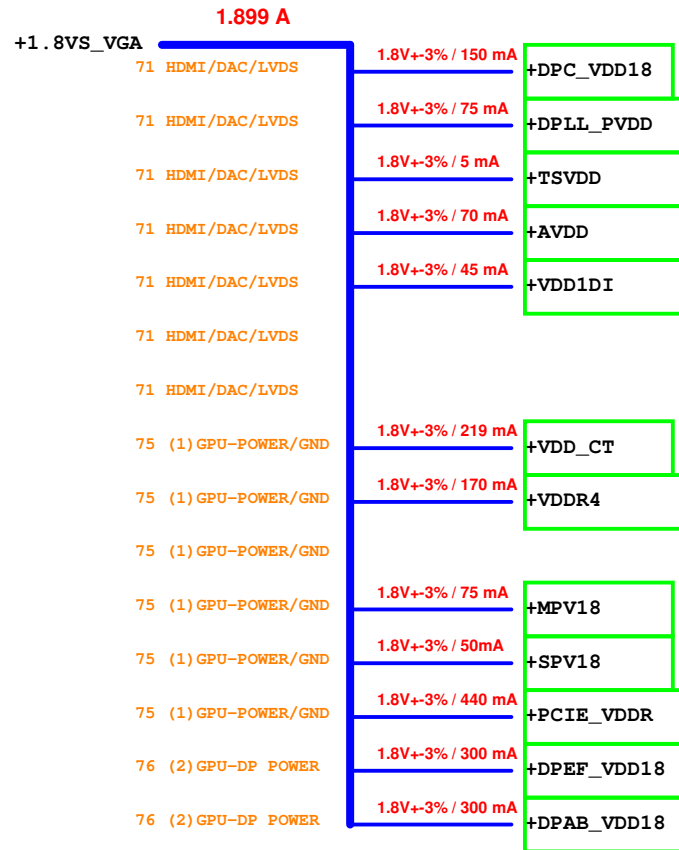
+1.0VS_VGA 57,70,71,75,91
+1.8VS_VGA 57,71,74,75,91





DDRIII1866 128M*16-1.5V BGA96





Total:15W (w/o VRAM)

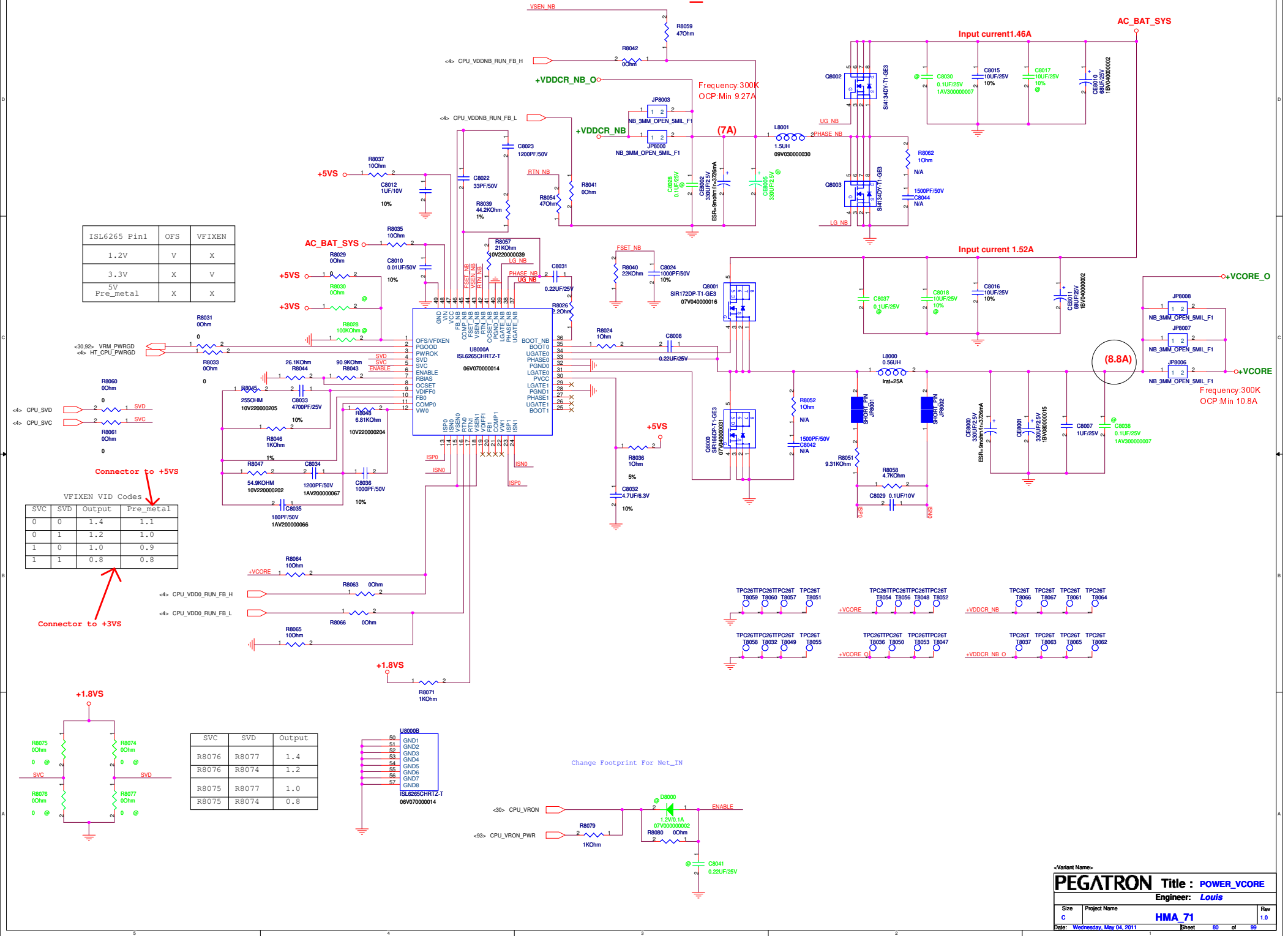
Power Up Sequence :

+VGA_VCORE -> +1.0VS_VGA -> +1.5VS_VGA -> +1.8VS_VGA -> +3VS_VGA_DELAY

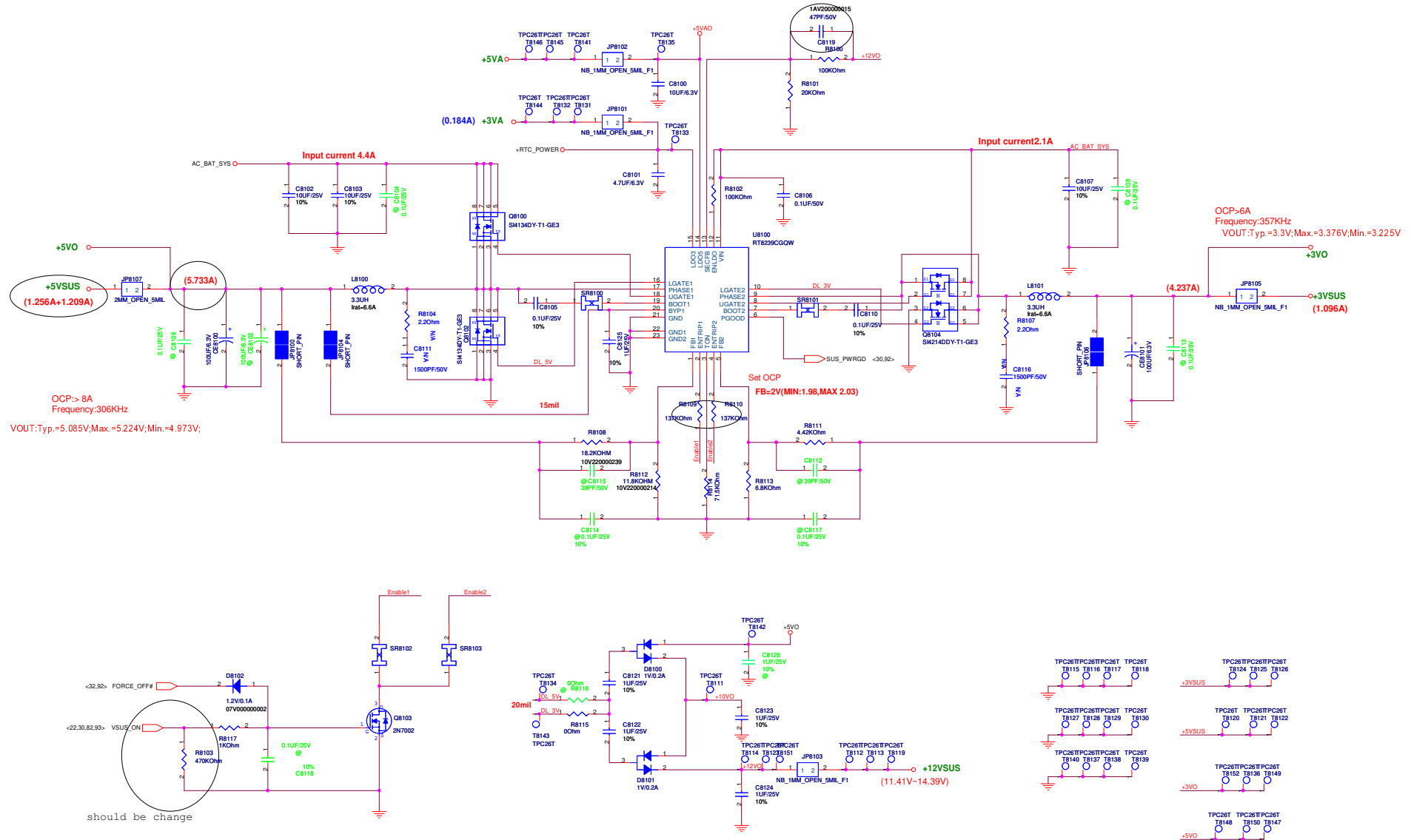
Power Down Sequence :

+3VS_VGA_DELAY -> +1.8VS_VGA -> +1.5VS_VGA -> +1.0VS_VGA -> +VGA_VCORE

HMA71_AB DSC +VCORE POWER SUPPLY



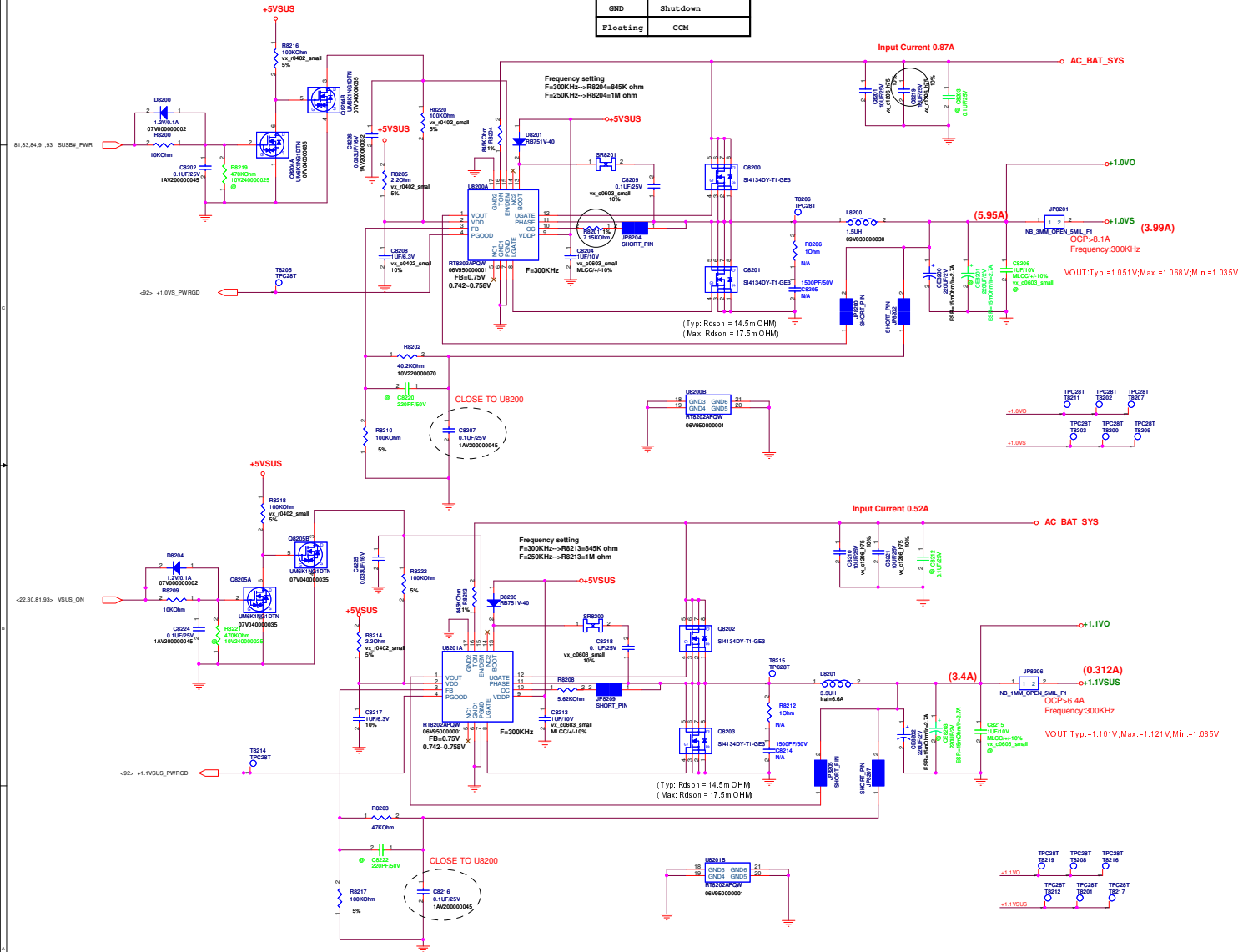
HMA71 DSC +SYSTEM POWER SUPPLY



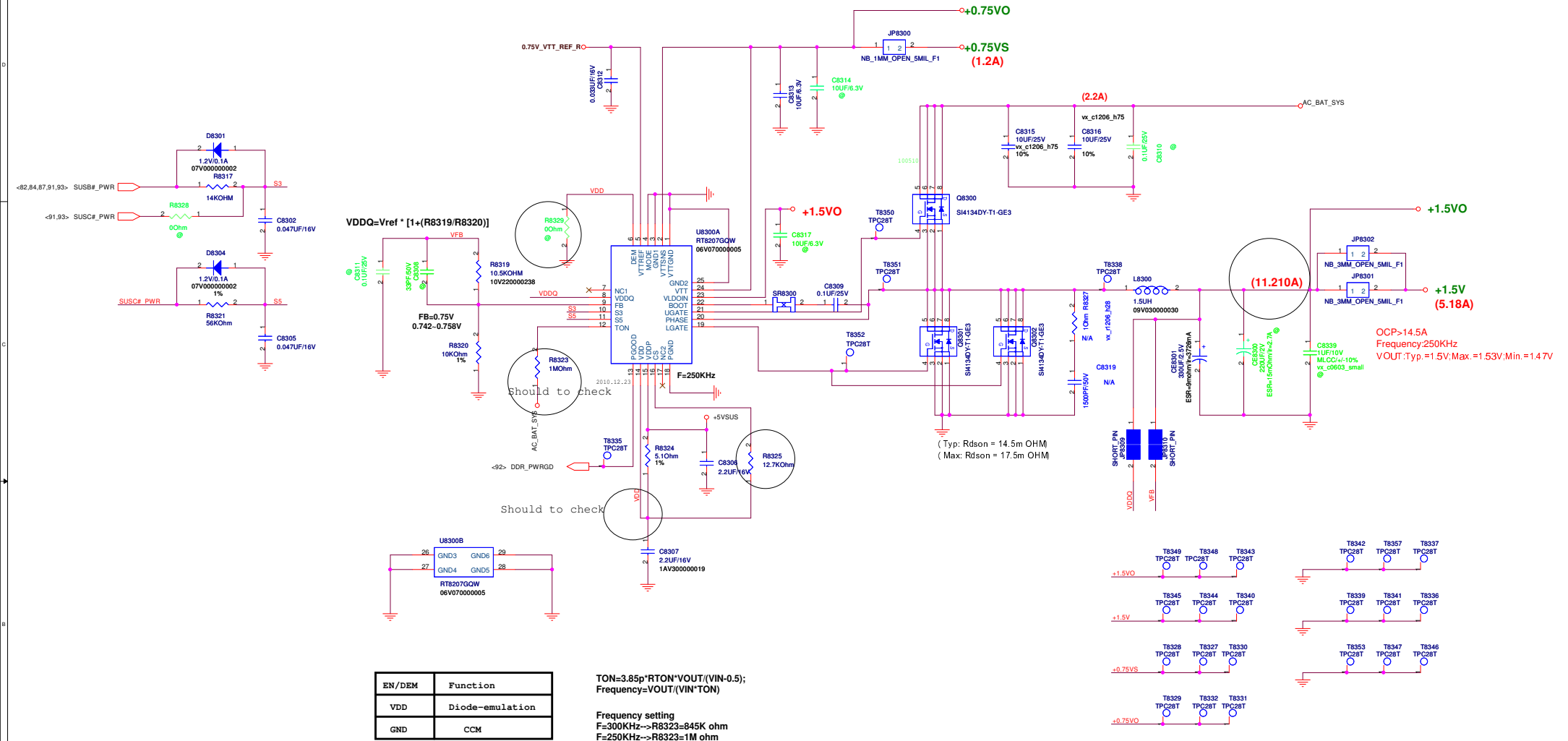
HMA71 DSC +1.0V0&+1.1V0 POWER SUPPLY

P.82

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM



+1.5VO & +0.75VS POWER SUPPLY



EN/DEM	Function
VDD	Diode-emulation
GND	CCM

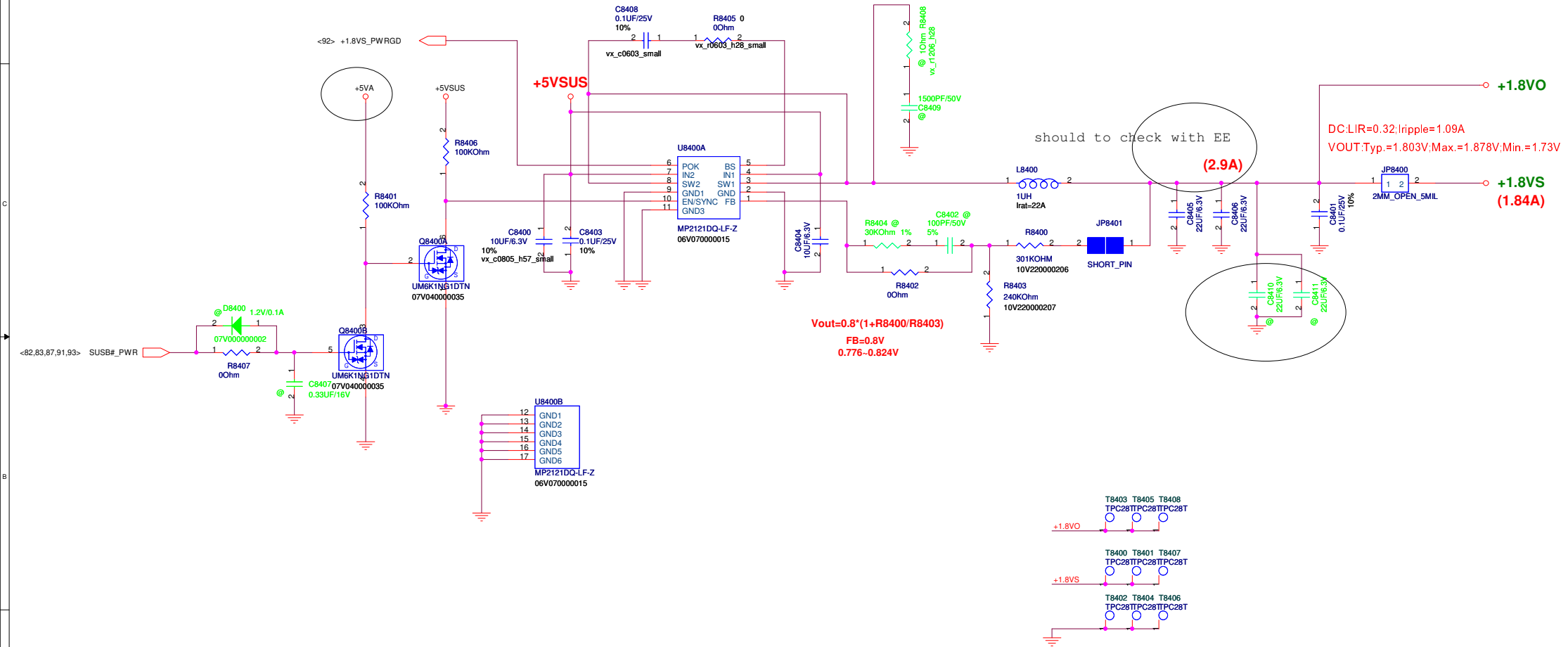
$$\text{TON} = 3.85 \mu\text{s} \cdot \text{R}_{\text{TON}} \cdot \text{V}_{\text{OUT}} / (\text{V}_{\text{IN}} - 0.5);$$

$$\text{Frequency} = \text{V}_{\text{OUT}} / (\text{V}_{\text{IN}} \cdot \text{TON})$$

Frequency setting
F=300KHz-->R8323=845K ohm
F=250KHz-->R8323=1M ohm

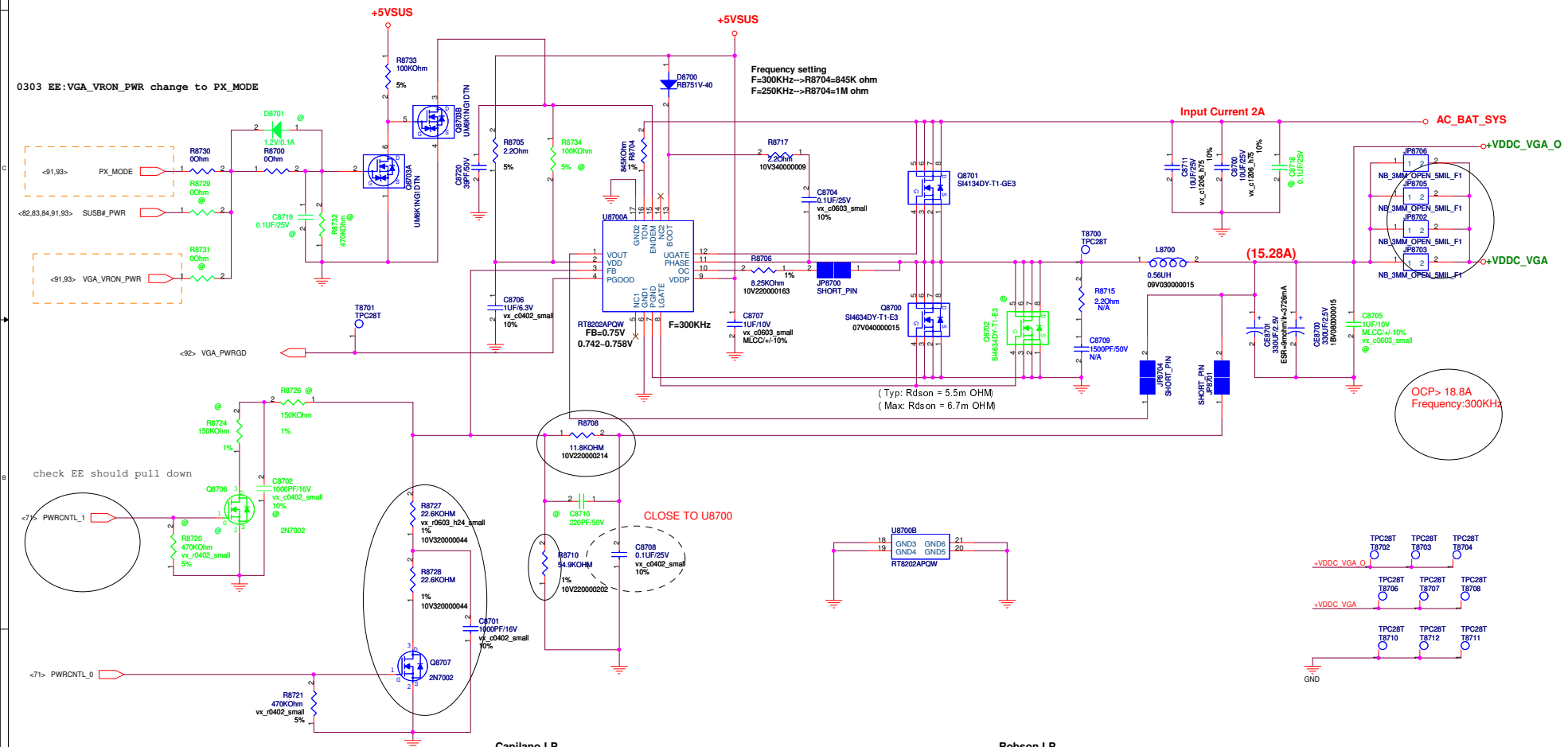
+1.8VS POWER SUPPLY

P.84



AAB70 DSC +VGA_VCORE POWER SUPPLY

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM



Seymour XT (17W)

PWRCNTL_1 (GPIO20)	PWRCNTL_0 (GPIO15)	+VGA_VCORE
LOW	LOW	0.9V/real 0.911V
LOW	HIGH	1.1V / real1.107V

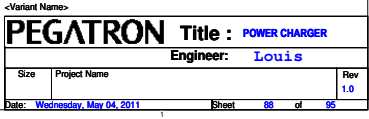
Capilano LP

PWRCNTL_1 (GPIO20)	PWRCNTL_0 (GPIO15)	+VGA_VCORE
LOW	LOW	1V
LOW	HIGH	0.9V
HIGH	HIGH	0.95V

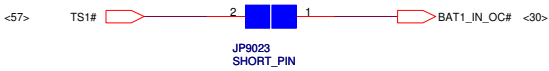
R8727=75K ohm
R8728=75K ohm
R8726, R8724, R8720, Q8708 must be mounted.

Robson LP

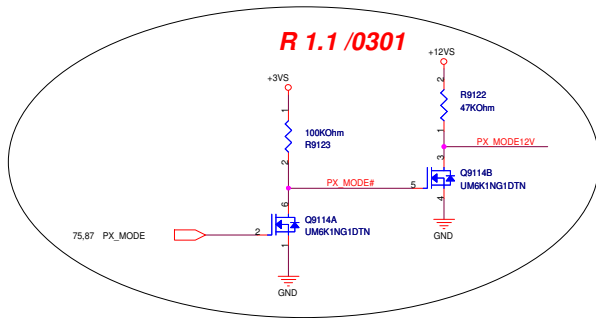
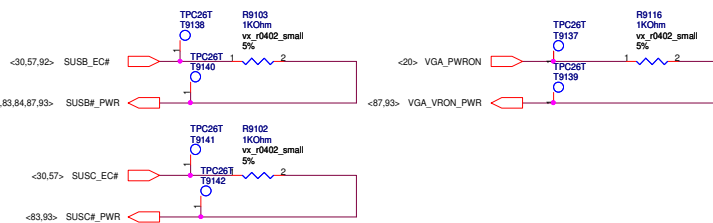
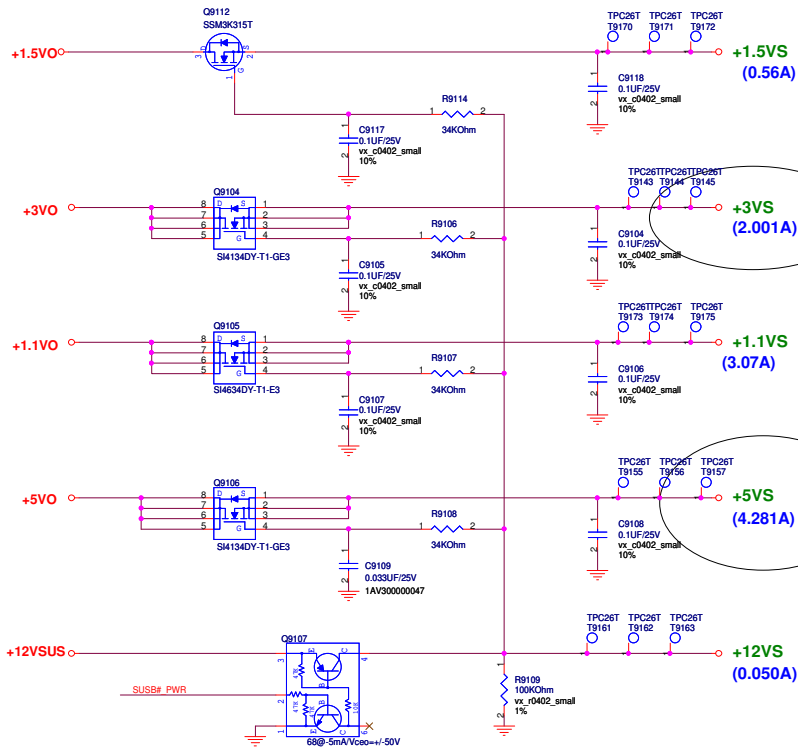
PWRCNTL_1 (GPIO20)	PWRCNTL_0 (GPIO15)	+VGA_VCORR
LOW	LOW	0.95V
LOW	HIGH	0.9V



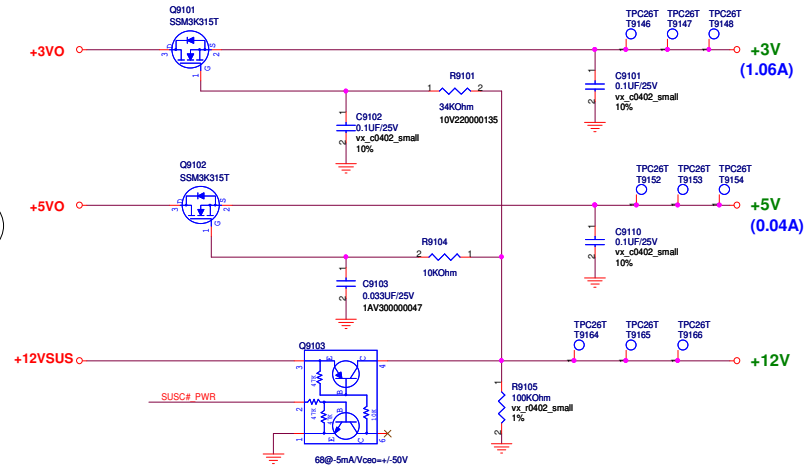
BATTERY IN DETECT



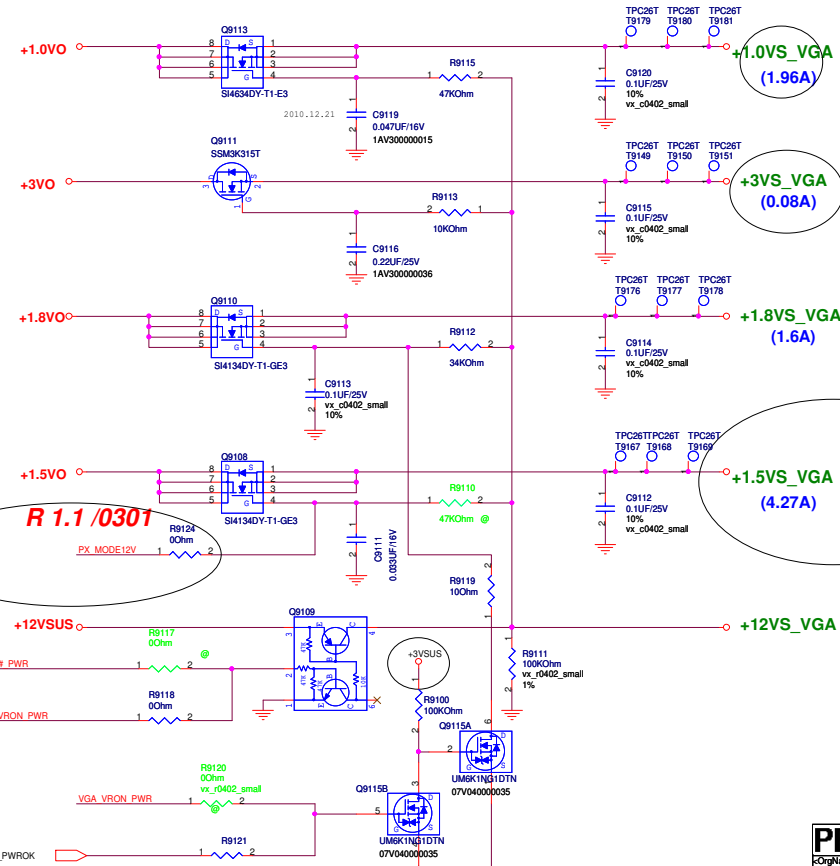
SUSB#_PWR POWER



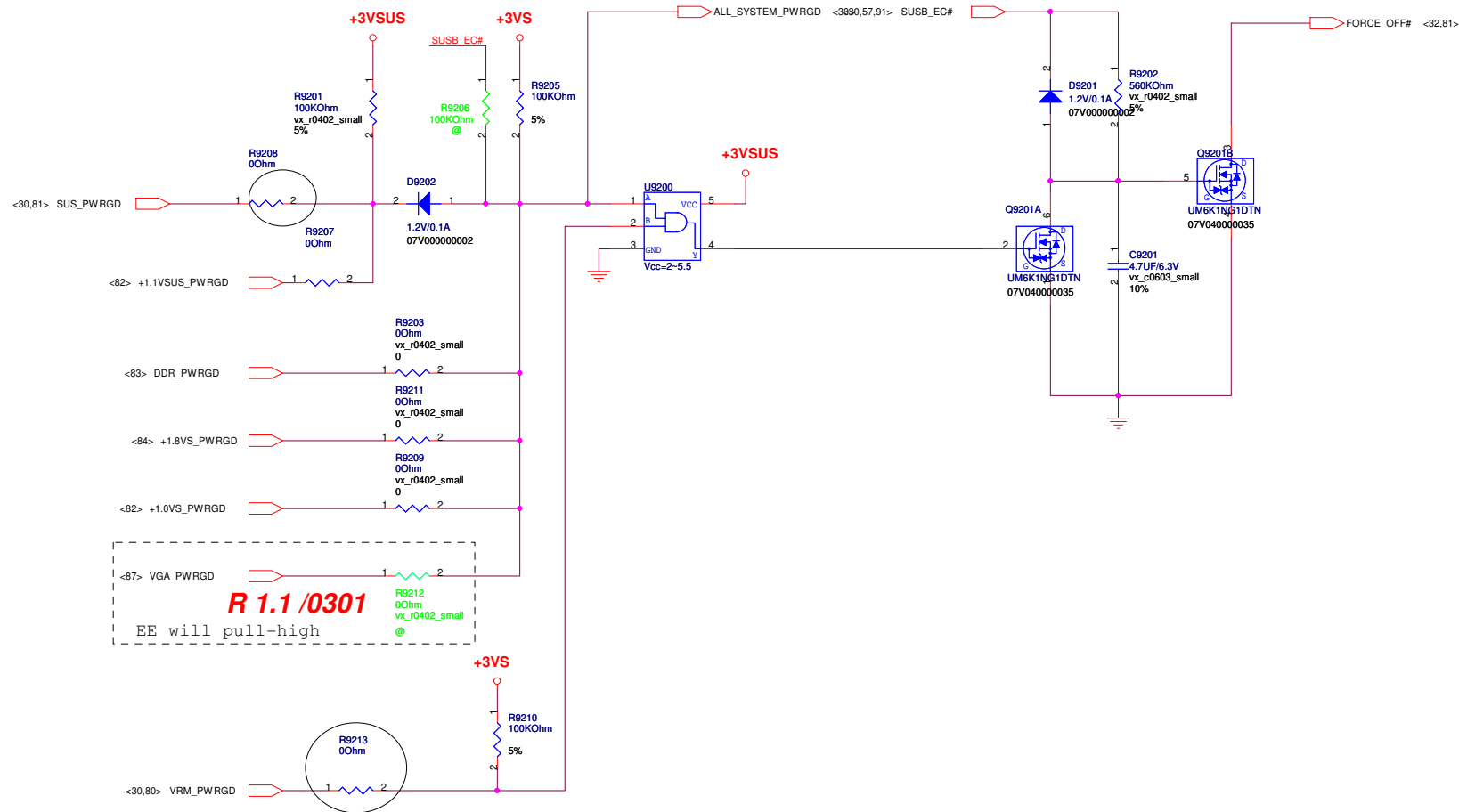
SUSC#_PWR POWER

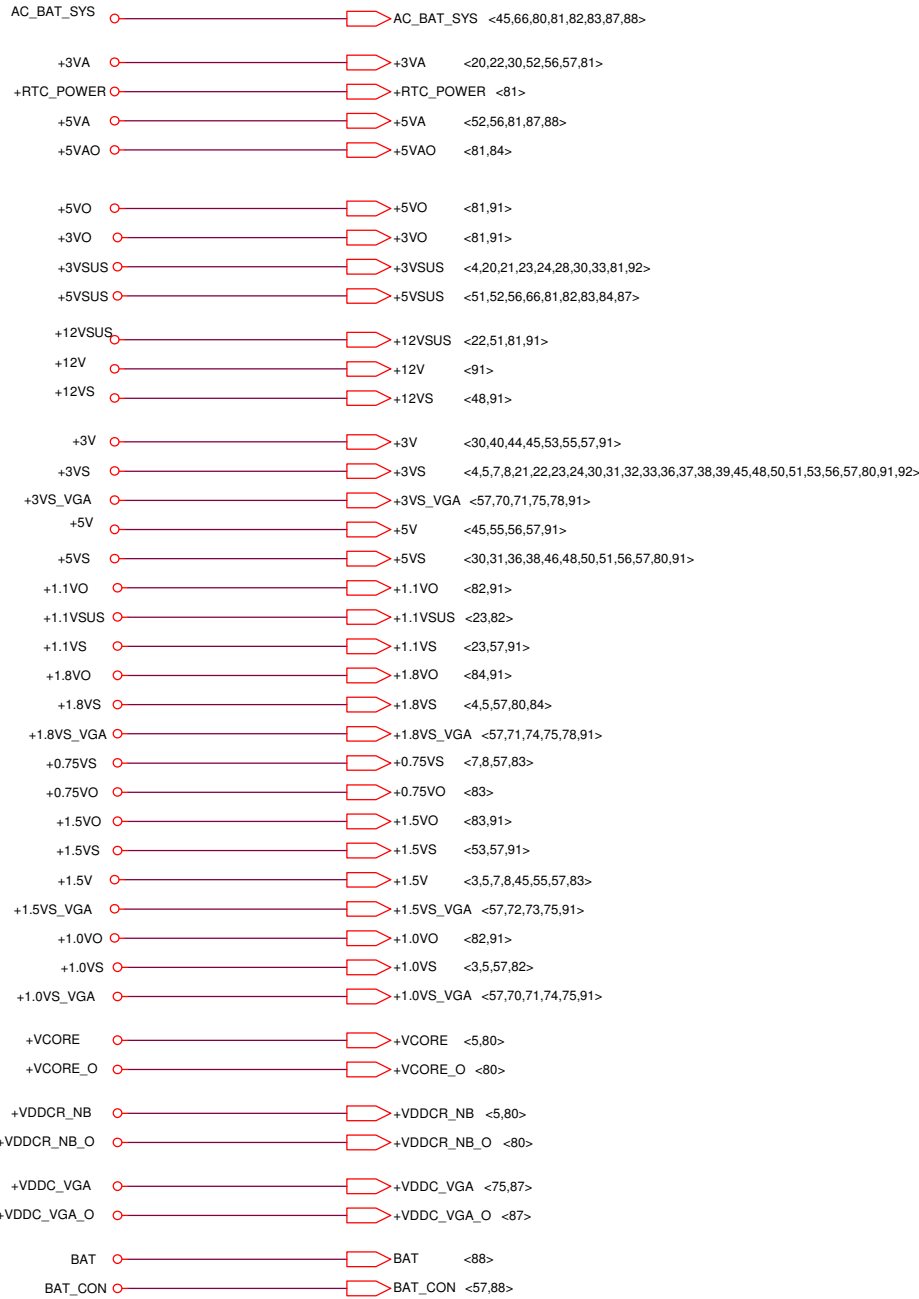


VGA_VRON_PWR_PWR POWER

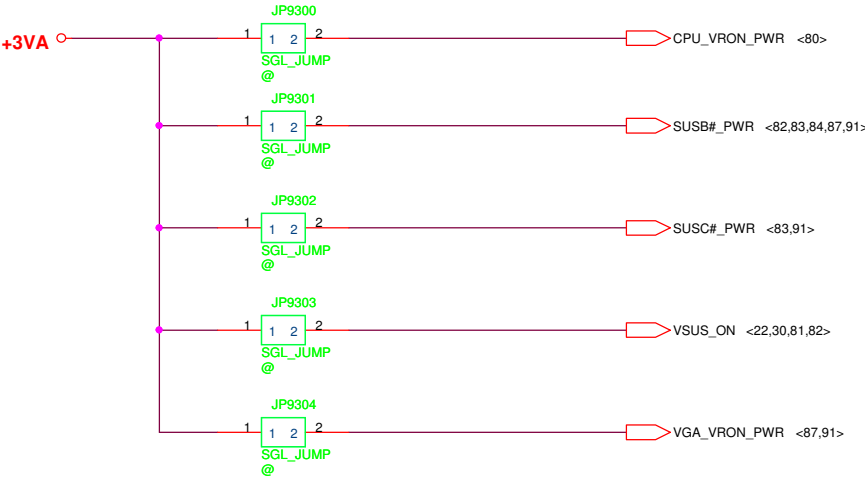


POWER GOOD DETECTOR

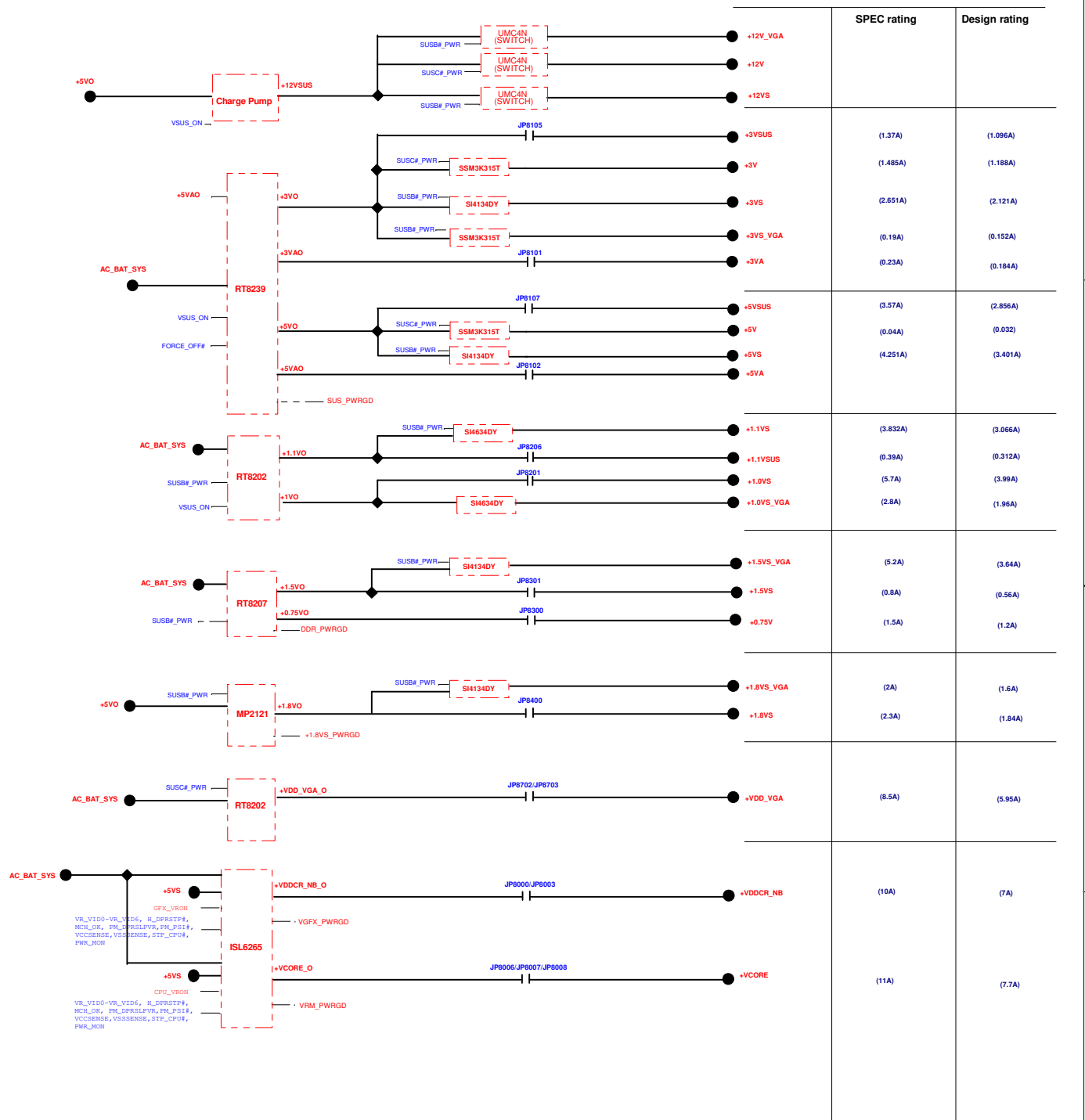




FOR POWER TEST



<Variant Name>		
PEGATRON Title :POWER_SIGNAL		
Engineer: Louis		
Size B	Project Name	Rev 1.0
Date: Wednesday, May 04, 2011 Sheet 93 of 99		



R20

Item	Date	Description
1	0328-11	P.72 Add R7210~R7215, C7201, C7202 for VRAM Channel A reseved. P.5 Change C0508=>0805, L0501=>1K 0603 for CRT ripple noise. P.39 Add R3909, R3910, R3914, R3915 for POP issue P.50 Add R5010, C5020, C5021, Q5001, U5005 for Thermal Palm rest. P.04 Add SP0410, SP0411 for Thermal Palm rest. P.32 Add R3210 for Thermal Palm rest.
7	0330-11	P.98 Copy TP BTN Board from AIH24
8		P.66 Add 2nd USB power switch (U6605) for Audio board USB port voltage drop
9		P.50 Un-mount R5010, C5020, C5021, Q5001, U5005
10	0331-11	P.22 Add Test Pad T2201, T2202 for U2001.W5 and AE29 ICT function.
11		P38. Update CON3801, CON3802=>1217-00P1000
12		P66. Update CON6602=>1218-01BJ000
13		P99. Update IOCON5=>1218-01BJ000
14		P31. CON3102, CON3103=>1218-00C7000
15	0404-11	P65. Change H6539, H6541, H6542, H6545, H6633 to NPTH
16		P66. Change CON6603, CON6605 to 4 pin. Del C6605, C6608. Un-mount R6609
17		P97. Change PWR_U01 to 4 pin, delete PWR_R2, PWR_LED2
18	0406-11	P65. Modify H6541, H6542, H6545 GND
19		P33. Add L3303 for AVDDL EMI issue
20		P34. Add U3405 for EMI Home issue
21	0407-11	P66. Add CON6608
22		P99. Add IOCON6
23		P34. Un-mount R3408, R3409
24		P72. Un-mount C7201, C7202
25	0410-11	P39. R3905, R3906=> 51 ohm
26		P33. Mount R3317=> 10K
27		P46. Change L4601~L4603=> 56nH (Not yet)
28		P66. Change U6601=>1.5A, Mount U6605
29	0411-11	P30. Change R3035 option as /SJV_ID
30		P21. Change R3042 option as /SJV_ID
31	0421-11	P66. Change U6601, U6605 => 2.5A
32		P50. Change R5001 => 39K ohm for Thermal
33		P56. Change R5603,R5621 => 100 ohm,390 ohm ; LED5610,R5611=> 0713-1QJ000,0713-1QK000
34		P33. Change C3321,C3322 => 15PF
35		P33. Change L3303 => 0 ohm (0603)
36		P46. Change L4601, L4602, L4603 => 56nH for EMI
37		Update Power AAB7A_BRAZO_PWR_2R0_0411_DSC_A& AIC70 Sub board AIC70_R20_201104211100
38	0503-11	P66 unmount con6608
39	0504-11	P34 Mount R3408
40		P65 Un-mount H6535, H6536
41		P99 Un-mount IOCON6
42		Update Power AAB7A_BRAZO_PWR_2R0_0504_DSC_A
43	0505-11	P39 Un-mount R3910, Mount R3914=1M ohm

PEGATRON

Title :History

<OrgName>

Engineer: <OrgAddr1>

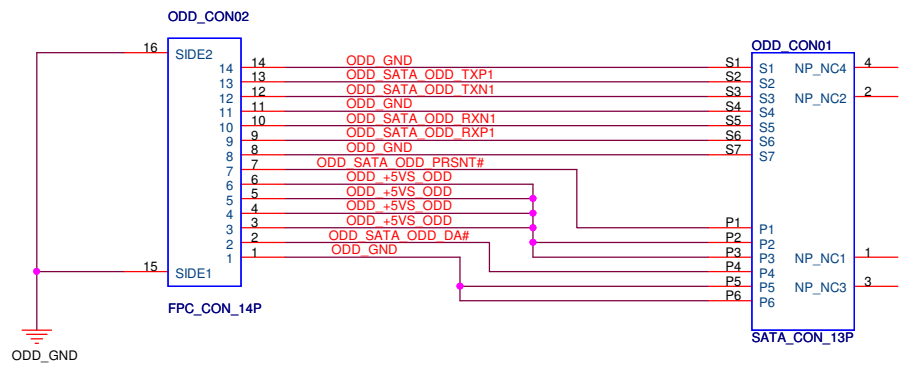
Size
B

Project Name
AAB70

Rev
1.1

Date: Thursday, May 05, 2011

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ODD_H5
C102D102N

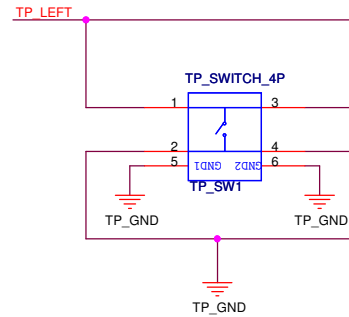
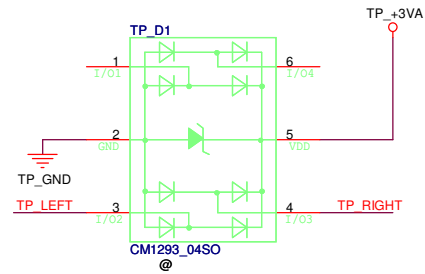
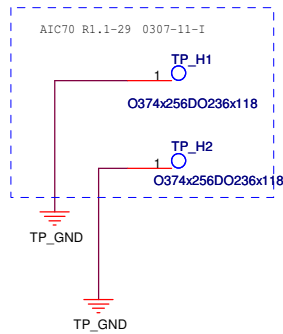
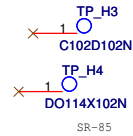
SR-88

ODD_H01
C256D118

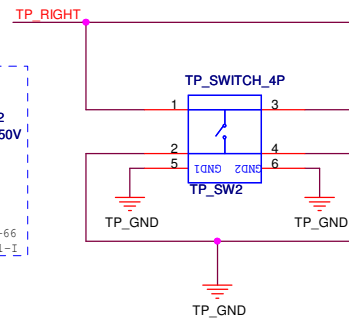
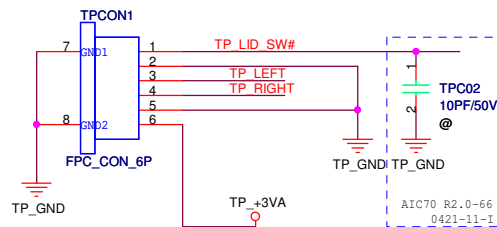
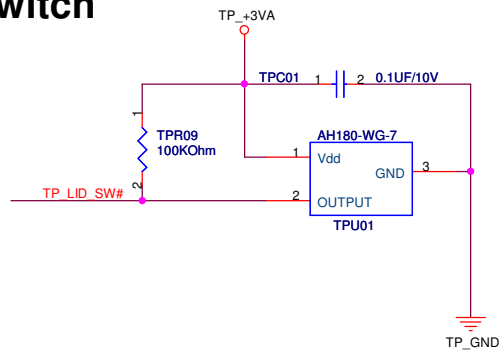
ODD_GND

SR-85

PEGATRON		Title : ODD	
BU1-RD Div.1-HW RD Dept.1		Engineer: Johnson Huang	
Size B	Project Name TOD ODD BOARD		Rev 2.0
Date: Thursday, April 21, 2011		Sheet 96 of 77	



LID Switch



AIC70 R2.0-48 0330-11-I
AIC70 R2.0-67 0421-11-I

PEGATRON		Title : A03 TP	
<OrgName>		Engineer: Johnson Huang	
Size B	Project Name AIH70		Rev 1.0
Date: Thursday, April 21, 2011		Sheet 98 of 99	

