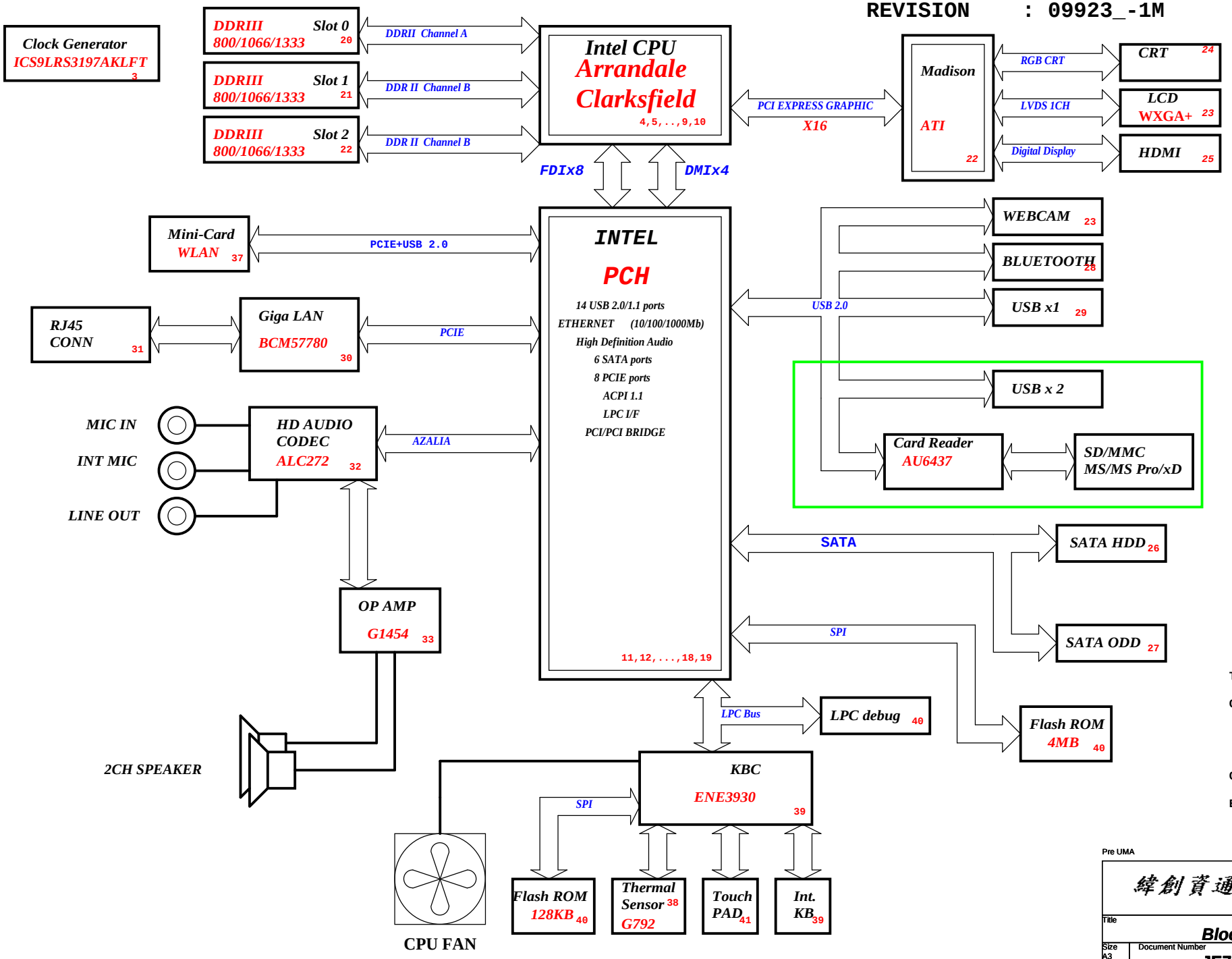
JE70-CP Block Diagram

Project code: 91.4HN01.001
PCB P/N : 48.4HN01.0SD
REVISION : 09923_-1M



SYSTEM DC/DC RT8223	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 47

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 48

SYSTEM DC/DC RT8209B	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 49

SYSTEM DC/DC TPS51611	
INPUTS	OUTPUTS
DCBATOUT	GFX_CORE 52

CPU DC/DC TPS51621	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 45,46

MAXIM CHARGER BQ24745	
INPUTS	OUTPUTS
DCBATOUT	BT+ 51

PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size	Document Number	Rev
A3	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 1 of 67

PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

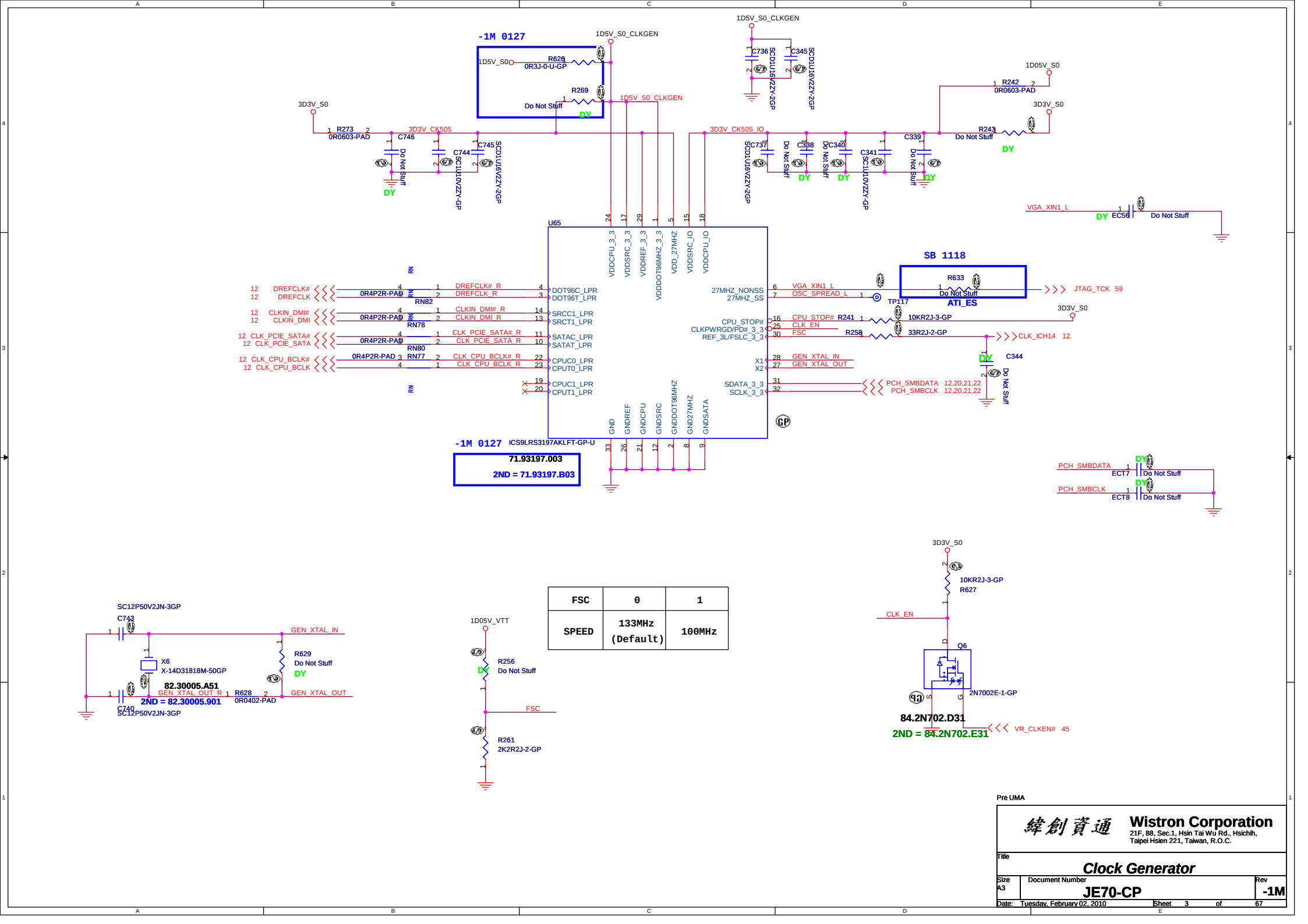
Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

Size	Document Number	Rev
A3	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 2 of 67



FSC	0	1
SPEED	133MHz (Default)	100MHz

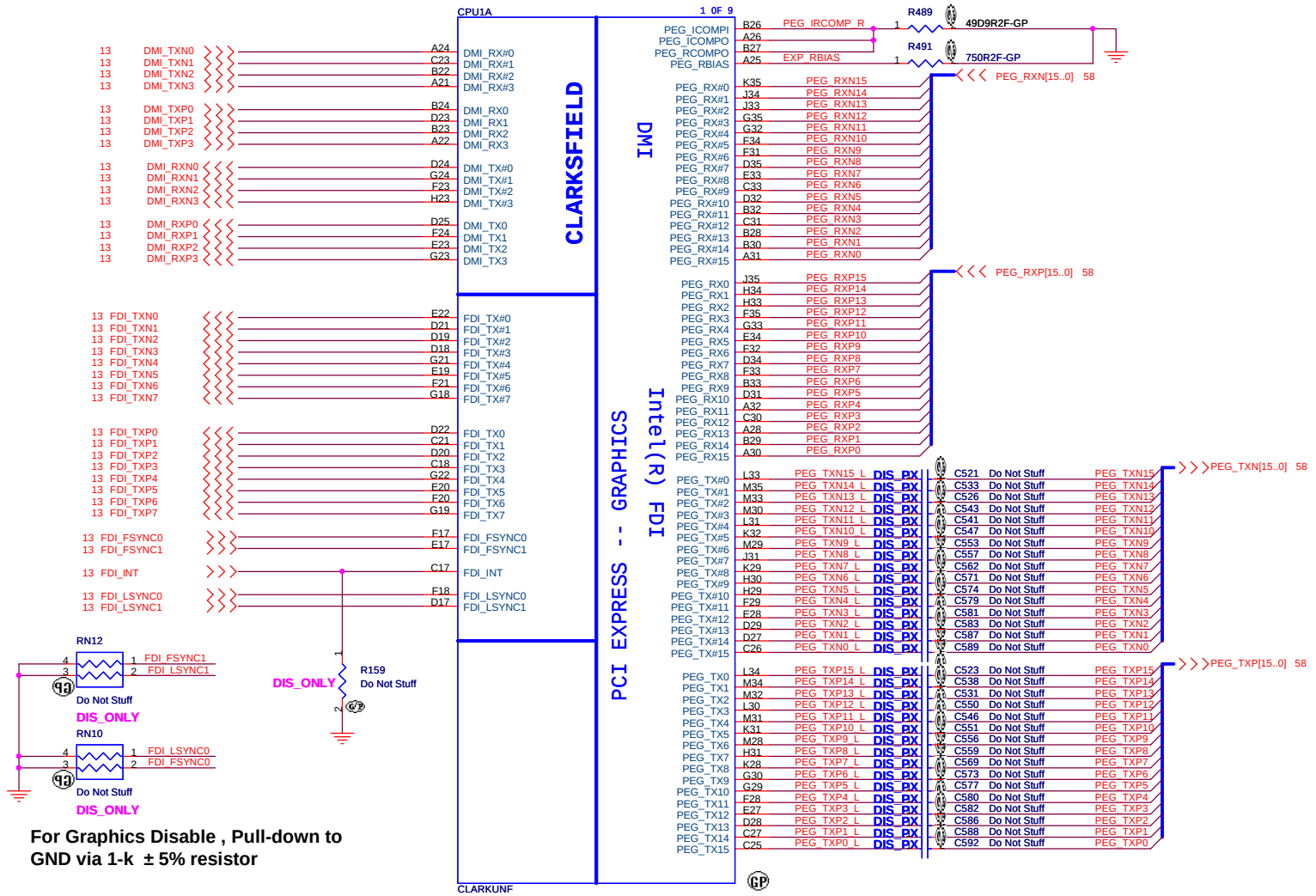
Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator

Size	Document Number	Rev
A3	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 3 of 67



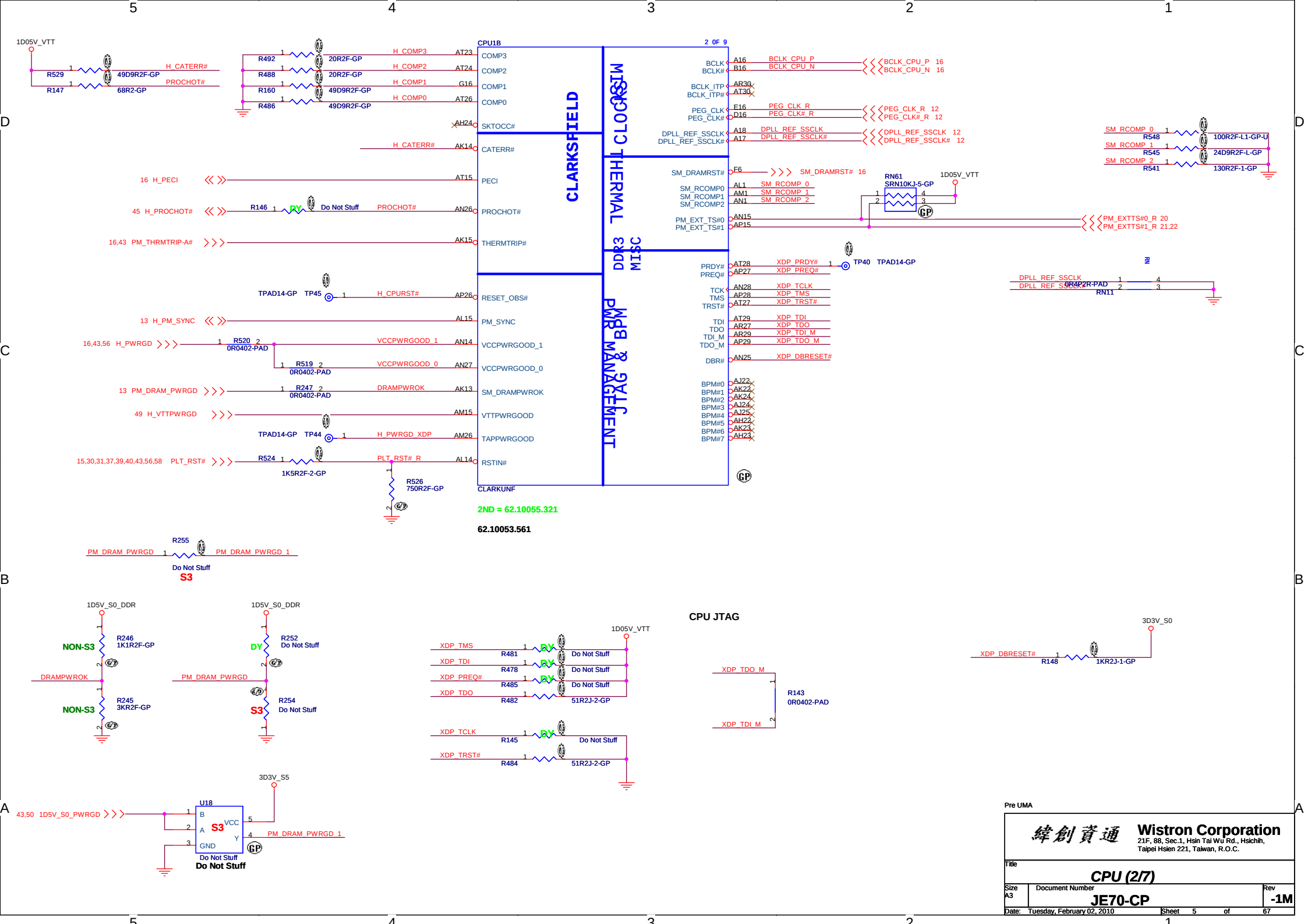
Pre UMA

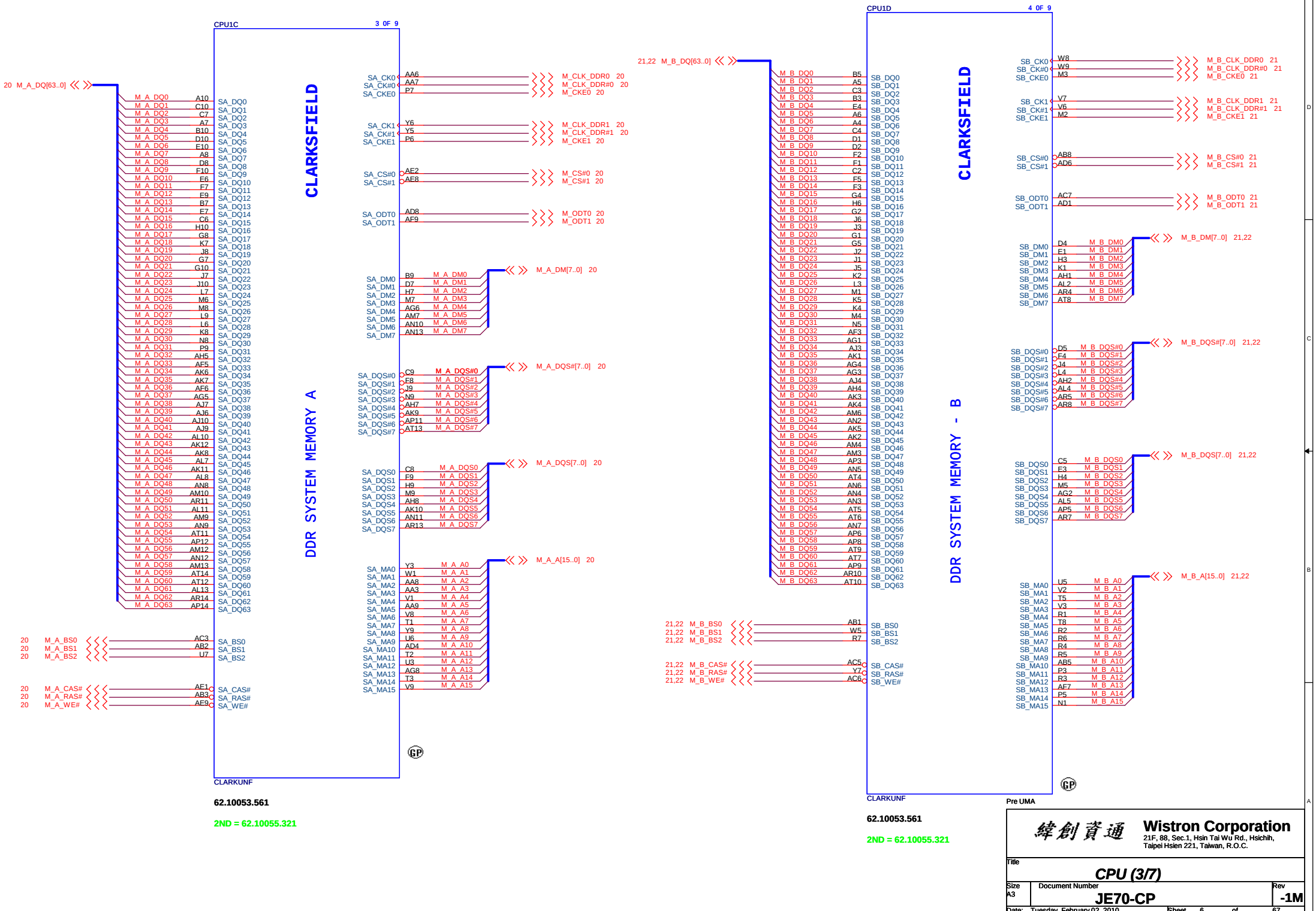
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

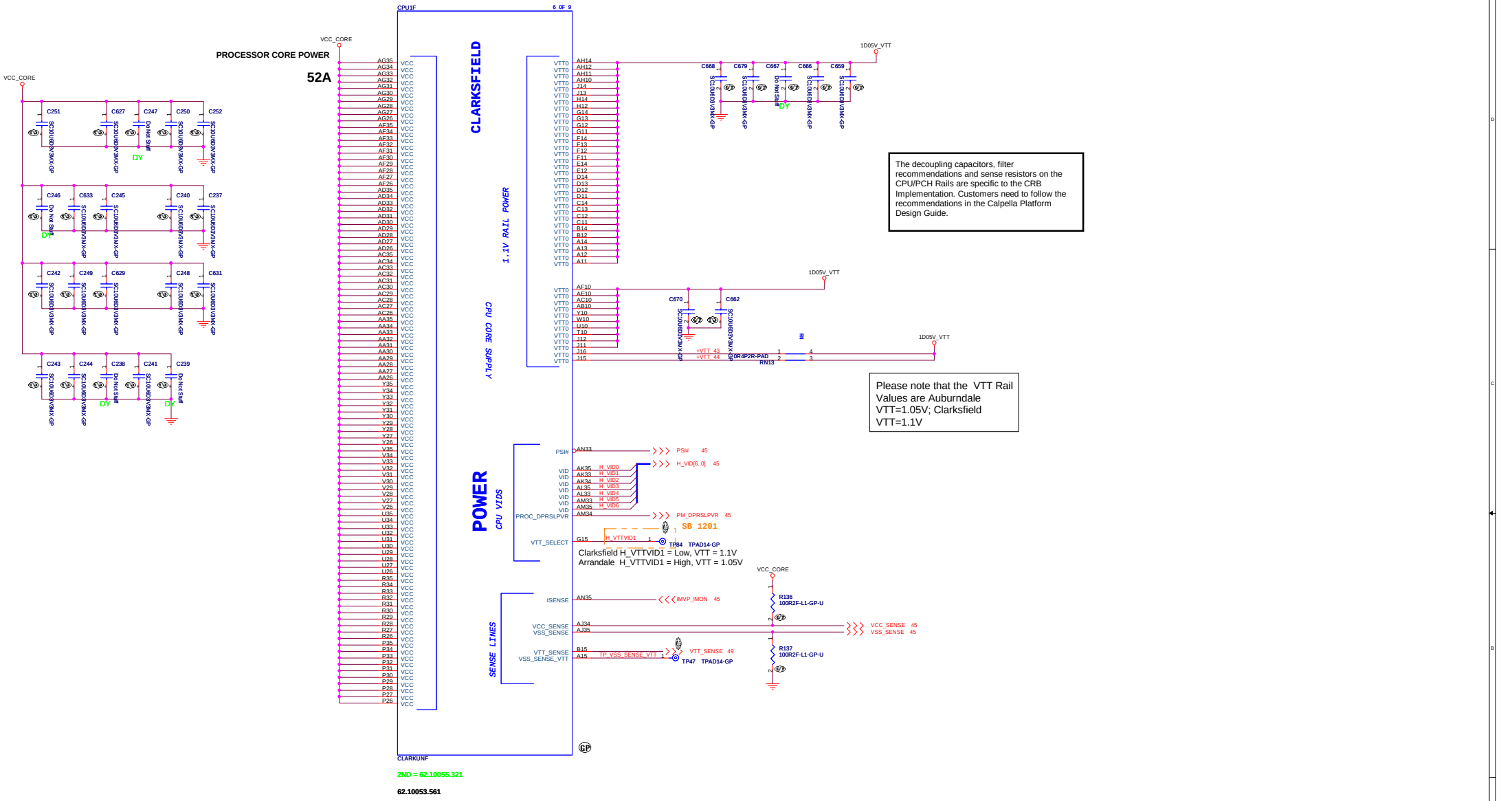
Title: CPU (1/7)

Size	Document Number	Rev
A3	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 4 of 67

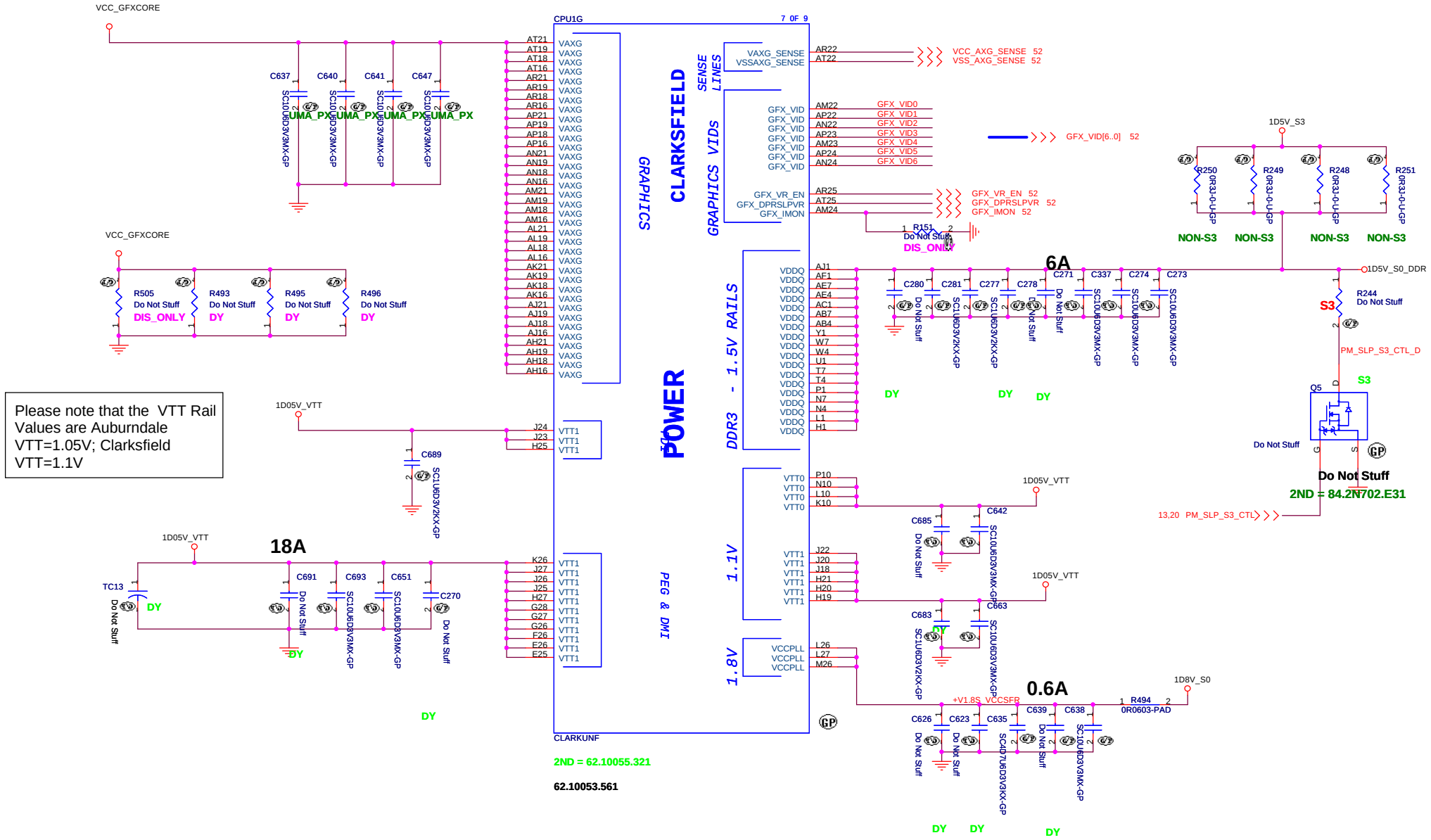

CPU1B
2 OF 9
CLARKSFIELD
MISC CLOCKS
THERMAL
DDR3
MISC
PWR MANAGEMENT
CLARKUNF
1D05V_VTT
H_CATERR#
PROCHOT#
H_COMP3
H_COMP2
H_COMP1
H_COMP0
R492
R488
R160
R486
20R2F-GP
49D9R2F-GP
R529
R147
68R2-GP
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
RESET_OBS#
PM_SYNC
VCCPWRGOOD_1
VCCPWRGOOD_0
SM_DRAMPWROK
VTTPWRGOOD
TAPPWRGOOD
RSTIN#
H_PECI
H_PROCHOT#
PM_THRMTRIP#A#
H_CPURST#
H_PM_SYNC
H_PWRGD
R520
R519
0R0402-PAD
PM_DRAM_PWRGD
R247
H_VTTPWRGD
H_PWRGD_XDP
PLT_RST#
R524
1K5R2F-2-GP
R526
750R2F-GP
TPAD14-GP
TP45
TP44
R146
DY
Do Not Stuff
BCLK
BCLK_ITP
PEG_CLK
DPLL_REF_SSCLK
SM_DRAMRST#
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
PM_EXT_TS#0
PM_EXT_TS#1
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
TDI_M
TDO_M
DBR#
BPM#0
BPM#1
BPM#2
BPM#3
BPM#4
BPM#5
BPM#6
BPM#7
BCLK_CPU_P
BCLK_CPU_N
PEG_CLK_R
PEG_CLK#_R
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2
RN61
SRN10KJ-5-GP
PM_EXTTS#0_R
PM_EXTTS#1_R
XDP_PRDY#
XDP_PREQ#
XDP_TCLK
XDP_TMS
XDP_TRST#
XDP_TDI
XDP_TDO
XDP_TDI_M
XDP_TDO_M
XDP_DBRESET#
TP40
TPAD14-GP
100R2F-L1-GP-U
24D9R2F-L-GP
130R2F-1-GP
0R2P2R-PAD
RN11
2ND = 62.10055.321
62.10053.561
R255
Do Not Stuff
S3
1D05V_S0_DDR
NON-S3
R246
1K1R2F-GP
R245
3KR2F-GP
R252
R254
CPU JTAG
R481
R478
R485
R482
R145
R484
51R2J-2-GP
R143
0R0402-PAD
R148
1KR2J-1-GP
3D3V_S0
3D3V_S5
U18
VCC
GND
43,50 1D5V_S0_PWRGD
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU (2/7)
JE70-CP
-1M
Tuesday, February 02, 2010
Sheet 5 of 67


CPU1C
3 OF 9
CLARKSFIELD
DDR SYSTEM MEMORY A
CLARKUNF
62.10053.561
2ND = 62.10055.321
CPU1D
4 OF 9
CLARKSFIELD
DDR SYSTEM MEMORY - B
CLARKUNF
62.10053.561
2ND = 62.10055.321
Pre UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (3/7)
Size A3
Document Number
JE70-CP
Rev
-1M
Date: Tuesday, February 02, 2010
Sheet 6 of 67



Pre UMA

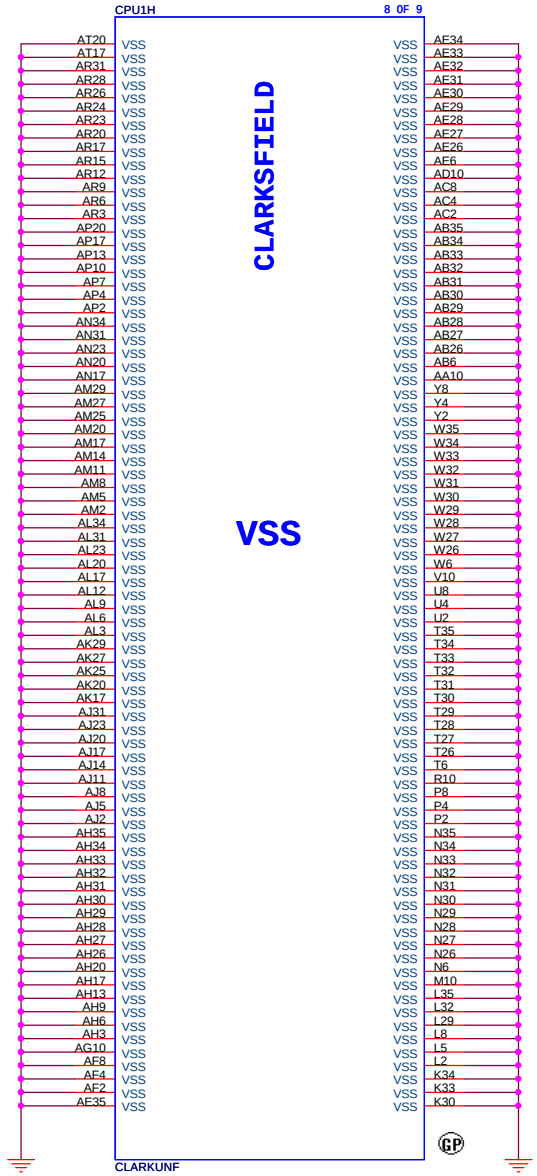
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU (4/7)		
Size: A2	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 7 of 67	

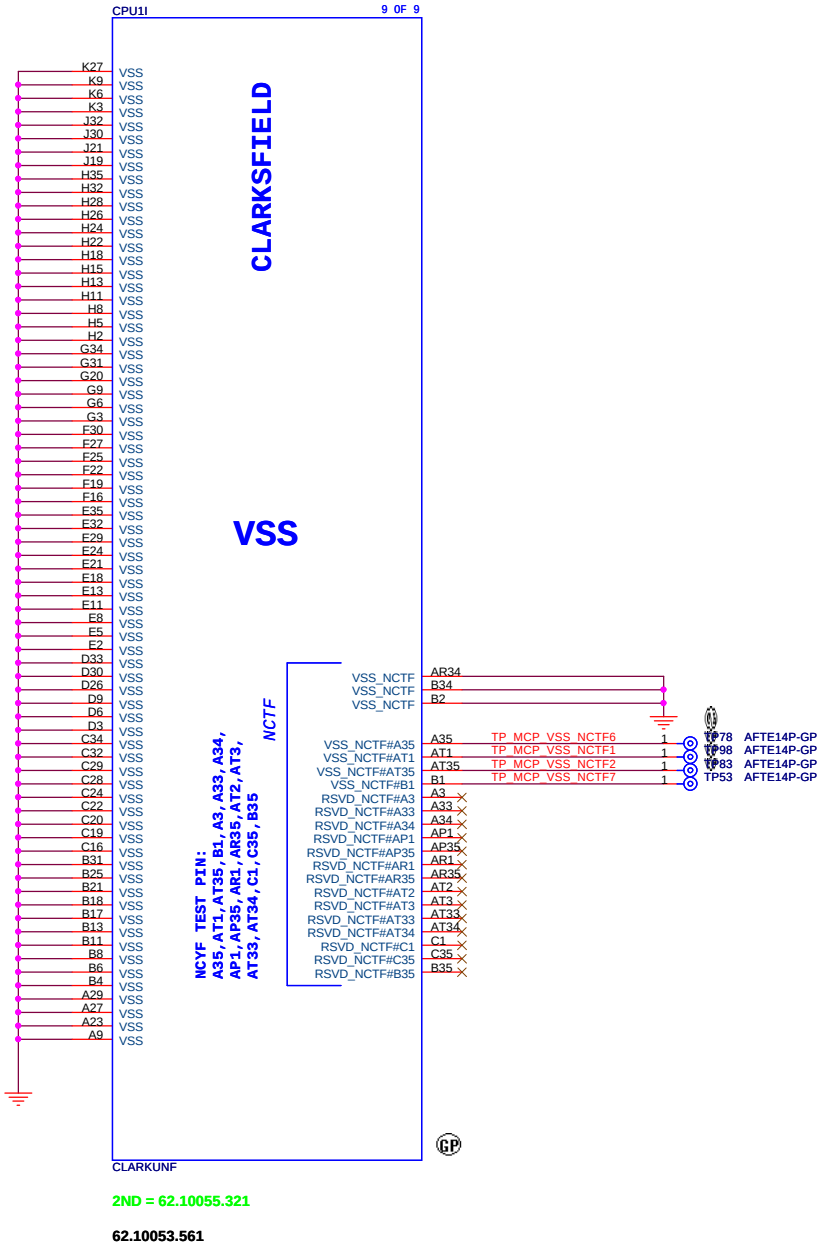


Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (5/7)	
Size A3	Document Number JE70-CP	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 8 of 67	





Pre UMA

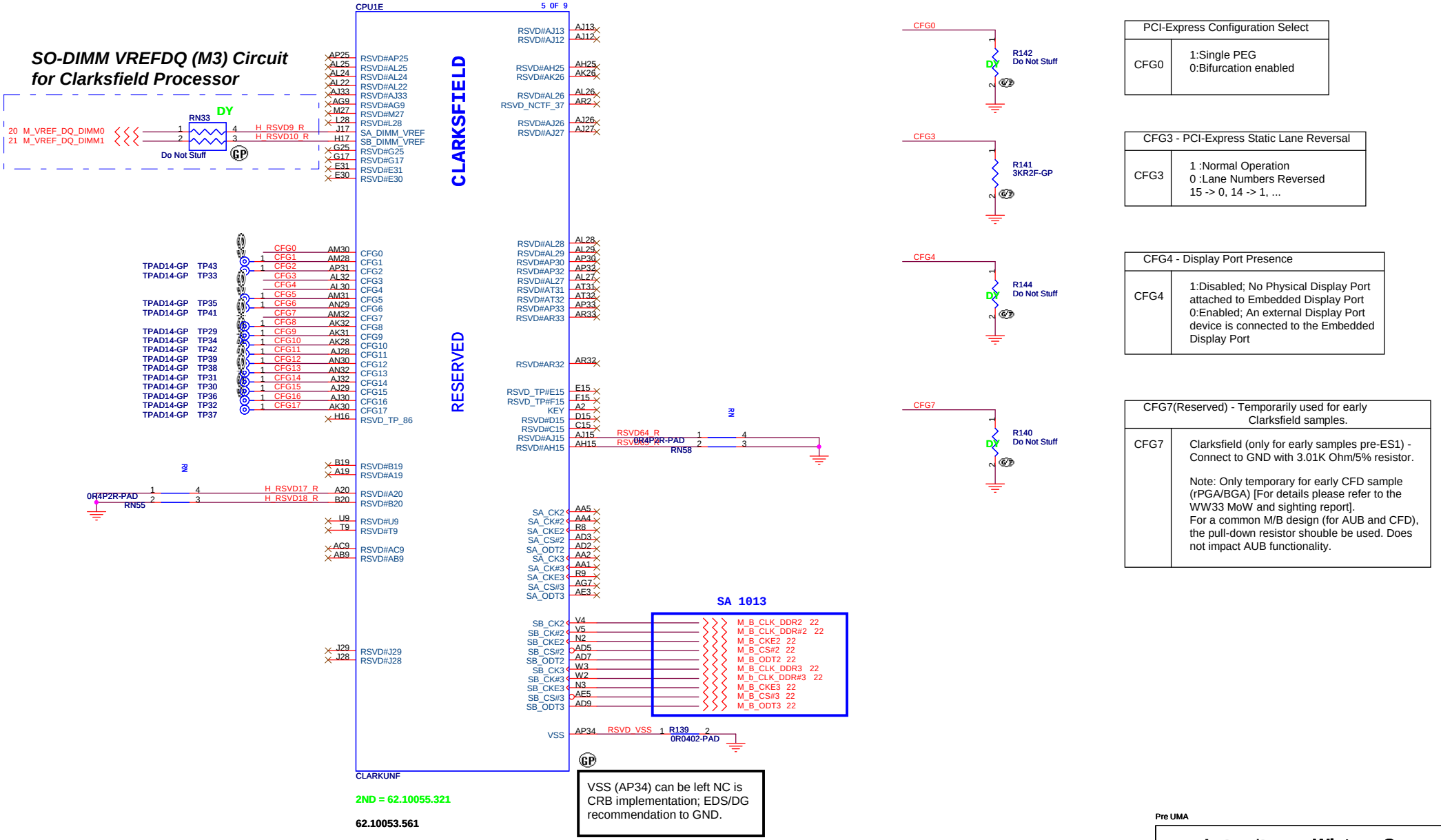
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (6/7)***

Size	Document Number	Rev
A3	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 9 of 67

SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (7/7)**

Size	Document Number	Rev
A3	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 10 of 67

integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

ICH_RTCX1 — R553 10MR2J-L-GP — ICH_RTCX2
X5 — X-32D768KHZ-34GPU — 82.30001.661 — 2nd = 82.30001.B21
C712 SC7P50V2DN-2GP — C709 SC7P50V2DN-2GP

RTC_AUX_S5 — RN22 SRN20KJ-GP-U — C315 SC1U6D3V2KX-GP
RTC_AUX_S5 — R550 1MR2J-1-GP — SM_INTRUDER#
R551 330KR2F-L-GP — ICH_INTVRMEN

ACZ_RST# — DY ECT3 — Do Not Stuff
ACZ_SYNC — DY ECT5 — Do Not Stuff
ACZ_BIT_CLK — DY ECT4 — Do Not Stuff
ACZ_SDATAOUT — DY ECT6 — Do Not Stuff

C322 SC1U6D3V2KX-GP — G121 GAP-OPEN — Close to DM1 connector
SRTCRST# new signal Pin

33 ACZ_RST#_AUDIO
33 ACZ_SYNC_AUDIO
33 ACZ_BITCLK_AUDIO
33 ACZ_SDATAOUT_AUDIO
SRN33J-4-GP — RN20 — ACZ_RST# ACZ_SYNC ACZ_BIT_CLK ACZ_SDATAOUT

1D5V_S0 — R549 — DY — Do Not Stuff — ACZ_SYNC

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.

NO REBOOT STRAP

3D3V_S0 — R583 — DY — Do Not Stuff — ACZ_SPKR

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

3D3V_S5
PCH_JTAG_TMS — R592 — Do Not Stuff
PCH_JTAG_TDO — R589 — DY — Do Not Stuff
PCH_JTAG_TDI — R591 — DY — Do Not Stuff
PCH_JTAG_RST# — R590 — DY — Do Not Stuff
PCH_JTAG_TMS — R224 — Do Not Stuff
PCH_JTAG_TDO — R221 — DY — Do Not Stuff
PCH_JTAG_TDI — R223 — DY — Do Not Stuff
PCH_JTAG_RST# — R220 — DY — Do Not Stuff
PCH_JTAG_TCK — R593 — 51R2F-2-GP

When unused all JTAG pins may be NC

SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

40 PCH_SPI_CLK — R239 15R2J-GP — SPI_CLK_R
40 PCH_SPI_CS#0 — R236 15R2J-GP — SPI_CS#0_R
40 PCH_SPI_MOSI — R238 15R2J-GP — SPI_MOSI_R
40 SPI_MOSO_R

SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required

3D3V_S0 — R219 — DY — Do Not Stuff — SPI_MOSI_R

PCH1A — 1 OF 10 — IBEXPEAK-M-GP-NF

RTC: ICH_RTCX1 B13 RTCX1; ICH_RTCX2 D13 RTCX2; ICH_RTCRST# C14 RTCRST#; SRTCRST# D17 SRTCRST#; SM_INTRUDER# A16 INTRUDER#; ICH_INTVRMEN A14 INTVRMEN

LPC: FWH0/LAD0 D33 — LPC_LAD0 39,40; FWH1/LAD1 B33 — LPC_LAD1 39,40; FWH2/LAD2 C32 — LPC_LAD2 39,40; FWH3/LAD3 A32 — LPC_LAD3 39,40; FWH4/LFRAME# C34 — LPC_LFRAME# 39,40; LDRQ0# A34; LDRQ1#/GPIO23 F34 — PCH_GPIO23 — TP52 TPAD14-GP; SERIRQ AB9 — INT_SERIRQ — INT_SERIRQ 39

IHDA: ACZ_BIT_CLK A30 HDA_BCLK; ACZ_SYNC D29 HDA_SYNC; SPKR P1 — 33 ACZ_SPKR; ACZ_RST# C30 HDA_RST#; 33 ACZ_SDATAIN0 — G30 HDA_SDIN0; ACZ_SDATAIN1 F30 HDA_SDIN1 — TPAD14-GP TP55; HDA_SDIN2 F32 — TPAD14-GP TP54; F32 HDA_SDIN3; ACZ_SDATAOUT B29 HDA_SDO

SATA: 39 ME_UNLOCK# — R182 0R0402-PAD — HDA_DOCK_EN# H32 HDA_DOCK_EN#/GPIO33; R186 — DY — Do Not Stuff — J30 HDA_DOCK_RST#/GPIO13

SATA0RXN AK7 — SATA_RXN0 27; SATA0RXP AK6 — SATA_RXP0 27; SATA0TXN AK11 — SATA_TXN0 27; SATA0TXP AK9 — SATA_TXP0 27 — **HDD**
SATA1RXN AH6; SATA1RXP AH5; SATA1TXN AH9; SATA1TXP AH8
SATA2RXN AF11; SATA2RXP AF9; SATA2TXN AF7; SATA2TXP AF6
SATA3RXN AH3; SATA3RXP AH1; SATA3TXN AF3; SATA3TXP AF1
SATA4RXN AD9 — SATA_RXN4 28; SATA4RXP AD8 — SATA_RXP4 28; SATA4TXN AD6 — SATA_TXN4 28; SATA4TXP AD5 — SATA_TXP4 28 — **ODD**
SATA5RXN AD3; SATA5RXP AD1; SATA5TXN AB3; SATA5TXP AB1

JTAG: PCH_JTAG_TCK M3 JTAG_TCK; PCH_JTAG_TMS K3 JTAG_TMS; PCH_JTAG_TDI K1 JTAG_TDI; PCH_JTAG_TDO J2 JTAG_TDO; PCH_JTAG_RST# J4 TRST#

SPI: SPI_CLK BA2; SPI_CS0# AV3; SPI_CS1# AY3; SPI_MOSI AY1; SPI_MISO AV1

SATAICOMPO AF16; SATAICOMPI AF15 — SATAICOMP — R192 37D4R2F-GP — 1D05V_S0
SATALED# T3 — SATA_LED# — SATA_LED# 42
SATA0GP/GPIO21 Y9 — SATA_DET#0_R
SATA1GP/GPIO19 V1 — SATA_DET#1_R

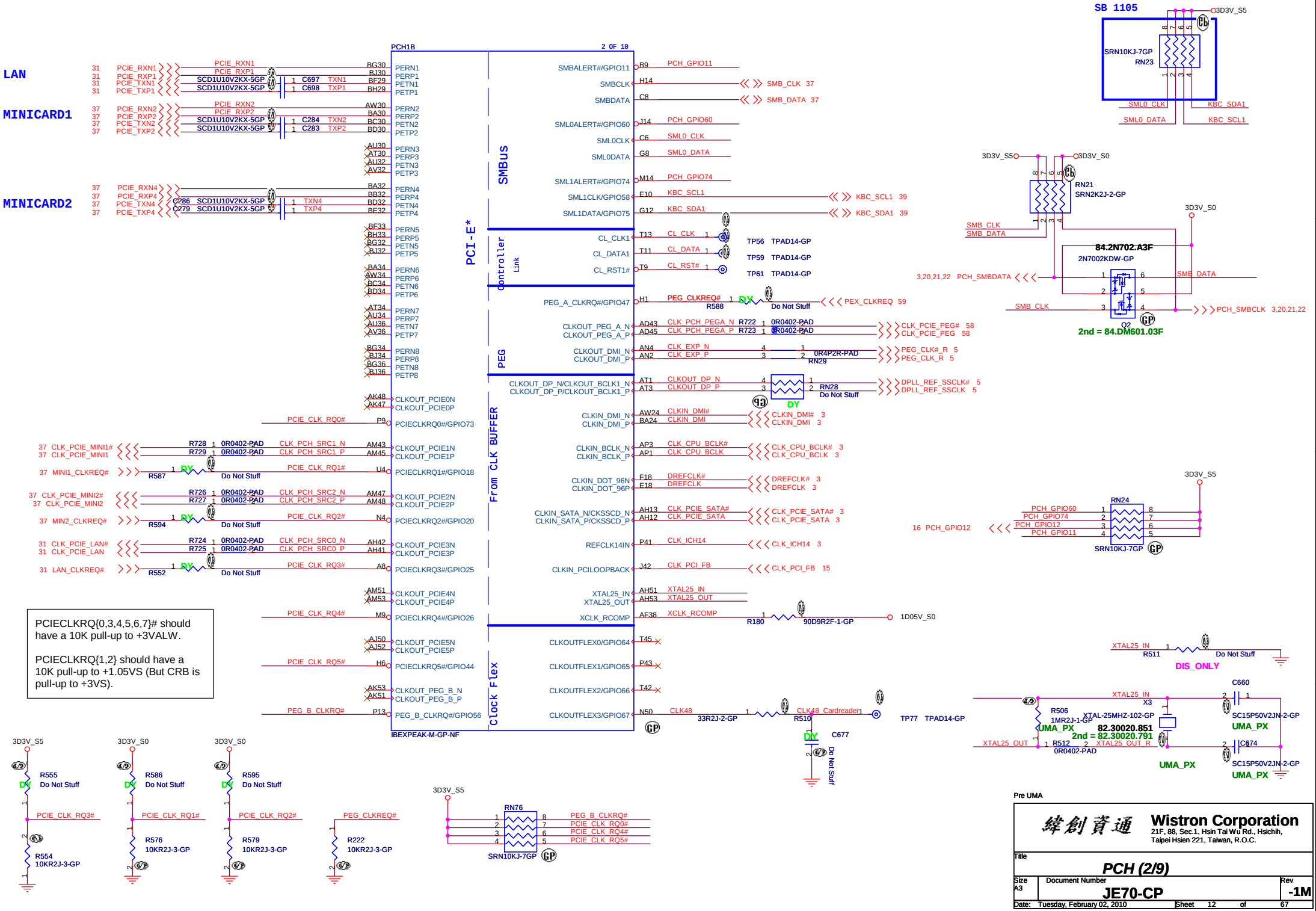
RN26 — SRN10KJ-7GP — 3D3V_S0
SATA_DET#0_R
SATA_LED#
SATA_DET#1_R
INT_SERIRQ

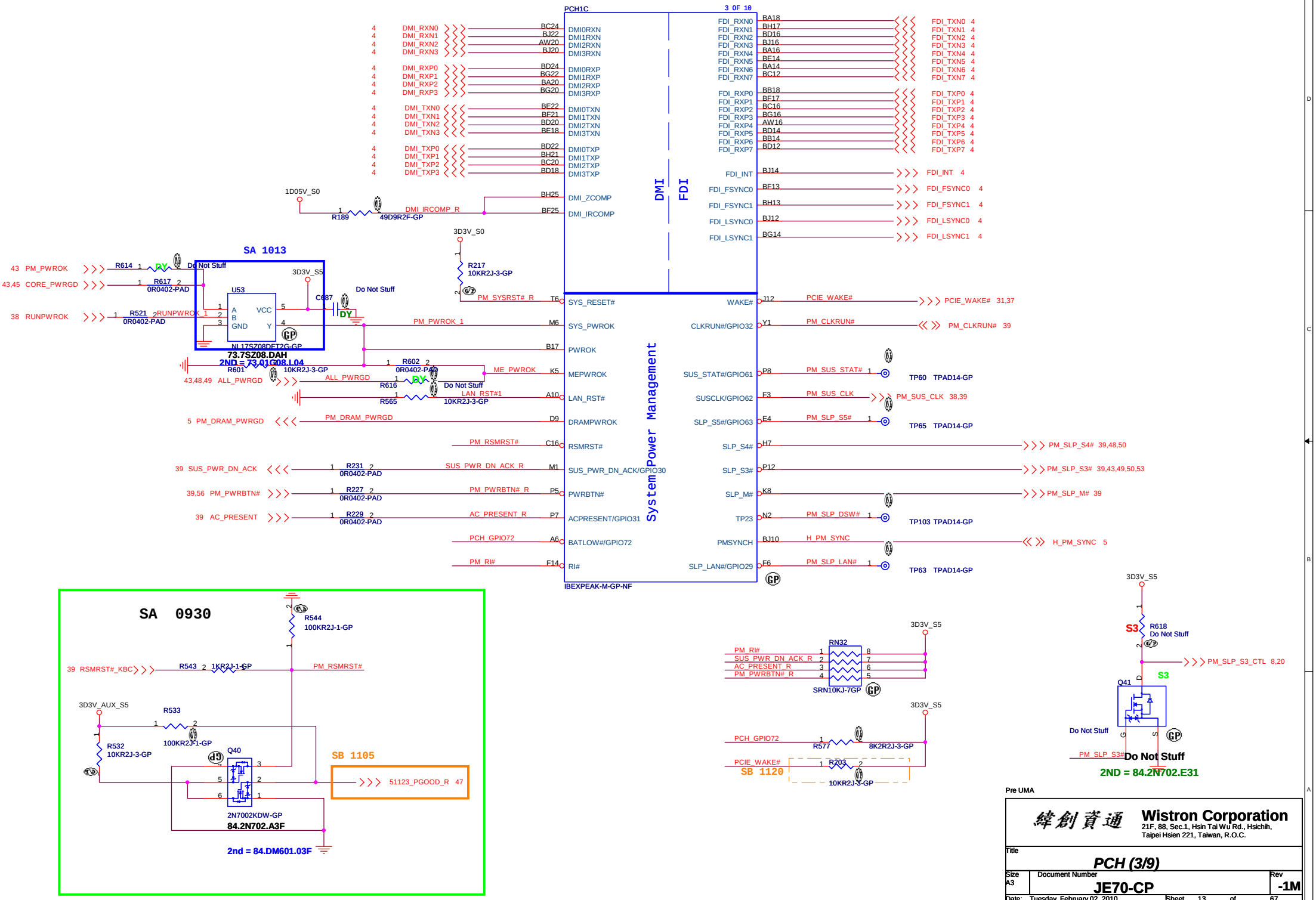
RTC_AUX_S5 — R339 0R0603-PAD — RTC_PWR_L — C459 SC1U10V2ZY-GP
3D3V_AUX_S5 — D8 BAS40CW-GP — 83.00040.E81 — 2nd = 83.00040.M81
RTC_PWR — R331 1KR2J-1-GP — RTC_BAT — RTC1 BAT-CON2-1-GP-U — 62.70001.011 — 2nd = 62.70001.041

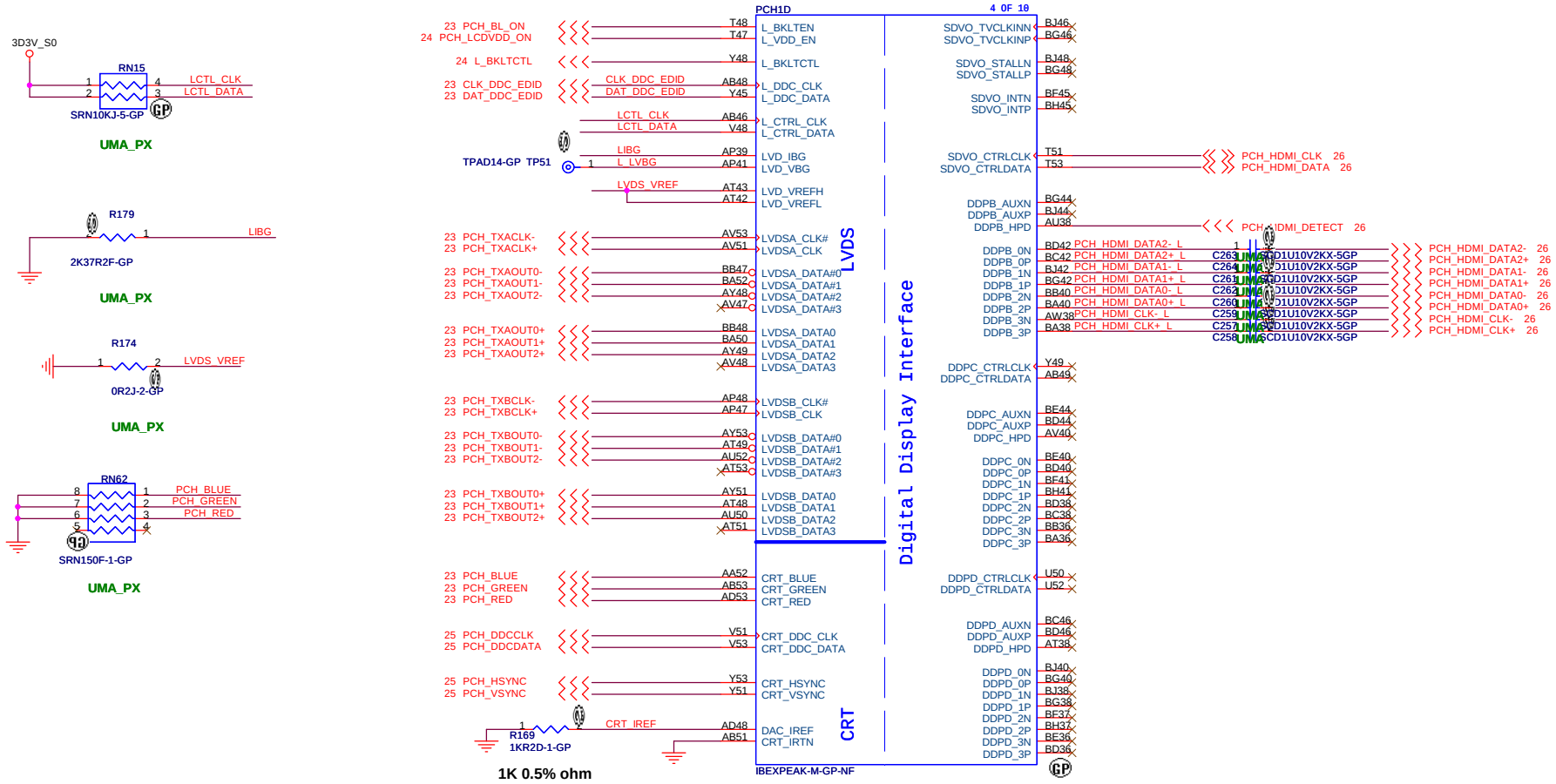
Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (1/9)
Size: A3 | Document Number: JE70-CP | Rev: -1M
Date: Tuesday, February 02, 2010 | Sheet 11 of 67


LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
SB 1105
SRN10KJ-7GP
RN23
SML0_CLK
SML0_DATA
KBC_SDA1
KBC_SCL1
RN21
SRN2K2J-2-GP
84.2N702.A3F
2N7002KDW-GP
Q2
2nd = 84.DM601.03F
RN24
SRN10KJ-7GP
PCH_GPIO60
PCH_GPIO74
PCH_GPIO12
PCH_GPIO11
RN76
SRN10KJ-7GP
PEG_B_CLKRQ#
PCIE_CLK_RQ0#
PCIE_CLK_RQ4#
PCIE_CLK_RQ5#
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
Pre UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (2/9)
Size A3
Document Number
JE70-CP
Rev
-1M
Date: Tuesday, February 02, 2010
Sheet 12 of 67


PCH1C
3 OF 10
DMI
FDI
System Power Management
IBEXPEAK-M-GP-NF
SA 1013
SA 0930
SB 1105
SB 1120
Do Not Stuff
73.7SZ08.DAH
2ND = 73.01G08.L04
84.2N702.A3F
2nd = 84.DM601.03F
2ND = 84.2N702.E31
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (3/9)
JE70-CP
-1M
Date: Tuesday, February 02, 2010
Sheet 13 of 67



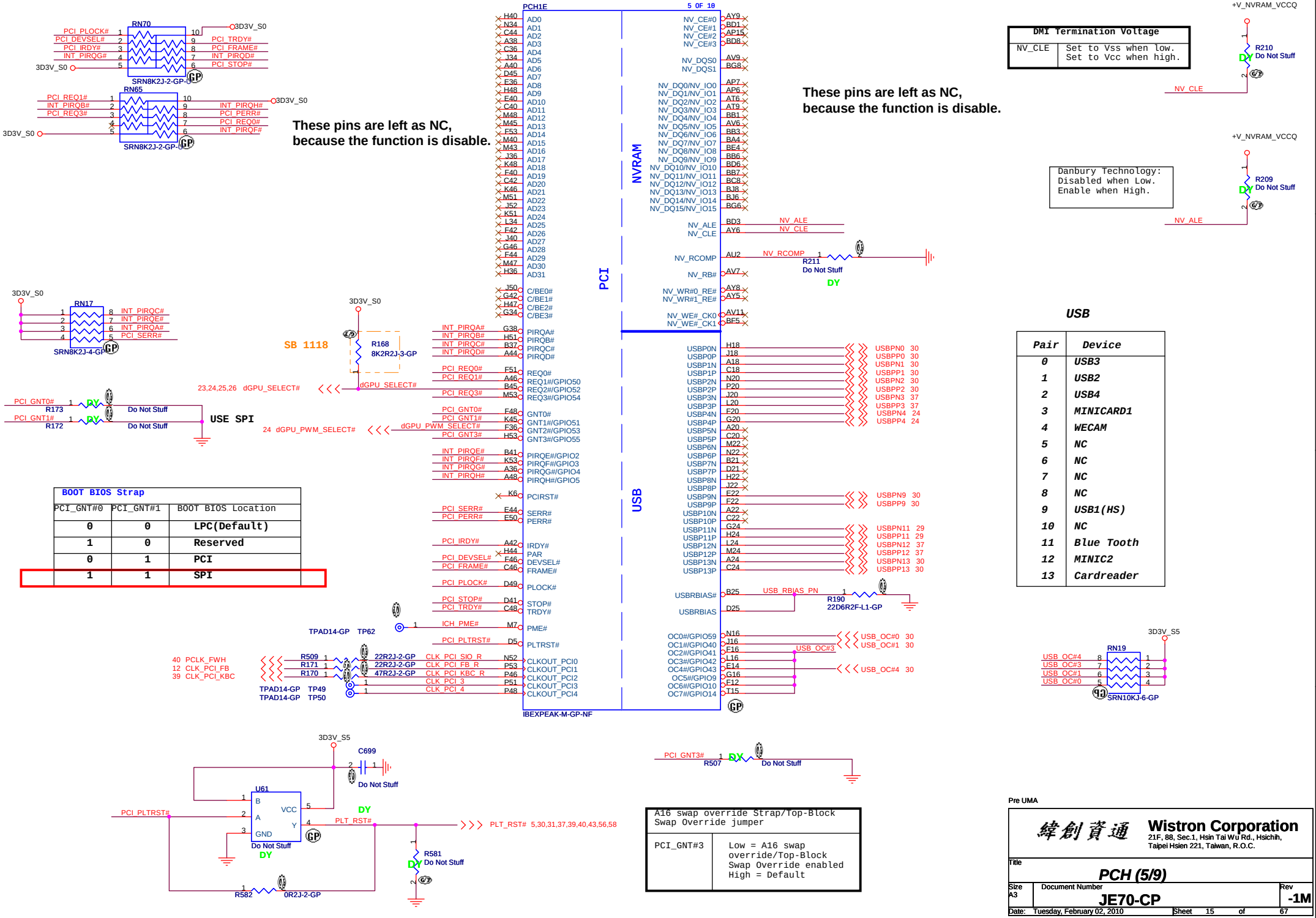
Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (4/9)***

Size	Document Number	Rev
A3	JE70-CP	-1M

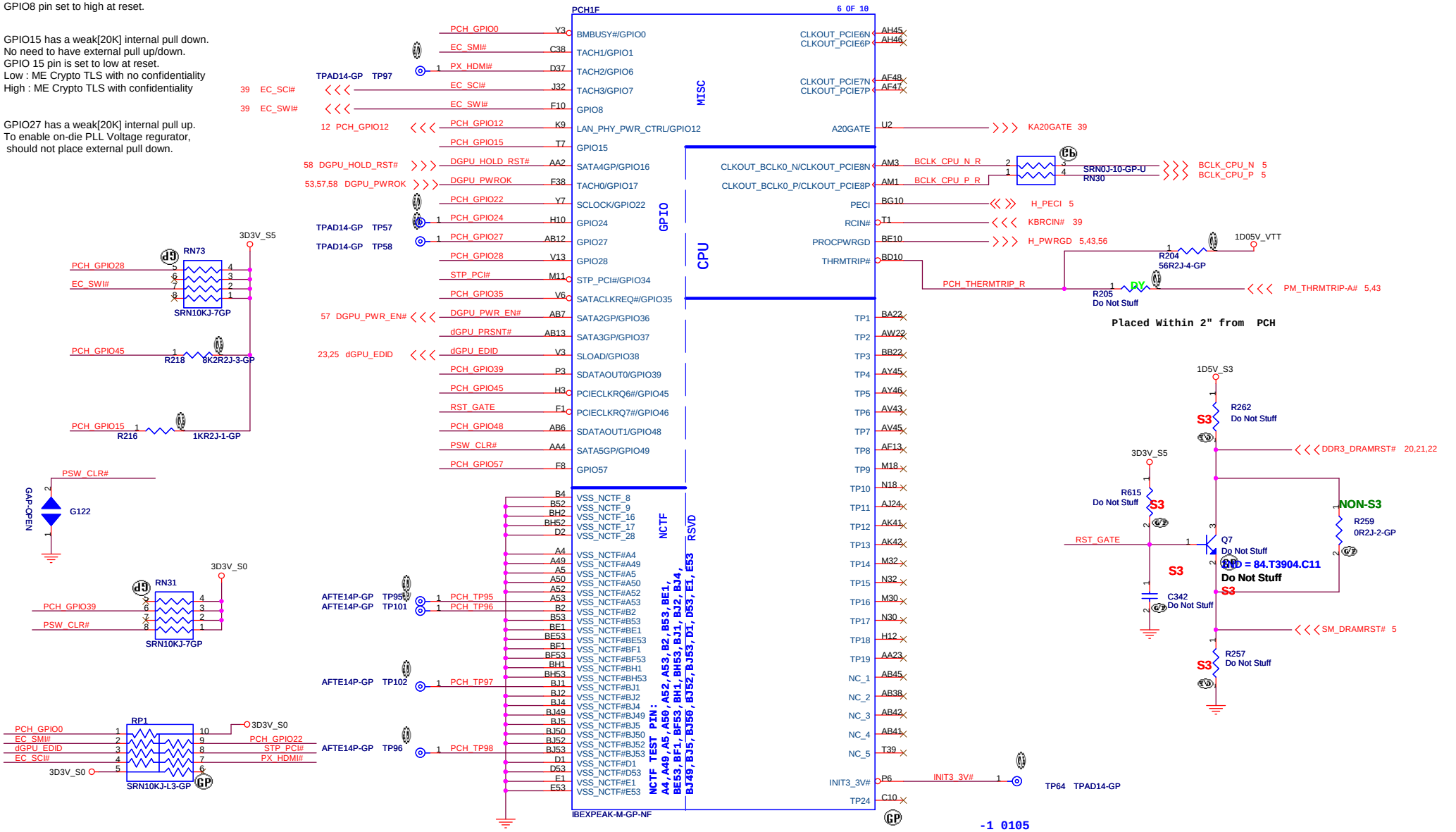
Date: Tuesday, February 02, 2010 Sheet 14 of 67


PCH1E
5 OF 10
PCI
NVRAM
USB
IBEXPEAK-M-GP-NF
RN70
SRN8K2J-2-GP-U
RN65
SRN8K2J-2-GP-U
These pins are left as NC, because the function is disable.
These pins are left as NC, because the function is disable.
DMI Termination Voltage
NV_CLE | Set to Vss when low. Set to Vcc when high.
Danbury Technology: Disabled when Low. Enable when High.
R210 Do Not Stuff
R209 Do Not Stuff
R211 Do Not Stuff
RN17
SRN8K2J-4-GP
SB 1118
R168 8K2R2J-3-GP
USE SPI
R173 Do Not Stuff
R172 Do Not Stuff
USB
Pair | Device
0 | USB3
1 | USB2
2 | USB4
3 | MINICARD1
4 | WECAM
5 | NC
6 | NC
7 | NC
8 | NC
9 | USB1(HS)
10 | NC
11 | Blue Tooth
12 | MINIC2
13 | Cardreader
BOOT BIOS Strap
PCI_GNT#0 | PCI_GNT#1 | BOOT BIOS Location
0 | 0 | LPC(Default)
1 | 0 | Reserved
0 | 1 | PCI
1 | 1 | SPI
R190 22D6R2F-L1-GP
RN19
SRN10KJ-6-GP
C699 Do Not Stuff
U61
R581 Do Not Stuff
R582 0R2J-2-GP
R507 Do Not Stuff
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3 | Low = A16 swap override/Top-Block Swap Override enabled High = Default
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: PCH (5/9)
Size: A3
Document Number: JE70-CP
Rev: -1M
Date: Tuesday, February 02, 2010
Sheet 15 of 67

GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

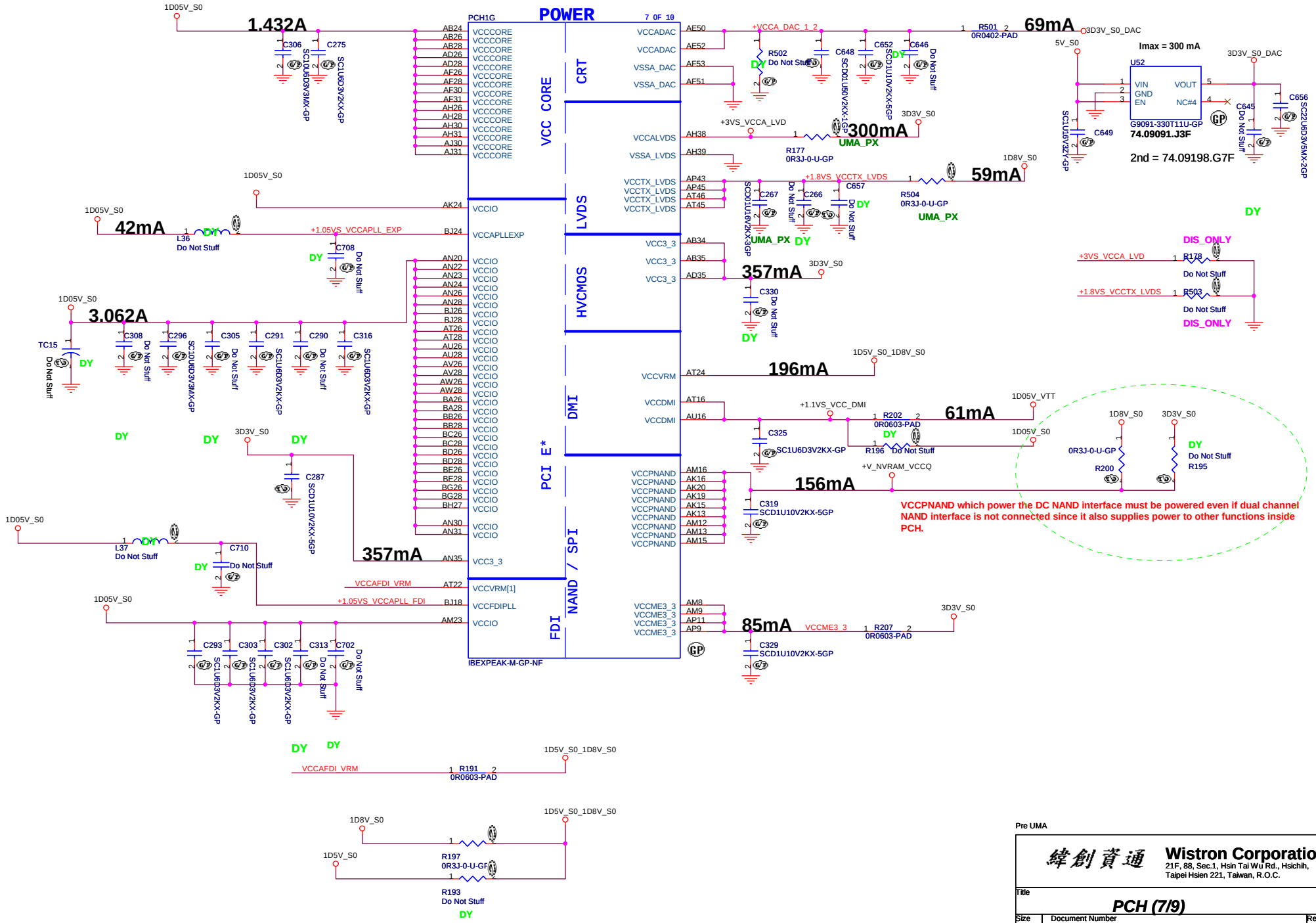
GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

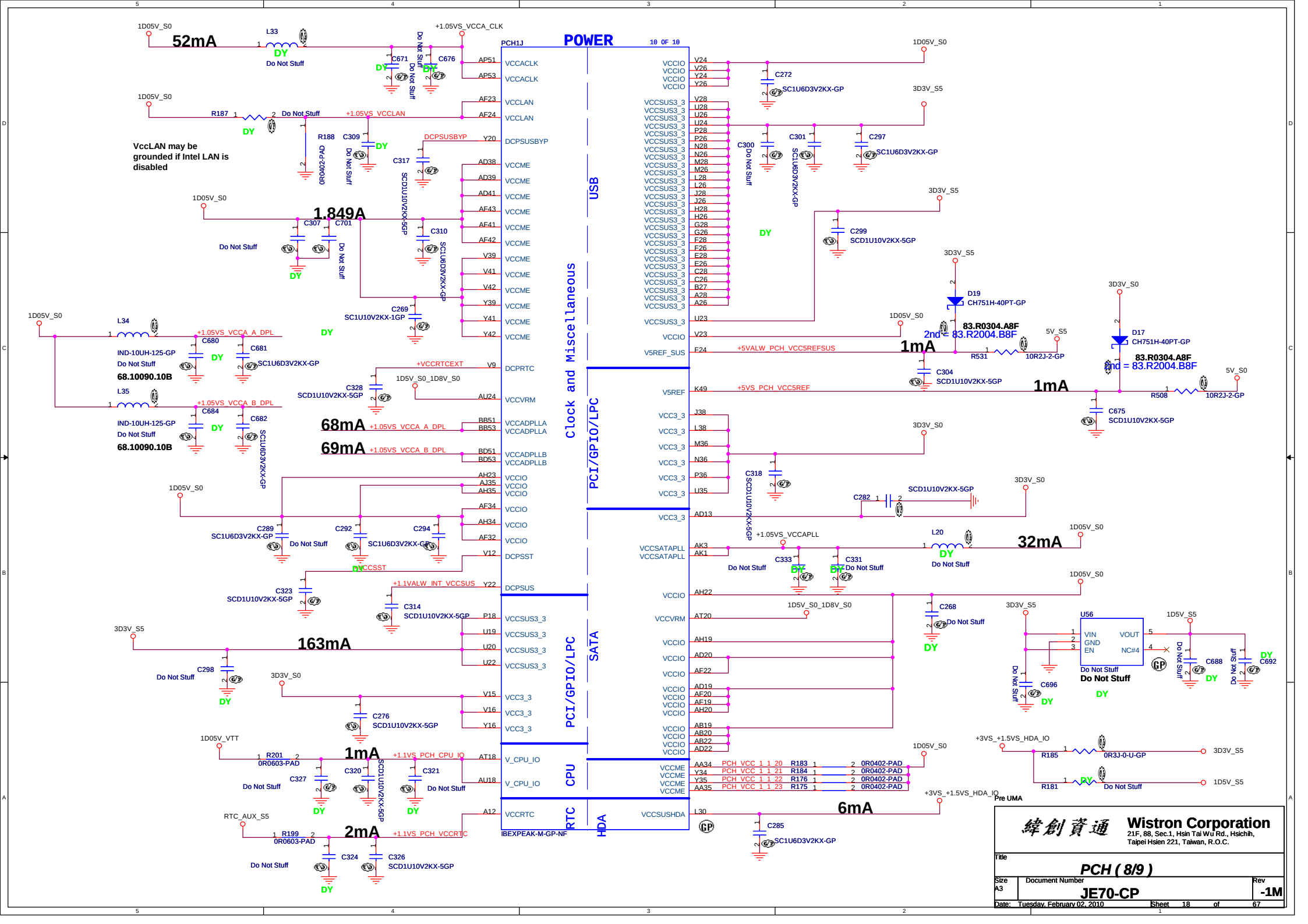
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

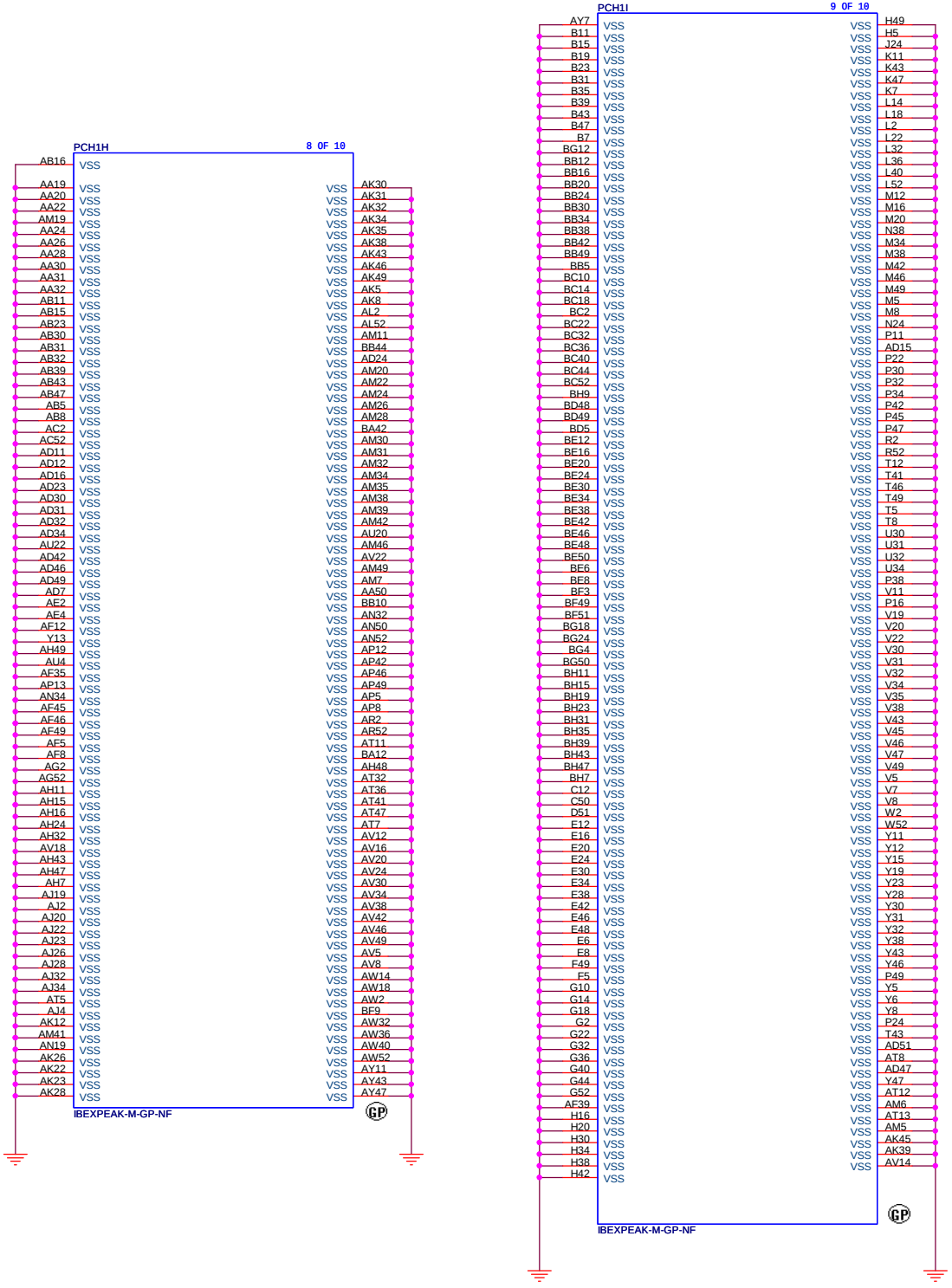


Pre UMA

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (6/9)		
Size: A3	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 16 of 67	


POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.432A
3.062A
42mA
357mA
196mA
61mA
156mA
85mA
69mA
300mA
59mA
357mA
Imax = 300 mA
G9091-330T11U-GP
74.09091.J3F
2nd = 74.09198.G7F
UMA_PX
DIS_ONLY
DY
Do Not Stuff
IBEXPEAK-M-GP-NF
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (7/9)
Size A3
Document Number
JE70-CP
Rev -1M
Date: Tuesday, February 02, 2010
Sheet 17 of 67


POWER
10 OF 10
PCH1J
IBEXPEAK-M-GP-NF
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
52mA
1.849A
163mA
68mA
69mA
1mA
32mA
6mA
2mA
VccLAN may be grounded if Intel LAN is disabled
Do Not Stuff
DY
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (8/9)
Size A3
Document Number
JE70-CP
Rev
-1M
Date: Tuesday, February 02, 2010
Sheet 18 of 67



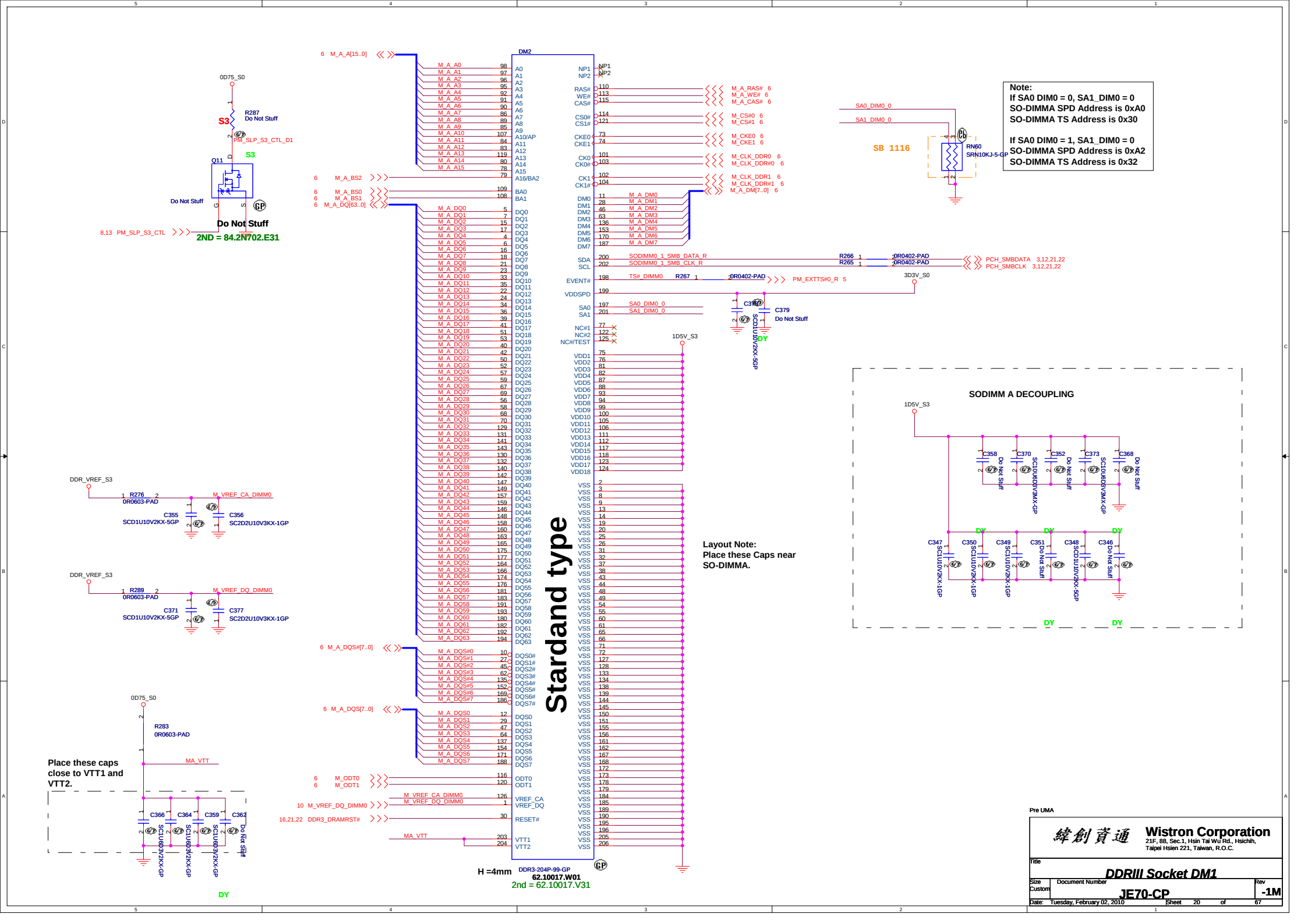
Pre UMA

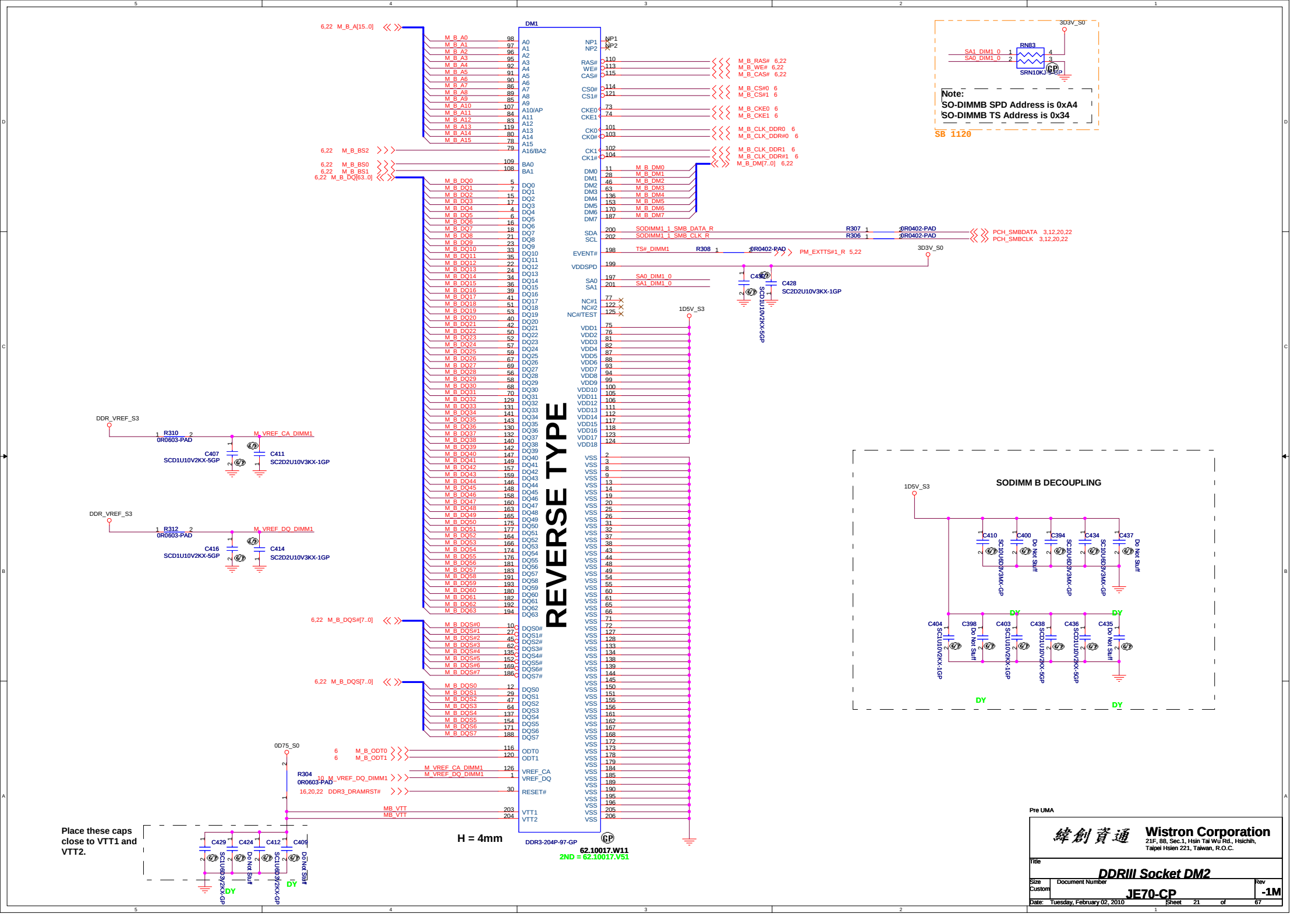
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

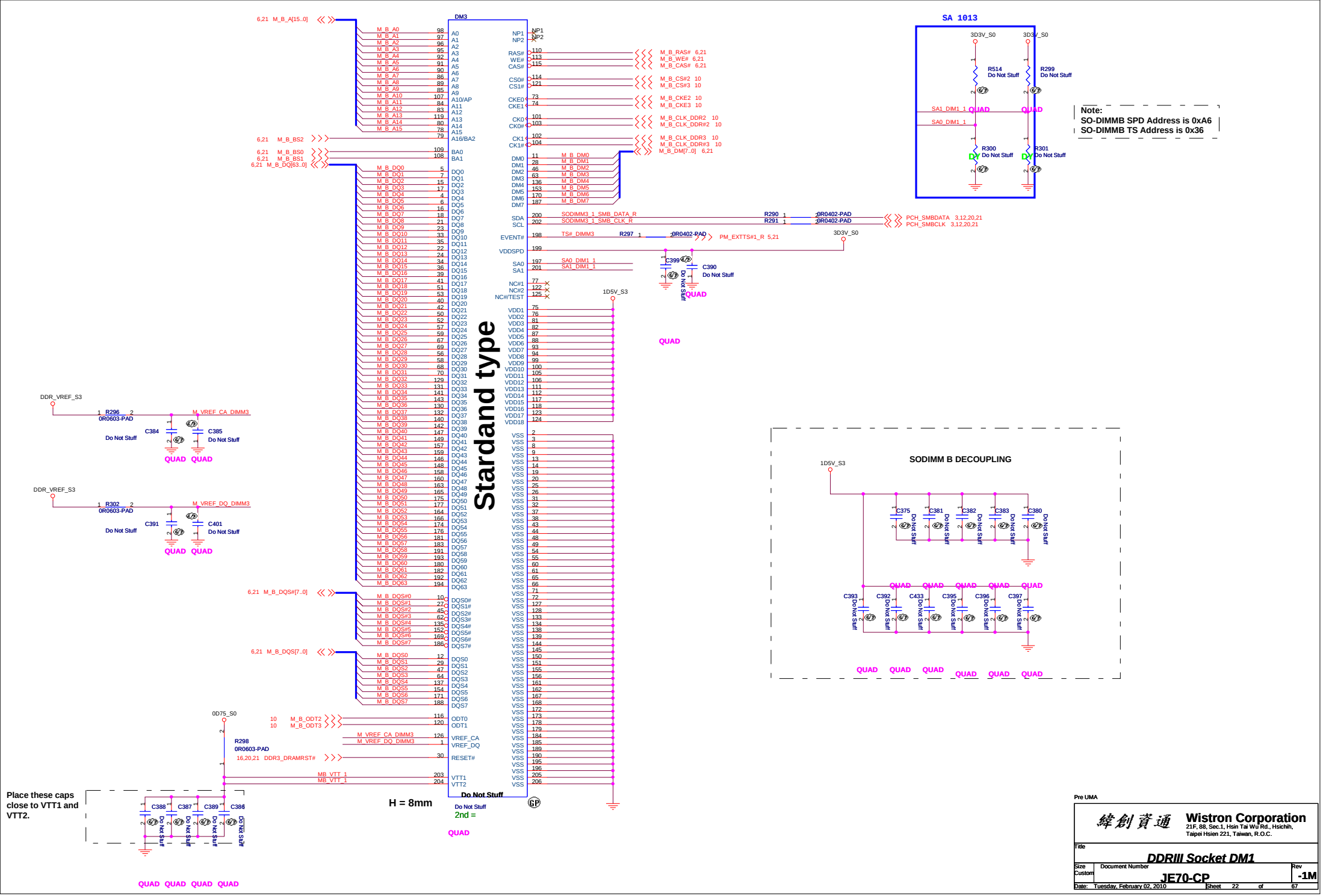
Title: ***PCH (9/9)***

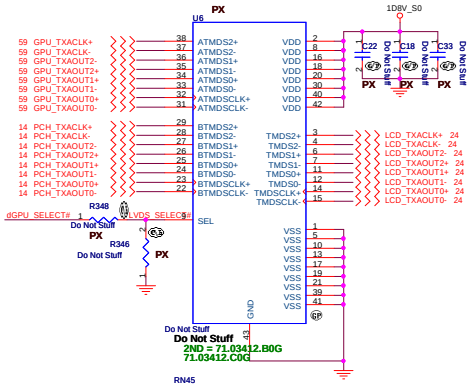
Size	Document Number	Rev
A3	**JE70-CP**	**-1M**

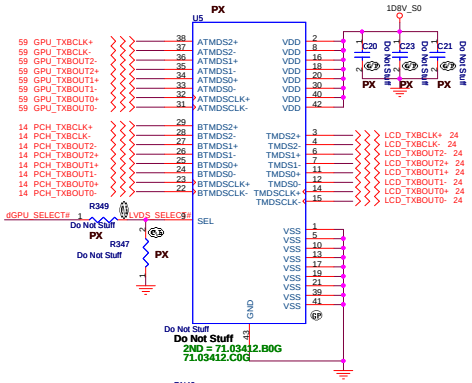
Date: Tuesday, February 02, 2010 Sheet 19 of 67

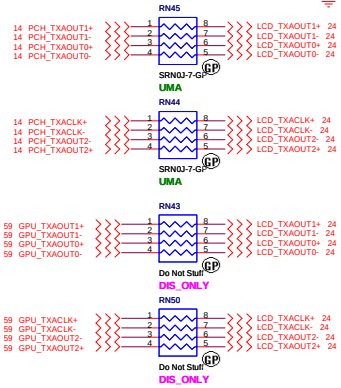

DM2
Stardand type
H =4mm
DDR3-204P-99-GP
62.10017.W01
2nd = 62.10017.V31
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
SB 1116
SODIMM A DECOUPLING
Layout Note:
Place these Caps near
SO-DIMMA.
Place these caps
close to VTT1 and
VTT2.
Do Not Stuff
2ND = 84.2N702.E31
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRIII Socket DM1
JE70-CP
-1M
Tuesday, February 02, 2010
Sheet 20 of 67

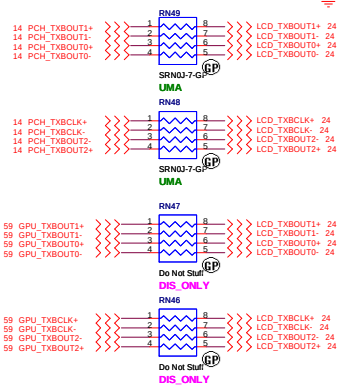

DM1
REVERSE TYPE
DDR3-204P-97-GP
62.10017.W11
2ND = 62.10017.V51
H = 4mm
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SB 1120
SODIMM B DECOUPLING
Place these caps close to VTT1 and VTT2.
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
DDRIII Socket DM2
JE70-CP
-1M
Tuesday, February 02, 2010
21
67

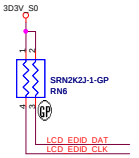

DM3
Stardand type
SA 1013
Note:
SO-DIMMB SPD Address is 0xA6
SO-DIMMB TS Address is 0x36
SODIMM B DECOUPLING
Place these caps close to VTT1 and VTT2.
H = 8mm
Do Not Stuff
2nd =
QUAD
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRIII Socket DM1
Size
Custom
Document Number
JE70-CP
Rev
-1M
Date: Tuesday, February 02, 2010
Sheet 22 of 67

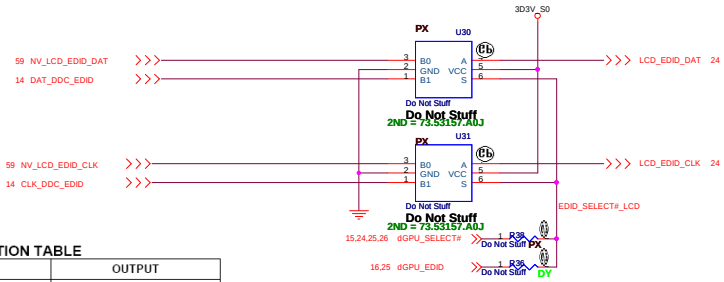






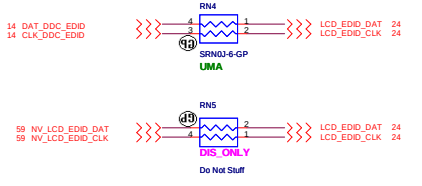


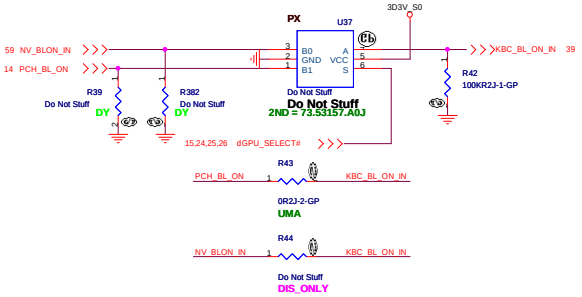


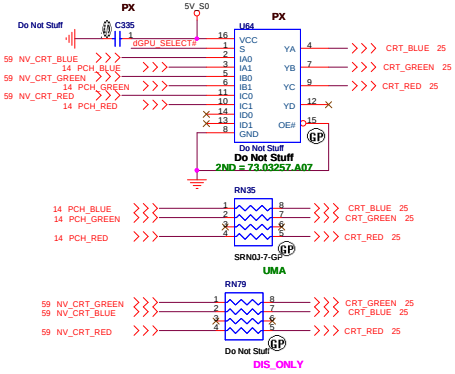


FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-







$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

Pre UMA

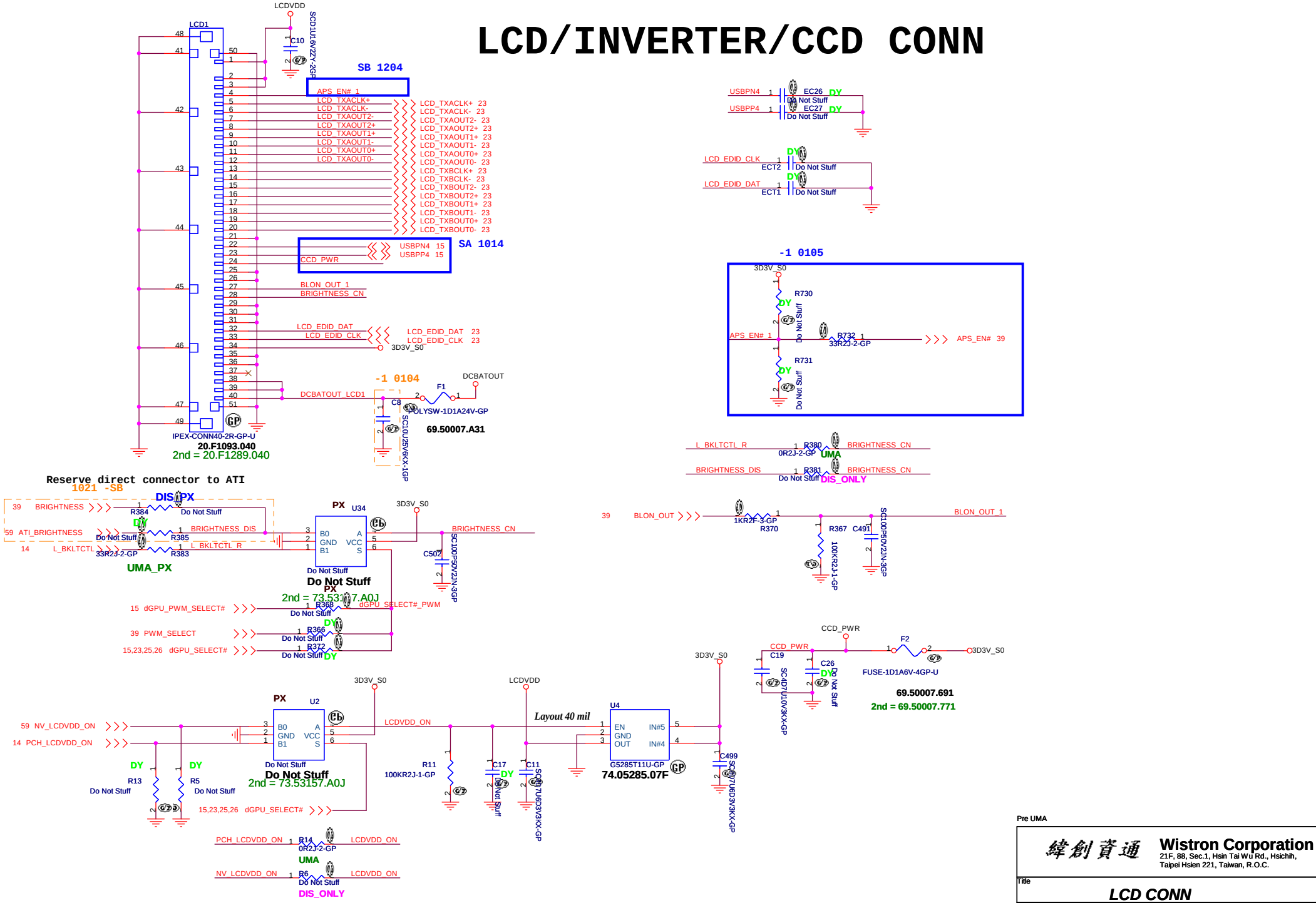
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PX SWITCH**

Size: A2 | Document Number: **JE70-CP** | Rev: **-1M**

Date: Tuesday, February 02, 2010 | Sheet 23 of 67

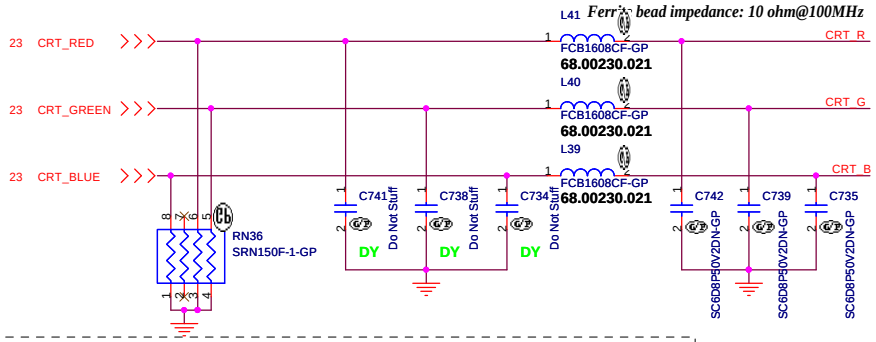
LCD/INVERTER/CCD CONN



Pre UMA

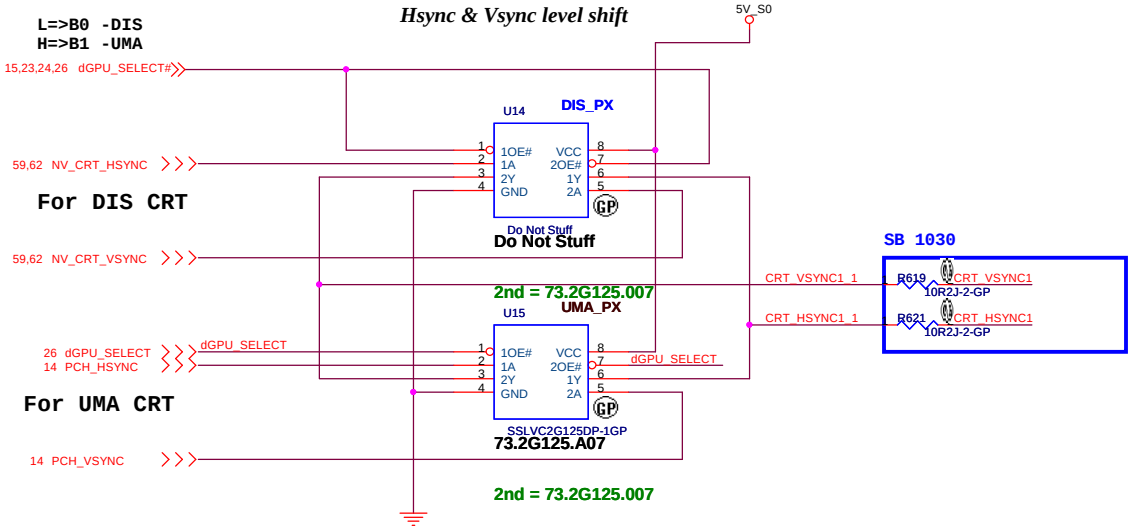
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LCD CONN***	
Size	Document Number **JE70-CP**	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 24 of 67	

Layout Note:
Place these resistors close to the CRT-out connector

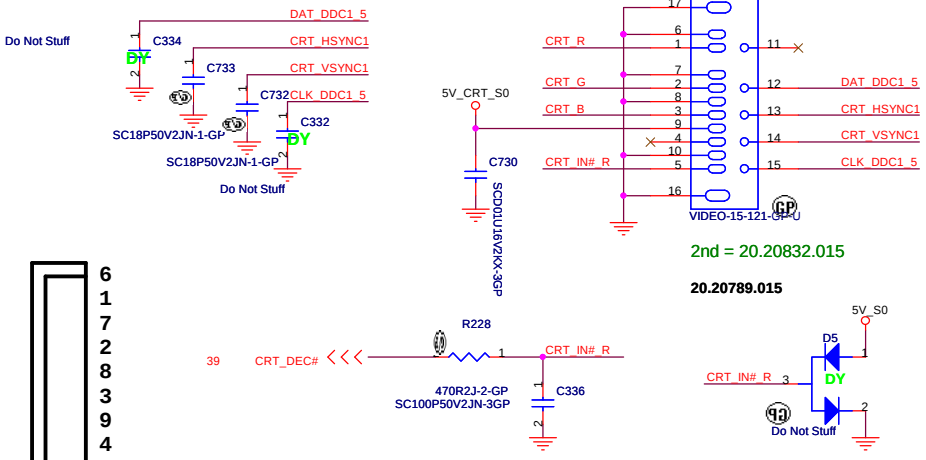


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

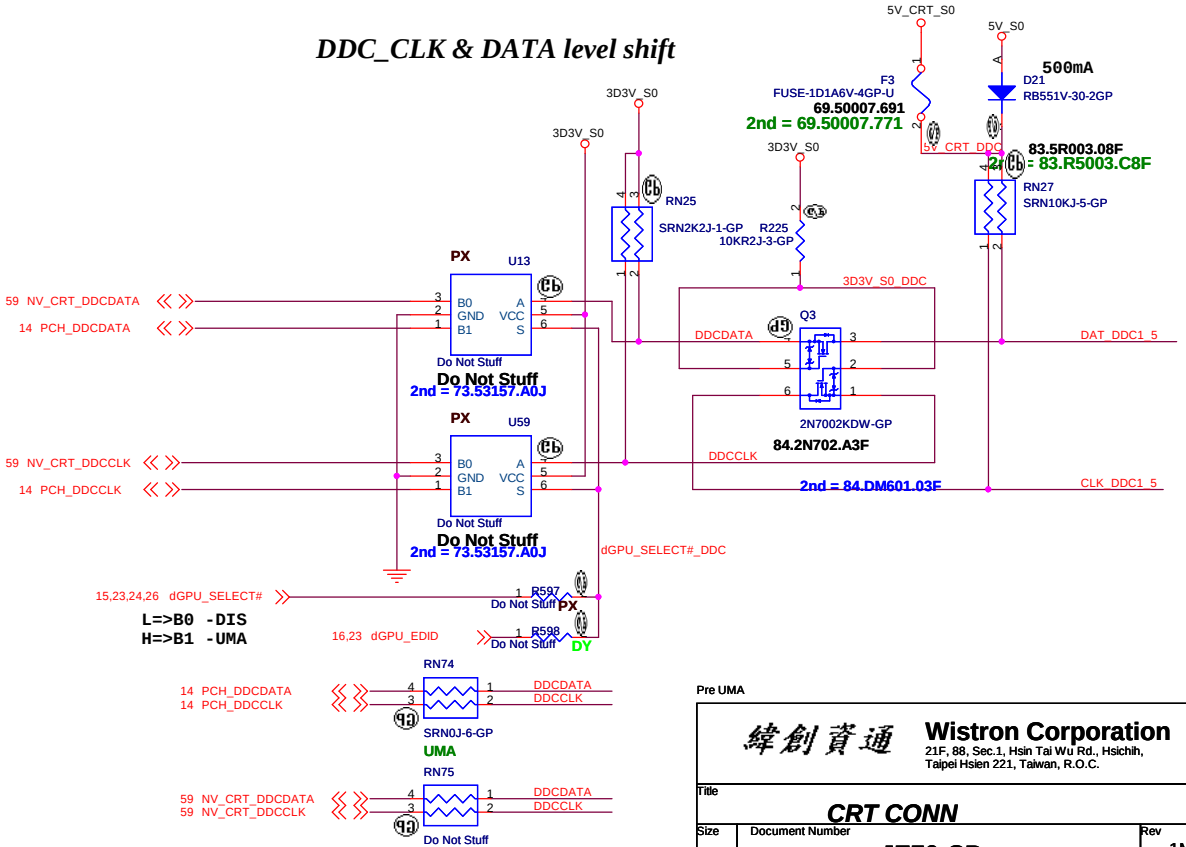
Hsync & Vsync level shift



CRT I/F & CONNECTOR



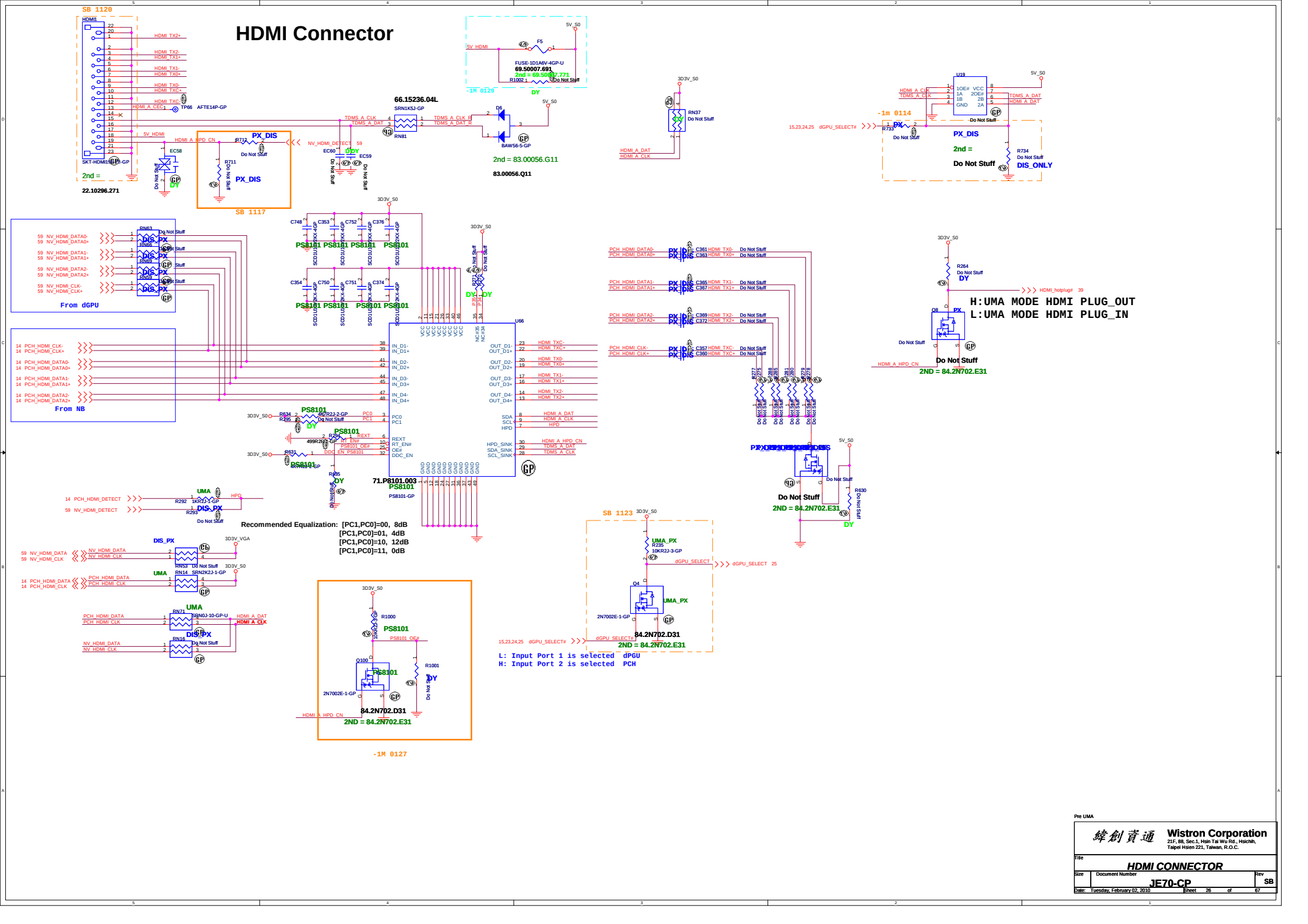
DDC_CLK & DATA level shift



Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT CONN***	
Size	Document Number **JE70-CP**	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 25 of 67	

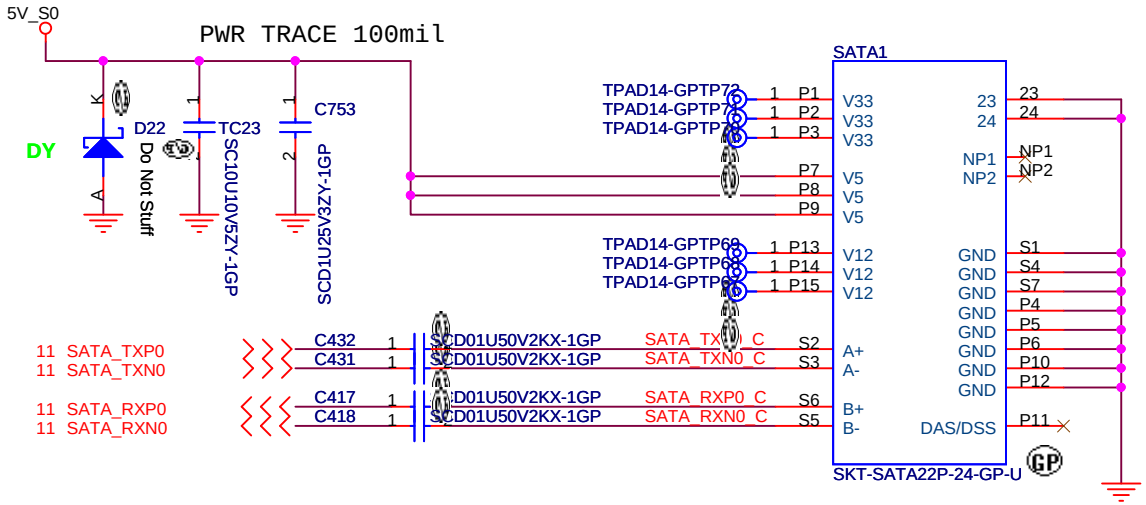
HDMI Connector



Pre UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDMI CONNECTOR	
Size	Document Number: JE70-CP	Rev: SB
Date: Tuesday, February 02, 2010	Sheet 26 of 67	

SATA Connector



2nd = 20.F1212.022

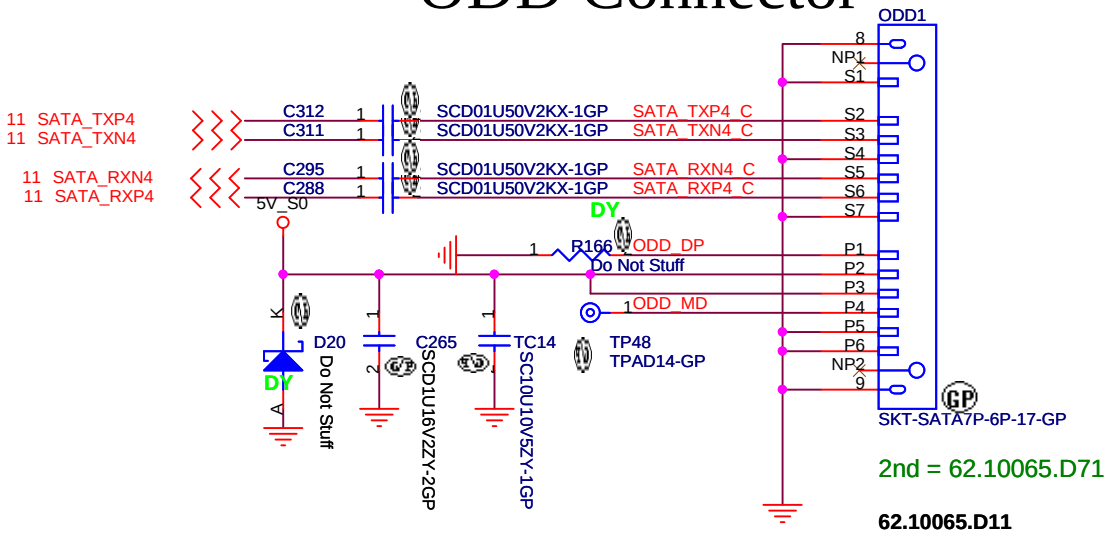
20.F1265.022

Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***HDD CONN***	
Size	Document Number **JE70-CP**	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 27 of 67	

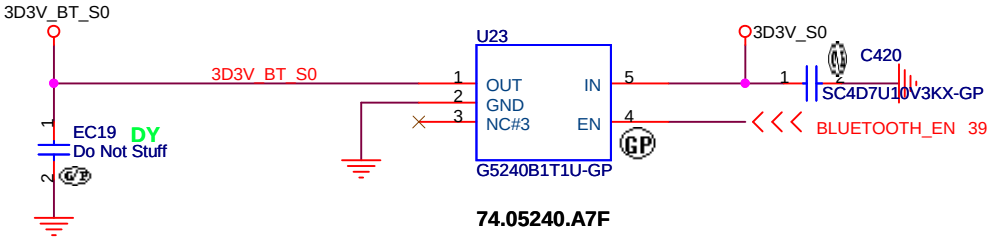
ODD Connector



Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***ODD***	
Size	Document Number **JE70-CP**	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 28 of 67	

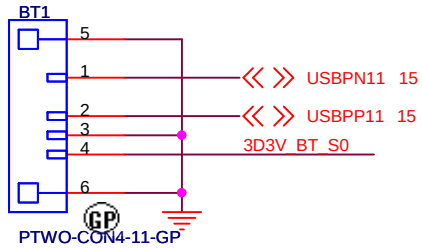
BLUETOOTH MODULE



74.05240.A7F

2nd = 74.09711.A7F

EC20 put near BLUE1 / all USB put one choke near connector by EMI request



20.F1561.004

2nd = 20.F1621.004

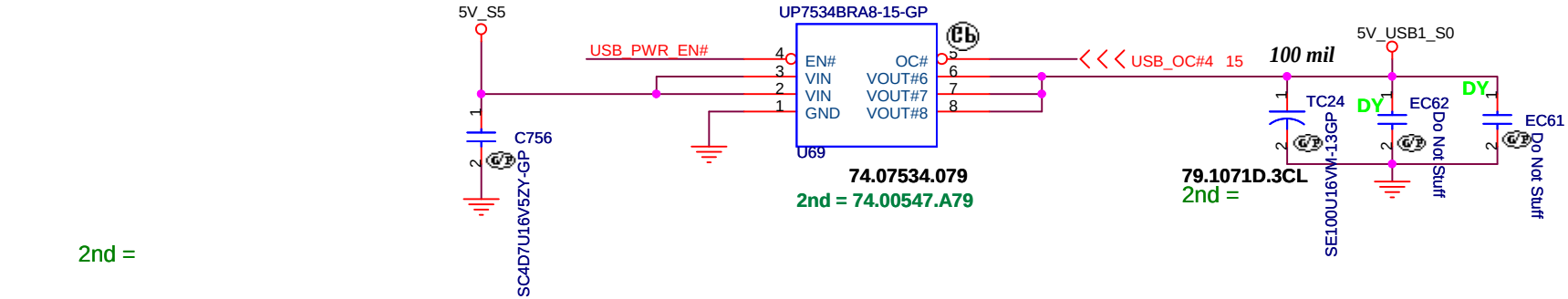
Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLUETOOTH

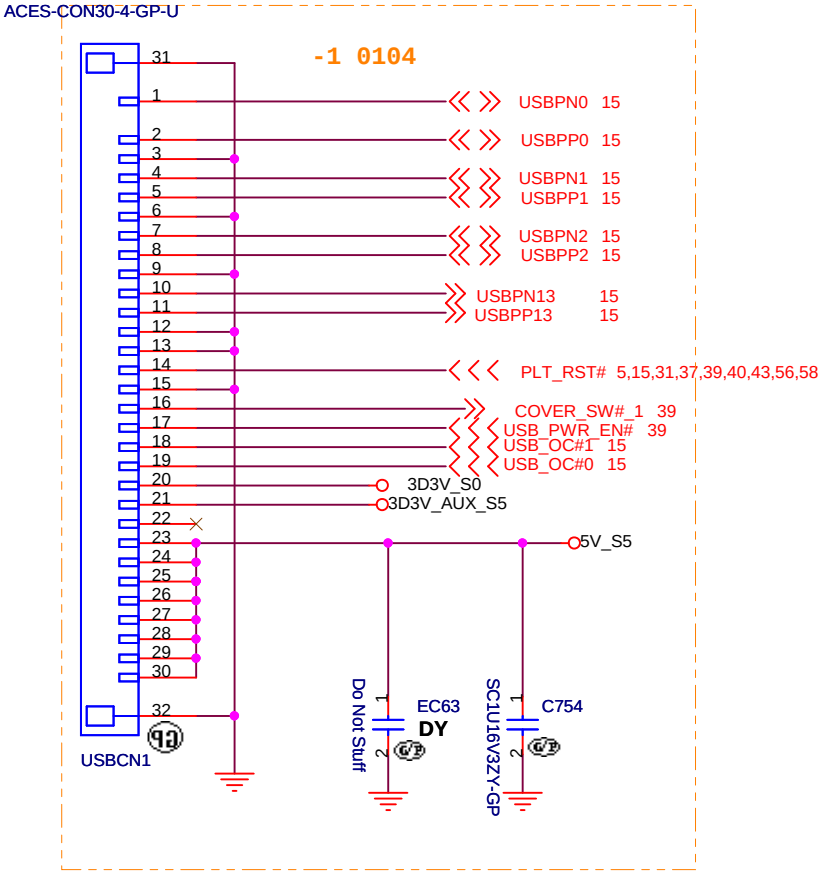
Size | Document Number: JE70-CP | Rev: -1M

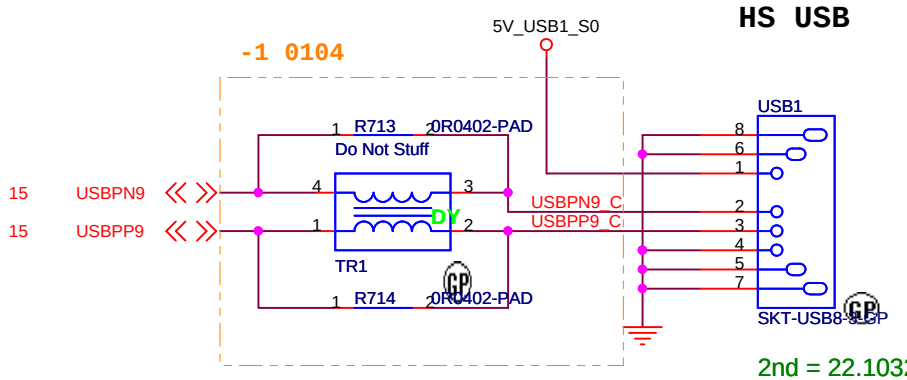
Date: Tuesday, February 02, 2010 | Sheet 29 of 67



2nd =

20.K0276.030





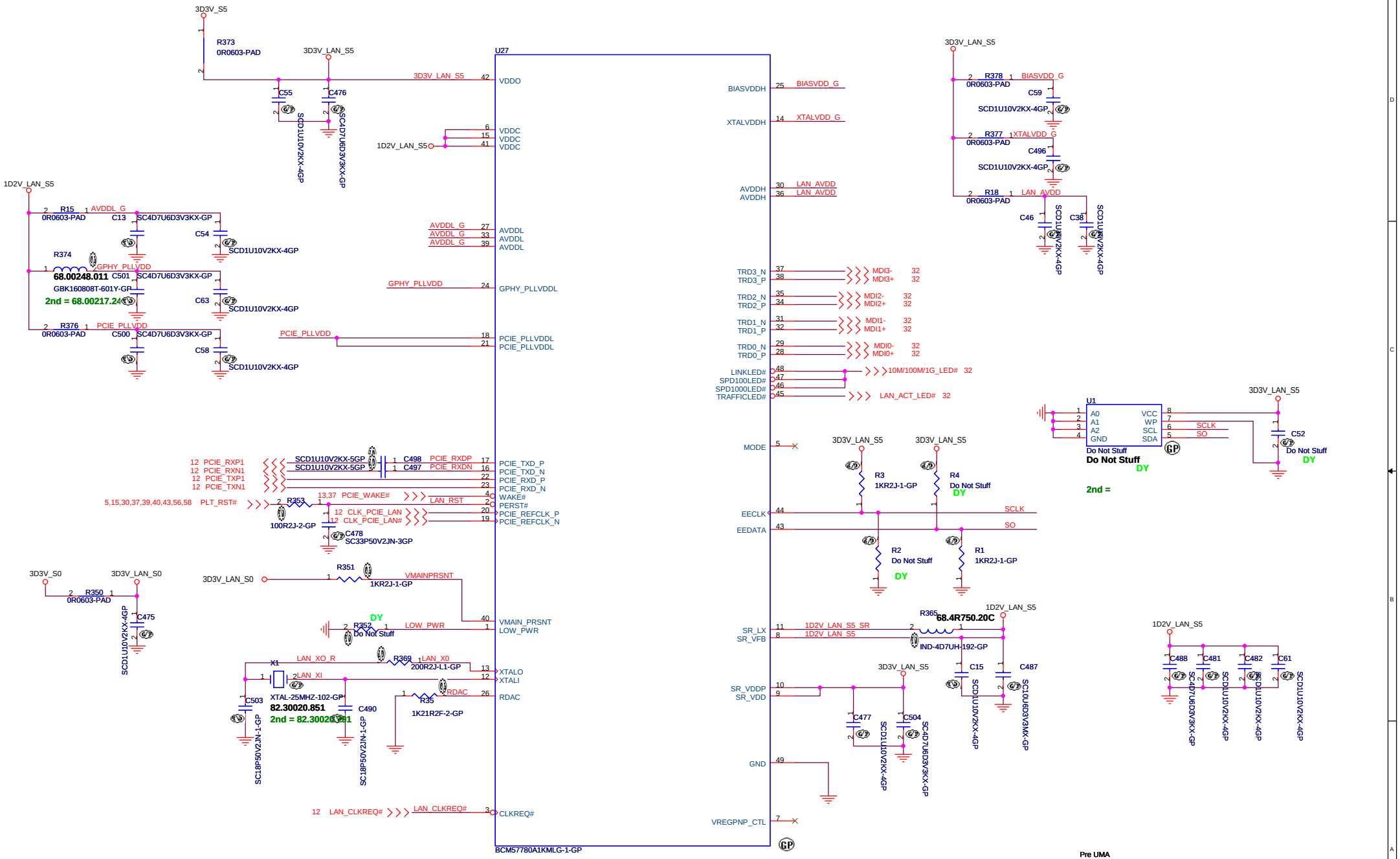
2nd = 22.10321.C41

22.10321.B81

Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

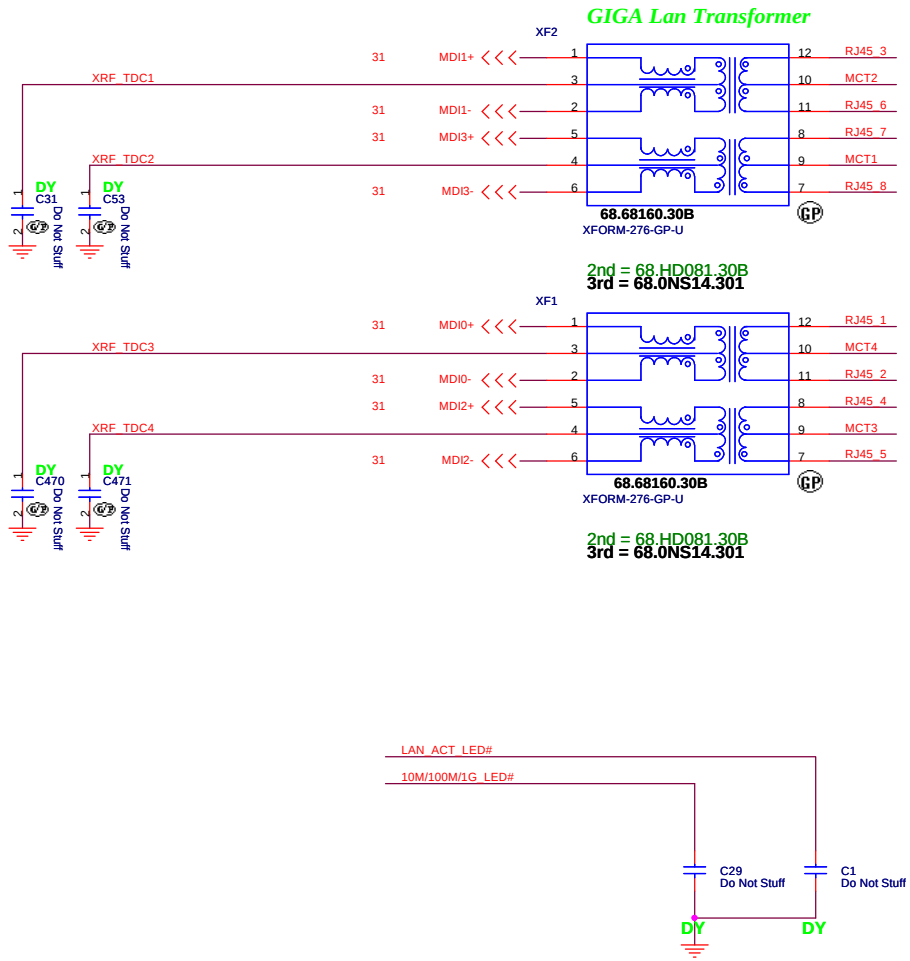
Title	*USB CONN*	
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 30 of 67	

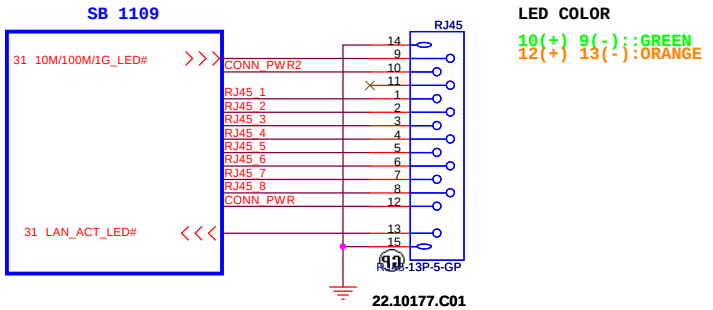

U27
BCM57780A1KMLG-1-GP
71.57780.M04
3D3V_S5
3D3V_LAN_S5
1D2V_LAN_S5
3D3V_S0
3D3V_LAN_S0
R373 0R0603-PAD
R15 0R0603-PAD
R374
68.00248.011
GBK160808T-601Y-GP
2nd = 68.00217.241
R376 0R0603-PAD
R350 0R0603-PAD
R351 1KR2J-1-GP
R352 Do Not Stuff
R353 100R2J-2-GP
R369 200R2J-L1-GP
XTAL-25MHZ-102-GP
82.30020.851
2nd = 82.30026.281
R35 1K21R2F-2-GP
R365 68.4R750.20C
IND-4D7UH-192-GP
R3 1KR2J-1-GP
R4 Do Not Stuff
R2 Do Not Stuff
R1 1KR2J-1-GP
R378 0R0603-PAD
R377 0R0603-PAD
R18 0R0603-PAD
U1
Do Not Stuff
2nd =
C55
C476
C13
C54
C63
C500
C58
C475
C503
C490
C498
C497
C478
C59
C496
C46
C38
C15
C487
C477
C504
C52
C488
C481
C482
C61
SCD1U10V2KX-4GP
SC4D7U6D3V3KX-GP
SC4D7U6D3V3KX-GP-1
SCD1U10V2KX-5GP
SC33P50V2JN-3GP
SC18P50V2JN-1-GP
SCD1U10V2KX-4GP-1
SCD1U10V3MX-GP
SC4D7U6D3V3MX-GP
3D3V_LAN_S5
BIASVDD_G
XTALVDD_G
LAN_AVDD
AVDDL_G
GPHY_PLLVDD
PCIE_PLLVDD
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
10M/100M/1G_LED#
LAN_ACT_LED#
SCLK
SO
PCIE_RXP1
PCIE_RXN1
PCIE_TXP1
PCIE_TXN1
PCIE_RXDP
PCIE_RXDN
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
PCIE_WAKE#
PLT_RST#
LAN_RST
CLK_PCIE_LAN
CLK_PCIE_LAN#
PCIE_REFCLK_P
PCIE_REFCLK_N
VMAINPRSNT
LOW_PWR
LAN_XO_R
LAN_XO
LAN_XI
RDAC
LAN_CLKREQ#
1D2V_LAN_S5_SR
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM57780
Size Custom
Document Number
JE70-CP
Rev
-1M
Date: Tuesday, February 02, 2010
Sheet 31 of 67

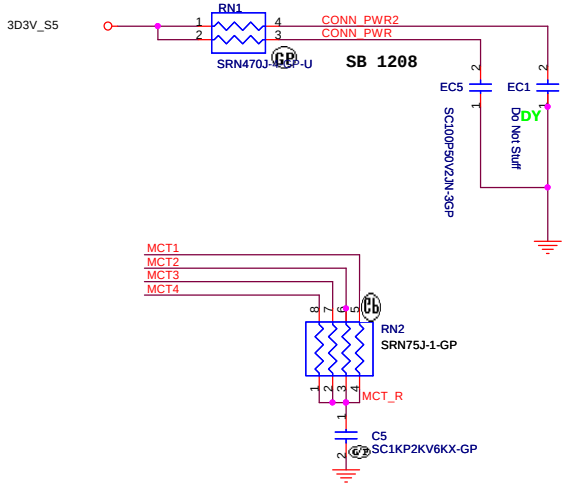
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

LAN Connector



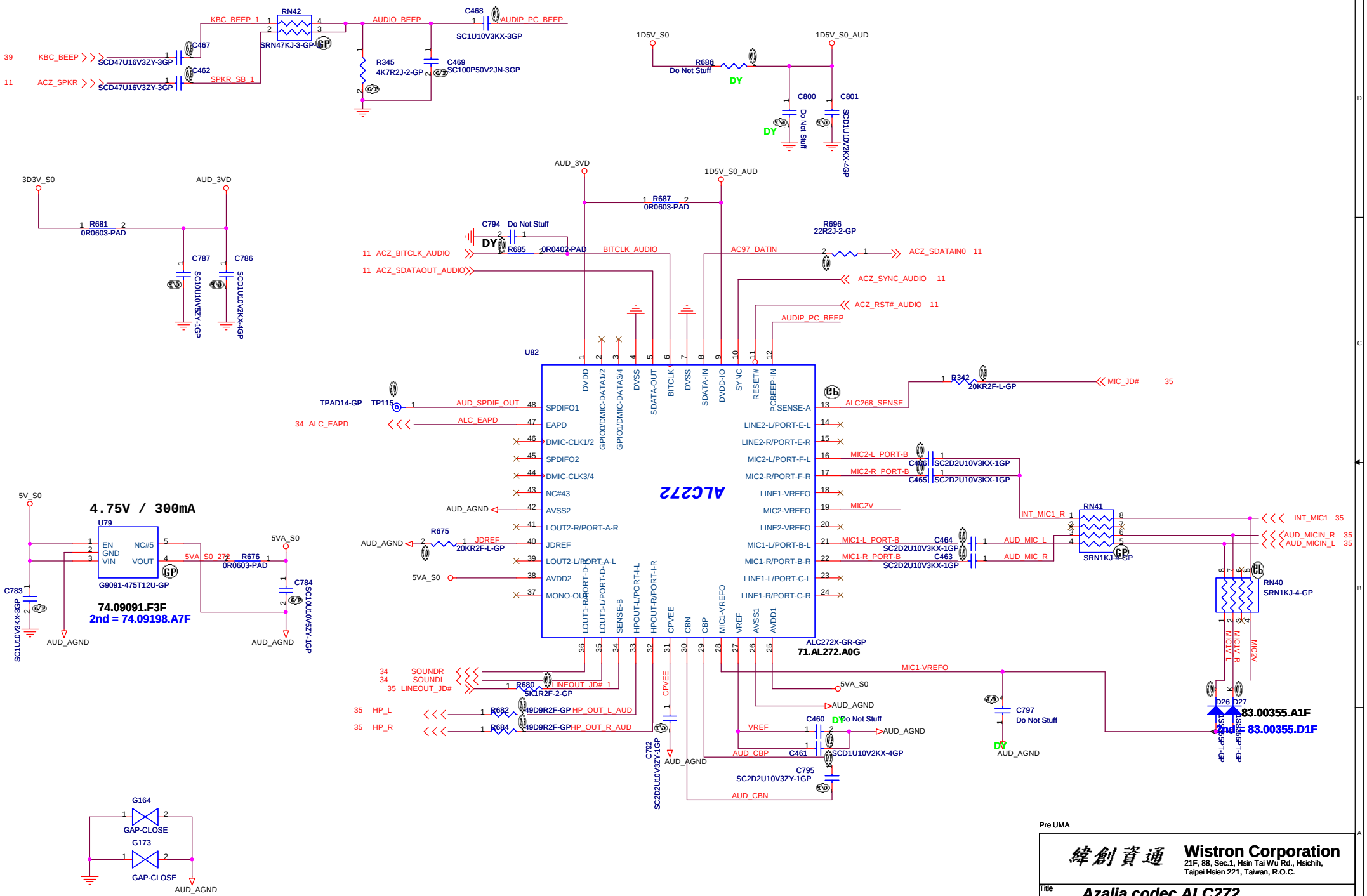




Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

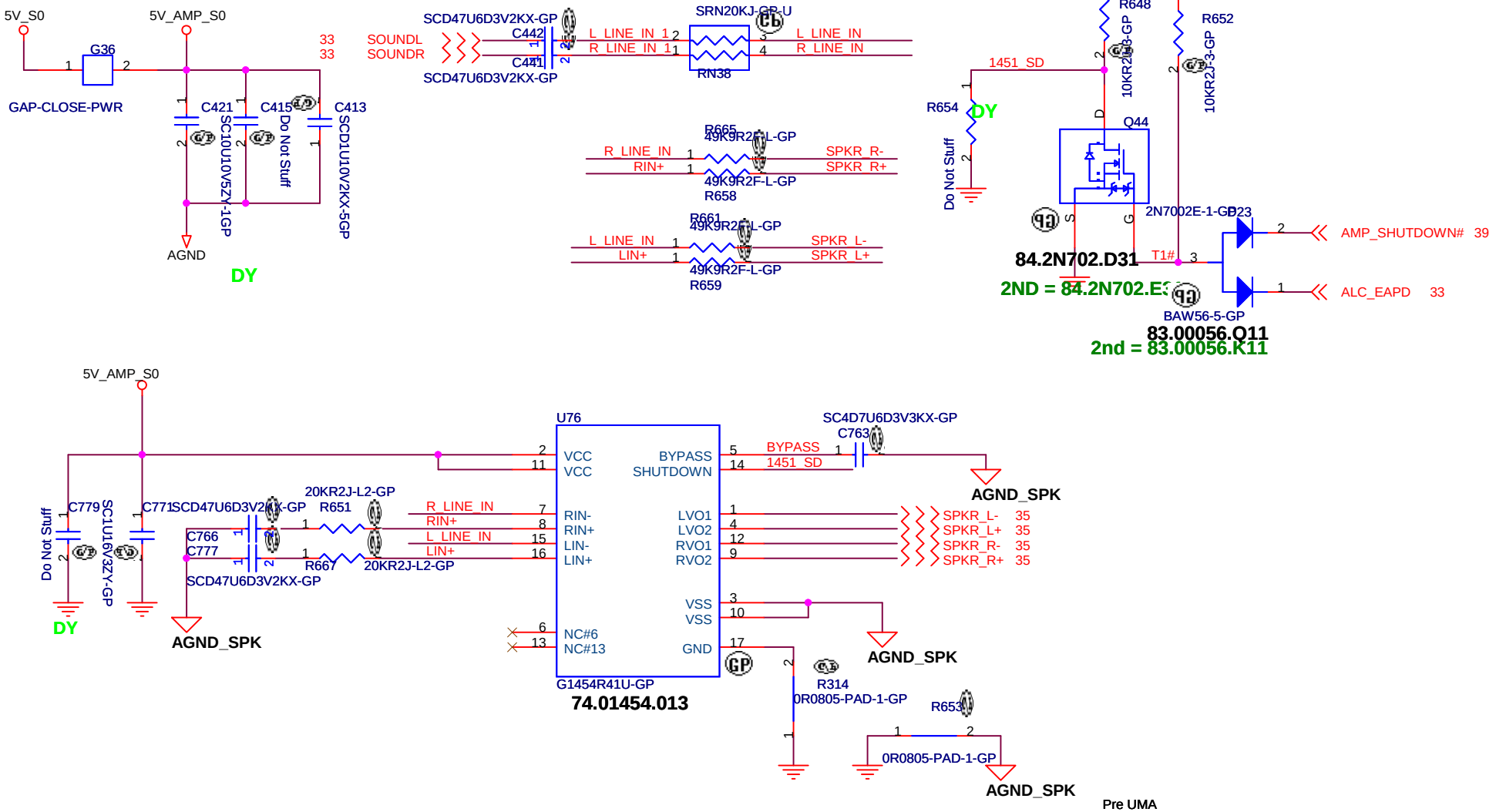
Title: **LAN CONN**		
Size: A3	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 32 of 67	



Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Azalia codec ALC272***
Size A3	Document Number **JE70-CP** Rev **-1M**
Date: Tuesday, February 02, 2010	Sheet 33 of 67

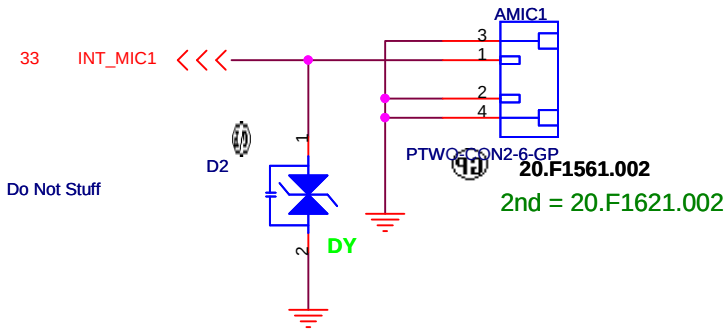
AUDIO OP AMPLIFIER



Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *AUDIO AMP*		
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 34 of 67	

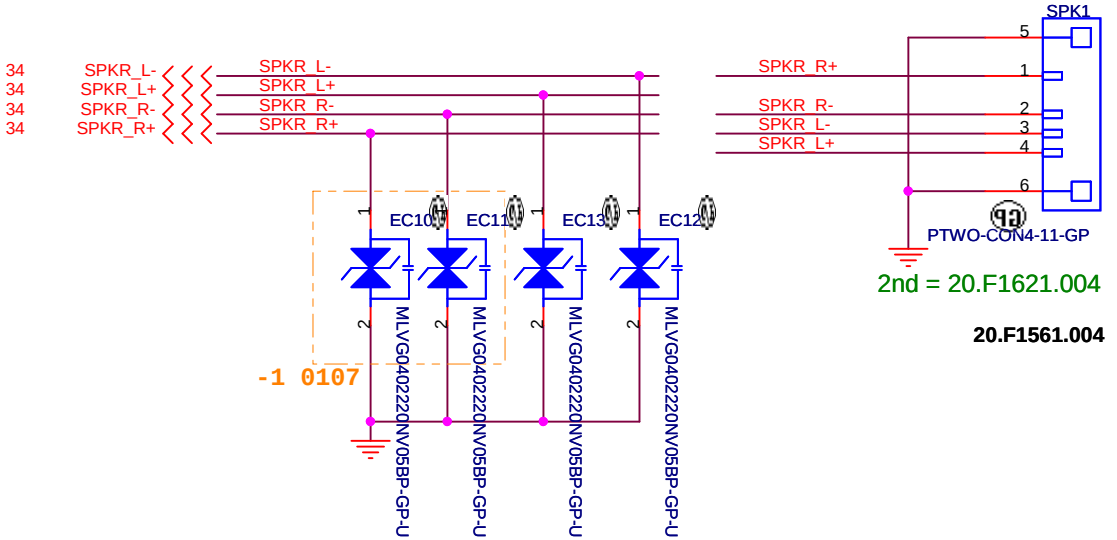
Internal Mic



20.F1561.002

2nd = 20.F1621.002

Internal Speaker



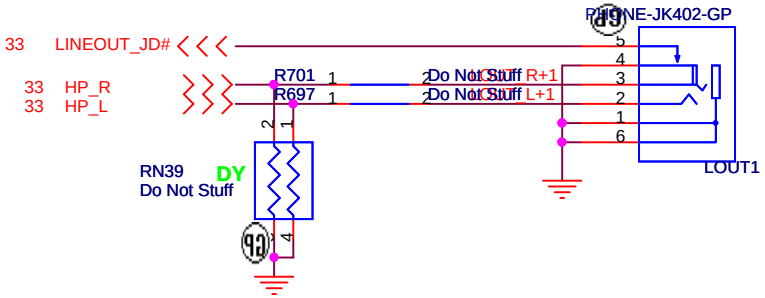
2nd = 20.F1621.004

20.F1561.004

LINE OUT

22.10265.261

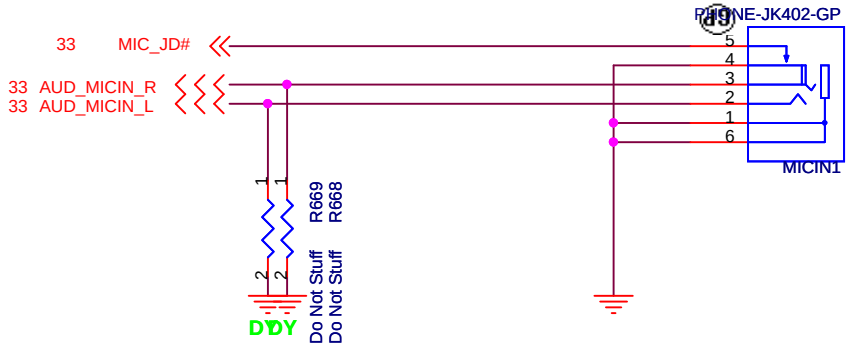
2nd =

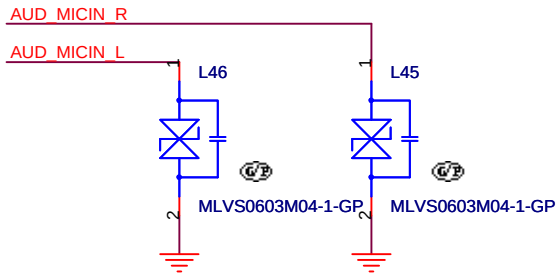


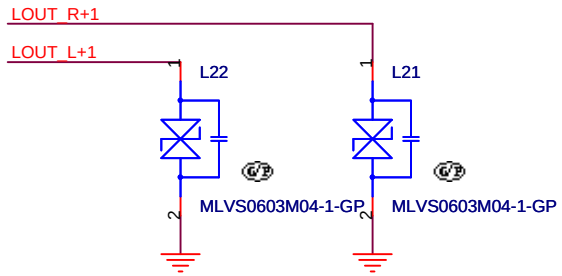
MIC IN

22.10265.261

2nd =







Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*AUDIO jack*	
Size	Document Number JE70-CP	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 35 of 67	

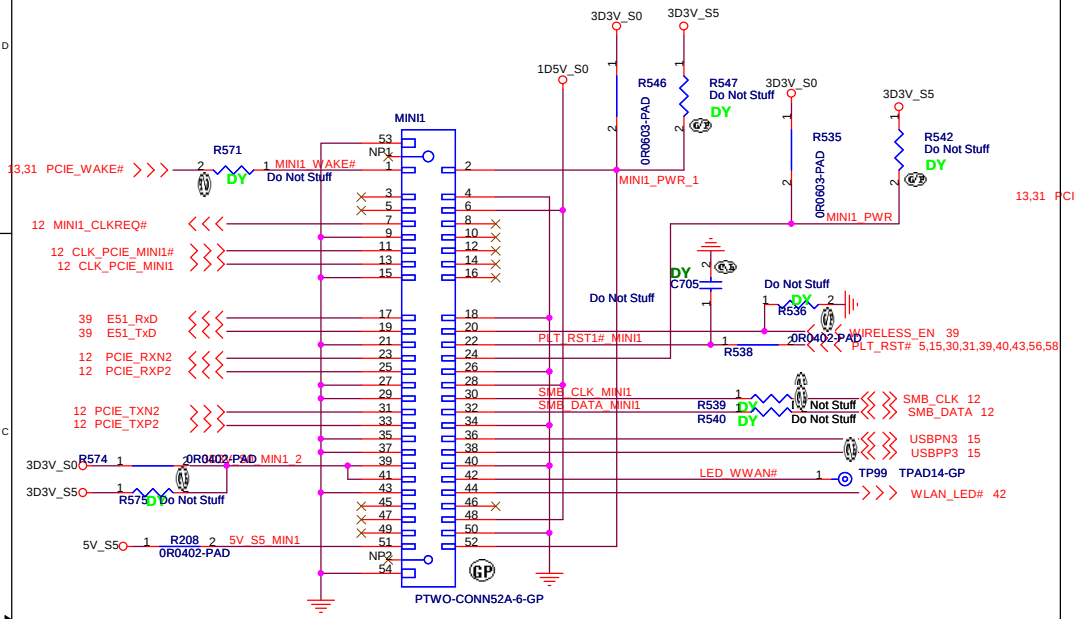
Pre UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cardreader*		
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 36 of 67	

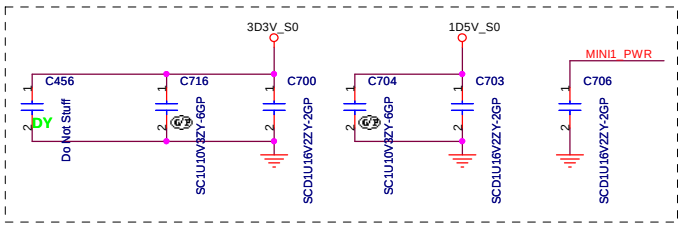
Mini Card Connector(WLAN)
Support debug-card



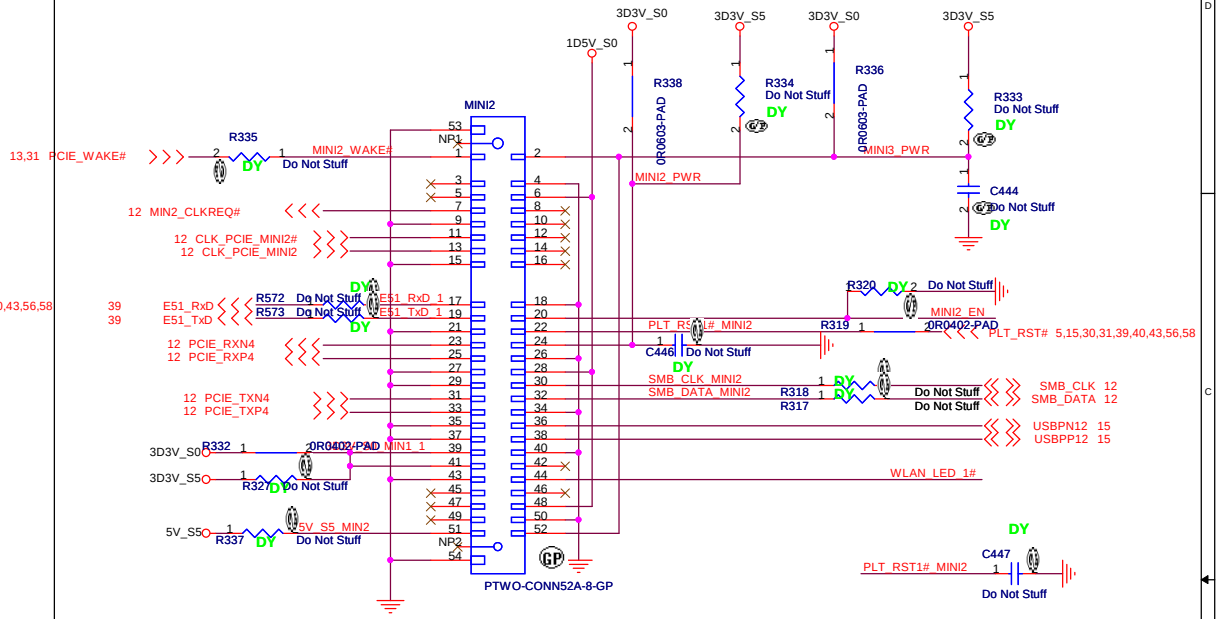
2nd = 62.10043.461

20.F1517.052

Place near MINI1

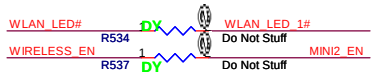


Mini Card Connector(Robson2 and 3G)

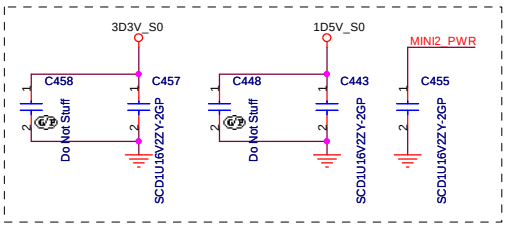


2nd =

20.F1518.052

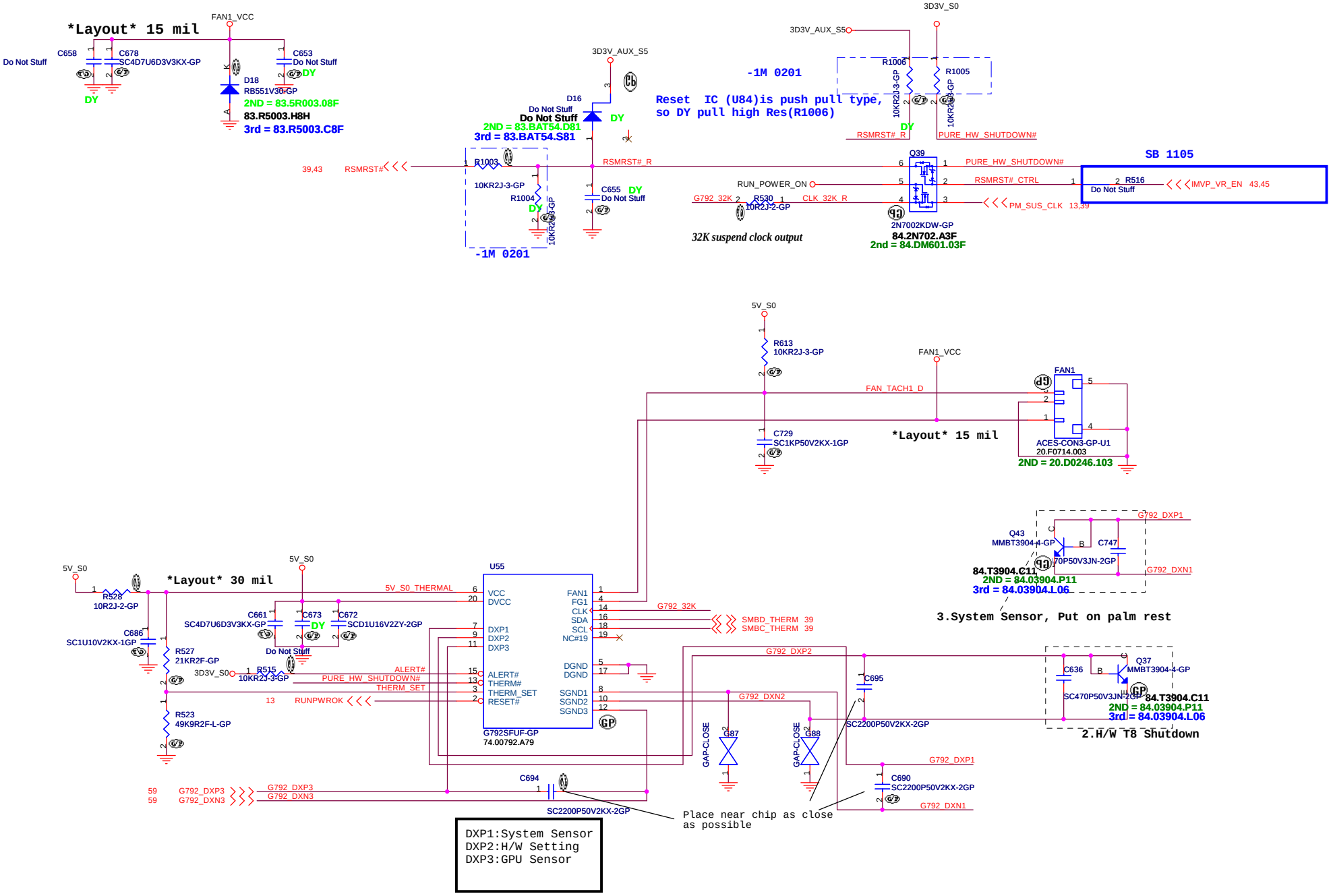


Place near MINIC2



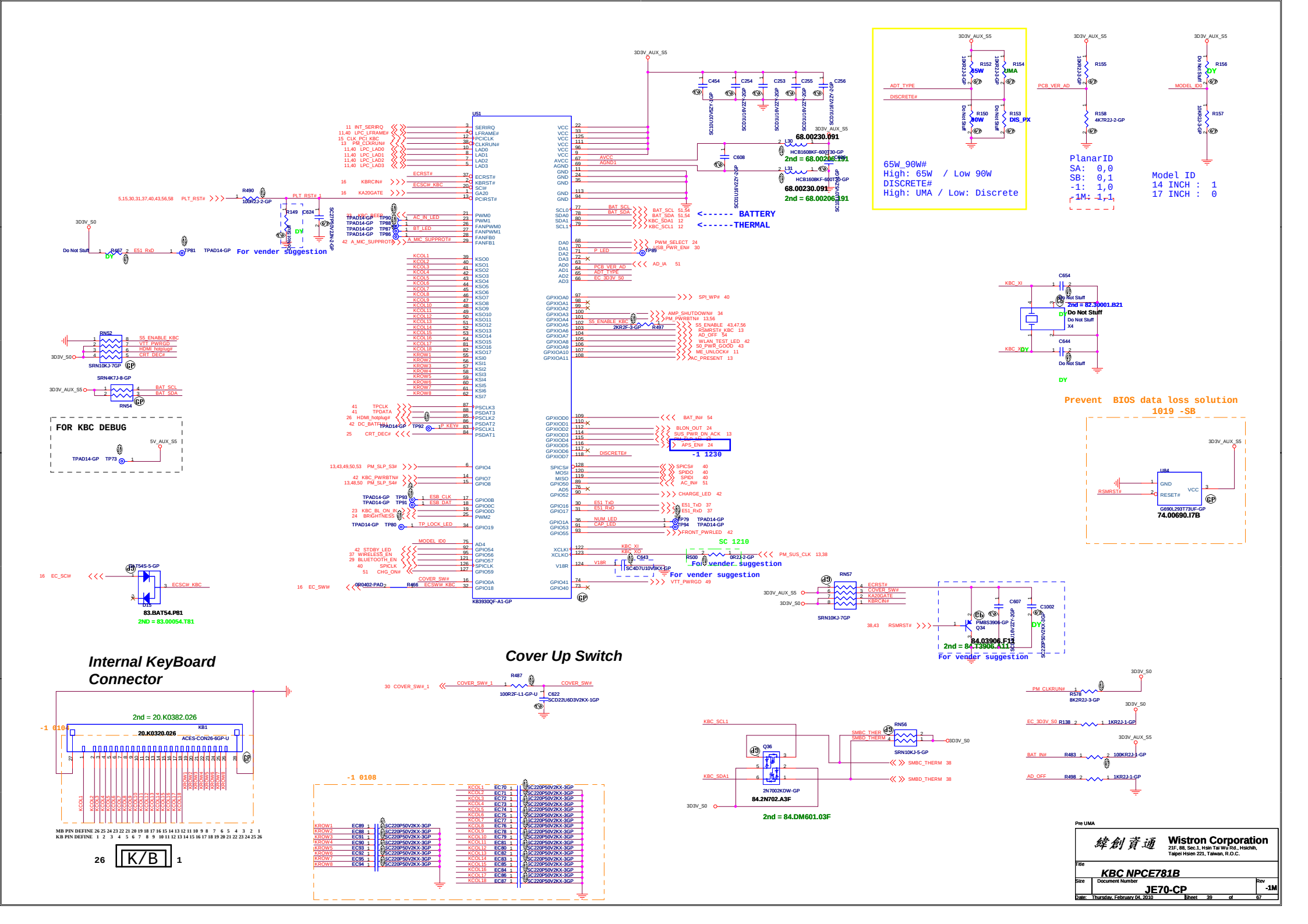
Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **MINI CARD**		
Size: A3	Document Number: **JE70-CP**	Rev: **-1M**
Date: Tuesday, February 02, 2010	Sheet 37 of 67	

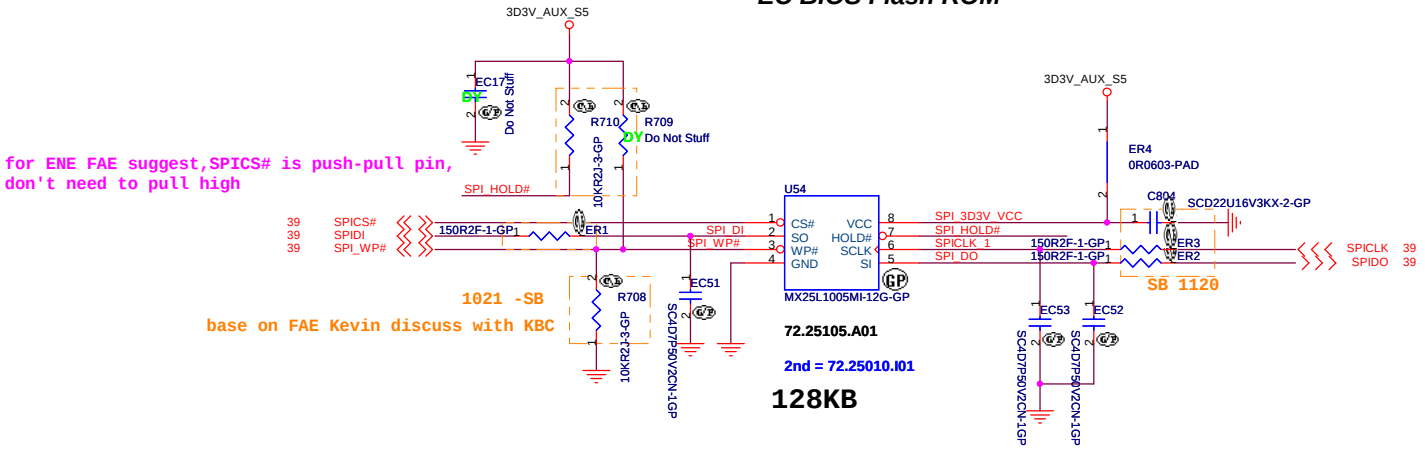


Pre UMA

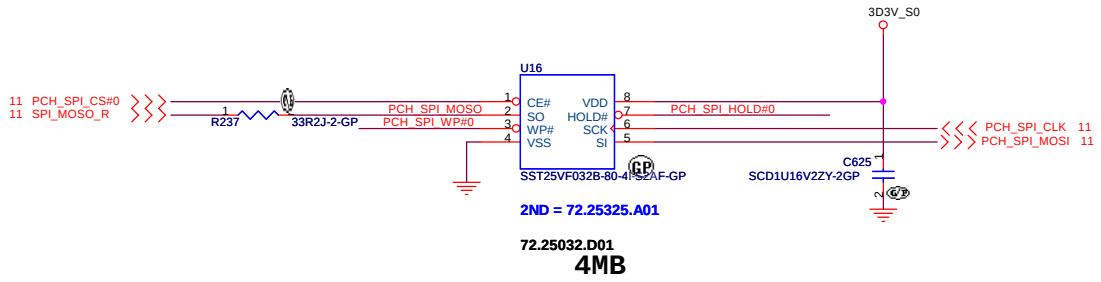
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Thermal/Fan Connector***	
Size	Document Number **JE70-CP**	Rev **-1M**
Date: Wednesday, February 03, 2010	Sheet 38 of 67	


65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
Model ID
14 INCH : 1
17 INCH : 0
U51
KB3930QF-A1-GP
<------ BATTERY
<------THERMAL
FOR KBC DEBUG
For vender suggestion
Prevent BIOS data loss solution
1019 -SB
Internal KeyBoard Connector
Cover Up Switch
MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
26 K/B 1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Pre UMA
KBC NPCE781B
JE70-CP
-1M
Date: Thursday, February 04, 2010
Sheet 39 of 67

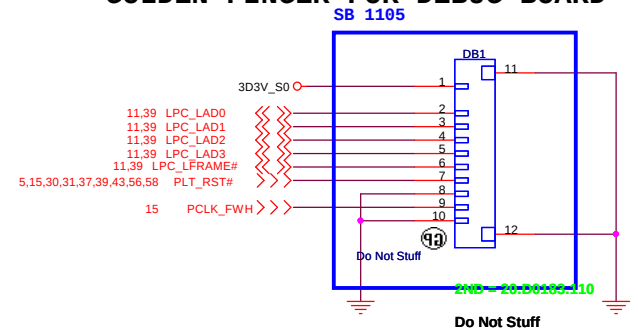
EC BIOS Flash ROM

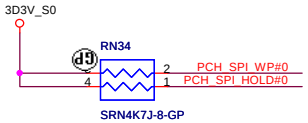


System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD





Pre UMA

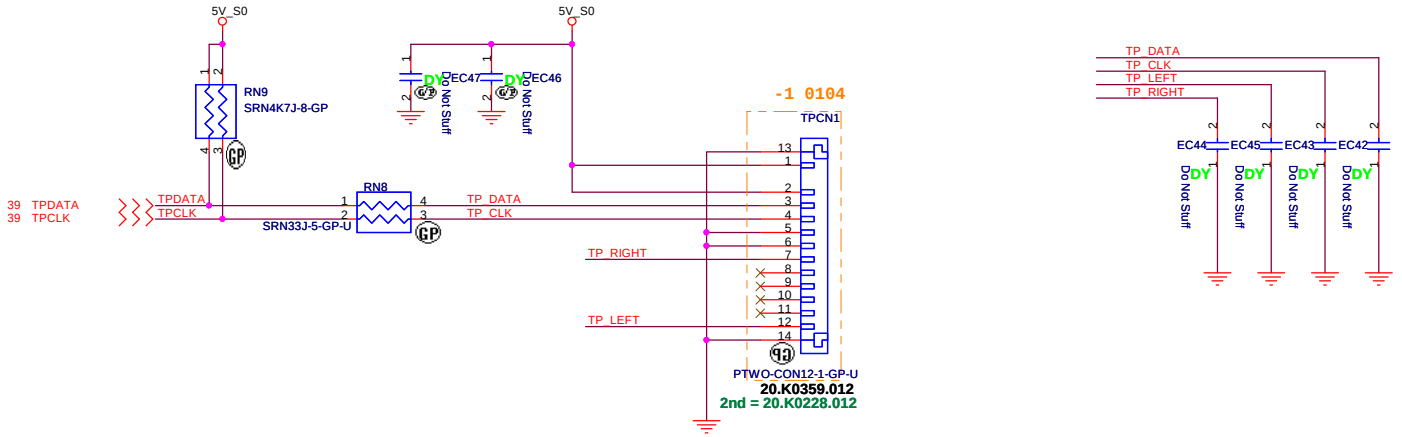
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS**

Size	Document Number	Rev
	JE70-CP	-1M

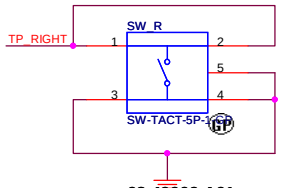
Date: Tuesday, February 02, 2010 Sheet 40 of 67

TOUCH PAD

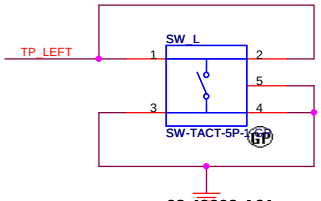


1 12

T/P



62.40009.A61
2nd = 62.40009.B21

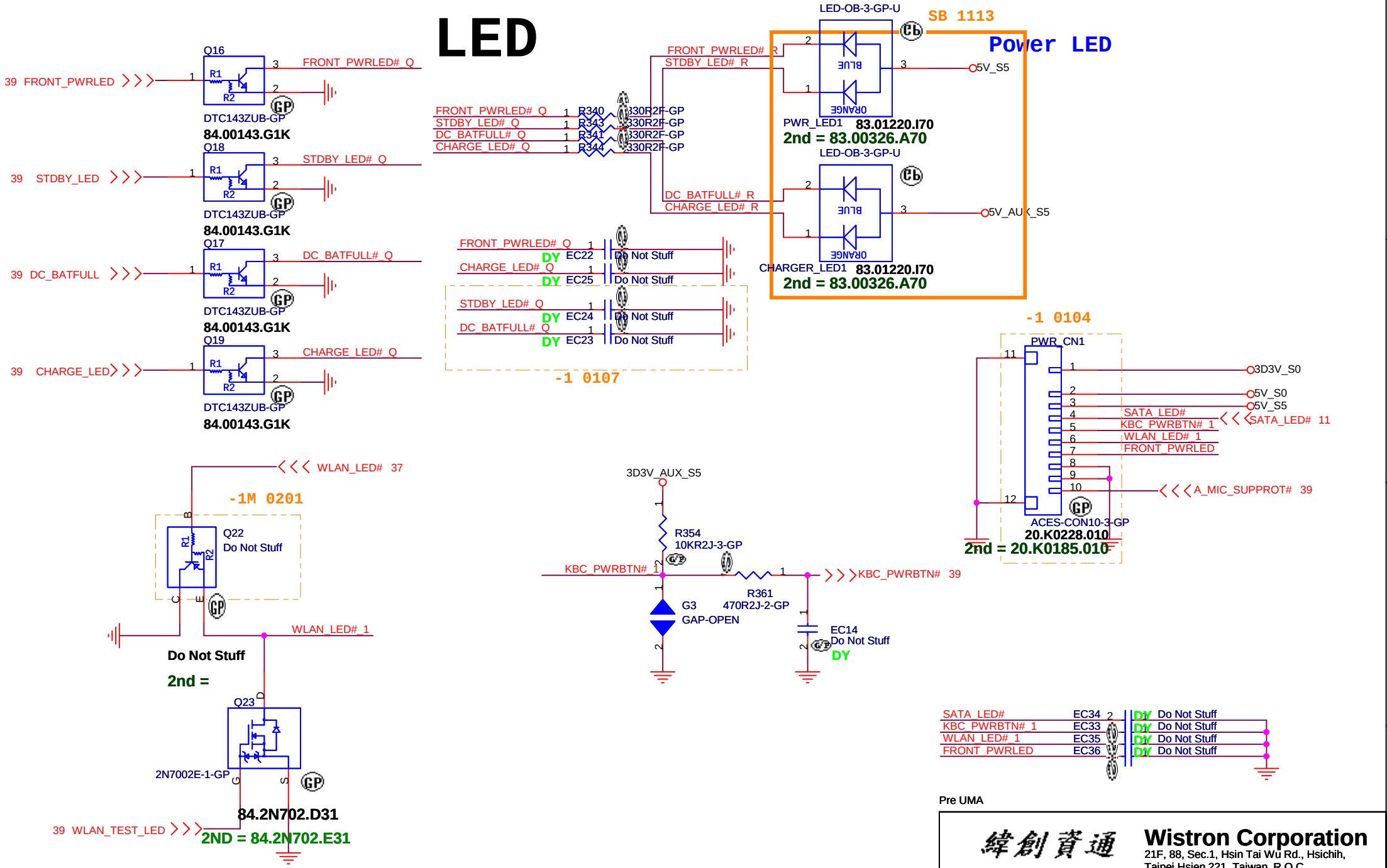


62.40009.A61
2nd = 62.40009.B21

Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Touch PAD and FP		
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 41 of 67	

LED



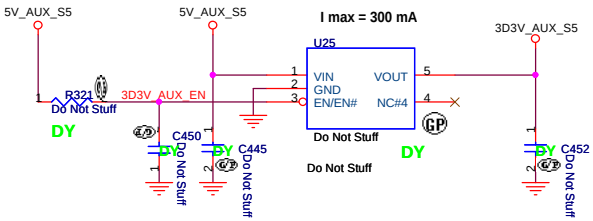
Pre UMA

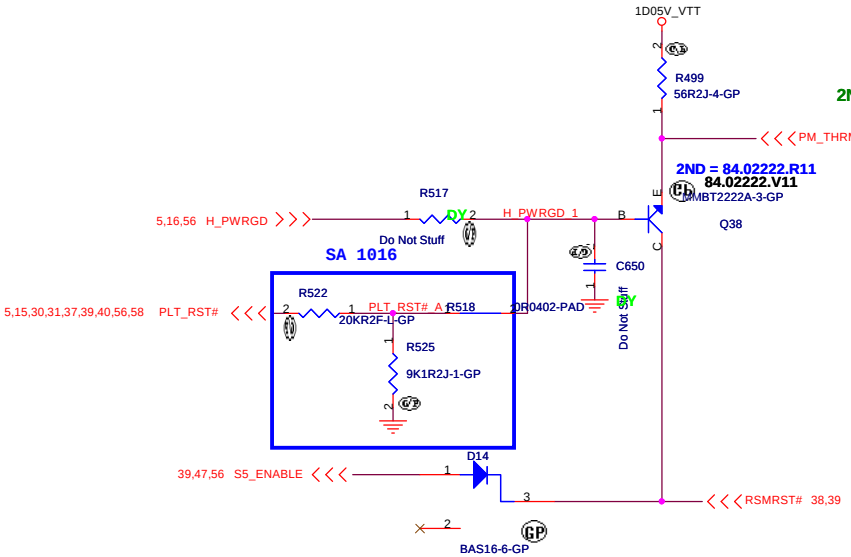
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LED&POWERBD CONN***	
Size	Document Number **JE70-CP**	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 42 of 67	

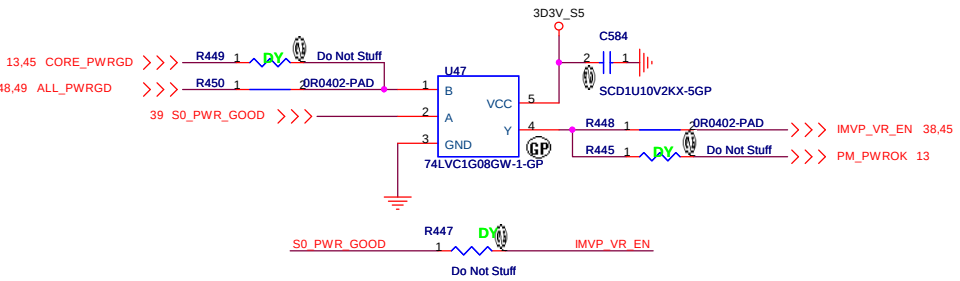
Run Power

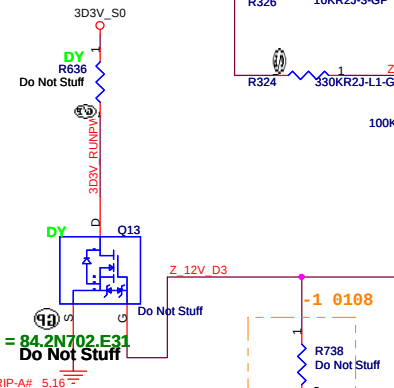
Aux Power

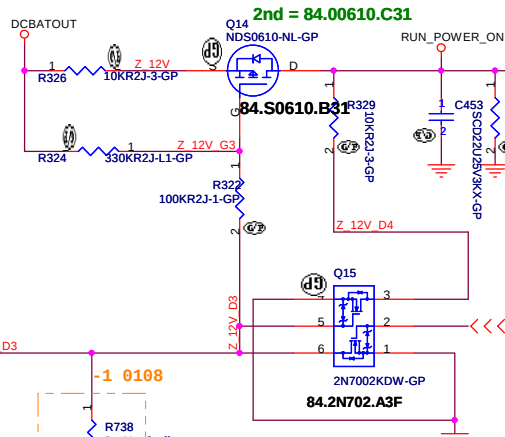
3D3V_AUX_S5

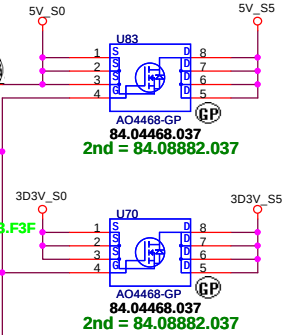


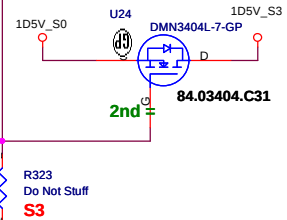


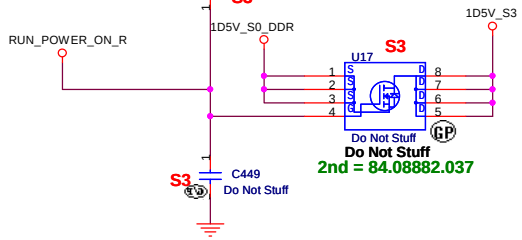


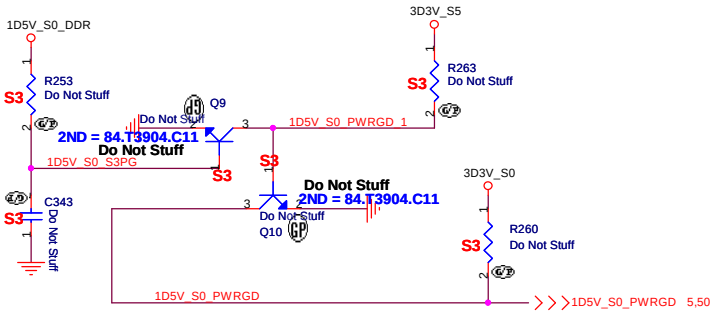












Pre UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RUN POWER and 3D3V_AUX_S5	
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 43 of 67	

ISL62883 VCC_CORE

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Output Signal
PGOOD → CORE_PWRGD

IMVP_VR_EN

Input Signal
EN (I / 3.3V)

VCC_SENSE
VSS_SENSE

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Power
VCC_CORE_PWR → VCC_CORE(Imax=65A)

DCBATOUT_62883
5V_S5
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

TPS51123 5V/3D3V

DCBATOUT_51123_1
DCBATOUT_51123_2

Input Power
VIN_1
VIN_2

Output Power
5V(O) → 5V_S5 (8A)
3D3V(O) → 3D3V_S5 (6A)
5V_AUX(O) → 5V_AUX_S5 (100mA)
3D3V_AUX(O) → 3D3V_AUX_S5 (100mA)

S5_ENABLE

Input Signal
EN1
EN2

Output Signal
PGOOD → ALL_PWRGD

RT9026 0D75V_S0

5V_S5
1D5V_S3
PM_SLP_S3#
PM_SLP_S4#

VIN
VLDOIN
S3
S5

VTT → 0D75V_S0 (1.2A)
VTTREF → DDR_VREF_S3

RT9025 1D5V

5V_S5
DCBATOUT_7141_1D5V

Input Power
VDD
VCC

Output Power
1D5V (O) → 1D5V_S3 (10A)

PM_SLP_S4#

Input Signal
EN

ALL_PWRGD

Output Signal
PGOOD

RT9025 1D8V

5V_S5
3D3V_S0
PM_SLP_S3#
ALL_PWRGD

VIN
VLDOIN
EN
PGOOD

1D8V (O) → 1D85V_S0

Charger BQ24745

BATT_SENSE

Input Signal
FBS

Output Signal
ACGOOD# → AC_IN#
SRSET → AD_IA

AD+

Input Power
ACN

Output Power
VOUT (O) → BT+
VOUT (O) → DCBATOUT

Adapter

AD_OFF

Input Signal
(I)

Output Signal
(O) → AD_IN#

AD_JK
5V_AUX_S5

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O) → AD+

RT8209B 1D05V

5V_S5
DCBATOUT_RT8209B_1D05V

Input Power
VDD
VCC

Output Power
1D05V (O) → 1D05V_S0 (10A)

PM_SLP_S3#

Input Signal
EN

ALL_PWRGD

Output Signal
PGOOD

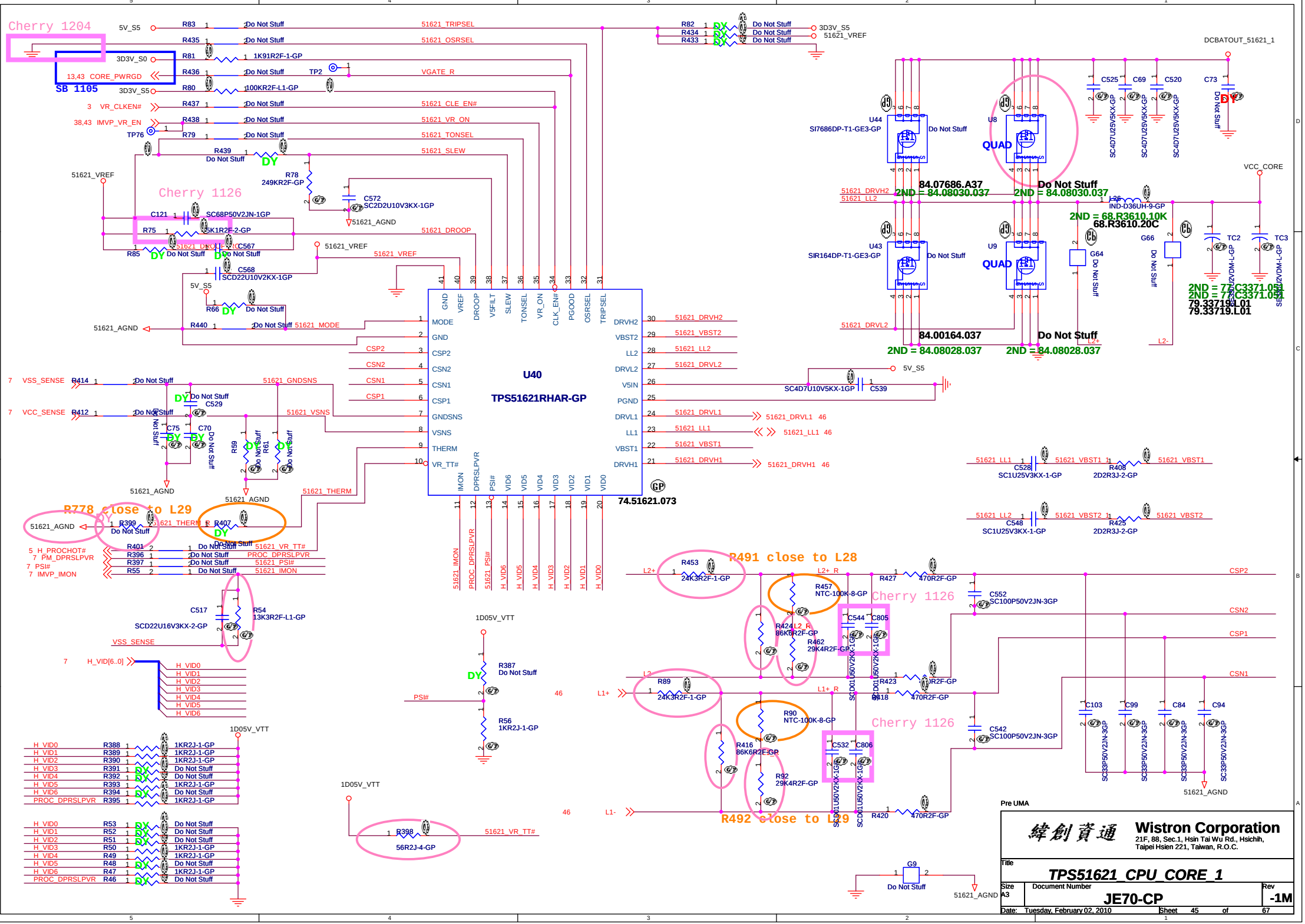
Pre UMA

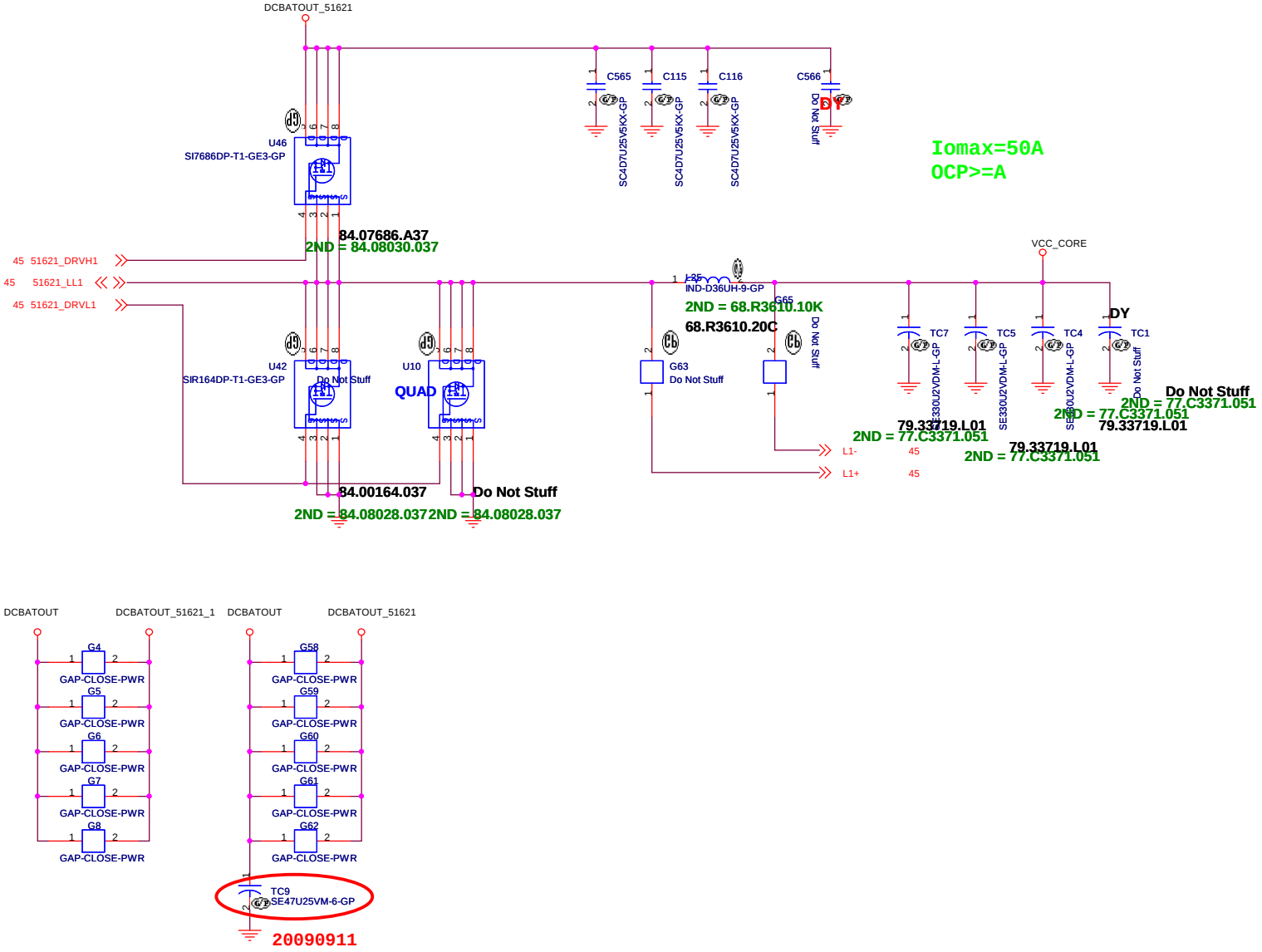
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 44 of 67


Cherry 1204
SB 1105
Cherry 1126
U40
TPS51621RHAR-GP
74.51621.073
R778 close to L29
R491 close to L28
R492 close to L29
Cherry 1126
Cherry 1126
U44
SI7686DP-T1-GE3-GP
U8
QUAD
U43
SIR164DP-T1-GE3-GP
U9
QUAD
84.07686.A37
2ND = 84.08030.037
84.00164.037
2ND = 84.08028.037
2ND = 84.08030.037
2ND = 84.08028.037
2ND = 68.R3610.10K
68.R3610.20C
2ND = 77C3371.051
2ND = 77C3371.051
79.33719.L01
79.33719.L01
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51621_CPU_CORE_1
JE70-CP
-1M
Tuesday, February 02, 2010
45
67



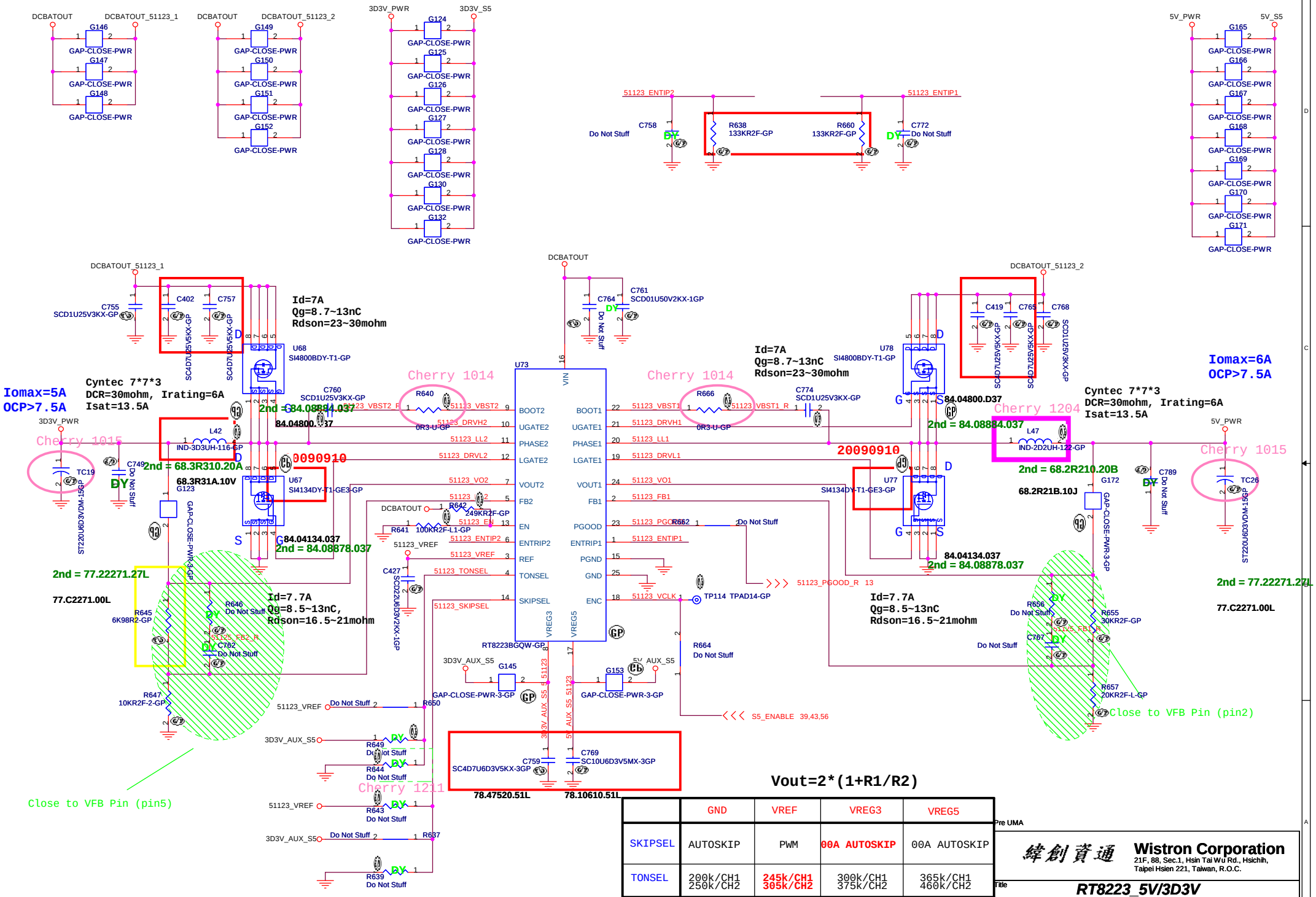
Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ISL62882 CPU CORE (1/2)*

Size	Document Number	Rev
	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 46 of 67



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

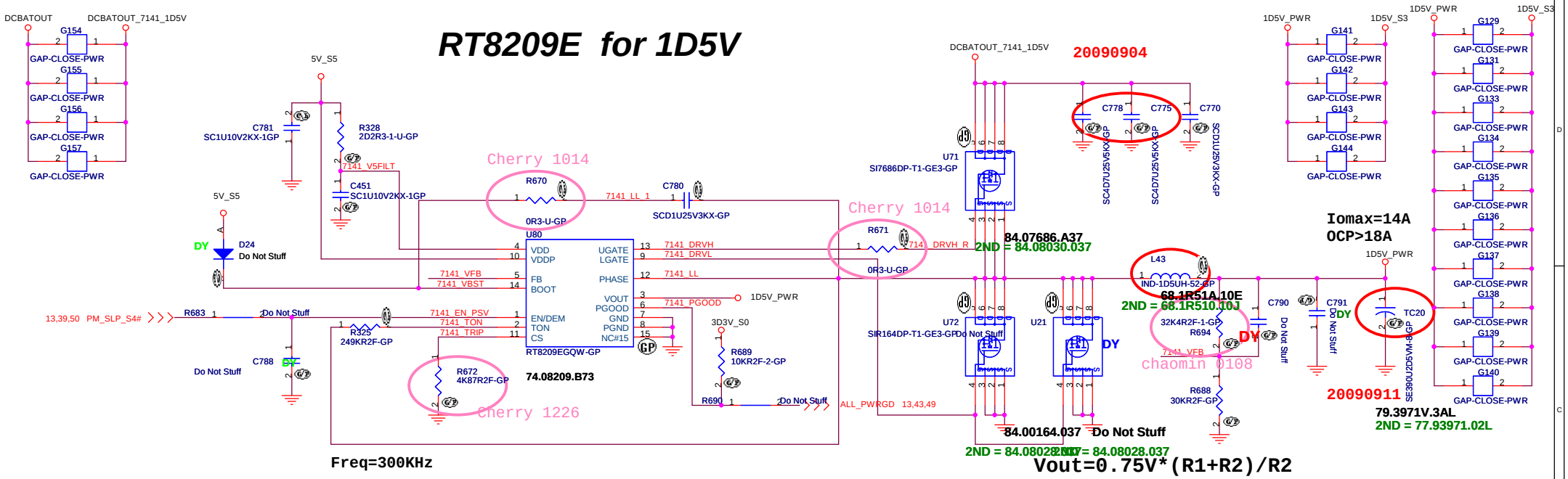
Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223_5V/3D3V

Size | Document Number: JE70-CP | Rev: -1M

Date: Tuesday, February 02, 2010 | Sheet 47 of 67



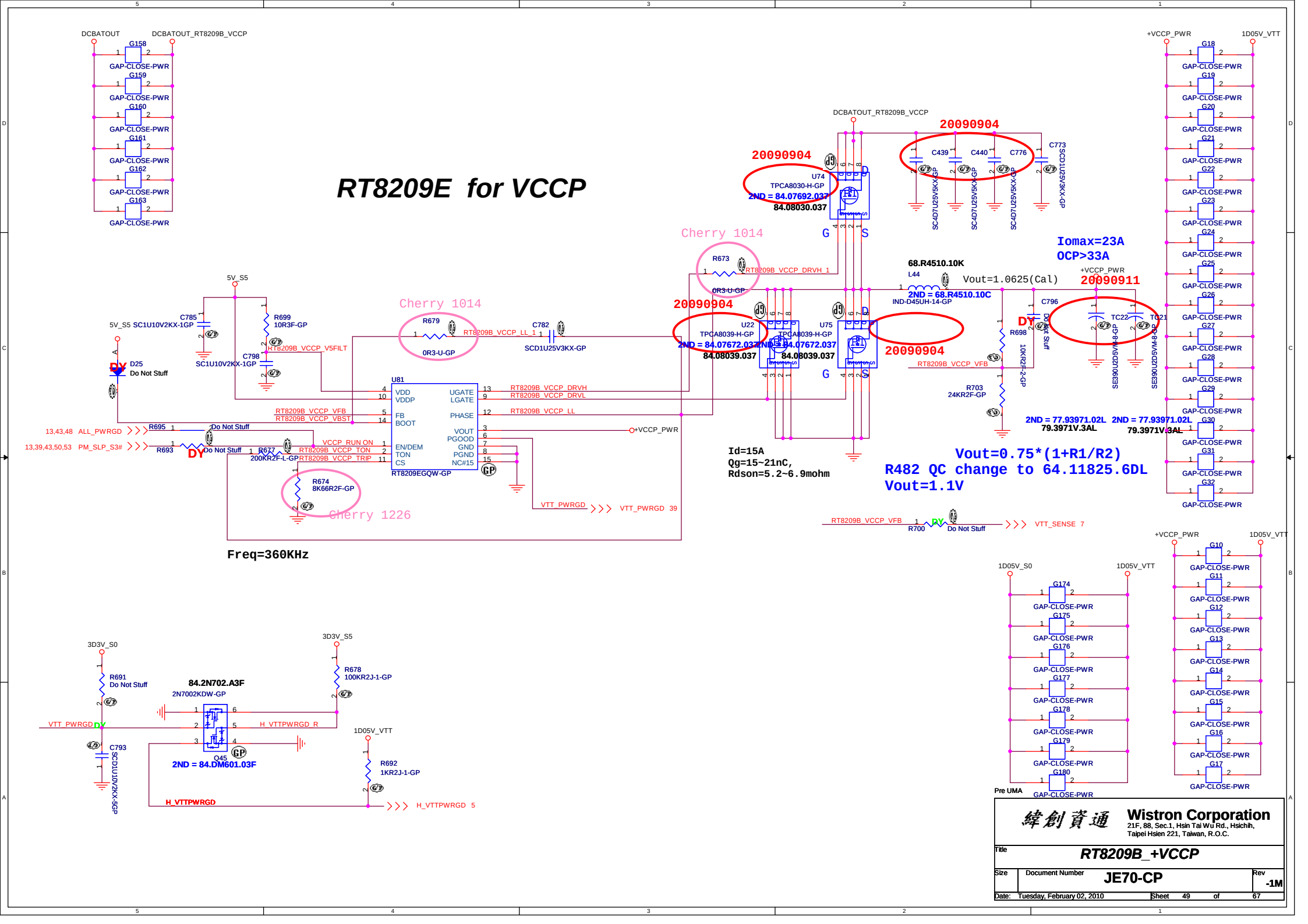
Pre UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

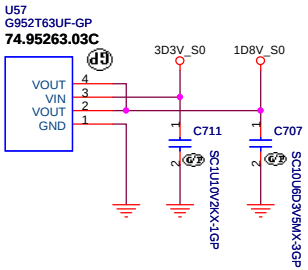
Title: RT8209E 1D5V

Size | Document Number: JE70-CP | Rev: -1M

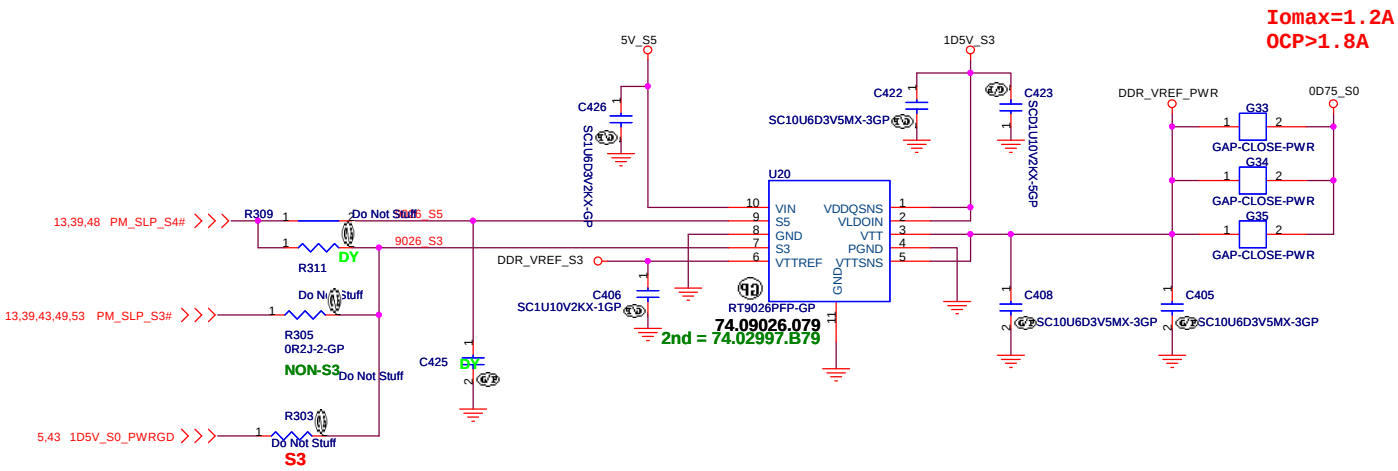
Date: Tuesday, February 02, 2010 | Sheet 48 of 67


RT8209E for VCCP
DCBATOUT
DCBATOUT_RT8209B_VCCP
GAP-CLOSE-PWR
5V_S5
SC1U10V2KX-1GP
D25
Do Not Stuff
R699
10R3F-GP
C798
RT8209B_VCCP_V5FILT
Cherry 1014
R679
0R3-U-GP
RT8209B_VCCP_LL_1
C782
SCD1U25V3KX-GP
U81
VDD
VDDP
FB
BOOT
EN/DEM
TON
CS
UGATE
LGATE
PHASE
VOUT
PGOOD
GND
PGND
NC#15
RT8209EGQW-GP
RT8209B_VCCP_DRVH
RT8209B_VCCP_DRVL
RT8209B_VCCP_LL
RT8209B_VCCP_VFB
RT8209B_VCCP_VBST
RT8209B_VCCP_TON
RT8209B_VCCP_TRIP
VCCP_RUN ON
+VCCP_PWR
R695
R693
R677
200KR2F-L-GP
R674
8K66R2F-GP
Cherry 1226
VTT_PWRGD
VTT_PWRGD 39
13,43,48 ALL_PWRGD
13,39,43,50,53 PM_SLP_S3#
Freq=360KHz
20090904
U74
TPCA8030-H-GP
2ND = 84.07692.037
84.08030.037
C439
C440
C776
C773
SC4D7U25V5KX-GP
SC4D7U25V5KX-GP
SC4D7U25V5KX-GP
SCD1U25V3KX-GP
U22
TPCA8039-H-GP
2ND = 84.07672.037
84.08039.037
U75
TPCA8039-H-GP
2ND = 84.07672.037
84.08039.037
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
68.R4510.10K
L44
2ND = 68.R4510.10C
IND-D45UH-14-GP
Vout=1.0625(Cal)
Iomax=23A
OCP>33A
20090911
C796
R698
10KR2F-2-GP
R703
24KR2F-GP
TC22
TC21
SE390U2D5VM-8-GP
SE390U2D5VM-8-GP
2ND = 77.93971.02L
79.3971V.3AL
2ND = 77.93971.02L
79.3971V.3AL
Vout=0.75*(1+R1/R2)
R482 QC change to 64.11825.6DL
Vout=1.1V
R700
VTT_SENSE 7
3D3V_S0
3D3V_S5
R691
Do Not Stuff
84.2N702.A3F
2N7002KDW-GP
R678
100KR2J-1-GP
H_VTTPWRGD_R
Q45
2ND = 84.DM601.03F
C793
SCD1U10V2KX-5GP
1D05V_VTT
R692
1KR2J-1-GP
H_VTTPWRGD
H_VTTPWRGD 5
1D05V_S0
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8209B_+VCCP
Size
Document Number
JE70-CP
Rev
-1M
Date: Tuesday, February 02, 2010
Sheet 49 of 67

1.8V_S0 1.8V 1A Regulator

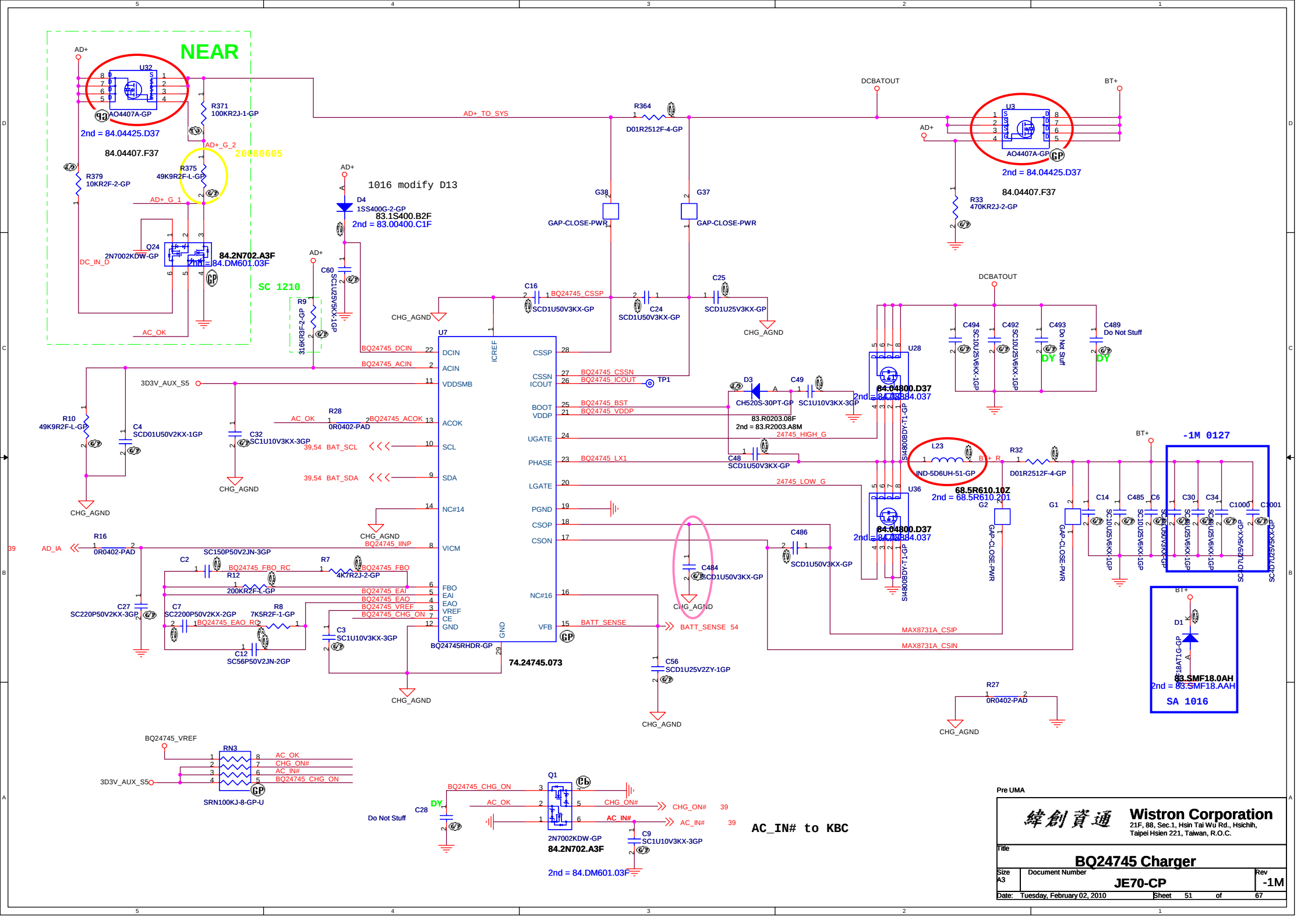


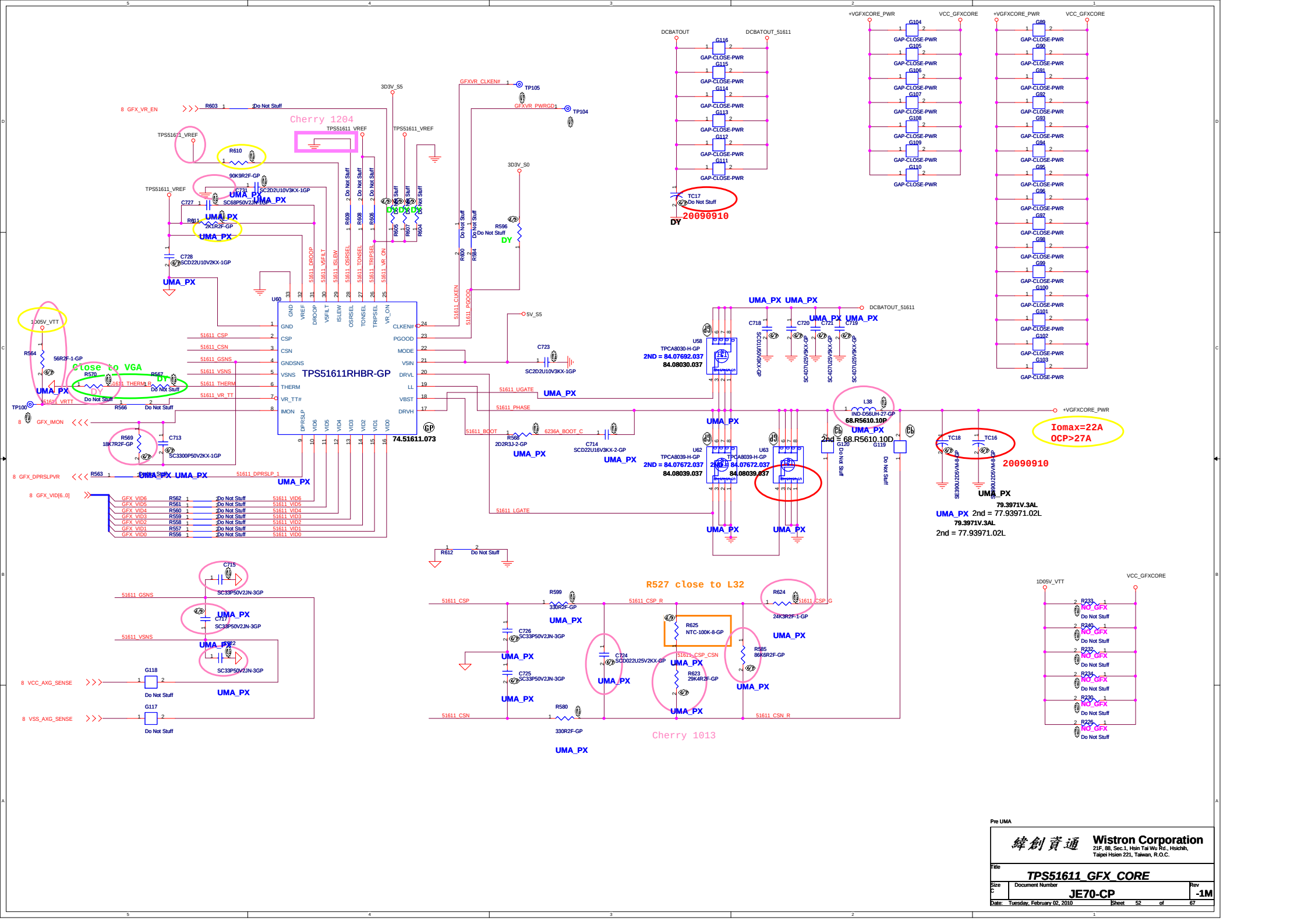
RT9026 for 0D75V_S3



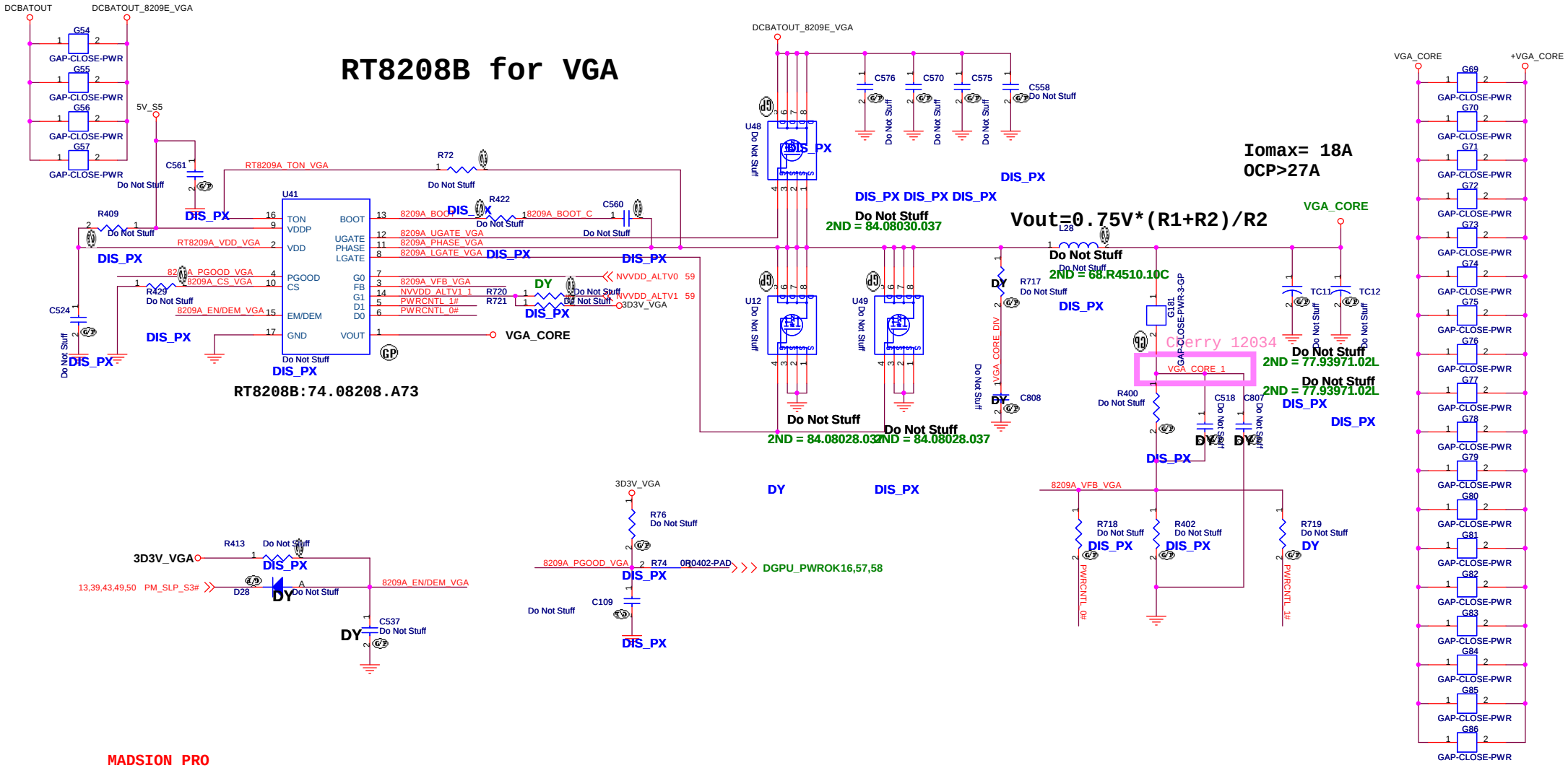
Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8015A for 1D8V/RT9026_0D75		
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 50 of 67	


NEAR
U32
AO4407A-GP
2nd = 84.04425.D37
84.04407.F37
R371
100KR2J-1-GP
AD+_G_2
20080605
R379
10KR2F-2-GP
R375
49K9R2F-L-GP
AD+_G_1
Q24
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
DC_IN_D
AC_OK
SC 1210
AD+
D4
1SS400G-2-GP
83.1S400.B2F
2nd = 83.00400.C1F
1016 modify D13
C60
SC1U25V5KX-1GP
R9
316KR3F-2-GP
AD+_TO_SYS
R364
D01R2512F-4-GP
G38
G37
GAP-CLOSE-PWR
DCBATOUT
BT+
U3
AO4407A-GP
2nd = 84.04425.D37
84.04407.F37
R33
470KR2J-2-GP
C16
SCD1U50V3KX-GP
BQ24745_CSSP
C24
SCD1U50V3KX-GP
C25
SCD1U25V3KX-GP
CHG_AGND
U7
BQ24745_DCIN
BQ24745_ACIN
3D3V_AUX_S5
R10
49K9R2F-L-GP
C4
SCD01U50V2KX-1GP
C32
SC1U10V3KX-3GP
R28
0R0402-PAD
BQ24745_ACOK
39,54 BAT_SCL
39,54 BAT_SDA
BQ24745_CSSN
BQ24745_ICOUT
TP1
BQ24745_BST
BQ24745_VDDP
BQ24745_LX1
24745_HIGH_G
24745_LOW_G
D3
CH520S-30PT-GP
C49
SC1U10V3KX-3GP
83.R0203.08F
2nd = 83.R2003.A8M
C48
SCD1U50V3KX-GP
U28
U36
SI4800BDY-T1-GP
84.04800.D37
2nd = 84.04884.037
L23
IND-5D6UH-51-GP
68.5R610.10Z
2nd = 68.5R610.201
R32
D01R2512F-4-GP
-1M 0127
C494
C492
C493
C489
Do Not Stuff
DY
R16
0R0402-PAD
AD_IA
SC150P50V2JN-3GP
C2
R12
200KR2F-L-GP
R7
4K7R2J-2-GP
BQ24745_FBO_RC
BQ24745_FBO
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
C27
SC220P50V2KX-3GP
C7
SC2200P50V2KX-2GP
R8
7K5R2F-1-GP
BQ24745_EAO_RC
C12
SC56P50V2JN-2GP
C3
SC1U10V3KX-3GP
BQ24745_IINP
C484
C486
SCD1U50V3KX-GP
MAX8731A_CSIP
MAX8731A_CSIN
BATT_SENSE
BATT_SENSE 54
C56
SCD1U25V2ZY-1GP
74.24745.073
BQ24745RHDR-GP
C14
C485
C6
C30
C34
C1000
C1001
SC1U25V6KX-1GP
SCD1U50V3KX-GP
SCD1U25V5KX-1GP
D1
18AT1G-GP
83.SMF18.0AH
2nd = 83.SMF18.AAH
SA 1016
R27
0R0402-PAD
BQ24745_VREF
RN3
SRN100KJ-8-GP-U
3D3V_AUX_S5
AC_OK
CHG_ON#
AC_IN#
BQ24745_CHG_ON
Q1
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
C28
C9
SC1U10V3KX-3GP
Do Not Stuff
AC_IN# to KBC
Pre UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size
A3
Document Number
JE70-CP
Rev
-1M
Date: Tuesday, February 02, 2010
Sheet 51 of 67


Cherry 1204
TPS51611RHBR-GP
74.51611.073
U60
Close to VGA
DY
20090910
Iomax=22A
OCP>27A
R527 close to L32
Cherry 1013
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51611_GFX_CORE
JE70-CP
-1M
Date: Tuesday, February 02, 2010
Sheet 52 of 67

RT8208B for VGA



MADSION PRO

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.00V GPU VOLTAGE H: 0.90V

PARK XT

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.12V GPU VOLTAGE H: 0.90V

Park==>R718=33K (64.33025.6DL)
Madison==>R718=71.5K (64.71525.6DL)

NVVDD_ALTV1	NVVDD_ALTV0	+VGA_CORE
H	L	1.12V or 1V OUT=[R400+(R402//R718)}/(R402//R718)
H	H	0.9V OUT=(R400+R402)/R402

Pre UMA

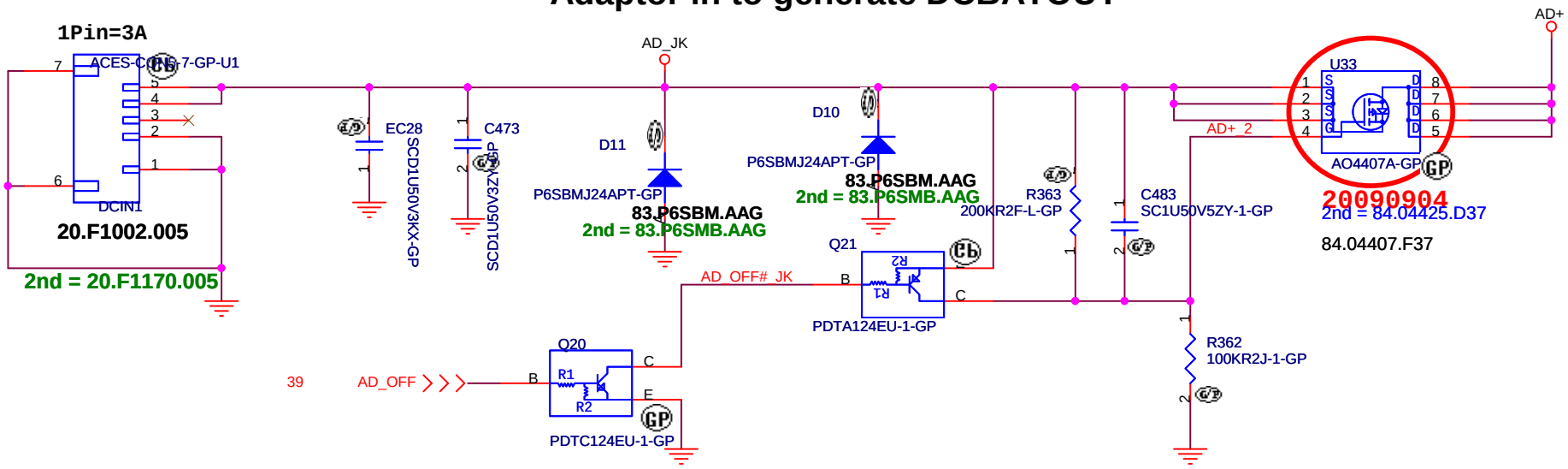
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E VGA CORE

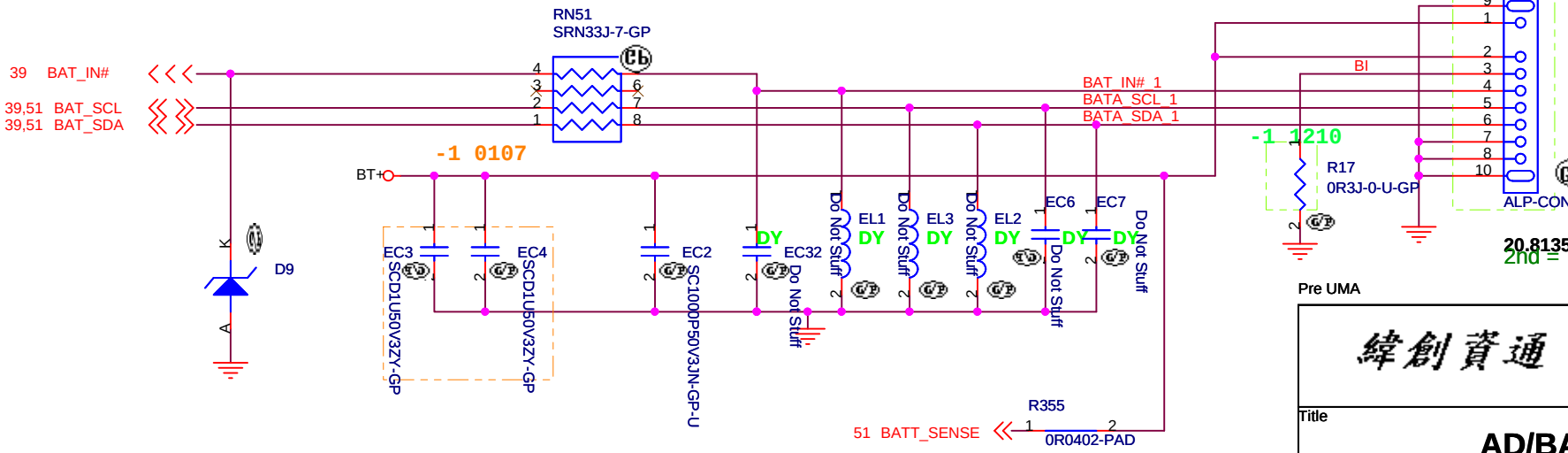
Size: A3 | Document Number: JE70-CP | Rev:

Date: Tuesday, February 02, 2010 | Sheet 53 of 67

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



Pin NO	Symbol
1	GND
2	GND
3	SMD
4	SMC
5	TS
6	B/I
7	BT+
8	BT+

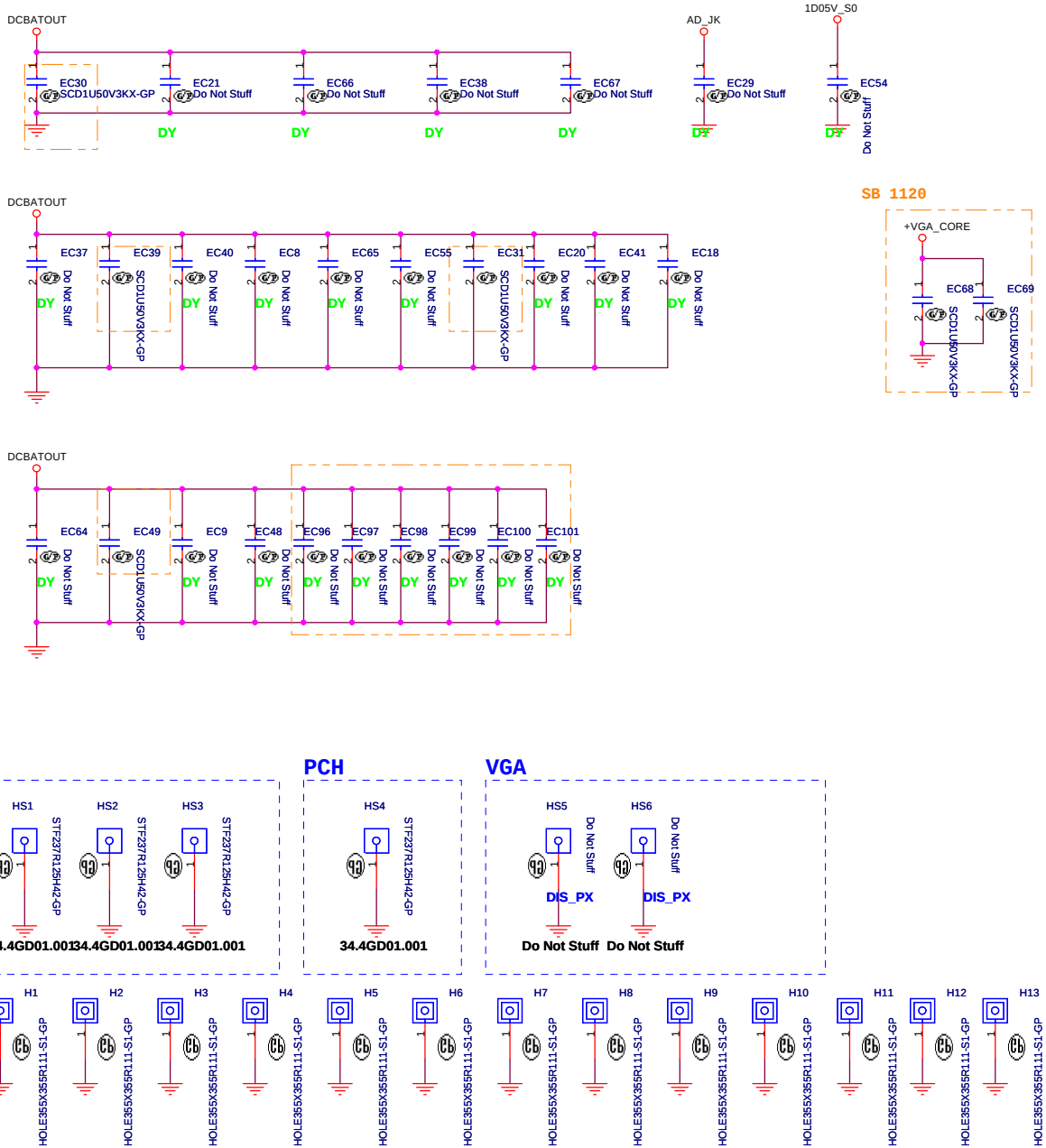
Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 54 of 67



Pre UMA

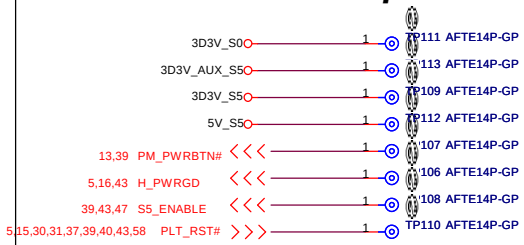
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size | Document Number: **JE70-CP** | Rev: -1M

Date: Tuesday, February 02, 2010 | Sheet 55 of 67

Check test point



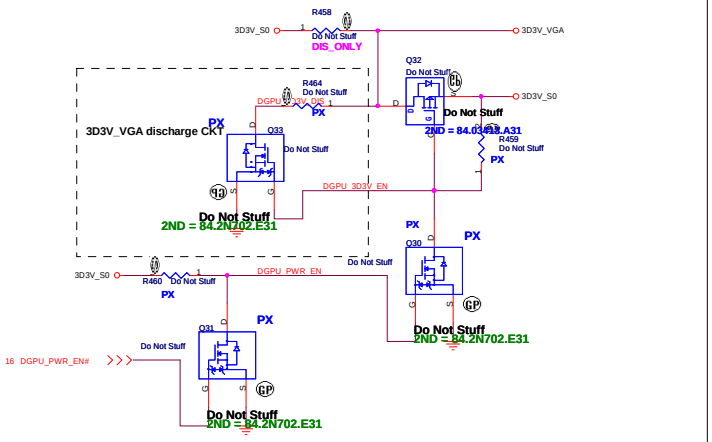
Test Point放在Dimm Door打開可量測處

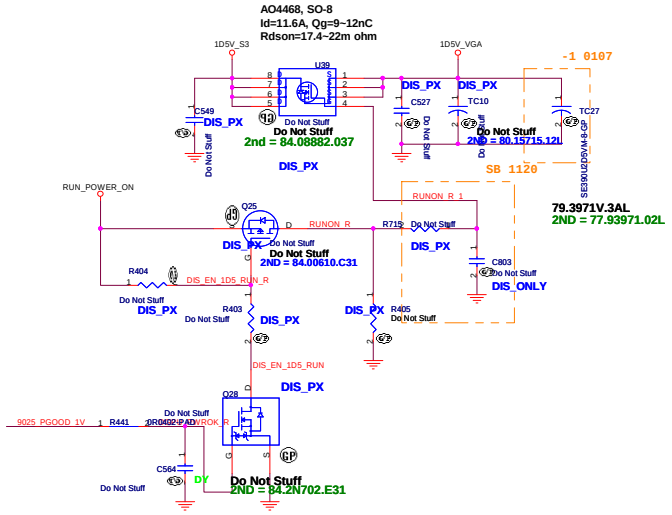
Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

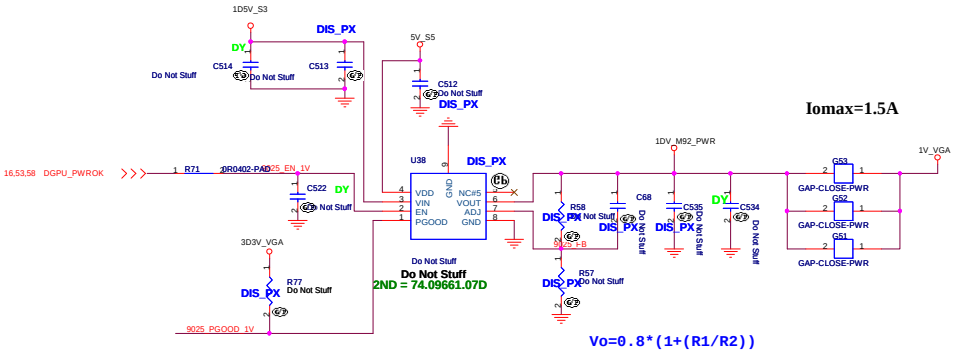
Title: ***AFTE_TP***		
Size	Document Number: **JE70-CP**	Rev: **-1M**
Date: Tuesday, February 02, 2010	Sheet 56 of 67	

+3VS to 3.3V_DELAY Transfer





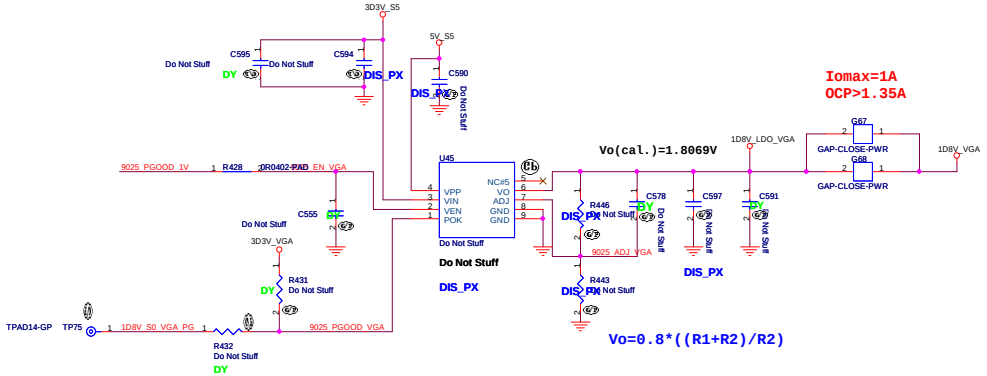
RT9025 for 1V_VGA



Iomax=1.5A

Vo=0.8*(1+(R1/R2))

G9661 for 1D8V_VGA



Iomax=1A
OCP>1.35A

Vo(cal.)=1.8069V

Vo=0.8*((R1+R2)/R2)

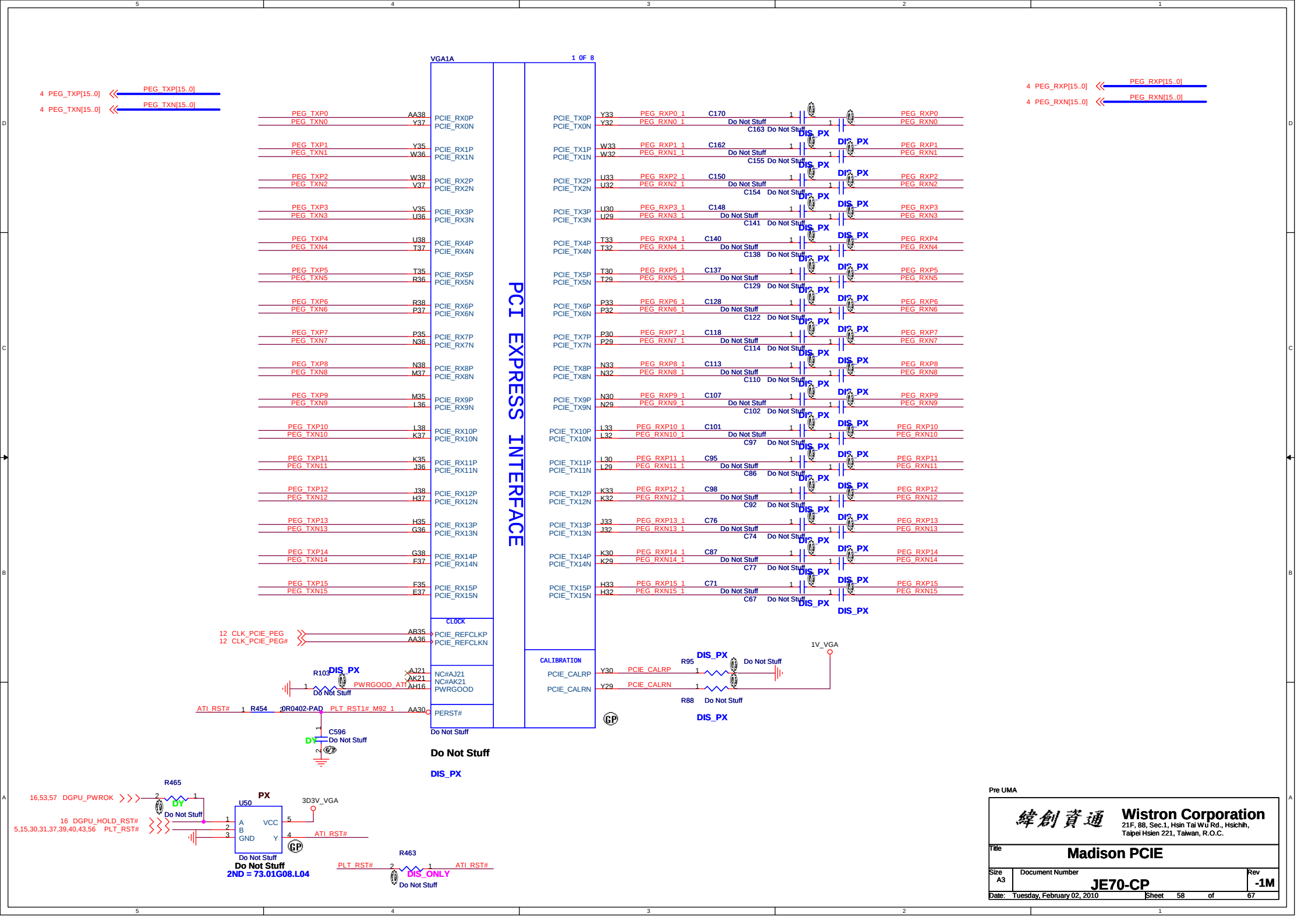
Pre UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI POWER

Size	Document Number	Rev
A2	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 57 of 67



Do Not Stuff

DIS_PX

Pre UMA

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Madison PCIE
Size A3	Document Number JE70-CP
Rev	-1M
Date: Tuesday, February 02, 2010	Sheet 58 of 67

Layout notice:
It should be pleace near HDMI connector

JV50-CP_JV70-CP_SJV50-CP / Madsion-Pro

0 1 0 0 Hynix Orion-die (H5TQ1G63BFR-12C, 800MHz)64*16 x 8 pcs2GB
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 8 pcs1GB
1 1 0 0 Reserve64*16 x 8 pcs1GB

JV50-CP_JV70-CP_SJV50-CP / Park-XT

0 1 0 0 Hynix Orion-die (H5TQ1G63BFR-12C, 800MHz)64*16 x 4 pcs512MB
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 4 pcs512MB
1 1 0 0 Reserve64*16 x 4 pcs512MB

It's strap for GDDR3-136ball
Need to Clarify

VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

SB 1118

For Thermal sensor

SB 1120

SB 1117

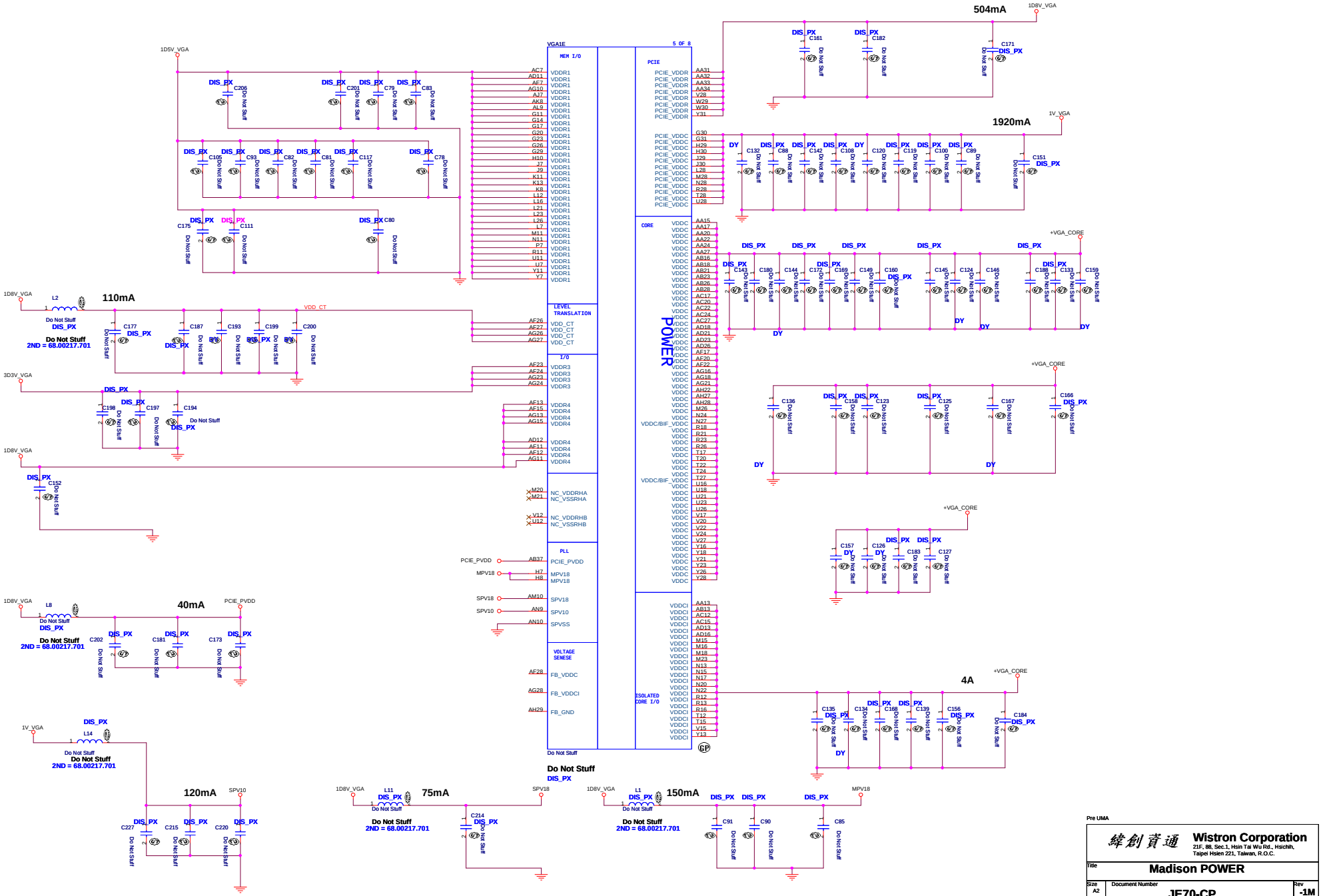
Do Not Stuff
2ND = 68.00217.701

Do Not Stuff
2ND = 82.30034.461

Do Not Stuff
2ND = 84.2N702.E31

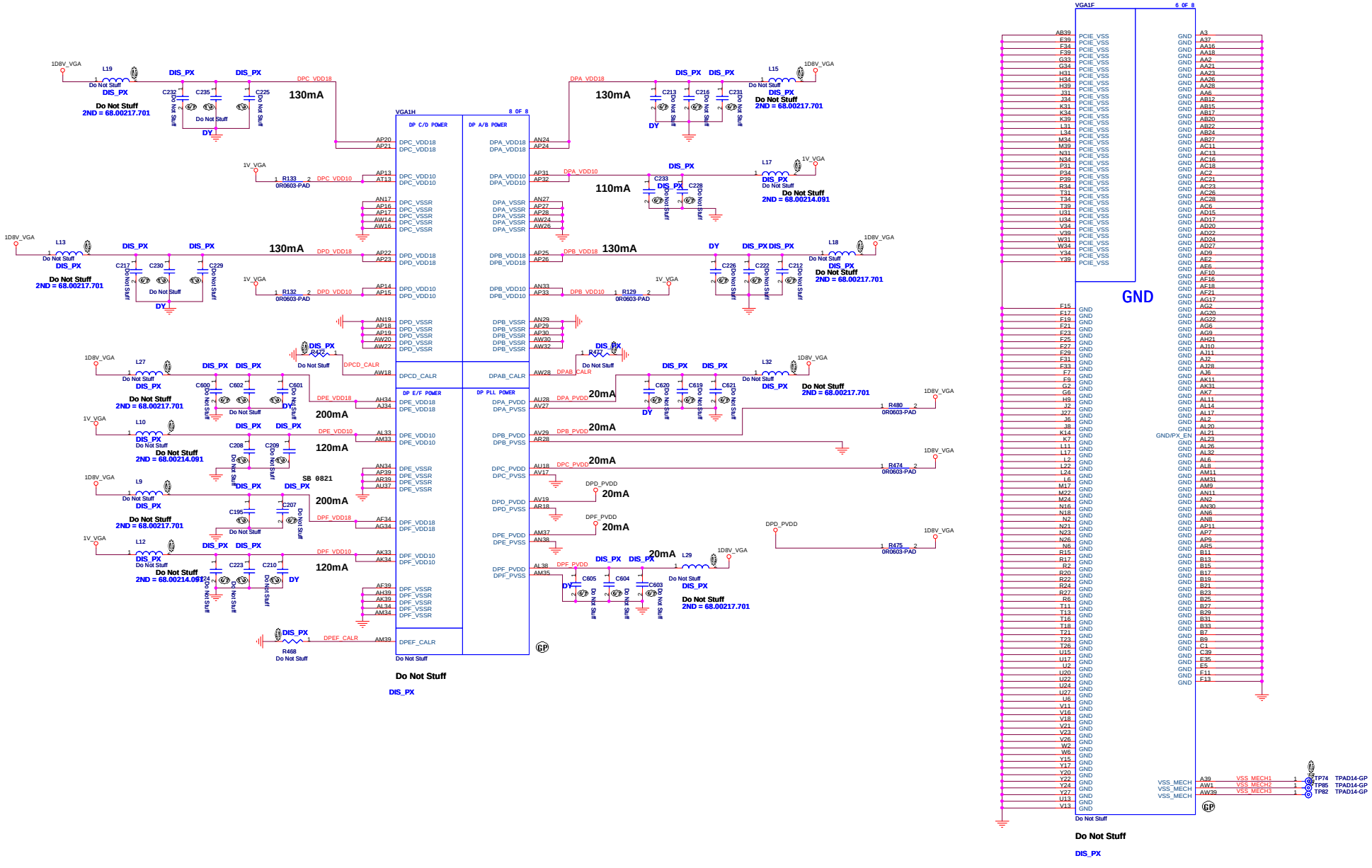
Pre UMA

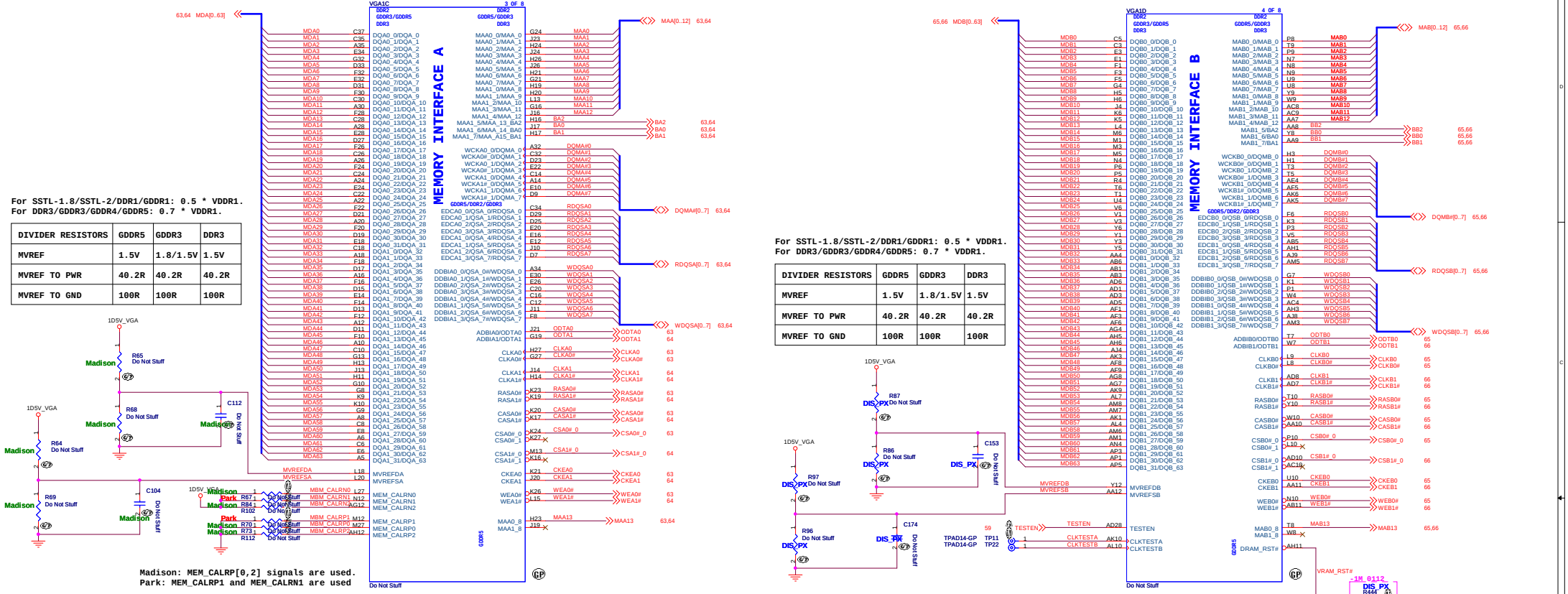
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Madison IO		
Size: A2	Document Number: JE70-CP	Rev: SB
Date: Tuesday, February 02, 2010	Sheet 59 of 67	



Pre UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Madison POWER
Size A2	Document Number JE70-CP
Rev	-1M
Date: Tuesday, February 02, 2010	Sheet 60 of 67


VGA1H
8 OF 8
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
130mA
110mA
20mA
200mA
120mA
SB 0821
Do Not Stuff
DIS_PX
2ND = 68.00217.701
2ND = 68.00214.091
VGA1F
6 OF 8
GND
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DP POWER_GND
JE70-CP
-1M
Tuesday, February 02, 2010
61
67



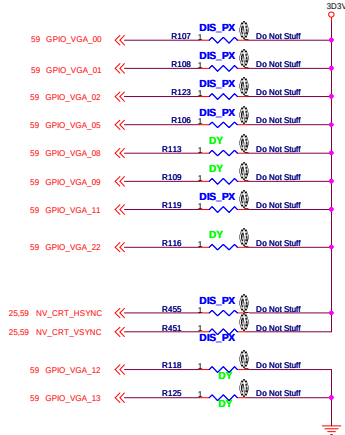
STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			



Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

Pre UMA

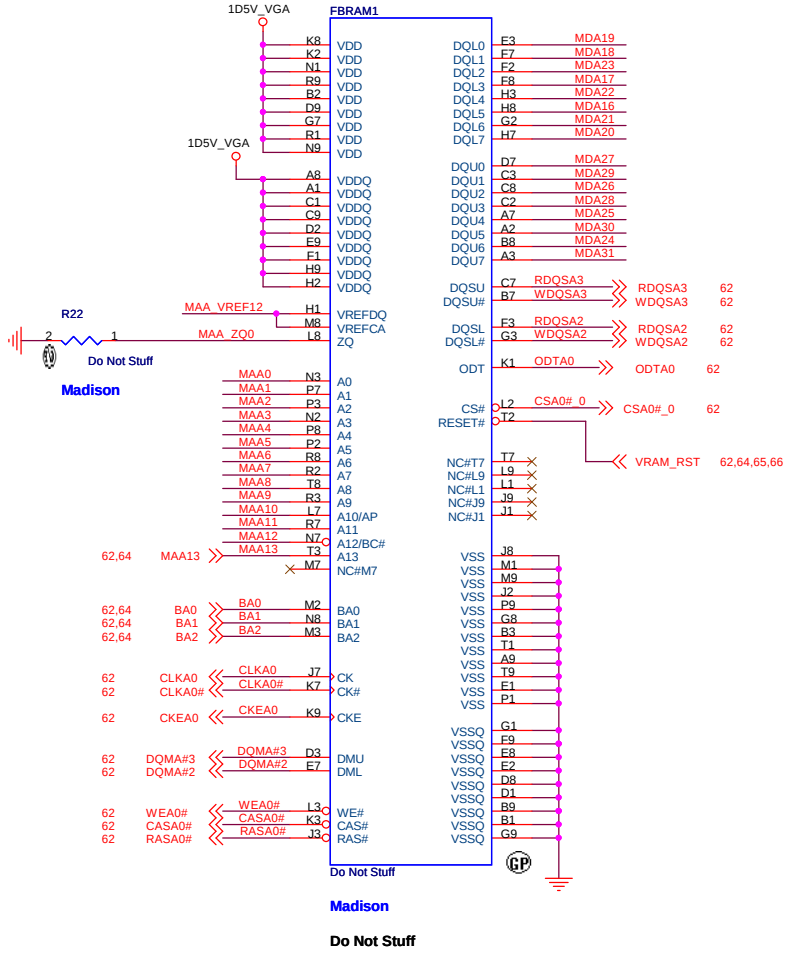
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

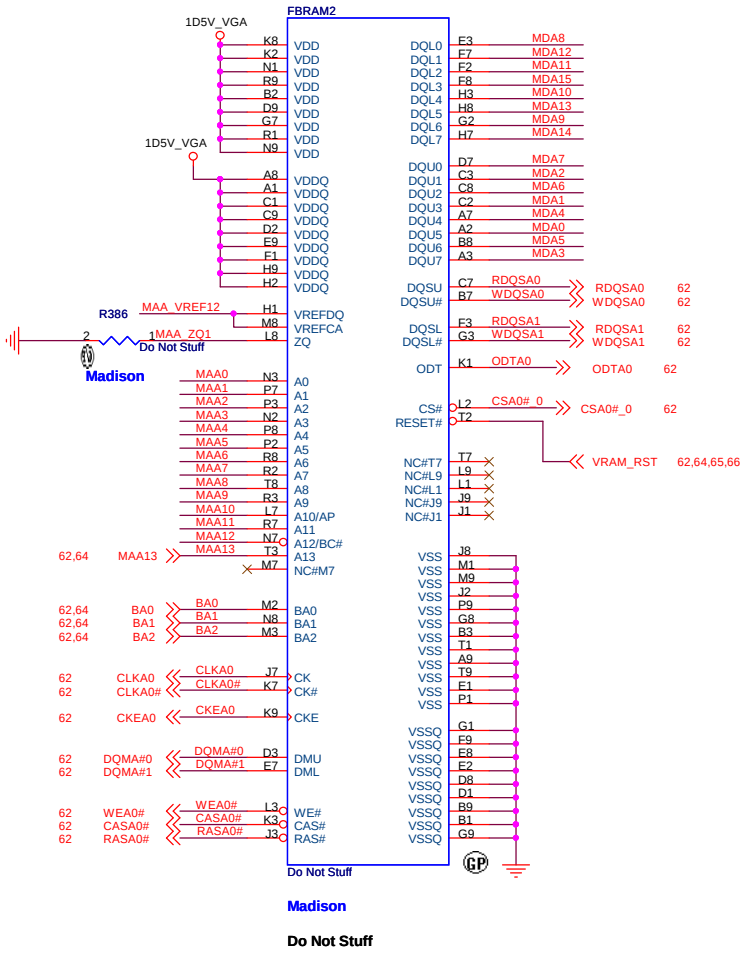
Title: **Madison Memory / Straps**

Size: A2 | Document Number: JE70-CP | Rev: -1M

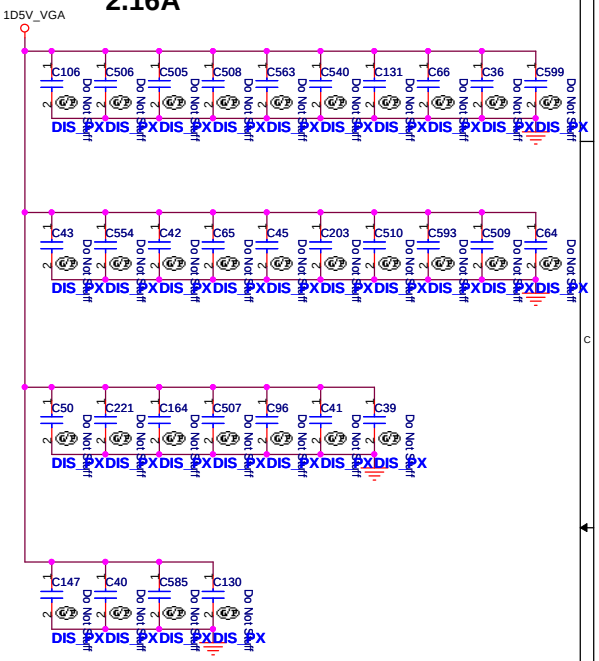
Date: Tuesday, February 02, 2010 | Sheet 62 of 67

DDR3

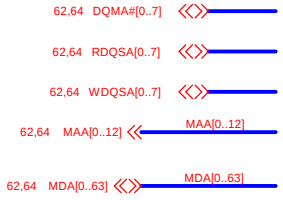


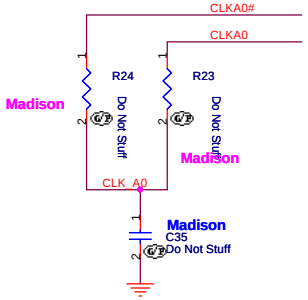


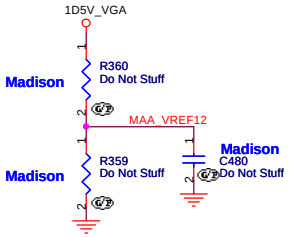
2.16A



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U





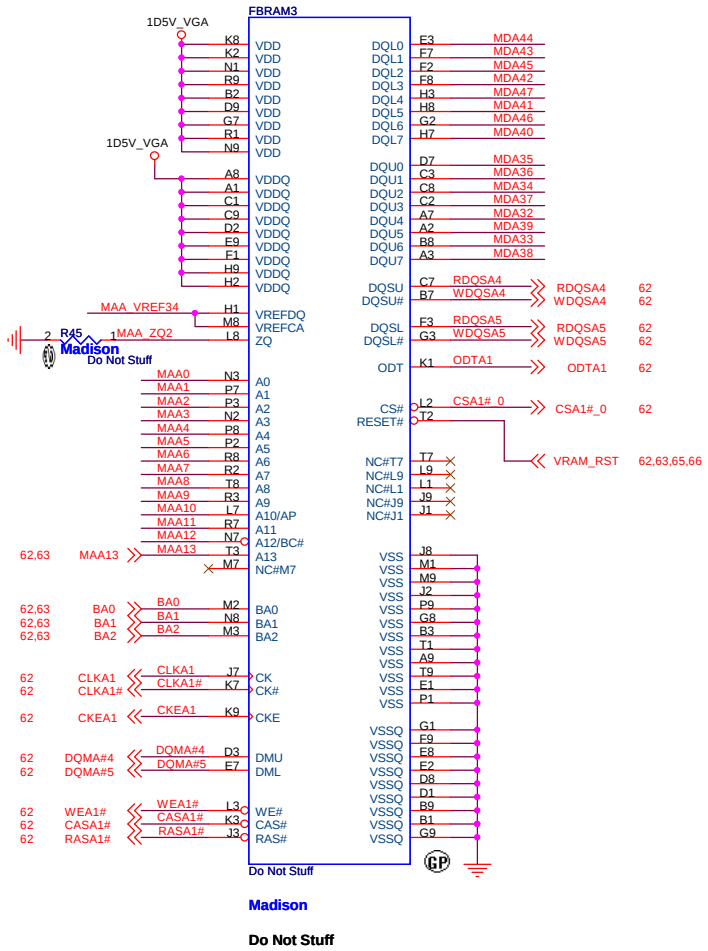


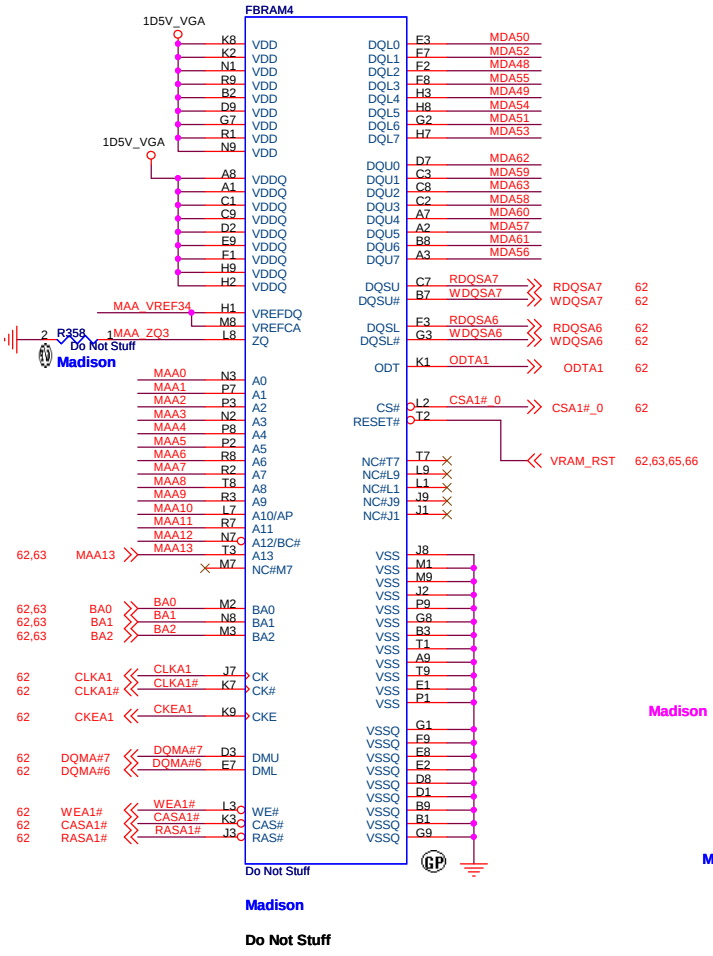
Pre UMA

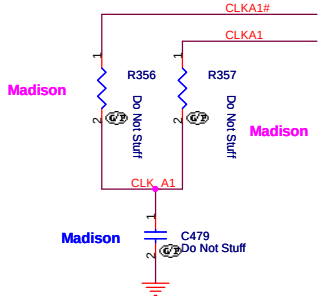
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*VRAM(1/4)*	
Size A3	Document Number JE70-CP	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 63 of 67	

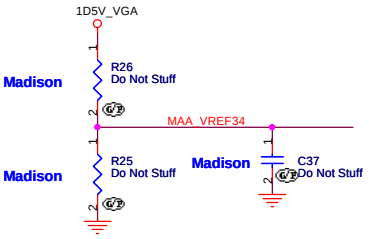
DDR3







SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

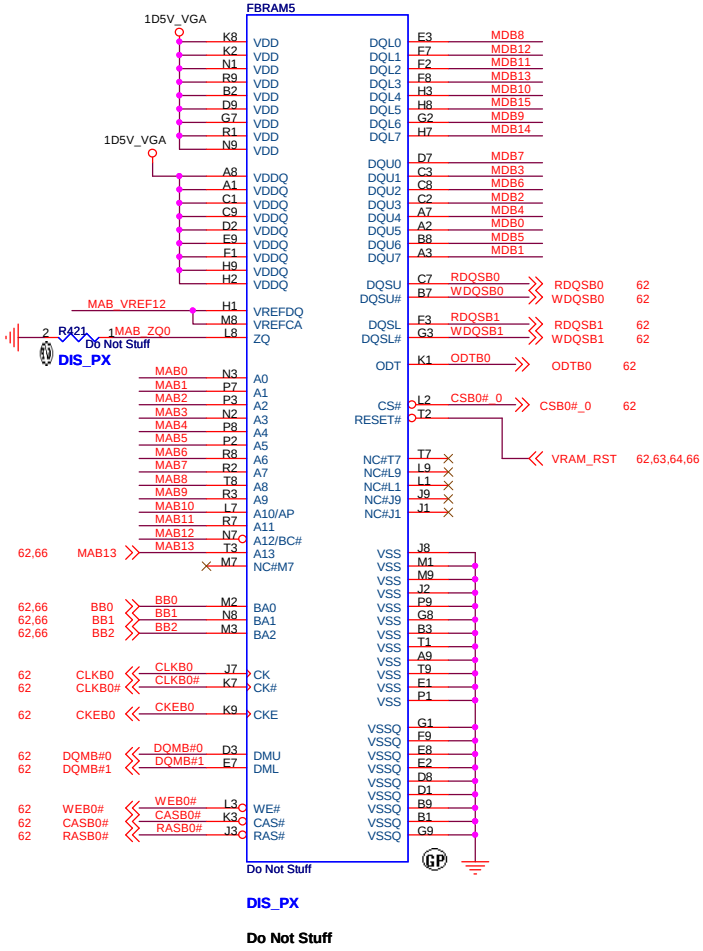


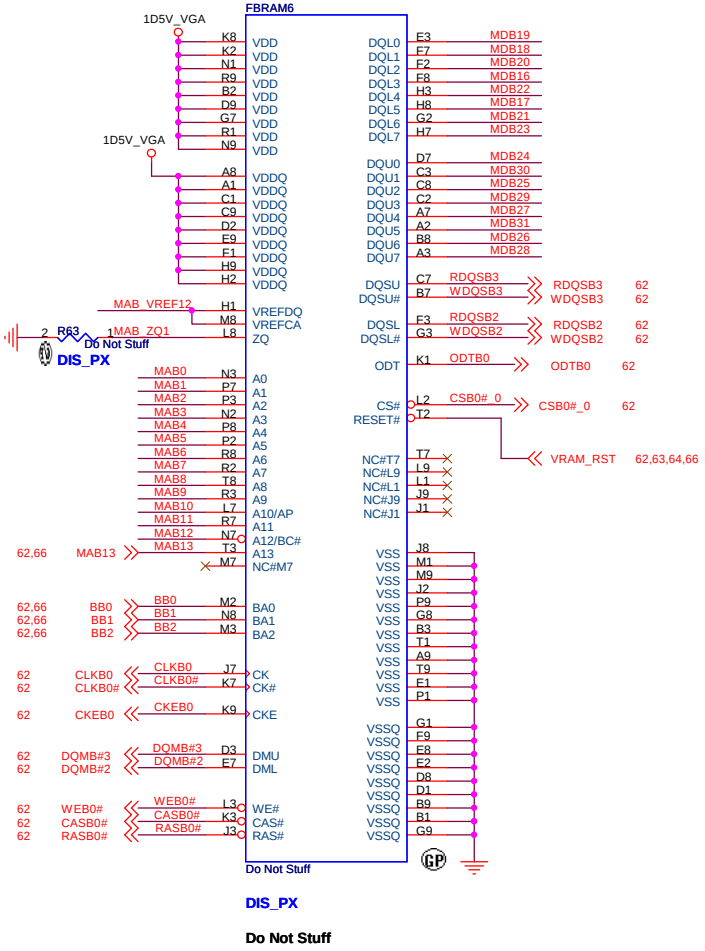
62,63 DQMA#[0..7]
62,63 RDQSA[0..7]
62,63 WDQSA[0..7]
62,63 MAA[0..12] MAA[0..12]
62,63 MDA[0..63] MDA[0..63]

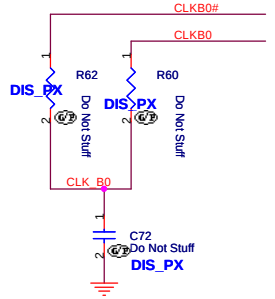
Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM(2/4)		
Size: A3	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 64 of 67	

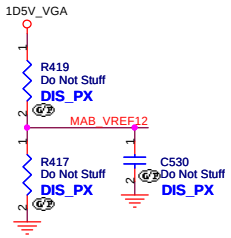
DDR3

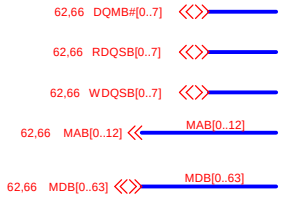






SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



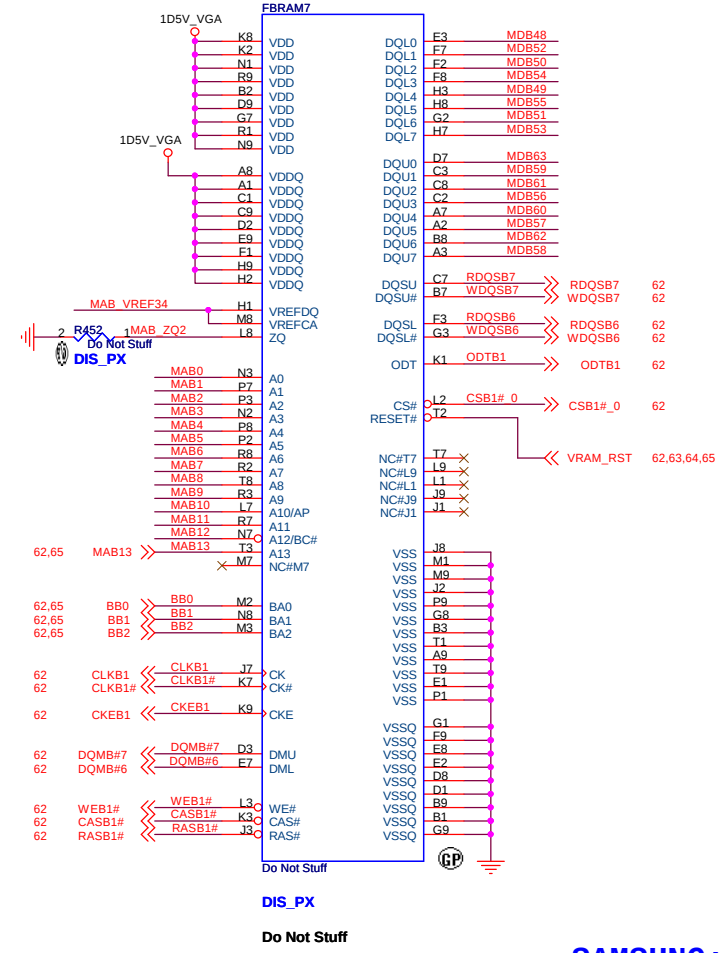


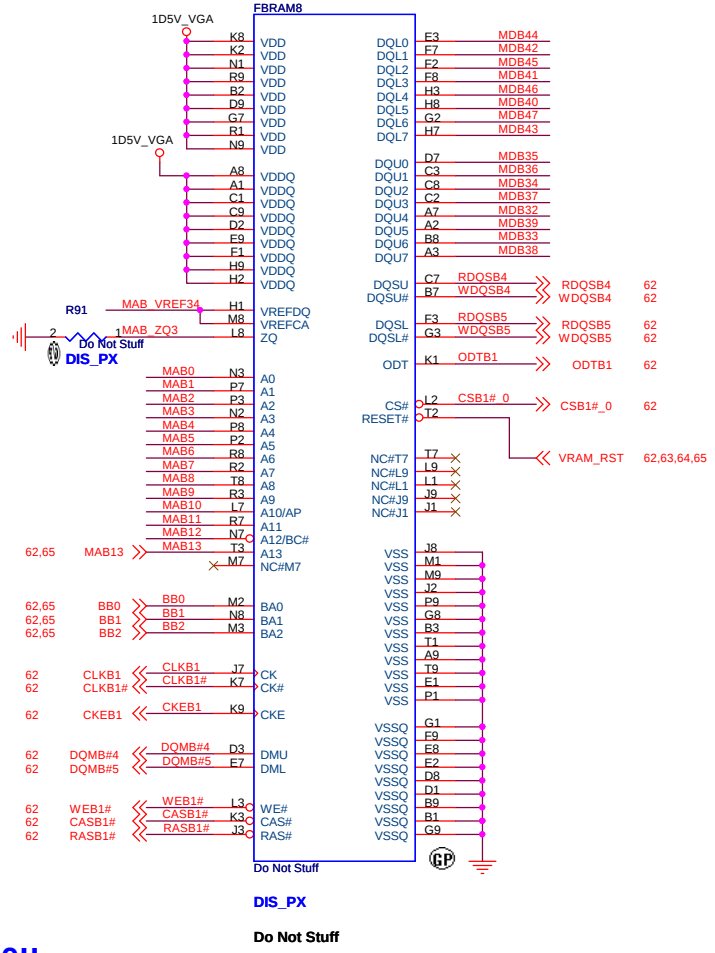
Pre UMA

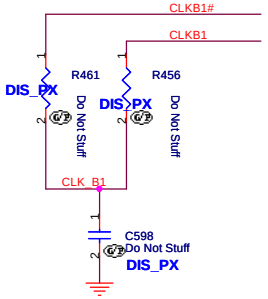
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*VRAM(3/4)*	
Size A3	Document Number JE70-CP	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 65 of 67	

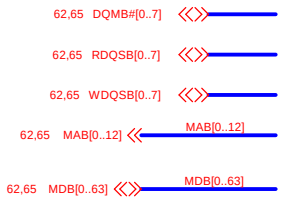
DDR3

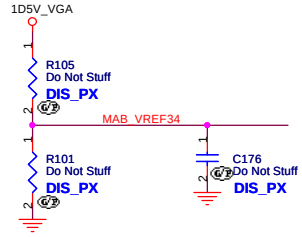






SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U





Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM(4/4)***

Size	Document Number	Rev
A3	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 66 of 67

Pre UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Modify History

Size	Document Number	Rev
	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 67 of 67