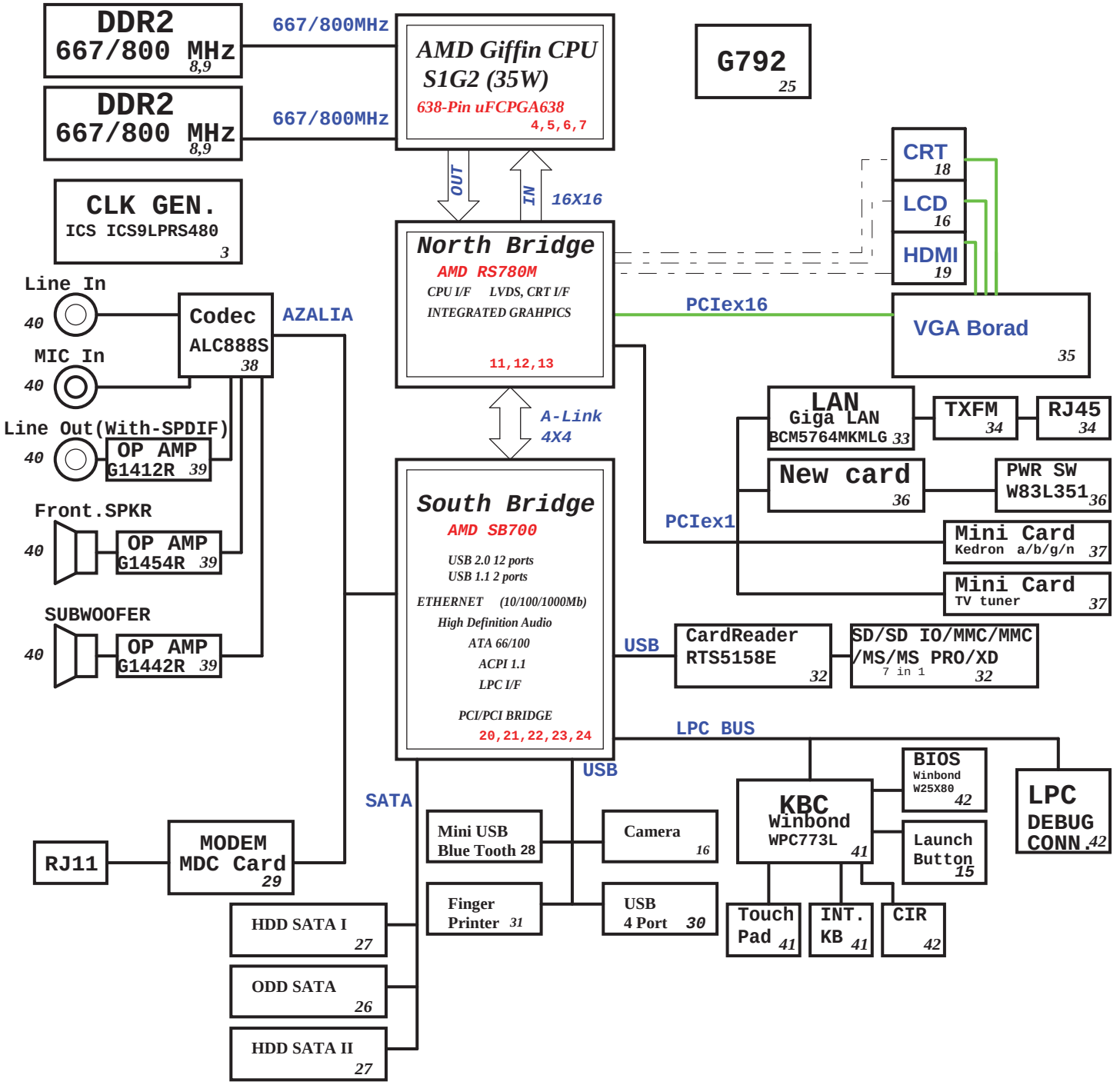
Big Bear 2A (AS 18") Block Diagram

Project code: 91.4AJ01.001
PCB P/N : 48.4AJ01.001
REVISION : 08208-1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 47	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A)

SYSTEM DC/DC TPS51124 48	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(8A) 1D2V_S0(5A)

SYSTEM DC/DC TPS51117 49	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(10A)
RT9026PFP 50	
1D8V_S3	DDR_VREF_S3 0D9V_S3(1A)
RT9166 50	
3D3V_S0	2D5V_S0 (300mA)
G957 50	
3D3V_S0	1D5V_S0(1A)
G9161 50	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731A 51	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 46	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	Big Bear 2A	SC

Date: Monday, October 27, 2008 Sheet 1 of 55

<Core Design>

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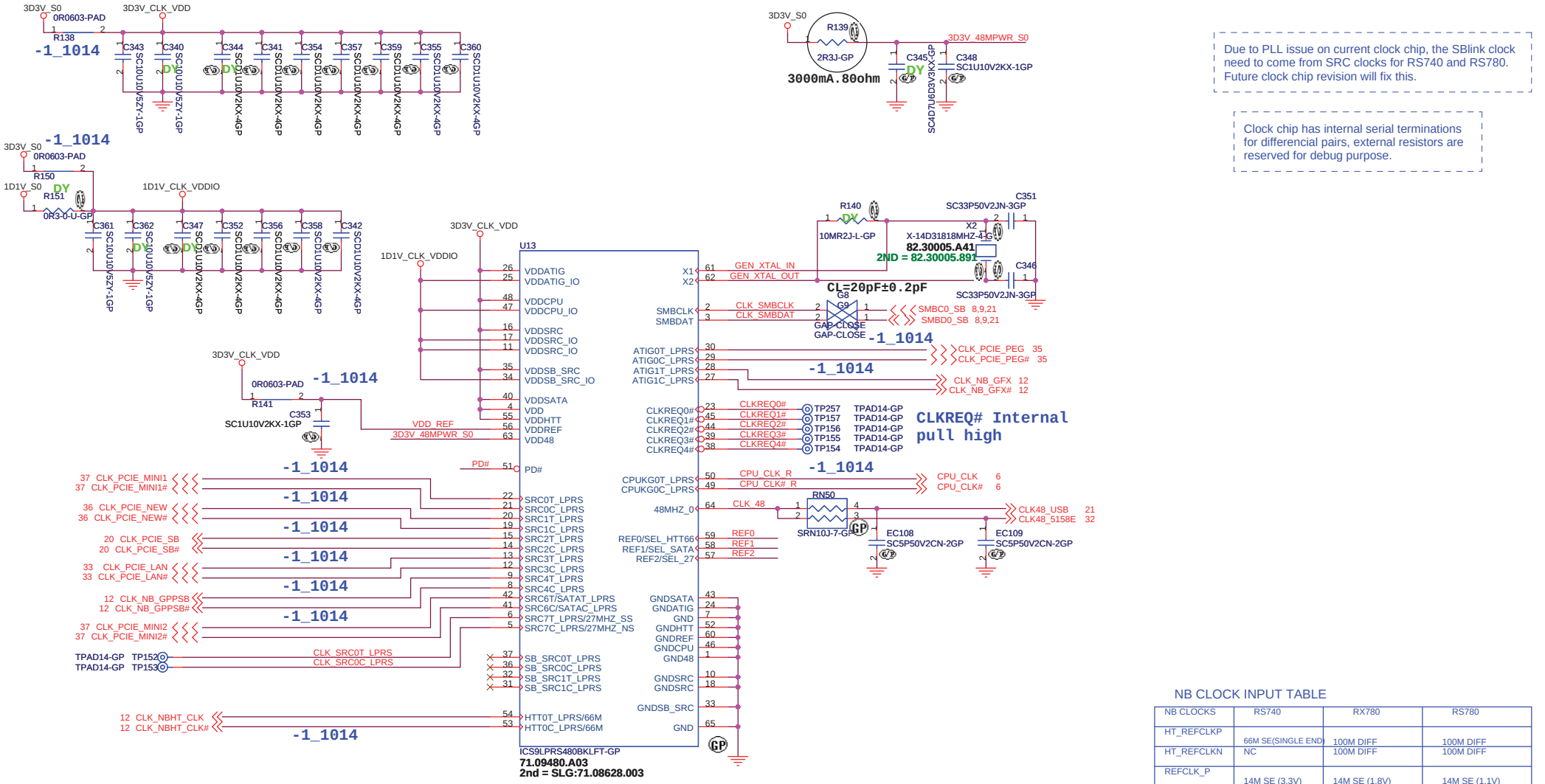
Title
HISTORY

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 2 of 55



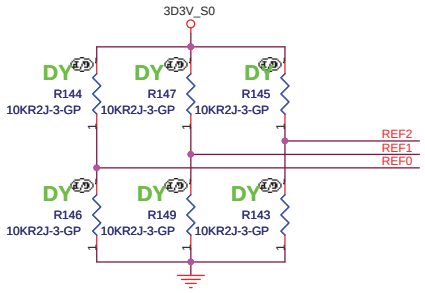
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

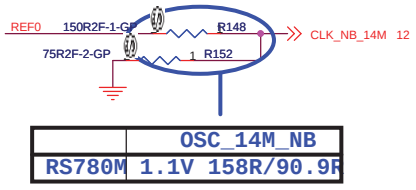
* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.



SEL_27 REF2	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0*	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0 *	100MHz differential HTT clock

* default

CPU_CLK(200MHz)



	OSC_14M_NB
RS780M	1.1V 158R/90.9R

<Core Design>

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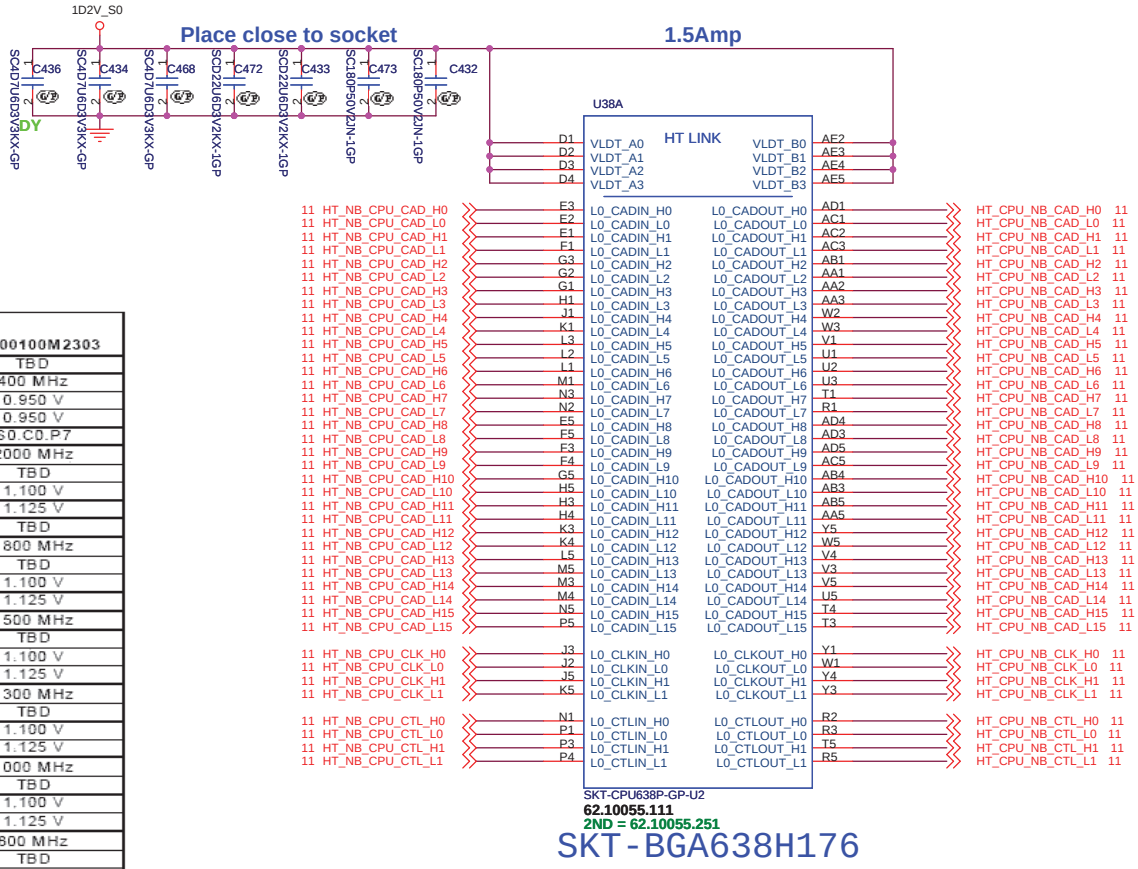
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS9LPRS480

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 3 of 55



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Core Design>

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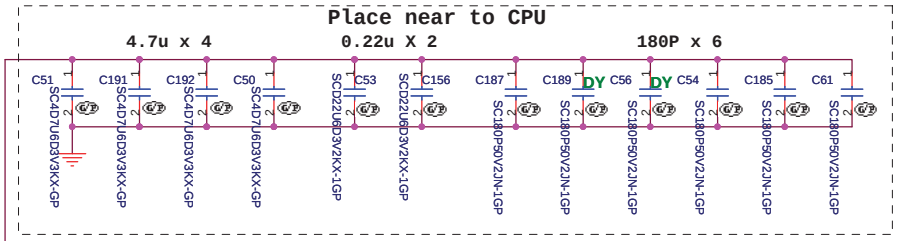
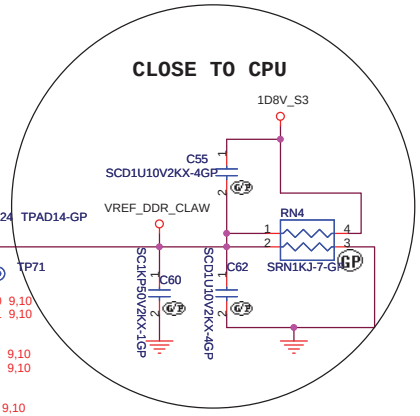
Taipei Hsien 221, Taiwan, R.O.C.

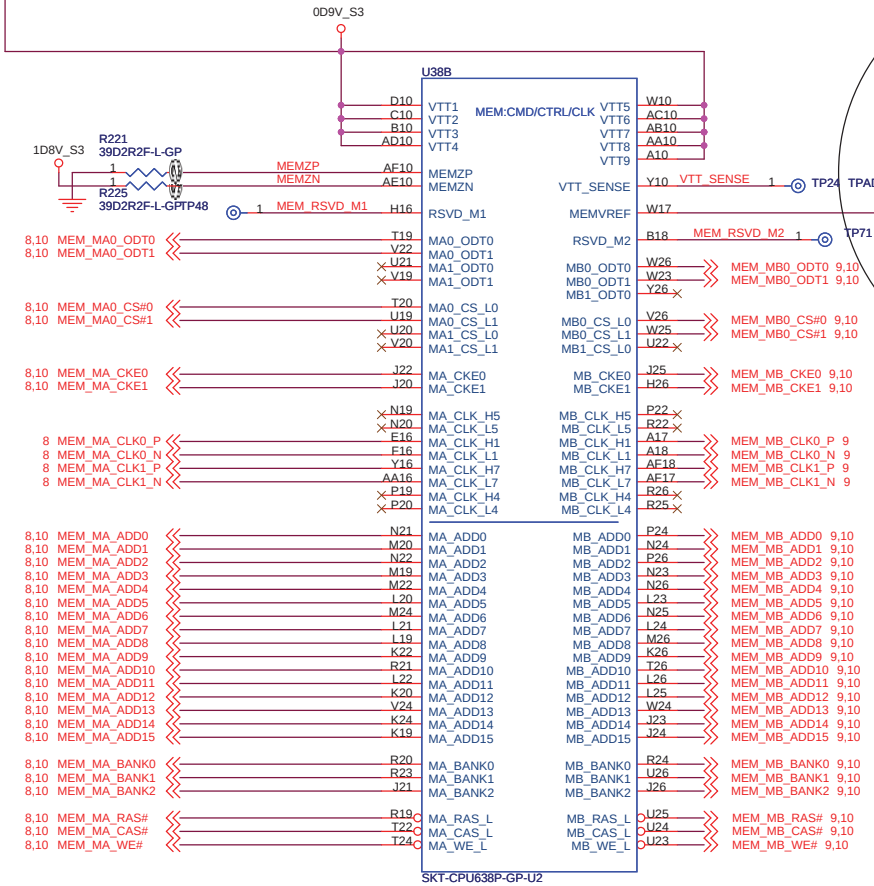
Title: CPU_HT_LINK I/F_(1/4)

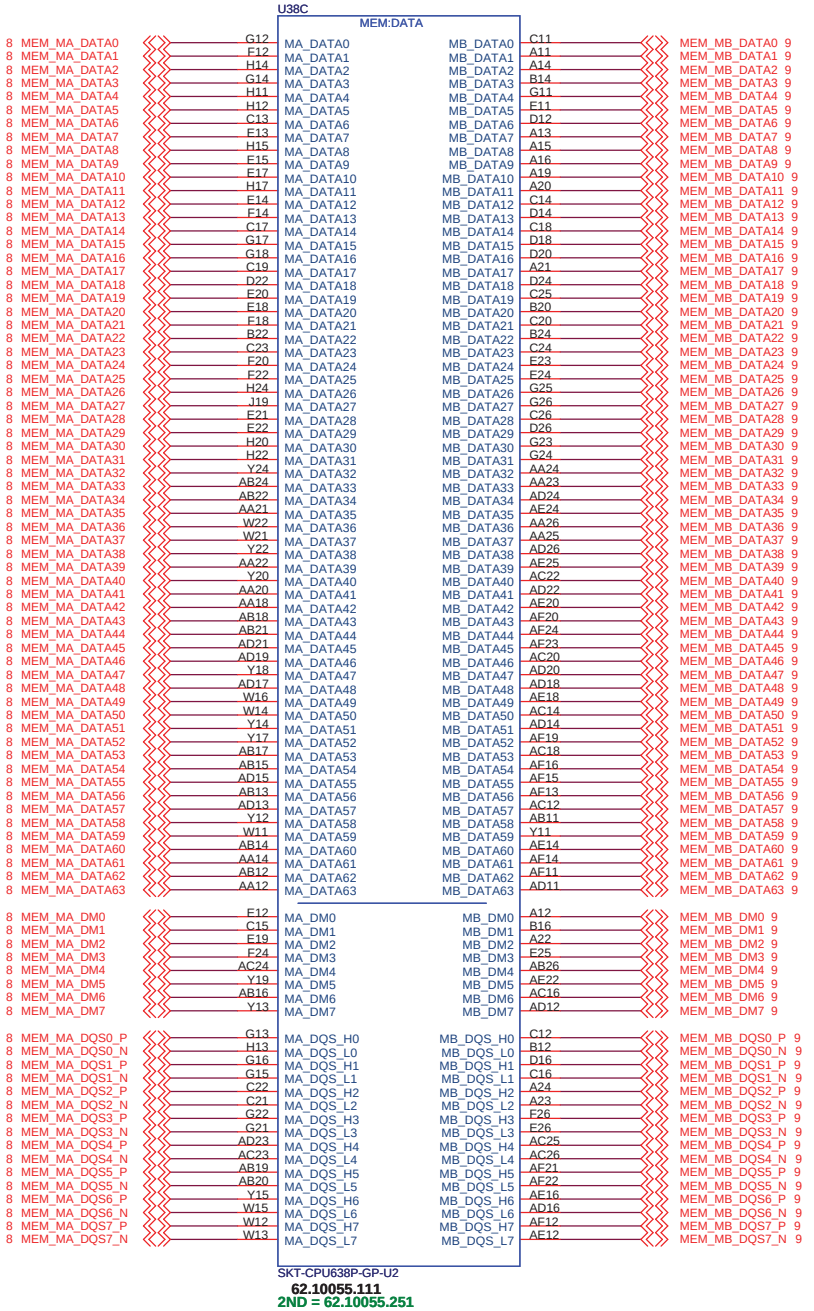
Size: A3 | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 4 of 55









<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU_DDR_(2/4)***	
Size: A3	Document Number: **Big Bear 2A**	Rev: SA
Date: Monday, October 27, 2008	Sheet 5 of 55	

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

1D8V_S0
RN31
SRN300J-1-GP
-1_1014
20,53 CPU_LDT_RST# — R257 0R0402-PAD — LDT_RST#_CPU
20,53 CPU_PWRGD — R258 0R0402-PAD — LDT_PWROK
20 CPU_LDT_STOP# — R62 0R0402-PAD — LDT_STP#_CPU 12
12,20 ALLOW_LDTSTOP — R255 0R0402-PAD — CPU_LDT_REQ#_CPU
SB with 0402 PAD

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491
LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.
2D5V_S0 — R55 0R3-0-U-GP — 2D5V_VDDA_S0
C162 DY SC10U10V5ZY-1GP
C163 SC4D7U6D3V3KX-GP
C153 SC3300P50V2KX-1GP
C164 SC10U10V5ZY-1GP
C161 SCD22U10V3KX-2GP

Cloce To CPU
3 CPU_CLK — C481 SC3900P50V2KX-2GP — R263 169R2F-GP — CLKCPU_IN
3 CPU_CLK# — C488 SC3900P50V2KX-2GP — CLKCPU# IN

LDT_RST# CPU
HDT_RST# — R256 0R0402-PAD
For HDT DBG

1D2V_S0 — R48 44D2R2F-GP — R49 44D2R2F-GP
TPAD14-GP TP180 CPU_SIC
TPAD14-GP TP175 CPU_SID
TPAD14-GP TP174 CPU_ALERT#
CPU_HTREF0
CPU_HTREF1

U38D
F8 VDDA1
F9 VDDA2
A9 CLKIN_H
A8 CLKIN_L
B7 RESET_L
A7 PWROK
F10 LDTSTOP_L
C6 LDTREQ_L
AF4 SIC
AF5 SID
AE6 ALERT_L
R6 HT_REF0
P6 HT_REF1
F6 VDD0_FB_H
E6 VDD0_FB_L
Y6 VDD1_FB_H
AB6 VDD1_FB_L
G10 DBRDY
AA9 TMS
AC9 TCK
AD9 TRST_L
AF9 TDI
AD7 TEST23
H10 TEST18
G9 TEST19
F9 TEST25_H
E8 TEST25_L
AB8 TEST21
AF7 TEST20
AF7 TEST24
AE8 TEST22
AC8 TEST12
AF8 TEST27
C2 TEST9
AA6 TEST6
A3 RSVD1
A5 RSVD2
B3 RSVD3
B5 RSVD4
C1 RSVD5
M11 KEY1
W18 KEY2
A6 SVC
A4 SVD
THERMTRIP_L
PROCHOT_L
MEMHOT_L
THERMDC
THERMDA
VDDIO_FB_H
VDDIO_FB_L
VDDNB_FB_H
VDDNB_FB_L
DBREQ_L
TDO
TEST28_H
TEST28_L
TEST17
TEST16
TEST15
TEST14
TEST7
TEST10
TEST8
TEST29_H
TEST29_L
H18 RSVD10
H19 RSVD9
AA7 RSVD8
D5 RSVD7
C5 RSVD6
SKT-CPU638P-GP-U2
62.10055.111
2ND = 62.10055.251

RN84
SRN300J-1-GP
TP69 CPU_TEST23
CPU_TEST18
CPU_TEST19
TP65 CPU_TEST25_H
TP64 CPU_TEST25_L
TP176 CPU_TEST21
CPU_TEST20
CPU_TEST24
CPU_TEST22
CPU_TEST12
CPU_TEST27
R254 0R0402-PAD CPU_TEST9

1D8V_S3
RN30
SRN1KJ-7-GP
A6 CPU_SVC 46
A4 CPU_SVD 46
RN65
SRN300J-1-GP
R433 300R2J-4-GP DY
CPU_TEST27
CPU_DBREQ#
-1_1014
AF6 THERMTRIP#
AC7 PROCHOT#
AA8 CPU_MEMHOT#
R227 0R0402-PAD PROCHOT#_SB 20
internal pull high 300 ohm
W7 H_THERMDC 25
W8 H_THERMDA 25
C58 DY SC100P50V2JN-3GP
W9 CPU_VDDIO_SUS_FB_H — TP28
Y9 CPU_VDDIO_SUS_FB_L — TP27
H6 CPU_VDDNB_RUN_FB_H 46
G6 CPU_VDDNB_RUN_FB_L 46
LAYOUT: Route FBCLKOUT_H/L differentially impedance 80
E10 CPU_DBREQ#
AE9 CPU_TDO
J7 CPU_TEST28_H — TP52
H8 CPU_TEST28_L — TP54
D7 CPU_TEST17 — TP68
E7 CPU_TEST16 — TP63
F7 CPU_TEST15
C7 CPU_TEST14
C3
K8
C4
C9 CPU_TEST29H — TP184
C8 CPU_TEST29L — TP185
H18
H19
AA7
D5
C5

-1_1014
46 CPU_PWRGD_SVID_REG — R259 0R0402-PAD — LDT_PWROK
C483 DY SCD1U16V2ZY-2GP
Near CPU PIN

LDT_PWROK
R261 2K2R2J-2-GP
C482 1D8V_1US_Q2 SCD1U16V2ZY-2GP
Q21 MMBT3904-4-GP
THERMTRIP# — KBC_THERMTRIP# 25,41
84.T3904.C11
2ND = 84.03904.T11
CPU exceeds to 125℃

HDT Connectors
CPU_DBREQ# — TP17 TPAD14-GP
CPU_DBRDY — TP50 TPAD14-GP
CPU_TCK — TP21 TPAD14-GP
CPU_TMS — TP23 TPAD14-GP
CPU_TDI — TP20 TPAD14-GP
CPU_TRST# — TP19 TPAD14-GP
CPU_TDO — TP18 TPAD14-GP
1D8V_S3 — TP29 TPAD14-GP
HDT_RST# — TP183 TPAD14-GP

CPU_TEST19 — R226 300R2J-4-GP DY
CPU_TEST18 — R45 300R2J-4-GP DY
CPU_TEST14 — R431 300R2J-4-GP DY
CPU_TEST15 — R432 300R2J-4-GP DY

<Core Design>
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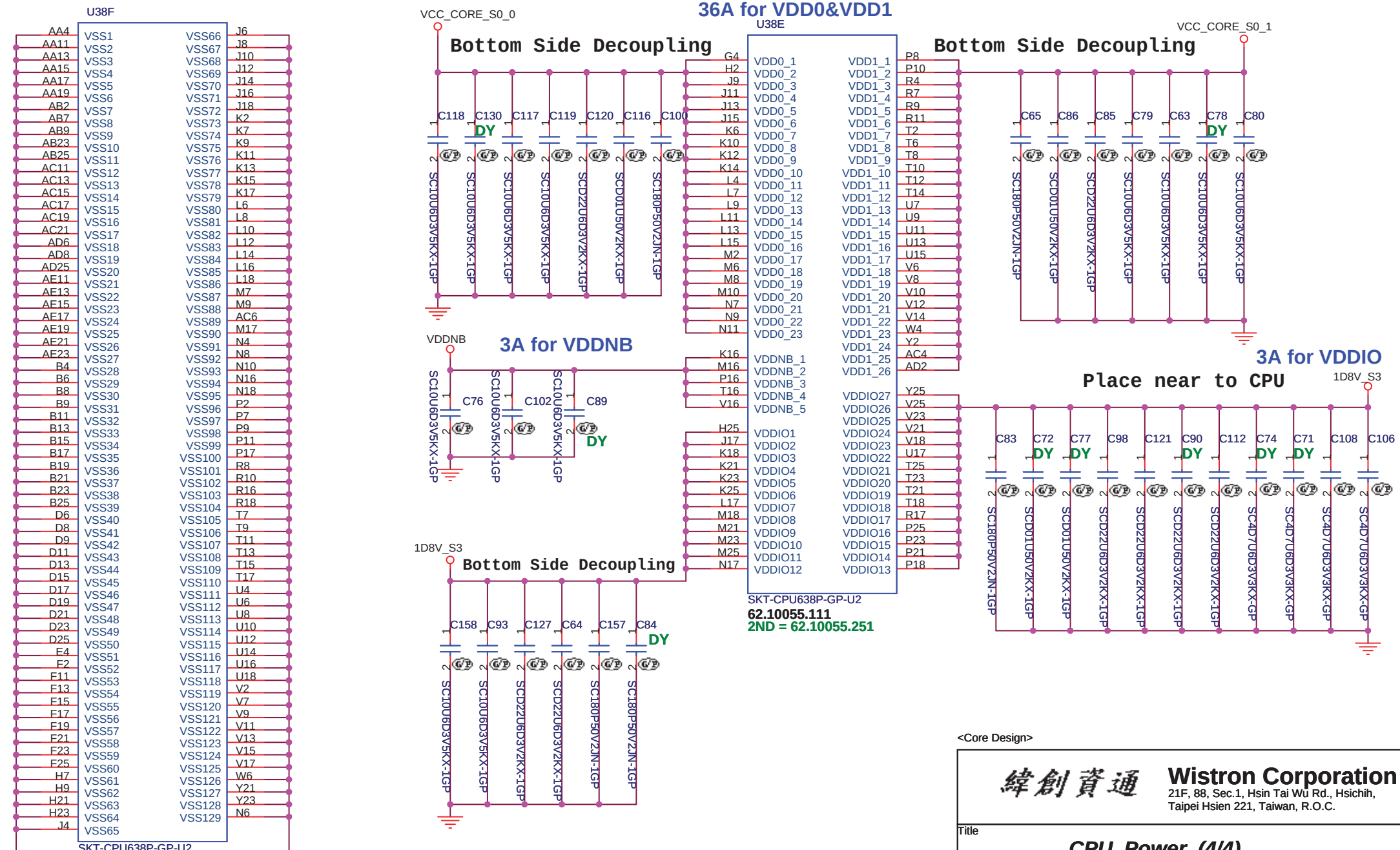
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU_Control&Debug_(3/4)
Size: A3 | Document Number: Big Bear 2A | Rev: SC
Date: Monday, October 27, 2008 | Sheet 6 of 55



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Power_(4/4)

Size	Document Number	Rev
A4	Big Bear 2A	SA

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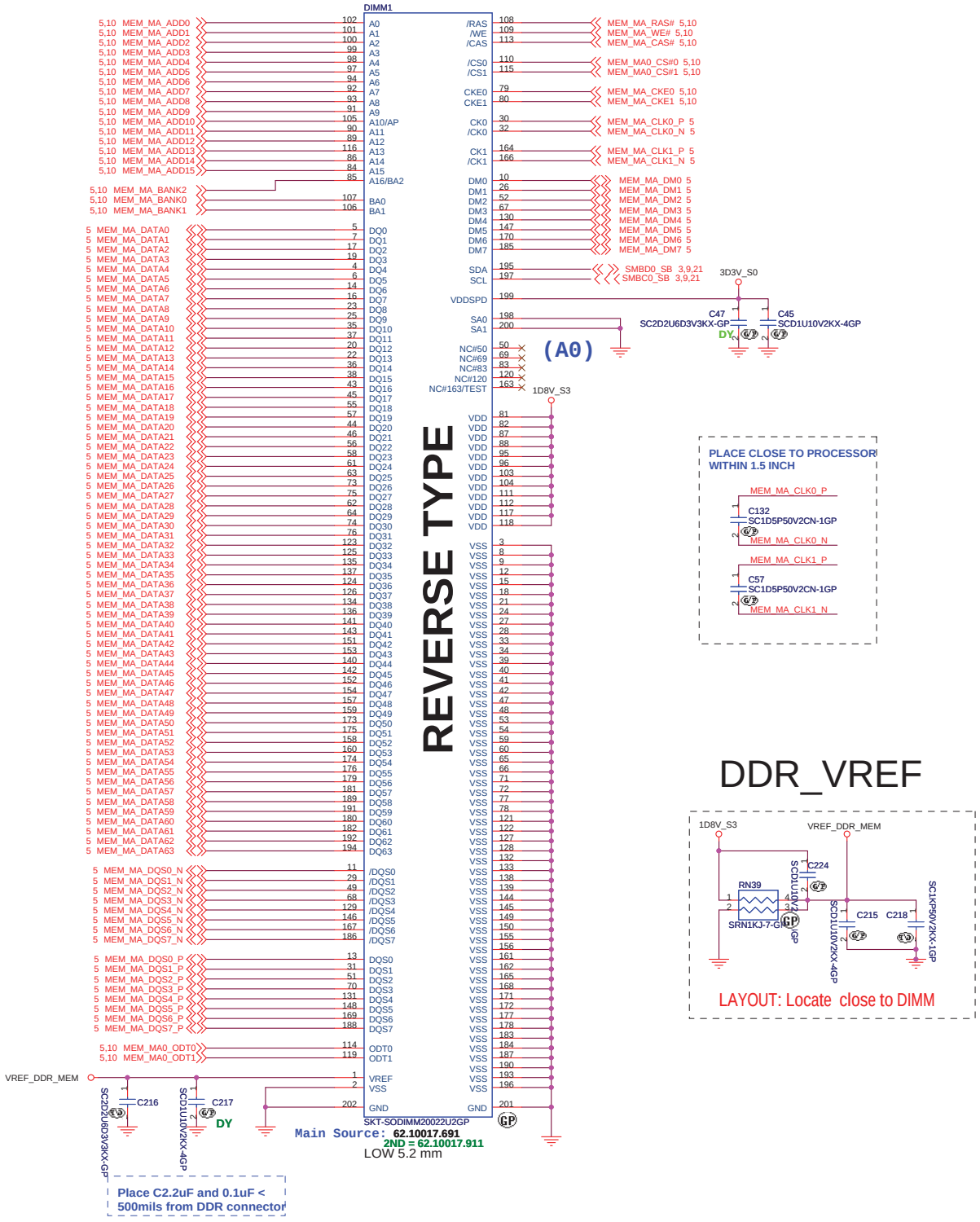

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size	Document Number	Rev
Custom	Big Bear 2A	SA

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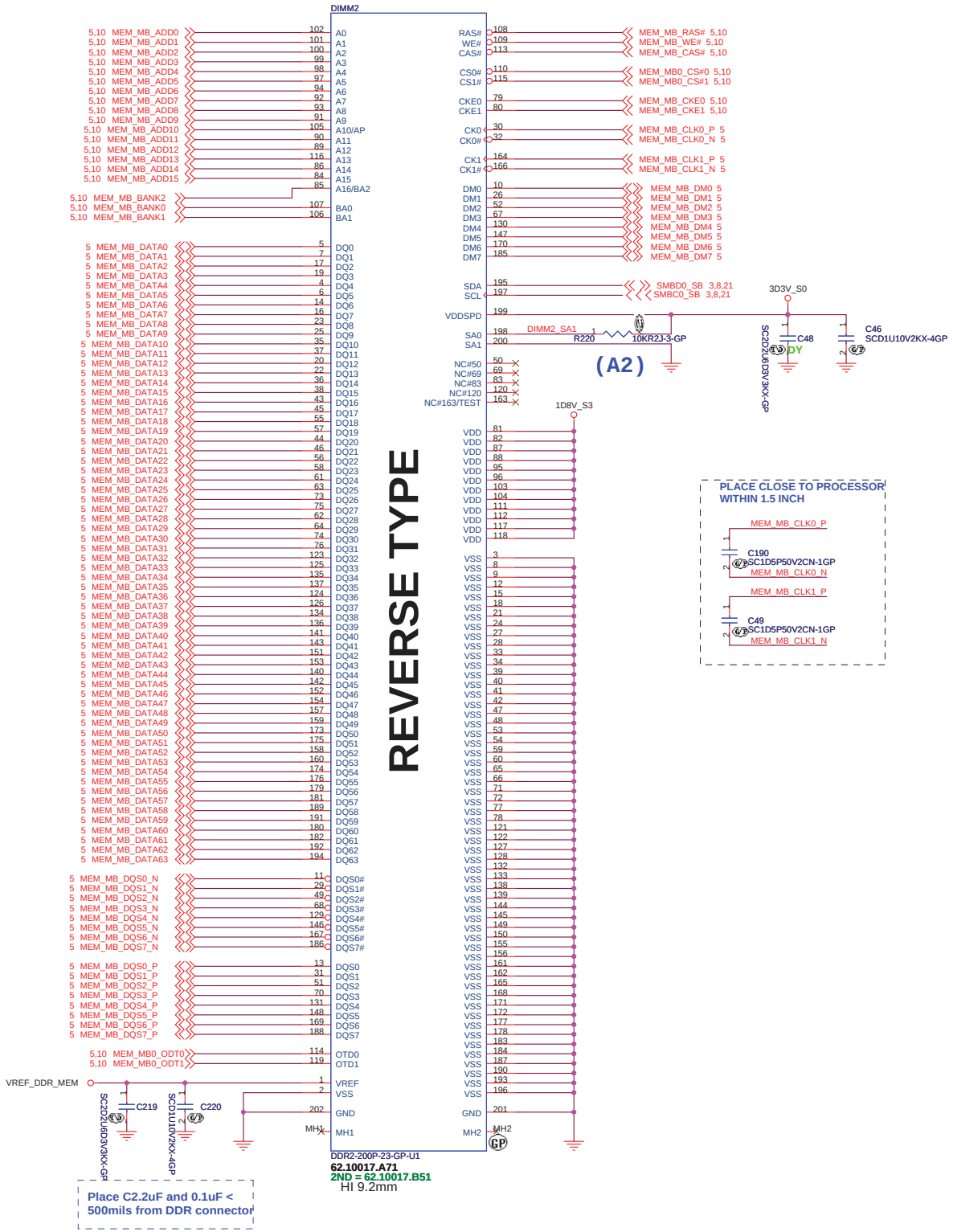

<Core Design>

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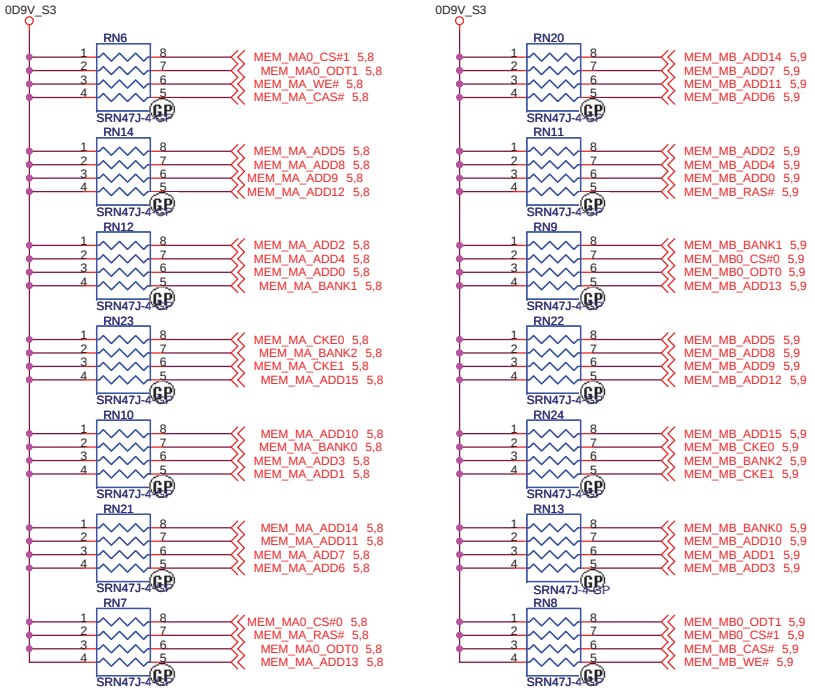
Title: DDR_SO-DIMM SKT_2

Size: Custom | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 9 of 55

PARALLEL TERMINATION

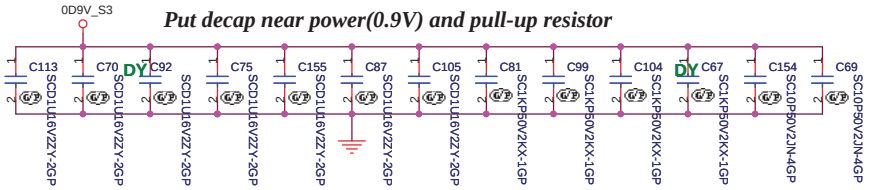
Put decap near power(0.9V) and pull-up resistor



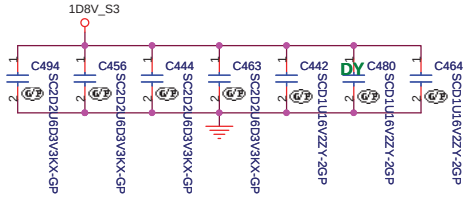
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

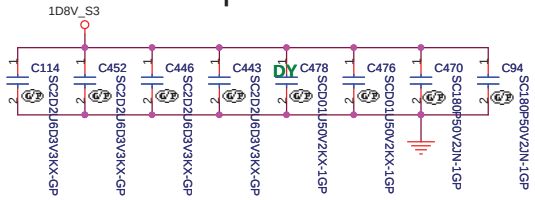


Place these Caps near DM1



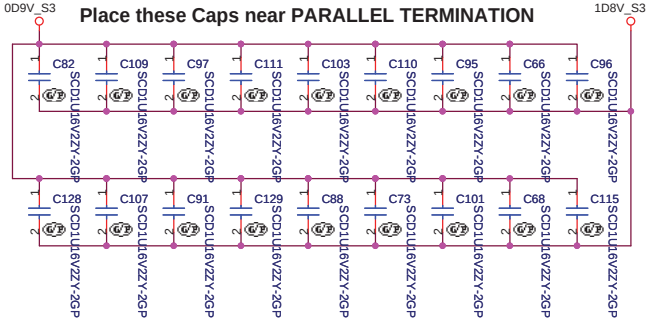
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



<Core Design>

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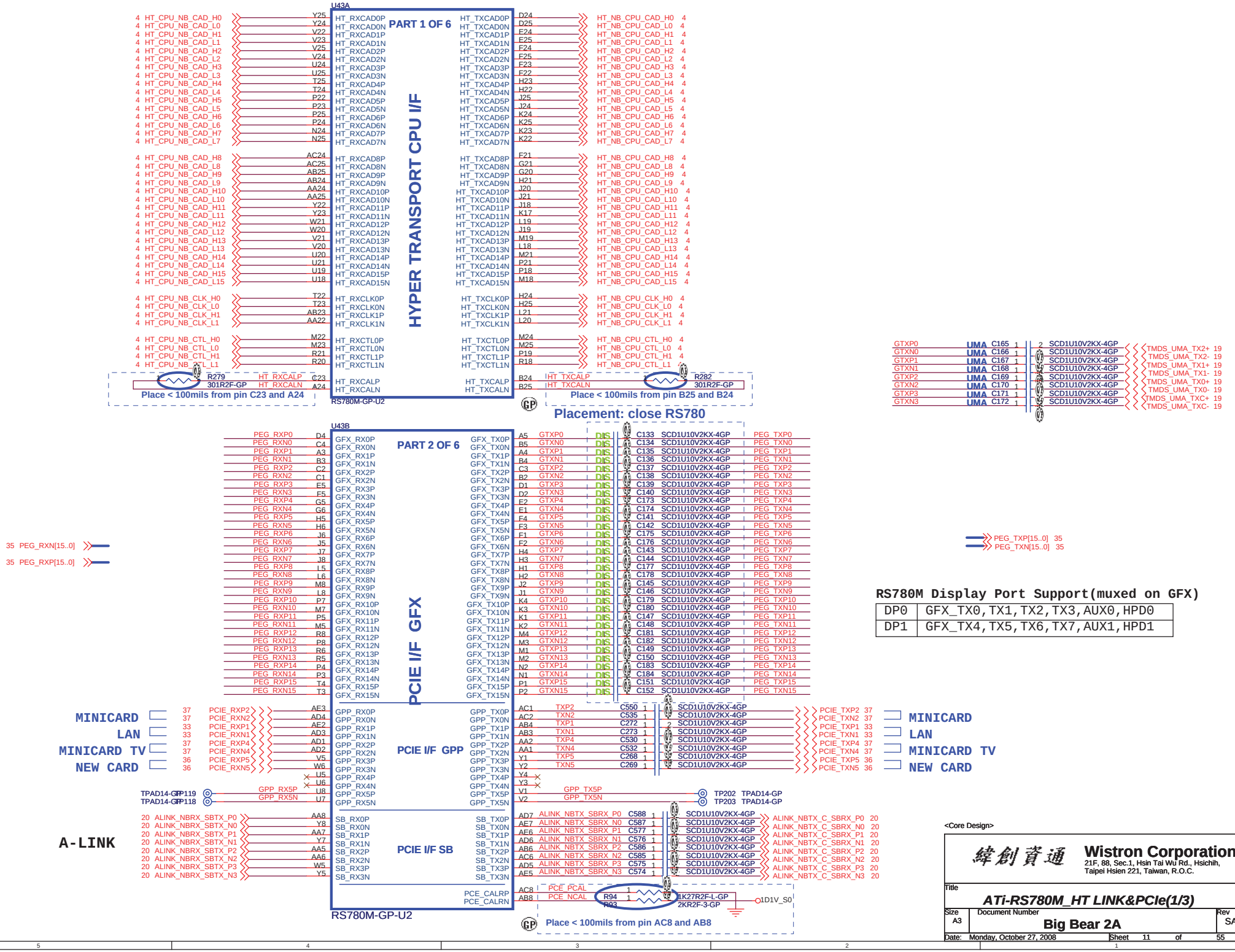
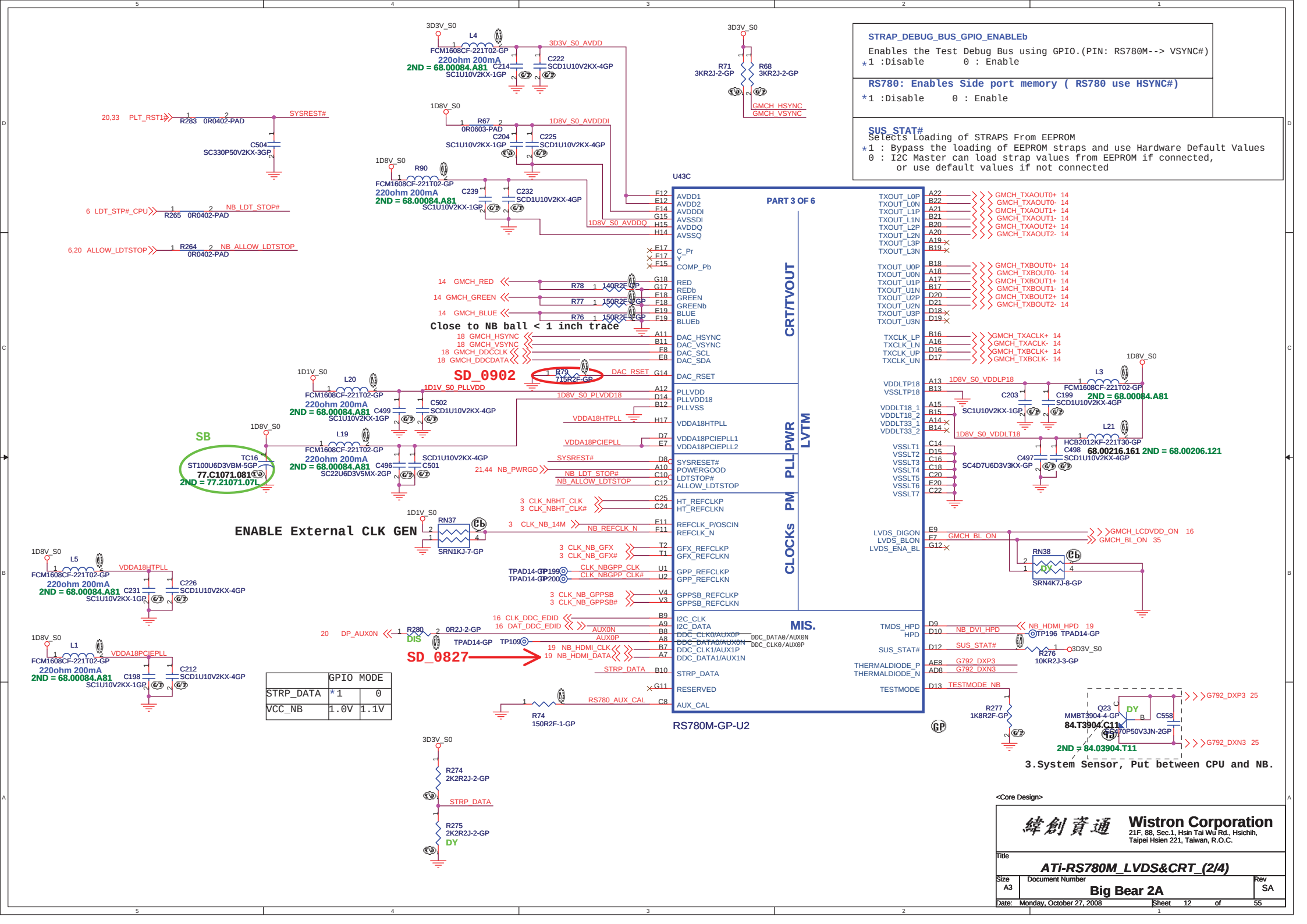
Taipei Hsien 221, Taiwan, R.O.C.

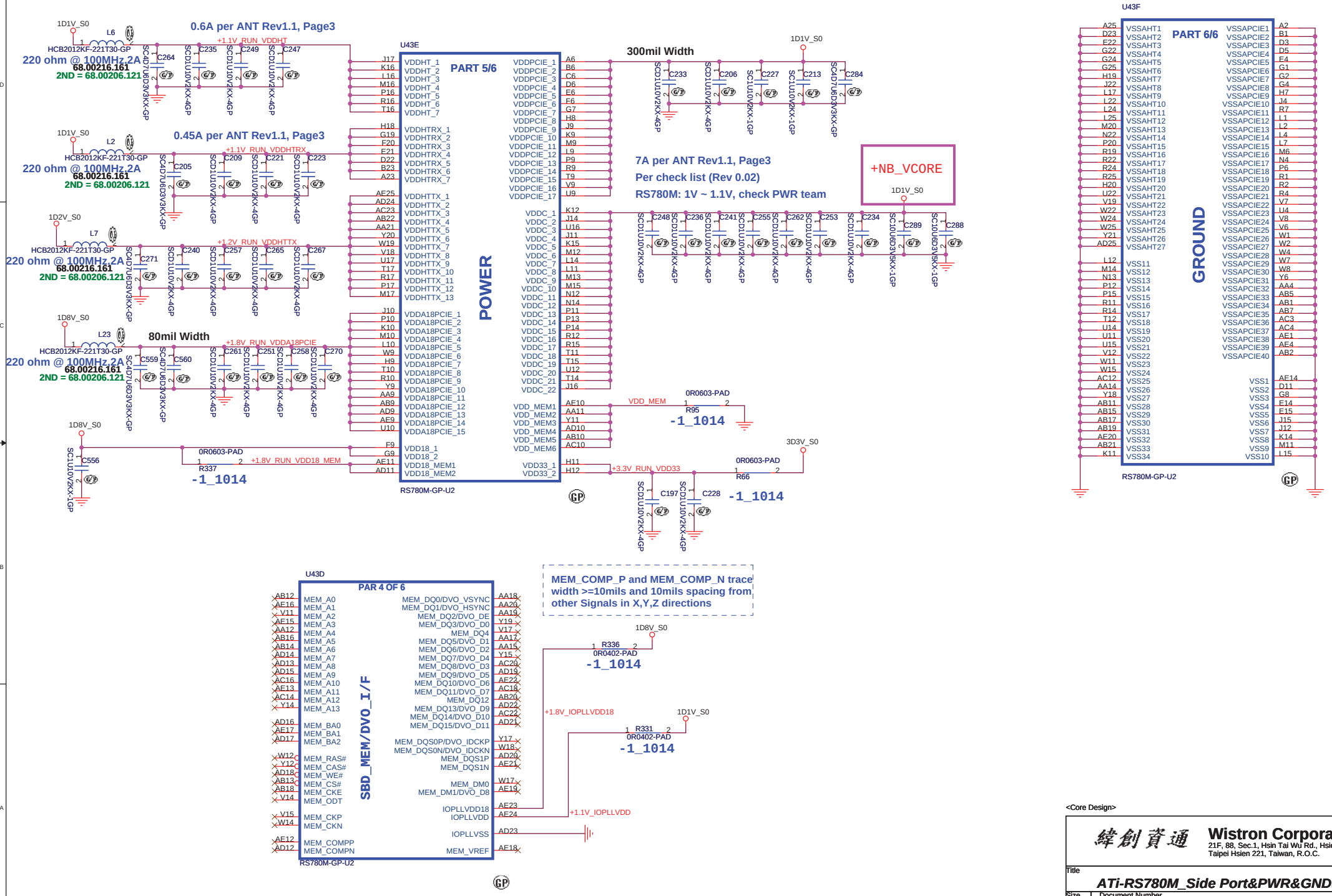
Title: ***DDR_DAMPING & TERMINATION***

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 10 of 55


U43A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
Placement: close RS780
U43B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
Place < 100mils from pin AC8 and AB8
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
MINICARD
LAN
MINICARD TV
NEW CARD
A-LINK
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M_HT LINK&PCIe(1/3)
Size A3
Document Number Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 11 of 55


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
U43C
PART 3 OF 6
RS780M-GP-U2
Close to NB ball < 1 inch trace
SD_0902
SD_0827
ENABLE External CLK GEN
SB
DIS
3.System Sensor, Put between CPU and NB.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS780M_LVDS&CRT_(2/4)
Big Bear 2A
Monday, October 27, 2008

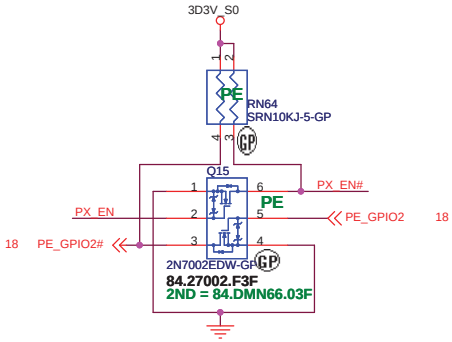


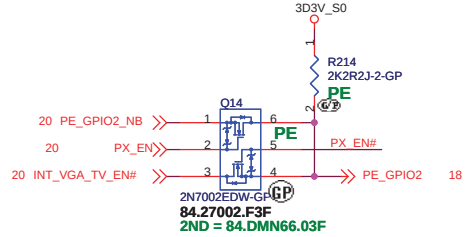
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_Side Port&PWR&GND(3/3)

Size: A3 | Document Number: Big Bear 2A | Rev: SA

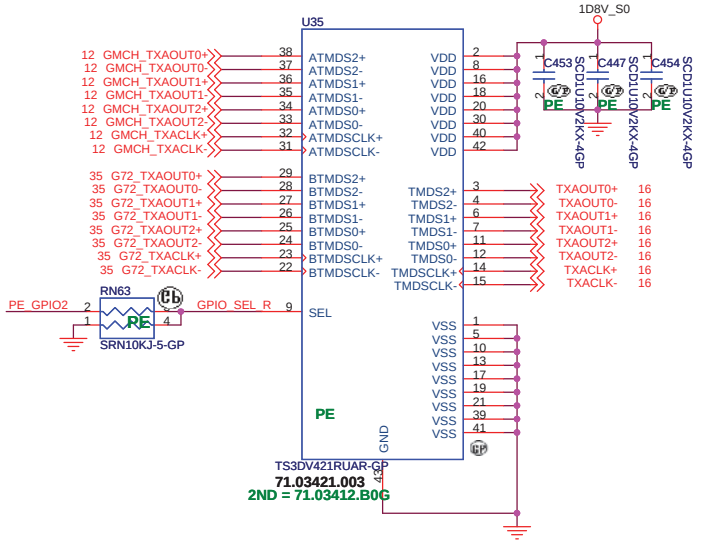
Date: Monday, October 27, 2008 | Sheet 13 of 55

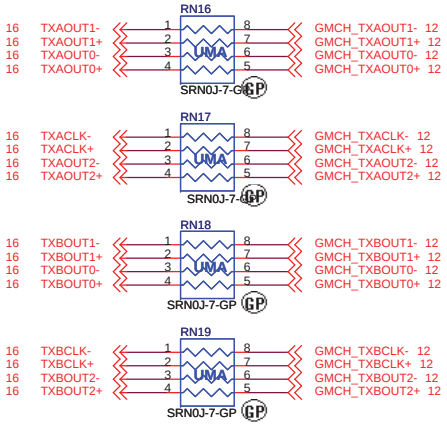


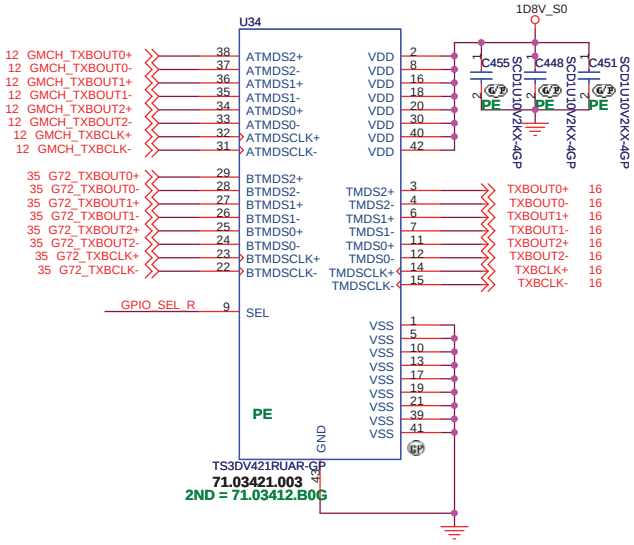


FUNCTION TABLE

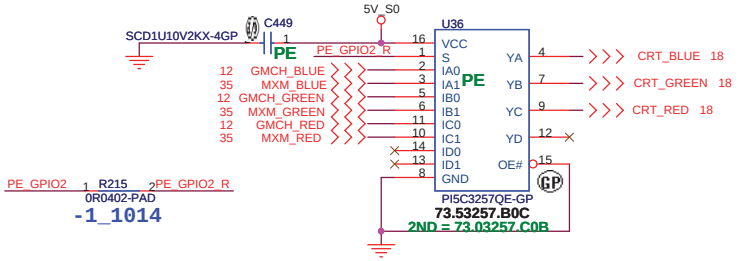
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

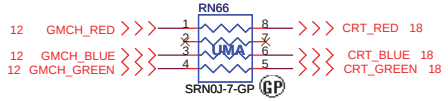






$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SWITCH**

Size: A3 | Document Number: **Big Bear 2A** | Rev: SB

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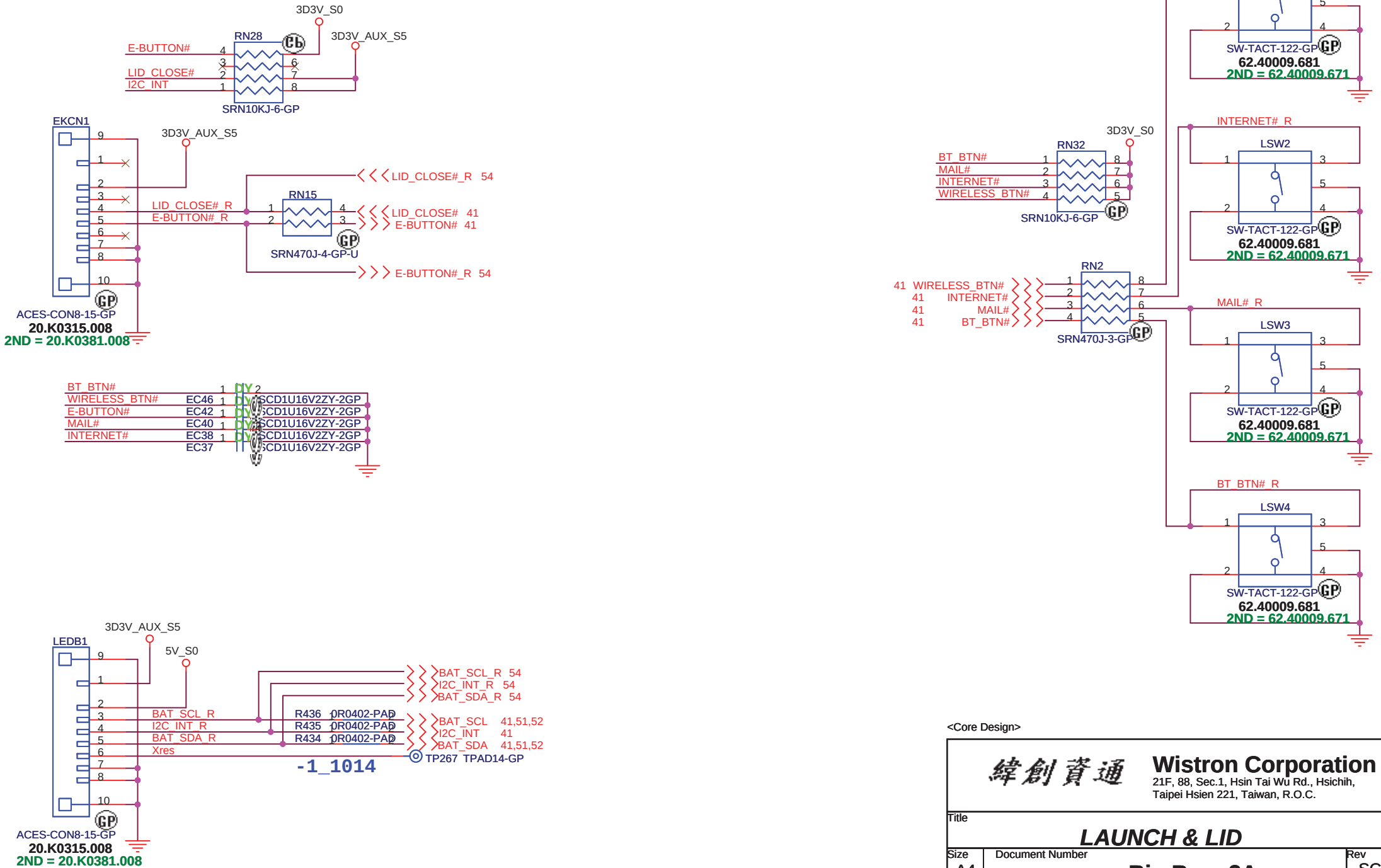
LAUNCH



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAUNCH & LID**

Size	Document Number	Rev
A4	Big Bear 2A	SC

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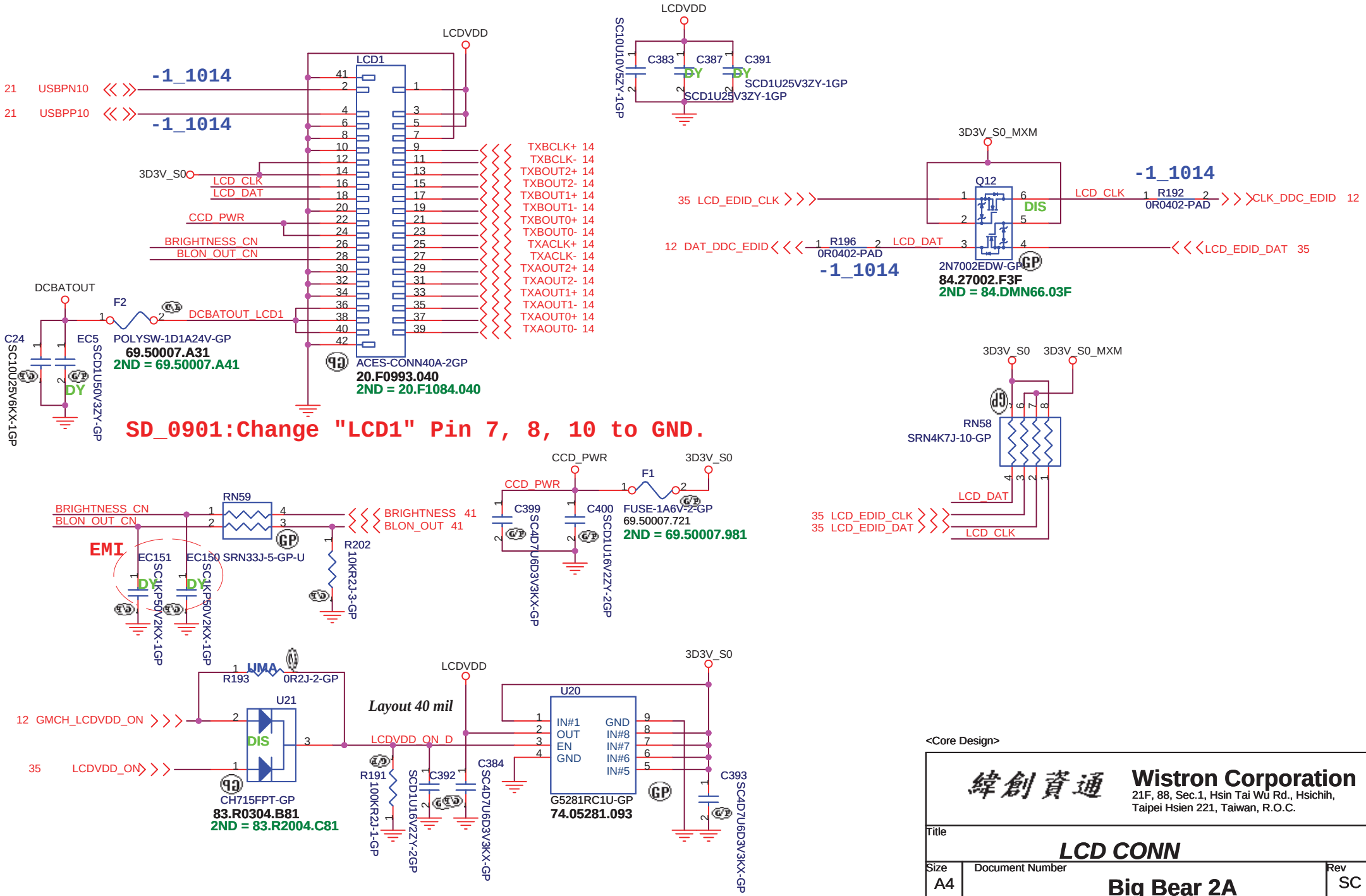
LCD/INVERTER/CCD CONN



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LCD CONN***

Size	Document Number	Rev
A4	**Big Bear 2A**	SC

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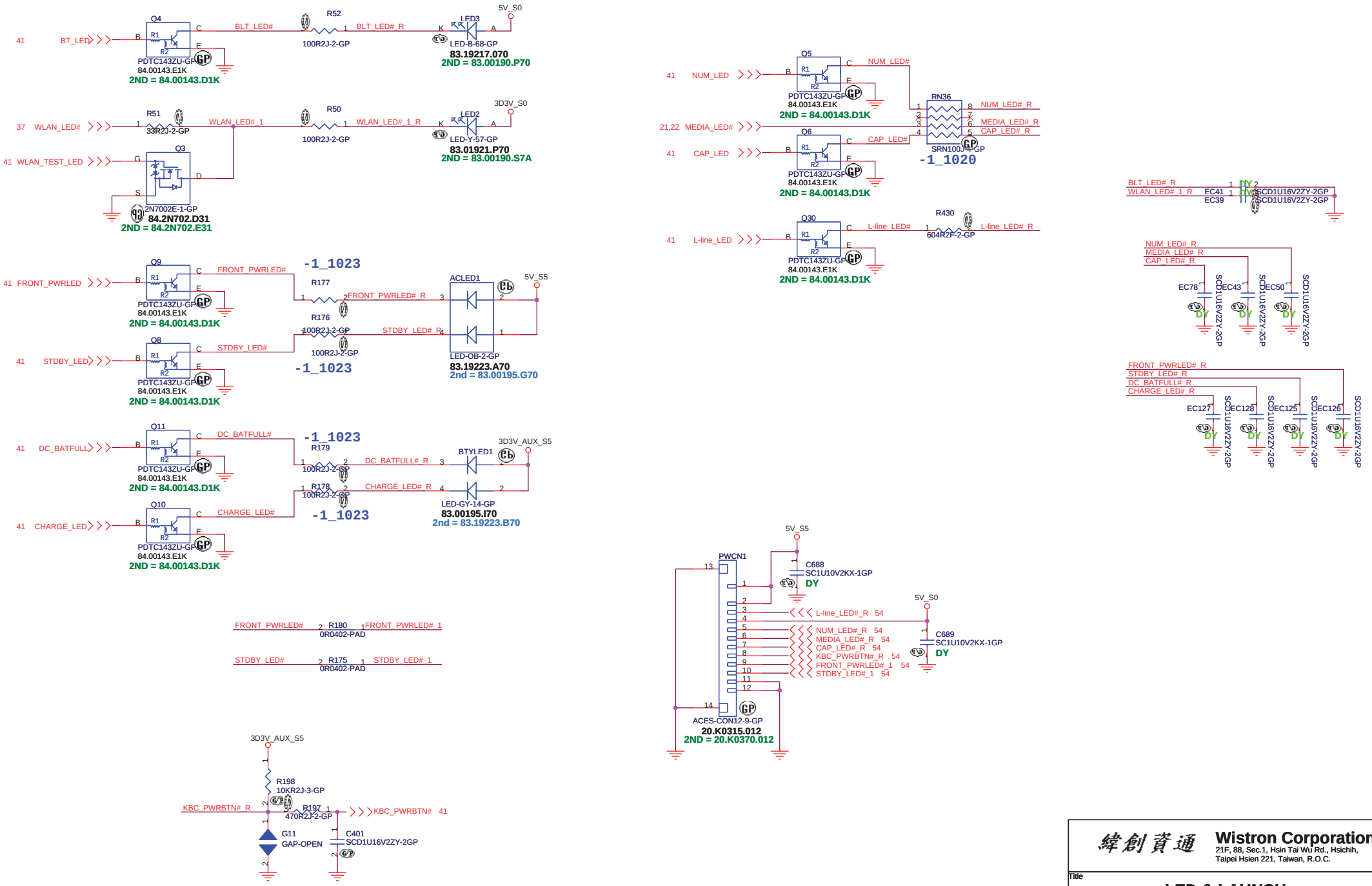
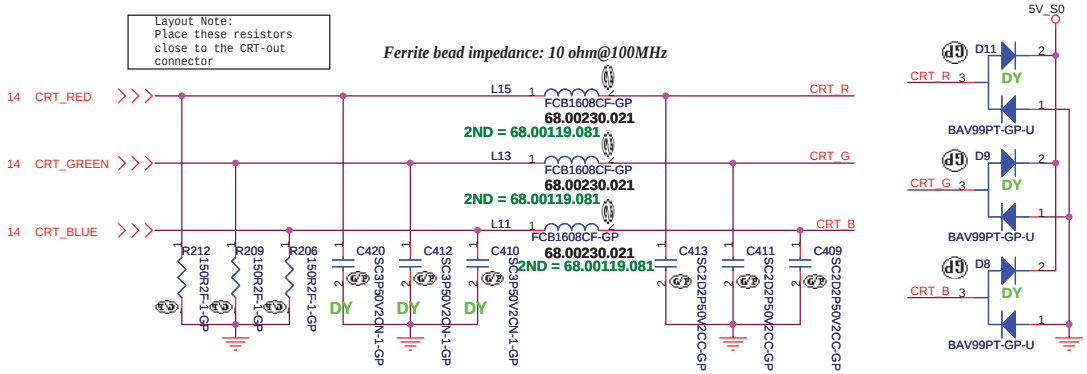
LED

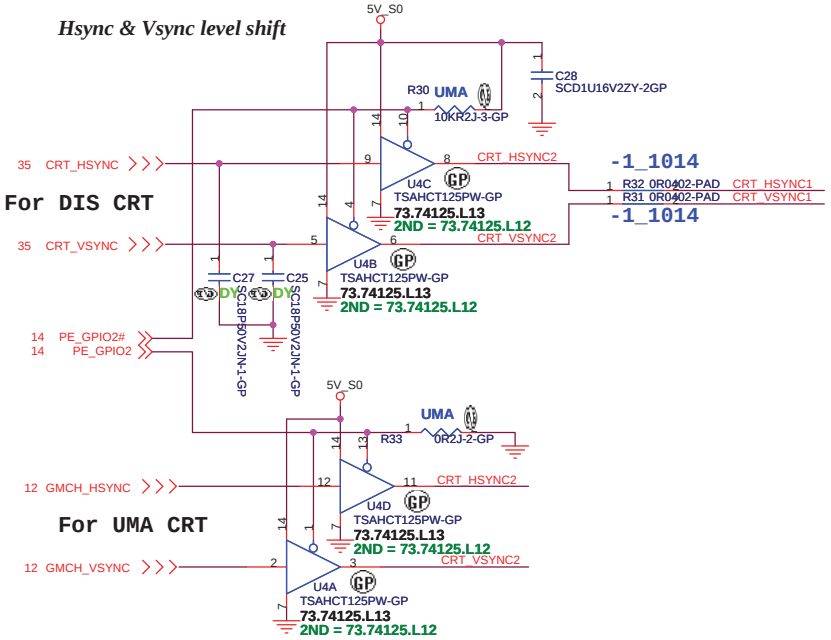


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***LED & LAUNCH***		
Size A3	Document Number **Big Bear 2A**		Rev SC
Date: Monday, October 27, 2008		Sheet 17 of 55	

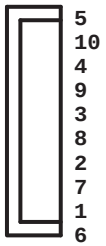


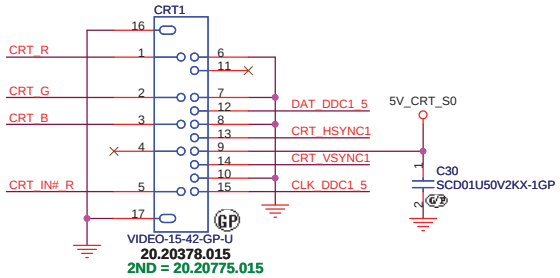
Change C409; C411, C413 to 1.5pF (78.1R574.1FL) in UMA

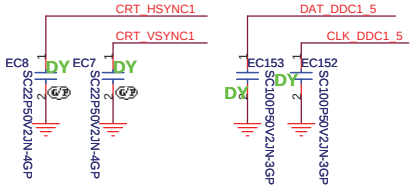
Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

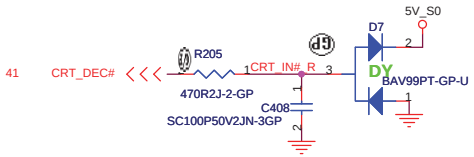


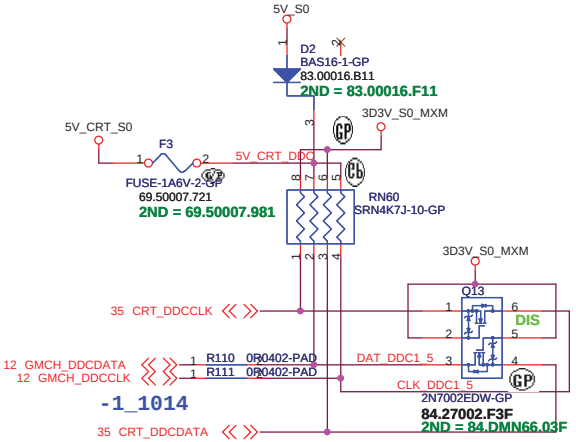
CRT I/F & CONNECTOR











<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
	Big Bear 2A	SA

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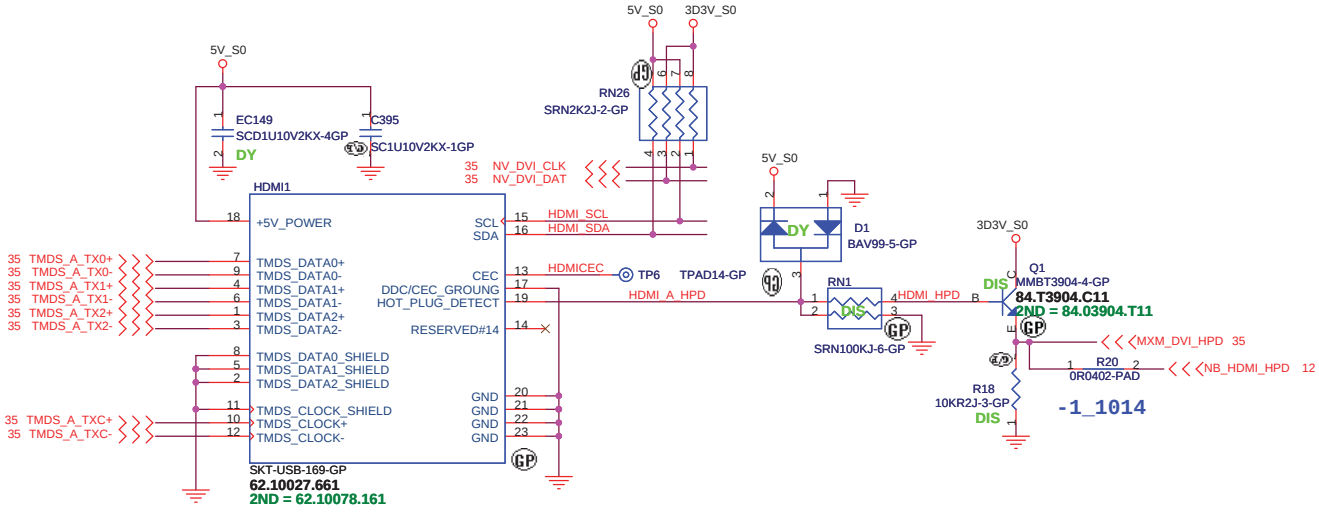
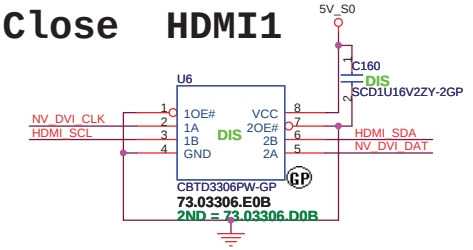
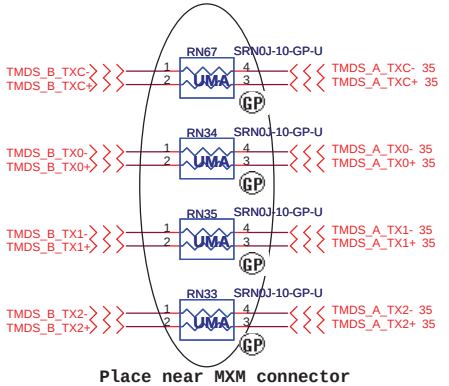
HDMI SM BUS LEVEL shifter

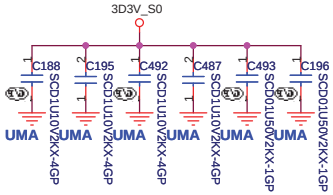
Close HDMI1

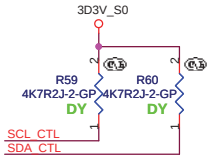


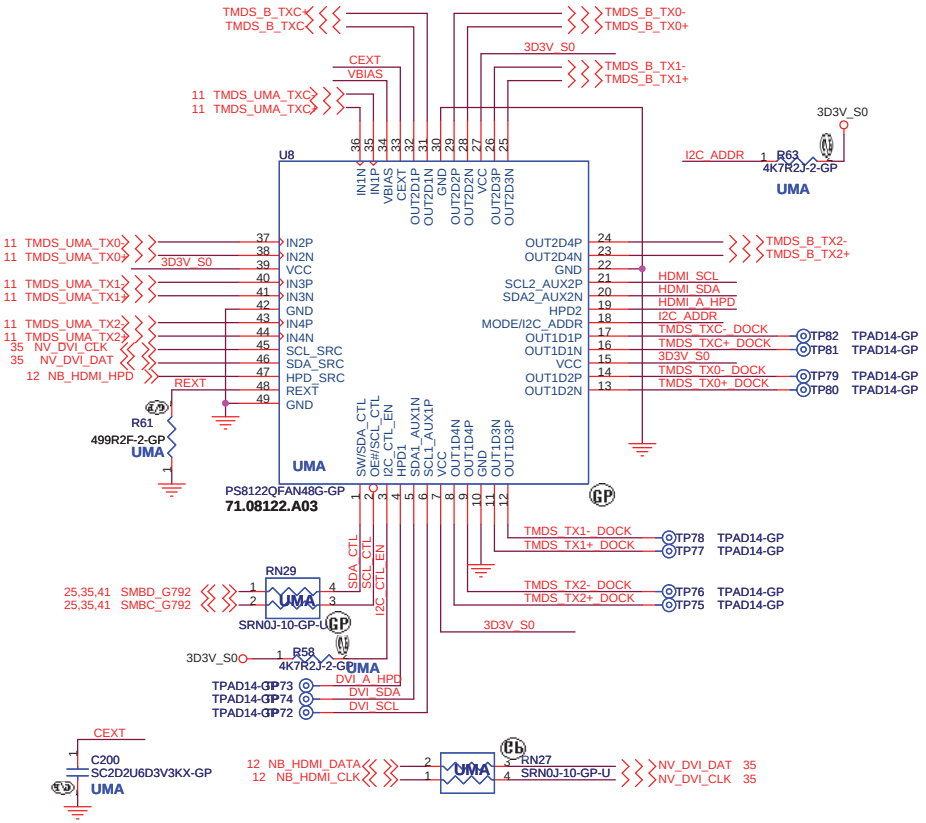




Place near MXM connector







<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI CONNECTOR

Size	Document Number	Rev
A3	Big Bear 2A	SD

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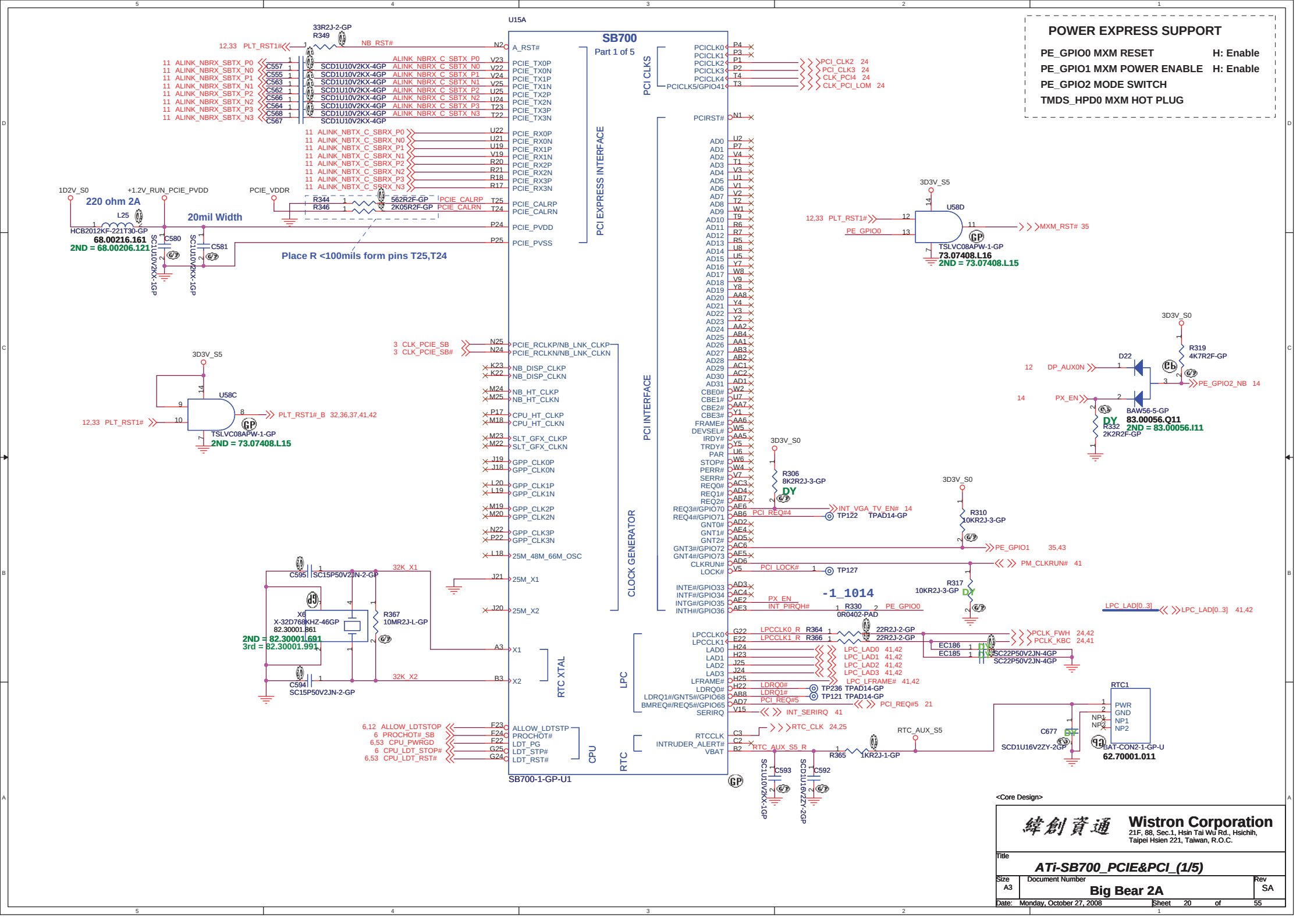
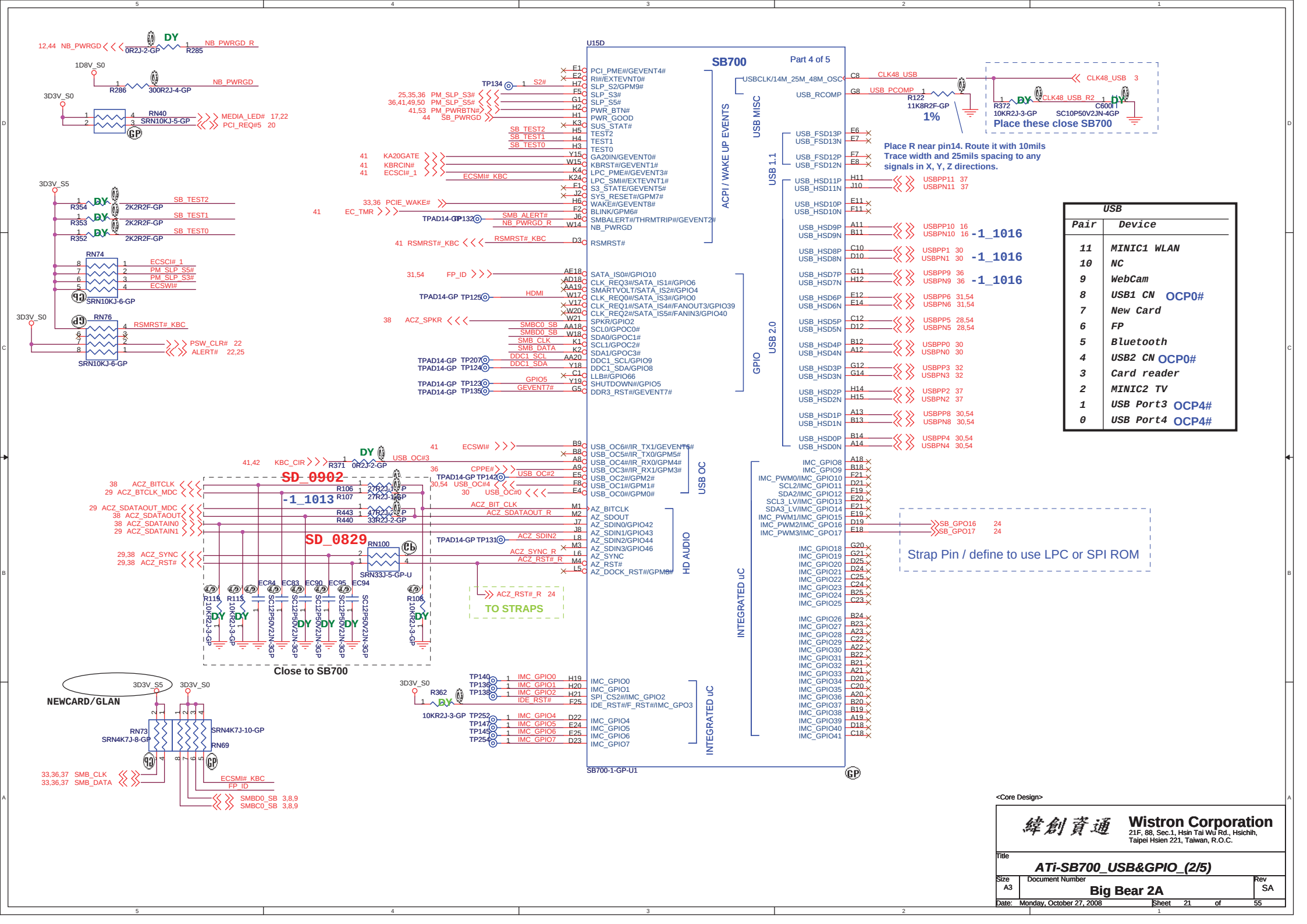
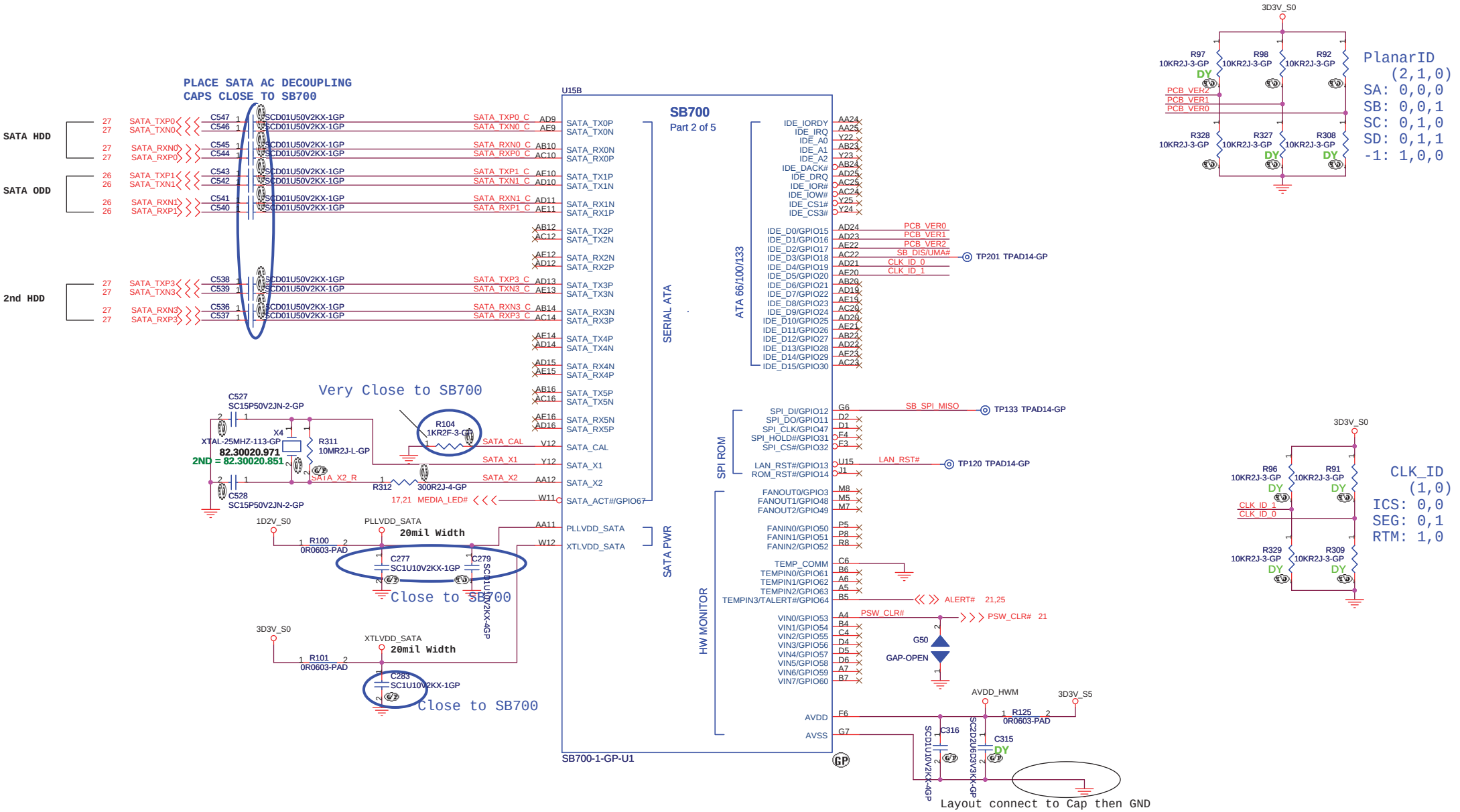

POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH
TMDS_HPD0 MXM HOT PLUG
U15A
SB700
Part 1 of 5
SB700-1-GP-U1
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
33R2J-2-GP
R349
NB_RST#
12,33 PLT_RST1#
ALINK_NBRX_SBTX_P0
ALINK_NBRX_SBTX_N0
ALINK_NBRX_SBTX_P1
ALINK_NBRX_SBTX_N1
ALINK_NBRX_SBTX_P2
ALINK_NBRX_SBTX_N2
ALINK_NBRX_SBTX_P3
ALINK_NBRX_SBTX_N3
SCD1U10V2KX-4GP
ALINK_NBTX_C_SBRX_P0
ALINK_NBTX_C_SBRX_N0
ALINK_NBTX_C_SBRX_P1
ALINK_NBTX_C_SBRX_N1
ALINK_NBTX_C_SBRX_P2
ALINK_NBTX_C_SBRX_N2
ALINK_NBTX_C_SBRX_P3
ALINK_NBTX_C_SBRX_N3
1D2V_S0
+1.2V_RUN_PCIE_PVDD
PCIE_VDDR
220 ohm 2A
L25
HCB2012KF-221T30-GP
68.00216.161
2ND = 68.00206.121
20mil Width
C580
C581
SC1U10V2KX-1GP
R344
562R2F-GP
R346
2K05R2F-GP
PCIE_CALRP
PCIE_CALRN
Place R <100mils form pins T25,T24
3D3V_S5
U58C
TSLVC08APW-1GP
2ND = 73.07408.L15
3 CLK_PCIE_SB
3 CLK_PCIE_SB#
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
25M_48M_66M_OSC
25M_X1
25M_X2
32K_X1
32K_X2
C595
SC15P50V2JN-2-GP
X6
X-32D768KHZ-46GP
82.30001.861
2ND = 82.30001.691
3rd = 82.30001.991
R367
10MR2J-L-GP
C594
SC15P50V2JN-2-GP
6,12 ALLOW_LDTSTOP
6 PROCHOT#_SB
6,53 CPU_PWRGD
6 CPU_LDT_STOP#
6,53 CPU_LDT_RST#
ALLOW_LDTSTP
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5/GPIO41
PCI_CLK2 24
PCI_CLK3 24
CLK_PCI4 24
CLK_PCI_LOM 24
PCIRST#
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_CALRP
PCIE_CALRN
PCIE_PVDD
PCIE_PVSS
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
CBE0#
CBE1#
CBE2#
CBE3#
FRAME#
DEVSEL#
IRDY#
TRDY#
PAR
STOP#
PERR#
SERR#
REQ0#
REQ1#
REQ2#
REQ3#/GPIO70
REQ4#/GPIO71
GNT0#
GNT1#
GNT2#
GNT3#/GPIO72
GNT4#/GPIO73
CLKRUN#
LOCK#
INTE#/GPIO33
INTF#/GPIO34
INTG#/GPIO35
INTH#/GPIO36
LPCCLK0
LPCCLK1
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ0#
LDRQ1#/GNT5#/GPIO68
BMREQ#/REQ5#/GPIO65
SERIRQ
RTCCLK
INTRUDER_ALERT#
VBAT
3D3V_S0
R306
8K2R2J-3-GP
DY
INT_VGA_TV_EN# 14
TP122
TPAD14-GP
PCI_REQ#4
R310
10KR2J-3-GP
PE_GPIO1 35,43
PM_CLKRUN# 41
PCI_LOCK#
TP127
R317
10KR2J-3-GP
-1_1014
PX_EN
INT_PIRQH#
R330
0R0402-PAD
PE_GPIO0
LPC_LAD[0..3]
LPC_LAD[0..3] 41,42
LPCCLK0_R
LPCCLK1_R
R364
R366
22R2J-2-GP
PCLK_FWH 24,42
PCLK_KBC 24,41
EC186
EC185
SC22P50V2JN-4GP
LPC_LAD0 41,42
LPC_LAD1 41,42
LPC_LAD2 41,42
LPC_LAD3 41,42
LPC_LFRAME# 41,42
LDRQ0#
LDRQ1#
TP236 TPAD14-GP
TP121 TPAD14-GP
PCI_REQ#5
PCI_REQ#5 21
INT_SERIRQ 41
RTC_CLK 24,25
RTC_AUX_S5
RTC_AUX_S5_R
R365
1KR2J-1-GP
C593
C592
SC1U10V2KX-1GP
SCD1U16V2ZY-2GP
C677
SCD1U16V2ZY-2GP
RTC1
BAT-CON2-1-GP-U
62.70001.011
PWR
GND
NP1
NP2
U58D
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
12,33 PLT_RST1#
PE_GPIO0
MXM_RST# 35
D22
BAW56-5-GP
DY
83.00056.Q11
2ND = 83.00056.I11
R319
4K7R2F-GP
R332
2K2R2F-GP
DP_AUX0N
PE_GPIO2_NB 14
PX_EN
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_PCIE&PCI_(1/5)
Size A3
Document Number
Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 20 of 55


SB700
Part 4 of 5
U15D
SB700-1-GP-U1
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
CLK48_USB
USB_PCOMP
R122
11K8R2F-GP
1%
R372
10KR2J-3-GP
CLK48_USB_R2
C600
SC10P50V2JN-4GP
Place these close SB700
Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.
-1_1016
-1_1013
SD_0902
SD_0829
Close to SB700
TO STRAPS
Strap Pin / define to use LPC or SPI ROM
NEWCARD/GLAN
USB
Pair Device
11 MINIC1 WLAN
10 NC
9 WebCam
8 USB1 CN OCP0#
7 New Card
6 FP
5 Bluetooth
4 USB2 CN OCP0#
3 Card reader
2 MINIC2 TV
1 USB Port3 OCP4#
0 USB Port4 OCP4#
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_USB&GPIO_(2/5)
Size A3
Document Number
Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 21 of 55



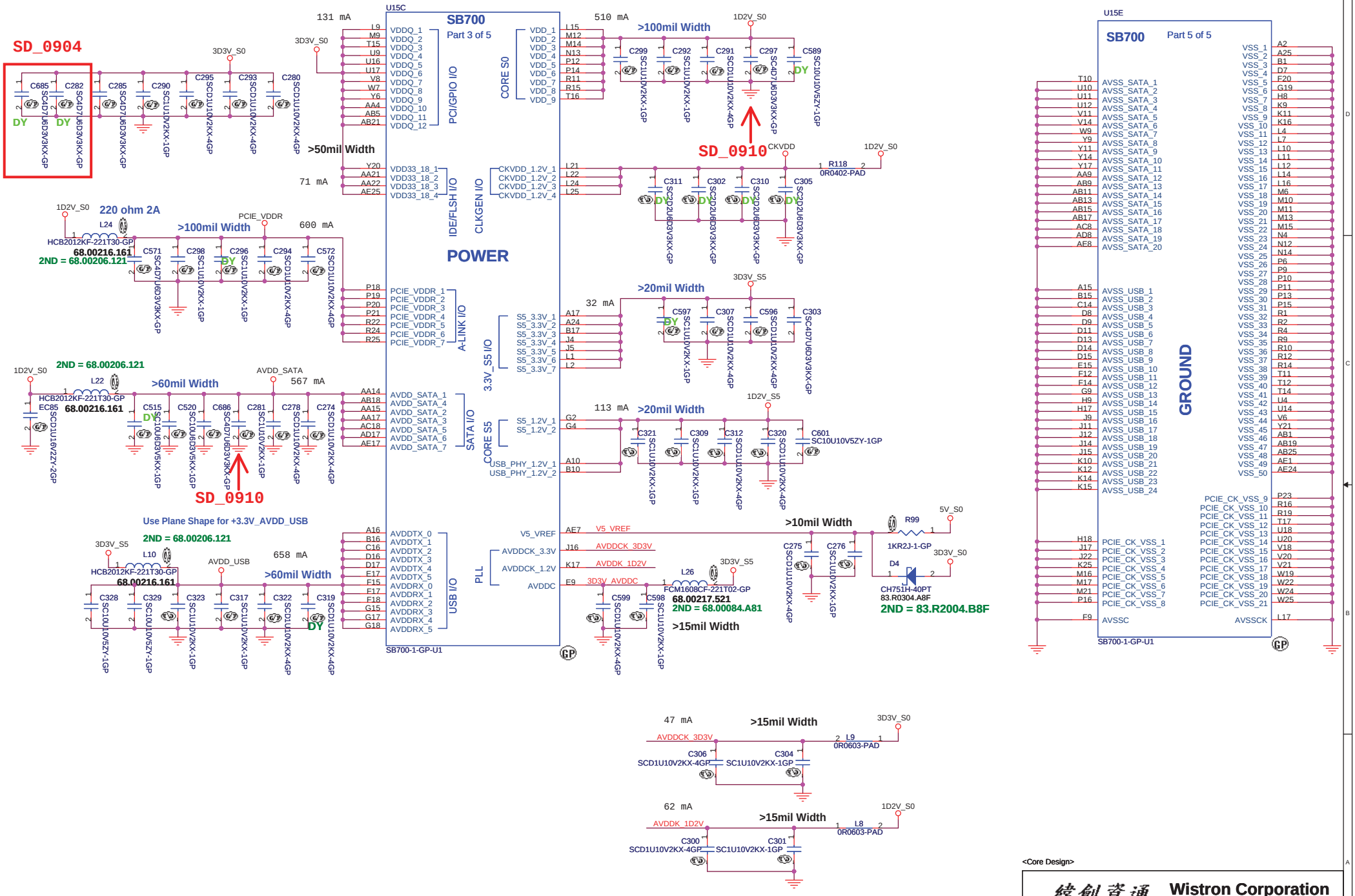
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_SATA-IDE_(3/5)

Size	Document Number	Rev
A3	Big Bear 2A	SB

Date: Monday, October 27, 2008 Sheet 22 of 55



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

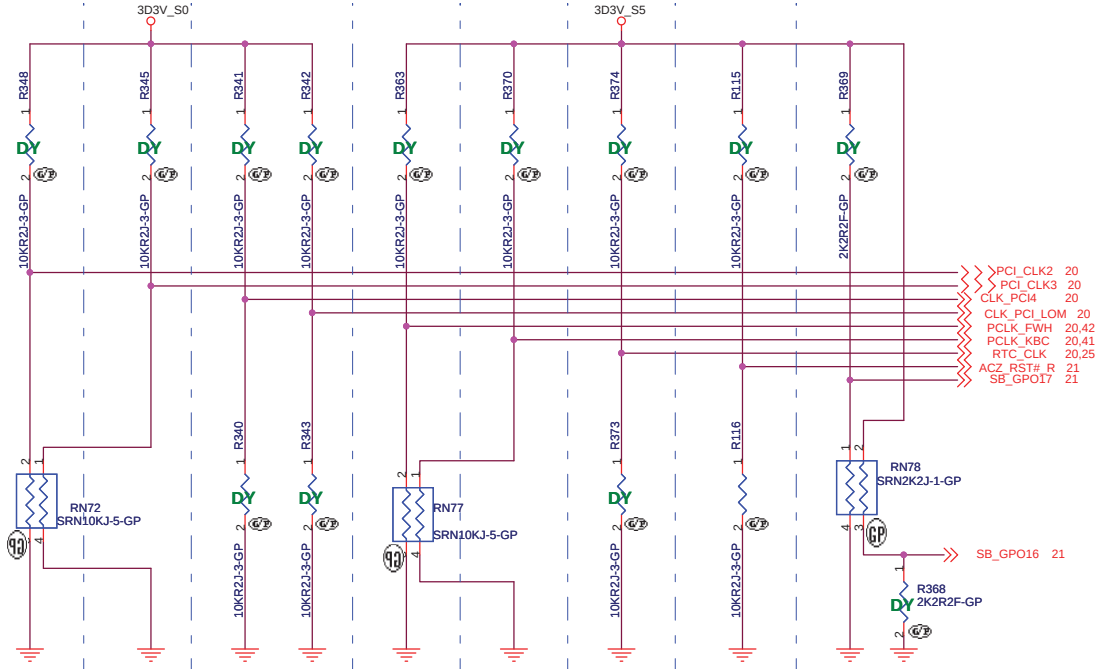
Title: ATi-SB700_POWER&GND_(4/5)

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 23 of 55

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

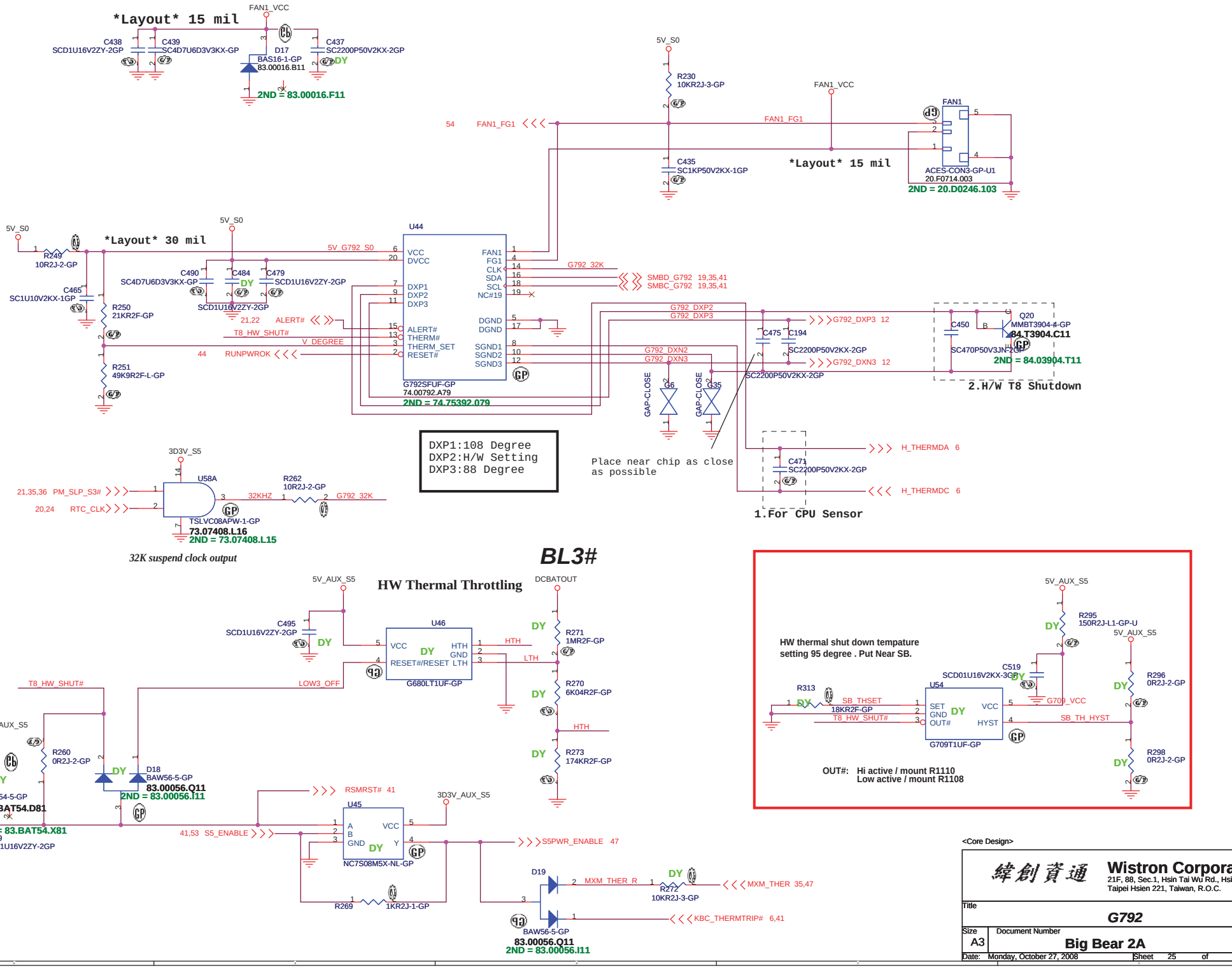
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 24 of 55



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G792

Size: A3 | Document Number: Big Bear 2A | Rev: SA

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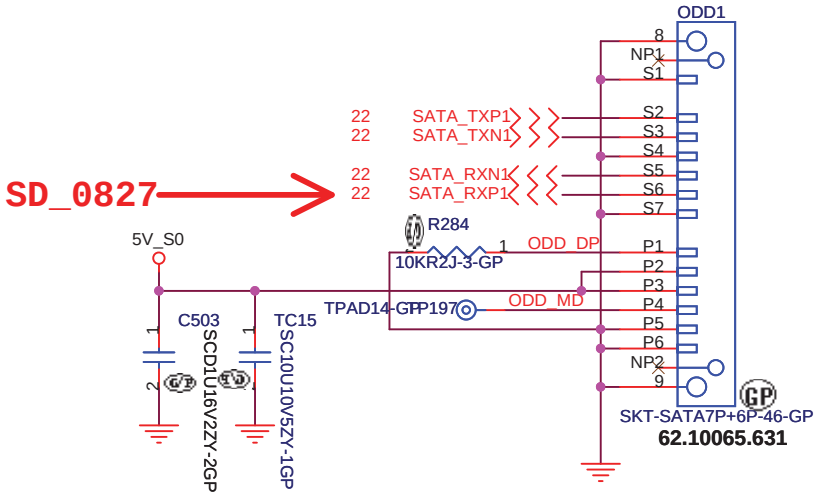
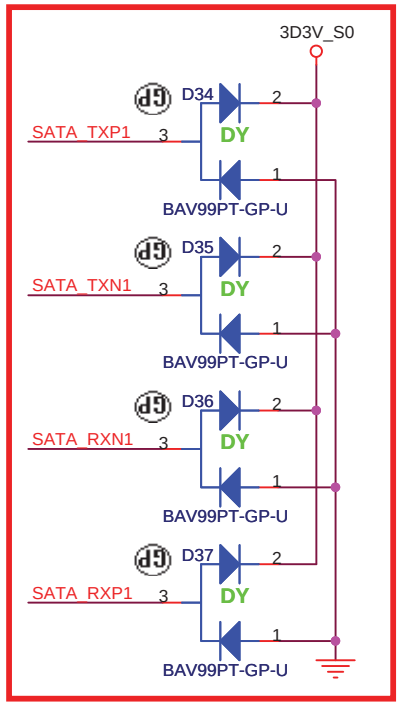
ODD Connector



SD_0828



<Core Design>

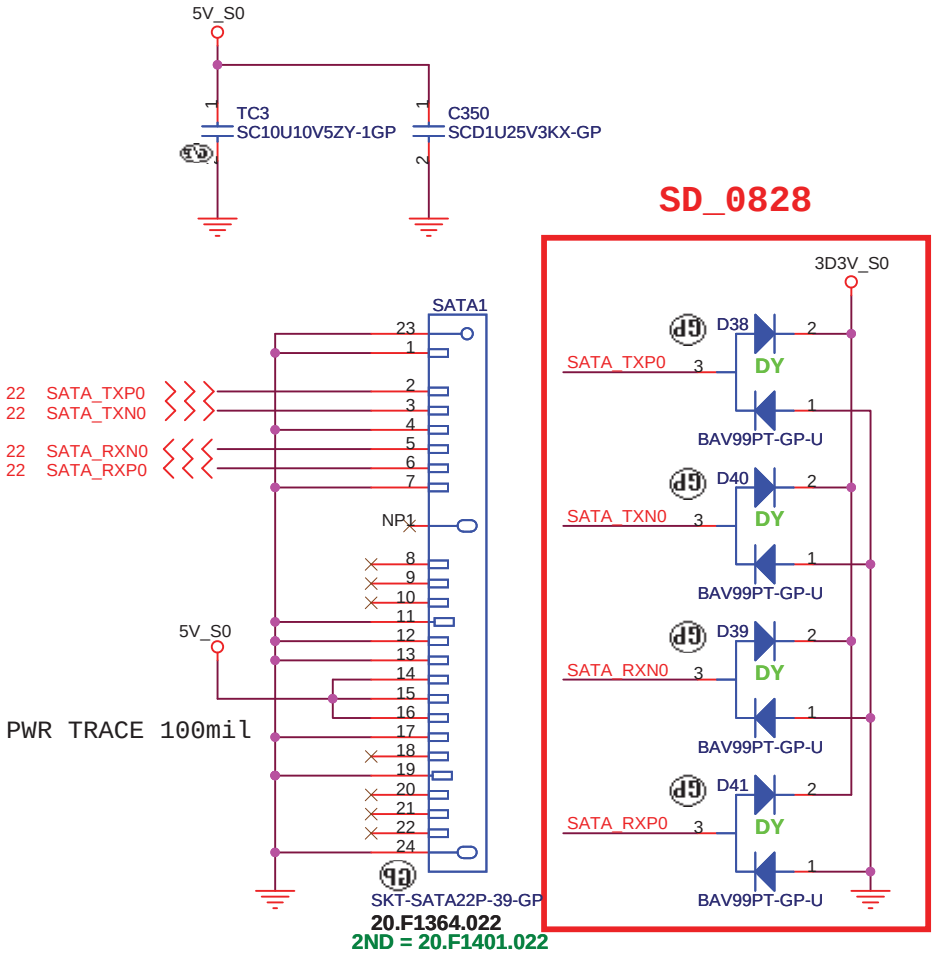
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CDROM

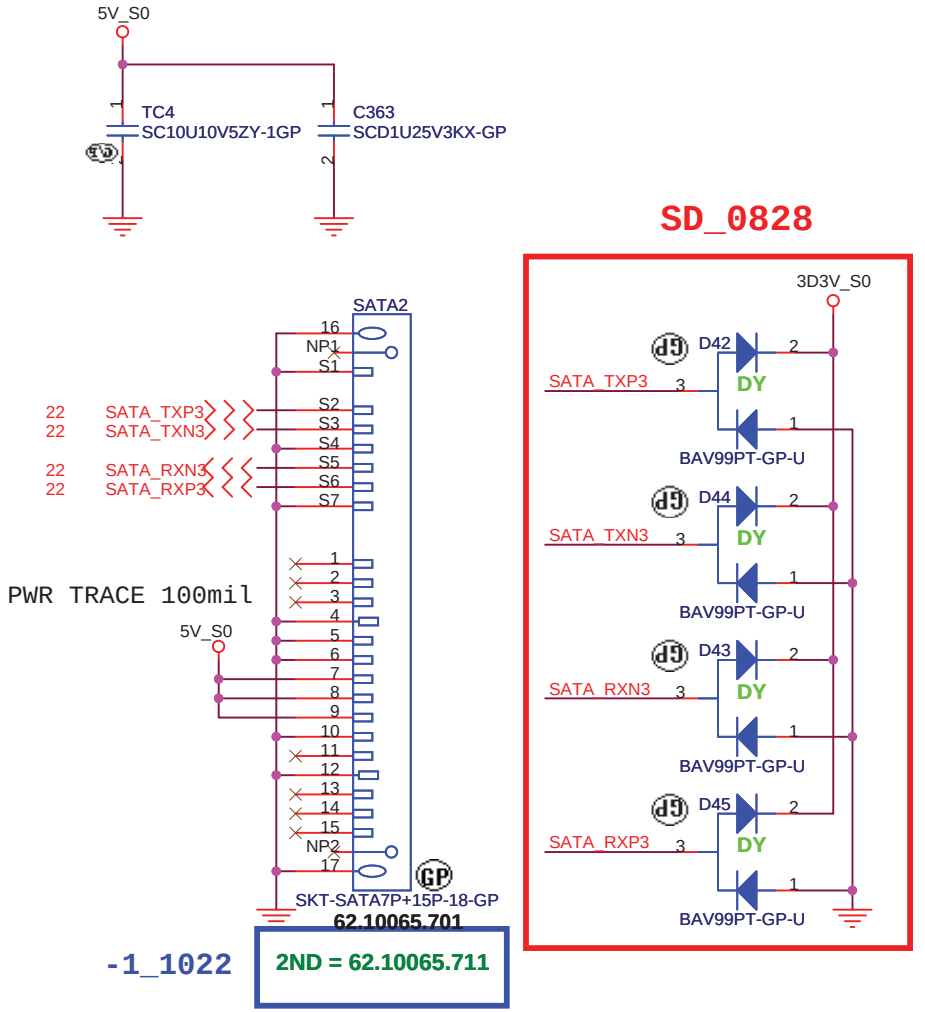
Size	Document Number	Rev
A4	Big Bear 2A	SD

Date: Monday, October 27, 2008 Sheet 26 of 55

SATA HDD Connector



2ND SATA HDD Connector

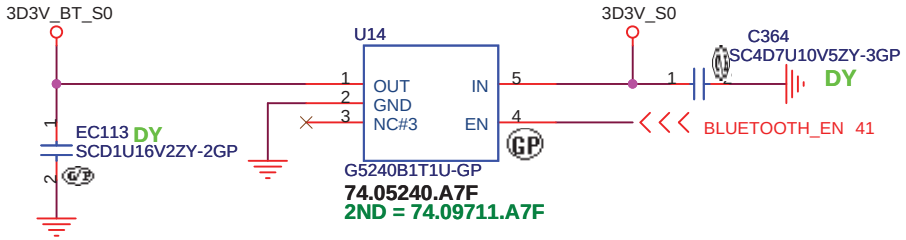


<Core Design>

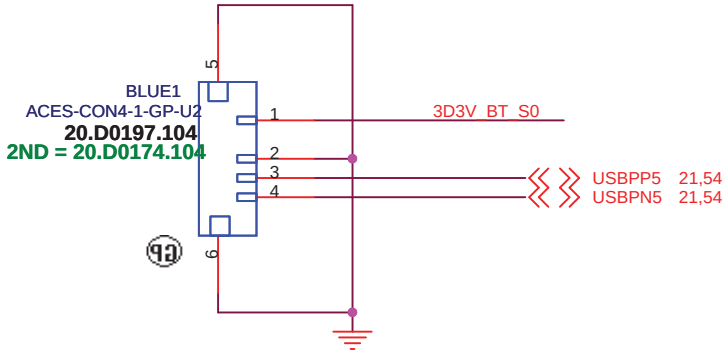
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD***		
Size: A4	Document Number: **Big Bear 2A**	Rev: SD
Date: Monday, October 27, 2008	Sheet 27 of 55	

BLUETOOTH MODULE



EC40 put near BLUE1 / all USB put one choke near connector by EMI request



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLUETOOTH

Size	Document Number	Rev
A4	Big Bear 2A	SA

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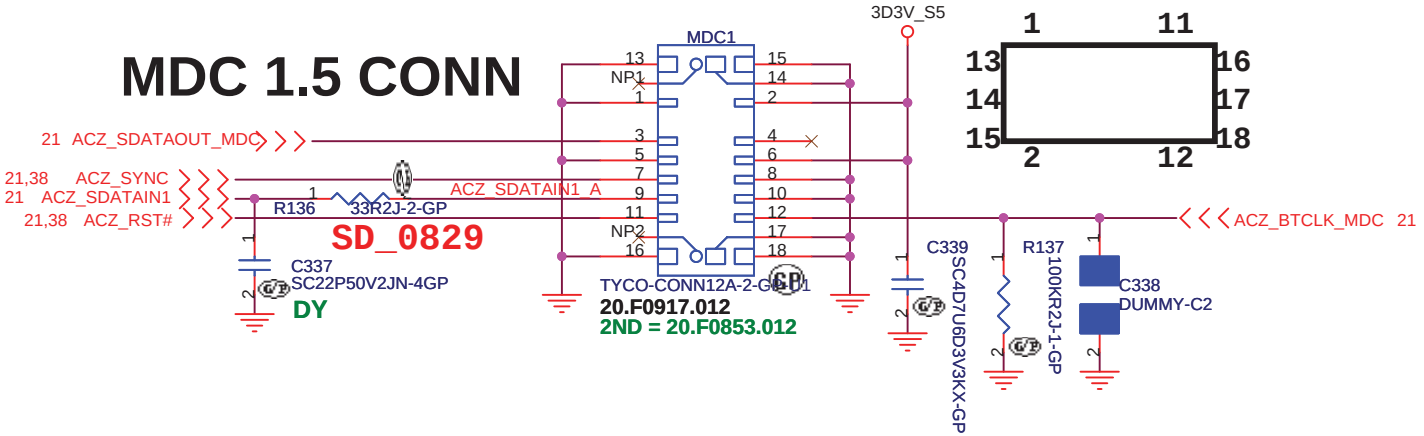
MDC 1.5 CONN



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MDC

Size	Document Number	Rev
A4	Big Bear 2A	SA

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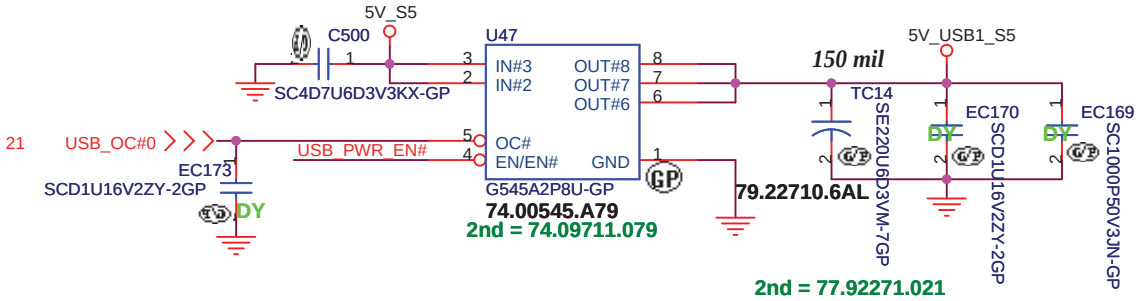

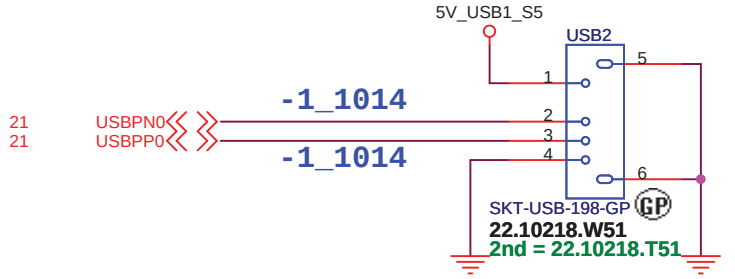

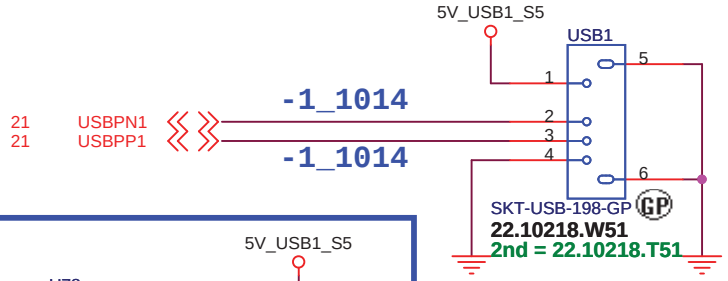

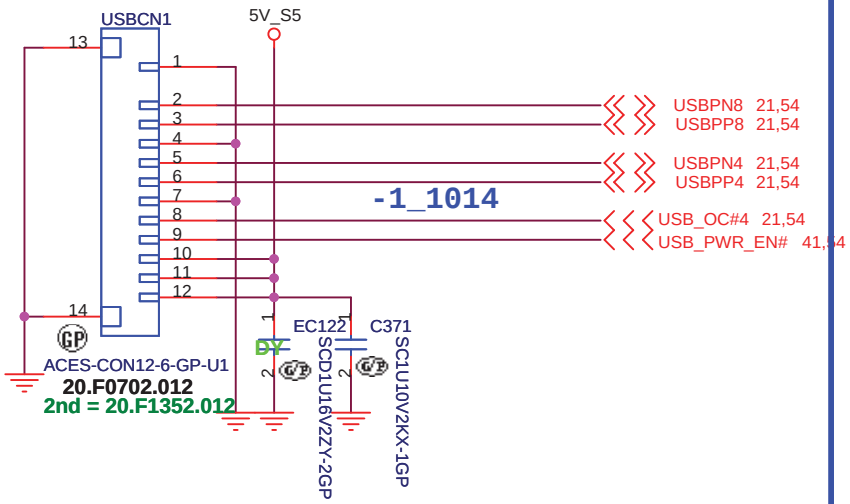

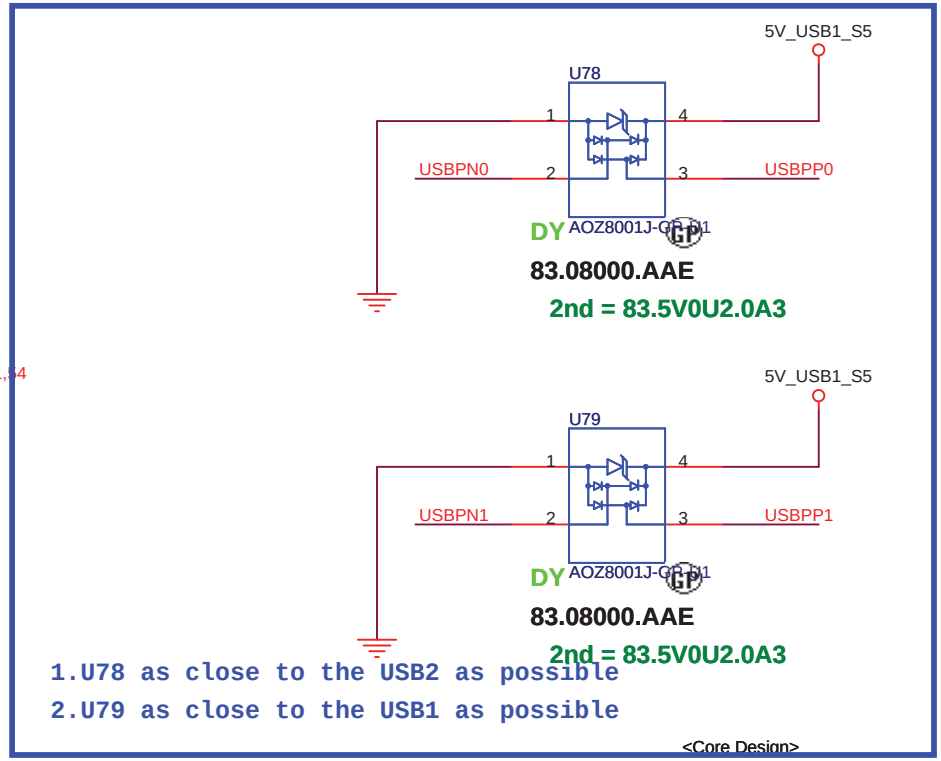

ESD Protection

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB

Size	Document Number	Rev
A4	Big Bear 2A	SB

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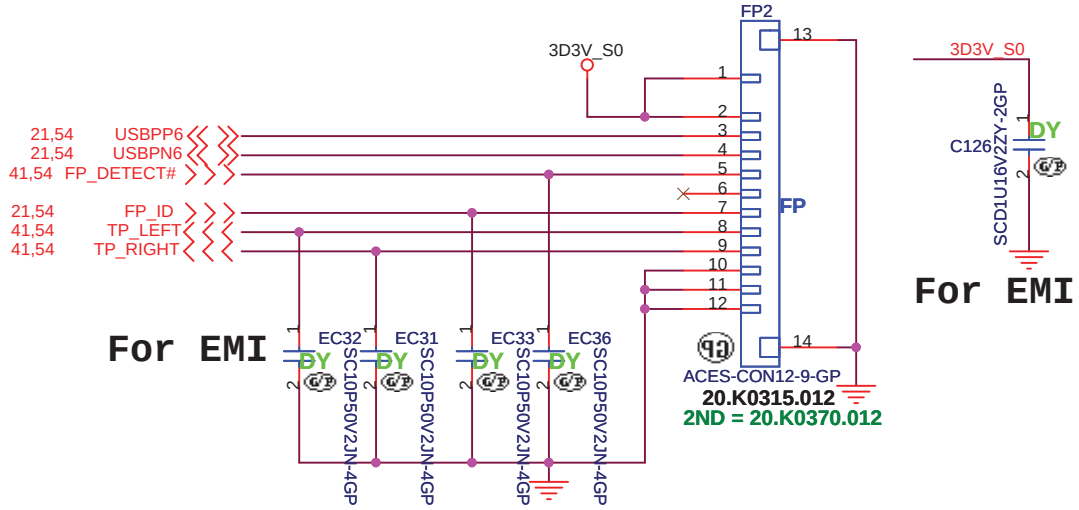
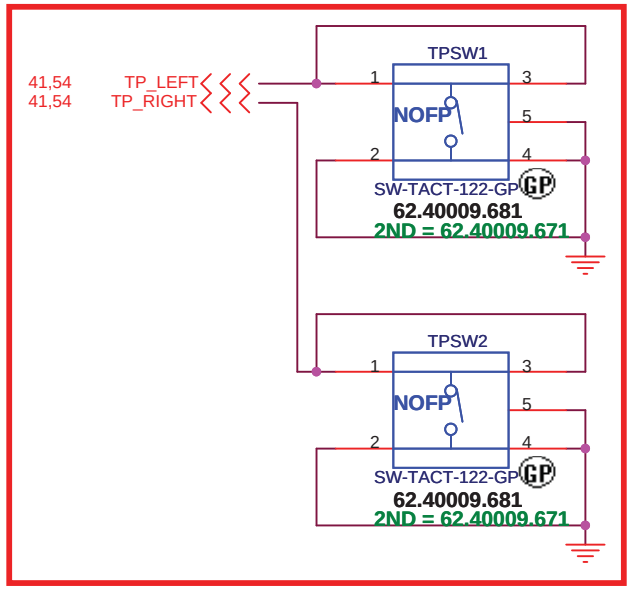
Finger printer



SD_0903



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Finger Printer*

Size	Document Number	Rev
A4	Big Bear 2A	SD

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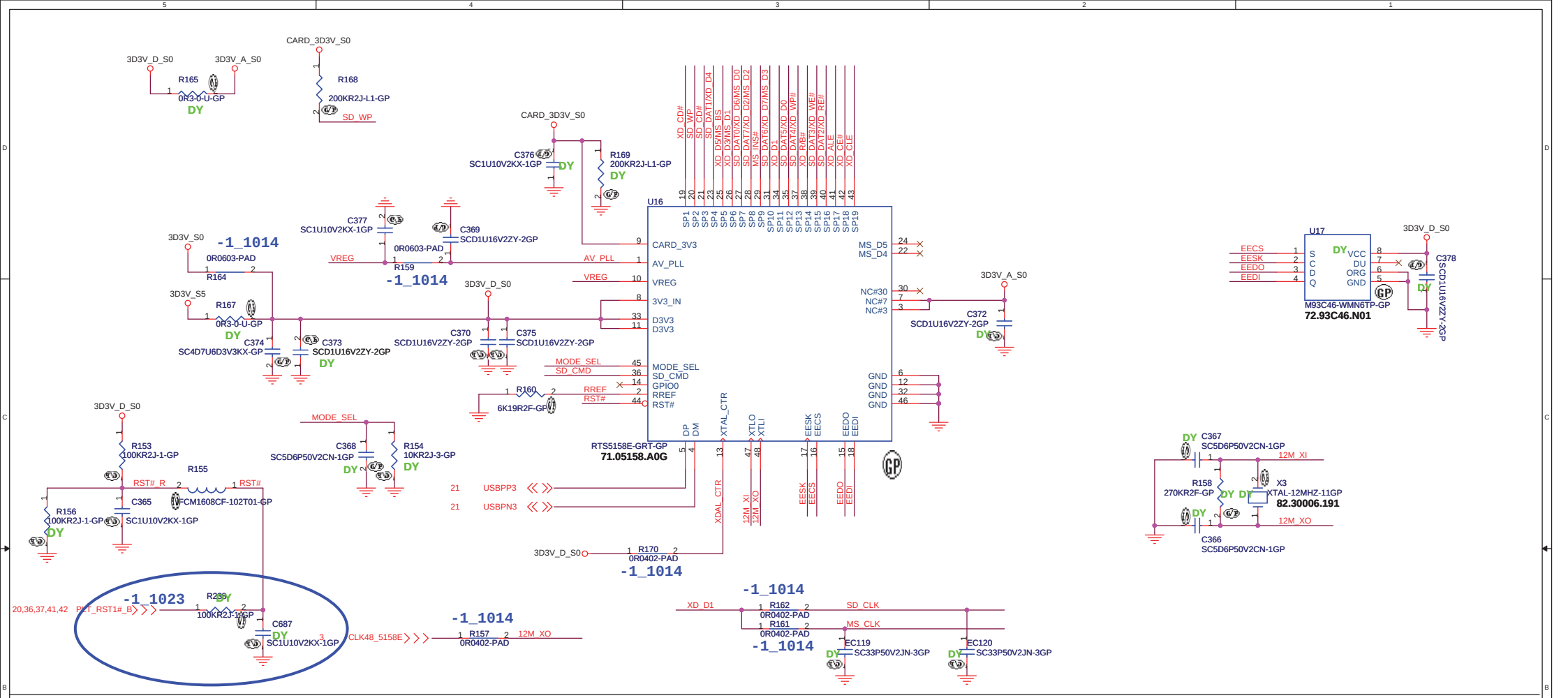
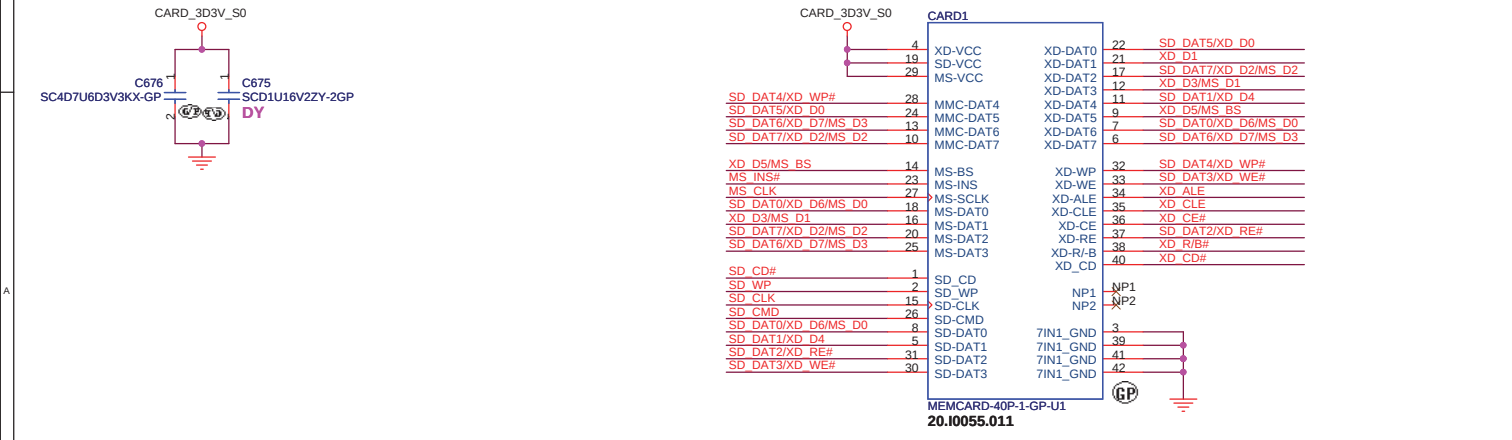


7 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)



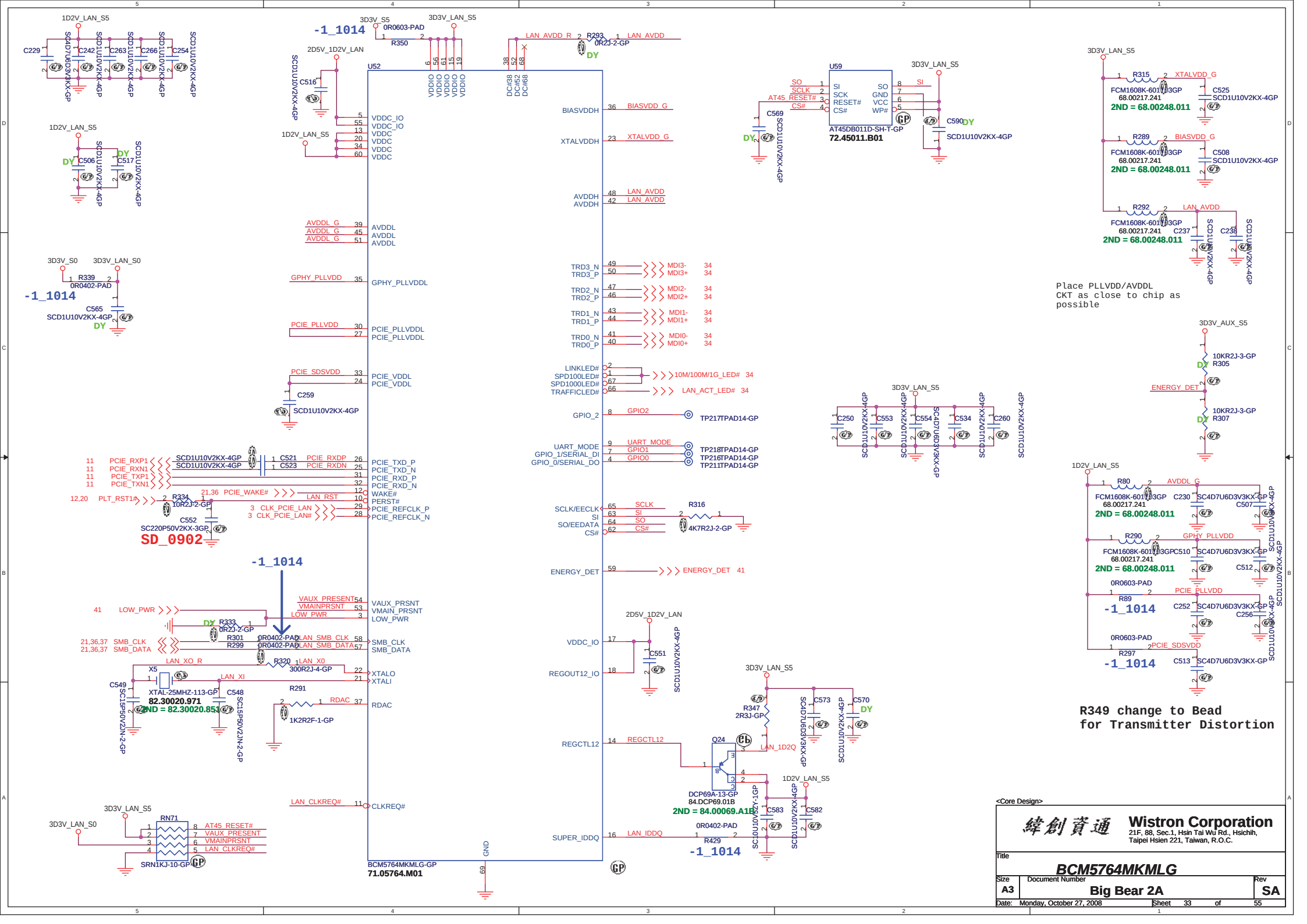
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

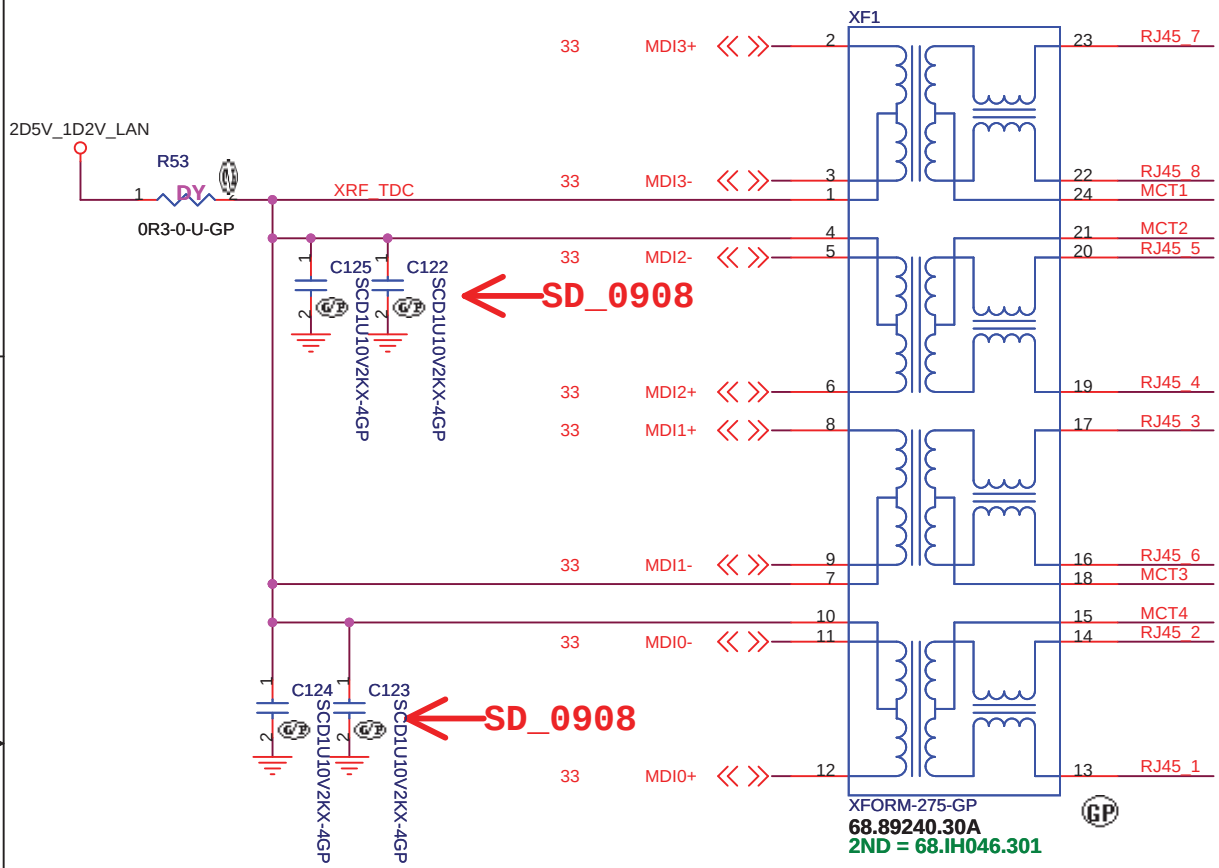
Title: *Card Reader Connector*

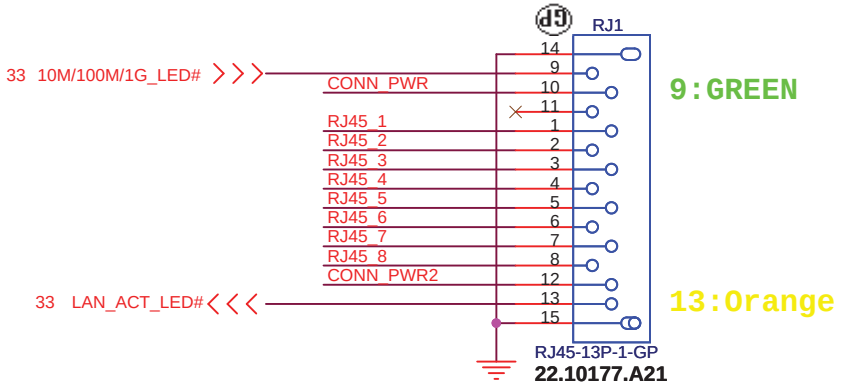
Size	Document Number	Rev
A3	Big Bear 2A	SD

Date: Monday, October 27, 2008 Sheet 32 of 55


BCM5764MKMLG-GP
71.05764.M01
U52
-1_1014
SD_0902
Place PLLVDD/AVDDL
CKT as close to chip as
possible
R349 change to Bead
for Transmitter Distortion
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5764MKMLG
Size A3
Document Number Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 33 of 55

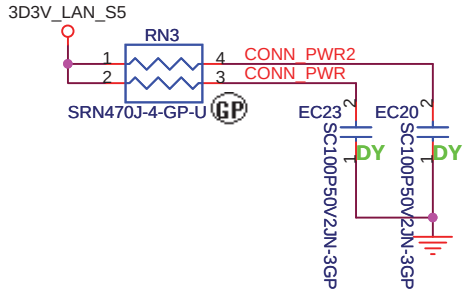
LAN Connector

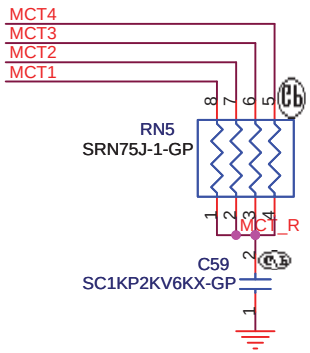




LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

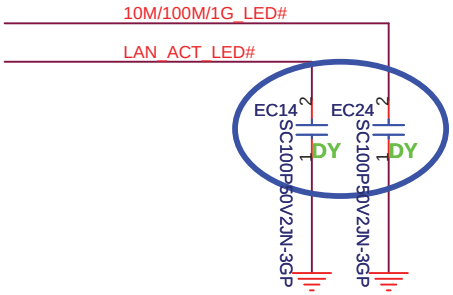
LAN Data: Yellow(B2), when LAN is transfering data.





1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

For EMI Near LAN1 CONN



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**

Size	Document Number	Rev
A4	Big Bear 2A	SB

Date: Monday, October 27, 2008 Sheet 34 of 55

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

-1_1022

-1_1016

-1_1014

SD_0902

MXM1 DIS
SPD-CONN230A-4-GP-U3
20.F1031.230
2ND = 20.F1384.230

BAS16-1-GP
83.00016.B11
2ND = 83.00016.F11

Q31
2N7002EDW-GP
84.27002.F3F
2ND = 84.DMN66.03F

CH715FPT-GP
83.R0304.B81
2ND = 83.R2004.C8

79.10712.L02
2ND = 79.10712.6JL

<Core Design>

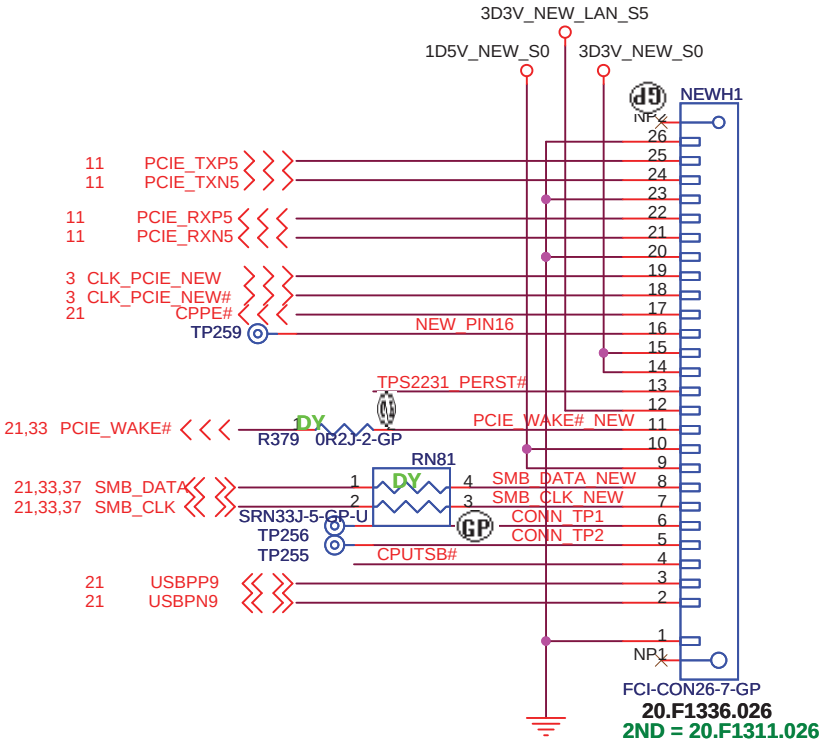
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

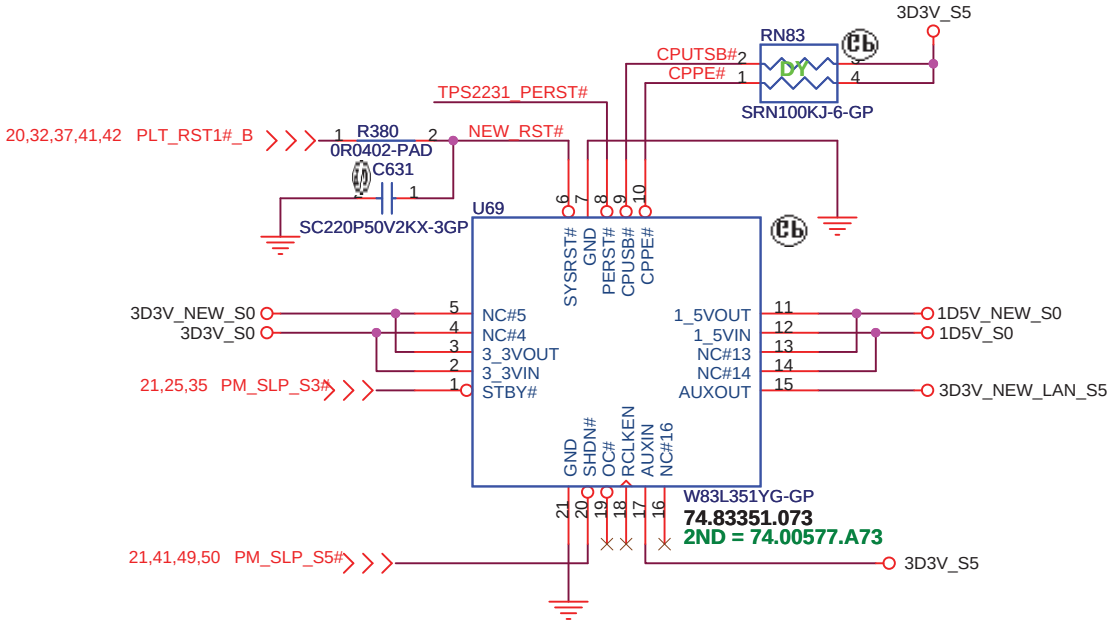
Title: Graphic MXM CONN

Size: A3 | Document Number: Big Bear 2A | Rev: SD

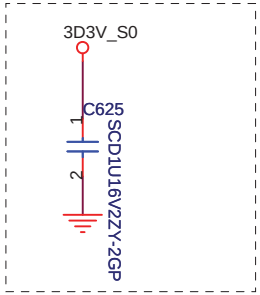
Date: Monday, October 27, 2008 | Sheet 35 of 55

NEWCARD Connector

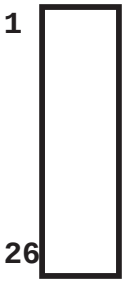


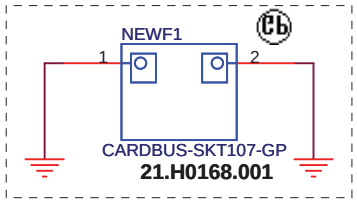


Place them Near to Chip

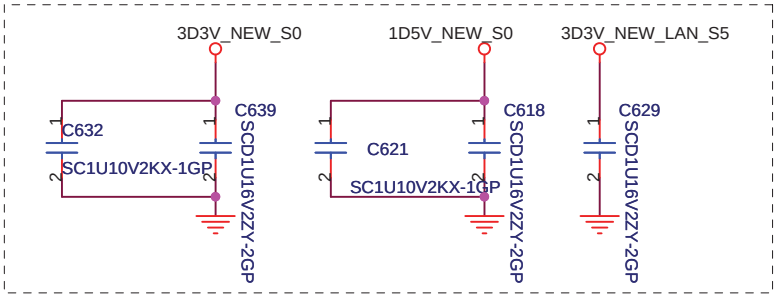


TOP VIEW





Place them Near to Connector



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **NEW CARD**

Size	Document Number	Rev
A4	Big Bear 2A	SC

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Mini Card Connector(TV) UPPER SLOT
Mini Card Connector(WLAN) LOWER SLOT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Mini Card

Size: A3 | Document Number: Big Bear 2A | Rev: SA

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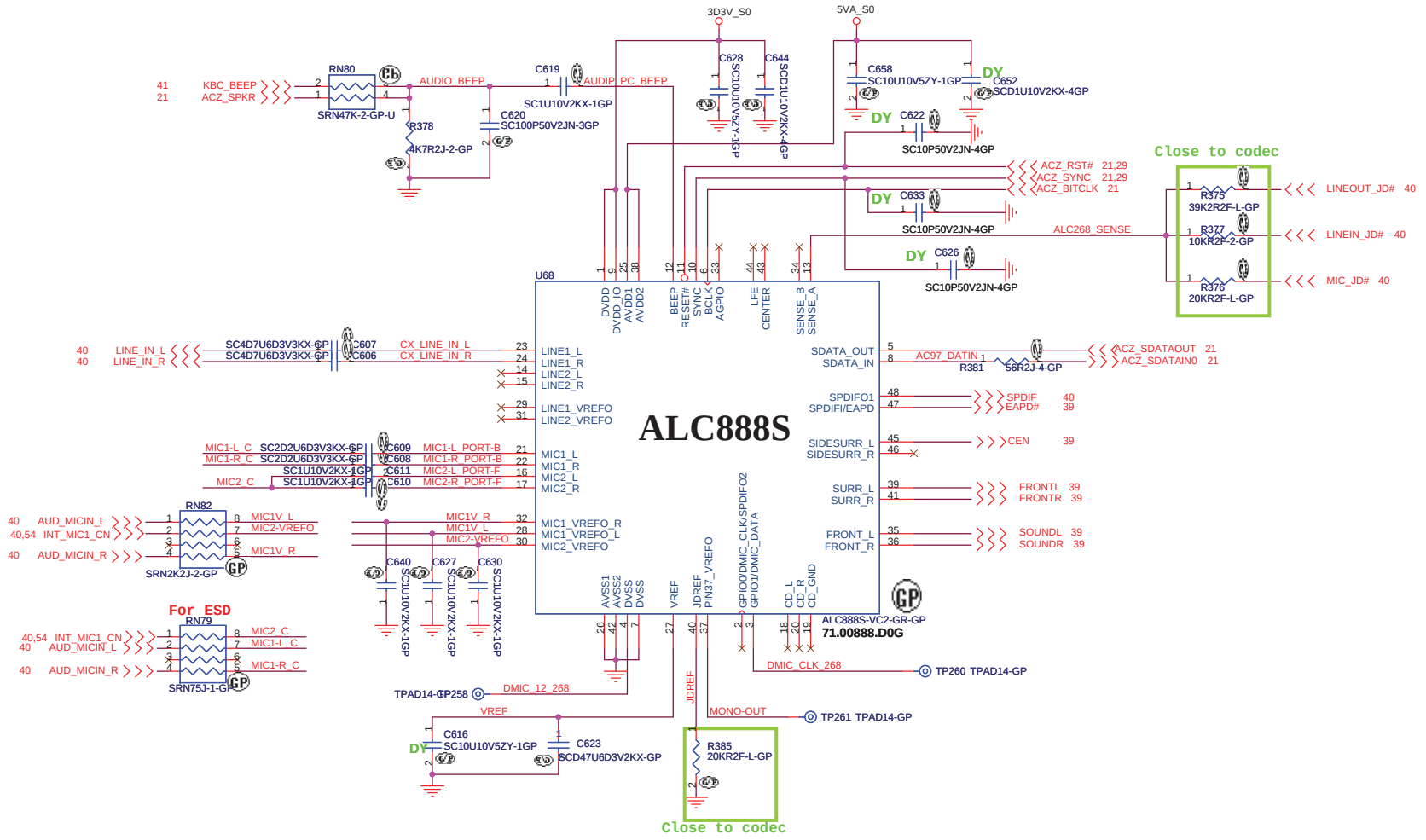
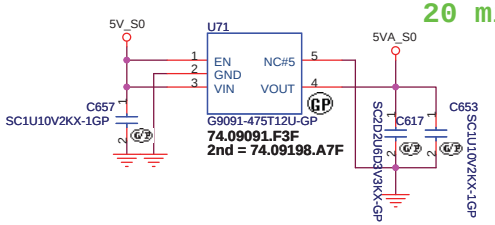


POWER GENERATE

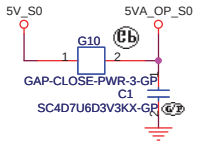
Layout
20 mil

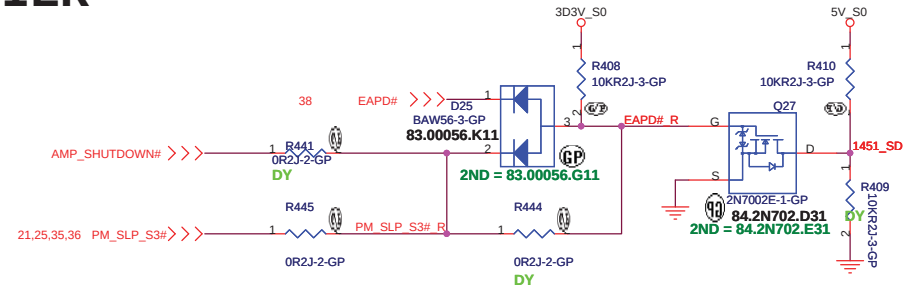


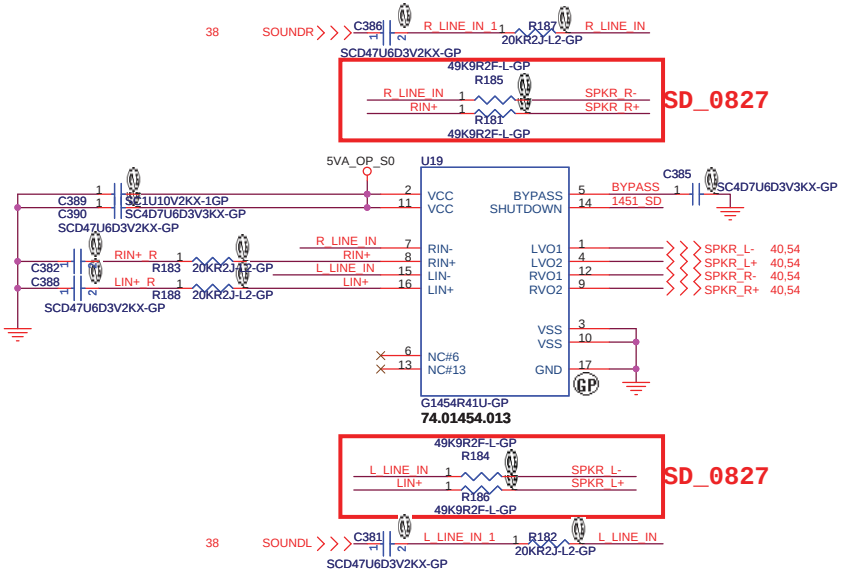
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Azalia codec ALC268*		
Size: A3	Document Number: Big Bear 2A	Rev: SA
Date: Monday, October 27, 2008	Sheet 38 of 55	

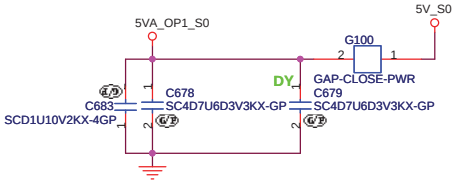
AUDIO OP AMPLIFIER

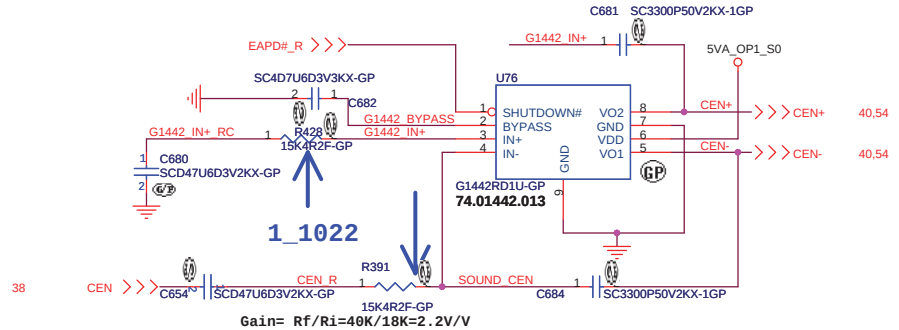






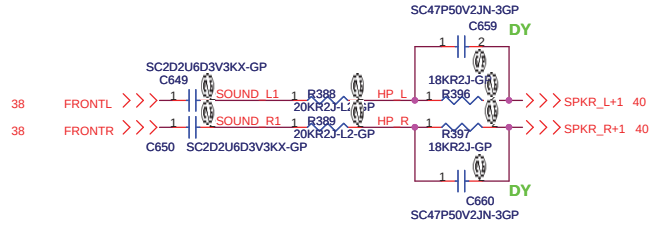
Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.828^2/4=1.999W



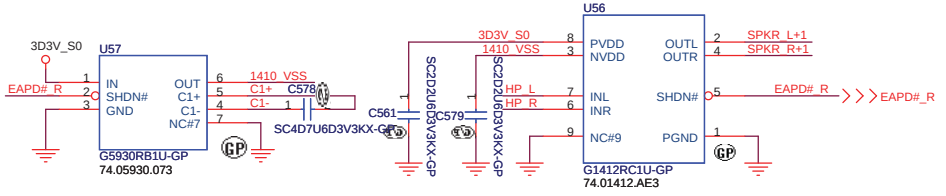


Gain= Rf/Ri=40K/18K=2.2V/V
f(HP)=1/(2 Pi*18K*0.47uf)=18Hz
If VIN= 1.54V Gain=2.2V/V RL=4Ω VO(peak) =3.38V V(rms)=2.390V
Power= 2.390^2/4=1.428W

KBC_MUTE_GPIO8



Gain= Rf/Ri=20K/18K=0.9V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=0.9V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= ?



<Core Design>

緯創資通 **Wistron Corporation**
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Title: AUDIO AMP

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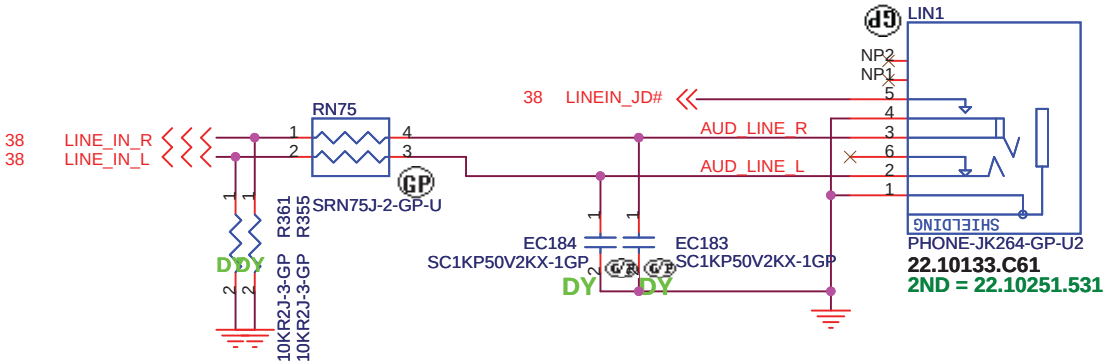
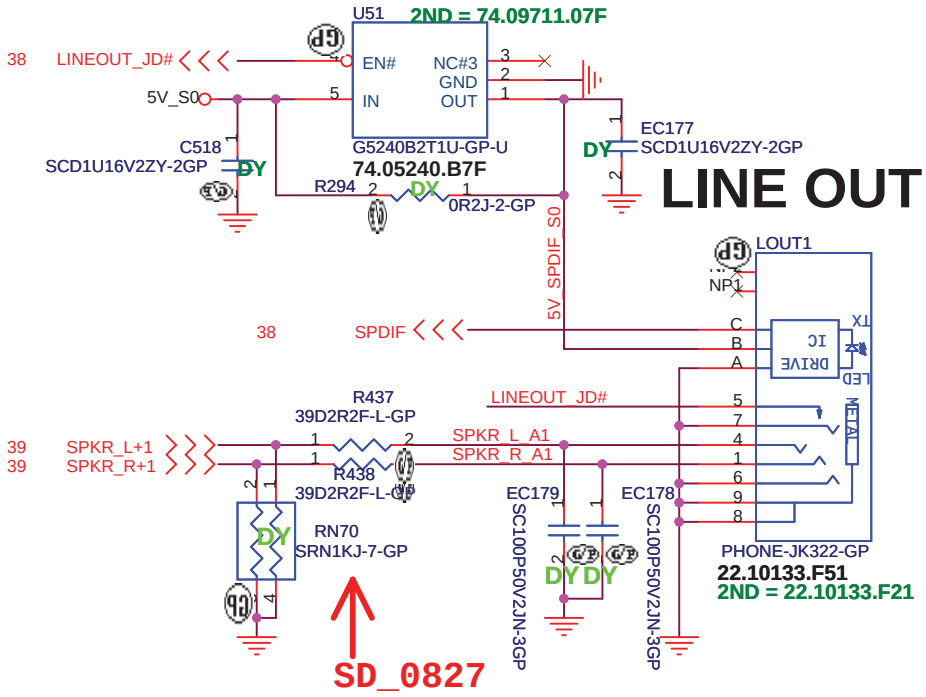
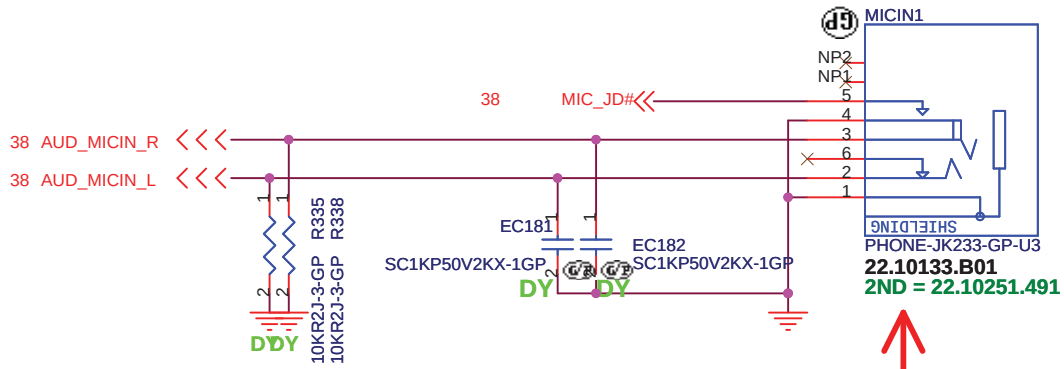
LINE IN



LINE OUT

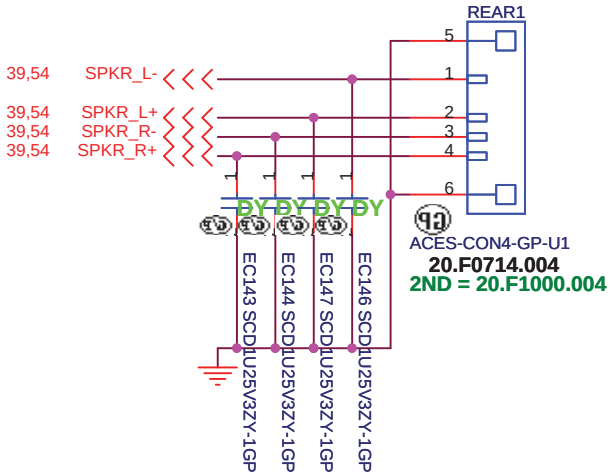


MIC IN

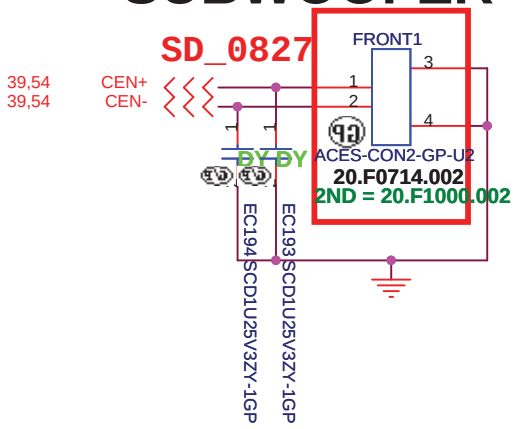


SD_0912 change 2nd

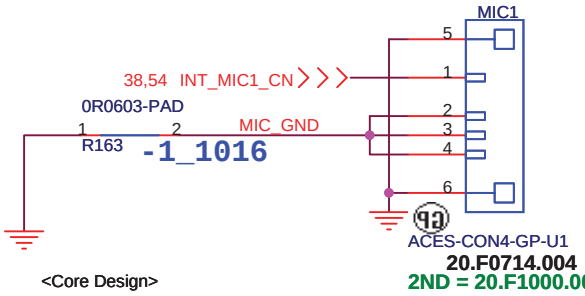
REAR Speaker



SUBWOOFER



INT. MIC



<Core Design>

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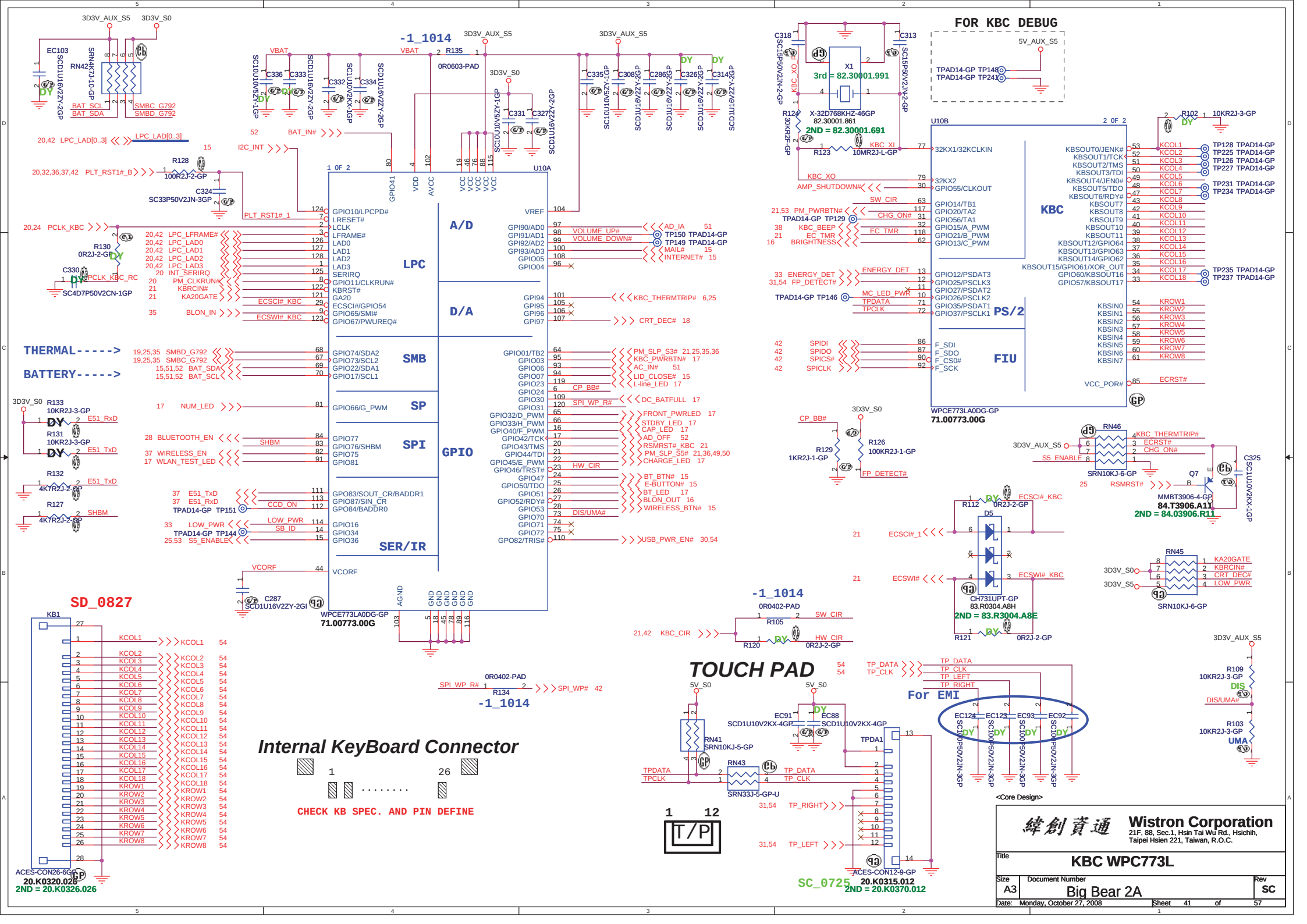
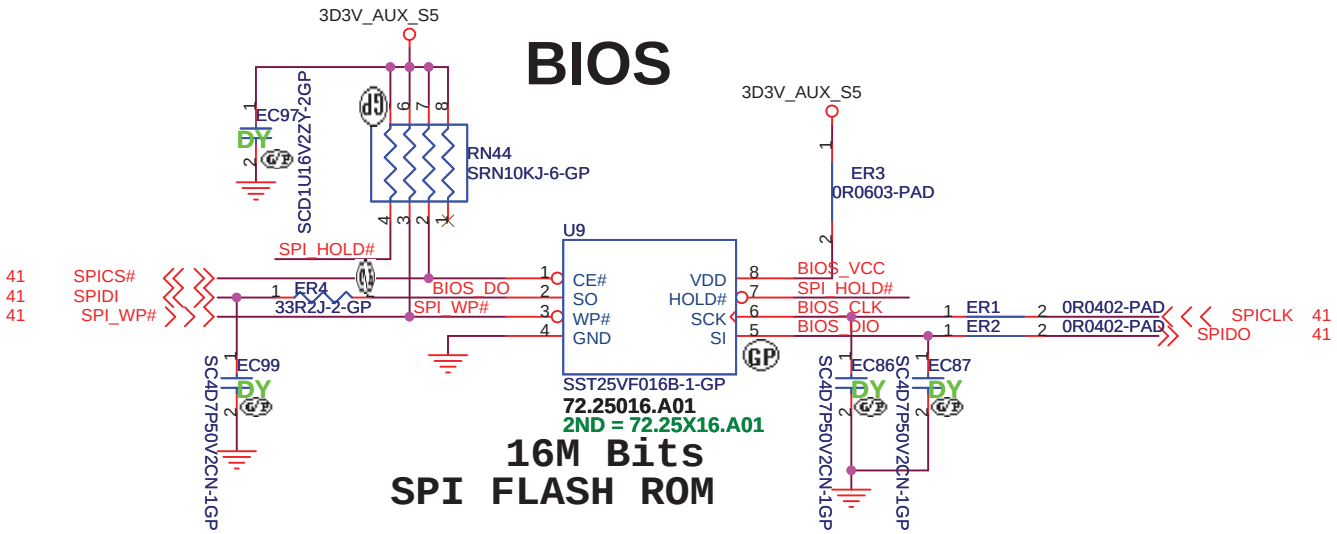
Title	AUDIO JACK	
Size A4	Document Number Big Bear 2A	Rev SD
Date: Monday, October 27, 2008	Sheet 40 of 55	

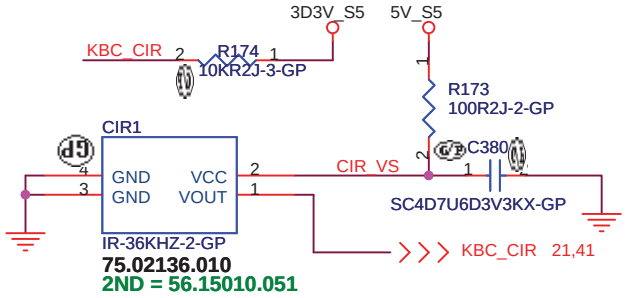

FOR KBC DEBUG
-1_1014
KBC
PS/2
FIU
SD_0827
Internal KeyBoard Connector
CHECK KB SPEC. AND PIN DEFINE
TOUCH PAD
For EMI
THERMAL----->
BATTERY----->
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773L
Big Bear 2A
Monday, October 27, 2008

BIOS



16M Bits
SPI FLASH ROM

CIR Module

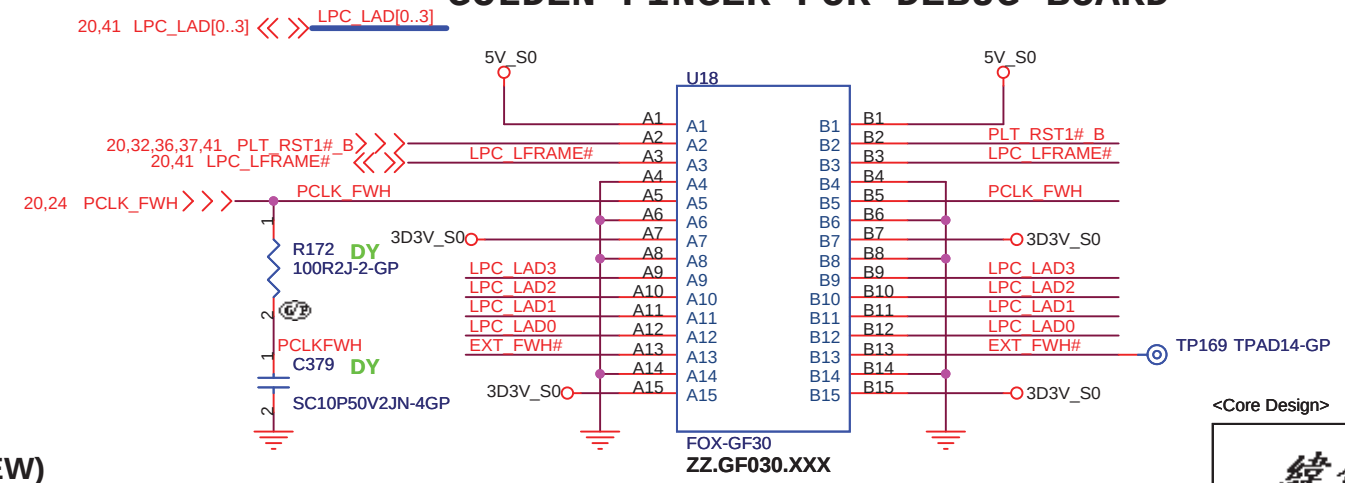


GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)



<Core Design>

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Title	BIOS & CIR	
Size: A4	Document Number: Big Bear 2A	Rev: SB
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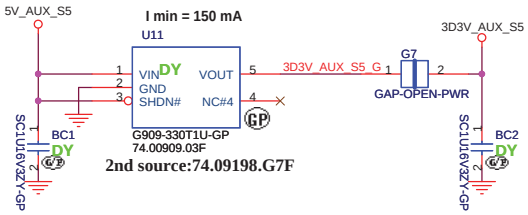
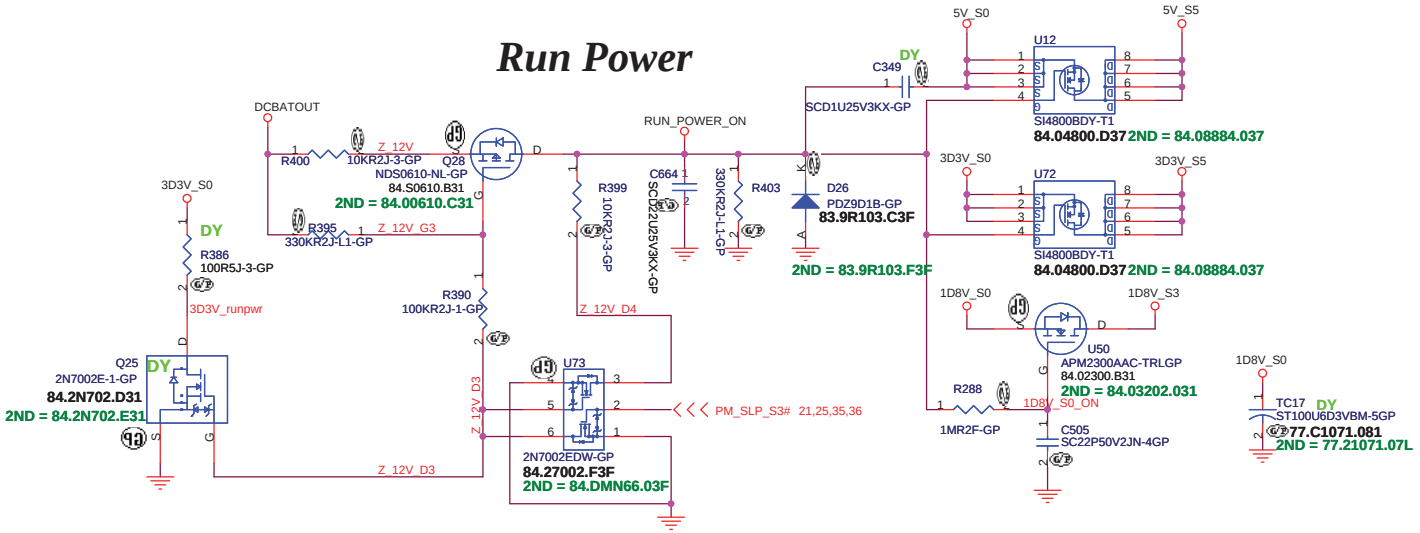
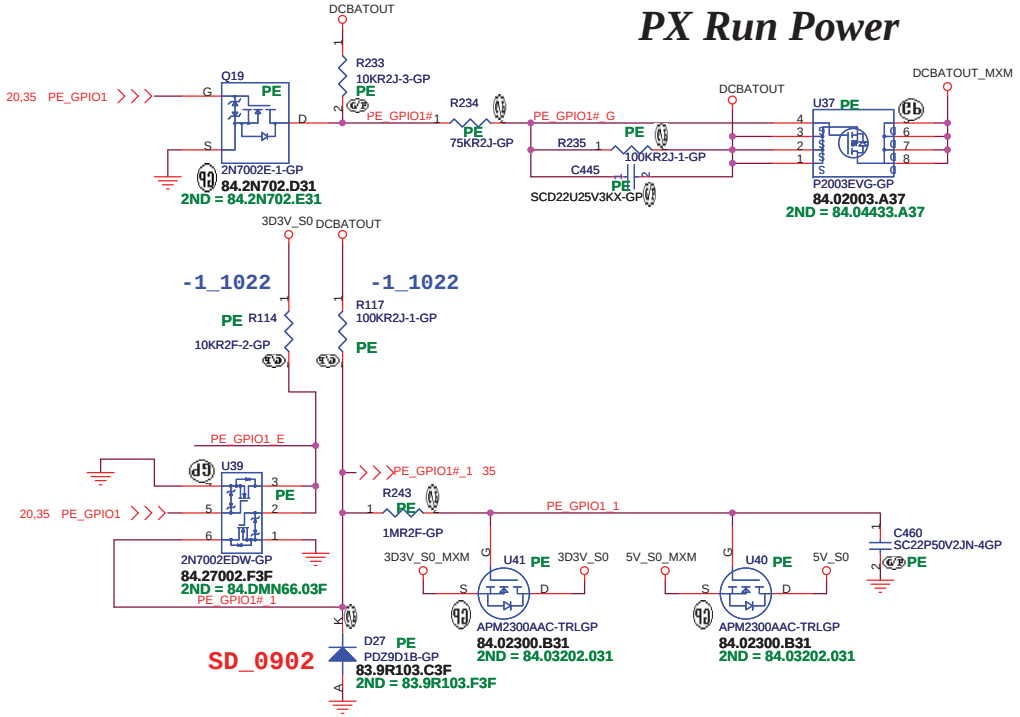
Aux Power 3D3V_AUX_S5



Run Power

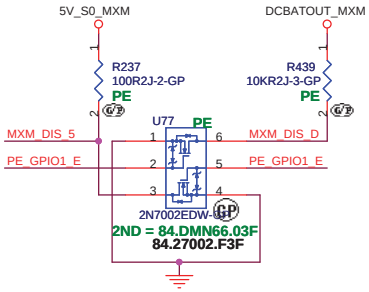


PX Run Power



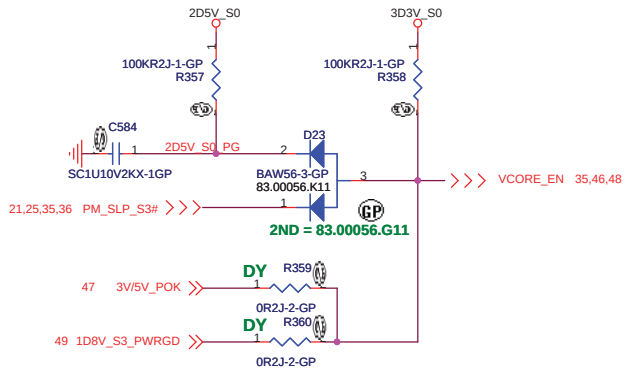
SD_0902

PX Run Power Discharge circuit

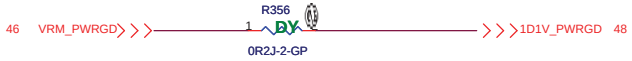


<Core Design>

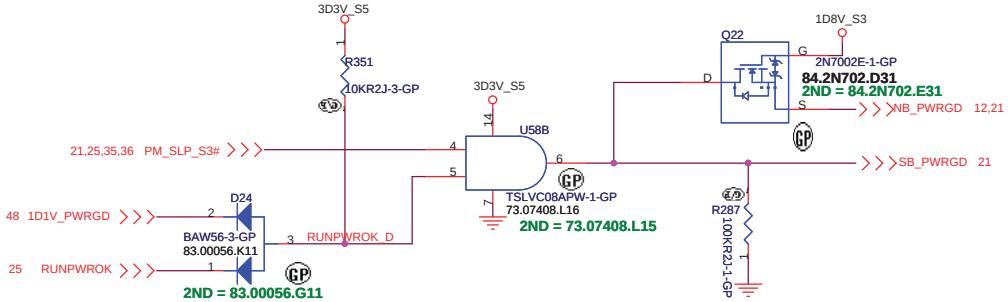
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RUN POWER and 3D3V_AUX_S5		
Size: A3	Document Number: Big Bear 2A	Rev: SD
Date: Monday, October 27, 2008	Sheet 43 of 57	



P/H @ 1D8V_S3 PAGE



Reference schematic recommend



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER ON LOGIC***

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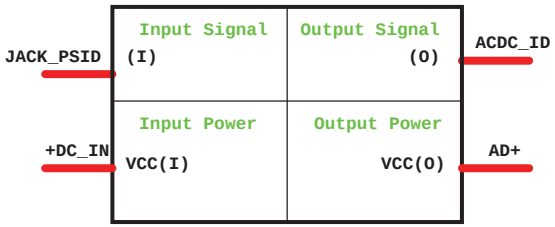
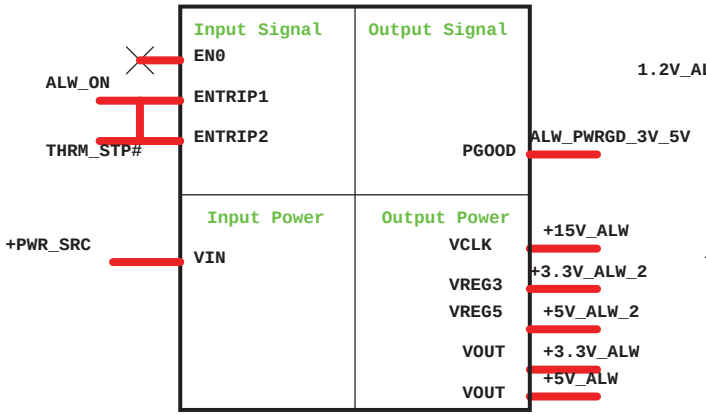
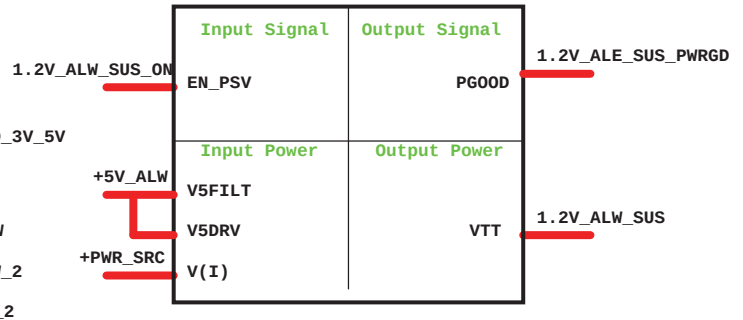
Adapter



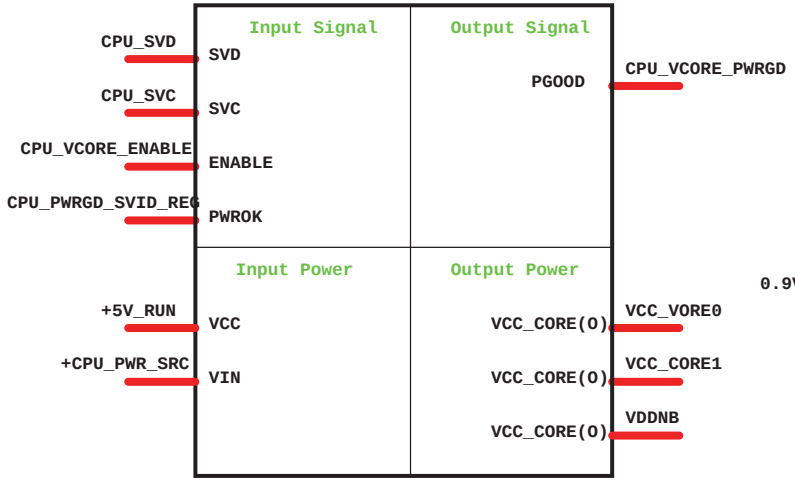
SN0608098



DCDC 1D2V(TPS5117)

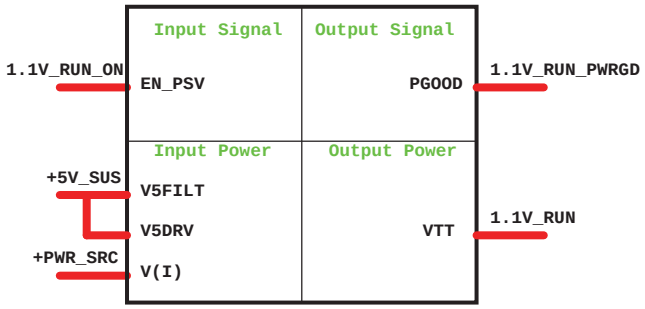


CPU_CORE
ISL6265HRTZ

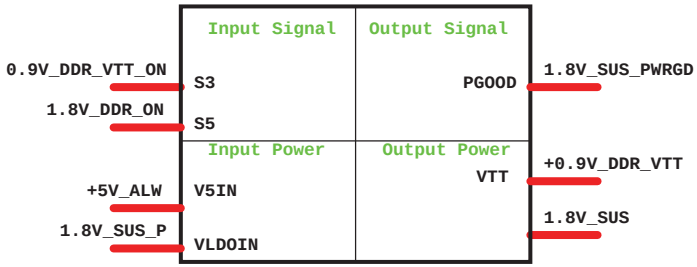


	S3	S5	VDDQ	VTTREF	VTT
S0 S3	1	1	1	1	1
S4 S5	0	0	0	0	0

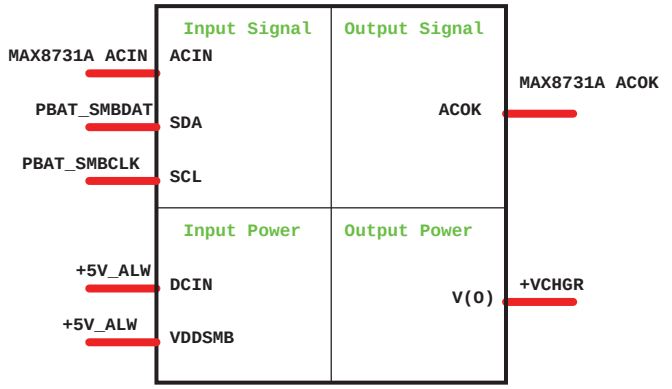
1D1V(TPS5117)



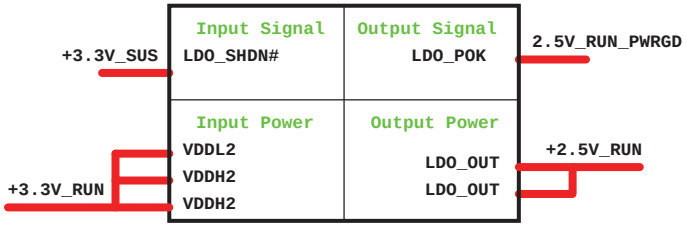
1D8V/0D9V(TPS5116)



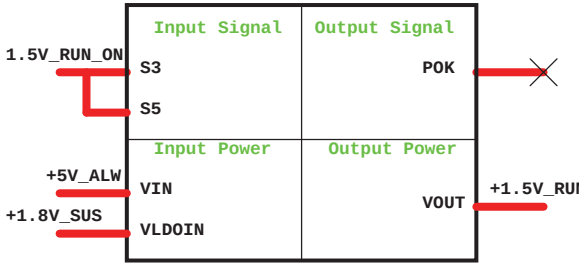
CHARGER BQ24745



2.5V LDO
EMC4002



1.5V_LDO



<Core Design>

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Title: **Power Block Diagram**

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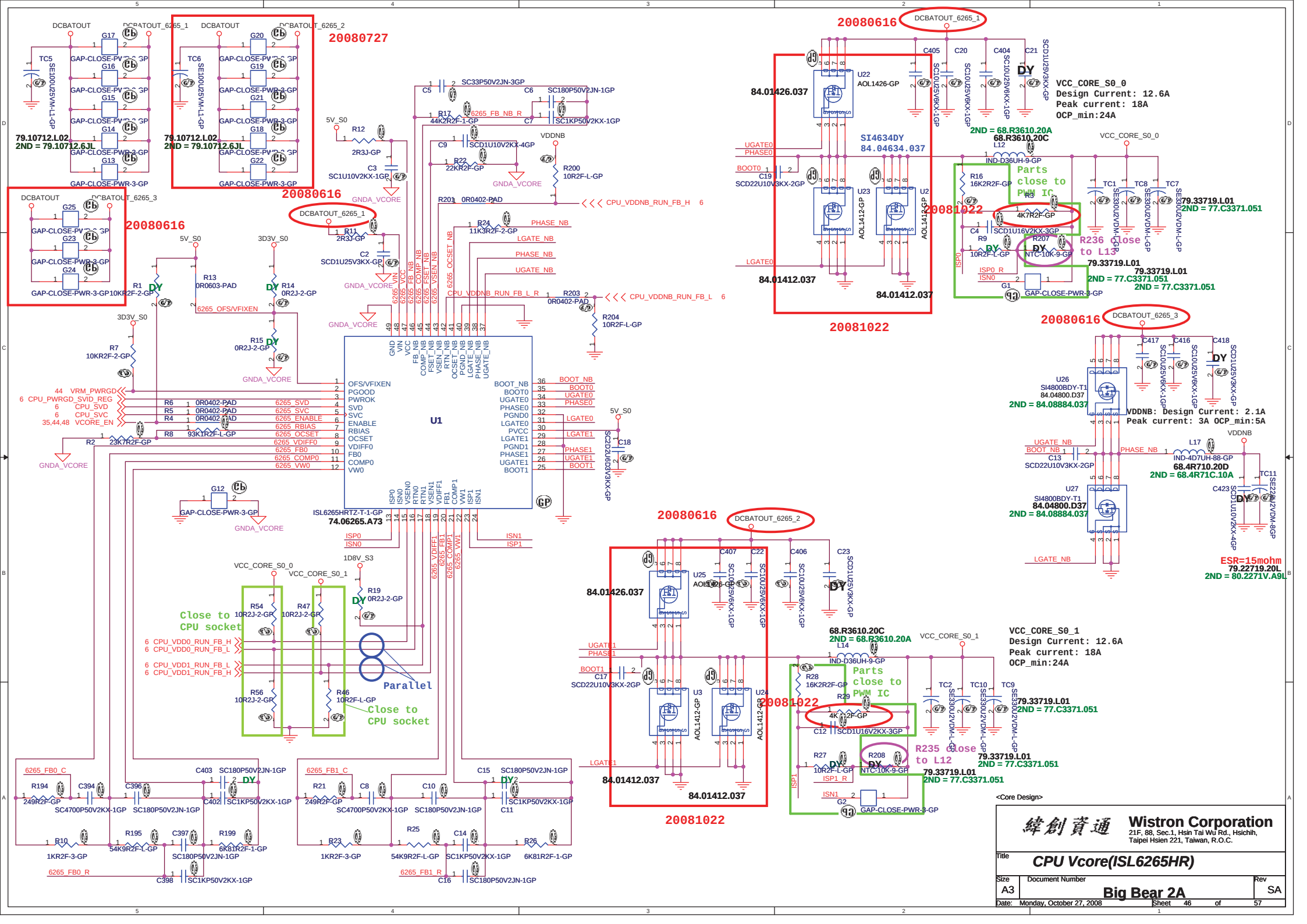
20080727
20080616
20081022
U1
ISL6265HRTZ-T-1-GP
74.06265.A73
OFS/VFIXEN
PGOOD
PWROK
SVD
SVC
ENABLE
RBIAS
OCSET
VDIFF0
FB0
COMP0
VW0
GND
VIN
VCC
FB_NB
COMP_NB
FSET_NB
VSEN_NB
RTN_NB
OCSET_NB
PGND_NB
LGATE_NB
PHASE_NB
UGATE_NB
BOOT_NB
BOOT0
UGATE0
PHASE0
PGND0
LGATE0
PVCC
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISP0
ISN0
VSEN0
RTN0
VSEN1
VDIFF1
FB1
COMP1
VW1
ISP1
ISN1
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
ESR=15mohm
79.22719.20L
2ND = 80.2271V.A9L
Close to CPU socket
Parallel
Parts close to PWM IC
R236 Close to L13
R235 Close to L12
Wistron Corporation
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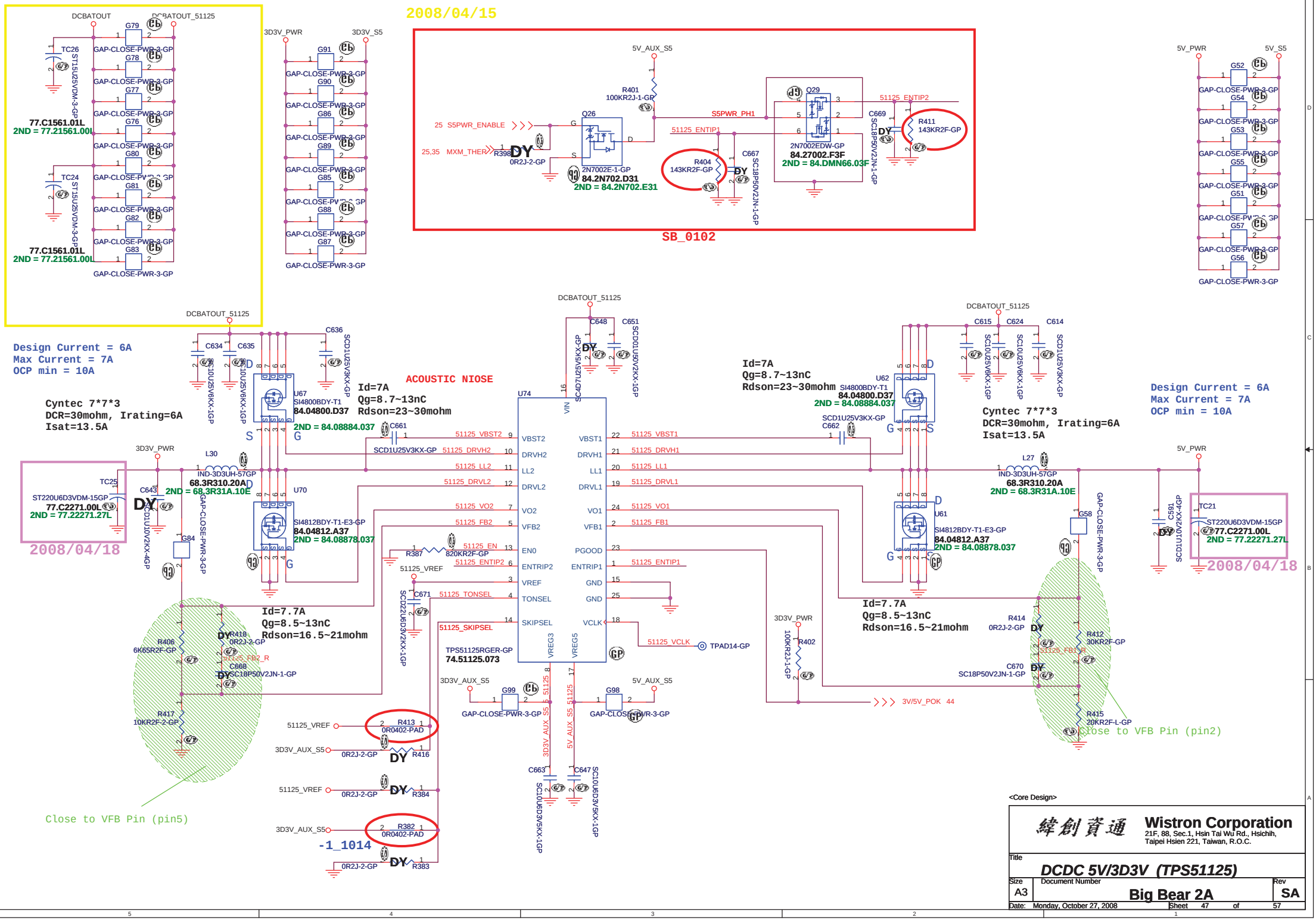
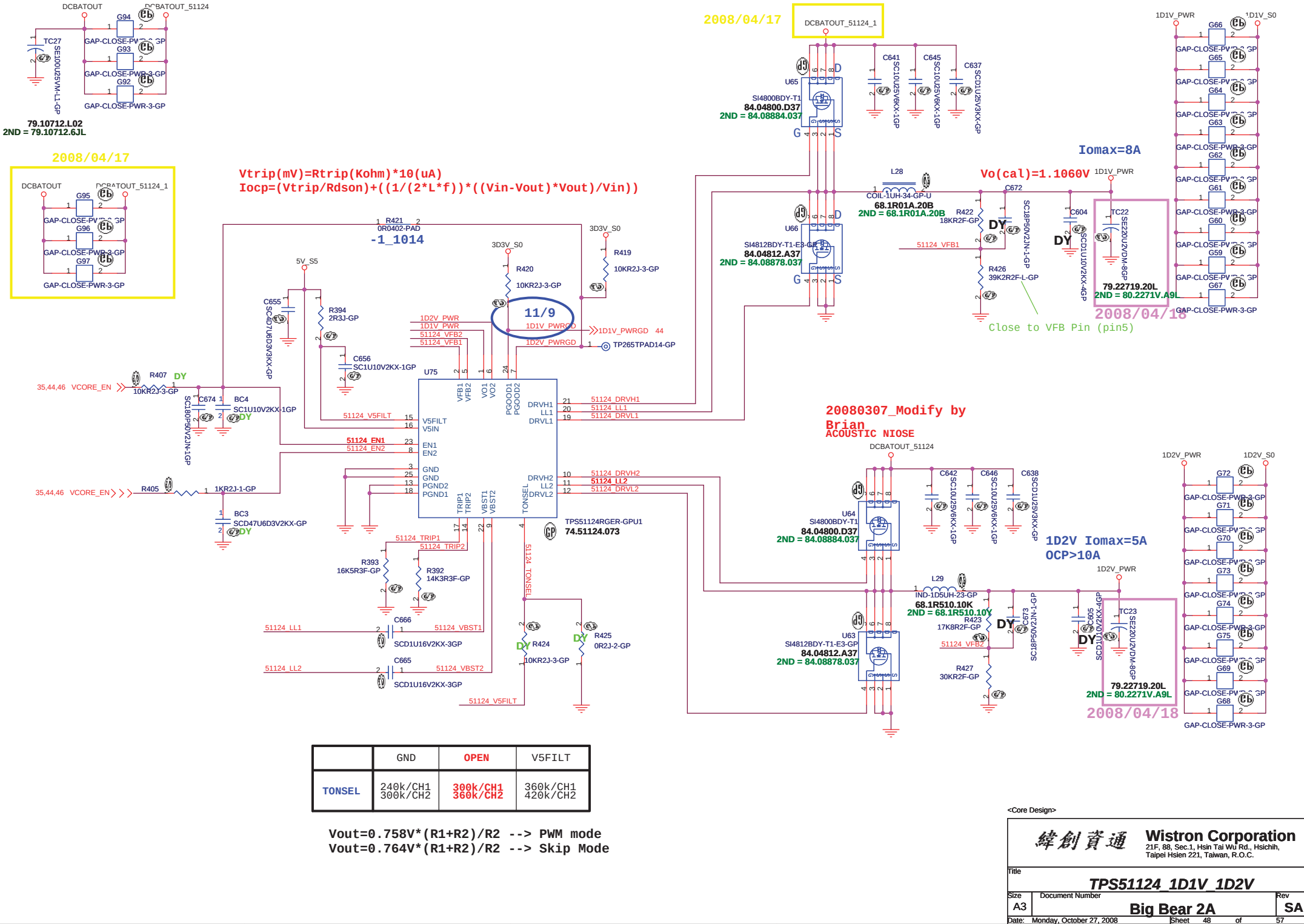
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
Big Bear 2A
Monday, October 27, 2008


2008/04/15
SB_0102
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
ACOUSTIC NIOSE
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
2008/04/18
2008/04/18
-1_1014
TPS51125RGER-GP
74.51125.073
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Big Bear 2A
Monday, October 27, 2008



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

<Core Design>

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Title: TPS51124_1D1V_1D2V

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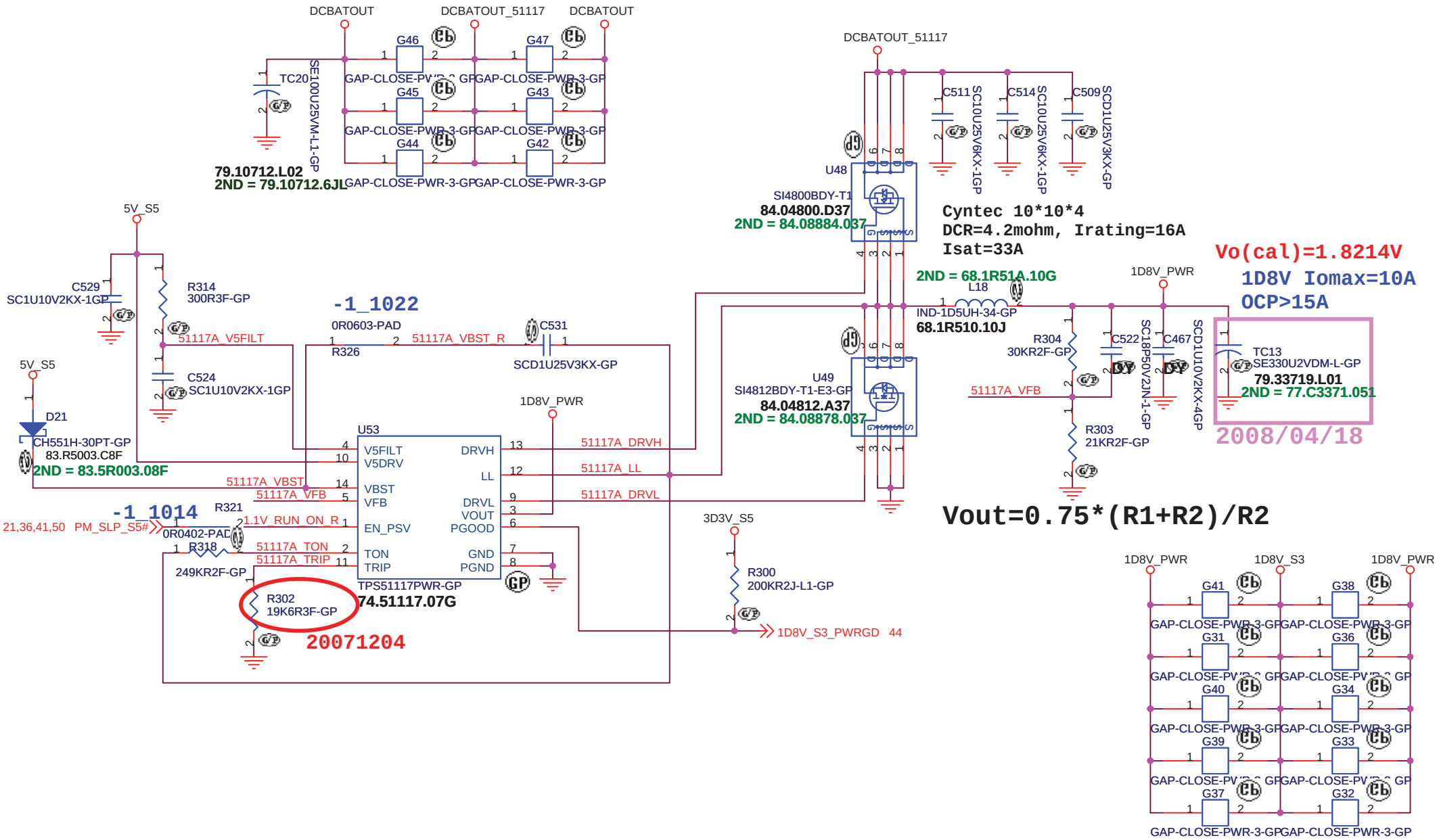

<Core Design>

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Title: *1D8V(TPS5117)*

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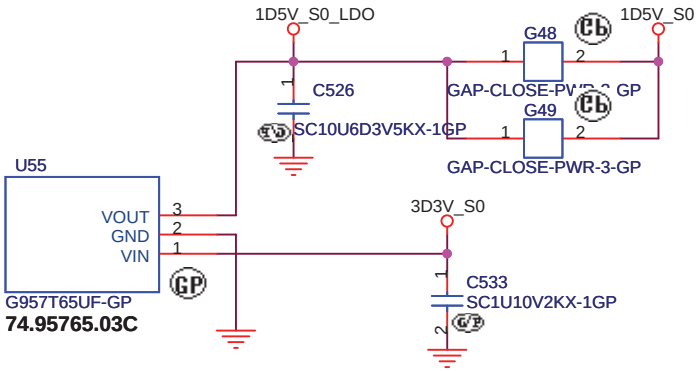
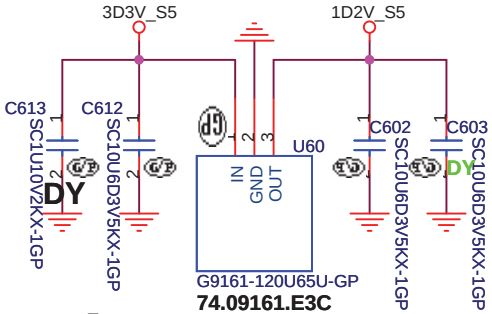
G957

1D5V_S0
Iomax=1A

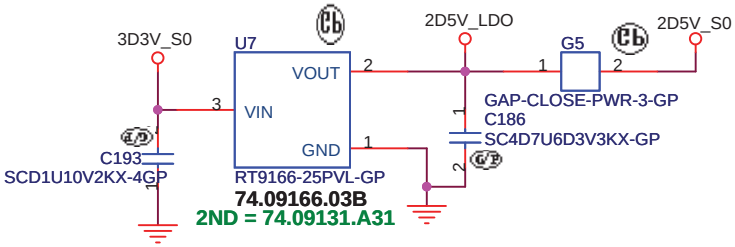


1D2V_S5
Iomax=400mA

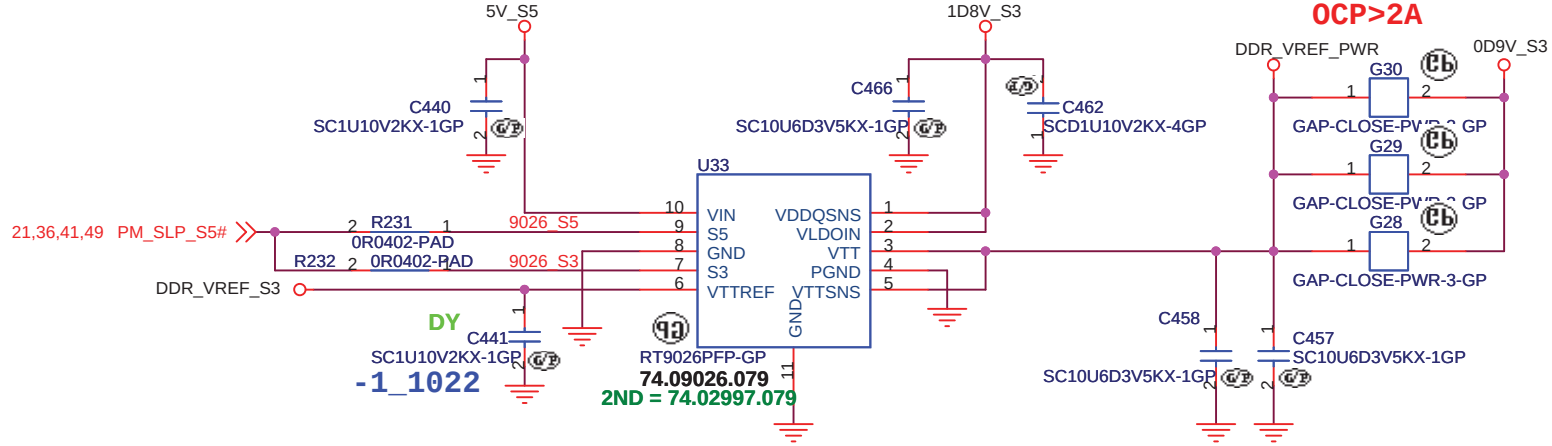


Place near to SB700

2D5V_S0
Iomax=0.3A 2D5V/300mA



Iomax=1A
OCP>2A



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V&2D5V&1D25V&1D5V

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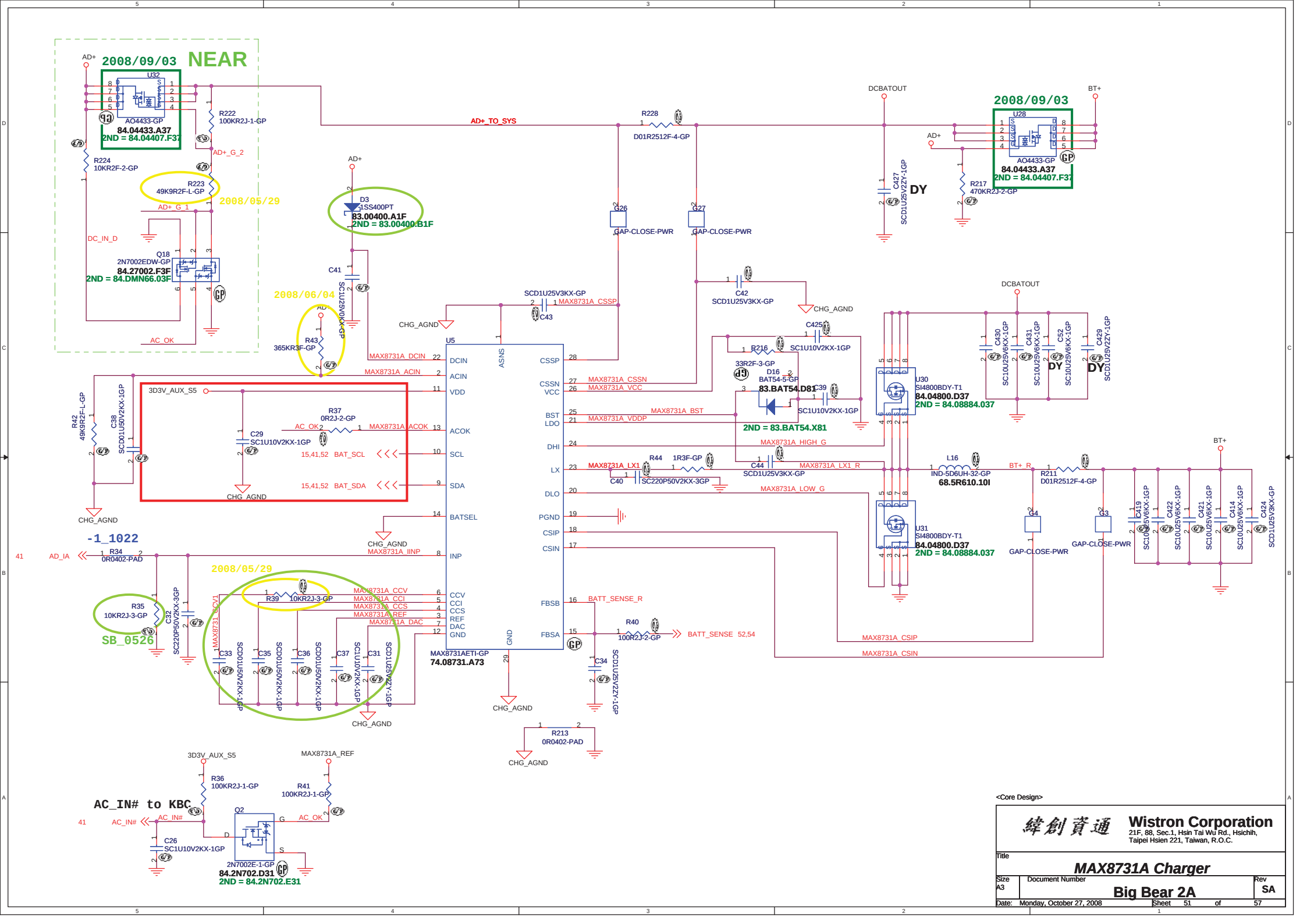

<Core Design>

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Title: **MAX8731A Charger**

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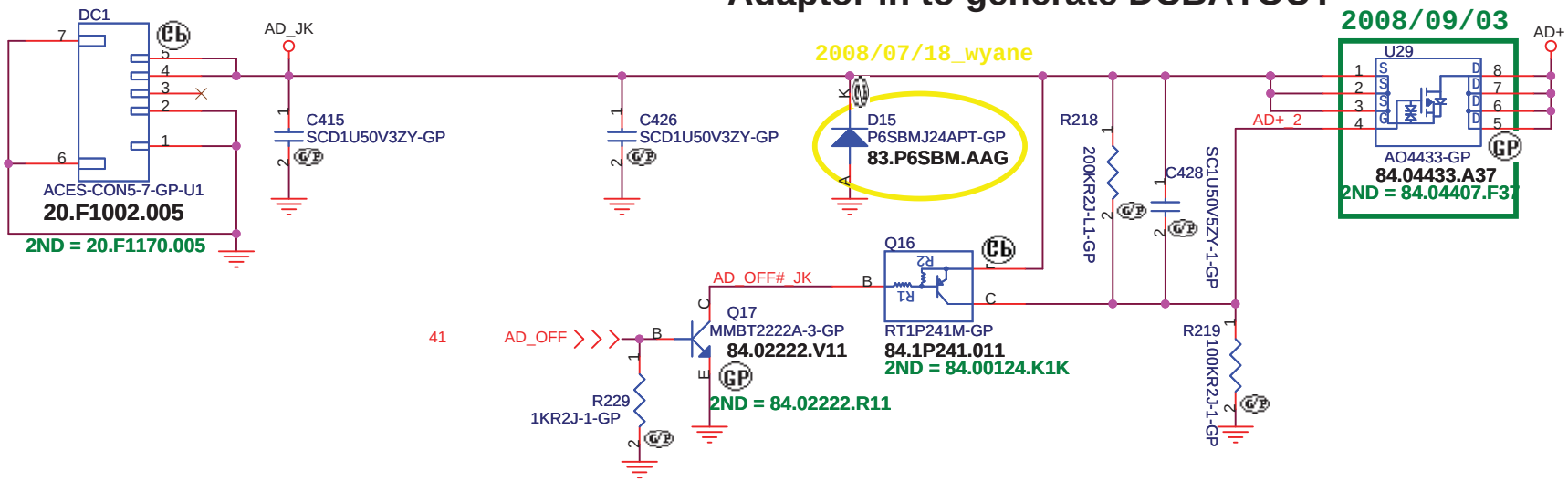
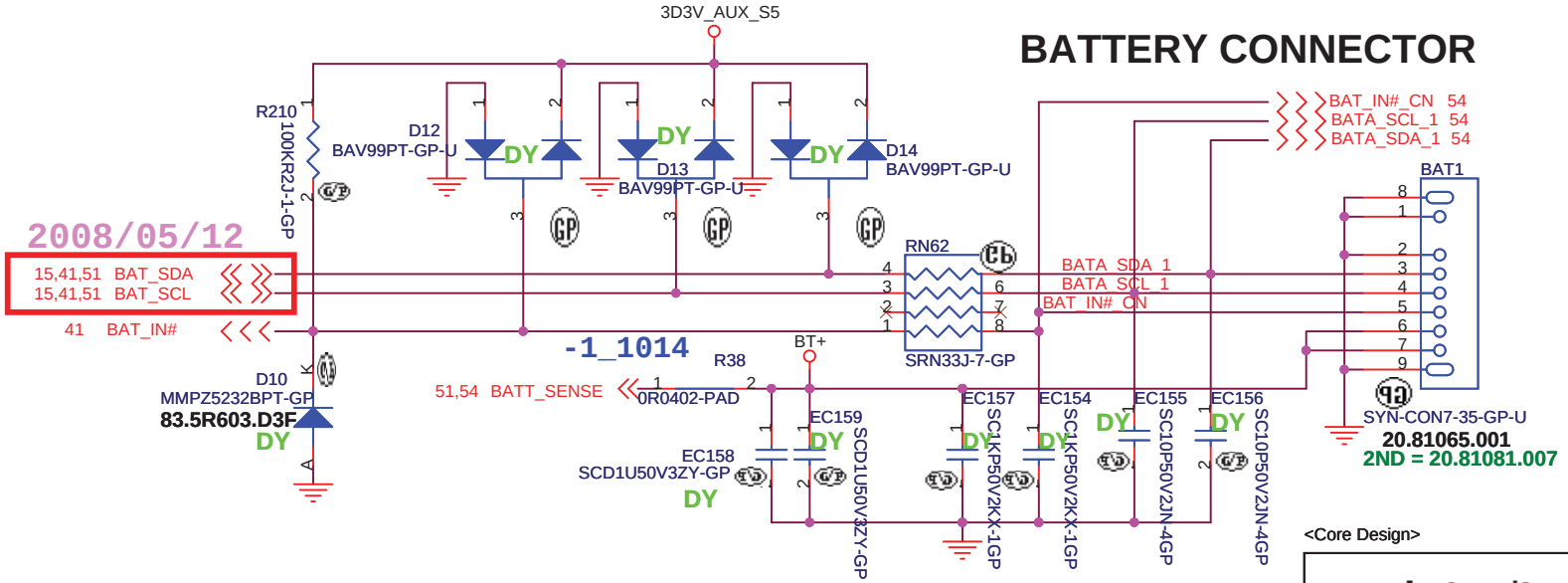
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AD/BATT CONN***

Size	Document Number	Rev
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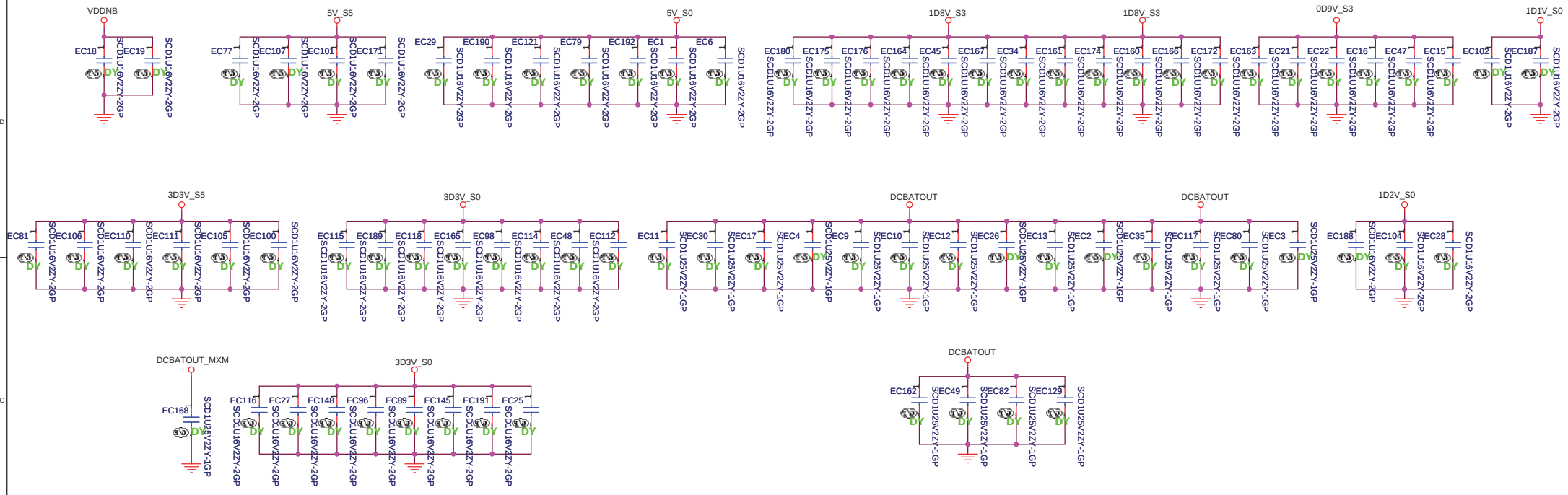

SPRING ON BOTTOM

DIMM

GND3 SPRING-62-GP 34.39S07.003 DY

GND1 SPRING-62-GP 34.39S07.003 DY

MXM

S1 SPRING-37-GP-U 34.15F09.001 DY

S2 SPRING-37-GP-U 34.15F09.001 DY

S3 SPRING-37-GP-U 34.15F09.001 DY

SPRING ON TOP

SD_0903

Touch Pad

H30 SPRING-57-GP 34.42T14.002

HDMI

SW2 SPRING-15-GP DY

SB-U15

SW3 SPRING-7 DY

SW4 SPRING-7 DY

SW5 SPRING-7 DY

USB

SW6 SPRING-6 DY

SW7 SPRING-6 DY

Jack

SW8 SPRING-15-GP DY

RN24

SW9 SPRING-7 DY

STAND OFF ON BOTTOM

CPU & NB

H31 HOLE 34.42Y01.011

H32 HOLE 34.42Y01.011

H33 HOLE 34.42Y01.011

H34 HOLE 34.42Y01.011

Mini Card

H19 HOLE 34.4Z402.001

H20 HOLE 34.4Z402.001

MXM

H14 HOLE DIS 34.4Z401.001

H17 HOLE DIS 34.4Z401.001

STAND OFF ON TOP

MDC

H21 HOLE 34.42Y01.011

H22 HOLE 34.42Y01.011

H1 PAD-1P-3-GP

H2 PAD-1P-3-GP

H3 PAD-1P-3-GP

H4 PAD-1P-3-GP

H5 PAD-1P-3-GP

H6 PAD-1P-3-GP

H7 PAD-1P-3-GP

H8 PAD-1P-3-GP

H9 PAD-1P-3-GP

H10 PAD-1P-3-GP

H13 PAD-1P-3-GP

H18 PAD-1P-3-GP

PAD1 PAD-1P-4-GP

H39 PAD-1P-3-GP

H40 PAD-1P-3-GP

Check test point

3D3V_S0	TP263 TPAD14-GP
3D3V_AUX_S5	TP226 TPAD14-GP
3D3V_S5	TP262 TPAD14-GP
5V_S5	TP246 TPAD14-GP
21,41 PM_PWRBTN#	TP253 TPAD14-GP
6,20 CPU_PWRGD	TP141 TPAD14-GP
25,41 S5_ENABLE	TP143 TPAD14-GP
6,20 CPU_LDT_RST#	TP238 TPAD14-GP

Test Point放在Dimm Door打開可量測處

<Core Design>

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Title: EMI/Spring/Boss

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<Core Design>

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