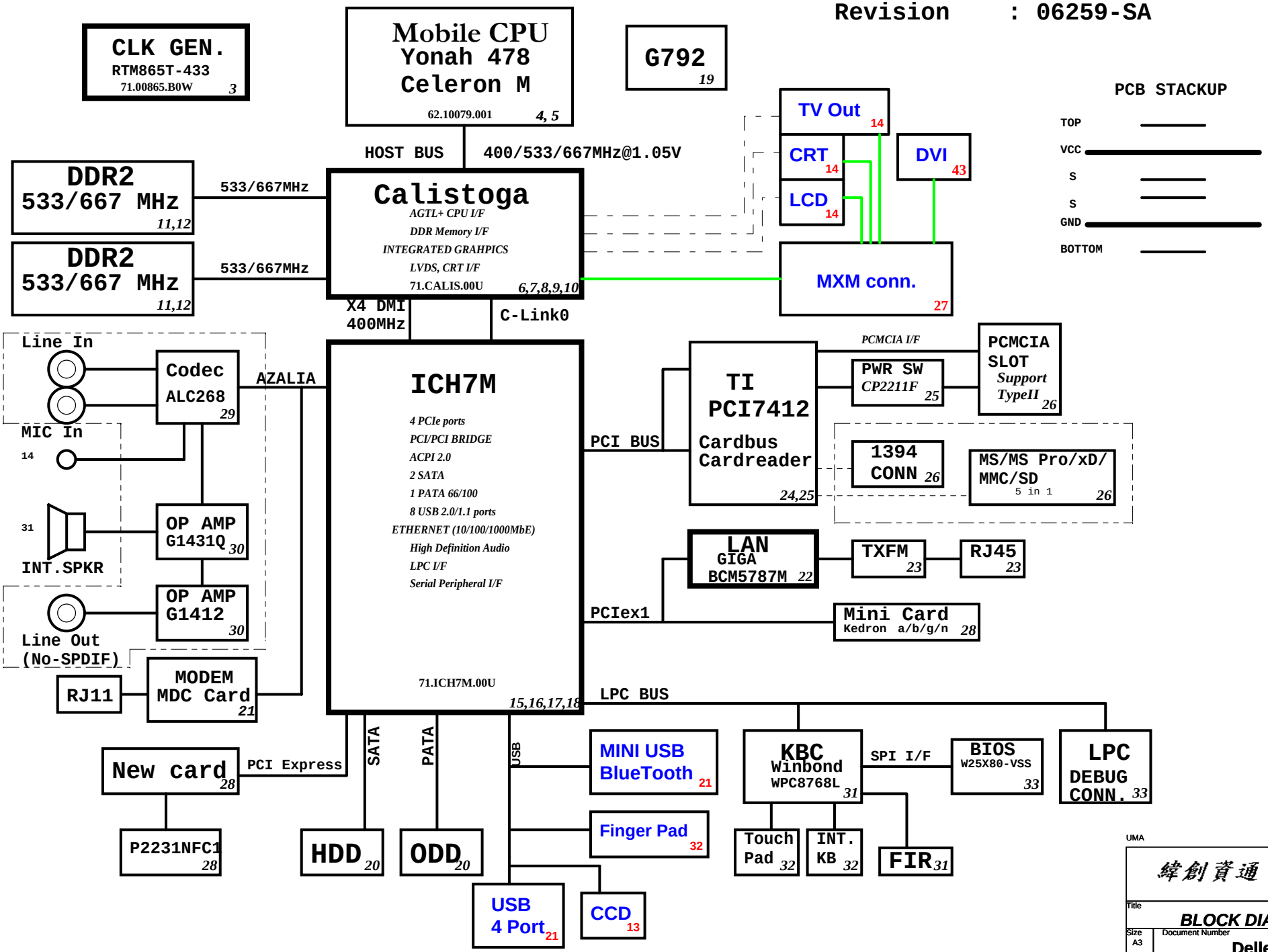
Dellen Block Diagram

Project code: 91.4V401.001
PCB P/N : 48.4T307.0SA
Revision : 06259-SA



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC MAX8744 37	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5(6A) 5V_S5 (6A) 5V_AUX_S5

SYSTEM DC/DC Max8717 38	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(12A) 1D8V_S3(8.5A)

TPS51100 39	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL531230 39	
3D3V_S0	2D5V_S0(130 mA

APL5912 39	
1D8V_S3	1D5V_S0(5A)

ISL CHARGER ISL6255 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC MAX8770 35,36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

UMA

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Title: BLOCK DIAGRAM

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Date: Tuesday, January 16, 2007 | Sheet 1 of 43

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

Calistoga Strapping Signals and Configuration

EDS 17050 0.71

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	FingerPad
5	BlueTooth
6	CCD
7	NewCard

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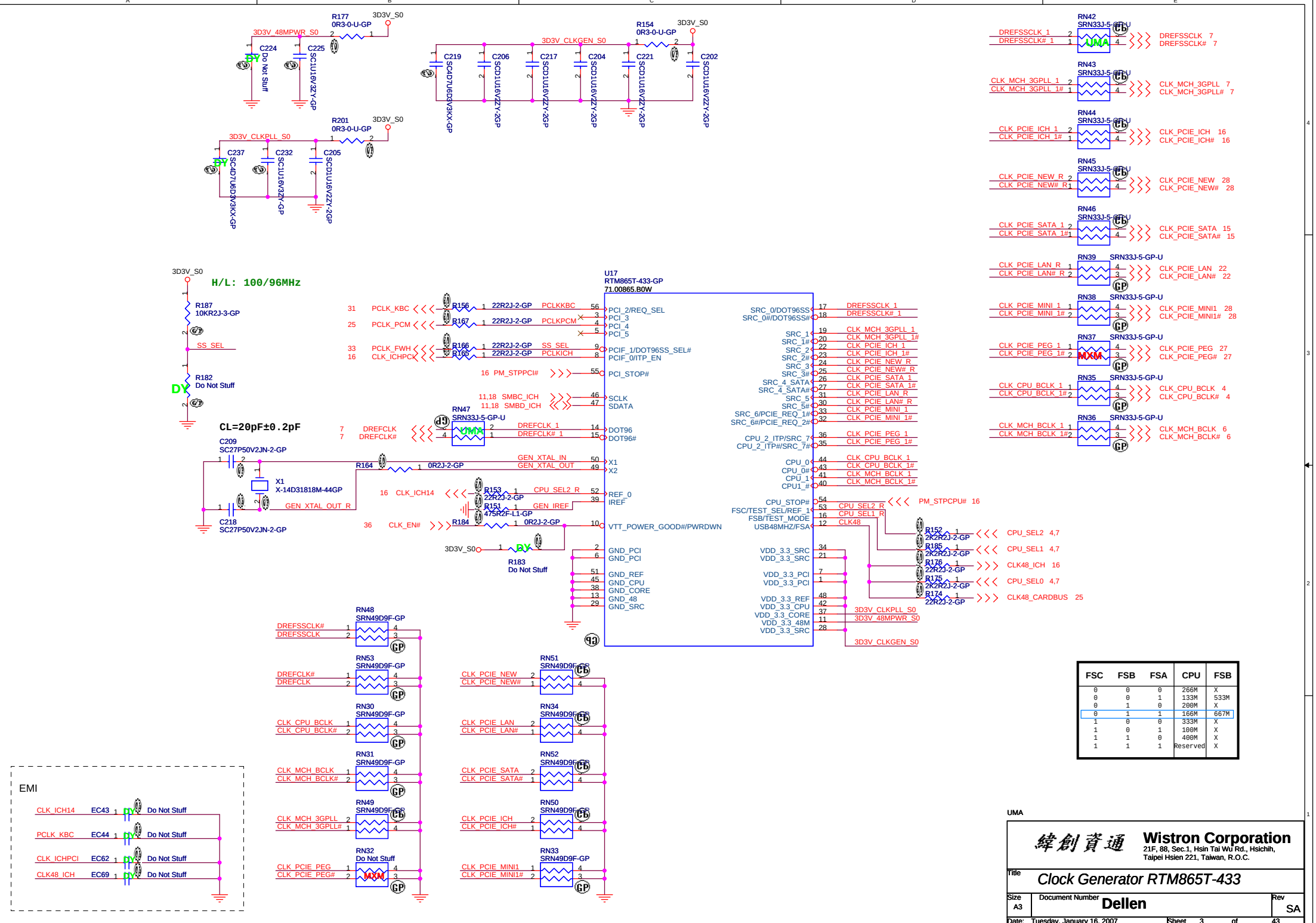
Title: Reference

Size: A3 | Document Number: Dellen | Rev: SA

Date: Tuesday, January 16, 2007 | Sheet 2 of 43



FSC	FSB	FSA	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

2nd source: 62.10053.401

U41A
BGA479-SKT6-GPU3
62.10079.001

ADDR GROUP 0 / ADDR GROUP 1 / CONTROL / XDP/ITP SIGNALS / THERM / H CLK / RESERVED

TP10 TPAD30

R80 56R2J-4-GP (1D05V_S0)

R79 56R2J-4-GP (1D05V_S0)

C89 SC2200P50V2KX-2GP

R53 1KR2J-1-GP (1D05V_S0)

R52 2KR2F-3-GP

C38 DY Do Not Stuff

Place testpoint on H_IERR# with a GND 0.1" away

PM_THRMTRIP# should connect to ICH7 and Calistoga without T-ing (No stub)

Layout Note: 0.5" max length.

U41B
BGA479-SKT6-GPU3
62.10079.001

DATA GRP 0 / DATA GRP 2 / DATA GRP 1 / DATA GRP 3 / MISC

R78 DY Do Not Stuff (TEST1)

R77 51R2F-2-GP (TEST2)

R67 27D4R2F-L1-GP
R66 54D9R2F-L1-GP
R65 27D4R2F-L1-GP
R62 54D9R2F-L1-GP

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .

1D05V_S0

R59 150R2F-1-GP
R56 DY 39D2R3F-2-GP
R57 DY Do Not Stuff
R82 Do Not Stuff

3D3V_S0

R76 DY Do Not Stuff

R54 27D4R2F-L1-GP
R55 680R3F-GP

All place within 2" to CPU

H_INIT# — C447 DY Do Not Stuff

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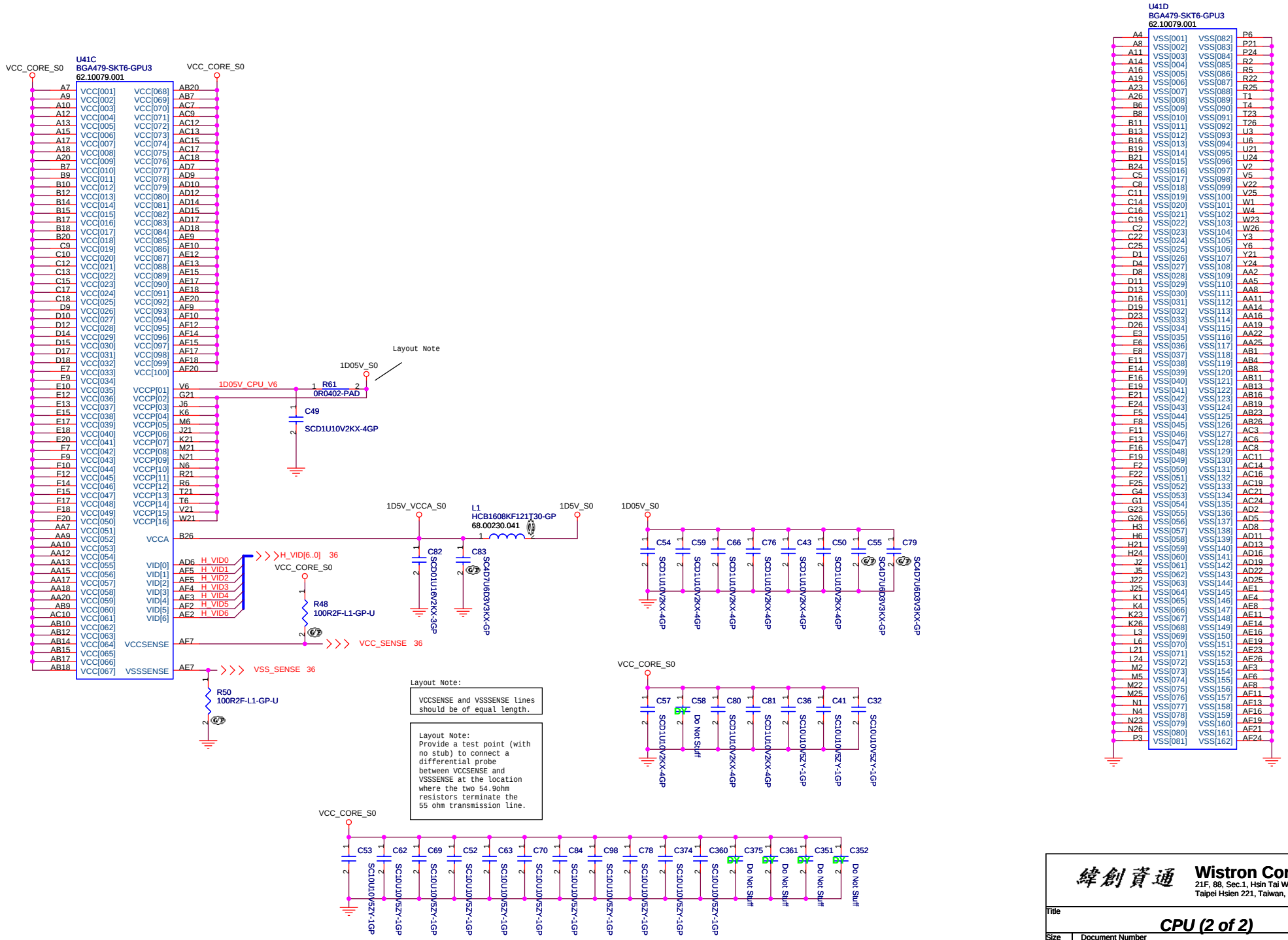
Title: CPU (1 of 2)

Size: A3 | Document Number: Dellen | Rev: SA

Date: Tuesday, January 16, 2007 | Sheet 4 of 43



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU (2 of 2)***
Size A3	Document Number **Dellen** Rev SA
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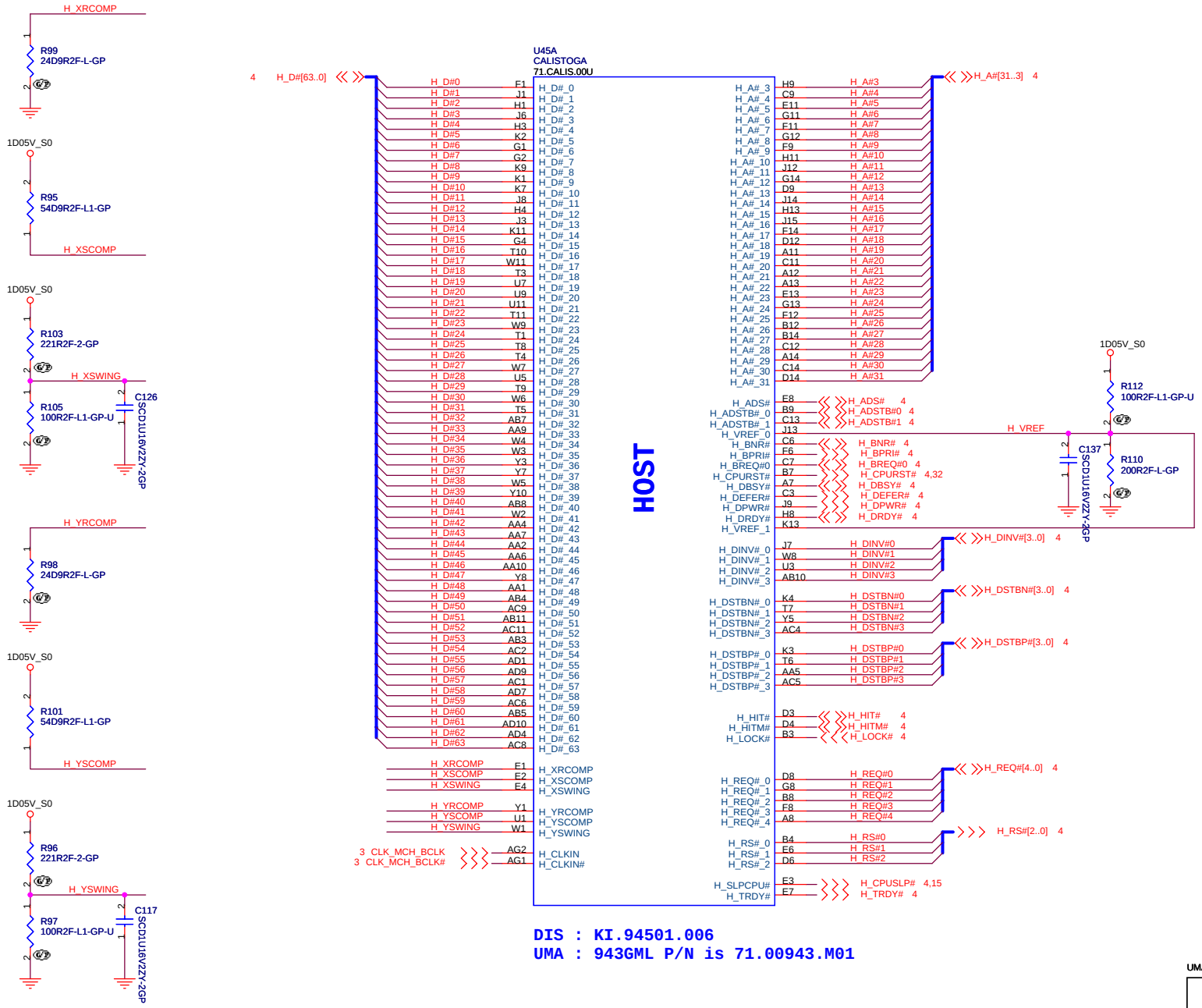

DIS : KI.94501.006
UMA : 943GML P/N is 71.00943.M01

Place them near to the chip (< 0.5")

UMA

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Title	***GMCH (1 of 5)***
Size A3	Document Number **Dellen**
Rev	SA
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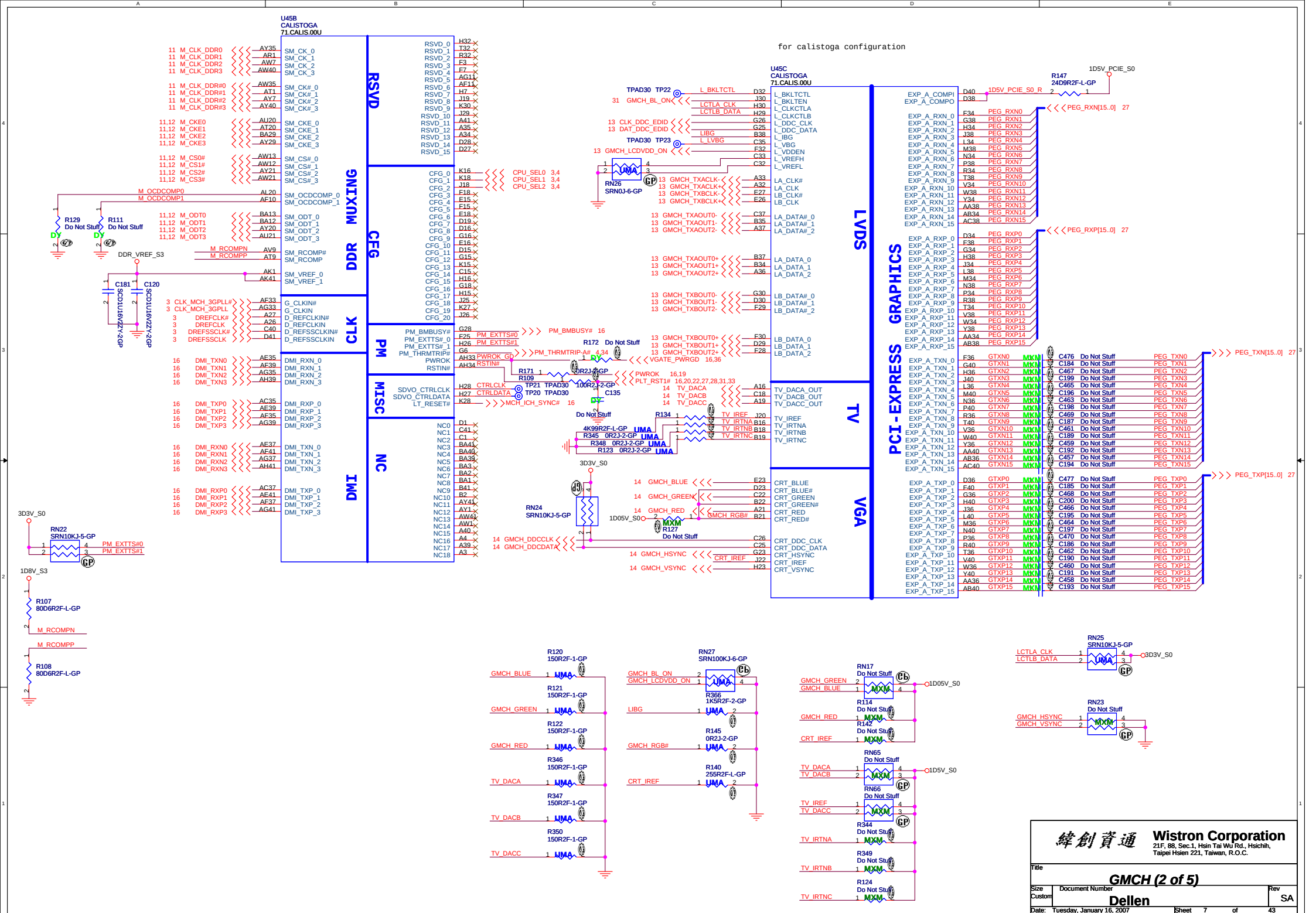
U45B
CALISTOGA
71.CALIS.00U
RSVD
MUXING
DDR
CFG
CLK
PM
MISC
NC
DMI
U45C
CALISTOGA
71.CALIS.00U
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
for calistoga configuration
RN22
SRN10KJ-5-GP
RN24
SRN10KJ-5-GP
RN26
SRN0J-6-GP
RN27
SRN100KJ-6-GP
RN25
SRN10KJ-5-GP
RN17
Do Not Stuff
RN65
Do Not Stuff
RN66
Do Not Stuff
RN23
Do Not Stuff
R147
24D9R2F-L-GP
R107
80D6R2F-L-GP
R108
80D6R2F-L-GP
R120
150R2F-1-GP
R121
150R2F-1-GP
R122
150R2F-1-GP
R346
150R2F-1-GP
R347
150R2F-1-GP
R350
150R2F-1-GP
R366
1K5R2F-2-GP
R145
0R2J-2-GP
R140
255R2F-L-GP
R114
Do Not Stuff
R142
Do Not Stuff
R344
Do Not Stuff
R349
Do Not Stuff
R124
Do Not Stuff
R127
Do Not Stuff
R134
R172
Do Not Stuff
R171
R109
C135
C181
SCD1U16V2ZY-2GP
C120
SCD1U16V2ZY-3GP
R129
Do Not Stuff
R111
Do Not Stuff
DDR_VREF_S3
3D3V_S0
1D8V_S3
1D05V_S0
1D5V_PCIE_S0
PEG_RXN[15..0] 27
PEG_RXP[15..0] 27
PEG_TXN[15..0] 27
PEG_TXP[15..0] 27
PM_BMBUSY# 16
PM_THRMTRIP# 4,34
VGATE_PWRGD 16,36
PWROK 16,19
PLT_RST1# 16,20,22,27,28,31,33
CPU_SEL0 3,4
CPU_SEL1 3,4
CPU_SEL2 3,4
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Title
GMCH (2 of 5)
Size
Custom
Document Number
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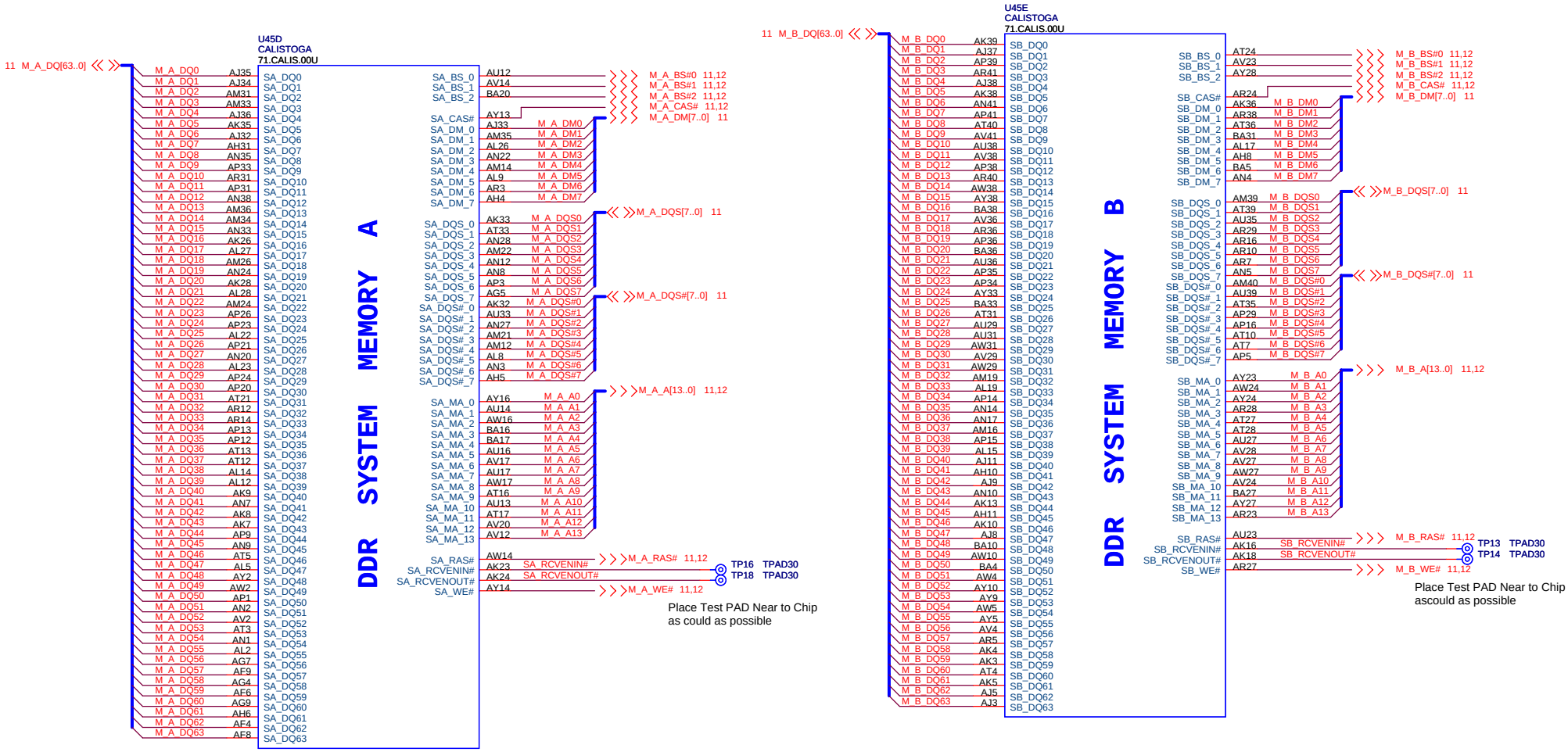

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Title: ***GMCH (3 of 5)***

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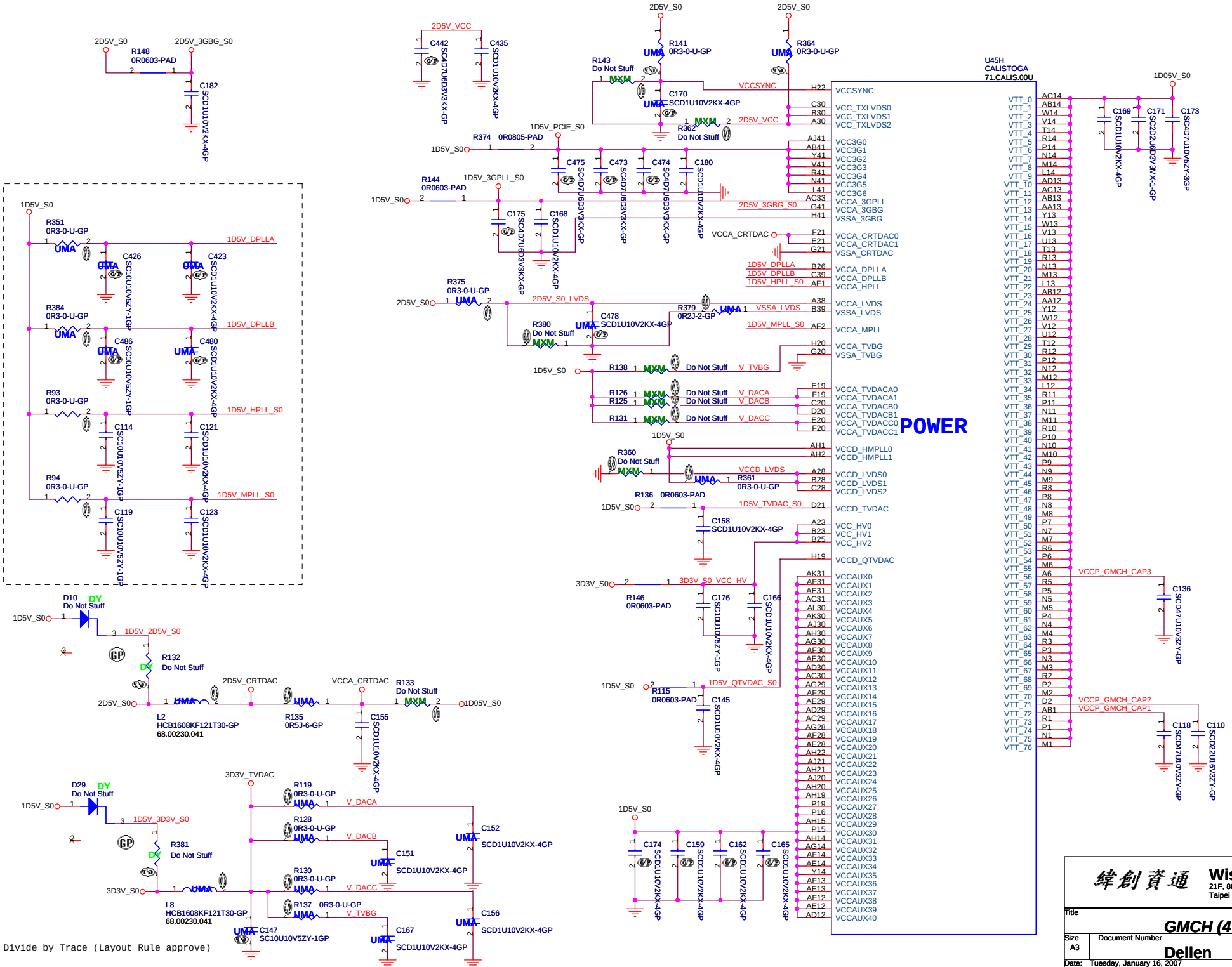
U45H
CALISTOGA
71.CALIS.00U
POWER
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
VCCP_GMCH_CAP3
VCCP_GMCH_CAP2
VCCP_GMCH_CAP1
2D5V_S0
2D5V_3GBG_S0
2D5V_VCC
1D5V_PCIE_S0
1D5V_3GPLL_S0
2D5V_3GBG_S0
2D5V_S0_LVDS
VSSA_LVDS
1D5V_MPLL_S0
V_TVBG
V_DACA
V_DACB
V_DACC
1D5V_TVDAC_S0
3D3V_S0_VCC_HV
1D5V_QTVDAC_S0
1D05V_S0
1D5V_DPLLA
1D5V_DPLLB
1D5V_HPLL_S0
1D5V_HPLL_S0
1D5V_MPLL_S0
1D5V_2D5V_S0
2D5V_CRTDAC
VCCA_CRTDAC
3D3V_TVDAC
1D5V_3D3V_S0
3D3V_S0
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Title
GMCH (4 of 5)
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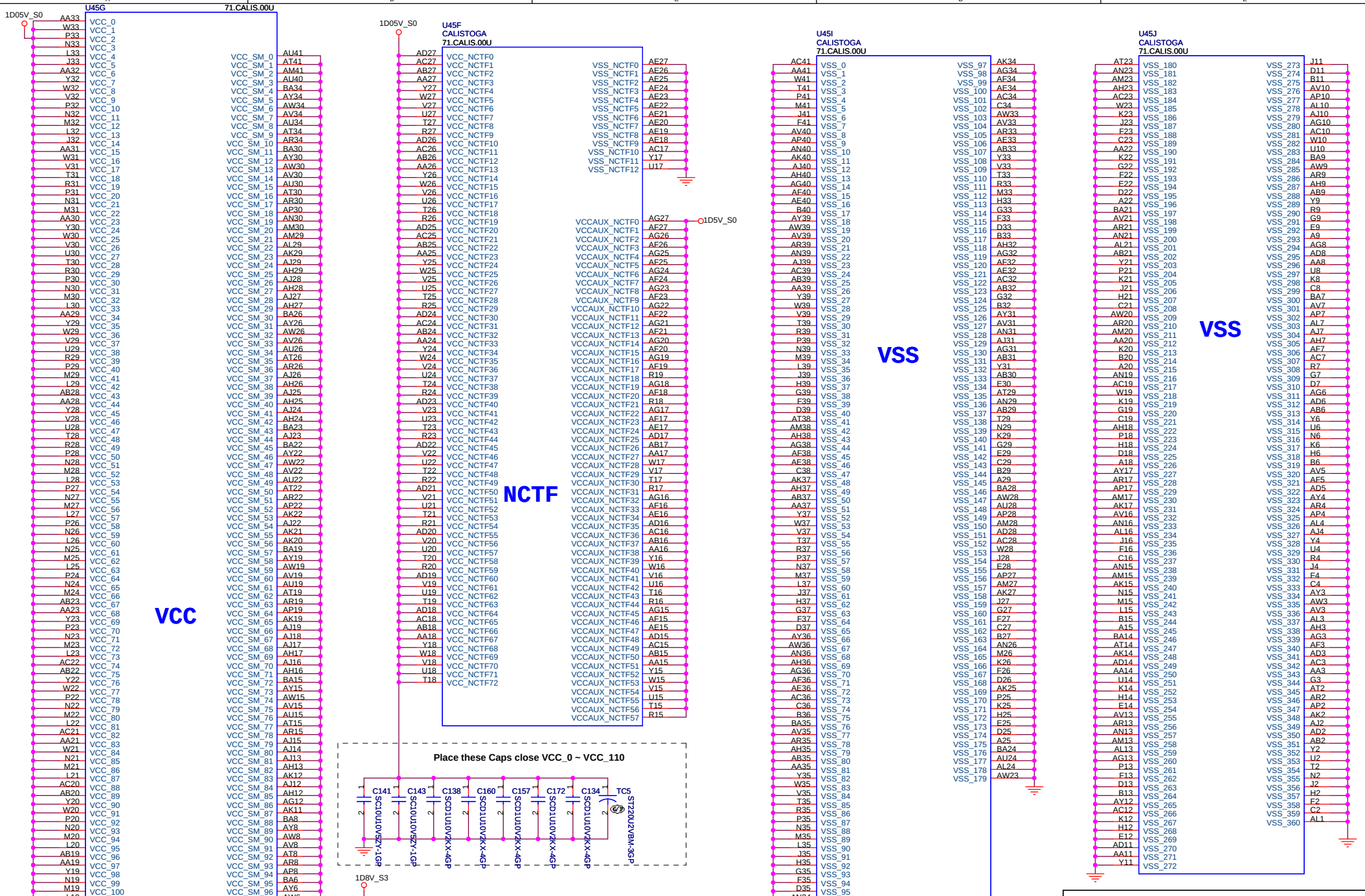
Divide by Trace (Layout Rule approve)



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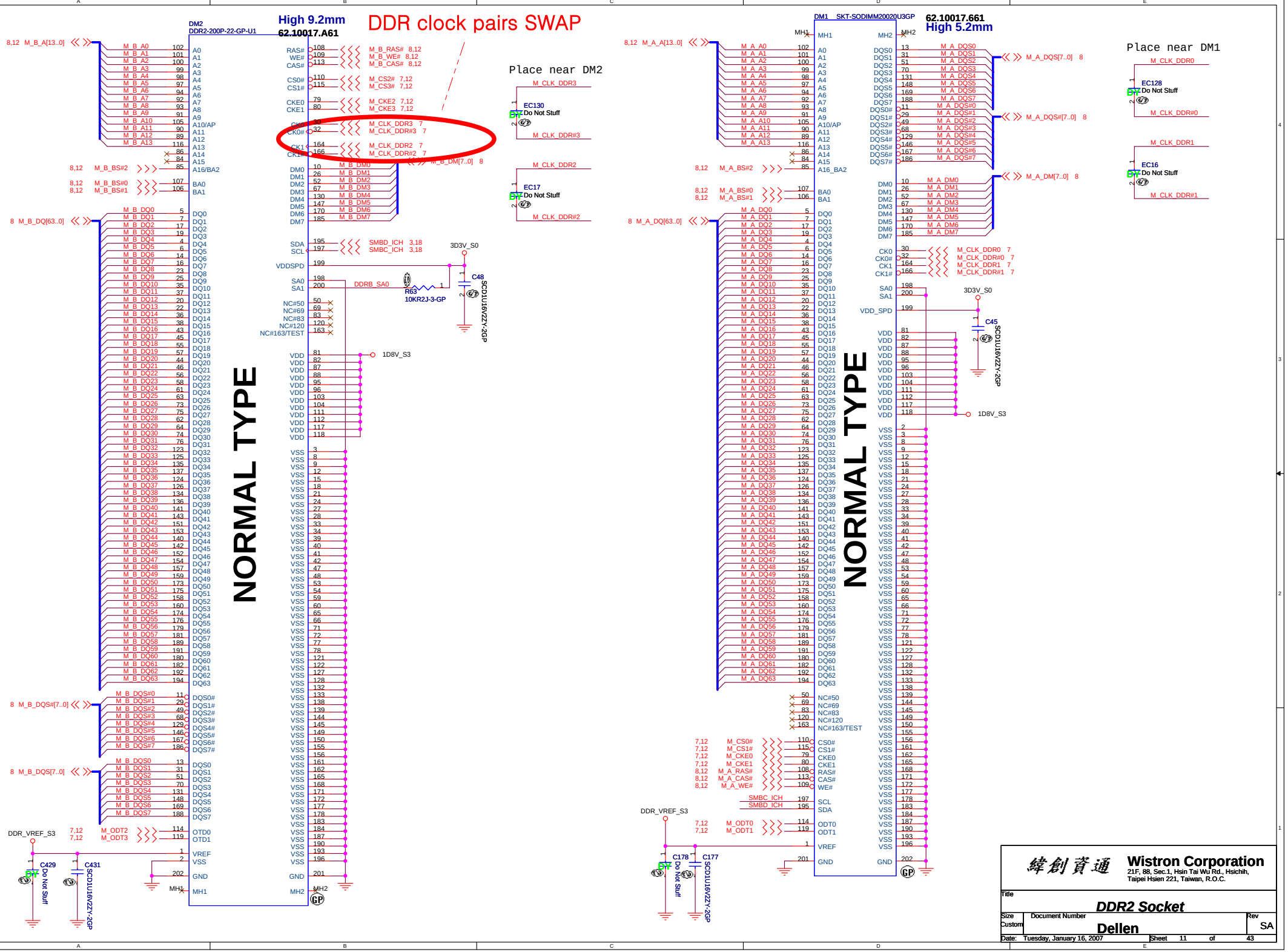
Title: **GMCH (5 of 5)**

Size: A3 | Document Number: **Dellen** | Rev: SA

Date: Tuesday, January 16, 2007 | Sheet 10 of 43


DDR clock pairs SWAP
High 9.2mm
62.10017.A61
DM2
DDR2-200P-22-GP-U1
NORMAL TYPE
Place near DM2
EC130
Do Not Stuff
EC17
Do Not Stuff
R63
10KR2J-3-GP
C48
SCD1U16V2Y-2GP
3D3V_S0
1D8V_S3
DDR_VREF_S3
C429
Do Not Stuff
C431
SCD1U16V2Y-2GP
DM1
SKT-SODIMM20020U3GP
62.10017.661
High 5.2mm
Place near DM1
EC128
Do Not Stuff
EC16
Do Not Stuff
C45
SCD1U16V2Y-2GP
C178
Do Not Stuff
C177
SCD1U16V2Y-2GP
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DDR2 Socket
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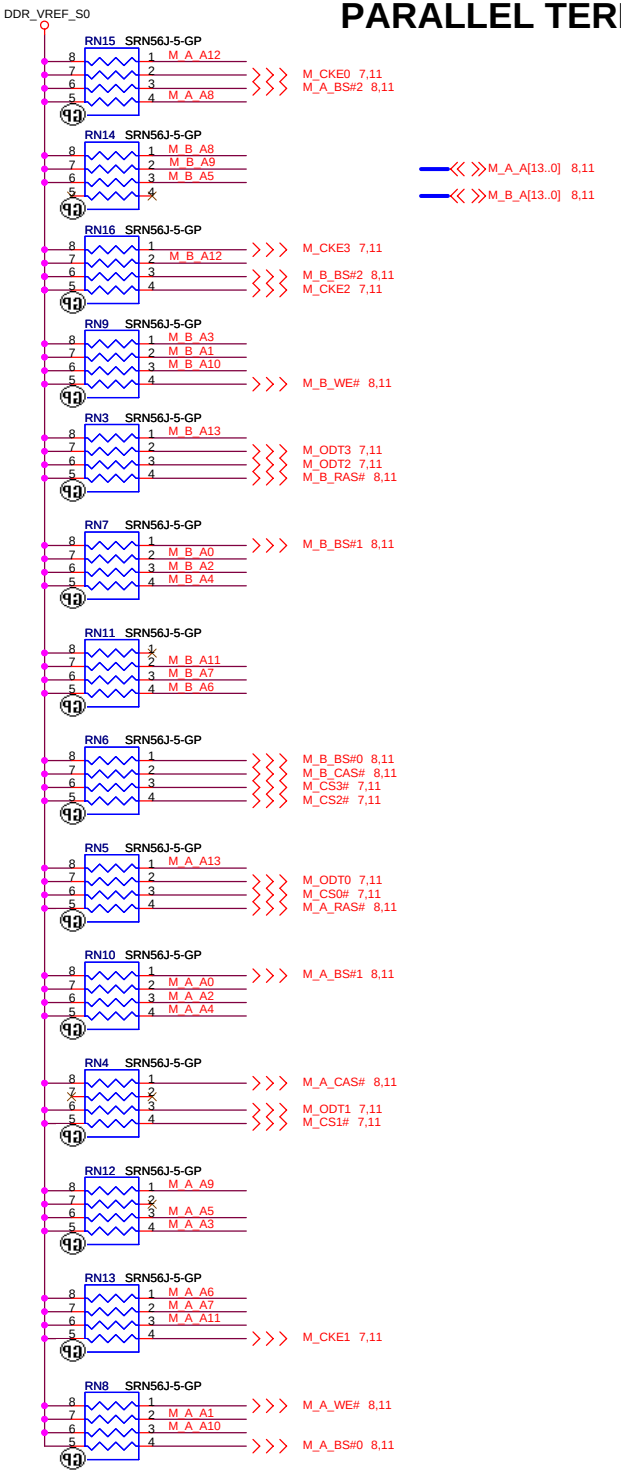
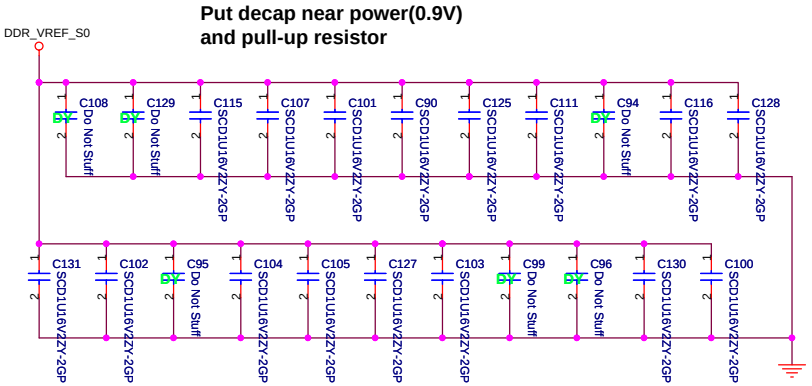
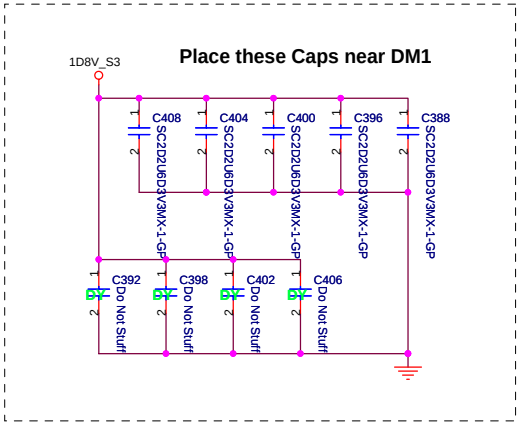
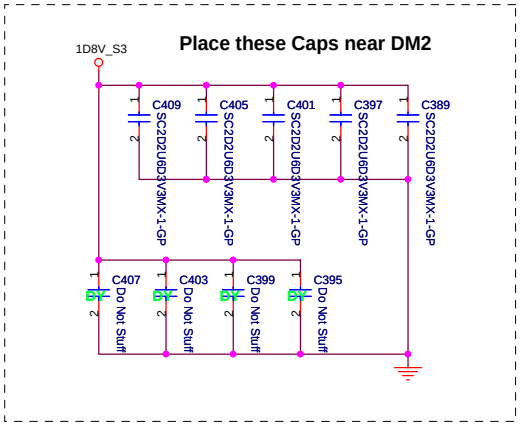
PARALLEL TERMINATION



Decoupling Capacitor







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Title: **DDR2 Termination Resistor**

Size	Document Number	Rev
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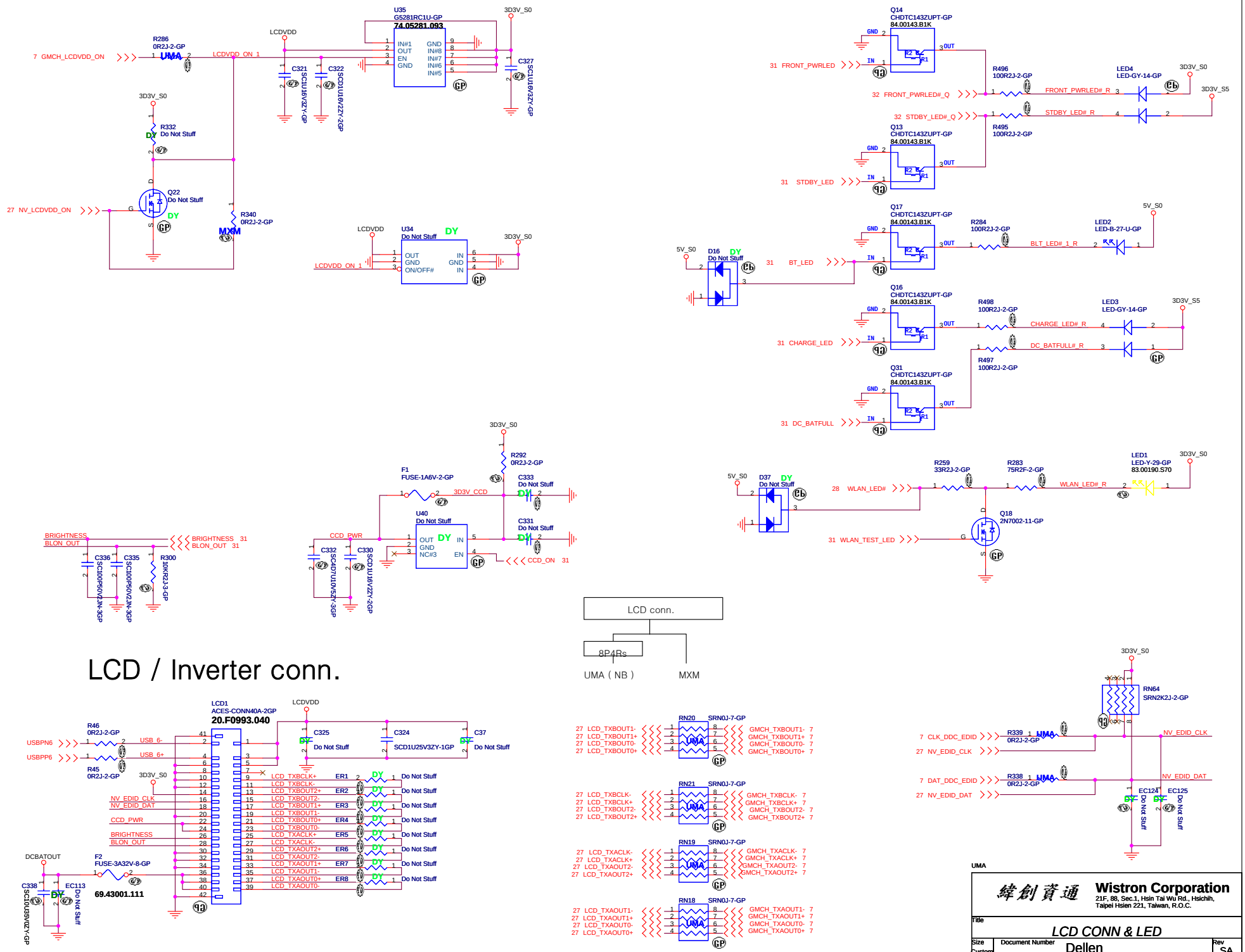
LCD / Inverter conn.
LCD conn.
8P4Rs
UMA (NB)
MXM
U35
G5281RC1U-GP
74.05281.093
R286
0R2J-2-GP
7 GMCH_LCDVDD_ON
LCDVDD_ON_1
LCDVDD
3D3V_S0
C321
SCD1U16V2ZY-GP
C322
SCD1U16V2ZY-2GP
C327
SCD1U16V2ZY-GP
R332
Do Not Stuff
Q22
Do Not Stuff
27 NV_LCDVDD_ON
R340
0R2J-2-GP
U34
Do Not Stuff
OUT
GND
ON/OFF#
IN
GND
IN
Q14
CHDTC143ZUPT-GP
84.00143.B1K
31 FRONT_PWRLED
R496
100R2J-2-GP
32 FRONT_PWRLED#_Q
FRONT_PWRLED#_R
LED4
LED-GY-14-GP
3D3V_S5
32 STDBY_LED#_Q
STDBY_LED#_R
R495
100R2J-2-GP
Q13
CHDTC143ZUPT-GP
84.00143.B1K
31 STDBY_LED
Q17
CHDTC143ZUPT-GP
84.00143.B1K
R284
100R2J-2-GP
LED2
LED-B-27-U-GP
5V_S0
BLT_LED#_1_R
5V_S0
D16
Do Not Stuff
31 BT_LED
Q16
CHDTC143ZUPT-GP
84.00143.B1K
R498
100R2J-2-GP
LED3
LED-GY-14-GP
3D3V_S5
31 CHARGE_LED
CHARGE_LED#_R
DC_BATFULL#_R
R497
100R2J-2-GP
Q31
CHDTC143ZUPT-GP
84.00143.B1K
31 DC_BATFULL
BRIGHTNESS
BLON_OUT
BRIGHTNESS 31
BLON_OUT 31
C336
SCD100P50V2JN-3GP
C335
SCD100P50V2JN-3GP
R300
10KR2J-3-GP
F1
FUSE-1A6V-2-GP
3D3V_S0
R292
0R2J-2-GP
3D3V_CCD
C333
Do Not Stuff
U40
Do Not Stuff
C331
Do Not Stuff
CCD_PWR
C332
SCD47U10V5ZY-3GP
C330
SCD1U16V2ZY-2GP
CCD_ON 31
5V_S0
D37
Do Not Stuff
28 WLAN_LED#
R259
33R2J-2-GP
R283
75R2F-2-GP
LED1
LED-Y-29-GP
83.00190.S70
WLAN_LED#_R
Q18
2N7002-11-GP
31 WLAN_TEST_LED
LCD1
ACES-CONN40A-2GP
20.F0993.040
R46
0R2J-2-GP
16 USBPN6
USB_6-
16 USBPP6
USB_6+
R45
0R2J-2-GP
C325
Do Not Stuff
C324
SCD1U25V3ZY-1GP
C37
Do Not Stuff
NV_EDID_CLK
NV_EDID_DAT
CCD_PWR
BRIGHTNESS
BLON_OUT
LCD_TXBCLK+
LCD_TXBCLK-
LCD_TXBOUT2+
LCD_TXBOUT2-
LCD_TXBOUT1+
LCD_TXBOUT1-
LCD_TXBOUT0+
LCD_TXBOUT0-
LCD_TXACLK+
LCD_TXACLK-
LCD_TXAOUT2+
LCD_TXAOUT2-
LCD_TXAOUT1+
LCD_TXAOUT1-
LCD_TXAOUT0+
LCD_TXAOUT0-
ER1
ER2
ER3
ER4
ER5
ER6
ER7
ER8
Do Not Stuff
DCBATOUT
F2
FUSE-3A32V-8-GP
69.43001.111
C338
SCD1U35V2ZY-GP
EC113
Do Not Stuff
RN20
SRN0J-7-GP
27 LCD_TXBOUT1-
27 LCD_TXBOUT1+
27 LCD_TXBOUT0-
27 LCD_TXBOUT0+
GMCH_TXBOUT1-
GMCH_TXBOUT1+
GMCH_TXBOUT0-
GMCH_TXBOUT0+
RN21
SRN0J-7-GP
27 LCD_TXBCLK-
27 LCD_TXBCLK+
27 LCD_TXBOUT2-
27 LCD_TXBOUT2+
GMCH_TXBCLK-
GMCH_TXBCLK+
GMCH_TXBOUT2-
GMCH_TXBOUT2+
RN19
SRN0J-7-GP
27 LCD_TXACLK-
27 LCD_TXACLK+
27 LCD_TXAOUT2-
27 LCD_TXAOUT2+
GMCH_TXACLK-
GMCH_TXACLK+
GMCH_TXAOUT2-
GMCH_TXAOUT2+
RN18
SRN0J-7-GP
27 LCD_TXAOUT1-
27 LCD_TXAOUT1+
27 LCD_TXAOUT0-
27 LCD_TXAOUT0+
GMCH_TXAOUT1-
GMCH_TXAOUT1+
GMCH_TXAOUT0-
GMCH_TXAOUT0+
RN64
SRN2K2J-2-GP
7 CLK_DDC_EDID
27 NV_EDID_CLK
R339
0R2J-2-GP
NV_EDID_CLK
7 DAT_DDC_EDID
27 NV_EDID_DAT
R338
0R2J-2-GP
NV_EDID_DAT
EC124
EC125
Do Not Stuff
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
LCD CONN & LED
Size
Custom
Document Number
Dellen
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SA
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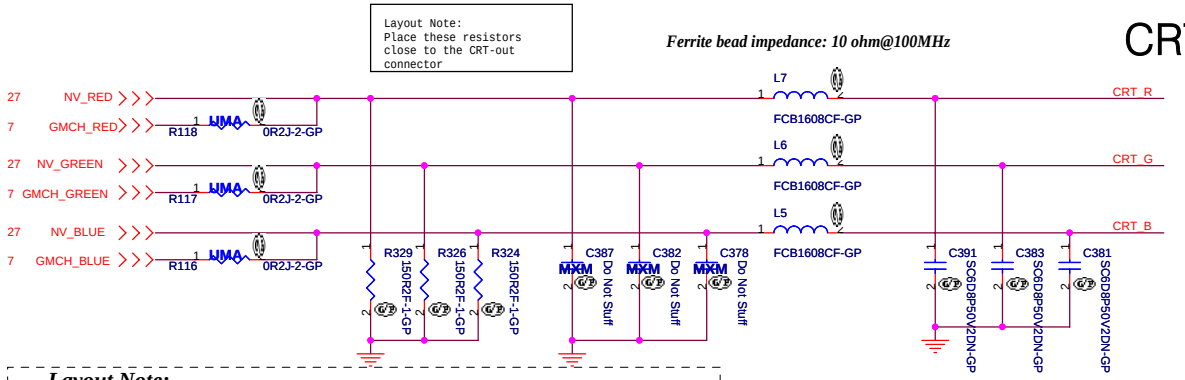
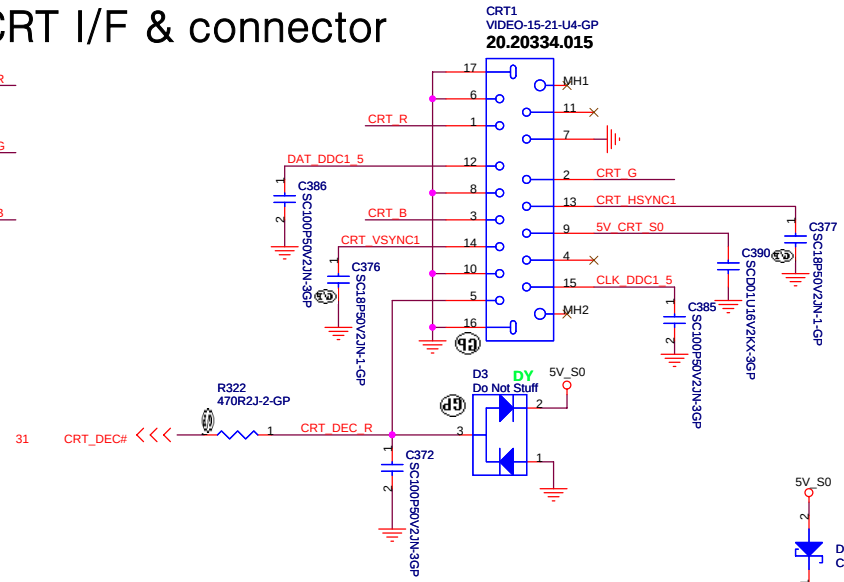
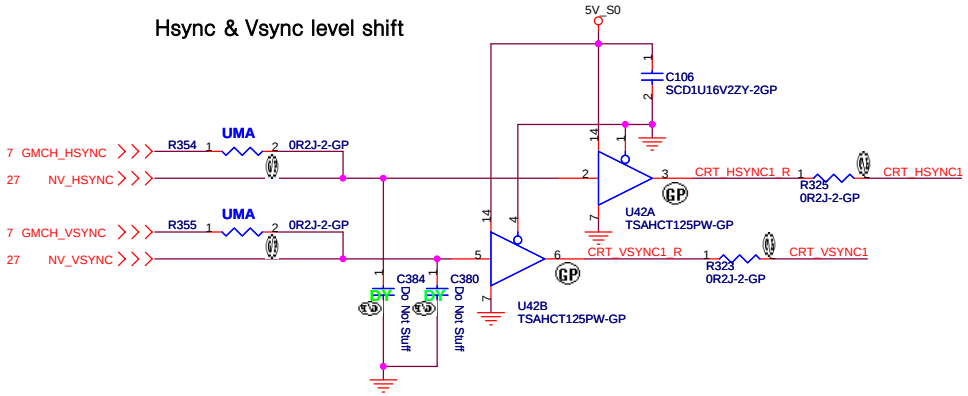
CRT I/F & connector



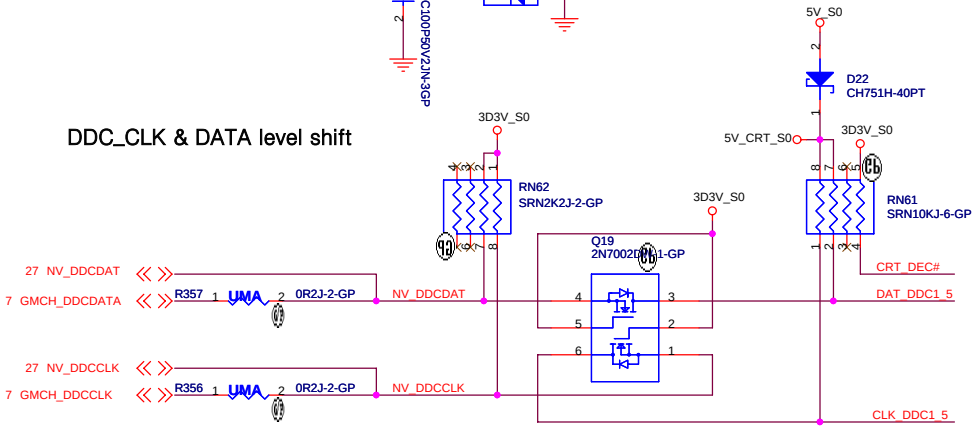


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

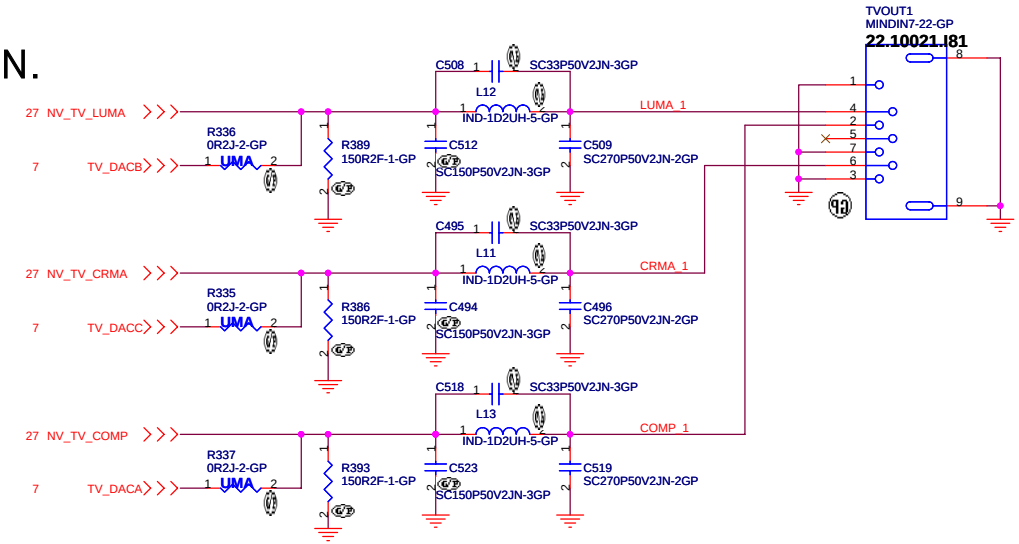
Hsync & Vsync level shift

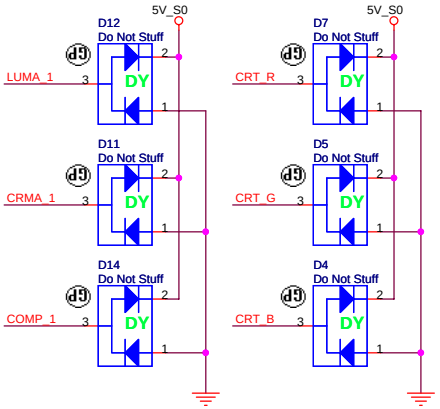


DDC_CLK & DATA level shift



TV CONN.





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Title: CRT/TV Connector

Size: A3 | Document Number: Dellen | Rev: SA

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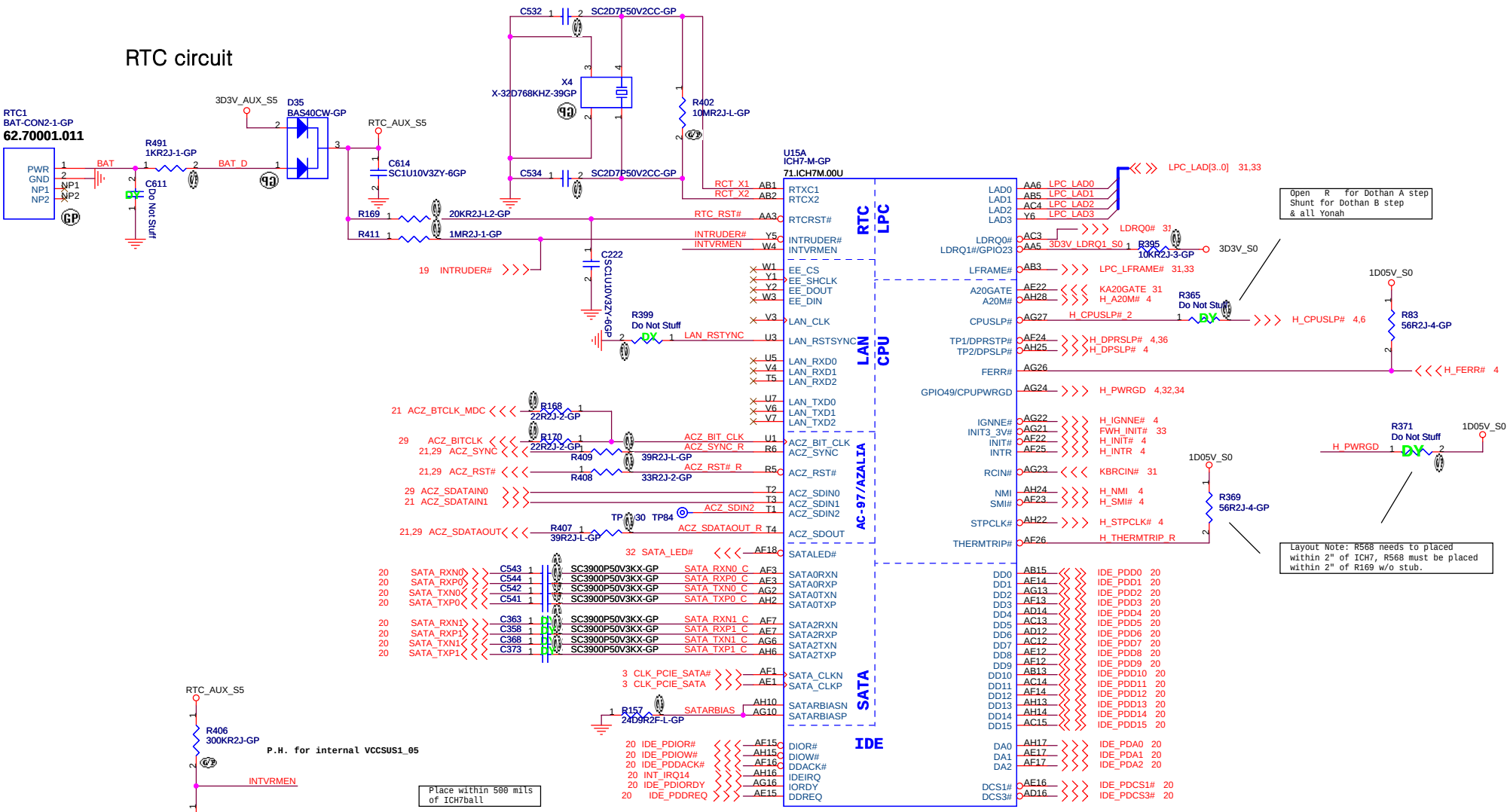
RTC circuit



	INTVRMEN
Enable	1
Disable	0

Placement Note:
Diatance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.

UMA

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Title: *ICH7-M (1 of 4)*

Size: A3 | Document Number: Dellen | Rev: SA

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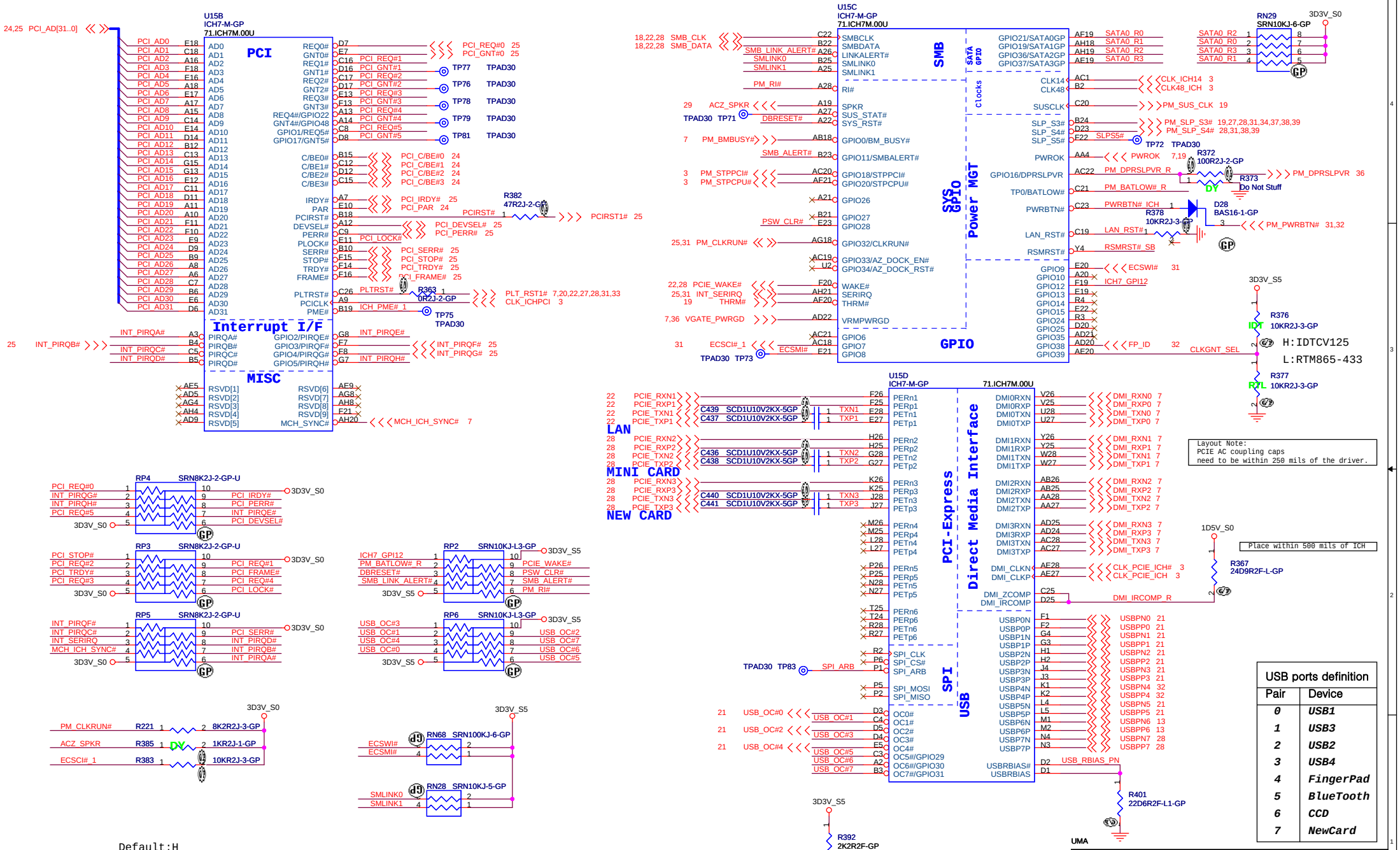
U15B
ICH7-M-GP
71.ICH7M.00U
PCI
Interrupt I/F
MISC
U15C
ICH7-M-GP
71.ICH7M.00U
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
U15D
ICH7-M-GP
71.ICH7M.00U
PCI-Express
Direct Media Interface
SPI
USB
LAN
MINI CARD
NEW CARD
H:IDTCV125
L:RTM865-433
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
USB ports definition
Pair Device
0 USB1
1 USB3
2 USB2
3 USB4
4 FingerPad
5 BlueTooth
6 CCD
7 NewCard
Default:H
GNT5# GNT4#
LPC H H
PCI H L
SPI L H
GAP放在Dimm Door打開可量測處
GAP-OPEN
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (2 of 4)
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Document Number
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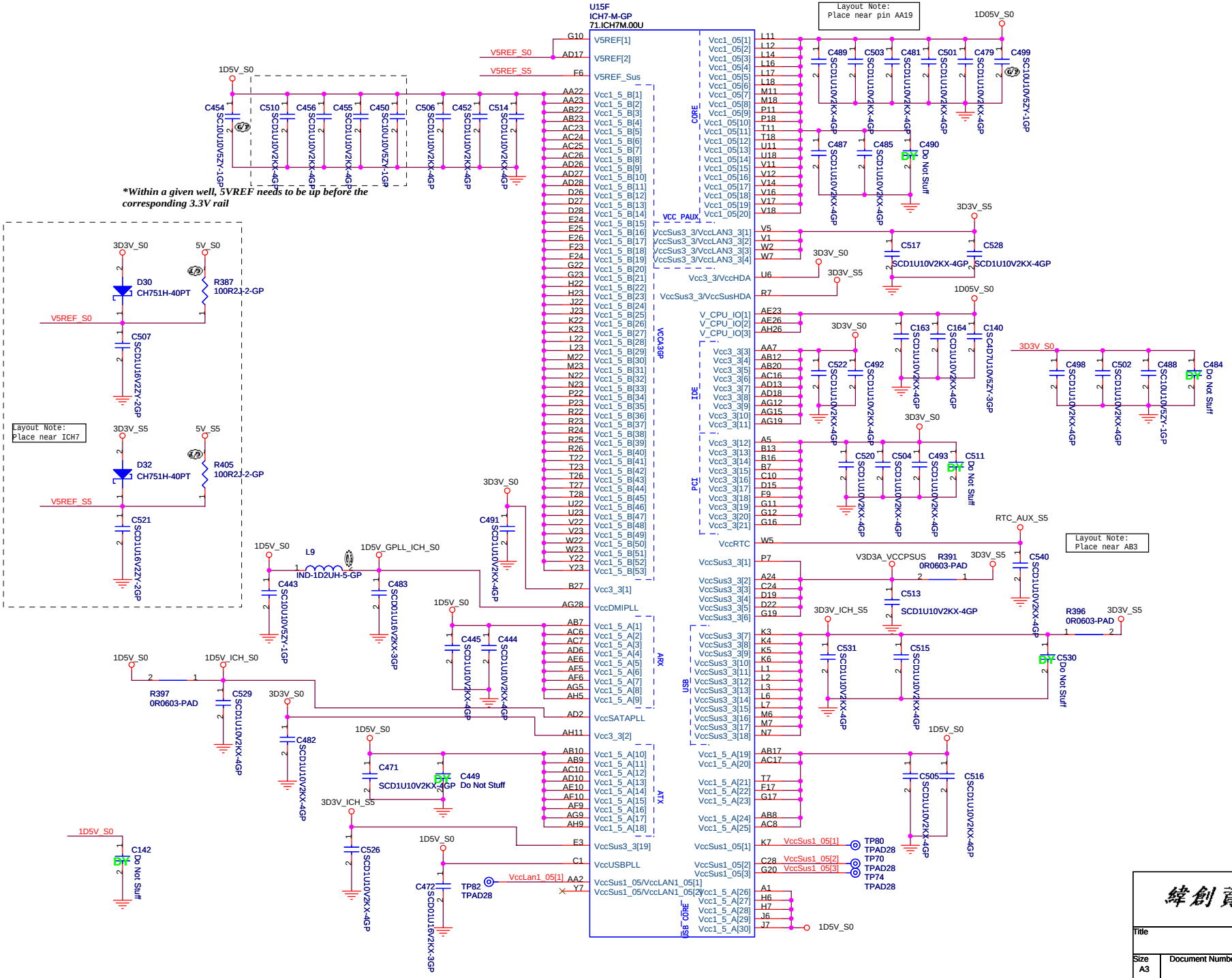

Wistron Corporation
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Title: ICH7-M (3 of 4)

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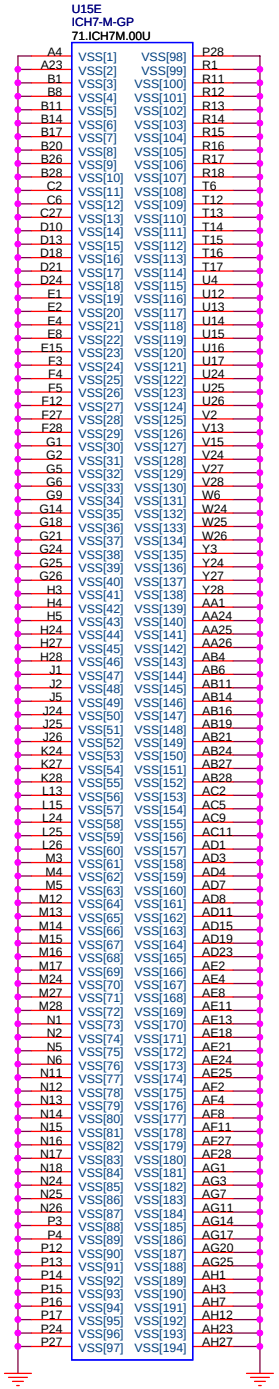
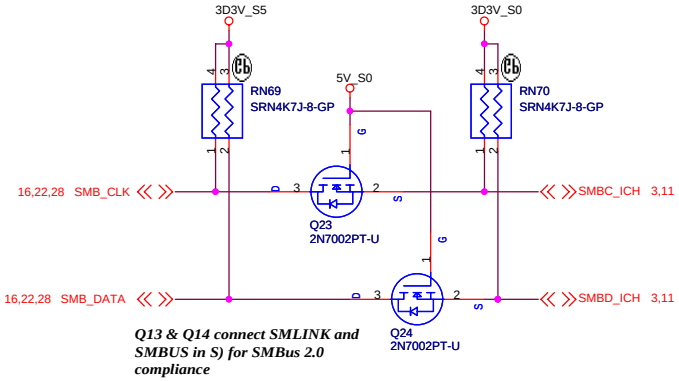


SMBUS



Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

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Title	***ICH7-M (4 of 4)***	
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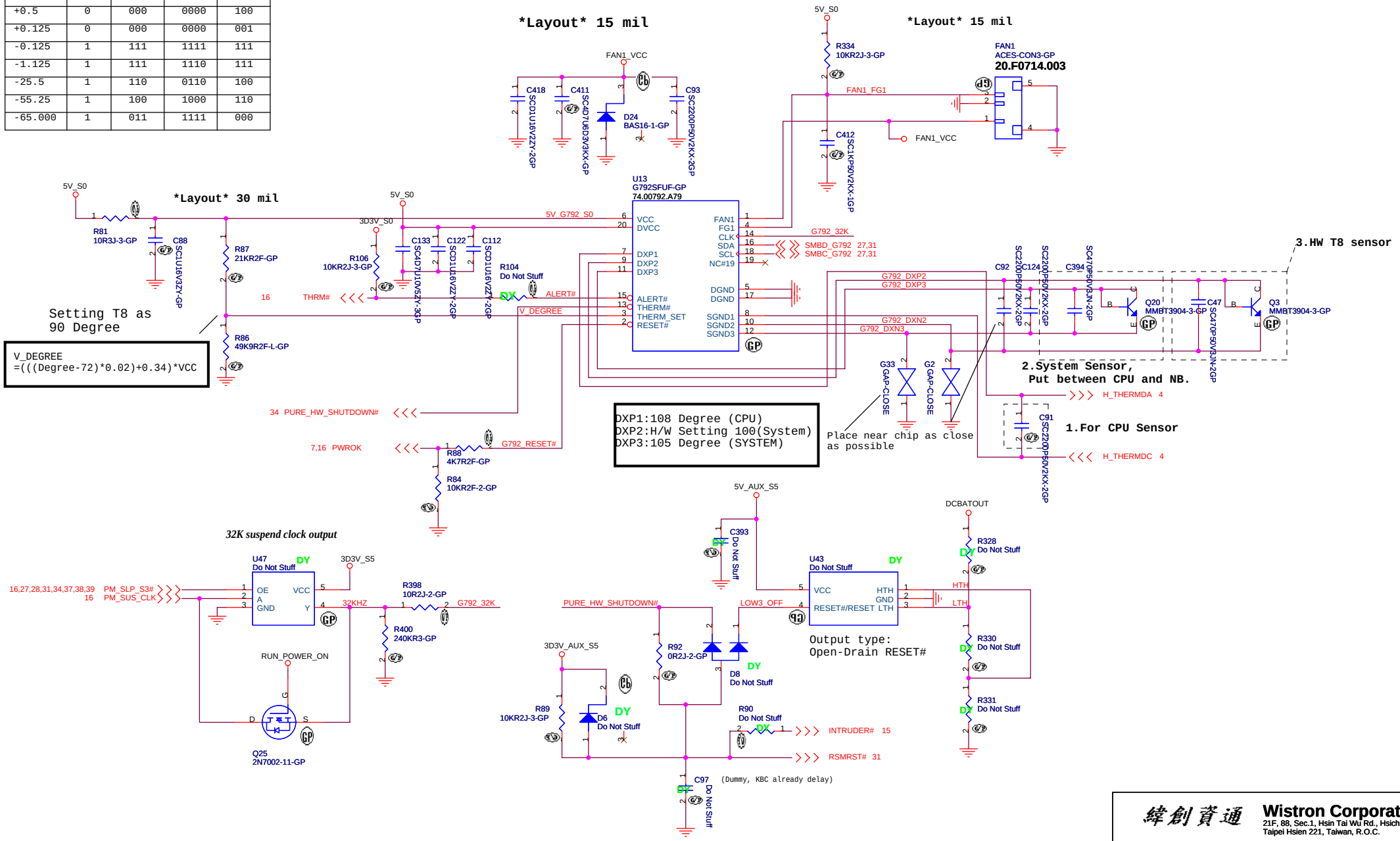
TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



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Title: ***Thermal / Fan Controllor***

Size: A3 | Document Number: **Dellen** | Rev: SA

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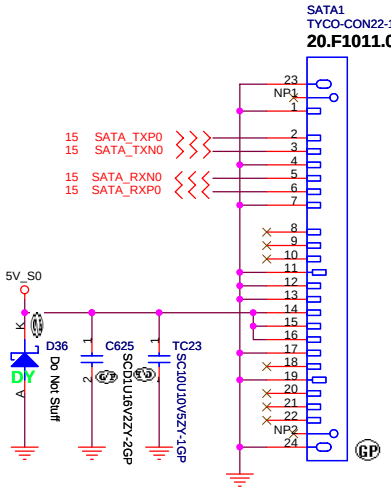
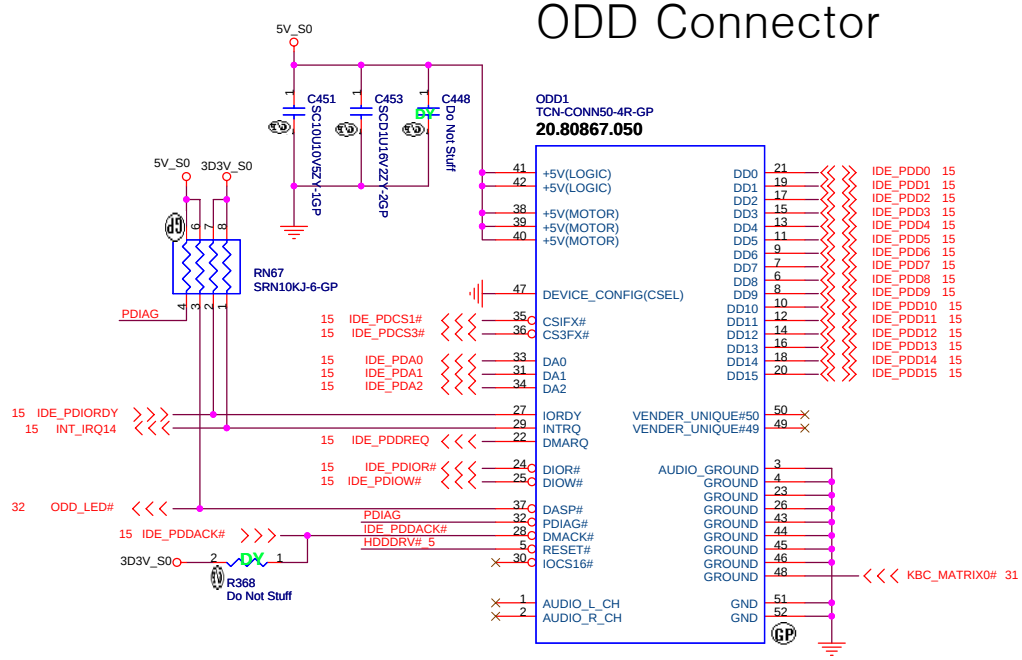
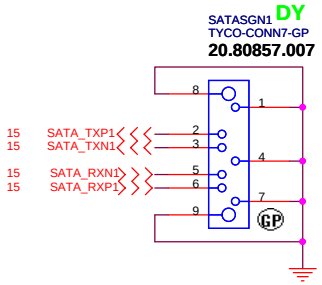
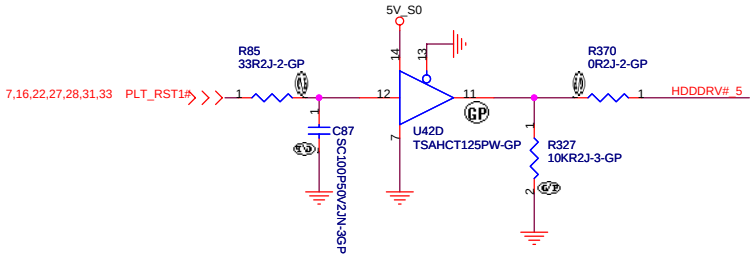
SATA HD Connector

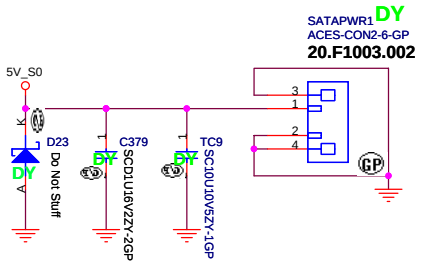


ODD Connector









UMA

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Title: ***HDD and CDROM***

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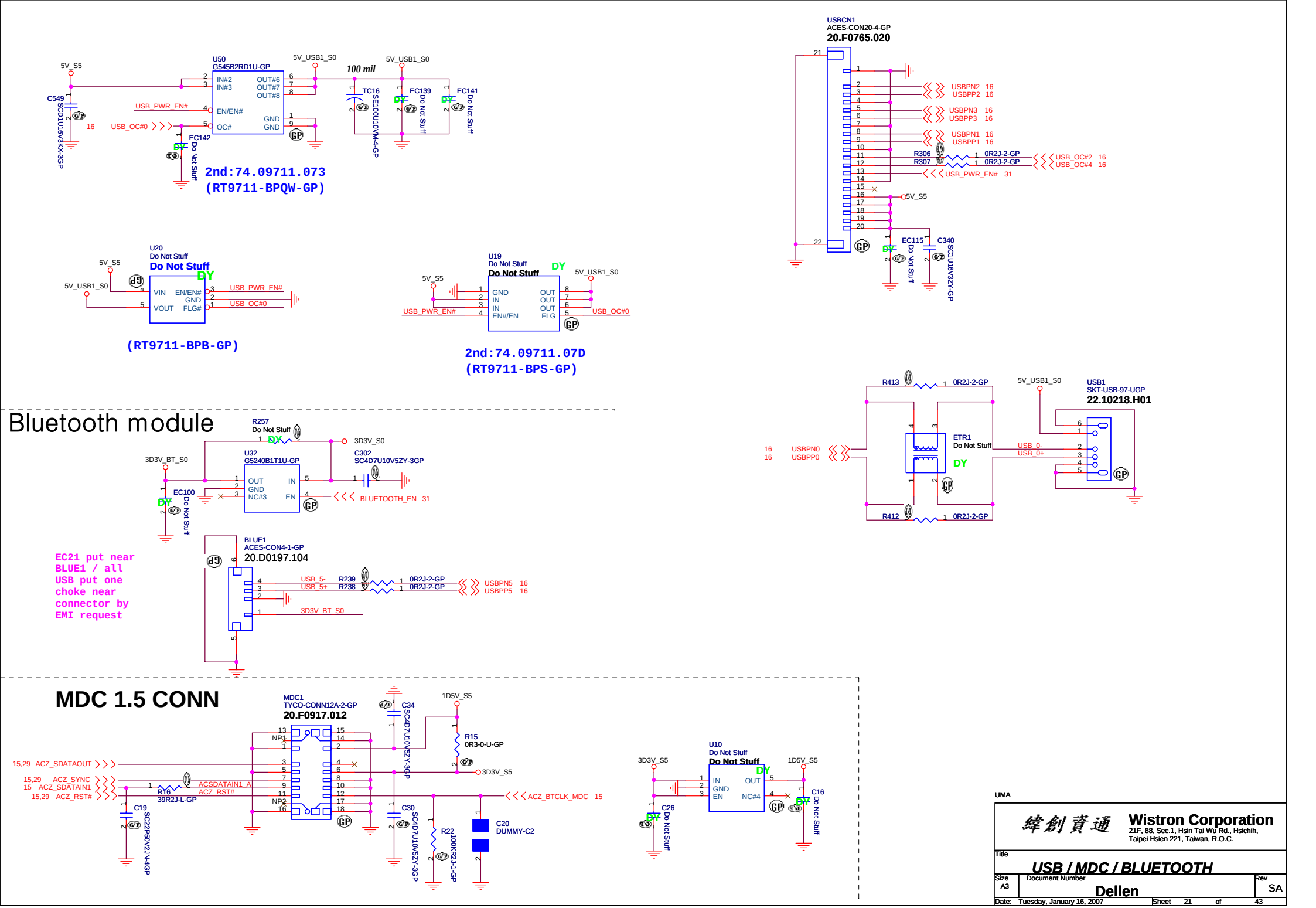
U50
G545B2RD1U-GP
2nd:74.09711.073
(RT9711-BPQW-GP)
100 mil
USBCN1
ACES-CON20-4-GP
20.F0765.020
U20
Do Not Stuff
(RT9711-BPB-GP)
U19
Do Not Stuff
2nd:74.09711.07D
(RT9711-BPS-GP)
Bluetooth module
U32
G5240B1T1U-GP
BLUE1
ACES-CON4-1-GP
20.D0197.104
EC21 put near BLUE1 / all USB put one choke near connector by EMI request
ETR1
Do Not Stuff
USB1
SKT-USB-97-UGP
22.10218.H01
MDC 1.5 CONN
MDC1
TYCO-CONN12A-2-GP
20.F0917.012
U10
Do Not Stuff
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
USB / MDC / BLUETOOTH
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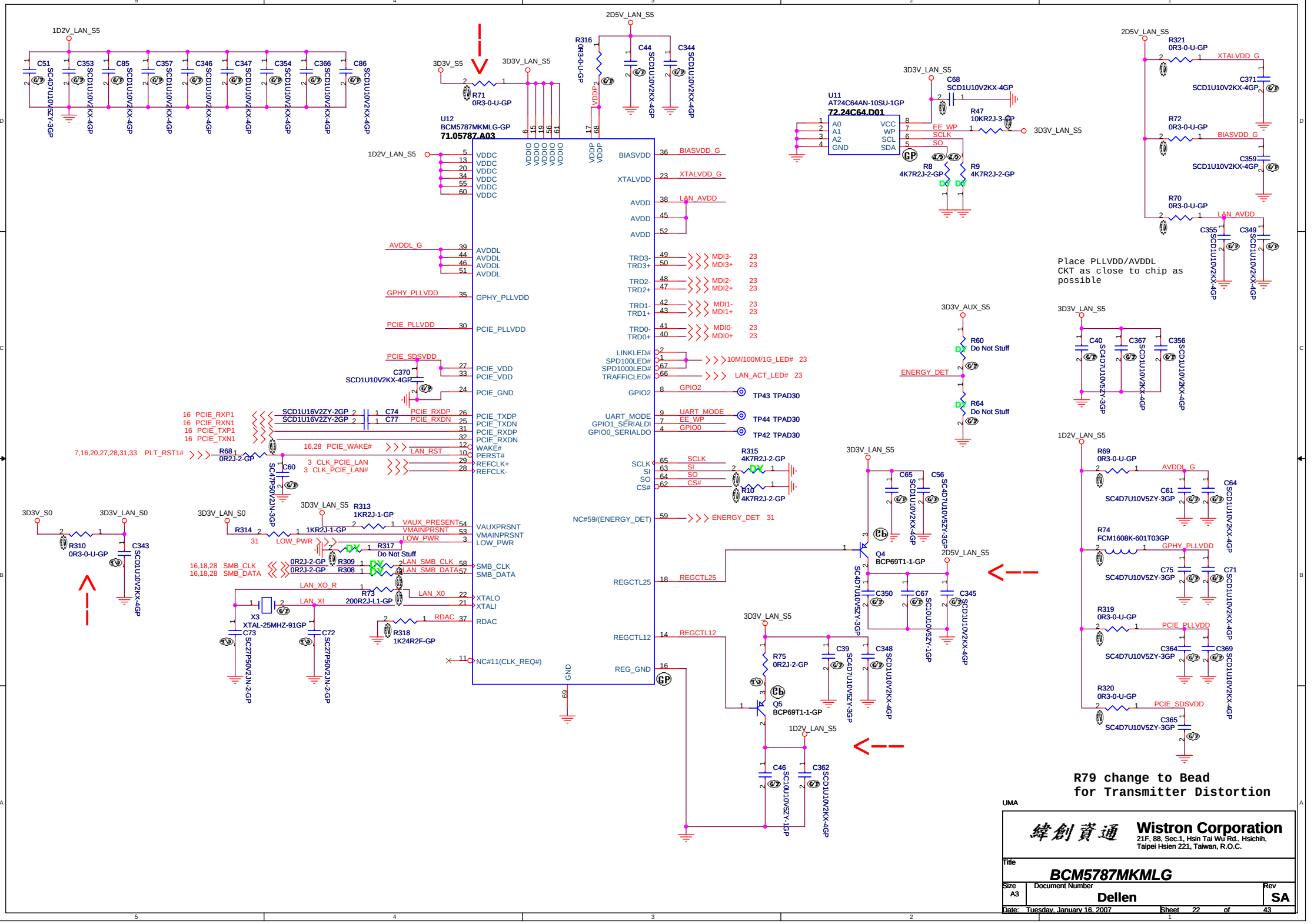
U12
BCM5787MKMLG-GP
71.05787.A03
U11
AT24C64AN-10SU-1GP
72.24C64.D01
Place PLLVDD/AVDDL
CKT as close to chip as
possible
R79 change to Bead
for Transmitter Distortion
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5787MKMLG
Size
A3
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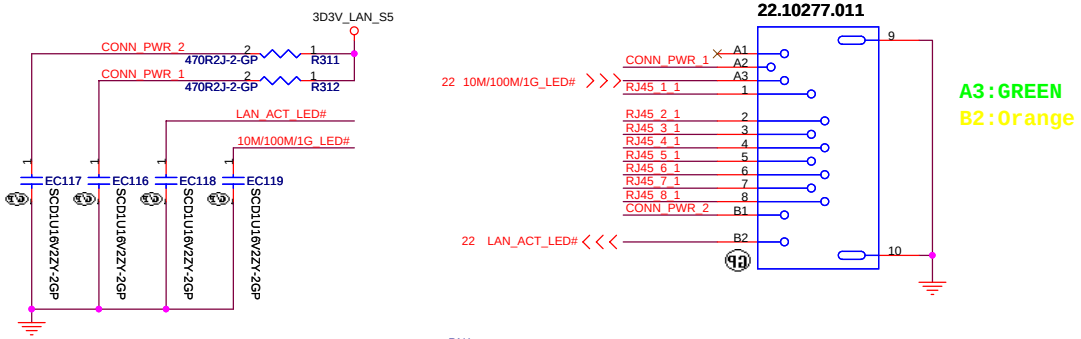
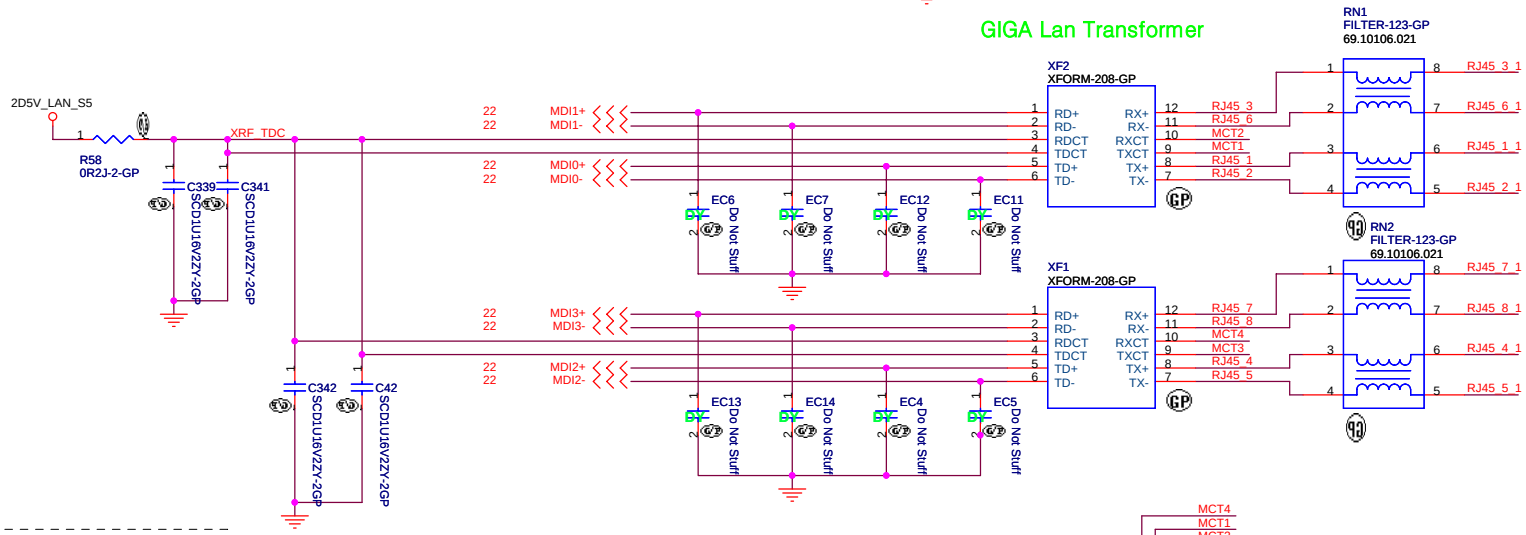
LAN Connector

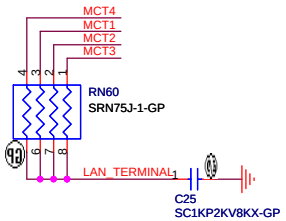
Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	





LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

UMA

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Title: **LAN Connector**

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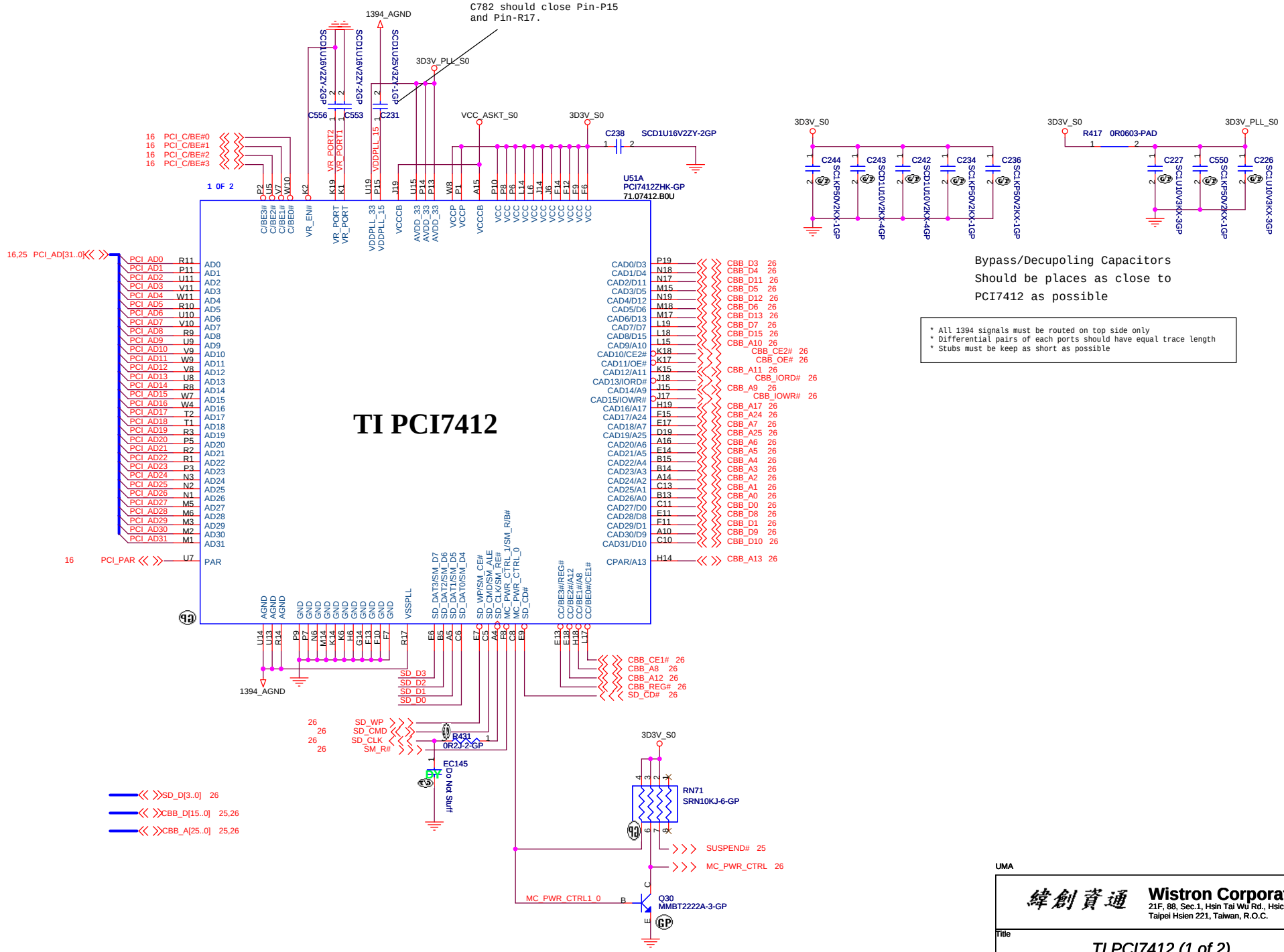
C782 should close Pin-P15
and Pin-R17.
1394_AGND
3D3V_PLL_S0
VCC_ASKT_S0
3D3V_S0
SCD1U16V2ZY-2GP
C238
U51A
PCI7412ZHK-GP
71.07412.B0U
1 0F 2
TI PCI7412
16,25 PCI_AD[31..0]
16 PCI_PAR
16 PCI_C/BE#0
16 PCI_C/BE#1
16 PCI_C/BE#2
16 PCI_C/BE#3
CBB_CE1# 26
CBB_A8 26
CBB_A12 26
CBB_REG# 26
SD_CD# 26
SD_D3
SD_D2
SD_D1
SD_D0
SD_WP
SD_CMD
SD_CLK
SM_R#
R431
0R2J-2-GP
EC145
Do Not Stuff
RN71
SRN10KJ-6-GP
SUSPEND# 25
MC_PWR_CTRL 26
MC_PWR_CTRL1_0
Q30
MMBT2222A-3-GP
SD_D[3..0] 26
CBB_D[15..0] 25,26
CBB_A[25..0] 25,26
R417
0R0603-PAD
Bypass/Decupoling Capacitors
Should be places as close to
PCI7412 as possible
* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TI PCI7412 (1 of 2)
Size A3
Document Number
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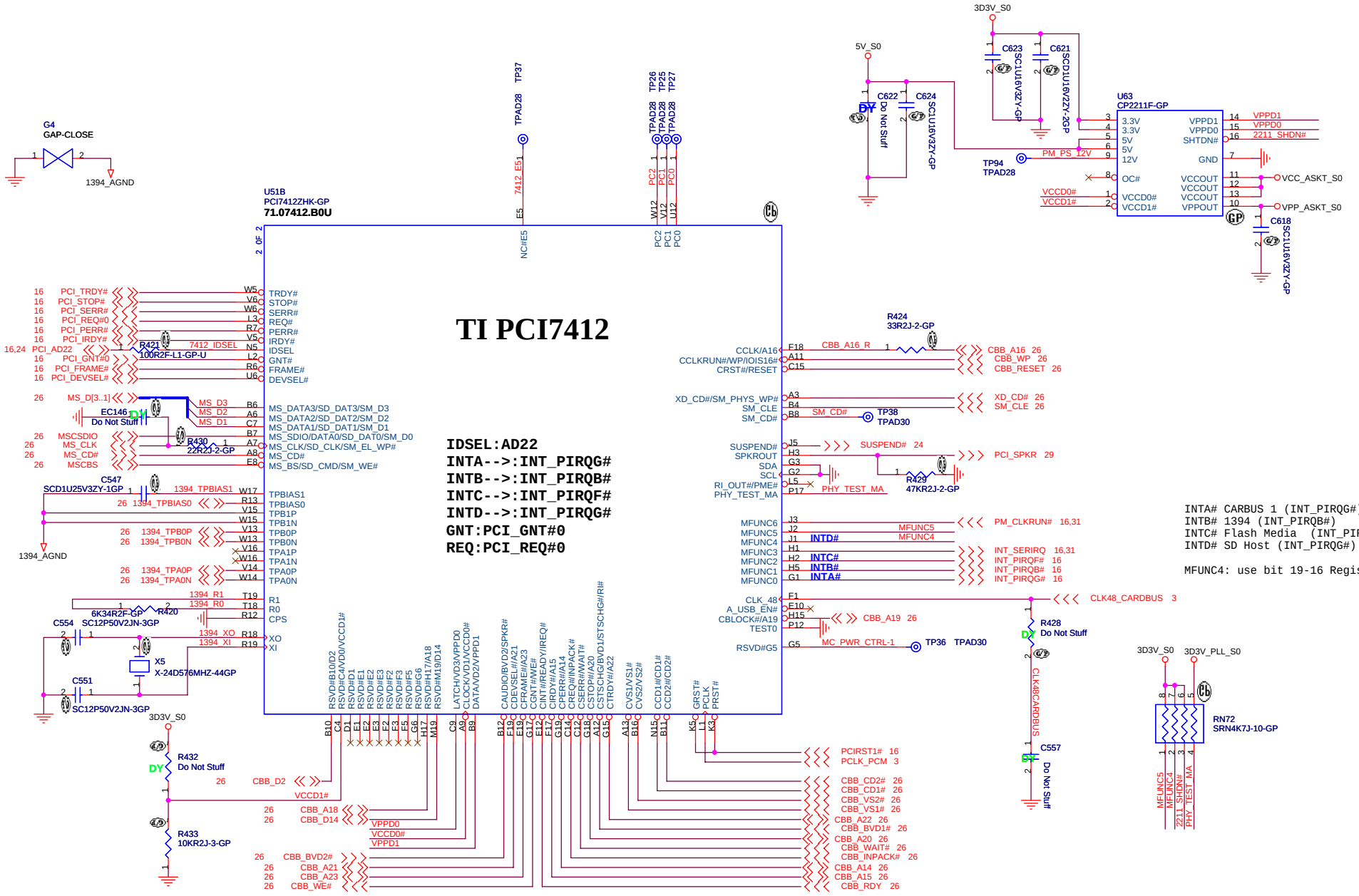
TI PCI7412
U51B
PCI7412ZHK-GP
71.07412.B0U
2 OF 2
IDSEL:AD22
INTA-->:INT_PIRQG#
INTB-->:INT_PIRQB#
INTC-->:INT_PIRQF#
INTD-->:INT_PIRQG#
GNT:PCI_GNT#0
REQ:PCI_REQ#0
U63
CP2211F-GP
G4
GAP-CLOSE
1394_AGND
3D3V_S0
5V_S0
3D3V_PLL_S0
TP94
TPAD28
TP38
TPAD30
TP36
TPAD30
X5
X-24D576MHZ-44GP
RN72
SRN4K7J-10-GP
R424
33R2J-2-GP
R429
47KR2J-2-GP
R428
Do Not Stuff
C557
Do Not Stuff
R432
Do Not Stuff
R433
10KR2J-3-GP
R421
100R2F-L1-GP-U
R430
22R2J-2-GP
EC146
Do Not Stuff
C547
SCD1U25V3ZY-1GP
R420
6K34R2F-GP
C554
SC12P50V2JN-3GP
C551
SC12P50V2JN-3GP
C622
Do Not Stuff
C624
SC1U16V3ZY-GP
C623
SC1U16V3ZY-GP
C621
SCD1U16V2ZY-2GP
C618
SC1U16V3ZY-GP
VCC_ASKT_S0
VPP_ASKT_S0
CLK48_CARDBUS
INTA# CARBUS 1 (INT_PIRQG#)
INTB# 1394 (INT_PIRQB#)
INTC# Flash Media (INT_PIRQF#)
INTD# SD Host (INT_PIRQG#) share
MFUNC4: use bit 19-16 Register define.
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TI PCI7412 (2 of 2)
Size
A3
Document Number
Dellen
Rev
SA
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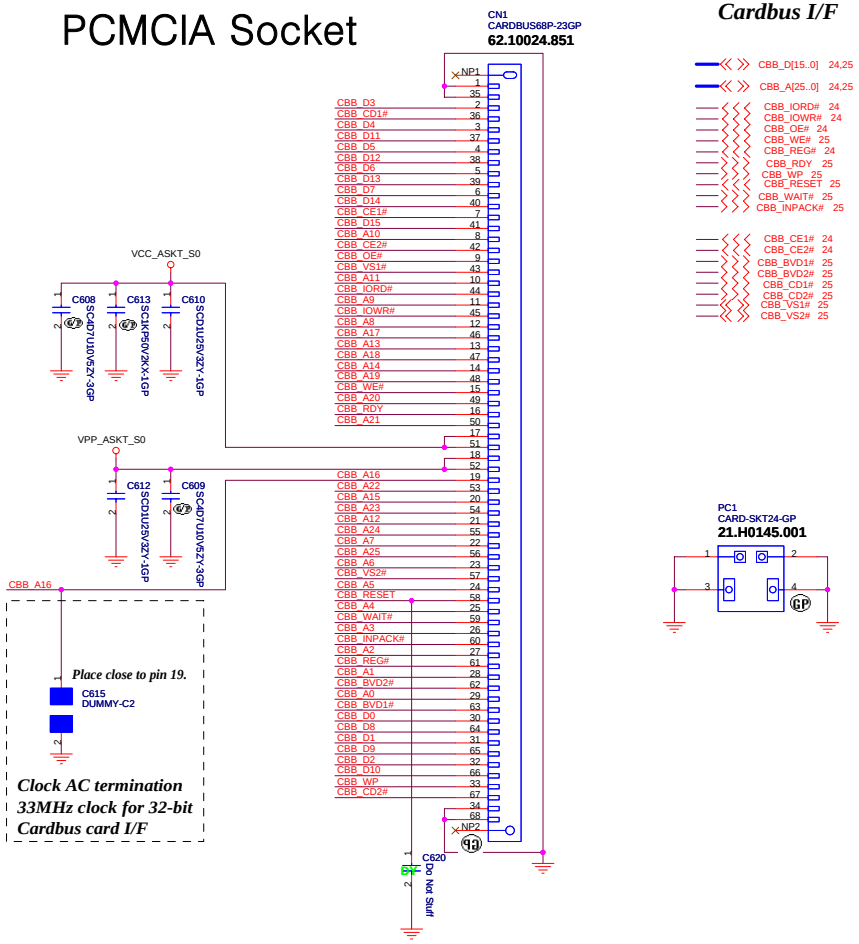
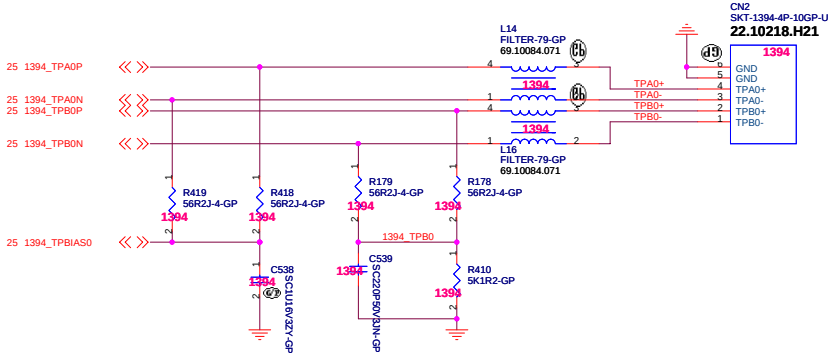
Sheet 25 of 43

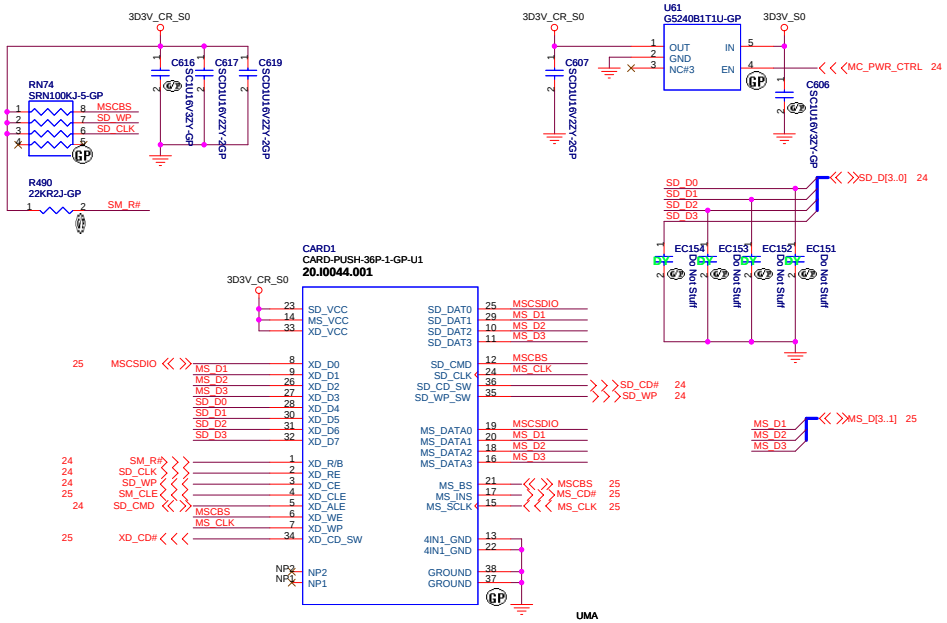
PCMCIA Socket



Cardbus I/F

1394 Connector





XD
MS / MS PRO
SD / SD IO / MMC

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCMCIA / 1394 / CARD READER	
Size Custom	Document Number Dellen	Rev SA
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NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

7 PEG_TXP[15..0]
7 PEG_TXN[15..0]
7 PEG_RXP[15..0]
7 PEG_RXN[15..0]

13 LCD_TXBOUT0+
13 LCD_TXBOUT0-
13 LCD_TXBOUT1+
13 LCD_TXBOUT1-
13 LCD_TXBOUT2+
13 LCD_TXBOUT2-
13 LCD_TXBCLK+
13 LCD_TXBCLK-
14 NV_BLUE
14 NV_GREEN
14 NV_RED
14 NV_TV_COMP
14 NV_TV_LUMA
14 NV_TV_CRMA

LCD_TXACLK- 13
LCD_TXACLK+ 13
LCD_TXAOUT2- 13
LCD_TXAOUT2+ 13
LCD_TXAOUT1- 13
LCD_TXAOUT1+ 13
LCD_TXAOUT0- 13
LCD_TXAOUT0+ 13
NV_EDID_DAT 13
NV_EDID_CLK 13
NV_LCDVDD_ON 13
NV_BLON 31
NV_DVI_DAT 42
NV_DVI_CLK 42

36,37,38,39 CPUCORE_ON
16,19,28,31,34,37,38,39 PM_SLP_S3#
1D8V_S3
5V_S0
DCBATOUT
2D5V_S0
3D3V_S0

R343 Do Not Stuff
R333 Do Not Stuff
C416 Do Not Stuff
C420 Do Not Stuff
C419 Do Not Stuff
C434 Do Not Stuff
C433 Do Not Stuff
C432 Do Not Stuff
C427 Do Not Stuff
C430 Do Not Stuff
R113 Do Not Stuff
C417 Do Not Stuff
C415 Do Not Stuff
MXM1 Do Not Stuff
MXM Do Not Stuff

TP49 TPAD30
TP12 TPAD30
TP48 TP51 TPAD30 TPAD30
TP50 TP47 TPAD30 TPAD30
TPAD30 TP46
TP15 TPAD30
TP59 TPAD30

3 CLK_PCIE_PEG#
3 CLK_PCIE_PEG

7,16,20,22,28,31,33 PLT_RST1#
R359 Do Not Stuff
PLT_RST1#_MXM
C428 Do Not Stuff

19,31 SMBD_G792
19,31 SMBC_G792
R139 Do Not Stuff
R358 Do Not Stuff
SMBD_MXM
SMBC_MXM

34 MXM_THER
14 NV_HSYNC
14 NV_VSYNC
14 NV_DDCCLK
14 NV_DDCDAT

TPAD30 TP17 SPDIF_HDMI
TPAD30 TP63 GPU_BUFRST#
TPAD30 TP67 MP_INT
TPAD30 TP65 GPU_PRGM#

TPAD30 TP56 IGP_UTX2#
TPAD30 TP57 IGP_UTX2
TPAD30 TP60 TMDS_GPIO6_SW
TPAD30 TP19

EMI REQUEST

TMDS_A_TX0+ 1 — ERN4 — 4 — TMDS_A_TX0+ 42
TMDS_A_TX0- 1 — 3 — TMDS_A_TX0- 42
Do Not Stuff
TMDS_A_TX1+ 1 — ERN3 — 4 — TMDS_A_TX1+ 42
TMDS_A_TX1- 1 — 3 — TMDS_A_TX1- 42
Do Not Stuff
TMDS_A_TX2+ 1 — ERN2 — 4 — TMDS_A_TX2+ 42
TMDS_A_TX2- 1 — 3 — TMDS_A_TX2- 42
Do Not Stuff
TMDS_A_TXC+ 1 — ERN1 — 4 — TMDS_A_TXC+ 42
TMDS_A_TXC- 1 — 3 — TMDS_A_TXC- 42
Do Not Stuff

ERN77~ERN80要靠近MXM1

DVI_A_HPD 42

TMDS_B_TX0+ TP69 TPAD30
TMDS_B_TX0- TP68 TPAD30
TMDS_B_TX1+ TP55 TPAD30
TMDS_B_TX1- TP54 TPAD30
TMDS_B_TX2+ TP62 TPAD30
TMDS_B_TX2- TP61 TPAD30
G72_27MHZ TP58 TPAD30
G72_27MHZSS TP66 TPAD30

DVI_B_HPD TP64 TPAD30
TMDS_B_TXC+ TP53 TPAD30
TMDS_B_TXC- TP52 TPAD30

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Graphic MXM CONN

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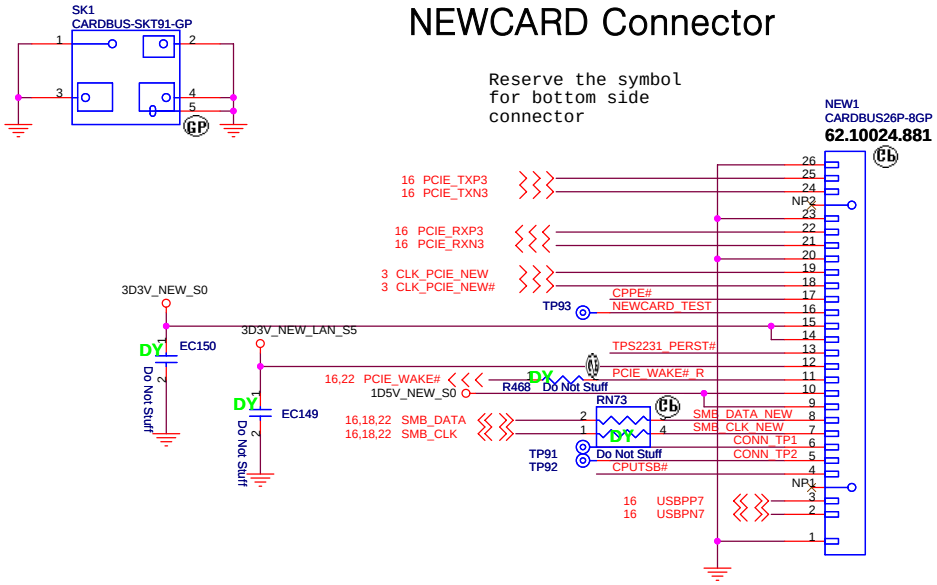
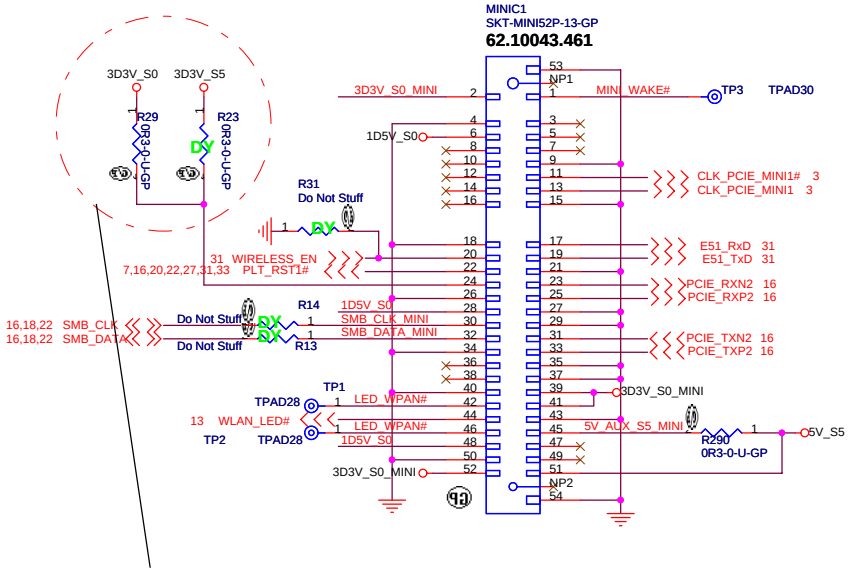
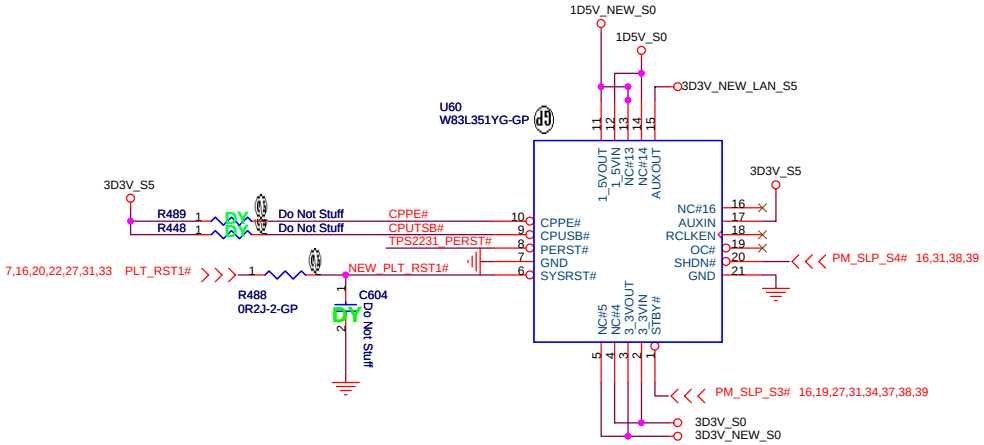
NEWCARD Connector

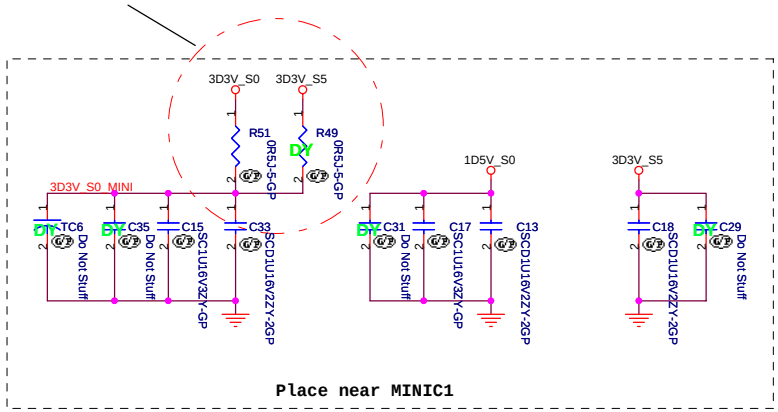


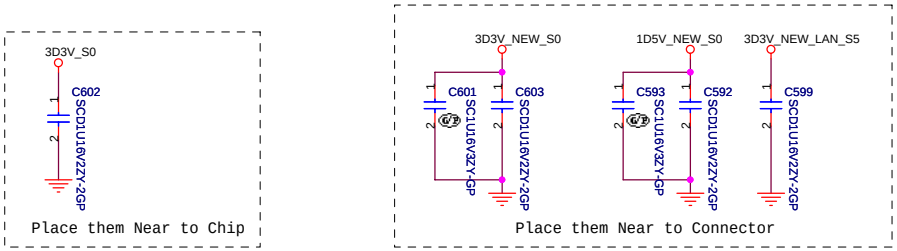
Mini Card Connector



PCIE Mini Card For WLA W/O iAMT, TV or 3G







UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINI CARD / NEW CARD***

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A3	Dellen	SA

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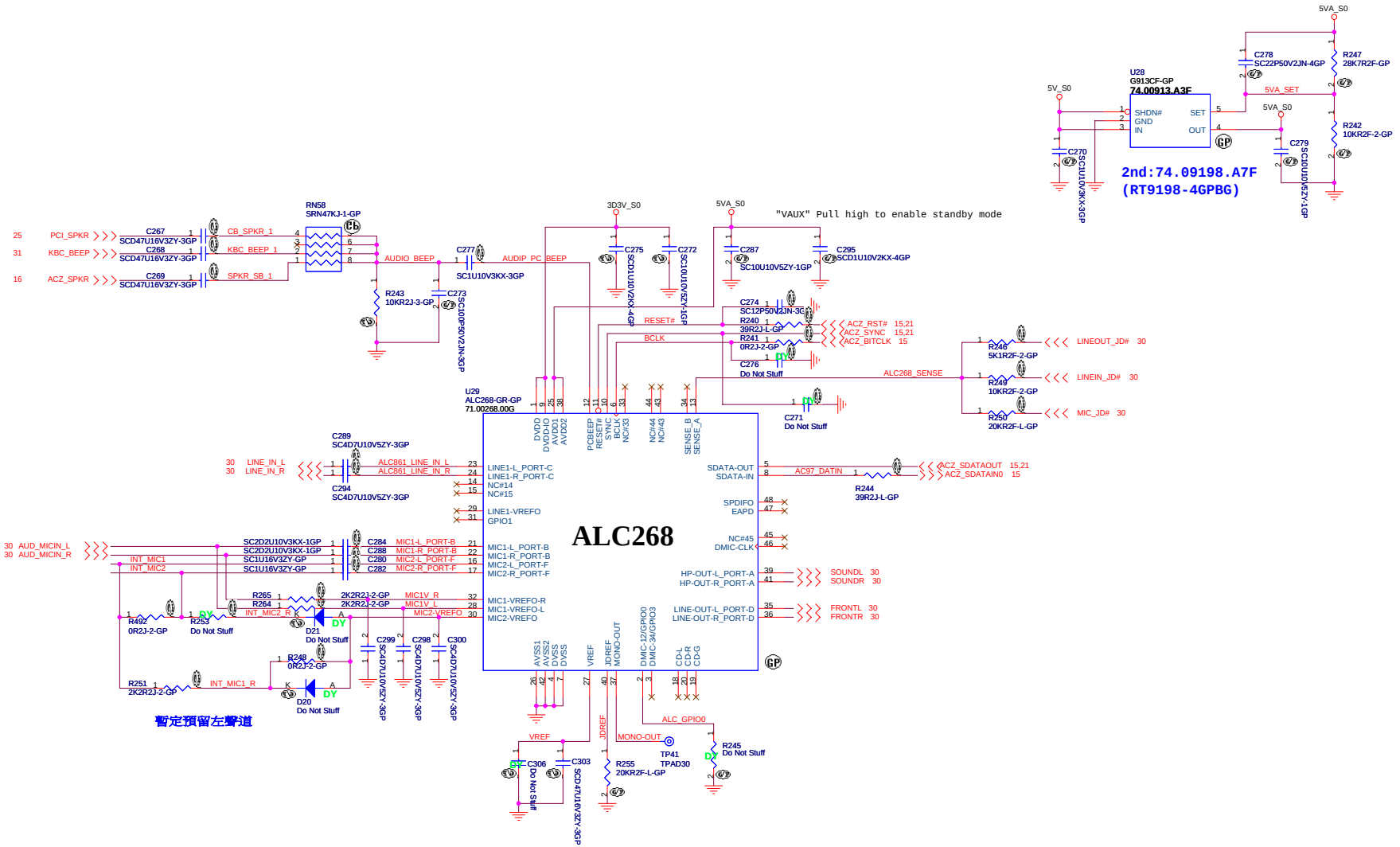

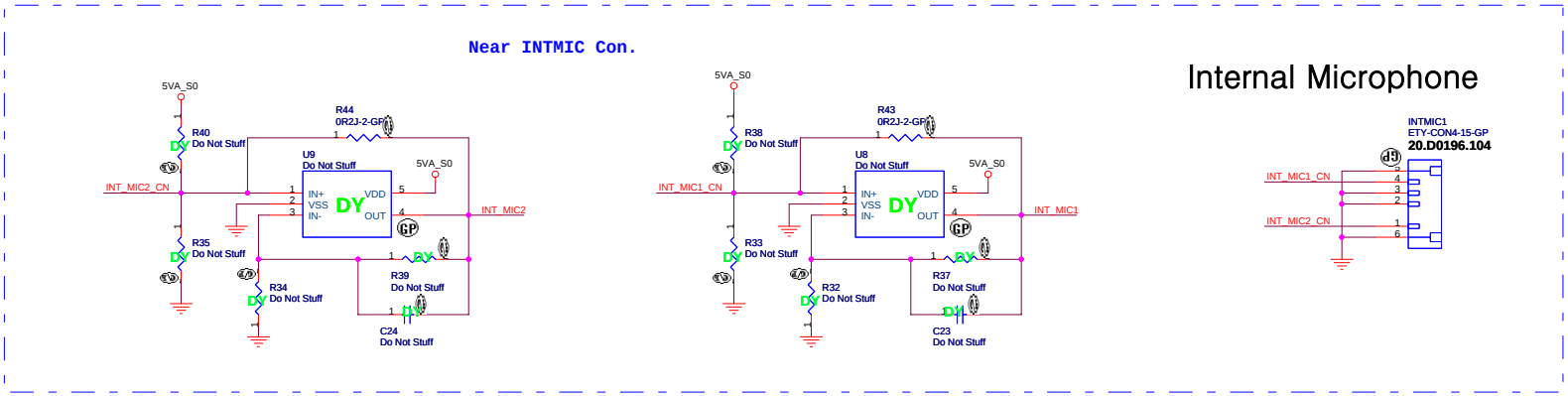

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AZALIA CODEC - ALC268*

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Custom	Dellen	SA

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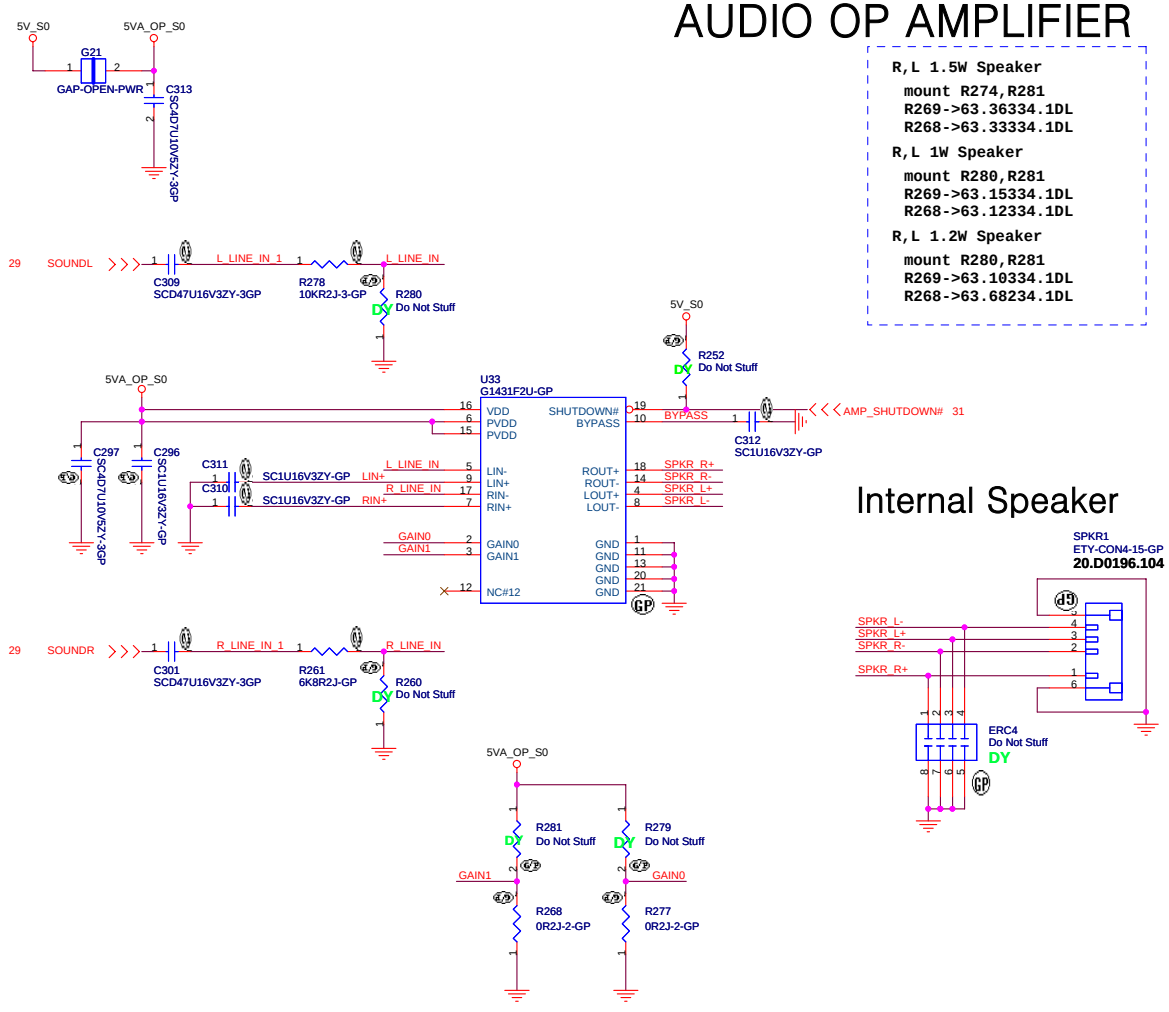
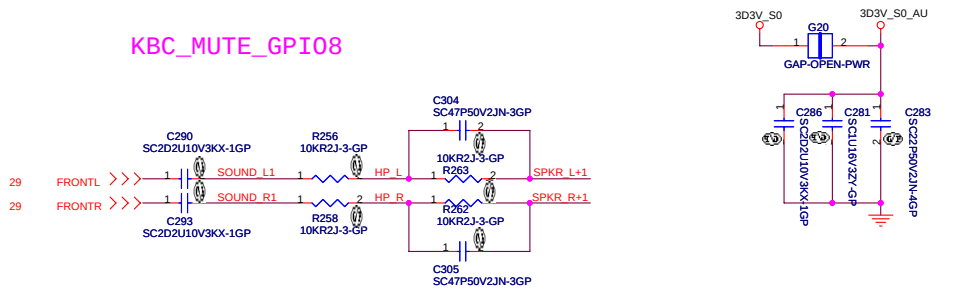
AUDIO OP AMPLIFIER

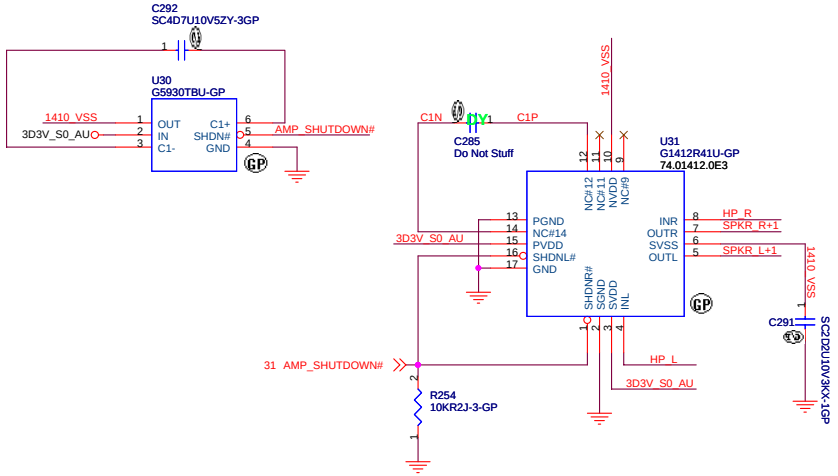
```
R,L 1.5W Speaker
  mount R274,R281
  R269->63.36334.1DL
  R268->63.33334.1DL
R,L 1W Speaker
  mount R280,R281
  R269->63.15334.1DL
  R268->63.12334.1DL
R,L 1.2W Speaker
  mount R280,R281
  R269->63.10334.1DL
  R268->63.68234.1DL
```



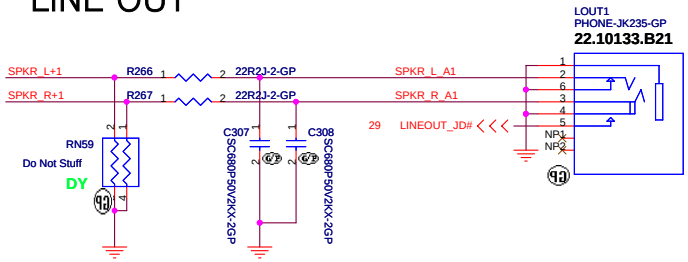
Internal Speaker

KBC_MUTE_GPIO8

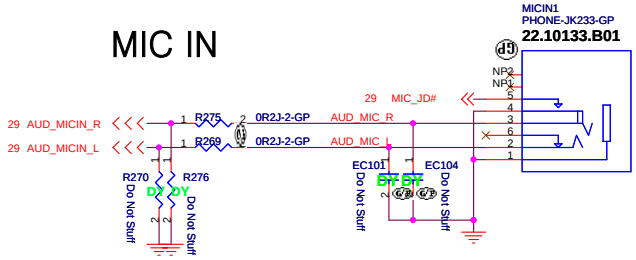




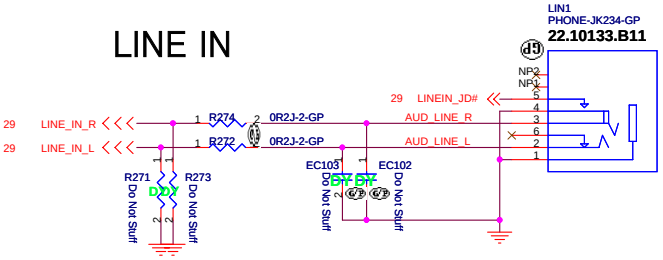
LINE OUT



MIC IN



LINE IN



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AUDIO AMP AND JACK*	
Size: Custom	Document Number: Dellen	Rev: SA
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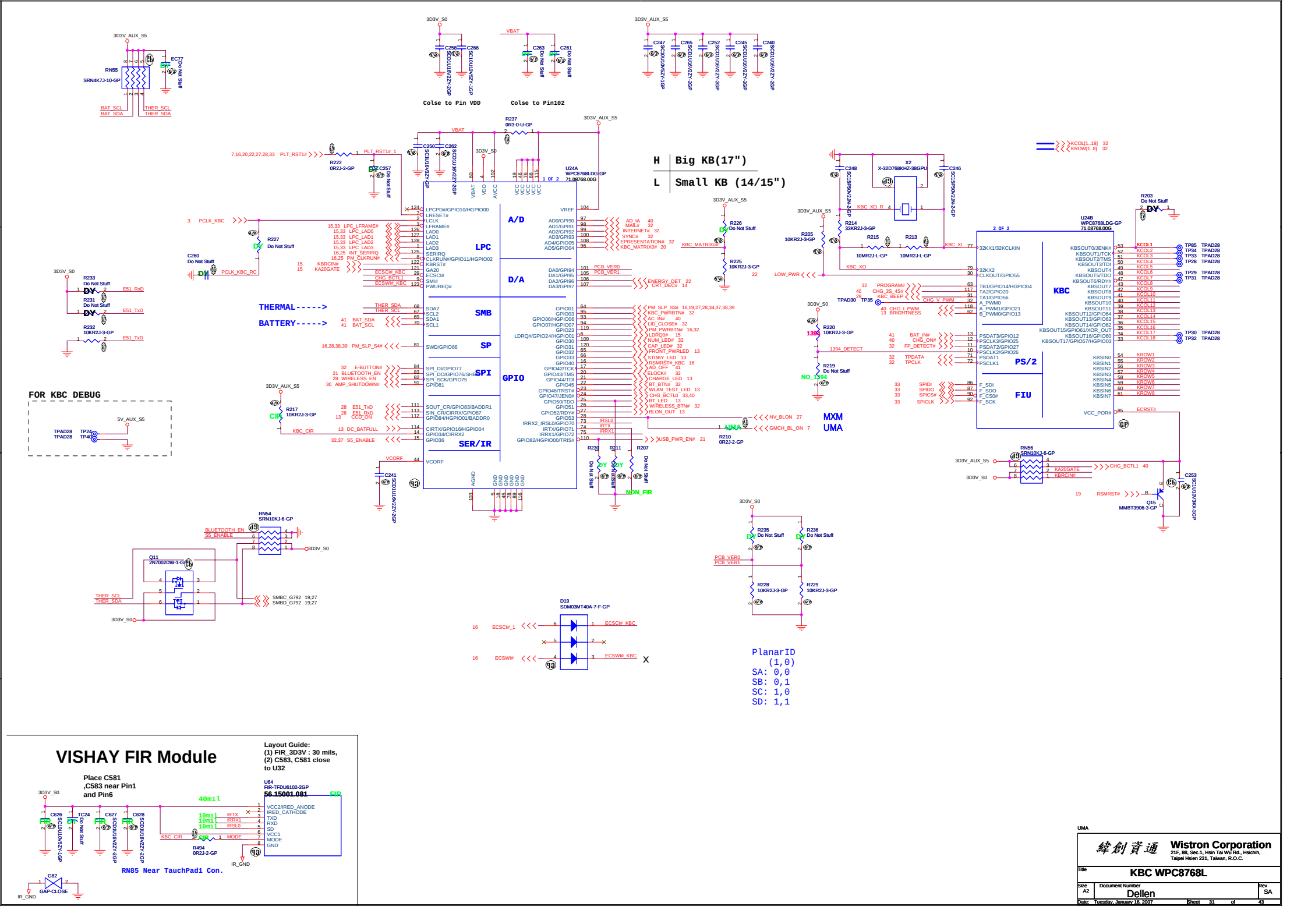
H Big KB(17")
L Small KB (14/15")
U24A WPC8768LDG-GP 71.08768.00G
U24B WPC8768LDG-GP 71.08768.00G
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
THERMAL----->
BATTERY----->
FOR KBC DEBUG
Colse to Pin VDD
Colse to Pin102
MXM
UMA
NON_FIR
PlanarID
(1,0)
SA: 0,0
SB: 0,1
SC: 0,1
SD: 1,1
VISHAY FIR Module
Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32
Place C581 ,C583 near Pin1 and Pin6
40mil
U64 FIR-TFDU6102-2GP
56.15001.081
RN85 Near TauchPad1 Con.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
Dellen
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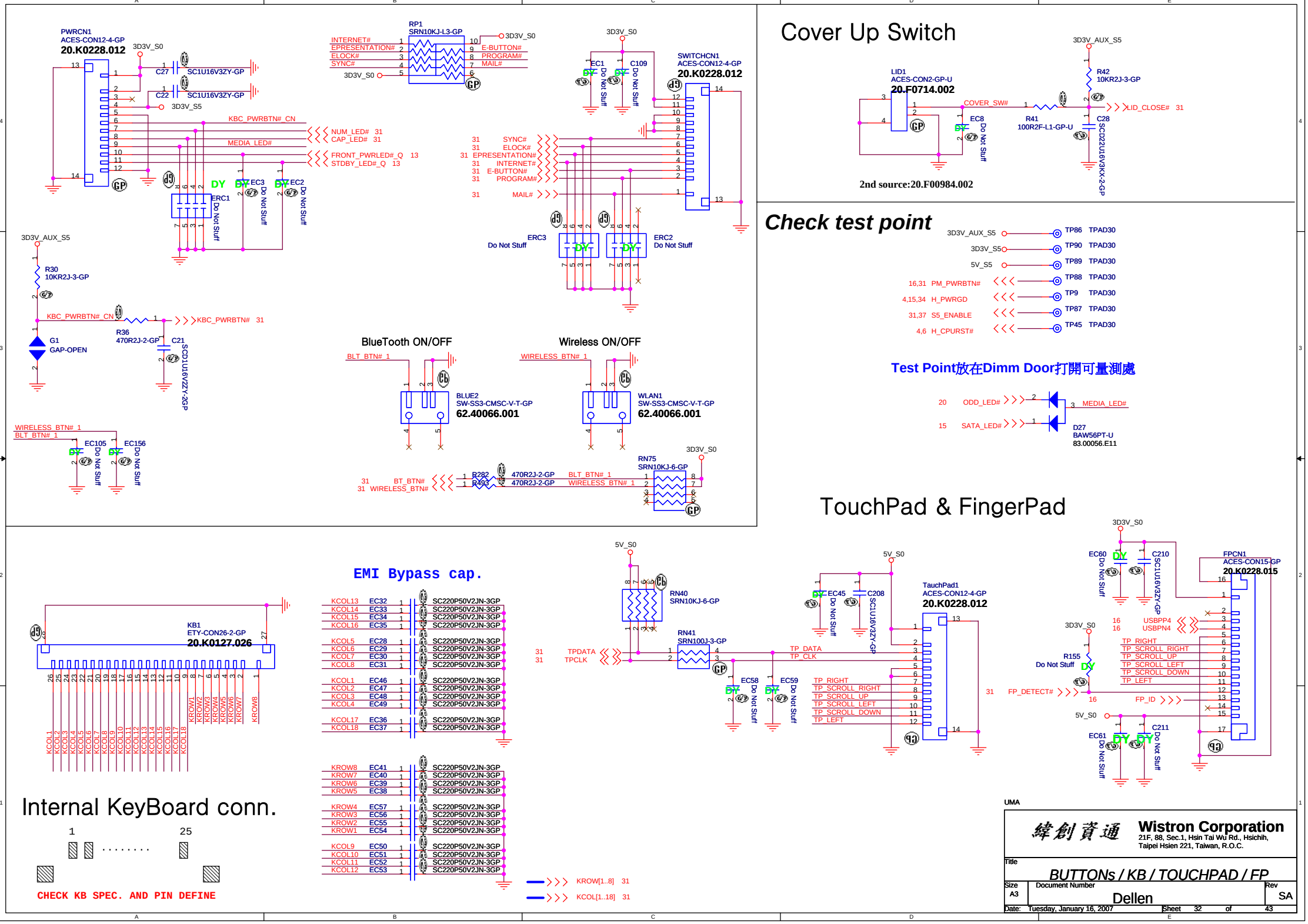
Cover Up Switch
LID1
ACES-CON2-GP-U
20.F0714.002
2nd source:20.F00984.002
COVER_SW#
LID_CLOSE# 31
R42
10KR2J-3-GP
R41
100R2F-L1-GP-U
C28
SCD22U16V3KX-2-GP
EC8
Do Not Stuff
3D3V_AUX_S5
Check test point
3D3V_AUX_S5 TP86 TPAD30
3D3V_S5 TP90 TPAD30
5V_S5 TP89 TPAD30
16,31 PM_PWRBTN# TP88 TPAD30
4,15,34 H_PWRGD TP9 TPAD30
31,37 S5_ENABLE TP87 TPAD30
4,6 H_CPURST# TP45 TPAD30
Test Point放在Dimm Door打開可量測處
20 ODD_LED#
15 SATA_LED#
MEDIA_LED#
D27
BAW56PT-U
83.00056.E11
PWRCN1
ACES-CON12-4-GP
20.K0228.012
3D3V_S0
C27
SC1U16V3ZY-GP
C22
SC1U16V3ZY-GP
3D3V_S5
KBC_PWRBTN#_CN
MEDIA_LED#
NUM_LED# 31
CAP_LED# 31
FRONT_PWRLED#_Q 13
STDBY_LED#_Q 13
ERC1
EC3
EC2
Do Not Stuff
RP1
SRN10KJ-L3-GP
INTERNET#
EPRESENTATION#
ELOCK#
SYNC#
E-BUTTON#
PROGRAM#
MAIL#
EC1
C109
SWITCHCN1
ACES-CON12-4-GP
20.K0228.012
31 SYNC#
31 ELOCK#
31 EPRESENTATION#
31 INTERNET#
31 E-BUTTON#
31 PROGRAM#
31 MAIL#
ERC3
ERC2
R30
10KR2J-3-GP
KBC_PWRBTN#_CN
KBC_PWRBTN# 31
R36
470R2J-2-GP
C21
SCD1U16V2ZY-2GP
G1
GAP-OPEN
WIRELESS_BTN# 1
BLT_BTN# 1
EC105
EC156
BlueTooth ON/OFF
BLT_BTN# 1
BLUE2
SW-SS3-CMSC-V-T-GP
62.40066.001
Wireless ON/OFF
WIRELESS_BTN# 1
WLAN1
SW-SS3-CMSC-V-T-GP
62.40066.001
RN75
SRN10KJ-6-GP
31 BT_BTN#
31 WIRELESS_BTN#
R282
R493
470R2J-2-GP
BLT_BTN# 1
WIRELESS_BTN# 1
TouchPad & FingerPad
5V_S0
RN40
SRN10KJ-6-GP
RN41
SRN100J-3-GP
31 TPDATA
31 TPCLK
EC45
C208
SC1U16V2ZY-GP
EC58
EC59
TP_DATA
TP_CLK
TauchPad1
ACES-CON12-4-GP
20.K0228.012
TP_RIGHT
TP_SCROLL_RIGHT
TP_SCROLL_UP
TP_SCROLL_LEFT
TP_SCROLL_DOWN
TP_LEFT
31 FP_DETECT#
EC60
C210
SC1U16V3ZY-GP
FPCN1
ACES-CON15-GP
20.K0228.015
16 USBPP4
16 USBPN4
R155
Do Not Stuff
16 FP_ID
EC61
C211
EMI Bypass cap.
KCOL13 EC32 SC220P50V2JN-3GP
KCOL14 EC33 SC220P50V2JN-3GP
KCOL15 EC34 SC220P50V2JN-3GP
KCOL16 EC35 SC220P50V2JN-3GP
KCOL5 EC28 SC220P50V2JN-3GP
KCOL6 EC29 SC220P50V2JN-3GP
KCOL7 EC30 SC220P50V2JN-3GP
KCOL8 EC31 SC220P50V2JN-3GP
KCOL1 EC46 SC220P50V2JN-3GP
KCOL2 EC47 SC220P50V2JN-3GP
KCOL3 EC48 SC220P50V2JN-3GP
KCOL4 EC49 SC220P50V2JN-3GP
KCOL17 EC36 SC220P50V2JN-3GP
KCOL18 EC37 SC220P50V2JN-3GP
KROW8 EC41 SC220P50V2JN-3GP
KROW7 EC40 SC220P50V2JN-3GP
KROW6 EC39 SC220P50V2JN-3GP
KROW5 EC38 SC220P50V2JN-3GP
KROW4 EC57 SC220P50V2JN-3GP
KROW3 EC56 SC220P50V2JN-3GP
KROW2 EC55 SC220P50V2JN-3GP
KROW1 EC54 SC220P50V2JN-3GP
KCOL9 EC50 SC220P50V2JN-3GP
KCOL10 EC51 SC220P50V2JN-3GP
KCOL11 EC52 SC220P50V2JN-3GP
KCOL12 EC53 SC220P50V2JN-3GP
KROW[1..8] 31
KCOL[1..18] 31
KB1
ETY-CON26-2-GP
20.K0127.026
Internal KeyBoard conn.
1
25
CHECK KB SPEC. AND PIN DEFINE
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BUTTONs / KB / TOUCHPAD / FP
Size A3
Document Number
Dellen
Rev SA
Date: Tuesday, January 16, 2007
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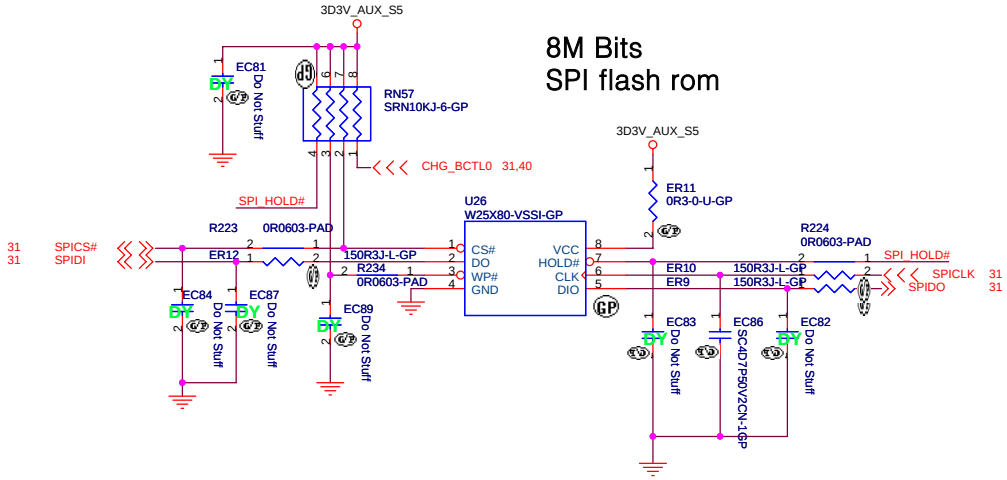

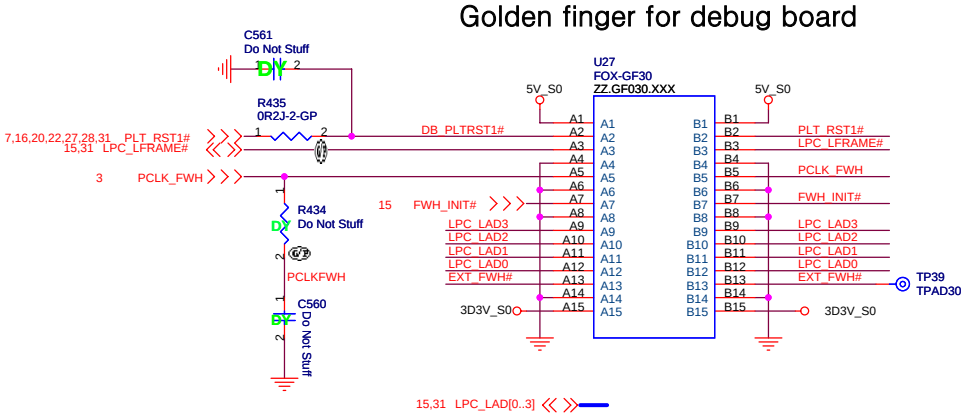

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BIOS		
Size A3	Document Number Dellen	Rev SA
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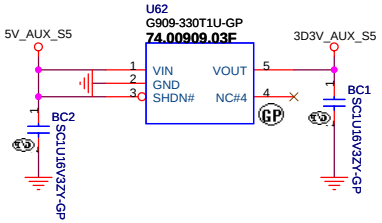
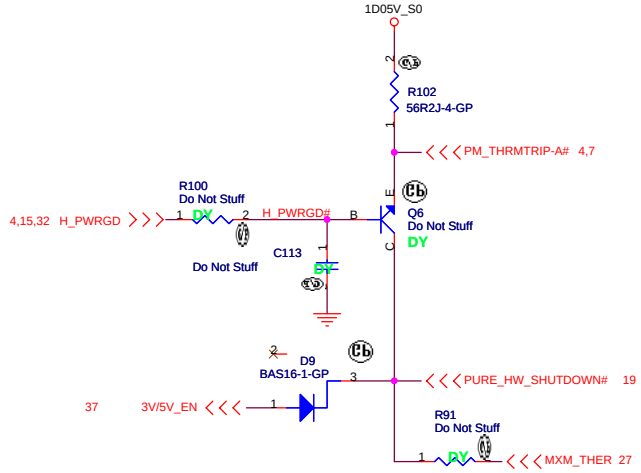
Aux Power

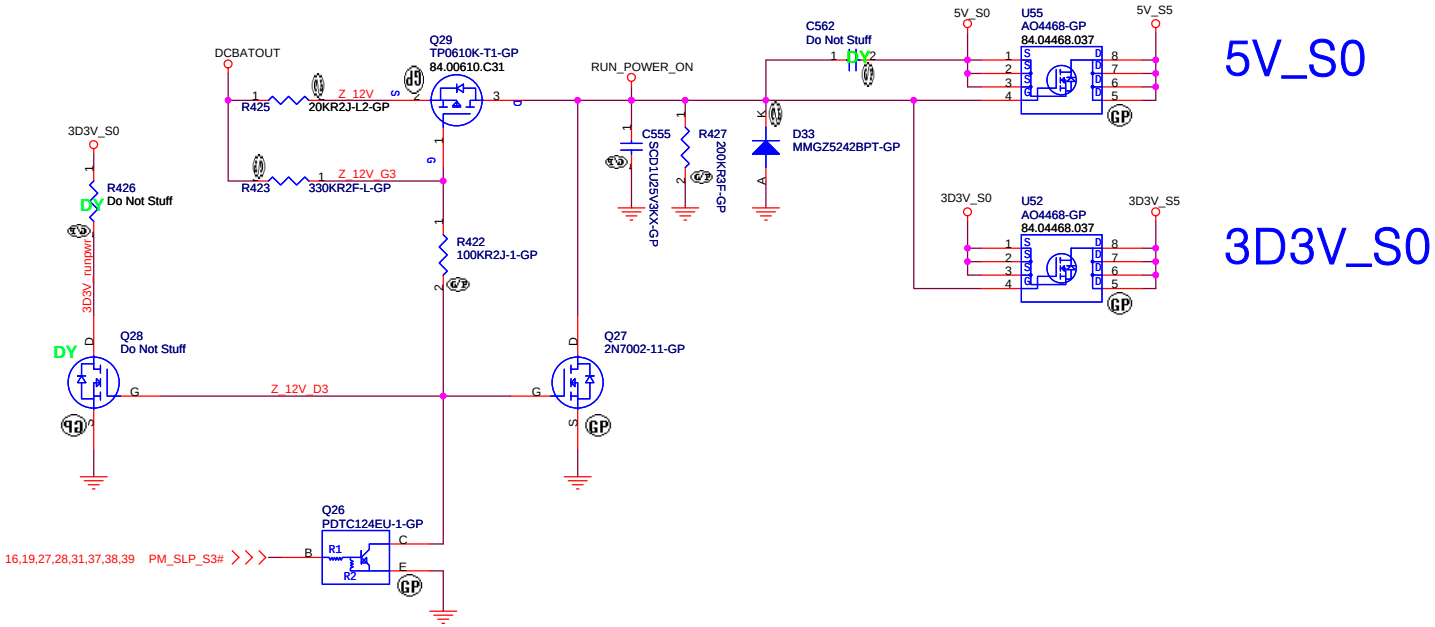
3D3V_AUX_S5

I max = 150 mA





Run Power



5V_S0

3D3V_S0

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***3D3V_AUX_S5 / 3D3V_S0 / 5V_S0***	
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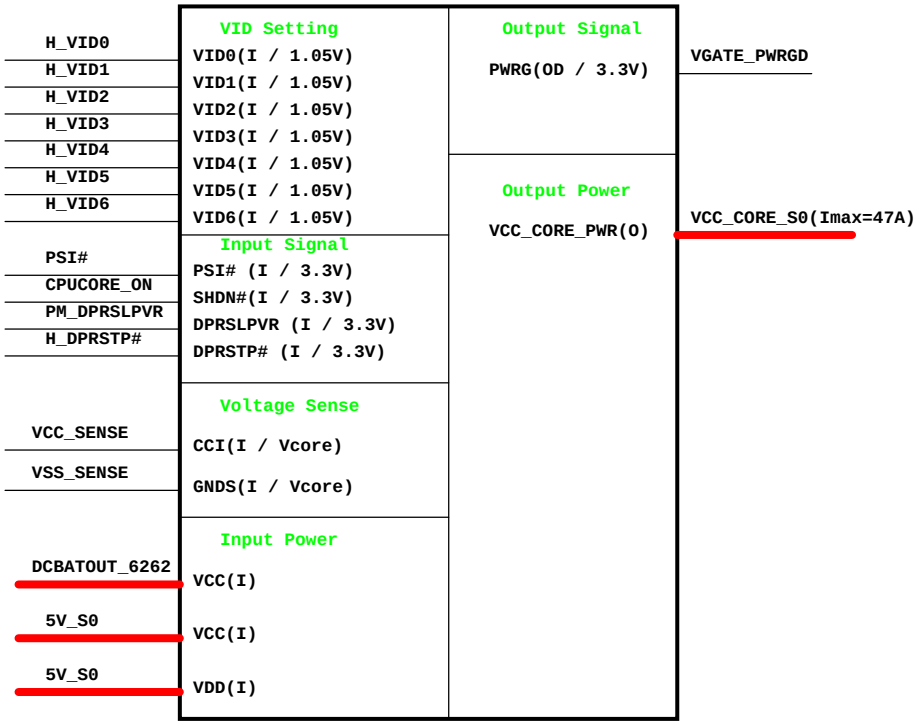
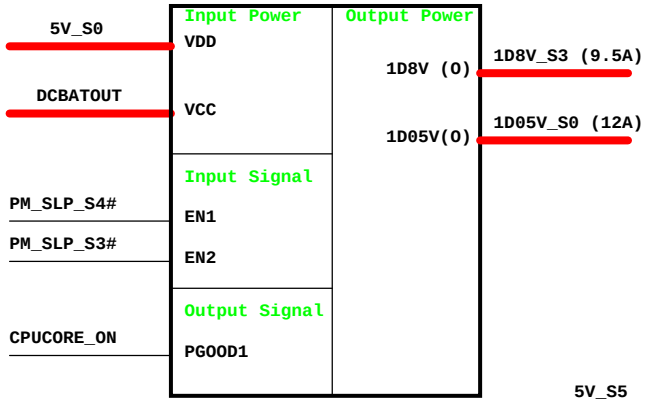
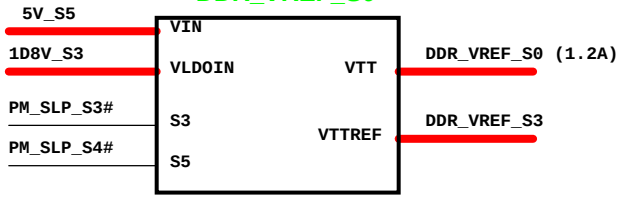
CPU_CORE
MAX8770



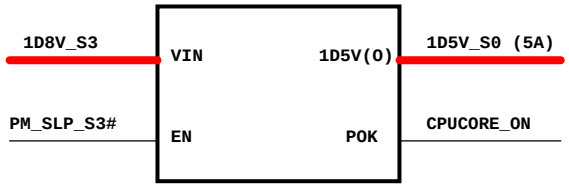
MAX8717
1D8V_S3 / 1D05V_S0



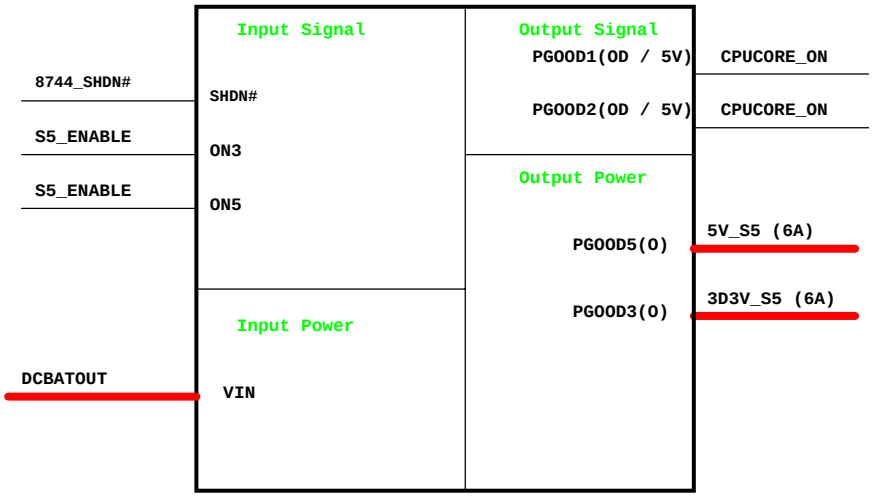
TPS51100
DDR_VREF_S0



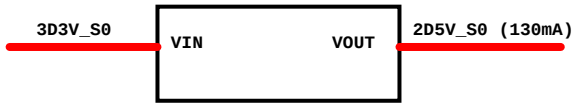
APL5912
1D5V_S0



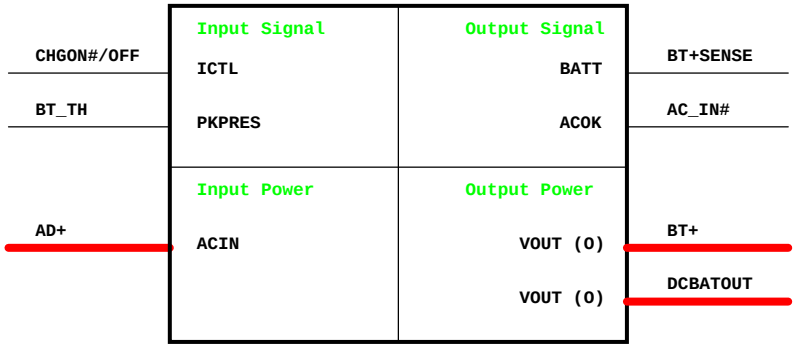
MAX8744
5V_S5 / 3D3V_S5



APL5312
2D5V_S0



Charger ISL6255



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

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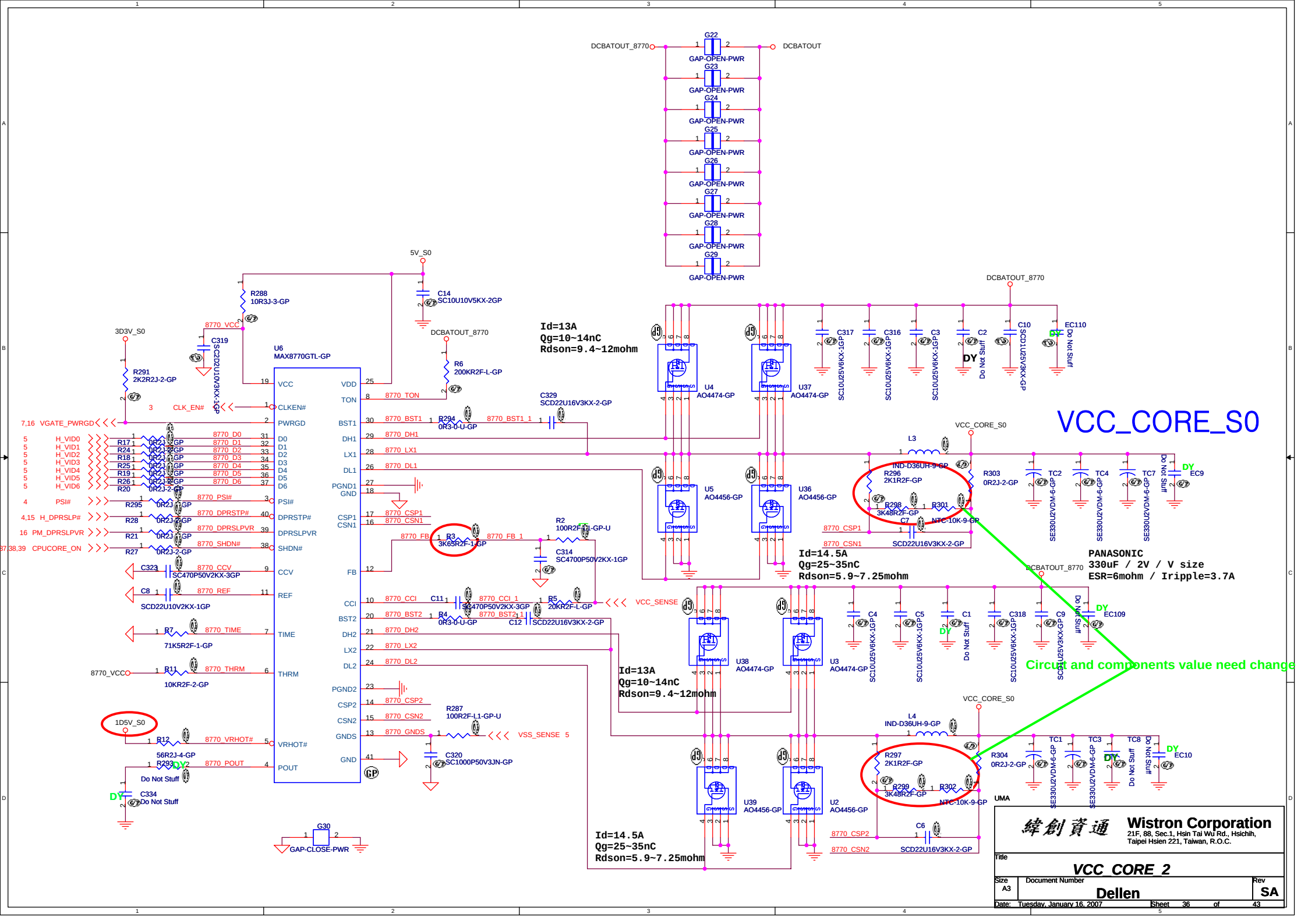
DCBATOUT_8770
DCBATOUT
GAP-OPEN-PWR
5V_S0
3D3V_S0
U6
MAX8770GTL-GP
VCC
CLKEN#
PWRGD
D0
D1
D2
D3
D4
D5
D6
PSI#
DPRSTP#
DPRSLPVR
SHDN#
CCV
REF
TIME
THRM
VRHOT#
POUT
VDD
TON
BST1
DH1
LX1
DL1
PGND1
GND
CSP1
CSN1
FB
CCI
BST2
DH2
LX2
DL2
PGND2
CSP2
CSN2
GNDS
GND
VGATE_PWRGD
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
PSI#
H_DPRSLP#
PM_DPRSLPVR
CPUCORE_ON
CLK_EN#
8770_VCC
8770_TON
8770_BST1
8770_DH1
8770_LX1
8770_DL1
8770_CSP1
8770_CSN1
8770_FB
8770_CCI
8770_BST2
8770_DH2
8770_LX2
8770_DL2
8770_CSP2
8770_CSN2
8770_GNDS
8770_CCV
8770_REF
8770_TIME
8770_THRM
8770_VRHOT#
8770_POUT
8770_SHDN#
8770_BST1_1
8770_FB_1
8770_CCI_1
8770_BST2_1
VCC_SENSE
VSS_SENSE 5
1D5V_S0
G30
GAP-CLOSE-PWR
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
U4
AO4474-GP
U37
AO4474-GP
U5
AO4456-GP
U36
AO4456-GP
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
U38
AO4474-GP
U3
AO4474-GP
U39
AO4456-GP
U2
AO4456-GP
VCC_CORE_S0
L3
IND-D36UH-9-GP
L4
IND-D36UH-9-GP
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
Circuit and components value need change
UMA
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VCC_CORE_2
Size
A3
Document Number
Dellen
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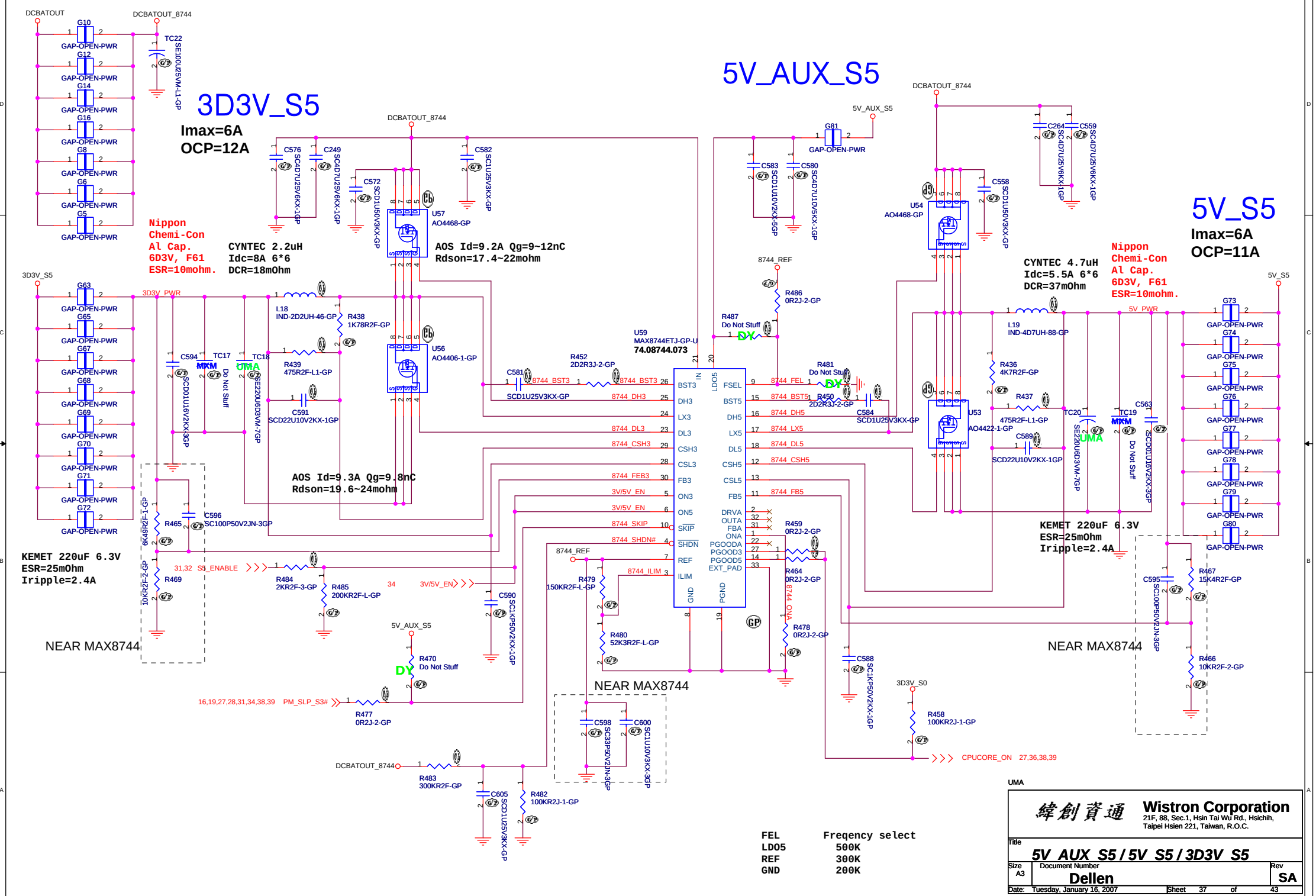
3D3V_S5
Imax=6A
OCP=12A
5V_AUX_S5
5V_S5
Imax=6A
OCP=11A
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
CYNTEC 2.2uH Idc=8A 6*6 DCR=18mOhm
AOS Id=9.2A Qg=9~12nC Rdson=17.4~22mohm
AOS Id=9.3A Qg=9.8nC Rdson=19.6~24mohm
CYNTEC 4.7uH Idc=5.5A 6*6 DCR=37mOhm
KEMET 220uF 6.3V ESR=25mOhm Iripple=2.4A
NEAR MAX8744
U59 MAX8744ETJ-GP-U 74.08744.073
U57 AO4468-GP
U56 AO4406-1-GP
U54 AO4468-GP
U53 AO4422-1-GP
DCBATOUT
DCBATOUT_8744
3D3V_PWR
5V_PWR
3D3V_S0
CPUCORE_ON 27,36,38,39
S5_ENABLE
PM_SLP_S3#
FEL Freqency select
LDO5 500K
REF 300K
GND 200K
UMA
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
5V_AUX_S5 / 5V_S5 / 3D3V_S5
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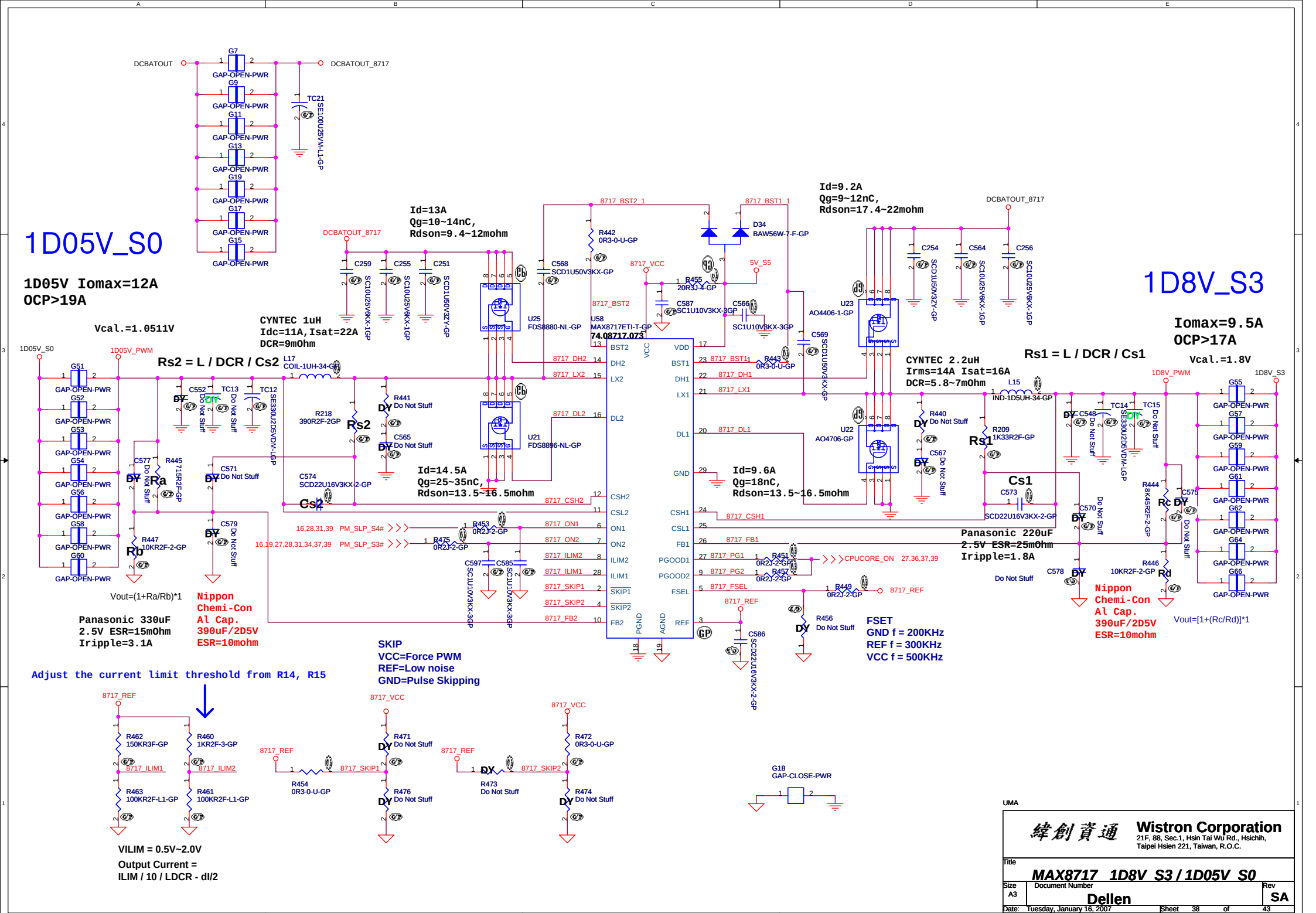
1D05V_S0
1D05V Iomax=12A
OCP>19A
Vcal.=1.0511V
Rs2 = L / DCR / Cs2
CYNTEC 1uH
Idc=11A,Isat=22A
DCR=9mOhm
Id=13A
Qg=10~14nC,
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC,
Rdson=13.5~16.5mohm
Id=9.6A
Qg=18nC,
Rdson=13.5~16.5mohm
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
74.08717.073
1D8V_S3
Iomax=9.5A
OCP>17A
Vcal.=1.8V
Rs1 = L / DCR / Cs1
CYNTEC 2.2uH
Irms=14A Isat=16A
DCR=5.8~7mOhm
Panasonic 330uF
2.5V ESR=15mOhm
Iripple=3.1A
Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm
Vout=(1+Ra/Rb)*1
Panasonic 220uF
2.5V ESR=25mOhm
Iripple=1.8A
Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm
Vout=[1+(Rc/Rd)]*1
SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping
FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz
Adjust the current limit threshold from R14, R15
VILIM = 0.5V~2.0V
Output Current =
ILIM / 10 / LDCR - dI/2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MAX8717 1D8V S3 / 1D05V S0
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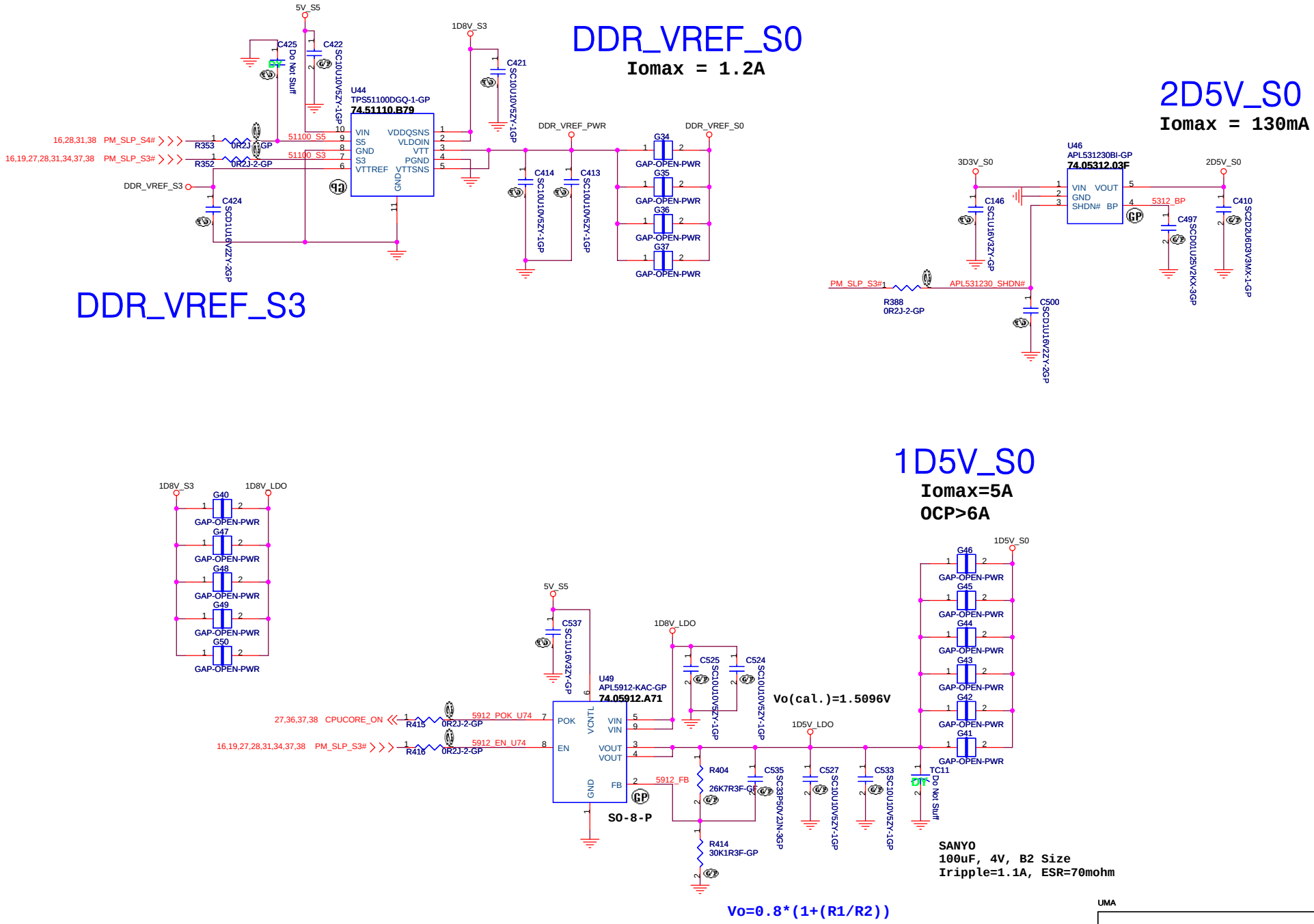

UMA

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Title: *1D5V_S0 / 2D5V_S0 / DDR_VREF_S0*

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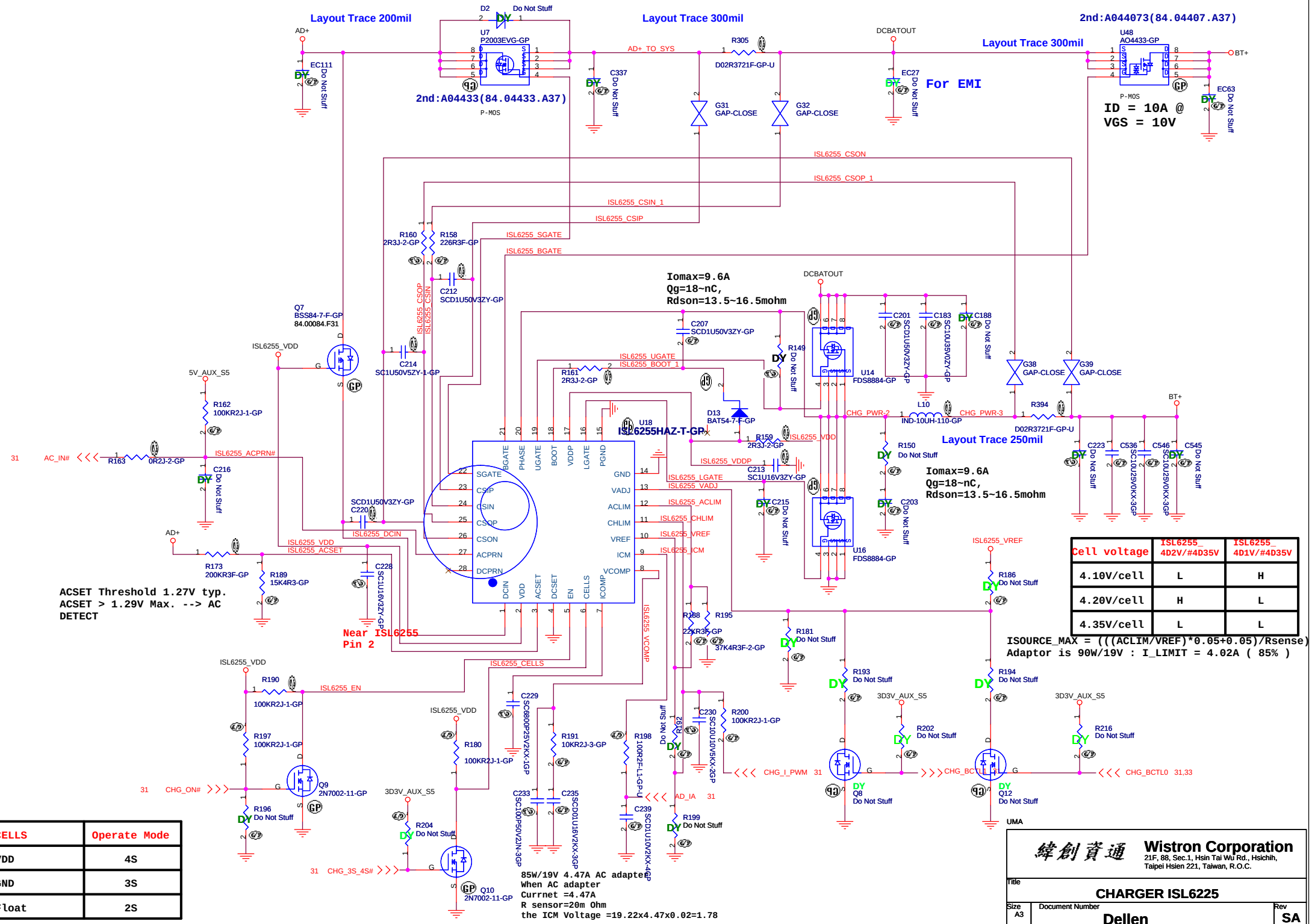
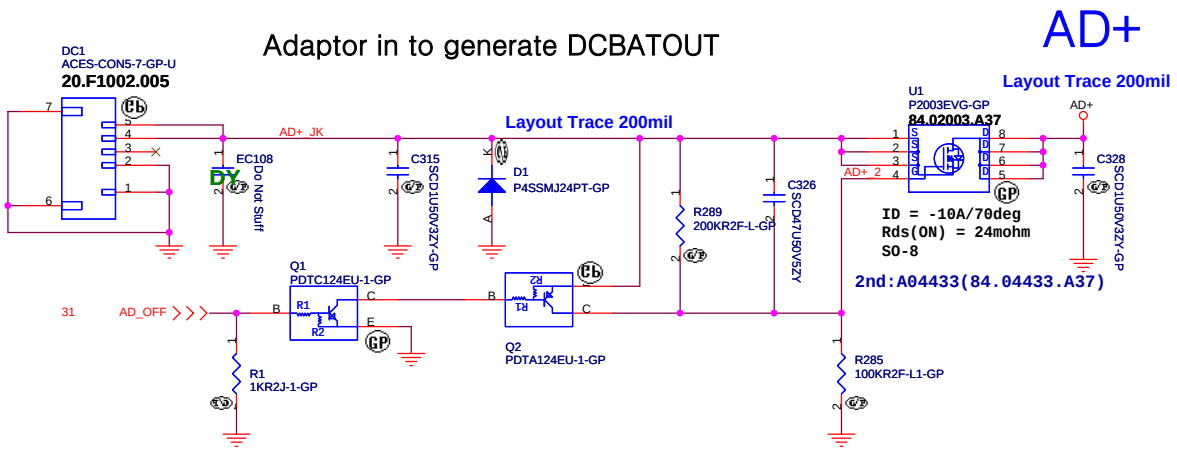
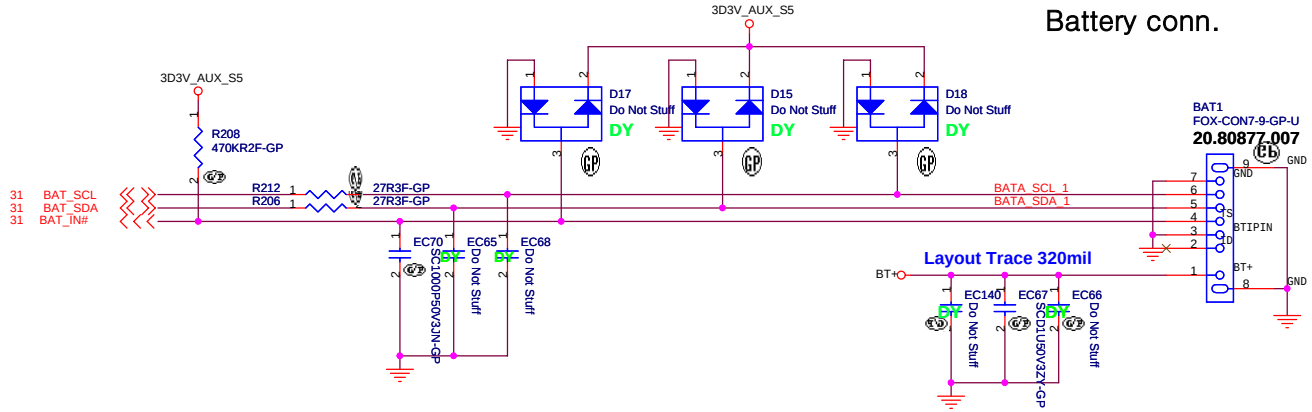


Cell voltage	ISL6255_ 4D2V/#4D35V	ISL6255_ 4D1V/#4D35V
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S





UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AD / BATT conn.**	
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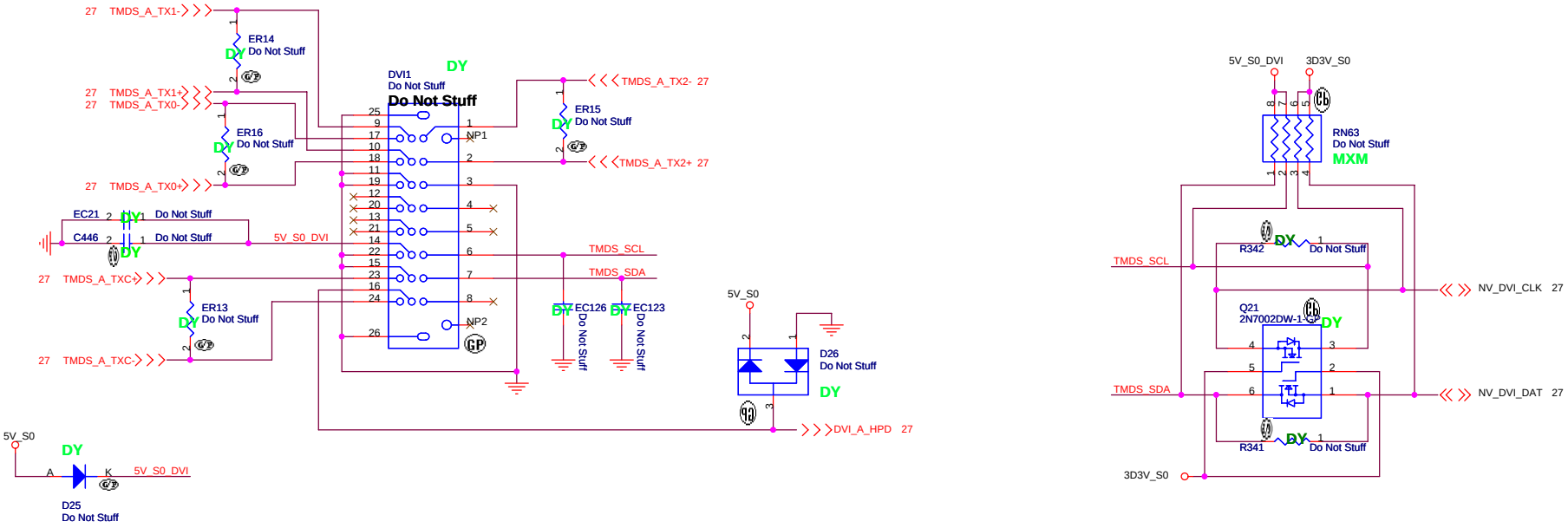

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**DVI CONNECTOR**	
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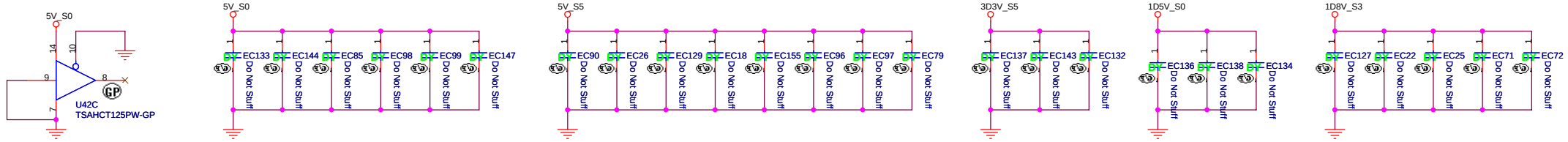
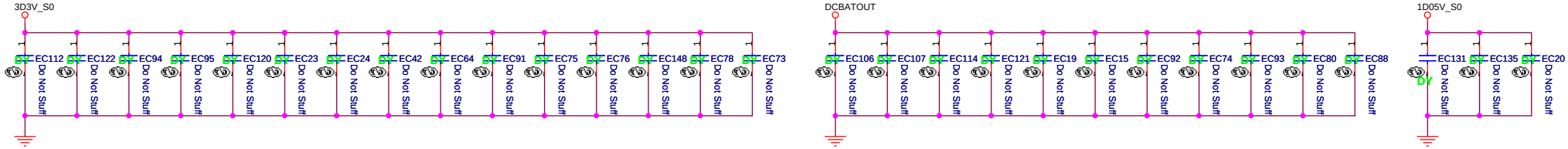
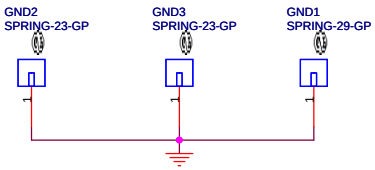
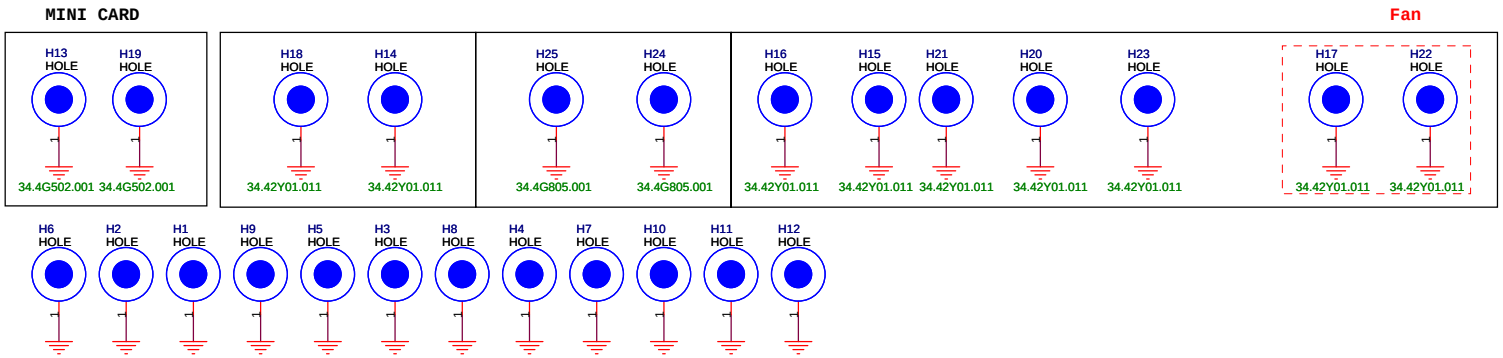






Spring

GND 1 : 34.42T14.001
GND 2/3 : 34.39S07.003



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI / Spring / Boss***

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