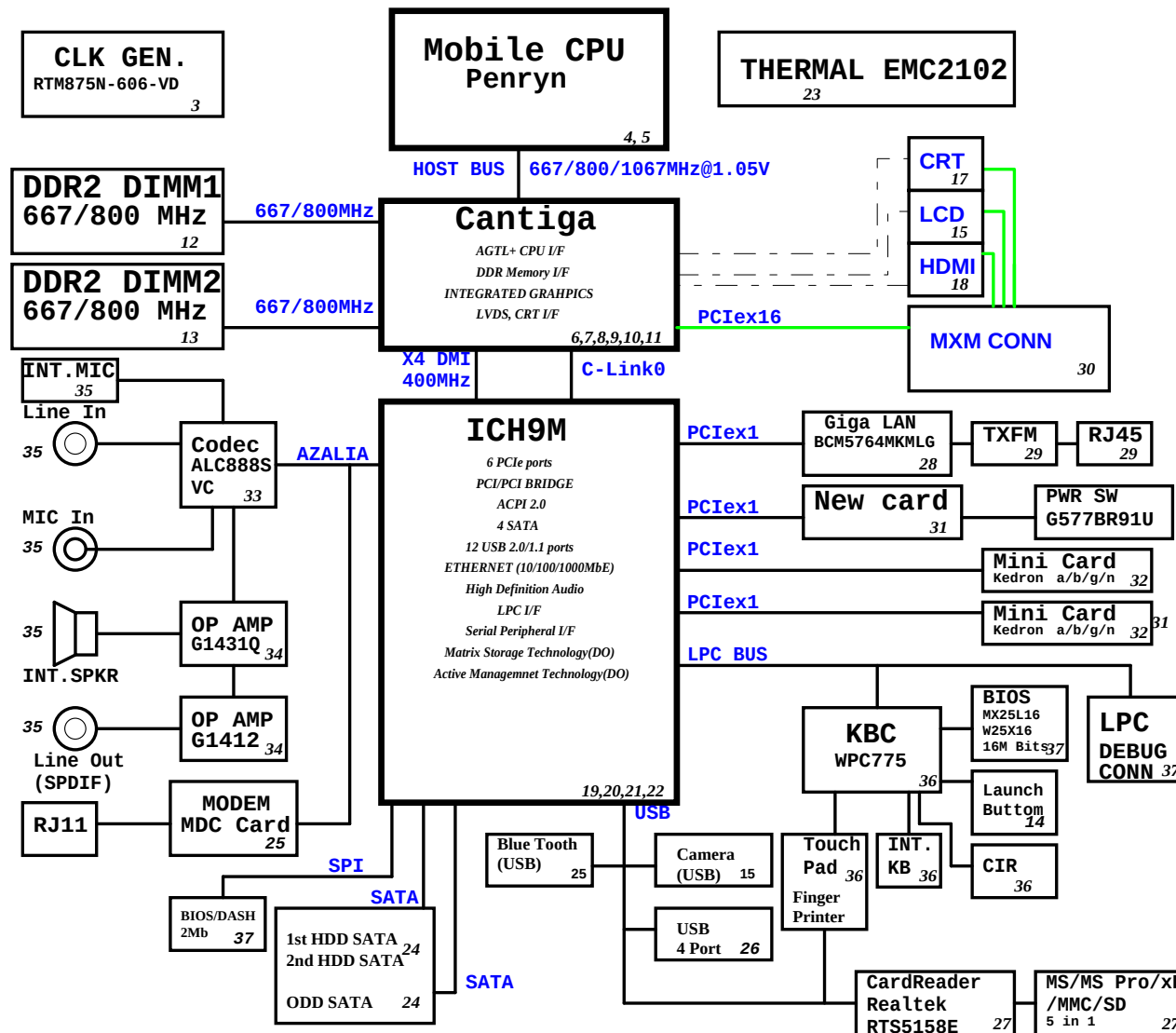


Big Bear 2 Block Diagram

Project code: 91.4AV01.001
PCB P/N : 48.4AV01.
REVISION : -1



PCB STACKUP

TOP _____

VCC _____

S _____

S _____

GND _____

BOTTOM _____

SYSTEM DC/DC	
TPS51125 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
SYSTEM DC/DC	
TPS51124 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
RT9026 44	
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3
RT9018A 44	
1D8V_S3	1D5V_S0
G9131 44	
3D3V_S0	2D5V_S0
GFXCORE DC/DC	
ISL6263 46	
INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7-1.25V
CPU DC/DC	
ISL6266A 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35-1.5V
CHARGER	
BQ24745 47	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

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Title			
BLOCK DIAGRAM			
Size	Document Number	Rev	
Custom	Big Bear 2	-1	
Date: Wednesday, October 22, 2008		Sheet 1	of 50

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

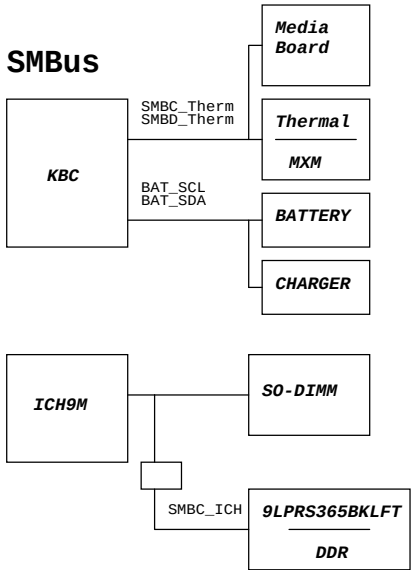
PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN/TV
LANE4	JMB385 Card Reader
LANE5	NewCard
LANE6	NC

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	USB5(DOCK)
4	USB3
5	Bluetooth
6	FP
7	MINIC1
8	WEBCAM
9	NEW1
10	MINIC2
11	NC

SMBus



ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default). 1 = Digital display Port and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

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Title

Reference

Size A3

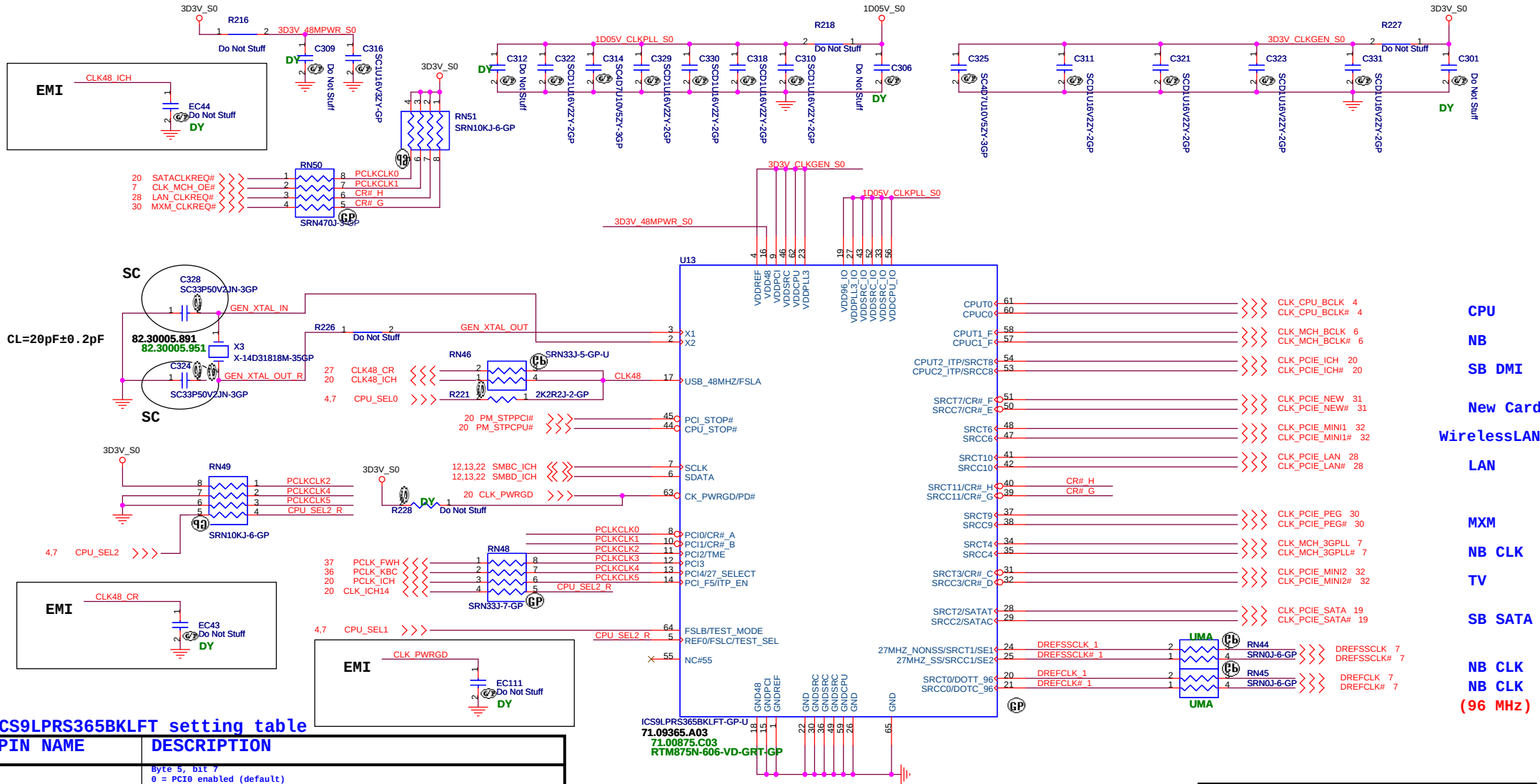
Document Number

Date: Wednesday, October 22, 2008

Sheet 2 of 50

Rev -1

Big Bear 2



ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1 = CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1 = CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1 = CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1 = CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1 = CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1 = CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1 = CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

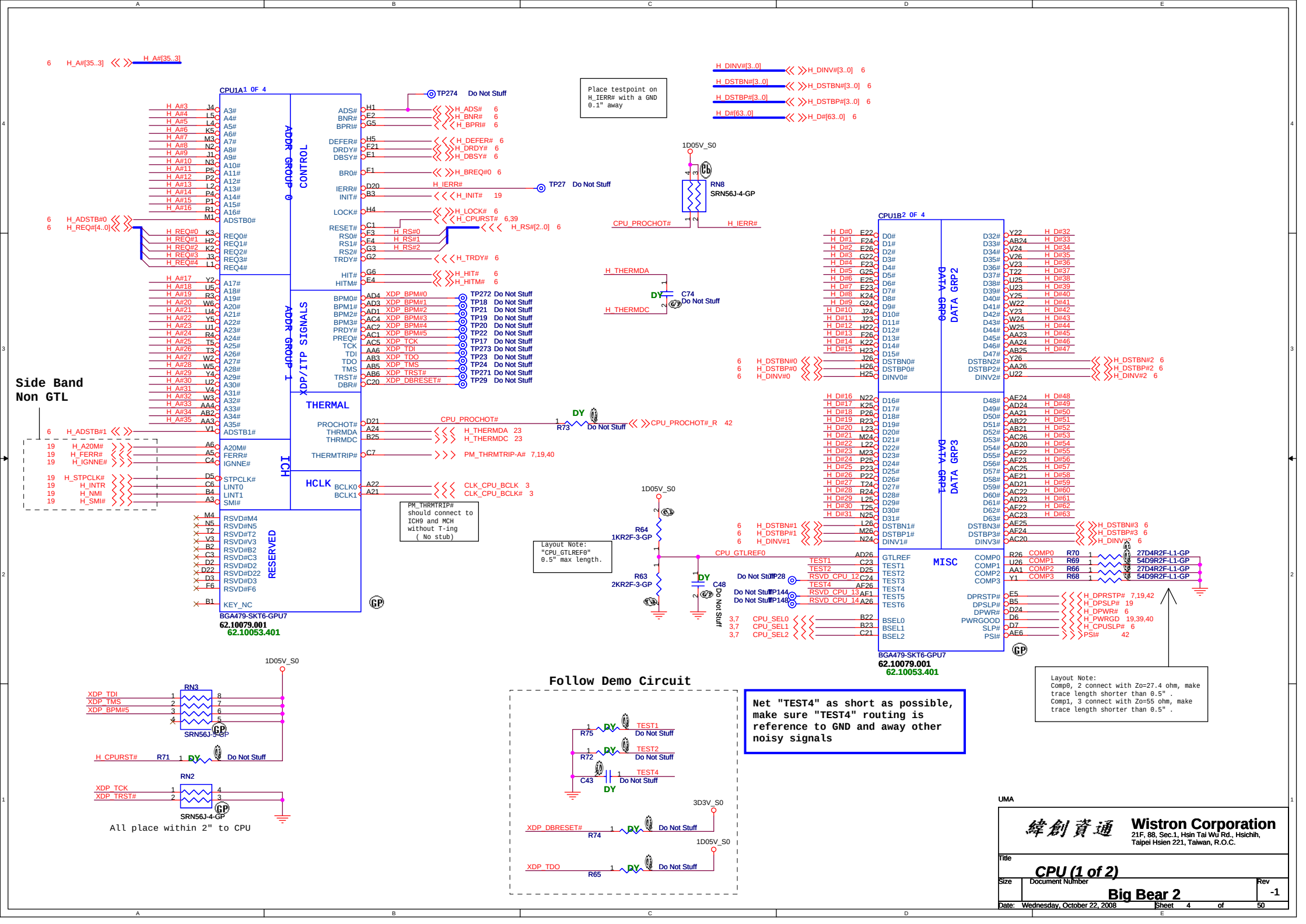
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Title: **Clock Generator**

Size: Document Number **Big Bear 2** Rev: -1

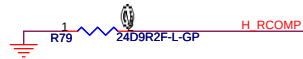
Date: Wednesday, October 22, 2008 Sheet 3 of 50



H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)

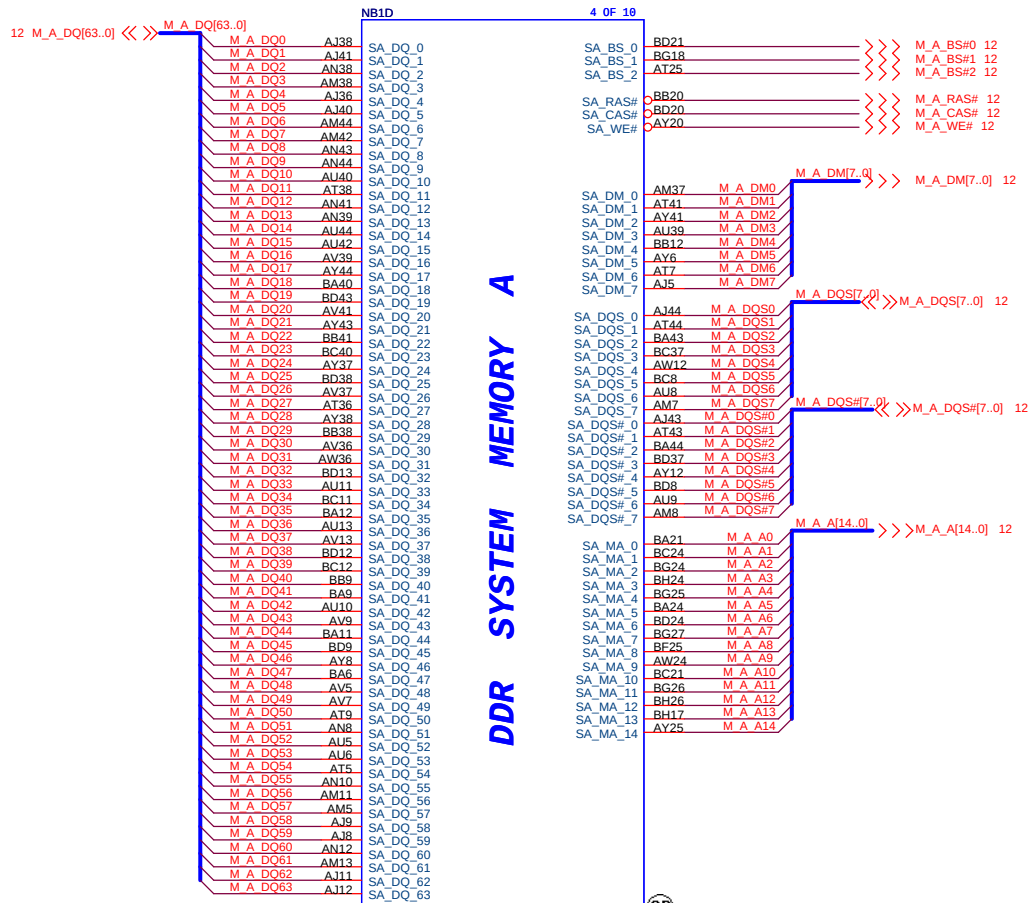


H_RCOMP routing Trace width and
Spacing use 10 / 20 mil

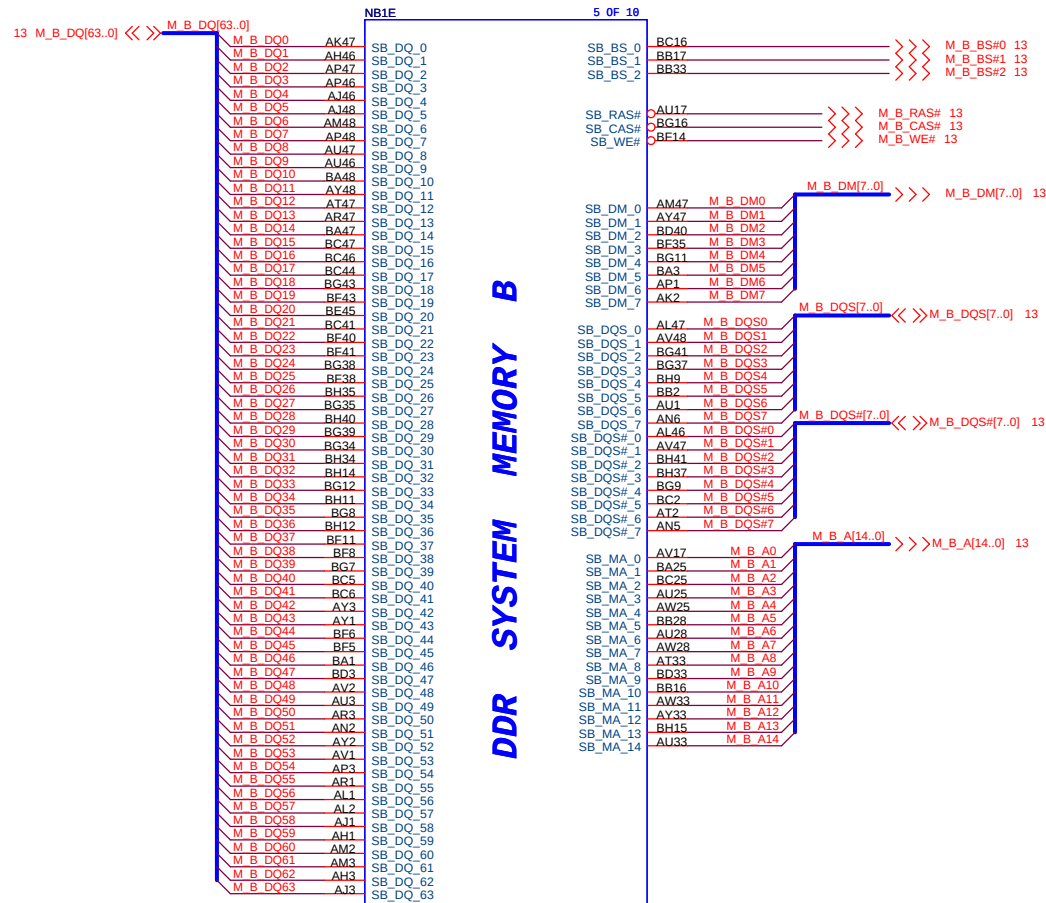


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71.CNTIG.D1U

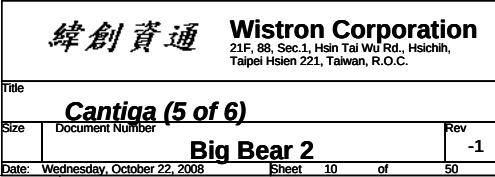


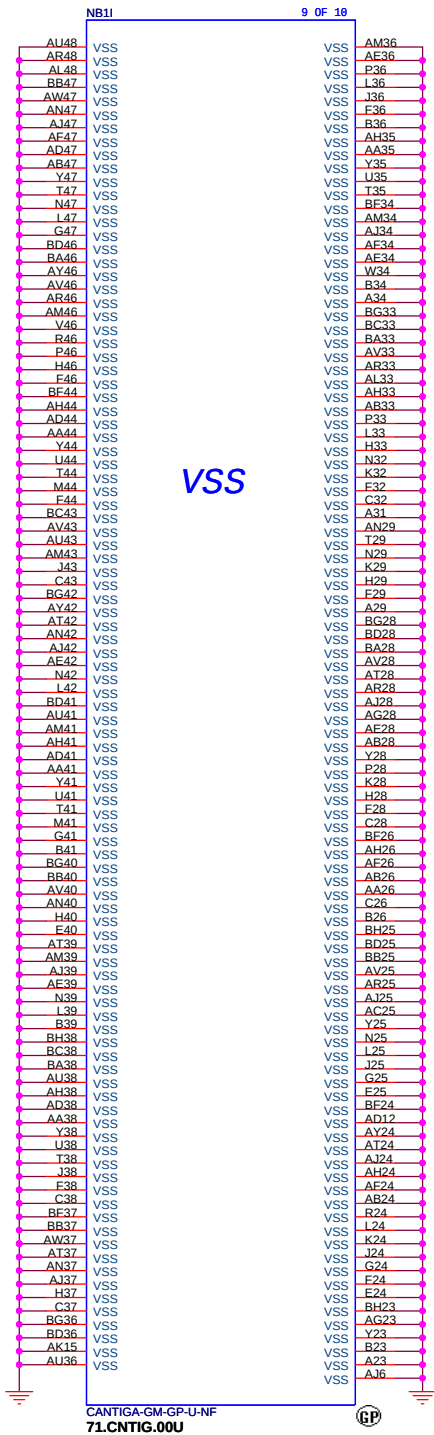


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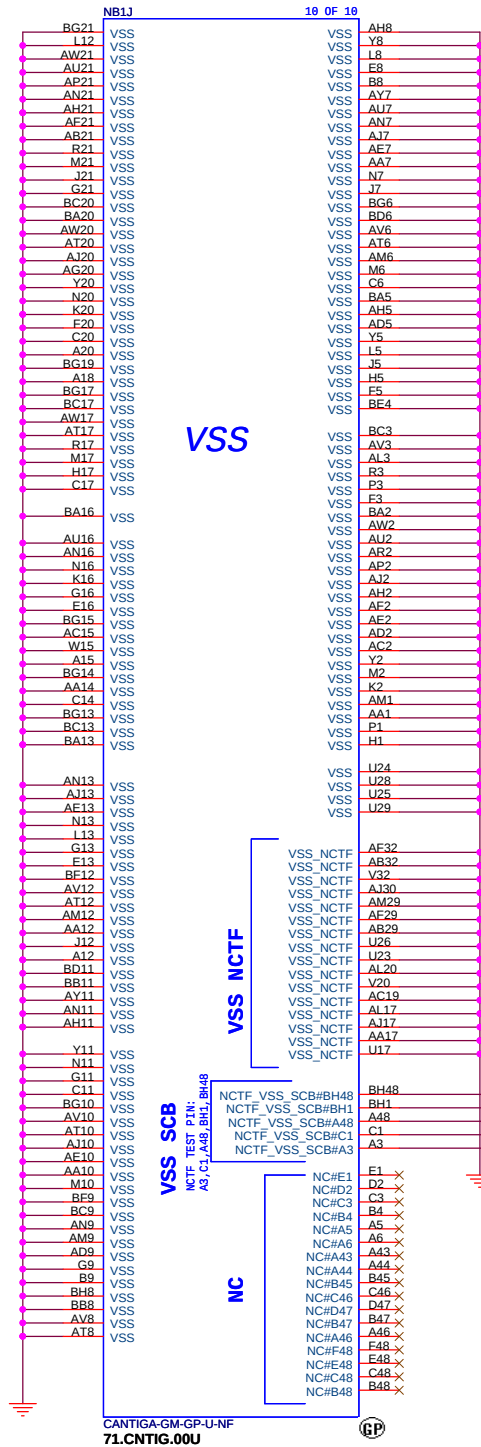


CANTIGA-GM-GP-U-NF
71.CNTIG.00U





CANTIGA-GM-GP-U-NF
71.CNTIG.00U



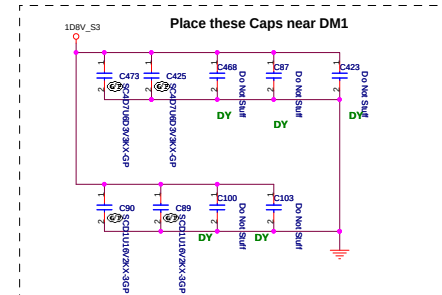
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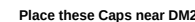
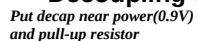


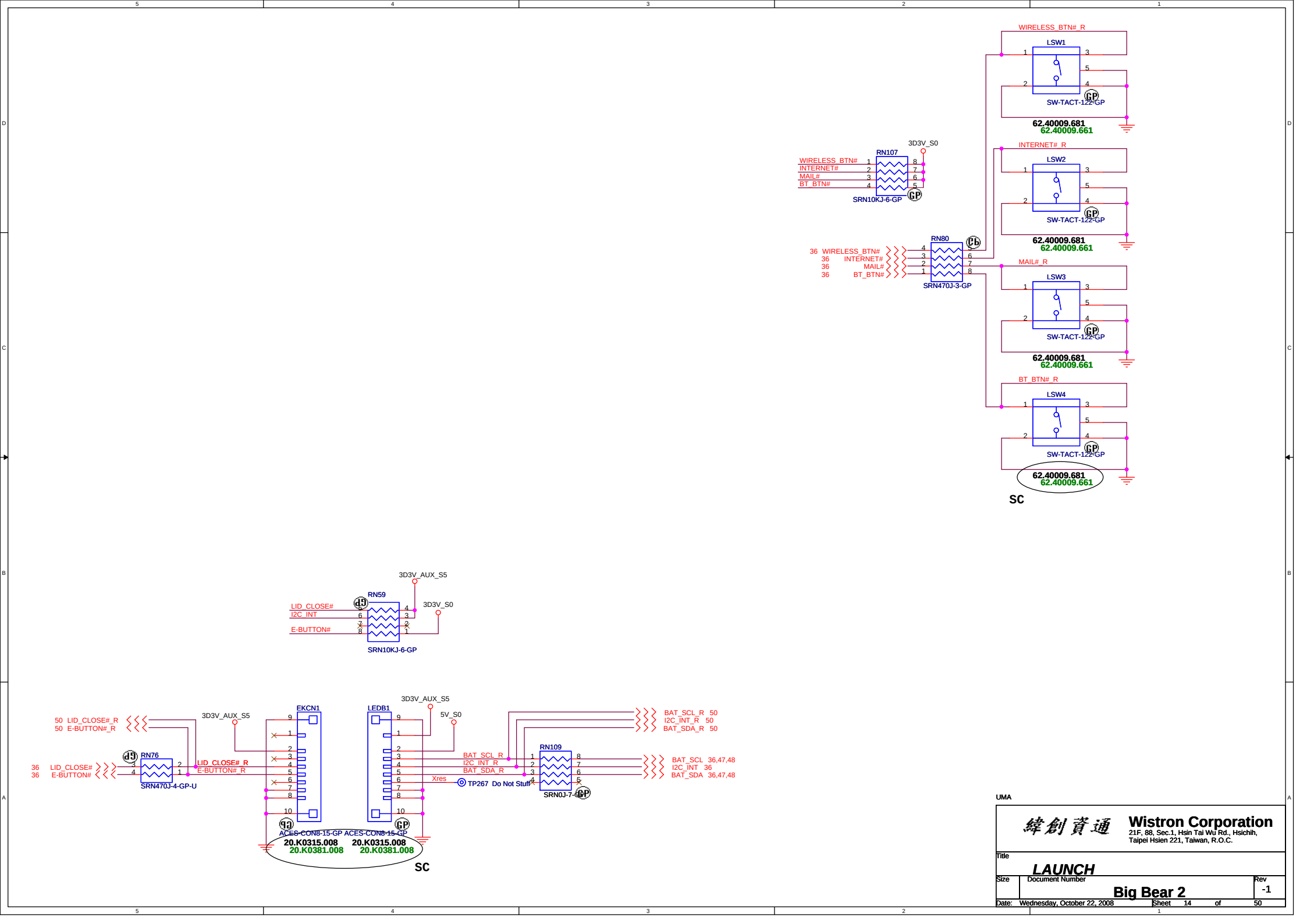
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Title: Cantiga (6 of 6)
Size: Document Number
Date: Wednesday, October 22, 2008
Sheet: 11 of 50
Rev: -1

Put decap near power(0.9V) and pull-up resistor

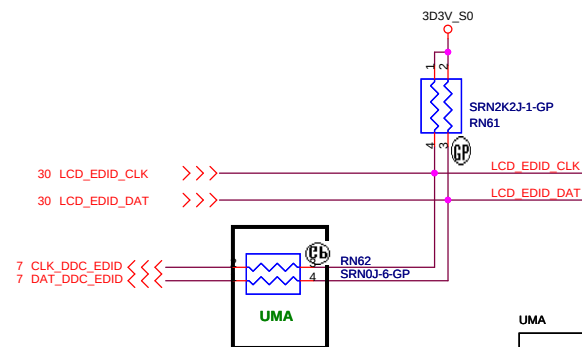
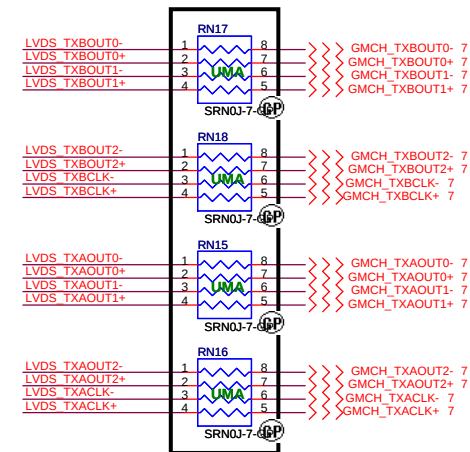
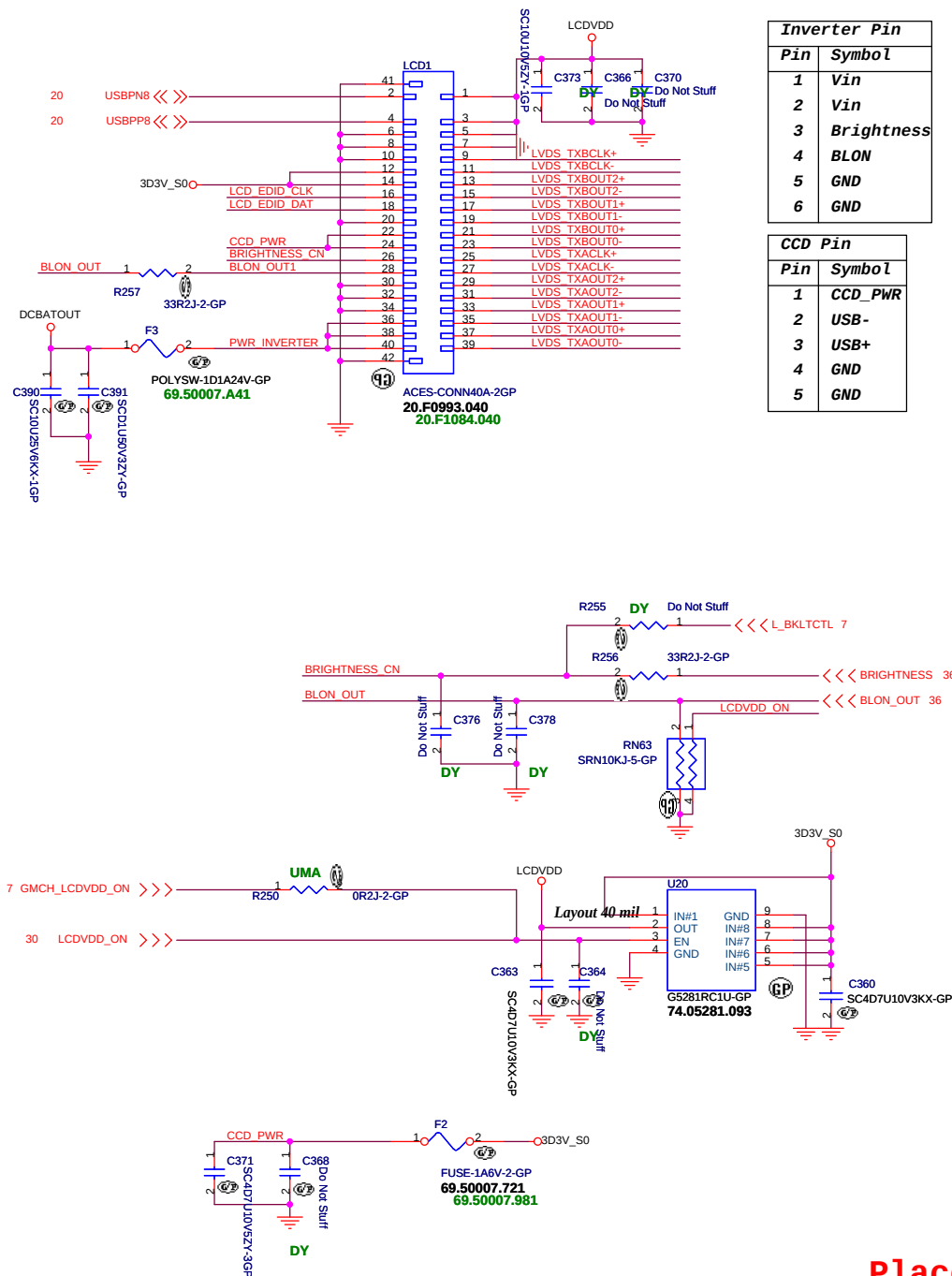




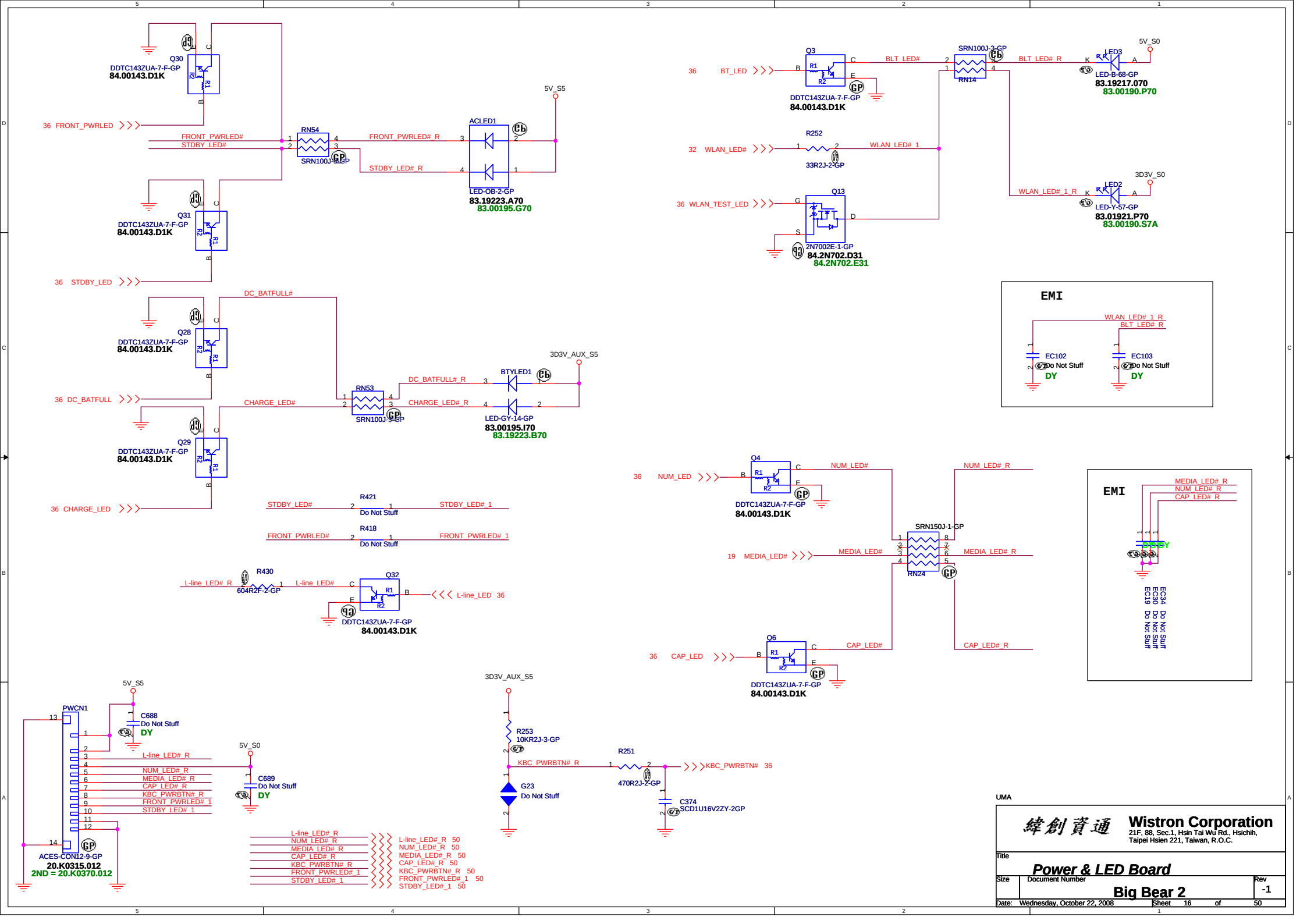


LCD/INVERTER/CCD CONN

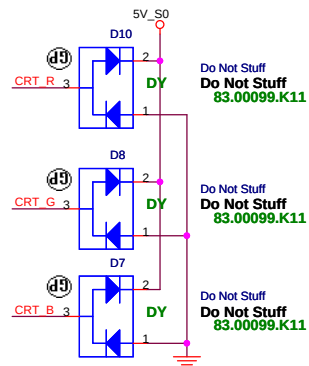
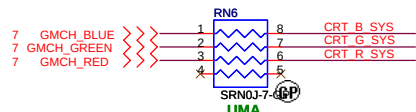
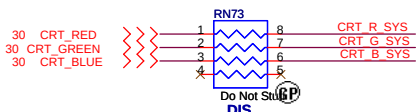
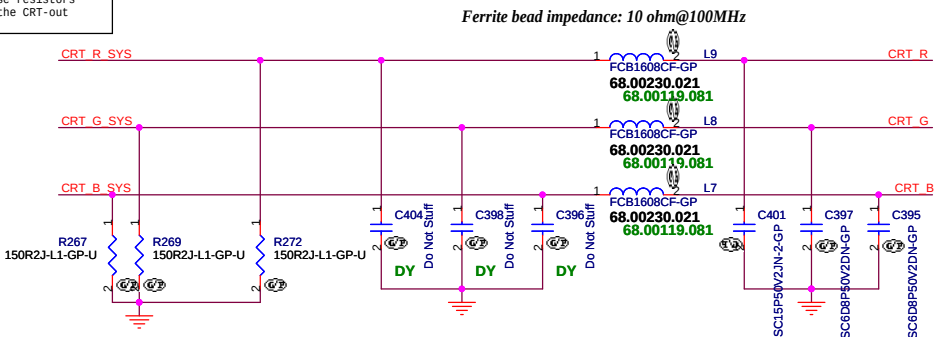
Place close to MXM slot for BB2



Place close to MXM slot for BB2

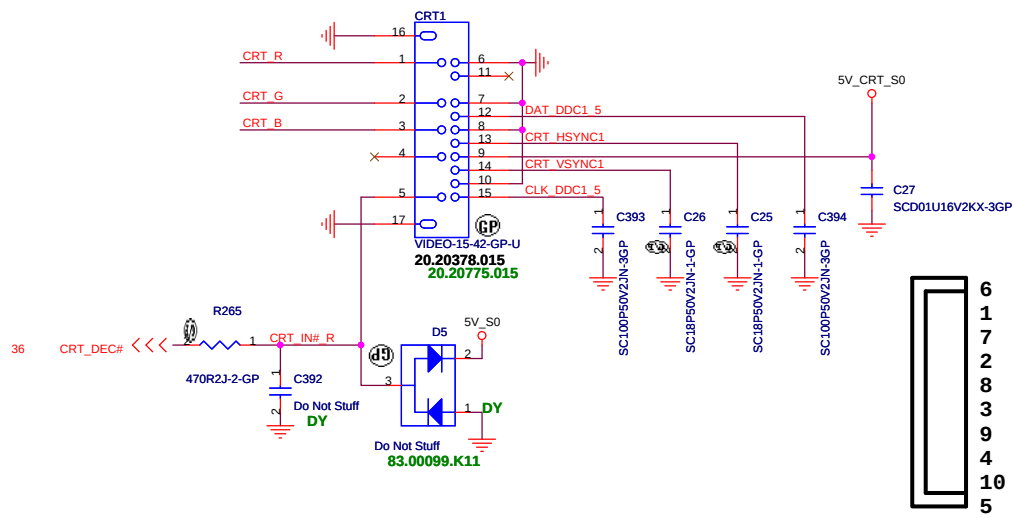


Layout Note:
Place these resistors
close to the CRT-out
connector

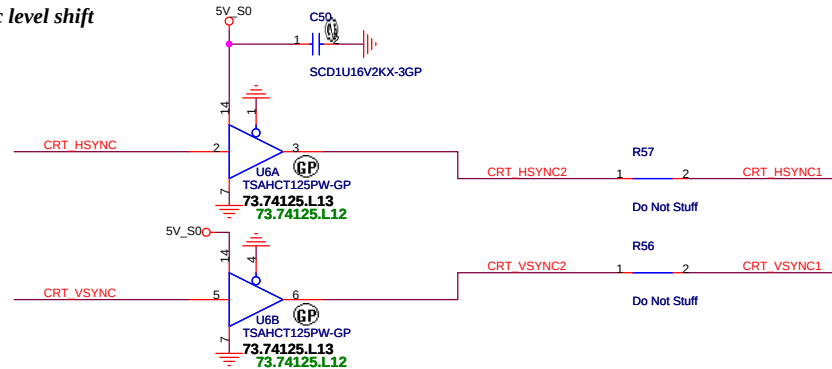


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

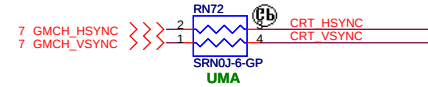
CRT I/F & CONNECTOR



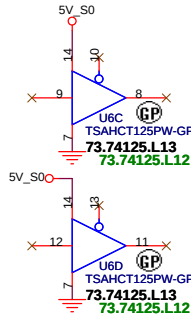
Hsync & Vsync level shift



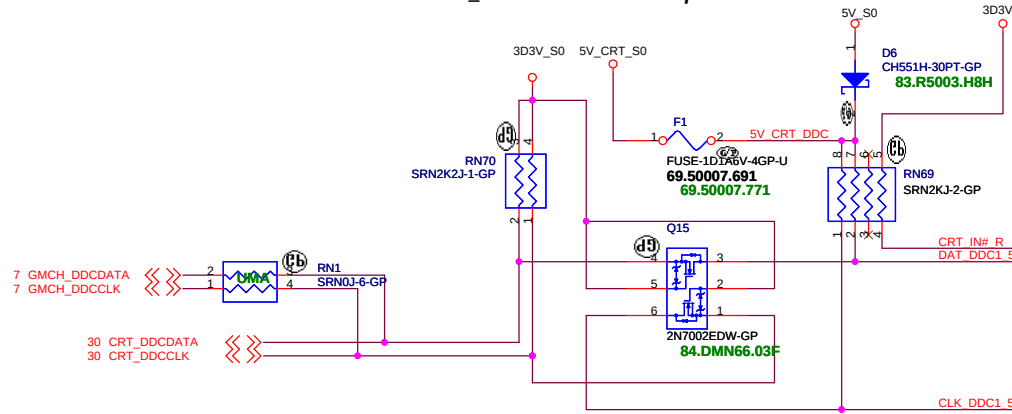
For UMA CRT



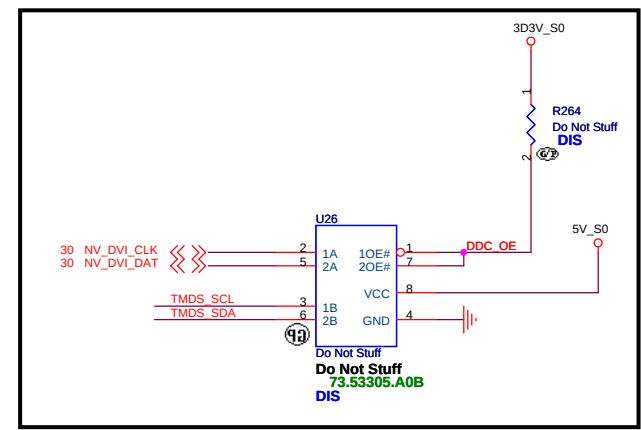
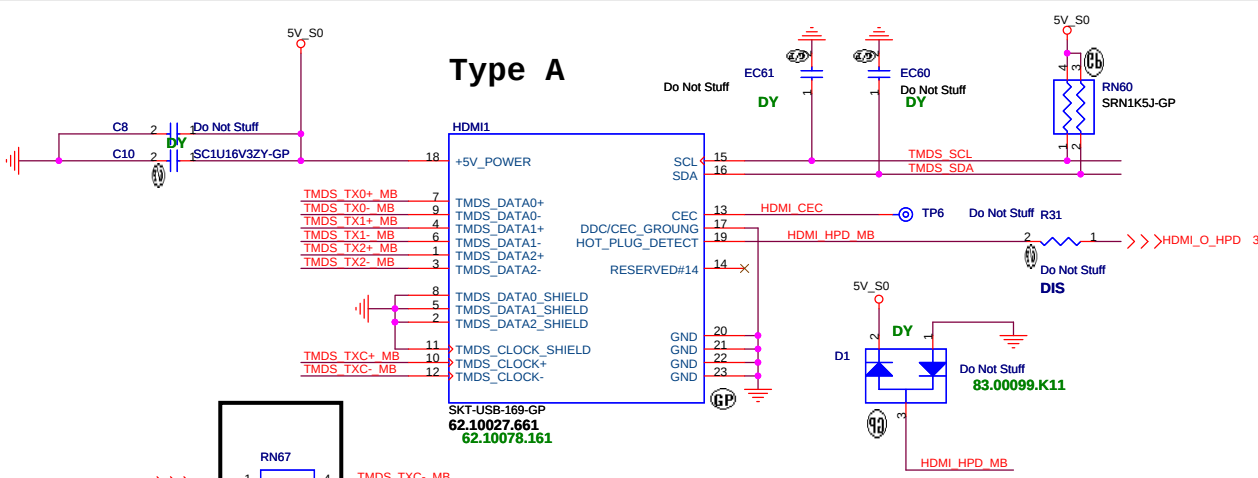
For DIS CRT



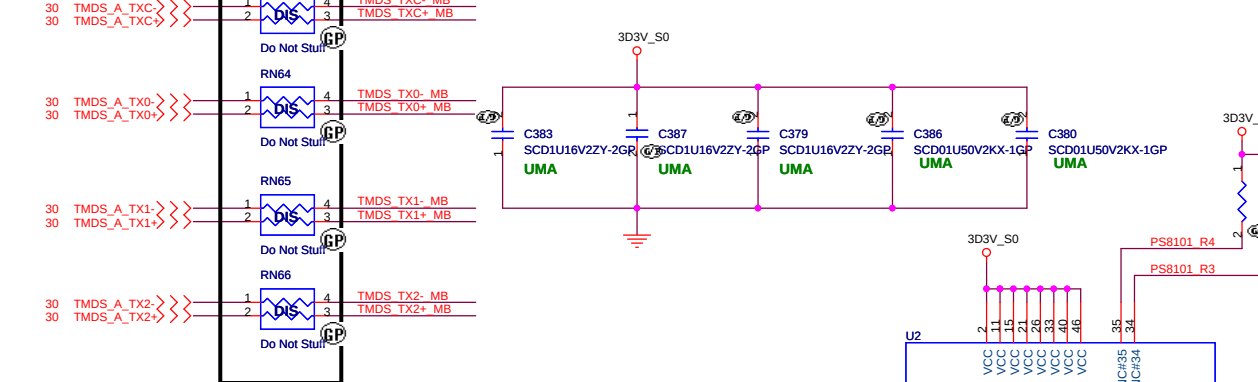
DDC_CLK & DATA level shift



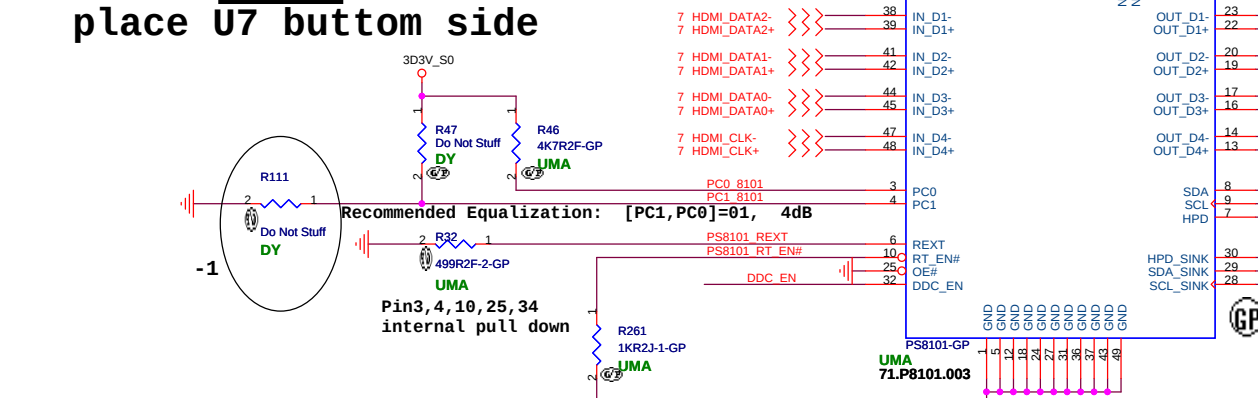
Type A



Close HDMI1

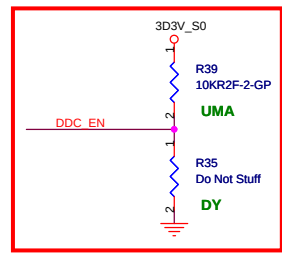


place U7 bottom side

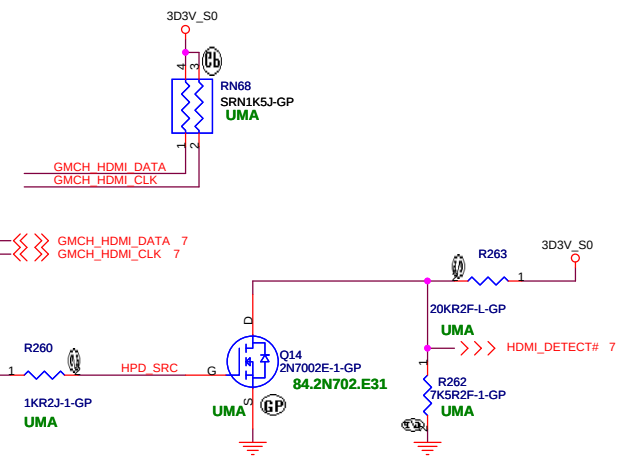


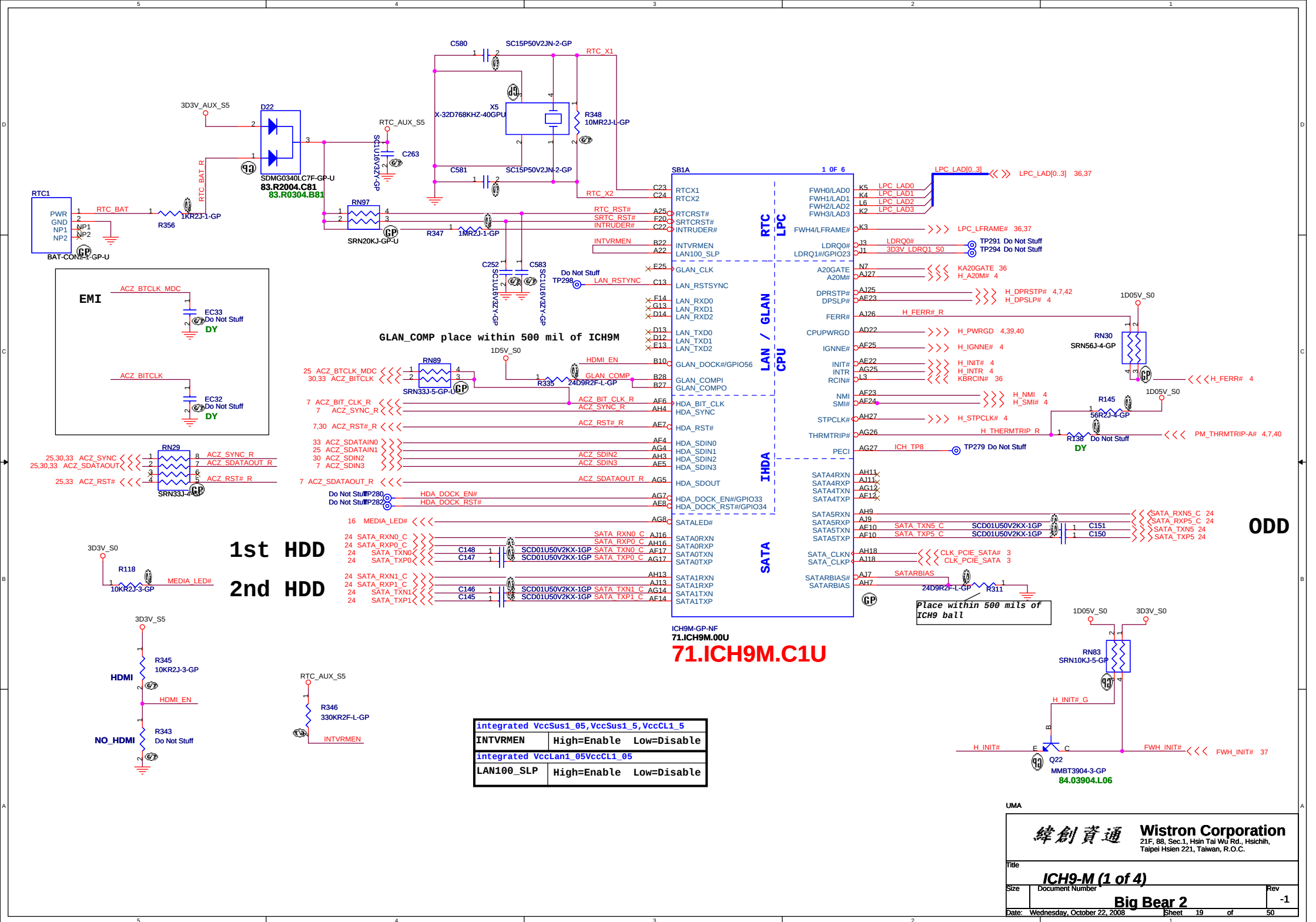
Recommended Equalization: [PC1,PC0]=01, 4dB

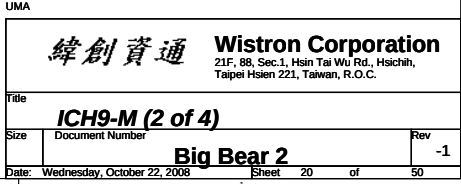
Pin3,4,10,25,34 internal pull down

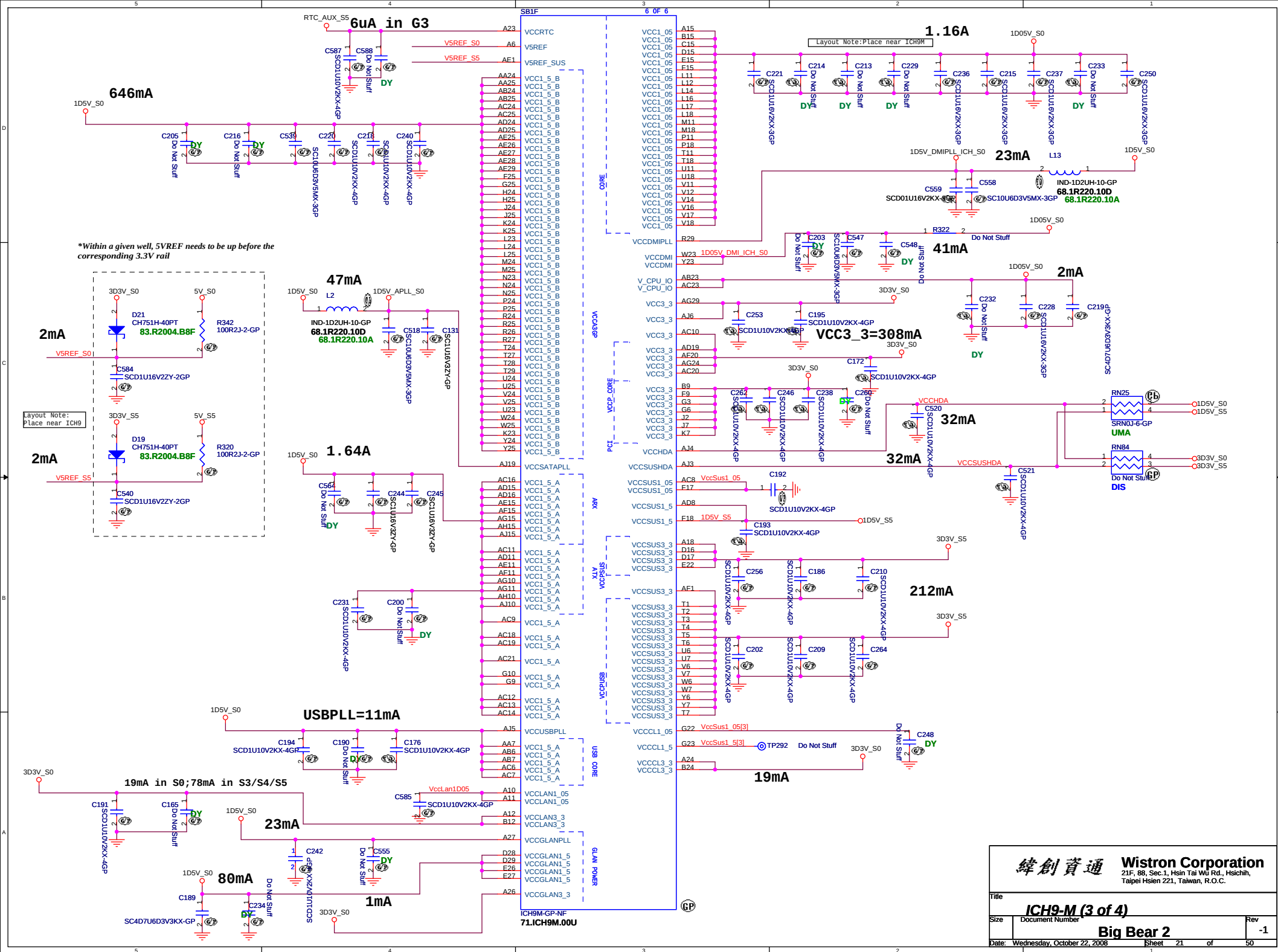


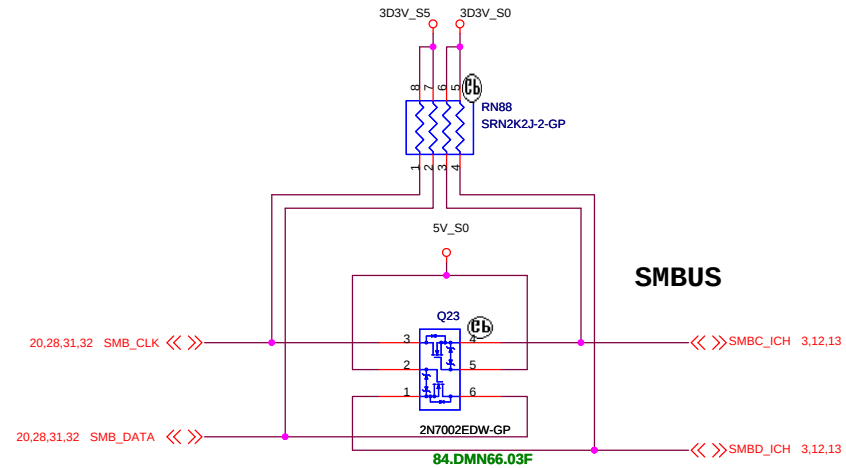
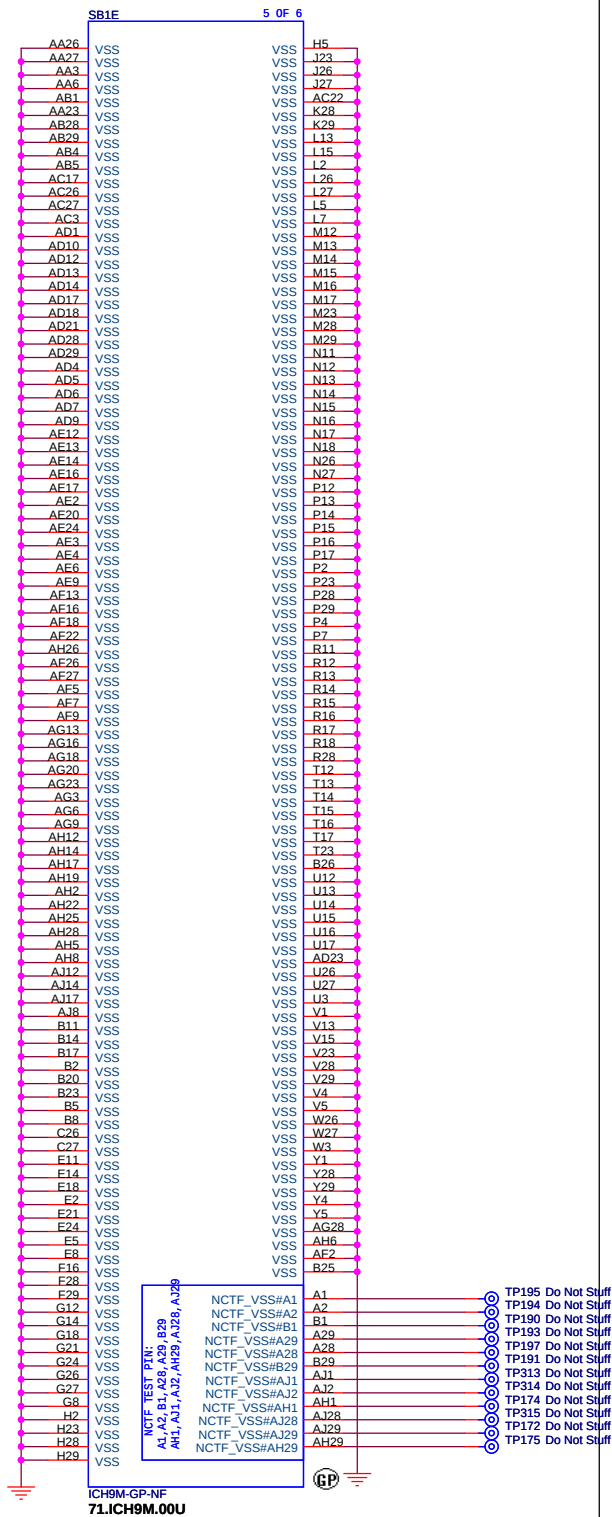
PIN34 DDCBUF:
1:DDC active buffer
0:DDC passive buffer

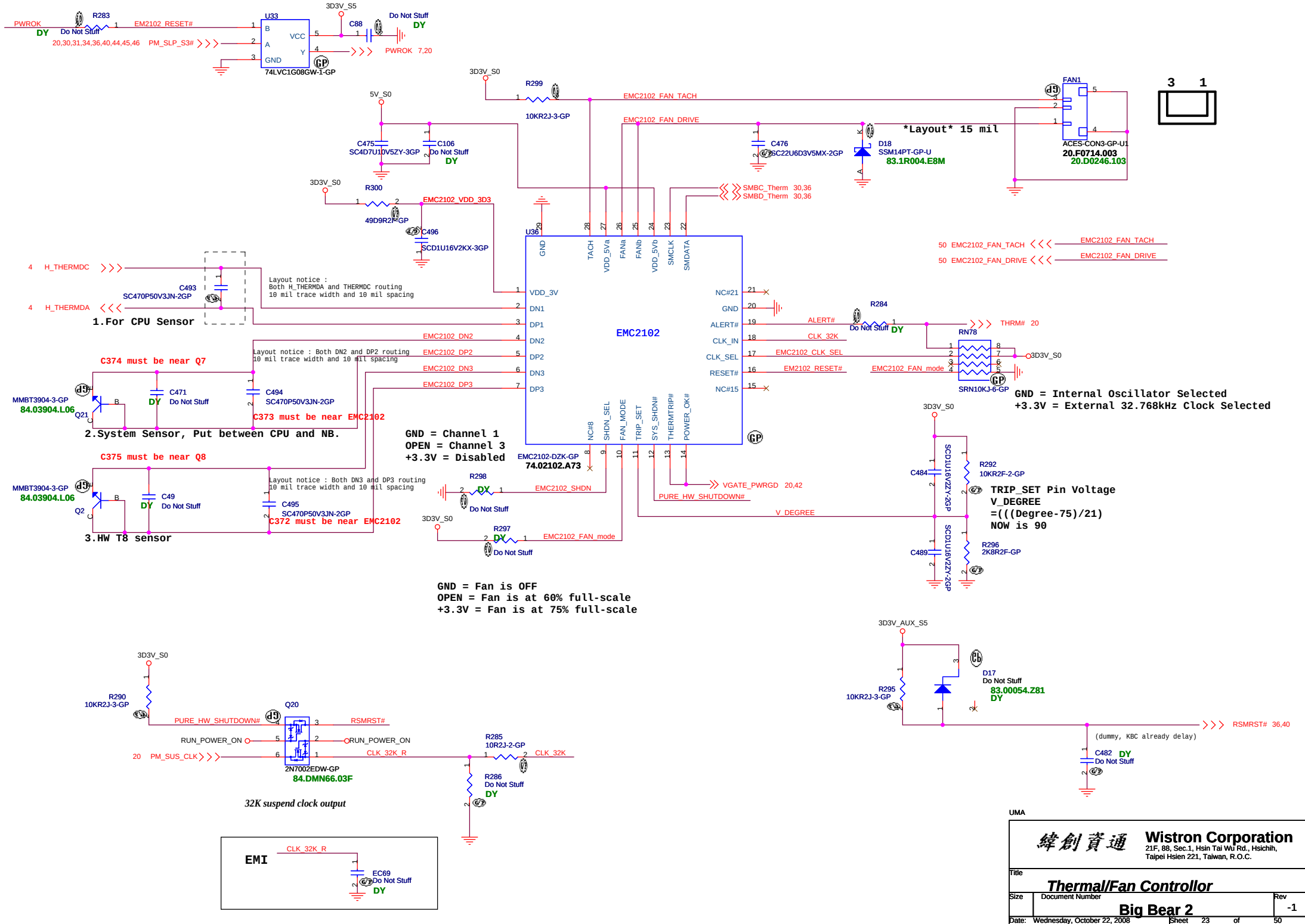






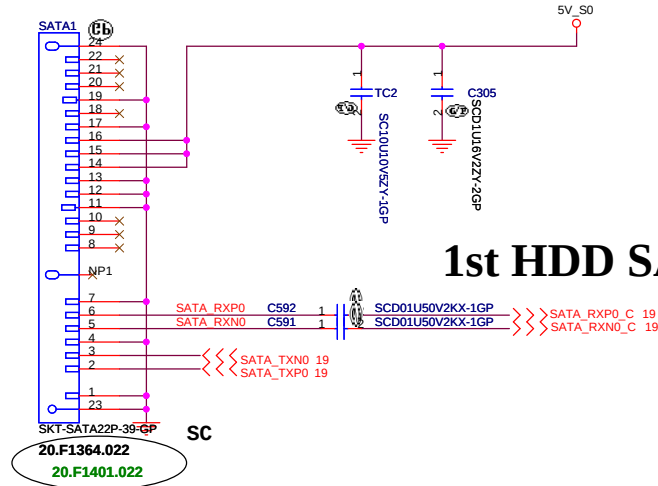




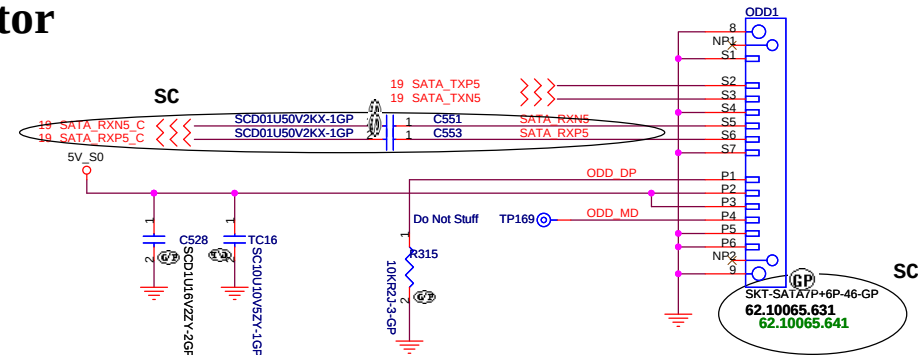
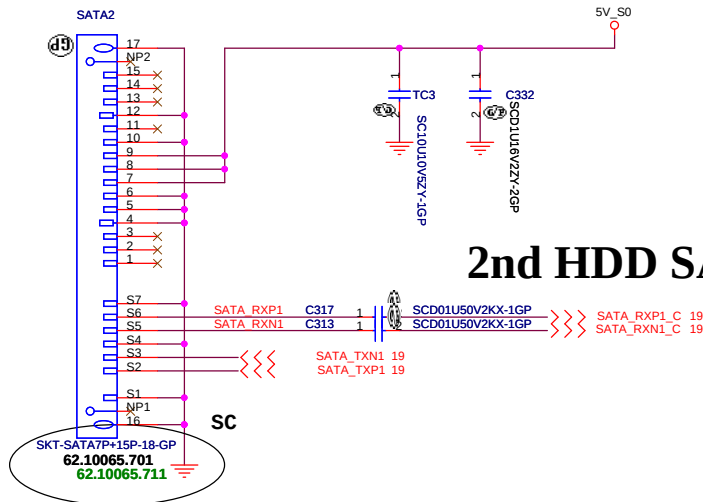


SATA ODD Connector

1st HDD SATA Connector



2nd HDD SATA Connector



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Title

HDD & ODD

Size Document Number

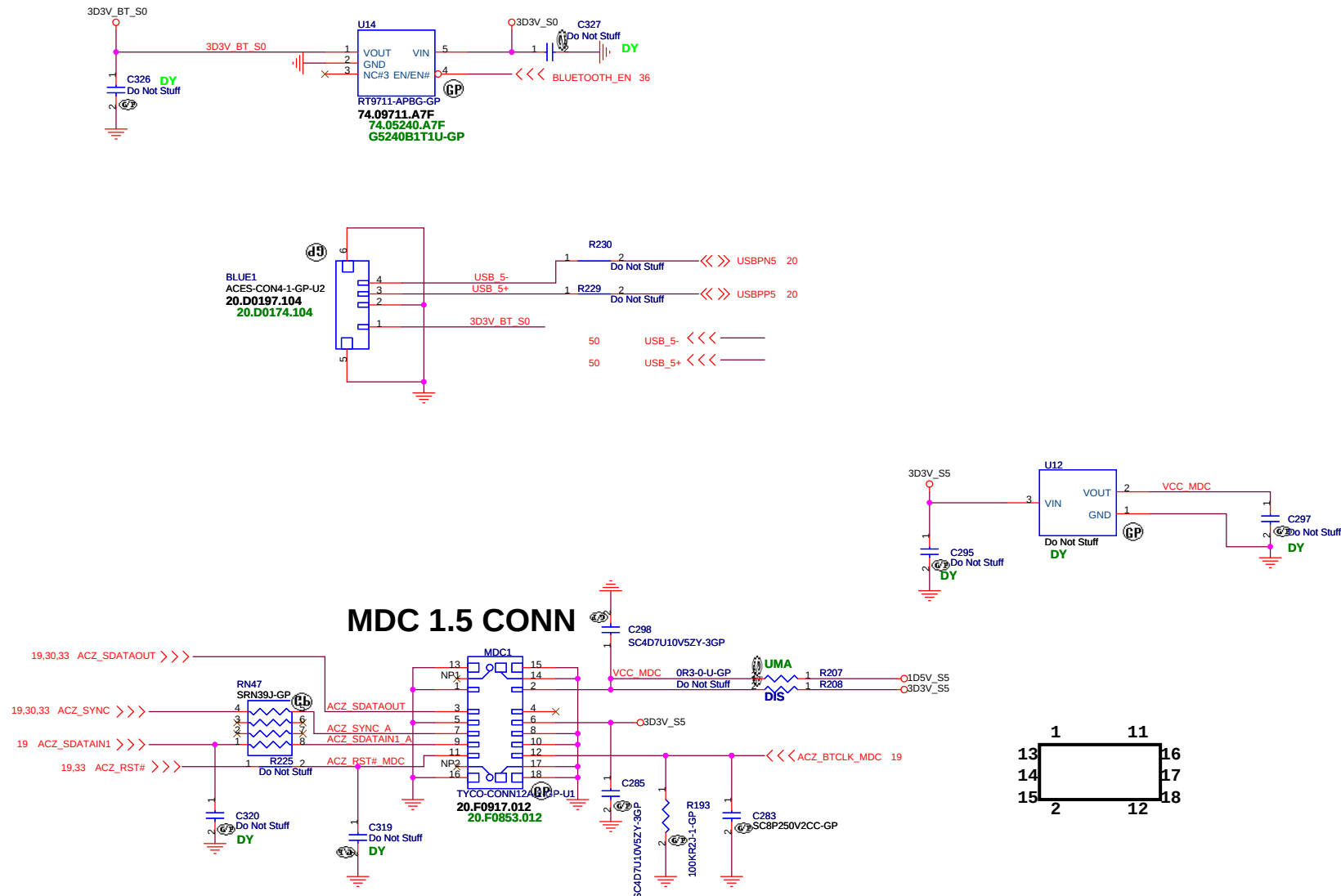
Big Bear 2 -1

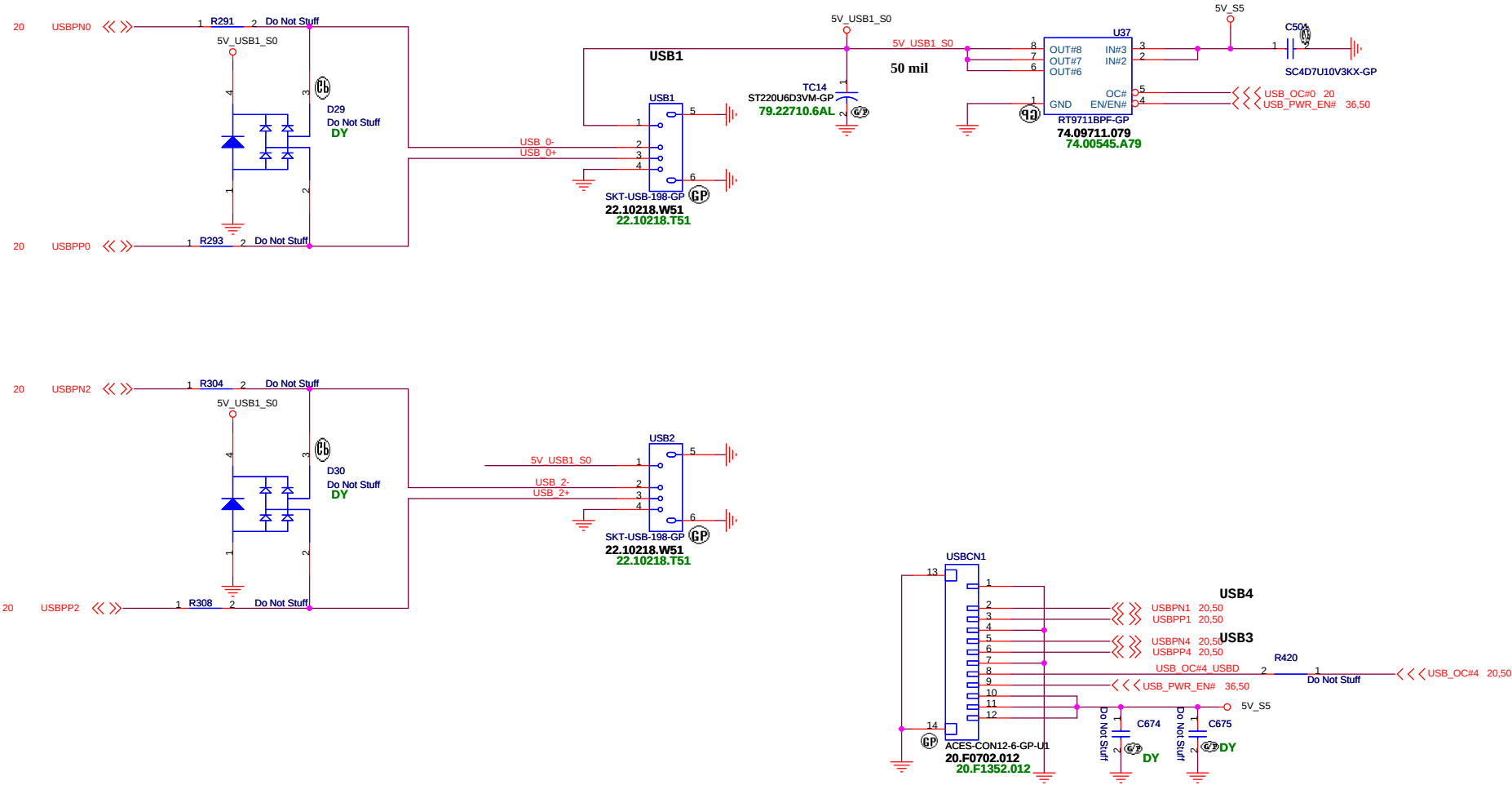
Date: Wednesday, October 22, 2008

Sheet 24 of 50

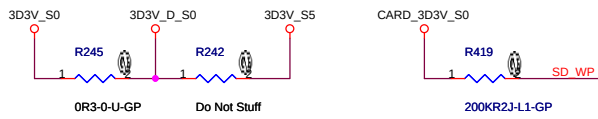
BLUETOOTH MODULE

1.5A / High Active Voltage 2V

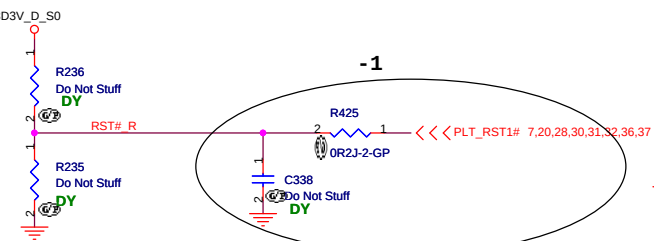
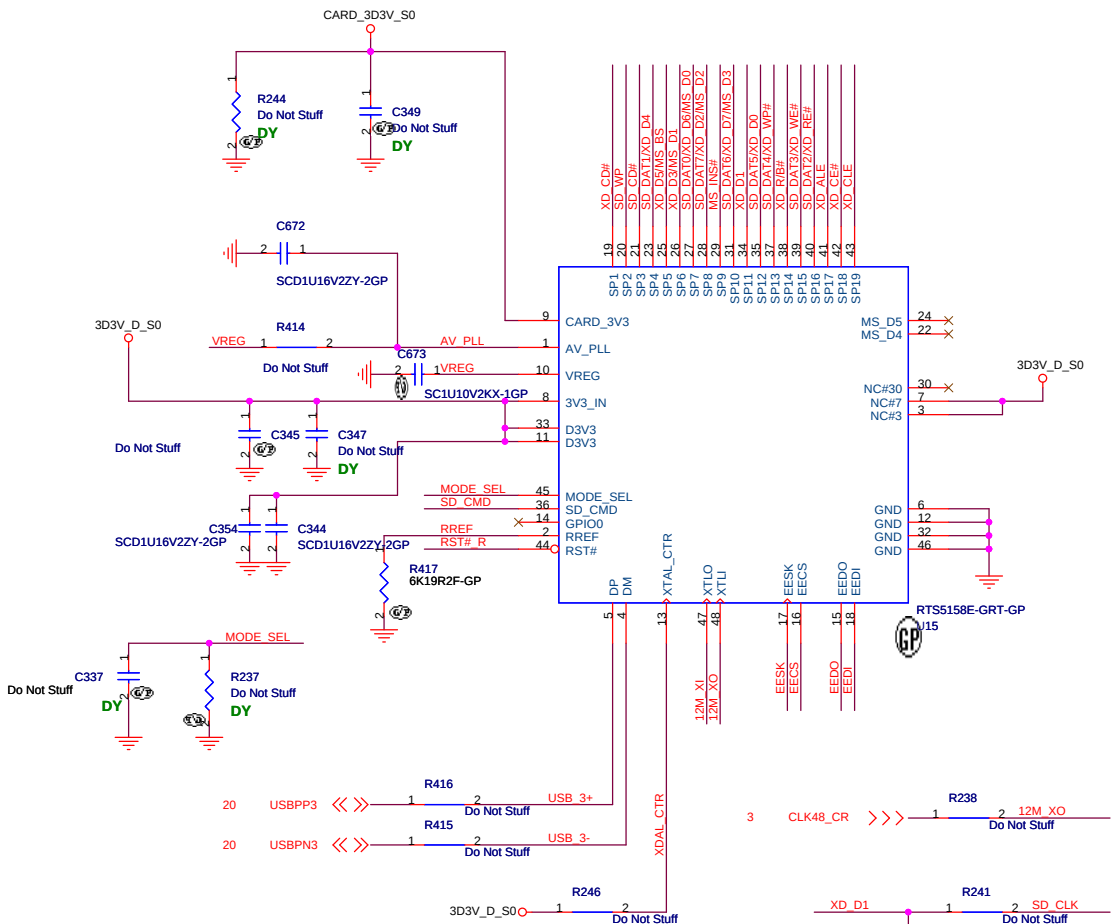




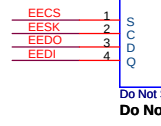
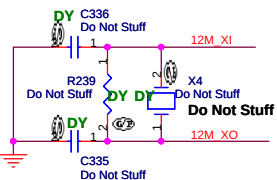
UMA



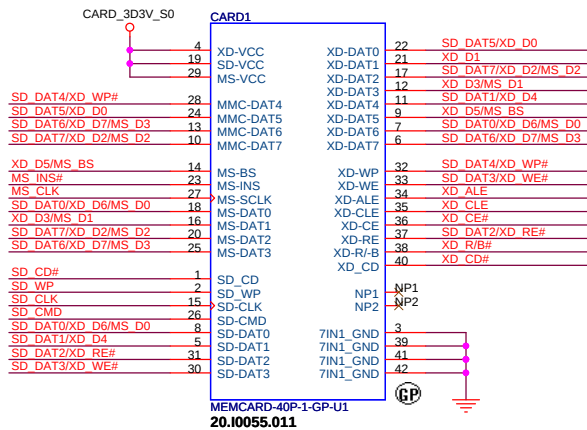
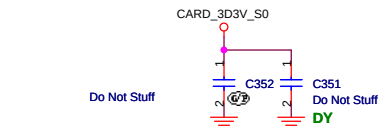
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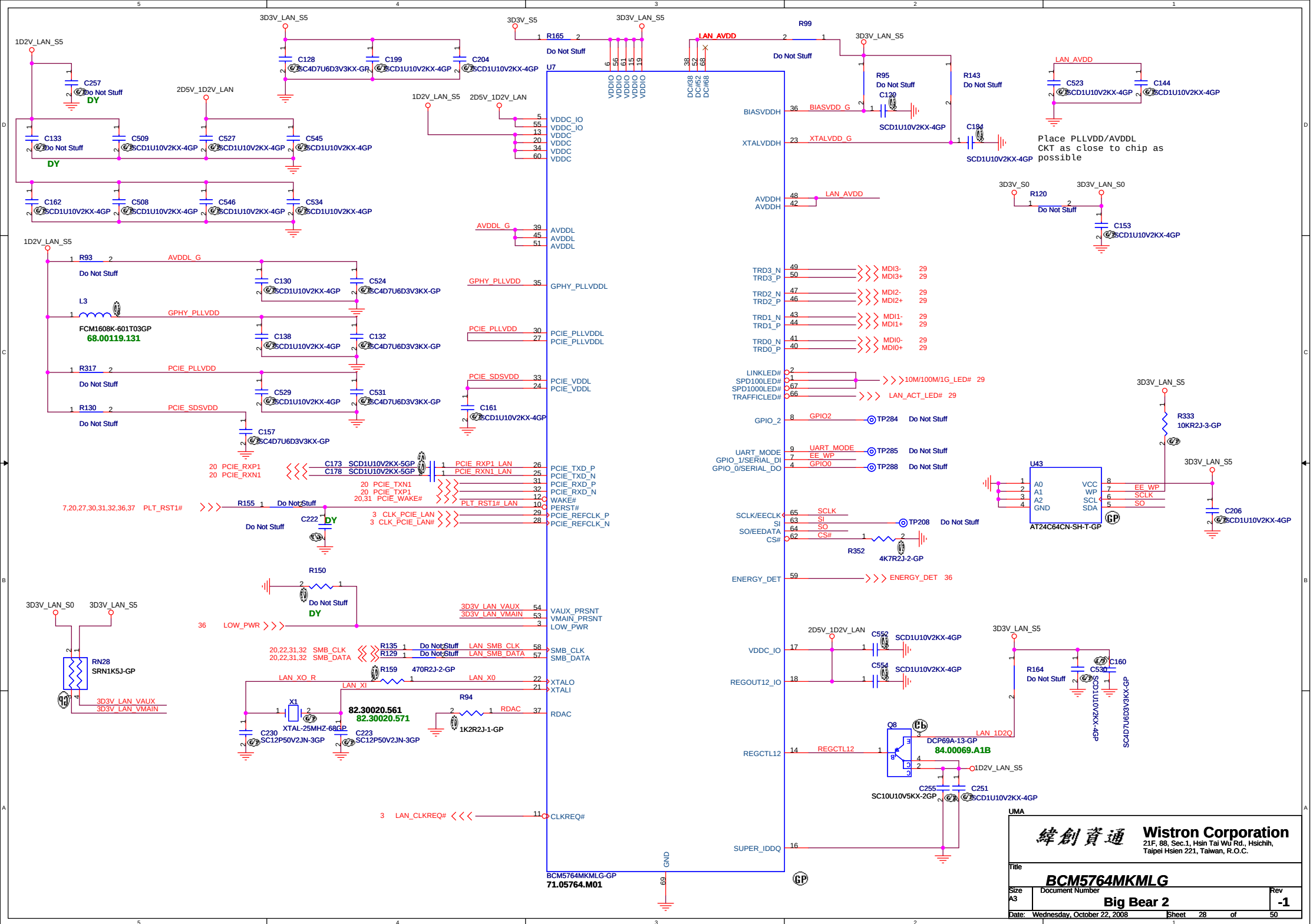


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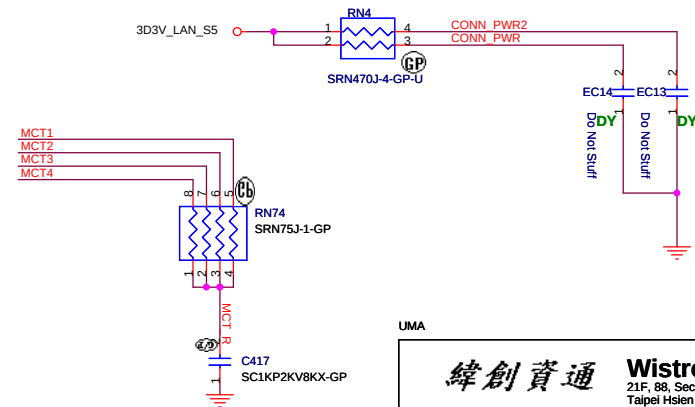
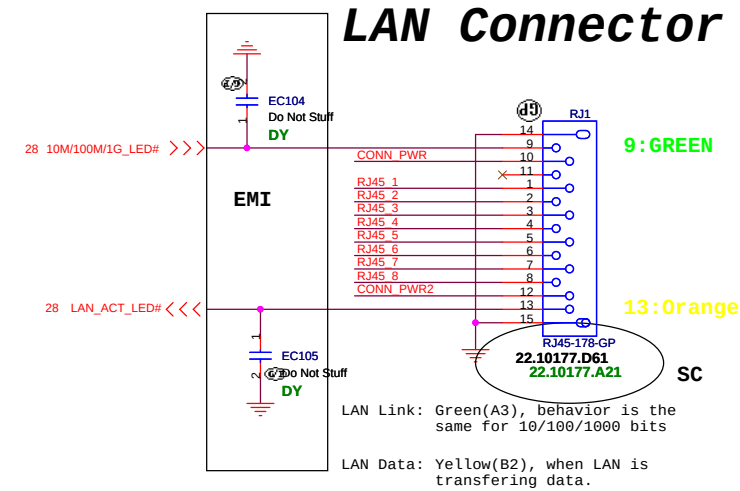
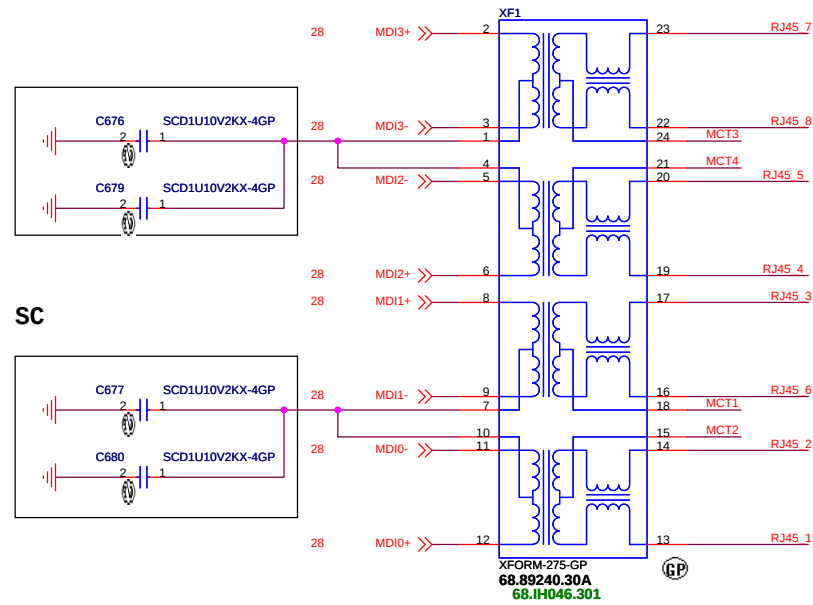
7 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)





LAN Connector

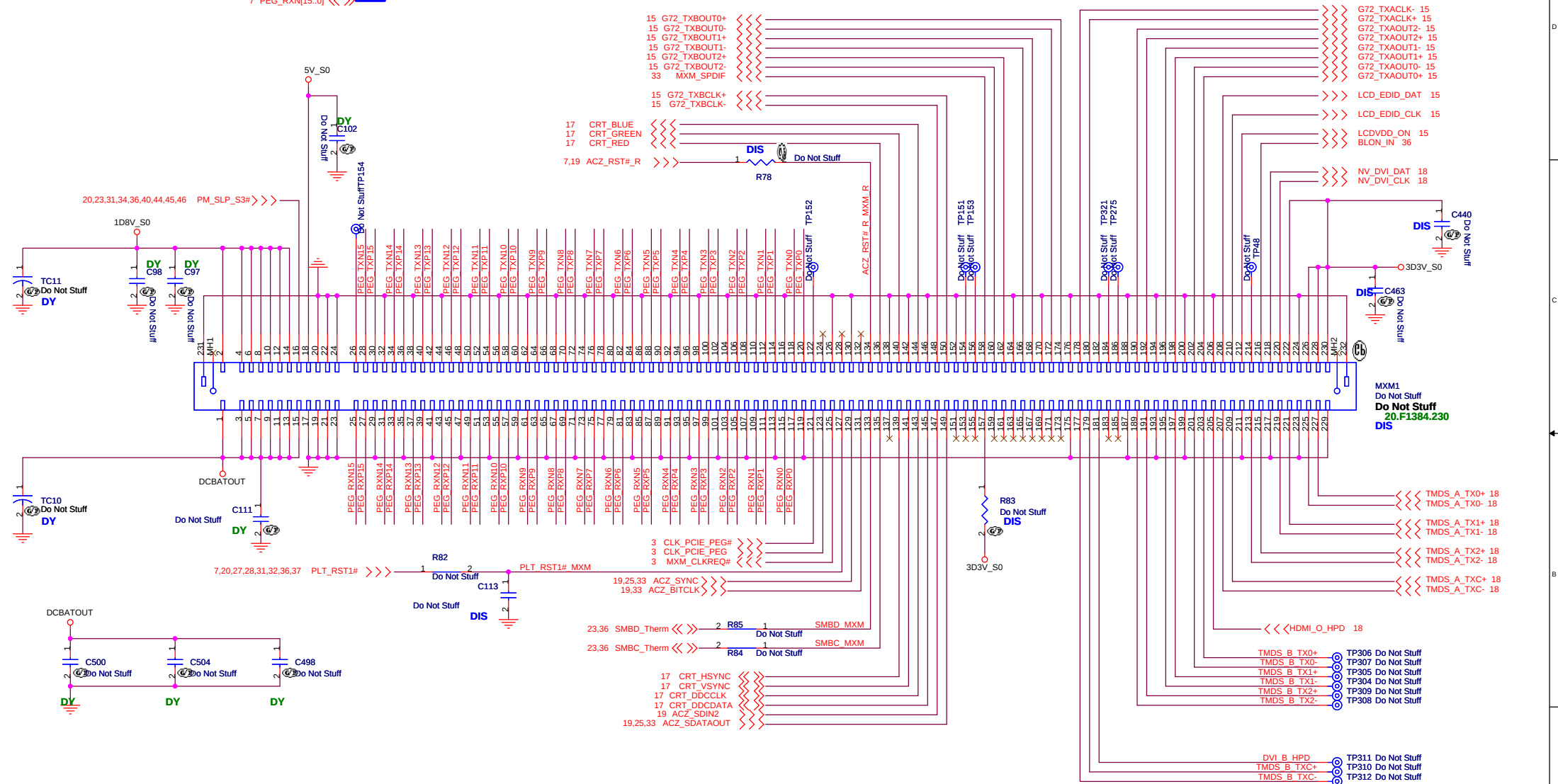
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



7 PEG_TXP[15..0] << >> 
7 PEG_TXN[15..0] << >> 

7 PEG_RXP[15..0] << >> 
7 PEG_RXN[15..0] << >> 

NV SMBus
A(pin143&145) : VGA(CRT) / Dock
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

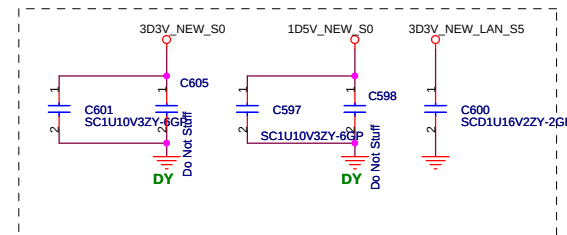


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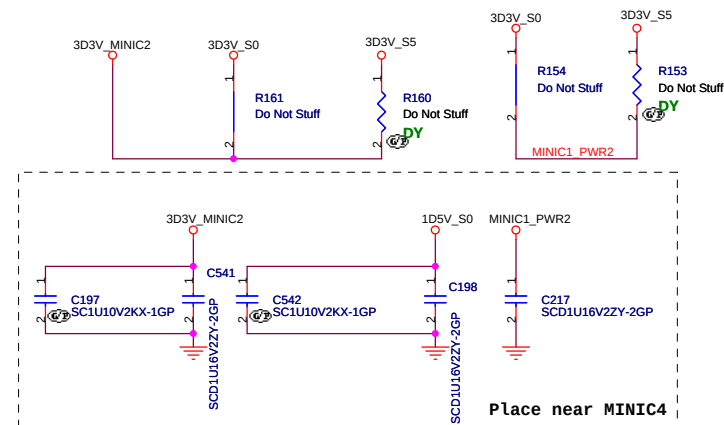
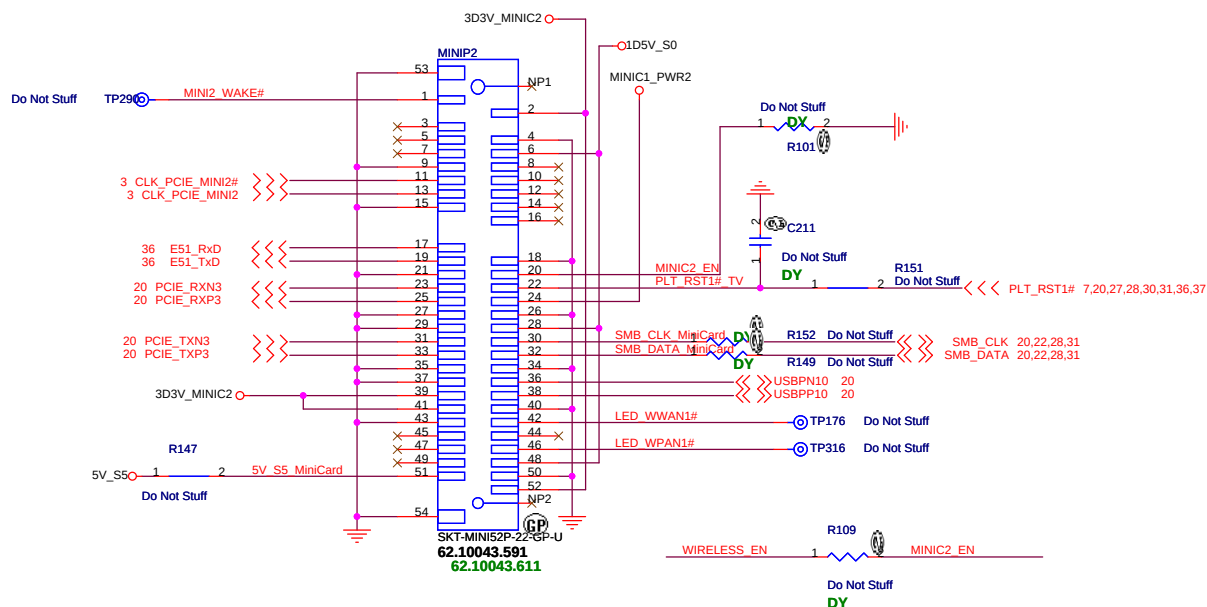
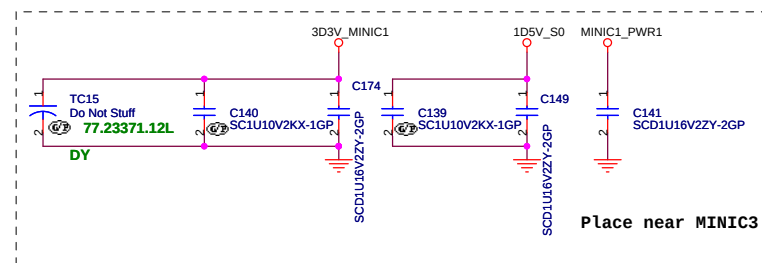
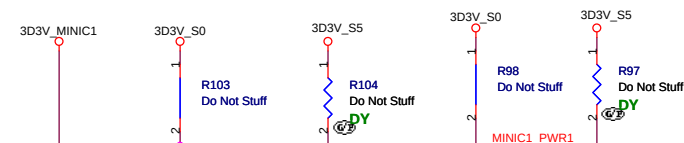
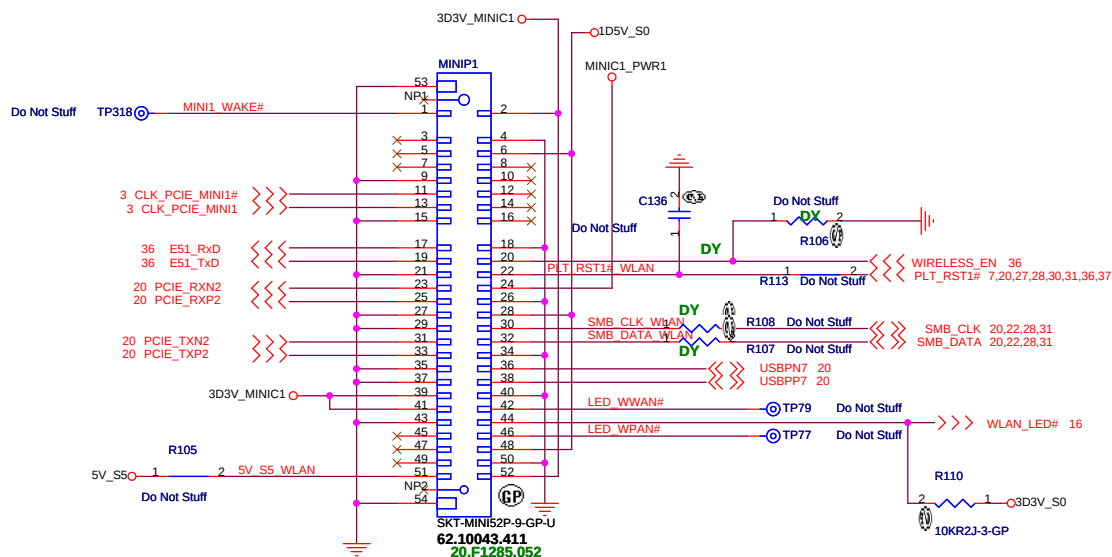
TOP VIEW

26
1

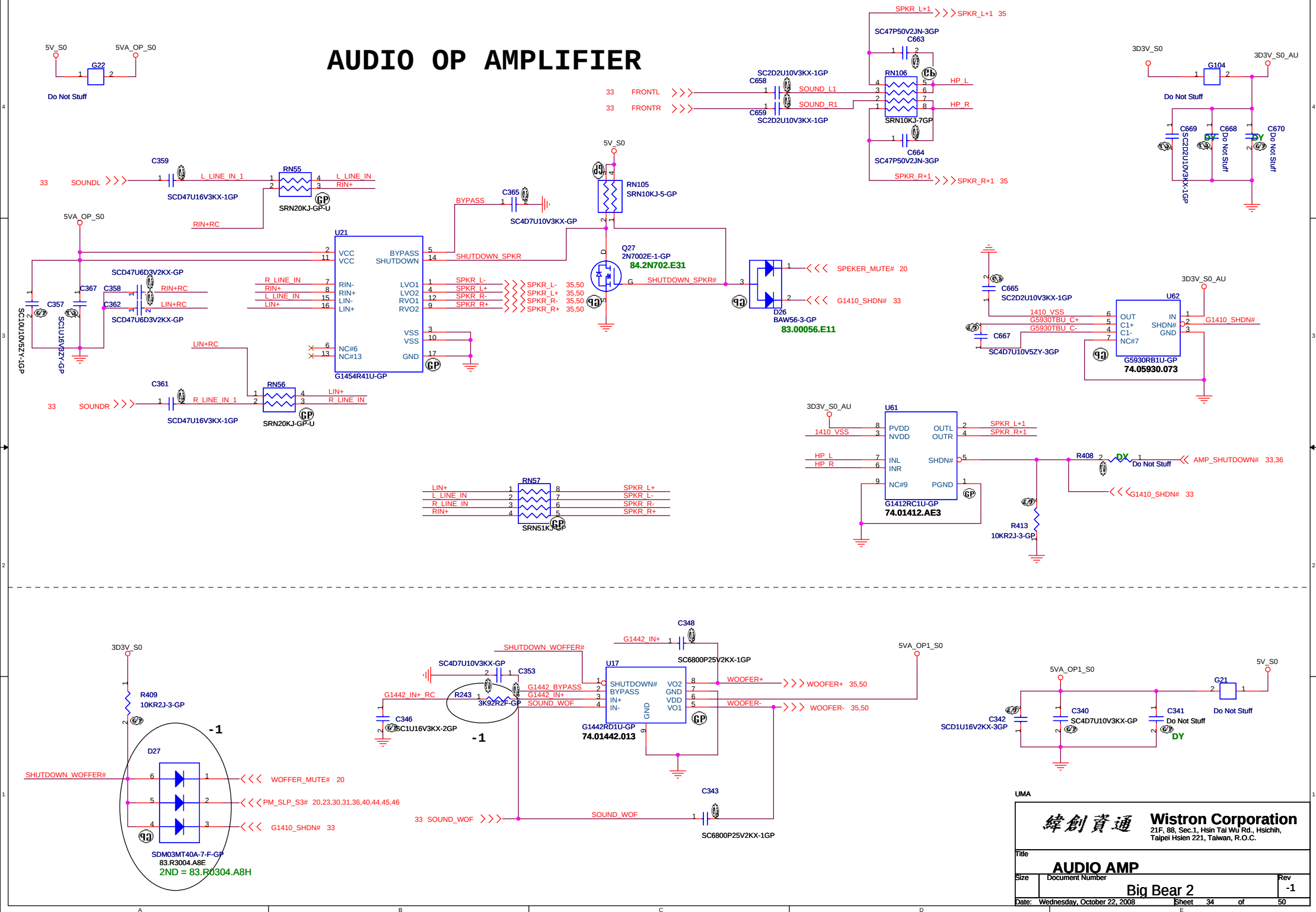


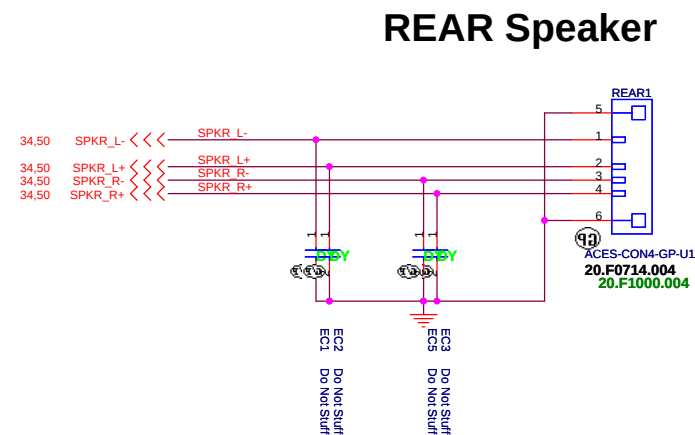
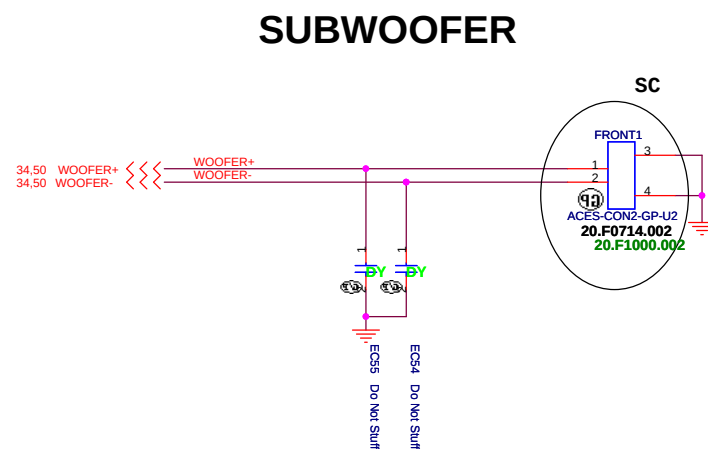
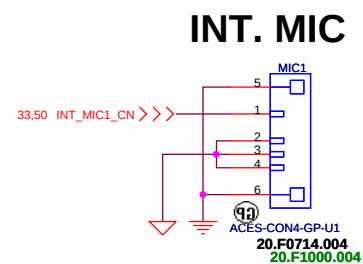
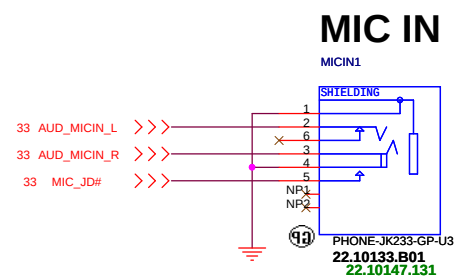
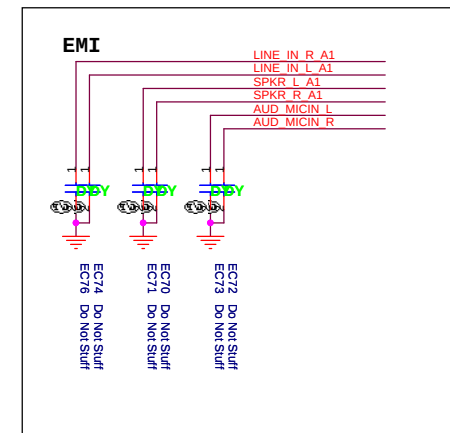
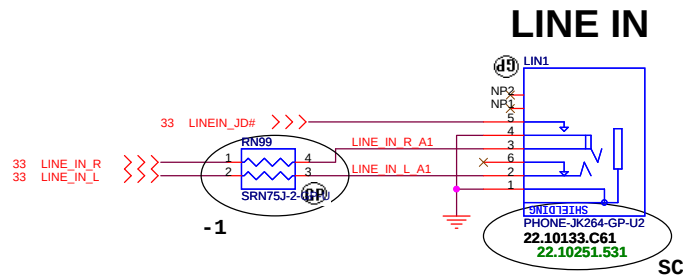
Title			
NEW CARD			
Size	Document Number	Rev	
	Big Bear 2	-1	
Date:	Wednesday, October 22, 2008	Sheet	31 of 50

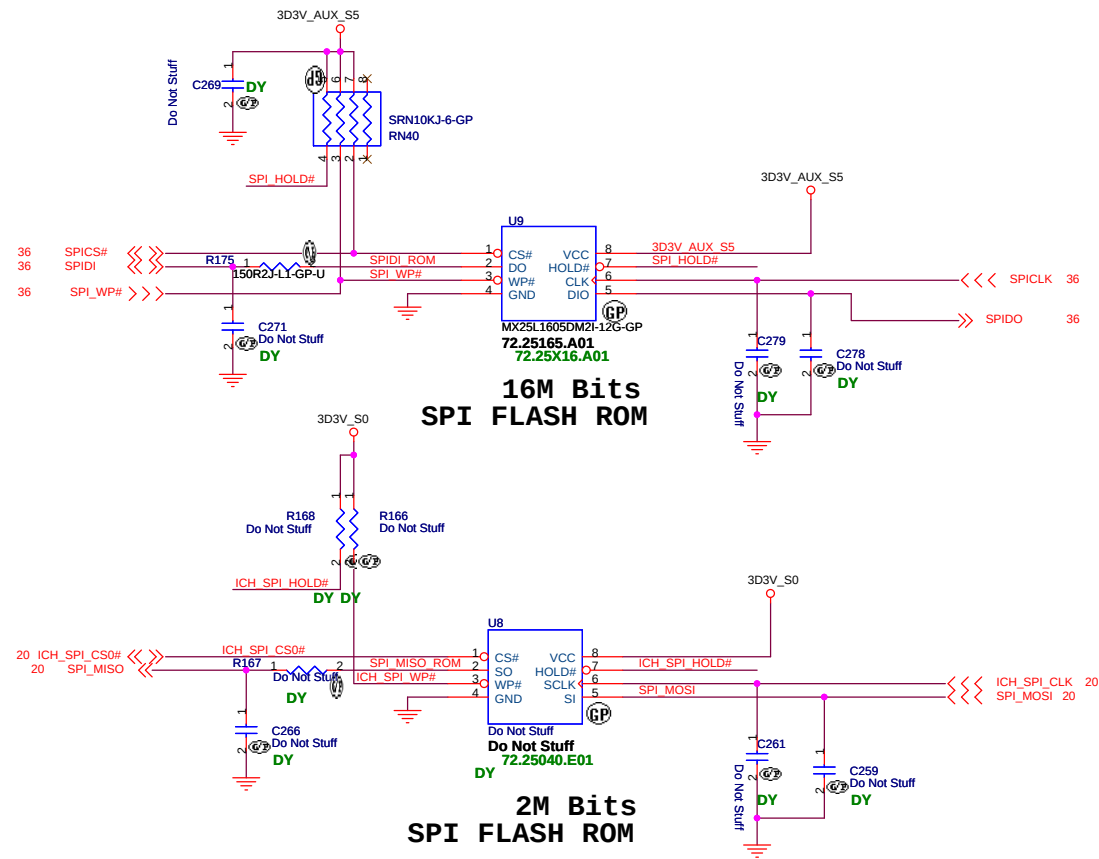
Mini Card Connector(WLAN)



AUDIO OP AMPLIFIER







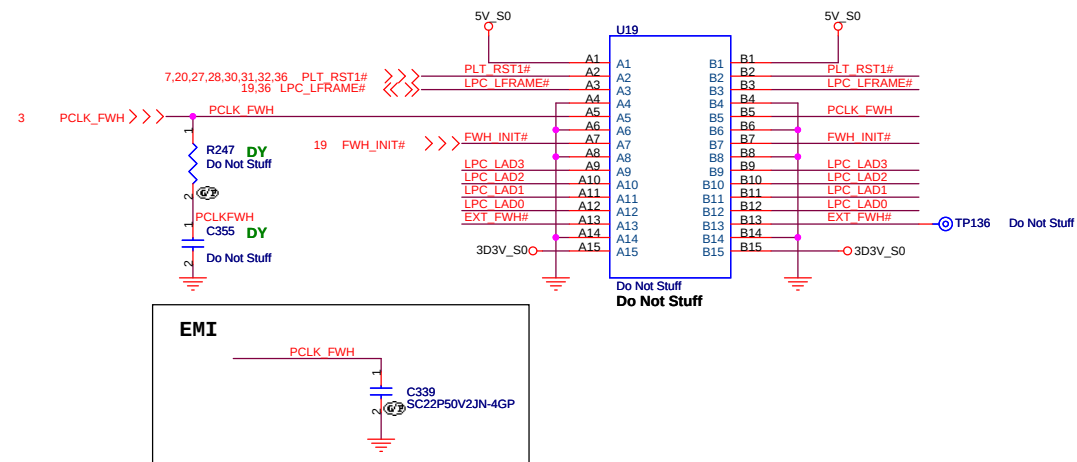
TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

19,36 LPC_LAD[0..3] <<< LPC_LAD[0..3]

GOLDEN FINGER FOR DEBUG BOARD

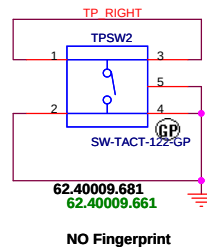
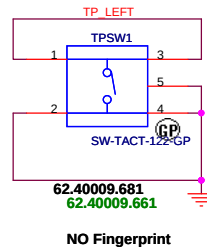
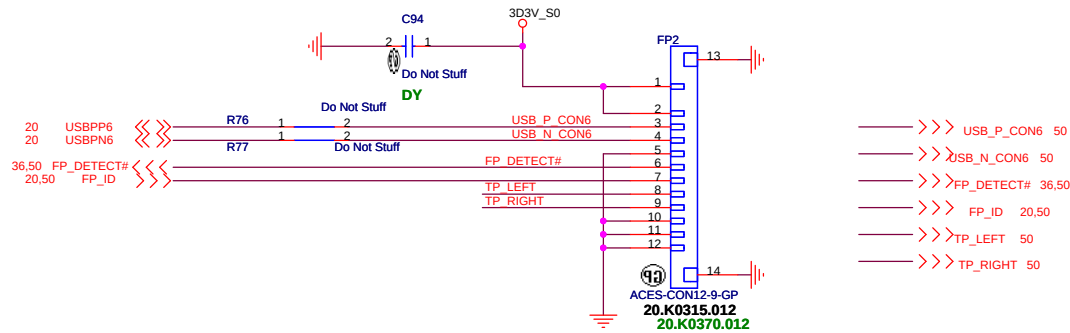


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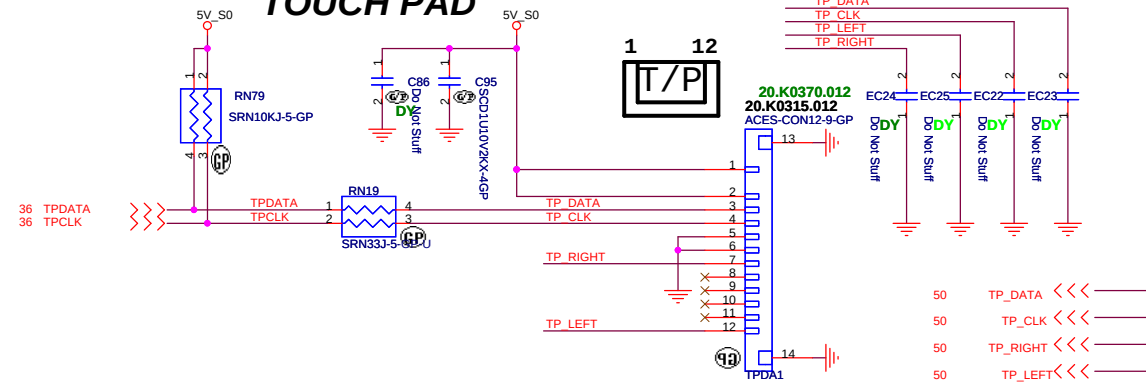
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Title		BIOS	
Size	Document Number	Big Bear 2	
Date: Wednesday, October 22, 2008	Sheet 37 of 50	Rev	-1

Finger printer



TOUCH PAD

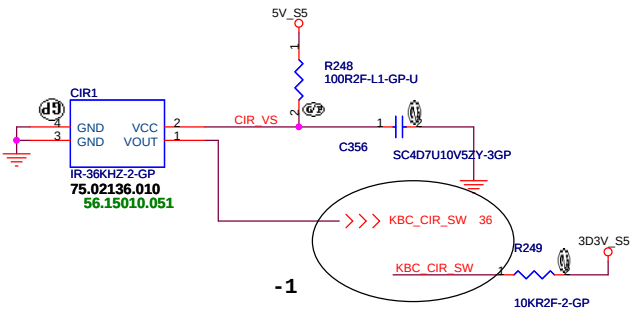


UMA

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Title		Finger Printer and Touch PAD	
Size	Document Number	Rev	
A3	Big Bear 2	-1	
Date:	Wednesday, October 22, 2008	Sheet	38 of 50

CIR Module

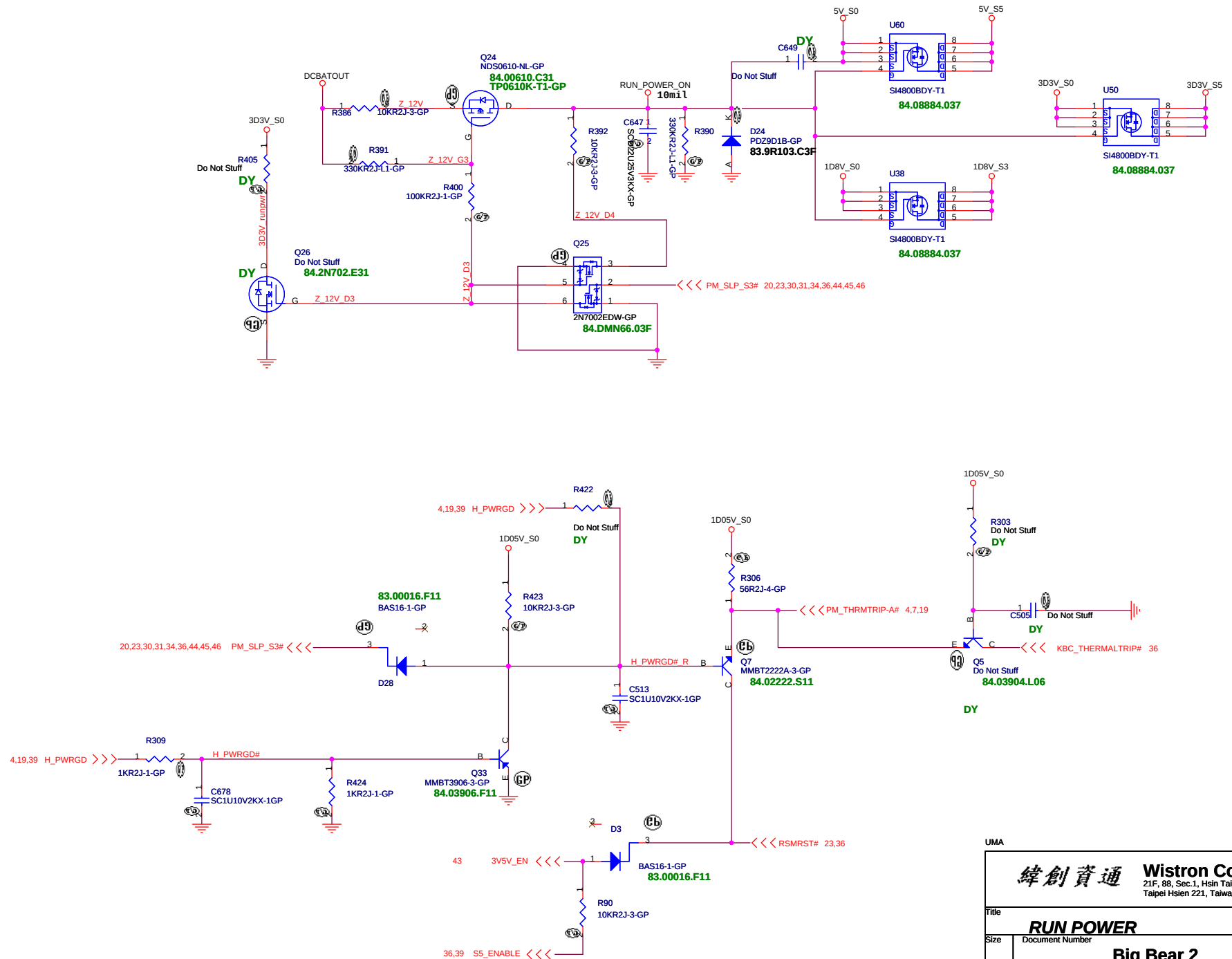


Check test point

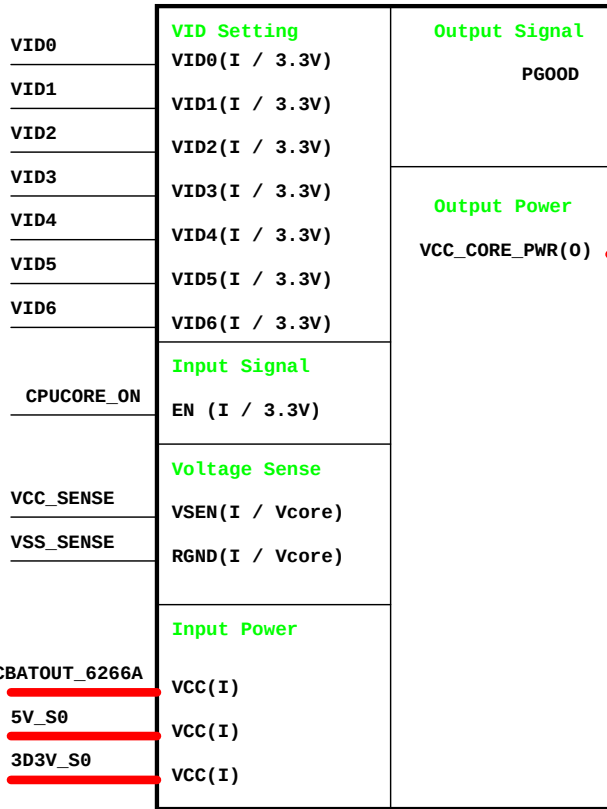
- 3D3V_S0 — TP202 Do Not Stuff
- 3D3V_AUX_S5 — TP141 Do Not Stuff
- 3D3V_S5 — TP120 Do Not Stuff
- 5V_S5 — TP130 Do Not Stuff
- 20,36 PM_PWRBTN# <<< — TP115 Do Not Stuff
- 4,19,40 H_PWRGD <<< — TP320 Do Not Stuff
- 36,40 S5_ENABLE <<< — TP110 Do Not Stuff
- 4,6 H_CPURST# <<< — TP278 Do Not Stuff

Test Point 放在 Dimm Door 打開可量測處

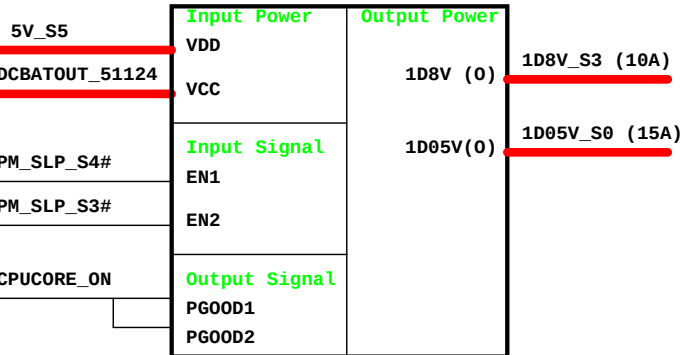
Run Power



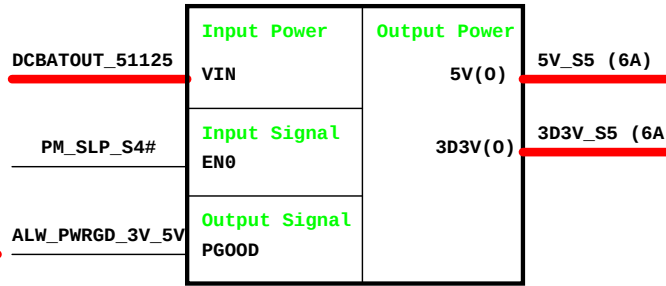
CPU_CORE
ISL6266A



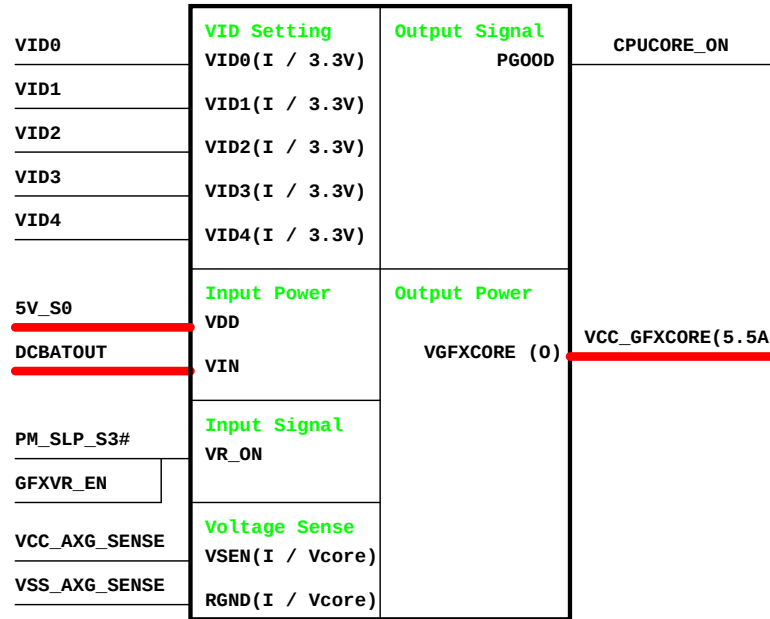
TPS51124
1D8V/1D05V



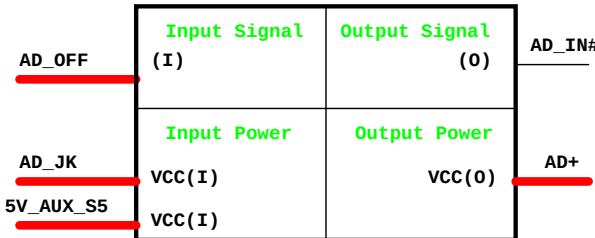
TPS51125
5V/3D3V



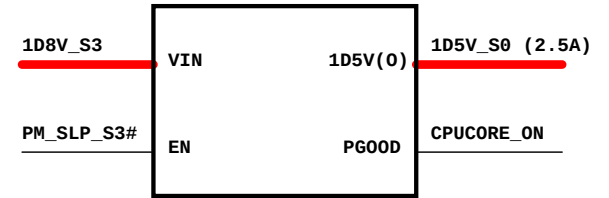
GFX_CORE
ISL6263A



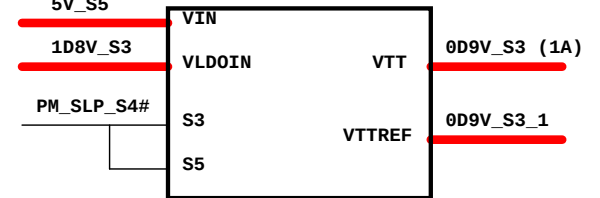
Adapter



RT9018A
1D5V_S0



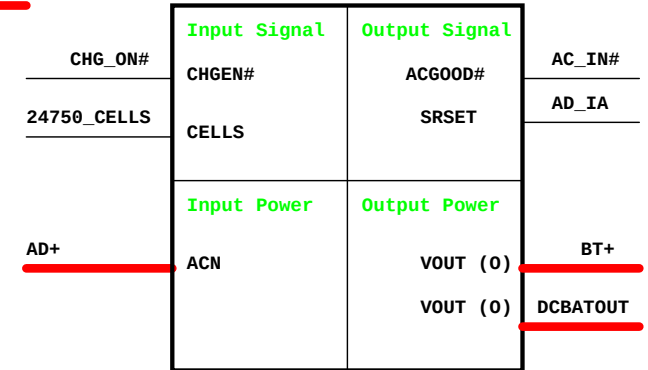
RT9026 0D9V_S0

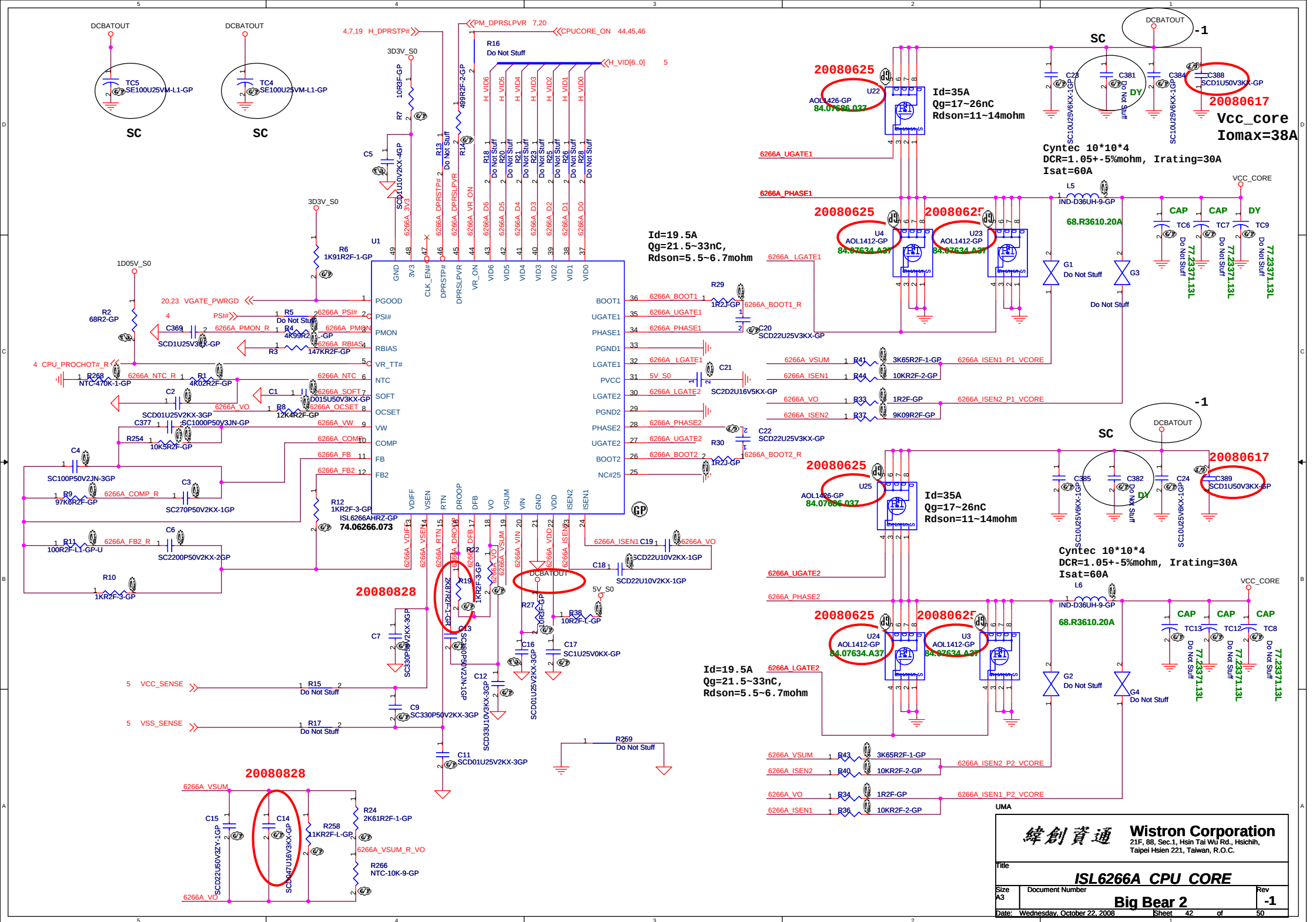


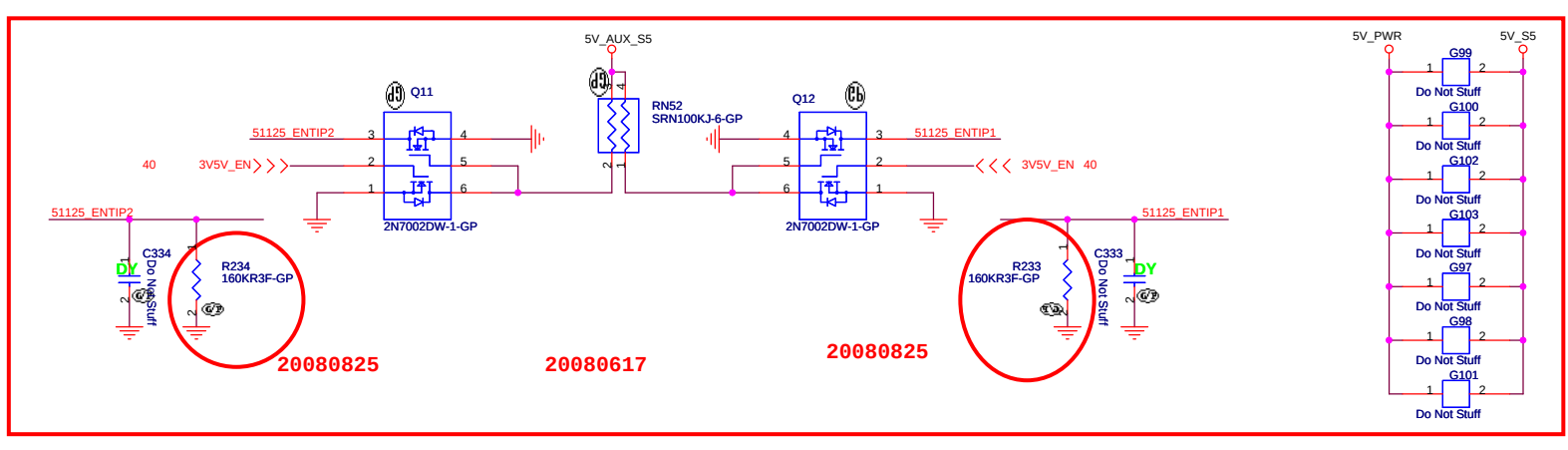
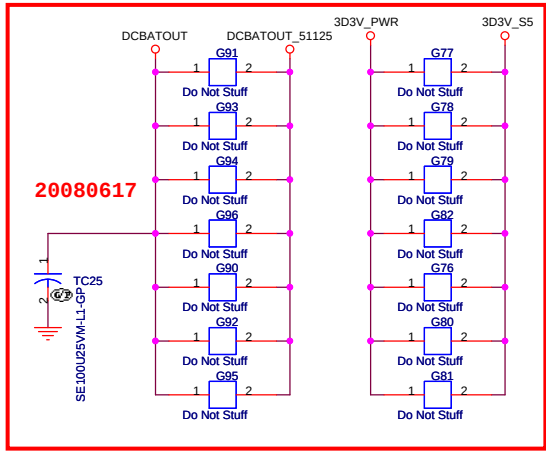
G9131 2D5V_S0



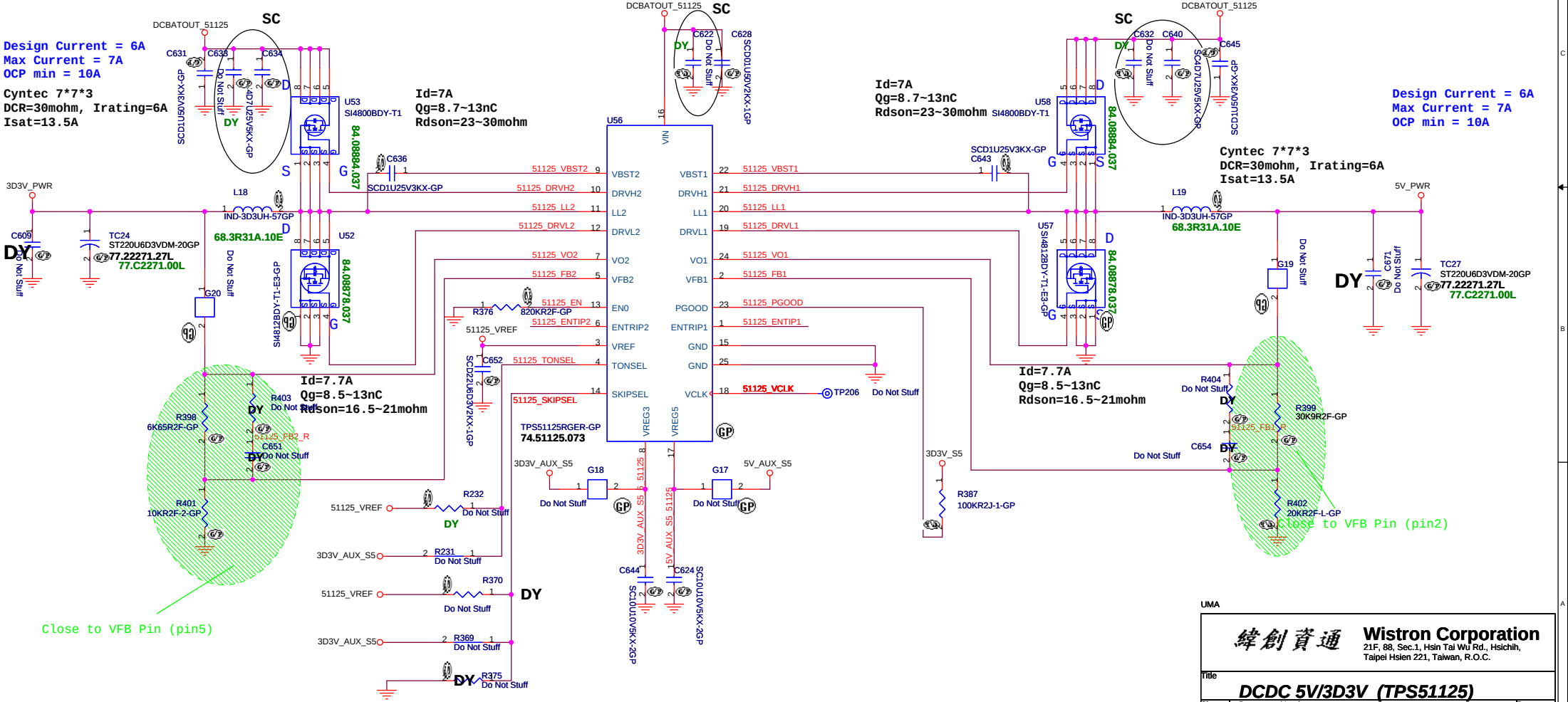
Charger BQ24750



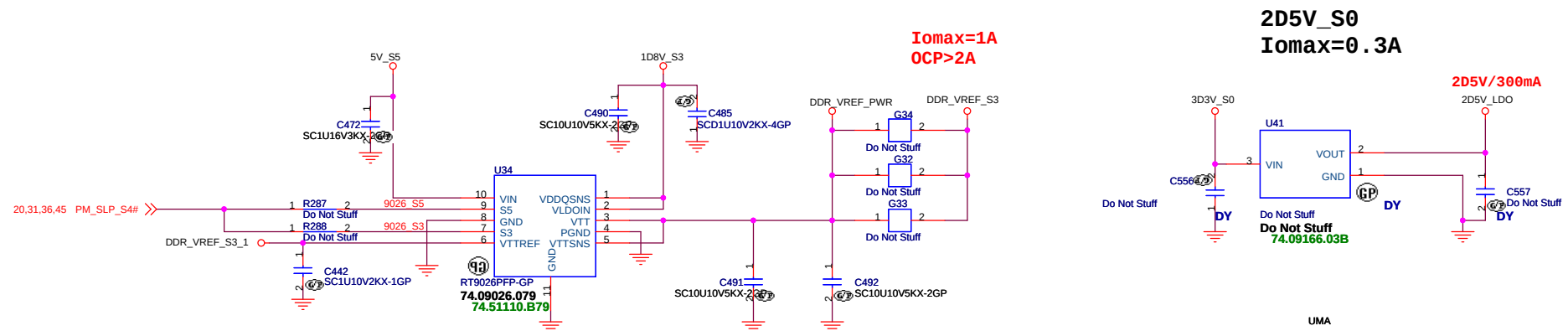
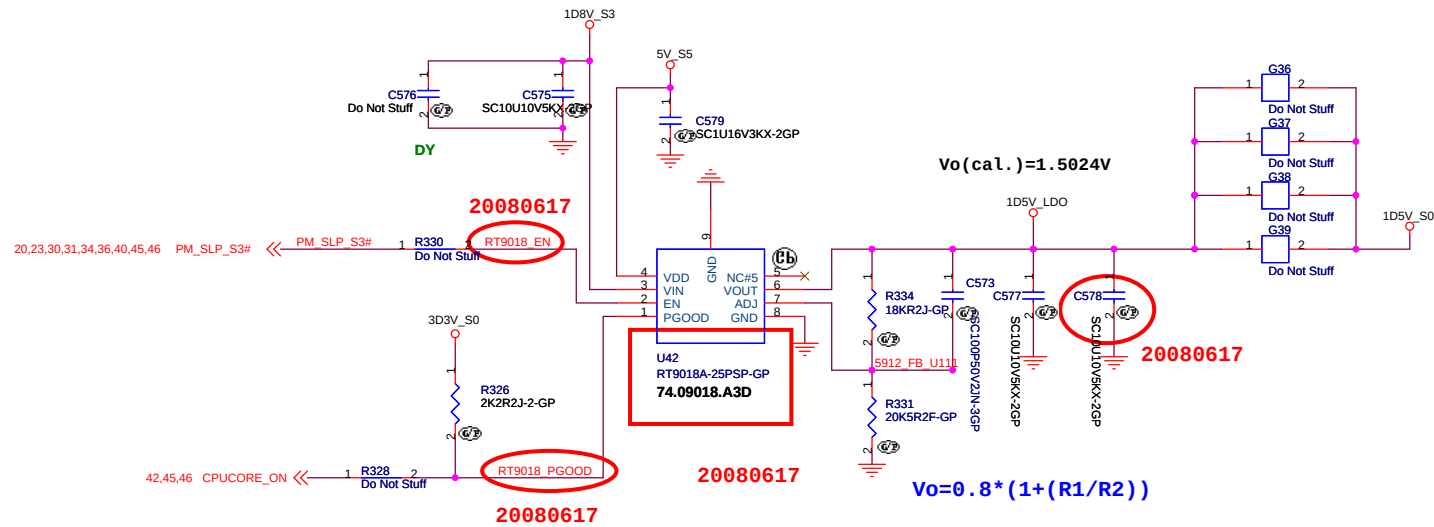




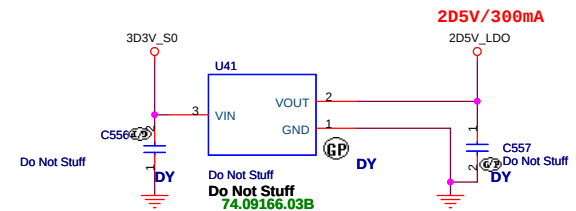
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A

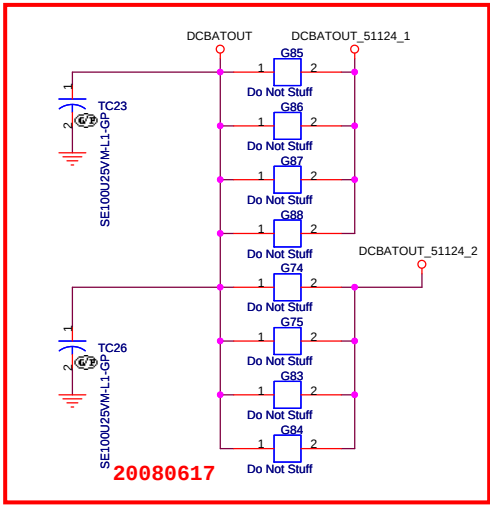


1D5V_S0
Iomax=2.5A



2D5V_S0
Iomax=0.3A

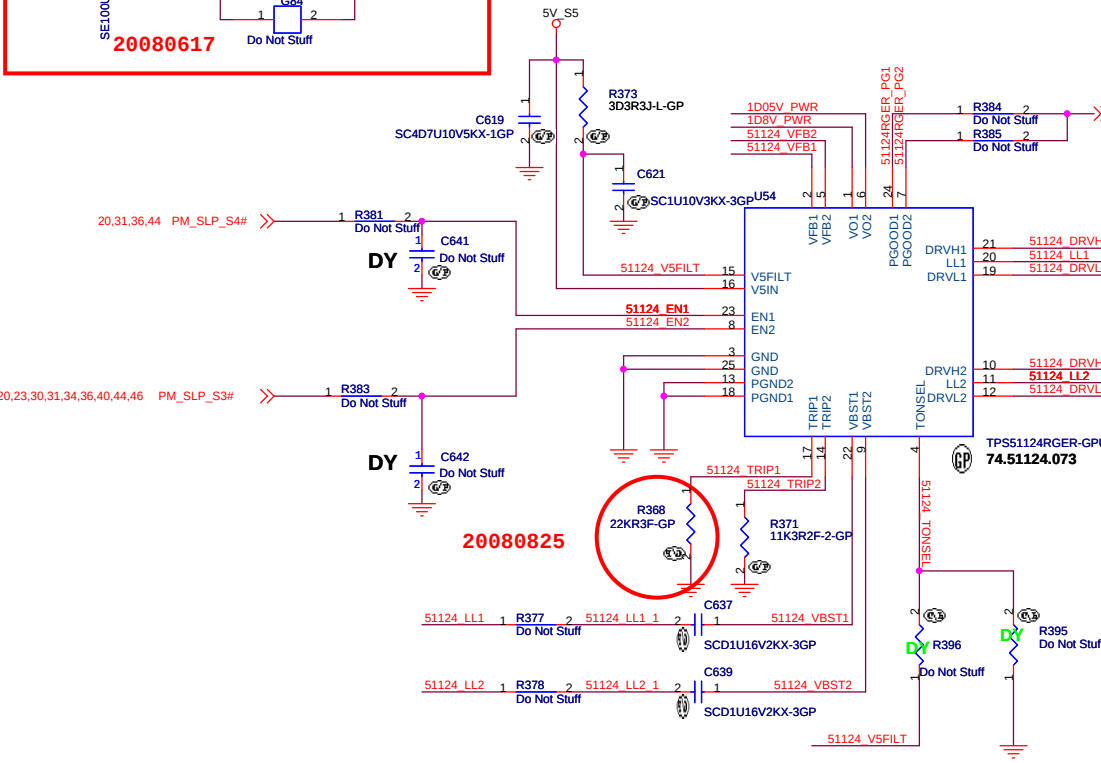




$$V_{trip}(mV) = R_{trip}(Kohm) * I_{10}(uA)$$

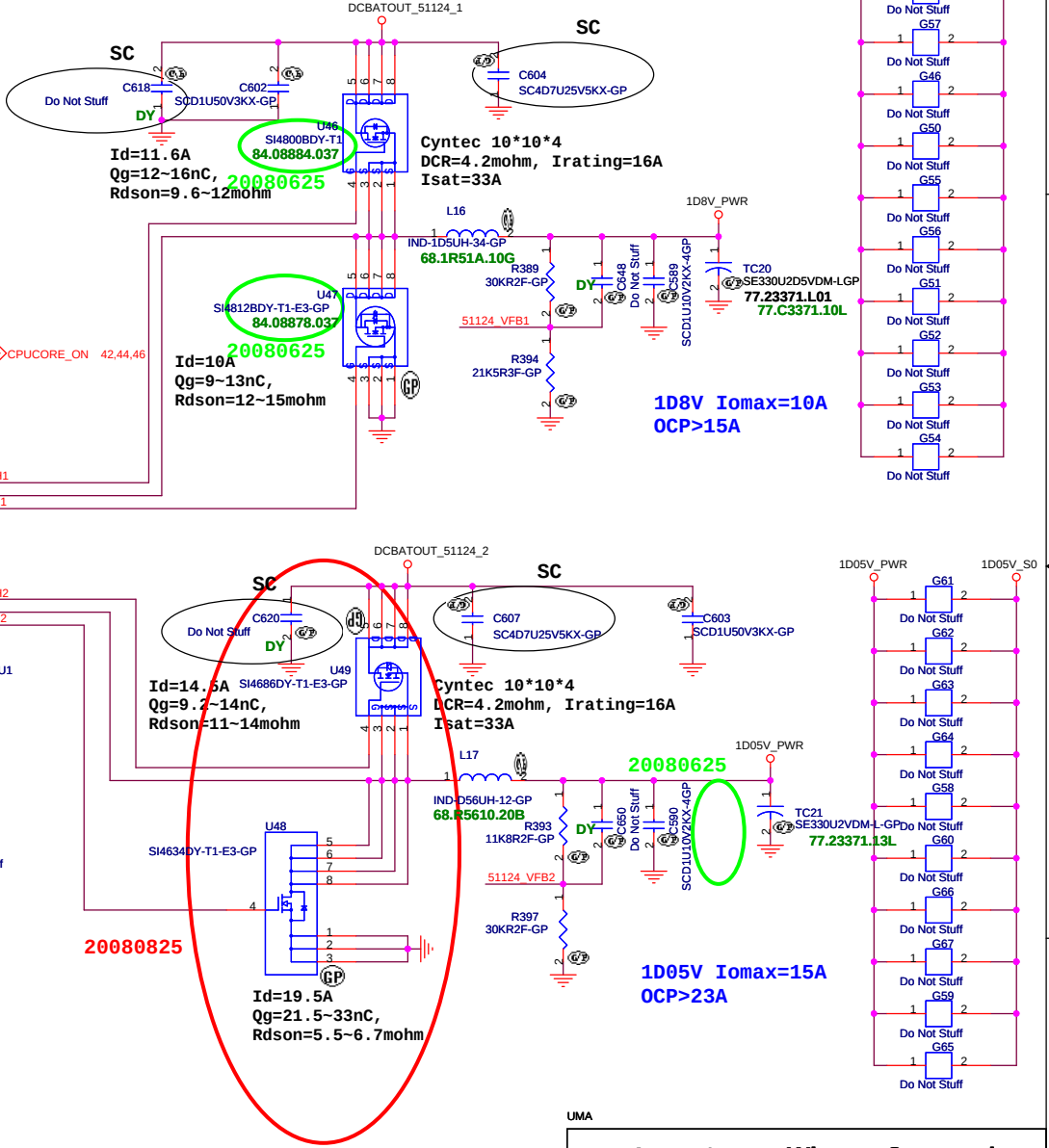
$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in}))$$

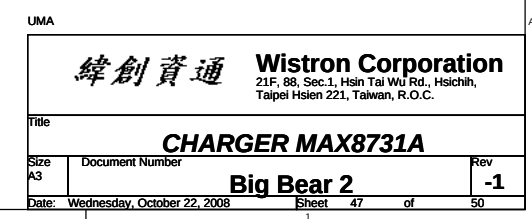
$$I/P \text{ cap: } 10U \ 25V \ K1206 \ X5R / 78.10622.52L$$



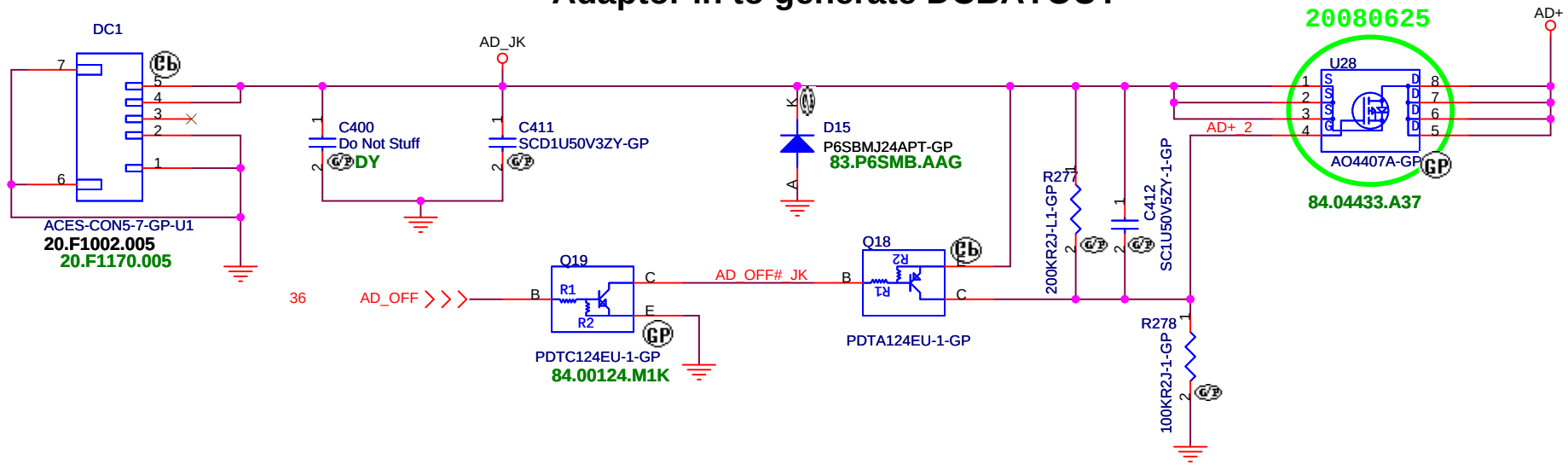
	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode

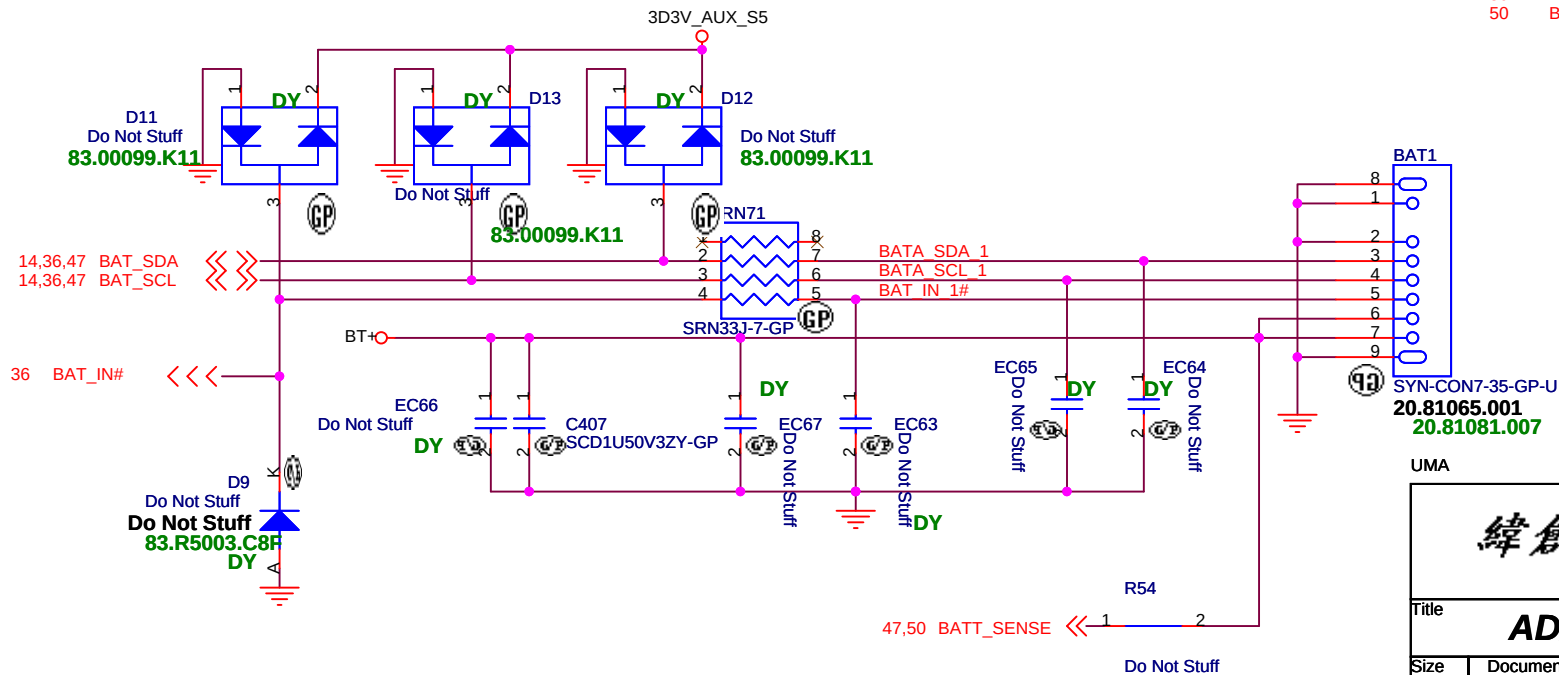




Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



47,50 BATT_SENSE <<< BATT_SENSE

50 BAT_IN_1# <<< BAT_IN_1#

50 BATA_SDA_1 <<< BATA_SDA_1

50 BATA_SCL_1 <<< BATA_SCL_1

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Title **AD/BATT CONN**

Size Document Number

Big Bear 2

Rev
-1

Date: Wednesday, October 22, 2008

Sheet 48 of 50

STAND OFF

SPRING ON BOTTOM

CPU & NB

MDC

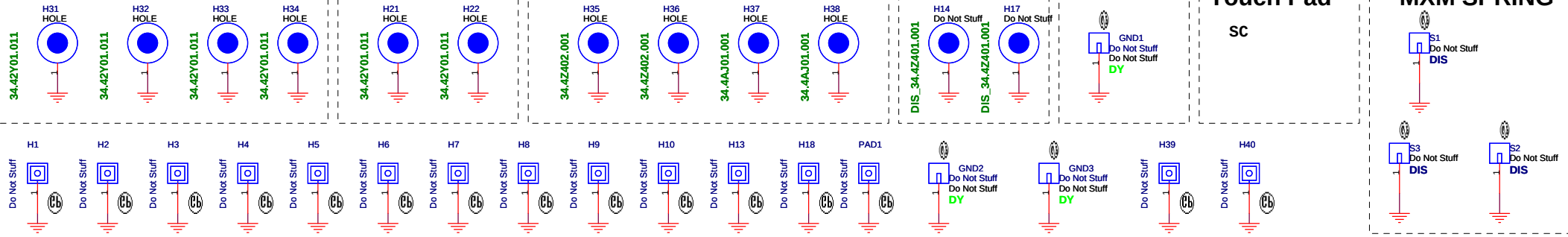
Mini Card

MXM

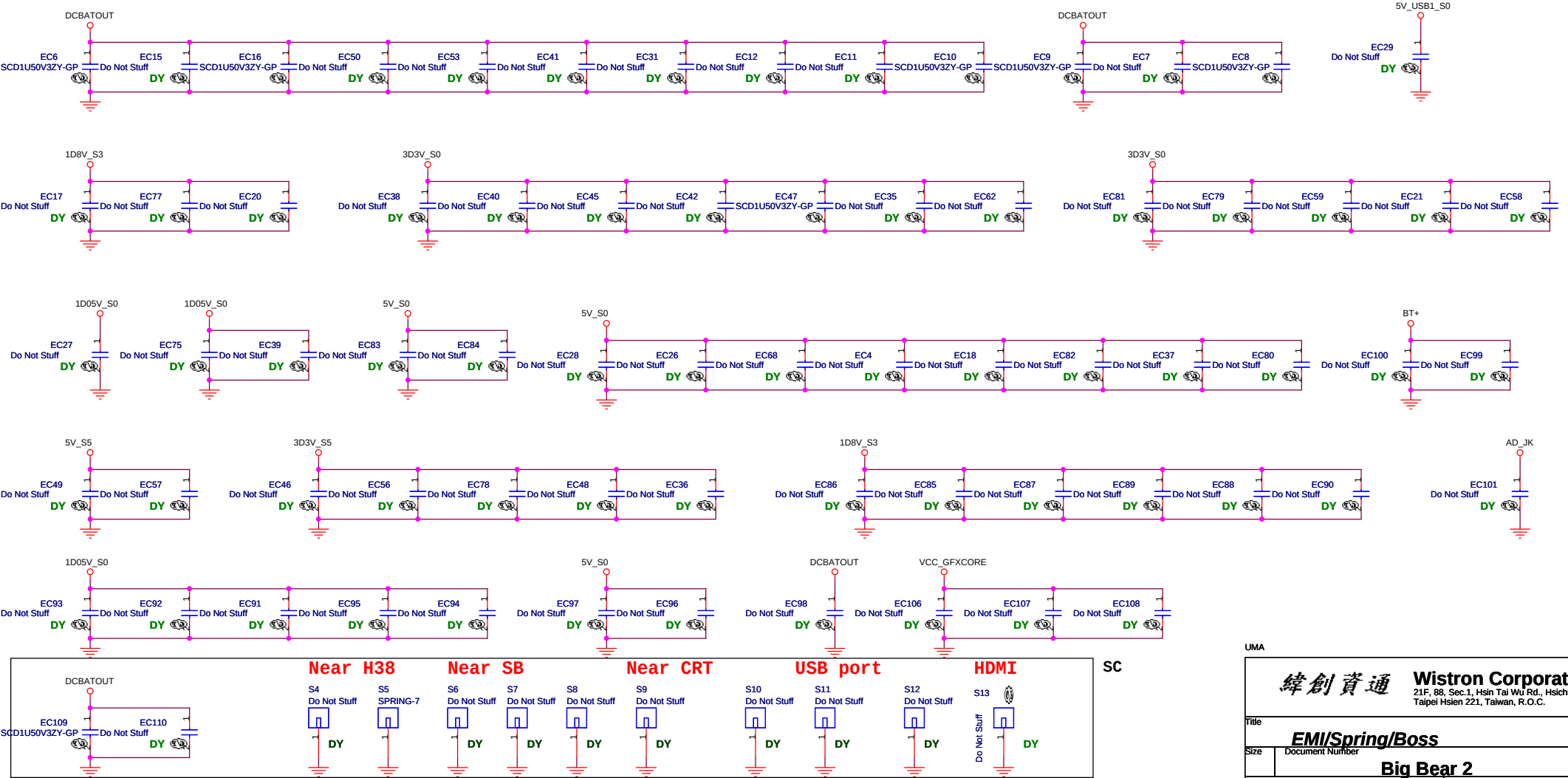
DIMM

Touch Pad

MXM SPRING

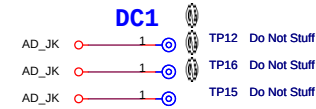
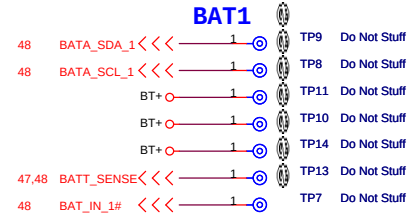
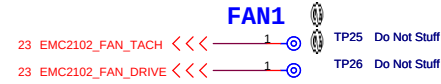
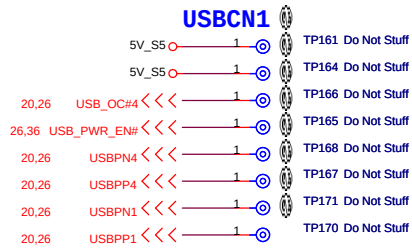
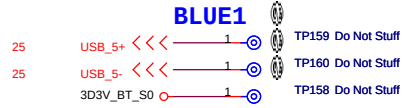
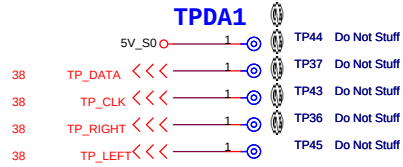
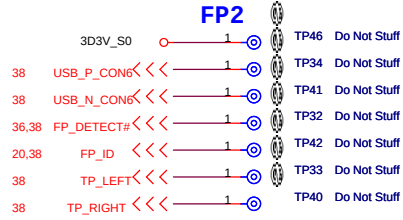
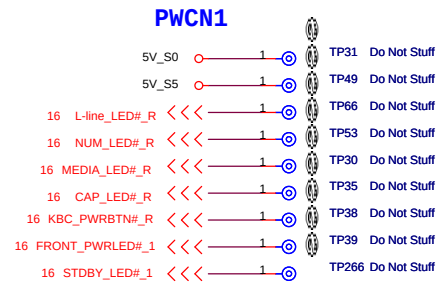
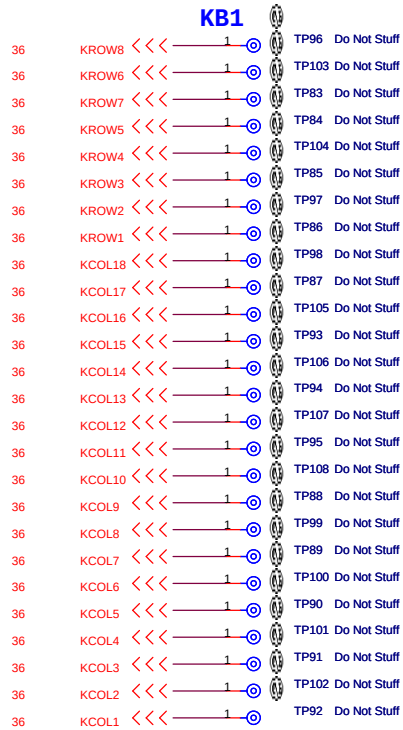
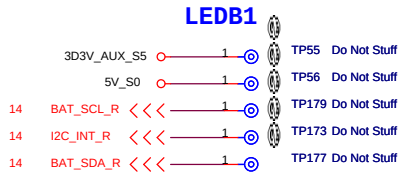
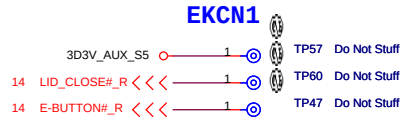
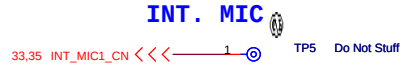
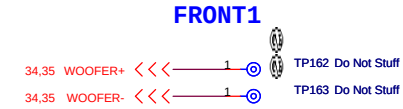
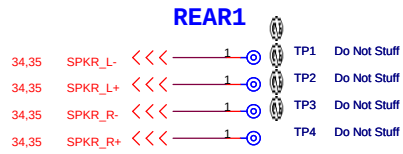


EMI



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Title			
AFTE			
Size	Document Number		Rev
A3	Big Bear 2		-1
Date: Wednesday, October 22, 2008		Sheet 50 of 51	

Big Bear 2 Schematic EC Tracking Record LAB 0911 , 2008
EC #/ Page / Description / Part Affected

- EC SC01/20/Change R316 to 20R2F(For USB eye diagram)
- EC SC02/24/Swap net SATA_RXN5 SATA_RXP5
- EC SC03/29/Add C679 C680 for XF1(For IEEE common voltage channel D fail)
- EC SC04/33/Add RN95 RN104(vendor realtek request)
- EC SC05/36/Swap KBI1 pin definition