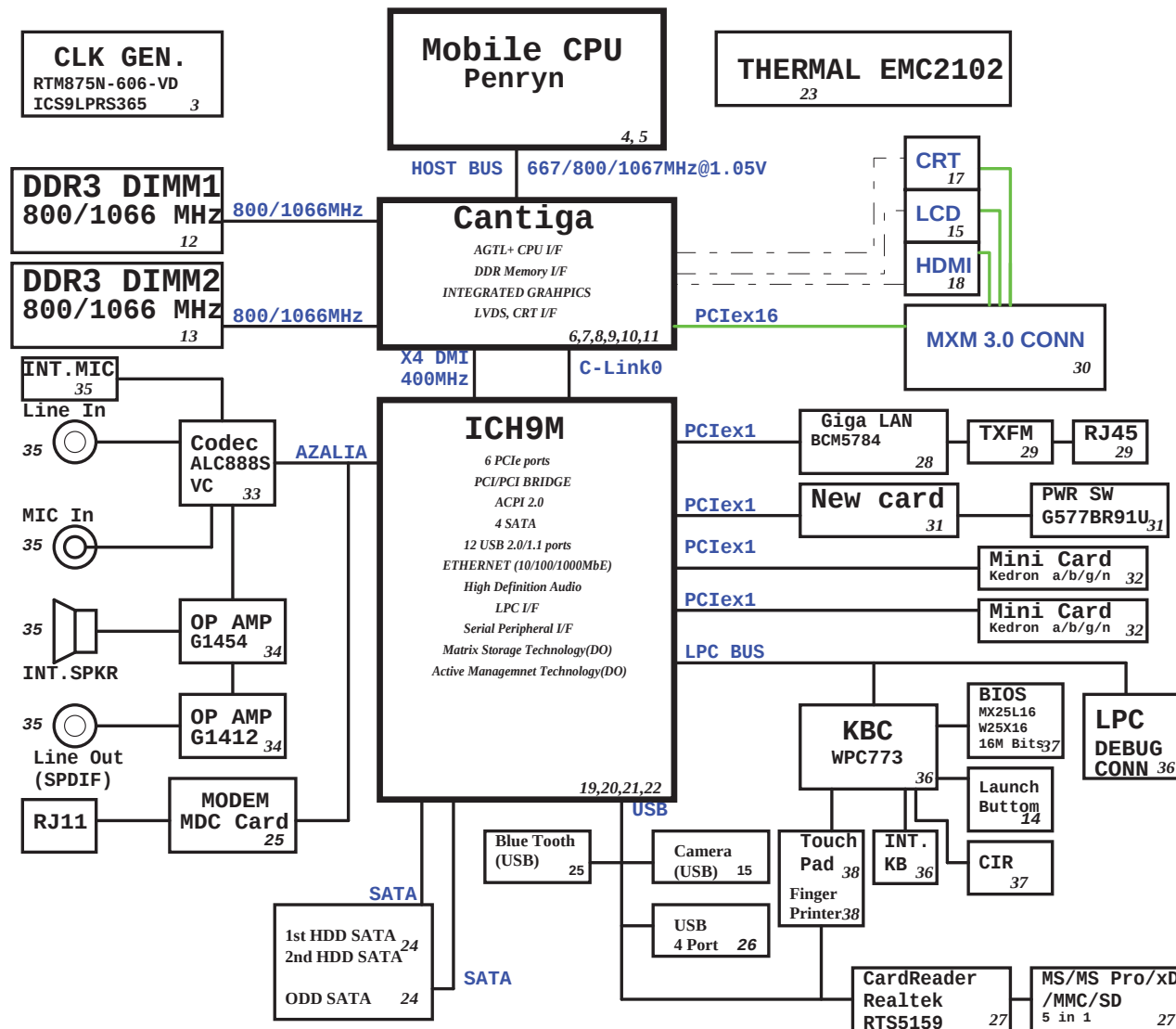


SJM80_MV/JV80_MV Block Diagram

Project code: 91.4DW01.001
PCB P/N : 48.4DW01.0SB
REVISION : 09221 -1



PCB STACKUP

TOP

VCC

S

S

GND

BOTTOM

SYSTEM DC/DC	
TPSS1125 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
SYSTEM DC/DC	
TPSS1124 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D5V_S3
RT9026 44	
1D5V_S3	DDR_VREF_S3 DDR_VREF_S3_1
A04468 44	
1D5V_S3	1D5V_S0
GFXCORE DC/DC	
ISL6263A 46	
INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7-1.25V
CPU DC/DC	
ISL6266A 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35-1.5V
CHARGER	
MAX8731A 47	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

SJM80 UMA ONLY SB

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Title			
BLOCK DIAGRAM			
Size Custom	Document Number		Rev
	SJM80/JV80		-1
Date:	Monday, May 25, 2009	Sheet 1 of	51

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default). 1 = Digital Display Port and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

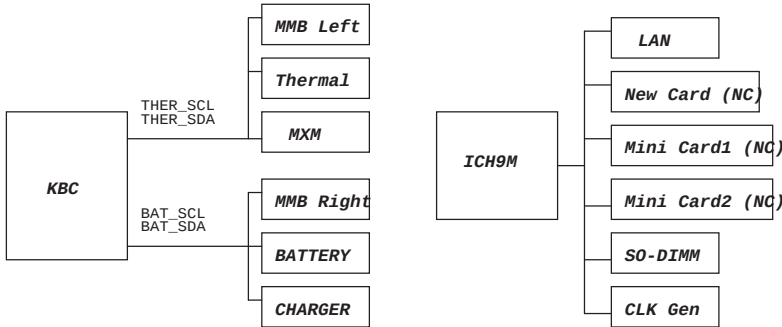
USB Table

USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINI1 (WL)
4	CCD
5	NEW CARD
6	FP
7	BT
8	NC
9	USB1
10	MINI2
11	CARD READER

PCIE Routing

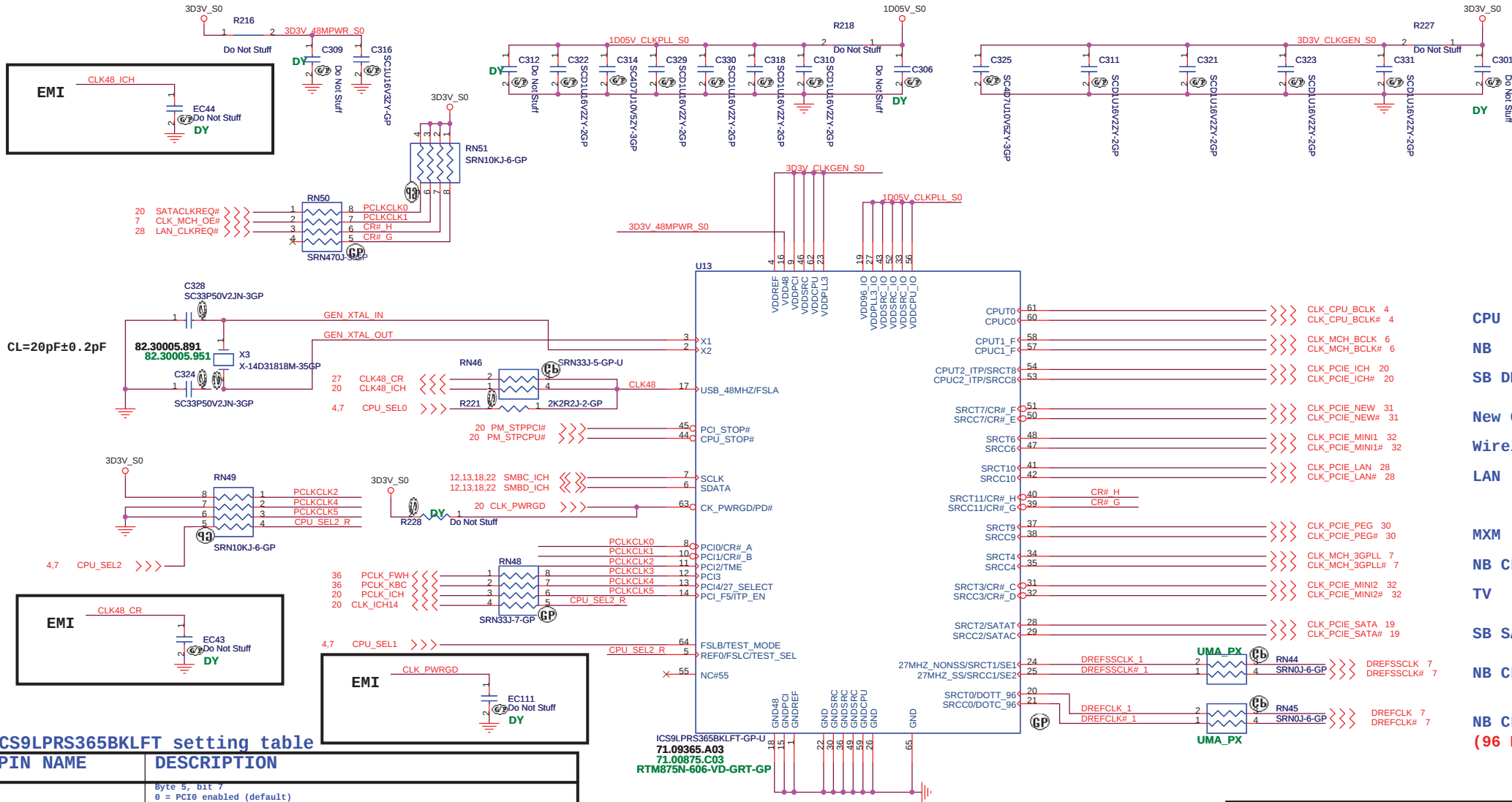
LANE1	LAN Broadcom 5784
LANE2	MiniCard WLAN
LANE3	MiniCard TV
LANE4	NC
LANE5	NewCard
LANE6	NC

SMBus



SJM80 UMA ONLY SB

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Title	
Reference	
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ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

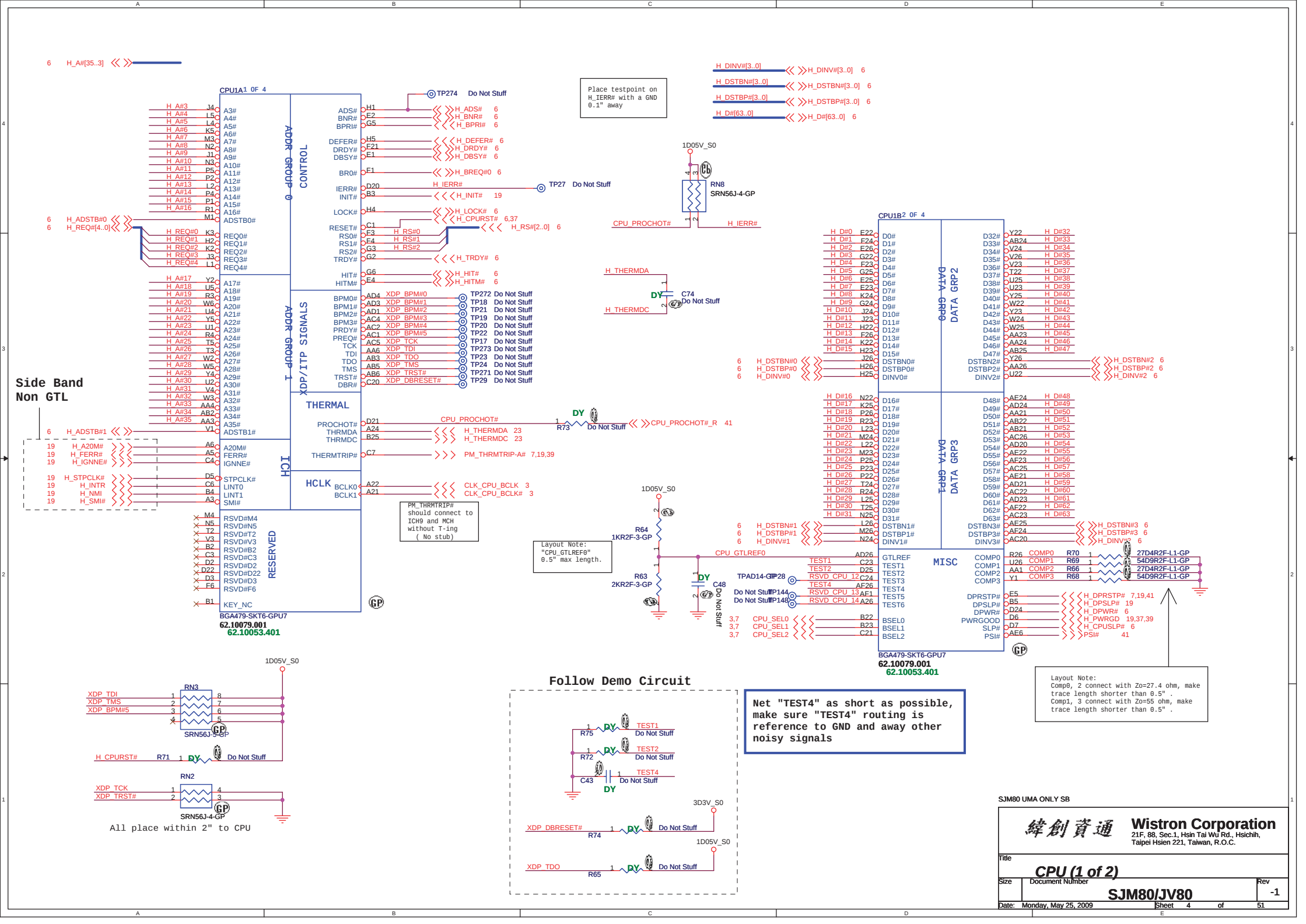
PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

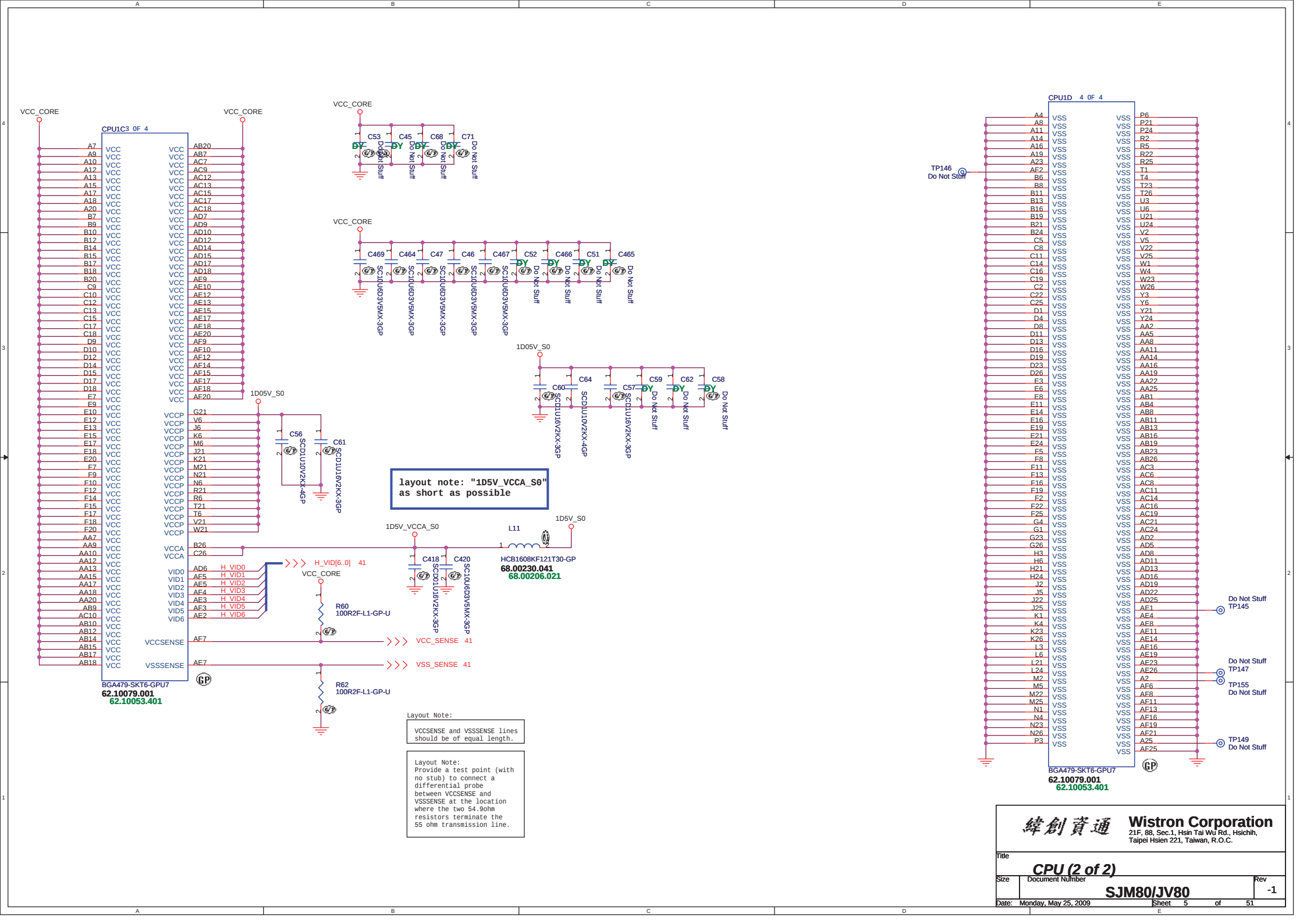
SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

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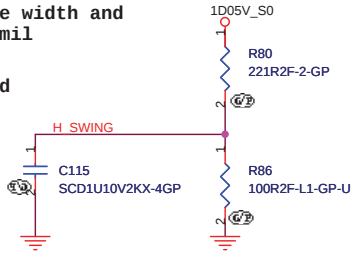
Title			Clock Generator	
Size	Document Number			Rev
SJM80/JV80				-1
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H_SWING routing Trace width and Spacing use 10 / 20 mil

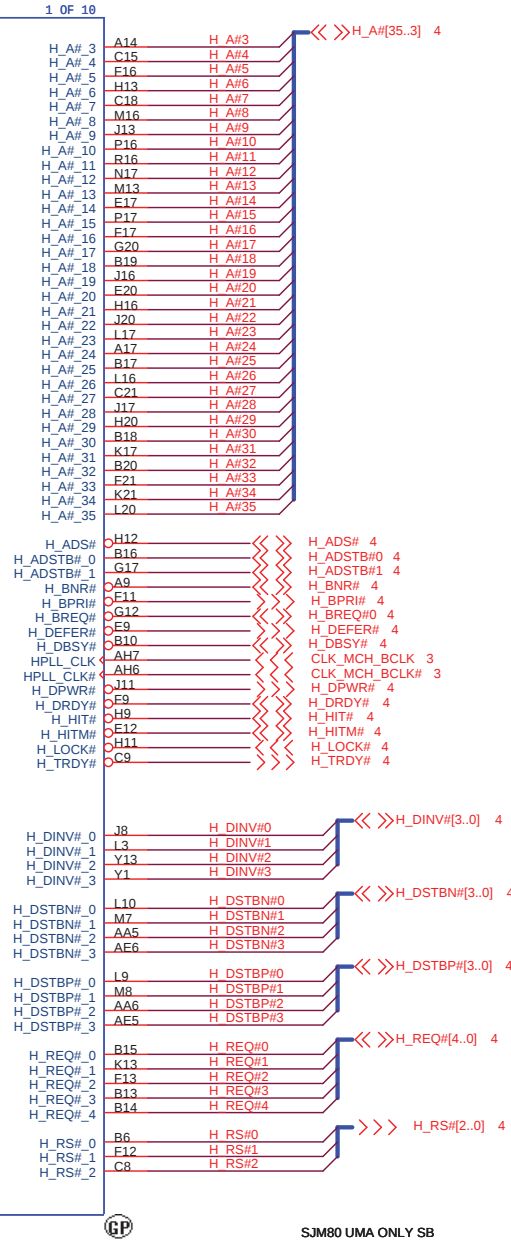
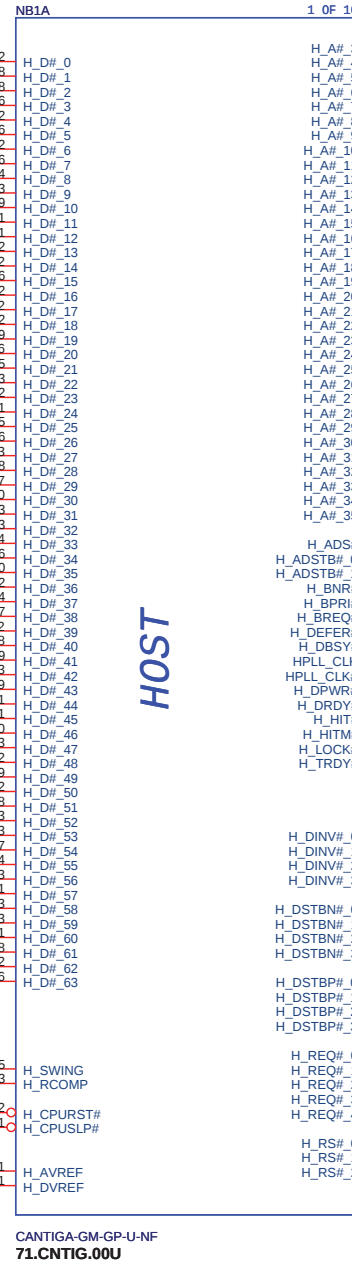
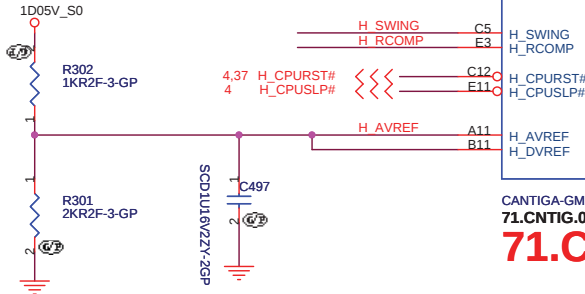
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

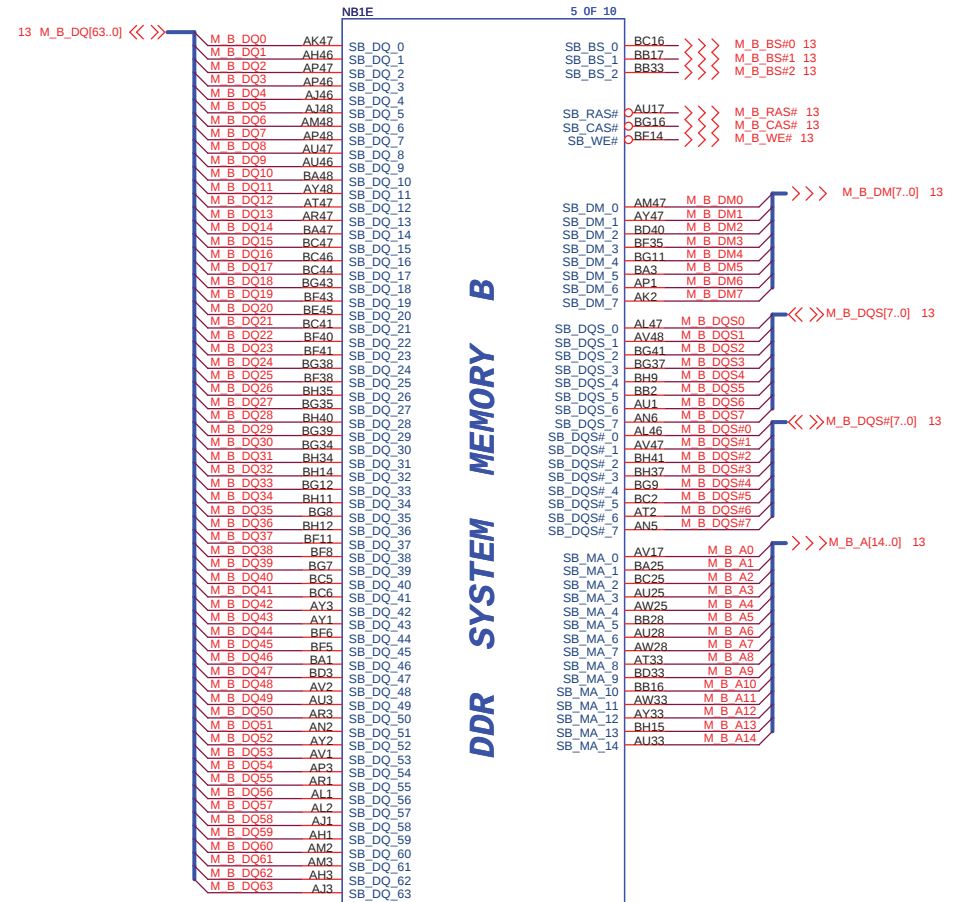
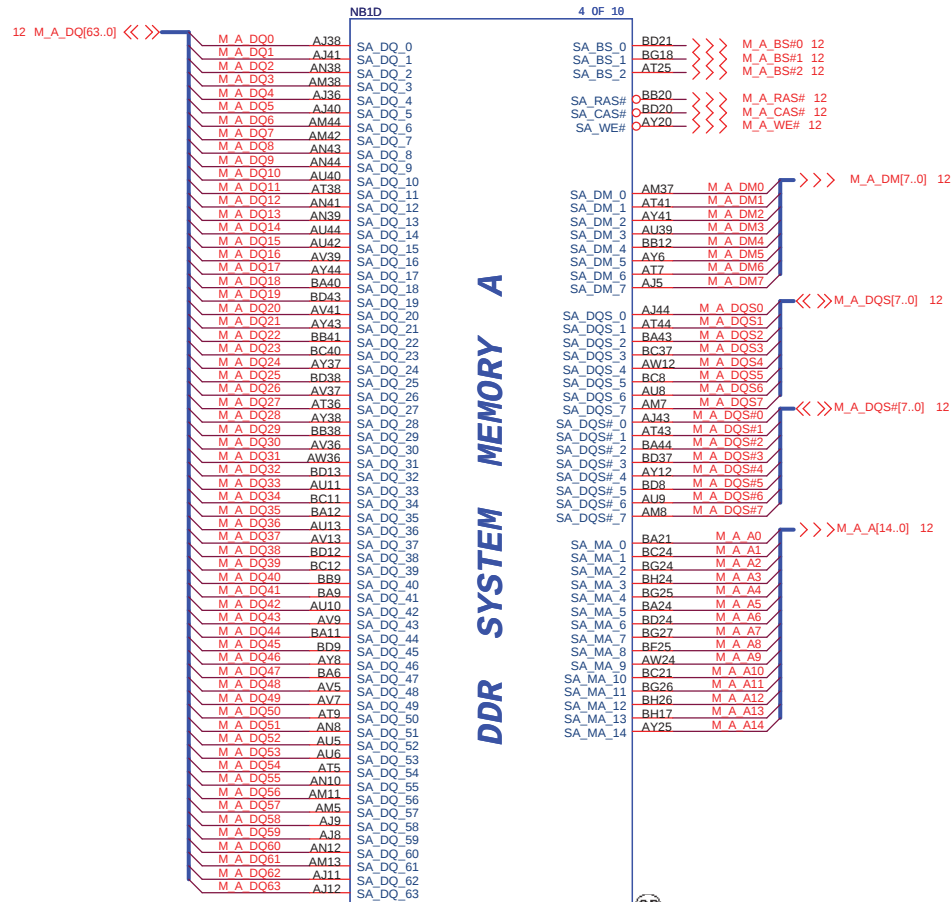


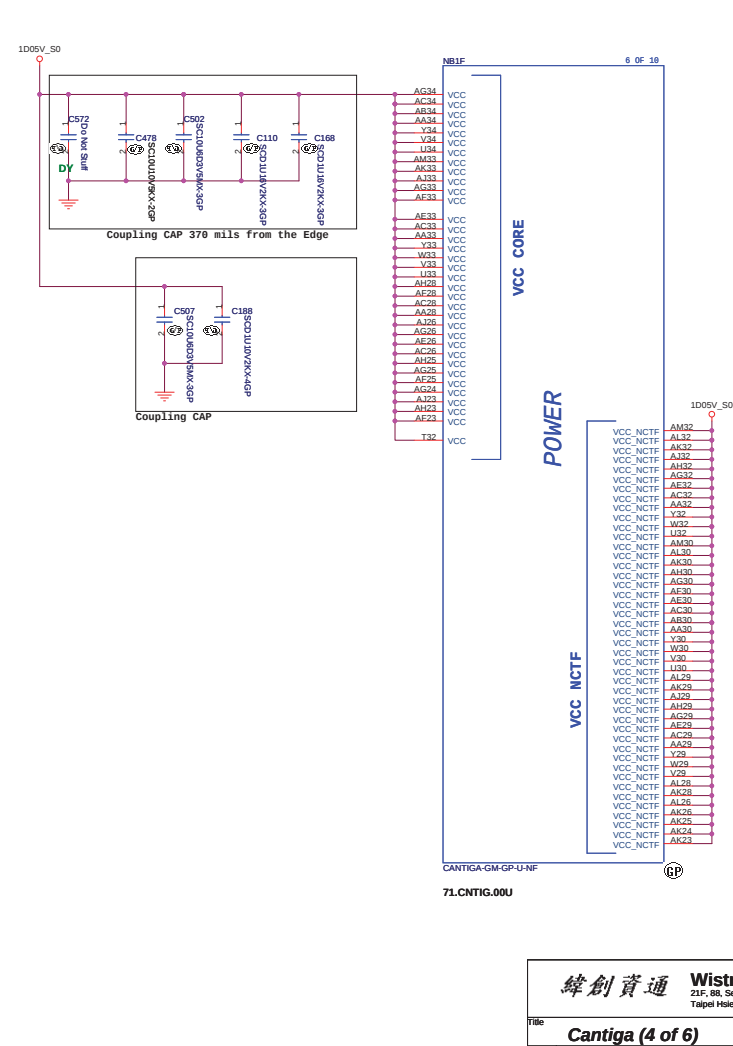
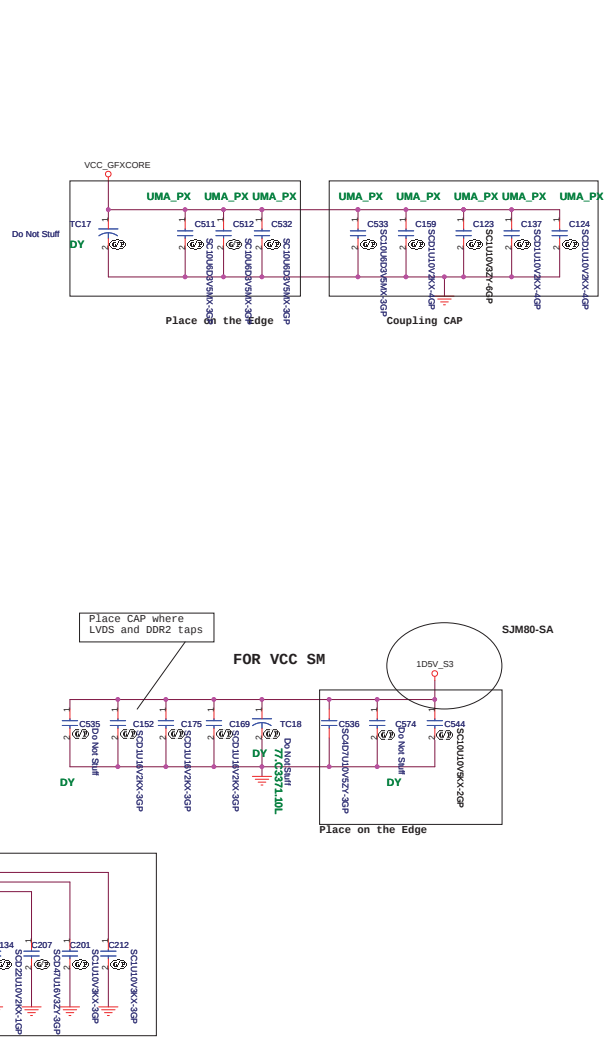
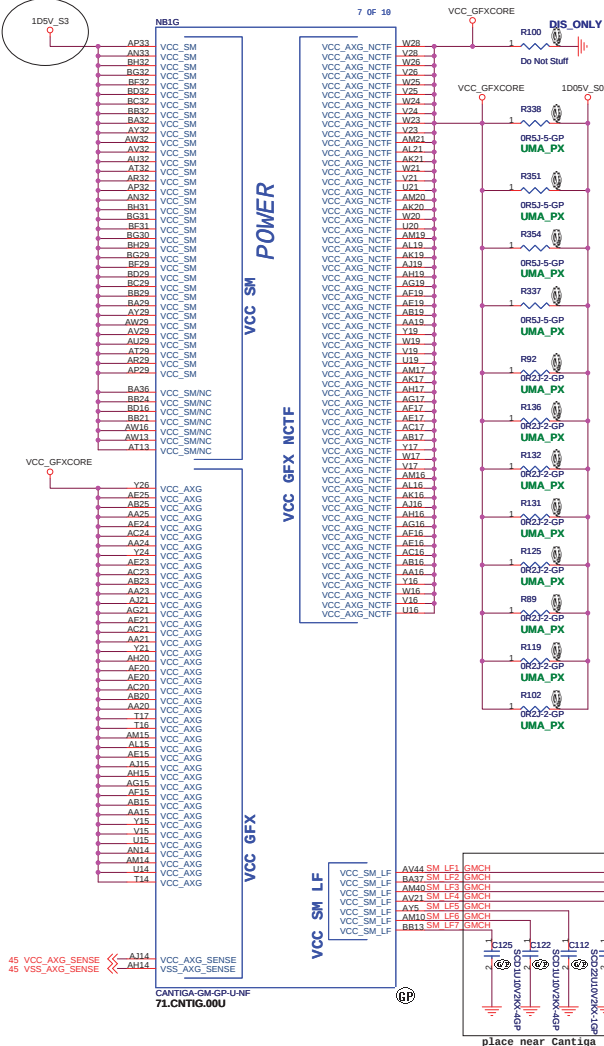
SJM80 UMA ONLY SB

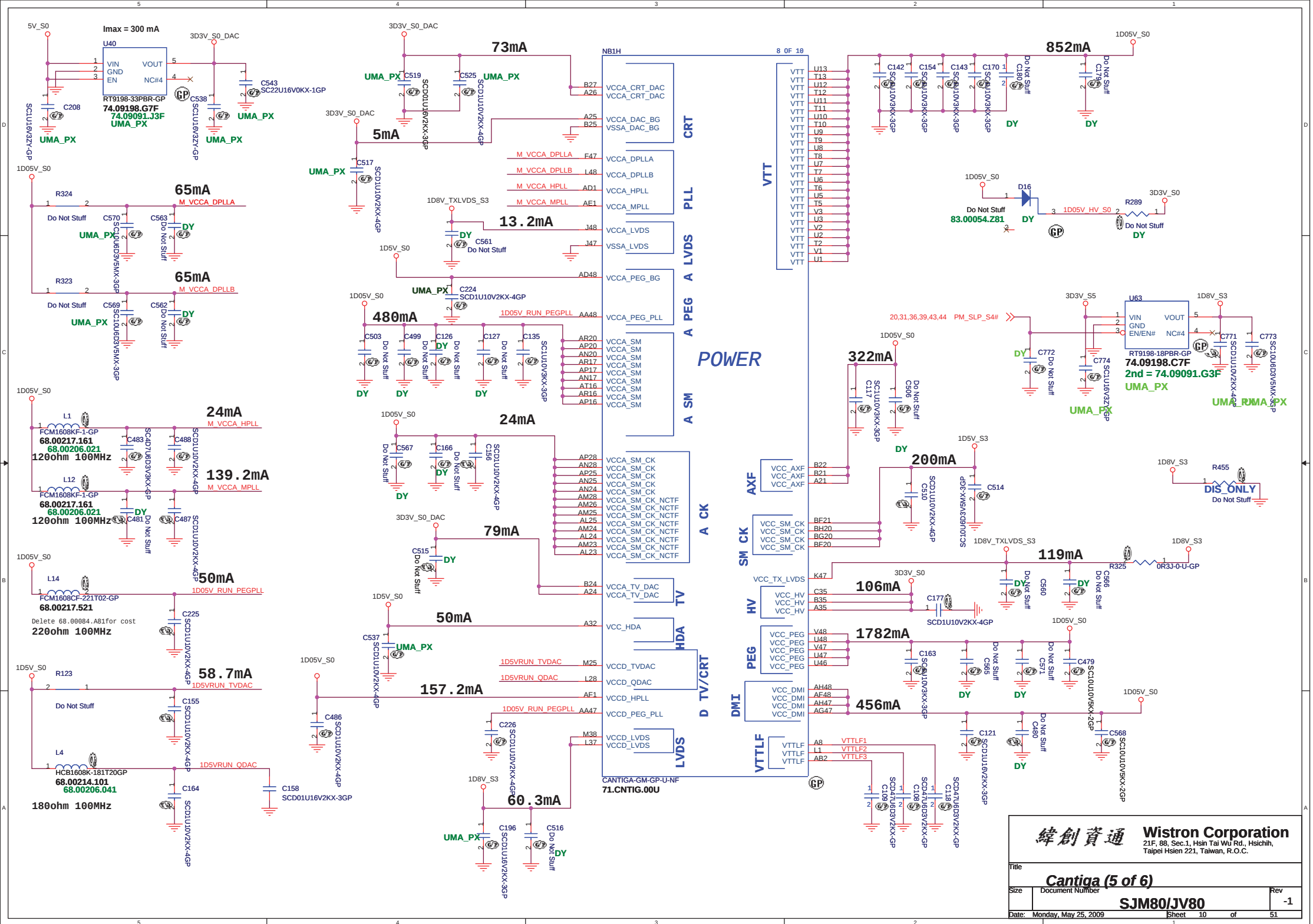
緯創資通

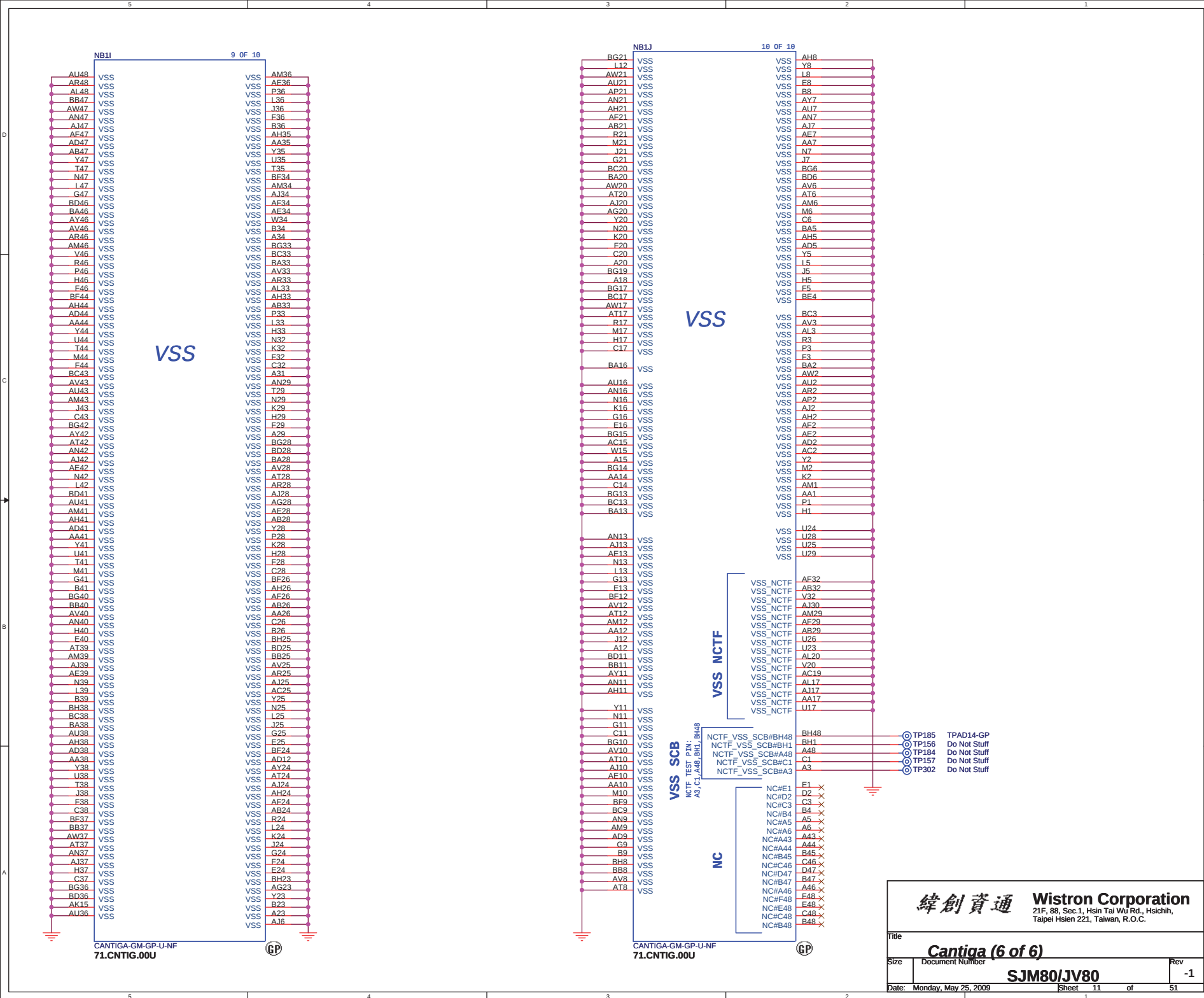
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Title			Cantiga (1 of 6)	
Size	Document Number			Rev
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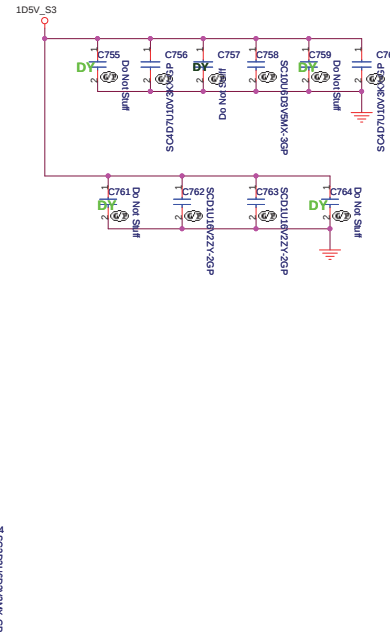
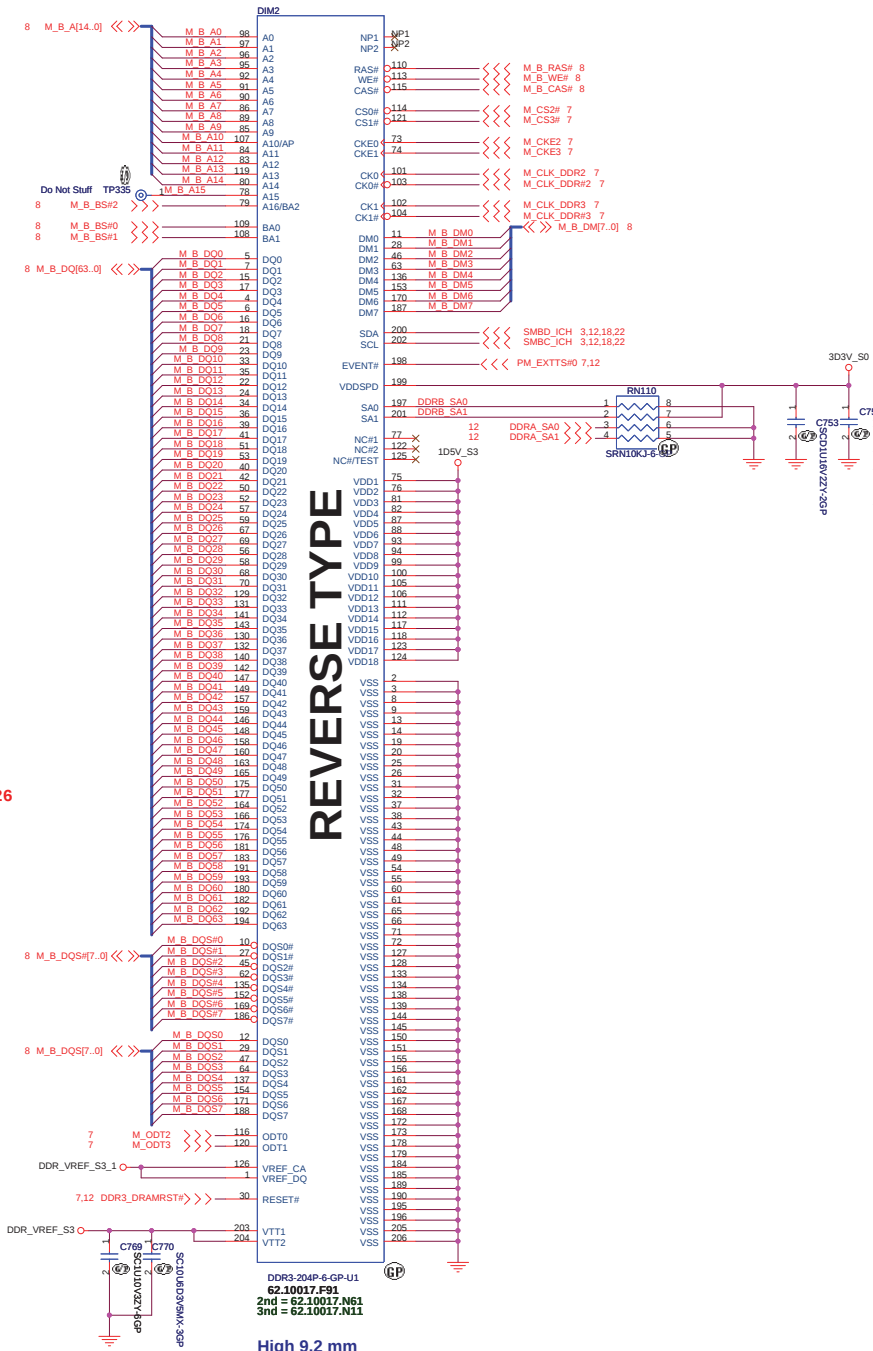




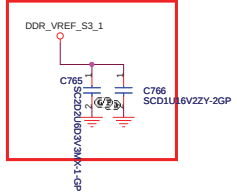




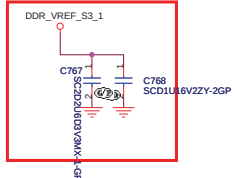
DDR3 SOCKET_2



Layout Note : Near Pin 126

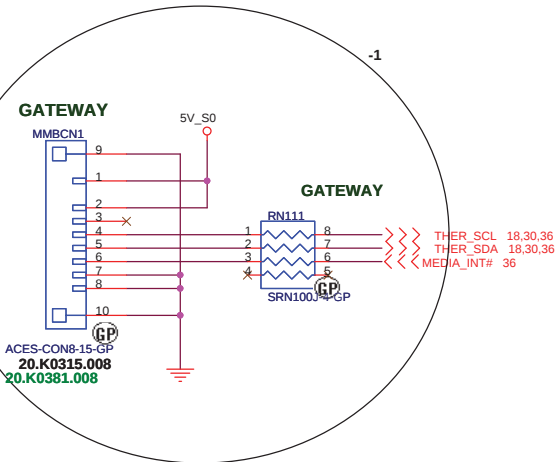


Layout Note : Near Pin 1

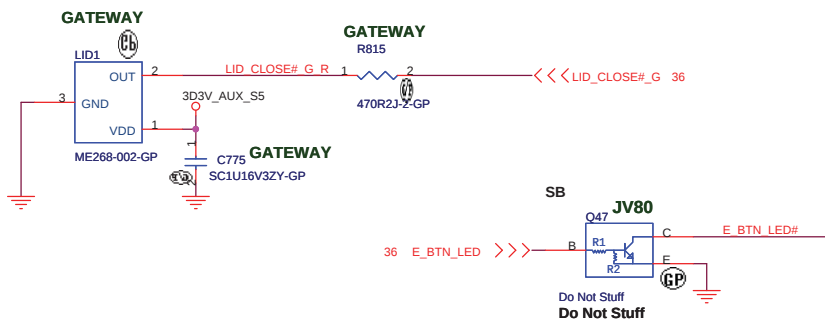


High 9.2 mm

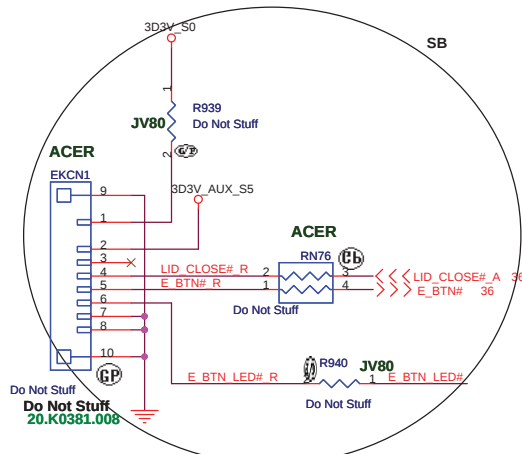
MMB Lunch For GATEWAY



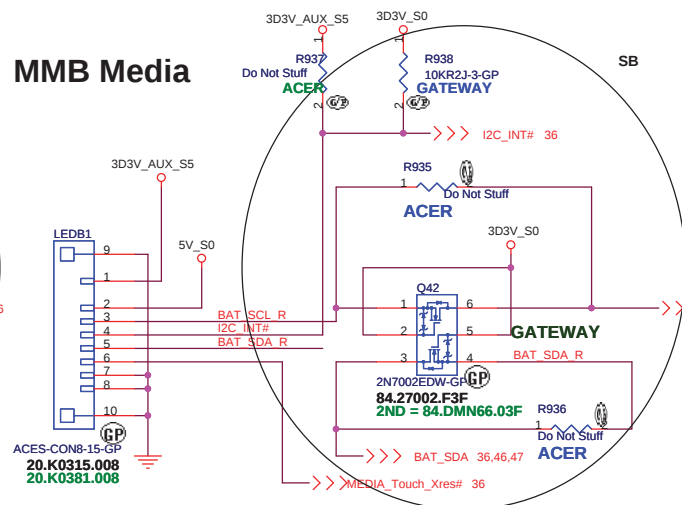
LID SWITCH



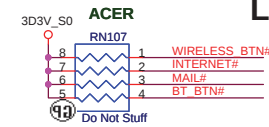
E-KEY Button



MMB Media

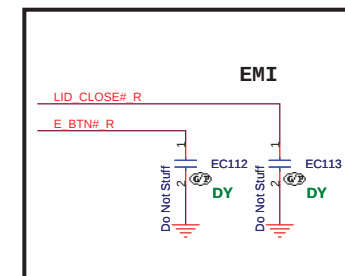
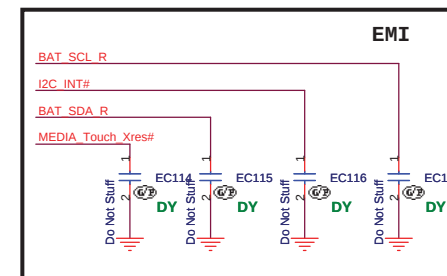
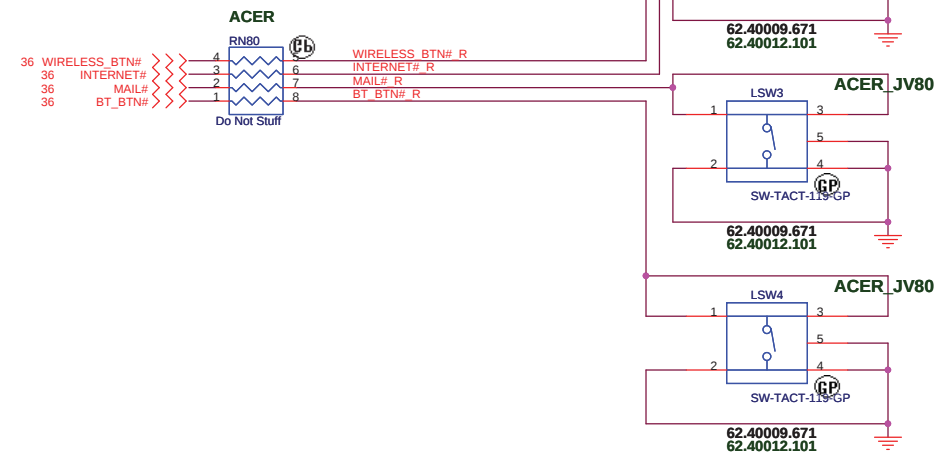


LAUNCH Button



JV80_MV change Function

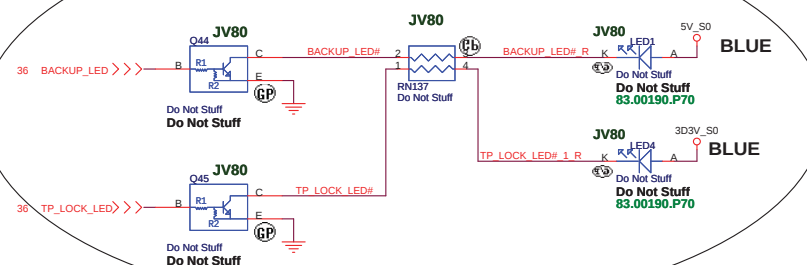
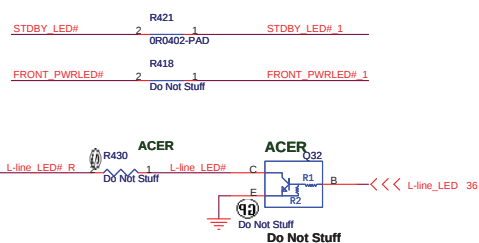
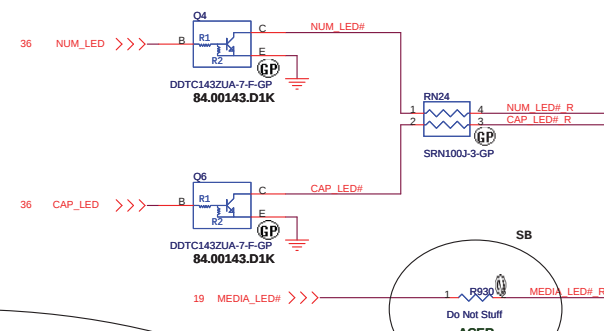
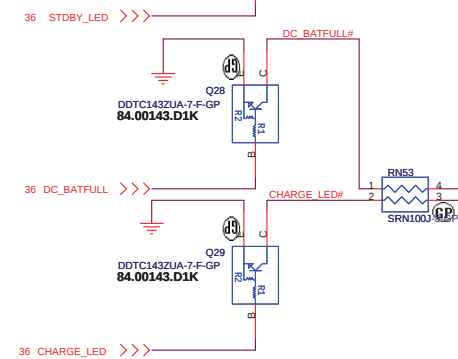
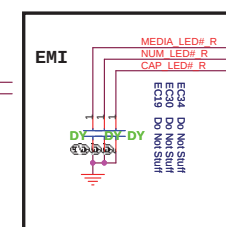
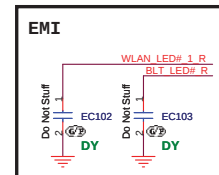
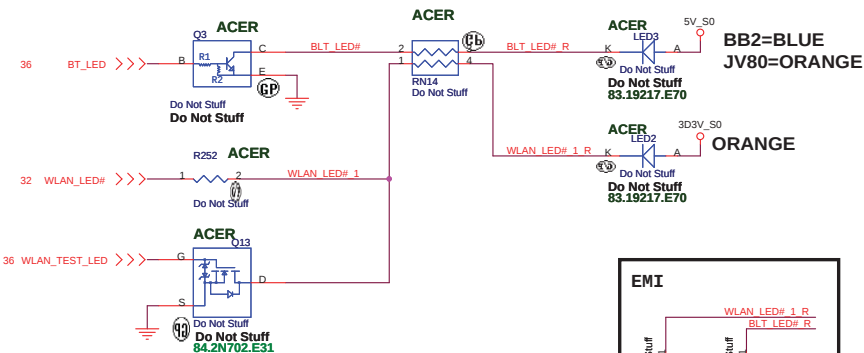
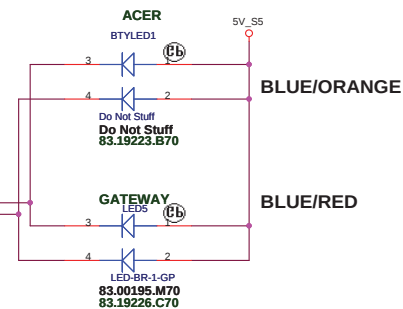
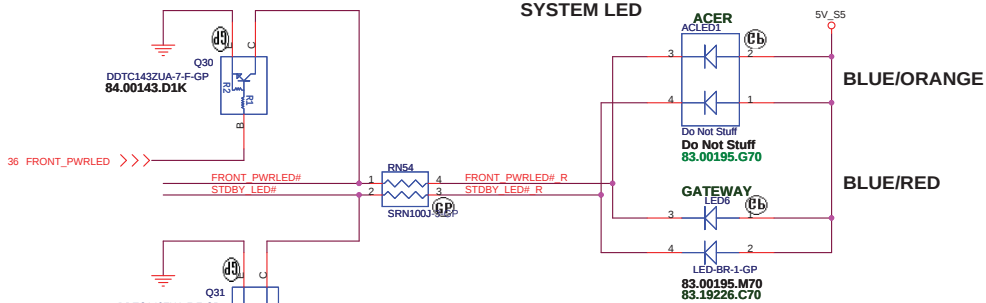
Internet ==> BlueTooth
Mail ==> Backup
BlueTooth ==> TouchPad Lock



SJM80 UMA ONLY SB

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LAUNCH			
Size	Document Number		Rev
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36 ALL_LED_OFF >>>

SJM80-SA

GATEWAY

Q35

G

S

MEDIA_LED# R

100R2-2-GP

1

D

84.2N702.D31

84.2N702.E31

2N7002E-1-GP

MEDIA_LED# 19 <<<

GATEWAY

Q36

1

6

WLAN_LED# 1

WLAN_LED# 1 R

2

5

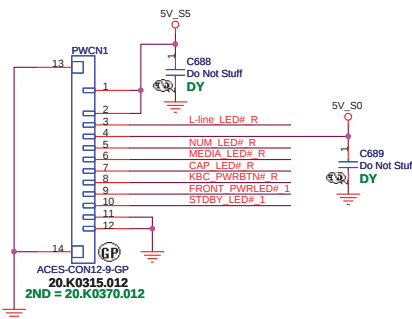
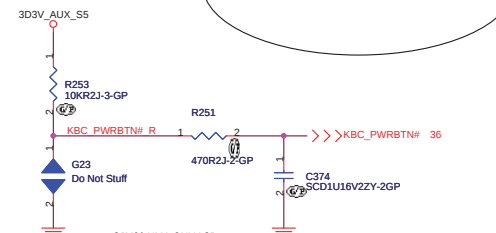
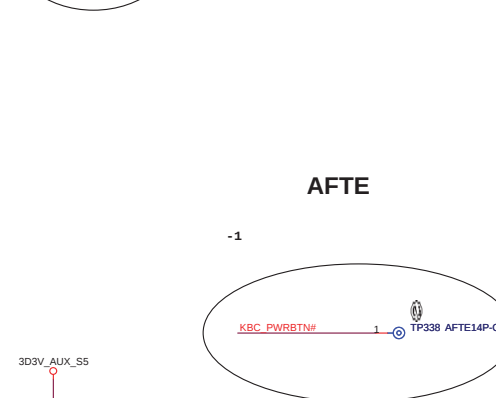
WLAN_LED# 1 R

3

4

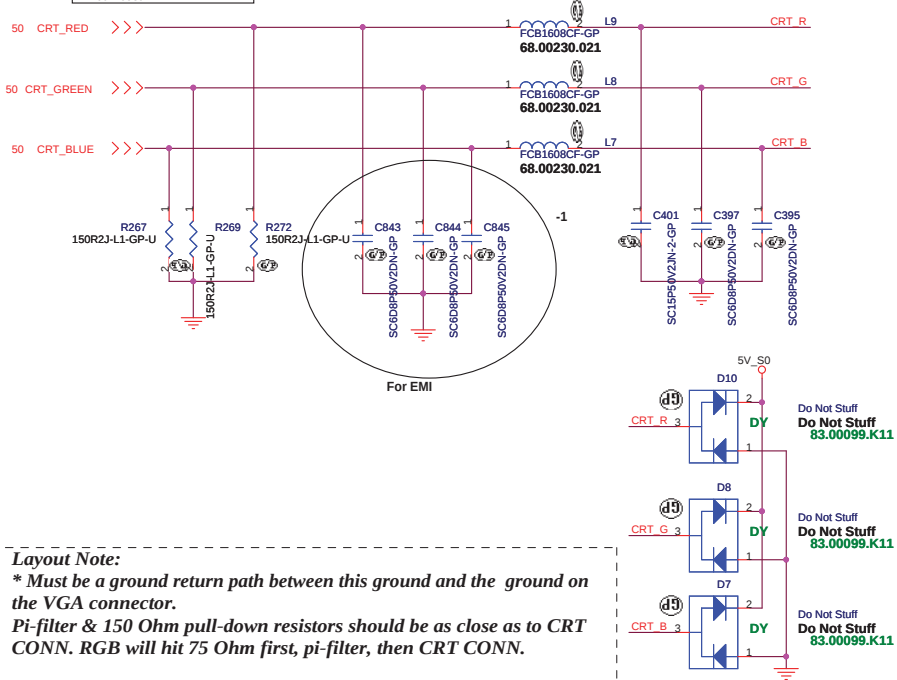
WLAN_TEST_LED 36 <<<

DMN66D0LDW-7-GP

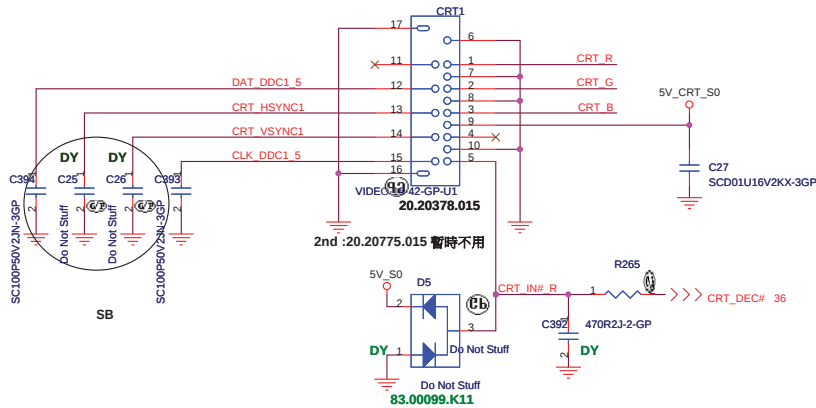


2nd =68.00119.081 source Check

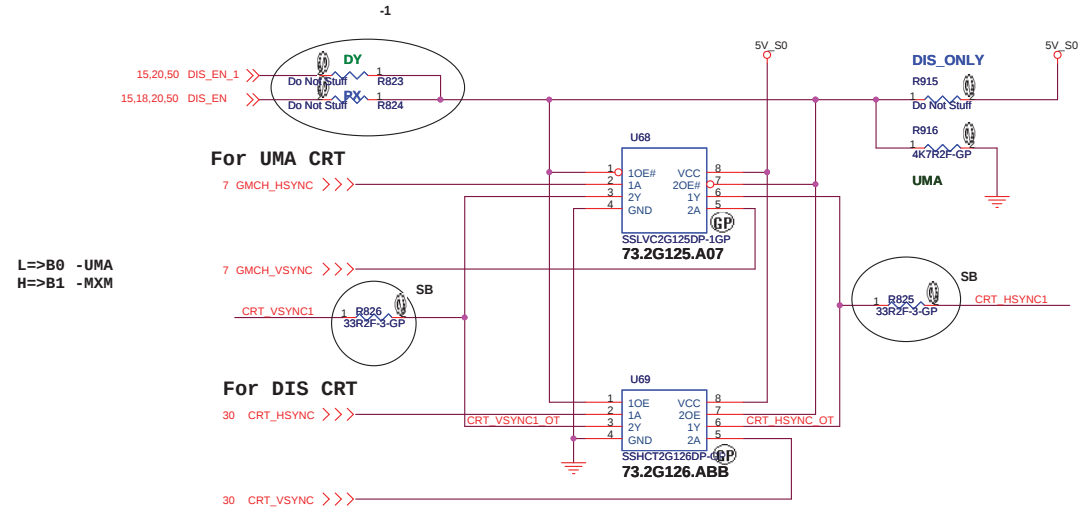
Ferrite bead impedance: 10 ohm@100MHz



CRT I/F & CONNECTOR

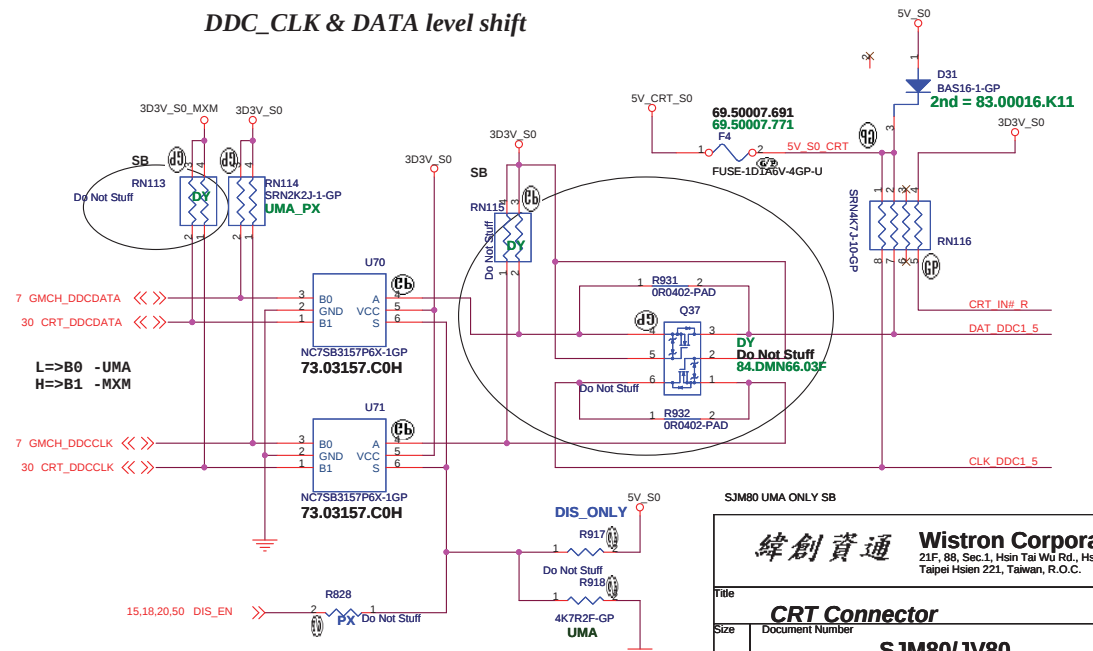


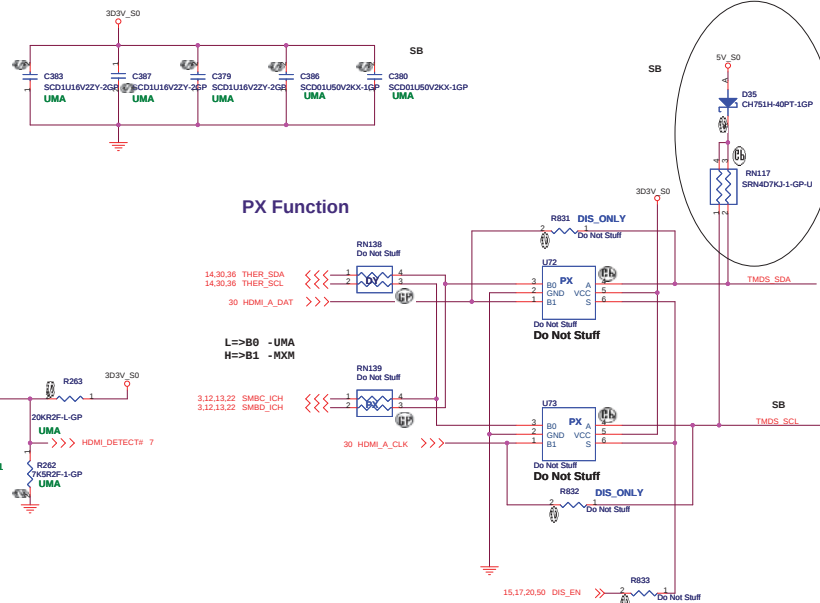
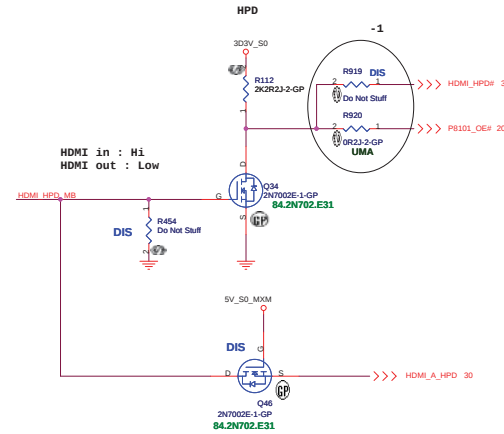
Hsync & Vsync level shift



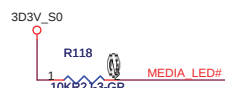
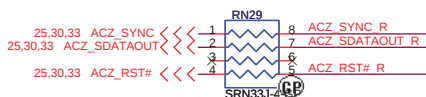
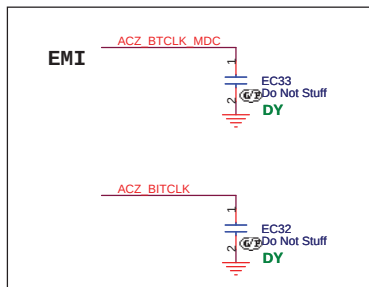
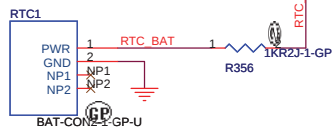
DDC_CLK & DATA level shift

DDC_CLK & DATA level shift

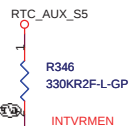




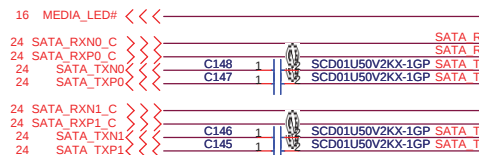
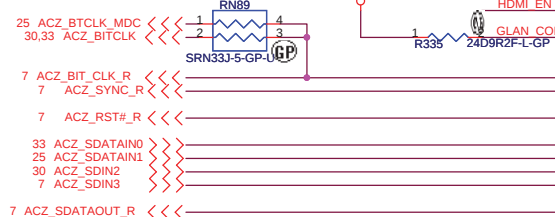
62.70001.011



PH=HDMI
PL=NO HDMI



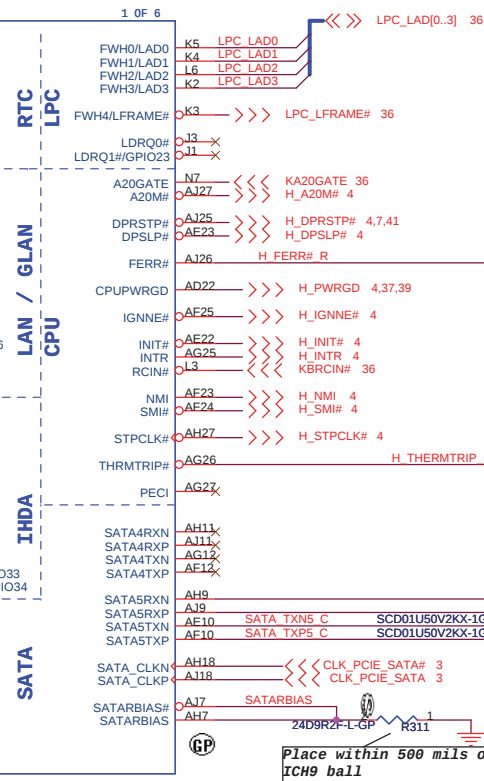
GLAN_COMP place within 500 mil of ICH9M



Integrated VccSus1_05, VccSus1_5, VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

ICH9M-GP-NF
71.ICH9M.00U

71.ICH9M.C1U



Place within 500 mils of
ICH9 ball

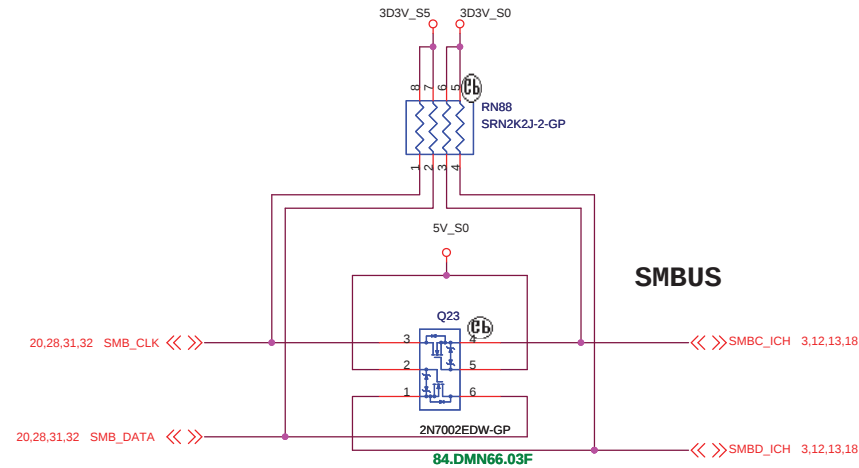
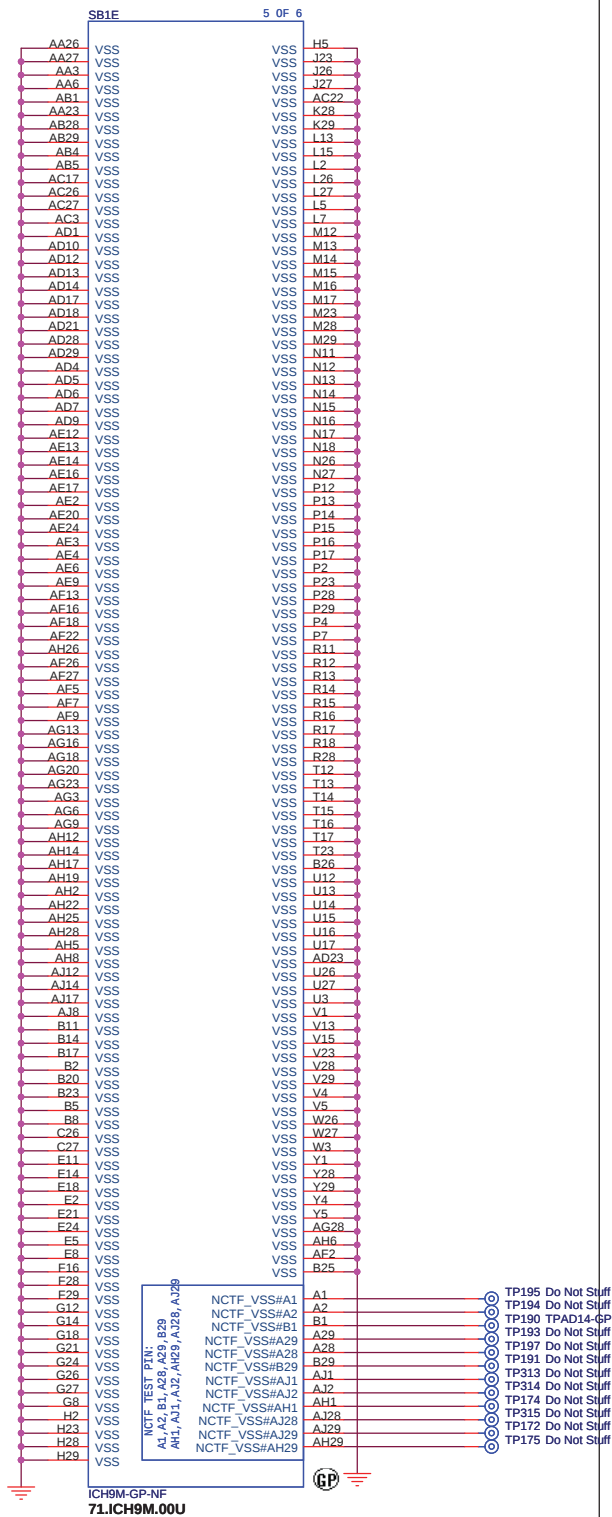
ODD

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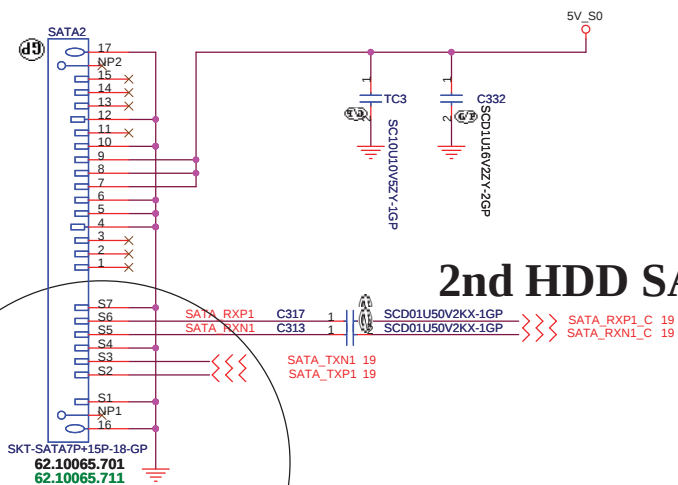
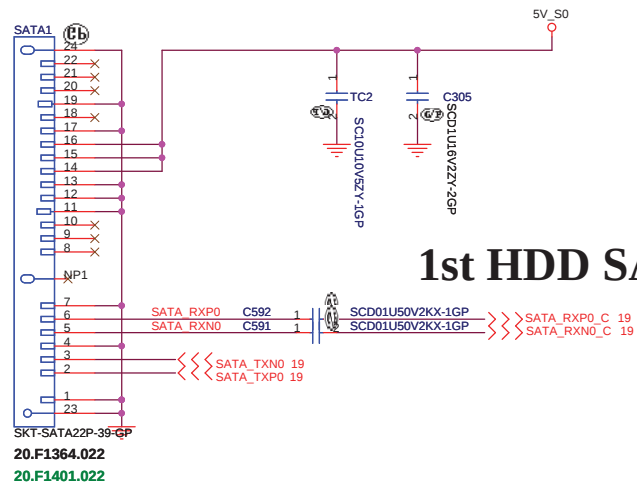
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Title		ICH9-M (1 of 4)	
Size	Document Number	SJM80	
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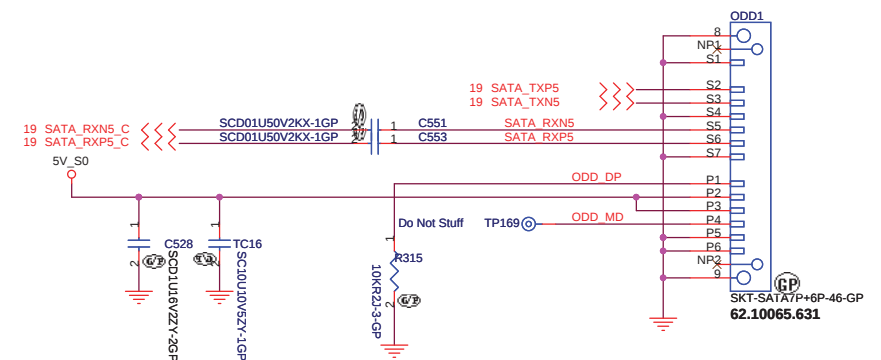






SB 不打Main source

SATA ODD Connector



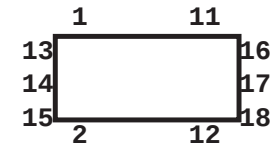
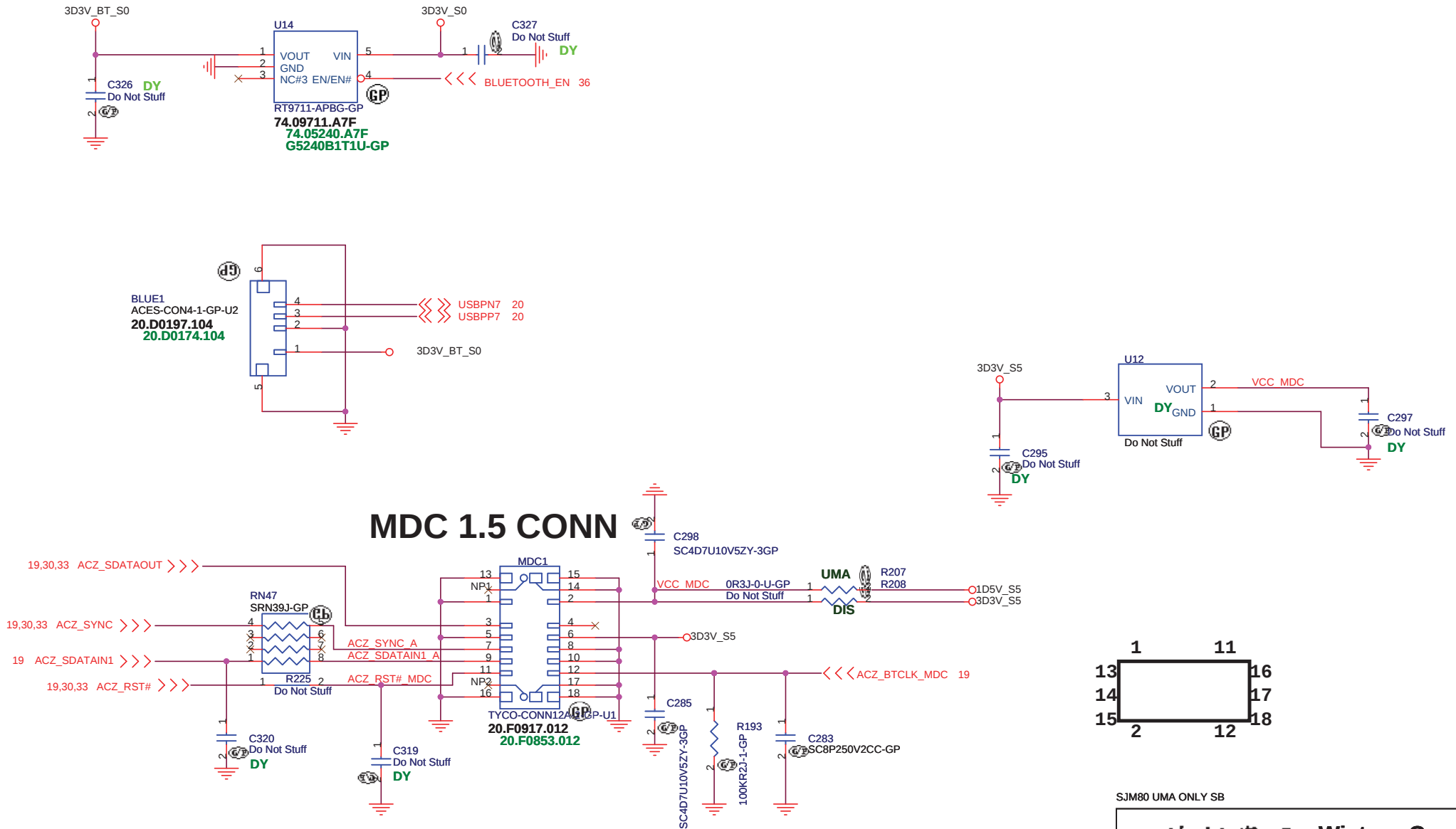
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
HDD & ODD			
Size	Document Number		Rev
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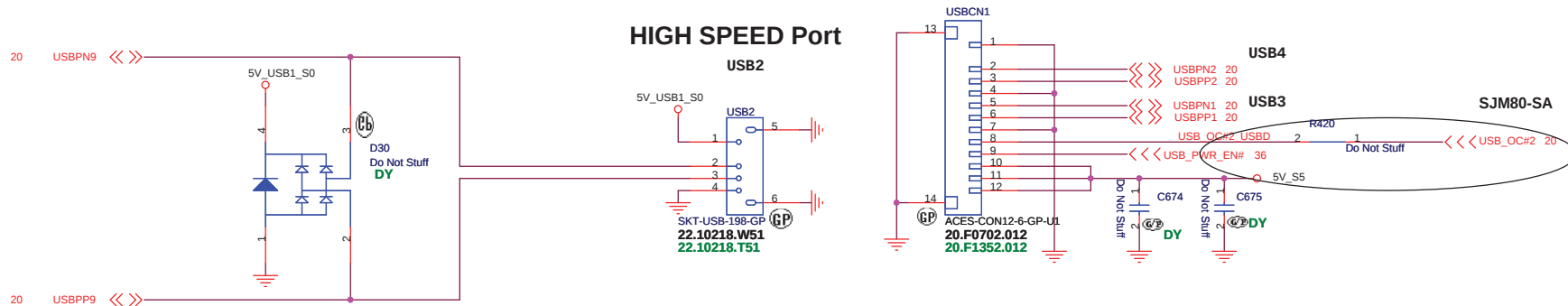
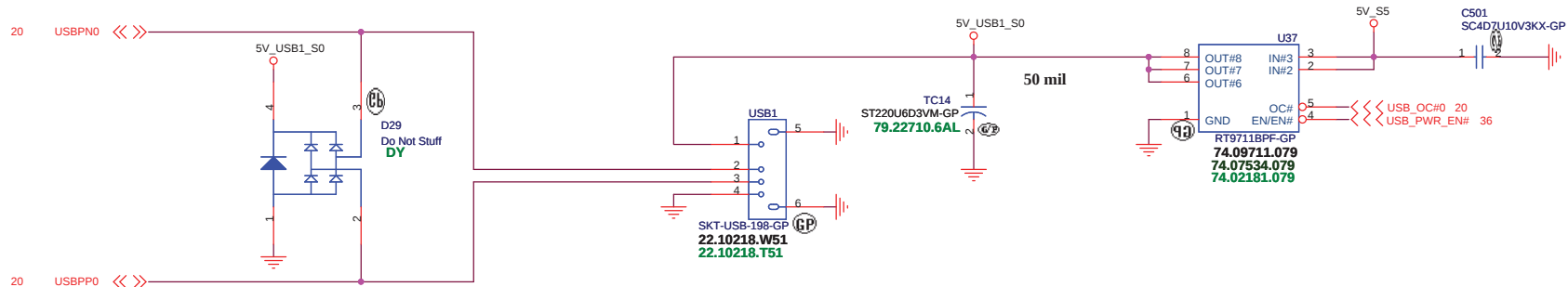
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



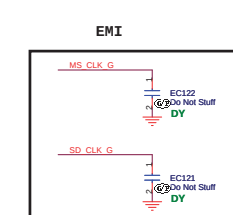
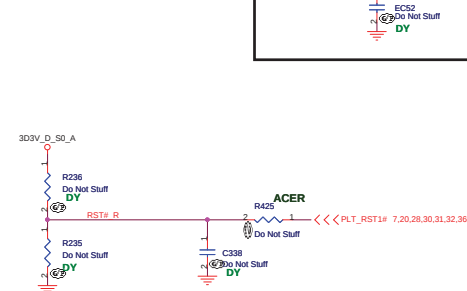
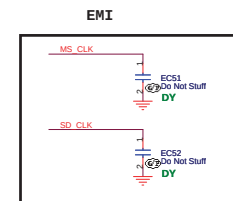
SJM80 UMA ONLY SB

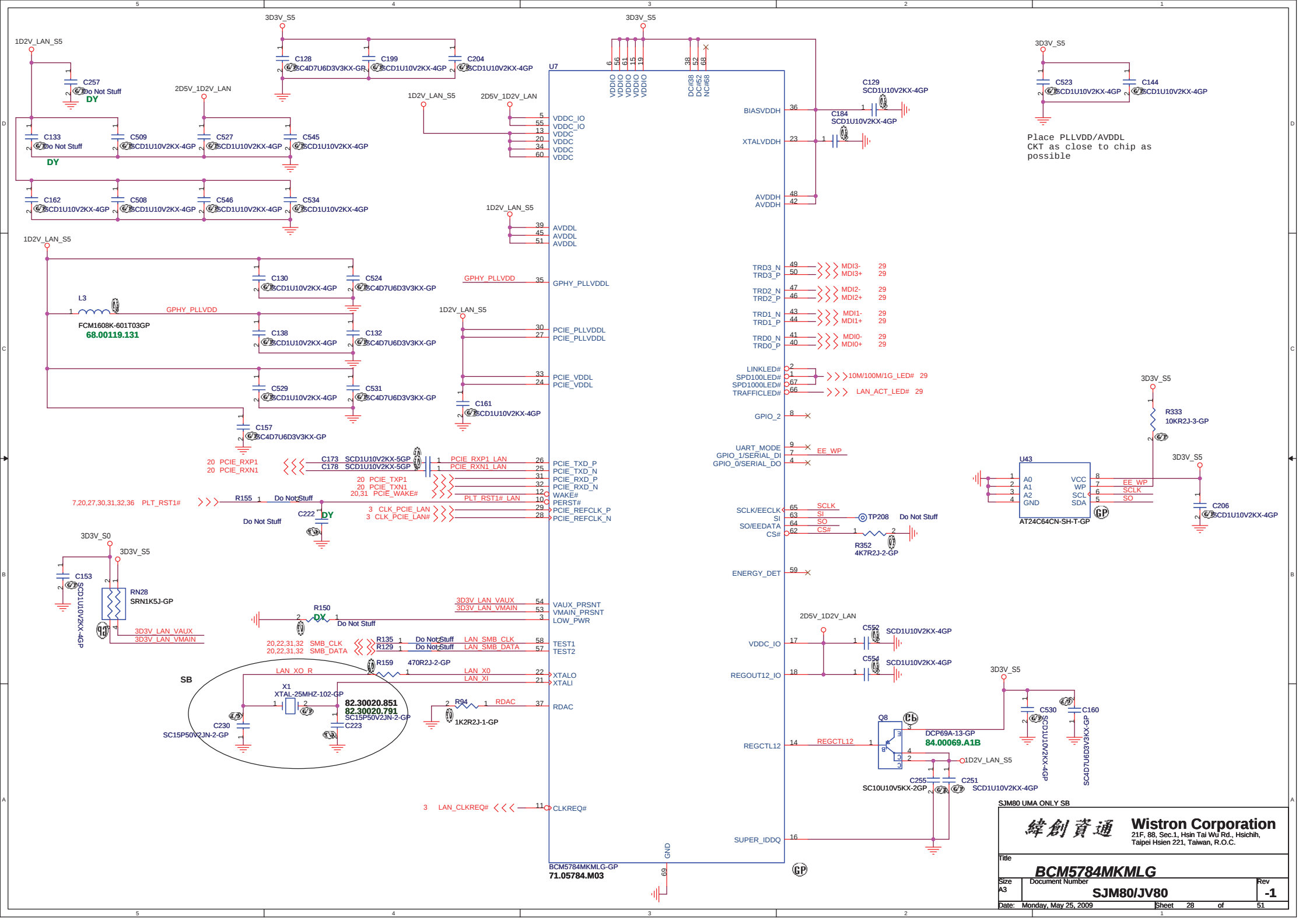
Title		Wistron Corporation	
Size		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Document Number		SJM80/JV80	
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USB connector			
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Title		BCM5784MKMLG	
Size	A3	Document Number	
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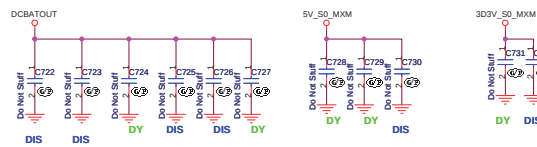
1. route on bottom as differential pairs.
2. Tx+Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

1. route on bottom as differential pairs.
2. Tx+Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LAN CONN			
Size	Document Number	Rev	
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PX Function

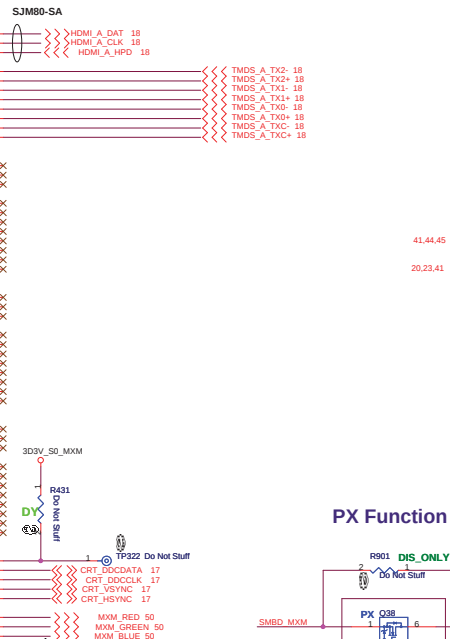
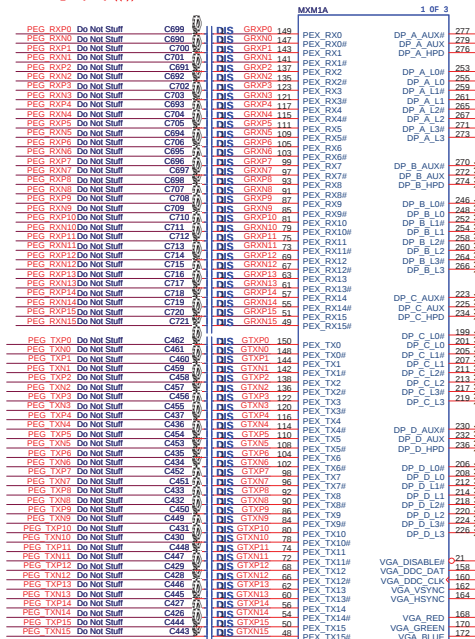


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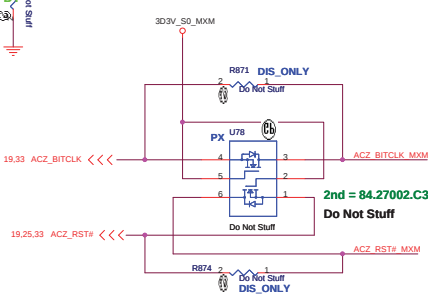
7 PEG_TXP[15..0] << >>
7 PEG_TXN[15..0] << >>

7 PEG_RXP[15..0] << >>
7 PEG_RXN[15..0] << >>

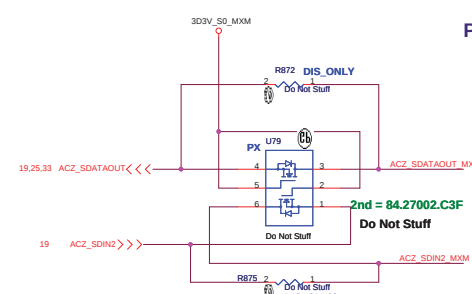
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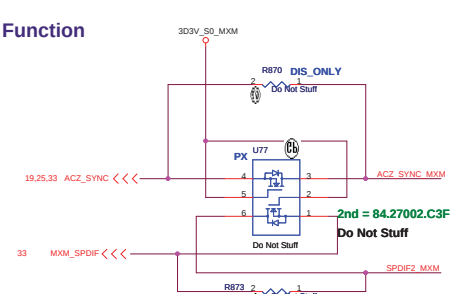
PX Function



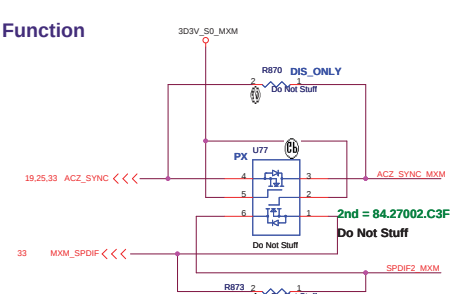
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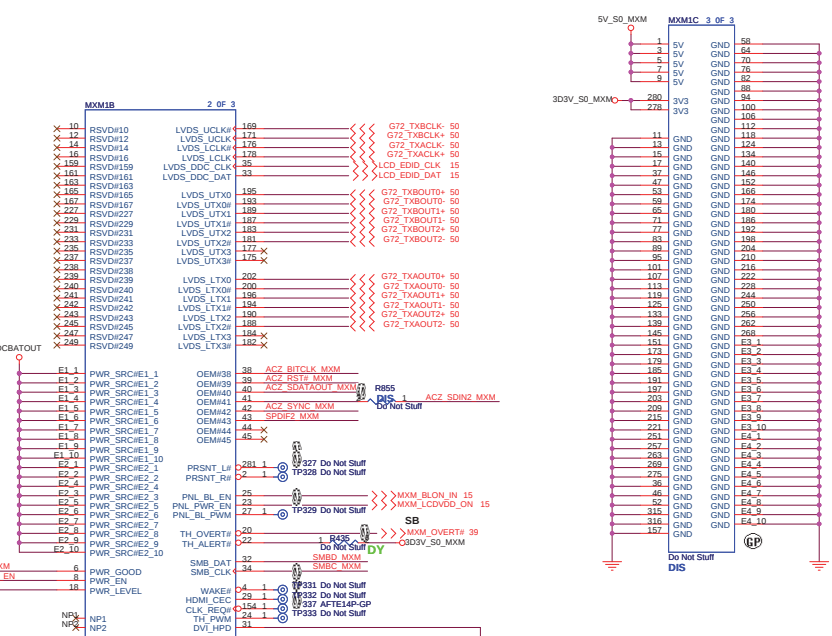
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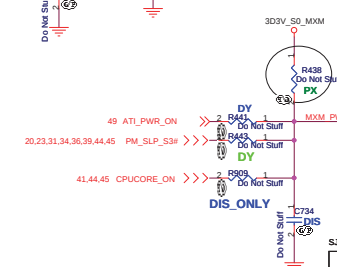
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PX Function

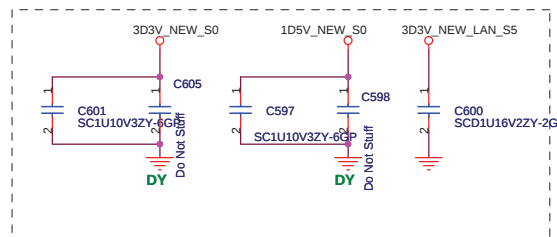


PX Function



TOP VIEW

26



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Title	Author	Date	Page
1. Introduction	John Doe	2023-10-27	10
2. Methodology	Jane Smith	2023-10-28	15
3. Results	Mike Johnson	2023-10-29	20
4. Discussion	Emily White	2023-10-30	25
5. Conclusion	David Brown	2023-10-31	30

NEW CARD

Size

Document Number

Rev

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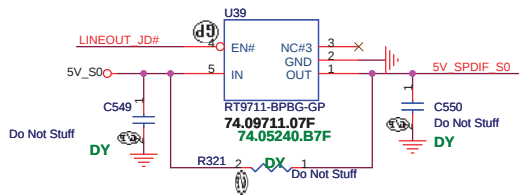
Date: Monday, May 25, 2009

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51

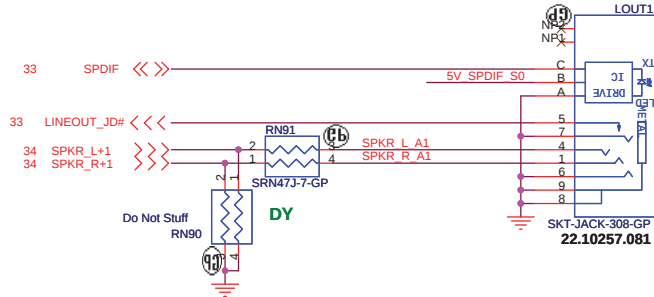
緯創資通 **Wistron Corporation**
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Title			
AUDIO AMP			
Size	Document Number		Rev
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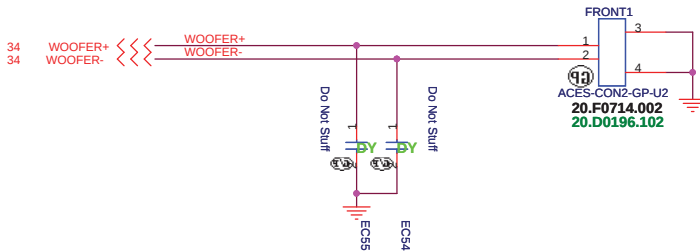


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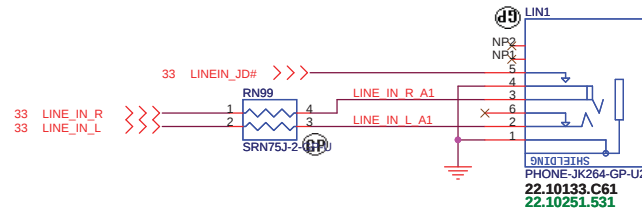
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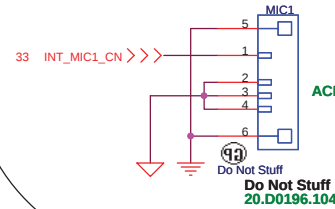
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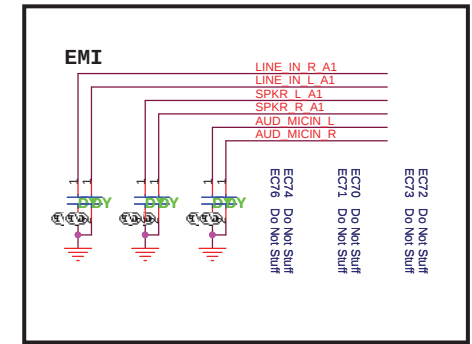
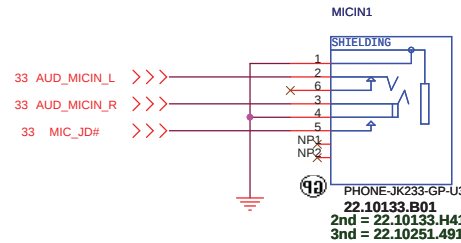
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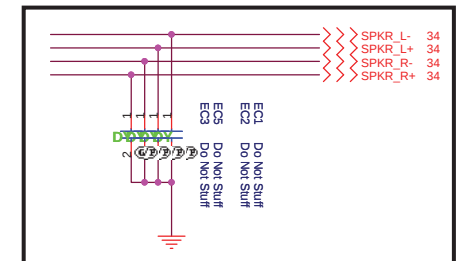
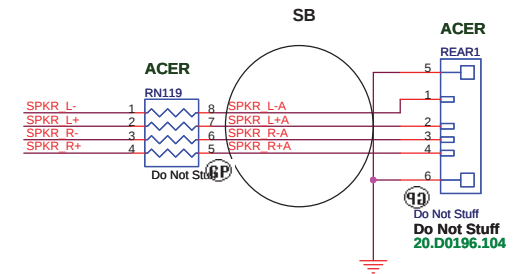
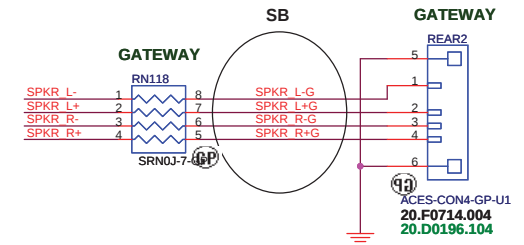
INT. MIC



MIC IN



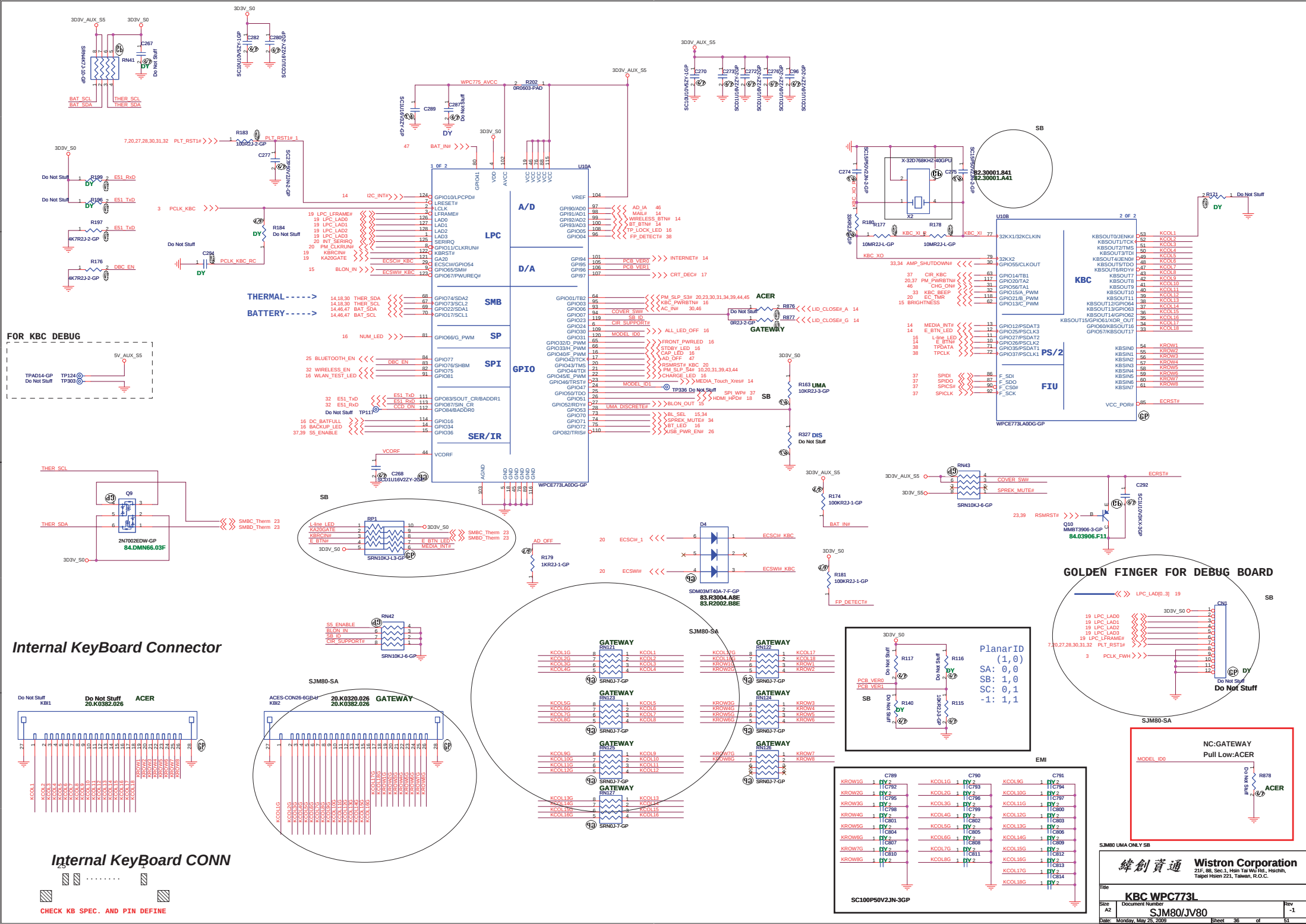
REAR Speaker



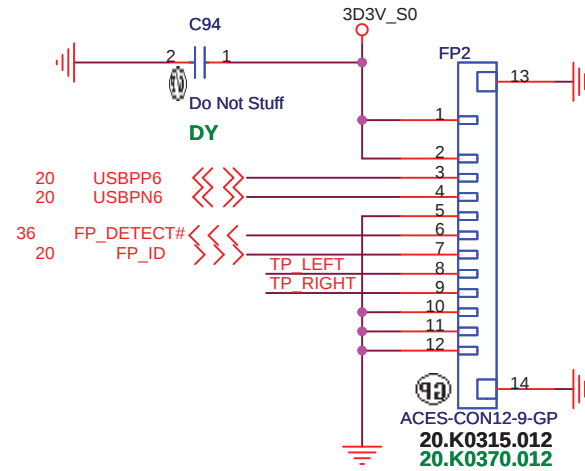
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Taipei Hsien 221, Taiwan, R.O.C.

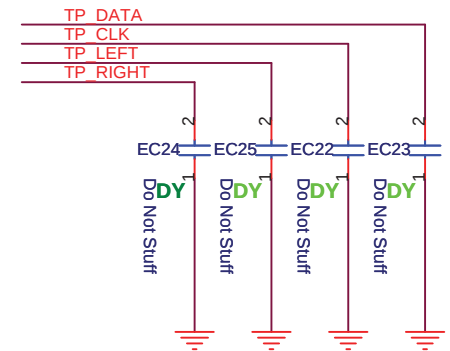
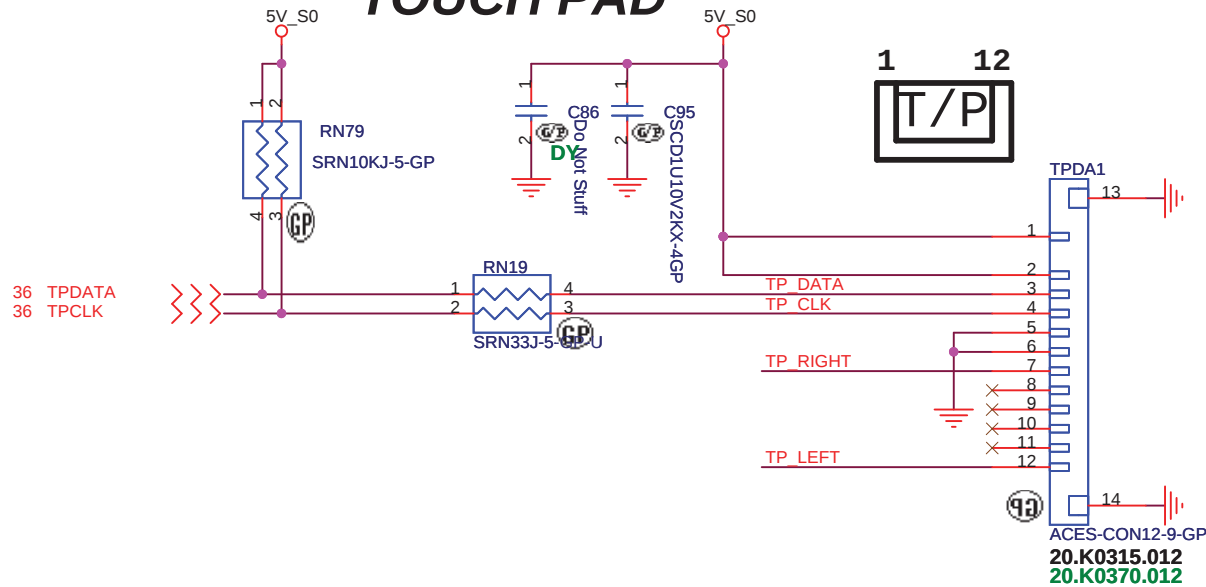
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AUDIO JACK		
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Finger printer



TOUCH PAD



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Title

Finger Printer and Touch PAD

Size
A4

Document Number

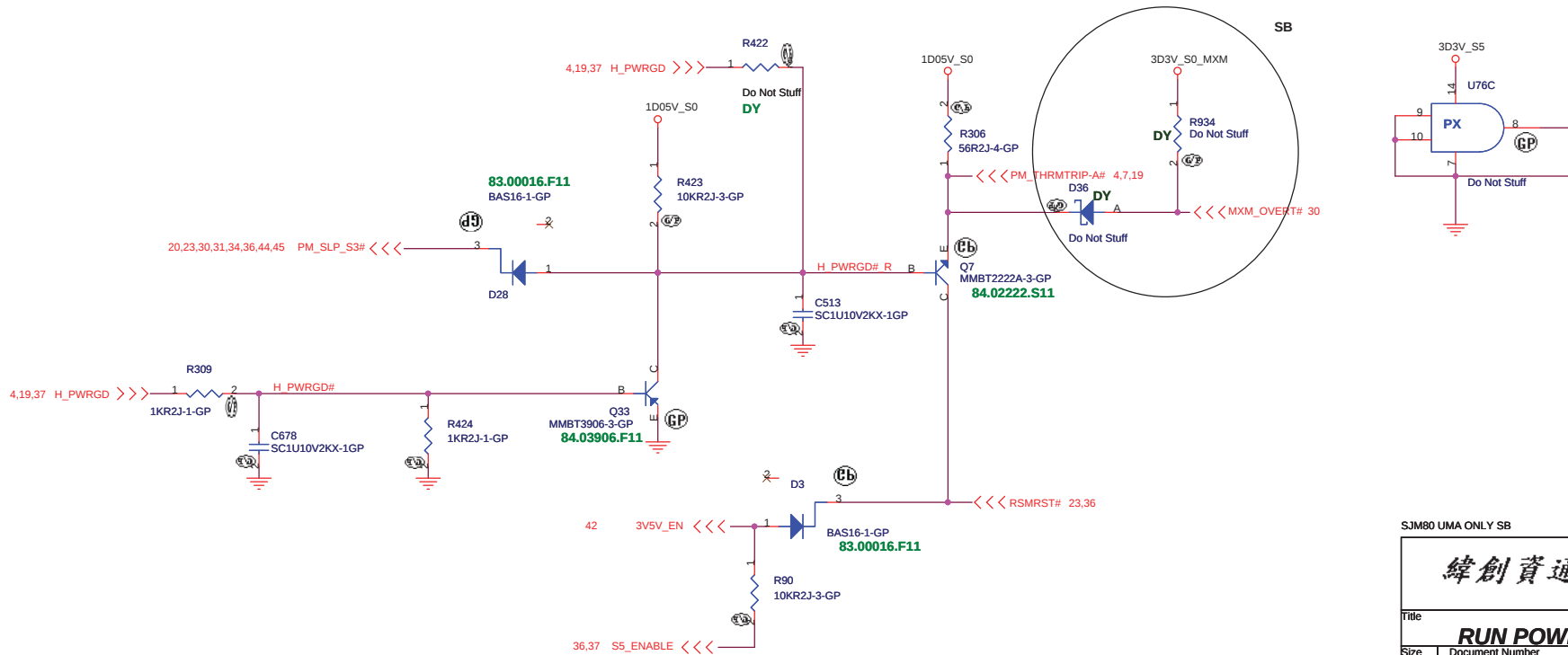
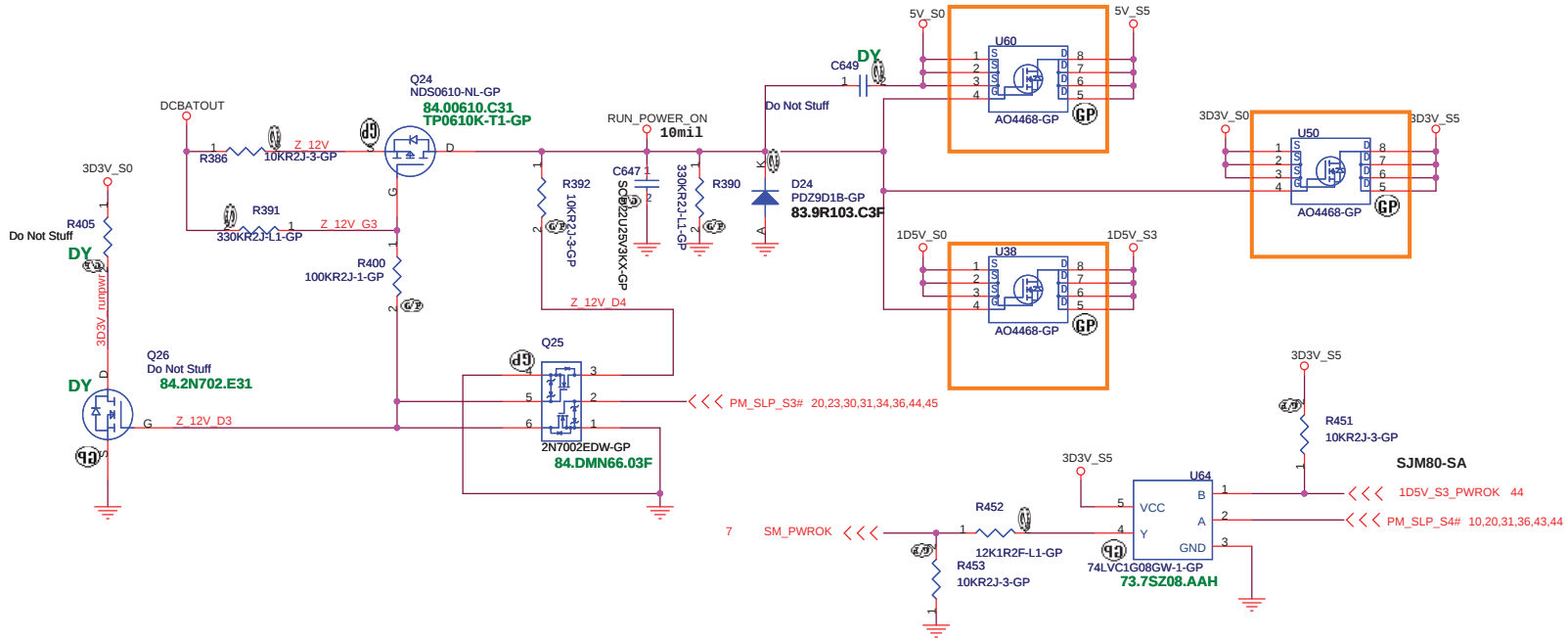
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Run Power



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Title

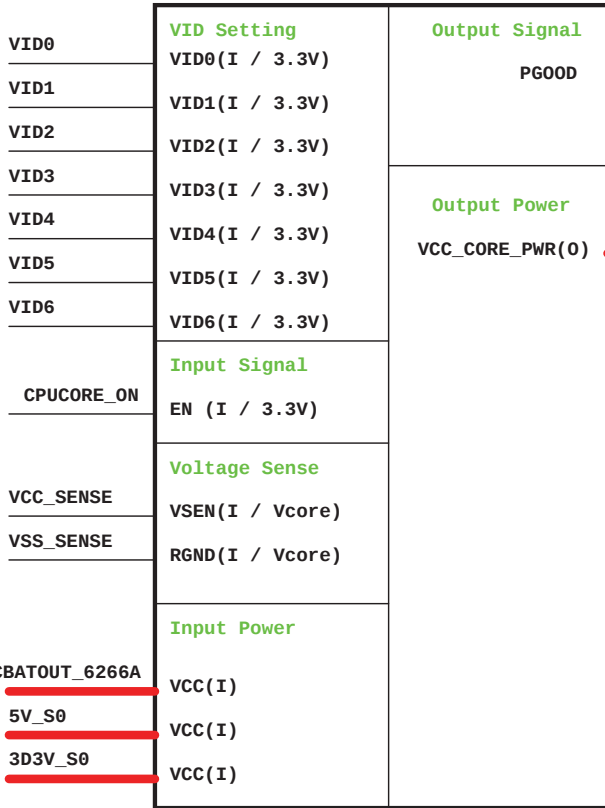
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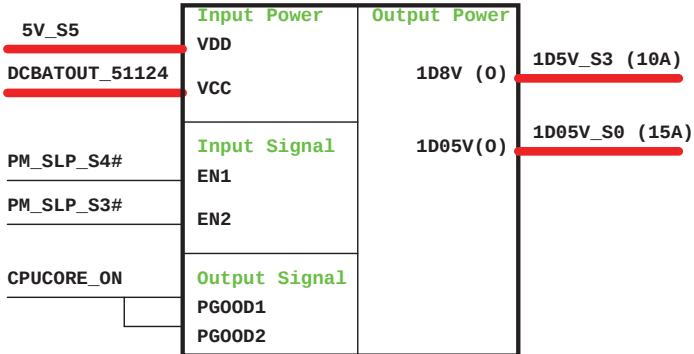
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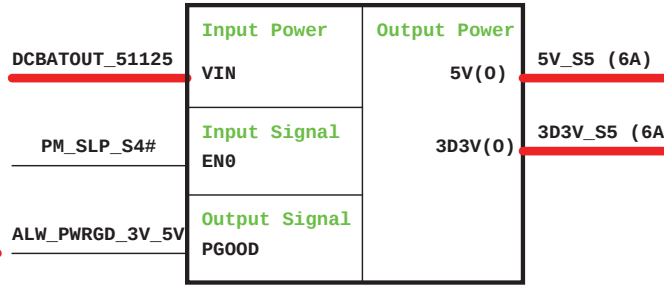
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ISL6266A



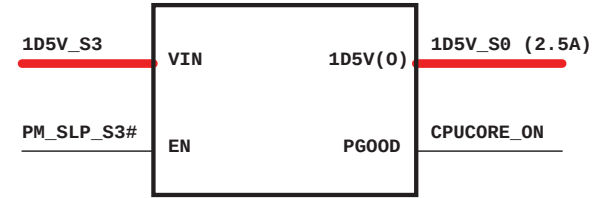
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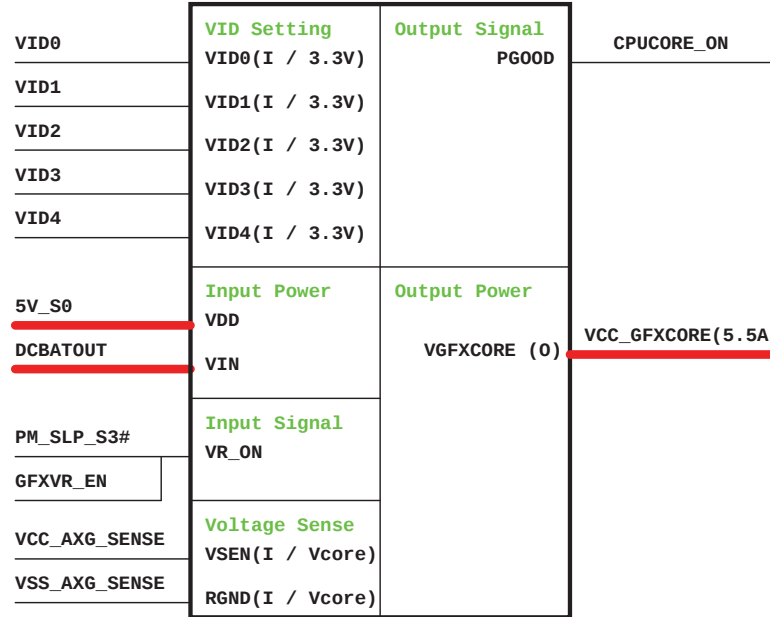
TPS51125
5V/3D3V



TPS51124
1D5V_S0



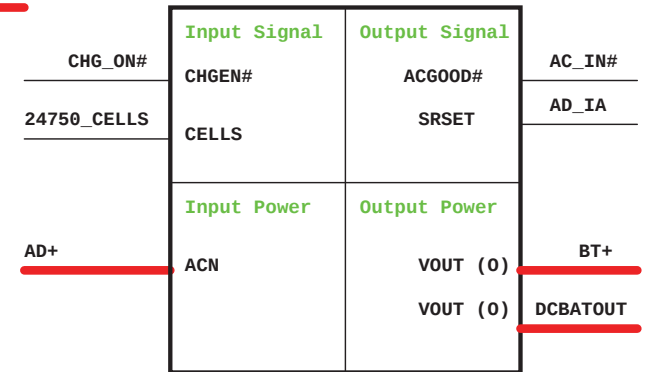
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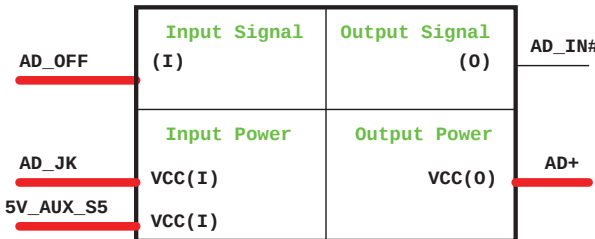
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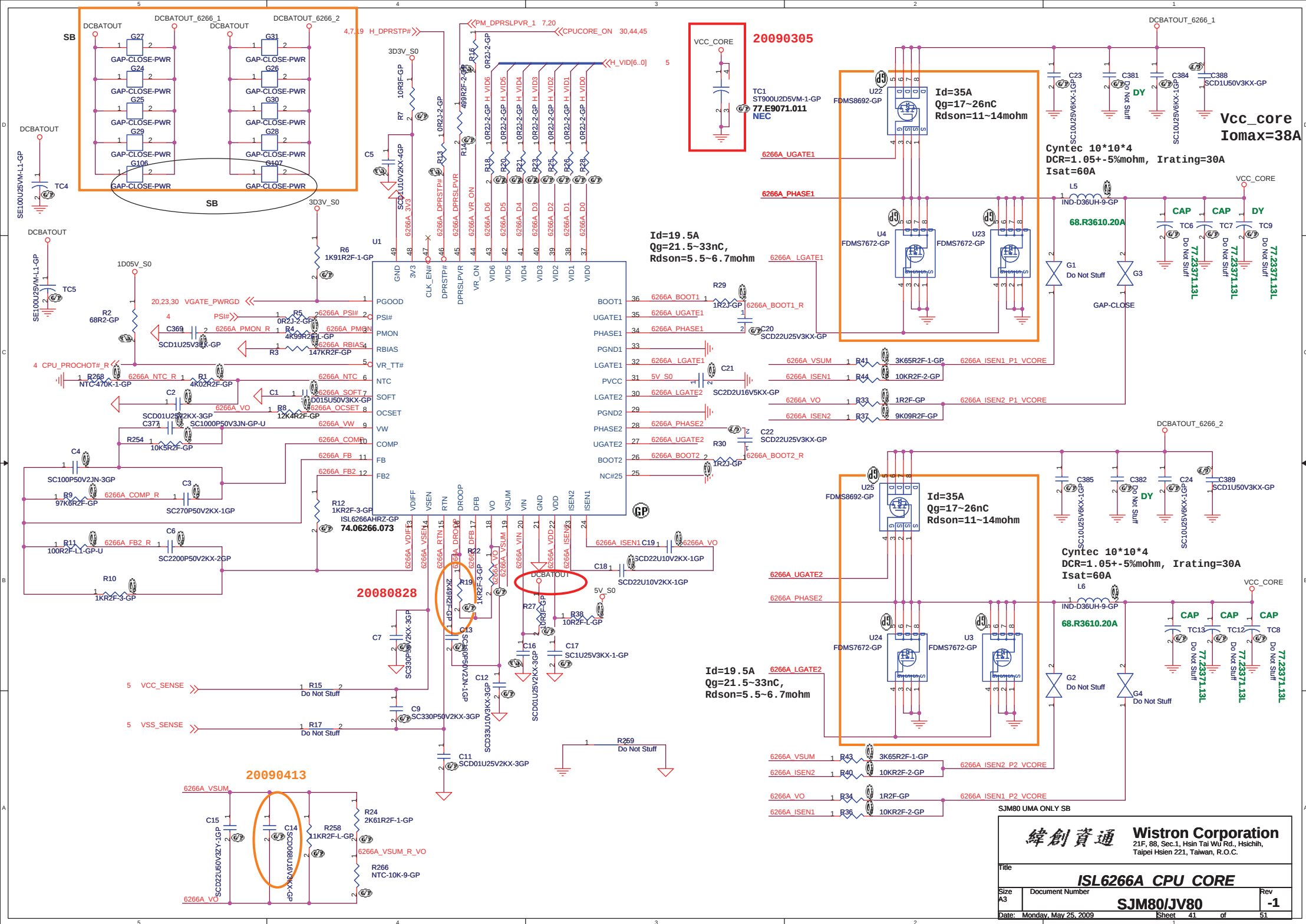


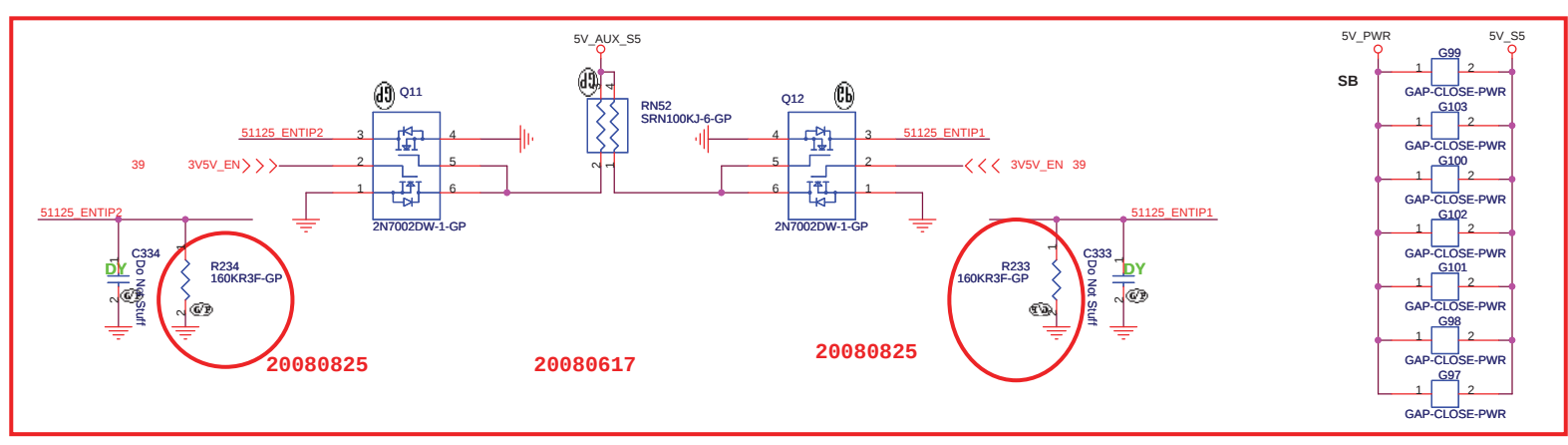
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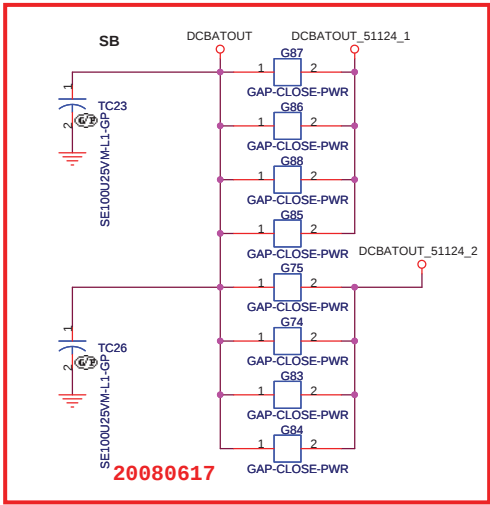


Adapter





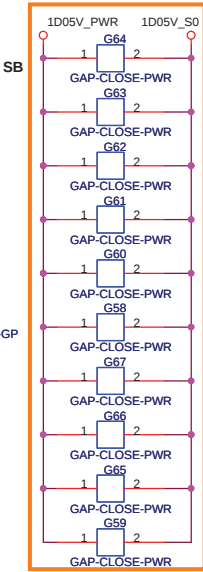
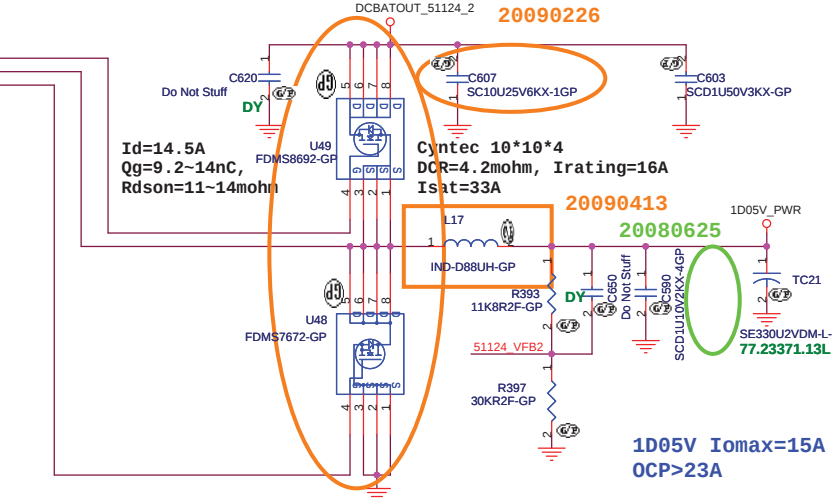
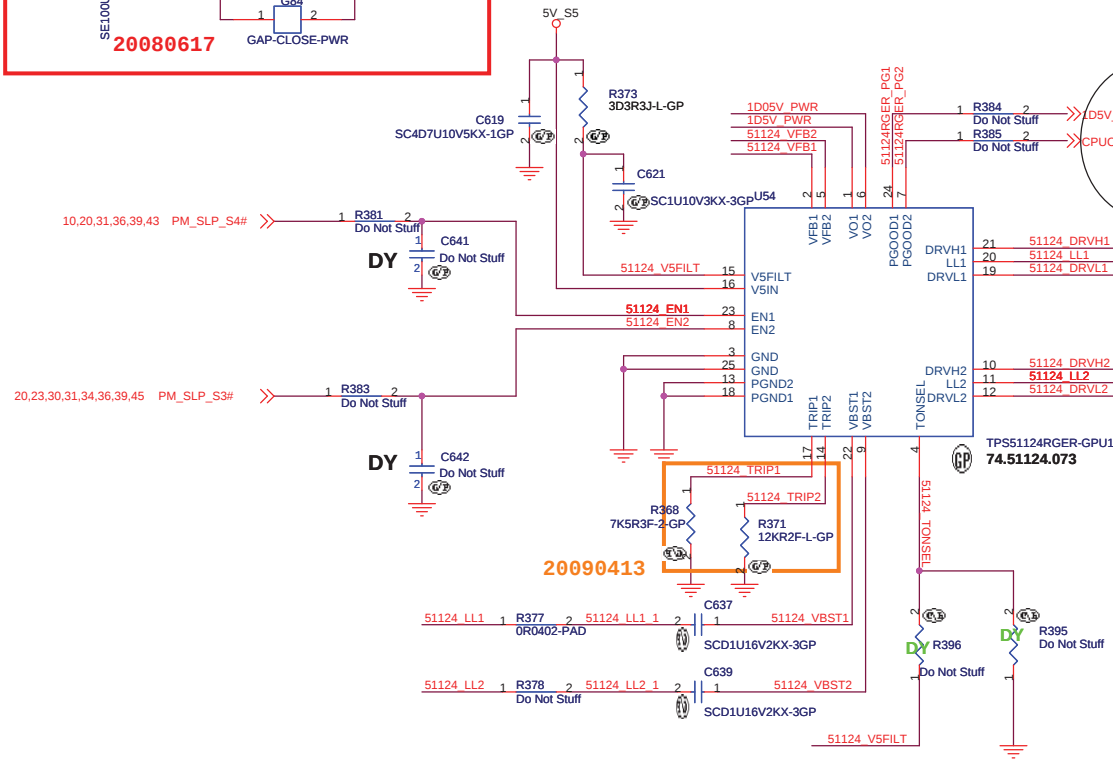
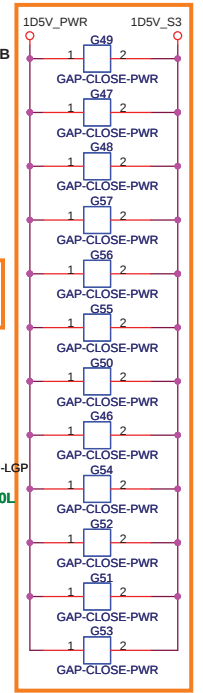
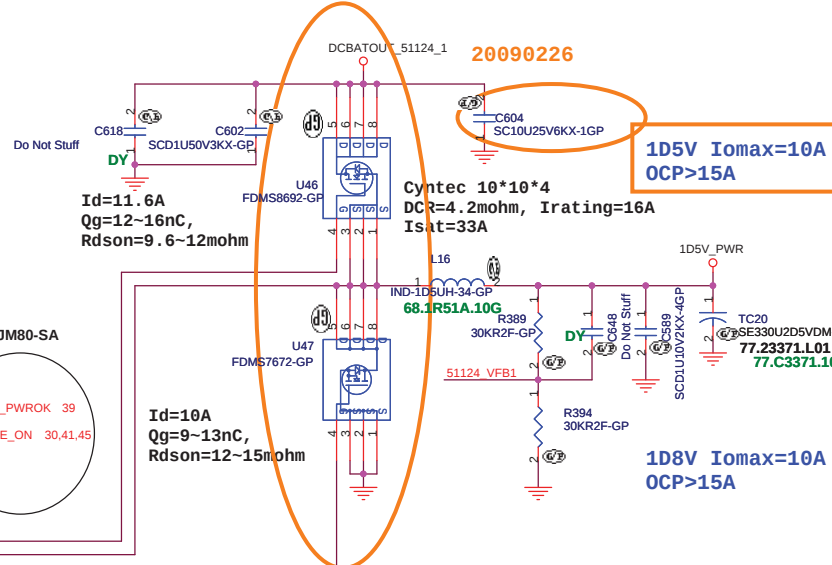




$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{ds(on)}) + ((1/(2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$$

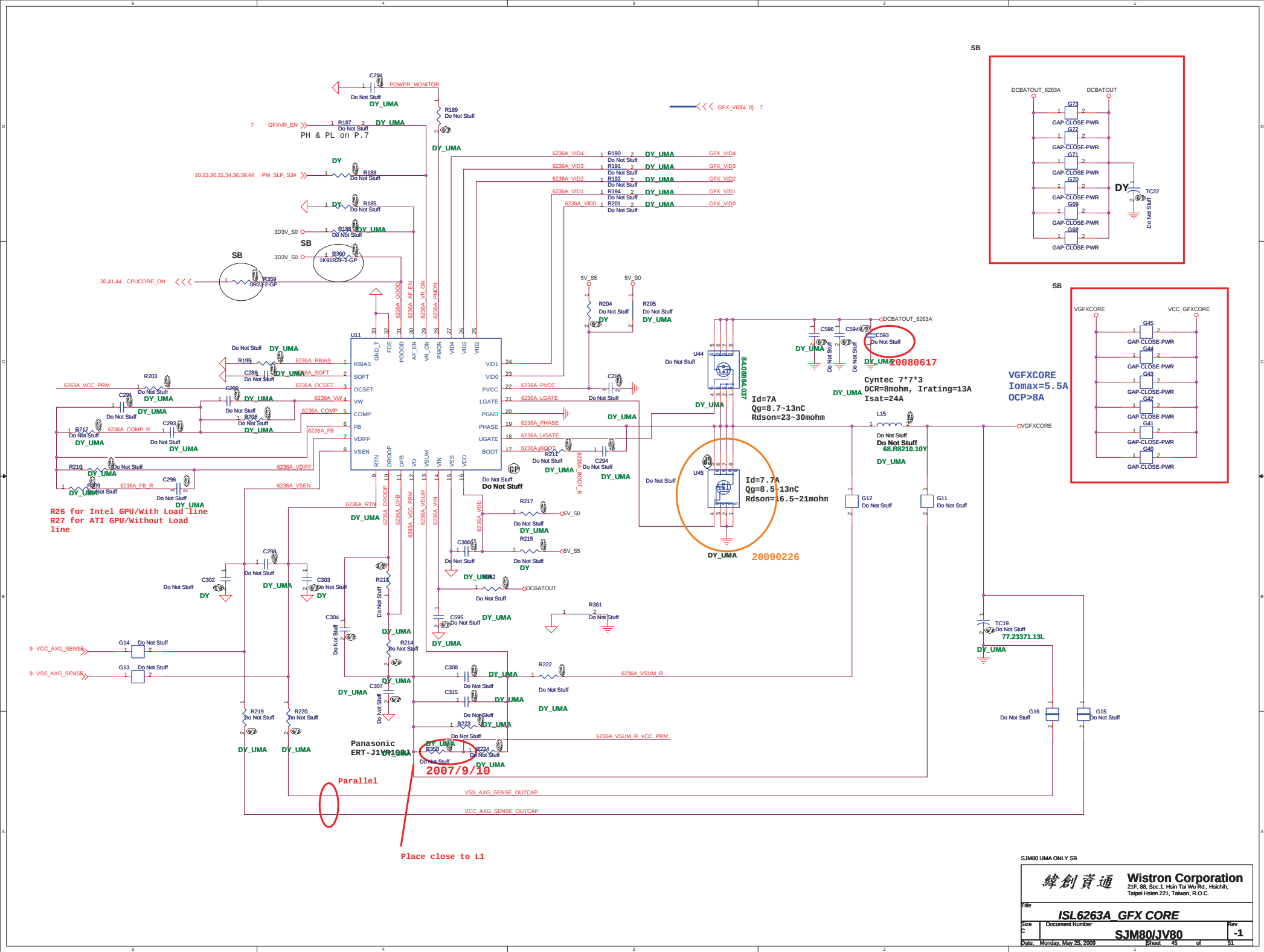
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L

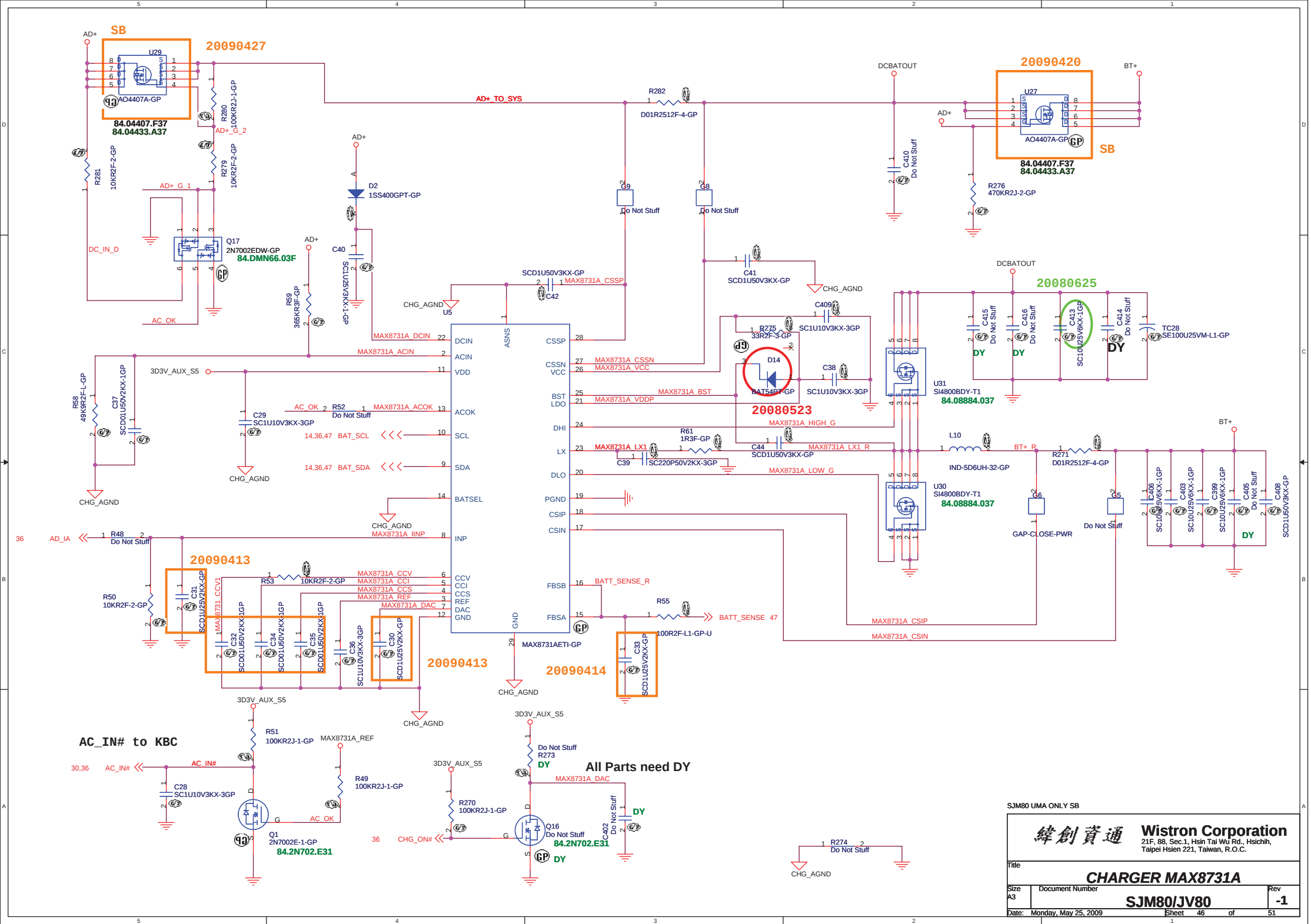


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

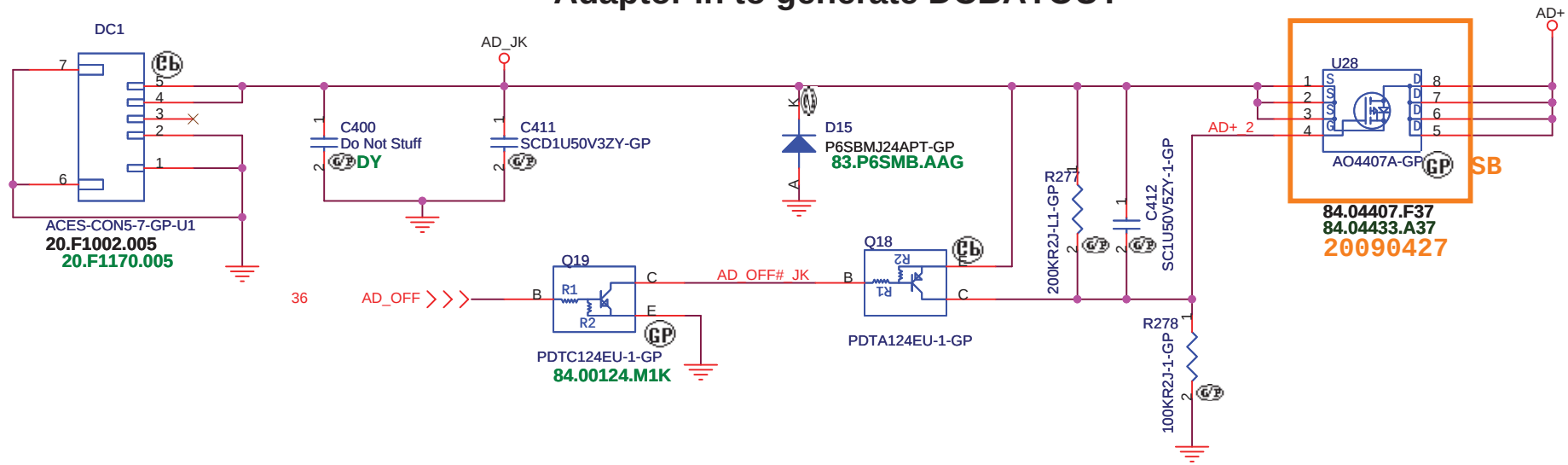
$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode

Id=19.5A
 Qg=21.5~33nC,
 Rdson=5.5~6.7mohm

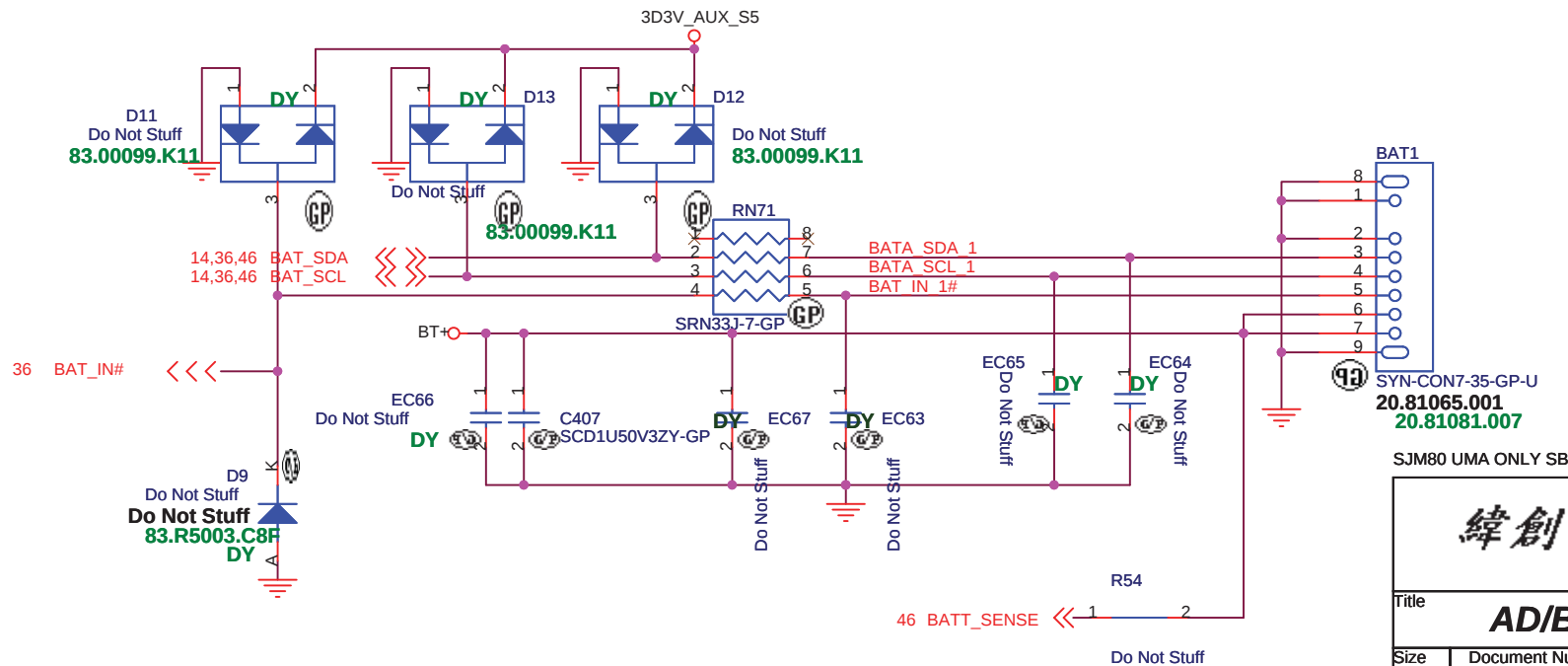




Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Taipei Hsien 221, Taiwan, R.O.C.

Title **AD/BATT CONN**

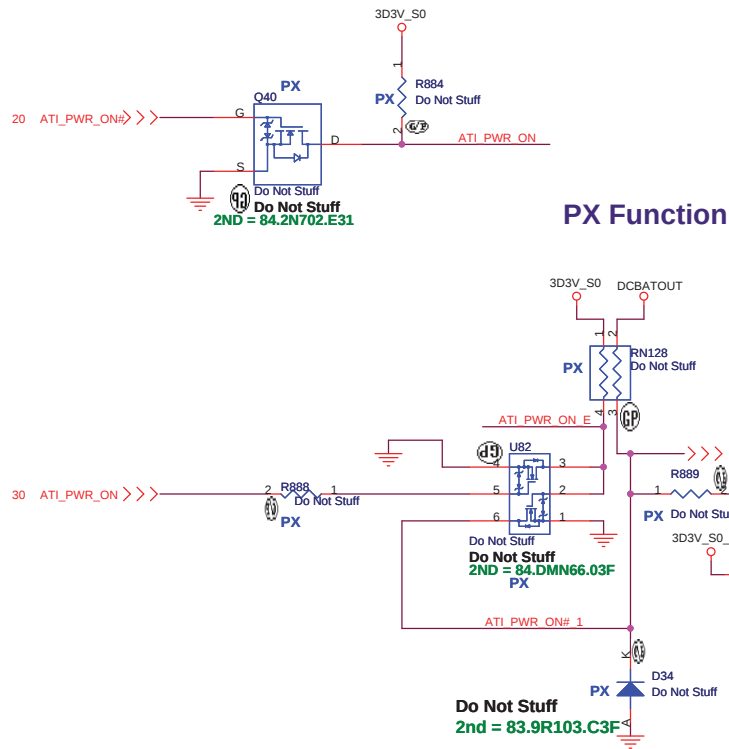
Size Document Number

SJM80/JV80

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-1

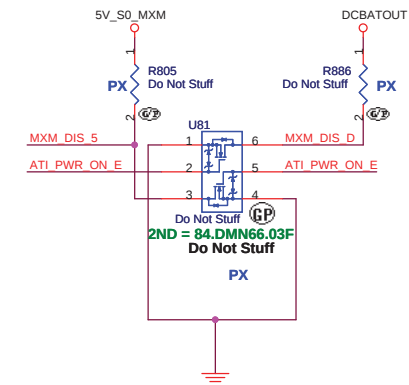
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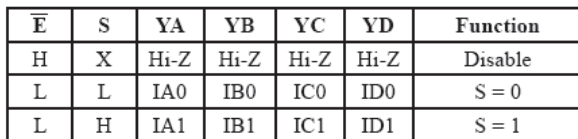
PX Function

PX Run Power Discharge circuit



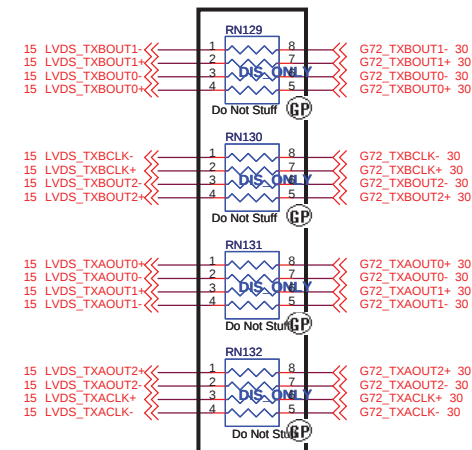
SJM80 UMA ONLY SB

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PX Run Power			
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$\bar{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

PX Function



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Title			
PX Switch			
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SJM80 Schematic EC Tracking Record LAB 0325 , 2009
EC #/ Page / Description / Part Affected

- EC SB03/26/change R359 R360 上#(for PX function)
- EC SB03/26/change RN27 RN31 RN32 RN33 上#(for PX function)
- EC SC03/30 change REAR1,REAR2 Net name
- EC SB03/31 add digital Mic function
- EC SB04/03 change Brightness setting from NB
- EC SB04/03 modify MMB BD add switch
- EC SB04/06 Change LAN Crystal setting
- EC SB04/07 Close Power GAP
- EC SB04/07 Change PCB Version
- EC SB04/13 Keep JV80 GPIO and Function Key
- EC SB04/20 add R946 R947 for BRIGHTNESS Bypass
- EC -105/03 change C834~C841 to 0 ohm for HDMI no display design
- EC -105/03 add R948 for DIS ONLY HDP
- EC -105/03 change R823 to R824 for CRT no display
- EC -105/13 change MXM Card Stand off part number
- EC -105/19 MMBCN1 power 3D3V change 5V (for MMB LED light display)
- EC -105/19 Modify HDMI hot plug schematic Location Q46
- EC -105/20 change R316 to 22R2 (For USB eye diagram)
- EC -105/20 change R398 6.5k to 7.1K increase 3.3V to 3.4V
- EC -105/21 Q46 HDMI hot plug change power 3D3V_S0_MXM to 5V_S0
- EC -105/22 add Cap for EMI at CRT RGB

EC -1 01/20/Change R316 to 22D6R2F(For USB eye diagram)

SJM80 UMA ONLY SB

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Title

EC Tracking Record

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