ZYA SYSTEM BLOCK DIAGRAM

GPU CORE PWR ISL6264 P43	CHARGER ISL88731 P37
GPU IO PWR ISL62827 P44	3/5V SYS PWR RT8206 P38
DISCHARGER +3V,+ 5V,+1.5V,+1.05V,+1.1V_VTT P46	CPU CORE PWR ISL62882 P39
+1.0V/+1.8V RT9018A + TPS54418 P47	CPU VTT UP61111AQDD P40 (ARD: 1.05V CFD: 1.1V)
CPU VGFX_AXG ISL62881 P45	VTT 1.05V UP61111AQDD P41
THERMAL PROTECTION P47	DDR3 PWR RT8207A P42

CLOCK GENERATOR
SELGO: SLG8SP595V
P3
X'TAL 14.318MHz

BCLK: 133MHz
PEG_CLK: 100MHz
DPLL_REF_SSCLK: 120MHz

intel
<MCH Processor>
Arrandale (SG)*
Clarksfield (Discrete)
rPGA 989
(37.5mm X 37.5mm)
P4.5.6.7
DDR SYSTEM MEMORY
PCI-E X16
FDI
DMI

Fan Driver
(PWM Type)
P35

DDR III
SO-DIMM 0
SO-DIMM 1
SO-DIMM 2
SO-DIMM 3
P14, 15, 16, 17

Dual Channel
800/ 1066 MHz
800 MT/s 1066 MT/s

PCIE
2.5GT/s

AMD GPU
Broadway-Pro / Madison-Pro
1GB (64Mb x 32 IO x 8 pcs)
P19,20,21,22,23,24,25,26
X'TAL 27.0MHz

HDMI
CRT
LVDS

HDMI P28
CRT P27
LVDS P27

LVDS_CRT Switch Grapgics
P27

*[Arrandale Only]
X4 DMI interface

INT_CRT *[Arrandale Only]
INT_LVDS *[Arrandale Only]

intel
<PCH>
Ibex Peak_M
mBGA 676
(27mm X 25mm)
P8.9.10.11.12.13
Graphics Interfaces
SATA
3.0 GT/s
USB
HDA
SPI
LPC
PCI-E
RTC
P9
X'TAL 32.768KHz

Note:
HM55 does not support USB 6 & 7
HM55 does not support SATA 2 & 3

HDD (SATA) *2
P29
SATA0
SATA5

ODD (SATA)
P29
SATA1

eSATA Conn.
USB 9 (Debug) P34

eSATA Buffer
P34
SATA4

USB Port x 5
USB 1, 3, 11, 12 (Debug) P34
USB 2.0

Bluetooth
USB 4 P35

CCD
USB 8 P27

FingerPrint
USB 2 P35

Azalia

Audio CODEC
ALC669X
P31

SPI ROM
4MB x1 (Basic ME+Braidwood)
P9

EC (WPC781)
P36
X'TAL 32.768KHz

SPI ROM P36

Touch Pad P35

K/B COON. P36

CIR P36

PCI-Express
2.5GT/s

PCIE-5
CLKOUT_PCIE2

IEEE1394 & Media Cardreader
OZ888
P33
X'TAL 24.576MHz

IEEE1394a connector P33

Card Reader Connector P33

PCIE-6
CLKOUT_PEG_B

Atheros Giga-LAN
AR8151
P34 & Daughter Board
X'TAL 25MHz

Transformer
Daughter Board

RJ45 Connector
Daughter Board

PCIE-1 & 2
CLKOUT_PEG_1&3

Mini Card
WLAN / TV
USB 10 & 13
P30

Front Stereo Amp (G1453L/ 2W+2W) P32
Center Mono Amp (G1442/ 2W) P31
Rear Audio Amp & Head phone AN12947A P30
Sub-Amplifier (TPA311D1) P32

Front Speaker P32
Center Speaker P32
Speaker P30
S/PDIF P30
SUBWOOFER P32
Line in P32
MIC Jack P32
Int. D-MIC P32

SSID: DISCRETE: 030A
SSID: SWITCH GFX: 0308

SVID: 1025

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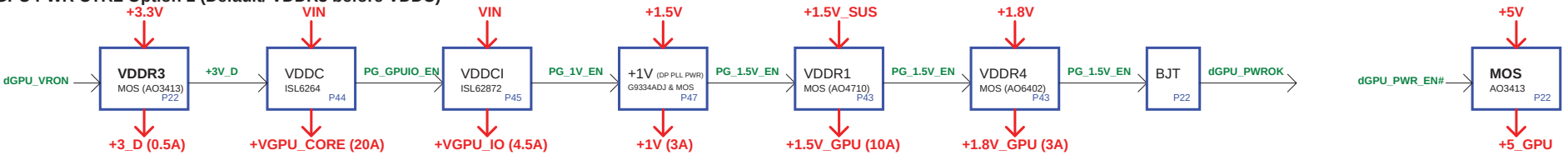
PROJECT : ZYA

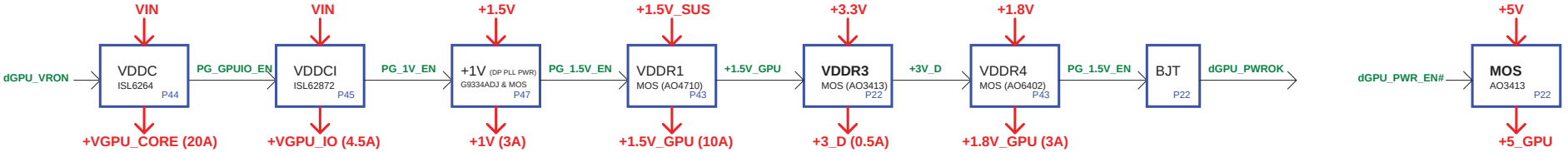
Size	Document Number	Rev
	ZYA Block Diagram	1A

Date: Wednesday, January 20, 2010 Sheet 1 of 50

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



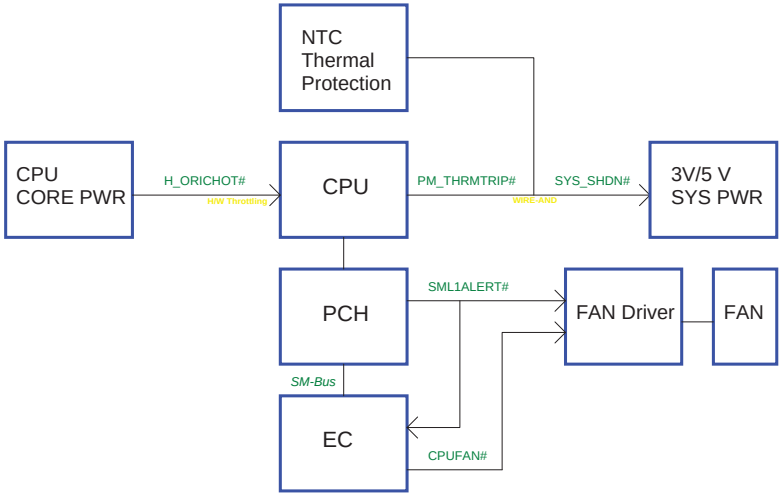
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

Date: Wednesday, January 20, 2010 Sheet 2 of 50

REV : B chenge pin define for B-test

+1.5V **150mA(20mil)** C10050 close L35

L26 BLM18AG601/0.2A_6

180ohm/1.5A

R402 *0_6

C579 *10u/6.3V_8 | C575 .1u/16V_4 | C535 .1u/16V_4 | C565 .1u/16V_4

+1.5V_CLK

+3V

L31 BLM18AG601/0.2A_6

+3V_CLK

C10000 close L72

C584 10u/6.3V_8 | C533 0.1u/10V_4 | C560 0.1u/10V_4

[10] CLK_ICH_14M R381 33_4 CPU_SEL

C556 33p_4 | C546 33p_4

Y2 14.318MHZ

XTAL_IN | XTAL_OUT

U20

1	VDD_DOT	VDD_SRC_I/O	15
17	VDD_SRC	VDD_CPU_I/O	18
24	VDD_CPU	DOT_96	3
5	VDD_27	DOT_96#	4
29	VDD_REF	27M	6
31	SDA	27M_SS	7
32	SCL	SRC_1/SATA	10
30	REF_0/CPU_SEL	SRC_1#/SATA#	11
28	XTAL_IN	SRC_2	13
27	XTAL_OUT	SRC_2#	14
2	VSS_DOT	*CPU_STOP#	16
8	VSS_27	CPU_1	20
9	VSS_SATA	CPU_1#	19
12	VSS_SRC	CPU_0	23
21	VSS_CPU	CPU_0#	22
26	VSS_REF	CKPWRGD/PD#	25
33	GND		

SLG8LV595V

+VDDIO_CLK

DOT_96 → CLK_BUF_DREFCLK [10]; DOT_96# → CLK_BUF_DREFCLK# [10]

R395 B@0_4 | R396 *0_4 → 27M_CLK [20]

For ATI suggest

SRC_1/SATA → CLK_BUF_DREFSSCLK [10]; SRC_1#/SATA# → CLK_BUF_DREFSSCLK# [10]

SRC_2 → CLK_BUF_PCIE_3GPLL [10]; SRC_2# → CLK_BUF_PCIE_3GPLL# [10]

Switch CLK_BUF_DREFSSCLK and CLK_BUF_PCIE_3GPLL on ver B(SATA)

R354 10K_4 → +3V

CPU_1 → TP23; CPU_1# → TP21

CPU_0 → CLK_BUF_BCLK [10]; CPU_0# → CLK_BUF_BCLK# [10]

CK_PWRGD_R

80mA(20mil) C465 close L36 +1.05V

BKP1608HS181T_6_1.5A L29

C534 .1u/16V_4 | C558 .1u/16V_4 | C557 10u/Y5V_8

SLG8SP595V	STUFF L35 (default)
SLG8SP585V	STUFF R10000

For EMI

CLK_ICH_14M C561 *10p/50V_4

27M_CLK C580 *10p/50V_4

CPU_CLK select

+1.05V

R386 *4.7K_4

CPU_SEL

R388 4.7K_4

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus

+3V

R399 4.7K_4

[10] ICH_SMBDATA — Q23 2N7002K — CLK_SDATA — CLK_SDATA [14,15,16,17,30]

+3V

R400 4.7K_4

[10] ICH_SMBCLK — Q24 2N7002K — CLK_SCLK — CLK_SCLK [14,15,16,17,30]

CLK Enable

+3V

R343 1K/F_4

CK_PWRGD_R

Q20 2N7002K

[39] VR_PWRGD_CK505# — R345 100K/F_4

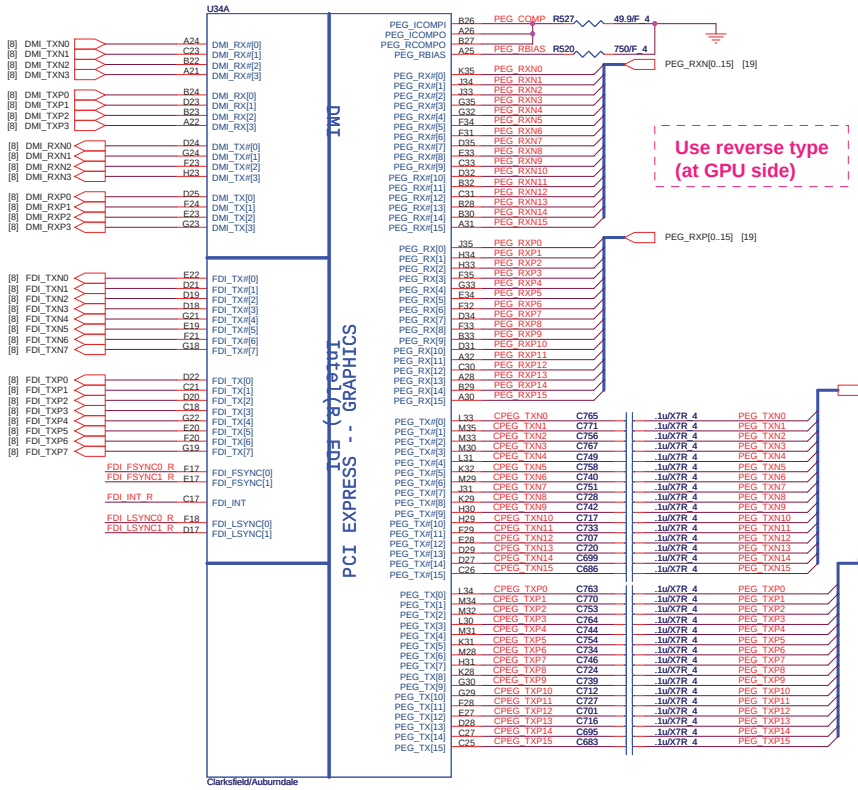
Quanta Computer Inc.

PROJECT : ZYA

Size	Document Number	Rev
	Clock Generator	1A

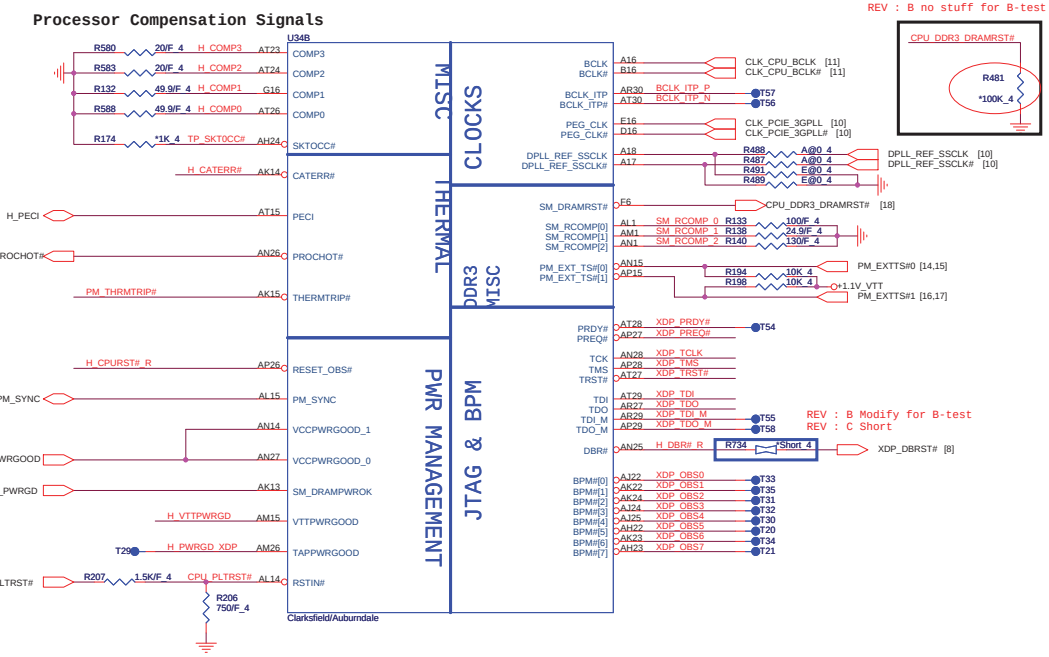
Date: Wednesday, January 20, 2010 Sheet 3 of 50

AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

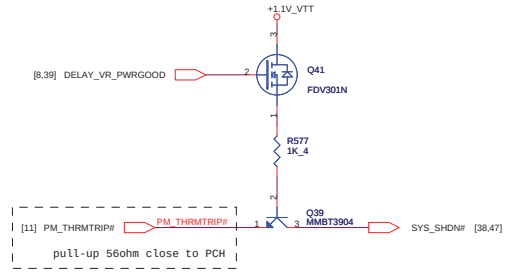


AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

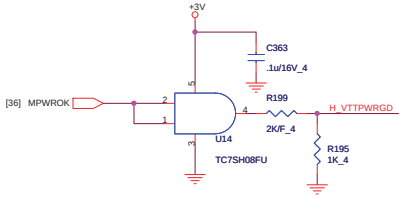
REV : B no stuff for B-test



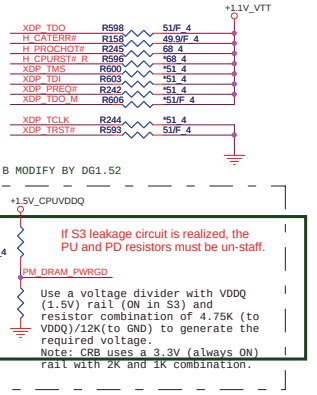
Thermaltrip protect

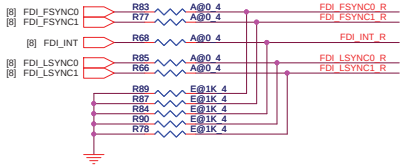


VTT PWR_Good



Processor pull-up



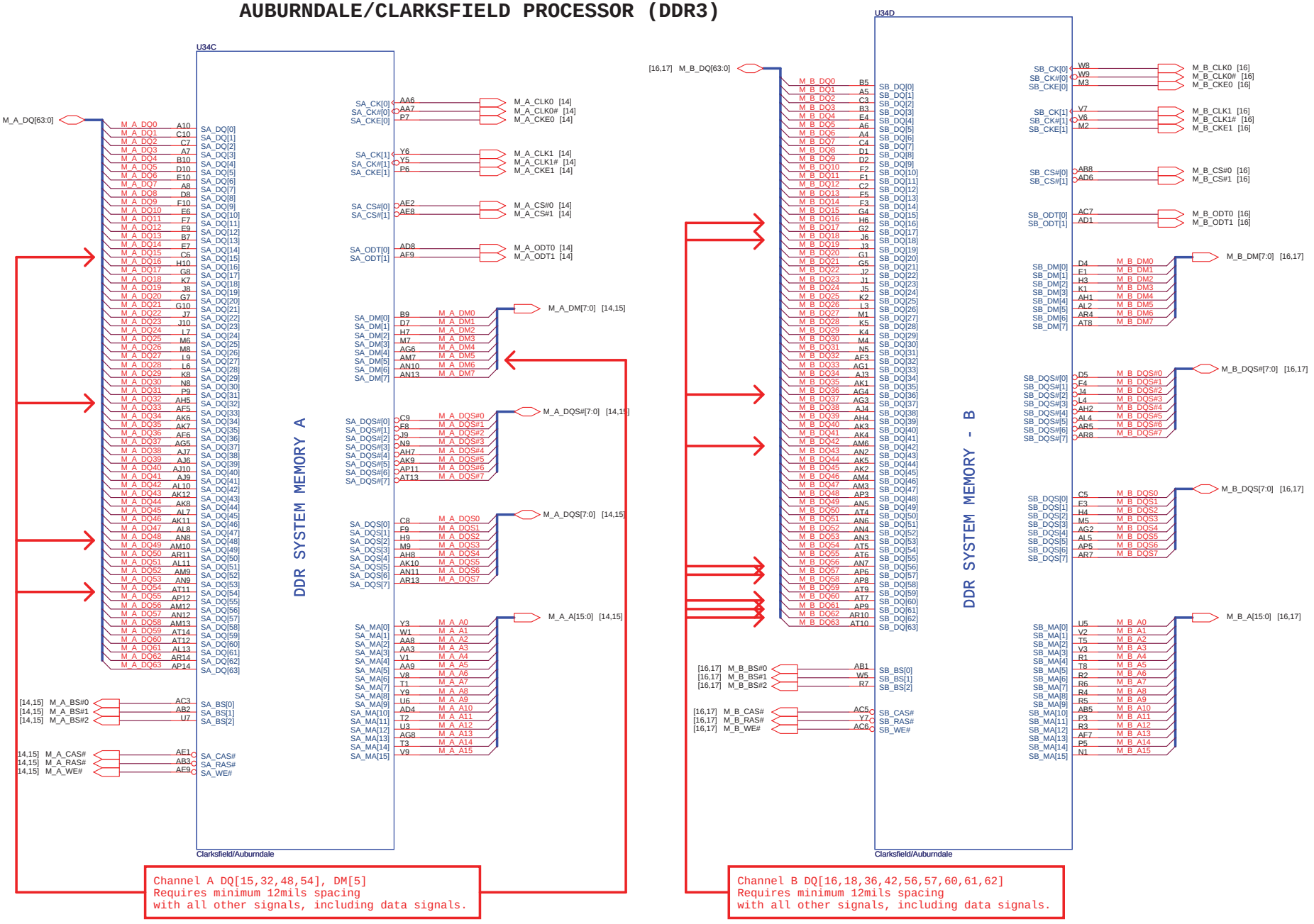


Quanta Computer Inc.
PROJECT : ZYA

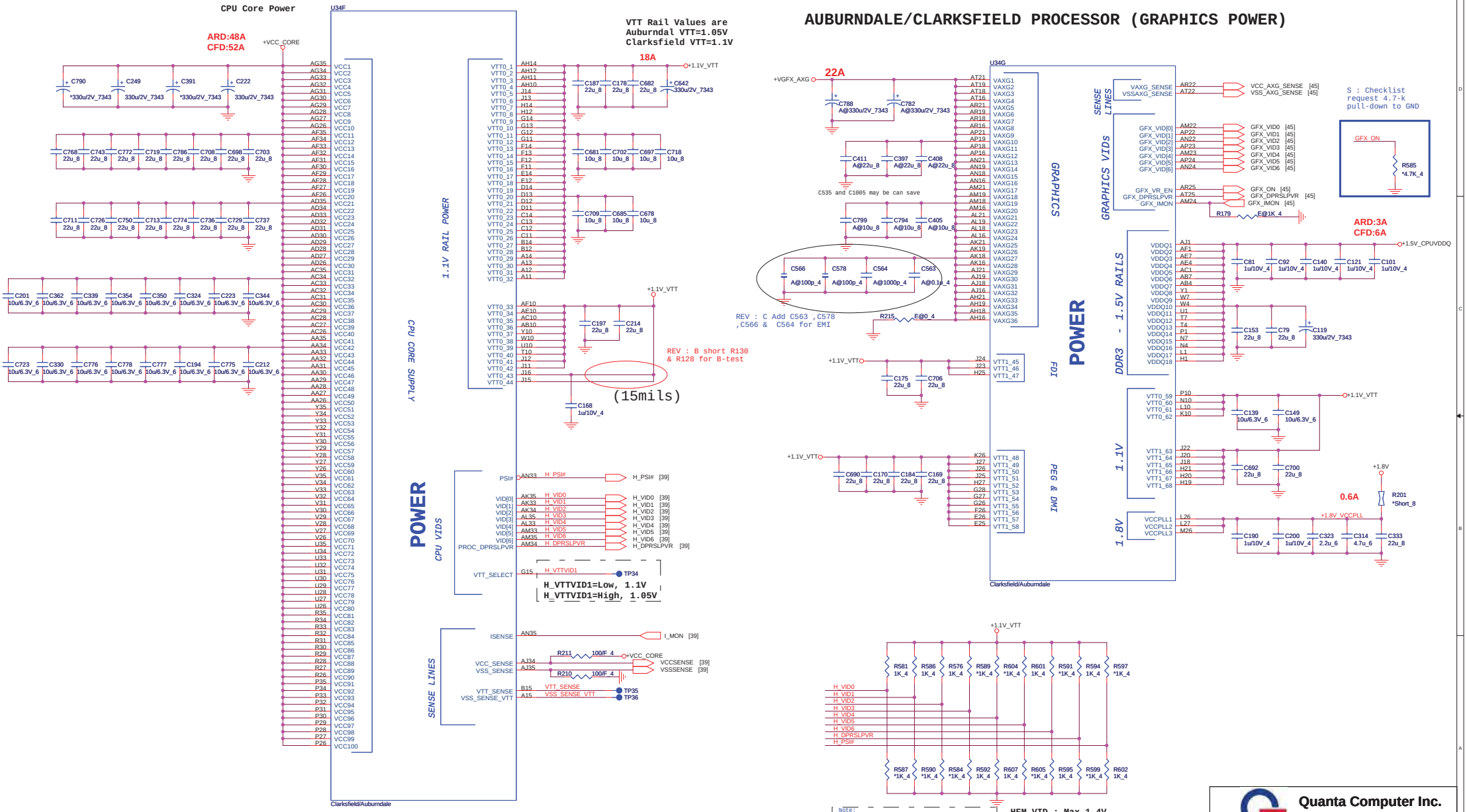
Size	Document Number	Rev
	AUBURNDA 1/4	1A

Date: Wednesday, January 20, 2010 Sheet 4 of 50

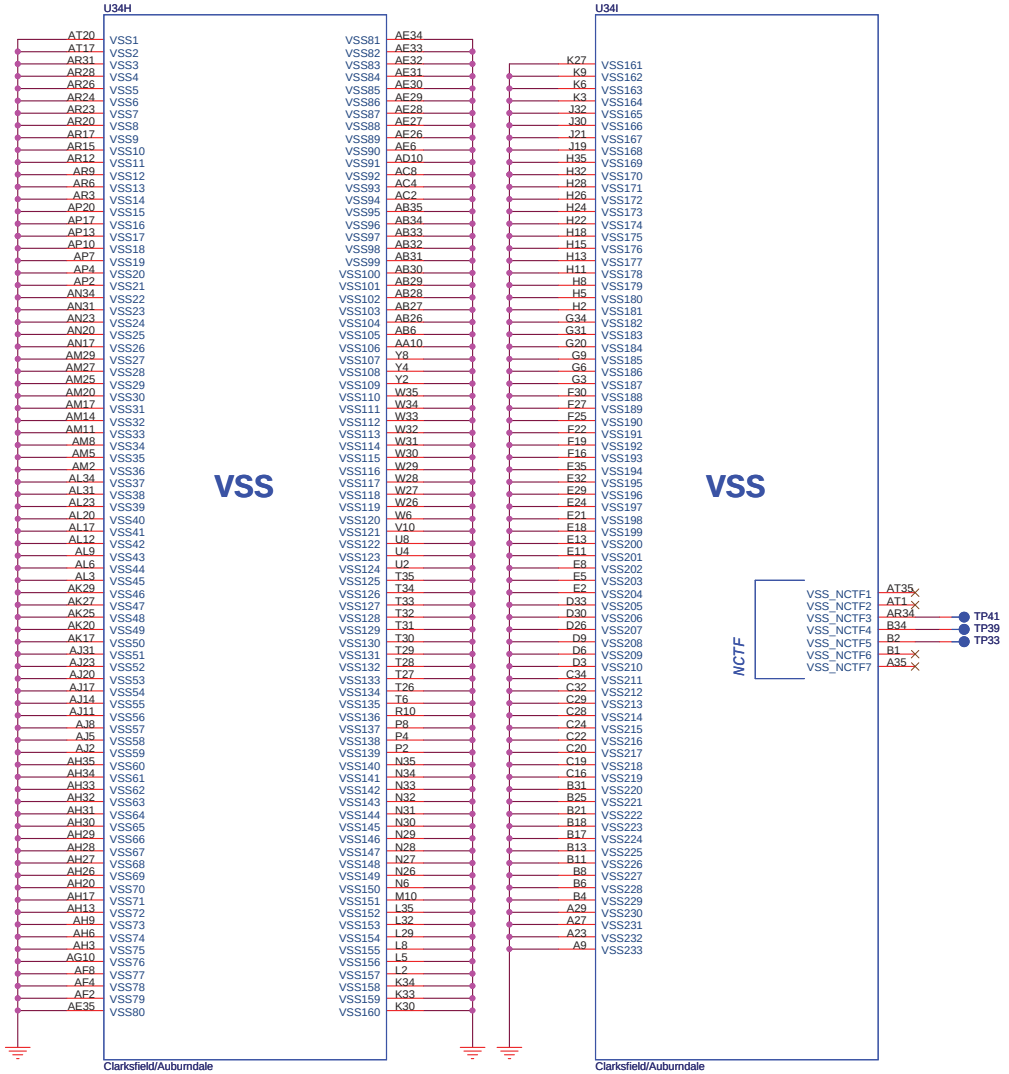
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



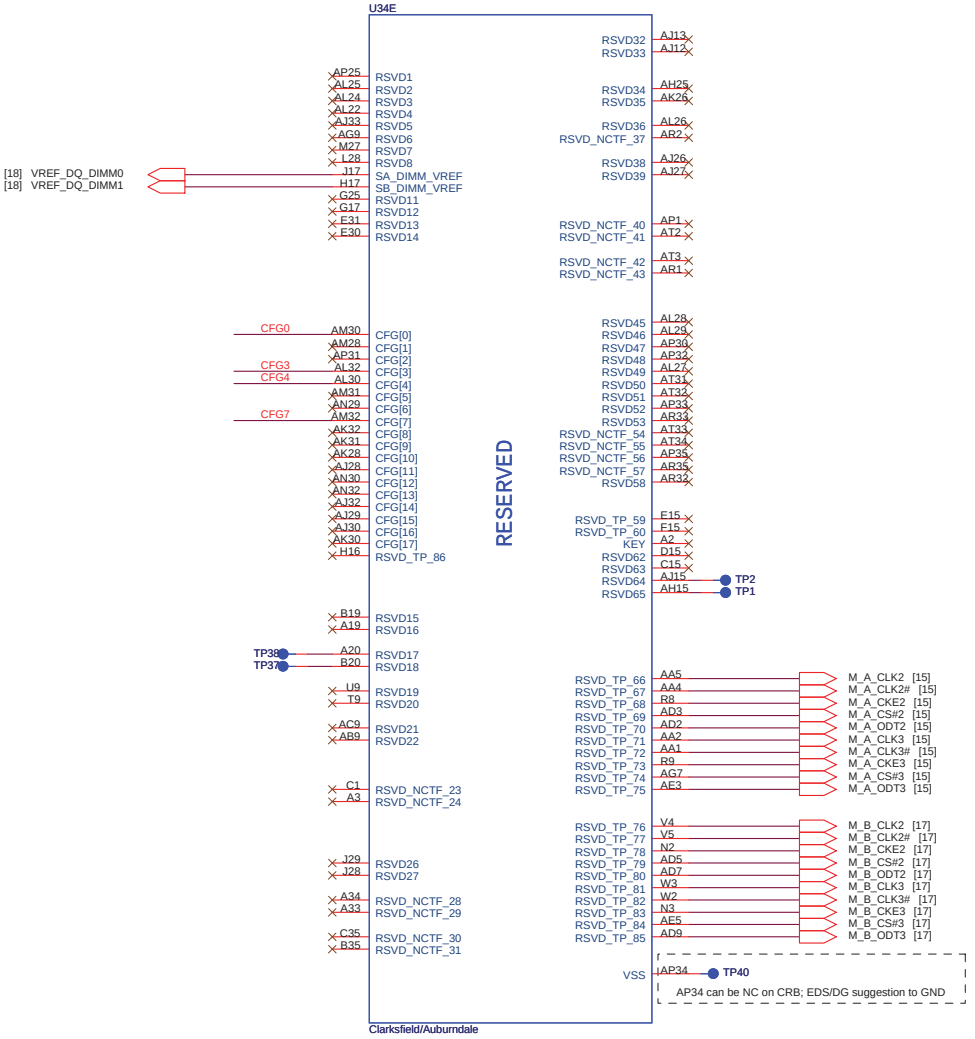
Quanta Computer Inc.			
PROJECT : ZYA			
Size	Document Number		Rev
	AUBURNDA 2/4		1A
Date:	Wednesday, January 20, 2010	Sheet 5 of 50	


CPU Core Power
ARD:48A
CFD:52A
+VCC_CORE
U34F
C790 *330u/2V_7343
C249 330u/2V_7343
C391 *330u/2V_7343
C222 330u/2V_7343
C768 C743 C772 C719 C786 C708 C698 C703 22u_8
C711 C726 C750 C713 C774 C736 C729 C737 22u_8
C201 C362 C339 C354 C350 C324 C223 C344 10u/6.3V_6
C723 C330 C776 C778 C777 C194 C775 C212 10u/6.3V_6
AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AE35 AE34 AE33 AE32 AE31 AE30 AE29 AE28 AE27 AE26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26
VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100
Clarksfield/Auburndale
1.1V RAIL POWER
CPU CORE SUPPLY
VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V
18A
+1.1V_VTT
C187 C178 C682 22u_8
C642 330u/2V_7343
C681 C702 C697 C718 10u_8
C709 C685 C678 10u_8
C197 C214 22u_8
REV : B short R130
& R128 for B-test
(15mils)
C168 1u/10V_4
POWER
CPU VIDS
PSI# H_PSI# H_PSI# [39]
VID[0] H_VID0 H_VID0 [39]
VID[1] H_VID1 H_VID1 [39]
VID[2] H_VID2 H_VID2 [39]
VID[3] H_VID3 H_VID3 [39]
VID[4] H_VID4 H_VID4 [39]
VID[5] H_VID5 H_VID5 [39]
VID[6] H_VID6 H_VID6 [39]
PROC_DPRSLPVR H_DPRSLPVR H_DPRSLPVR [39]
VTT_SELECT G15 H_VTTVID1 TP34
H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V
SENSE LINES
ISENSE AN35 I_MON [39]
VCC_SENSE AJ34 R211 100/F_4 +VCC_CORE VCCSENSE [39]
VSS_SENSE AJ35 R210 100/F_4 VSSSENSE [39]
VTT_SENSE B15 VTT_SENSE TP35
VSS_SENSE_VTT A15 VSS_SENSE_VTT TP36
AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)
AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)
22A
+VGFX_AXG
C788 A@330u/2V_7343
C782 A@330u/2V_7343
C411 A@22u_8
C397 A@22u_8
C408 A@22u_8
C535 and C1005 may be can save
C799 A@10u_8
C794 A@10u_8
C405 A@10u_8
C566 A@100p_4
C578 A@100p_4
C564 A@1000p_4
C563 A@0.1u_4
REV : C Add C563 ,C578
,C566 & C564 for EMI
R215 E@0_4
U34G
AT21 AT19 AT18 AR21 AR19 AR18 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ18 AJ16 AH21 AH19 AH18 AH16
VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36
GRAPHICS POWER
+1.1V_VTT
C175 22u_8
C706 22u_8
J24 J23 H25
VTT1_45 VTT1_46 VTT1_47
FDI
+1.1V_VTT
C690 C170 C184 C169 22u_8
K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25
VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58
PEG & DMI
SENSE LINES
VAXG_SENSE AR22 VCC_AXG_SENSE [45]
VSSAXG_SENSE AT22 VSS_AXG_SENSE [45]
GRAPHICS VIDs
GFX_VID[0] AM22 GFX_VID0 [45]
GFX_VID[1] AP22 GFX_VID1 [45]
GFX_VID[2] AN22 GFX_VID2 [45]
GFX_VID[3] AP23 GFX_VID3 [45]
GFX_VID[4] AM23 GFX_VID4 [45]
GFX_VID[5] AP24 GFX_VID5 [45]
GFX_VID[6] AN24 GFX_VID6 [45]
GFX_VR_EN AR25 GFX_ON [45]
GFX_DPRSLPVR AT25 GFX_DPRSLPVR [45]
GFX_IMON AM24 GFX_IMON [45]
R179 E@1K_4
S : Checklist
request 4.7-k
pull-down to GND
GFX_ON
R585 *4.7K_4
ARD:3A
CFD:6A
DDR3 - 1.5V RAILS
VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18
AJ1 AF1 AE7 AE4 AC1 AB7 AB4 Y1 W7 W4 U1 T7 T4 P1 N7 N4 L1 H1
+1.5V_CPUVDDQ
C81 C92 C140 C121 C101 1u/10V_4
C153 C79 22u_8
C119 330u/2V_7343
1.1V
VTT0_59 VTT0_60 VTT0_61 VTT0_62
P10 N10 L10 K10
+1.1V_VTT
C139 10u/6.3V_6
C149 10u/6.3V_6
VTT1_63 VTT1_64 VTT1_65 VTT1_66 VTT1_67 VTT1_68
J22 J20 J18 H21 H20 H19
C692 C700 22u_8
+1.8V
0.6A
R201 *Short_8
1.8V
VCCPLL1 VCCPLL2 VCCPLL3
L26 L27 M26
+1.8V_VCCPLL
C190 1u/10V_4
C200 1u/10V_4
C323 2.2u_6
C314 4.7u_6
C333 22u_8
Clarksfield/Auburndale
+1.1V_VTT
R581 R586 R576 R589 R604 R601 R591 R594 R597 1K_4 *1K_4
H_VID0 H_VID1 H_VID2 H_VID3 H_VID4 H_VID5 H_VID6 H_DPRSLPVR H_PSI#
R587 R590 R584 R592 R607 R605 R595 R599 R602 *1K_4 1K_4
Note:
For Validating IMVP VR R6451 should be STUFF
and R2N1 NO_STUFF
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
Quanta Computer Inc.
PROJECT : ZYA
Size
Document Number
AUBURNDA 3/4 (PWR)
Rev 1A
Date: Wednesday, January 20, 2010
Sheet 6 of 50

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

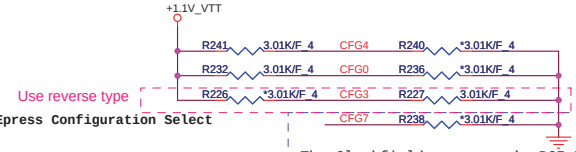


AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



S: The CFG signals have a default value of '1' if not terminated on the board.

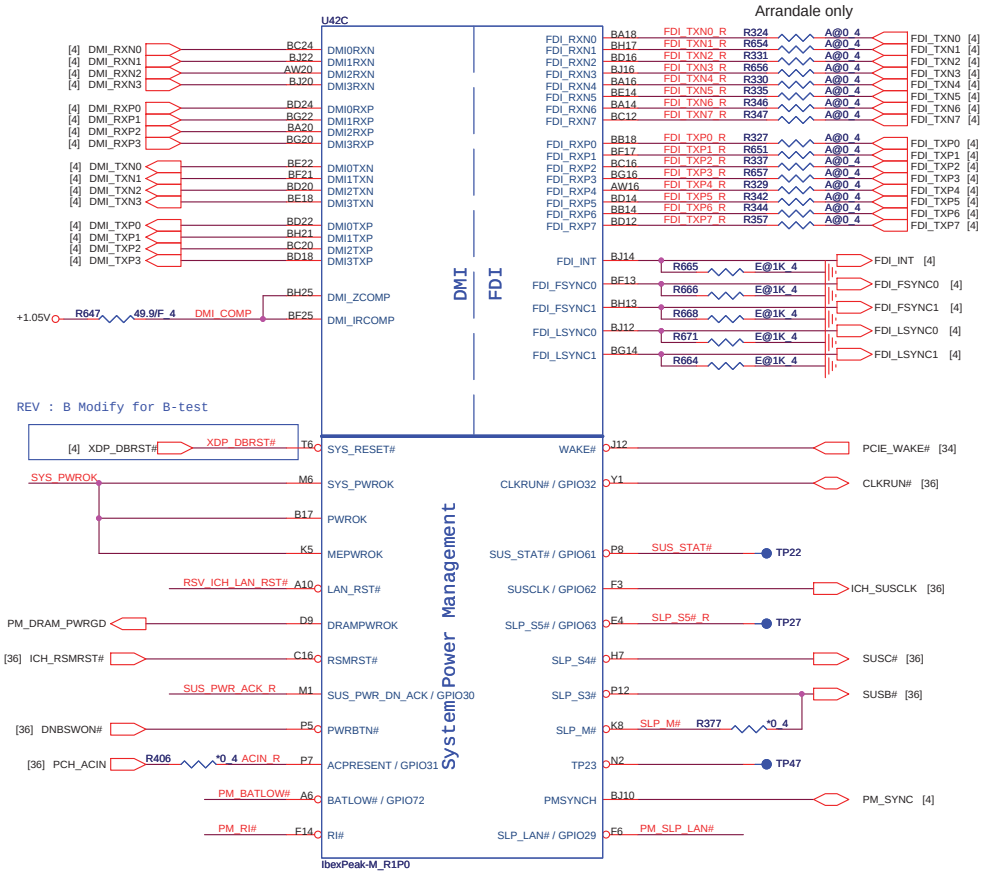
CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

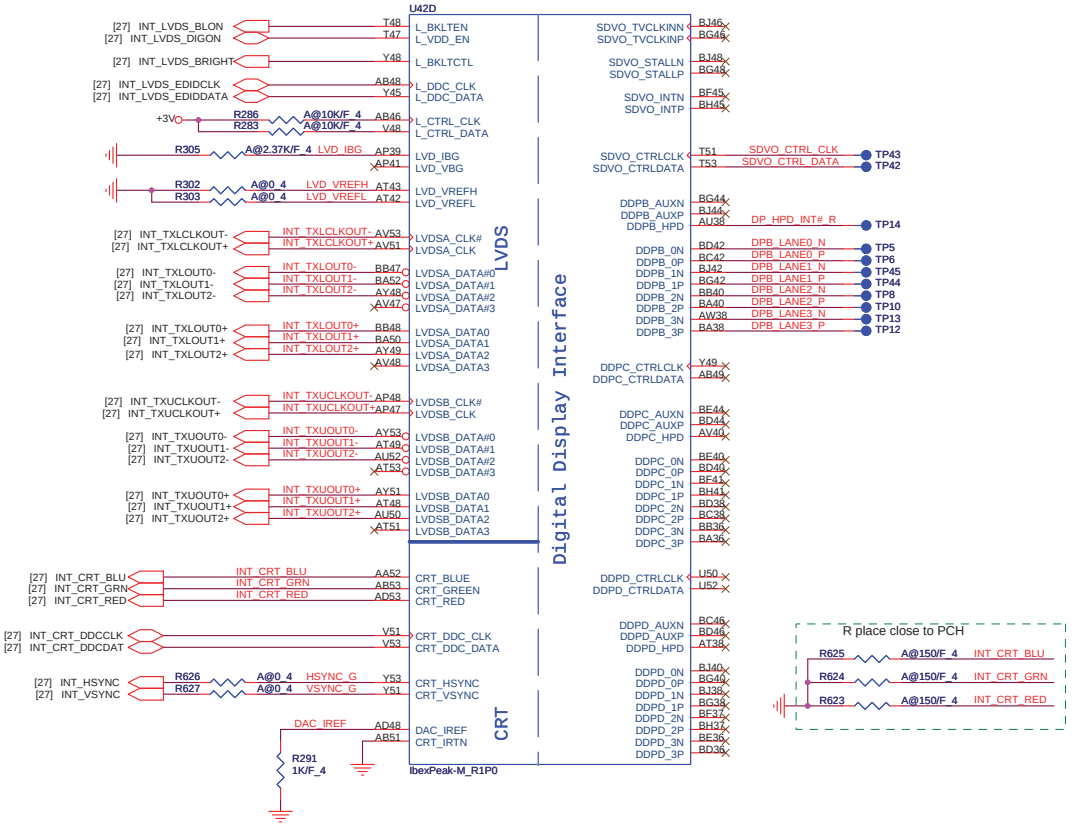
Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	AUBURNDA 4/4	1A
Date: Wednesday, January 20, 2010	Sheet 7 of 50	

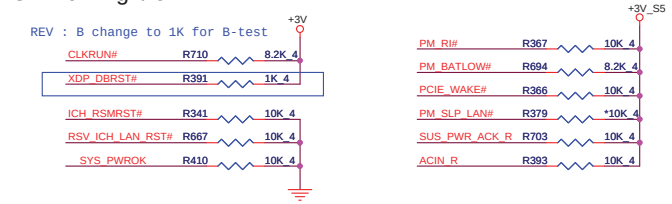
IBEX PEAK-M (DMI,FDI,GPIO)



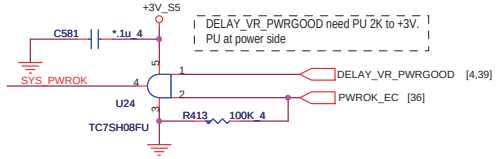
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low

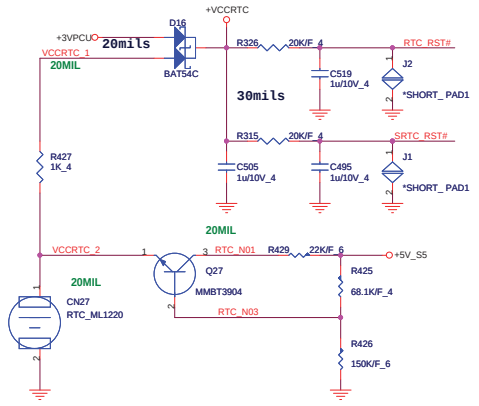


System PWR_OK

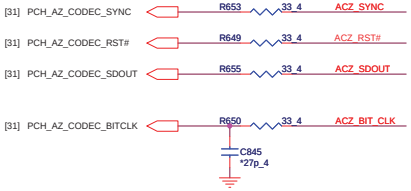


Quanta Computer Inc.		
PROJECT : ZYA		
Size	Document Number: IBEX PEAK-M 1/6	Rev: 1A
Date: Wednesday, January 20, 2010	Sheet 8 of 50	

RTC Circuitry

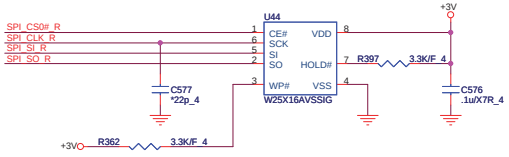


HDA Bus



Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

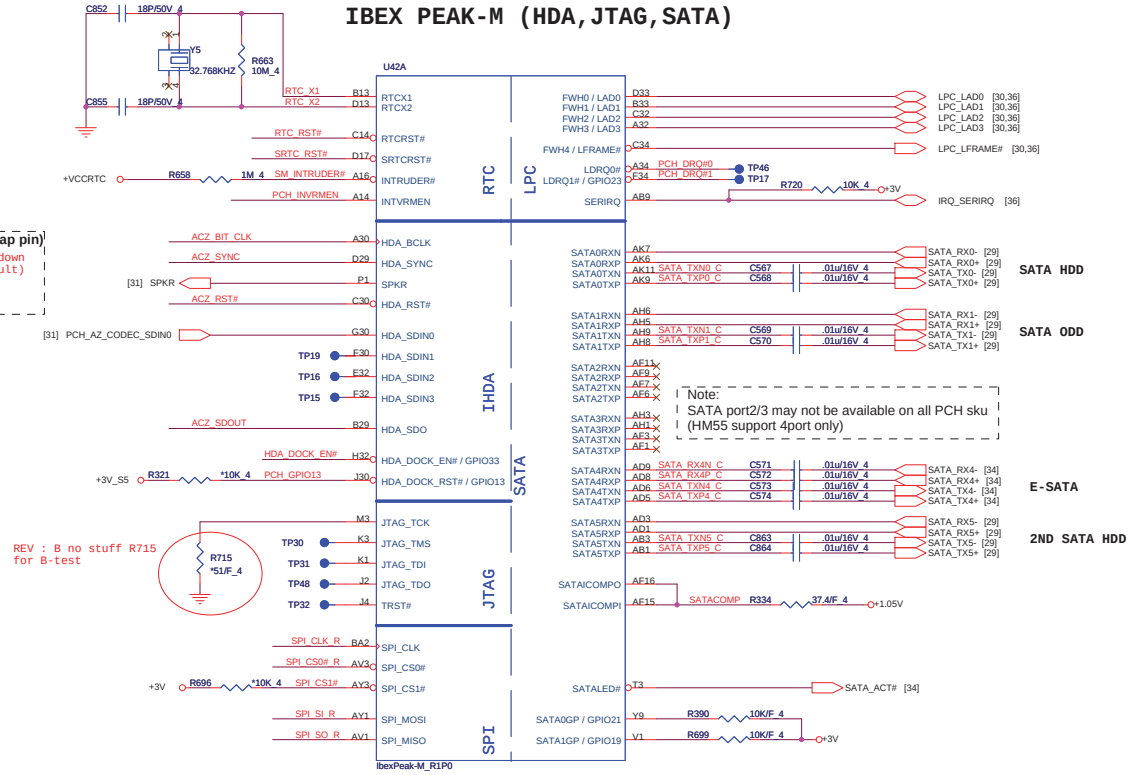
PCH SPI



At 11/24 add

Winbond W25X16AVSSIG		AKE38ZP0N01
EON	EN25F16-100HIP	AKE38ZA0Q00
AMIC	A25L016	AKE38ZN0800

IBEX PEAK-M (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZY9B note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R725 *10K_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R274 *10K_4 PCI_GNT3# [10]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+VCCRTC R660 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] +3V R288 *1K_4, R290 *1K_4 R287 1K_4, R301 1K_4 PCI_GNT0# [10] PCI_GNT1# [10]
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R695 *1K_4 NV_ALE NV_ALE [10]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R692 *1K_4 NV_CLE NV_CLE [10]
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V R311 *1K_4, R309 *10K_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R398 *1K_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R382 10K_4 RSV_GPIO8 [11]
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 R392 1K_4 CR_WAKE# [11]

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

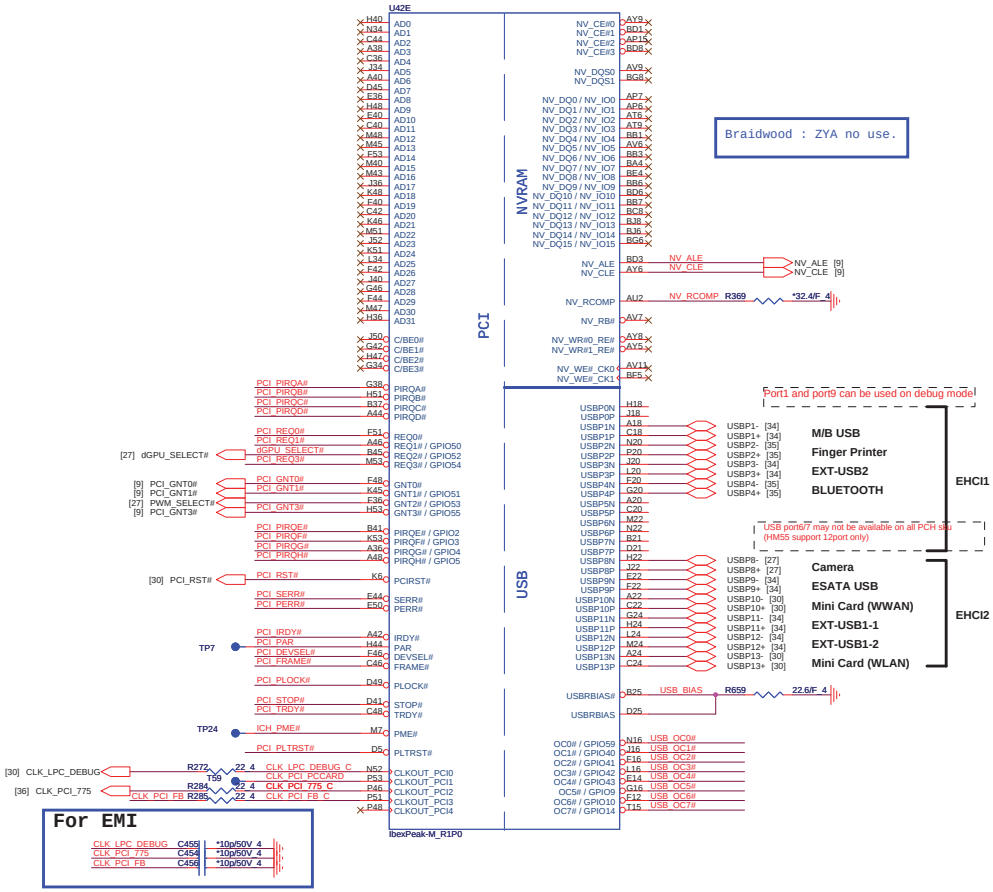
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Quanta Computer Inc.
PROJECT : ZYA

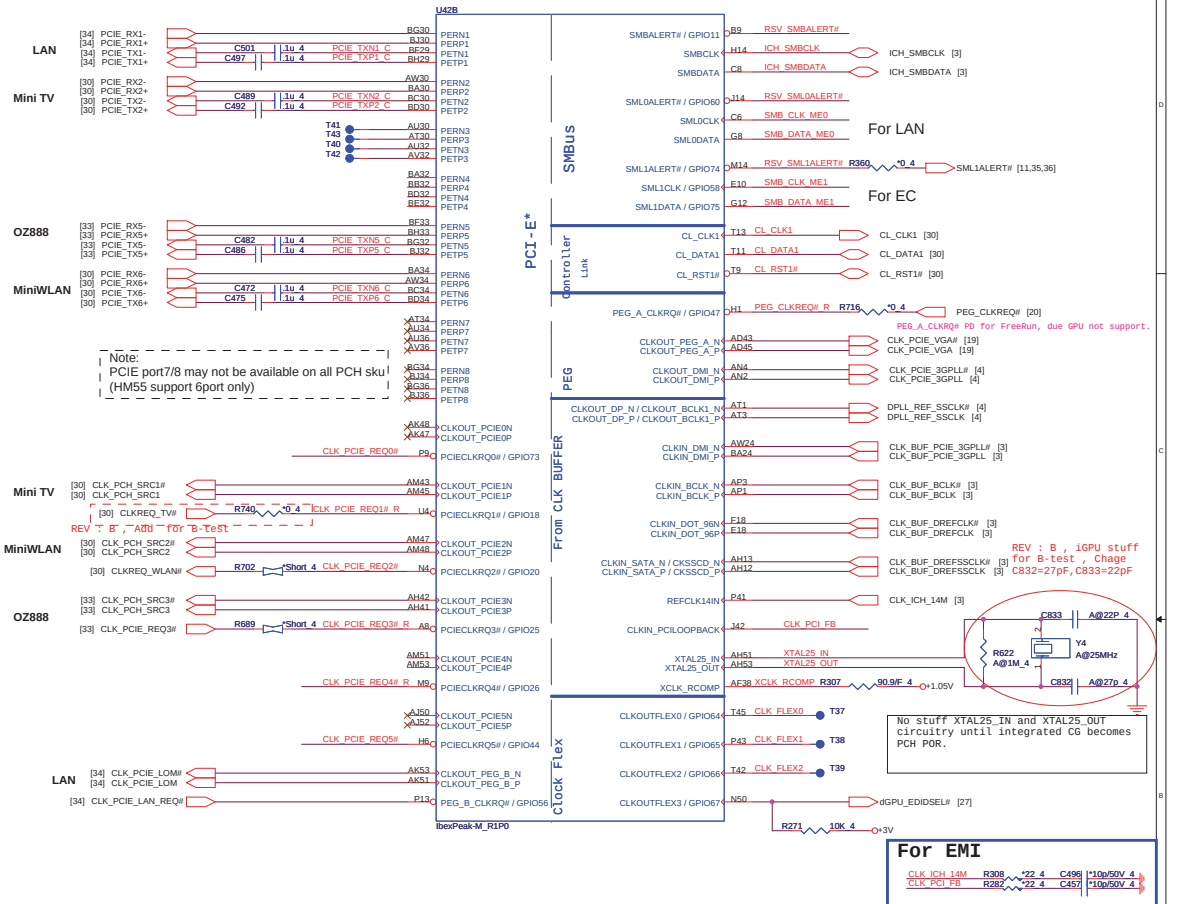
Size	Document Number	Rev
	IBEX PEAK-M 2/6	1A

Date: Wednesday, January 20, 2010 Sheet 9 of 50

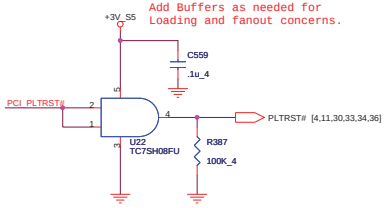
IBEX PEAK-M (PCI,USB,NVRAM)



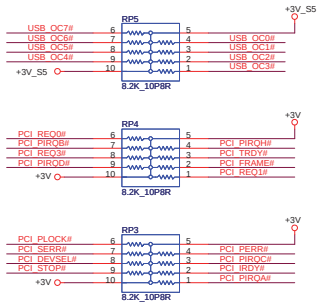
IBEX PEAK-M (PCI-E,SMBUS,CLK)



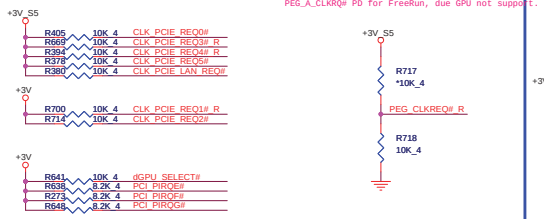
PLTRST#



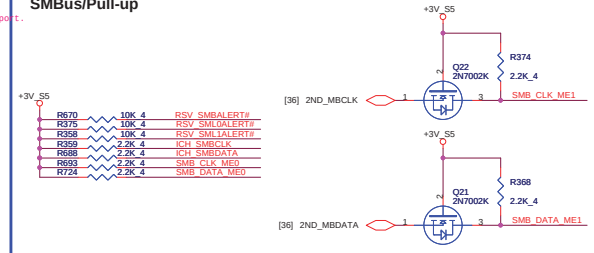
PCI/USBOC# Pull-up



CLK_REQ/Strap Pin



SMBus/Pull-up

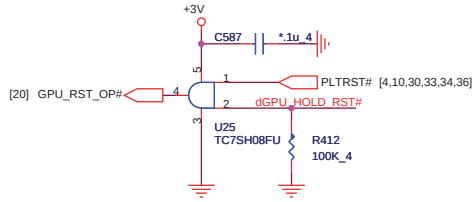


Quanta Computer Inc.			
PROJECT : ZYA			
Size	Document Number		Rev
	IBEX PEAK-M 3/6		1A
Date: Wednesday, January 20, 2010		Sheet 10 of 50	

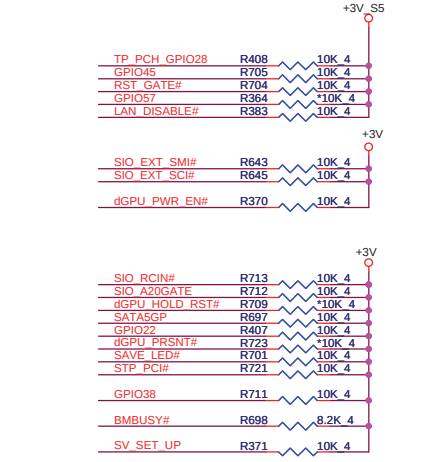
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

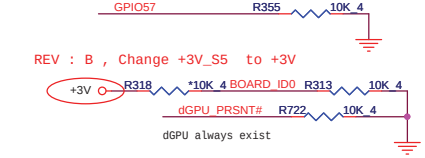
GPU RST#



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)



Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

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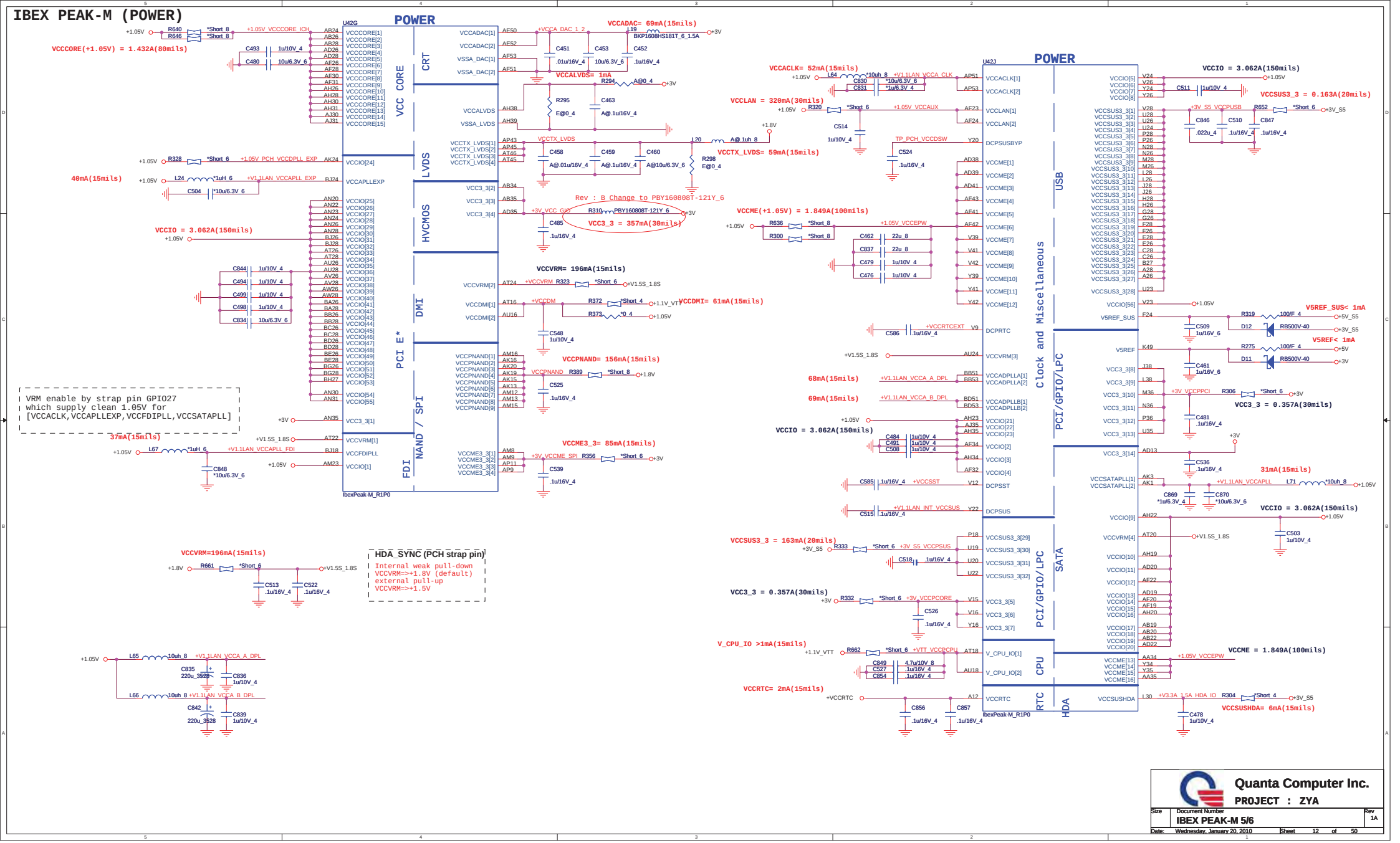
PROJECT : ZYA

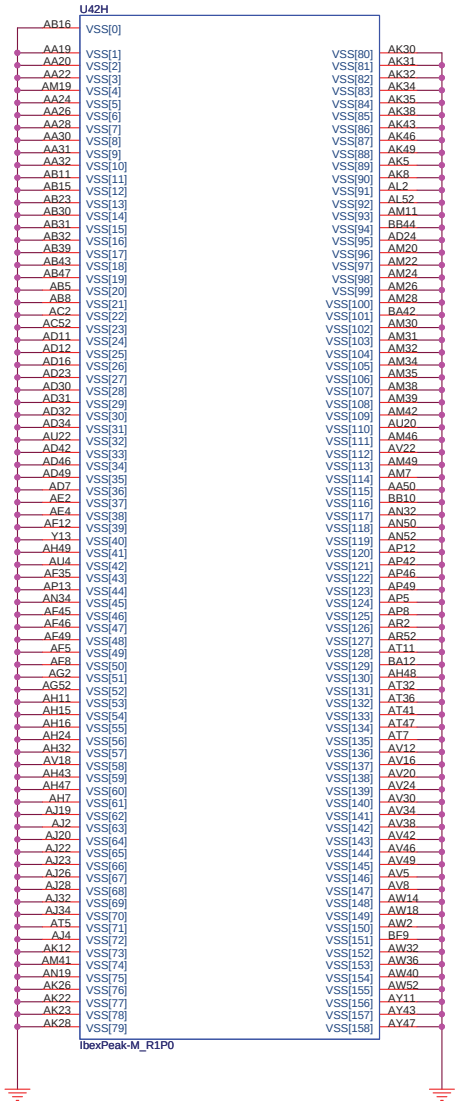
Size	Document Number	Rev
	IBEX PEAK-M 4/6	1A

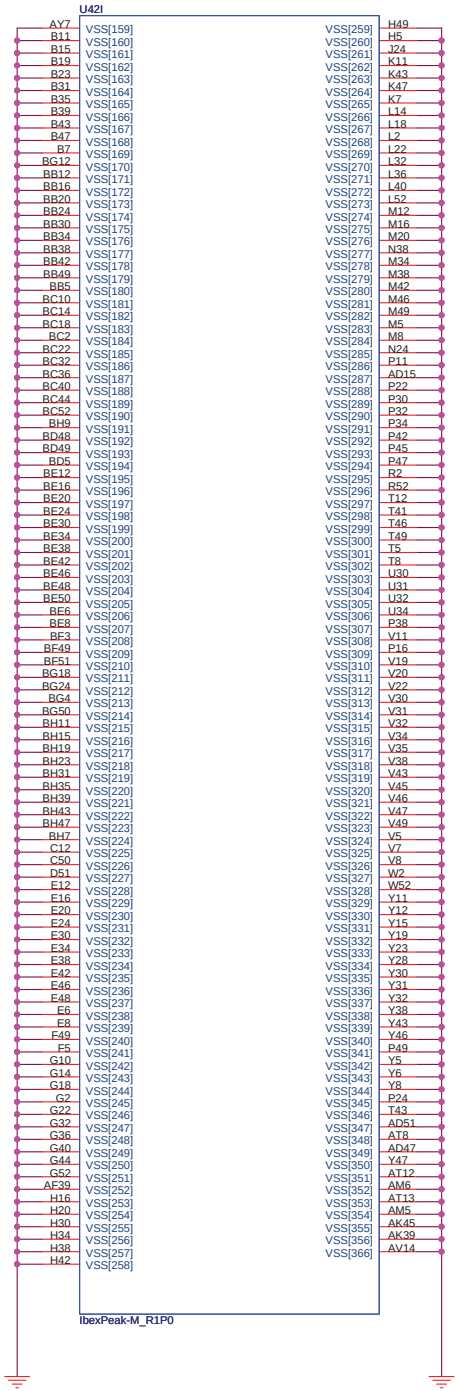
Date: Wednesday, January 20, 2010 Sheet 11 of 50

IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)





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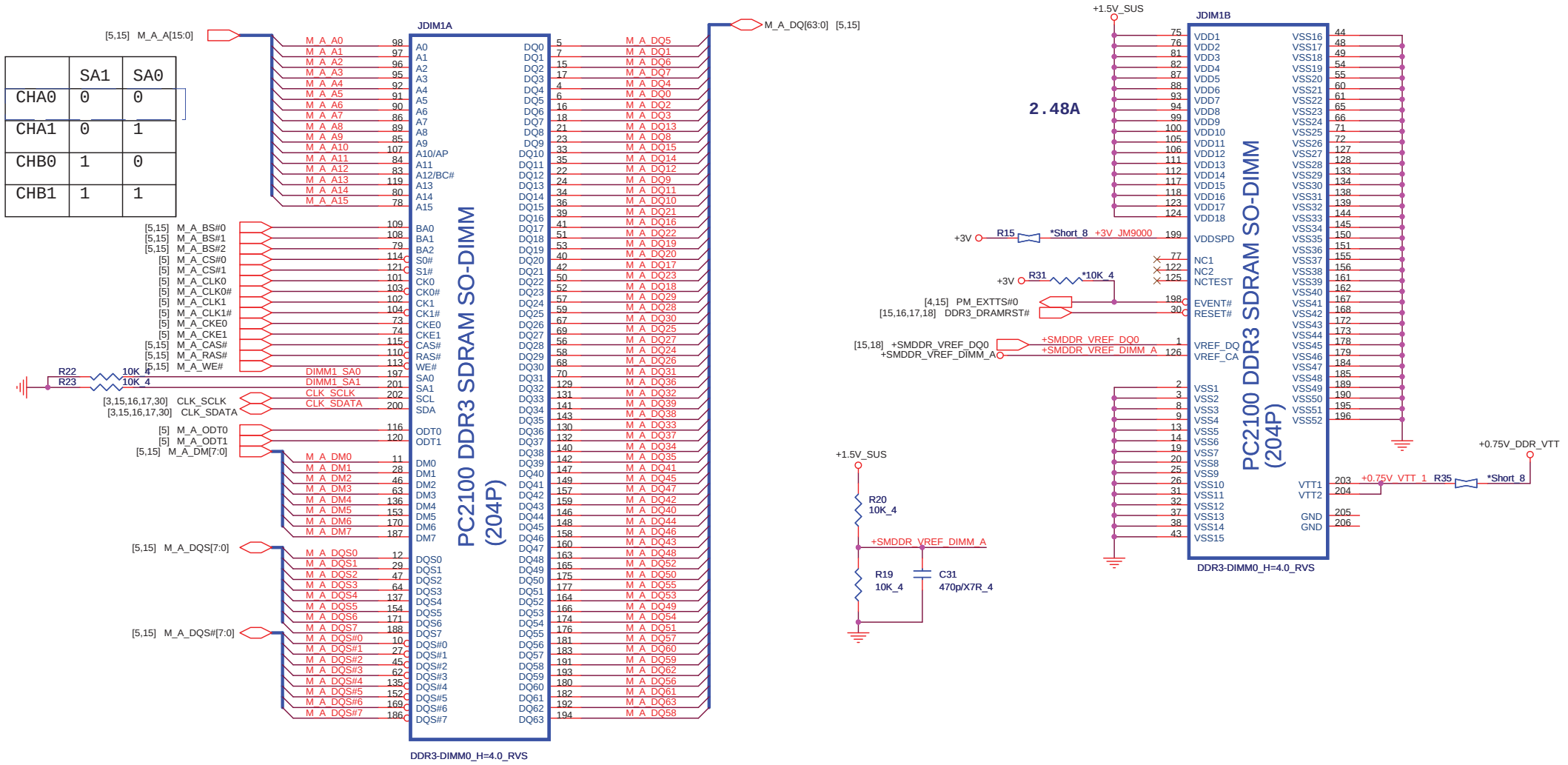
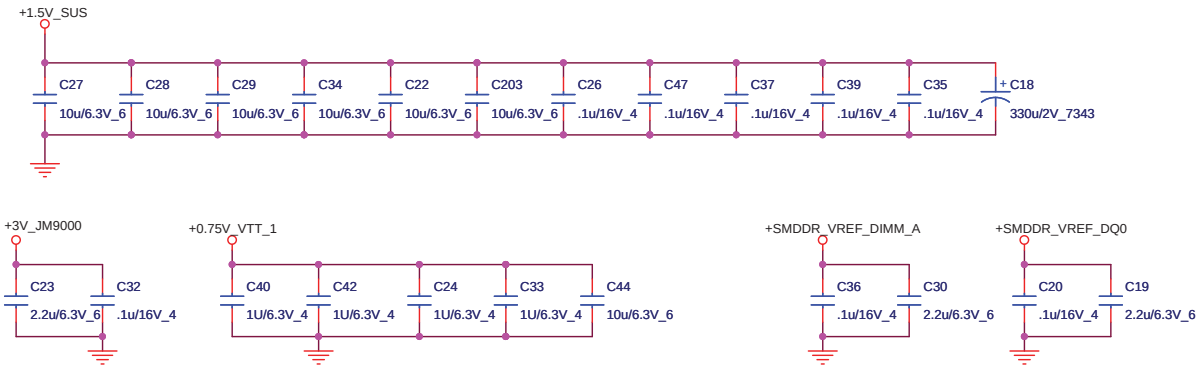
PROJECT : ZYA

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A

Date: Wednesday, January 20, 2010 Sheet 13 of 50



Place these Caps near So-Dimm0.



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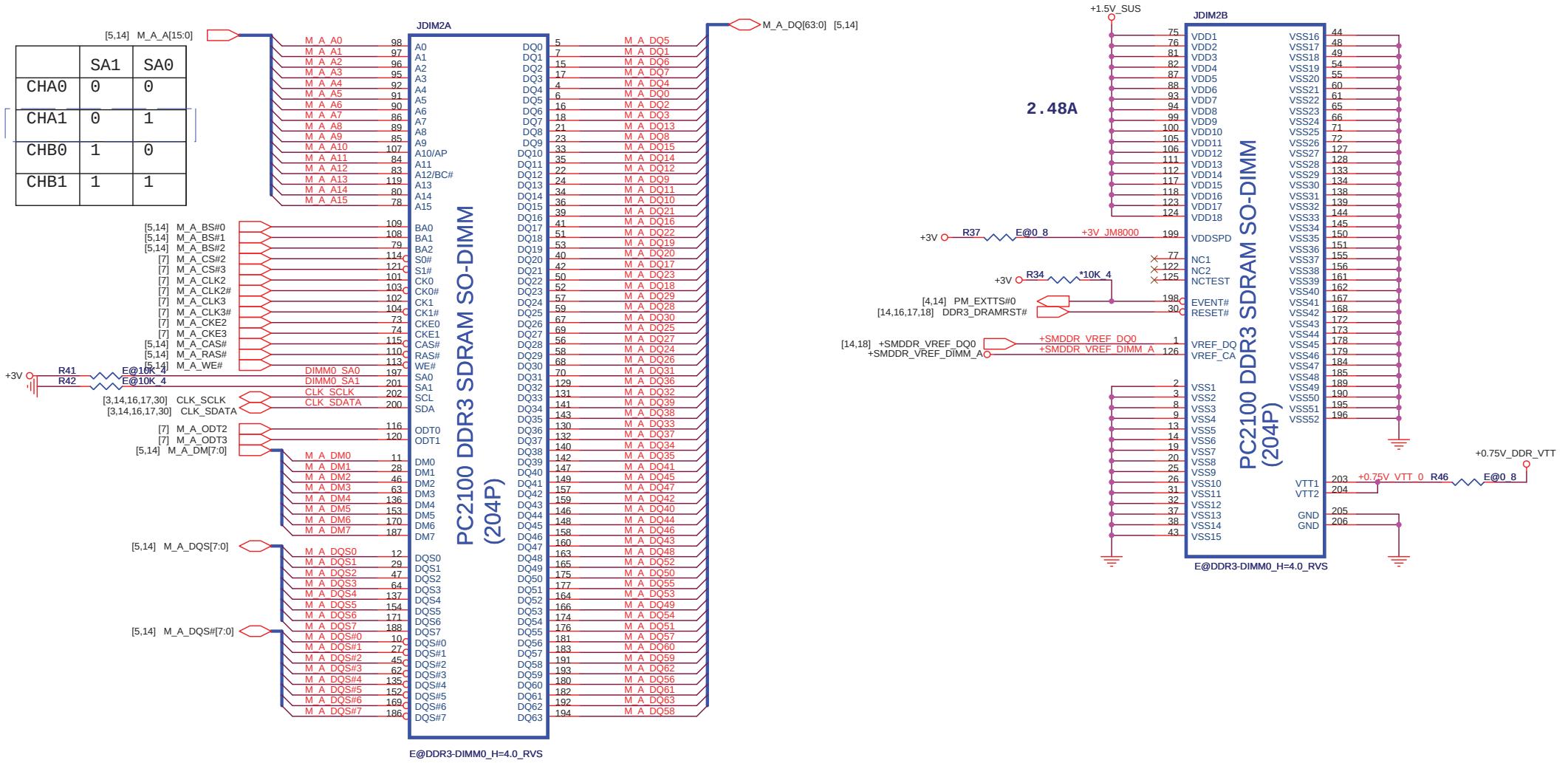
PROJECT : ZYA

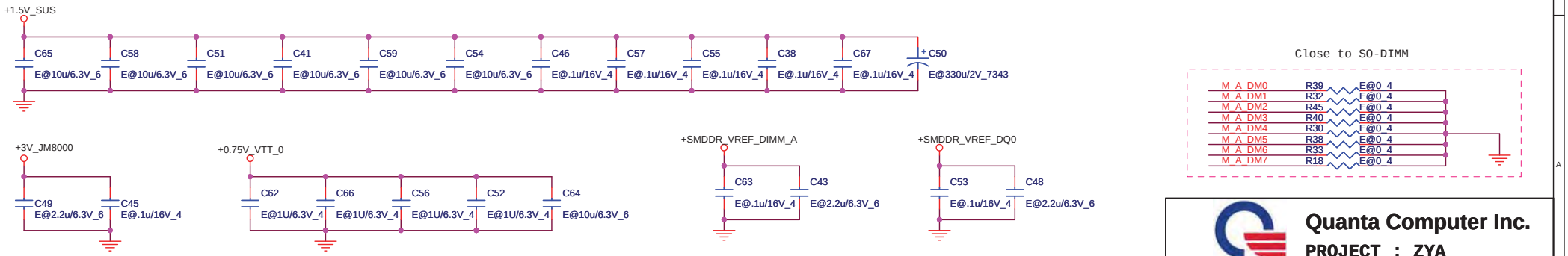
Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A

Date: Wednesday, January 20, 2010 Sheet 14 of 50



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

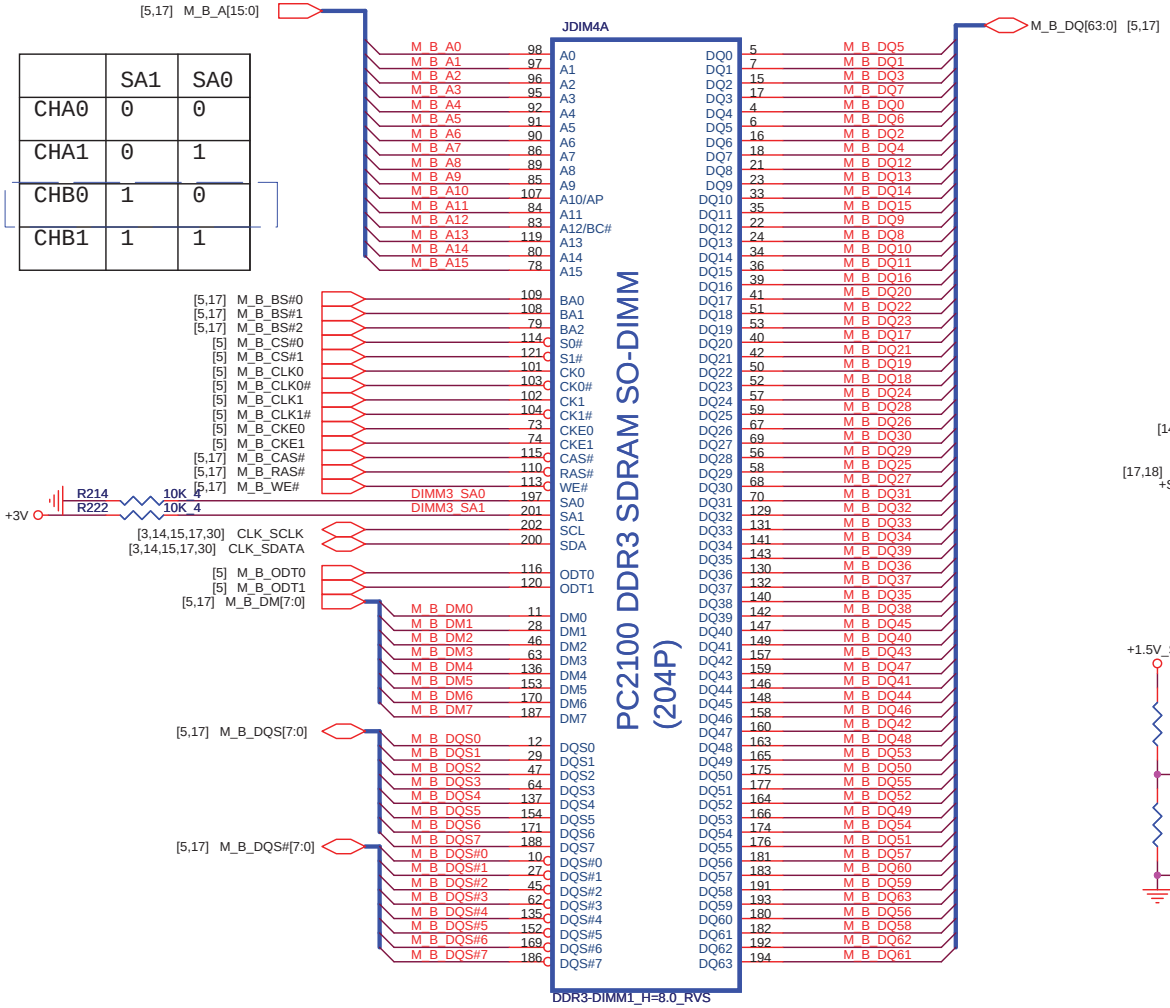
Place these Caps near So-Dimm0.

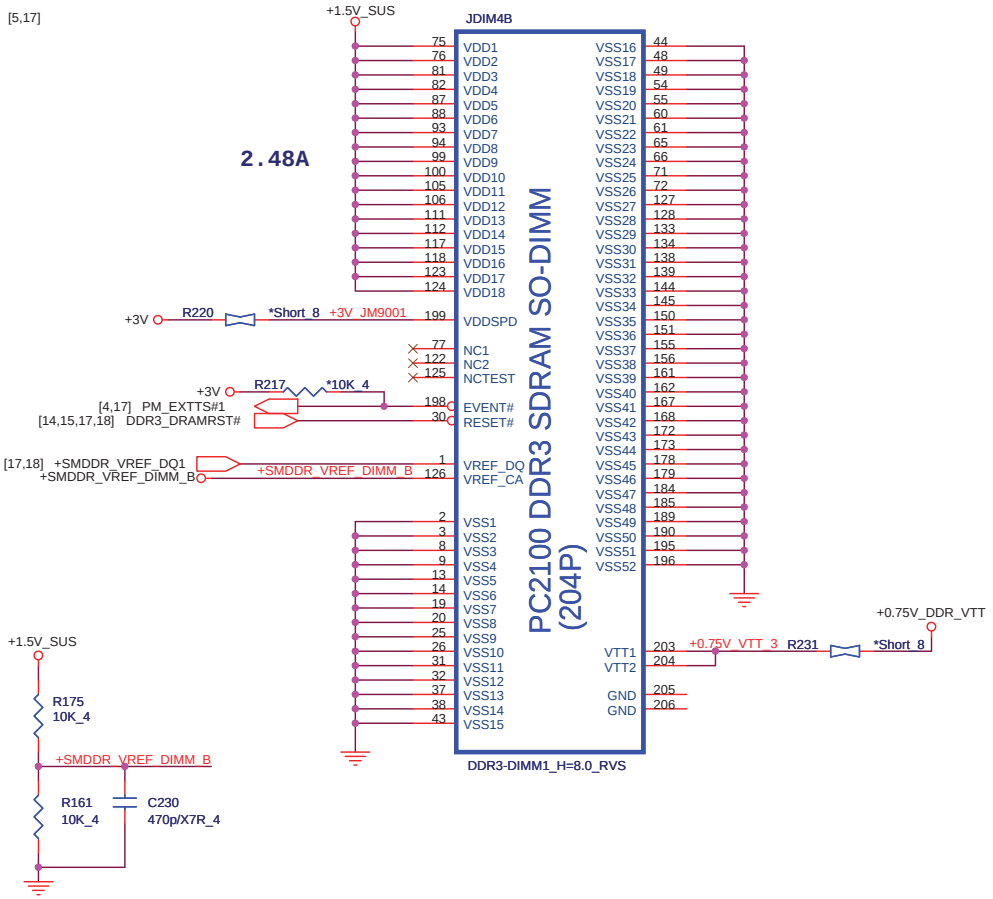


Quanta Computer Inc.
PROJECT : ZYA

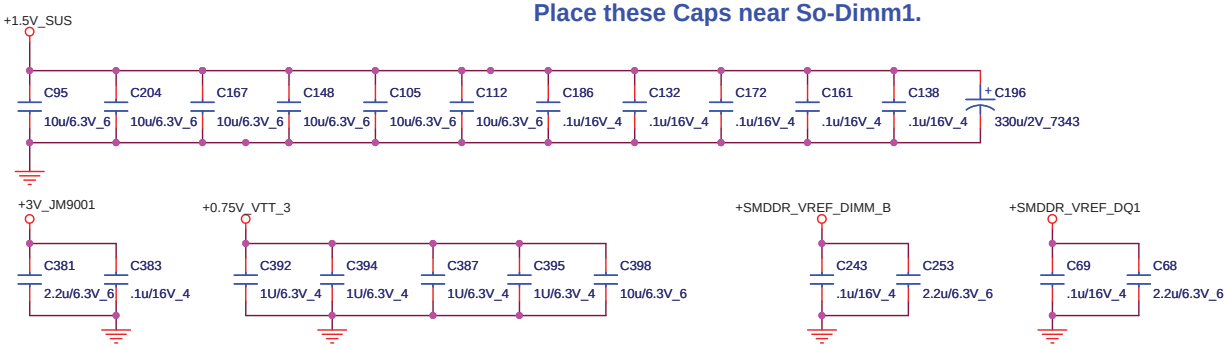
Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
Date: Wednesday, January 20, 2010	Sheet 15 of 50	

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1





Place these Caps near So-Dimm1.

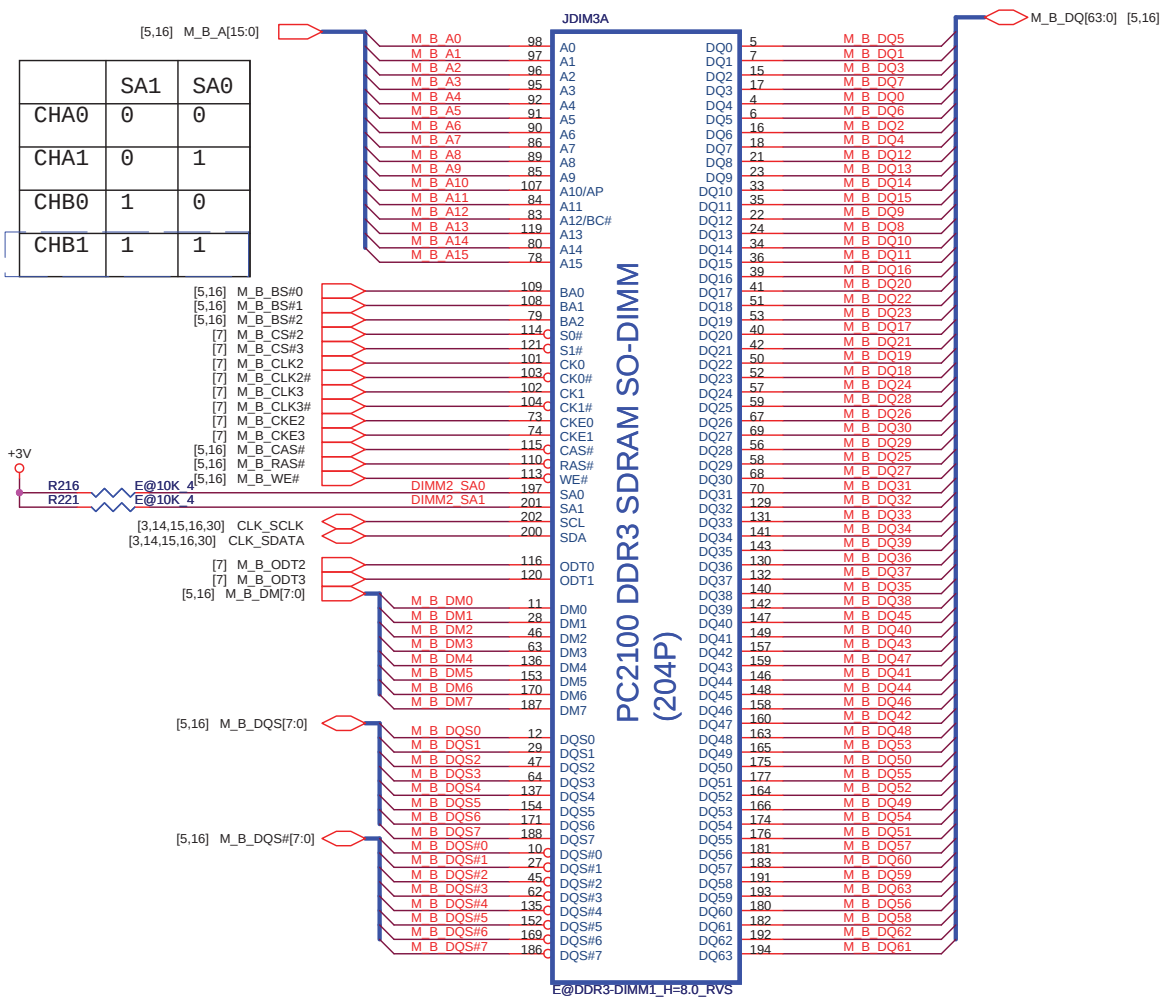


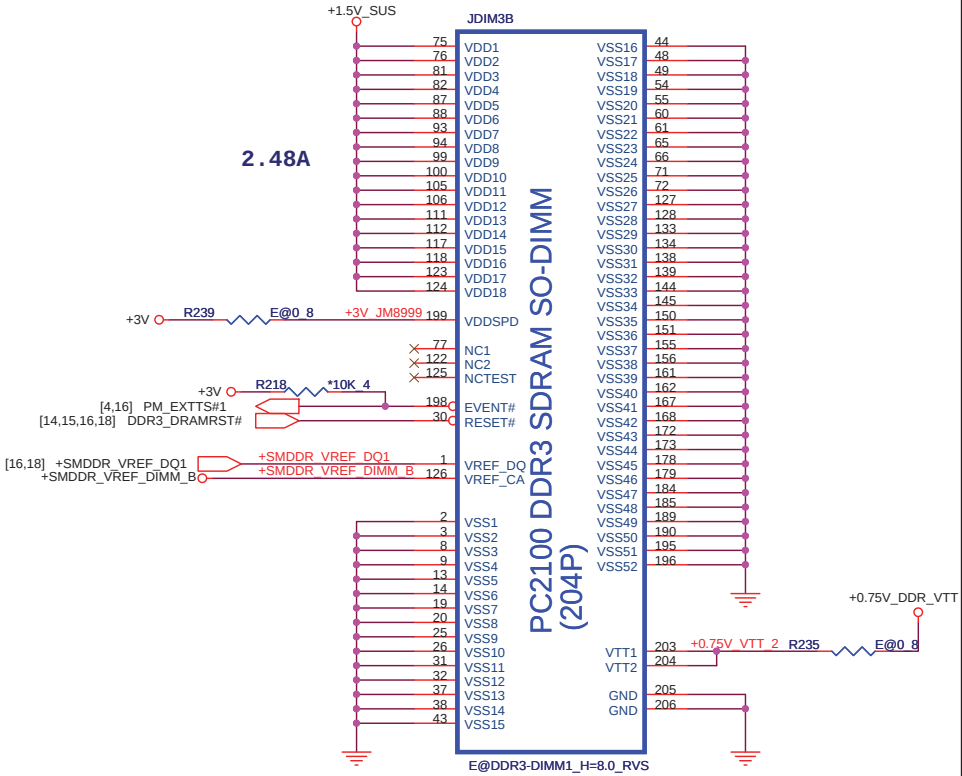
Quanta Computer Inc.

PROJECT : ZYA

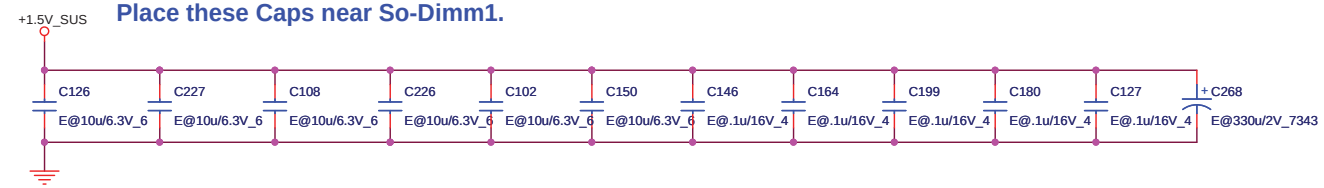
Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date: Wednesday, January 20, 2010	Sheet 16 of 50	

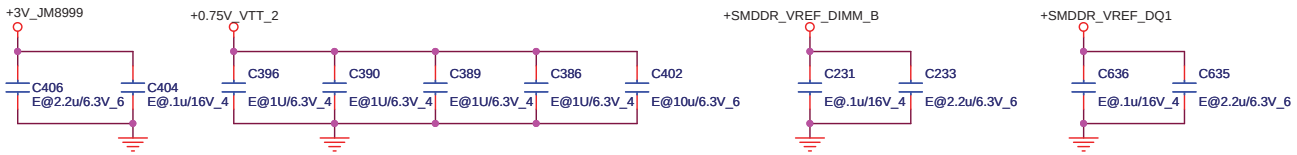
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1





Place these Caps near So-Dimm1.





Close to SO-DIMM

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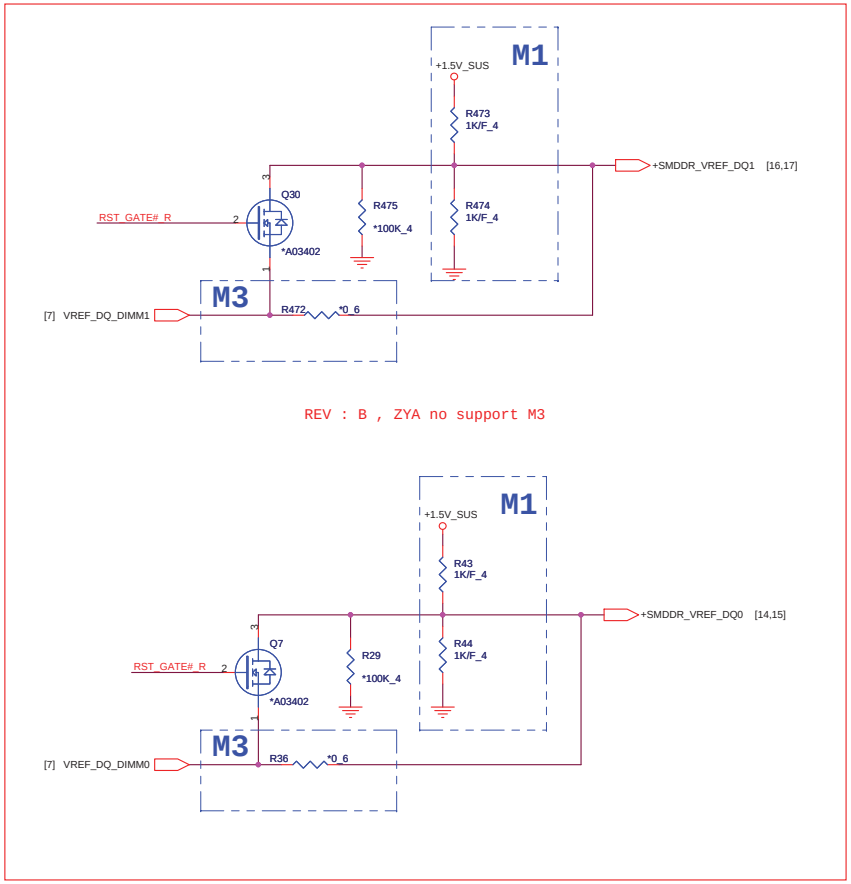
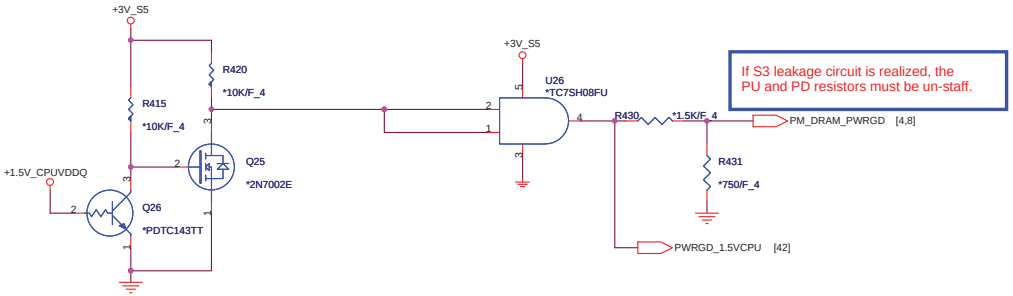
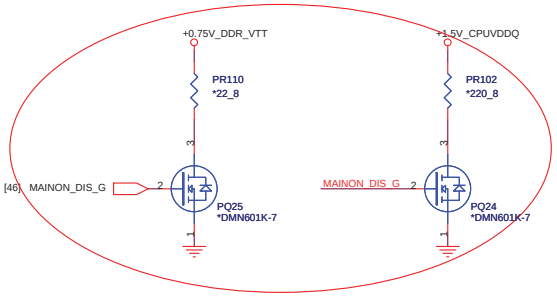
PROJECT : ZYA

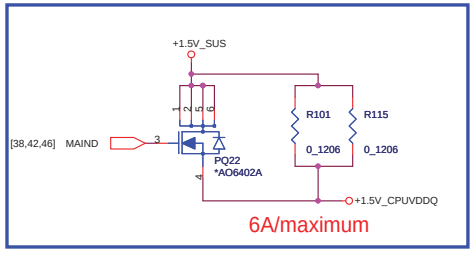
Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date: Wednesday, January 20, 2010	Sheet 17 of 50	

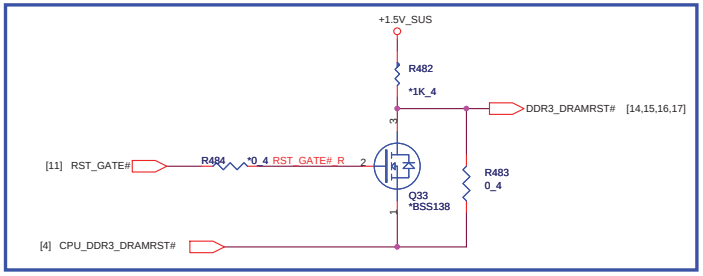




REV : B , No stuff for B-test







Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	XDP	1A

Date: Wednesday, January 20, 2010 Sheet 18 of 50

[4] PEG_TXP[0..15] PEG_TXP[0..15]
[4] PEG_TXN[0..15] PEG_TXN[0..15]
[4] PEG_RXP[0..15] PEG_RXP[0..15]
[4] PEG_RXN[0..15] PEG_RXN[0..15]

U35A

0518 SWAP PCIE for VGA side

[4] PEG_TXP15 / [4] PEG_TXN15	PEG_TXP15 / PEG_TXN15	AA38 / Y37	PCIE_RX0P / PCIE_RX0N
[4] PEG_TXP14 / [4] PEG_TXN14	PEG_TXP14 / PEG_TXN14	Y35 / W36	PCIE_RX1P / PCIE_RX1N
[4] PEG_TXP13 / [4] PEG_TXN13	PEG_TXP13 / PEG_TXN13	W38 / V37	PCIE_RX2P / PCIE_RX2N
[4] PEG_TXP12 / [4] PEG_TXN12	PEG_TXP12 / PEG_TXN12	V35 / U36	PCIE_RX3P / PCIE_RX3N
[4] PEG_TXP11 / [4] PEG_TXN11	PEG_TXP11 / PEG_TXN11	U38 / T37	PCIE_RX4P / PCIE_RX4N
[4] PEG_TXP10 / [4] PEG_TXN10	PEG_TXP10 / PEG_TXN10	T35 / R36	PCIE_RX5P / PCIE_RX5N
[4] PEG_TXP9 / [4] PEG_TXN9	PEG_TXP9 / PEG_TXN9	R38 / P37	PCIE_RX6P / PCIE_RX6N
[4] PEG_TXP8 / [4] PEG_TXN8	PEG_TXP8 / PEG_TXN8	P35 / N36	PCIE_RX7P / PCIE_RX7N
[4] PEG_TXP7 / [4] PEG_TXN7	PEG_TXP7 / PEG_TXN7	N38 / M37	PCIE_RX8P / PCIE_RX8N
[4] PEG_TXP6 / [4] PEG_TXN6	PEG_TXP6 / PEG_TXN6	M35 / L36	PCIE_RX9P / PCIE_RX9N
[4] PEG_TXP5 / [4] PEG_TXN5	PEG_TXP5 / PEG_TXN5	L38 / K37	PCIE_RX10P / PCIE_RX10N
[4] PEG_TXP4 / [4] PEG_TXN4	PEG_TXP4 / PEG_TXN4	K35 / J36	PCIE_RX11P / PCIE_RX11N
[4] PEG_TXP3 / [4] PEG_TXN3	PEG_TXP3 / PEG_TXN3	J38 / H37	PCIE_RX12P / PCIE_RX12N
[4] PEG_TXP2 / [4] PEG_TXN2	PEG_TXP2 / PEG_TXN2	H35 / G36	PCIE_RX13P / PCIE_RX13N
[4] PEG_TXP1 / [4] PEG_TXN1	PEG_TXP1 / PEG_TXN1	G38 / F37	PCIE_RX14P / PCIE_RX14N
[4] PEG_TXP0 / [4] PEG_TXN0	PEG_TXP0 / PEG_TXN0	F35 / E37	PCIE_RX15P / PCIE_RX15N

PCI EXPRESS INTERFACE

0518 SWAP PCIE for VGA side

PCIE_TX0P / PCIE_TX0N	Y33 / Y32	CPEG_RXP15 / CPEG_RXN15	C242 / C232	.1u/10V_4 / .1u/10V_4	PEG_RXP15 [4] / PEG_RXN15 [4]
PCIE_TX1P / PCIE_TX1N	W33 / W32	CPEG_RXP14 / CPEG_RXN14	C251 / C244	.1u/10V_4 / .1u/10V_4	PEG_RXP14 [4] / PEG_RXN14 [4]
PCIE_TX2P / PCIE_TX2N	U33 / U32	CPEG_RXP13 / CPEG_RXN13	C260 / C254	.1u/10V_4 / .1u/10V_4	PEG_RXP13 [4] / PEG_RXN13 [4]
PCIE_TX3P / PCIE_TX3N	U30 / U29	CPEG_RXP12 / CPEG_RXN12	C266 / C274	.1u/10V_4 / .1u/10V_4	PEG_RXP12 [4] / PEG_RXN12 [4]
PCIE_TX4P / PCIE_TX4N	T33 / T32	CPEG_RXP11 / CPEG_RXN11	C284 / C279	.1u/10V_4 / .1u/10V_4	PEG_RXP11 [4] / PEG_RXN11 [4]
PCIE_TX5P / PCIE_TX5N	T30 / T29	CPEG_RXP10 / CPEG_RXN10	C286 / C295	.1u/10V_4 / .1u/10V_4	PEG_RXP10 [4] / PEG_RXN10 [4]
PCIE_TX6P / PCIE_TX6N	P33 / P32	CPEG_RXP9 / CPEG_RXN9	C296 / C305	.1u/10V_4 / .1u/10V_4	PEG_RXP9 [4] / PEG_RXN9 [4]
PCIE_TX7P / PCIE_TX7N	P30 / P29	CPEG_RXP8 / CPEG_RXN8	C310 / C321	.1u/10V_4 / .1u/10V_4	PEG_RXP8 [4] / PEG_RXN8 [4]
PCIE_TX8P / PCIE_TX8N	N33 / N32	CPEG_RXP7 / CPEG_RXN7	C322 / C331	.1u/10V_4 / .1u/10V_4	PEG_RXP7 [4] / PEG_RXN7 [4]
PCIE_TX9P / PCIE_TX9N	N30 / N29	CPEG_RXP6 / CPEG_RXN6	C336 / C341	.1u/10V_4 / .1u/10V_4	PEG_RXP6 [4] / PEG_RXN6 [4]
PCIE_TX10P / PCIE_TX10N	L33 / L32	CPEG_RXP5 / CPEG_RXN5	C343 / C349	.1u/10V_4 / .1u/10V_4	PEG_RXP5 [4] / PEG_RXN5 [4]
PCIE_TX11P / PCIE_TX11N	L30 / L29	CPEG_RXP4 / CPEG_RXN4	C353 / C359	.1u/10V_4 / .1u/10V_4	PEG_RXP4 [4] / PEG_RXN4 [4]
PCIE_TX12P / PCIE_TX12N	K33 / K32	CPEG_RXP3 / CPEG_RXN3	C360 / C368	.1u/10V_4 / .1u/10V_4	PEG_RXP3 [4] / PEG_RXN3 [4]
PCIE_TX13P / PCIE_TX13N	J33 / J32	CPEG_RXP2 / CPEG_RXN2	C370 / C373	.1u/10V_4 / .1u/10V_4	PEG_RXP2 [4] / PEG_RXN2 [4]
PCIE_TX14P / PCIE_TX14N	K30 / K29	CPEG_RXP1 / CPEG_RXN1	C379 / C384	.1u/10V_4 / .1u/10V_4	PEG_RXP1 [4] / PEG_RXN1 [4]
PCIE_TX15P / PCIE_TX15N	H33 / H32	CPEG_RXP0 / CPEG_RXN0	C374 / C377	.1u/10V_4 / .1u/10V_4	PEG_RXP0 [4] / PEG_RXN0 [4]

CLOCK

[10] CLK_PCIE_VGA → AB35 PCIE_REFCLKP
[10] CLK_PCIE_VGA# → AA36 PCIE_REFCLKN

For Broadway, Madison and Park
the PWRGOOD ball must be connecected to ground

R530 10K_4 → AJ21 NC#1, AK21 NC#2, AH16 PWRGOOD

[20] GPU_RST# → AA30 PERSTB

CALIBRATION

PCIE_CALRP Y30 — R171 1.27K/F_4 — +1V
PCIE_CALRN Y29 — R178 2K/F_4 — +1V

SP@Madison/Broadway_M2

For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

+1.0V

Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	Madison/Broadway-PCIE I/F	1A
Date: Wednesday, January 20, 2010	Sheet 19 of 50	

GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK

1.8V GPIO

3.3V GPIO

For EMI

U35B

MUTI GFX

DVPCNTL_MVP_0 AR8
DVPCNTL_MVP_1 AU8
DVPCNTL_0 AP8
DVPCNTL_1 AW8
DVPCNTL_2 AR3
DVPCLK AR1
DVPDATA_0 AU1
DVPDATA_1 AU3
DVPDATA_2 AW3
DVPDATA_3 AP6
DVPDATA_4 AW5
DVPDATA_5 AU5
DVPDATA_6 AR6
DVPDATA_7 AW6
DVPDATA_8 AU6
DVPDATA_9 AT7
DVPDATA_10 AV7
DVPDATA_11 AN7
DVPDATA_12 AV9
DVPDATA_13 AT9
DVPDATA_14 AR10
DVPDATA_15 AW10
DVPDATA_16 AU10
DVPDATA_17 AP10
DVPDATA_18 AV11
DVPDATA_19 AT11
DVPDATA_20 AR12
DVPDATA_21 AW12
DVPDATA_22 AU12
DVPDATA_23 AP12

[24] RAM_STRAP0
[24] RAM_STRAP1
[24] RAM_STRAP2
T44

DPA
TXCAP_DPA3P AU24
TXCAM_DPA3N AV23
TX0P_DPA2P AT25
TX0M_DPA2N AR24
TX1P_DPA1P AU26
TX1M_DPA1N AV25
TX2P_DPA0P AT27
TX2M_DPA0N AR26

EXT_HDMICLK+ [28]
EXT_HDMICLK- [28]
EXT_HDMITX0P [28]
EXT_HDMITX0N [28]
EXT_HDMITX1P [28]
EXT_HDMITX1N [28]
EXT_HDMITX2P [28]
EXT_HDMITX2N [28]

DPB
TXCBP_DPB3P AR39
TXCBM_DPB3N AT39
TX3P_DPB2P AV31
TX3M_DPB2N AU30
TX4P_DPB1P AR32
TX4M_DPB1N AT31
TX5P_DPB0P AT33
TX5M_DPB0N AU32

DPC
TXCCP_DPC3P AU14
TXCCM_DPC3N AV13
TX0P_DPC2P AT15
TX0M_DPC2N AR14
TX1P_DPC1P AU16
TX1M_DPC1N AV15
TX2P_DPC0P AT17
TX2M_DPC0N AR16

T50 T47 T51 T52 T53 T45 T49 T46

DPD
TXCDP_DPD3P AU29
TXCDM_DPD3N AT19
TX3P_DPD2P AT21
TX3M_DPD2N AR29
TX4P_DPD1P AU22
TX4M_DPD1N AV21
TX5P_DPD0P AT23
TX5M_DPD0N AR22

I2C
SCL AK26
SDA AJ26
[24] GPU_GPIO0
[24] GPU_GPIO1
[24] GPU_GPIO2
[24] GPIO3_SMBDAT
[24] GPIO4_SMBCLK
[43] PWR_PSI#
[44] IO_VID0
[27] EV_LVDS_BLON
[24] SOUT_GPIO8
[24] SIN_GPIO9
[24] SCLK_GPIO10
[24] GPU_GPIO11
[24] GPU_GPIO12
[24] GPU_GPIO13
[43] GPU_VID2
[43] GPU_VID1
[24] ALT#_GPIO17
[43] GPU_VID3
[24] SCS#_GPIO22
[3] 27M_CLK
[10] PEG_CLKREQ#
[28] EXT_HDMI_HPD

GENERAL PURPOSE I/O
GPIO_0 AH20
GPIO_1 AH18
GPIO_2 AN16
GPIO_3_SMBDATA AH23
GPIO_4_SMBCLK AJ23
GPIO_5_AC_BATT AH17
GPIO_6 AJ17
GPIO_7_BLON AK17
GPIO_8_ROMSO AJ13
GPIO_9_ROMSI AH15
GPIO_10_ROMSCK AJ16
GPIO_11 AK16
GPIO_12 AL16
GPIO_13 AM16
GPIO_14_HPD2 AM14
GPIO_15_PWRCNTL_0 AM13
GPIO_16_SSIN AK14
GPIO_17_THERMAL_INT AG30
GPIO_18_HPD3 AN14
GPIO_19_CTF AM17
GPIO_20_PWRCNTL_1 AL13
GPIO_21_BB_EN AJ14
GPIO_22_ROMCSB AK13
GPIO_23_CLKREQB AN13
JTAG_TRSTB AM23
JTAG_TDI AN23
JTAG_TCK AK23
JTAG_TMS AL24
JTAG_TDO AM24
GENERICA AJ19
GENERICB AK19
GENERICC AJ20
GENERICD AK20
GENERICE_HPD4 AJ24
GENERICF AH26
GENERICG AH24
HPD1 AK24

T15 T48 T11 T10 T8

R152 B@10K/F_4 GPIO24_TRSTB
R147 *10K/F_4 27M_CLK
R125 B@10K/F_4

C193 *10p/50V_4 R154 *10K/F_4 27M_CLK

R496 *10K_4
R497 10K/F_4
R93 *10K/F_4
R103 *10K/F_4

R104 10K/F_4
R105 10K/F_4

R517 499/F_4
R529 249/F_4
C667 .1u_4
VREFG AH13
VREFG

PLL/CLOCK
DPLL_PVDD AM32
DPLL_PVSS AN32
DPLL_VDDC AN31
XTALIN AV33
XTALOUT AU34
DPLUS AF29
DMINUS AG29
THERMAL
TS_FDO AK32
TSVDD AJ32
TSVSS AJ33
T17 TS_VDD

Change C612/C613 from 18p to 27p at B-test
C670 27p/50V_4
Y3 27MHZ
R521 1M/F_4
C671 27p/50V_4

DAC1
R AD39
RB AD37
G AE36
GB AD35
B AE37
BB AE38
HSYNC AC36
VSYNC AC38
RSET AB34 R167 499/F_4
AVDD AD34
AVSSQ AE34
VDD1DI AC33
VSS1DI AC34

EXT_CRT_RED [27]
EXT_CRT_GRN [27]
EXT_CRT_BLU [27]
EXT_HSYNC [24,27]
EXT_VSYNC [24,27]
R540 150/F_4
R541 150/F_4
R542 150/F_4

DAC2
R2 AC39
R2B AC31
G2 AD39
G2B AD31
B2 AE39
B2B AE31
C AC32
Y AD32
COMP AE32
H2SYNC AD29
V2SYNC AC29
VDD2DI AG31
VSS2DI AG32
A2VDD AG33
A2VDDQ AD33
A2VSSQ AF33
R2SET AA29 R165 715/F_4

T19
V2SYNC [24]
+3V_D (3.3V@130mA A2VDD)
C209 .1u/10V_4

DDC/AUX
DDC1CLK AM26
DDC1DATA AN26
AUX1P AM27
AUX1N AL27
DDC2CLK AM19
DDC2DATA AL19
AUX2P AN20
AUX2N AM20
DDCCLK_AUX3P AL30
DDCDATA_AUX3N AM30
DDCCLK_AUX4P AL29
DDCDATA_AUX4N AM29
DDCCLK_AUX5P AN21
DDCDATA_AUX5N AM21
DDC6CLK AJ30
DDC6DATA AJ31
NC_DDCCLK_AUX7P AK30
NC_DDCDATA_AUX7N AK29

T16 T9 T7 T14

EV_HDMI_DDCCK [28]
EV_HDMI_DDCDAT [28]
EV_LVDS_DDCCLK [27]
EV_LVDS_DDCDAT [27]
EV_CRTDCLK [27]
EV_CRTDDAT [27]

HDMI
Display Port
LVDS
CRT

SP@Madison/Broadway_M2

U35G

LVDS CONTROL
VARY_BL AK27
DIGON AJ27
EV_LVDS_BRIGHT [27]
EV_LVDS_VDDEN [27]

TXCLK_UP_DPF3P AK35
TXCLK_UN_DPF3N AL36
EV_TXUCLKOUT+ [27]
EV_TXUCLKOUT- [27]
TXOUT_U0P_DPF2P AJ38
TXOUT_U0N_DPF2N AK37
EV_TXUOUT0+ [27]
EV_TXUOUT0- [27]
TXOUT_U1P_DPF1P AH35
TXOUT_U1N_DPF1N AJ36
EV_TXUOUT1+ [27]
EV_TXUOUT1- [27]
TXOUT_U2P_DPF0P AG38
TXOUT_U2N_DPF0N AH37
EV_TXUOUT2+ [27]
EV_TXUOUT2- [27]
TXOUT_U3P AF35
TXOUT_U3N AG36

LVTMDP
TXCLK_LP_DPE3P AP34
TXCLK_LN_DPE3N AR34
EV_TXLCLKOUT+ [27]
EV_TXLCLKOUT- [27]
TXOUT_L0P_DPE2P AW37
TXOUT_L0N_DPE2N AU35
EV_TXLOUT0+ [27]
EV_TXLOUT0- [27]
TXOUT_L1P_DPE1P AR37
TXOUT_L1N_DPE1N AU39
EV_TXLOUT1+ [27]
EV_TXLOUT1- [27]
TXOUT_L2P_DPE0P AP35
TXOUT_L2N_DPE0N AR35
EV_TXLOUT2+ [27]
EV_TXLOUT2- [27]
TXOUT_L3P AN36
TXOUT_L3N AP37

SP@Madison/Broadway_M2

(1.8V@70mA AVDD)
+1.8V_GPU
120 ohm/300mA L15 BLM15BD121SN1_4
AVDD
C210 .1u/10V_4
C211 1u/6.3V_4
C207 10u/6.3V_6

(1.8V@100mA VDD1DI)
120 ohm/300mA L8 BLM15BD121SN1_4
VDD1DI
C123 .1u/10V_4
C122 1u/6.3V_4
C117 10u/6.3V_6

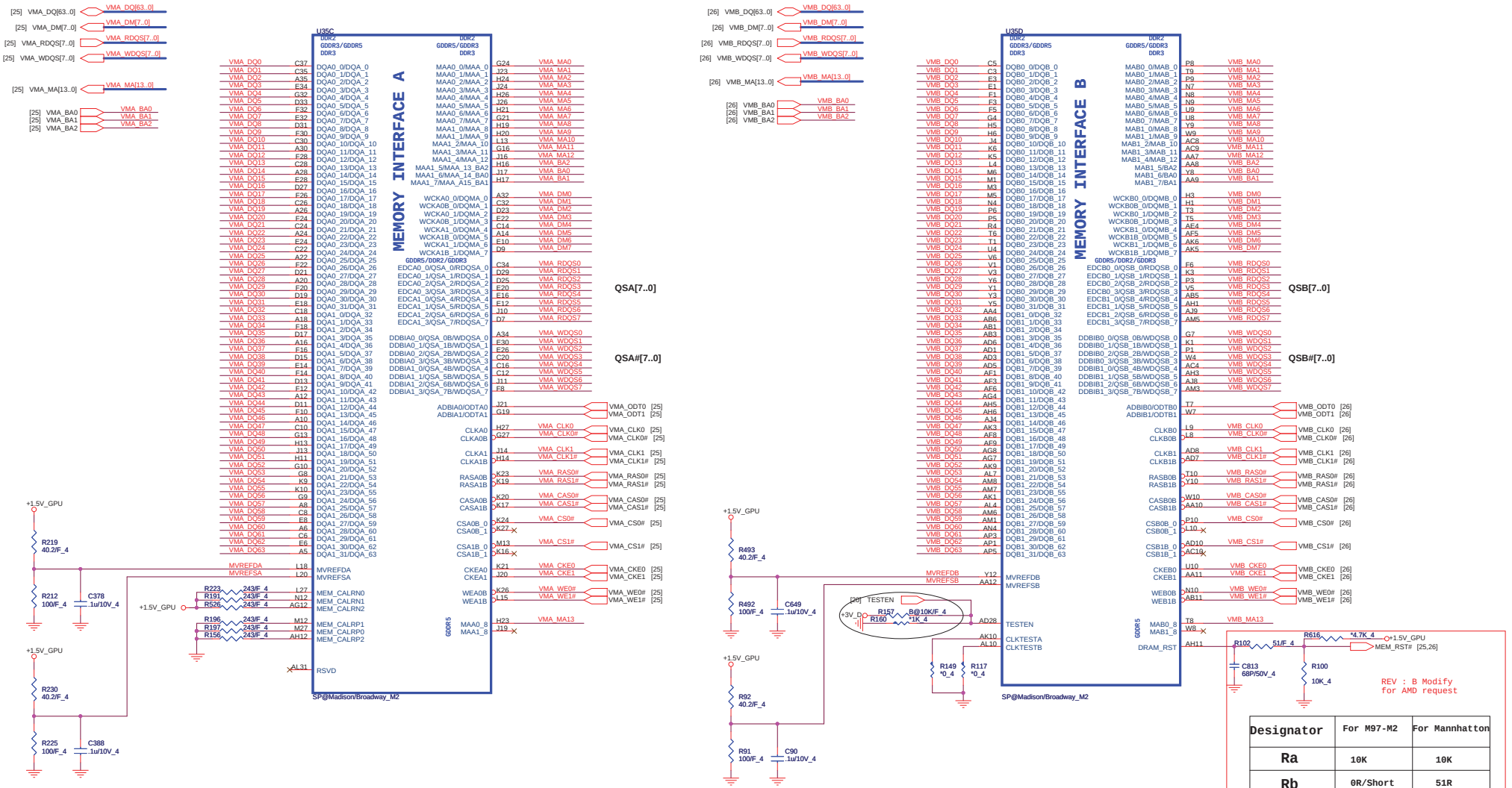
(1.8V@2mA A2VDDQ)
120 ohm/300mA L12 BLM15BD121SN1_4
A2VDDQ
C188 .1u/10V_4
C189 1u/6.3V_4

+1.8V(75mA)
120 ohm/300mA L47 BLM15BD121SN1_4 DPLL_PVDD
C654 10u_6
C676 1u_4
C666 .1u_4

+1.0V(125mA)
120 ohm/300mA L46 BLM15BD121SN1_4 DPLL_VDDC
C653 10u_6
C665 1u_4
C675 .1u_4

+1.8V(5mA)
120 ohm/300mA L11 BLM15BD121SN1_4 TS_VDD
C173 10u_6
C174 1u_4

+3V_D_ZY9B
C88 *.1u_4
U3 *74AHC125PW
GPIO24_TRSTB R96 *7.5K_4 C91 *100p/50V_6
C85 *100p/50V_6 R86 *7.5K_4
[11] GPU_RST_OP#
R106 *Short_4
[19] GPU_RST#
R110 *7.5K_4
C93 *100p/50V_6
TESTEN [21]



Designator	For M97-M2	For Mannhatton
Ra	10K	10K
Rb	0R/Short	51R
Rc	DNI	DNI
Ca	2.2nF	68pF

Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	Madison/Broadway-MEM I/F	1A

Date: Wednesday, January 20, 2010 Sheet 21 of 50

For DDR3, MVDDQ = 1.5V (7.5A)

(1.8V@400mA PCIE_VDDR)

(1.0V@1.1A PCIE_VDDC)

(30A or more)

(1.8V@110mA VDD_CT)

(3.3V@60mA))

(1.8V@40mA PCIE_PVDD)

(1.8V@150mA MPV18)

(1.8V@75mA SPV18)

(1.0V@120mA SPV10)

(DDR3 1.12V@4A VDDCI) or more

BIF_VDDC should be connected to VDDC if BACO feature not used.
For BACO, refer to the databook

PIN different between Broadway and Madison

Pin	Broadway	Madison
N27	VDDC	BIF_VDDC
AL31	TS_A	NC_TS_A
AL21	GND	PX_EN

PowerXpress control signal for Madsion and Park only
If not used, can be disconnected. (AL21 pin)

PX_EN = LOW, turn on
PX_EN = HIGH, turn off

Pin AL21 to Ground for Broadway

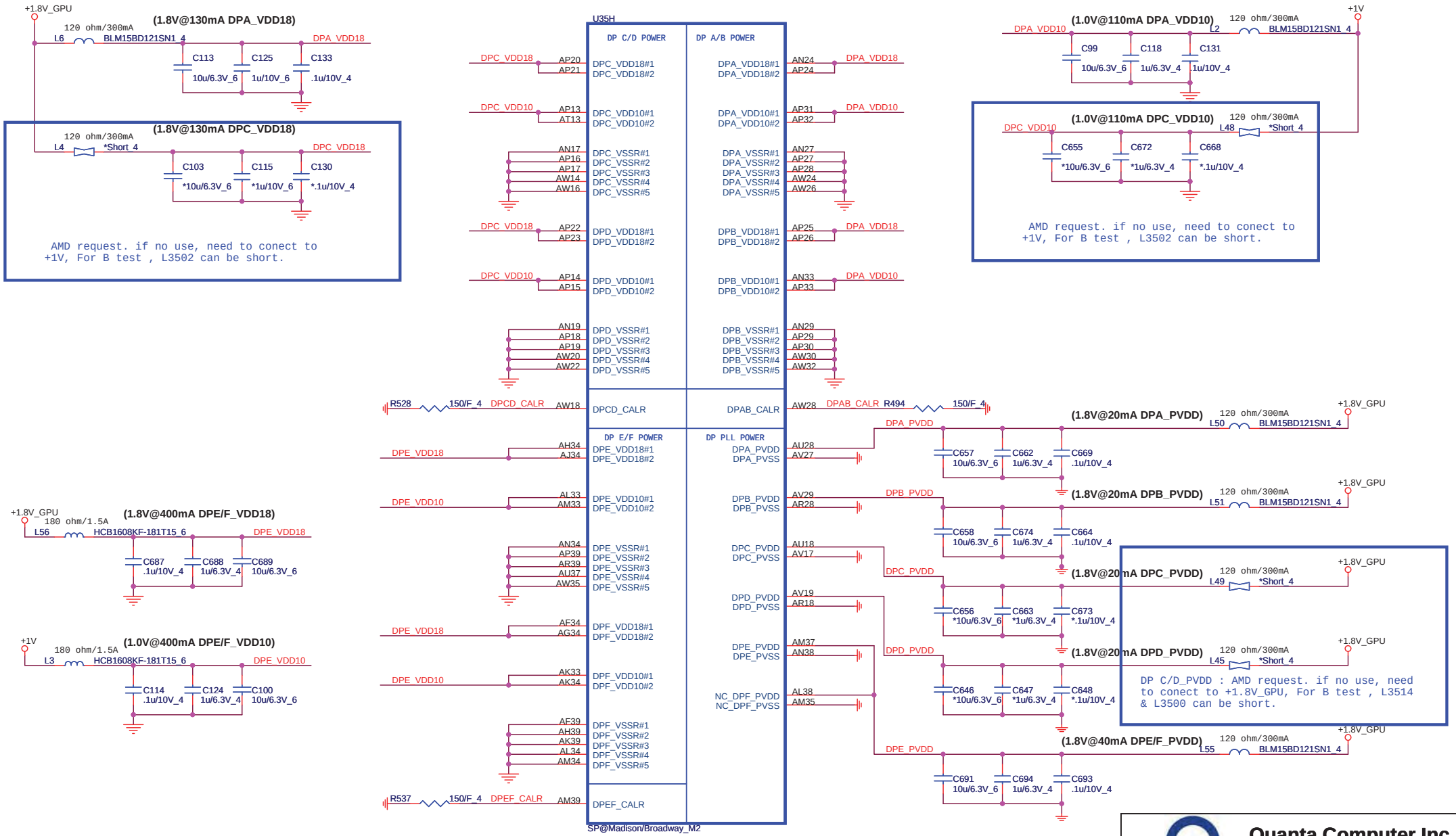
VDDC_SENSE/VSS_SENSE and VDDCI_SENSE/VSS_SENSE route as differetial pair

GPU +3V power

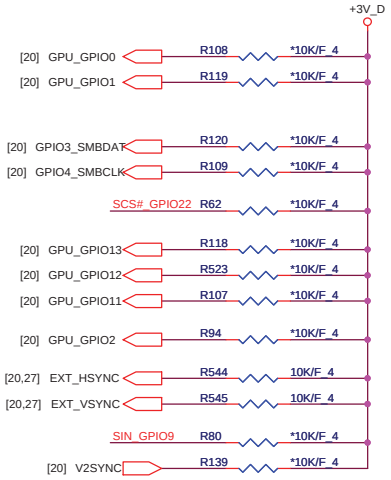
Fine-tune Power-on sequence

GPU all PWROK

Quanta Computer Inc.	
PROJECT : ZYA	
Size	Document Number: Madison/Broadway (PWR/GND) Rev: 1A
Date: Wednesday, January 20, 2010	Sheet 22 of 50


(1.8V@130mA DPA_VDD18)
(1.8V@130mA DPC_VDD18)
AMD request. if no use, need to conect to +1V, For B test , L3502 can be short.
U35H
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
SP@Madison/Broadway_M2
(1.0V@110mA DPA_VDD10)
(1.0V@110mA DPC_VDD10)
AMD request. if no use, need to conect to +1V, For B test , L3502 can be short.
(1.8V@20mA DPA_PVDD)
(1.8V@20mA DPB_PVDD)
(1.8V@20mA DPC_PVDD)
(1.8V@20mA DPD_PVDD)
DP C/D_PVDD : AMD request. if no use, need to conect to +1.8V_GPU, For B test , L3514 & L3500 can be short.
(1.8V@40mA DPE/F_PVDD)
(1.8V@400mA DPE/F_VDD18)
(1.0V@400mA DPE/F_VDD10)
Quanta Computer Inc.
PROJECT : ZYA
Madison/Broadway (DP_PWR/GND)
Size
Document Number
Rev 1A
Date: Wednesday, January 20, 2010
Sheet 23 of 50

PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

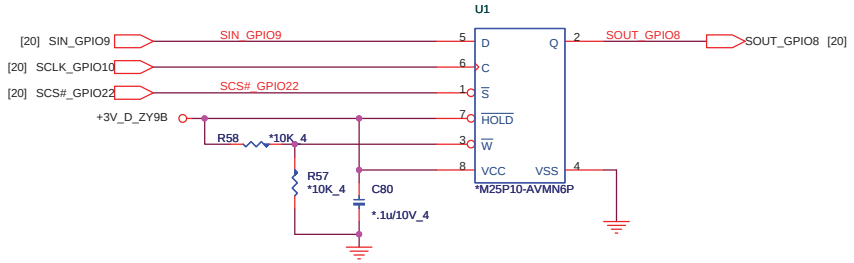
Audio Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

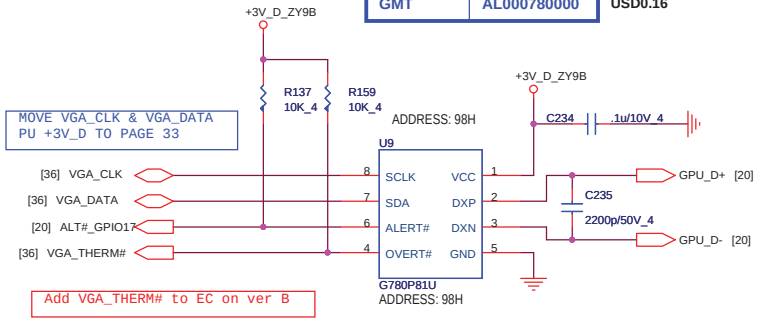
EEPROM



Thermal Sensor

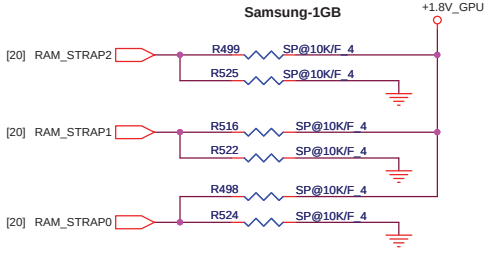
Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16



DDR3 VRAM SIZE Strap

DDR3 VRAM size						
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	512MB	1	1	0
			1GB	1	0	0
			2GB	1	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)				
			1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1
AMD	23EY2387MA-12	AKD5LGGT700	1GB	0	1	0

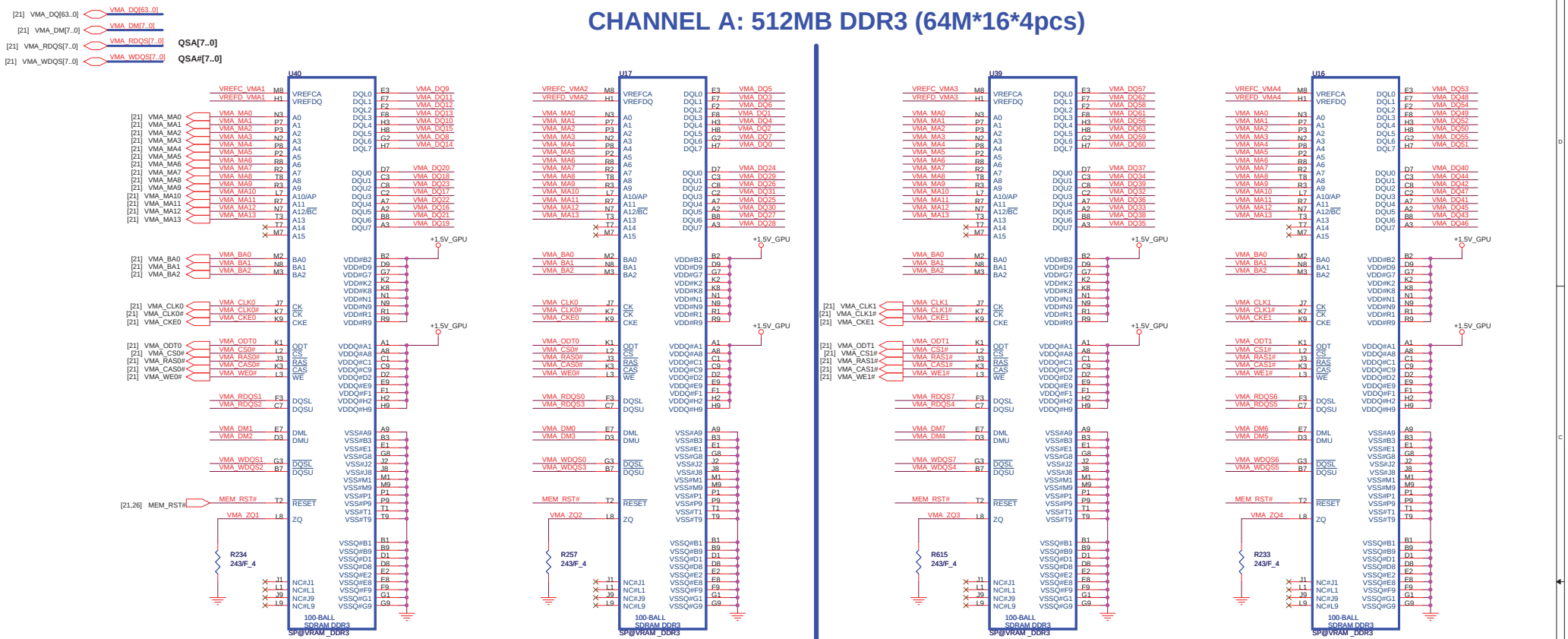


RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

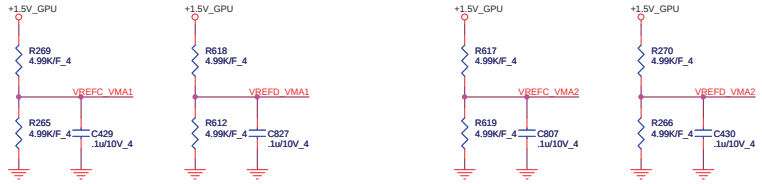
Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	Strip/Thermal	1A
Date: Wednesday, January 20, 2010	Sheet 24 of 50	

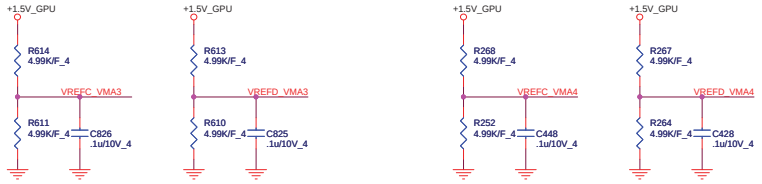
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



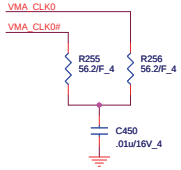
Group-A0 VREF



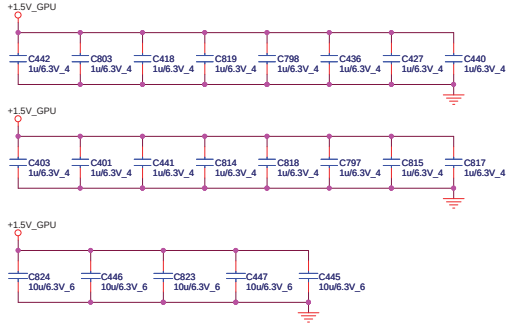
Group-A1 VREF



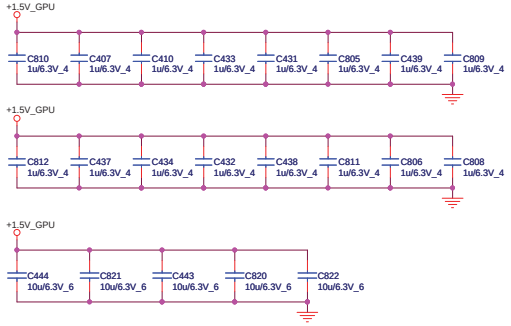
MEM_A0 CLK



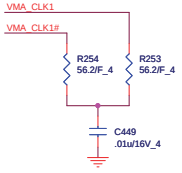
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



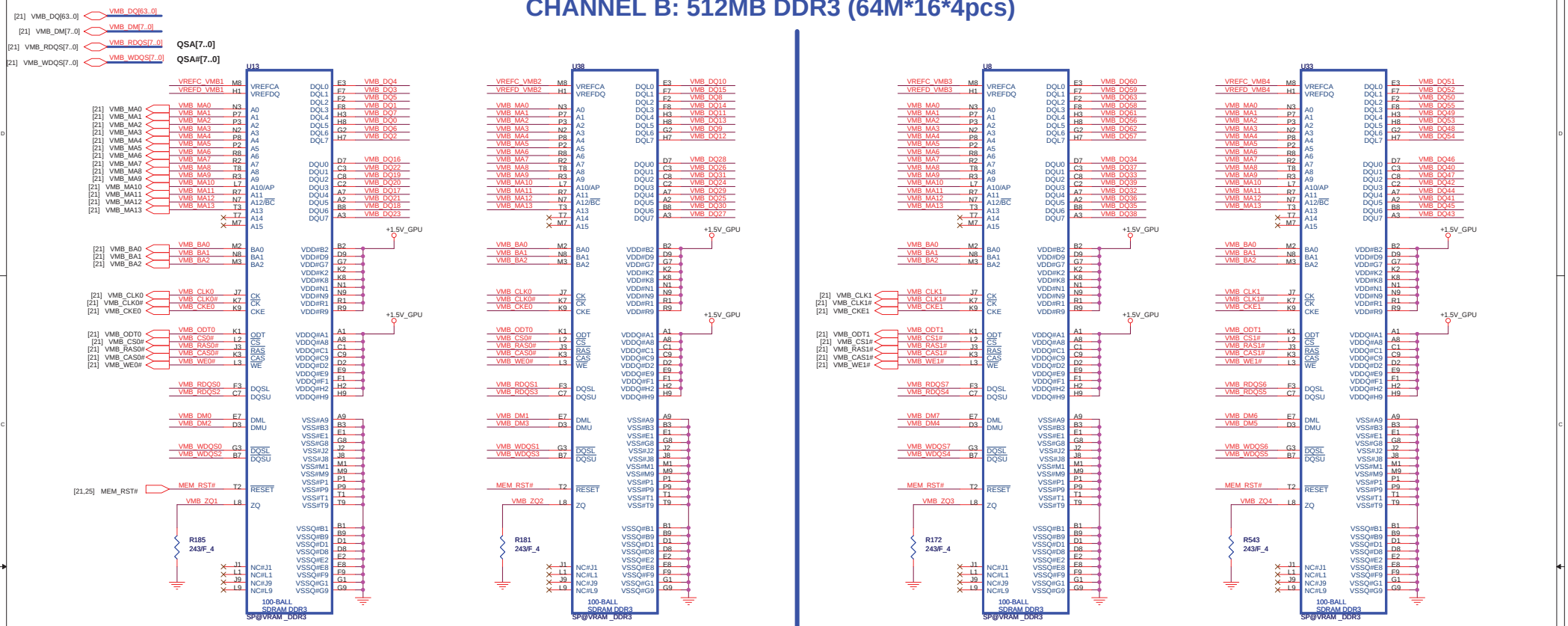
Quanta Computer Inc.

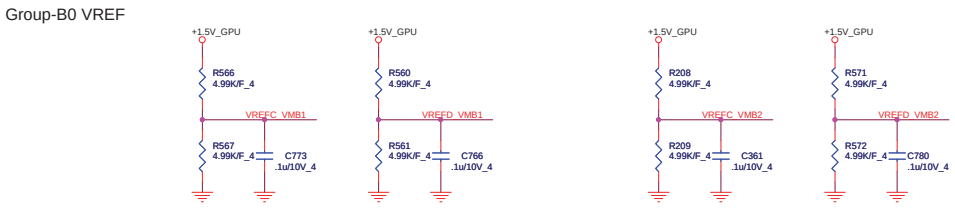
PROJECT : ZYA

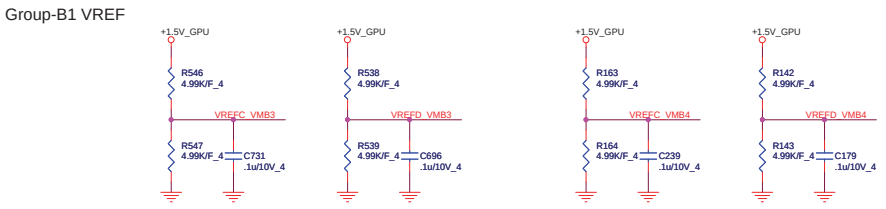
Size	Document Number	Rev
	MEMORY 1 channel A	1A

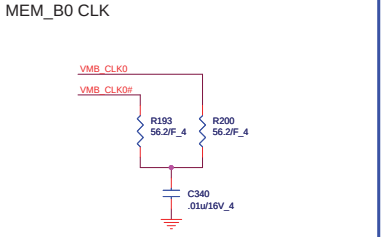
Date: Wednesday, January 20, 2010 Sheet 25 of 50

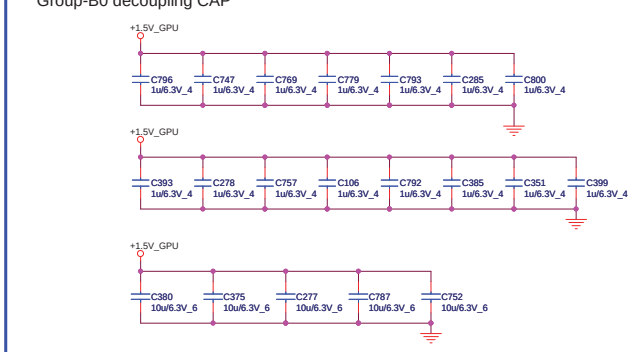
CHANNEL B: 512MB DDR3 (64M*16*4pcs)

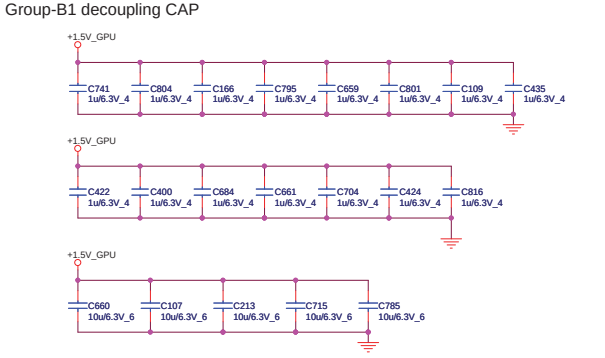


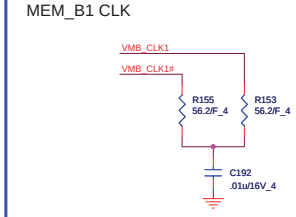










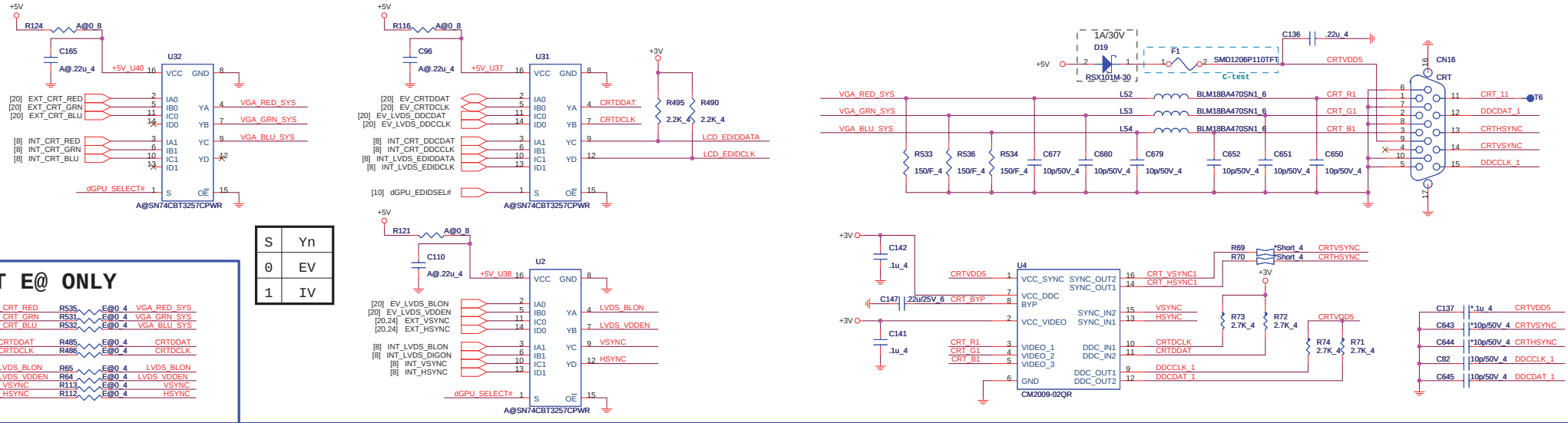


Quanta Computer Inc.

PROJECT : ZYA

Size	Document Number	Rev
	MEMORY 2 channel B	1A
Date: Wednesday, January 20, 2010	Sheet 26 of 50	

CRT

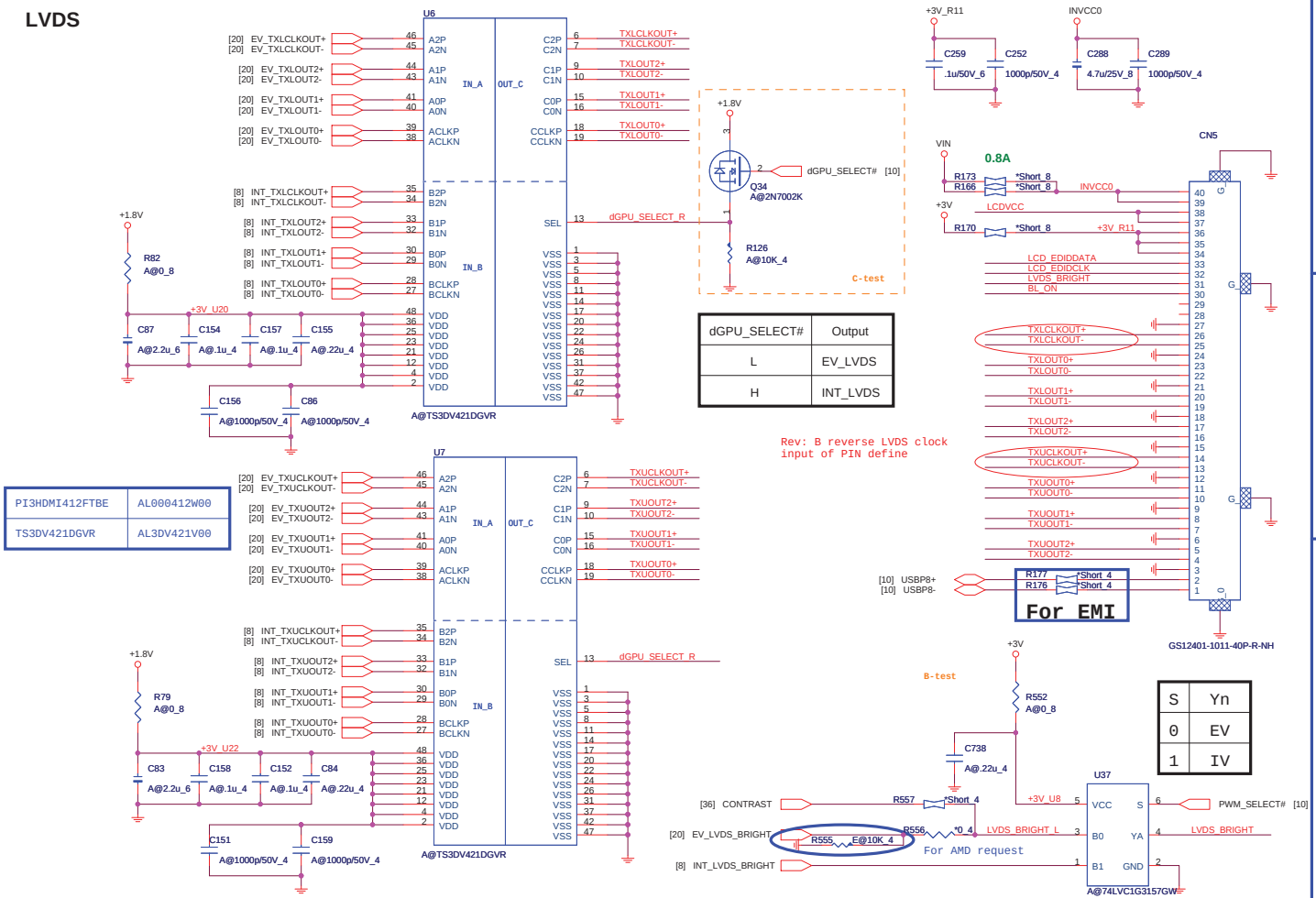


S	Yn
0	EV
1	IV

CRT E@ ONLY

EXT_CRT_RED	R535	E@0_4	VGA_RED_SYS
EXT_CRT_GRN	R531	E@0_4	VGA_GRN_SYS
EXT_CRT_BLU	R532	E@0_4	VGA_BLU_SYS
EV_CRTDDAT	R485	E@0_4	CRTDDAT
EV_CRTDCLK	R486	E@0_4	CRTDCLK
EV_LVDS_BLON	R65	E@0_4	LVDS_BLON
EV_LVDS_VDDEN	R64	E@0_4	LVDS_VDDEN
EXT_VSYNC	R113	E@0_4	VSYNC
EXT_HSYNC	R112	E@0_4	HSYNC

LVDS



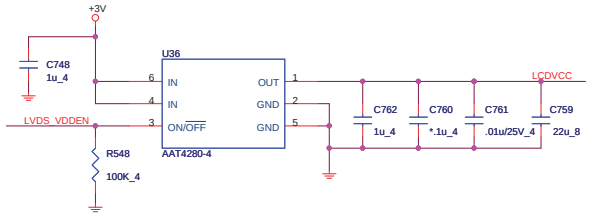
PI3HDMI412FTBE	AL000412W00
TS3DV421DGVR	AL3DV421V00

dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

Rev: B reverse LVDS clock input of PIN define

S	Yn
0	EV
1	IV

LCD Power

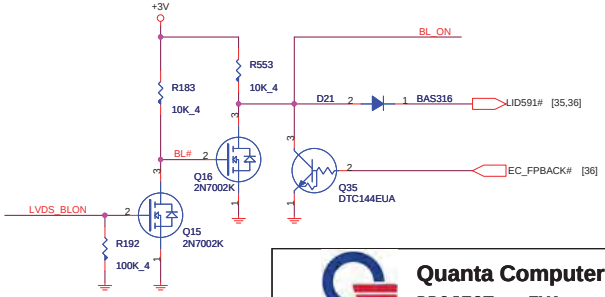


LVDS E@ ONLY

LVDS_BRIGHT R168 E@0_4 LVDS_BRIGHT_L

EV_TXLCLKOUT+	R500	E@0_4	TXLCLKOUT+
EV_TXLCLKOUT-	R501	E@0_4	TXLCLKOUT-
EV_TXLOUT2+	R502	E@0_4	TXLOUT2+
EV_TXLOUT2-	R503	E@0_4	TXLOUT2-
EV_TXLOUT1+	R504	E@0_4	TXLOUT1+
EV_TXLOUT1-	R505	E@0_4	TXLOUT1-
EV_TXLOUT0+	R506	E@0_4	TXLOUT0+
EV_TXLOUT0-	R507	E@0_4	TXLOUT0-
EV_TXUCLKOUT+	R508	E@0_4	TXUCLKOUT+
EV_TXUCLKOUT-	R509	E@0_4	TXUCLKOUT-
EV_TXUOUT2+	R510	E@0_4	TXUOUT2+
EV_TXUOUT2-	R511	E@0_4	TXUOUT2-
EV_TXUOUT1+	R512	E@0_4	TXUOUT1+
EV_TXUOUT1-	R513	E@0_4	TXUOUT1-
EV_TXUOUT0+	R514	E@0_4	TXUOUT0+
EV_TXUOUT0-	R515	E@0_4	TXUOUT0-
EV_LVDS_DDCDAT	R519	E@0_4	LCD_EDIDDATA
EV_LVDS_DDCCLK	R518	E@0_4	LCD_EDIDCLK

Backlight Control

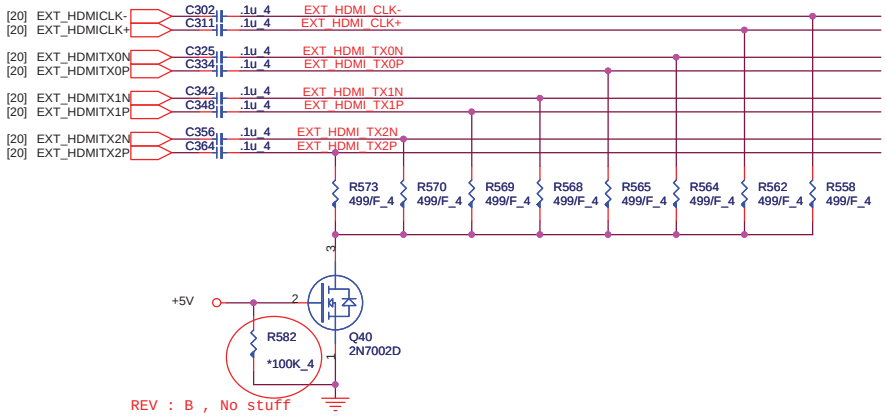


Quanta Computer Inc.
PROJECT : ZYA

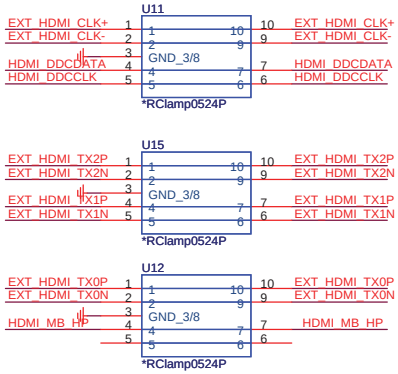
Size	Document Number	Rev
	CRT/LVDS/LID	1A

Date: Thursday, January 21, 2010 Sheet 27 of 50

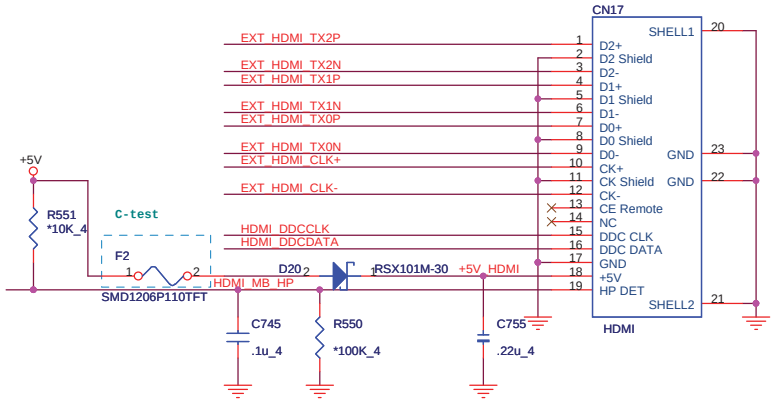
HDMI



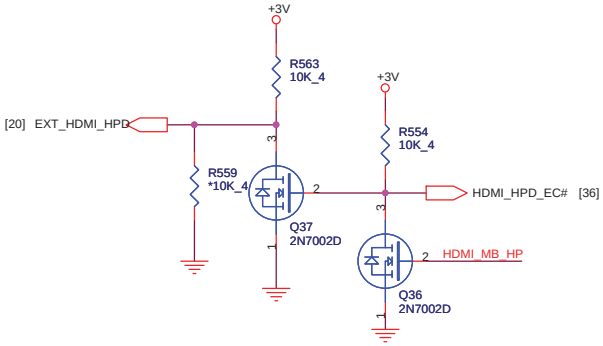
ESD Protect



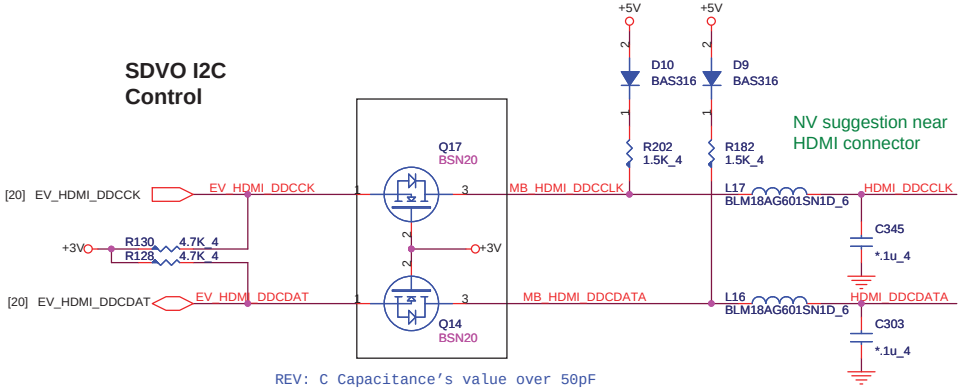
HDMI connector



HDMI Hot-PLUG to EC and GPU



SDVO I2C Control



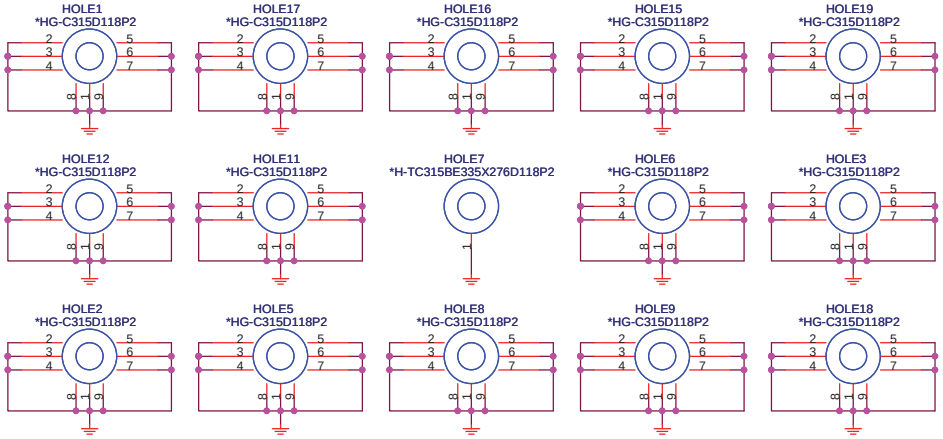
NV suggestion near HDMI connector

EXT_HDMI_CLK-	R1006	*100_4	EXT_HDMI_CLK+
EXT_HDMI_TX2N	R1007	*100_4	EXT_HDMI_TX2P
EXT_HDMI_TX1N	R1009	*100_4	EXT_HDMI_TX1P
EXT_HDMI_TX0N	R1008	*100_4	EXT_HDMI_TX0P

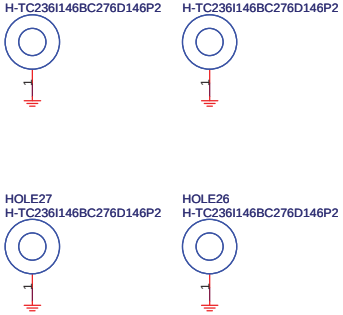
REV : B HDMI reserve 100 ohm parallel resister for EMI

REV: C Capacitance's value over 50pF

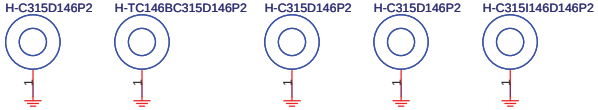
SCREW HOLE



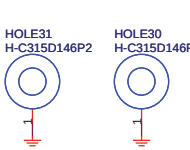
CPU NUT



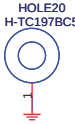
PCH & GPU NUT

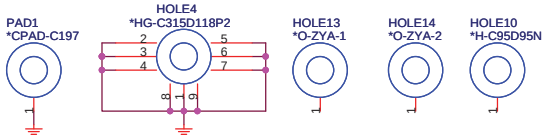


PCH NUT



MINI CARD NUT

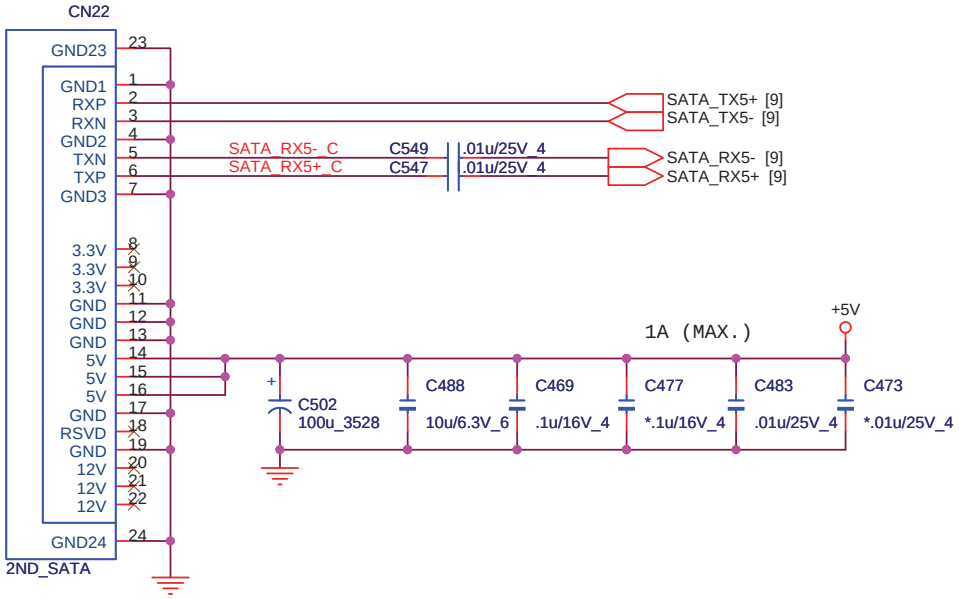




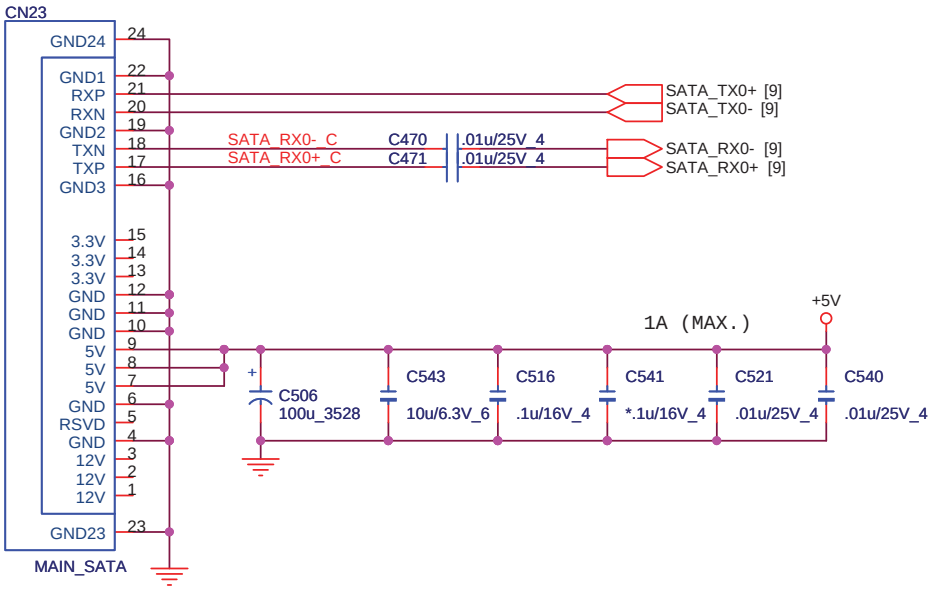
Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	HDMI/DP	1A
Date: Thursday, January 21, 2010	Sheet 28 of 50	

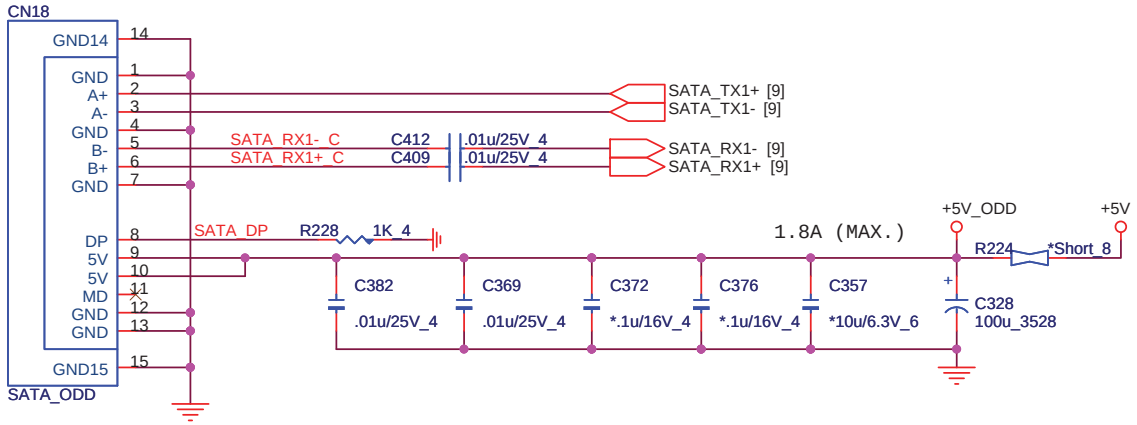
2nd SATA HDD (edge of board)



MAIN SATA HDD



ODD (SATA)



Quanta Computer Inc.

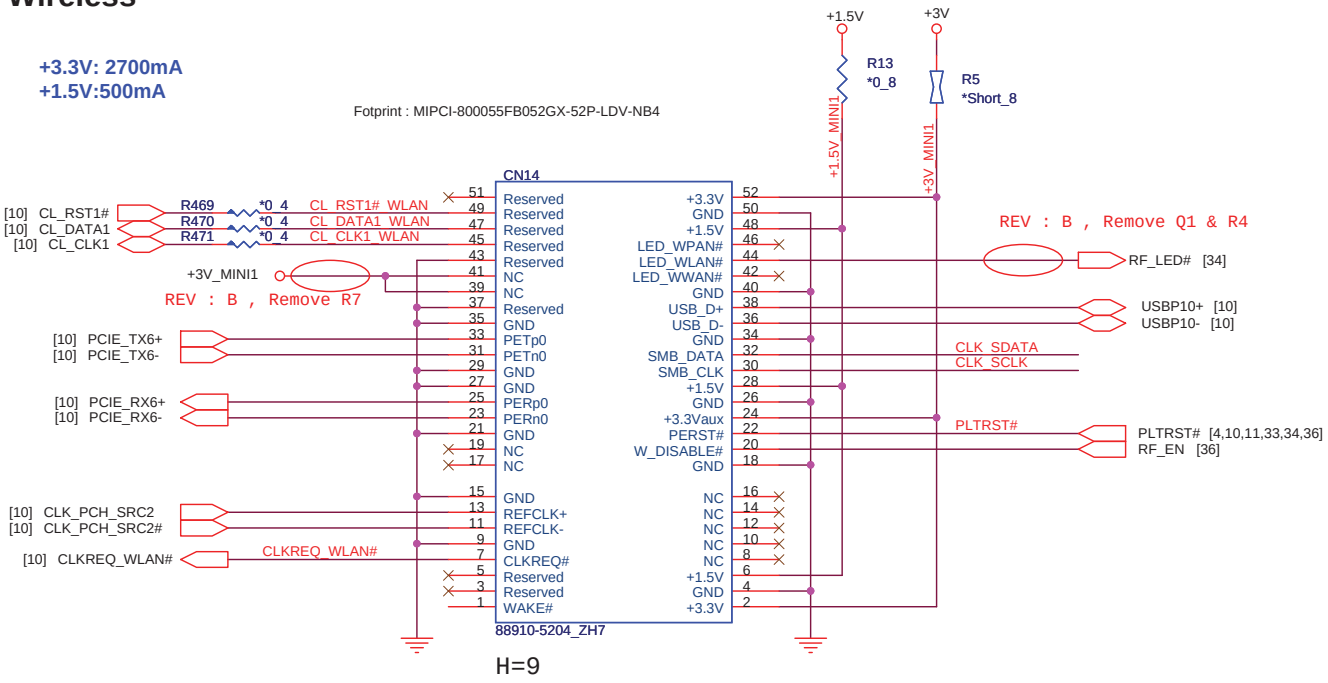
PROJECT : ZYA

Size	Document Number	Rev
	SATA-HDD/ODD	1A
Date: Wednesday, January 20, 2010	Sheet 29 of 50	

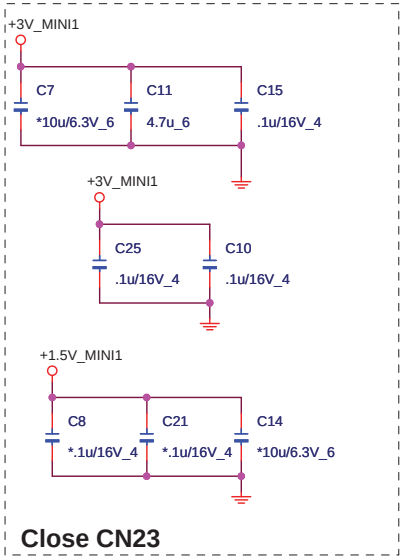
Wireless

+3.3V: 2700mA
+1.5V:500mA

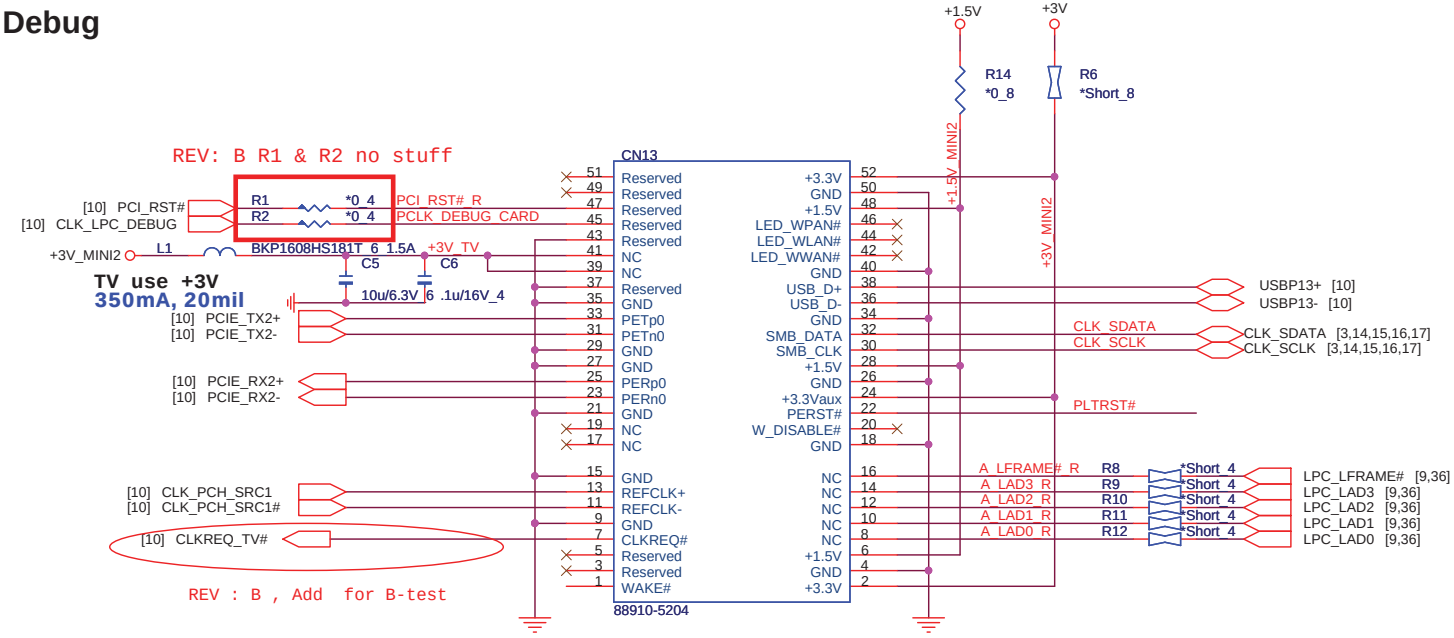
Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4



H=9



TV and Debug



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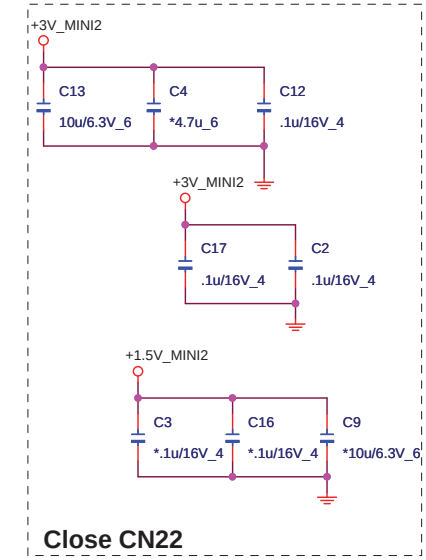
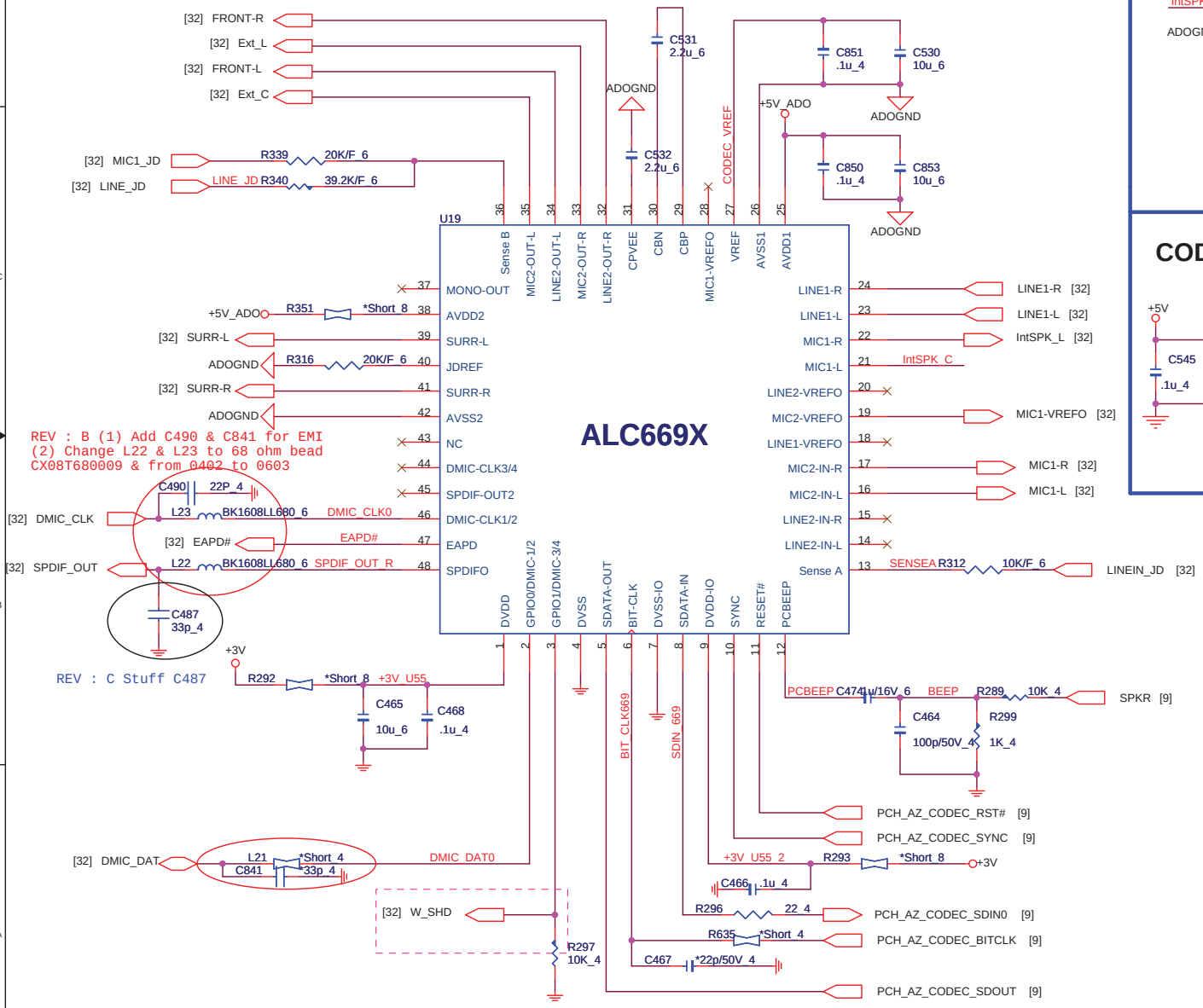
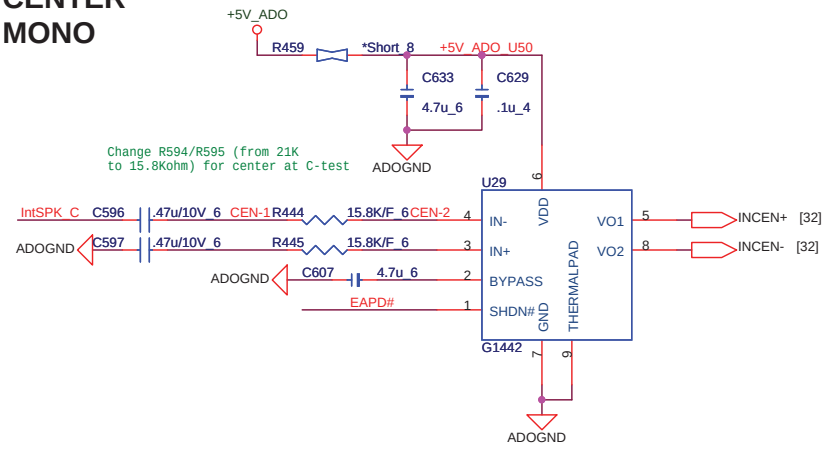


Quanta Computer Inc.		
PROJECT : ZYA		
Size	Document Number	Rev
	MINI PCI-E card/TV	1A
Date: Wednesday, January 20, 2010	Sheet 30 of 50	

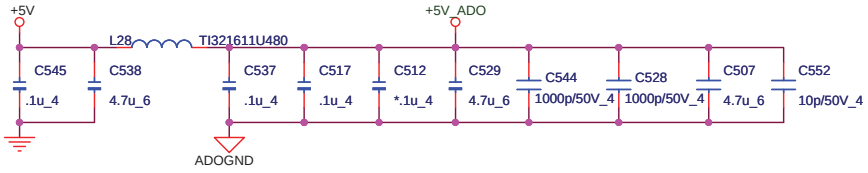
CODEC(ALC669X)



CENTER MONO



CODEC/AMP Power



PCH_AZ_CODEC_RST#

C840 *100p_6

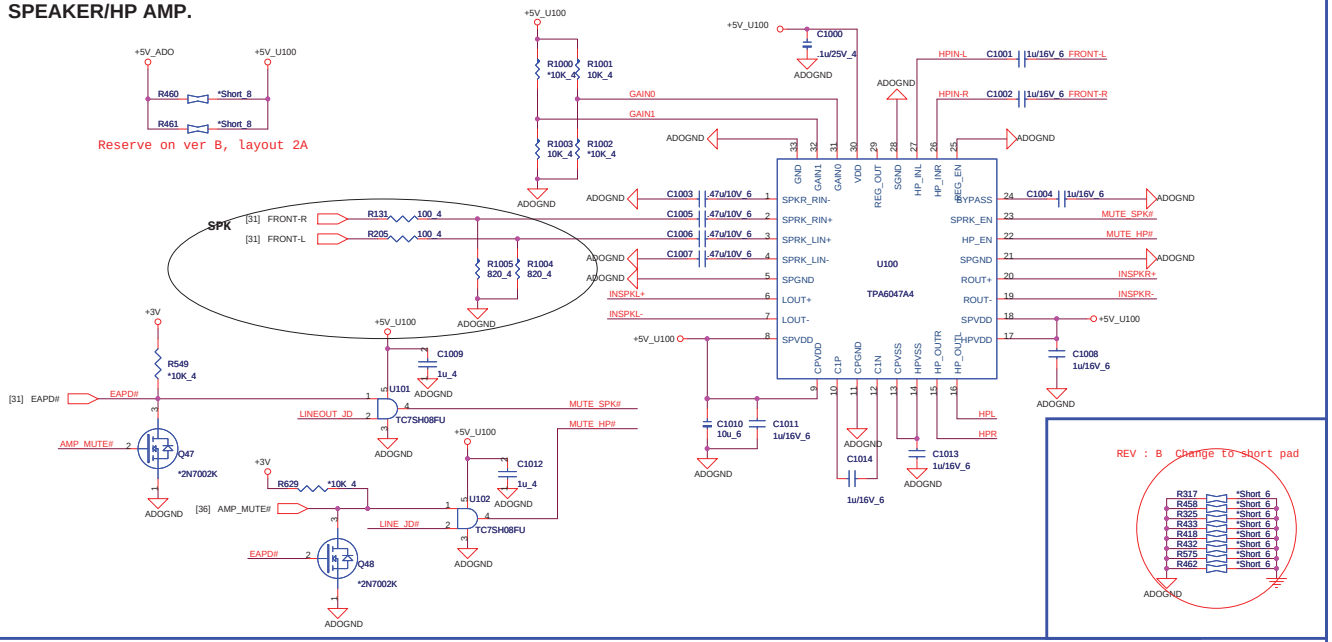
FOR ESD

Quanta Computer Inc.

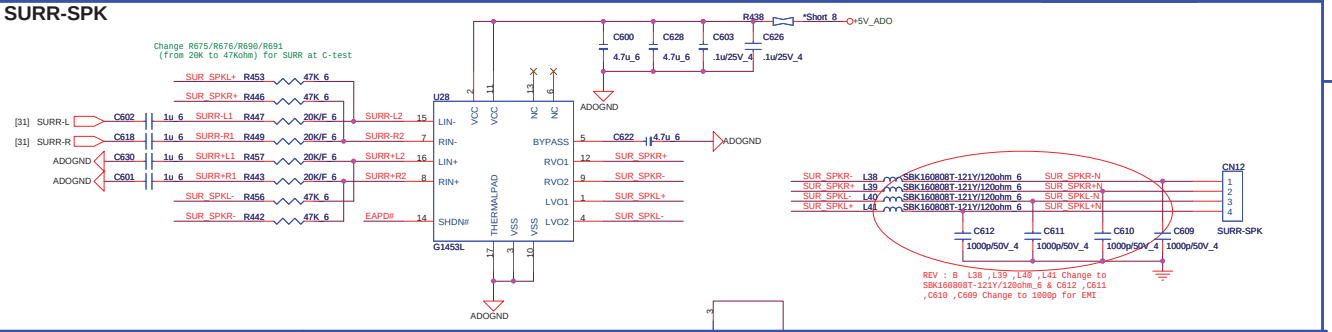
PROJECT : ZYA

Size	Document Number	Rev
	REALTEK ALC889X/MONO-AMP	1A
Date: Wednesday, January 20, 2010	Sheet 31 of 50	

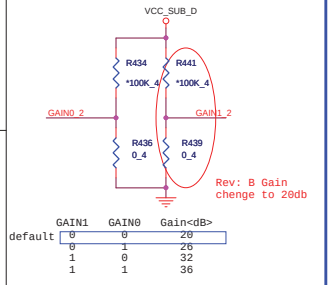
SPEAKER/HP AMP.



SURR-SPK



AMO GAIN



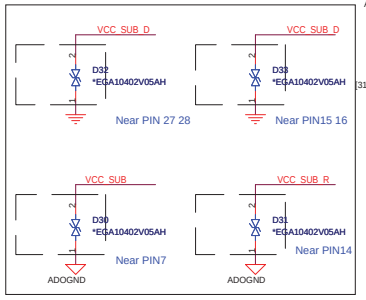
SUBWOOFER Power(AMP)

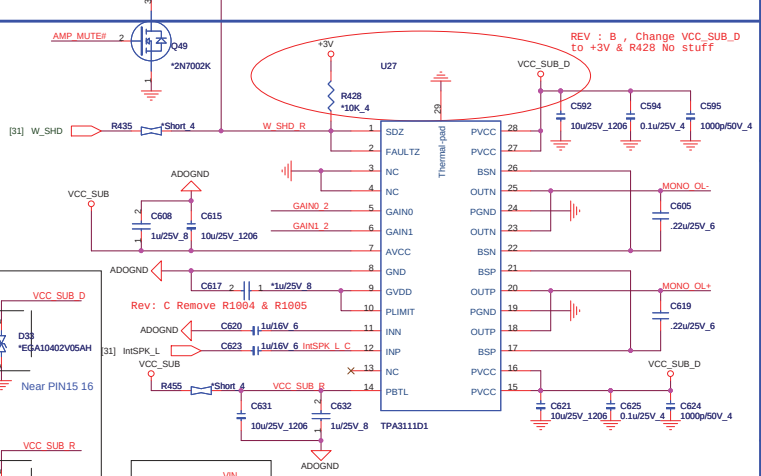
SUBWOOFER

LPF for fc(-3dB)=500Hz

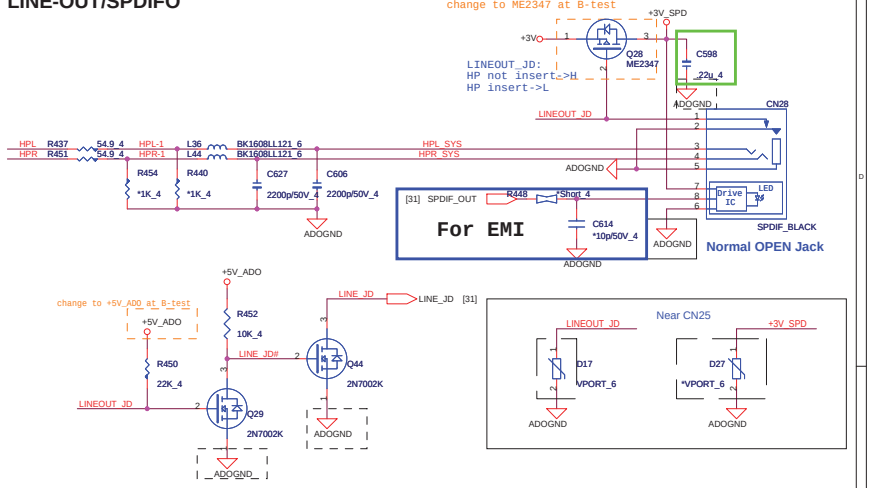
SDZ ::shutdown signal for
IC<LOW=disable , HIGH=enable>

SHUTDOWN	TPA3110D1
L (0V~0.8V)	SHUTDOWN
H (2V ~ VDD)	ACTIVE

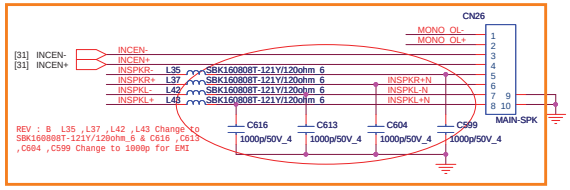




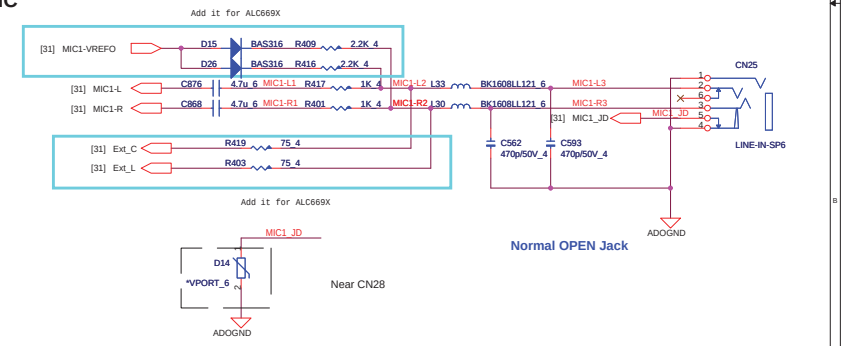
LINE-OUT/SPDIFO



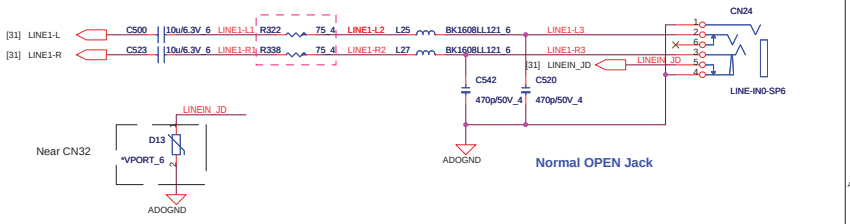
Main SPK/Center/Subwoofer EMI



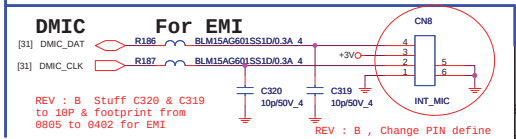
MIC



LINE IN



DMIC



Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	AMP/AUDIO JACK/WOOFER	1A
Date: Thursday, January 21, 2010	Sheet 32 of 50	

Remove R734

Each power pin is 100mA

REV : B , Remove L73 , L74

20mils

+3V R738 *Short_8 +3VCCD

C896 4.7U/6.3V_6 C894 0.1U/10V_4 C890 0.1U/10V_4

20mils

+3V L70 BLM18PG600SN1 +3VCCA

C874 4.7U/6.3V_6 C872 0.1U/10V_4

R726 *Short_6

REV : B , Change to 0 ohm

10mils

PE_3_3VCCA

As close as possible to OZ888GS0L3N

C884 *10U/6.3V_8 C885 *0.1U/10V_4

CORE_VCCD 40mils

C879 4.7U/6.3V_6 C883 0.1U/10V_4 C892 *0.1U/10V_4 C891 *0.1U/10V_4

L72 *BLM18PG600SN1_6 +1.8V

R736 *Short_8

C878 4.7U/6.3V_6

25mils

1394_PE_VCCA

L68 PBY160808T-301Y-N_6

C889 4.7U/6.3V_6 C886 *0.1U/10V_4 C882 0.1U/10V_4

L69 *BLM18PG600SN1_6 +1.8V

10mils

VCCA_OUT

C875 *4.7U/6.3V_6 C873 0.1U/10V_4

U45

OZ888GS0L3N

PE_3_3VCCA 3.3VCCA 3.3VCCD AUX_VCCD CORE_VCCD VCCD_OUT PE_VCCA VCCA_OUT

PLL_REF_RETURN R730 *1.2K/F_4 PCIE_RTERM2 R729 5.1K/F_4 PCIE_RTERM1

[10] PCIE_TX5+ [10] PCIE_TX5- PCIE_RXP PCIE_RXN

[10] PCIE_RX5+ [10] PCIE_RX5- C887 C888 0.1U/10V_4 PCIE_RX5+_C 0.1U/10V_4 PCIE_RX5-_C PCIE_TXP PCIE_TXN

[10] CLK_PCH_SRC3 [10] CLK_PCH_SRC3# CLK_PCH_SRC3 CLK_PCH_SRC3# PE_REFCLKP PE_REFCLKN

[4,10,11,30,34,36] PLTRST# R733 *Short_4 A_RST#_PCIC PE_RST#

[10] CLK_PCIE_REQ3# CLK_PCIE_REQ3# PE_CLKREQ#

[36] CR_CPPE#SD WAKEUP#

+3V R732 10K_4

These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.

1394_TPB0- 1394_TPB0+ 1394_TPA0- 1394_TPA0+ TPBIAS0 1394_TPBN 1394_TPBP 1394_TPAN 1394_TPAP 1394_TPBIAS

C881 18P/50V_4 1394_XIN Y6 24.576MHZ C880 18P/50V_4 1394_XOUT 1394_XI 1394_XO 1394_REF

H=1.2mm Better than 50ppm

R731 5.9K/F_4 1394_REF

As close as possible to OZ888GS0LN

OZ888GS0L3N-C1 vqfn64-8x8-4-65p

AGND DGND

MMI_VCC 40mils C893 *4.7U/10V_6

XD_CD# MS_CD# SD_CD# XD_CDSW# MS_INS# SD_C/D

SD_WPI XD_WPO XD_RE# XD_RB# XD_CLE MMI_CLK/CE# XD_WE# MMI_BS/CMD/ALE SD_WP# XD_WP# XD-RE# XD_R/B XD-CLE XD_CE# XD-WE SD/XD/MS_CMD

MMI_D7 MMI_D6 MMI_D5 MMI_D4 MMI_D3 MS_XD_D2 SD_D2 MS_XD_D1 SD_D1 MMI_D0 XD/MMS_DATA7 XD/MMS_DATA6 XD/MMS_DATA5 XD/MMS_DATA4 SD/XD/MS_DATA3 XD/MS_DATA2 SD_DATA2 XD/MS_DATA1 SD_DATA1 SD/XD/MS_DATA0

MMI_LED

REV : B , Remove the U46 circuit (LDO)

REV : B , remove 0 ohm

MMI_VCC C860 0.1U/10V_4 C859 0.1U/10V_4 C861 0.1U/10V_4

CN11

XD_R/B XD-RE# XD_CE# XD-CLE SD/XD/MS_CMD XD-WE XD_WP# SD/XD/MS_DATA0 XD/MS_DATA1 SD_DATA2 SD/XD/MS_DATA3 SD/XD/MS_CMD MMI_VCC XD_CE# SD/XD/MS_DATA3 MS_INS# XD/MS_DATA2 SD/XD/MS_DATA0

XD-R/B XD-RE XD-CE XD-CLE XD-ALE XD-WE XD-WP XD-D0 XD-D1 SD-DAT2 SD-DAT3 SD-CMD 4IN1-GND1 MS-VCC MS-SCLK MS-DATA3 MS-INS MS-DATA2 MS-DATA0

MS-DATA1 MS-BS 4IN1-GND2 SD-VCC SD-CLK SD-DAT0 XD-D2 XD-D3 XD-D4 SD-DAT1 XD-D5 XD-D6 XD-D7 XD-VCC XD-CD-SW SD-WP-SW SD-CD-SW

XD/MS_DATA1 SD/XD/MS_CMD XD_CE# SD/XD/MS_DATA0 XD/MS_DATA2 SD/XD/MS_DATA3 XD/MMS_DATA4 SD_DATA1 XD/MMS_DATA5 XD/MMS_DATA6 XD/MMS_DATA7 XD_CDSW# SD_WP# SD_C/D

SHIELD1-GND SHIELD2-GND SHIELD3-GND SHIELD4-GND

CONN_CARDREADER

MMI_VCC

As close as possible to CN35 Pin12

1394 [FIW]

TPBIAS0 C843 1U/10V_4

R642 56.2/F_4 R637 56.2/F_4

1394_TPA0+ 1394_TPA0-

As close as possible to OZ888GS0LN

1394_TPB0- 1394_TPB0+

R634 56.2/F_4 R631 56.2/F_4

1394_COM

R632 5.1K/F_4 C838 270P/25V_4

1394_TPB0- D23 *EGA10402V05AH

1394_TPA0- D24 *EGA10402V05AH

1394_TPA0+ D25 *EGA10402V05AH

1394_TPB0+ D22 *EGA10402V05AH

CN21

1394_TPA0+ 1394_TPB0+ 1394_TPB0- 1394_TPA0-

1394/STD

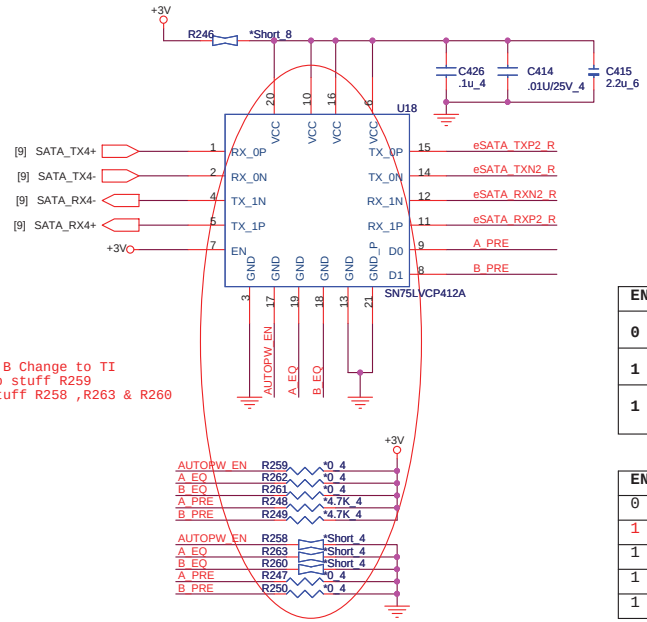
These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.

Quanta Computer Inc.

PROJECT : ZYA

Size	Document Number	Rev
	OZ888 Card Reader & 1394	1A
Date: Wednesday, January 20, 2010	Sheet 33 of 50	

ESATA & USB



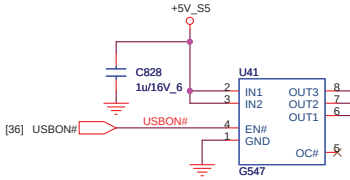
Rev : B Change to TI
(1) No stuff R259
(2) Stuff R258 ,R263 & R260

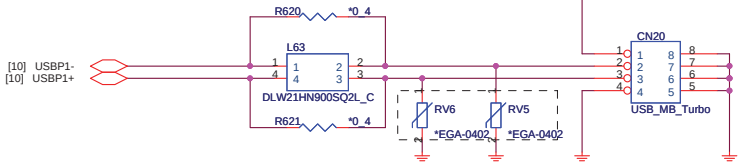
AL008511001

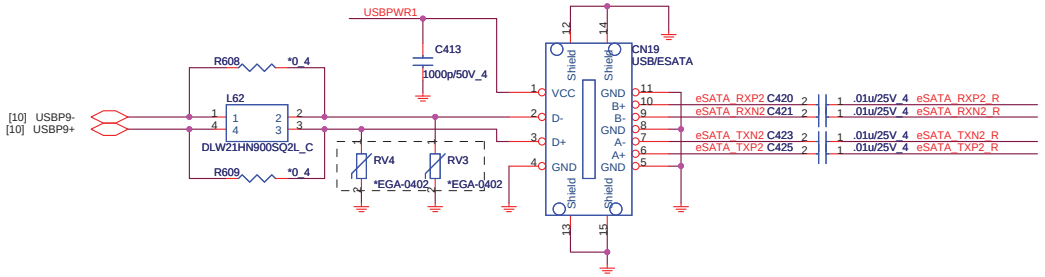
EN	A_PRE	B_PRE	dB
0	X	X	Power down mode
1	0	0	Pre-emphasis disable
1	1	1	Pre-emphasis enable

ALLVC412000

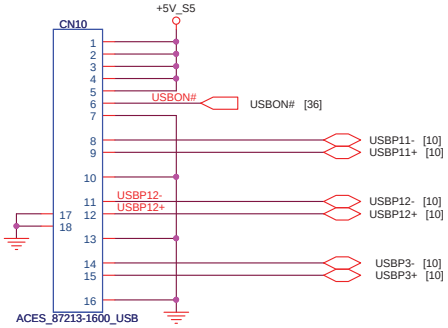
EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

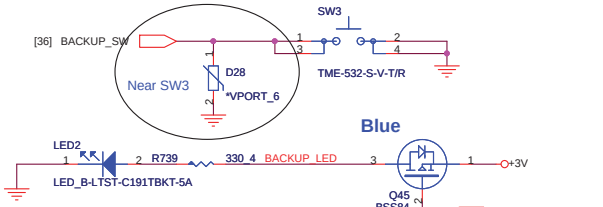


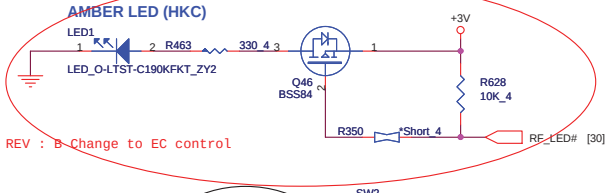


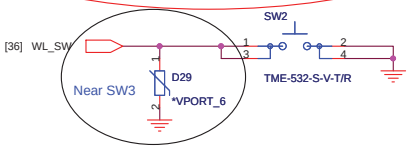


To USB/B

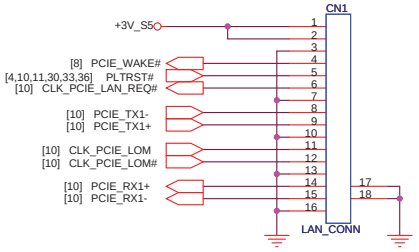




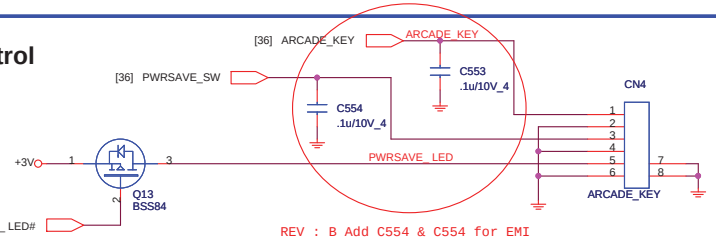


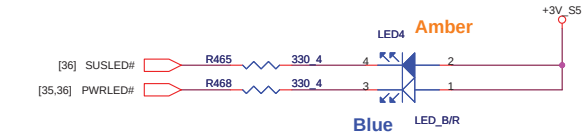


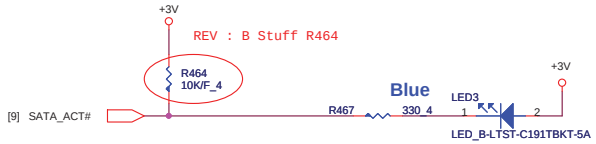
To LAN/B



Keyboard LED control





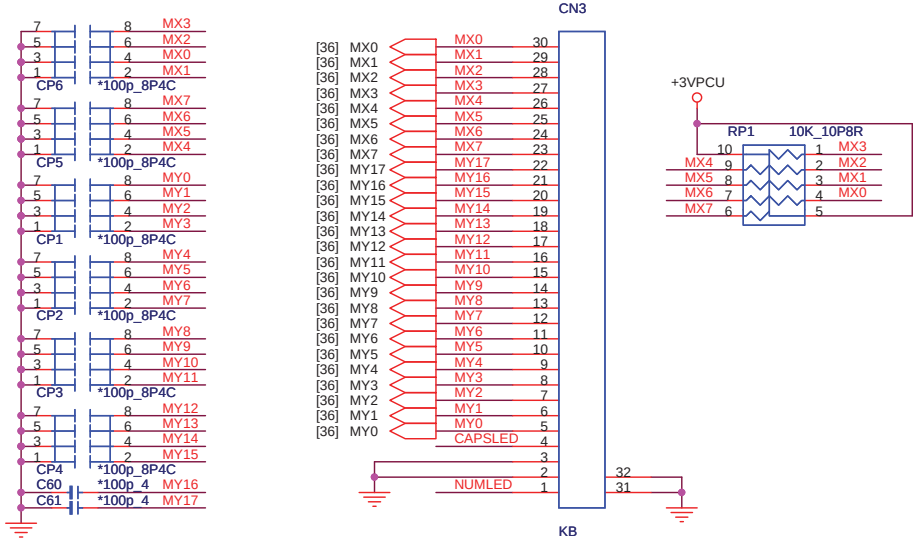


Quanta Computer Inc.
PROJECT : ZYA

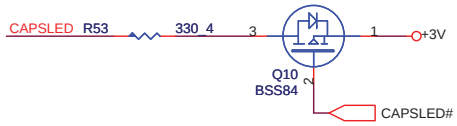
Size	Document Number	Rev
	USB/eSATA/TP_Screen	1A

Date: Wednesday, January 20, 2010 Sheet 34 of 50

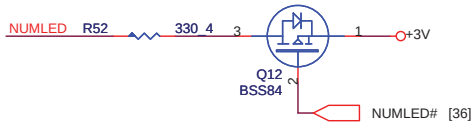
INT K/B



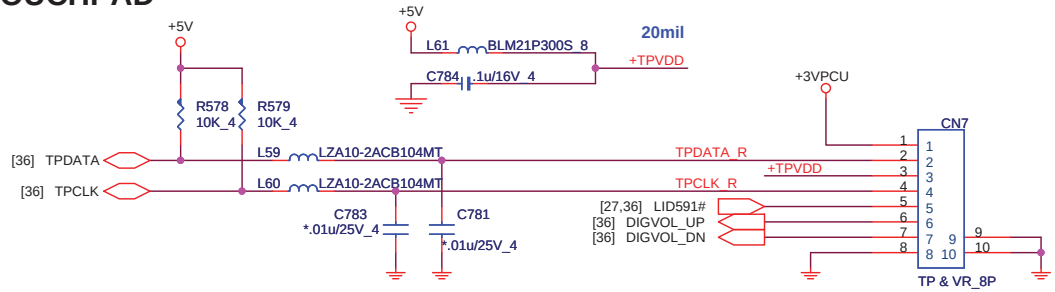
AMBER LED (HKC)



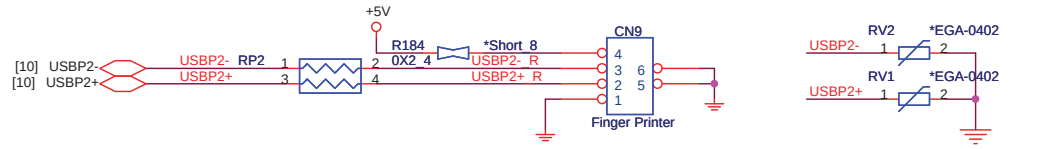
AMBER LED (HKC)



TOUCHPAD

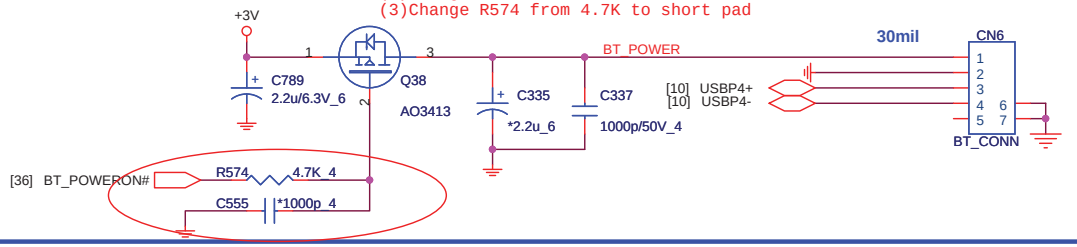


Finger-Printer

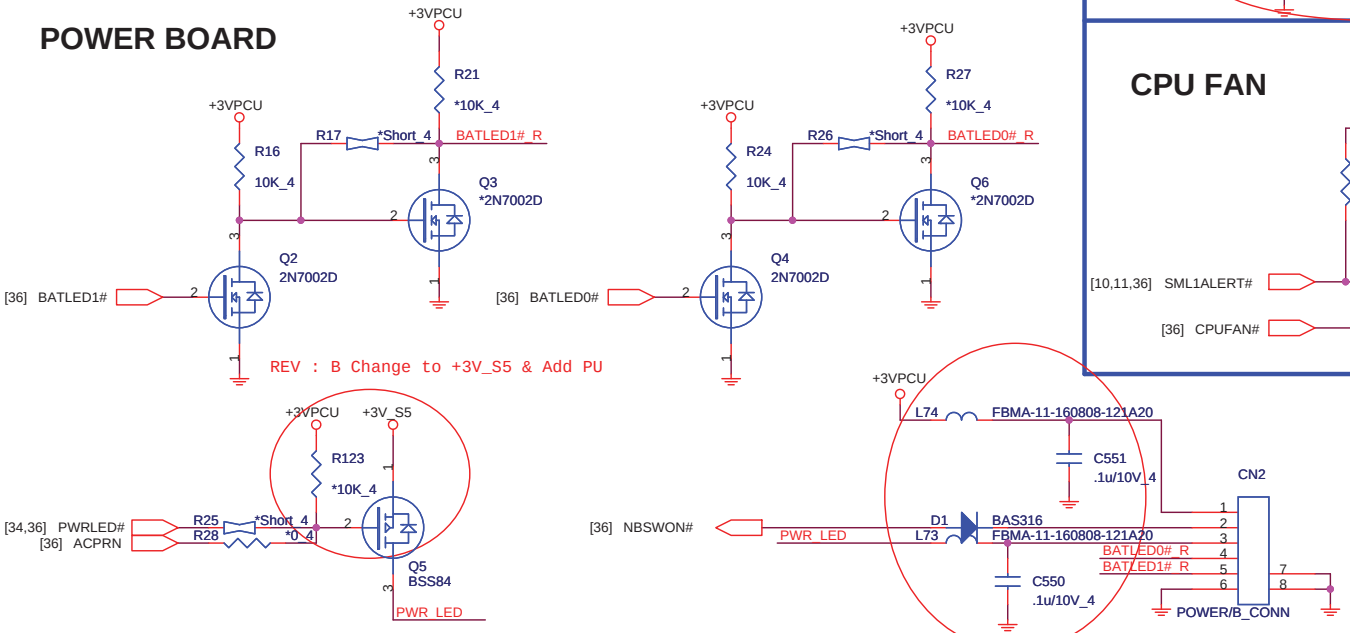


BLUETOOTH

Rev: B (1) del. R575
(2)change C789 from .33u to 2.2u
(3)Change R574 from 4.7K to short pad



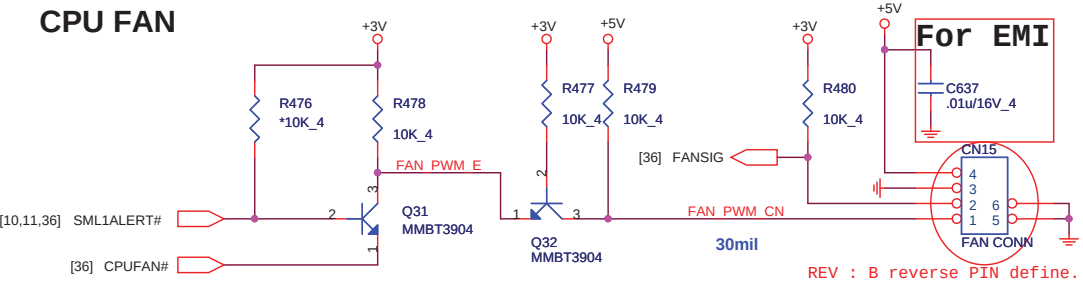
POWER BOARD



REV : B Add L73 ,L74 , C551 & C550 for EMI

CPU FAN

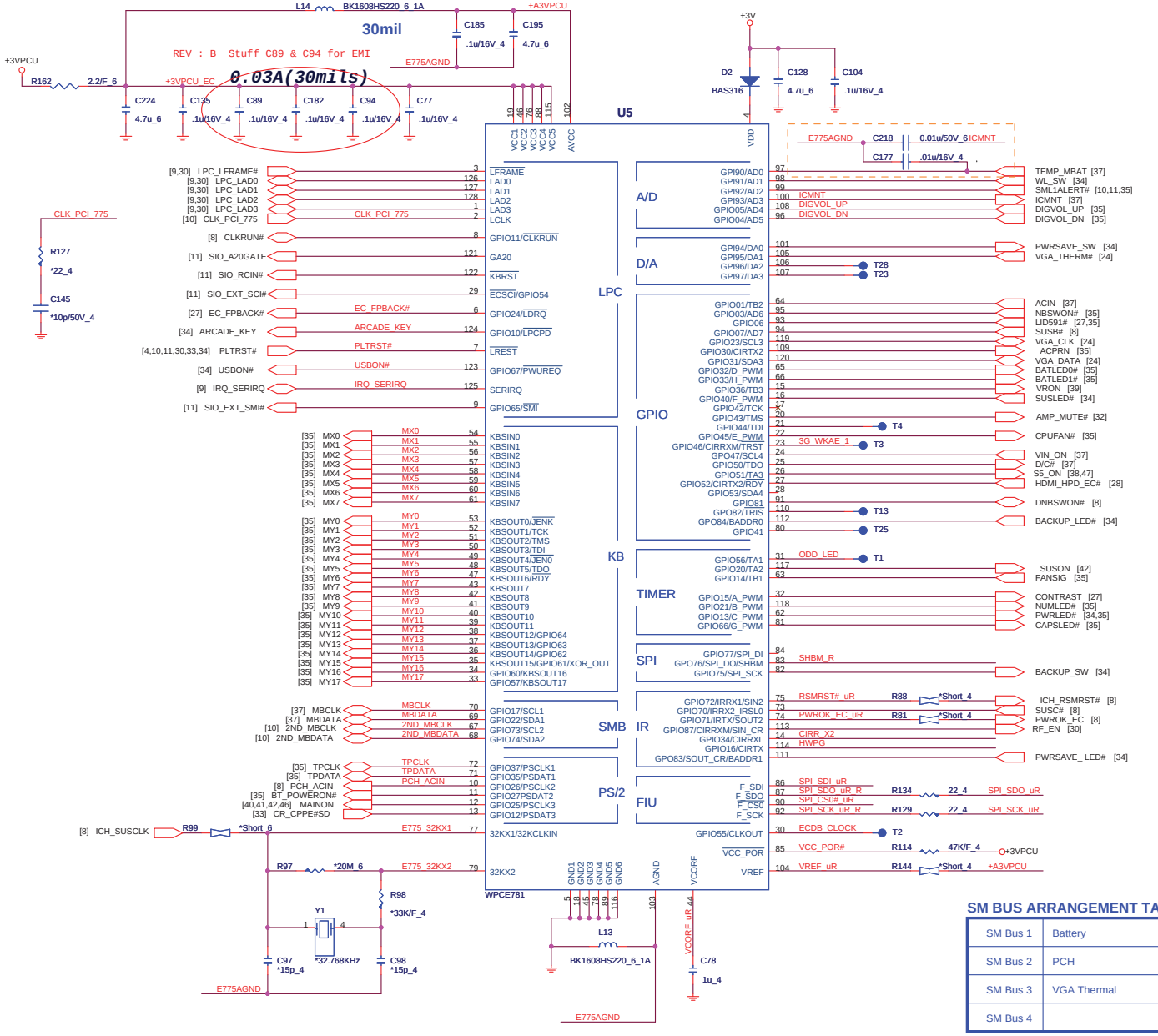
REV : B Stuff C637 for EMI



REV : B reverse PIN define.

Quanta Computer Inc.		
PROJECT : ZYA		
Size	Document Number	Rev
	KB/FAN/TP+FP/BT	1A
Date: Wednesday, January 20, 2010	Sheet 35 of 50	

EC



I/O ADDRESS SETTING

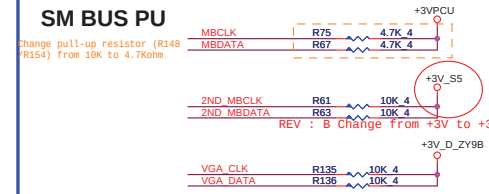
	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

SHBM SHBM_R R111 10K_4

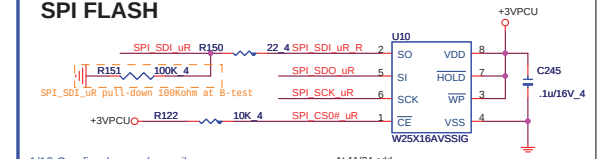
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU



INTERNAL KEYBOARD STRIP SET

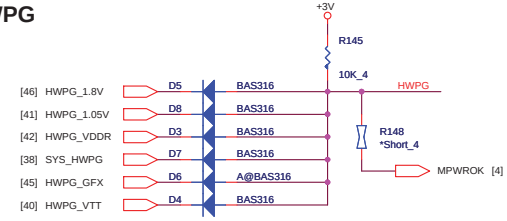
SPI FLASH



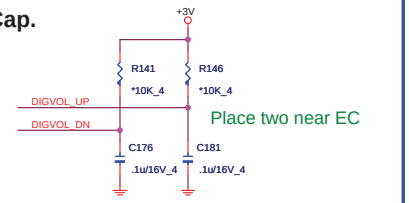
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add
Winbond W25X16AVSSIG AKE38ZP0N01
EON EN25F16-100HIP AKE38ZA0Q00
AMIC A25L016 AKE38ZN0800

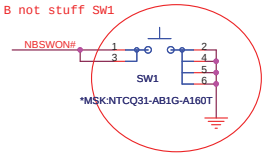
HWPG



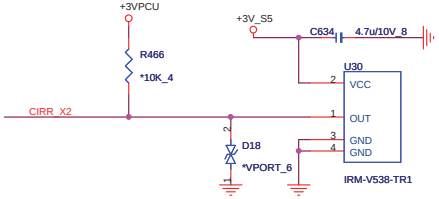
VR Cap.



POWER-ON Switch

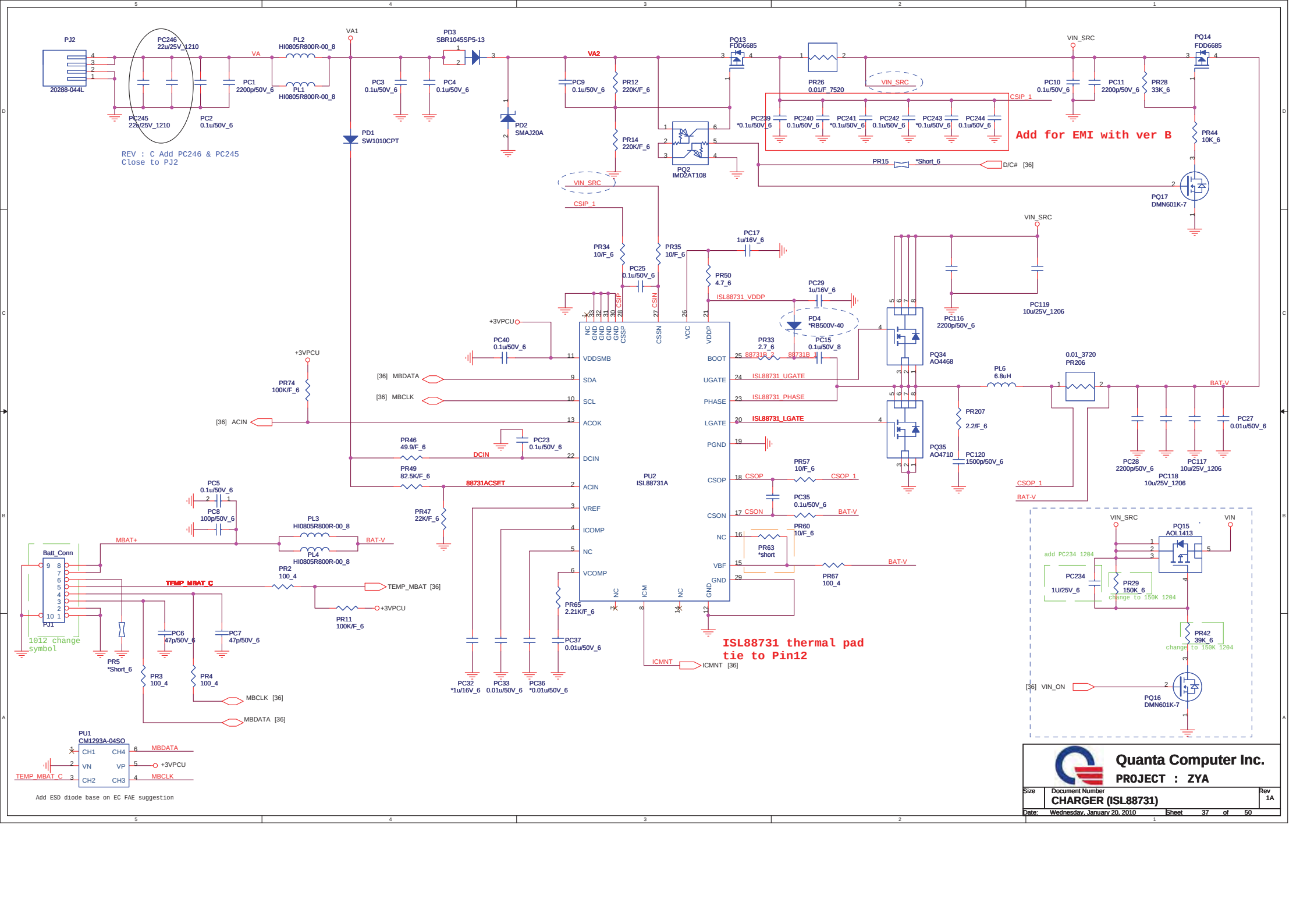


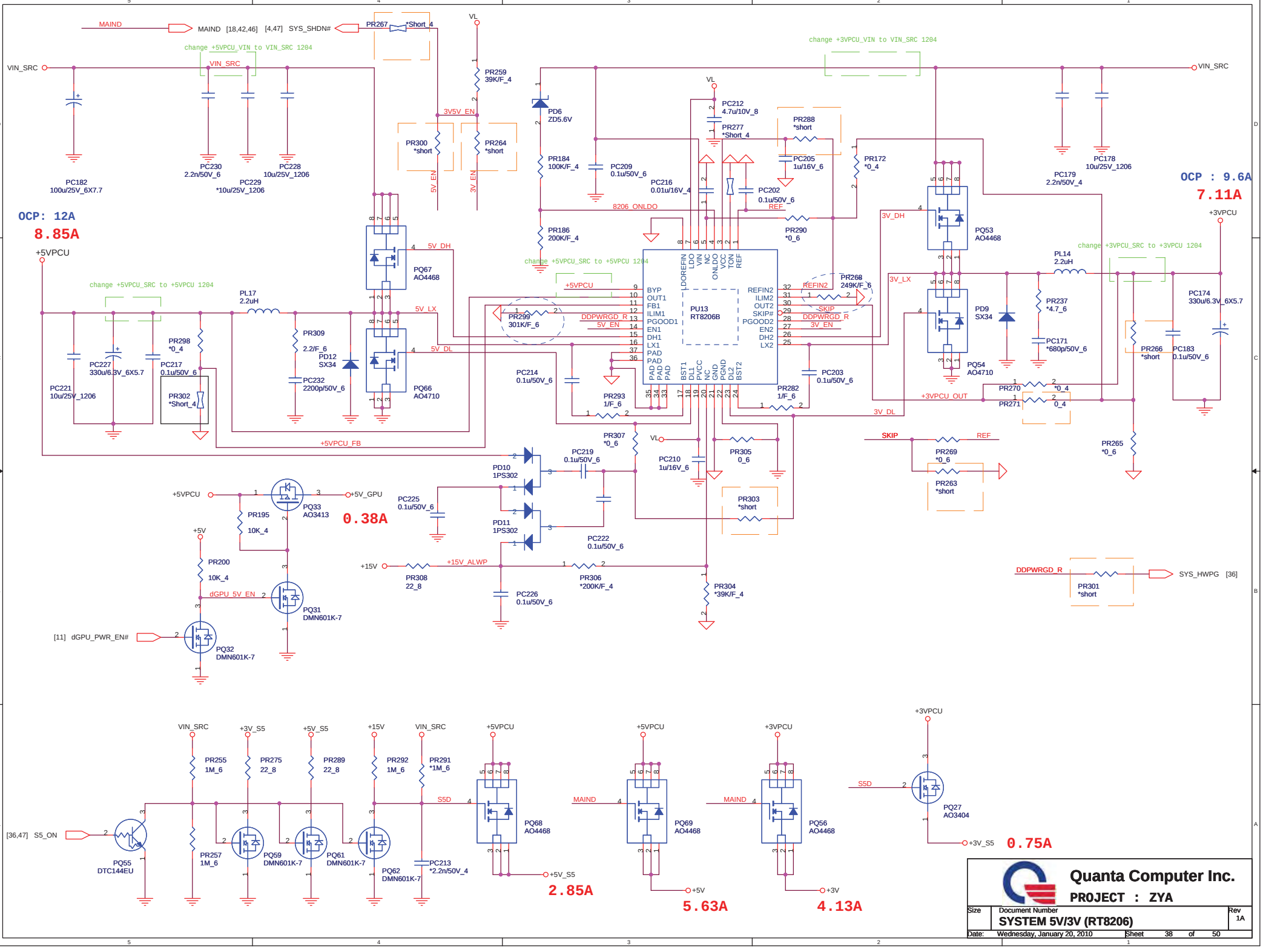
CIR



Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A
Date: Wednesday, January 20, 2010	Sheet 36 of 50	

Quanta Computer Inc.
PROJECT : ZYA


PJ2
20288-044L
PC246
22u/25V_1210
PC245
22u/25V_1210
PC1
2200p/50V_6
PC2
0.1u/50V_6
VA
PL2
HI0805R800R-00_8
PL1
HI0805R800R-00_8
VA1
PD1
SW1010CPT
PC3
0.1u/50V_6
PC4
0.1u/50V_6
PD3
SBR1045SP5-13
PD2
SMAJ20A
VA2
PC9
0.1u/50V_6
PR12
220K/F_6
PR14
220K/F_6
PQ2
IMD2AT108
PQ13
FDD6685
PR26
0.01/F_7520
VIN_SRC
CSIP_1
PC239
*0.1u/50V_6
PC240
0.1u/50V_6
PC241
*0.1u/50V_6
PC242
0.1u/50V_6
PC243
*0.1u/50V_6
PC244
0.1u/50V_6
Add for EMI with ver B
PR15
*Short_6
D/C#
[36]
PQ14
FDD6685
PC10
0.1u/50V_6
PC11
2200p/50V_6
PR28
33K_6
PR44
10K_6
PQ17
DMN601K-7
REV : C Add PC246 & PC245
Close to PJ2
PR34
10/F_6
PR35
10/F_6
PC25
0.1u/50V_6
PC17
1u/16V_6
PR50
4.7_6
ISL88731_VDDP
PC29
1u/16V_6
PD4
*RB500V-40
PC15
0.1u/50V_8
PC119
10u/25V_1206
PC116
2200p/50V_6
+3VPCU
PC40
0.1u/50V_6
PR74
100K/F_6
[36] ACIN
[36] MBDATA
[36] MBCLK
PR46
49.9/F_6
DCIN
PC23
0.1u/50V_6
PR49
82.5K/F_6
88731ACSET
PR47
22K/F_6
PU2
ISL88731A
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
ICM
NC
GND
PR33
2.7_6
88731B_2
88731B_1
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
PR57
10/F_6
CSOP_1
PC35
0.1u/50V_6
CSON
BAT-V
PR60
10/F_6
PR63
*short
PR67
100_4
PR65
2.21K/F_6
PC37
0.01u/50V_6
PC32
*1u/16V_6
PC33
0.01u/50V_6
PC36
*0.01u/50V_6
ICMNT
ICMNT [36]
ISL88731 thermal pad
tie to Pin12
PQ34
AO4468
PQ35
AO4710
PL6
6.8uH
0.01_3720
PR206
PR207
2.2/F_6
PC120
1500p/50V_6
PC27
0.01u/50V_6
PC28
2200p/50V_6
PC117
10u/25V_1206
PC118
10u/25V_1206
BAT-V
CSOP_1
PC5
0.1u/50V_6
PC8
100p/50V_6
PL3
HI0805R800R-00_8
PL4
HI0805R800R-00_8
MBAT+
BAT-V
Batt_Conn
PJ1
1012 change
symbol
TEMP_MBAT_C
PR2
100_4
TEMP_MBAT [36]
PR11
100K/F_6
+3VPCU
PC6
47p/50V_6
PC7
47p/50V_6
PR5
*Short_6
PR3
100_4
PR4
100_4
MBCLK [36]
MBDATA [36]
PU1
CM1293A-04SO
CH1
CH4
VN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT_C
Add ESD diode base on EC FAE suggestion
VIN_SRC
VIN
PQ15
AOL1413
add PC234 1204
PC234
1U/25V_6
PR29
150K_6
change to 150K 1204
PR42
39K_6
change to 150K 1204
[36] VIN_ON
PQ16
DMN601K-7
Quanta Computer Inc.
PROJECT : ZYA
Size
Document Number
CHARGER (ISL88731)
Rev
1A
Date: Wednesday, January 20, 2010
Sheet 37 of 50


MAIND
MAIND [18,42,46] [4,47] SYS_SHDN#
PR267 *Short_4
change +5VPCU_VIN to VIN_SRC 1204
VIN_SRC
VL
PR259 39K/F_4
3V5V_EN
PR300 *short
PR264 *short
5V_EN
3V_EN
PD6 ZD5.6V
PR184 100K/F_4
PC209 0.1u/50V_6
PC216 0.01u/16V_4
PC212 4.7u/10V_8
PR277 *Short_4
PR288 *short
PC205 1u/16V_6
PC202 0.1u/50V_6
PR172 *0_4
PC182 100u/25V_6X7.7
PC230 2.2n/50V_6
PC229 *10u/25V_1206
PC228 10u/25V_1206
PC179 2.2n/50V_4
PC178 10u/25V_1206
OCP: 12A
8.85A
OCP : 9.6A
7.11A
8206_ONLDO
REF
PR186 200K/F_4
PR290 *0_6
+5VPCU
+3VPCU
change +5VPCU_SRC to +5VPCU 1204
change +3VPCU_SRC to +3VPCU 1204
PQ67 AO4468
5V_DH
3V_DH
PQ53 AO4468
PL14 2.2uH
PL17 2.2uH
5V_LX
3V_LX
PR299 301K/F_6
DDPWRGD_R
5V_EN
3V_EN
PU13 RT8206B
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
DOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
DLL
PVCC
NC
GND
PGD
DL2
BST2
PR268 249K/F_6
SKIP
PR298 *0_4
PR309 2.2/F_6
PD12 SX34
PC227 330u/6.3V_6X5.7
PC217 0.1u/50V_6
PC221 10u/25V_1206
PR302 *Short_4
PC232 2200p/50V_6
PQ66 AO4710
PC214 0.1u/50V_6
PR293 1/F_6
PC203 0.1u/50V_6
PR282 1/F_6
PQ54 AO4710
PD9 SX34
PR237 *4.7_6
PC171 *680p/50V_6
PC174 330u/6.3V_6X5.7
PR266 *short
PC183 0.1u/50V_6
PR270 *0_4
PR271 0_4
+3VPCU_OUT
3V_DL
+5VPCU_FB
PR307 *0_6
VL
PR305 0_6
PC210 1u/16V_6
PC219 0.1u/50V_6
PD10 1PS302
PD11 1PS302
PC225 0.1u/50V_6
PC222 0.1u/50V_6
PR303 *short
SKIP
REF
PR269 *0_6
PR263 *short
PR265 *0_6
+5VPCU
PQ33 AO3413
+5V_GPU
0.38A
PR195 10K_4
+5V
PR200 10K_4
dGPU_5V_EN
PQ31 DMN601K-7
[11] dGPU_PWR_EN#
PQ32 DMN601K-7
+15V
+15V_ALWP
PR308 22_8
PR306 *200K/F_4
PR304 *39K/F_4
PC226 0.1u/50V_6
DDPWRGD_R
SYS_HWPG [36]
PR301 *short
VIN_SRC
+3V_S5
+5V_S5
+15V
PR255 1M_6
PR275 22_8
PR289 22_8
PR292 1M_6
PR291 *1M_6
S5D
[36,47] S5_ON
PQ55 DTC144EU
PR257 1M_6
PQ59 DMN601K-7
PQ61 DMN601K-7
PQ62 DMN601K-7
PC213 *2.2n/50V_4
PQ68 AO4468
+5V_S5
2.85A
MAIND
PQ69 AO4468
+5V
5.63A
PQ56 AO4468
+3V
4.13A
PQ27 AO3404
+3V_S5
0.75A
Quanta Computer Inc.
PROJECT : ZYA
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1A
Date: Wednesday, January 20, 2010
Sheet 38 of 50

[PWM]

VID 1.2875V

+3VPCU PR145 *0_4 H_VID0
PR147 *0_4 H_VID1
PR158 *0_4 H_VID2
PR161 *0_4 H_VID3
+3VPCU PR164 *0_4 H_VID4
PR163 *0_4 H_VID5
PR167 *0_4 H_VID6

VR_PWRGD_CK505# [3]
DELAY_VR_PWRGOOD [4,8]

change VCC_CORE_SRC1 to VIN

VIN
PC191 0.1u/50V_6
PC180 10u/25V_1206
PC185 10u/25V_1206
PC166 100U/25V

PQ52 AOL1448
62882_UG1
62882_PH1
PQ51 AOL1718
PQ48 AOL1718
62882_LG1A
PR112 2.2/F_6
PC65 2200P/50V_6
PL12 0.36uH
20A
+VCC_CORE
PC63 330u/2V_7343
PR108 *short
PR105 *short
62882_LG1B

VIN +3V
PR137 *short
PR173 1.91K/F_4
PR175 1.91K/F_4
+5V_S5
PR159 10_6
PC88 0.22u/25V_6
PR148 0_8
PC92 1u/6.3V_4

Rev: B checnge footprint for SMT request

+3V
PR181 *499/F_4
[6] H_PSI#
PR180 10K/F_4
PR183 147K/F_6
[4] H_PROCHOT#
Close to Phase 1 Inductor
PR191 *470K_4_NTC
PR182 *4.02K/F_4
PC102 *0.01u/16_4

PU8 ISL62882
PAD VDD VIN CLK_EN# PGOOD
UGATE1 BOOT1 PHASE1 LGATE1a LGATE1b VSSP1 ISEN1
PR131 2.2_6
PC81 0.22u/25V_6

62882_ISEN1 PR136 10K/F_4
62882_VSUM+ PR130 3.65K/F_4 62882_ISEN_1
62882_VSUM- PR157 1/F_4 62882_ISEN_2
62882_ISEN2 PR146 10K/F_4

change VCC_CORE_SRC1 to VIN
change VCC_CORE_SRC2 to VIN
VIN
PC167 0.1u/50V_6
PC78 10u/25V_1206
PC71 10u/25V_1206
PC165 100U/25V

[6] H_VID0 H_VID0 VID0
[6] H_VID1 H_VID1 VID1
[6] H_VID2 H_VID2 VID2
[6] H_VID3 H_VID3 VID3
[6] H_VID4 H_VID4 VID4
[6] H_VID5 H_VID5 VID5
[6] H_VID6 H_VID6 VID6
[36] VRON VR_ON
[6] H_DPRSLPVR DPRSLPVR DPRSLPVR
PR166 100K/F_4
PR171 499/F_4

PC99 0.22u/10V_4
62882_VSUM-
VCCP PR135 Short_4 +5V_S5
PC85 1u/6.3V_4
PC84 1u/6.3V_4
62882_UG2
62882_PH2
UGATE2 BOOT2 PHASE2 LGATE2 VSSP2 ISEN2
PR134 2.2_6
PC83 0.22u/25V_6
62882_LG2
PQ50 AOL1448
PQ49 AOL1718
PQ47 AOL1718
PR111 2.2/F_6
PC64 2200P/50V_6
PL11 0.36uH
20A
+VCC_CORE
PC62 330u/2V_7343
PR109 *short
PR106 *short

62882_FB
FB FB2 COMP VW
PR190 *10K/F_4
PC100 22P/50V_4
PR185 412K/F_4
PC107 150P/50V_4
62882_COMP
PC103 10P/50V_4
PR178 8.06K/F_4
PC104 1000P/50V_4

PC98 0.22u/10V_4
62882_VSUM-
IMON I_MON [6]
PR127 9.76K/F_4
PC82 0.033u/16_4
VSSSENSE
1019 change 9.76k ohm and 33PF

62882_ISEN2 PR129 10K/F_4
62882_VSUM+ PR126 3.65K/F_4 62882_ISEN_3
62882_VSUM- PR123 1/F_4 62882_ISEN_4
62882_ISEN1 PR122 10K/F_4

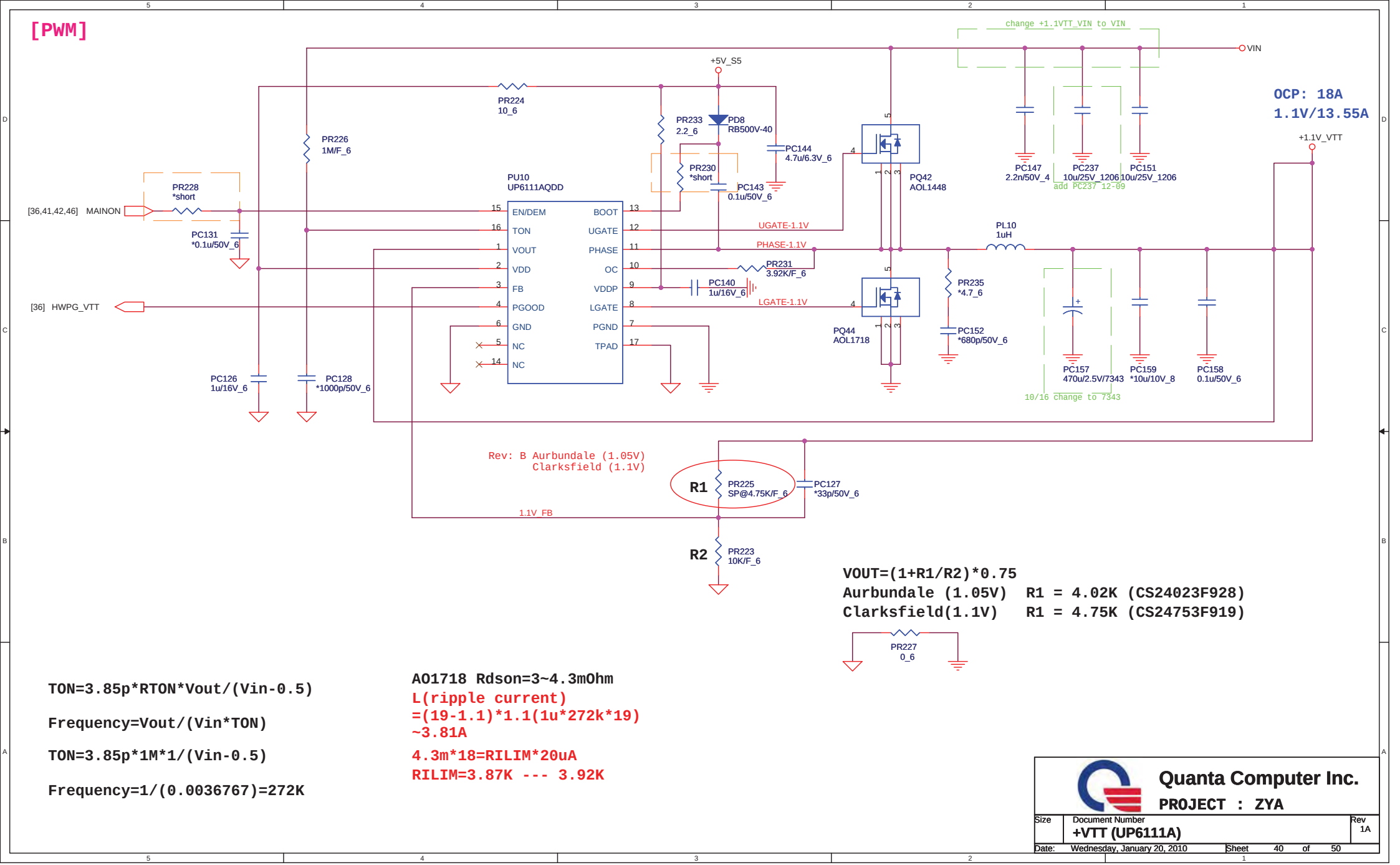
VSEN RTN ISUM- ISUM+
PR192 2.8K/F_4
PR193 562/F_4
PC108 390P/50V_4

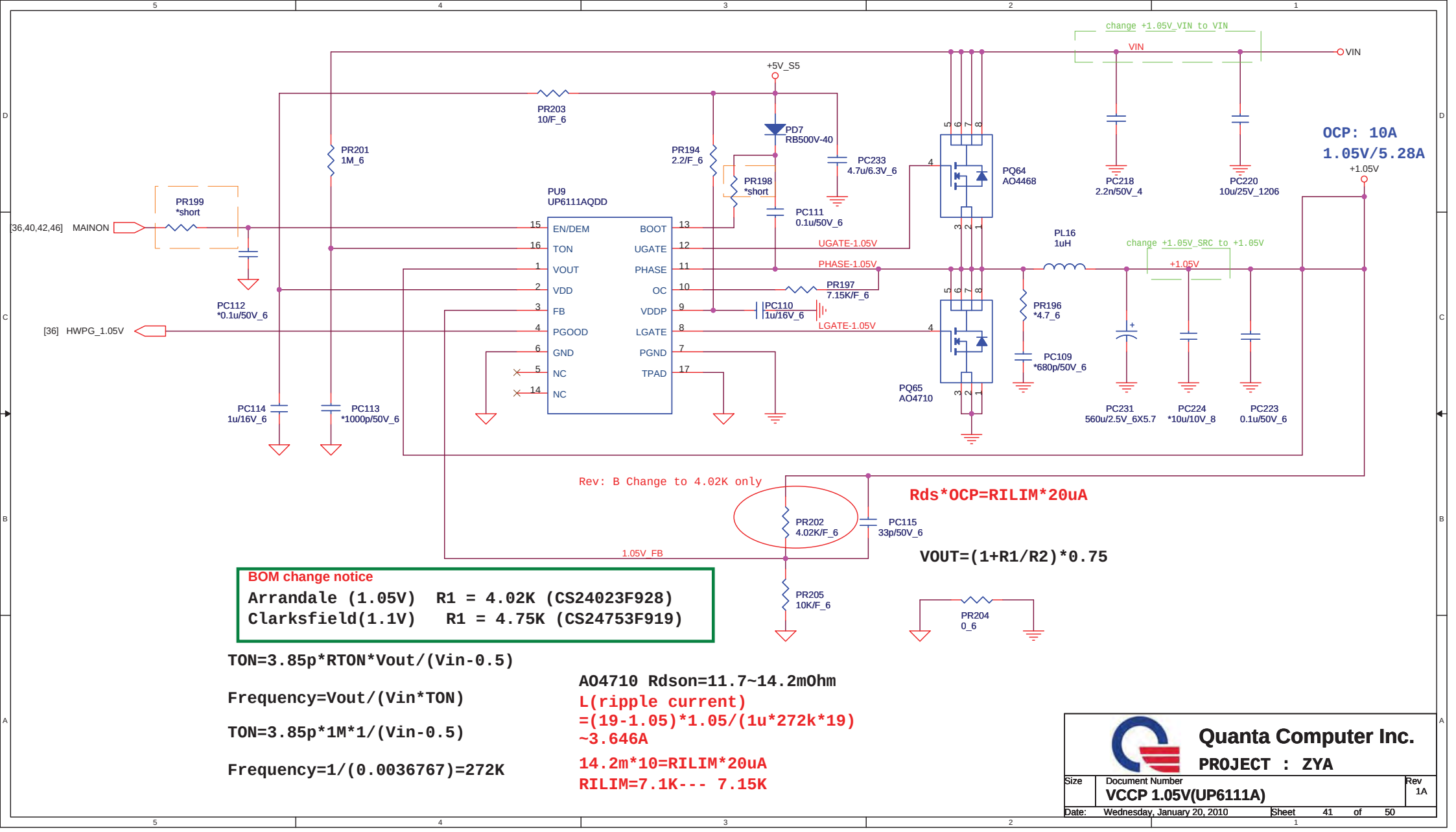
PC94 0.22u/10V_6
PC93 0.068u/25V_6
62882_VSUM+
PR168 82.5/F_4
PC95
PR169 11K/F_4
PR133 2.61K/F_4
PR107 10K_6_NTC
Panasonic
ERT-J1VR103J
PC96 0.01u/16_4
2700P/50V_4
PR170 *short
62882_VSUM-
PR174 1.24K/F_4
PC90 0.1u/10V_4
Close to Phase 1 Inductor
PC97 *1000P/50V_4
PR176 *100/F_4
Load Line setting to 1.9mV/A

+VCC_CORE PR189 *27.4_4 62882_VSEN
PC106 330P/50V_4
[6] VCCSENSE PR188 *short
[6] VSSSENSE PR179 *short
Parallel
PC101 330P/50V_4
PC105 1000P/50V_4
PR187 *27.4_4
62882_RTN

Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	CPU Core (ISL62882)	1A
Date: Wednesday, January 20, 2010	Sheet 39 of 50	


[PWM]
change +1.1VTT_VIN to VIN
VIN
+5V_S5
PR224
10_6
PR226
1M/F_6
PR233
2.2_6
PD8
RB500V-40
PC144
4.7u/6.3V_6
PR230
*short
PC143
0.1u/50V_6
PU10
UP6111AQDD
PQ42
AOL1448
PC147
2.2n/50V_4
PC237
10u/25V_1206
PC151
10u/25V_1206
add PC237 12-09
OCP: 18A
1.1V/13.55A
+1.1V_VTT
PR228
*short
[36,41,42,46] MAINON
PC131
*0.1u/50V_6
EN/DEM
TON
VOUT
VDD
FB
PGOOD
GND
NC
NC
BOOT
UGATE
PHASE
OC
VDDP
LGATE
PGND
TPAD
UGATE-1.1V
PHASE-1.1V
PR231
3.92K/F_6
PC140
1u/16V_6
LGATE-1.1V
PL10
1uH
PR235
*4.7_6
PQ44
AOL1718
PC152
*680p/50V_6
[36] HWPG_VTT
PC126
1u/16V_6
PC128
*1000p/50V_6
PC157
470u/2.5V/7343
PC159
*10u/10V_8
PC158
0.1u/50V_6
10/16 change to 7343
Rev: B Aurbundale (1.05V)
Clarksfield (1.1V)
R1
PR225
SP@4.75K/F_6
PC127
*33p/50V_6
1.1V_FB
R2
PR223
10K/F_6
VOUT=(1+R1/R2)*0.75
Aurbundale (1.05V) R1 = 4.02K (CS24023F928)
Clarksfield(1.1V) R1 = 4.75K (CS24753F919)
PR227
0_6
TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K
AO1718 Rdson=3~4.3mOhm
L(ripple current)
=(19-1.1)*1.1(1u*272k*19)
~3.81A
4.3m*18=RILIM*20uA
RILIM=3.87K --- 3.92K
Quanta Computer Inc.
PROJECT : ZYA
Size
Document Number
+VTT (UP6111A)
Rev
1A
Date: Wednesday, January 20, 2010
Sheet 40 of 50



BOM change notice

Arrandale (1.05V) R1 = 4.02K (CS24023F928)
Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

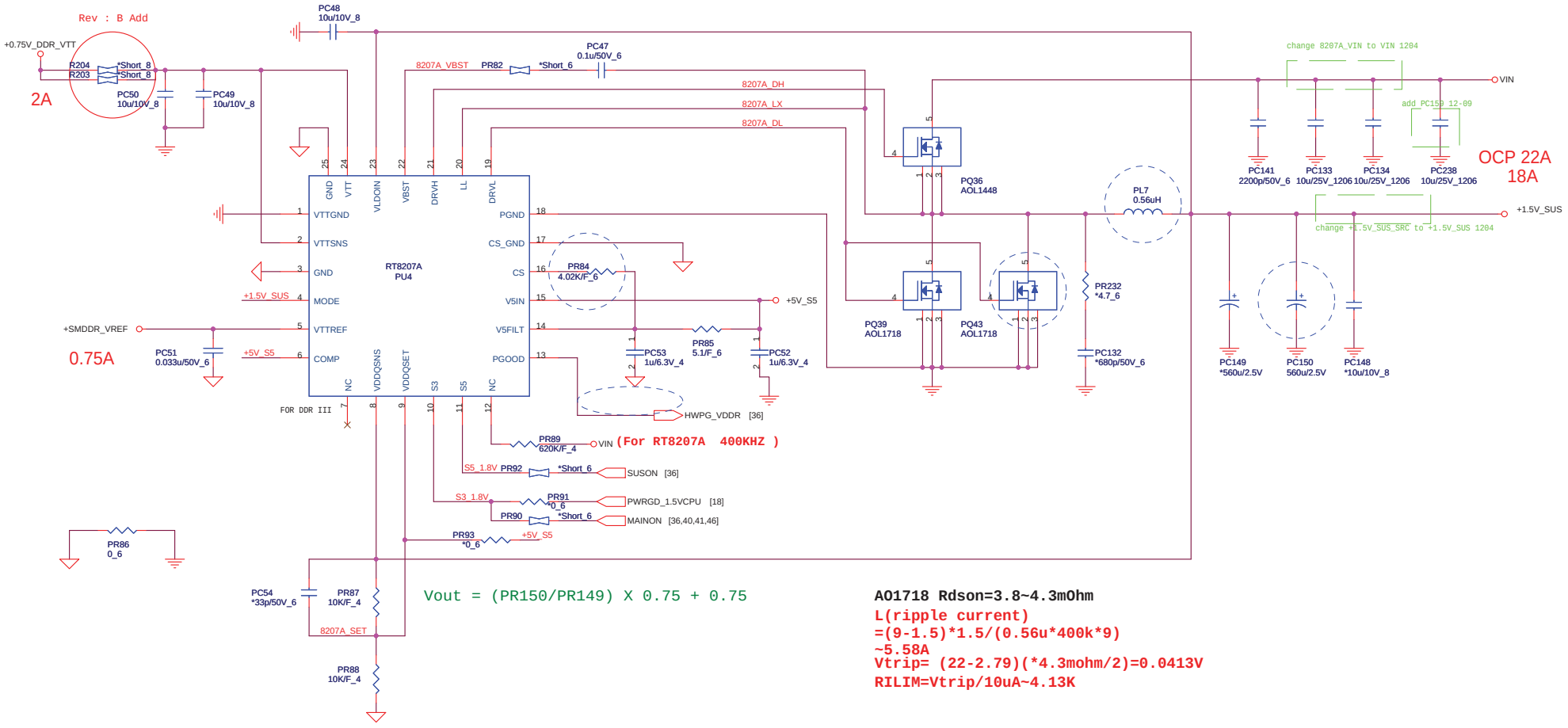
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

Quanta Computer Inc.
PROJECT : ZYA

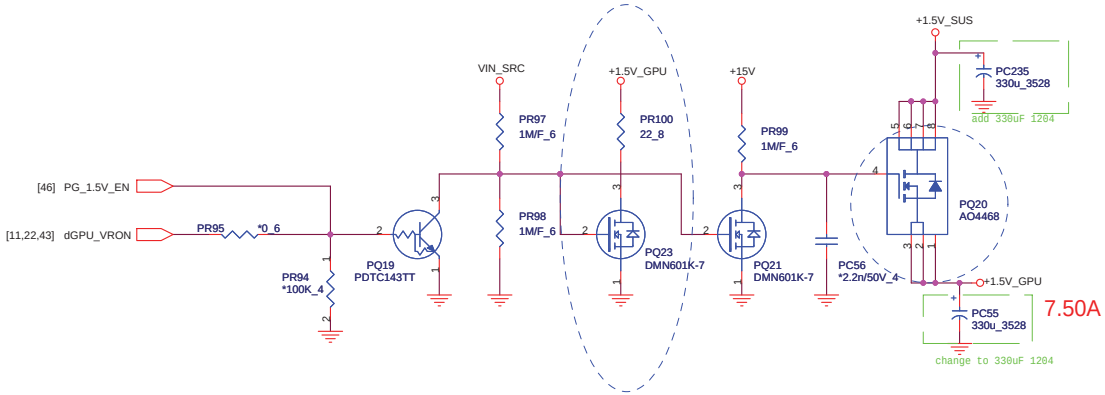
Size	Document Number	Rev
	VCCP 1.05V(UP6111A)	1A
Date: Wednesday, January 20, 2010	Sheet 41 of 50	

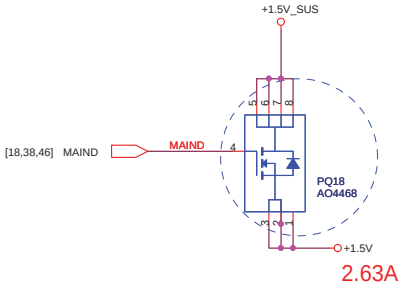
[PWM]



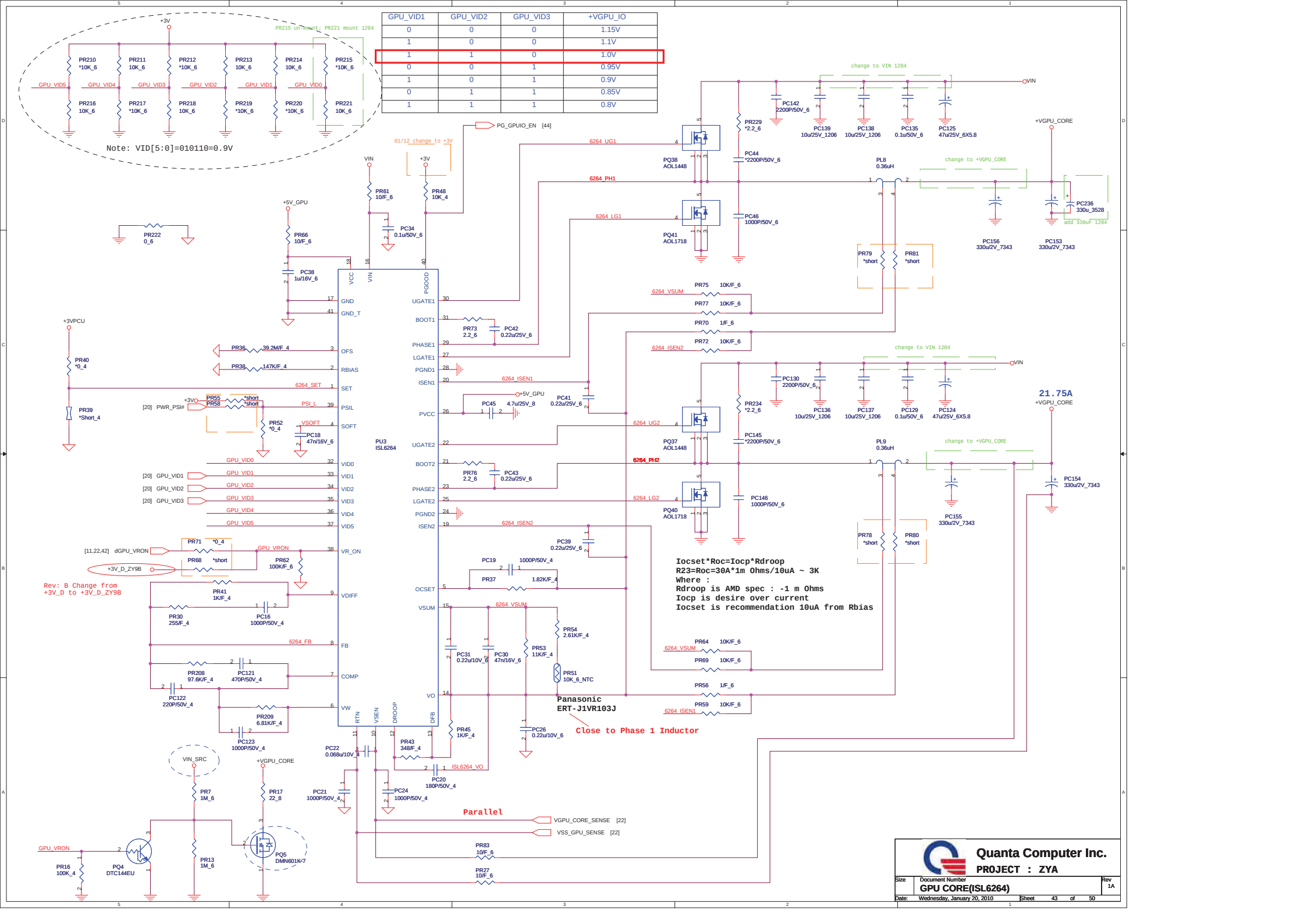
Vout = (PR150/PR149) X 0.75 + 0.75

AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(9-1.5)*1.5/(0.56u*400k*9)
~5.58A
Vtrip= (22-2.79)(*4.3mohm/2)=0.0413V
RILIM=Vtrip/10uA~4.13K





Quanta Computer Inc.		
PROJECT : ZYA		
Size	Document Number: DDR 1.5V(TPS51116)	Rev: 1A
Date: Wednesday, January 20, 2010	Sheet 42 of 50	

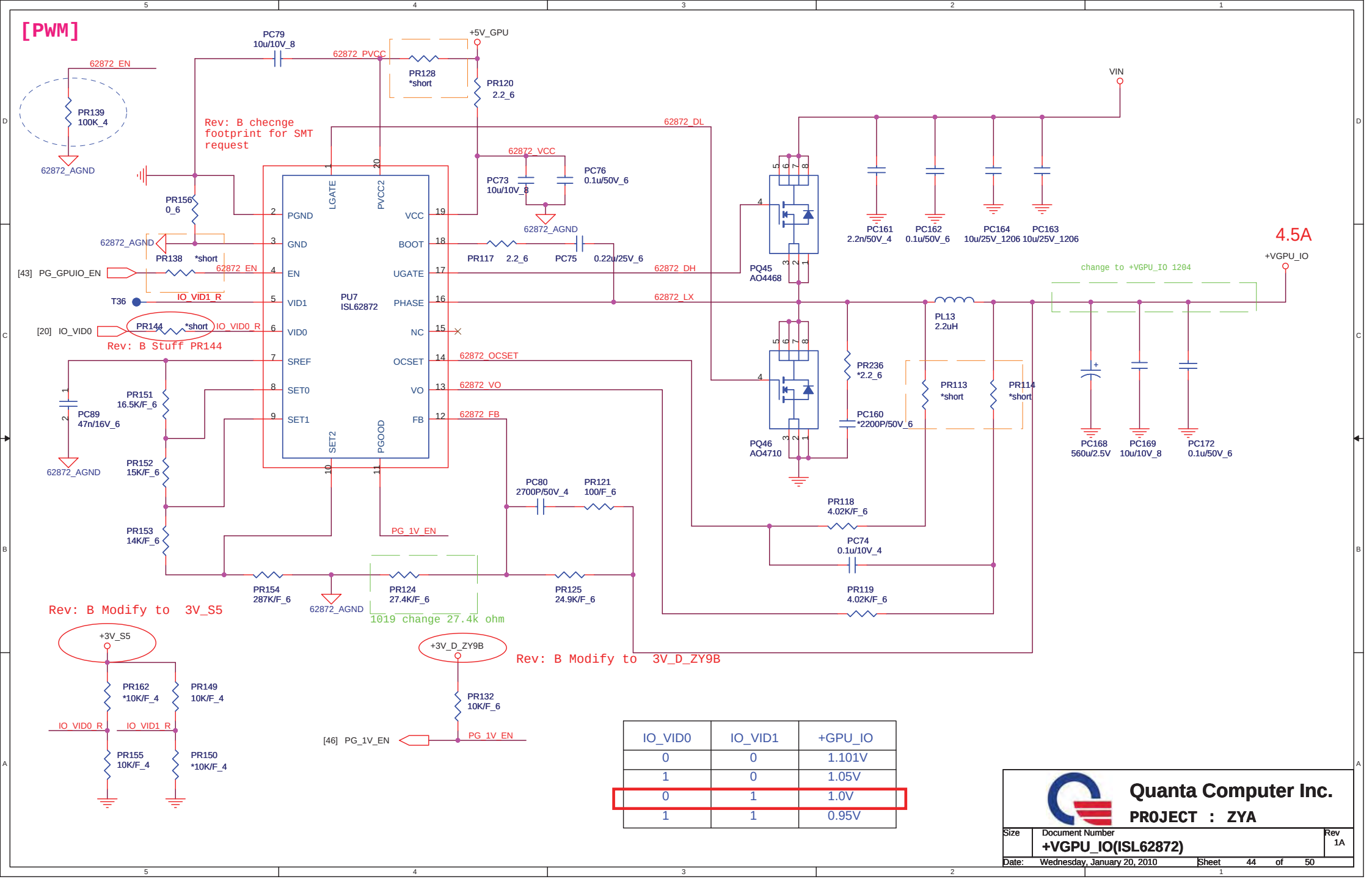


GPU_VID1	GPU_VID2	GPU_VID3	+VGPU_IO
0	0	0	1.15V
1	0	0	1.1V
1	1	0	1.0V
0	0	1	0.95V
1	0	1	0.9V
0	1	1	0.85V
1	1	1	0.8V

Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	GPU CORE(ISL6264)	1A

Date: Wednesday, January 20, 2010 Sheet 43 of 50



IO_VID0	IO_VID1	+GPU_IO
0	0	1.101V
1	0	1.05V
0	1	1.0V
1	1	0.95V

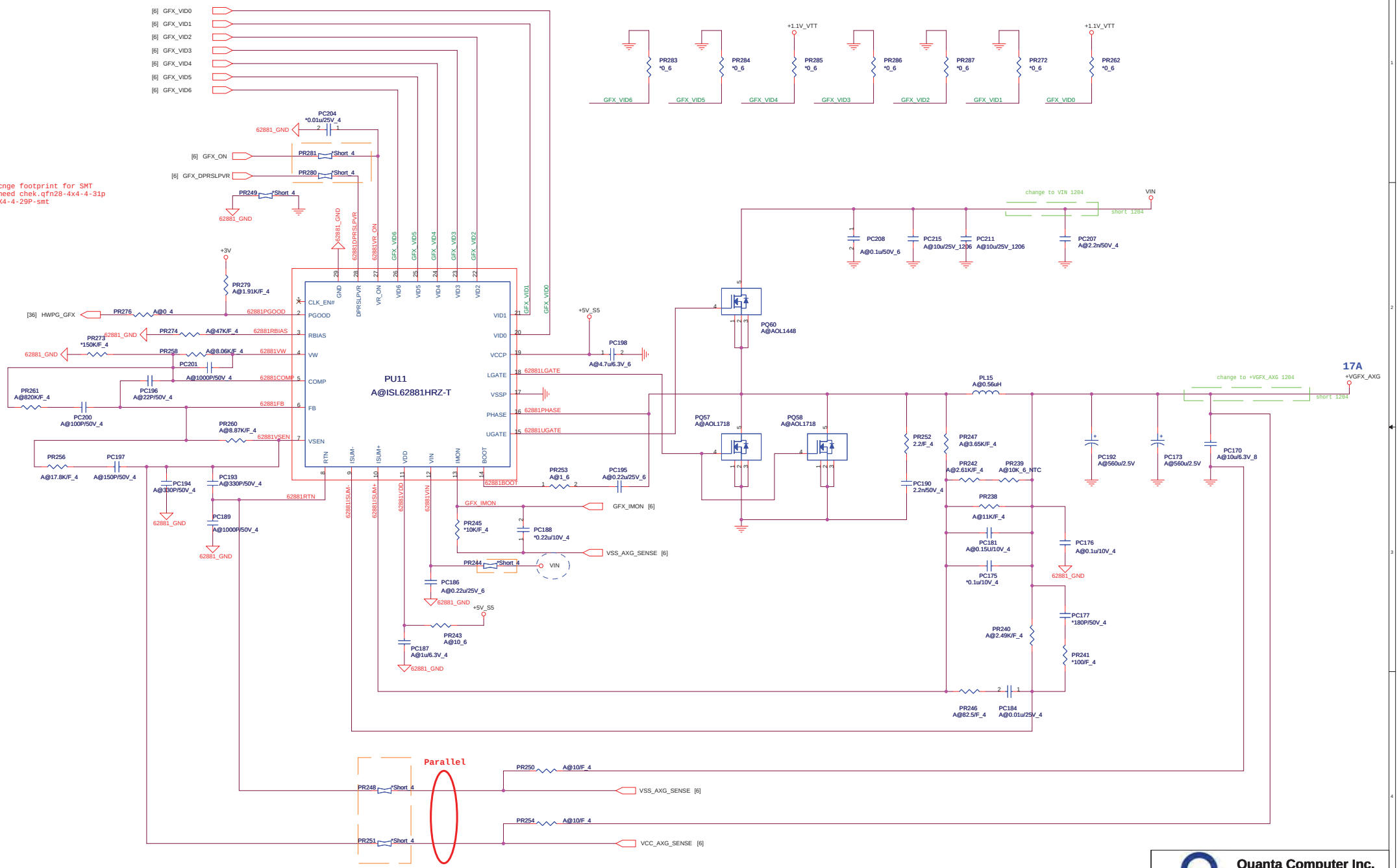
Quanta Computer Inc.

PROJECT : ZYA

Size	Document Number	Rev
	+VGPU_IO(ISL62872)	1A
Date: Wednesday, January 20, 2010	Sheet 44 of 50	

Int_VGA [PWM]

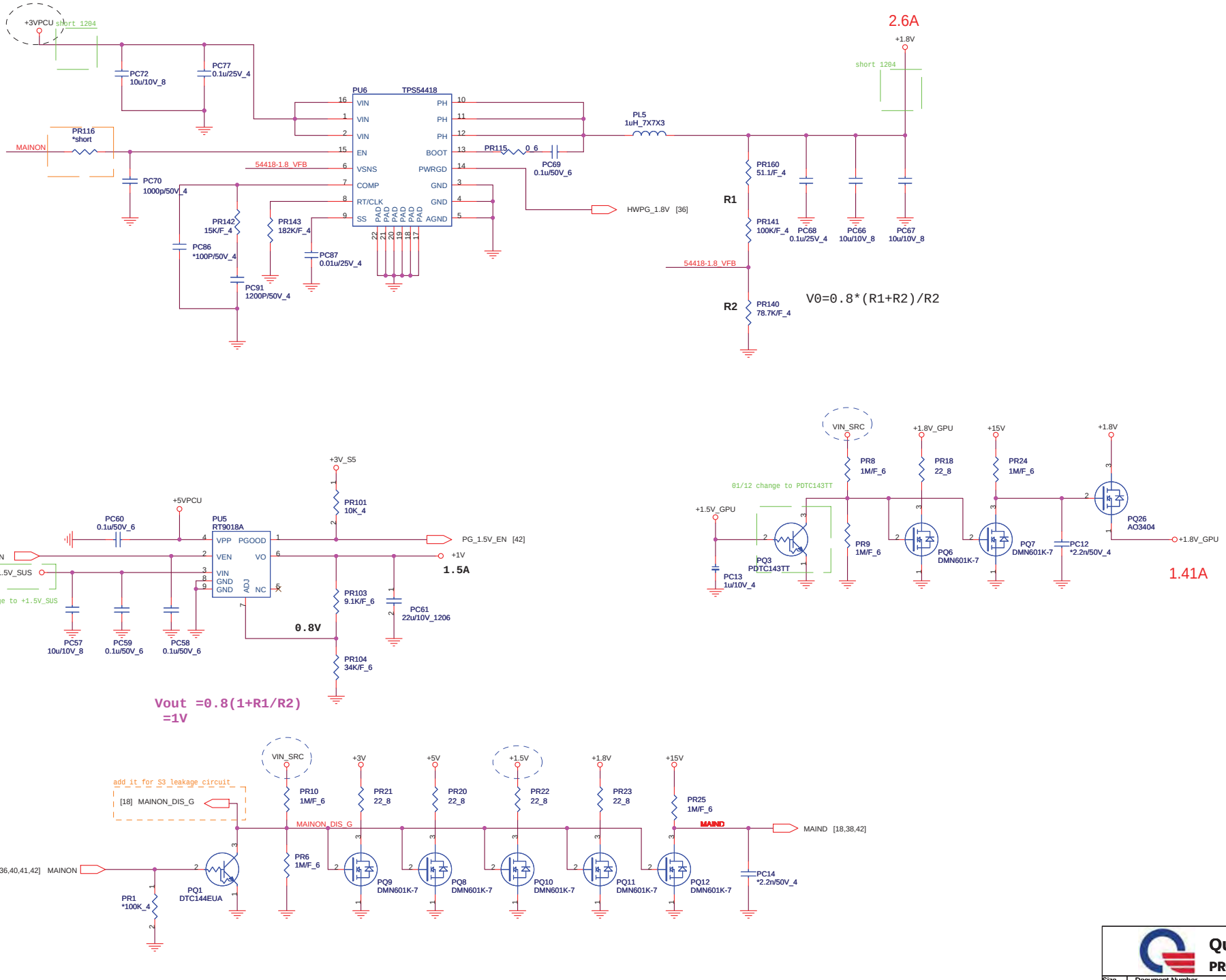
Rev: B checnge footprint for SMT
request , need chek.qfn28-4x4-4-31p
to QFN28-4X4-4-29P-smt



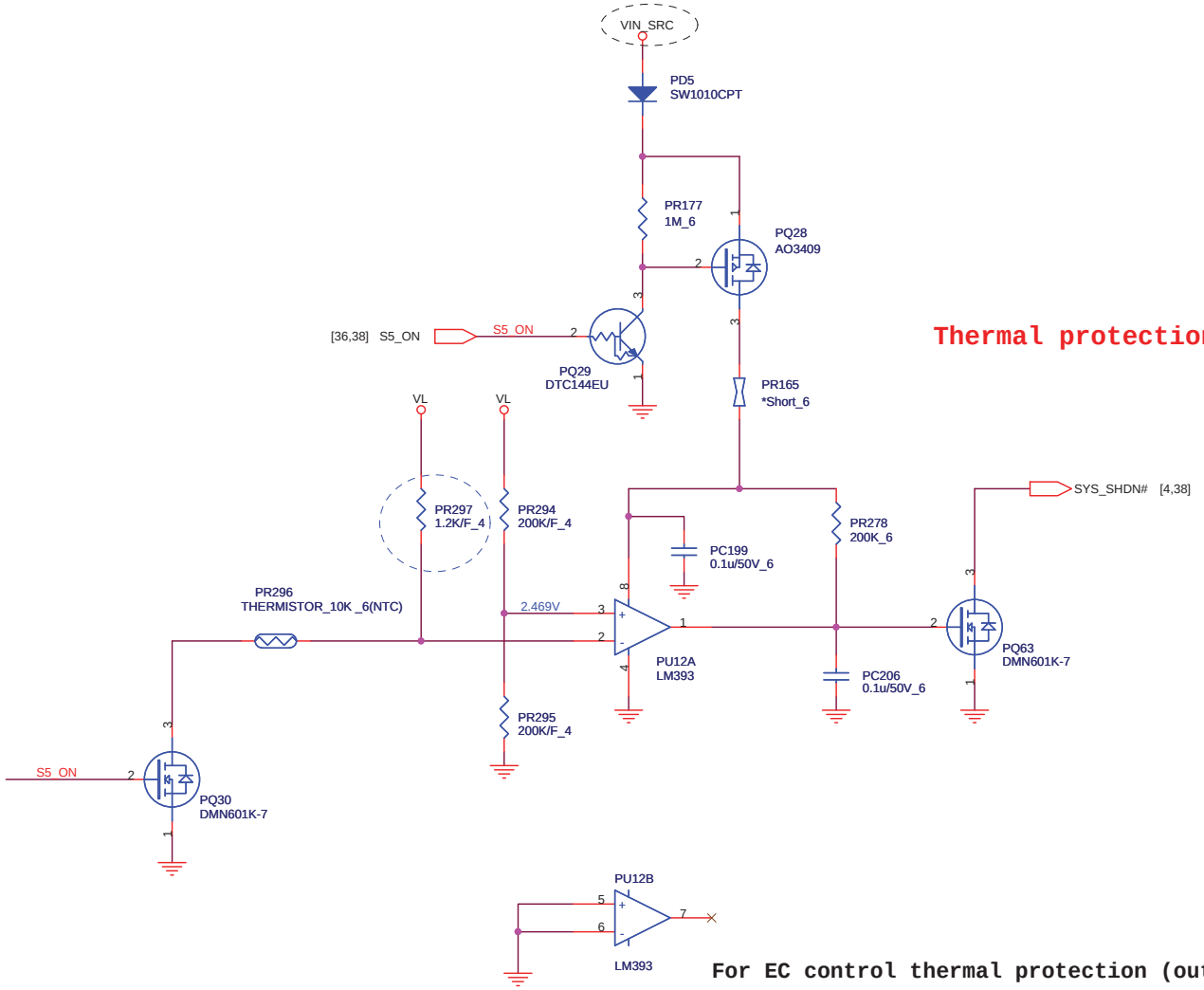
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	1A
Date: Wednesday, January 20, 2010	Sheet 45 of 50	



Quanta Computer Inc.		
PROJECT : ZYA		
Size	Document Number: Discharge/+1.8V/+1V	Rev: 1A
Date: Wednesday, January 20, 2010	Sheet 46 of 50	

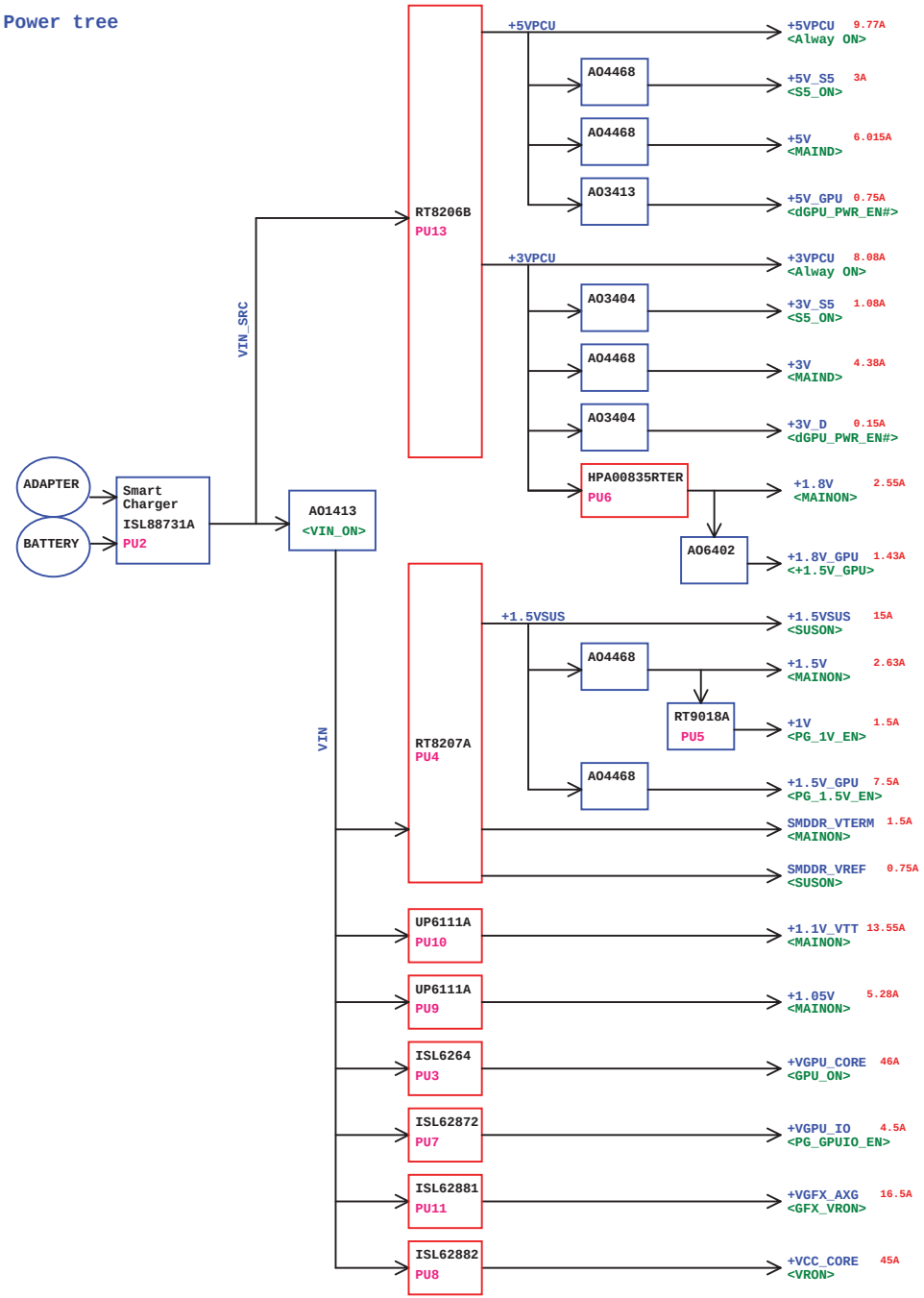


Thermal protection

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.		
PROJECT : ZYA		
Size	Document Number: Thermal protect	Rev: 1A
Date: Wednesday, January 20, 2010	Sheet 47 of 50	

ZYB Power tree



PROJECT : ZYB & ZYBA
Quanta Computer Inc.

Size	Document Number	Rev
	ZYA/B Power tree	1A
Date: Wednesday, January 20, 2010	Sheet 48 of 49	

CHANGE LIST

Model	REV	CHANGE LIST
ZY9B MB	1A	FIRST RELEASED
	2A	see below
	3A	see below
	3C	

1A

FIRST RELEASED

2A

Page 3 : U20 Change pin define
Page 4 : Not stuff R481
Page 4 : Add XDP_DBRST# contact CPU to PCH
Page 6 : Short , Remove R130 & R128
Page 9 : No stuff R715
Page 10 : Add R740 for TV funation
Page 10 : Add Y4(25 MHZ) for internal VGA & C832=27pF,C833=22pF
Page 11 : R318 Change PU from +3V_S5 to +3V for leakage
Page 18 : For ZYA no support M3, No stuff R472 & R36 , stuff R473 ,R474 ,R43 & R44
Page 18 : No stuff PR102 , PQ24 ,PR110 & PQ25 for leakage
Page 18 : Remove R131 & R123 for leakage
Page 18 : Modify DRAM_RST for AMD request
Page 27 : Reverse LVDS clock input of PIN define for design error
Page 28 : No stuff R582 for leakage
Page 28 : HDMI reserve 100 ohm parallel resister for EMI
Page 29 : Mpdify CN23 of symbol
Page 30 : Short , Remove R7
Page 30 : Remove Q1 , R4 ,R1 & R2
Page 31 : Add C490 & C487 for EMI
Page 31 : Change L22 & L23 to 68 ohm bead CX08T680009 & from 0402 to 0603 for EMI
Page 32 : Change AMP for buyer request
Page 32 : No stuff R428 amd PU to +3V
Page 32 : Change Audio conn. (CN24 & CN25) to normal open
Page 32 : Change PIN define of DMIC(CN8)
Page 32 : Stuff C320 & C319 to 10P & footprint from 0805 to 0402 for EMI
Page 32 : L35 ,L37 ,L42 ,L43 Change to SBK160808T-121Y/120ohm_6 & C616 ,C613 ,C604 ,C599 Change to 1000p for EMI
Page 32 : L38 ,L39 ,L40 ,L41 Change to SBK160808T-121Y/120ohm_6 & C612 ,C611 ,C610 ,C609 Change to 1000p for EMI
Page 33 : Change R726 to 0 ohm for card reader funation
Page 33 : Remove the U46 circuit (LDO)
Page 33 : Short 0 ohm for cost down
Page 34 : Add R349 (Change to EC control) & reserve R350
Page 34 : Add C554 & C554 for EMI
Page 34 : Add L75 ,L76 & L77 for EMI
Page 34 : Stuff L63 & L62 & not stuff R620 ,R621 ,R608 & R609 for EMI
Page 35 : (1) Reserve R123 & PU to +3VPCU (2)Cahnge Q5.3 PU from +3VPCU to +3V_S5
Page 35 : Change design for bluetooth
Page 35 : CN15 change pin define
Page 35 : Add L73 ,L74 , C551 & C550 for EMI
Page 35 : Stuff C637 for EMI
Page 35 : Change to short pad
Page 36 : No stuff SW1
Page 36 : U5.80 Change to WLAN_LED
Page 36 : R61 & R63 Change PU from +3V to +3V_S5 for leakage
Page 36 : Stuff C89 & C94 for EMI
Page 39 : PU8 change footprint for SMT request
Page 40 : PR225 (+1.1V_VTT) chage to SP@(Aurbundale (1.05V) ,Clarksfield (1.1V))
Page 41 : PR202 Change to 4.02K ohm
Page 43 : PR68 Change PU from +3V_D to +3V_D_ZY9B for VGA Sequenc
Page 44 : PU7 change footprint for SMT request
Page 44 : Stuff PR144
Page 43 : PR149 Change PU from +3V_D to +3V_S5
Page 44 : PR132 Change PU from +3V_D to +3V_D_ZY9B
Page 45 : PU11 change footprint for SMT request

3A

All Page :Change Location: R395 ,R734 ,R201 ,R702 ,R689 ,R708 ,R640 ,R646 ,R328 ,R661 ,R323 ,R372 ,R389 ,R456 ,R320 ,R636 ,R300 ,R333 ,R332 ,R662 ,R652 ,R306 ,R304 ,R15 ,R35 ,R220 ,R231 ,R106 ,R49 ,L4 ,L48 ,L49 ,L45 ,R69 ,R70 ,R173 ,R166 ,R170 ,R177 ,R176 ,R557 ,R224 ,R5 ,R6 ,R8 ,R9 ,R10 ,R11 ,R12 ,R351 ,R292 ,L21 ,R635 ,R738 ,R726 ,R736 ,R733 ,,R293 ,R459 ,R460 ,R461 ,R438 ,R435 ,R455 ,R448 ,R186 ,R187 ,R246 ,R258 ,R263 ,R260 ,R350 , R17 ,R26 ,R25 ,R184 ,R99 ,R128 ,R88 ,R81 ,R144 ,R148 ,R204 ,R203 to short pad

Page 27 : Add fuse Location : F1 for safety requirement
Page 27 : circuitry update Location : Q34 & R126 for leakage current
Page 28 : Add fuse Location : F2 for safety requirement
Page 28 : circuitry update Location : Q14 & Q17 , Add R128 & R130 for capacitance’s value over 50pF
Page 28 : HOLE4 contact to GND
Page 29 : Remove 0 ohm Location : R314 ,R336 for cost down.
Page 30 : Remove Q100 ,Q101 ,R1004 ,R1005
Page 30 : C622 change from 1u_0402 to 4.7u _0603
Page 30 : Add D27 for ESD
Page 33 : Remove 0 ohm Location : R644 ,R639 ,R633 ,R630 f, R349 for cost down.
Page 34 : Add D28 & D29 for ESD

3C

MODEL	ZY9B	
	FROM	To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
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EC GPIO Setting

Pin Name	Net Name	Setting	Description
GPIO1	ACIN	GPI	EC Detect AC Adapter State
GPIO3	NBSWON#	GPI	Pwer switch in
GPIO4/AD5	DIGVOL_DN	GPI	Digital Volume wheel.
GPIO5/AD4	DIGVOL_UP	GPI	Digital Volume wheel.
GPIO6	LID591#	GPI	Reserved for Lid function
GPIO7	SUSB#	GPI	S.B sleep S3 pin
GPIO10/LPCPD#	ARCADE_KEY	GPI	Arcade Button switch
GPIO11/CLKRUN#	CLKRUN#	O	Clock Run
GPIO12/PSDAT3	CR_CPPE#SD	GPI	OZ888 Wake indicator
GPIO13/C_PWM	PWRLED#	O	Power on LED drive
GPIO14/TB1	FANSIG	GPI	To detect FAN speed
GPIO15/A_PWM	CONTRAST	O	EC PWM for Panel Brightness
GPIO16/CIRTX	HWPG	GPI	
GPIO17/SCL1	MBCLK	O	SMBus Clock for M/B
GPIO20/TA2	SUSON	GPO	S3 Power Panel
GPIO21/B_PWM	NUMLED#	O	Number Lock LED drive
GPIO22/SDA1	MBDATA	I/O	SMBus Data for M/B
GPIO23/SCL3	VGA_CLK	O	SMBus Clock for acer ID flash
GPIO24/LDRQ#	EC_FPBACK#	GPO	Panel back light control
GPIO25/PSCLK3	MAINON	GPO	Turn On/Off main power
GPIO26/PSCLK2	PCH_ACIN	GPI	
GPIO27/PSDAT2	BT_POWERON#	GPO	Turn On/Off bule tooth power
GPIO30/CIRTX2	ACPRN	GPI	
GPIO31/SDA3	VGA_DATA	I/O	SMBus Data for acer ID flash
GPIO32/D_PWM	BATLED0#	GPO	Battery status LED drive
GPIO33/H_PWM	BATLED1#	GPO	Battery status LED drive
GPIO34/CIRRXL	CIRR_X2	GPI	CIR signal
GPIO35/PSDAT1	TPDATA	O	PS/2 data for touch pad
GPIO36/TB3	VRON	GPO	Turn On/Off CPU Power
GPIO37/PSCLK1	TPCLK	O	PS/2 clock for touch pad
GPIO40/F_PWM	SUSLED	GPO	S3 state LED drive
GPIO41		GPI	No used
GPIO42/TCK		GPI	No used
GPIO43/TMS	AMP_MUTE#	GPO	Turn On/Off Audio Amplier
GPIO44/TDI		GPI	No used
GPIO45/E_PWM	CPUFAN#	O	EC PWM for Fan Module
GPIO46/cirrxm/trst#		GPI	No used
GPO47/SCL4	VIN_ON	GPI	Turn On/Off VIN_SRC Power plane
GPIO50/TDO	D/C#	GPO	Battery charge / discharge control
GPIO51/TA3	S5_ON	GPO	Turn On/Off S5 Power plane
GPIO52/cirtx2/trdy#	HDMI_HPD_EC#	GPI	EC Detect HDMI State
GPIO53/SDA4		O	No used
GPIO54/ECSCI#	SIO_EXT_SCI#	GPI	EC SCI
GPIO55/CLKOUT	ECDB_CLOCK	GPI	EC core clock
GPIO56/TA1		GPI	No used
GPIO57/KBSOUT17	MY17	O	Keyboard scan output
GPIO60/KBSOUT16	MY16	O	Keyboard scan output
GPIO61/KBSOUT15	MY15	O	Keyboard scan output
GPIO62/KBSOUT14	MY14	O	Keyboard scan output
GPIO63/KBSOUT13	MY13	O	Keyboard scan output
GPIO64/KBSOUT12	MY12	O	Keyboard scan output
GPIO65/SMI#	SIO_EXT_SMI#	O	EC SMI
GPIO66/G_PWM	CAPSLED#	O	Caps Lock LED drive
GPIO67/PWUREQ	USBON#	GPO	USB power enable/disable
GPIO70/IRRX2_IRSL0	SUSC#	GPI	S.B sleep S4 pin
GPIO71/IRTX/SOUT2	PWROK_EC	GPO	System Power Good for PCI Reset
GPIO72/IRRX1/SIN2	ICH_RSMRST#	GPO	S.B Resume Power Reset
GPIO73/SCL2	2ND_MBCLK	O	SMBus Clock for CPU thermal
GPIO74/SDA2	2ND_MBDATA	I/O	SMBus Data for CPU thermal
GPIO75/SPI_SCK	BACKUP_SW	GPO	Backup Switch
GPO76/SPI_DO/SHBM	SHBM_R	GPO	Using SPI flash for BIOS and EC firmware
GPIO77/SPI_DI		GPI	No used
GPIO81	DNBSWON#	GPO	S.B Power button Event
GPO82/TRIS		GPI	No used
GPO83/SOUT_CR/BADDR1	PWRSAVE_LED#	GPI	Power Save LED
GPO84/BADDR0	BACKUP_LED#	GPI	Backup LED
GPIO87/CIRRRXM/SIN_CR	RF_EN	GPO	Mini card 1 (WLAN) enable/disable
GPI90/AD0	TEMP_MBAT	I	EC detect battery state
GPI91/AD1	WL_SW	GPI	Wireless Switch
GPI92/AD2	SML1ALERT#	GPI	Touchpad temperature / PCH thermal Hot
GPI93/AD3	ICMNT	I	EC detect system current in AC mode
GPI94/DA0	PWRSAVE_SW	GPI	Power Save (Battery) Button Switch
GPI95/DA1		GPI	No used
GPI96/DA2		GPI	No used
GPI97/DA3		GPI	No used

PCH GPIO Setting

Pin Name	Power	PCH Default	Net Name	Description	Setting	Internal PU/PD	External PU/PD
GPIO0 / BMBUSY#	Core	GPI	BMBUSY#	No used	GPO		PU 8.2KΩ to +3V
GPIO1 / TACH1	Core	GPI	SIO_EXT_SMI#	EC SMI	GPI		PU 10KΩ to +3V
GPIO2 / PIRQE#	Core	GPI	PCI_PIRQE#	No used	GPO		PU 8.2KΩ to +3V
GPIO3 / PIRQF#	Core	GPI	PCI_PIRQF#	No used	GPO		PU 8.2KΩ to +3V
GPIO4 / PIRQG	Core	GPI	PCI_PIRQG#	No used	GPO		PU 8.2KΩ to +3V
GPIO5 / PIRQH#	Core	GPI	PCI_PIRQH#	No used	GPO		PU 8.2KΩ to +3V
GPIO6 / TACH2	Core	GPI	SIO_EXT_SCI#	EC SCI interrupt	GPI		PU 10KΩ to +3V
GPIO7 / TACH3	Core	GPI	BOARD_ID0	M/B ID Setting	GPI		PD 10K to GND & PU to +3V
GPIO8	S5	GPO	RSV_GPIO8	No used	GPO		PU 10KΩ to +3V_S5
GPIO9 / OC5#	S5	Native	USB_OC5#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO10 / OC6#	S5	Native	USB_OC6#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO11 / SMBALERT#	S5	Native	RSV_SMBALERT#	No used	GPO		PU 10KΩ to +3V_S5
GPIO12 / LAN_PHY_PWR_CTRL	S5	Native	LAN_DISABLE#	No used	GPI		PU 10KΩ to +3V_S5
GPIO13 / HDA_DOCK_RST#	S5	GPI	PCH_GPIO13	No used	GPI		RV PU 10KΩ to +3V_S5
GPIO14 / OC7#	S5	Native	USB_OC7#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO15	S5	GPO	CR_WAKE#	No used	GPO	PU 20KΩ	PU 1KΩ to +3V_S5
GPIO16 / SATA4GP	Core	GPI	dGPU_HOLD_RST#	GPU Reset	GPO		PD 100K to G RV PU 10K to +3V
GPIO17 / TACH0	Core	GPI	dGPU_PWROK	GPU Power OK	GPI		PU 10KΩ to +3V
GPIO18 / PCIECLKRQ1#	Core	Native	CLK_PCIE_REQ1#_R	No used	GPO		PU 10KΩ to +3V
GPIO19 / SATA1GP	Core	GPI		No used	GPO		PU 10KΩ to +3V
GPIO20 / PCIECLKRQ2#	Core	Native	CLK_PCIE_REQ2#	Clock Request for PCIE Clocks	Native		PU 10KΩ to +3V
GPIO21 / SATA0GP	Core	GPI		No used	GPO		PU 10KΩ to +3V
GPIO22 / SCLOCK	Core	GPI	GPIO22	No used	GPO		PU 10KΩ to +3V
GPIO23 / LDRQ1#	Core	Native		No used	GPO		
GPIO24	S5	GPO		No used	GPO		
GPIO25 / PCIECLKRQ3#	S5	Native	CLK_PCIE_REQ3#_R	Clock Request for PCIE Clocks	Native		PU 10KΩ to +3V_S5
GPIO26 / PCIECLKRQ4#	S5	Native	CLK_PCIE_REQ4#_R	No used	GPO		PU 10KΩ to +3V_S5
GPIO27	S5	GPO		No used	GPO		
GPIO28	S5	GPI	TP_PCH_GPIO28	No used	GPO		PU 10KΩ to +3V_S5
GPIO29 / SLP_LAN#	S5	GPI	PM_SLP_LAN#	No used	GPO		RV PU 10KΩ to +3V_S5
GPIO30 / SUS_PWR_DN_ACK	S5	GPI	SUS_PWR_ACK_R	No used	GPO		PU 10KΩ to +3V_S5
GPIO31 / ACPRESENT	S5	GPI	ACIN_R	No used	GPO		PU 10KΩ to +3V_S5
GPIO32 / CLKRUN#	Core	GPO , Native	CLKRUN#	PCI Clock Run	Native		PU 8.2KΩ to +3V
GPIO33 / HDA_DOCK_EN#	Core	GPO	HDA_DOCK_EN#	No used	GPO	PU 20KΩ	RV PU 10K to +3V & 1K to GND
GPIO34 / STP_PCI#	Core	GPI	STP_PCI#	No used	GPO		PU 10KΩ to +3V
GPIO35 / SATACLKREQ#	Core	GPO	dGPU_VRON	GPU Voltage Regulator Enable	GPO		
GPIO36 / SATA2GP	Core	GPI	dGPU_PWR_EN#	GPU Power Enable	GPO		PU 10KΩ to +3V
GPIO37 / SATA3GP	Core	GPI	dGPU_PRSNT#	No used	GPI		PD 10KΩ to GND
GPIO38 / SLOAD	Core	GPI	GPIO38	No used	GPO		PU 10KΩ to +3V
GPIO39 / SDATAOUT0	Core	GPI	SAVE_LED#	No used	GPO		PU 10KΩ to +3V
GPIO40/OC1#	S5	Native	USB_OC1#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO41/OC2#	S5	Native	USB_OC2#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO42/OC3#	S5	Native	USB_OC3#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO43/OC4#	S5	Native	USB_OC4#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO44 / PCIECLKRQ5#	S5	Native	CLK_PCIE_REQ5#	No used	Native		PU 10KΩ to +3V_S5
GPIO45 / PCIECLKRQ6#	S5	Native	GPIO45	No used	GPO		PU 10KΩ to +3V_S5
GPIO46 / PCIECLKRQ7#	S5	Native	RST_GATE#	S3 Power Reduction	GPO		PU 10KΩ to +3V_S5
GPIO47 / PEG_A_CLKRQ#	S5	Native	PEG_CLKREQ#_R	Clock Request Signals for PEG	Native		PD 10KΩ to GND
GPIO48 / SDATAOUT1	Core	GPI	SV_SET_UP	No used	GPO		PU 10KΩ to +3V
GPIO49 / SATA5GP	Core	GPI	SATA5GP	CPU alert for EC	GPO		PU 10KΩ to +3V
GPIO50 / REQ1#	Core	Native	PCI_REQ1#	No used	GPO		PU 8.2KΩ to +3V
GPIO51 / GNT1#	Core	Native	PCI_GNT1#	Boot BIOS Selection	Native		PD 1K to GND RV PU 1K to +3V
GPIO52 / REQ2#	Core	Native	dGPU_SELECT#	GPU Output Select	GPO		PU 10KΩ to +3V
GPIO53 / GNT2#	Core	Native	PWM_SELECT#	LVDS_BRIGHT Select	GPO		
GPIO54 / REQ3#	Core	Native	PCI_REQ3#	No used	GPO		PU 8.2KΩ to +3V
GPIO55 / GNT3#	Core	Native	PCI_GNT3#	No used	Native		PU 8.2KΩ to +3V
GPIO56 / PEG_B_CLKRQ#	S5	Native	CLK_PCIE_LAN_REQ#	Clock Request Signals for PEG	Native		PU 10KΩ to +3V_S5
GPIO57	S5	GPI	GPIO57	No used	GPI		PD 10KΩ to GND
GPIO58 / SML1CLK	S5	Native	SMB_CLK_ME1	SMBus Clock for EC	Native		PU 2.2KΩ to +3V_S5
GPIO59 / OC0#	S5	Native	USB_OC0#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO60 / SML0ALERT#	S5	Native	RSV_SML0ALERT#	No used	Native		PU 10KΩ to +3V_S5
GPIO61 / SUS_STAT#	S5	Native	SUS_STAT#	No used	GPO		
GPIO62 / SUSCLK	S5	Native	ICH_SUSCLK	Suspend Clock	Native		
GPIO63 / SLP_S5#	S5	Native	SLP_S5#_R	No used	GPO		
GPIO64 / CLKOUTFLEX0	Core	Native	CLK_FLEX0	No used	GPO		
GPIO65 / CLKOUTFLEX1	Core	Native	CLK_FLEX1	No used	GPO		
GPIO66 / CLKOUTFLEX2	Core	Native	CLK_FLEX2	No used	GPO		
GPIO67 / CLKOUTFLEX3	Core	Native	dGPU_EDIDSEL#	GPU EDID Select	GPO		PU 10KΩ to +3V
GPIO72 / BATLOW#	S5	Native	PM_BATLOW#	No used	GPO		PU 8.2KΩ to +3V_S5
GPIO73 / PCIECLKRQ0#	S5	Native	CLK_PCIE_REQ0#	No used	GPO		PU 10KΩ to +3V_S5
GPIO74 / SML1ALERT#	S5	Native	RSV_SML1ALERT#	No used	GPO		PU 10KΩ to +3V_S5
GPIO75 / SML1DATA	S5	Native	SMB_DATA_ME1	SMBus Data for EC	Native		PU 2.2KΩ to +3V_S5

CK595 Clock Setting Table

Differential CPU Clock

Pin Name	Pin	Net Name	Description
CPU_0	23	CLK_BUF_BCLK	
CPU_0#	22	CLK_BUF_BCLK#	Differential CPU clock

CK595 PCI Express Clock

Pin Name	Pin	Net Name	Description
DOT96	3	CLK_BUF_DREFCLK	
DOT96#	4	CLK_BUF_DREFCLK#	96MHz DOT clock for PCH
SRC_2	13	CLK_BUF_DREFSSCLK	
SRC_2#	14	CLK_BUF_DREFSSCLK#	Clock output for PCH graphic contoller
SRC_1/SATA	10	CLK_BUF_PCIE_3GPLL	
SRC_1#/SATA#	11	CLK_BUF_PCIE_3GPLL#	Differential Serial Reference Clock for PCH

PCH PCI Express Clock

Pin Name	Pin	Net Name	Description
CLKOUT_BCLK0_P	AM3	CLK_CPU_BCLK	
CLKOUT_BCLK0_N	AM1	CLK_CPU_BCLK#	Differential Serial Reference Clock for CPU
CLKOUT_DP_P	AT1	DPLL_REF_SSCLK	
CLKOUT_DP_N	AT3	DPLL_REF_SSCLK#	Differential Serial Reference Clock for CPU
CLKOUT_DMI_P	AN2		
CLKOUT_DMI_N	AN4	CLK_PCIE_3GPLL#	Differential Serial Reference Clock for CPU
CLKOUT_PEG_A_P	AD43	CLK_PCIE_VGA	Differential Serial Reference Clock for PCI-Express
CLKOUT_PEG_A_N	AD45	CLK_PCIE_VGA#	Graphics device
CLKOUT_PCIE0P	AK47		
CLKOUT_PCIE0N	AK48		No use
CLKOUT_PCIE1P	AM45	CLK_PCH_SRC1	
CLKOUT_PCIE1N	AM43	CLK_PCH_SRC1#	Differential Serial Reference Clock for MINI CARD 2
CLKOUT_PCIE2P	AM48	CLK_PCH_SRC2	
CLKOUT_PCIE2N	AM47	CLK_PCH_SRC2#	Differential Serial Reference Clock for MINI CARD 1
CLKOUT_PCIE3P	AH41	CLK_PCH_SRC3	
CLKOUT_PCIE3N	AH42	CLK_PCH_SRC3#	Differential Serial Reference Clock for OZ888
CLKOUT_PCIE4P	AM53		
CLKOUT_PCIE4N	AM51		No use
CLKOUT_PCIE5P	AJ52		
CLKOUT_PCIE5N	AJ50		No use
CLKOUT_PEG_B_P	AK51	CLK_PCIE_LOM	
CLKOUT_PEG_B_N	AK53	CLK_PCIE_LOM#	Differential Serial Reference Clock for on board LAN

Other Clock

Pin Name	Pin	Net Name	Description
27M	6	27M_CLK	27MHz for GPU
27M_SS	7		
REF	30	CLK_ICH_14M	14.318MHz for PCH

Clock Request Table	
CLKREQ#	Control
PEG_A_CLKRQ#	GPU
PCIECLKRQ0#	N/A
PCIECLKRQ1#	MINI2
PCIECLKRQ2#	MINI1
PCIECLKRQ3#	OZ888
PCIECLKRQ4#	N/A
PCIECLKRQ5#	N/A
PEG_B_CLKRQ#	LAN

QUANTA COMPUTER

Title: **Schematic Setting**

Size	Document Number	Rev
	ZH7	1A

Date: Wednesday, January 20, 2010 Sheet 50 of 50