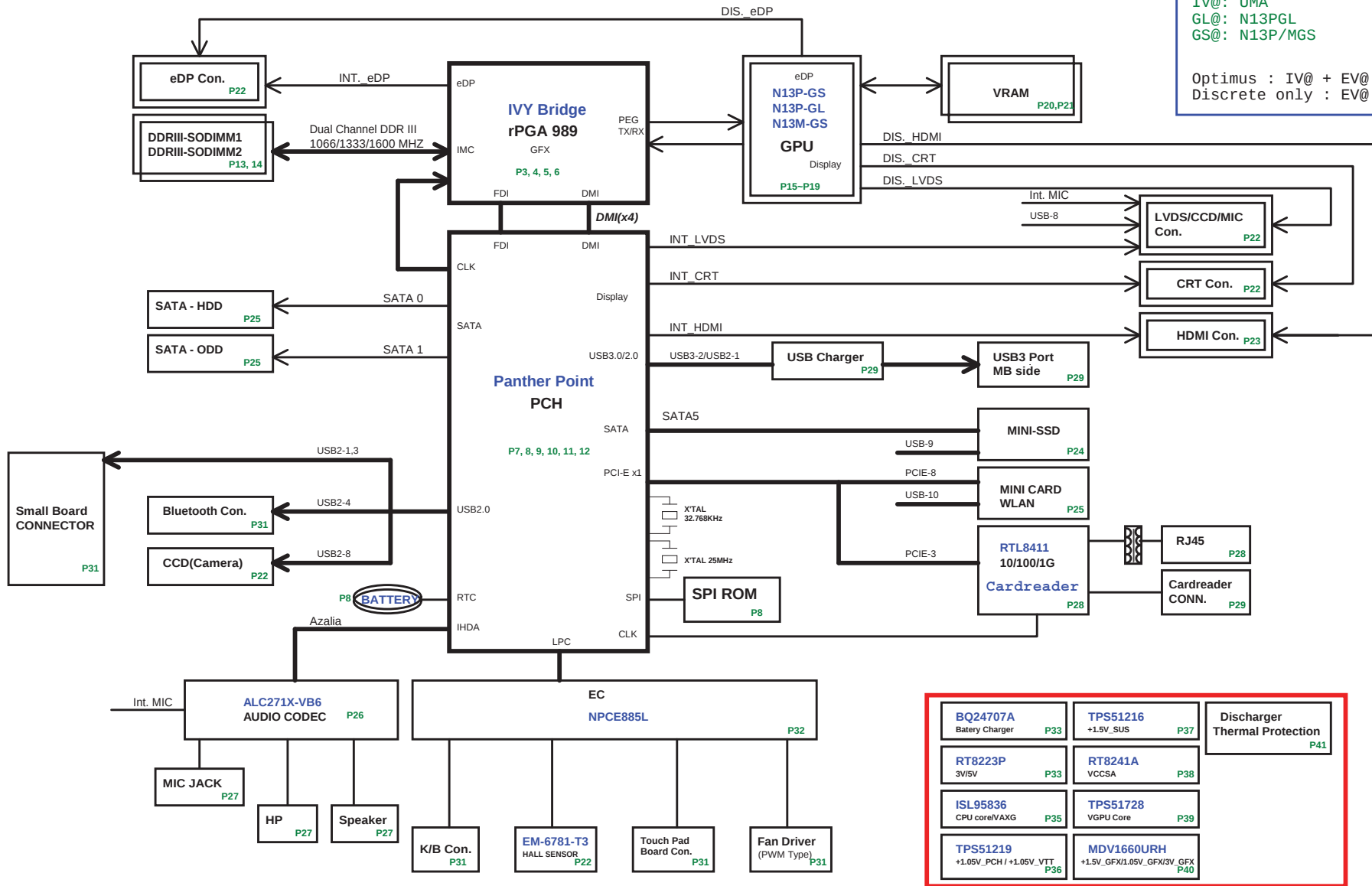


ZQTA/ZQSA CRV SYSTEM BLOCK DIAGRAM

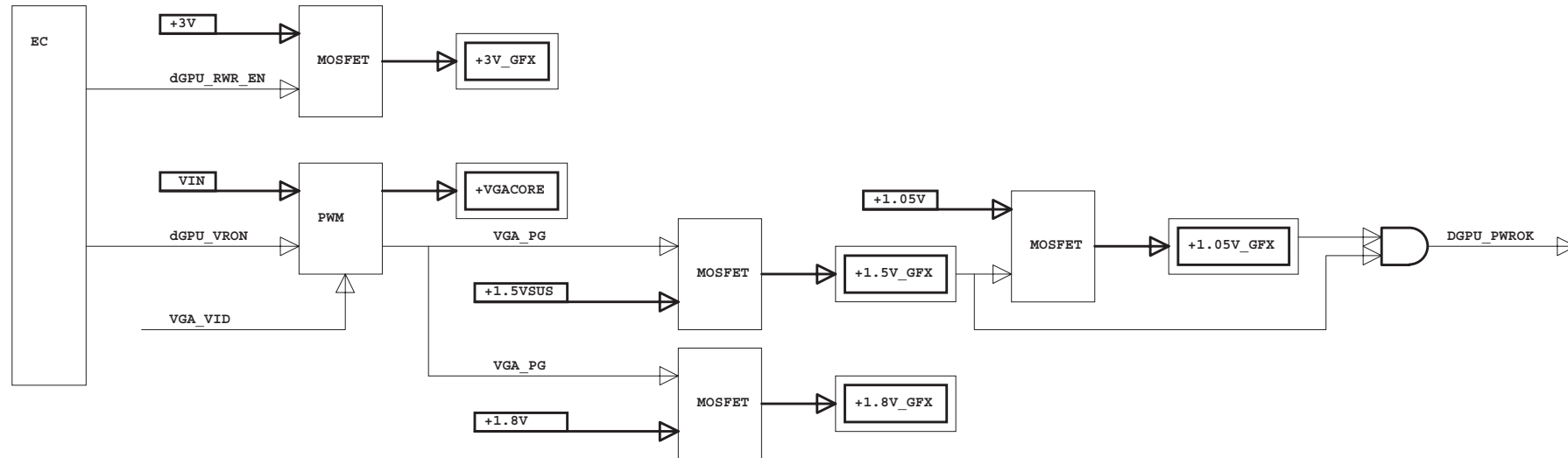
BOM

IV@ : iGPU
EV@ : dGPU
OP@ : Optimus
DO@ : Discrete only
SP@ : Special
SNP@ : N13PGS/GL
IV@ : UMA
GL@ : N13PGL
GS@ : N13P/MGS

Optimus : IV@ + EV@ + OP@
Discrete only : EV@ + DO@



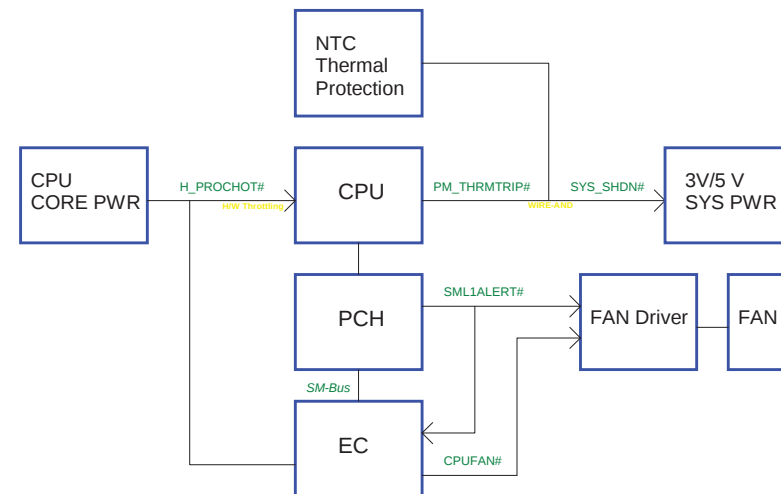
VGA power up sequence



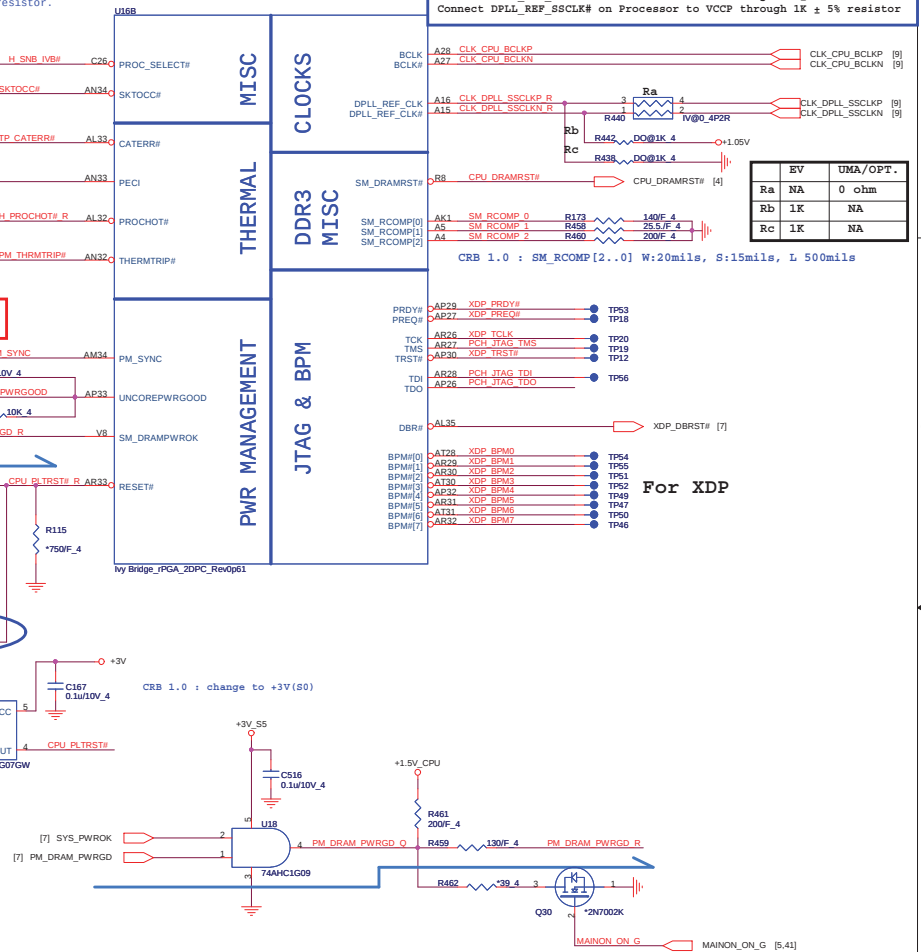
Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V--+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V--+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	VRON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER/IVY/SNB bridge VCCIO	MAINON	S0
+VCCSA	+0.9V	CPU POWER	HWPG_VTT	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
			MAINON	S0

Thermal Follow Chart



IVY Bridge Processor (CLK,MISC,JTAG)

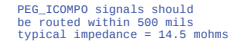


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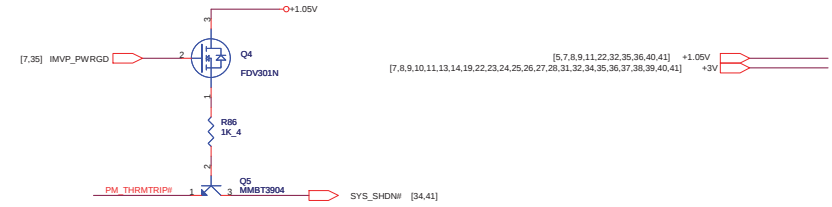
DG 1.0 :
The recommended AC cap value is changed to 220nF for compatibility with
PCIe Gen3 on future platforms.
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.

```

DP & PEG Compensation



9/27 modified

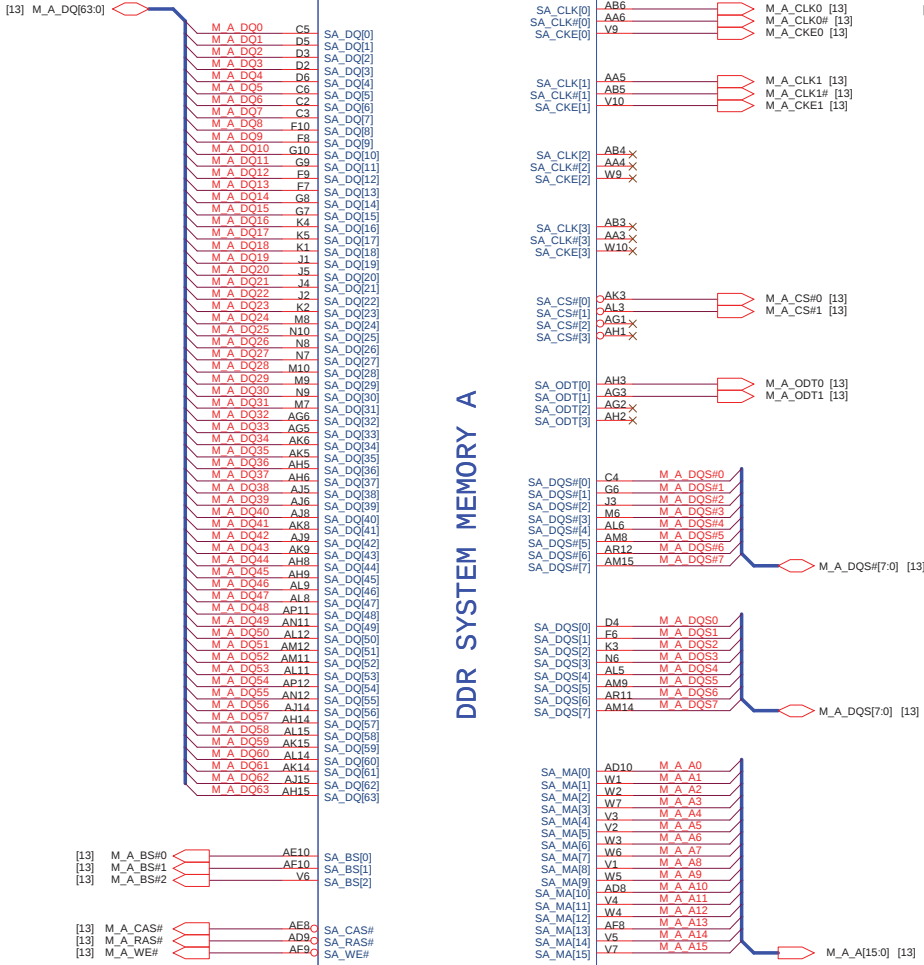


IVY Bridge Processor (DDR3)

U16C

Ivy Bridge_rPGA_2DPC_Rev0p61

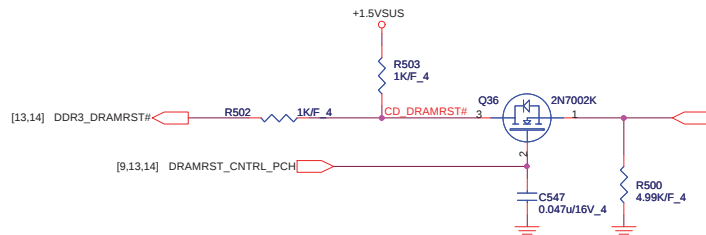
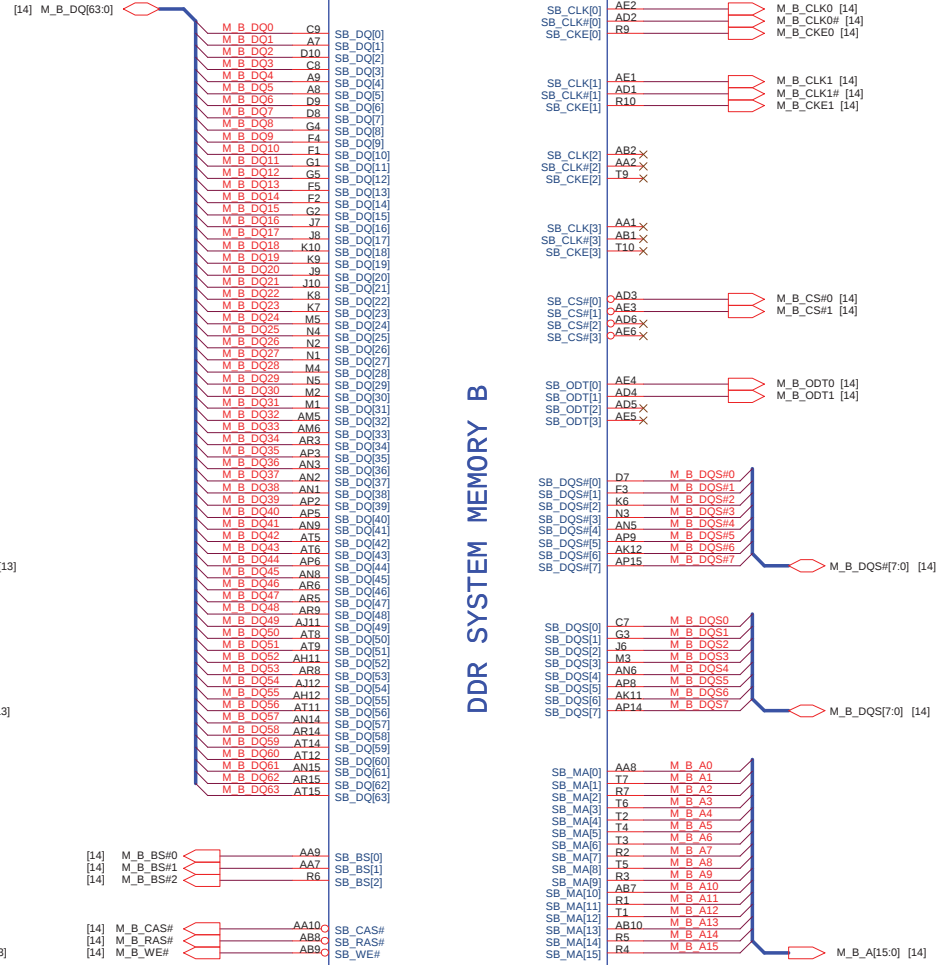
DDR SYSTEM MEMORY A

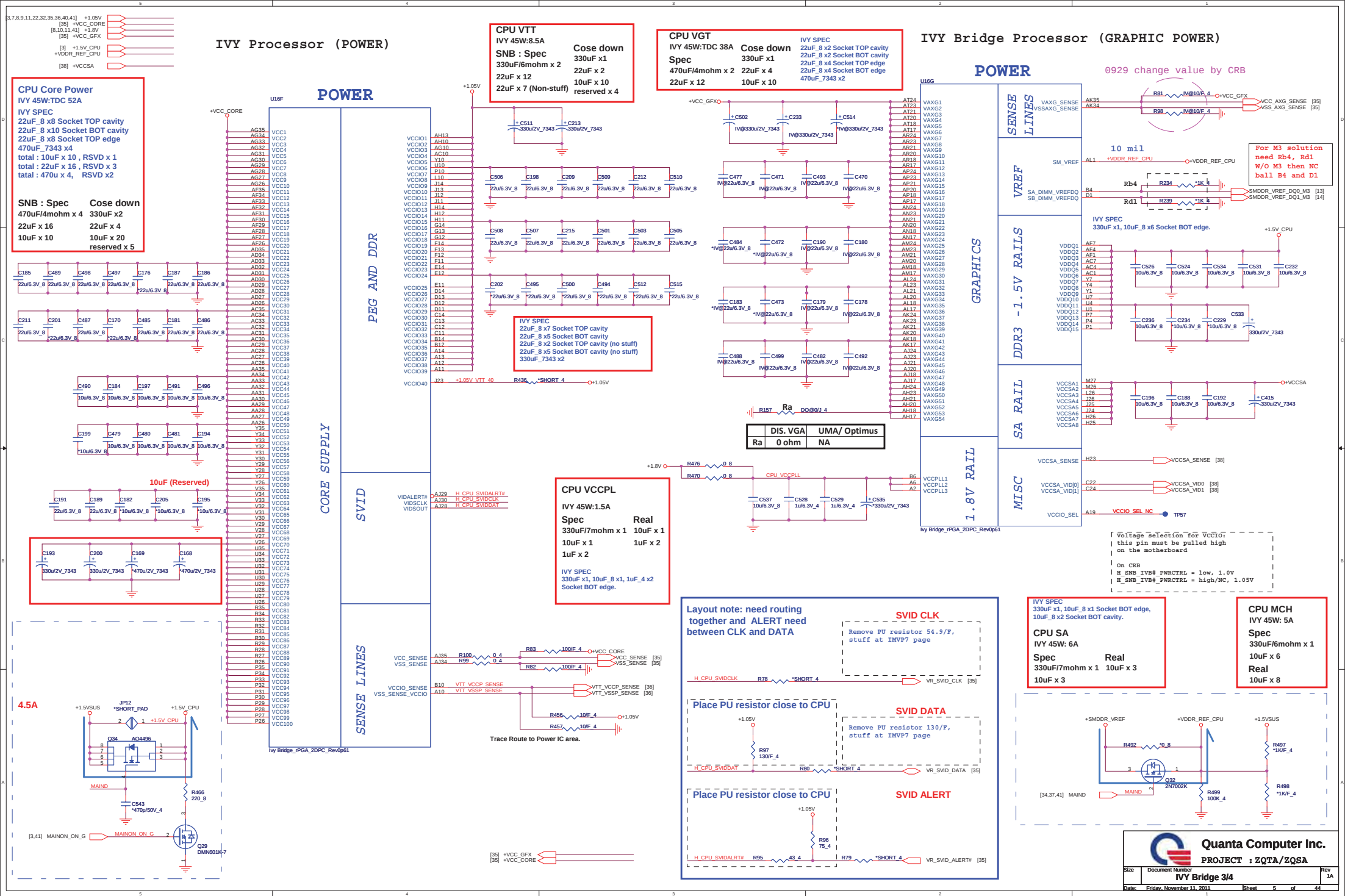


U16D

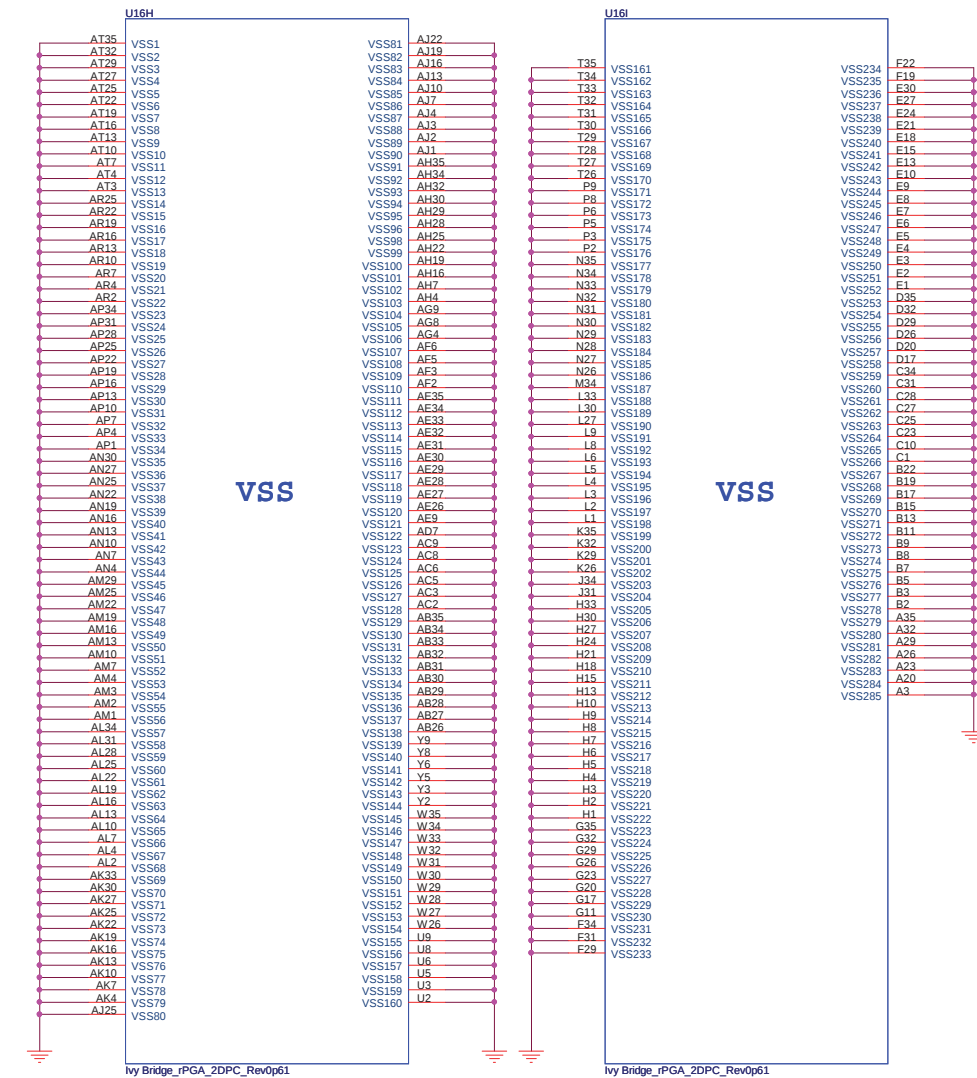
Ivy Bridge_rPGA_2DPC_Rev0p61

DDR SYSTEM MEMORY B

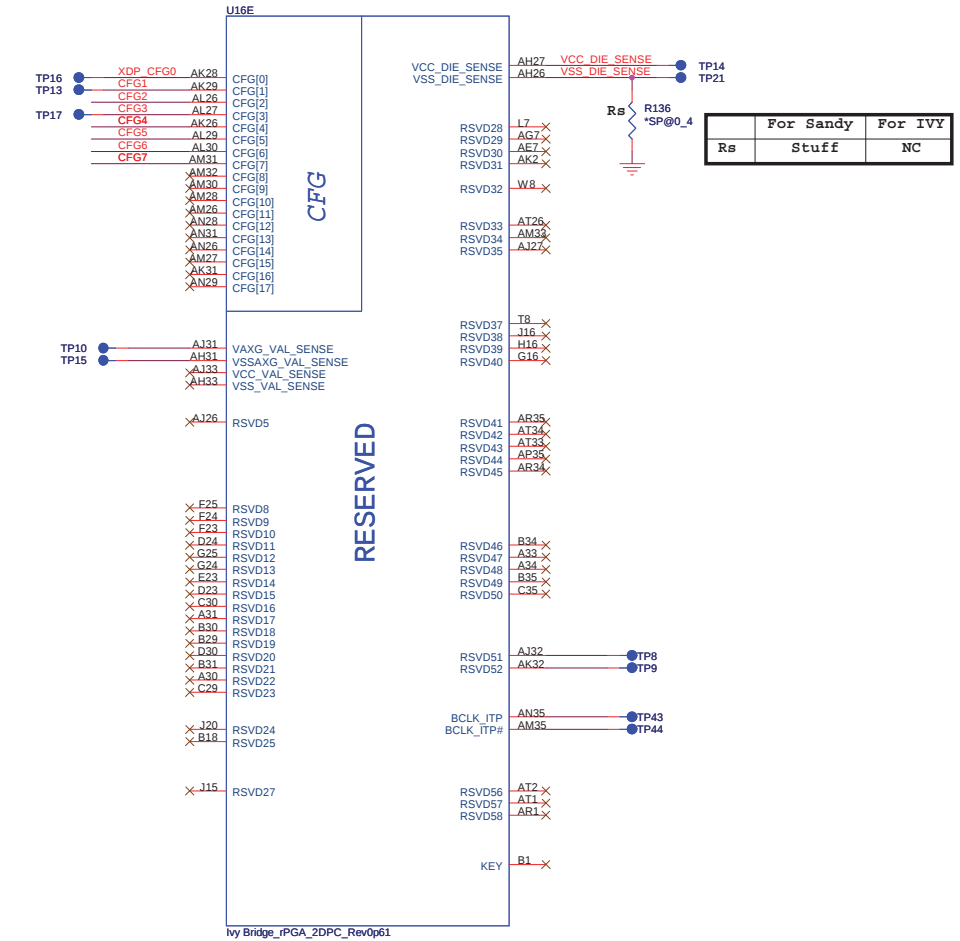




IVY Bridge Processor (GND)



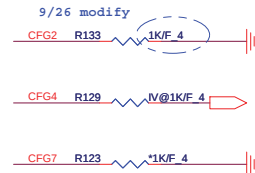
IVY Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG6

R130

1K/F 4

CFG5

R127

1K/F 4

CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled

10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled

01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)

00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Q

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Size

Document Number

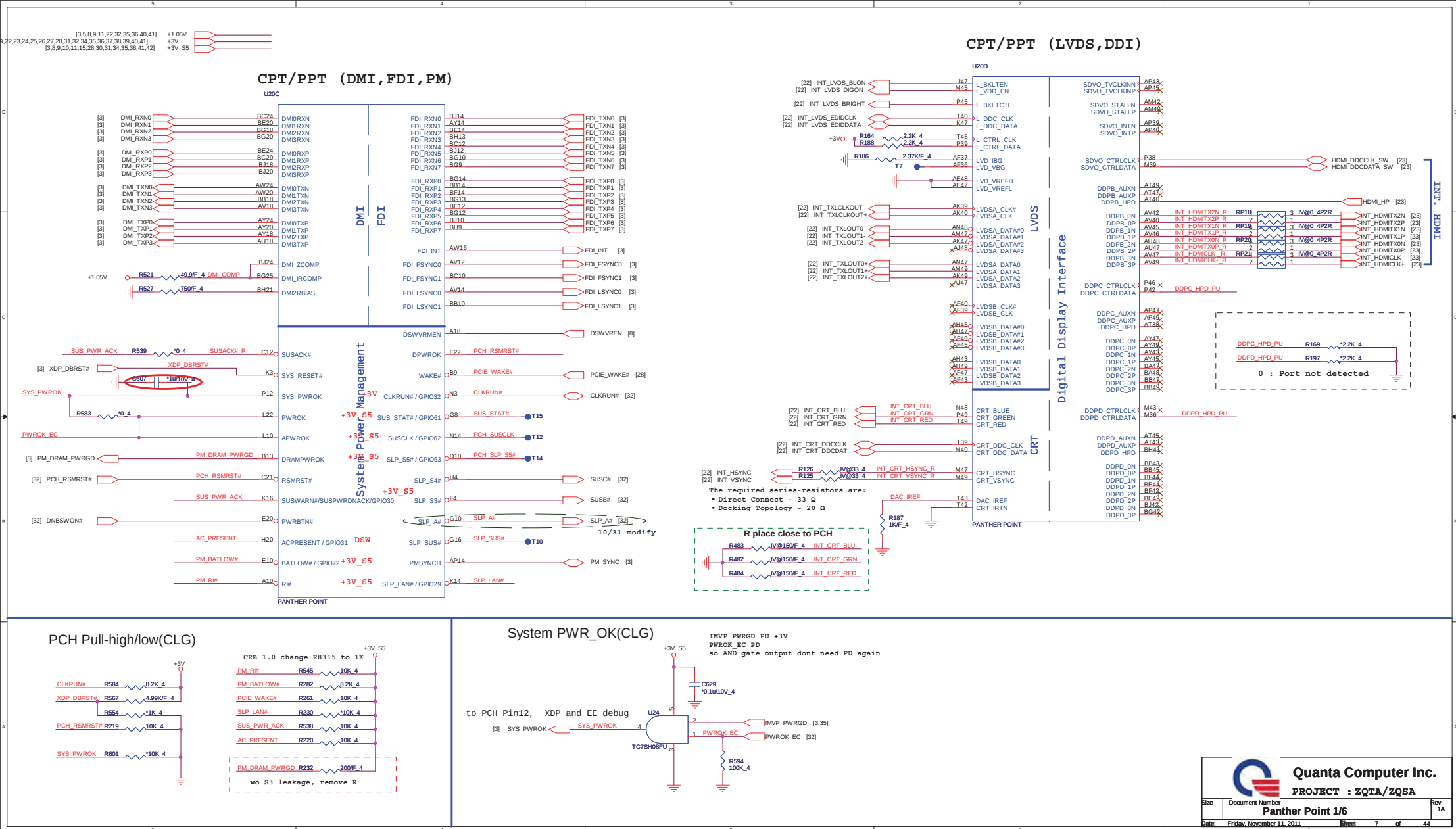
Rev

IVY Bridge 4/4

1A

Date: Friday, November 11, 2011

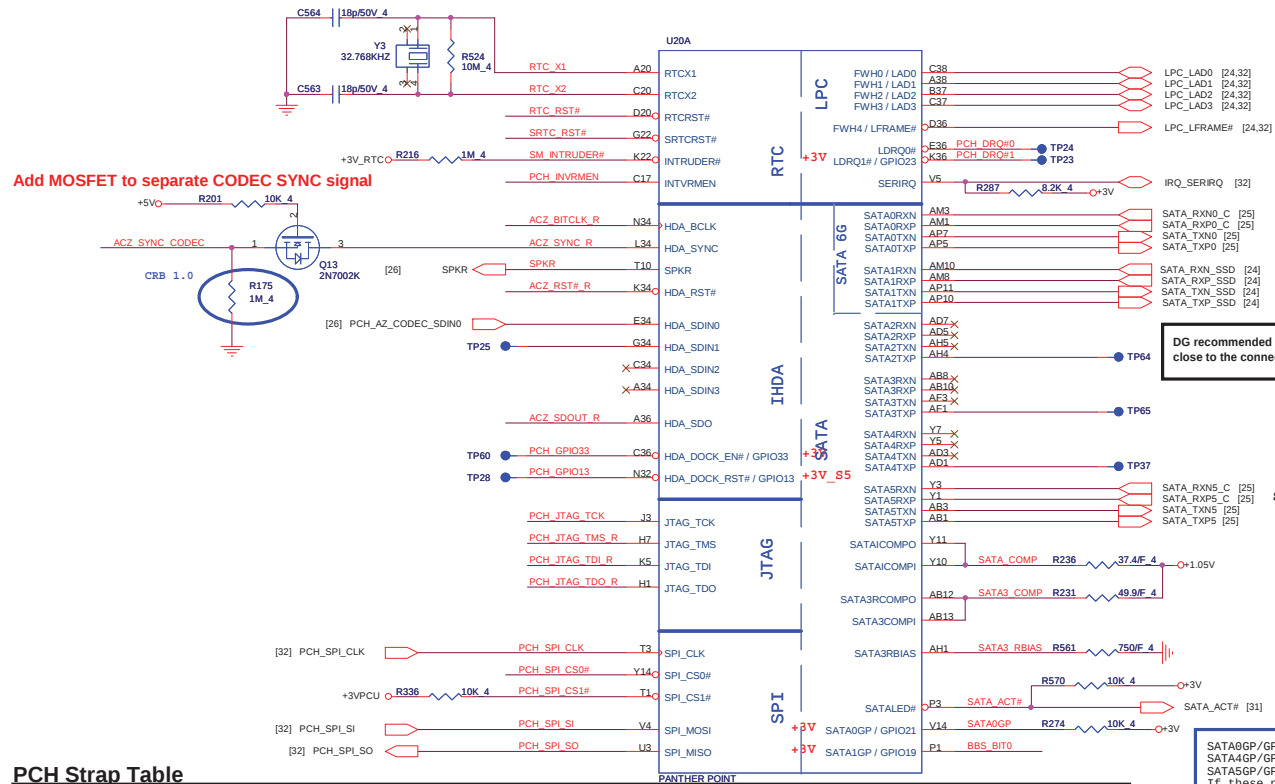
Sheet 6 of 44



20mils



PCH2 (CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V _{IO} 									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC 									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden	32] ME_WR 									
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc										
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 									
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable	+3V_S5 									
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable	+3V_RTC 									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V 									

SATA0GP/GPIO21
SATA4GP/GPIO16
SATA5GP/GPIO49
If these pins are unused use 8.2k
to 10k pull-up to +Vcc3_3 or 8.2k
to 10k pull-down to ground

Used as GPIO only. at chklist 1.2

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

ME_WR default EC setting folating

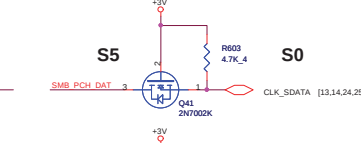
for future CPU, Sandy Bridge NC
DF_TVS needs to be pulled up to VccDFTERM power rail
through 2.2 kOhm $\pm 5\%$ - R8361 change to 0 or not??

Needs to be pulled High for Huron River platform.
chklist 1.2

U20B

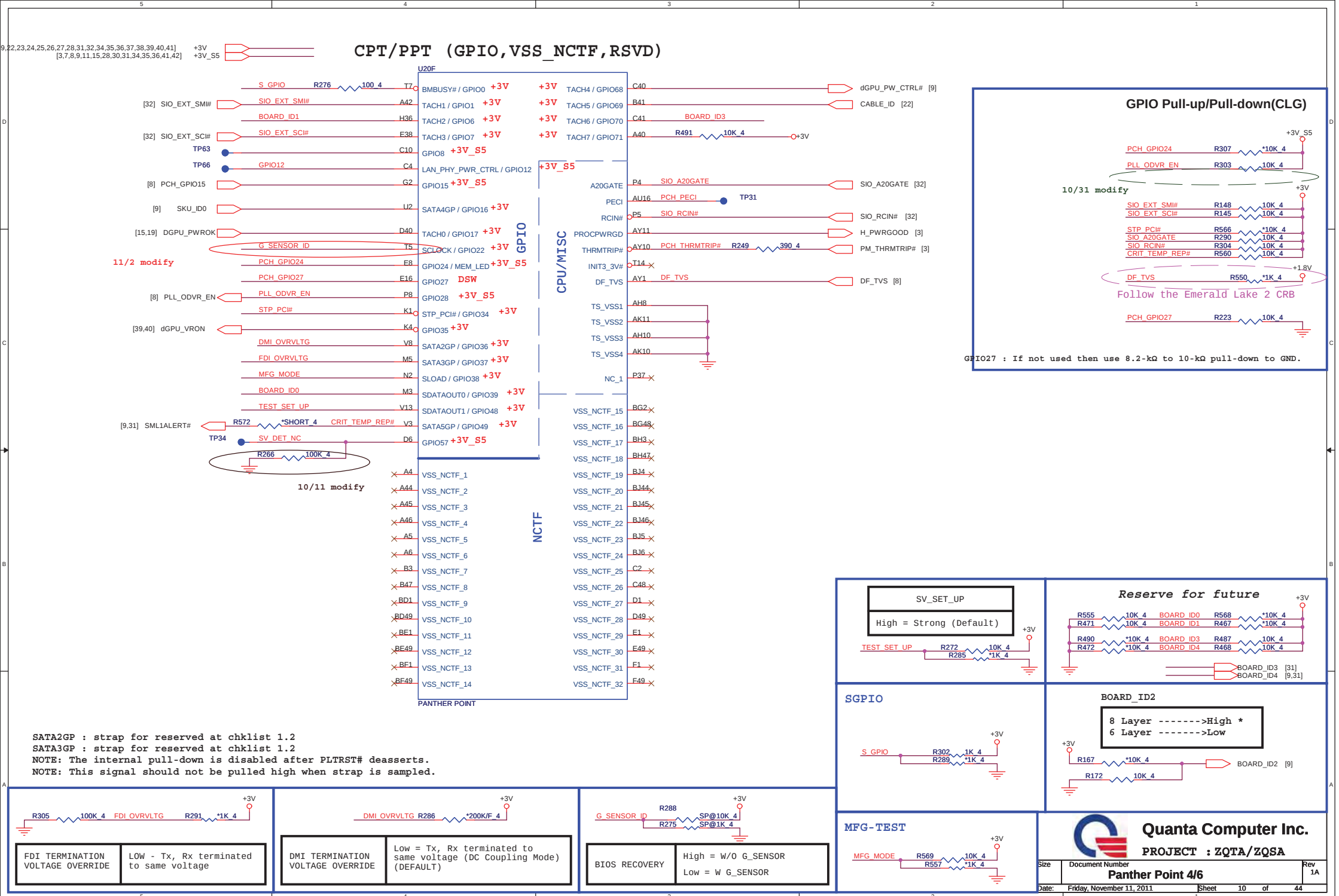


SMBus(PCH)

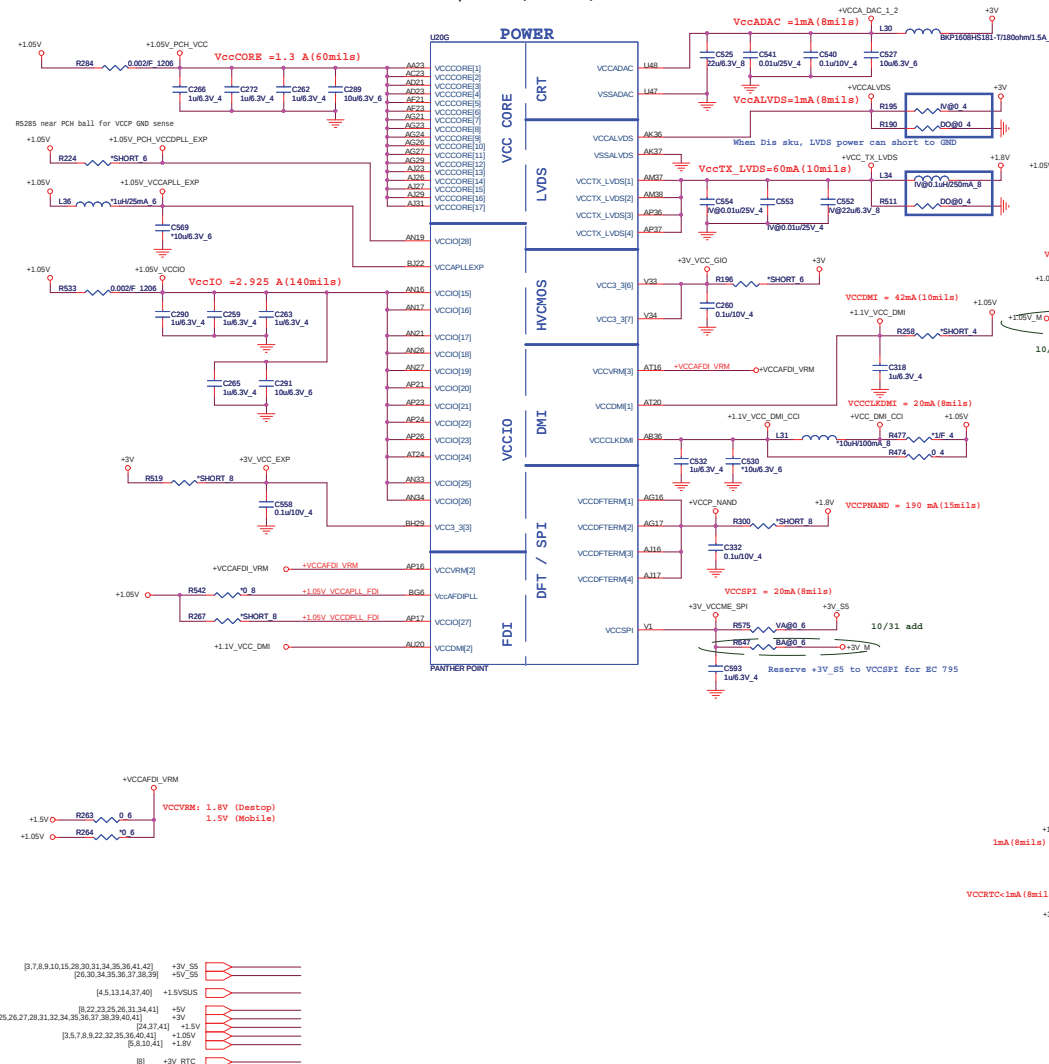


	GPIO PW_CTRLs (GPIO48) CTL = GPIO_YO08	GPIO ID1 (GPIO49)	SKD ID1 (GPIO14)	VGA R/W Signal	Setup Menu
UMA Only	1	0	0	UMA	UMA boot
GPU Only	0	0	1	GPU	HiDdan GPU boot
Switchable (Max)				UMA/GPU	UMA boot
Optimize (Maximize)	0	1	1	UMA	UMA/GS UMA boot

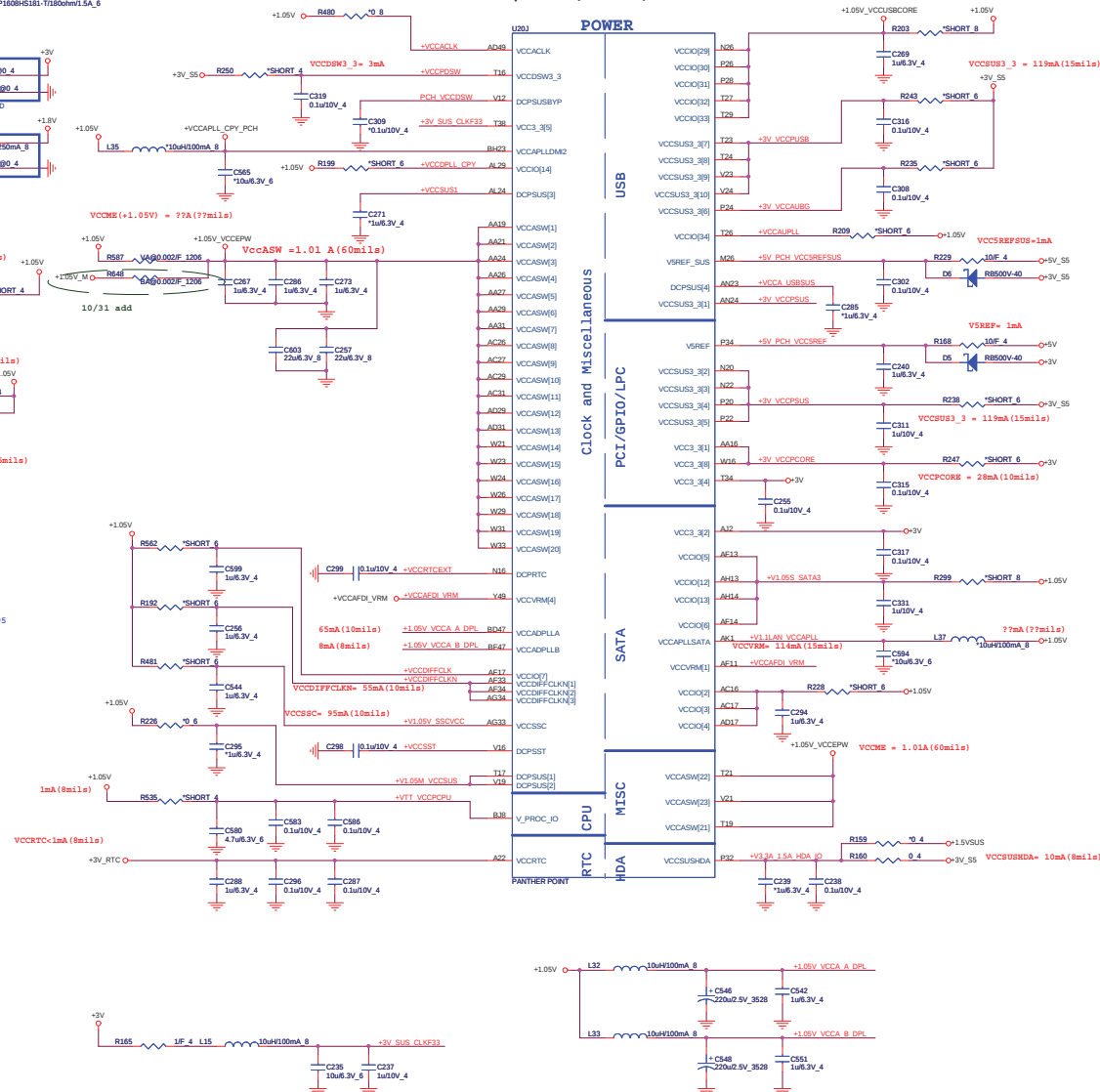
GPIO_PW_CTRLs
 1 = GPU power is control by R/W (non Discrete SW)
 0 = GPU power is control by PCM GPIO (Discrete, SG or Optimize)



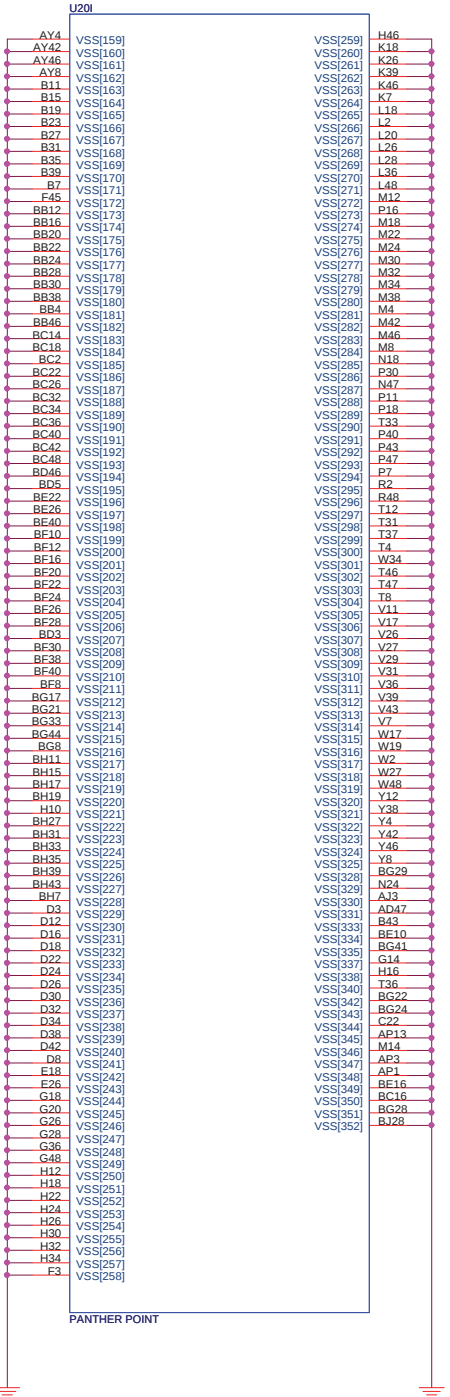
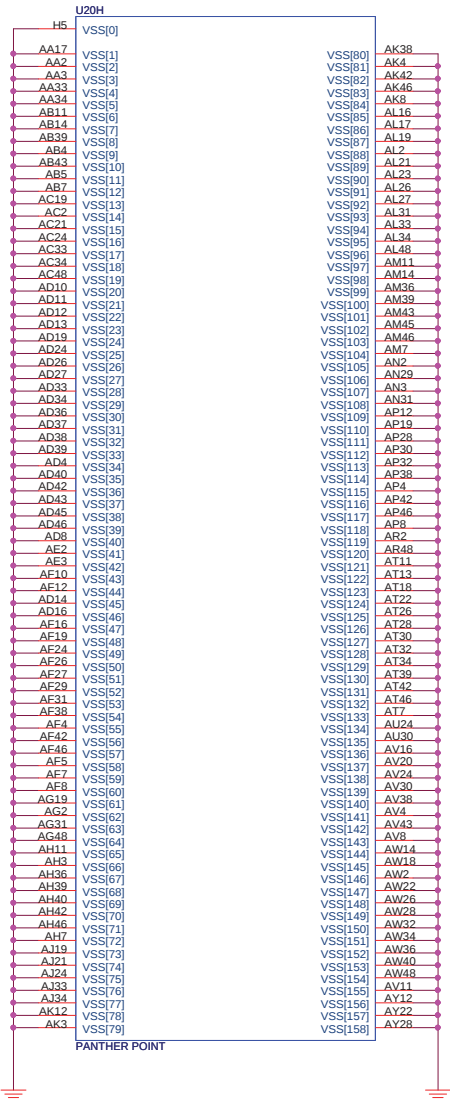
CPT/PPT (POWER)

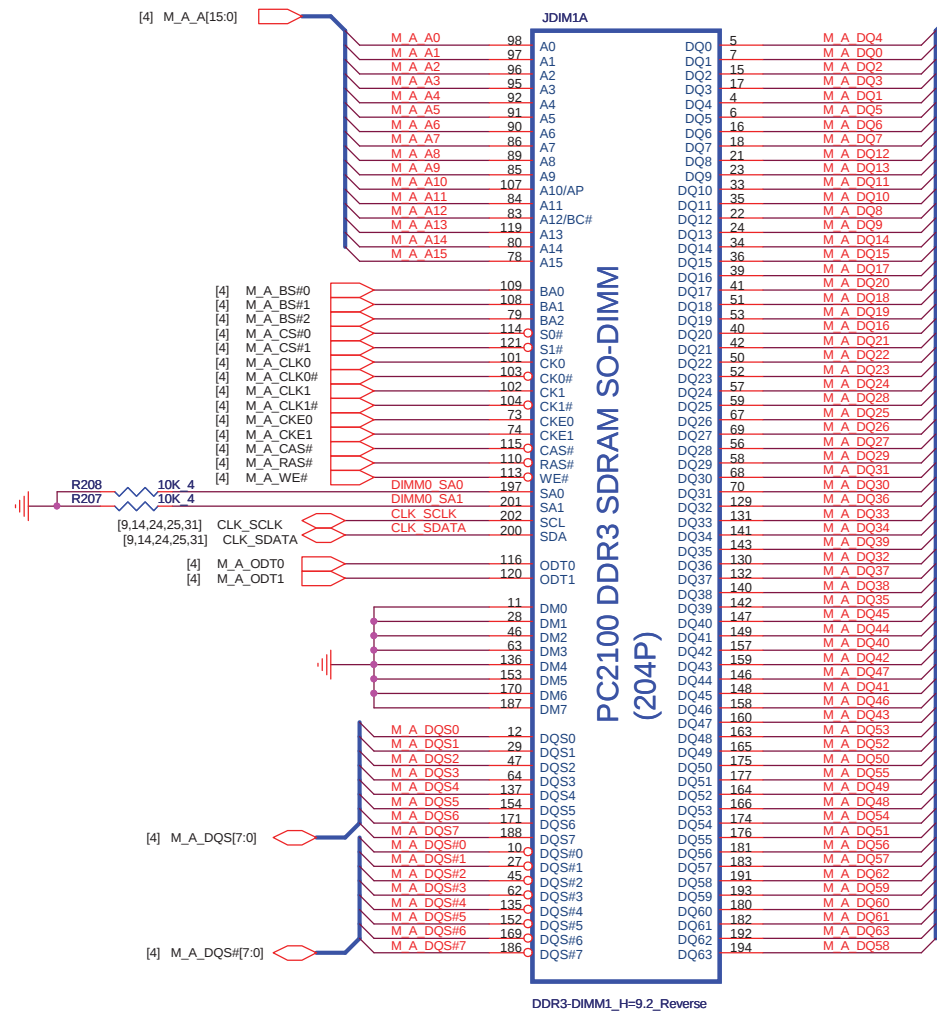


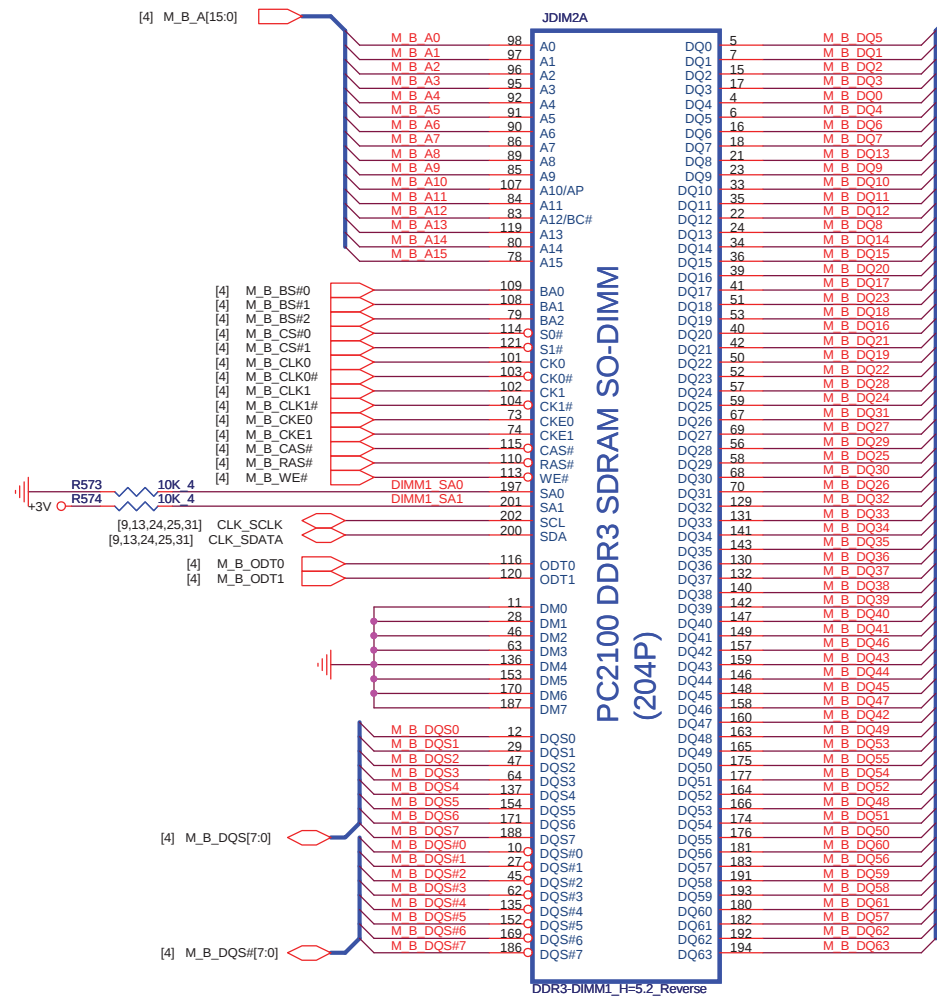
CPT/PPT (POWER)



IBEX PEAK-M (GND)

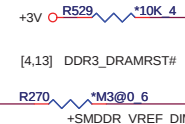




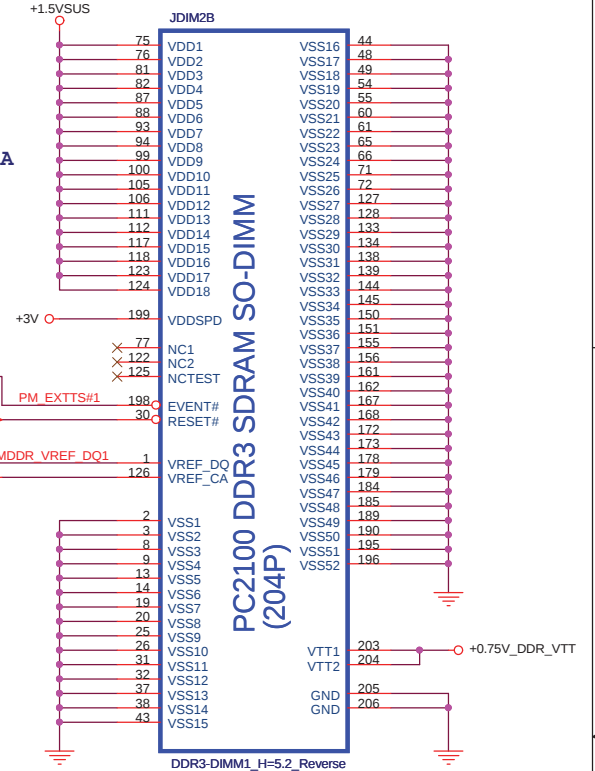


M3 solution

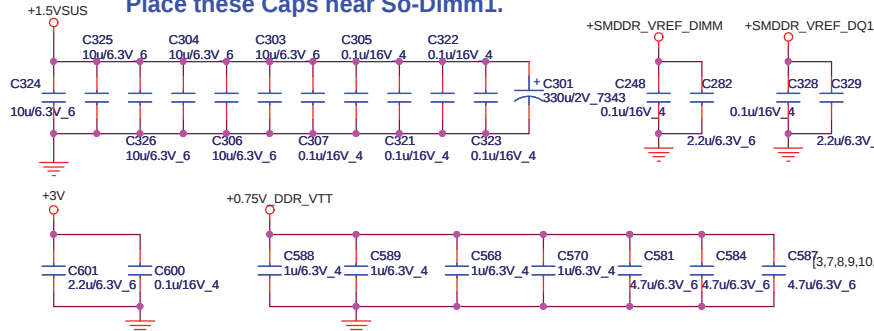
[5] SMDDR_VREF_DQ1_M3



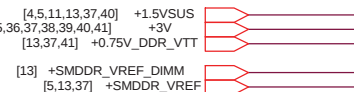
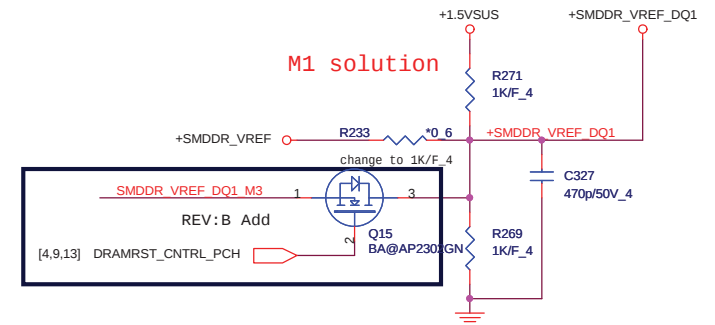
2.48A



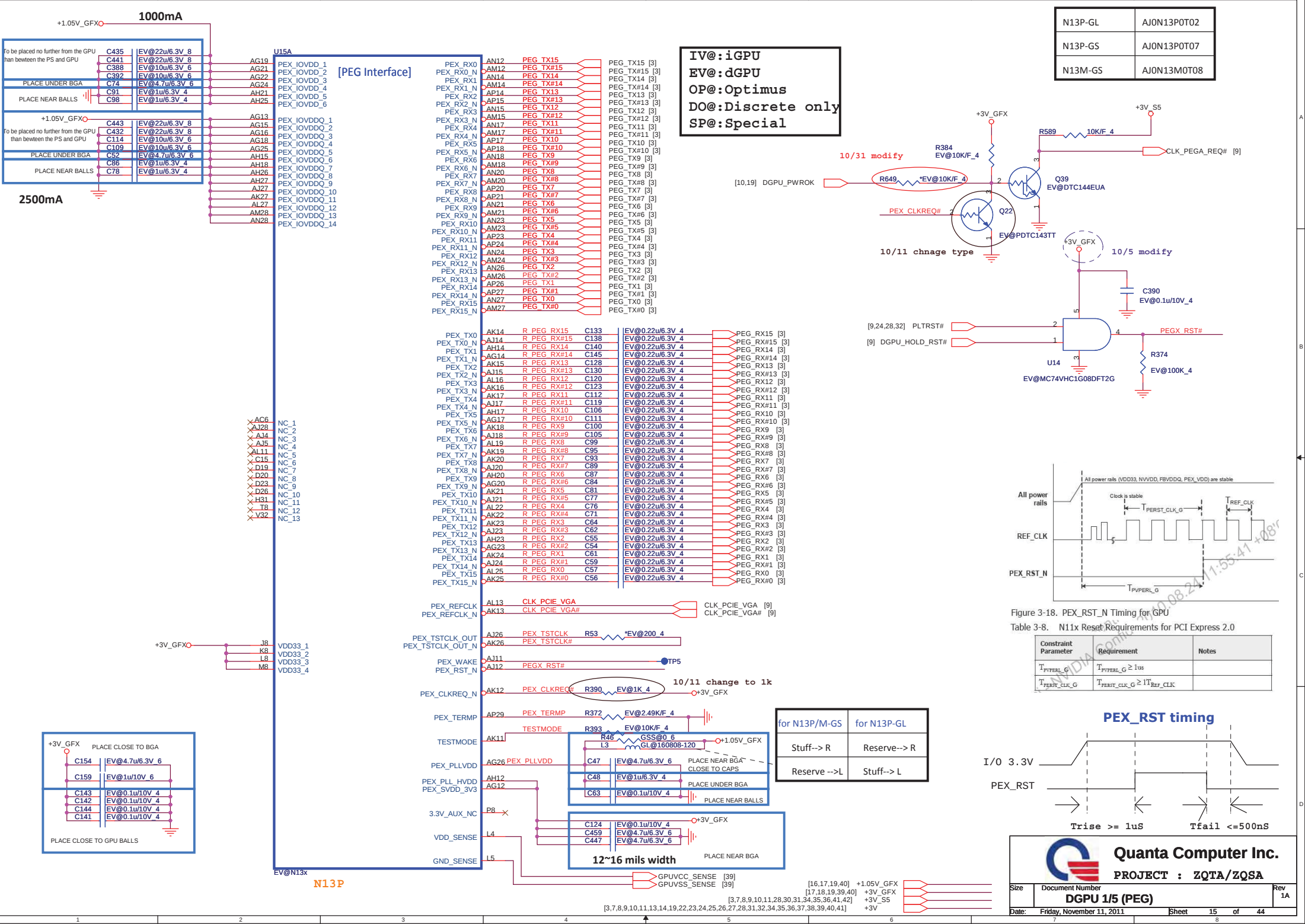
Place these Caps near So-Dimm1.



M1 solution



Quanta Computer Inc.
PROJECT : ZQTA/ZQSA



N13P-GL	AJON13P0T02
N13P-GS	AJON13P0T07
N13M-GS	AJON13M0T08

IV@:iGPU
EV@:dGPU
OP@:Optimus
DO@:Discrete only
SP@:Special

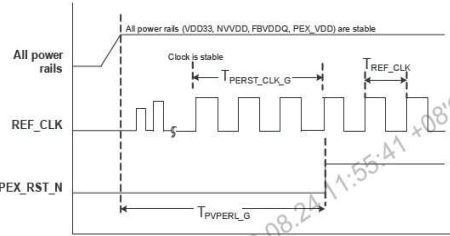
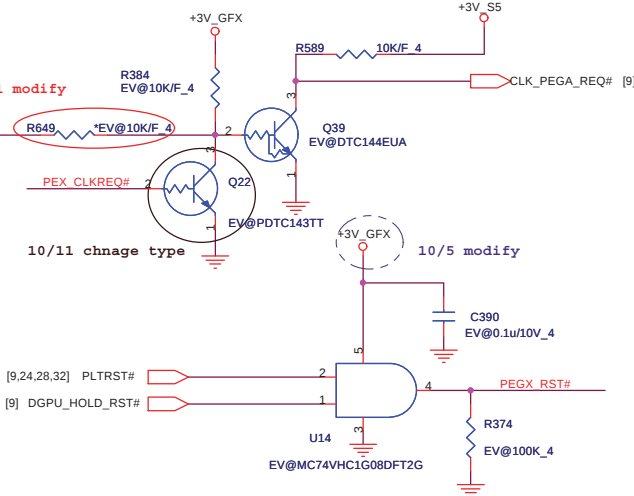
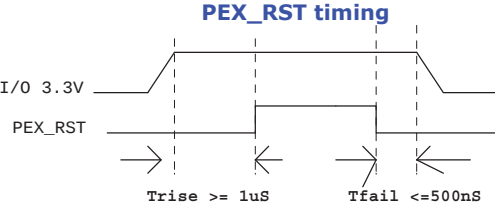
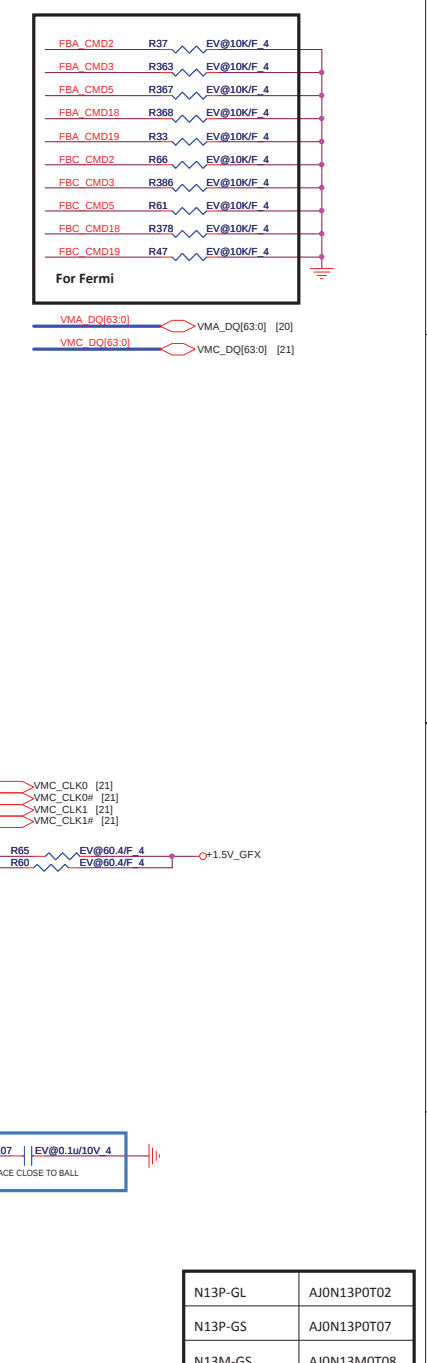
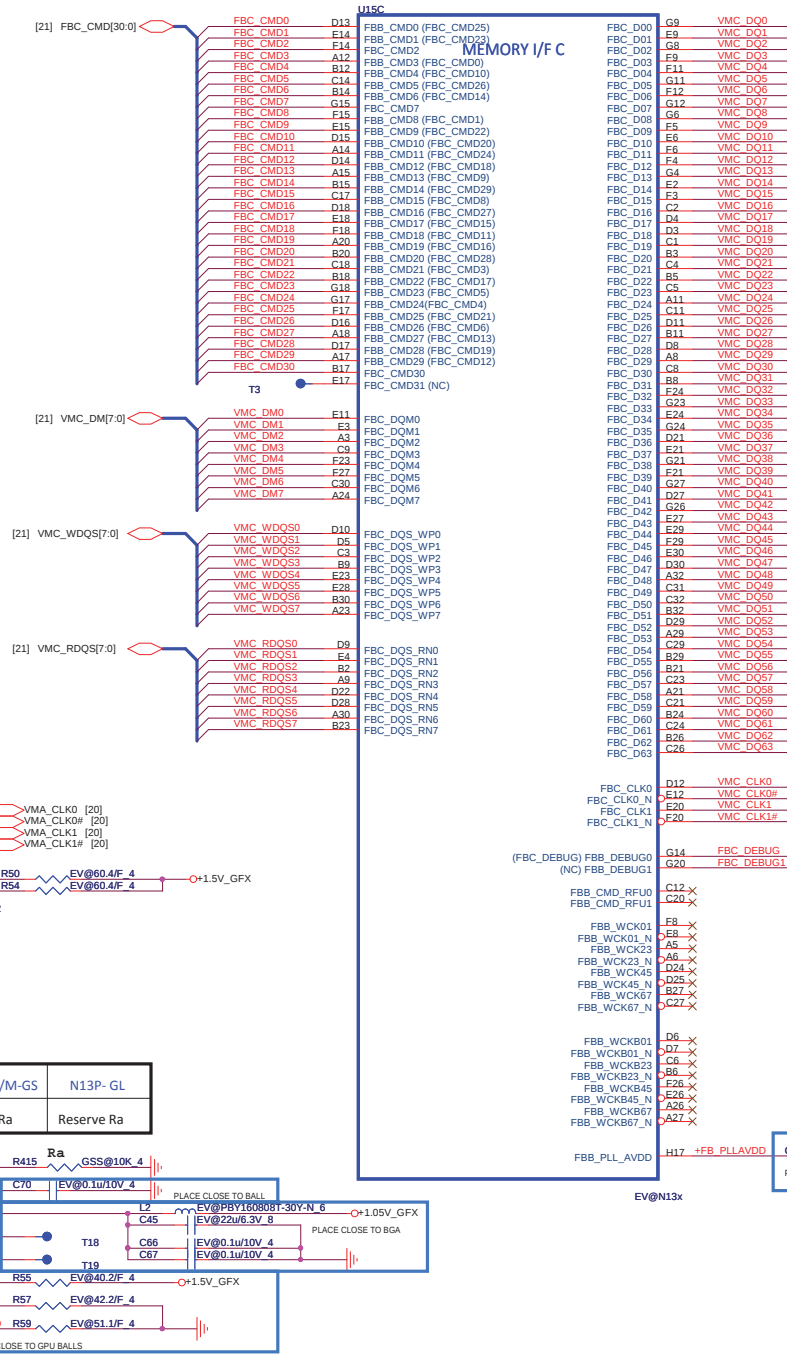
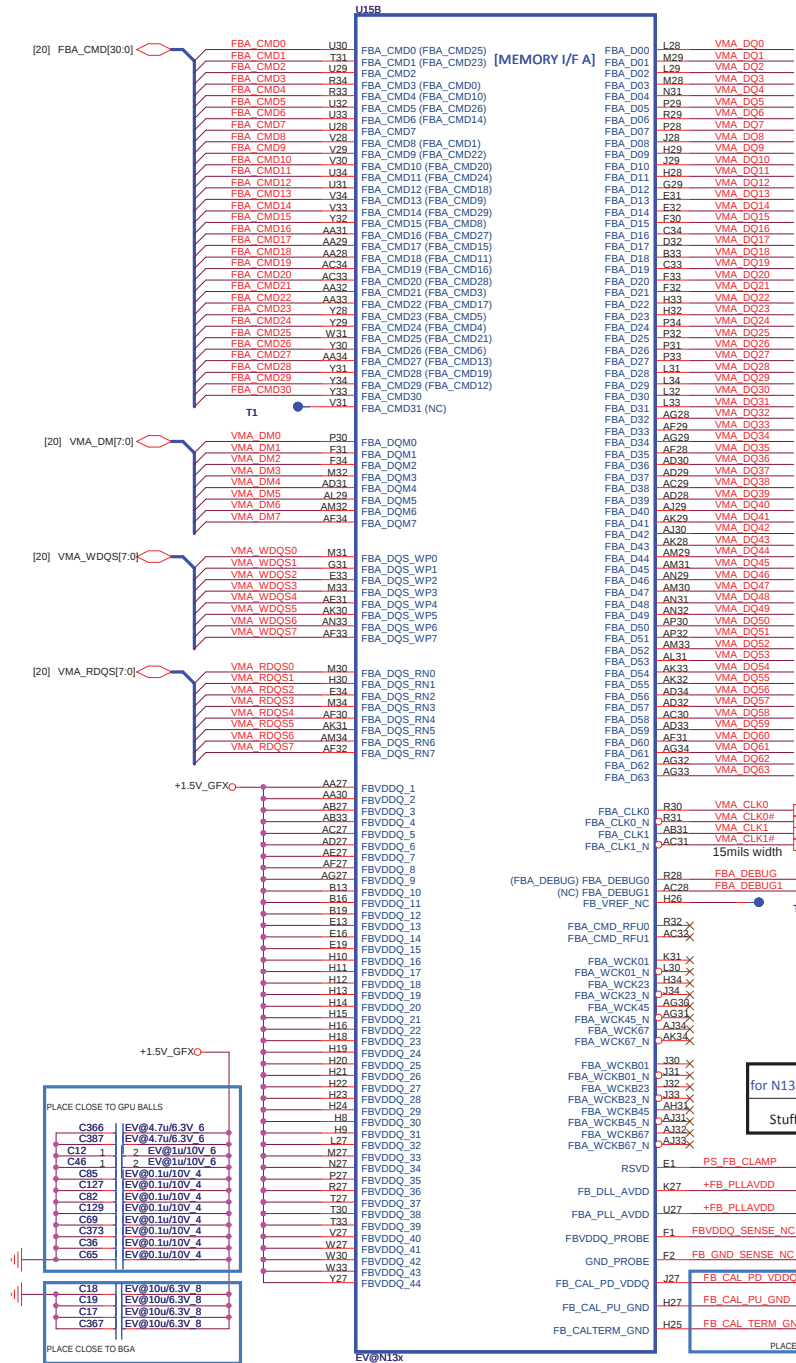


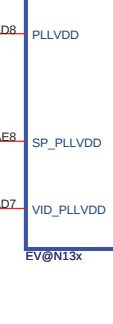
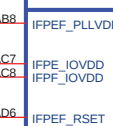
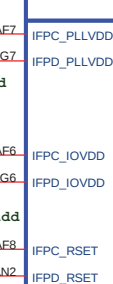
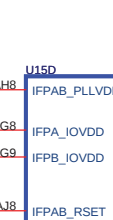
Figure 3-18. PEX_RST_N Timing for GPU
Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T _{PERST_CLK_G}	T _{PERST_CLK_G} ≥ 1μs	
T _{PERST_CLK_G}	T _{PERST_CLK_G} ≥ 1T _{REF_CLK}	

	for N13P/M-GS	for N13P-GL
Stuff--> R	Reserve--> R	
Reserve -->L	Stuff--> L	







EV_TXLCLK- [22]
 EV_TXLCLK+ [22]
 EV_TXLOUT0- [22]
 EV_TXLOUT0+ [22]
 EV_TXLOUT1- [22]
 EV_TXLOUT1+ [22]
 EV_TXLOUT2- [22]
 EV_TXLOUT2+ [22]



 Quanta Computer Inc. PROJECT : ZQTA/ZQSA	
Size	Document Number DGPU 3/5 (Display)
Date:	Friday, November 11, 2011 Sheet 17 of 44

[15,17,19,39,40] +3V_GFX

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

N13P-GL	AJ0N13P0T02
N13P-GS	AJ001070T00
N13M-GS	AJ001170T00

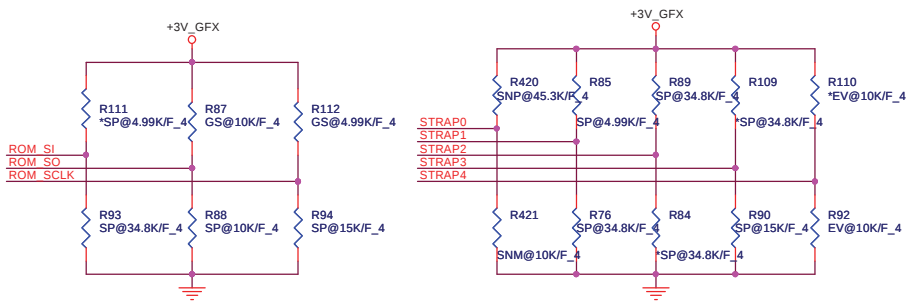
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1110
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0010
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	0011

STRAP2
N13P-GL (1001) ----> 10k PU
N13P-GS (1011) ----> 20K PU

STRAP1
N13P-GL (0111) ----> 45.3K PD
N13P-GS (0110) ----> 34.8K PD

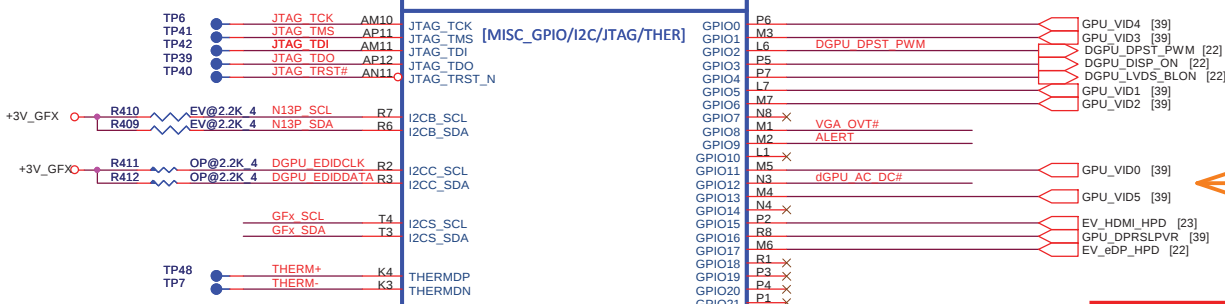
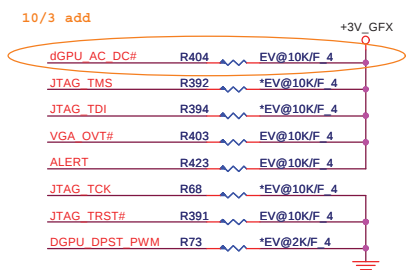
STRAP3
Optimus ----> 4.99k PD
Discrete only ----> 15K PD

Resistor P/N
4.99K----> CS24992FB26
10K ----> CS31002FB26
15K ----> CS31502FB24
20K ----> CS32002FB29
34.8K----> CS33482FB22
45.3K ----> CS34532FB18



N13P-GS/-GL Strapping table

ROM_SI 1G Hynix 64Mx16 1G Micron 64Mx16 2G Hynix 128Mx16 2G Micron 128Mx16	-->15K PD -->20K PD -->35K PD (Default) -->45K PD	ROM_SO N13P-GL --> 10K PD N13P-GS --> 10K PU	ROM_SCLK N13P-GL (0010) ----> 15k PD N13P-GS (1000) ----> 4.99K PU
--	--	--	--

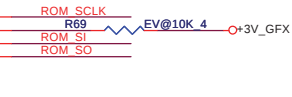
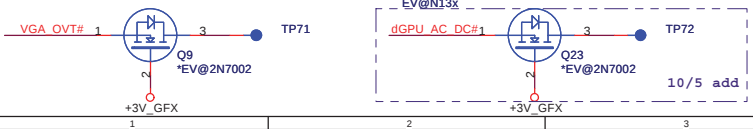


N13M-GS Strapping table

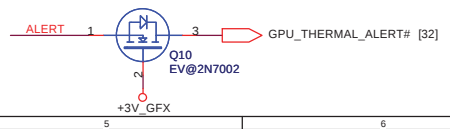
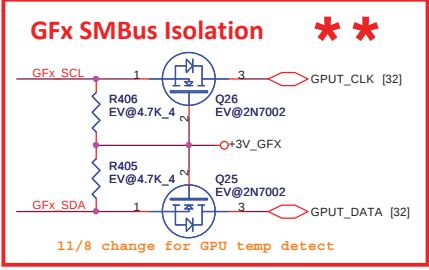
Pin Name	Strap Mapping	Value
ROM_SCLK	SMB_ALT_ADDR	0
ROM_SI	SUB_VENDOR	0
ROM_SO	VGA_DEVICE	0
STRAP[3..0]	RAM_CFG[3..0]	0010(Hynix 64Mx16) 0110(Hynix 128Mx16)
STRAP[4]	PCIE_MAX_SPEED	0

Remark :
0 -> 10K PD
1 -> 10K PU

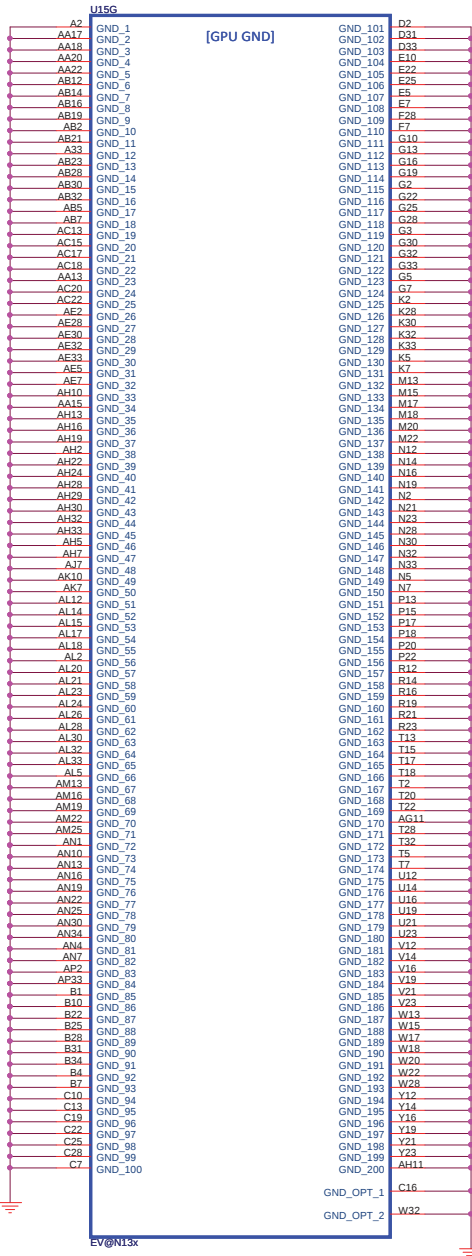
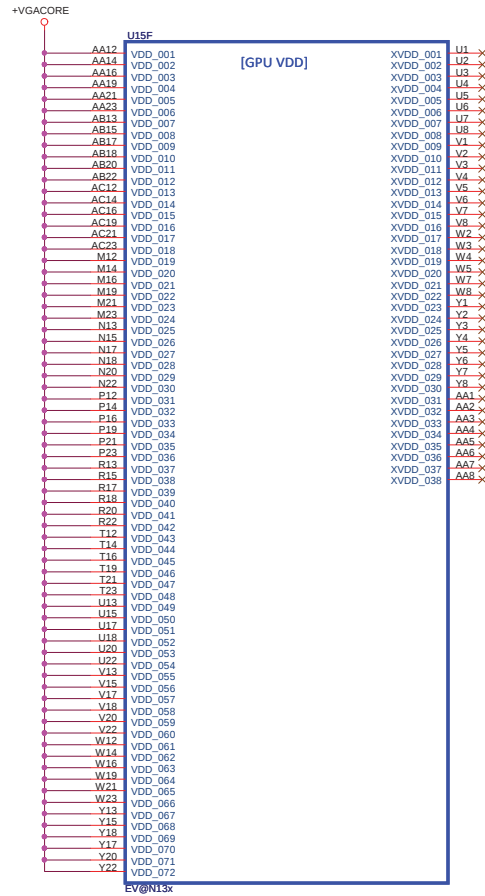
R422	
N13P-GS/GL	40.2K
N13M-GS	NC



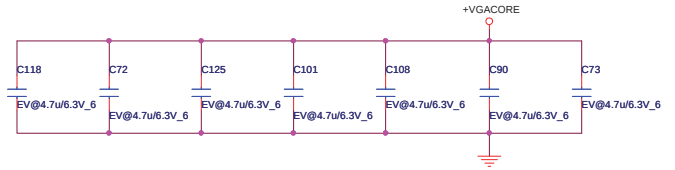
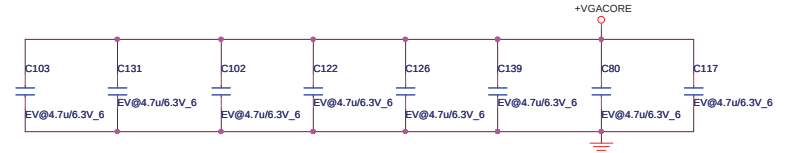
for N13P/M-GS	for N13P- GL
Reserve R108	Stuff R108



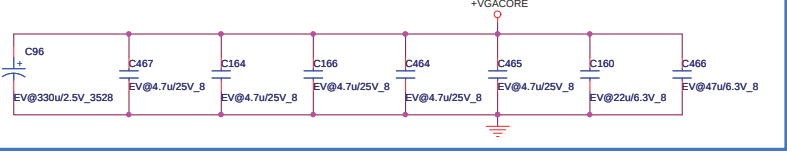
N13P-GL	AJON13POT02
N13P-GS	AJON13POT07
N13M-GS	AJON13MOT08



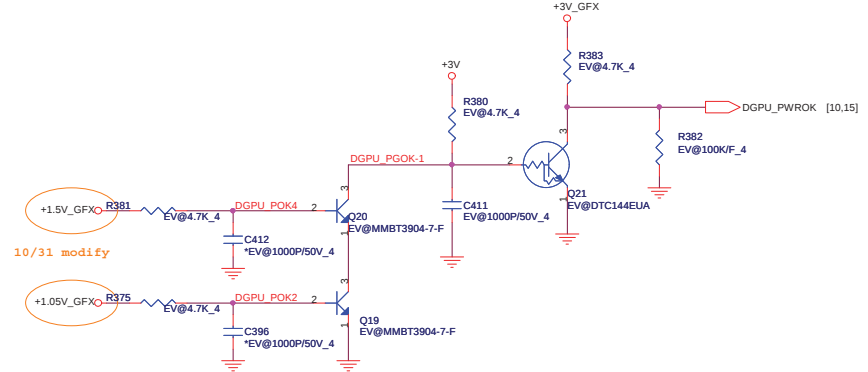
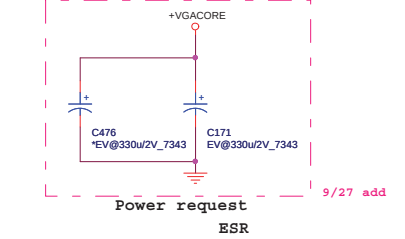
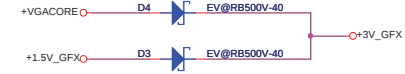
PLACE UNDER GPU



PLACE NEAR GPU



for meet Power down sequence for +3V_GFX

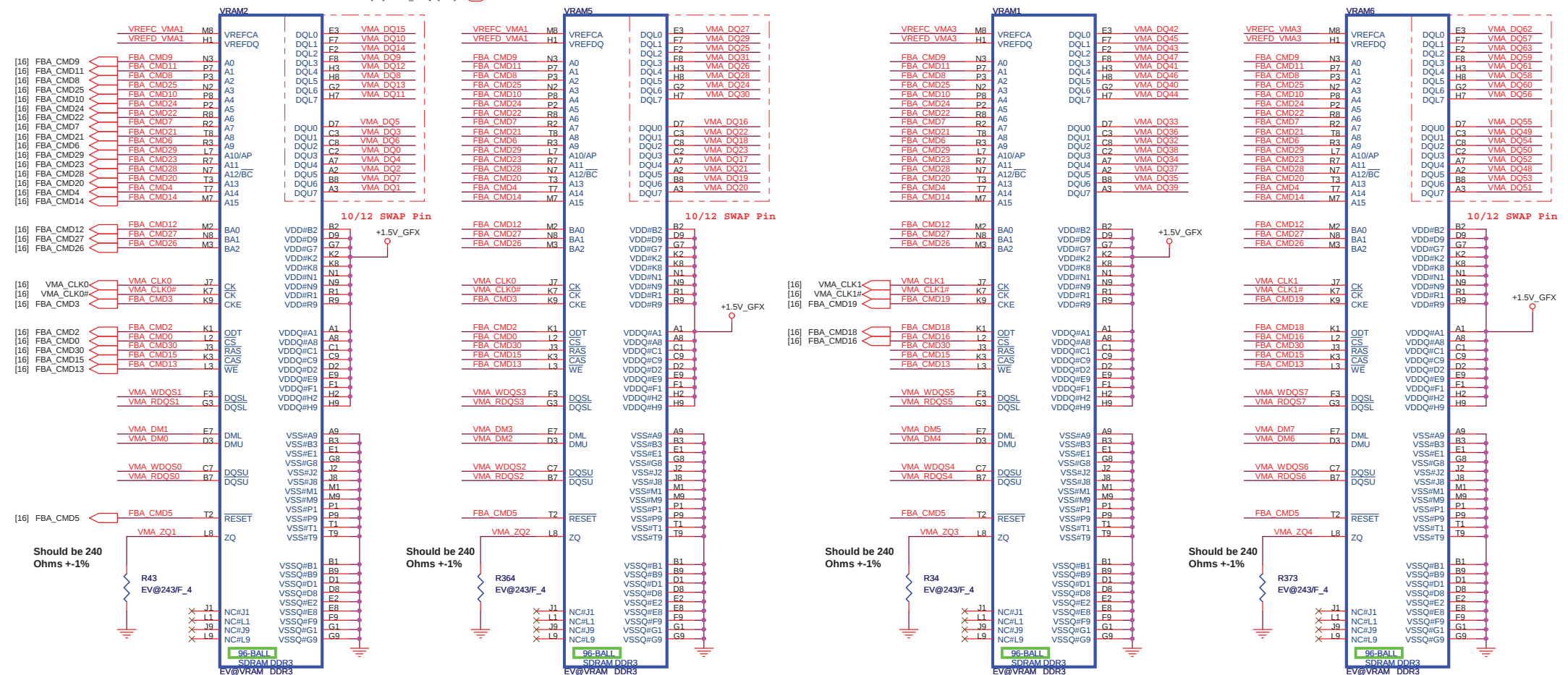


10/31 modify

[31.39] +VGACORE
[15.16,17,40] +1.05V GFX
[16.20,21,40] +1.5V GFX
[15.17,18,39,40] +3V GFX
[3,7,8,9,10,11,13,14,22,23,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V

[16] VMA_DQ[63..0]
[16] VMA_DM[7..0]
[16] VMA_WDQS[7..0]
[16] VMA_RDQS[7..0]

CHANNEL A: 256MB/512MB DDR3



Should be 240 Ohms +-1%

R43 EV@243/F_4

VMA_CLK0

R371 EV@162/F_4

VMA_CLK0#

Fermi : Change to 160 ohm

1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)

2 : CS11622PB07 ,RES CHIP 162 1/16W +-1% (0402)

Should be 240 Ohms +-1%

R34 EV@243/F_4

VMA_CLK1

R41 EV@162/F_4

VMA_CLK1#

Fermi : Change to 160 ohm

1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)

2 : CS11622PB07 ,RES CHIP 162 1/16W +-1% (0402)

Should be 240 Ohms +-1%

R373 EV@243/F_4

VMA_CLK1

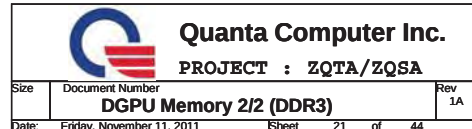
R370 EV@162/F_4

VMA_CLK1#

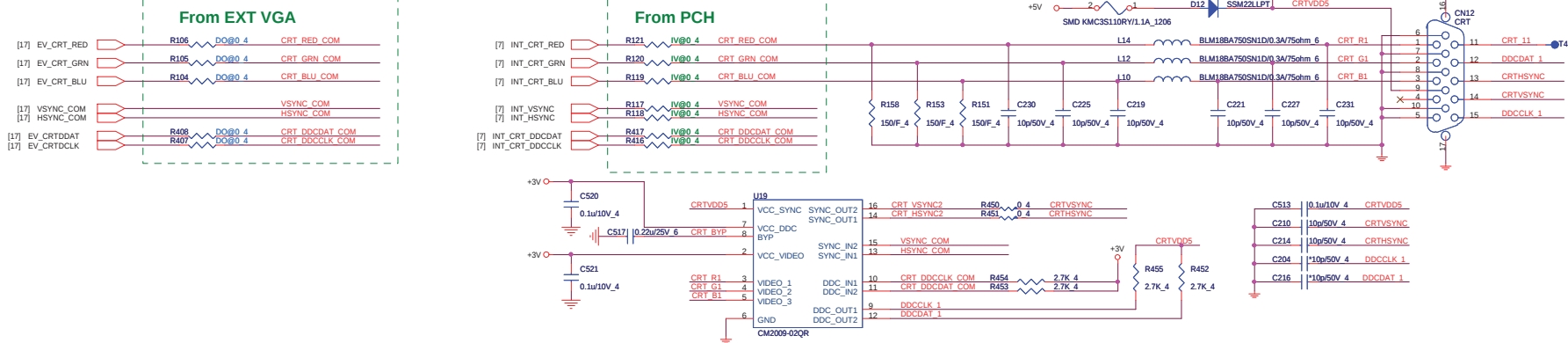
Fermi : Change to 160 ohm

1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)

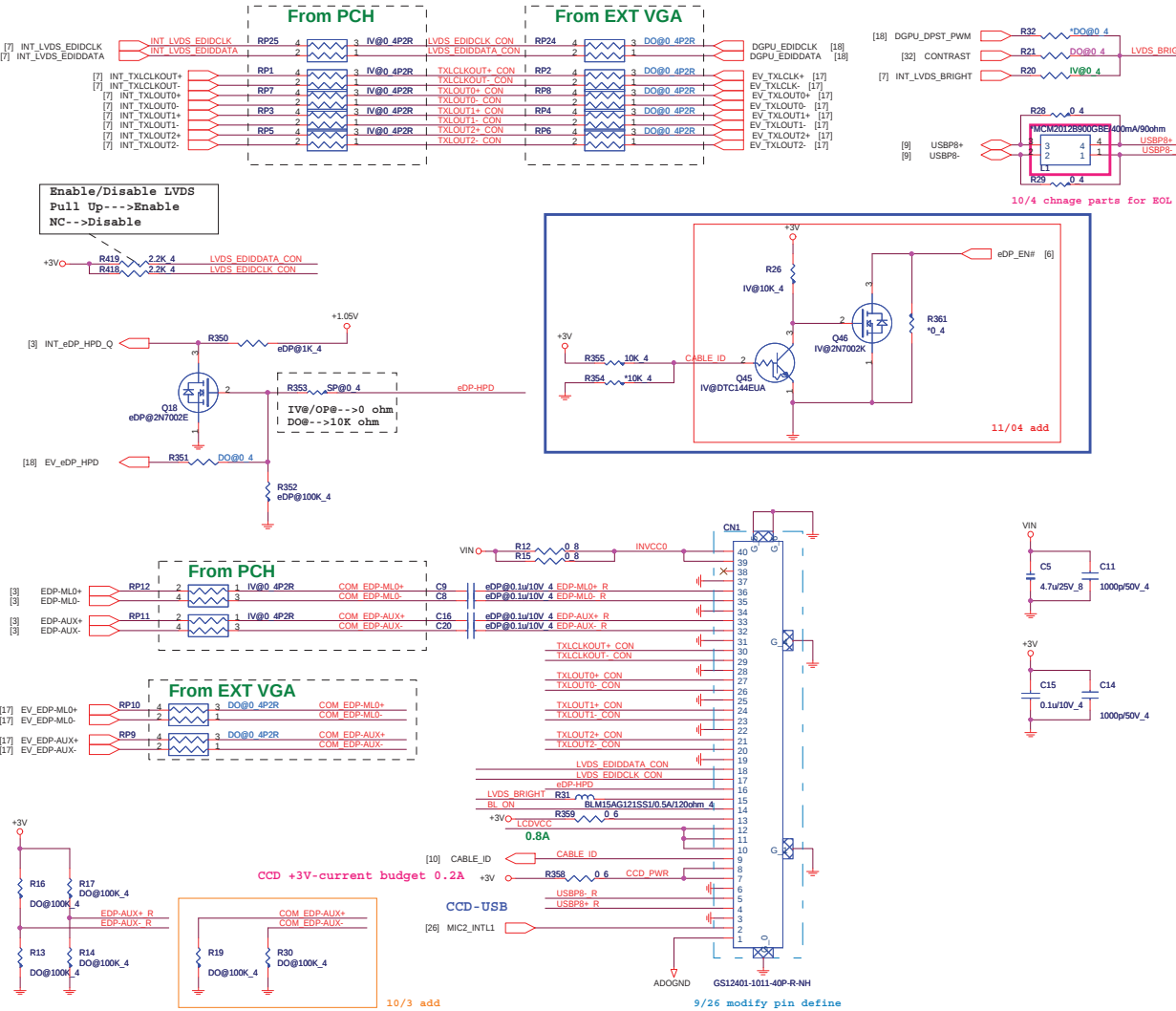
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1% (0402)



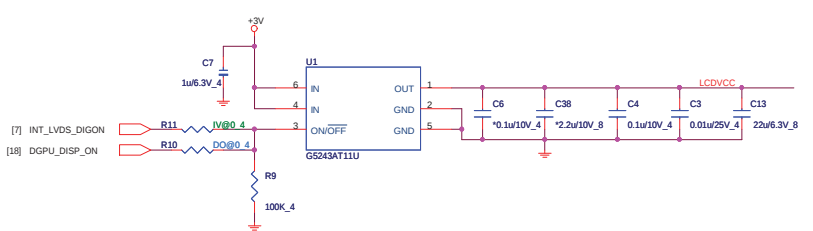
CRT



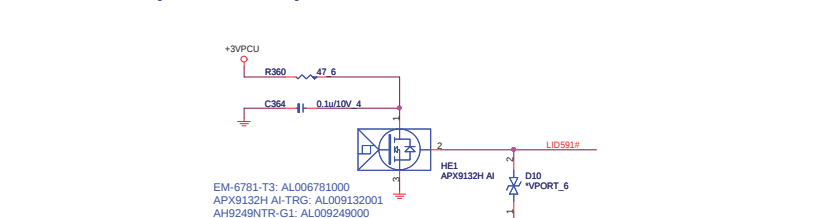
LVDS & eDP



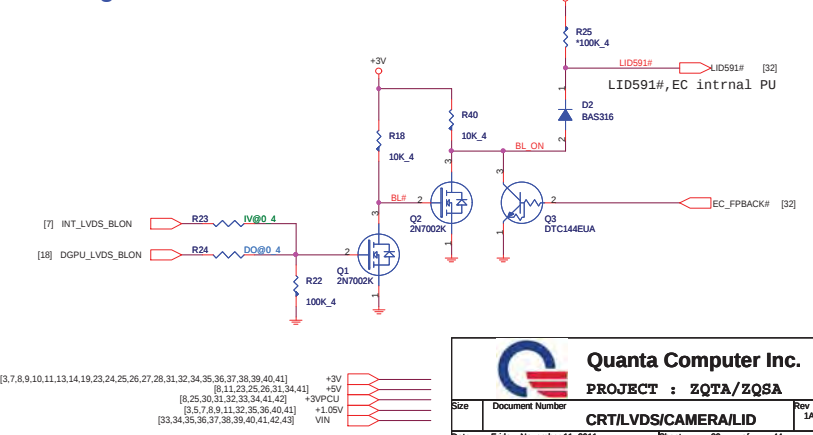
LCD Power



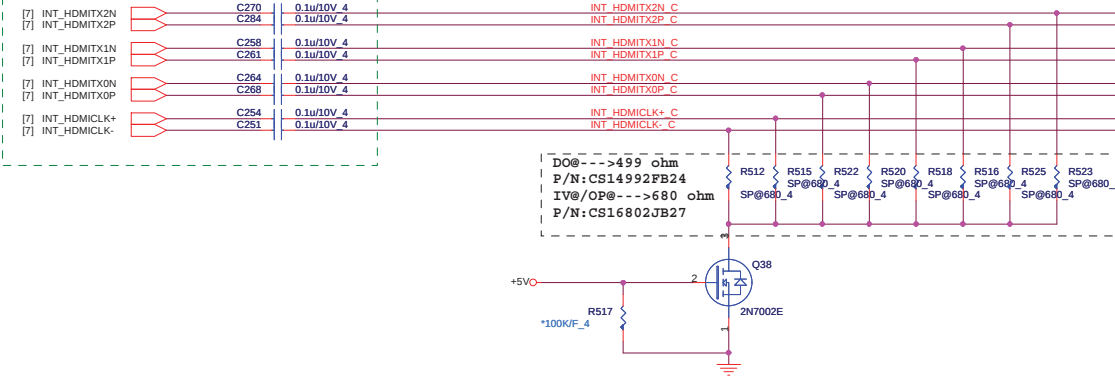
Lid Switch (Hall sensor)



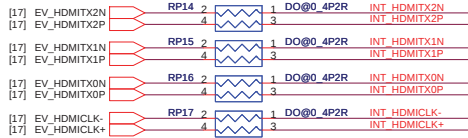
Backlight Control



From PCH

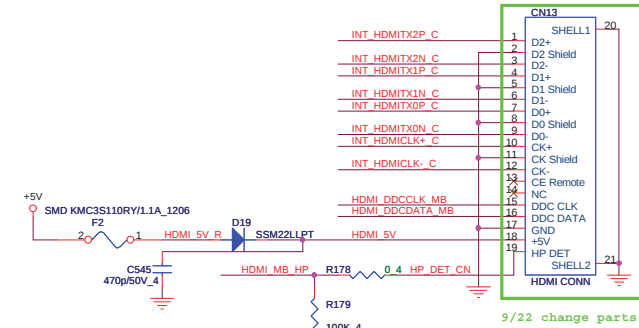


From EXT VGA

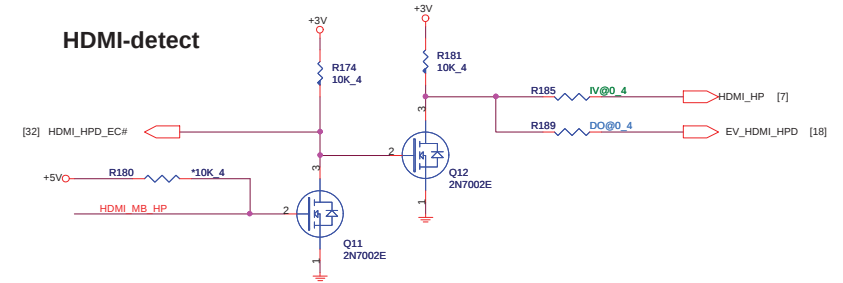


IV@:iGPU
EV@:dGPU
OP@:Optimus
DO@:Discrete only
SP@:Special

HDMI connector



HDMI-detect



I2C

UMA	R239	CS22202JB18
	R245	
DIS	R239	CS24702JB38
	R245	

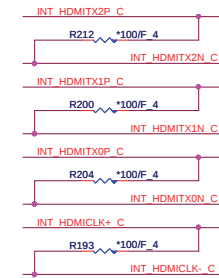
From EXT VGA



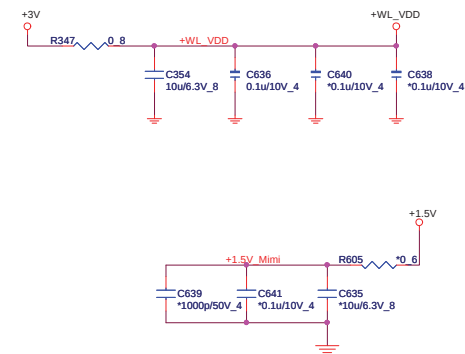
From PCH



EMI

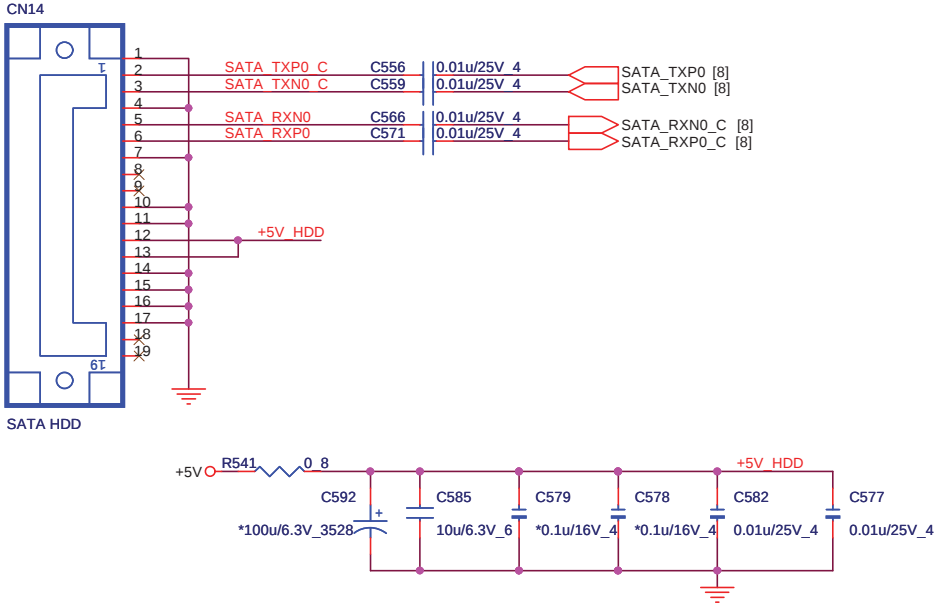


+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

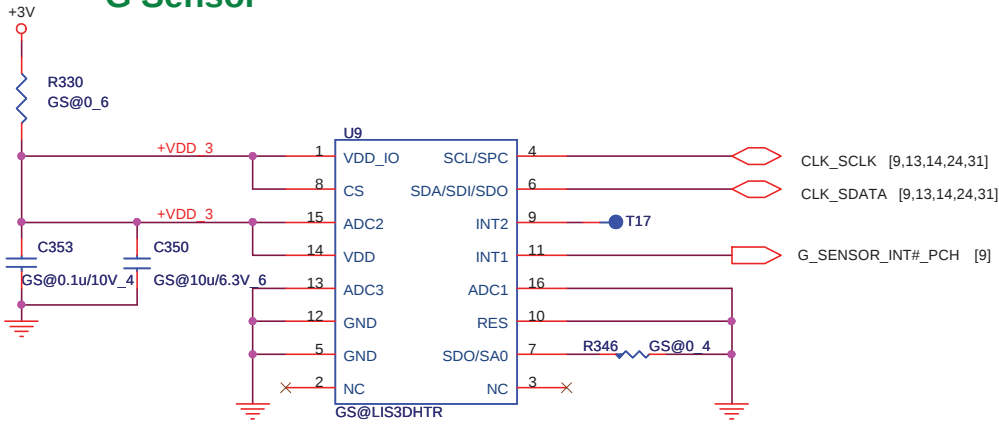


The schematic diagram illustrates the electrical connections for the USB3+ mini-card module. The module is a central component with pins numbered 1 to 54. It is powered by a +3V_SATA source through a series of capacitors (C616, C615, C647) and a resistor (R615). The module also has a +3V_SATA input and a USB3+ / USBP- output. Various pins are labeled with functions such as LED_WPAEN#, LED_WLAN#, LED_WWAN#, USB_D+, USB_D-, SMB_DATA, SMB_CLK, +3.3Vaux, GND, UIM_C4, UIM_C8, UIM_VPP, UIM_RESET, UIM_CLK, UIM_DATA, UIM_PWR, +1.5V, GND, W_DISABLE#, and WAKE#. The module is connected to a MINI-CARD1 connector at the bottom, which is further connected to a GND plane.

MAIN SATA HDD(HDD)

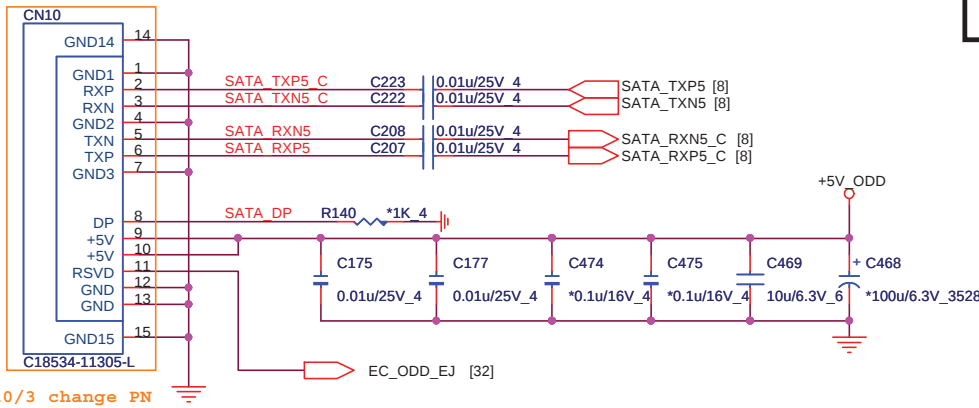


G Sensor

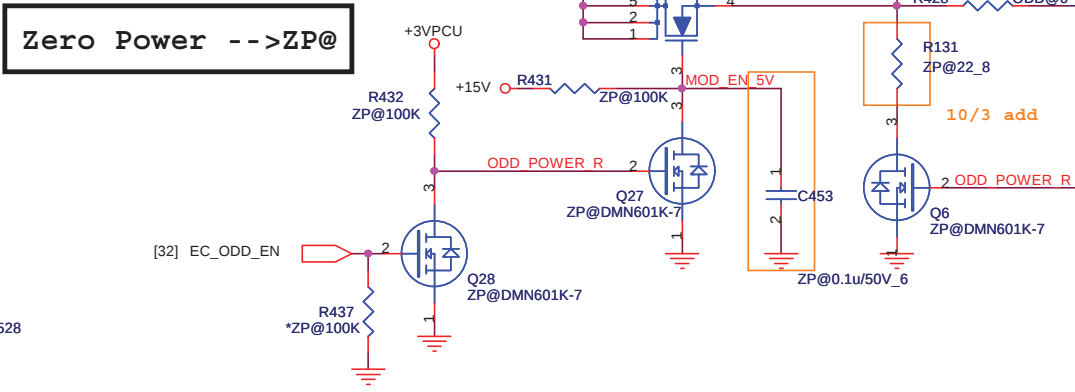


G-Sensor -->GS@

ODD (ODD)



Zero Power (ODD)



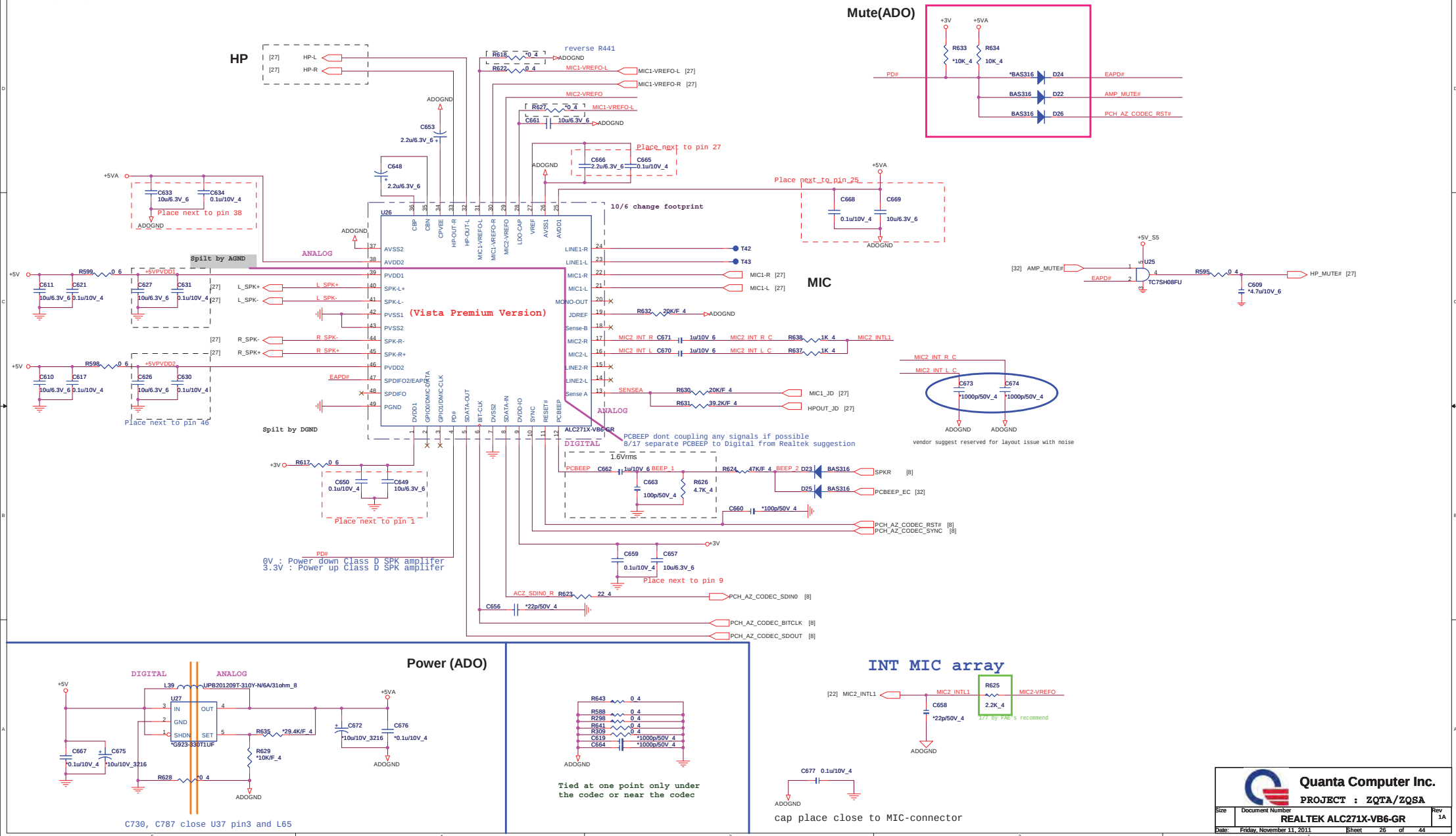
Zero Power -->ZP@



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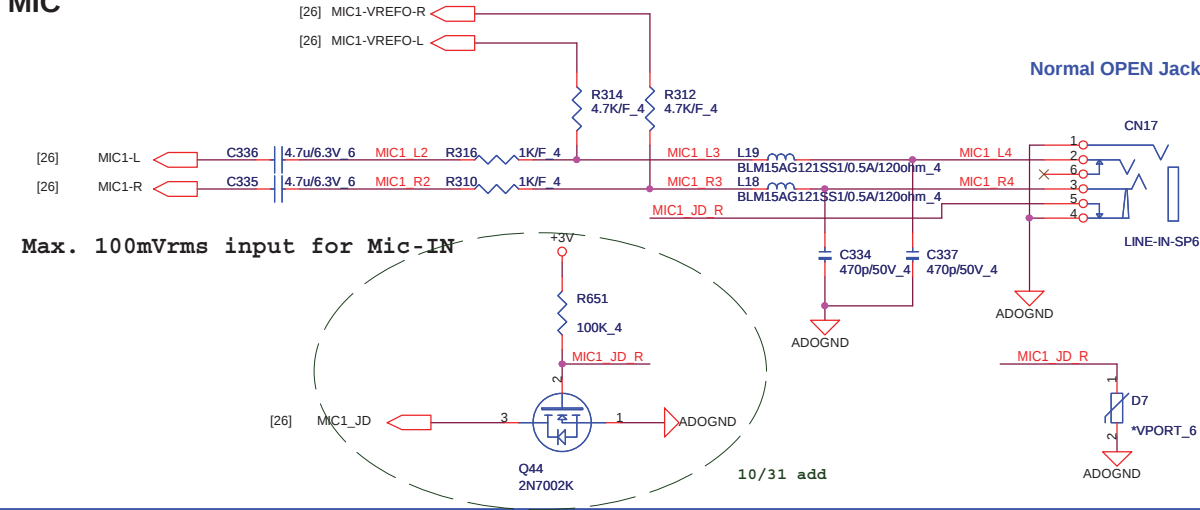
Size	Document Number	Rev
	SATA-HDD/ODD/G Sensor	1A
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Codec(ADO)

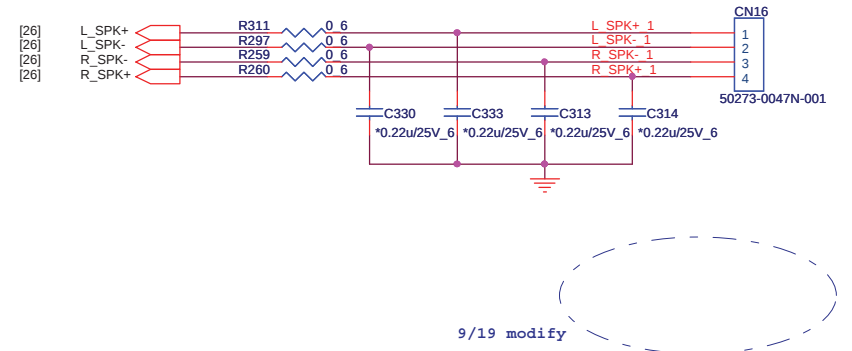


MIC

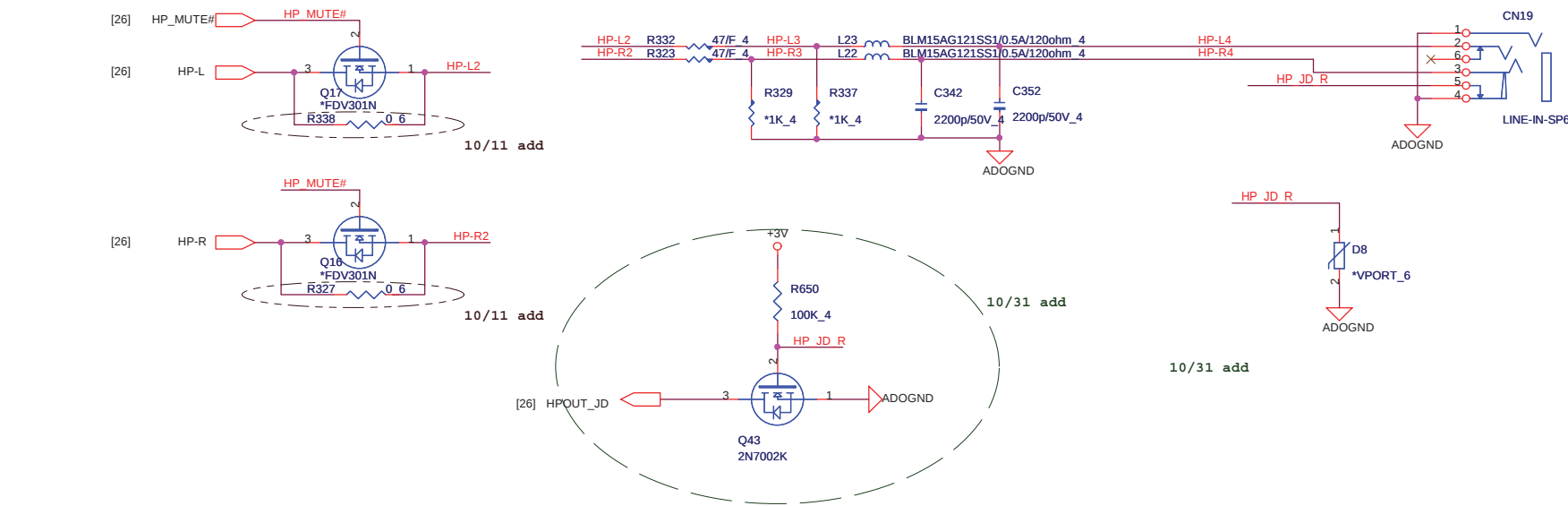
Max. 100mVrms input for Mic-IN



Internal Speaker



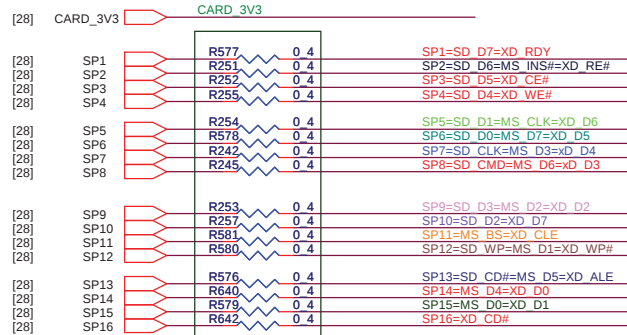
HP



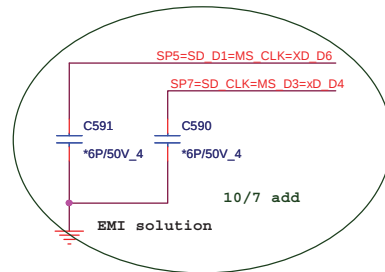
CARD READER CONNECTOR

Share Pin

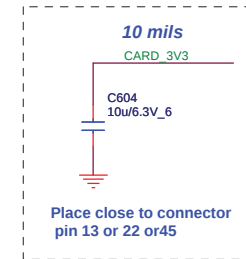
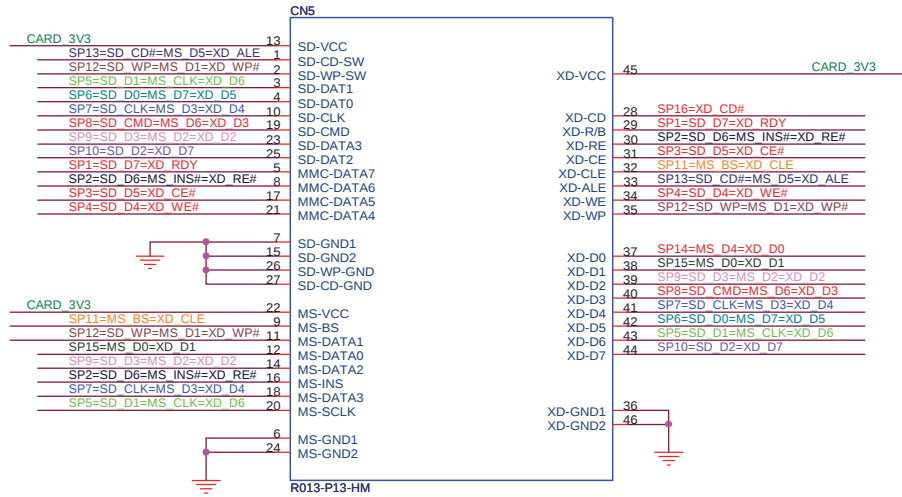
SP1	SD_D7		xD_RDY
SP2	SD_D6	MS_INS#	xD_RE#
SP3	SD_D5		xD_CE#
SP4	SD_D4		xD_WE#
SP5	SD_D1	MS_CLK	xD_D6
SP6	SD_D0	MS_D7	xD_D5
SP7	SD_CLK	MS_D3	xD_D4
SP8	SD_CMD	MS_D6	xD_D3
SP9	SD_D3	MS_D2	xD_D2
SP10	SD_D2		xD_D7
SP11		MS_BS	xD_CLE
SP12	SD_WP	MS_D1	xD_WP#
SP13	SD_CD#	MS_D5	xD_ALE
SP14		MS_D4	xD_D0
SP15		MS_D0	xD_D1
SP16			xD_CD#



10/7 change 0 ohm

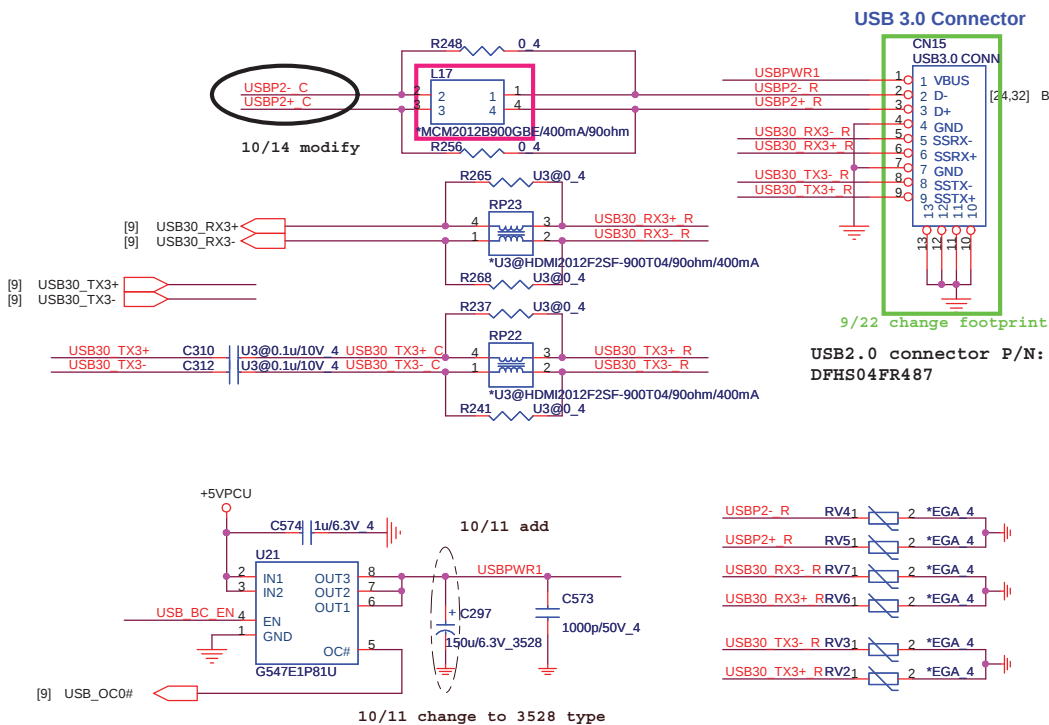


XD,MMC 4.2/SD,MS/MSP 7 IN1 CARD READER

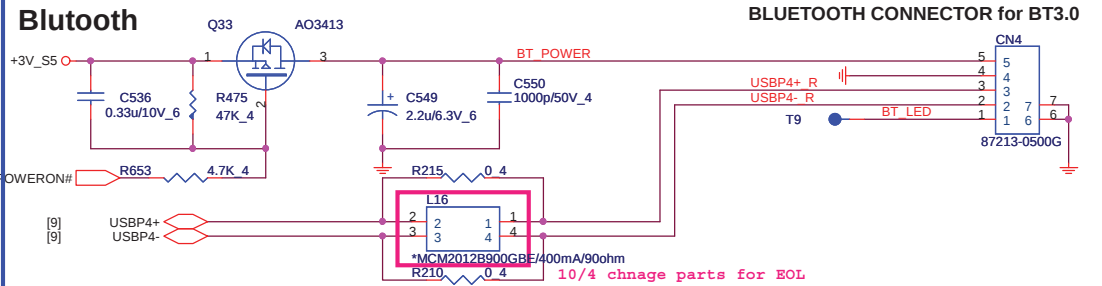


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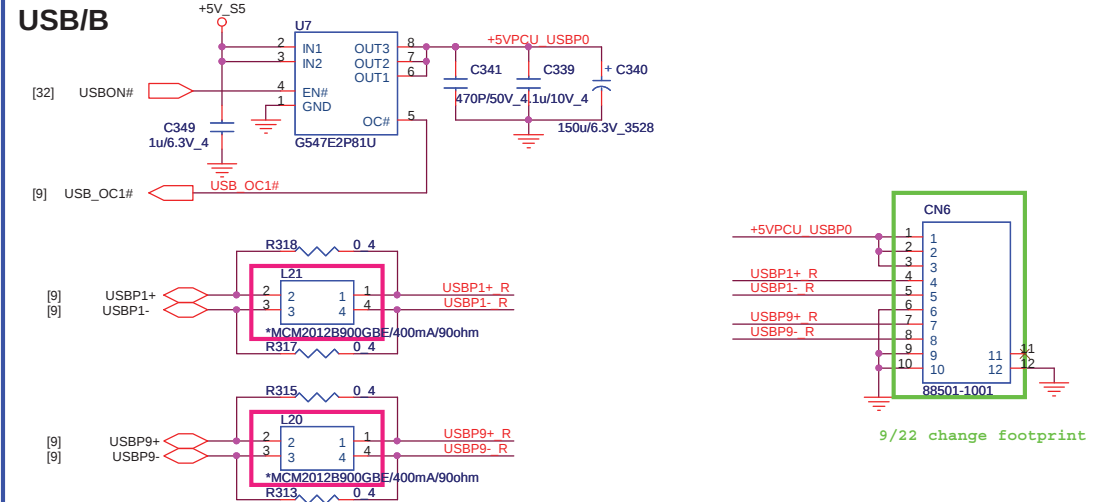
USB3.0/2.0



Bluetooth

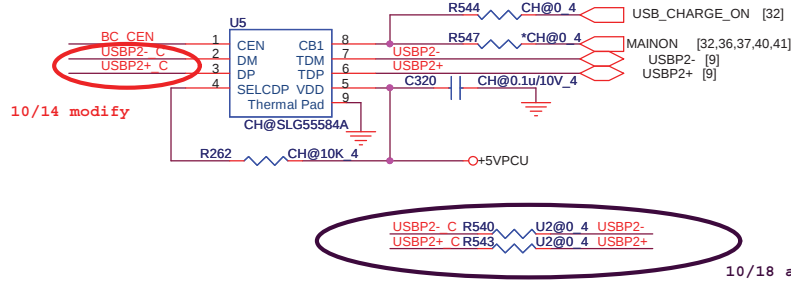


USB/B

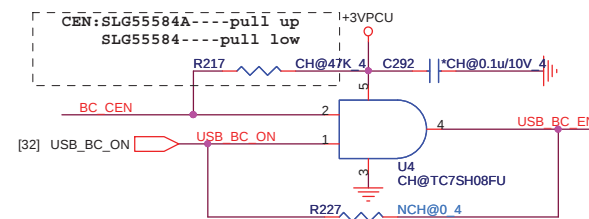


USB Charger to 3.0

CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)



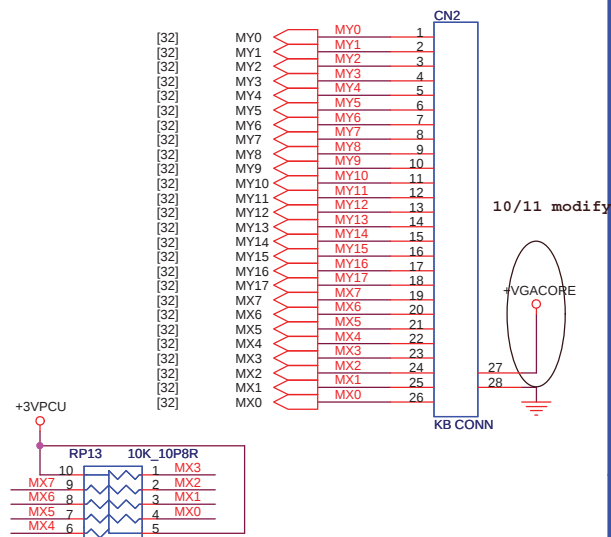
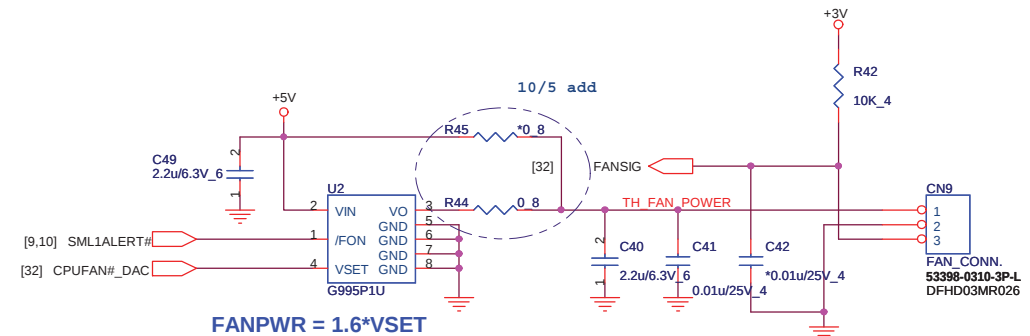
USB Charger -->CH@
None Charger--> NCH@



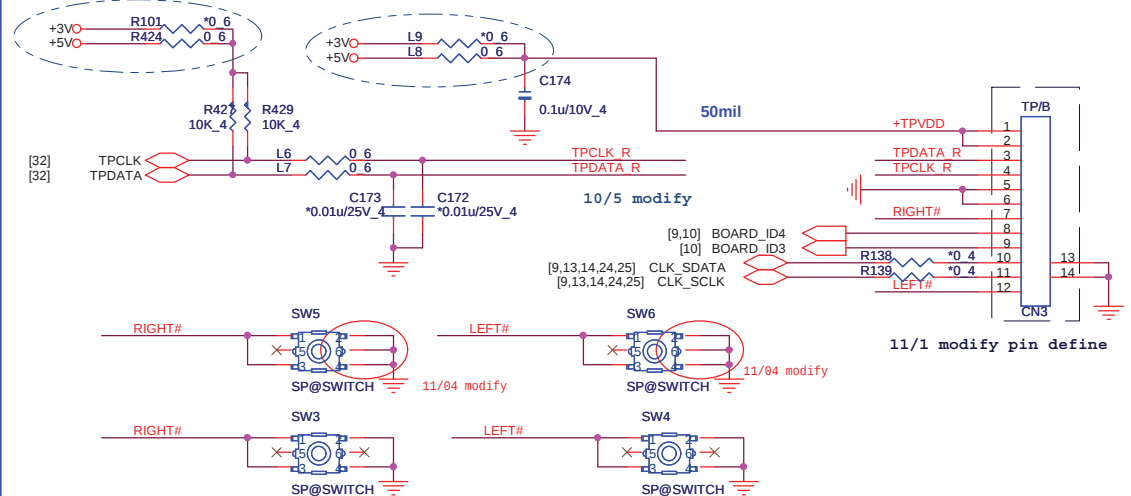
Quanta Computer Inc.
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Size Document Number
USB/ BT/CHARGER
Date: Friday, November 11, 2011 Sheet 30 of 44

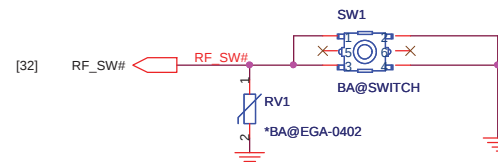
9/14 modify


$$\text{FANPWR} = 1.6 \cdot \text{VSET}$$


Model EA/EG/BA---->SW3, SW4
VA/VG----->SW5, SW6

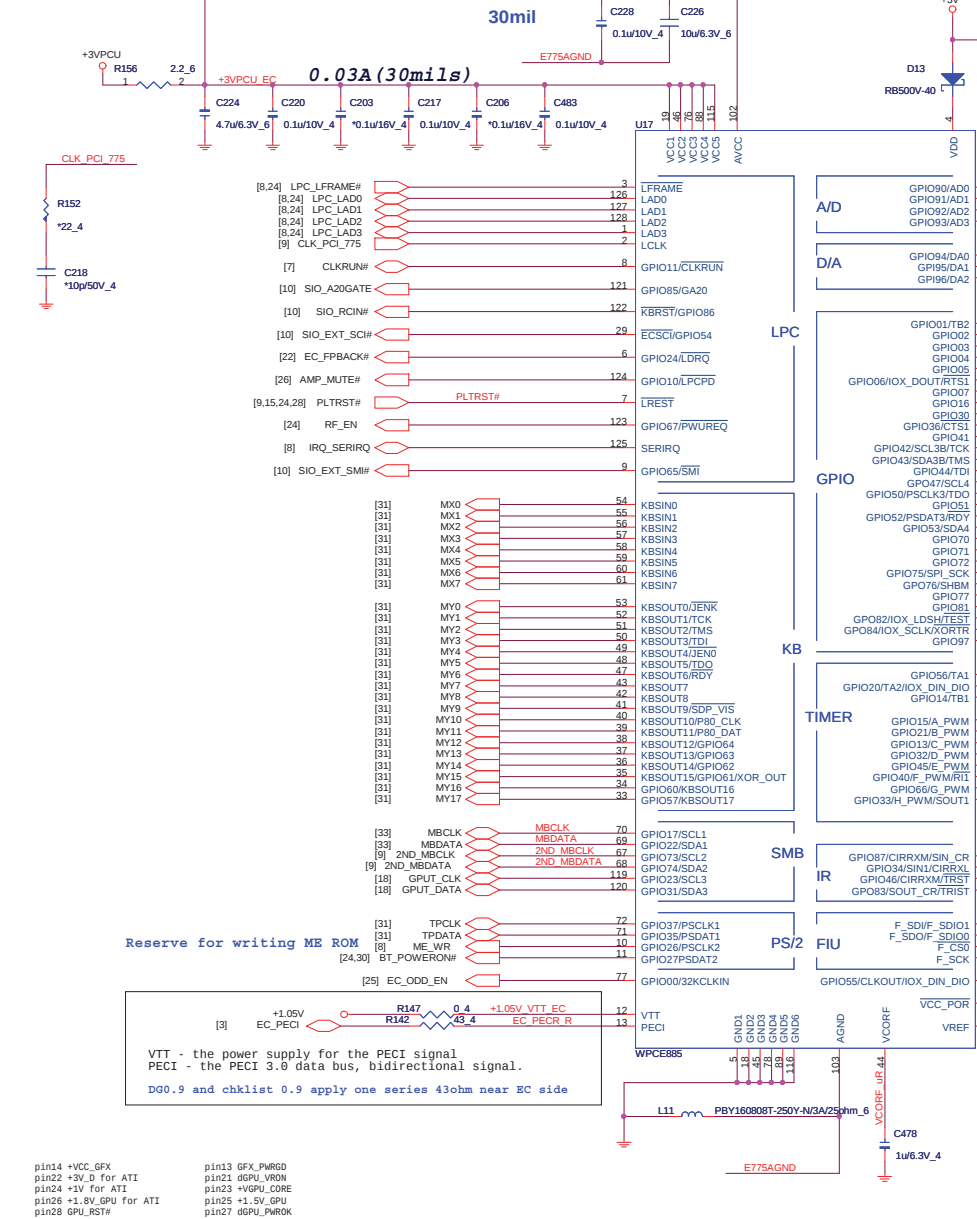


[32]



 Quanta Computer Inc. PROJECT : ZQTA/ZQSA		
Size	Document Number	Rev
	KB/FAN/TP+FP/LED	1A
Date:	Friday, November 11, 2011	Sheet 31 of 44

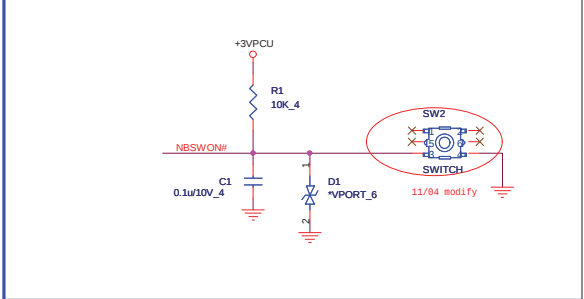
EC(KBC)



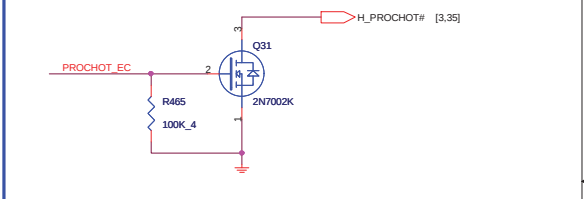
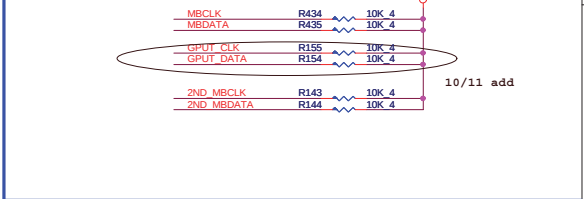
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA
SM Bus 4	HDMI

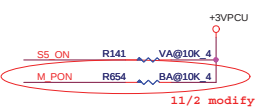
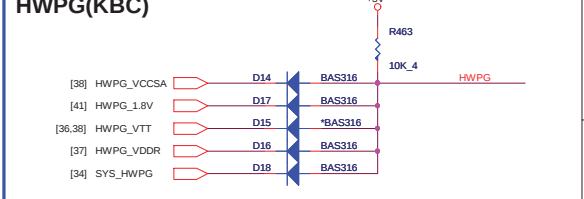
Power on bottom

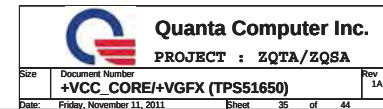


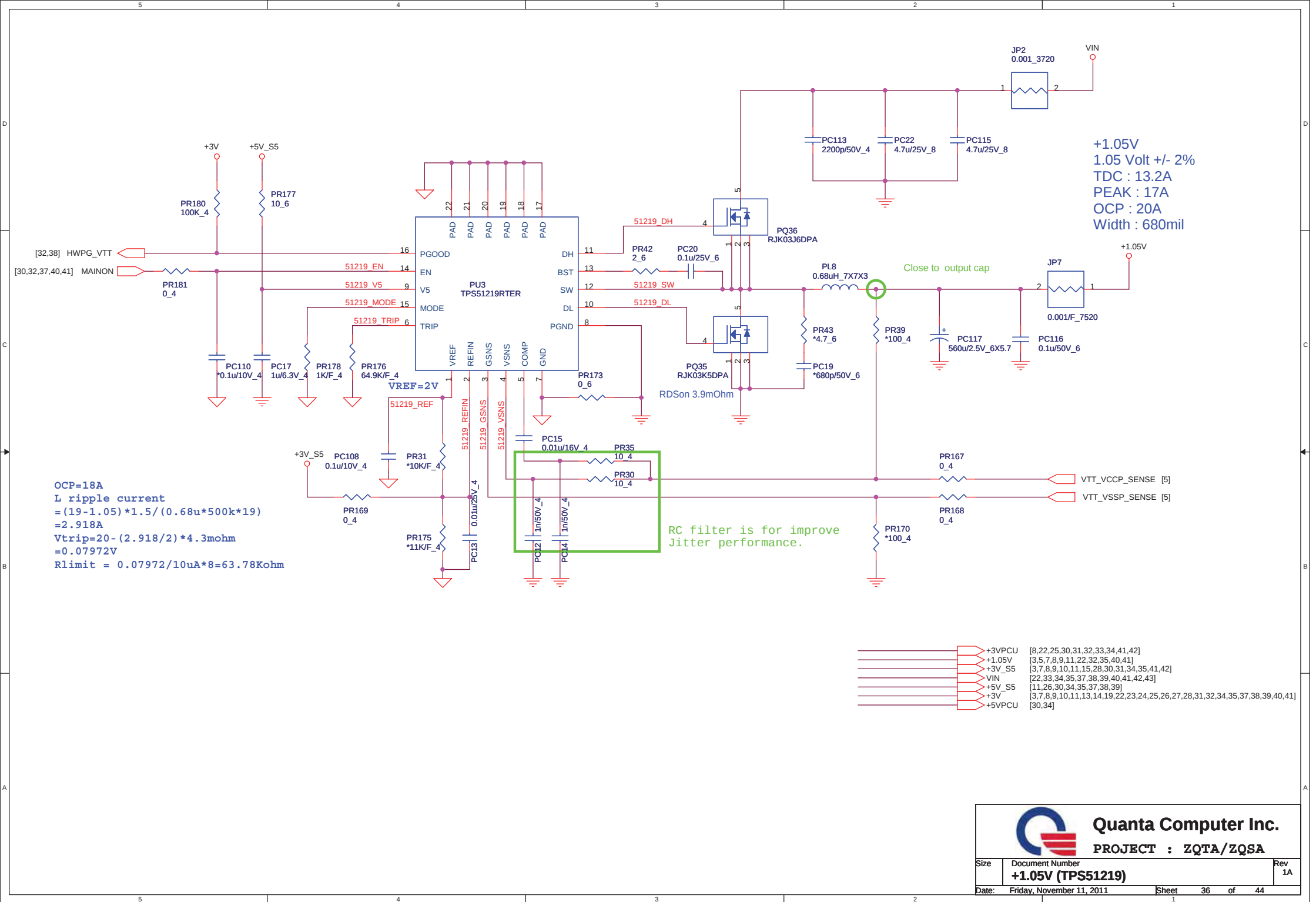
SM BUS PU(KBC)



HWP (KBC)







TDC : 0.38A
PEAK : 0.5A
Width : 20mil

TDC : 0.75A
PEAK : 1A
Width : 40mil

+SMDDR_VREF

PC182
0.22u/10V_4

PR265
100K/F_4

VREF=1.8V

PC183
0.1u/10V_4

PR140
10K/F_4

PR260
51K/F_4

PC181
0.01u/25V_4

PC85
10u/6.3V_8

PC86
10u/6.3V_8

Close to IC

Greater than or equal 40mil

+5V_S5

PC87
1u/10V_4

PC184
10u/6.3V_8

JP18
0.001_3720

PC194
4.7u/25V_8

JP17
0.001/F_7520

+1.5V_SUS
1.5 Volt +/- 5%
TDC : 14.67A
PEAK : 18A
OCP : 20A
Width : 600mil

Close to output cap

+1.5VSUS

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

PQ18
AO3404

OCP=20A
I ripple current
= (19-1.5)*1.5/(0.68u*400k*19)
=5.079A
Vtrip=20-(5.079/2)*4.3mohm
=0.07508V
Rlimit=0.07508/10uA*8=60.063Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

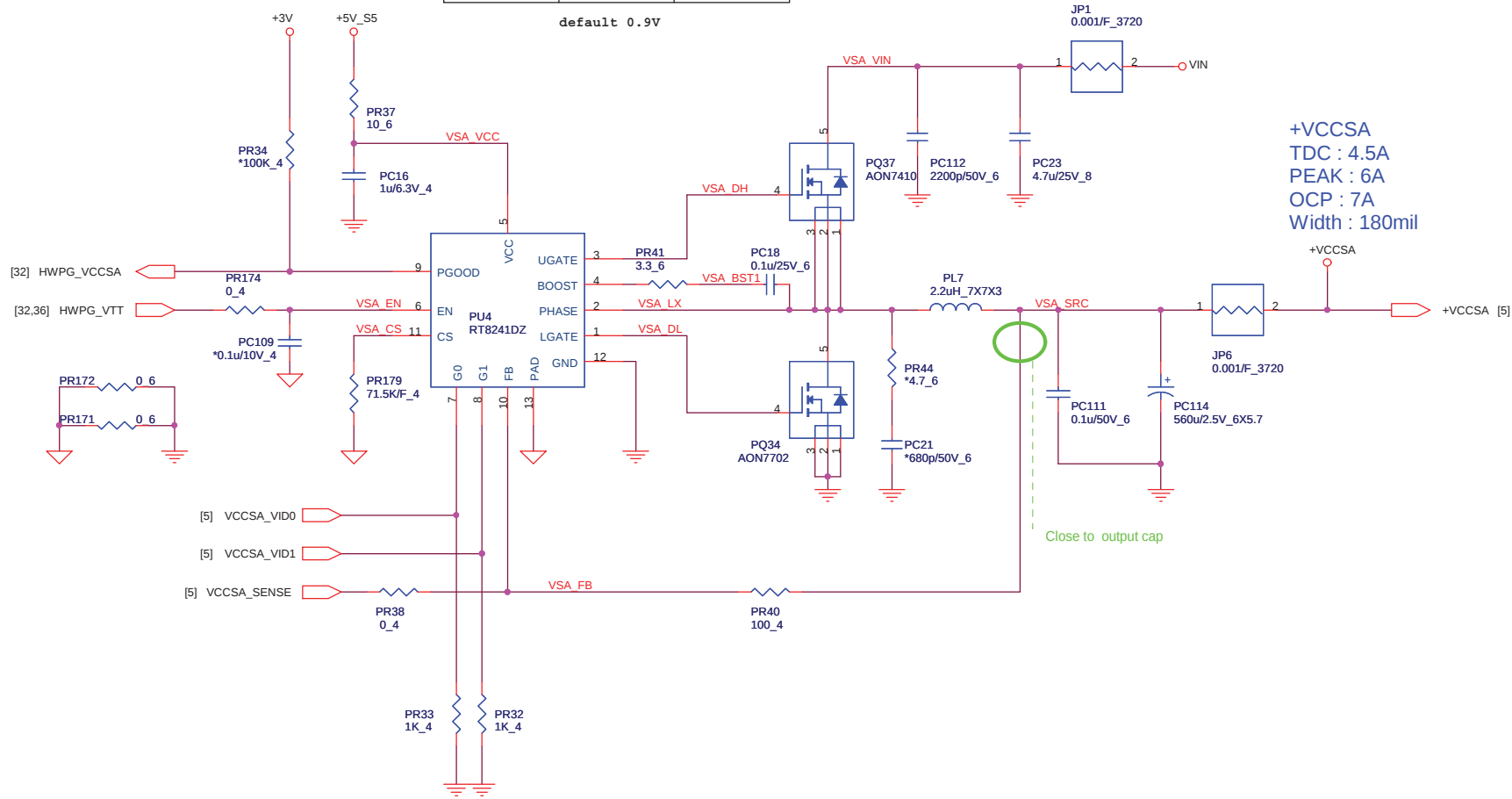


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Size	Document Number	Rev
	DDR 1.5V(TPS51216)	1A
Date	Friday, November 11, 2011	Sheet 37 of 44

G0	G1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V



+VCCSA
TDC : 4.5A
PEAK : 6A
OCP : 7A
Width : 180mil

Close to output cap

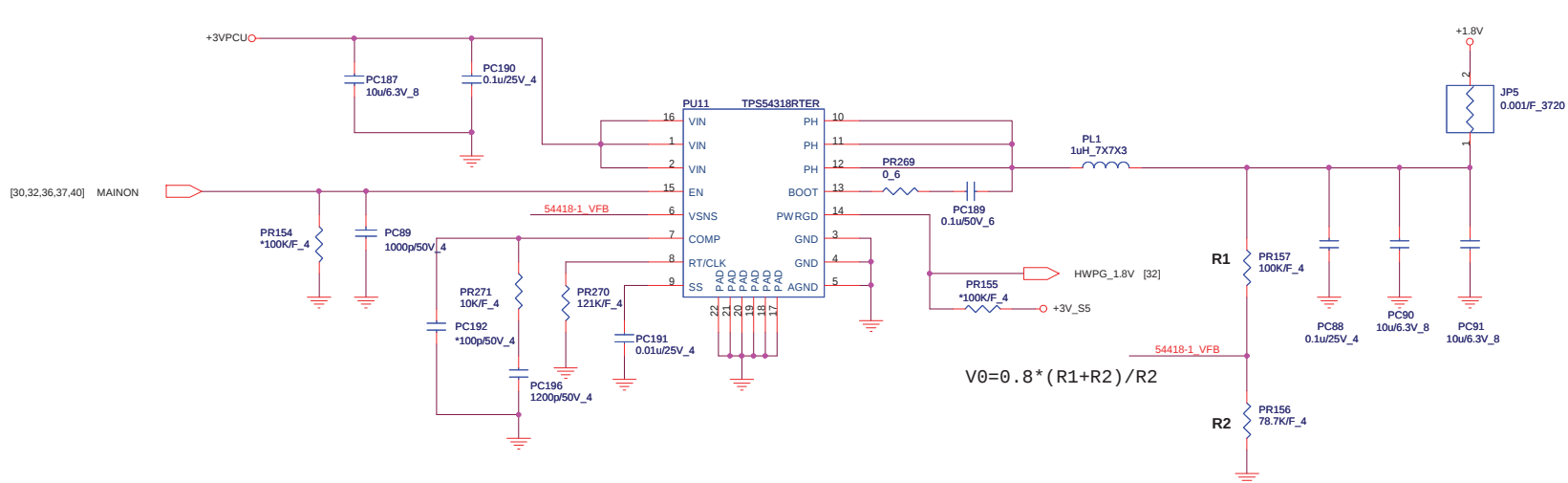
OCP=7A
Iripple=(19-0.9)*0.9/(2.2u*300K*19)
=1.299A
Rth=14mohm*8*(7-0.65)/10uA
=71.125K
Ipeak=8.299A



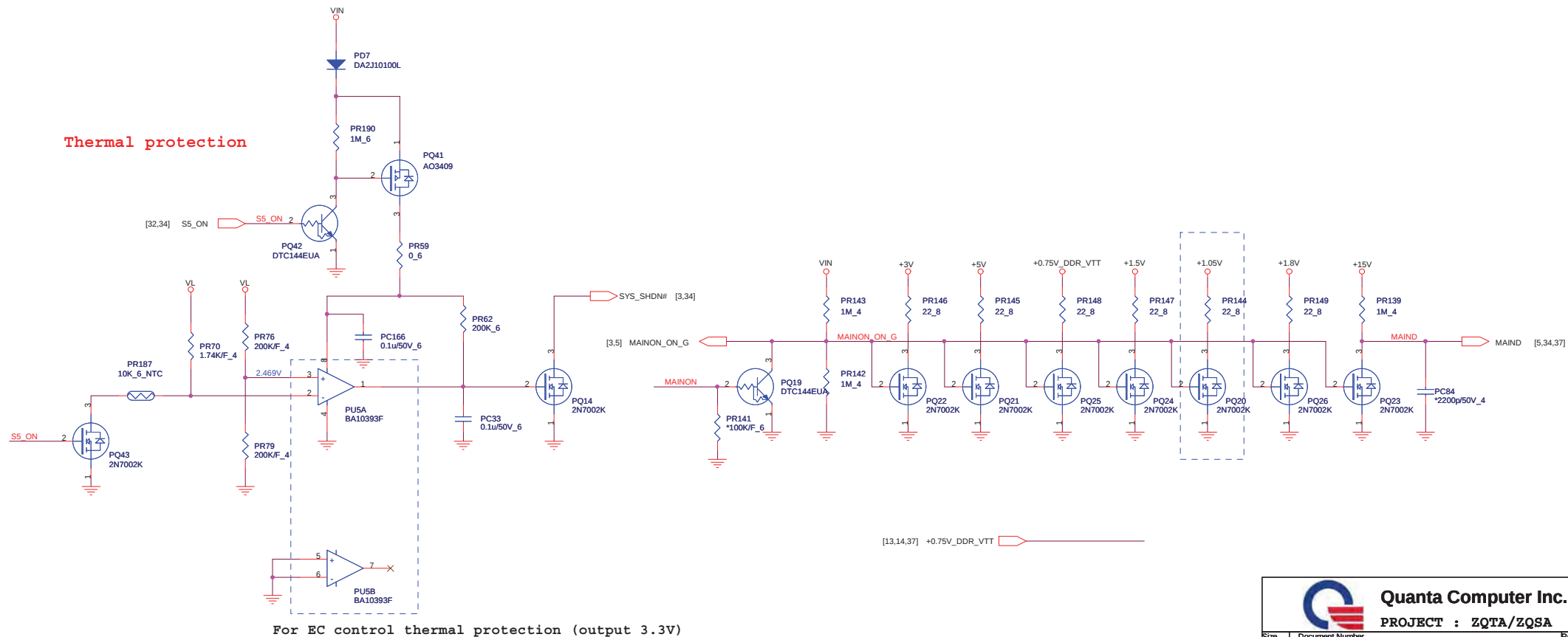
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

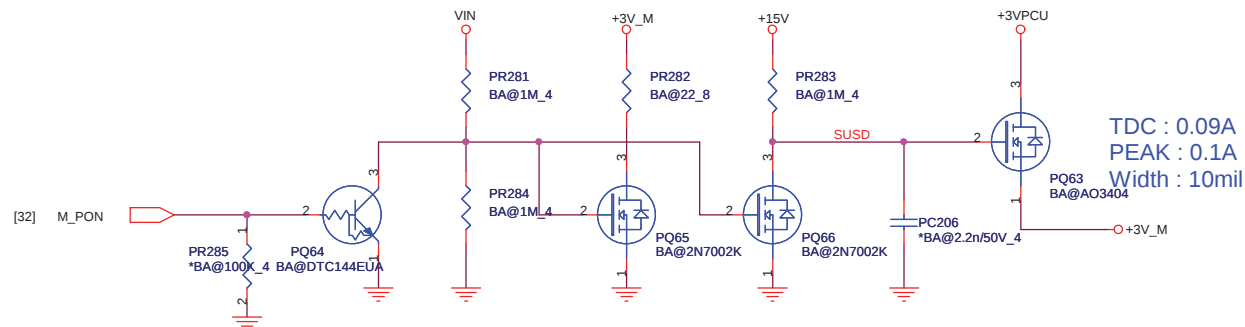
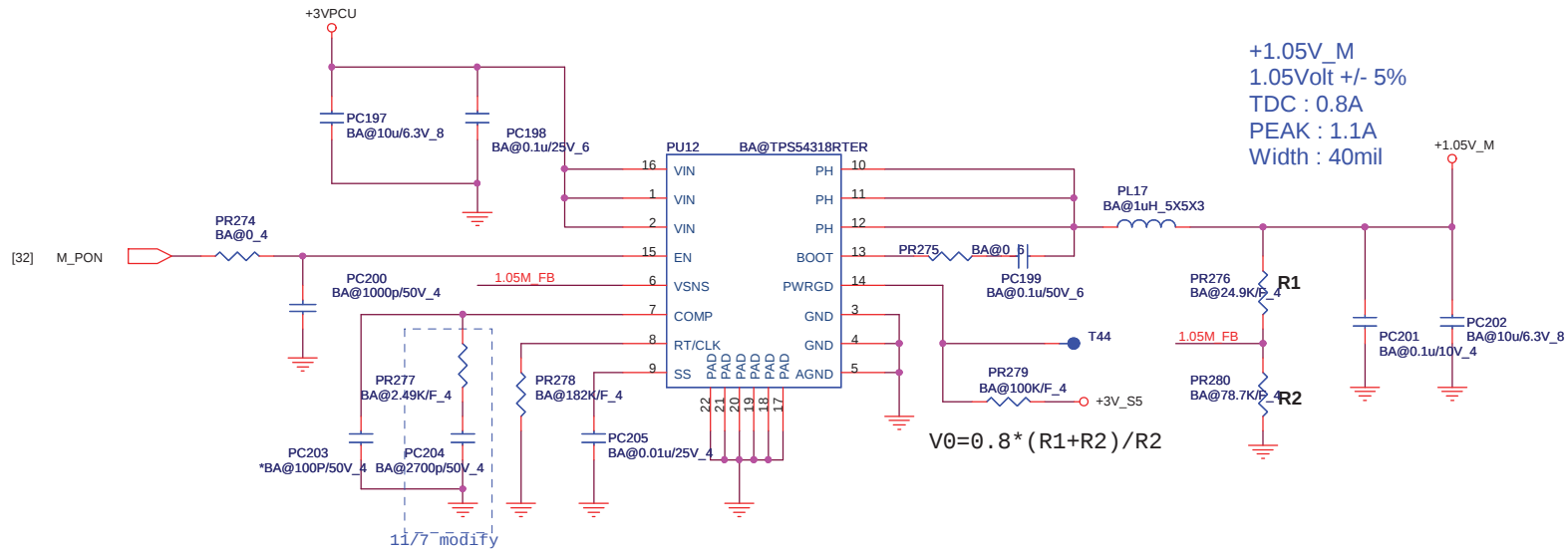
Size	Document Number	Rev
	VCCSA(RT8241DZ)	1A
Date:	Friday, November 11, 2011	Sheet 38 of 44





Thermal protection

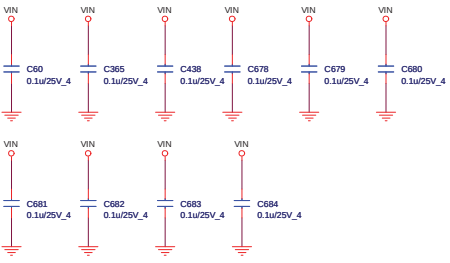
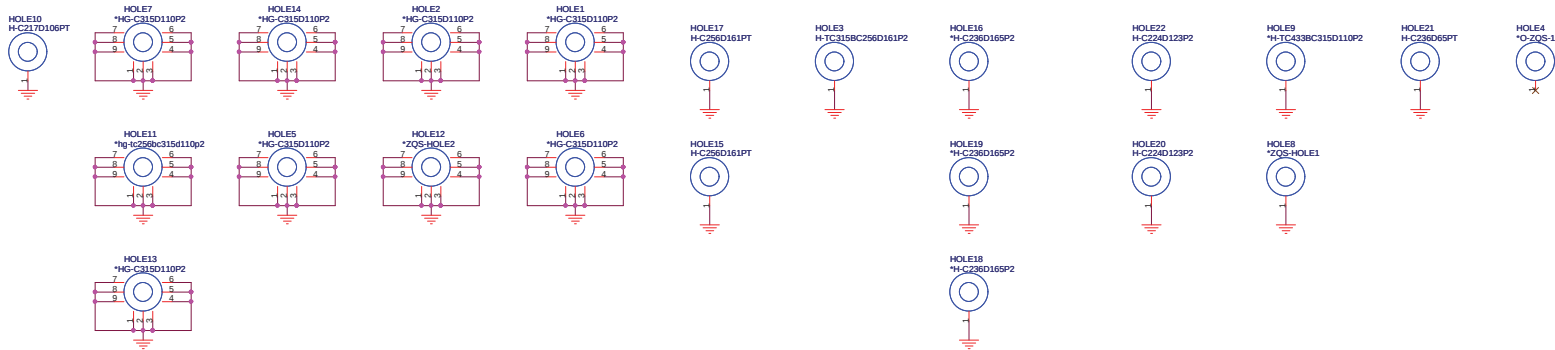




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Size	Document Number	Rev
	+1.05V_M/+3V_M	1A
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Hole



5		4		3		2		1	
Model		date		CHANGE LIST					
ZASA/ZSQTA		9/26		page3 : add R511,R525,R527,R528,R529 for Discrete Only &PCH_JTAG_TDO net change pull-up from +3V_S5 to +1.05 rail					
		9/27		Update power circuit Page19 : add C3777,C3778					
		9/30		Page18 : add Q3508 for U7 GPU_THERMAL_ALERT net Page31 : Del CN1					
		10/3		Page18 : add dGPU_ACDC# net to U7 GPI004 & add R347 Page22 : add R557,R554 to pull-down & R548,R547 stuff for Discrete only Page25 : add R3693,C116 for ODD zero power circuit					
		10/4		Page31 : CN8 add board id3 & board id4 net for touch pad ID control					
		10/5		Page31 : CN8.2,CN8.3 add CLK_SDATA & CLK_SCLK net for touch pad & add R278,R279 Page15 : U41 Power rail change to +3V_GFX Page24 : Del Q16 no't support wake up function Page18 : add Q3509 for dGPU_ACDC# net Page31 : add L35,R3694,R3695 for touch pad 5V & 3V option & add R297,R295 Fan PWR option					
		10/6		Page17 : IFPAB_PLLVDD rail change from +1.8V_GFX to +3V_GFX Page27 : U6 change footprint Page39 : PWR engineer add PQ3006,PQ3005 Page40 : PWR engineer Del PR193,PQ51,PQ54					
		10/7		Page16 :add C3779,C3780 Page29 :add C542,C530 for EMI solution & C544 change to 4.7u 0603 type Page35 :PWR engineer add PC3037,PC3038,PC3039 Page35 :PWR engineer add PC3035,PC3036					
		10/11		Page8 :add R376,R381,R393,R407,R421,R434 for Dual SPI ROM Page9 :U13 power rail change to +3V Page10 :SV_DET_NC net add R250 to pull-down Page27 :add R133,R235 Page30 :C443 change to 3528 type & add C366,R340 Page31 :CN2.27 pin change to +VGACORE Page32 :add R330,R328 pull-up +3VPCU for GPUT_CLK,GPUT_DATA net					
10/14		Page20 :add C3781,C3782,R3569,R3570,R3571,R3576 Page21 :add C3783,C3784,R3577,R3578,R3579,R3581							