ZHG SYSTEM DIAGRAM

AMD Smarter Choice

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

EDP@ -----> eDP panel
LVDS@ -----> LVDS panel
HDT@ -----> HDT fucntion
3G@ -----> 3G function
U2@ -----> USB2.0 only
U3@ -----> USB3.0 function
885S@ -----> EC885S
885L@ -----> EC885L

DDR3- SODIMM1
DDR3-1066 PAGE 6

DDR3 Channel A

AMD Brazos2.0
C60 TDP~9W
FT1
19mmX19mm 413pin BGA
PAGE 3,4,5

TDP1
VGA
LTDP0

HDMI PAGE 13
CRT PAGE 12
LVDS PAGE 12
eDP (Optional) PAGE 12

CPU (PROCHOT)
E.C. (CPUFAN#)

FAN SCH.
PAGE 19

CPU SideBand TemperatureSense I2C

PCI-Expresss

UMI x4

AMD
Hudson-M3L
24.5mmX24.5mm, 656pin BGA
TDP~4.7W
PAGE 7,8,9,10,11

PCLK_DEBUG

Mini Card
WLAN & Debug
PAGE 15

Mini Card
3G
PAGE 15

LAN
Realtek
RTL8105
(10/100)
PAGE 16

25MHz

RJ45
PAGE 16

SIM
PAGE 15

SATA - HDD
PAGE 17

SATA0 150MB
3 Gb/s

USB2.0

Web-Camera
PAGE 12

USB2.0/3.0 Port
MB x1
PAGE 18

FFC

IO D/B

CardReader
AU6435

USB2.0 Port
DB x2

12MHz

INT MIC

AUDIO CONN
Combo Jack

PAGE 18

USB3.0

32.768KHz

25MHz

LPC

Azalia

CLK_PCI_EC

KBC
NPCE885
PAGE 20

CPU SideBand TemperatureSense I2C

Audio CODEC
Realtek
ALC271X-VB6
PAGE 16

Keyboard TouchPad (Image Sensor)
PAGE 19

SPI ROM
PAGE 9

Speaker
PAGE 16

CHARGER (BQ24707A) PAGE 21

AMD CPU CORE (OZ8380) PAGE 23 — *CPU*

1.-05V (TPS51211) PAGE25 — *NB*

DDR 1.5V(TPS51216) PAGE 26

SYSTEM 5V/3V (RT8223P) PAGE 22

1.1V(TPS51211) PAGE 24

Discharge /Thermal protection PAGE 27

Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	Block Diagram	1A

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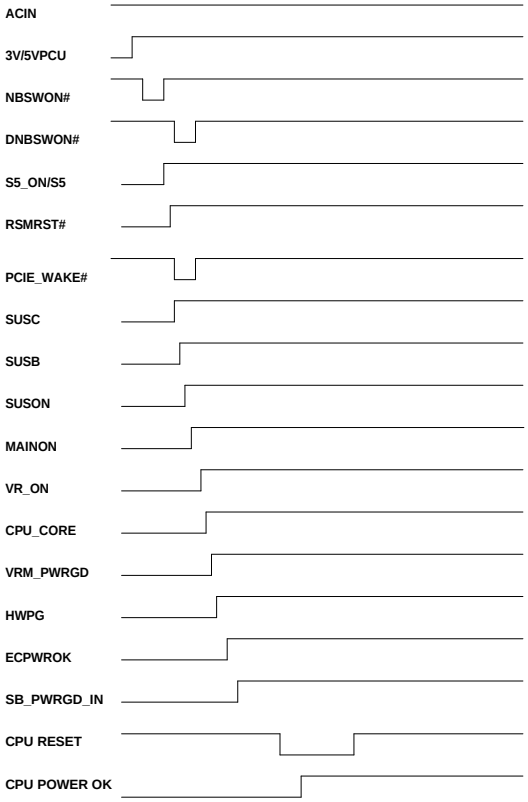
Power Sequence



Hudson M3L SMBUS

A68M SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD26 AE25	DDR / WLAN / 3G / Image Sensor
SCLK1 SDATA1 (+3V_S5)	T7 R7	Not used
SMB_EC_CLK SMB_EC_DAT (+3V_S5)	H19 G19	Charger / Battery
SB_SCLK3 SB_SDATA3 (+3V_S5)	G22 G21	APU

KBC(EC) SMBUS

NPCE885 SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	70 69	Battery / Charger
APU_SIC_EC APU_SID_EC (+3VPCU)	67 68	APU

Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	System Information	1A
Date: Tuesday, January 10, 2012	Sheet 2 of 28	

(CPU)

03

This page is different AMD Nile

U13E

ONTARIO (2.0) PART 1 OF 5

MEMORY I/F

(6) M_A_A[15:0]
M_A_A0 R17 M_ADD0
M_A_A1 H19 M_ADD1
M_A_A2 J17 M_ADD2
M_A_A3 H18 M_ADD3
M_A_A4 H17 M_ADD4
M_A_A5 G17 M_ADD5
M_A_A6 H15 M_ADD6
M_A_A7 G18 M_ADD7
M_A_A8 F19 M_ADD8
M_A_A9 E19 M_ADD9
M_A_A10 T19 M_ADD10
M_A_A11 F17 M_ADD11
M_A_A12 E18 M_ADD12
M_A_A13 W17 M_ADD13
M_A_A14 E16 M_ADD14
M_A_A15 G15 M_ADD15

(6) M_A_BS[2..0]
M_A_BS0 R18 M_BANK0
M_A_BS1 T18 M_BANK1
M_A_BS2 F16 M_BANK2

(6) M_A_DM[7..0]
M_A_DM0 D15 M_DM0
M_A_DM1 B19 M_DM1
M_A_DM2 D21 M_DM2
M_A_DM3 H22 M_DM3
M_A_DM4 P23 M_DM4
M_A_DM5 V23 M_DM5
M_A_DM6 AB20 M_DM6
M_A_DM7 AA16 M_DM7

(6) M_A_DQSP0 A16 M_DQS_H0
(6) M_A_DQSN0 B16 M_DQS_L0
(6) M_A_DQSP1 B20 M_DQS_H1
(6) M_A_DQSN1 A20 M_DQS_L1
(6) M_A_DQSP2 E23 M_DQS_H2
(6) M_A_DQSN2 F22 M_DQS_L2
(6) M_A_DQSP3 J22 M_DQS_H3
(6) M_A_DQSN3 J23 M_DQS_L3
(6) M_A_DQSP4 R22 M_DQS_H4
(6) M_A_DQSN4 P22 M_DQS_L4
(6) M_A_DQSP5 W22 M_DQS_H5
(6) M_A_DQSN5 V22 M_DQS_L5
(6) M_A_DQSP6 AC20 M_DQS_H6
(6) M_A_DQSN6 AC21 M_DQS_L6
(6) M_A_DQSP7 AB16 M_DQS_H7
(6) M_A_DQSN7 AC16 M_DQS_L7

(6) M_A_CLKP0 M17 M_CLK_H0
(6) M_A_CLKN0 M16 M_CLK_L0
(6) M_A_CLKP1 M19 M_CLK_H1
(6) M_A_CLKN1 M18 M_CLK_L1
N18 M_CLK_H2
N19 M_CLK_L2
L18 M_CLK_H3
L17 M_CLK_L3

(6) M_A_RST# L23 M_RESET_L
(6) M_A_EVENT# M_A_EVENT# N17 M_EVENT_L

(6) M_A_CKE0 M_A_CKE0 F15 M_CKE0
(6) M_A_CKE1 M_A_CKE1 E15 M_CKE1

(6) M_A_ODT0 W19 M0_ODT0
(6) M_A_ODT1 V15 M0_ODT1
U19 M1_ODT0
W15 M1_ODT1

(6) M_A_CS#0 T17 M0_CS_L0
(6) M_A_CS#1 W16 M0_CS_L1
U17 M1_CS_L0
V16 M1_CS_L1

(6) M_A_RAS# U18 M_RAS_L
(6) M_A_CAS# V19 M_CAS_L
(6) M_A_WE# V17 M_WE_L

M_A_DQ[0..63] (6)

M_DATA0 B14 M_A_DQ0
M_DATA1 A15 M_A_DQ1
M_DATA2 A17 M_A_DQ2
M_DATA3 D18 M_A_DQ3
M_DATA4 A14 M_A_DQ4
M_DATA5 C14 M_A_DQ5
M_DATA6 C16 M_A_DQ6
M_DATA7 D16 M_A_DQ7
M_DATA8 C18 M_A_DQ8
M_DATA9 A19 M_A_DQ9
M_DATA10 B21 M_A_DQ10
M_DATA11 D20 M_A_DQ11
M_DATA12 A18 M_A_DQ12
M_DATA13 B18 M_A_DQ13
M_DATA14 A21 M_A_DQ14
M_DATA15 C20 M_A_DQ15
M_DATA16 C23 M_A_DQ16
M_DATA17 D23 M_A_DQ17
M_DATA18 F23 M_A_DQ18
M_DATA19 F22 M_A_DQ19
M_DATA20 C22 M_A_DQ20
M_DATA21 D22 M_A_DQ21
M_DATA22 F20 M_A_DQ22
M_DATA23 F21 M_A_DQ23
M_DATA24 H21 M_A_DQ24
M_DATA25 H23 M_A_DQ25
M_DATA26 K22 M_A_DQ26
M_DATA27 K21 M_A_DQ27
M_DATA28 G23 M_A_DQ28
M_DATA29 H20 M_A_DQ29
M_DATA30 K20 M_A_DQ30
M_DATA31 K23 M_A_DQ31
M_DATA32 N23 M_A_DQ32
M_DATA33 P21 M_A_DQ33
M_DATA34 T20 M_A_DQ34
M_DATA35 T23 M_A_DQ35
M_DATA36 M20 M_A_DQ36
M_DATA37 P20 M_A_DQ37
M_DATA38 R23 M_A_DQ38
M_DATA39 T22 M_A_DQ39
M_DATA40 V20 M_A_DQ40
M_DATA41 V21 M_A_DQ41
M_DATA42 Y23 M_A_DQ42
M_DATA43 Y22 M_A_DQ43
M_DATA44 T21 M_A_DQ44
M_DATA45 U23 M_A_DQ45
M_DATA46 W23 M_A_DQ46
M_DATA47 Y21 M_A_DQ47
M_DATA48 Y20 M_A_DQ48
M_DATA49 AB22 M_A_DQ49
M_DATA50 AC19 M_A_DQ50
M_DATA51 AA18 M_A_DQ51
M_DATA52 AA23 M_A_DQ52
M_DATA53 AA20 M_A_DQ53
M_DATA54 AB19 M_A_DQ54
M_DATA55 Y18 M_A_DQ55
M_DATA56 AC17 M_A_DQ56
M_DATA57 Y16 M_A_DQ57
M_DATA58 AB14 M_A_DQ58
M_DATA59 AC14 M_A_DQ59
M_DATA60 AC18 M_A_DQ60
M_DATA61 AB18 M_A_DQ61
M_DATA62 AB15 M_A_DQ62
M_DATA63 AC15 M_A_DQ63

M_VREF M23 +M_VREF
M_ZVDDIO_MEM_S M22 39.2/F_4 R51 +1.5VSUS

FT1_ONTARIO

U13A

ONTARIO (2.0) PART 2 OF 5

PCIE I/F

(14) PCIE_RXP0_LAN AA6 P_GPP_RXP0
(14) PCIE_RXN0_LAN Y6 P_GPP_RXN0
(15) PCIE_RXP1 AB4 P_GPP_RXP1
(15) PCIE_RXN1 AC4 P_GPP_RXN1
(15) PCIE_RXP2 AA1 P_GPP_RXP2
(15) PCIE_RXN2 AA2 P_GPP_RXN2
Y4 P_GPP_RXP3
Y3 P_GPP_RXN3

VDD_10
R251 2K/F_4 ON_ZVDD Y14 P_ZVDD_10

P_GPP_TXP0 AB6 PCIE_TXP0_LAN_C C349 0.1u/10V_4 PCIE_TXP0_LAN (14) LAN
P_GPP_TXN0 AC6 PCIE_TXN0_LAN_C C348 0.1u/10V_4 PCIE_TXN0_LAN (14) LAN
P_GPP_TXP1 AB3 PCIE_TXP1_C C352 0.1u/10V_4 PCIE_TXP1 (15) WLAN
P_GPP_TXN1 AC3 PCIE_TXN1_C C351 0.1u/10V_4 PCIE_TXN1 (15) WLAN
P_GPP_TXP2 Y1 PCIE_TXP2_C C160 0.1u/10V_4 PCIE_TXP2 (15) 3G
P_GPP_TXN2 Y2 PCIE_TXN2_C C159 0.1u/10V_4 PCIE_TXN2 (15) 3G
V3
V4
P_ZVSS AA14 ON_ZVSS R250 1.27K/F_4

UMI I/F

(8) UMI_RXP0 AA12 P_UMI_RXP0
(8) UMI_RXN0 Y12 P_UMI_RXN0
(8) UMI_RXP1 AA10 P_UMI_RXP1
(8) UMI_RXN1 Y10 P_UMI_RXN1
(8) UMI_RXP2 AB10 P_UMI_RXP2
(8) UMI_RXN2 AC10 P_UMI_RXN2
(8) UMI_RXP3 AC7 P_UMI_RXP3
(8) UMI_RXN3 AB7 P_UMI_RXN3

P_UMI_TXP0 AB12 UMI_TXP0_C C337 0.1u/10V_4 UMI_TXP0 (8)
P_UMI_TXN0 AC12 UMI_TXN0_C C336 0.1u/10V_4 UMI_TXN0 (8)
P_UMI_TXP1 AC11 UMI_TXP1_C C339 0.1u/10V_4 UMI_TXP1 (8)
P_UMI_TXN1 AB11 UMI_TXN1_C C338 0.1u/10V_4 UMI_TXN1 (8)
P_UMI_TXP2 AA8 UMI_TXP2_C C345 0.1u/10V_4 UMI_TXP2 (8)
P_UMI_TXN2 Y8 UMI_TXN2_C C342 0.1u/10V_4 UMI_TXN2 (8)
P_UMI_TXP3 AB8 UMI_TXP3_C C347 0.1u/10V_4 UMI_TXP3 (8)
P_UMI_TXN3 AC8 UMI_TXN3_C C346 0.1u/10V_4 UMI_TXN3 (8)

FT1_ONTARIO

+M_VREF +1.5VSUS
R49 1K/F_4
R53 1K/F_4
C77 0.1u/10V_4
C74 1000p/50V_4

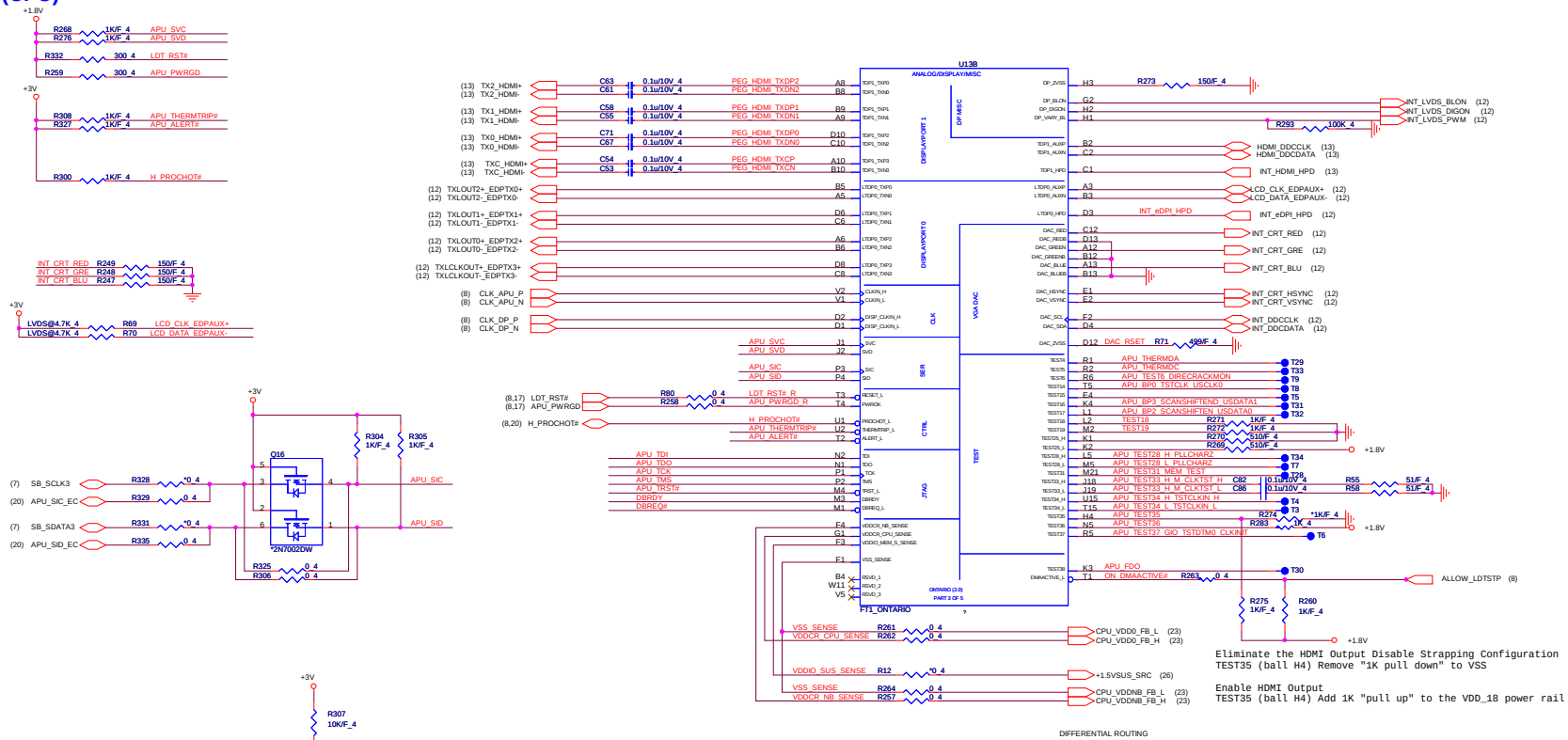
+1.5VSUS R45 *2.2K_4
+1.5VSUS R54 1K/F_4
M_A_EVENT#
Q3 *MMBT3904
R48 *0_4
APU_MEMHOT# (7)

P/N Item Description
AJ00C60VT00CPU(413P)CMC60AFPB22GV 1.0G(BGA)
AJ00C60VT01CPU(413P)CMC60AFPB22GV 1.0G(BGA)STN BSQ

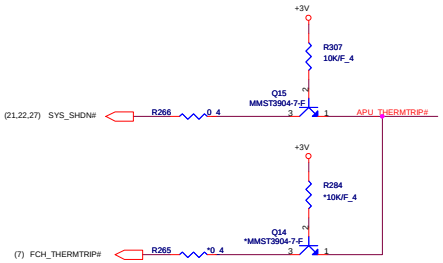
Quanta Computer Inc.
PROJECT : ZHG

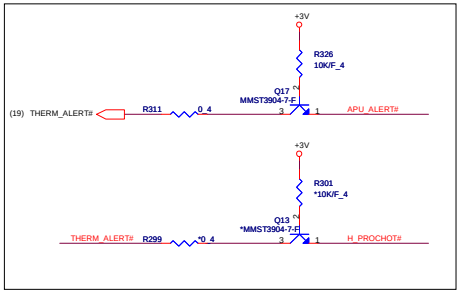
Size	Document Number	Rev
	ONTARIO MEM & PCIE I/F(1/3)	1A
Date: Tuesday, January 10, 2012	Sheet 3 of 28	

(CPU)

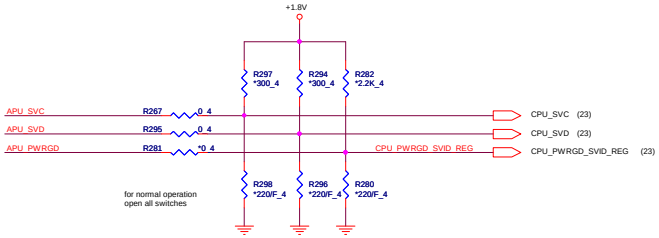


	3	2	1	0	DP AUX+	DP AUX-
HDMI	Clock	CH0	CH1	CH2	DDC Clock	DDC Data
LVDS Panel	Clock	CH0	CH1	CH2	DDC Clock	DDC Data
eDP Panel	ML3	ML2	ML1	ML0	AUX+	AUX-

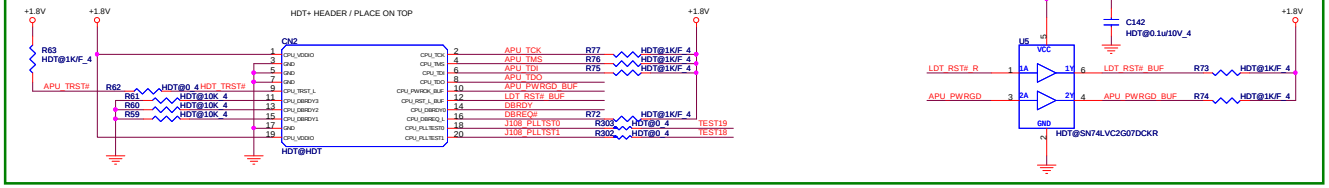




VID Override Circuit



HDT+ Connector(CPU)



Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	ONTATIO DISPLAY/CLK/MI(2/3)	1A

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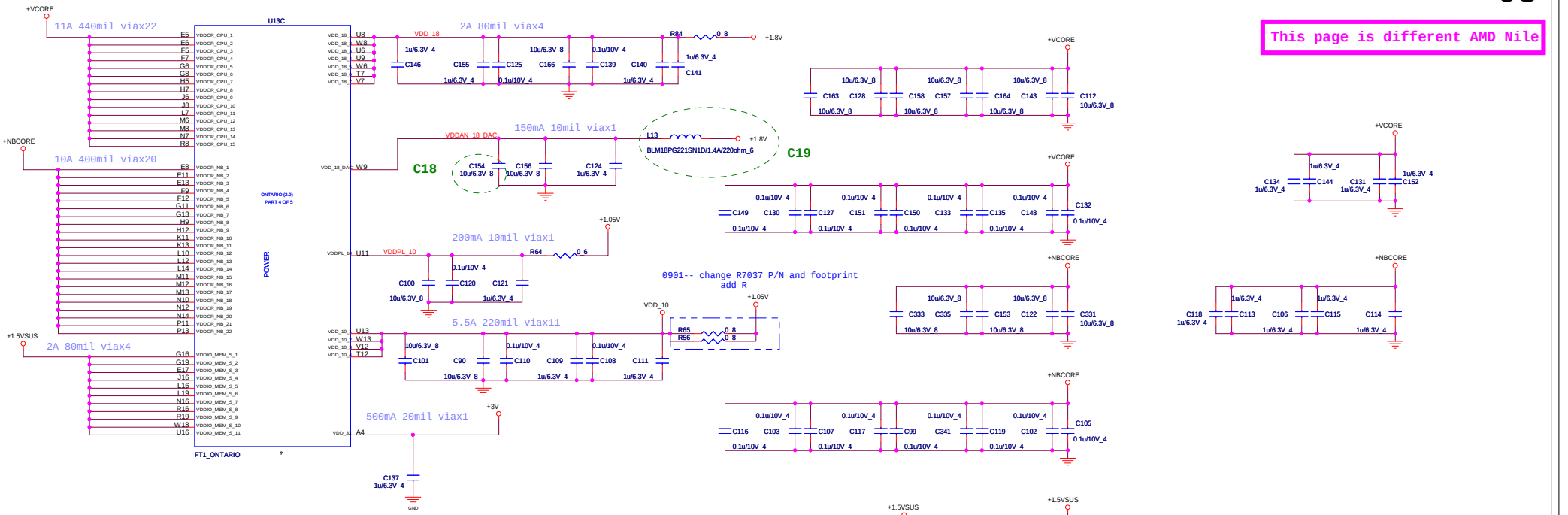
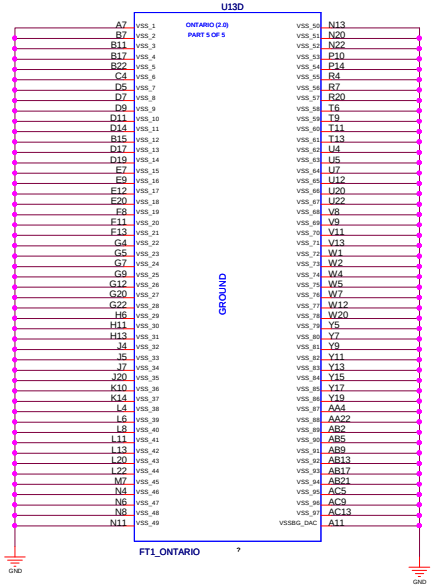
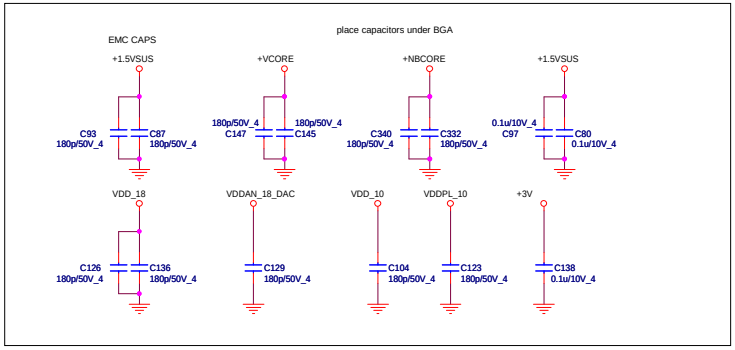
(CPU)

This page is different AMD Nile



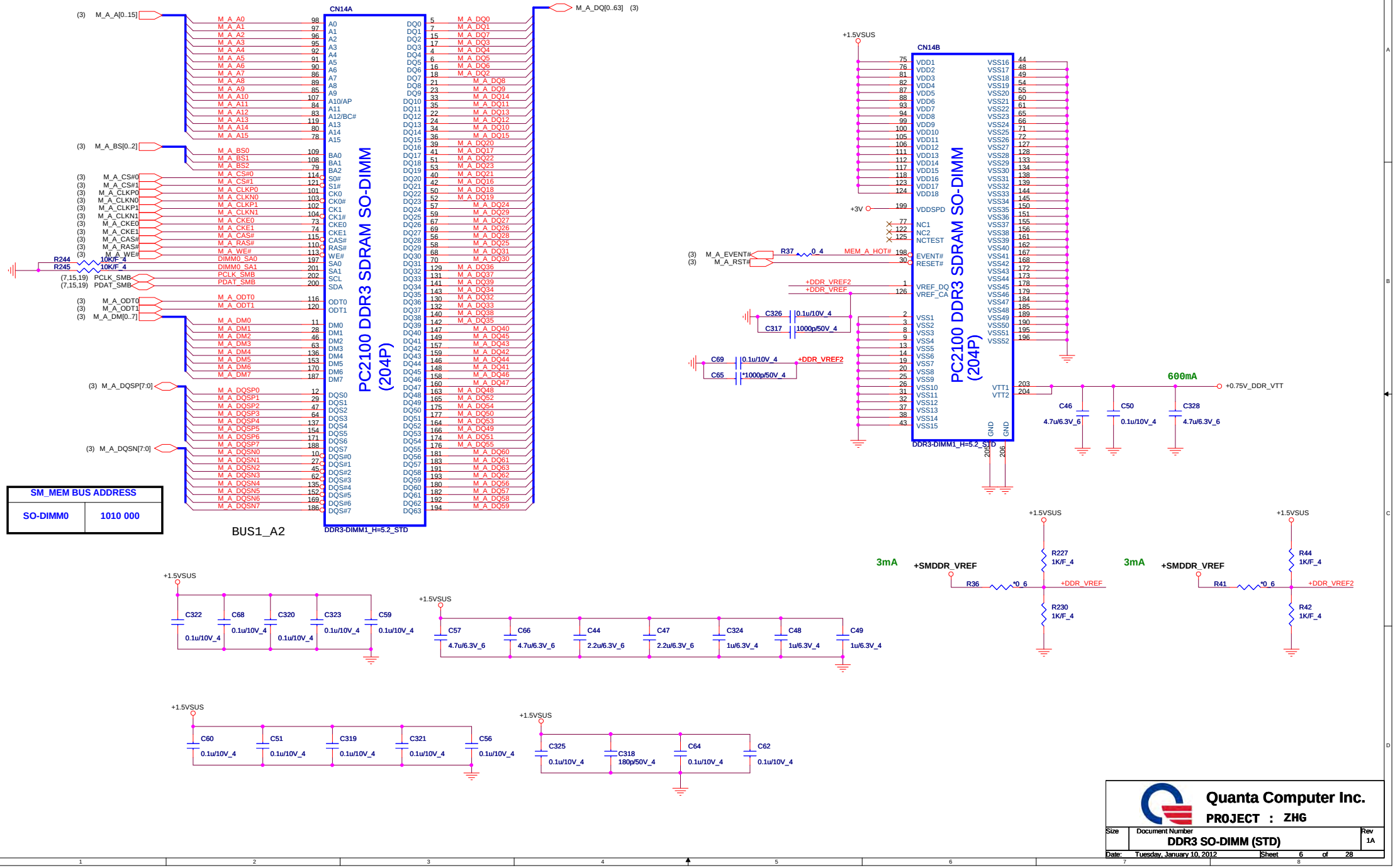




Quanta Computer Inc.

PROJECT : ZHG

Size	Document Number	Rev
	ONTARIO POWER & DECOUP(3/3)	1A
Date: Tuesday, January 10, 2012	Sheet 5 of 28	


CN14A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=5.2_STD
CN14B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=5.2_STD
M_A_A[0..15]
M_A_BS[0..2]
M_A_DQ[0..63]
M_A_DQSP[7:0]
M_A_DQSN[7:0]
M_A_DM[0..7]
SM_MEM BUS ADDRESS
SO-DIMM0
1010 000
BUS1_A2
+1.5VSUS
+3V
+DDR_VREF
+DDR_VREF2
+SMDDR_VREF
+0.75V_DDR_VTT
600mA
3mA
3mA

NC,no install by default

Internal have PD

For Dimm, WLAN, TP

Integrated 8.2-kΩ PU

GEVENT12# ~18# are +3V_S5

HDaudio interface are +3V_S5

Note:LLB#, WAKE# and PWR_BTN need pull up to +3VPCU only if S5+ mode is supported

Provided test points from checklist

GPIO193 ~196 are +3V_S5

USB3.0

HUB3

HUB2

HUB1

MB co-lay USB3.0 port

SIM

WLAN+BT

CCD

Card Reader

D/B

3G

DB debug port

Note: USB P/N pairs with trace lengths up to 10"

To Azalia

EC	FCH	Device	I2C_Device(S)		
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery		ALL/S5
I2Ce_2(M)		APU			ALL
I2Ce_3(M)					
	I2Cf_3(M)	APU			S5
	I2Cf_1(M)				S5
	I2Cf_0(M)	DDR	WLAN/3G	Image Sensor	S0

EC will Conflict with FCH. Do not mount

Quanta Computer Inc.

PROJECT : ZHG

Size	Document Number	Rev
	FCH 1/5(GPIO/USB/AZ)	1A

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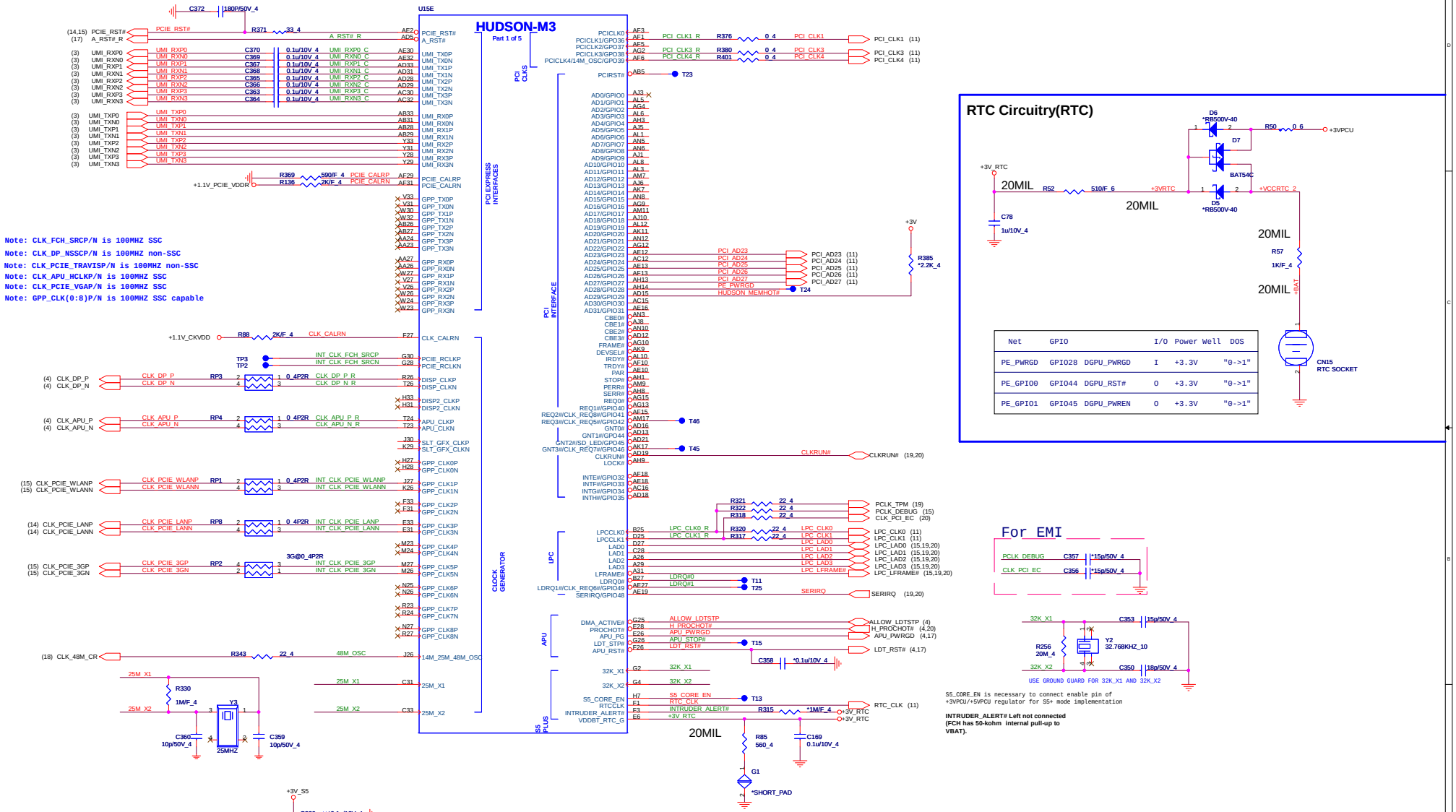
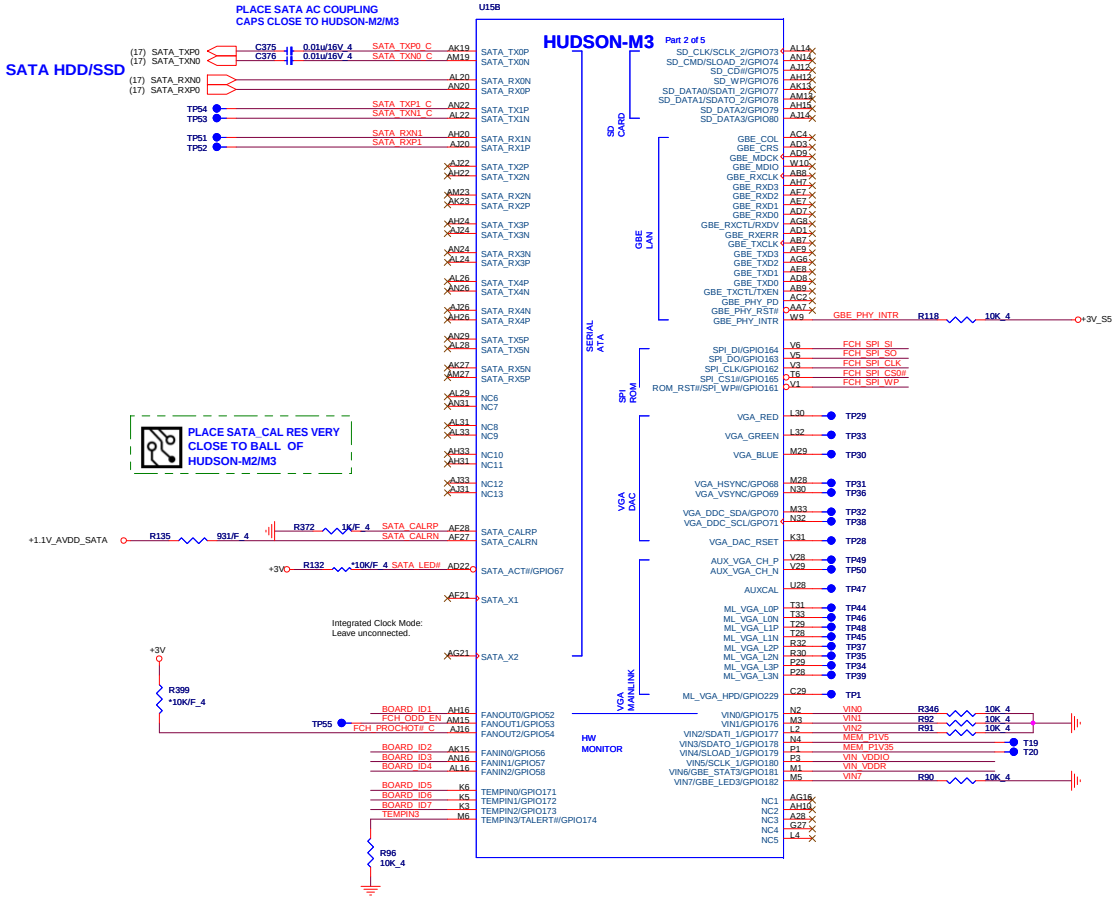
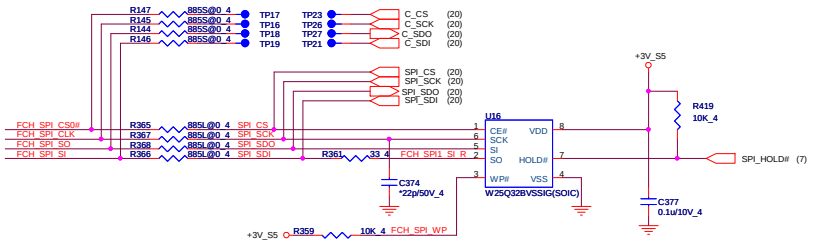
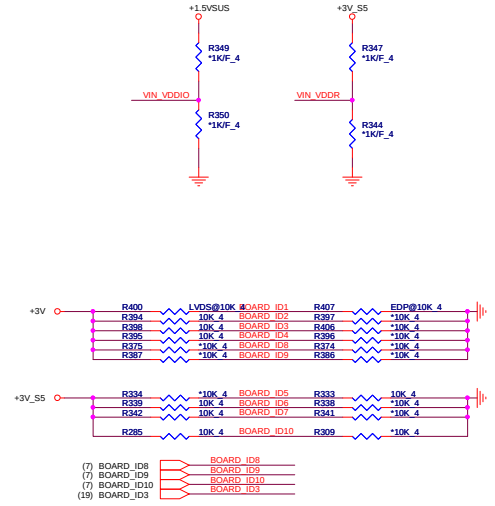


Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	FCH 2/5(ACPI/PCI/CLK)	1A
Date: Tuesday, January 10, 2012	Sheet 8 of 28	







BOARD ID SETTING

BOARD_ID1	LCD
0	eDP
1	LVDS

BOARD_ID3	For TP
0	ELAN
1	Synaptics

Quanta Computer Inc.

PROJECT : ZHG

Size	Document Number	Rev
	FCH 3/5(SATA/VGA/GND/SPI)	1A

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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

VDDQ--3.3V I/O power

VDD-- S/B CORE power

HUDSON-M3 Part 3 of 5

HUDSON-M3 Part 5 of 5

CKVDD_1.1V-- Internal clock Generator I/O power

PCIE_VDDR--PCIE I/O power

AVDD_SATA--SATA phy power

S5_3.3--3.3v standby power

S5 plus mode

S5_1.1V--1.1V standby power

POWER

GROUND

Quanta Computer Inc.

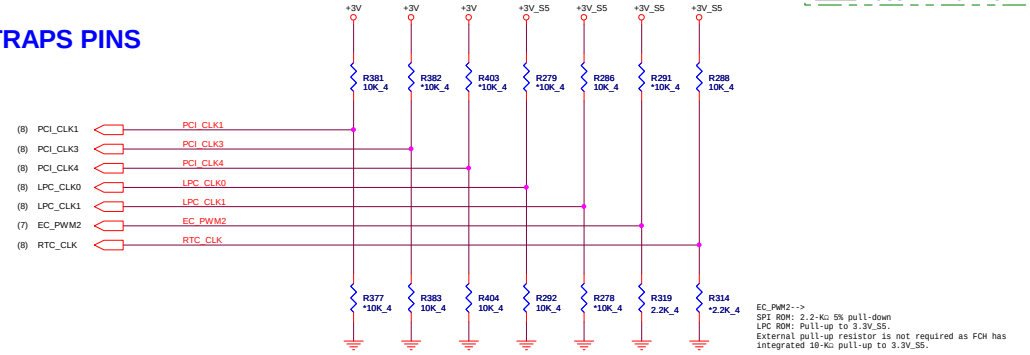
PROJECT :ZHG

Size | Document Number: FCH 4/5(POWER) | Rev: 1A

Date: Tuesday, January 10, 2012 | Sheet 10 of 28

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

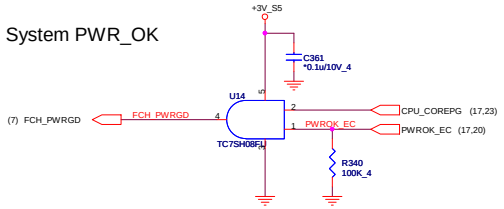


Remove PCI_CLK2 function

REQUIRED STRAPS

	--------	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

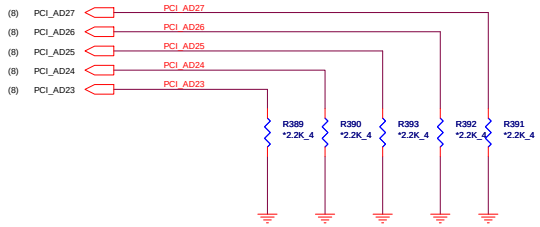
System PWR_OK



FCH PWRGD CKT

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Quanta Computer Inc.
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Size	Document Number	Rev
	FCH 5/5(STRAP & PWRGD)	1A

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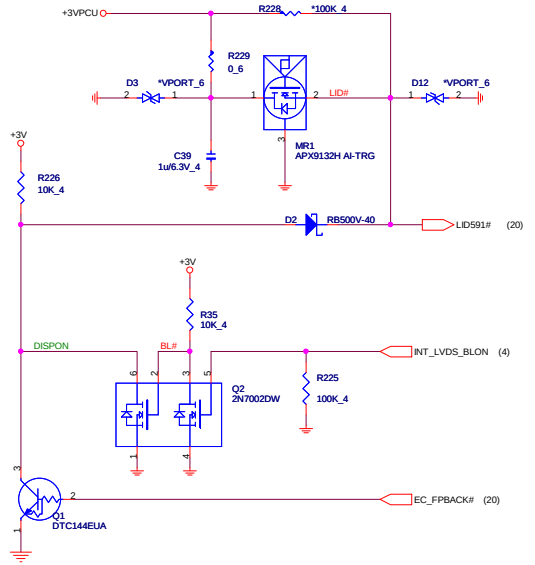
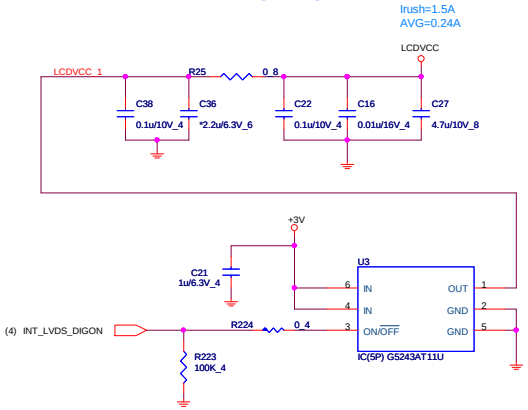
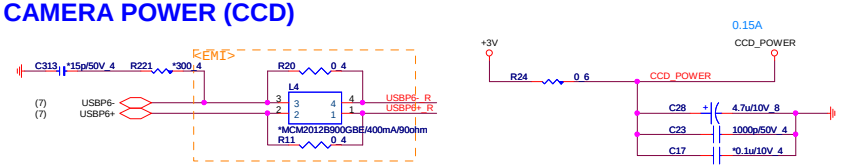
HALL IC (HSR)



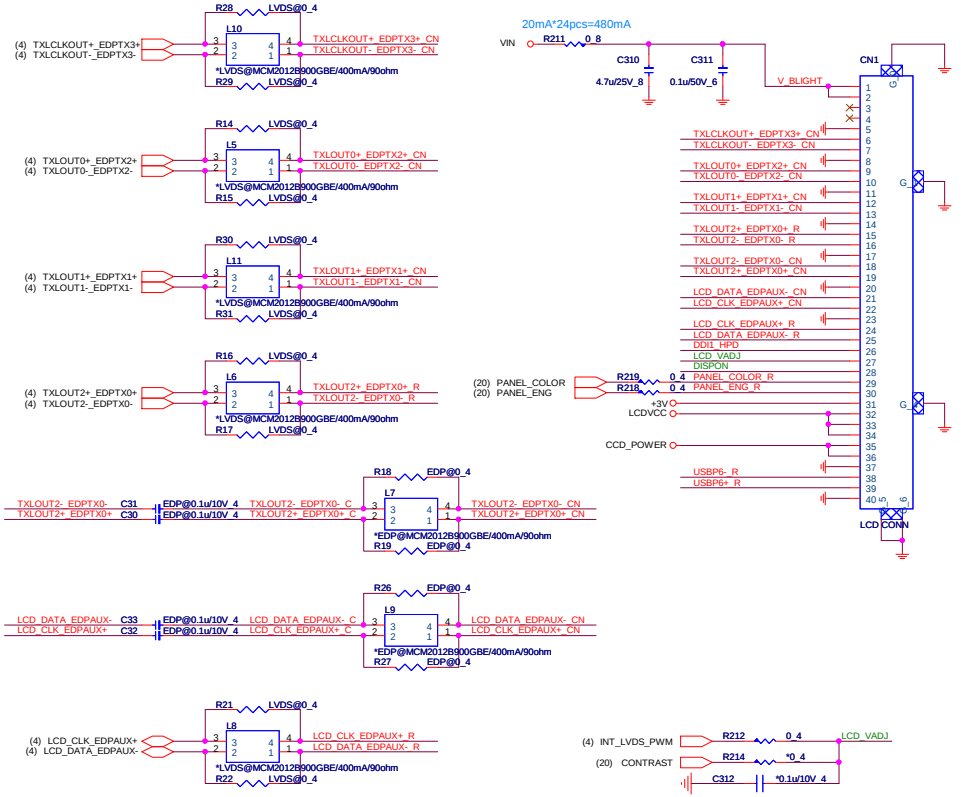
LCD POWER SWITCH (LDS)



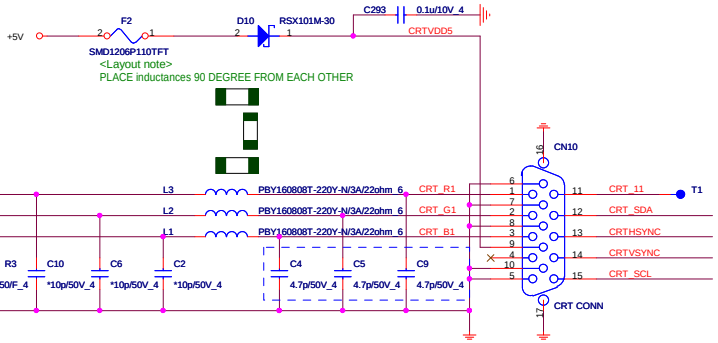
CAMERA POWER (CCD)

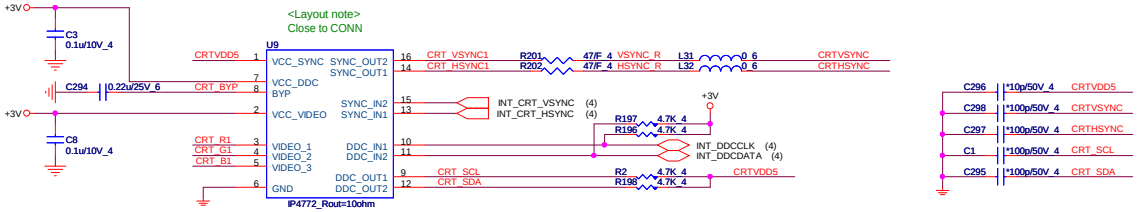


LCD MODULE (LDS)



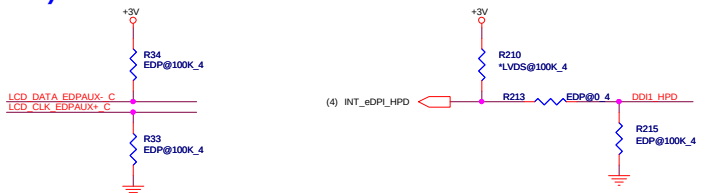
CRT(CRT)





2nd source: AL002009W01 (CMD CM2009-02QR Rout=15ohm)

eDP (LDS)



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Size	Document Number	Rev
	CRT/LVDS/EDP	1A
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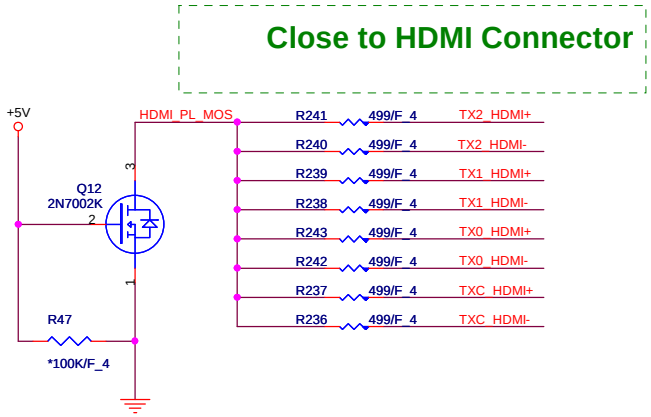
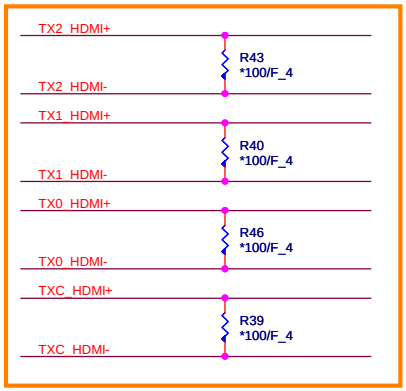
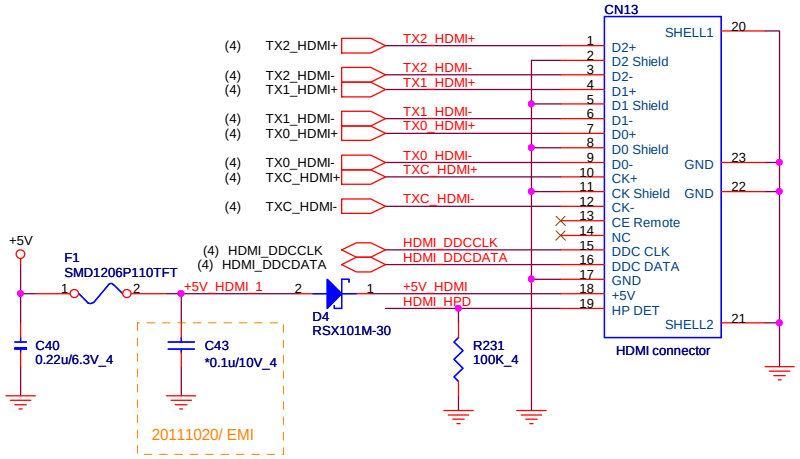
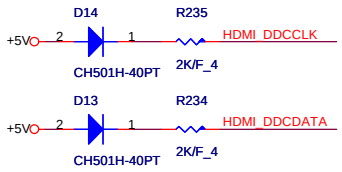
HDMI (HDM)

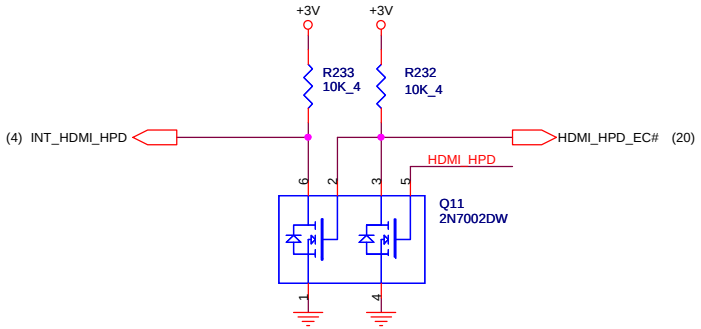






SDVO I2C Control (HDM)





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Size	Document Number	Rev
	HDMI	1A
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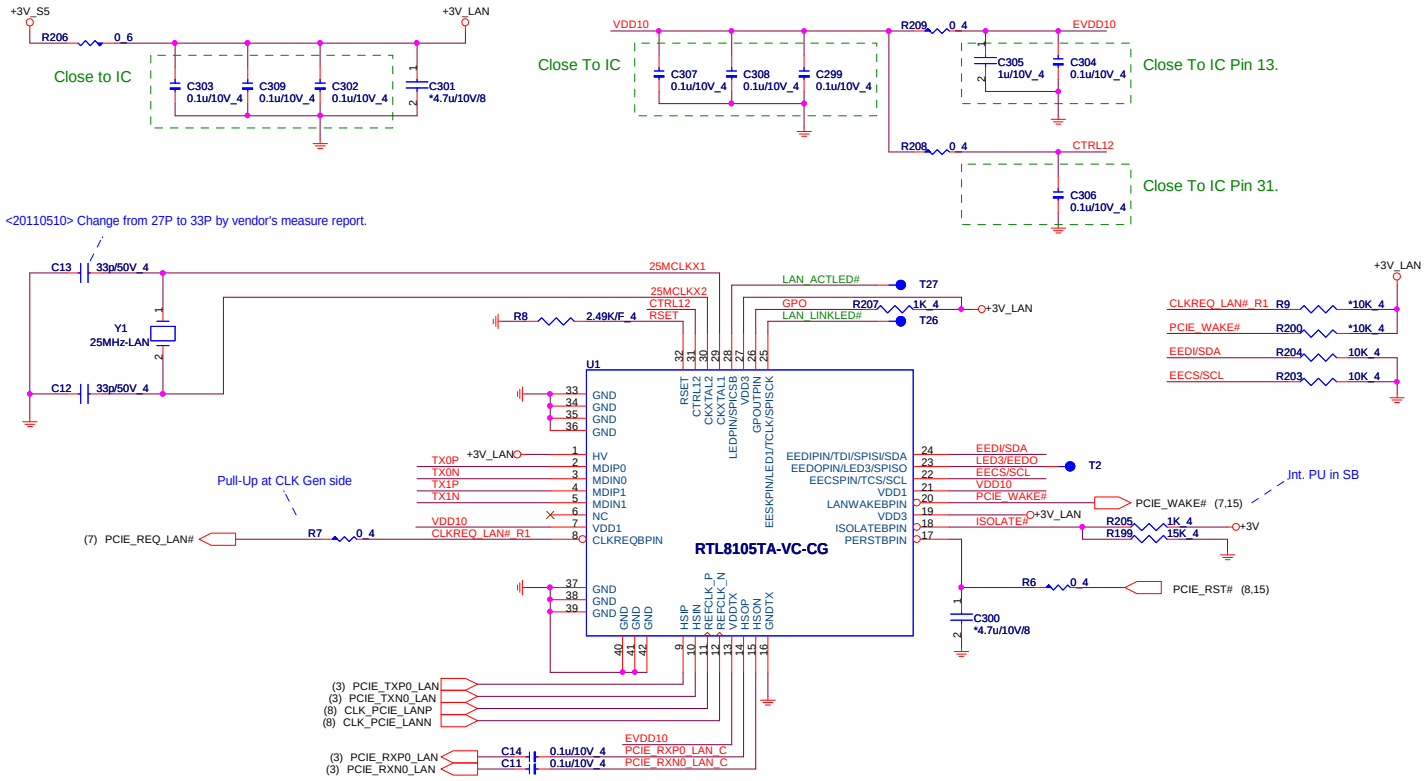
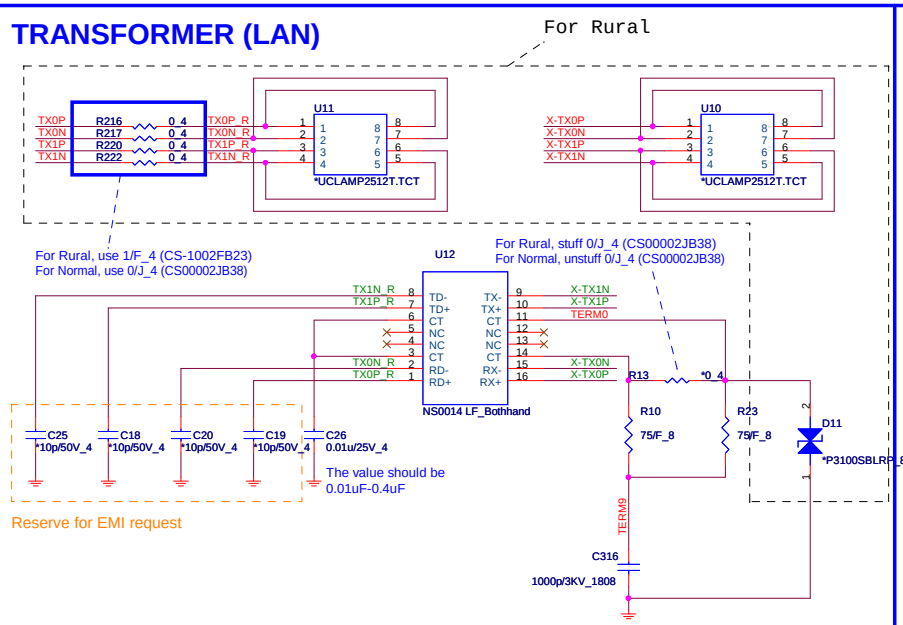
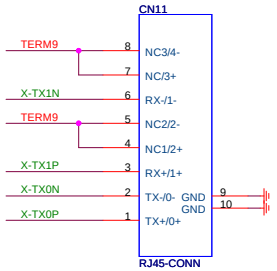
LAN (LAN)



TRANSFORMER (LAN)



RJ45 Connector (LAN)



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Size	Document Number	Rev
	LAN RTL8105TA-VC-CG	1A

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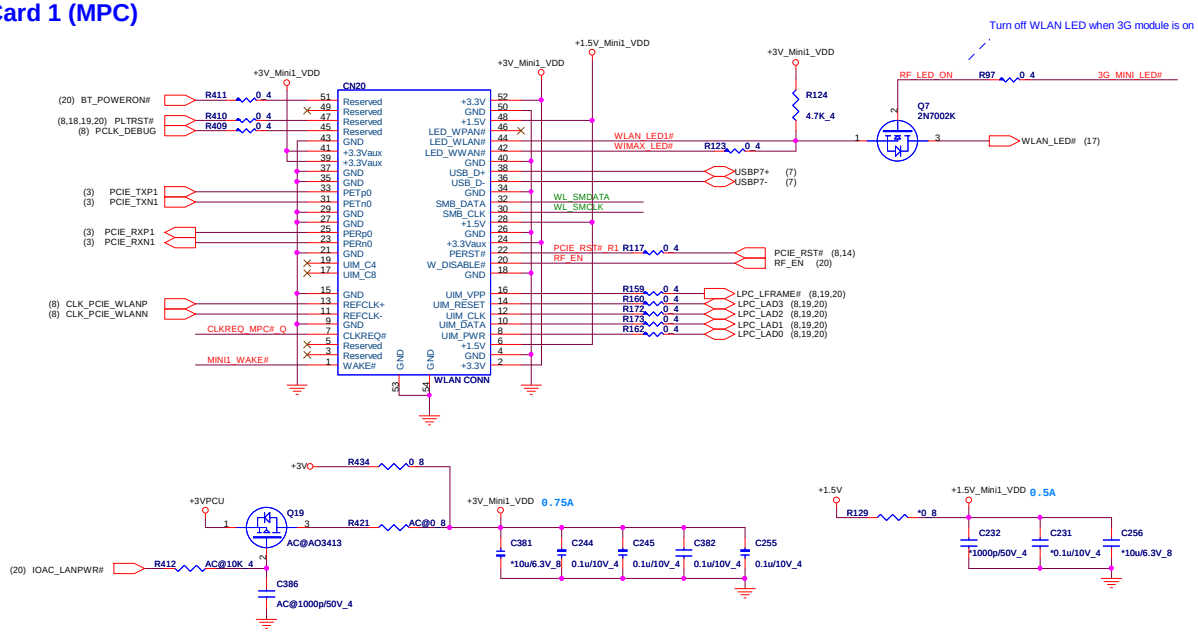
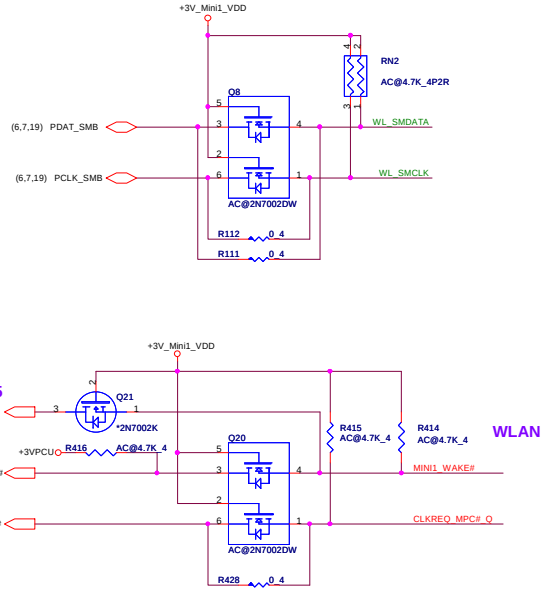
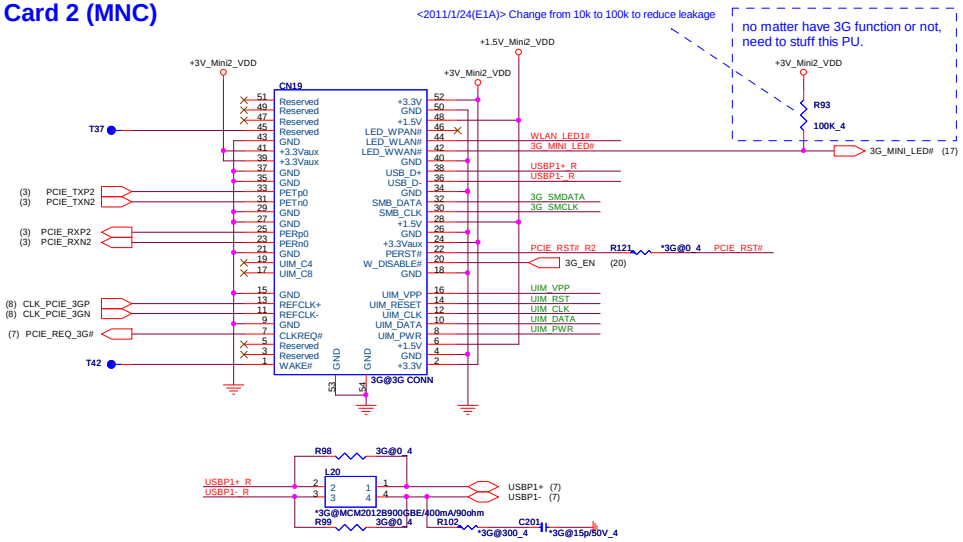
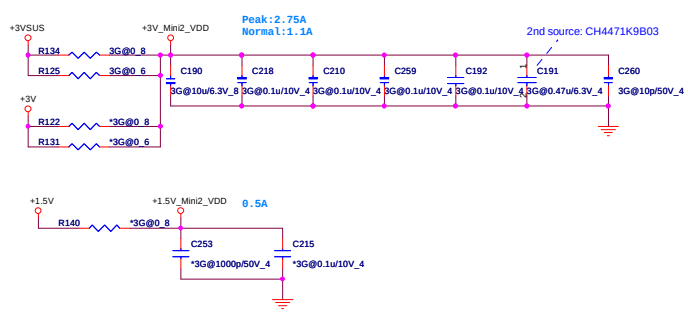
Mini Card 1 (MPC)

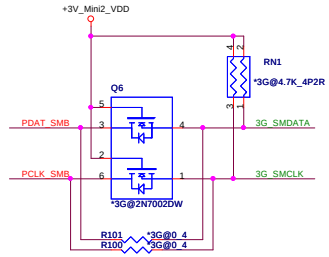




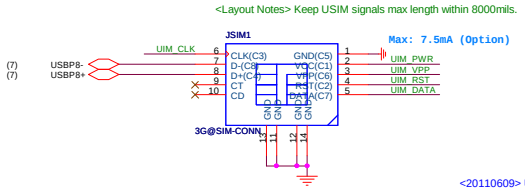
Mini Card 2 (MNC)

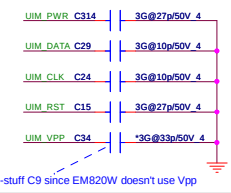


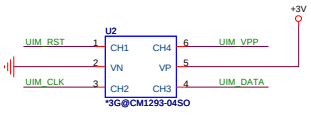


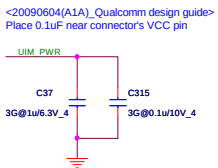


MultiMedia SIM (MNC)









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	Mini-Card/WL/3G/SIM	1A
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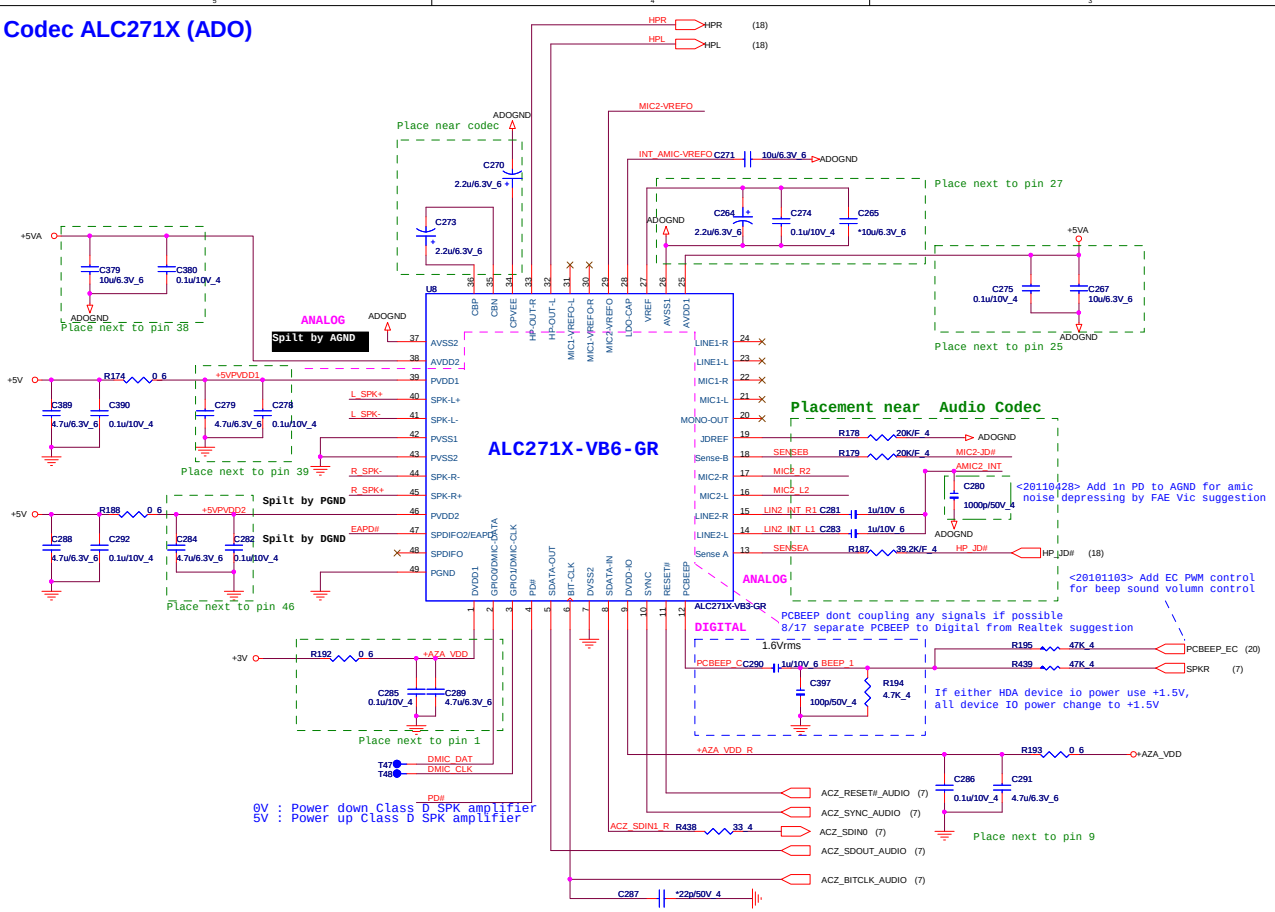
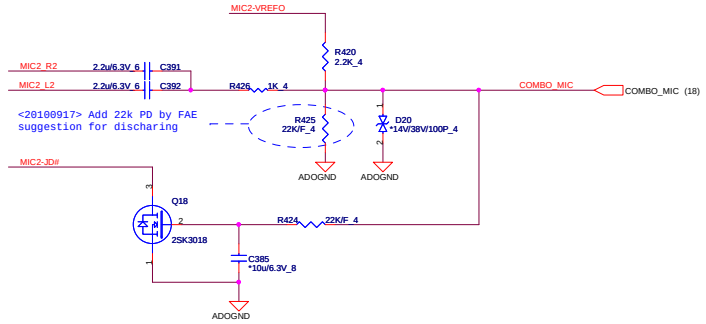
Codec ALC271X (ADO)

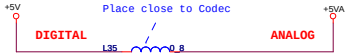


EARPHONE (AMP)

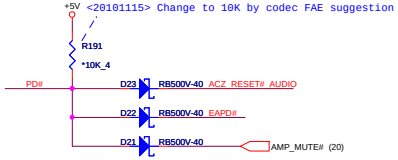


Power (ADO)

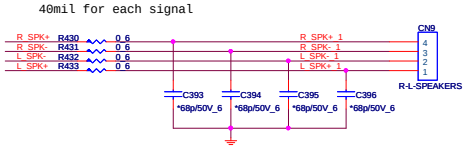
Demodulation Filter



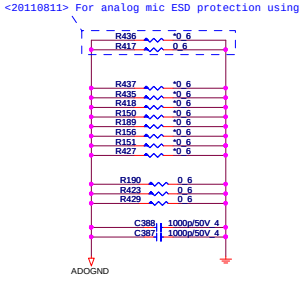
Mute (ADO)



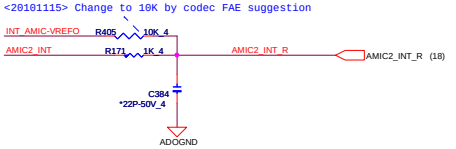
Internal Speaker (AMP)



GND(ADO)



Internal Analog MIC (AMP)



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	ALC271X / AMP / SPK	1A
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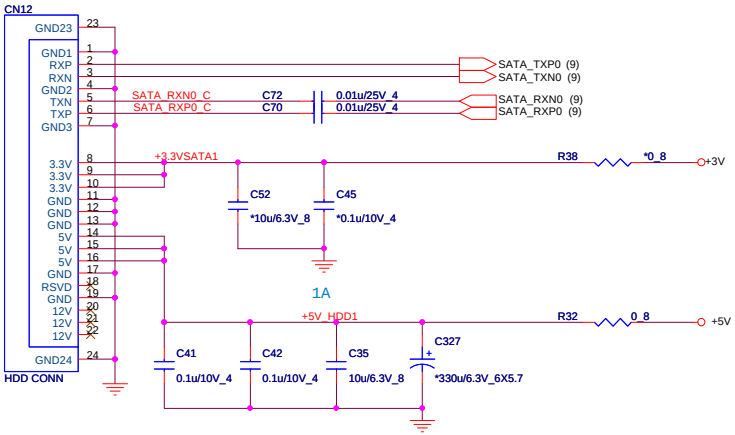
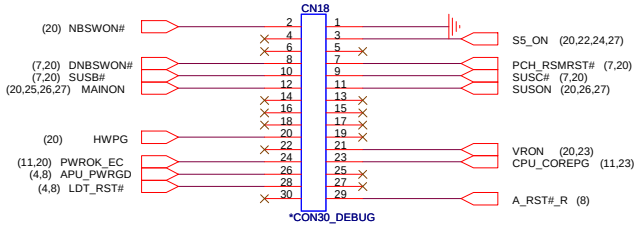
2.5" SATA HDD (HDD)

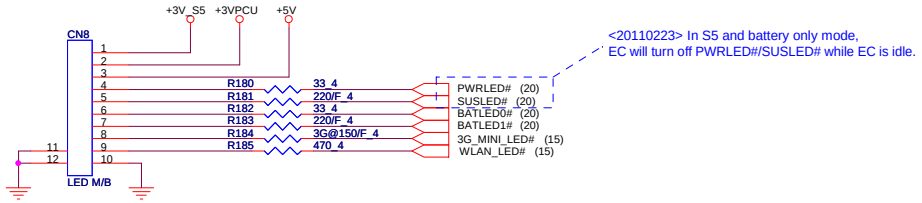


Power Sequence Connector(CPU)

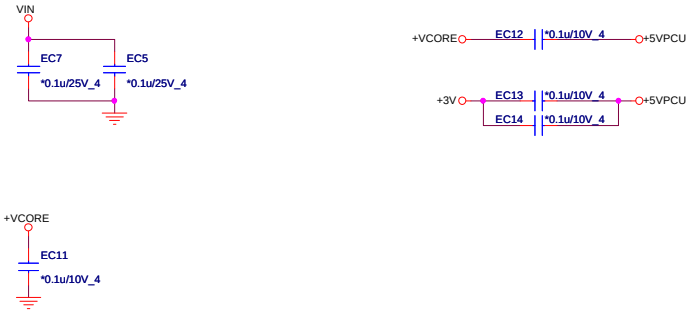


1	GND	11	SUSON	21	VRON
2	NBSWON#	12	MAINON	22	RESERVE
3	S5_ON	13	RESERVE	23	CPU_COREPG
4	RESERVE	14	RESERVE	24	PWROK_EC
5	RESERVE	15	RESERVE	25	RESERVE
6	RESERVE	16	RESERVE	26	APU_PWRGD
7	PCH_RSMRST#	17	RESERVE	27	RESERVE
8	DNBSWON#	18	RESERVE	28	LDT_RST#
9	SUSC#	19	RESERVE	29	A_RST#_R
10	SUSB#	20	HWPG	30	RESERVE

LED DB (UIF)

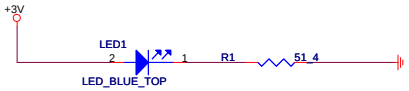


Stitching Cap(EMC)



POWER LED(UIF)

PWR indicator



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	SATA HDD/LED/SW	1A

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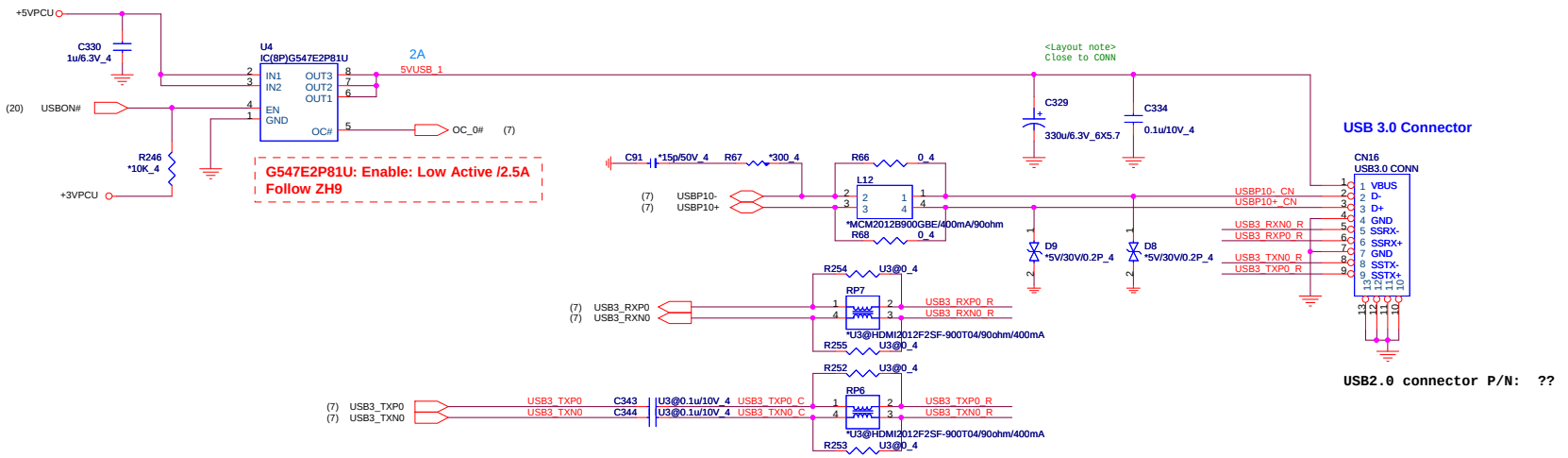
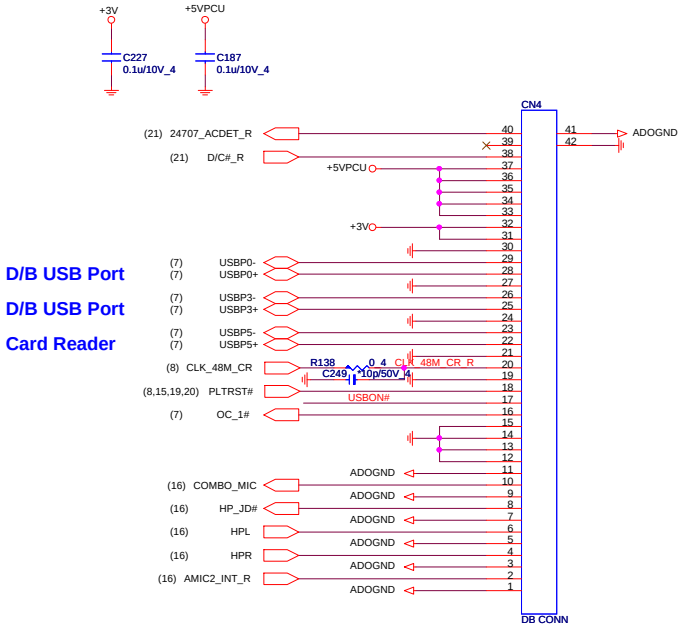
USB Left (USB)



USB2.0 connector P/N: ??

IO D/B (UIF)

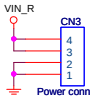


D/B USB Port

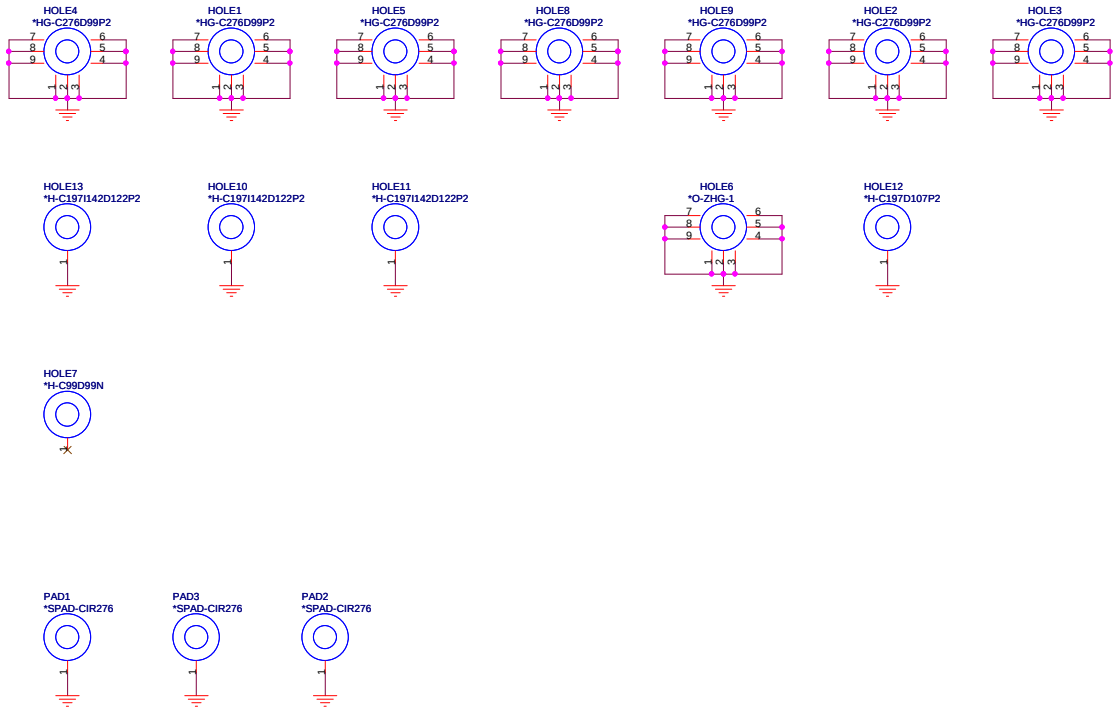
D/B USB Port

Card Reader

POWER M/B (DCD)



HOLE(OTH)



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	USB Port/ DB	1A
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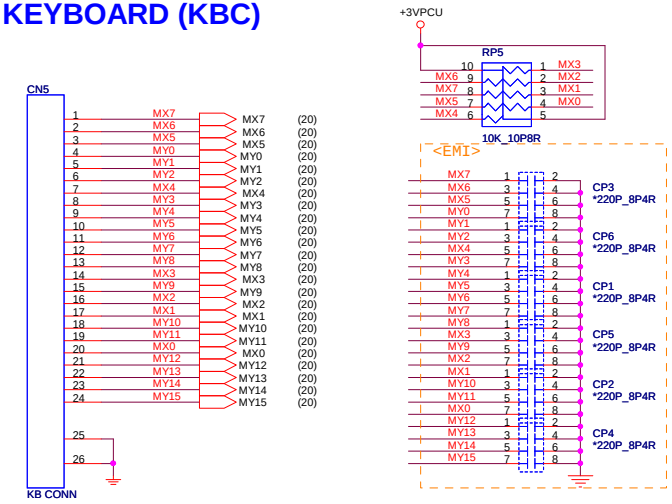
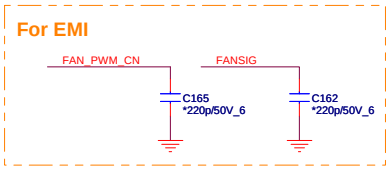
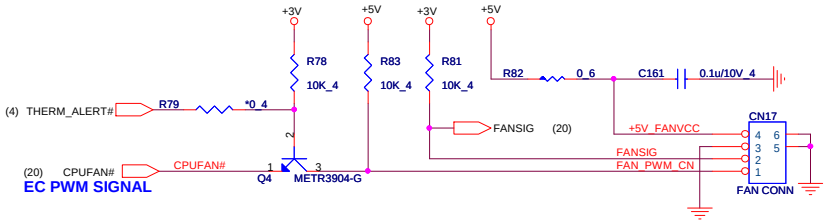
KEYBOARD (KBC)

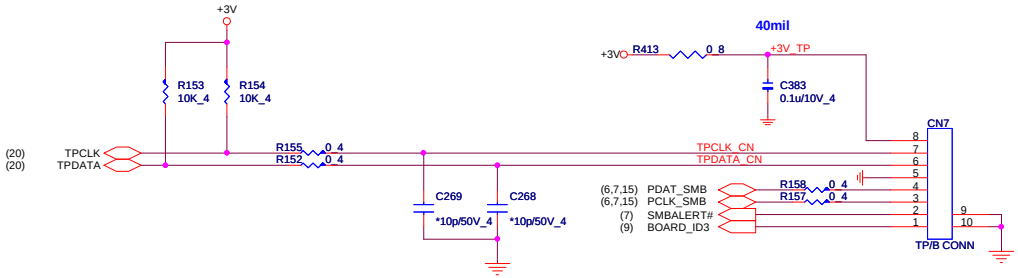


CPU FAN CTRL(THM)

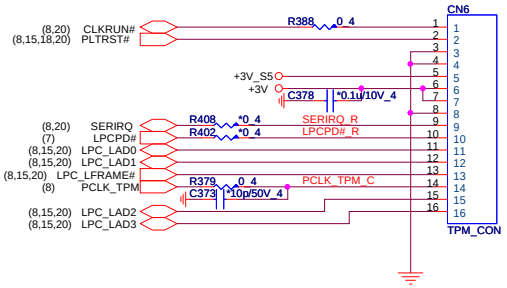




TOUCH PAD (TPD)



TPM (TPM)



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Size	Document Number	Rev
	KB/BT/TP/LED/Power Connector	1A

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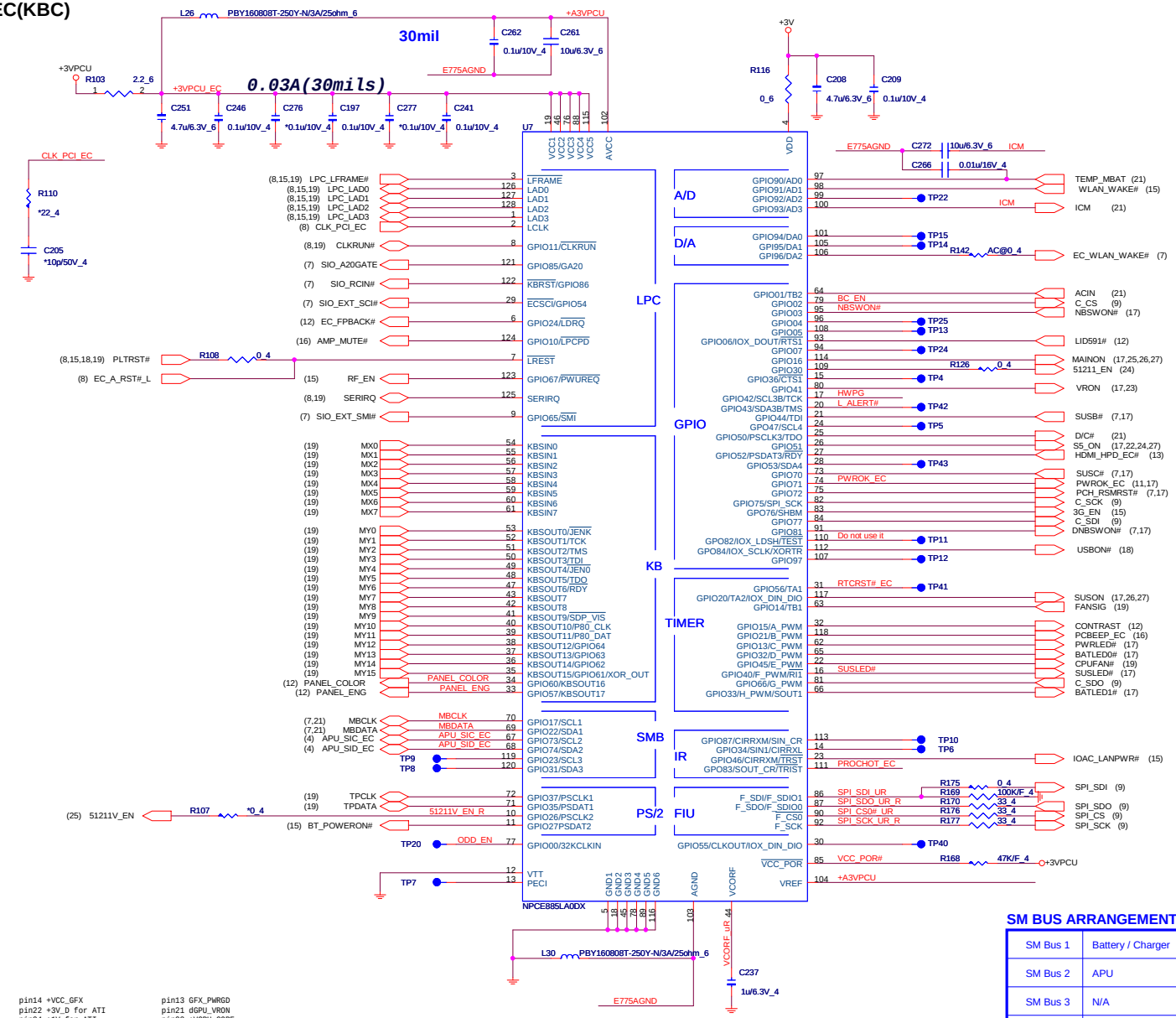
EC(KBC)



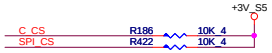
pin14 +VCC_GFX
pin22 +3V_D for ATI
pin24 +1V for ATI
pin26 +1.8V_GPU for ATI
pin28 GPU_RST#

pin13 GFX_PWRGD
pin21 dGPU_VRON
pin23 +VGPU_CORE
pin25 +1.5V_GPU
pin27 dGPU_PWROK

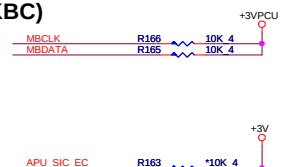
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery / Charger
SM Bus 2	APU
SM Bus 3	N/A
SM Bus 4	N/A

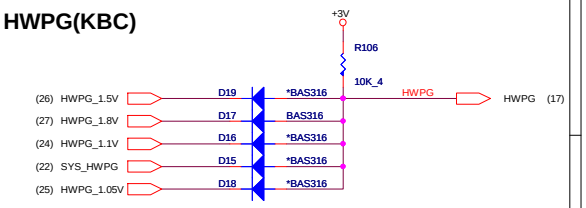
SPI PU(KBC)



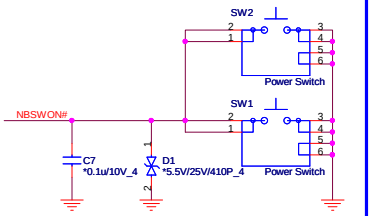
SM BUS PU(KBC)



HWPG(KBC)



POWER-ON SWITCH (UIF)



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	EC NPCE795CA0DX	1A
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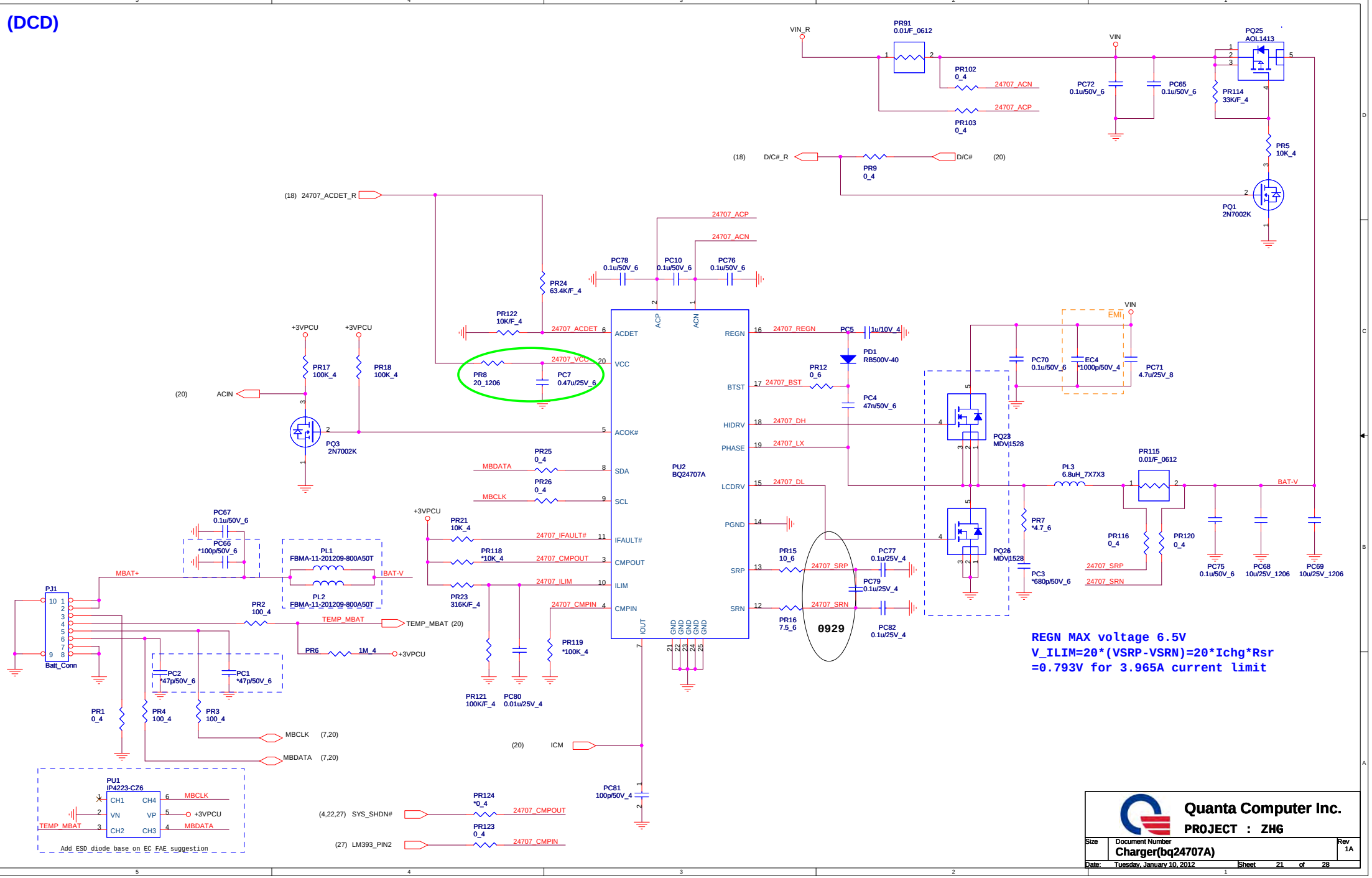
(DCD)
VIN_R
PR91 0.01/F_0612
PR102 0_4
24707_ACN
24707_ACP
PR103 0_4
VIN
PC72 0.1u/50V_6
PC65 0.1u/50V_6
PQ25 AOL1413
PR114 33K/F_4
PR5 10K_4
(18) D/C#_R
PR9 0_4
D/C#
(20)
PQ1 2N7002K
(18) 24707_ACDET_R
PR24 63.4K/F_4
PC78 0.1u/50V_6
PC10 0.1u/50V_6
PC76 0.1u/50V_6
PR122 10K/F_4
+3VPCU
PR17 100K_4
PR18 100K_4
(20) ACIN
PQ3 2N7002K
PR8 20_1206
PC7 0.47u/25V_6
ACDET
VCC
ACOK#
SDA
SCL
IFAULT#
CMPOUT
ILIM
CMPIN
IOUT
ACP
ACN
REGN
BTST
HIDRV
PHASE
LCDRV
PGND
SRP
SRN
PU2 BQ24707A
24707_REGN
PC5 1u/10V_4
PD1 RB500V-40
PR12 0_6
24707_BST
PC4 47n/50V_6
24707_DH
24707_LX
24707_DL
PR15 10_6
PR16 7.5_6
24707_SRP
24707_SRN
PC77 0.1u/25V_4
PC79 0.1u/25V_4
PC82 0.1u/25V_4
0929
PC70 0.1u/50V_6
EC4 *1000p/50V_4
PC71 4.7u/25V_8
EMI
PQ23 MDV1528
PQ26 MDV1528
PL3 6.8uH_7X7X3
PR115 0.01/F_0612
BAT-V
PR7 *4.7_6
PC3 *680p/50V_6
PR116 0_4
PR120 0_4
PC75 0.1u/50V_6
PC68 10u/25V_1206
PC69 10u/25V_1206
MBDATA
MBCLK
PR25 0_4
PR26 0_4
PC67 0.1u/50V_6
PC66 *100p/50V_6
PL1 FBMA-11-201209-800A50T
PL2 FBMA-11-201209-800A50T
MBAT+
IBAT-V
PJ1
Batt_Conn
PR2 100_4
TEMP_MBAT
TEMP_MBAT (20)
PR6 1M_4
+3VPCU
PC2 *47p/50V_6
PC1 *47p/50V_6
PR1 0_4
PR4 100_4
PR3 100_4
MBCLK (7,20)
MBDATA (7,20)
PR21 10K_4
PR118 *10K_4
PR23 316K/F_4
24707_IFAULT#
24707_CMPOUT
24707_ILIM
24707_CMPIN
PR119 *100K_4
PR121 100K/F_4
PC80 0.01u/25V_4
(20) ICM
PC81 100p/50V_4
PU1 IP4223-CZ6
CH1
CH2
VN
VP
CH3
CH4
Add ESD diode base on EC FAE suggestion
PR124 *0_4
PR123 0_4
(4,22,27) SYS_SHDN#
(27) LM393_PIN2
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
Quanta Computer Inc.
PROJECT : ZHG
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Charger(bq24707A)
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(DCD)

MAIND (24,26,27) SYS_SHDN# (4,21,27) SUSD (27)

Ven=7.23V

+5VPCU
5 Volt +/- 5%
TDC : 5A
PEAK : 6.6A
OCP : 8A
Width : 200mil

+3VPCU
3.3Volt +/- 5%
TDC : 5.02A
PEAK : 6.3A
OCP : 7.5A
Width : 200mil

OCP:8A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=8-(2.525/2)=6.74A
Vth=6.74A*14mOhm=94.32mV
R(Ilim)=(94.32mV*10)/10uA
=94.32K

OCP:7.5A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=7.5-(1.9/2)=6.55A
Vth=6.55A*14mOhm=91.7mV
R(Ilim)=(91.7mV*10)/10uA
~91K

+5V_S5
TDC : 1.88A
PEAK : 2.5A
Width : 80mil

+5V
TDC : 3.08A
PEAK : 4.1A
Width : 120mil

+3V
TDC : 2.48A
PEAK : 3.3A
Width : 100mil

+3VSUS
TDC : 1.426A
PEAK : 1.9A
Width : 60mil

+3V_S5
TDC : 0.62A
PEAK : 0.84A
Width : 40mil

Quanta Computer Inc.
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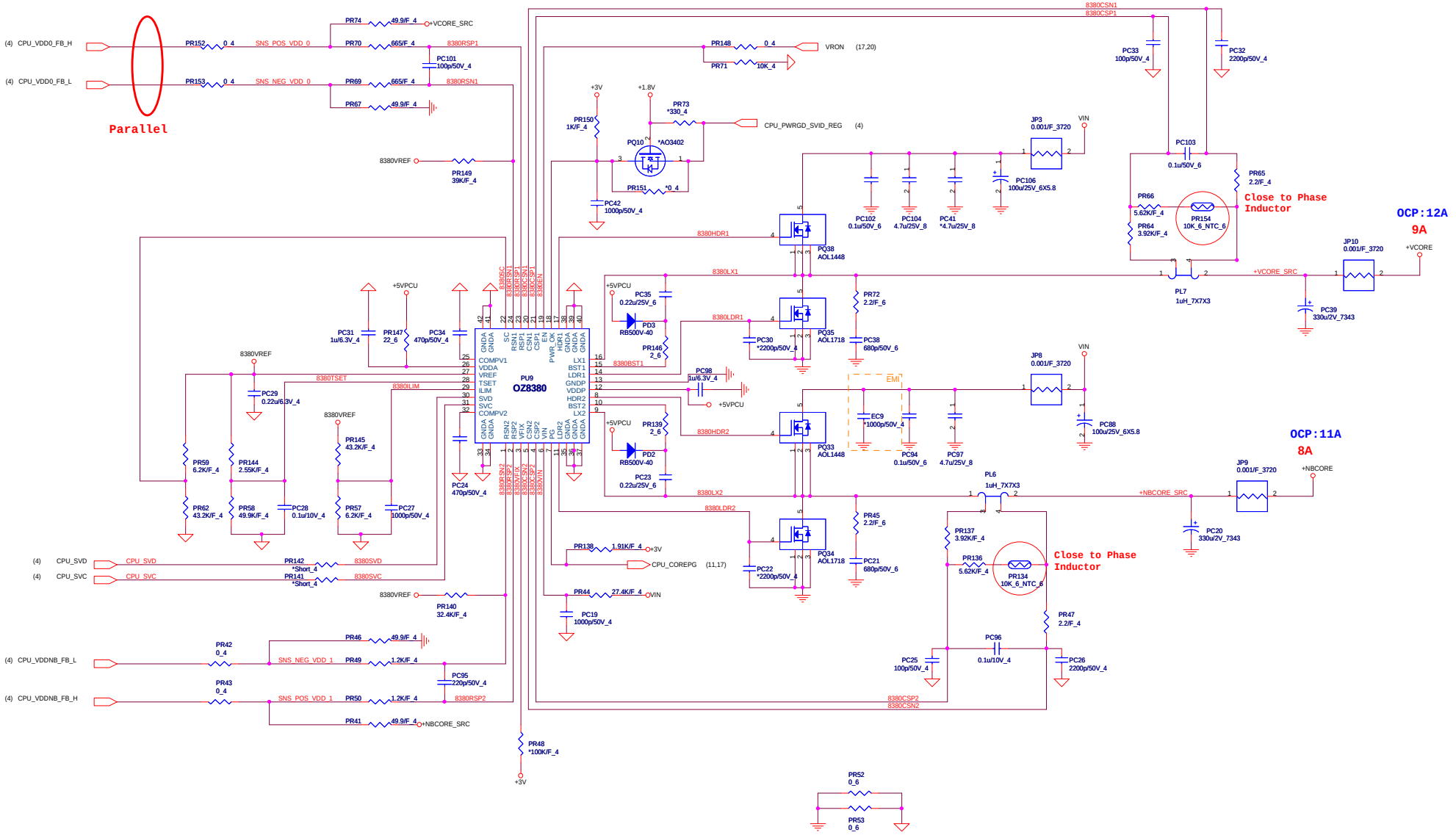
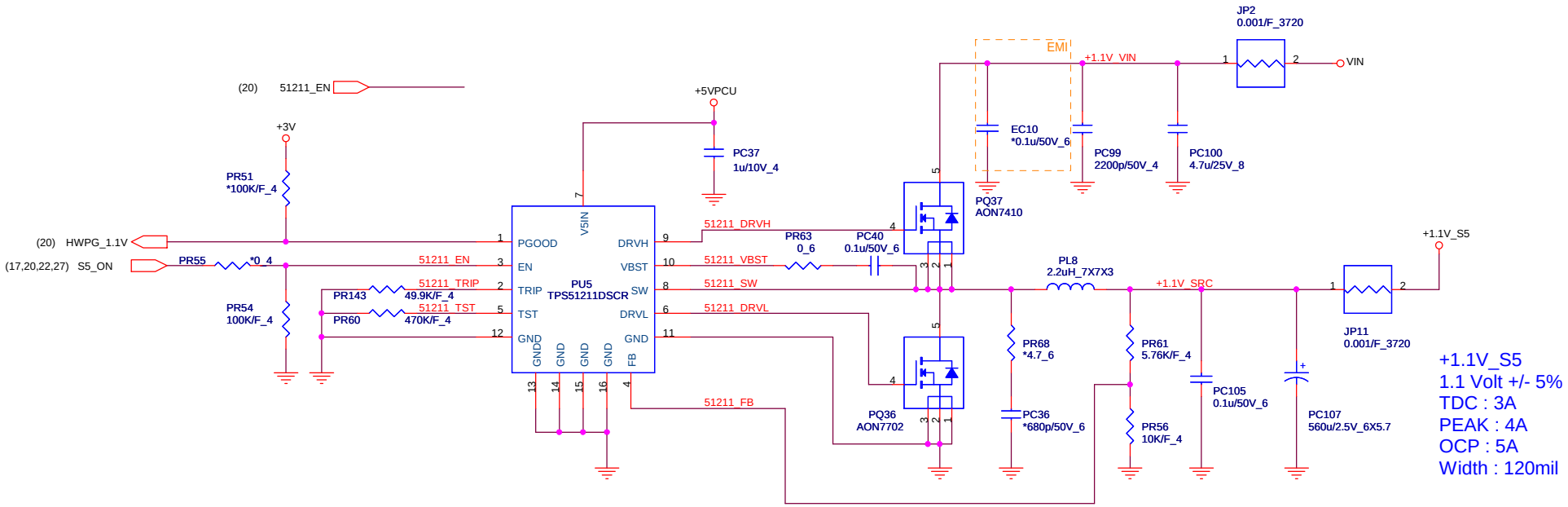
Size	Document Number	Rev
	SYSTEM 5V/3V (RT8223P)	1A
Date: Tuesday, January 10, 2012	Sheet 22 of 28	

(DCD)



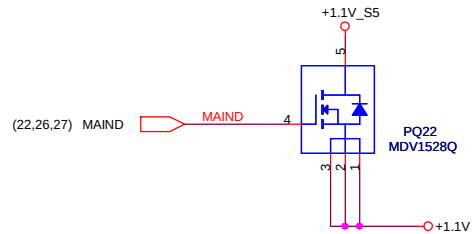
Quanta Computer Inc.		
PROJECT : ZHG		
Size	Document Number: CPU Core (OZ8380)	Rev: 1A
Date: Tuesday, January 10, 2012	Sheet 23 of 28	

(DCD)



+1.1V_S5
1.1 Volt +/- 5%
TDC : 3A
PEAK : 4A
OCP : 5A
Width : 120mil

OCP=5A
L ripple current
=(19-1.1)*1.1/(2.2u*290k*19)
=1.624A
Vtrip=5-(1.624/2)*14mohm
=0.058629V
Rlimit=0.058629/10uA*8=46.9Kohm



+1.1V
TDC : 2.73A
PEAK : 3.64A
Width : 120mil

Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	VCCP 1.1V(TPS51211)	1A
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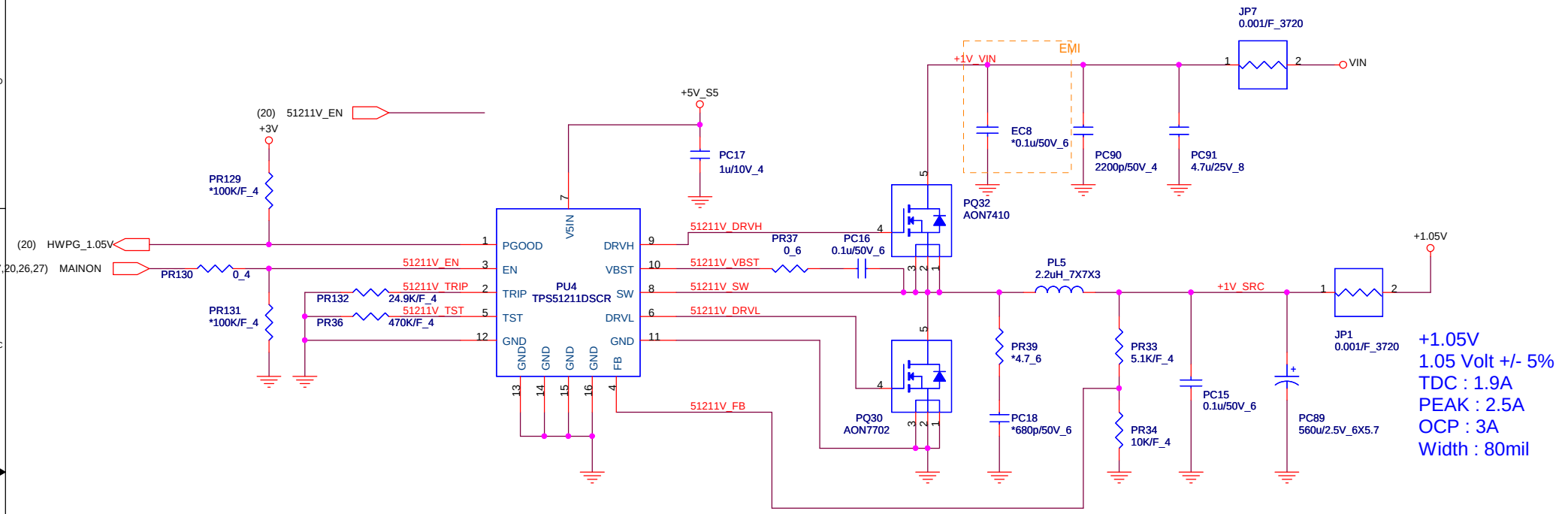
(DCD)



+1.05V
1.05 Volt +/- 5%
TDC : 1.9A
PEAK : 2.5A
OCP : 3A
Width : 80mil

OCP=3A
L ripple current
=(19-1.05)*1.05/(2.2u*290k*19)
=1.555A
Vtrip=3-(1.555/2)*14mohm
=0.03111V
Rlimit=0.03111/10uA*8=24.89Kohm

Quanta Computer Inc.		
PROJECT : ZHG		
Size	Document Number: +1.05V(TPS51211)	Rev: 1A
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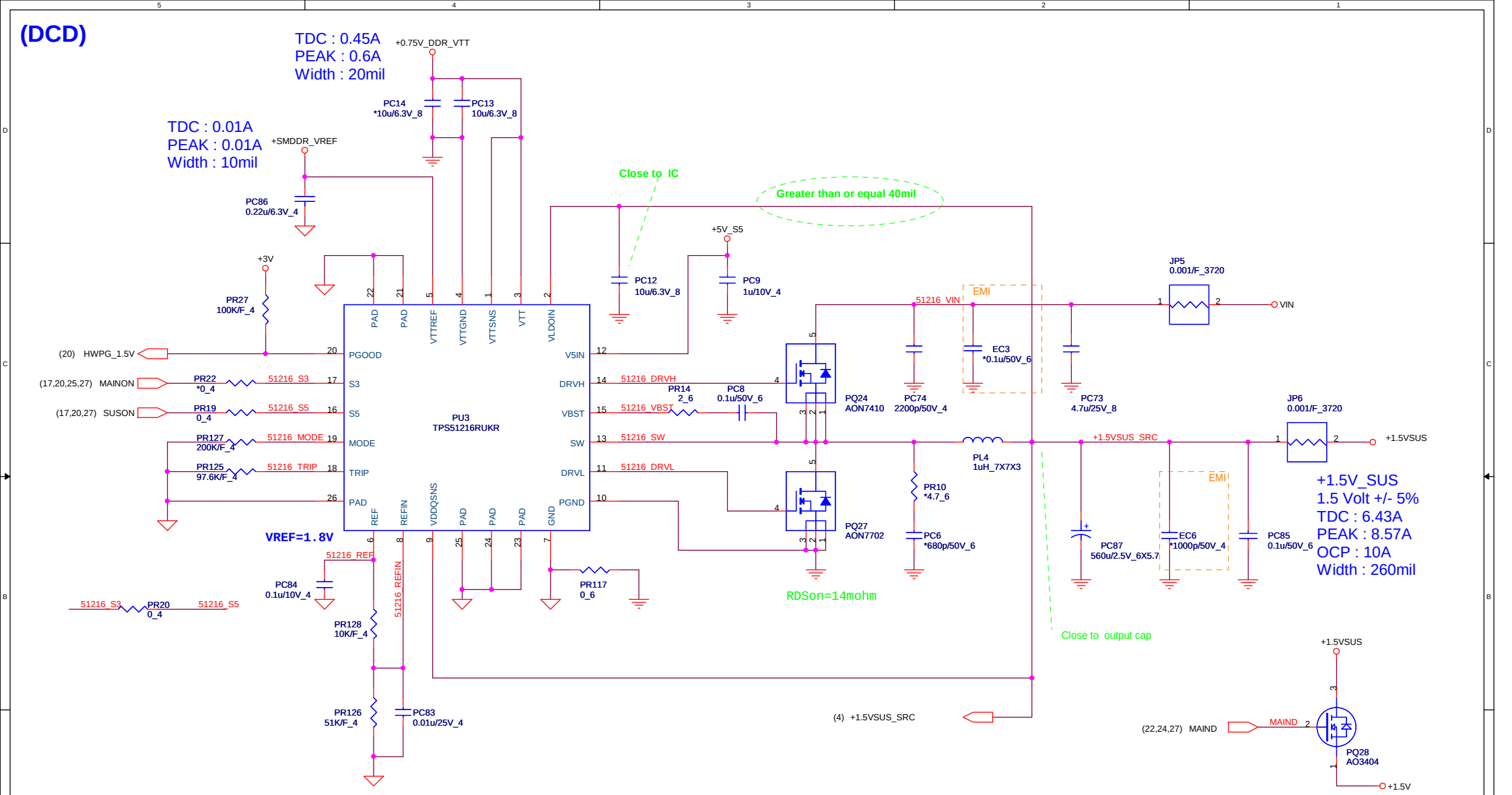

OCP=10A
L ripple current
=(19-1.5)*1.5/(1u*400k*19)
=3.454A
Vtrip=10-(3.454/2)*14mohm
=0.1158V
Rlimit=0.1158/10uA*8=92.657Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	DDR 1.5V(TPS51216)	1A

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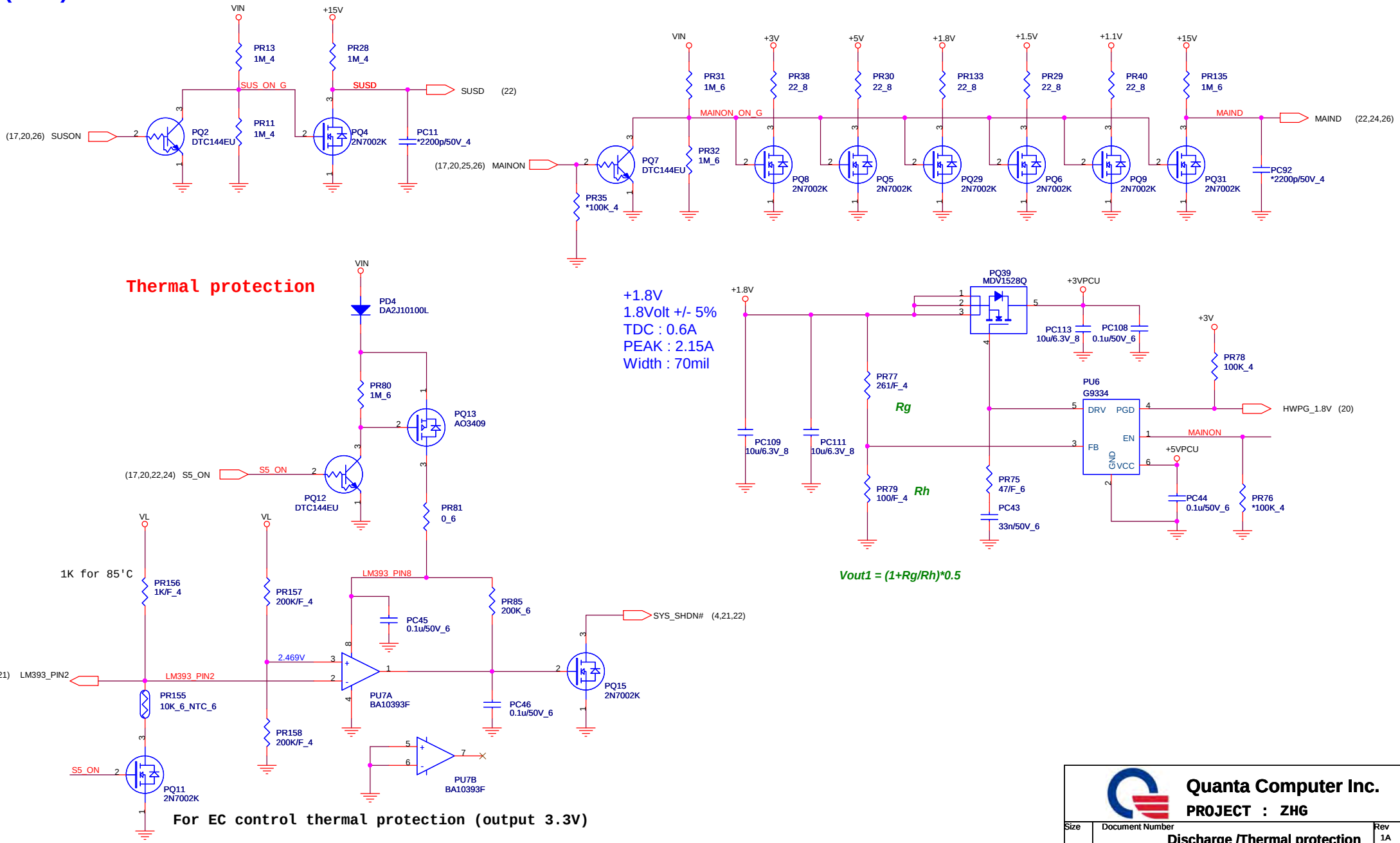
(DCD)



Quanta Computer Inc.		
PROJECT : ZHG		
Size	Document Number: Discharge /Thermal protection	Rev: 1A
Date: Tuesday, January 10, 2012	Sheet 27 of 28	

CHANGE LIST

MODEL	REV	
ZHG M/B	A	First Release

	B	Add R3439
		Del R237,R204,R222
		Change CN3016,CN3017,CN3018 footprint and PN
		Change PC101,PC104 PN
		
		Change CN3015,CN3006,CN3004 footprint
		SWAP RP9,RP10
		Add R3440,R3441,R3442,C6239,C6240,C6241
		Del TP53,TP15,TP14,TP24
		Change PR20 PN and footprint,PR12 PN
		Add R3443,R3444,R3446,R3445
		Update CN16,CN3011 PN
		
		Update CN16,CN3011 footprint
		Change PC73,PC79,PC80,PC82,PC83,PC90 footprint
		Swap CP3001,CP3002,CP3003,CP3004,CP3005,CP3006 pin
		Change CN3001 PN and footprint.
		Delete R3031,C3036,C3021
		Delete C3057,C3064,C3062,C3060,C3056,C3061
		Add R3447,R3448
		Delete TP21,TP11
		
		Add R3449 and change CN3008 PN and footprint
		Swap CN3001,RP8
		Change CN3017,CN3016 PN
		Delete R113,R125
		
		Change R3289 to 0ohm
		Swap Q3030 pin define
		PU Board_ID3 and Board_ID2, modify CN3008 net
		Delete R3009
		Change C3013 to 1uF
		Add R3450,R3451
		Change CN3003 pin define
		
		Swap L3026
		Change R142 to 100K
		Delete R3435,C3260. Change CN3008 PN and footprint
		Delete R3272,Q3019,R3256,R3270,TP18,TP25,TP28
		and add Q3036,Q3035,R3452
		Add PQ45,PR162,SW2,R3453,RP11,D3022
		Delete R3438
		Unstaff D10,D54,D55,R242,R206 and staff R369,R223,Q3033,RN3001
		
		Modify CN3003 and U4 pin define
		Add Q3037
		Unify the value, function code, P/N, description

	C	Delete T6,T15,R215,R202,Q12,R3425,R3426
		Add R3454,PQ46,C6242
		Add HOLE
		Update CN3015 PN
		Change CN3008 pin define
		Change CN3006 footprint
		Add R3460,C6243,R3457,R3459,R3455,
		R3456,Q3038,R3458,R3461 and reserve IOAC function
		
		Change Y3 footprint and staff R371
		Update U17,CN3015,CN14,CN3001 P/N
		Change CN3006 footprint
		Add R3462,Q3039
		Delete R163,RT1,R3459
		Add L3029~L3035,R3463~3476 for EMI
		Unstaff C418
		Staff R3418,R3200,R3434,R3439
		Change CN3008 PN and footprint
		
		Staff R115
		Delete CN3007 power trace for layout
		Add PQ47,PQ48,PR163,PR165,PR164,PC118
		Delete TP29 and add net 1.1V_S5_EN
		Add R3477,R3478
		
		Modify LVDS common choke pin define
		Add TP63~TP70 for layout
		Remove G2,G3 and add T3051,T3052
		Change Y3,C3041 footprint
		Modify PU2 pin define
		
		Change PR3,PR20,PR12,PC11 PN
		Add EC1~EC10 for RF
		Add EC11~EC18 for EMI
		Add R3479 and C6244,R3480,R3481
		Delete EC7,EC8,EC10,EC4,PAD3
		
		Staff PR154,R3480 and unstaff PR149
		Staff R206 and unstaff R223

Model	ZHG MB BOARD	
Page	From	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
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ZHG	PCBA NO : 31ZHGMB0000	REV: A	DOC. NO : 206
APPROVED BY : Edison Huang	CHECK BY : Kevin Hsieh	DRAWING BY : Benson Yo	DATE : 2012/01/10

Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	CHANGE LIST	1A
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