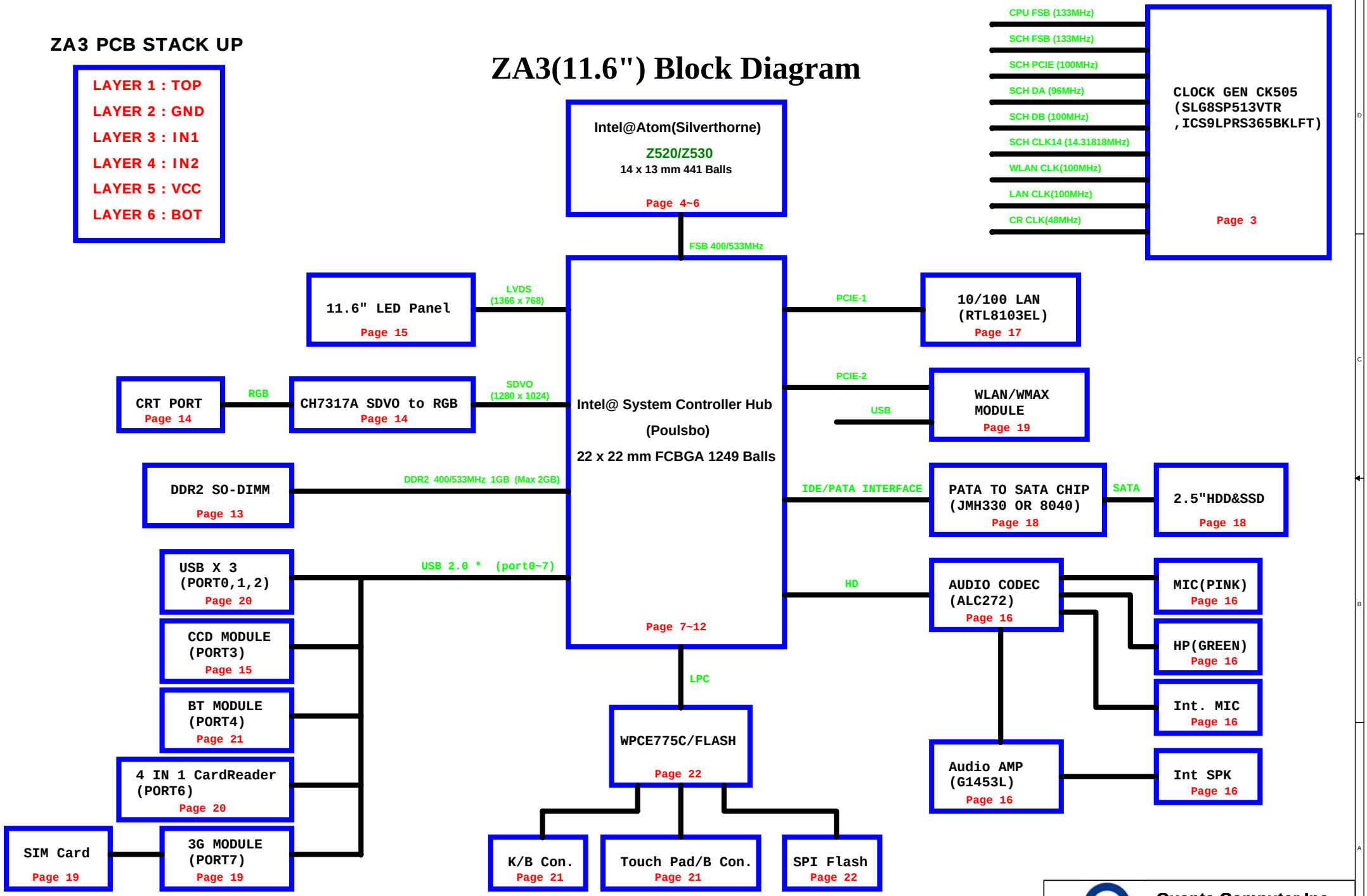
ZA3 PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

ZA3(11.6") Block Diagram

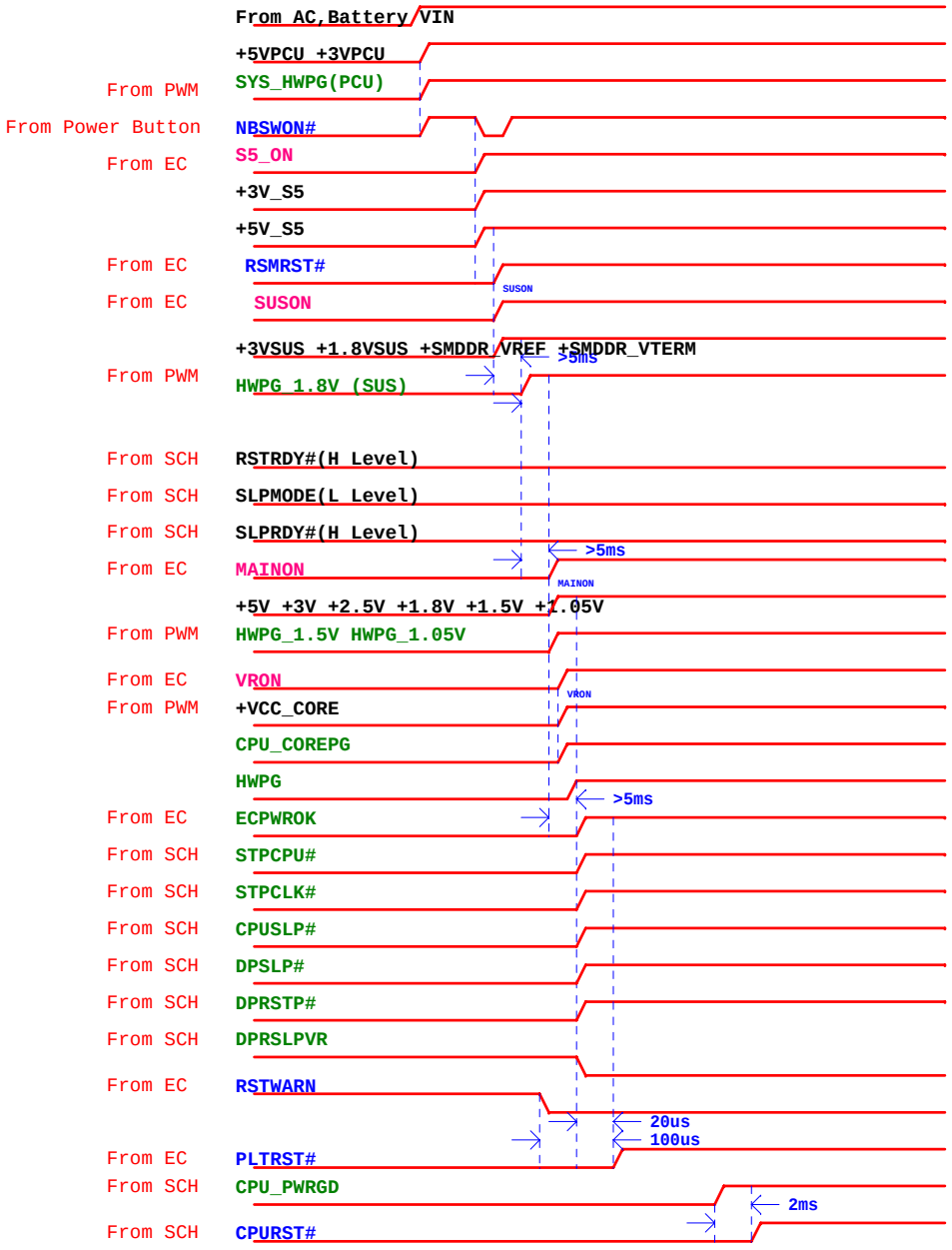


Quanta Computer Inc.
PROJECT : ZA3

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Sunday, March 08, 2009 Sheet 1 of 34

ZA3 Power On Sequence



BOM naming rule

Items	Function	Name	Description
1	PATA TO SATA BRIDGE	8040@	Marvell 88SE8040
2	PATA TO SATA BRIDGE	330@	Jmicron JMH330
3	3G Module	3G@	
4	FAN Module	FAN_PWM@	PWM FAN
5			
6			

Poulsbo SCH SMBUS Table

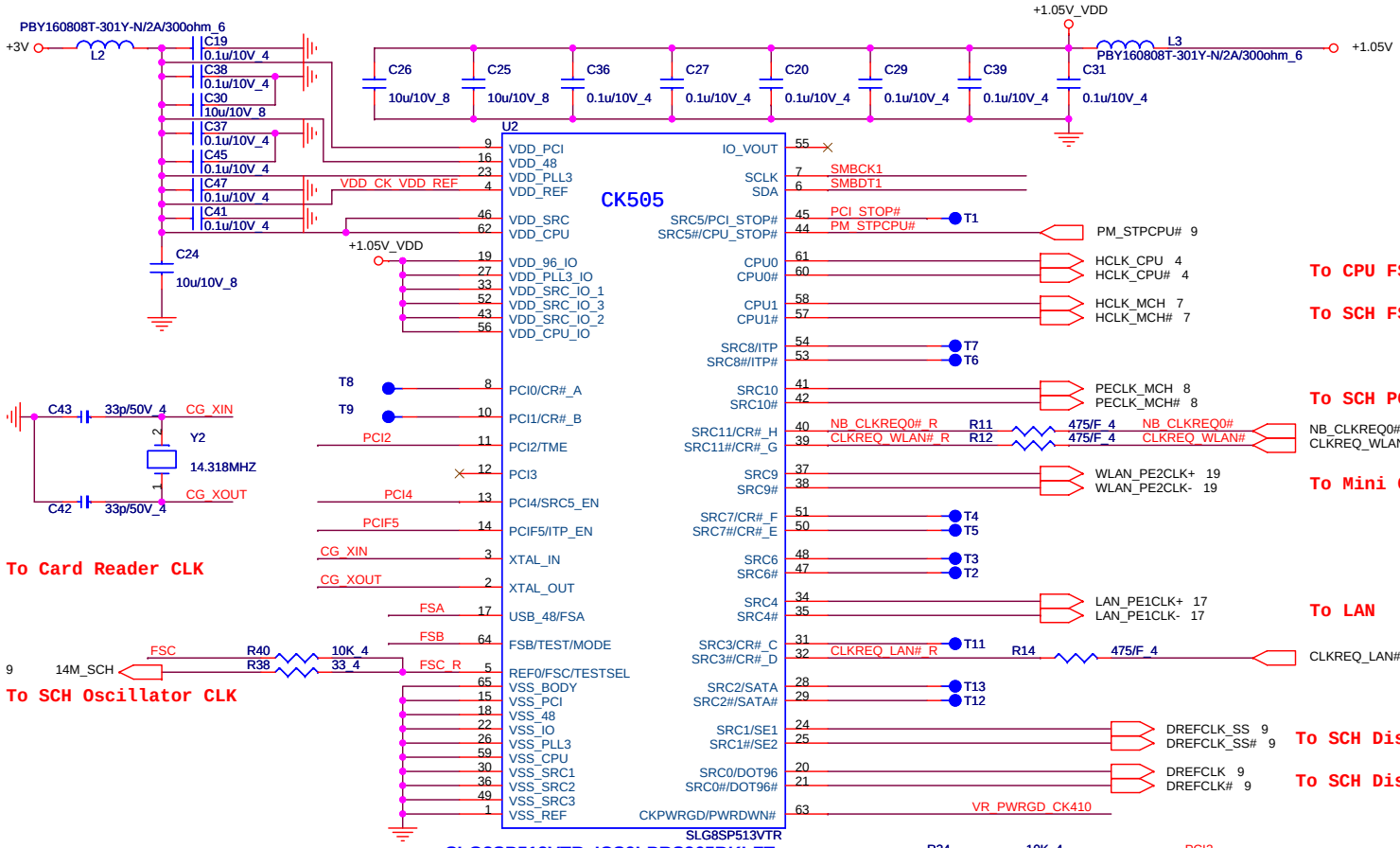
	CLK GEN	RAM	Mini Card (WLAN/WMAX)	Mini Card (3G)
(SMB_DATA) / (SMB_CLK) (+3V)	V	V	V	V
Power Plane	+3V	+3V	+3V	+3VSUS
MOS CKT	Reserve	Reserve	Reserve	Reserve

EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM
EC775 SDA1 / SCL1 (+3VPCU)	V		
EC775 SDA2 / SCL2 (+3VPCU)		V	V
Power Plane	+3VPCU	+3V	+3VPCU
MOS CKT	X	Stuff	X

Quanta Computer Inc.
PROJECT : ZA3
Size | Document Number: Power Sequence/ BOM Rule | Rev: 1A
Date: Sunday, March 08, 2009 | Sheet 2 of 34

Clock Generator(CLK)



To Card Reader CLK

To SCH Oscillator CLK

To CPU FSB CLK

To SCH FSB CLK

To SCH PCIE CLK

SCH PCIE CLKREQ

WLAN PCIE CLKREQ

To Mini Card 1 (WLAN/WMAX)

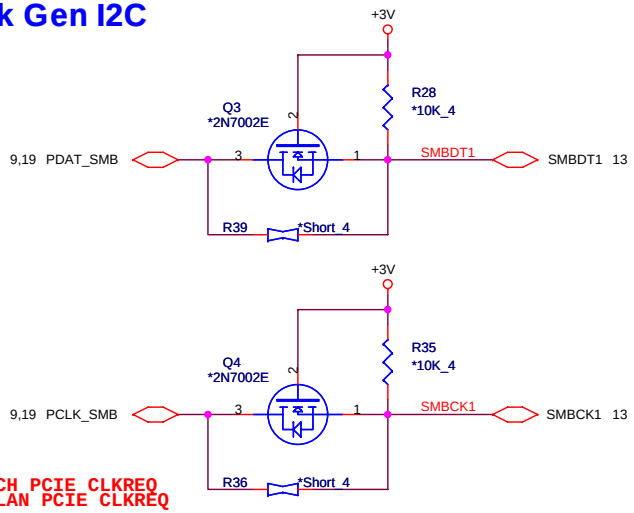
To LAN

LAN CLKREQ

To SCH Display PLLB CLK

To SCH Display PLLA CLK

Clock Gen I2C



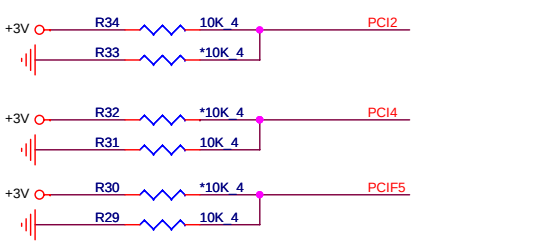
Modify R39 R36 footprint from RC0402 to SHORT0402 for 0 ohm cost down rev.c 20090301

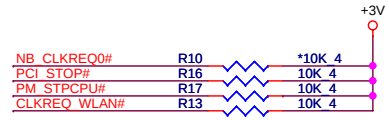
EMI

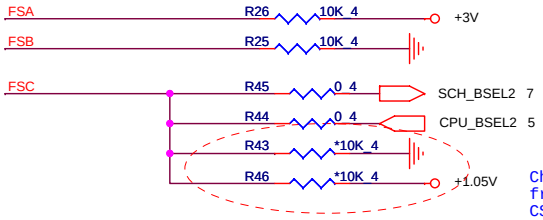
	SLG8SP513VTR (AL8SP513000)	ICS9LPRS365 (ALPRS365000)	PULL HIGH	PULL DOWN
Pin 11	PCI2/TME	PCI2/TME	NO OVERCLOCKING (default)	NORMAL RUN
Pin 13	PCI4/ 27_Select	PCI_4/ SEL_LCDCLK#	PIN 24/25 IS 27MHz	PIN 24/25 IS SRC/DOT (default)
Pin 14	PCIF-5/ITP_EN	PCIF-5/ITP_EN	PIN 53/54 IS CPUITP	PIN 53/54 IS SRC8 (default)

<MAIN> : SLG8SP513VTR(AL8SP513000)
<SECOND> : ICS9LPRS365BKLFT(ALPRS365000)

SLG8SP513VTR ,ICS9LPRS365BKLFT

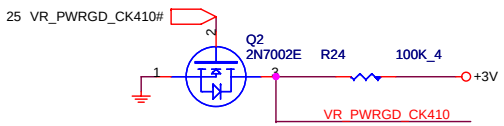






Change R43 P/N from CS00002JB38 to CS31002JB28 rev.c 20090301

CLK GEN & PWR



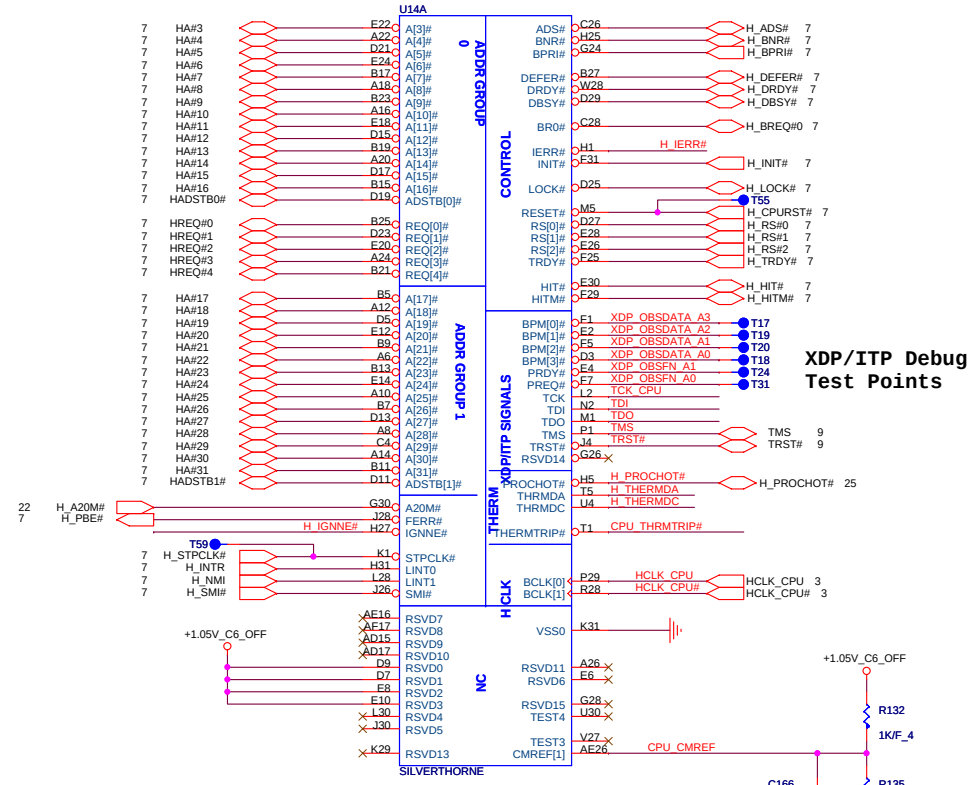
SEL2 SEL1 SEL0 Frequence select

FSC	FSB	FSA	CPU	SRC	PCI	States
1	0	1	100	100	33	
0	0	1	133	100	33	Default

Quanta Computer Inc.
PROJECT : ZA3

Size	Document Number	Rev
	CLOCK GEN(CK505)	1A
Date: Sunday, March 08, 2009	Sheet 3 of 34	

Silverthorne(CPU)

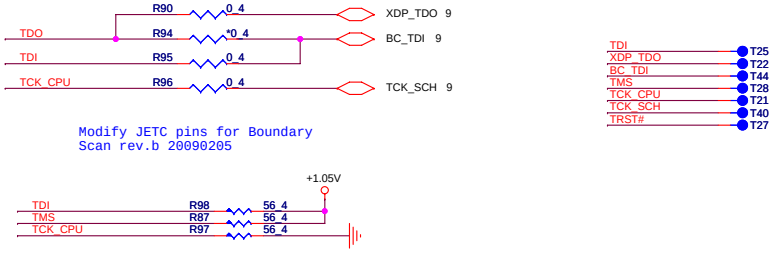


XDP/ITP Debug Test Points

T17 T19 T20 T18 T24 T31 T55 T59

Note : H_FERR# for layout length must be greater than 150mils 20081128

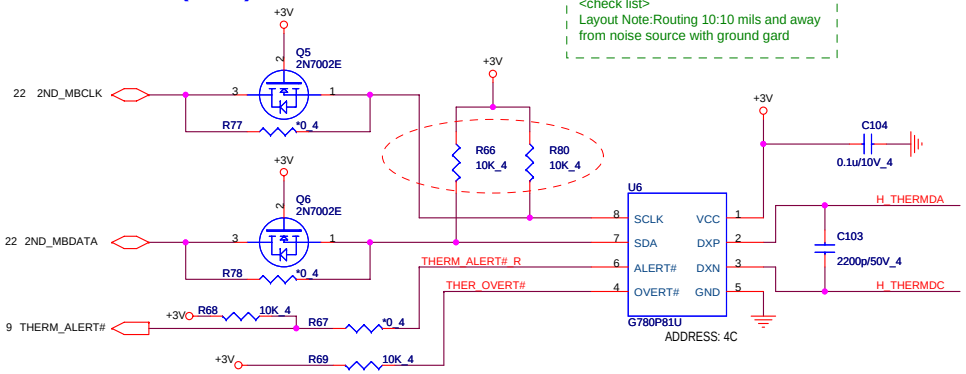
For intel suggest R115 connect to +1.05V_C6_OFF 20081218



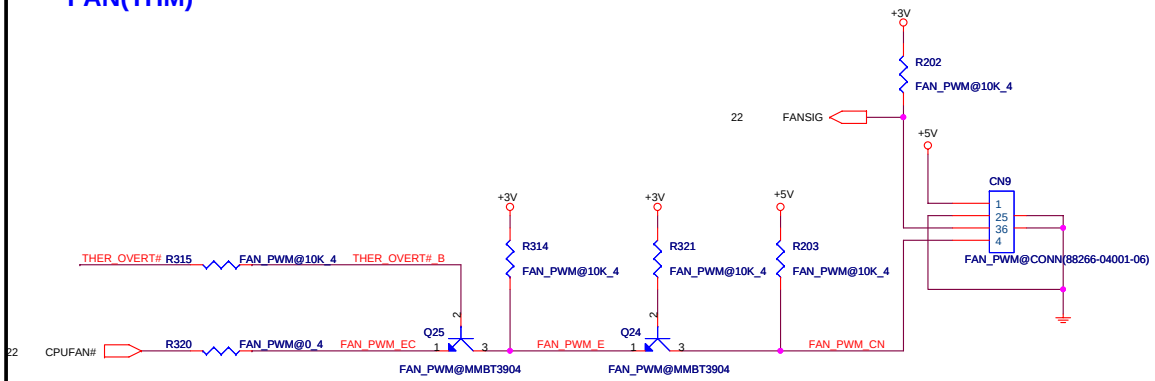
Modify JETC pins for Boundary Scan rev.b 20090205

CPU Thermal monitor(THM)

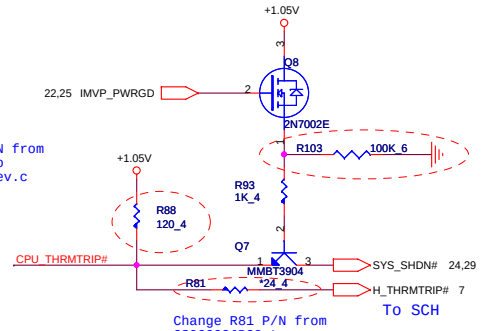
<check list>
Layout Note:Routing 10:10 mils and away from noise source with ground gard



FAN(THM)



Thermal Trip(CPU)



Change R88 P/N from CS05602JB17 to CS11202JB21 rev.c 20090301

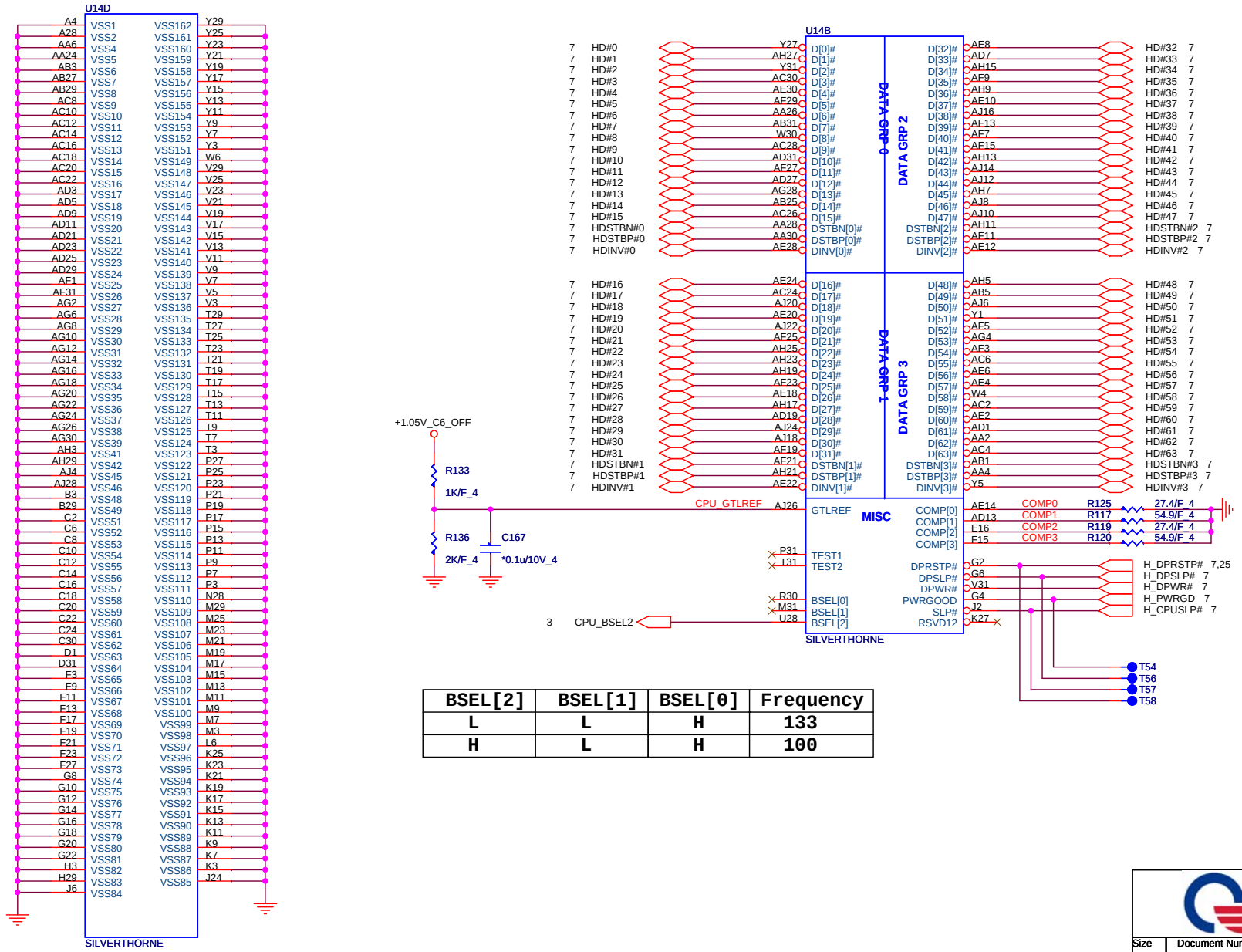
Change R81 P/N from CS00002JB38 to CS02402JB11 rev.c 20090301

Quanta Computer Inc.
PROJECT : ZA3

Size	Document Number	Rev
	Silverthorne CPU(01_HOST)	1A

Date: Sunday, March 08, 2009 Sheet 4 of 34

Silverthorne(CPU)



BSEL[2]	BSEL[1]	BSEL[0]	Frequency
L	L	H	133
H	L	H	100

Quanta Computer Inc.

PROJECT : ZA3

Size	Document Number	Rev
	Silverthorne CPU(02_HOST)	1A

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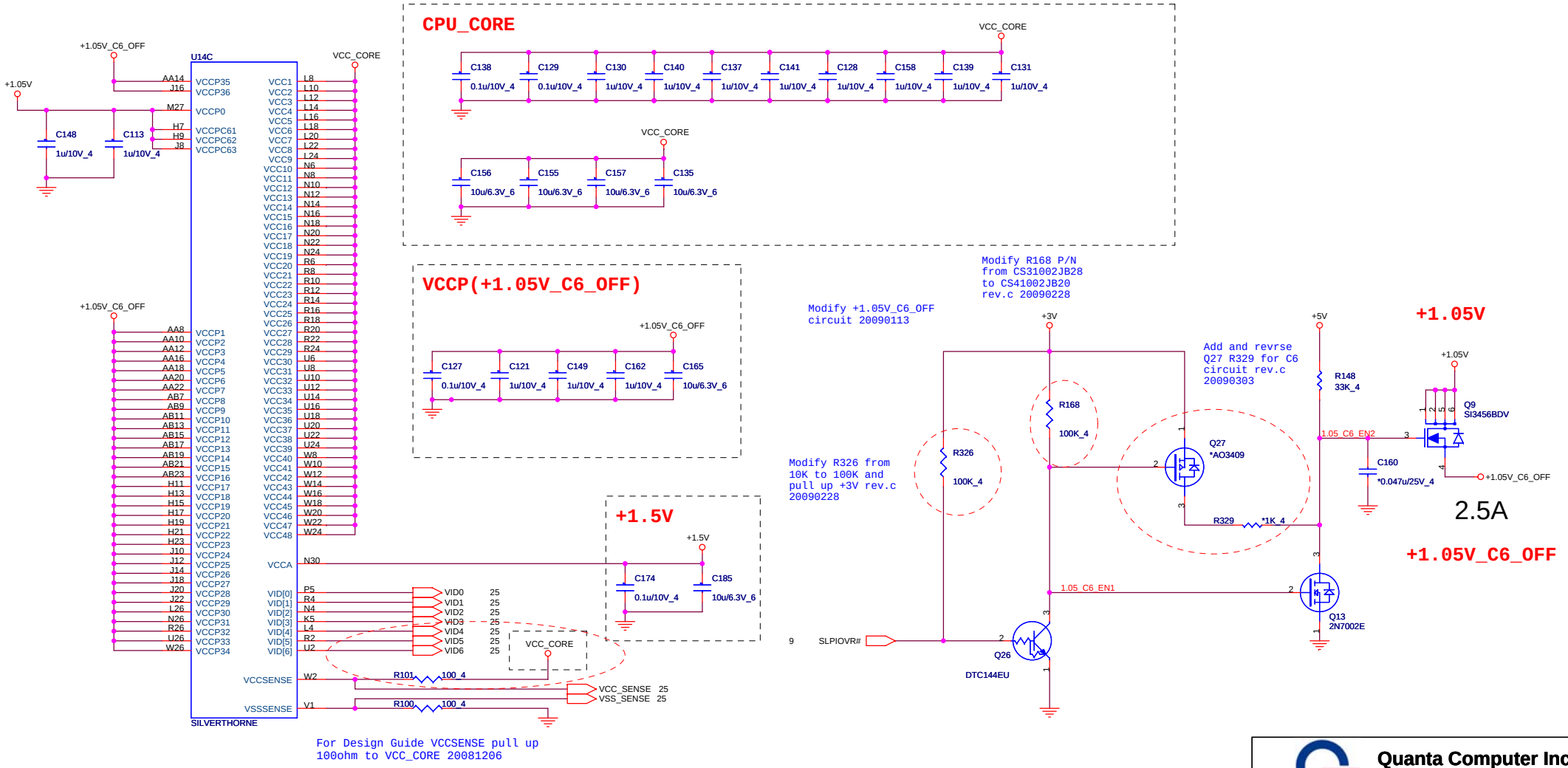
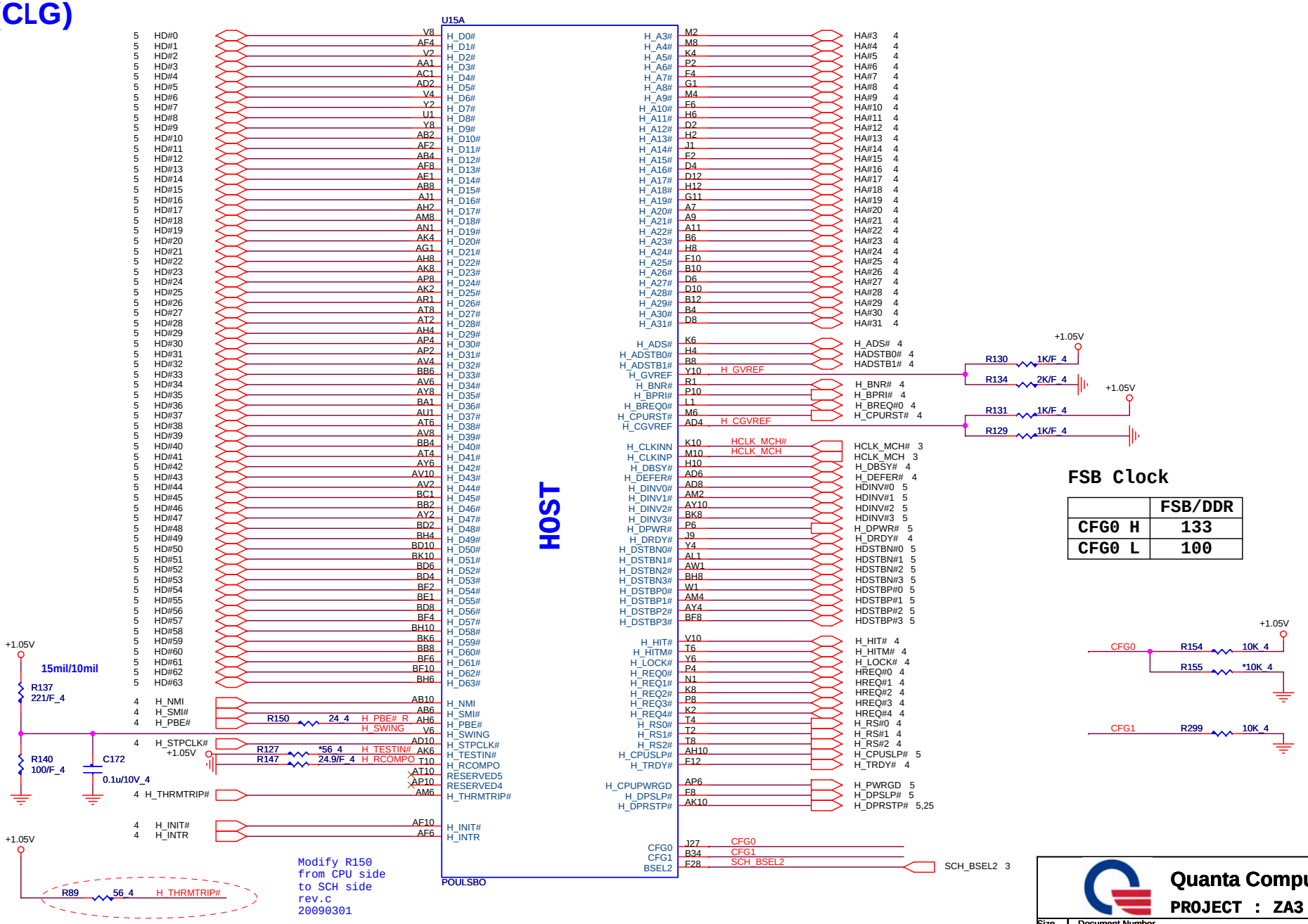
Silverthorne(CPU)



Quanta Computer Inc.		
PROJECT : ZA3		
Size	Document Number: Silverthorne CPU(03_Power)	Rev 1A
Date: Sunday, March 08, 2009	Sheet 6 of 34	

Poulsbo(CLG)



Quanta Computer Inc.	PROJECT : ZA3
Size	Document Number: Poulsbo(01_HOST) — Rev: 1A
Date: Sunday, March 08, 2009	Sheet 7 of 34

Poulsbo(CLG)

Stuff R312 for Keyboard
and TP issues rev.c
20090228

Add R333 R334
R335 R336 for
LPC AD0~AD3
rev.c 20090301

EMI

C192 *22p/50V_4 LCLK_EC

RTC Battery
SANYO: AHL03001502 ; ML1220-CM11
MATSUSHITA: AHL03001405 ; ML1220/USTC/TSB1
MAXELL: AHL03001404 ; ML1220-ZR1S

Add T60 T61 T62 T63
test point for
Boundary Scan rev.b
20090205

SCH_RSV1 : (LPC_CLKOUT0 buffer strength)
0 = 1 Load driver strength
1 = 2 Load driver strength
*** intel has integrated 300K puii-up

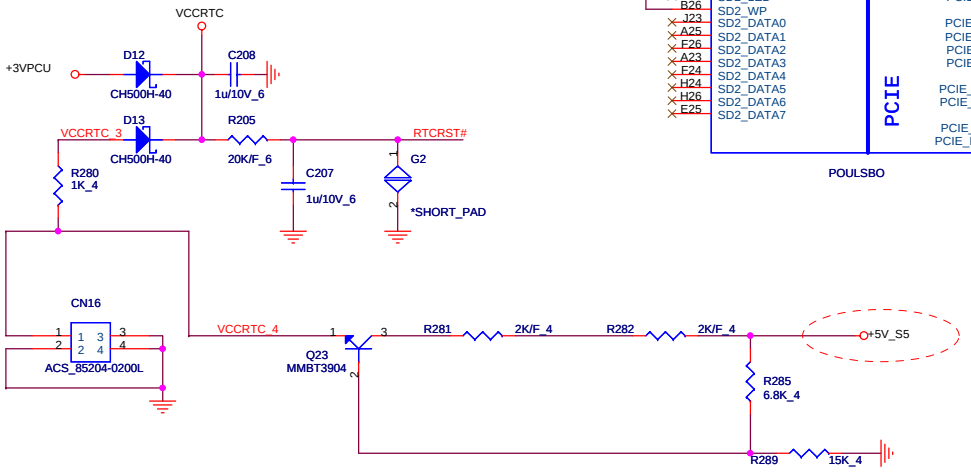
Change C233 C231 C243
C240 C239 C238 C237
C235 from SDVO chip
side to SCH side rev.c
20090301

SDVO to CRT

PCIE TO LAN

PCIE TO WLAN/WMAX

RTC(RTC)



Poulsbo(CLG)

0--MB USB PORT1
1--MB USB PORT2
2--DB USB PORT3
3--CCD Module
4--BT Module
5--MINI WLAN/WMAX
6--CARD READER
7--MINI 3G Module

U15C

USB I/F
Termination Voltage
PATA/IDE
JTAG
SYSTEM GPIOs
HD AUDIO
CLOCK I/F
SMB
No-Connect

USBP0- USBP0+ USBP1- USBP1+ USBP2- USBP2+ USBP3- USBP3+ USBP4- USBP4+ USBP5- USBP5+ USBP6- USBP6+ USBP7- USBP7+
USB_DN0 USB_DP0 USB_DN1 USB_DP1 USB_DN2 USB_DP2 USB_DN3 USB_DP3 USB_DN4 USB_DP4 USB_DN5 USB_DP5 USB_DN6 USB_DP6 USB_DN7 USB_DP7

USBOC#0_1 USBOC#2
USB_OC0# USB_OC1# USB_OC2# USB_OC3# USB_OC4# USB_OC5# USB_OC6# USB_OC7#

+3V_S5
R240 10K_4
R124 10K_4

R128 22.6/F_4 USB_RBIAS_P/N
USB_RBIASN USB_RBIASP

PDDREQ PIORDY IRQ14 PDDACK# PDIOW# PDIOR# PDCS3# PDCS1#
PATA_DDREQ PATA_IORDY PATA_IDEIRQ PATA_DDACK# PATA_DIOW# PATA_DIOR# PATA_DCS3# PATA_DCS1#

PDA2 PDA1 PDA0
PATA_DA2 PATA_DA1 PATA_DA0

PDD15 PDD14 PDD13 PDD12 PDD11 PDD10 PDD9 PDD8 PDD7 PDD6 PDD5 PDD4 PDD3 PDD2 PDD1 PDD0
PATA_DD15 PATA_DD14 PATA_DD13 PATA_DD12 PATA_DD11 PATA_DD10 PATA_DD9 PATA_DD8 PATA_DD7 PATA_DD6 PATA_DD5 PATA_DD4 PATA_DD3 PATA_DD2 PATA_DD1 PATA_DD0

+3V
R301 4.7K_4 PIORDY
R279 10K_4 IRQ14

VTT_1 VTT_2 VTT_3 VTT_4 VTT_5 VTT_6 VTT_7 VTT_8 VTT_9 VTT_10 VTT_11 VTT_12 VTT_13 VTT_14 VTT_15 VTT_16 VTT_17 VTT_18 VTT_19 VTT_20 VTT_21 VTT_22 VTT_23 VTT_24 VTT_25 VTT_26 VTT_27 VTT_28 VTT_29 VTT_16

+1.05V
C124 1u/10V_4
C143 *1u/10V_4
C153 *1u/10V_4
C145 10u/6.3V_6

Change R186 R184 R309 R296
P/N from CS31002JB28 to
CS21002JB34 rev.c 20090301

+3V
R316 *10K_4 BOARD_ID0 R317 *10K_4
R319 *10K_4 BOARD_ID1 R318 *10K_4

ID1	ID0	Functions
0	0	
0	1	
1	0	
1	1	

* : Default

+3V
R186 *1K_4 SCH_GPIO3 R184 *1K_4
R309 *1K_4 SCH_GPIO0 R296 *1K_4

GPIO3	GPIO0	CMC Base Add.
0	0	FFFB000h
0	1	FFFC000h
1	0	FFFD000h(*)
1	1	FFFE000h

* : Default

XDP/ITP Debug Test Points

Modify JETC pins for Boundary
Scan rev.b 20090205

+1.05V
BC_TDI R265 56_4
XDP_TDO R260 200_4
TMS R259 56_4
TRST# R244 1K_4
R257 *56_4
TCK_SCH R256 56_4

TRST# TMS TDI TDO TCK
TRST# 4
TMS 4
BC_TDI 4
XDP_TDO 4
TCK_SCH 4

STPCPU# PM_STPCPU# 3

RSTRDY# PM_RSTRDY# 22
RESET# PLTRST# 14,17,18,19,20,22
RSTWARN PM_RSTWARN 22

GPIOSUS0 SW# T45
GPIOSUS1
GPIOSUS2 DNBSWON# DNBSWON# 22
GPIOSUS3 T50

WAKE# PCIE_WAKE# R R116 *0_4 PCIE_WAKE# 17,19
SMI# EC_SMI# EC_SMI# 22
THRMB THERM_ALERT# 4
GPE# EC_SCI# EC_SCI# 22

Change R297 from
+3V_S5 to +3V
for SMI# rev.c
20090304

+3V
ACZ_SDOUT_AUDIO R263 *1K_4
EC_SMI# R297 10K_4

+3V_S5
DNBSWON# R236 10K_4
PCIE_WAKE# R R238 1K_4
EC_SCI# R245 *10K_4
SWI# R239 *10K_4

GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9
SCH_GPIO0 T51
T48
SCH_GPIO3 T52
BOARD_ID0 T41
BOARD_ID1
SLPIOVR# 6 T53
T49

NB_CLKREQ0# R295 10K_4

SPKR SB_BEEP 16
HDA_CLK ACZ_BITCLK_AUDIO_R R277 33_4 ACZ_BITCLK_AUDIO 16
HDA_SYNC ACZ_SYNC_AUDIO_R R283 33_4 ACZ_SYNC_AUDIO 16
HDA_RST# ACZ_RESET#_AUDIO_R R284 33_4 ACZ_RESET#_AUDIO 16
HDA_SDI0 ACZ_SDIN0 16
HDA_SDI1
HDA_SDO ACZ_SDOUT_AUDIO_R R264 33_4 ACZ_SDOUT_AUDIO 16
HDA_DOCKEN# T47
HDA_DOCKRST# T46

For intel suggest add R295 pull
down 20081218

RESERVED6
RESERVED7
DA_REFCLKINN DREFCLK# 3
DA_REFCLKINP DREFCLK 3
DB_REFCLKINNSSC DREFCLK_SS# 3
DB_REFCLKINPSSC DREFCLK_SS 3
CLKREQ# NB_CLKREQ0# 3
CLK14 14M_SCH 3
USB_CLK48 14M_SCH
SUSCLK

SCH GFX Clock
SCH GFX SS Clock

SMB_ALERT# SMB_DATA SMB_CLK
SMB_ALERT# R308 10K_4 +3V
PDAT_SMB PDAT_SMB 3,19
PCLK_SMB PCLK_SMB 3,19
R337 10K_4 +3V
R338 10K_4

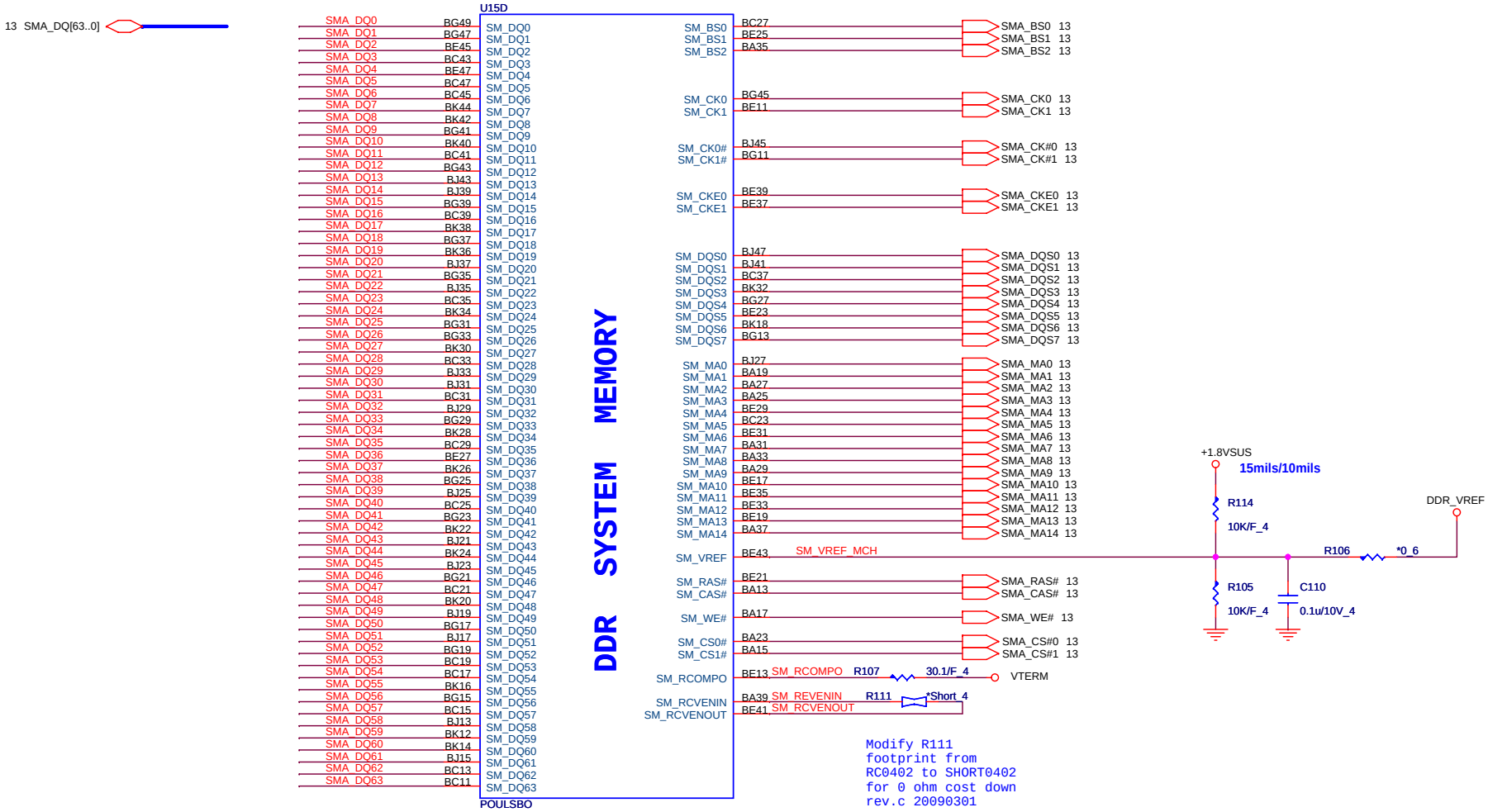
Del RN8 and Add R337 R338 to SCH
SMBUS rev.c 20090301

POULSBO

Quanta Computer Inc.
PROJECT : ZA3

Size	Document Number	Rev
	Poulsbo(03_USB/PATA/HD)	1A
Date: Sunday, March 08, 2009	Sheet 9 of 34	

Poulsbo(CLG)



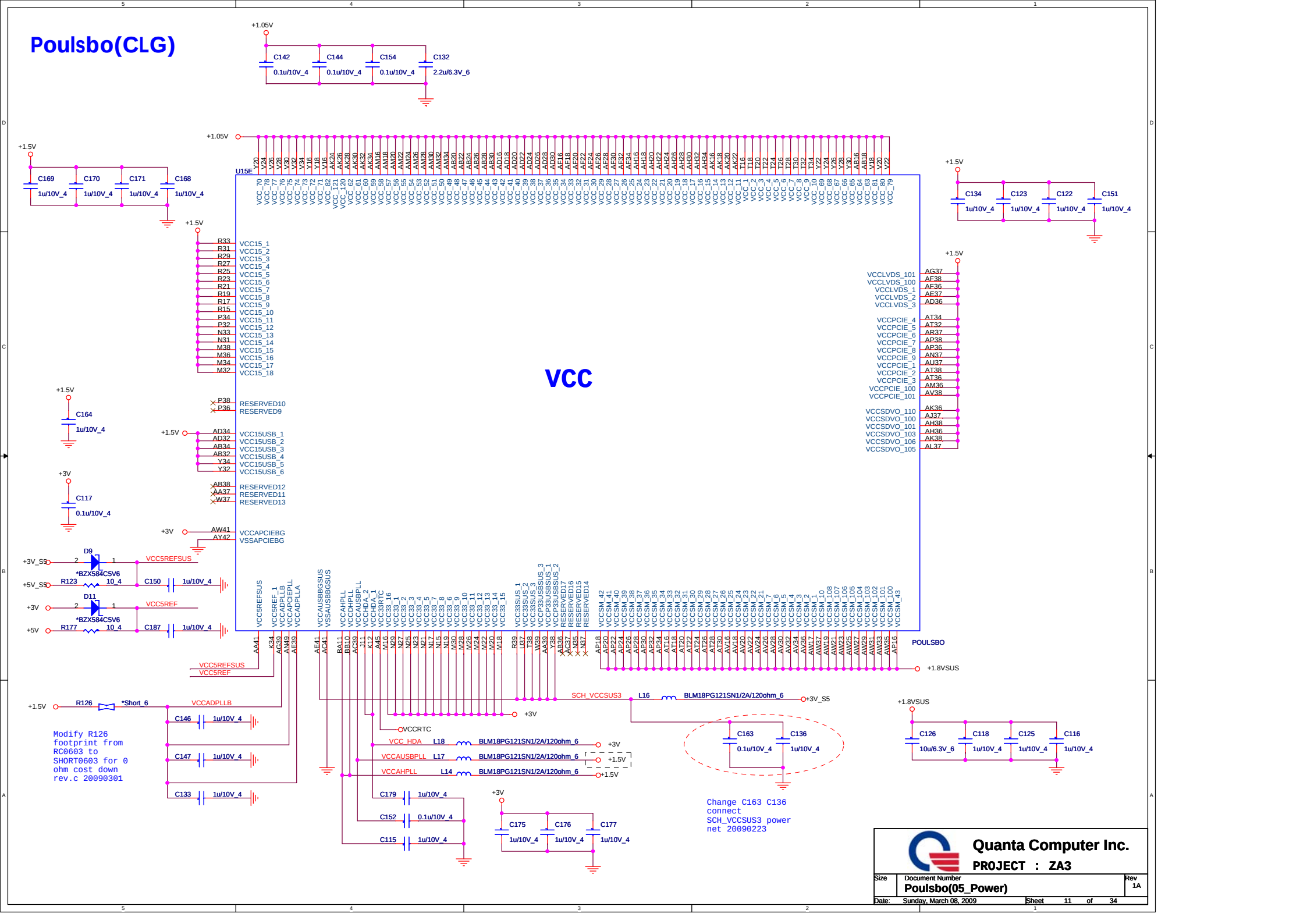
Quanta Computer Inc.

PROJECT : ZA3

Size	Document Number	Rev
	Poulsbo(04_MEM)	1A

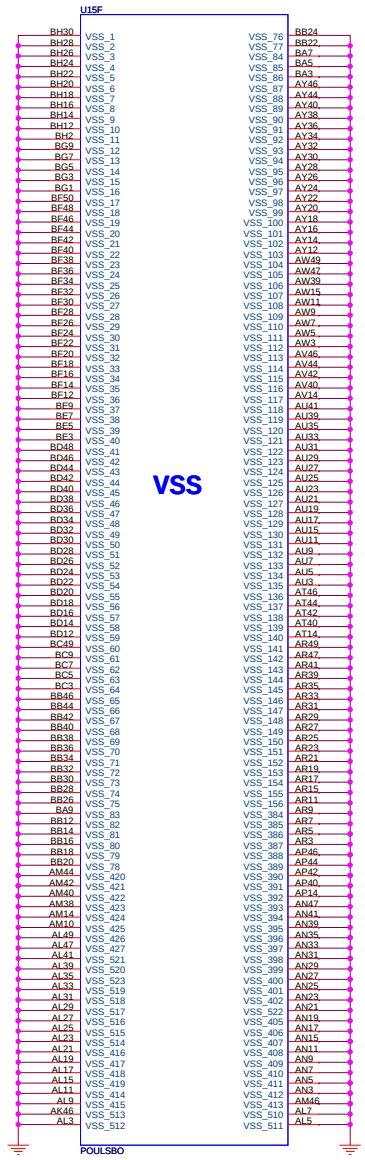
Date: Sunday, March 08, 2009 Sheet 10 of 34

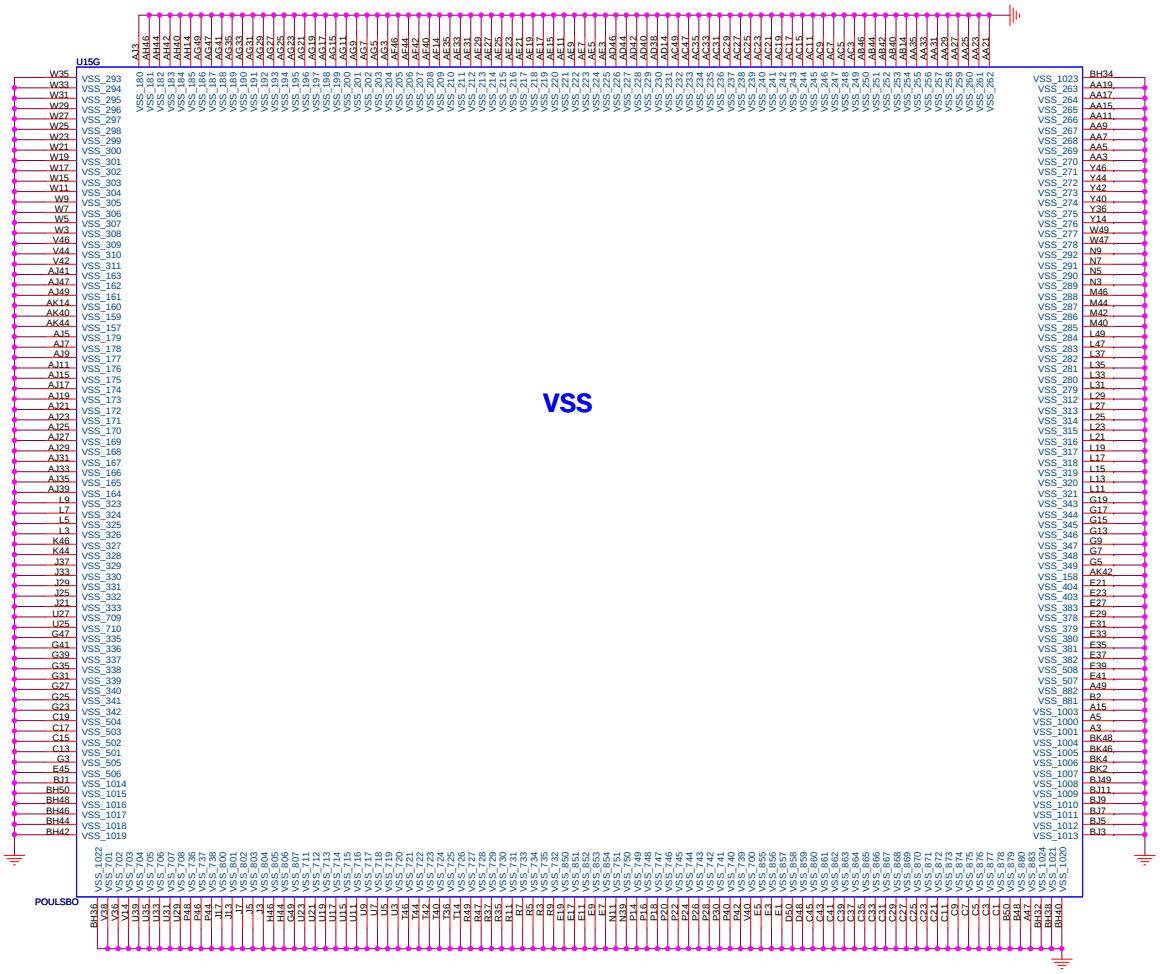
Poulsbo(CLG)



Quanta Computer Inc.			
PROJECT : ZA3			
Size	Document Number		Rev
	Poulsbo(05_Power)		1A
Date:	Sunday, March 08, 2009	Sheet 11 of 34	

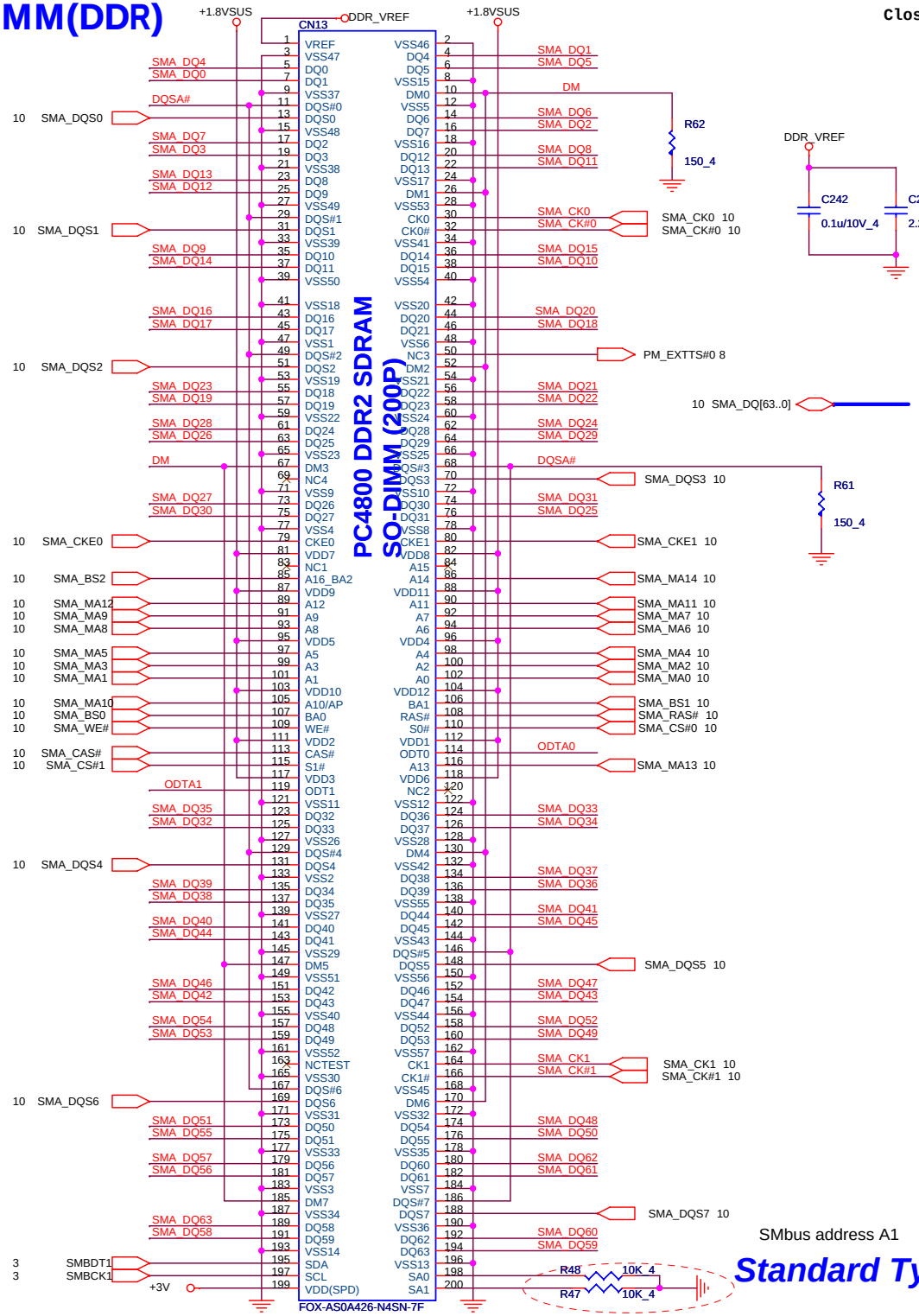
Poulsbo(CLG)



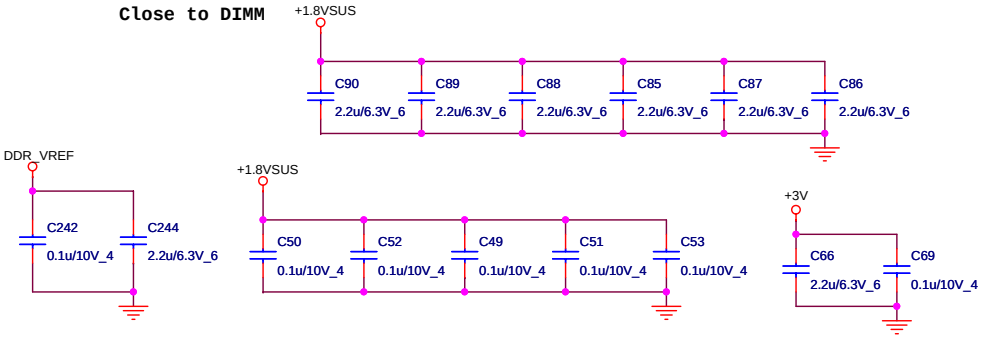


Quanta Computer Inc.	
PROJECT : ZA3	
Size	Document Number: Poulsbo(06_GND) — Rev: 1A
Date: Sunday, March 08, 2009	Sheet 12 of 34

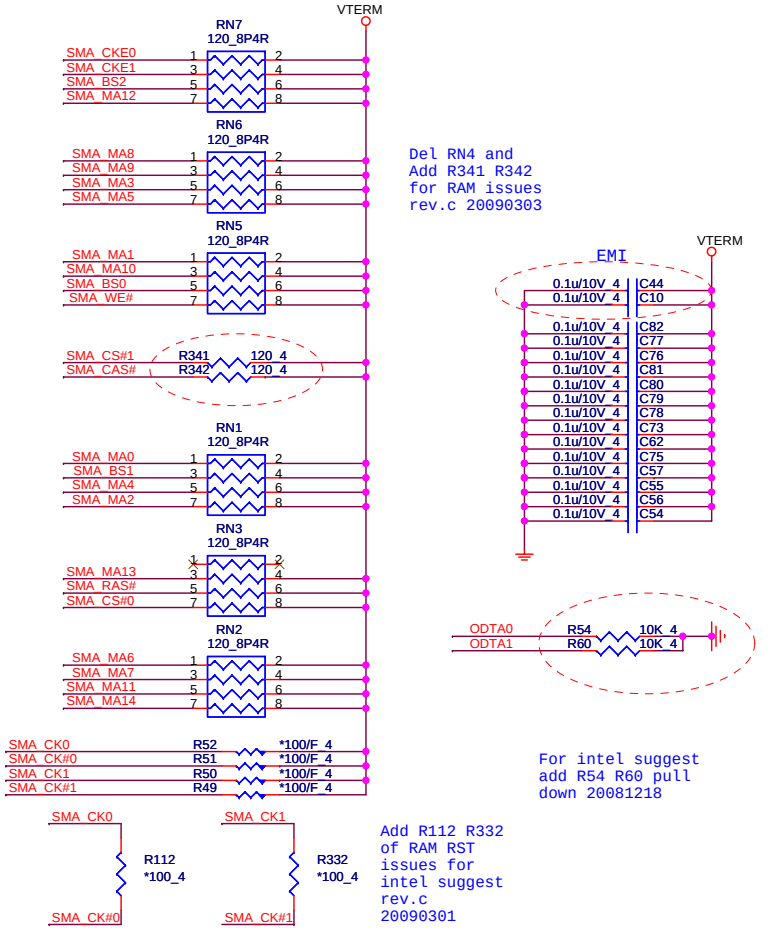
SO-DIMM(DDR)



Close to DIMM



Termination resistor



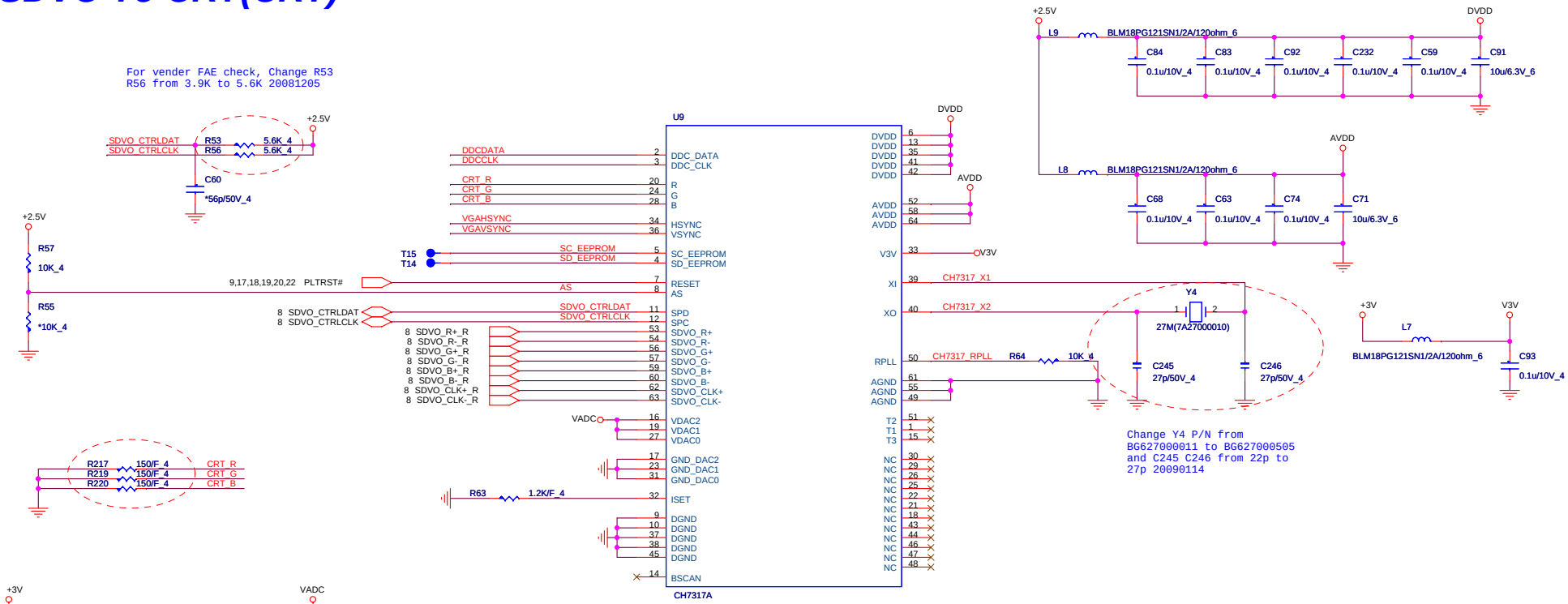
Standard Type H: 4.0mm

Quanta Computer Inc.

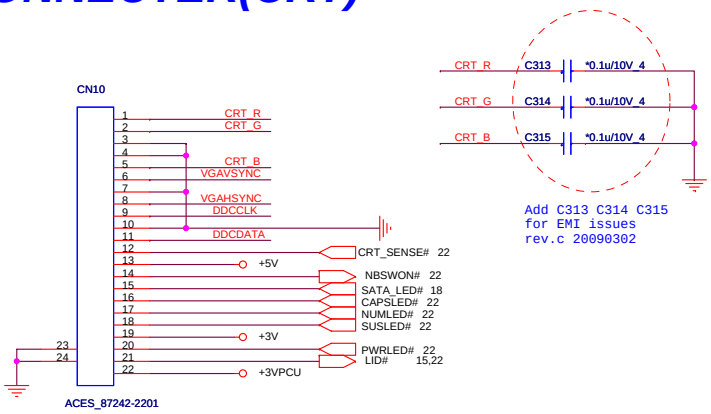
PROJECT : ZA3

Size	Document Number	Rev
	DDR2 SO-DIMM(200P)	1A
Date: Sunday, March 08, 2009	Sheet 13 of 34	

SDVO To CRT(CRT)

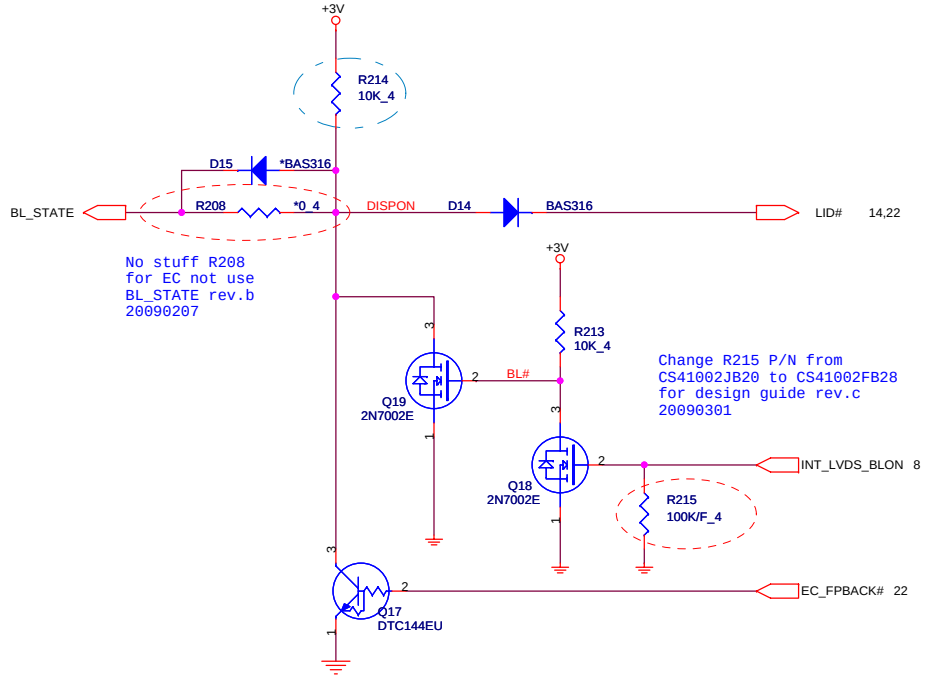


CRT DB CONNECTER(CRT)

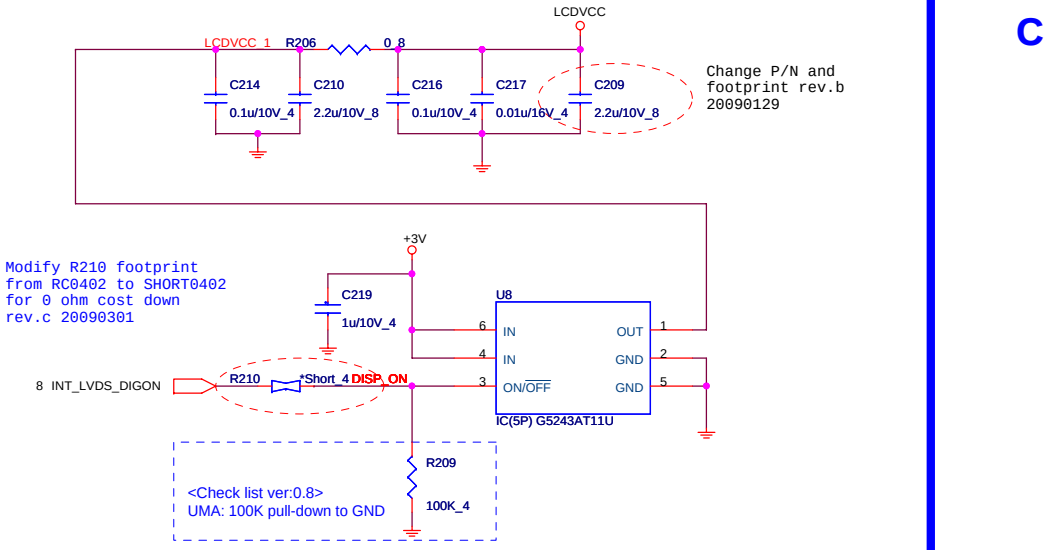


Quanta Computer Inc.		
PROJECT : ZA3		
Size	Document Number: SDVO TO CRT(CH7317A)	Rev: 1A
Date: Sunday, March 08, 2009	Sheet 14 of 34	

Backlight Control(LDS)

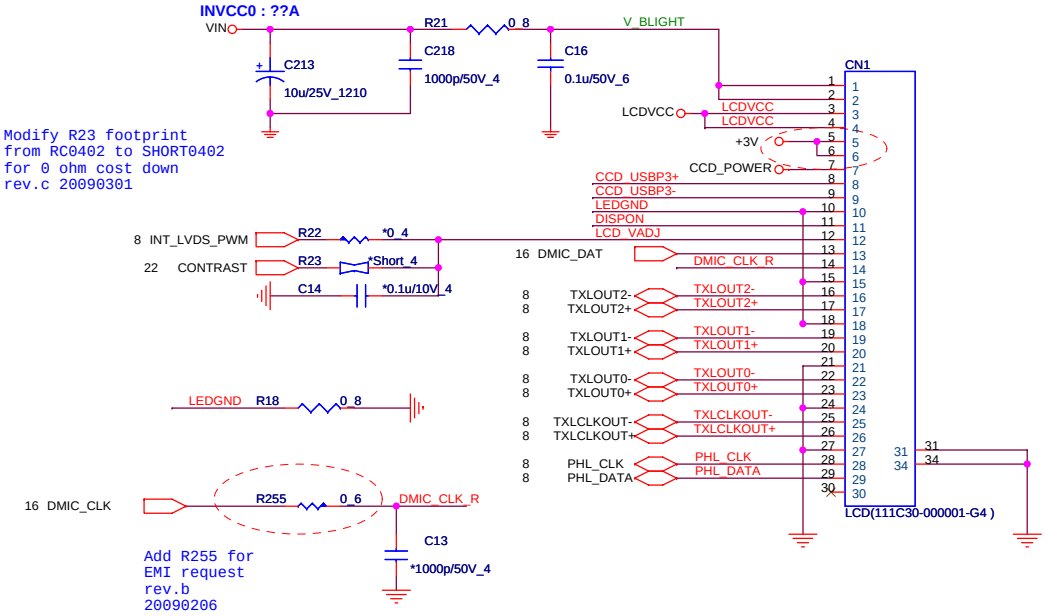


LED Panel POWER SWITCH(LDS)

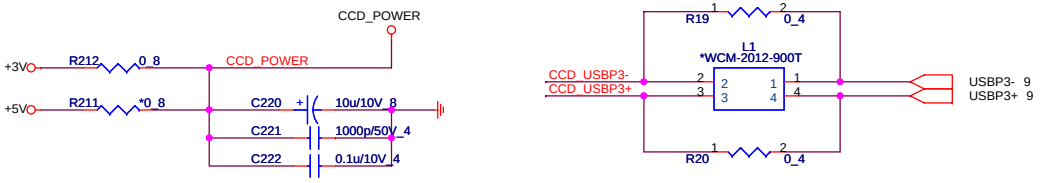


LED Panel(LDS)

V_BLIGHT : ?V ?A



Camera(CCD)

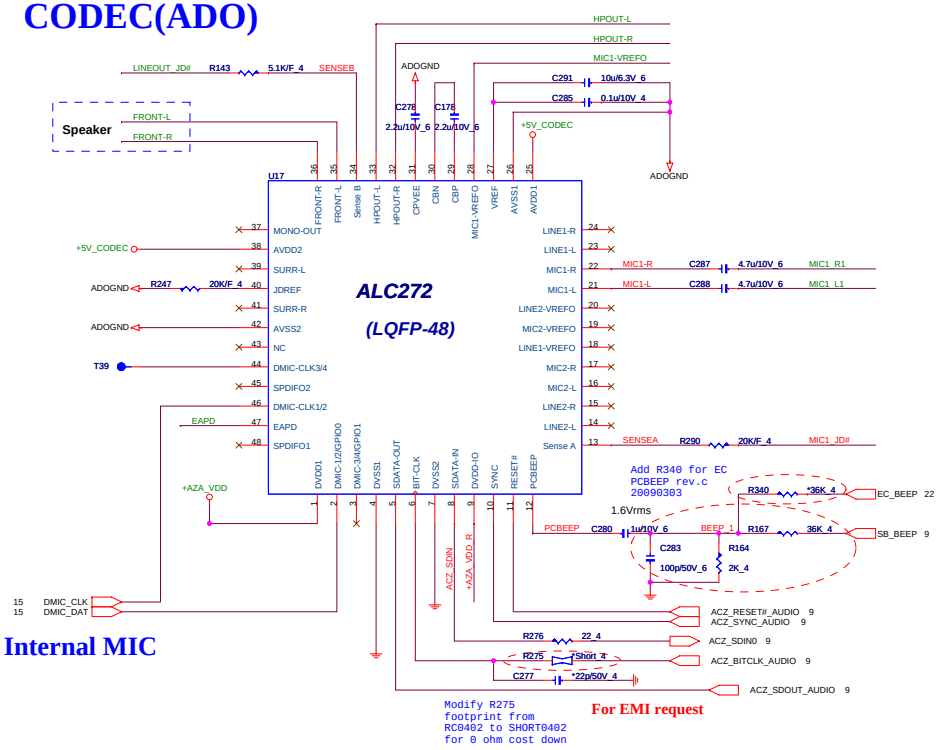


Quanta Computer Inc.

PROJECT : ZA3

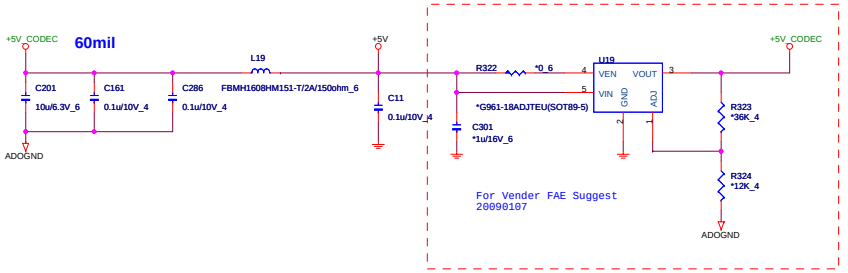
Size	Document Number	Rev
	LED PANEL/CCD MODULE	1A
Date: Sunday, March 08, 2009	Sheet 15 of 34	

CODEC(ADO)

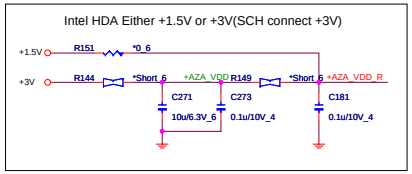


Internal MIC

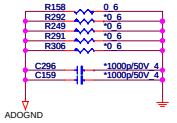
Codec Power(ADO)



HDA Power(ADO)

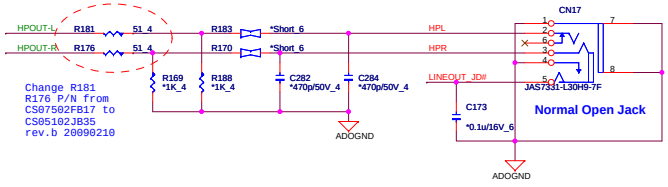


Modify R144 R149 footprint
from RC0603 to SHORT0603
for 0 ohm cost down rev.c
20090301



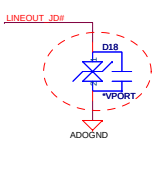
HP_Green(AMP)

Modify R170 R183 footprint
from RC0603 to SHORT0603
for 0 ohm cost down rev.c
20090301



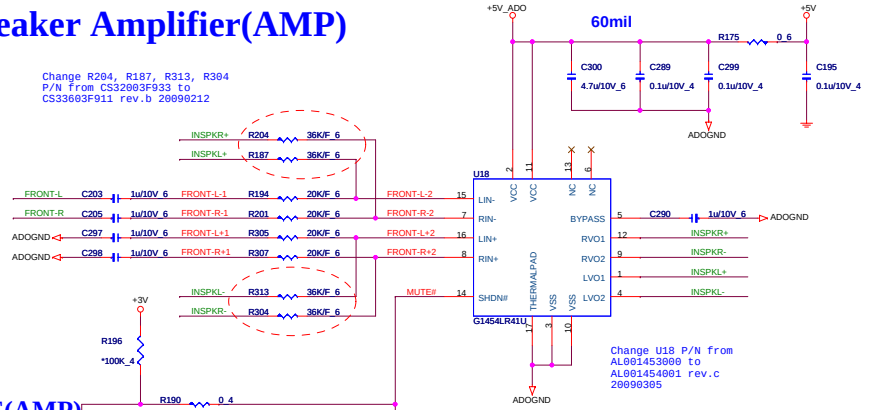
Change R181
R176 P/N from
CS07502FB17 to
CS05102JB35
rev.b 20090210

HP_Green ESD(EMC)

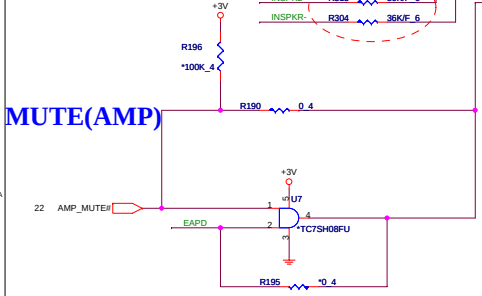


Speaker Amplifier(AMP)

Change R204, R187, R313, R304
P/N from CS32003F933 to
CS33603F911 rev.b 20090212

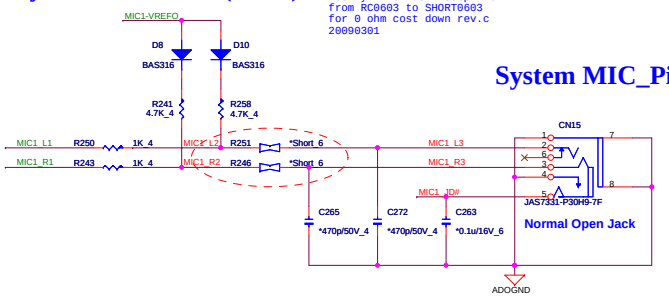


MUTE(AMP)

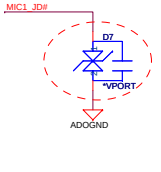


System MIC_Pink(AMP)

Modify R246 R251 footprint
from RC0603 to SHORT0603
for 0 ohm cost down rev.c
20090301

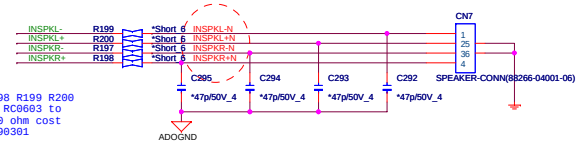


System MIC_Pink ESD(EMC)



Speaker(AMP)

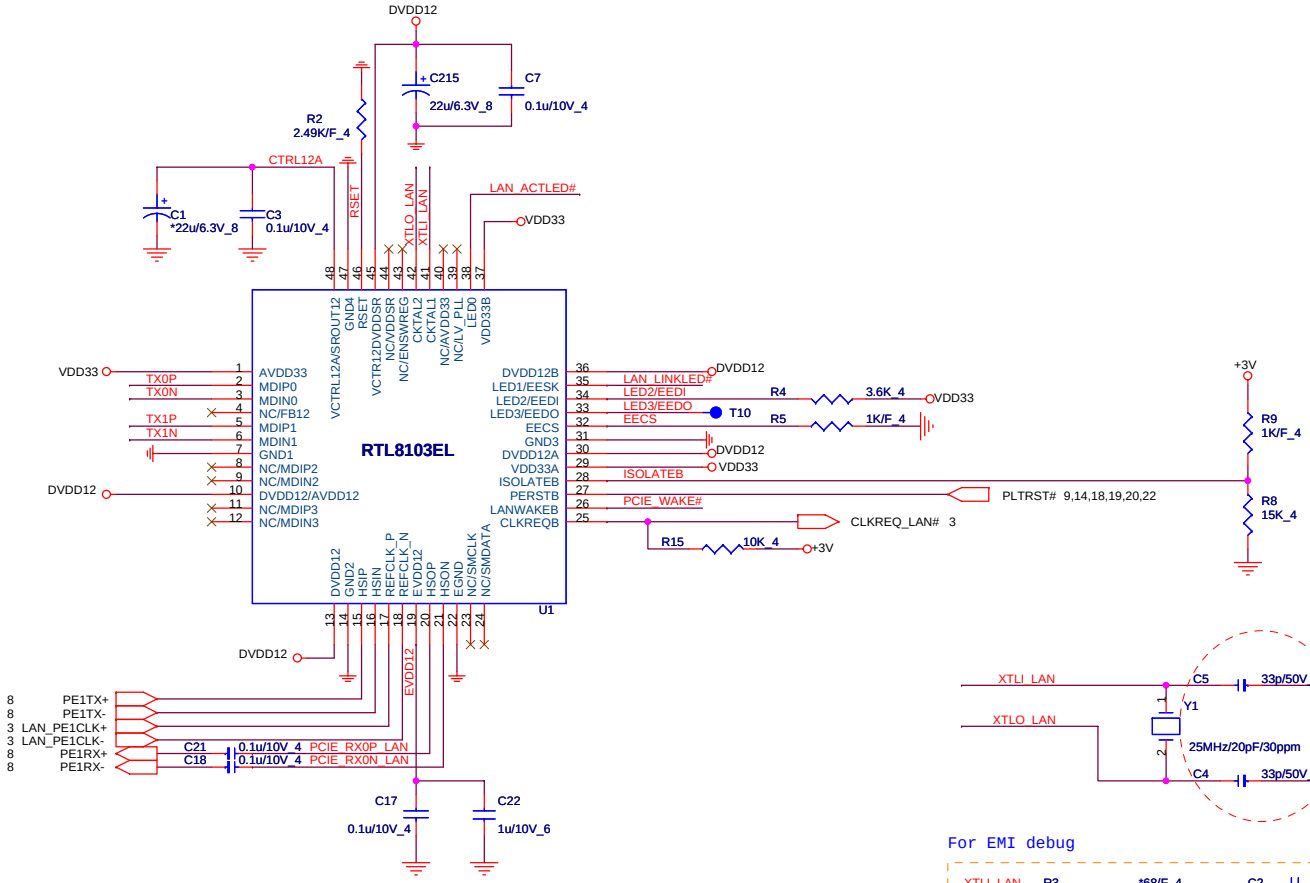
Modify SPK circuit 20090115

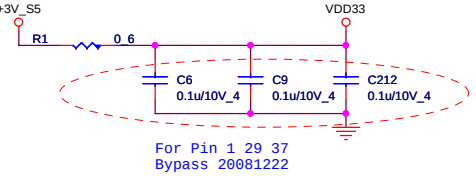


Modify R197 R198 R199 R200
footprint from RC0603 to
SHORT0603 for 0 ohm cost
down rev.c 20090301

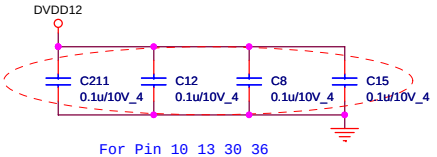
Quanta Computer Inc.		
PROJECT : ZA3		
Size	Document Number: AL272/AMP/MIC/LINE-OUT	Rev: 1A
Date: Sunday, March 08, 2009	Sheet 16 of 34	

LAN RTL8103EL (LAN)





For Pin 1 29 37
Bypass 20081222

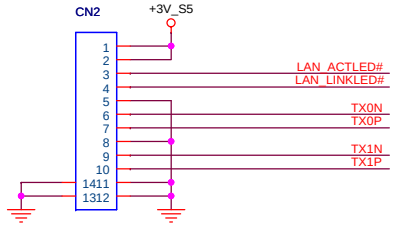


For Pin 10 13 30 36
Bypass 20081222

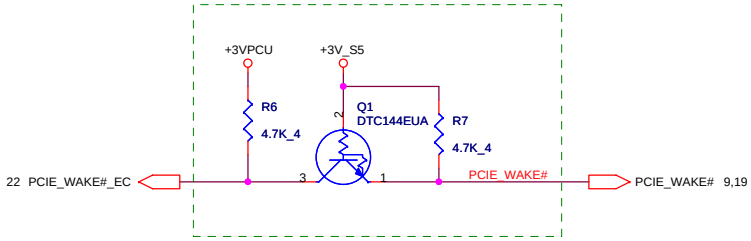
Change C4 C5 P/N from CH02706JB06 to CH03306JBD7 for vender suggest rev.b 20090212

For EMI debug

LAN D/B CONNECTER(LAN)



LAN CONN(88501-120N)



Quanta Computer Inc.		
PROJECT : ZA3		
Size	Document Number: LAN RTL8103EL	Rev: C
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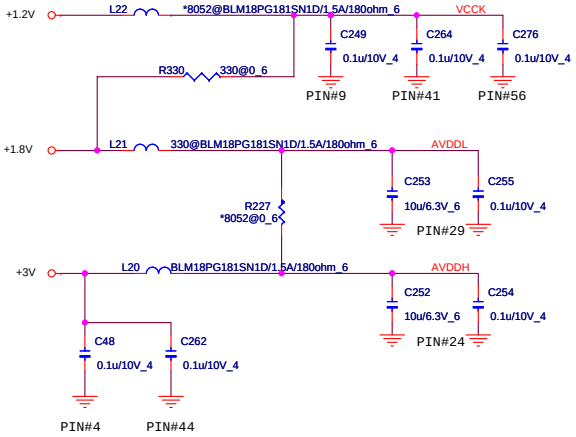
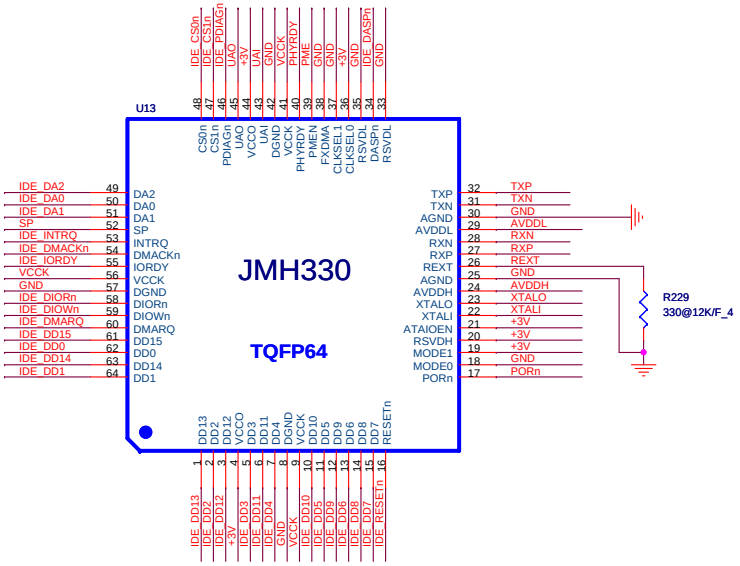
PATA TO SATA BRIDGE(HDD)

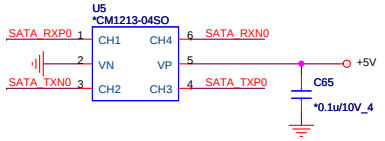
Bypass CAP must place close to power pins

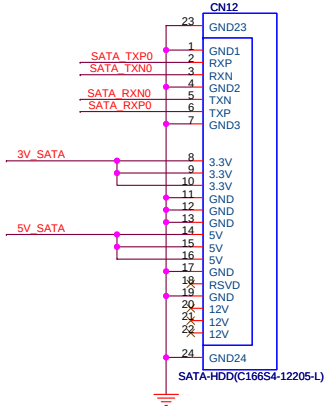




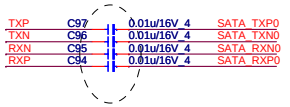
2.5" SATA HDD OR SSD(TOSHIBA)

SATA ESD(EMC)

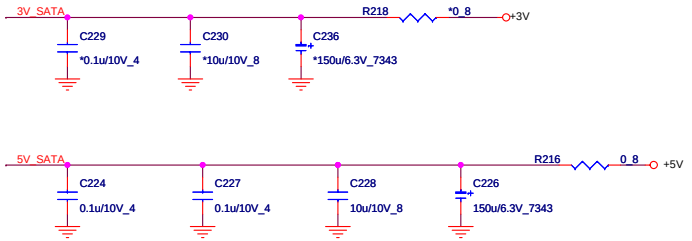




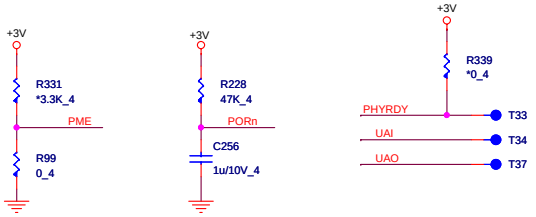
Close to SATA Connecter

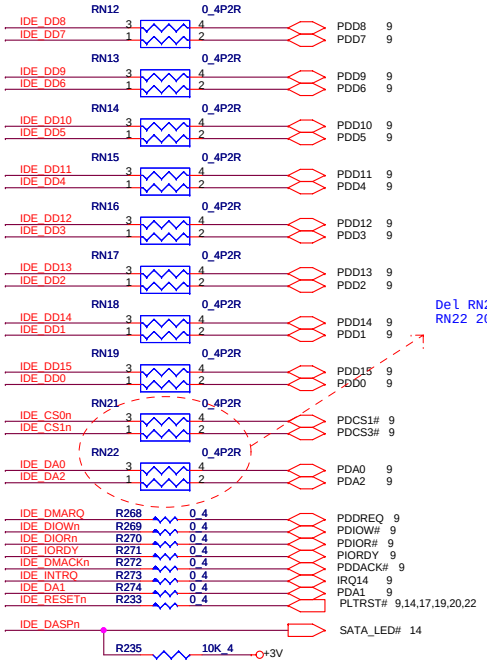


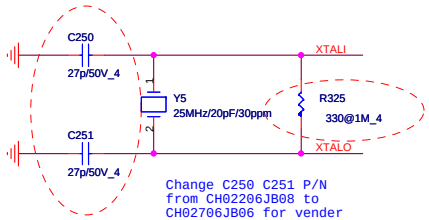
SATA POWER(HDD)



PME

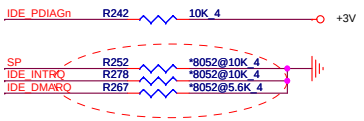






Add R325 for JMH330
XTAL issues 20090113

Change C250 C251 P/N
from CH02206JB08 to
CH02706JB06 for vender
suggest rev.b 20090212



Del RN20 and add RN21
RN22 20090113

	JMH330 (AJ003300H00)	88SA8052 (AJ080520H00)
Stuff	L21 R330 R325	L22 R227
No Stuff	L22 R227	L21 R330 R325
Change	R229 = 12K	R229 = 6.04K

For JMicron FAE Check : Can chenge RN20 R269 R270 R272 R274 from 82ohm to 0ohm, R268 R271 R273 from 22ohm to 0ohm, RN12 RN13 RN14 RN15 RN16 RN17 RN18 RN19 R233 from 33ohm to 0ohm 20081223

Quanta Computer Inc.
PROJECT : ZA3

Size	Document Number	Rev
	PATA TO SATA BRIDGE(88SA8052)	1A

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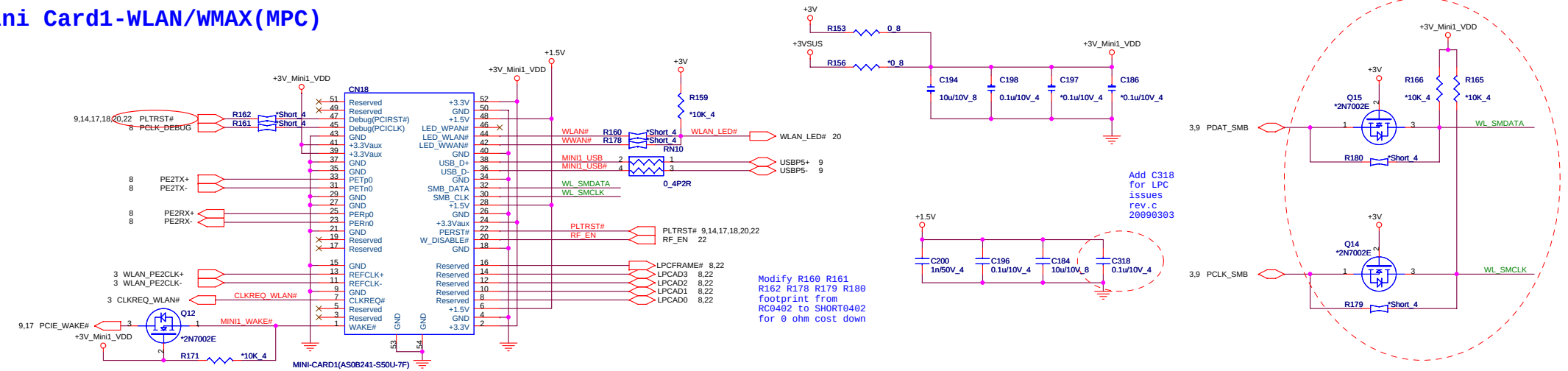
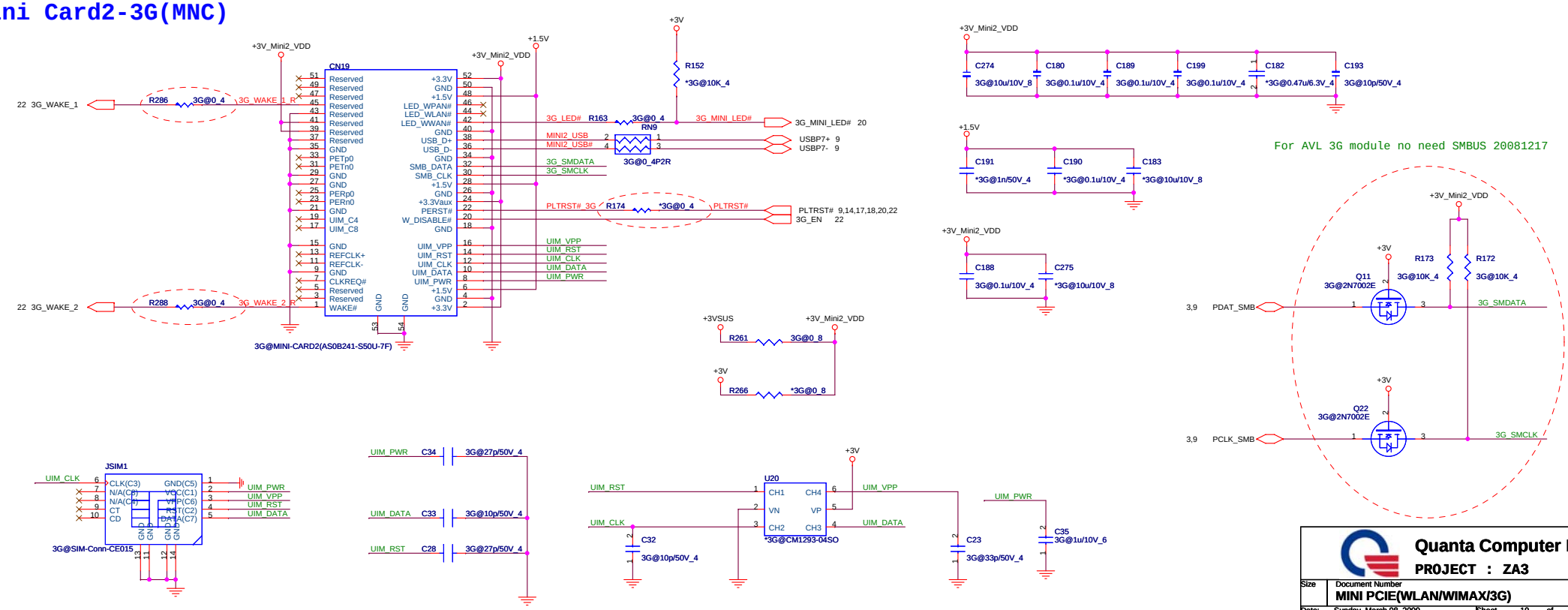
Mini Card1-WLAN/WMAX(MPC)

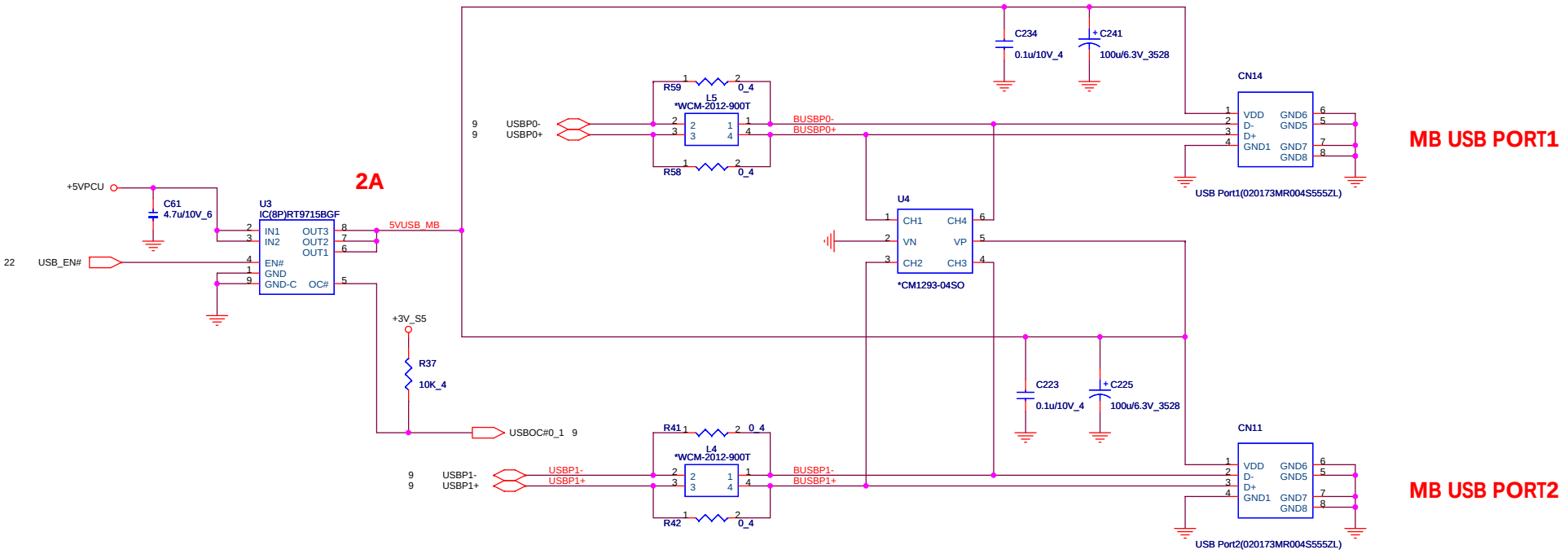


Mini Card2-3G(MNC)

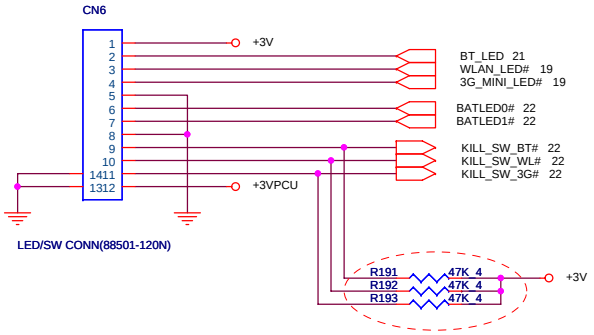


Quanta Computer Inc.	
PROJECT : ZA3	
Size	Document Number: MINI PCIE(WLAN/WIMAX/3G) — Rev 1A
Date: Sunday, March 08, 2009	Sheet 19 of 34

MB USB PORTS(USB)

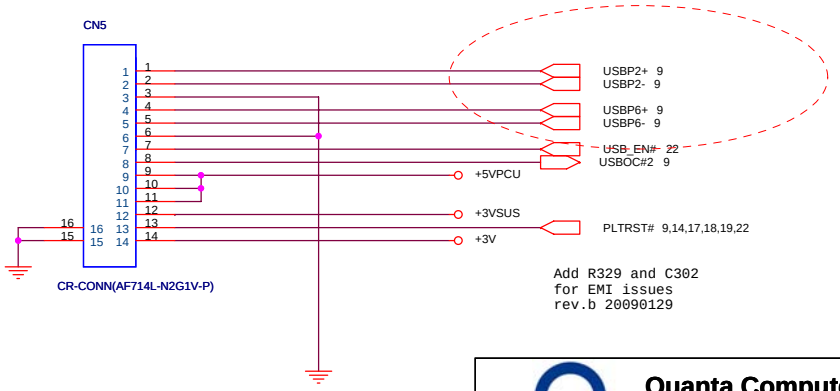


LED DB CONNECTER(UIF)



EC GPIO	Button
KILL_SW_WL#(GPIO57 PIN33)	WLAN Switch
KILL_SW_3G#(GPIO60 PIN34)	3G Switch
KILL_SW_BT#(GPIO12 PIN13)	BT Switch

Card Reader/USB DB CONNECTER(MMC)



Add R329 and C302
for EMI issues
rev.b 20090129

Quanta Computer Inc.
PROJECT : ZA3

Size	Document Number	Rev
	USB/SD_LED AND CR_USB DB	1A
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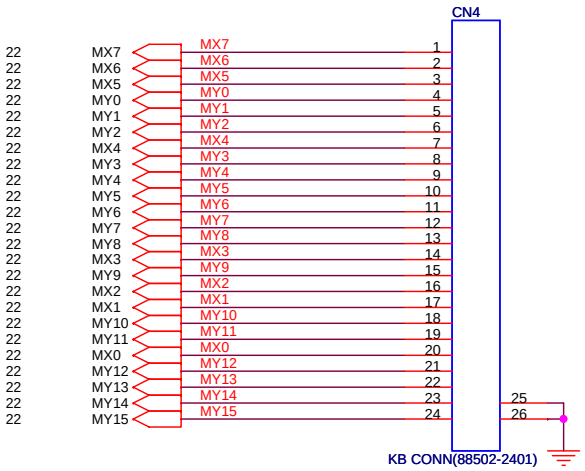
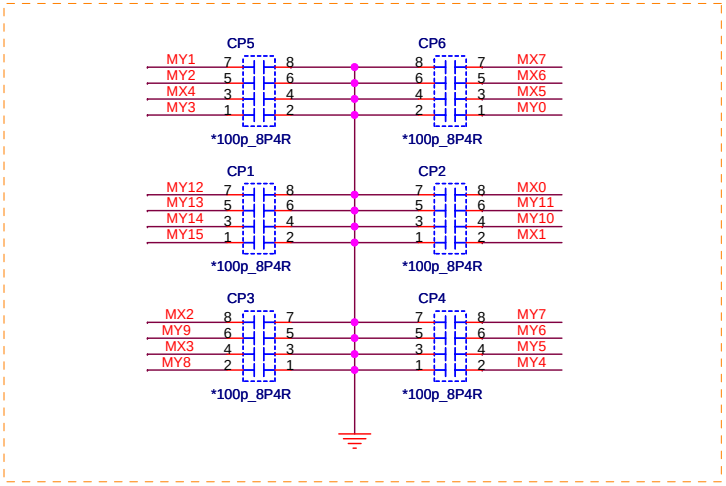
Keyboard(KBC)

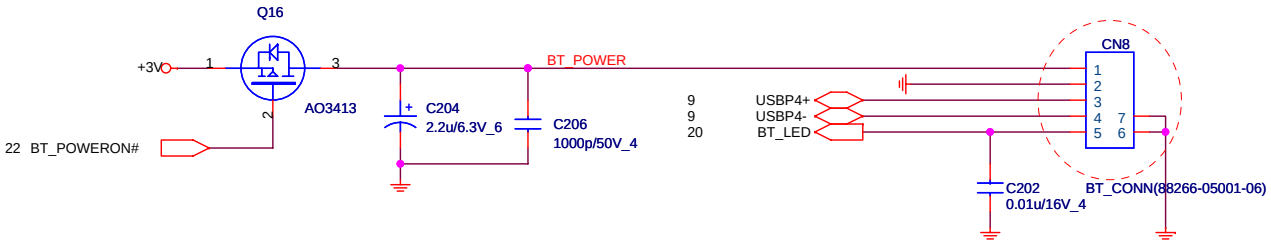


For EMI Reserve Caps for debug

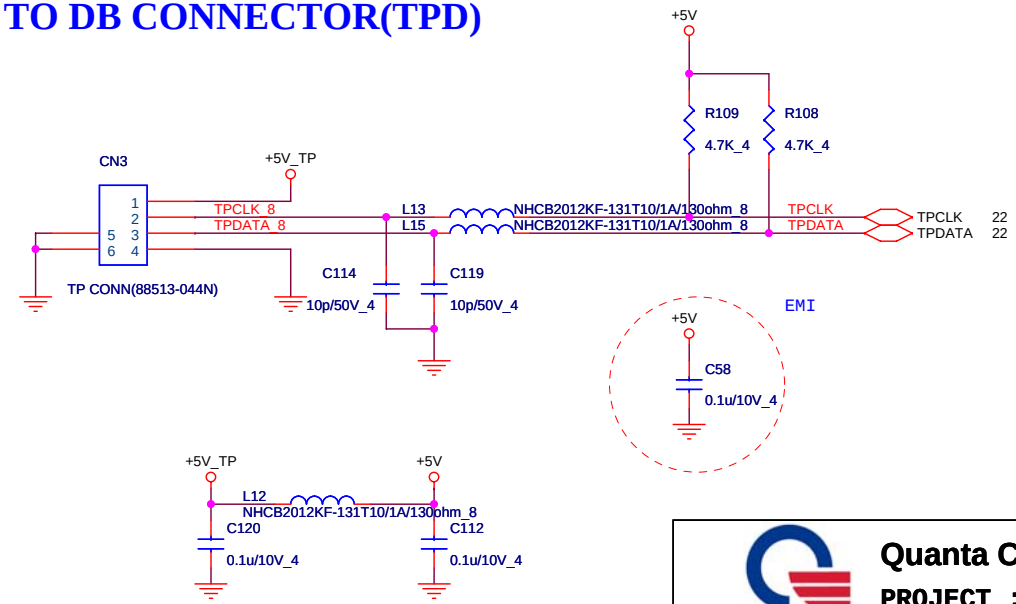


BT CONNECTER(BTM)

Modify CN8
footprint and
pin define rev.c
20090301



TO DB CONNECTOR(TPD)

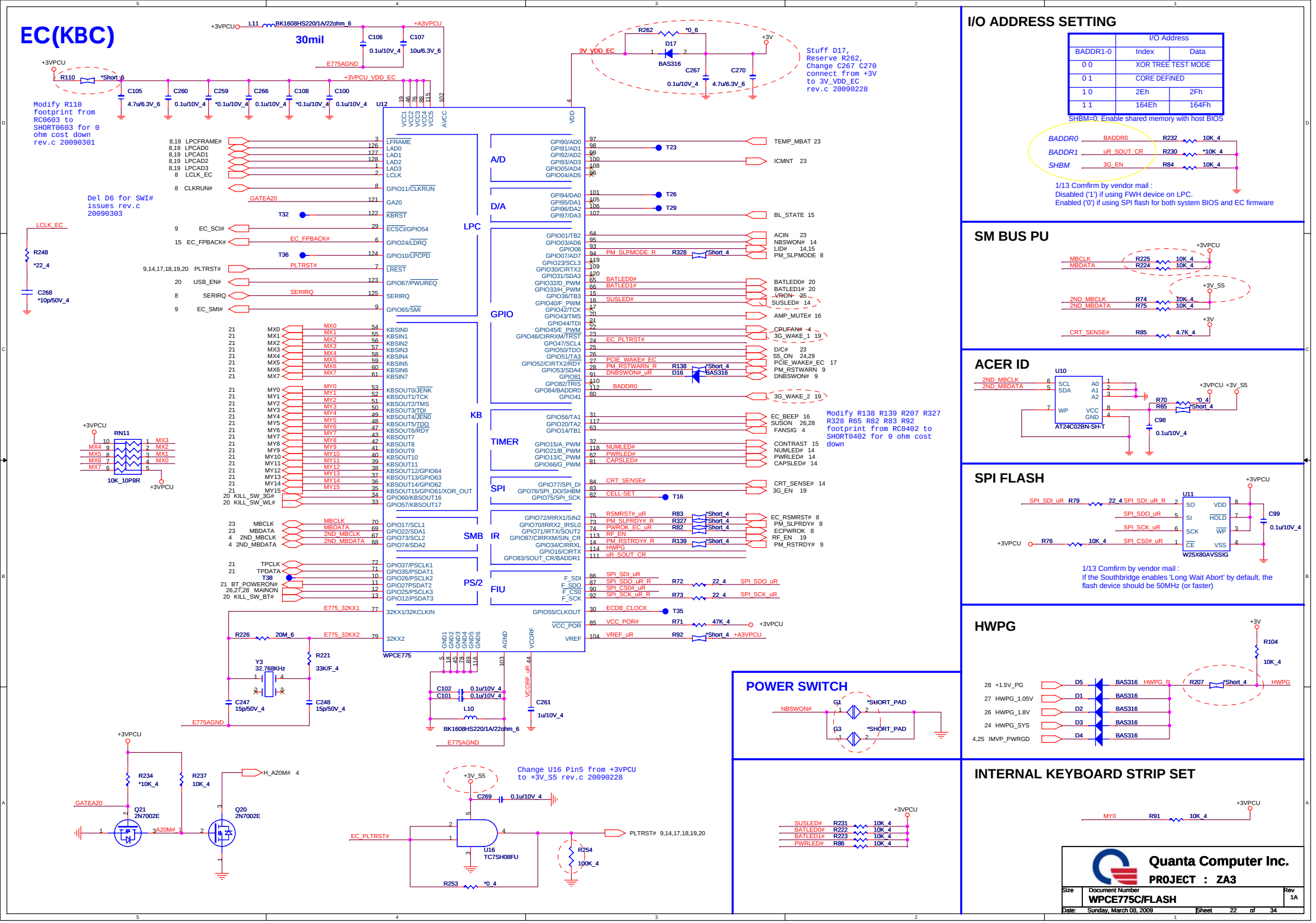


Quanta Computer Inc.

PROJECT : ZA3

Size	Document Number	Rev
	KB/BT/TP	1A
Date: Sunday, March 08, 2009	Sheet 21 of 34	

EC(KBC)



I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 — BADDR0 — R232 10K_4
BADDR1 — uR_SOUT_CR — R230 *10K_4
SHBM — 3G_EN — R84 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

MBCLK — R225 10K_4 — +3VPCU
MBDATA — R224 10K_4 — +3VPCU
2ND_MBCLK — R74 10K_4 — +3V_S5
2ND_MBDATA — R75 10K_4 — +3V_S5
CRT_SENSE# — R85 4.7K_4 — +3V

ACER ID

U10 AT24C02BN-SH-T
2ND_MBCLK, 2ND_MBDATA
R70 *0_4, R65 Short_4
C98 0.1u/10V_4

SPI FLASH

U11 W25X80AVSSIG
SPI_SDI_uR R79 22_4 SPI_SDI_uR_R
SPI_SDO_uR
SPI_SCK_uR
SPI_CS0#_uR R76 10K_4
C99 0.1u/10V_4

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG

28 +1.5V_PG — D5 BAS316 HWPG_R
27 HWPG_1.05V — D1 BAS316
26 HWPG_1.8V — D2 BAS316
24 HWPG_SYS — D3 BAS316
4,25 IMVP_PWRGD — D4 BAS316
R104 10K_4, R207 Short_4 → HWPG

POWER SWITCH

NBSWON# — G1 *SHORT_PAD, G3 *SHORT_PAD

INTERNAL KEYBOARD STRIP SET

MY0 — R91 10K_4 — +3VPCU

SUSLED# R231 10K_4
BATLED0# R222 10K_4
BATLED1# R223 10K_4
PWRLED# R86 10K_4
→ +3VPCU

Quanta Computer Inc.		
PROJECT : ZA3		
Size	Document Number: WPCE775C/FLASH	Rev: 1A
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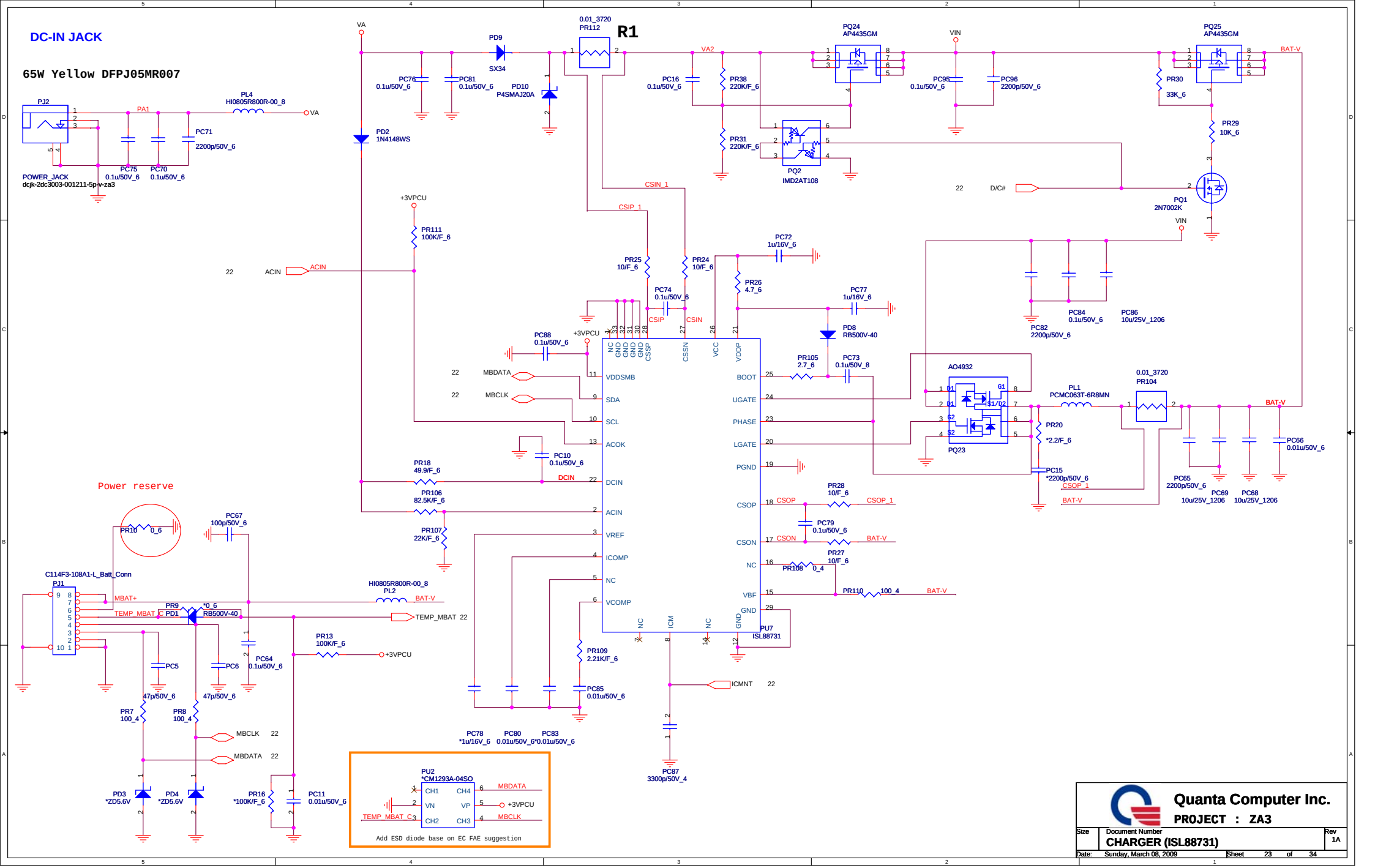
DC-IN JACK
65W Yellow DFPJ05MR007
R1
Power reserve
PJ2
POWER_JACK
dcjk-2dc3003-001211-5p-v-za3
PL4
HI0805R800R-00_8
PD2
1N4148WS
PD9
SX34
PD10
P4SMAJ20A
PQ2
IMD2AT108
PQ24
AP4435GM
PQ25
AP4435GM
PQ1
2N7002K
PQ23
AO4932
PD8
RB500V-40
PD1
RB500V-40
PD3
*ZD5.6V
PD4
*ZD5.6V
PU7
ISL88731
PU2
*CM1293A-04SO
Add ESD diode base on EC FAE suggestion
PJ1
C114F3-108A1-L_Batt_Conn
PL1
PCMC063T-6R8MN
VA
VIN
BAT-V
+3VPCU
ACIN
MBDATA
MBCLK
TEMP_MBAT
ICMNT
D/C#
CSIN_1
CSIP_1
CSOP_1
DCIN
MBAT+
PC76 0.1u/50V_6
PC81 0.1u/50V_6
PC16 0.1u/50V_6
PC95 0.1u/50V_6
PC96 2200p/50V_6
PC71 2200p/50V_6
PC75 0.1u/50V_6
PC70 0.1u/50V_6
PC72 1u/16V_6
PC74 0.1u/50V_6
PC77 1u/16V_6
PC88 0.1u/50V_6
PC84 0.1u/50V_6
PC86 10u/25V_1206
PC82 2200p/50V_6
PC73 0.1u/50V_8
PC10 0.1u/50V_6
PC79 0.1u/50V_6
PC64 0.1u/50V_6
PC67 100p/50V_6
PC5 47p/50V_6
PC6 47p/50V_6
PC11 0.01u/50V_6
PC78 *1u/16V_6
PC80 0.01u/50V_6*
PC83 *0.01u/50V_6
PC85 0.01u/50V_6
PC87 3300p/50V_4
PC65 2200p/50V_6
PC69 10u/25V_1206
PC68 10u/25V_1206
PC66 0.01u/50V_6
PC15 *2200p/50V_6
PR10 0_6
PR9 *0_6
PR13 100K/F_6
PR111 100K/F_6
PR18 49.9/F_6
PR106 82.5K/F_6
PR107 22K/F_6
PR109 2.21K/F_6
PR110 100_4
PR108 0_4
PR105 2.7_6
PR25 10/F_6
PR24 10/F_6
PR26 4.7_6
PR28 10/F_6
PR27 10/F_6
PR38 220K/F_6
PR31 220K/F_6
PR30 33K_6
PR29 10K_6
PR20 *2.2/F_6
PR7 100_4
PR8 100_4
PR16 *100K/F_6
0.01_3720 PR112
0.01_3720 PR104
HI0805R800R-00_8 PL2
NC
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
VBF
ICM
Quanta Computer Inc.
PROJECT : ZA3
CHARGER (ISL88731)
Sunday, March 08, 2009
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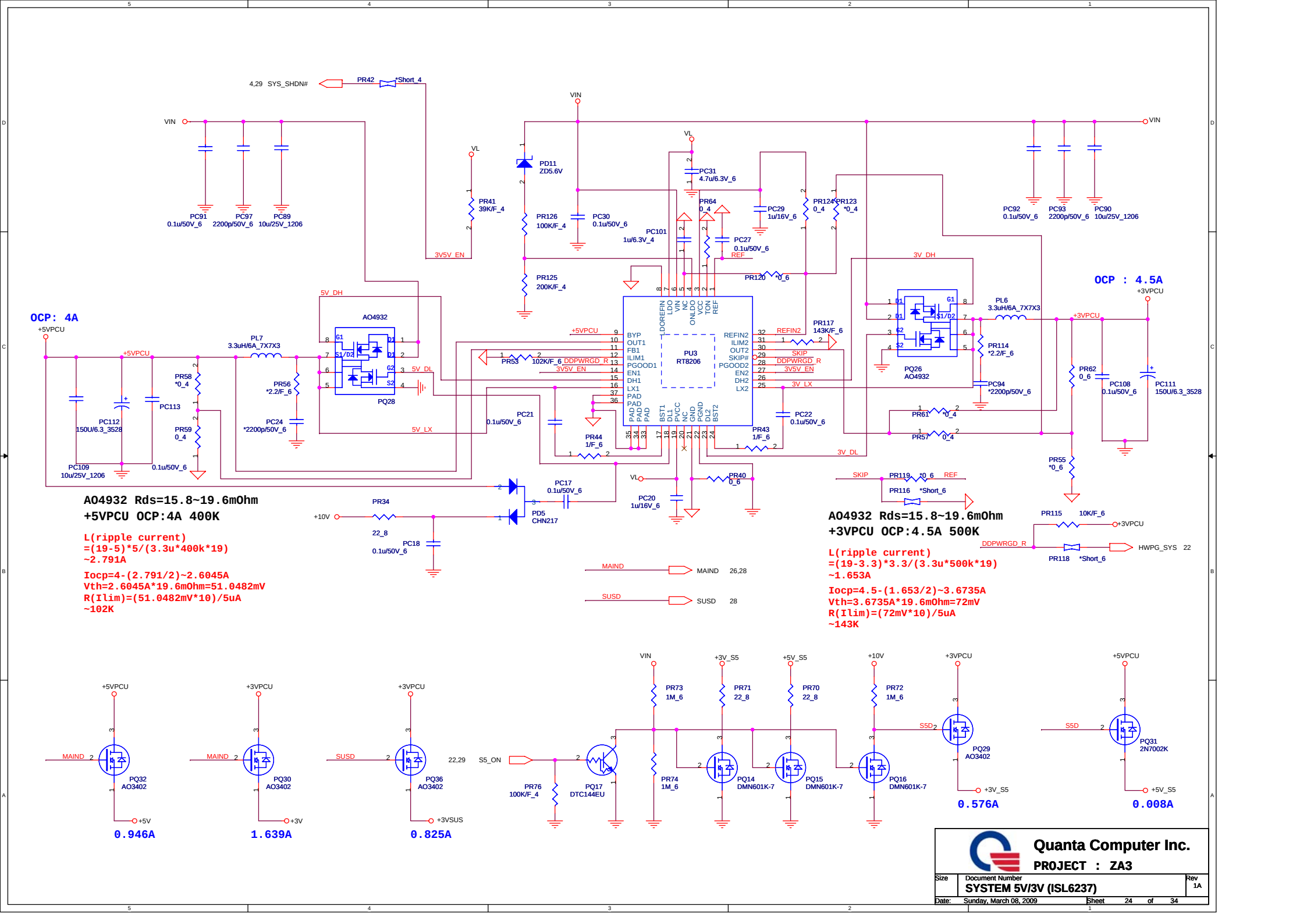
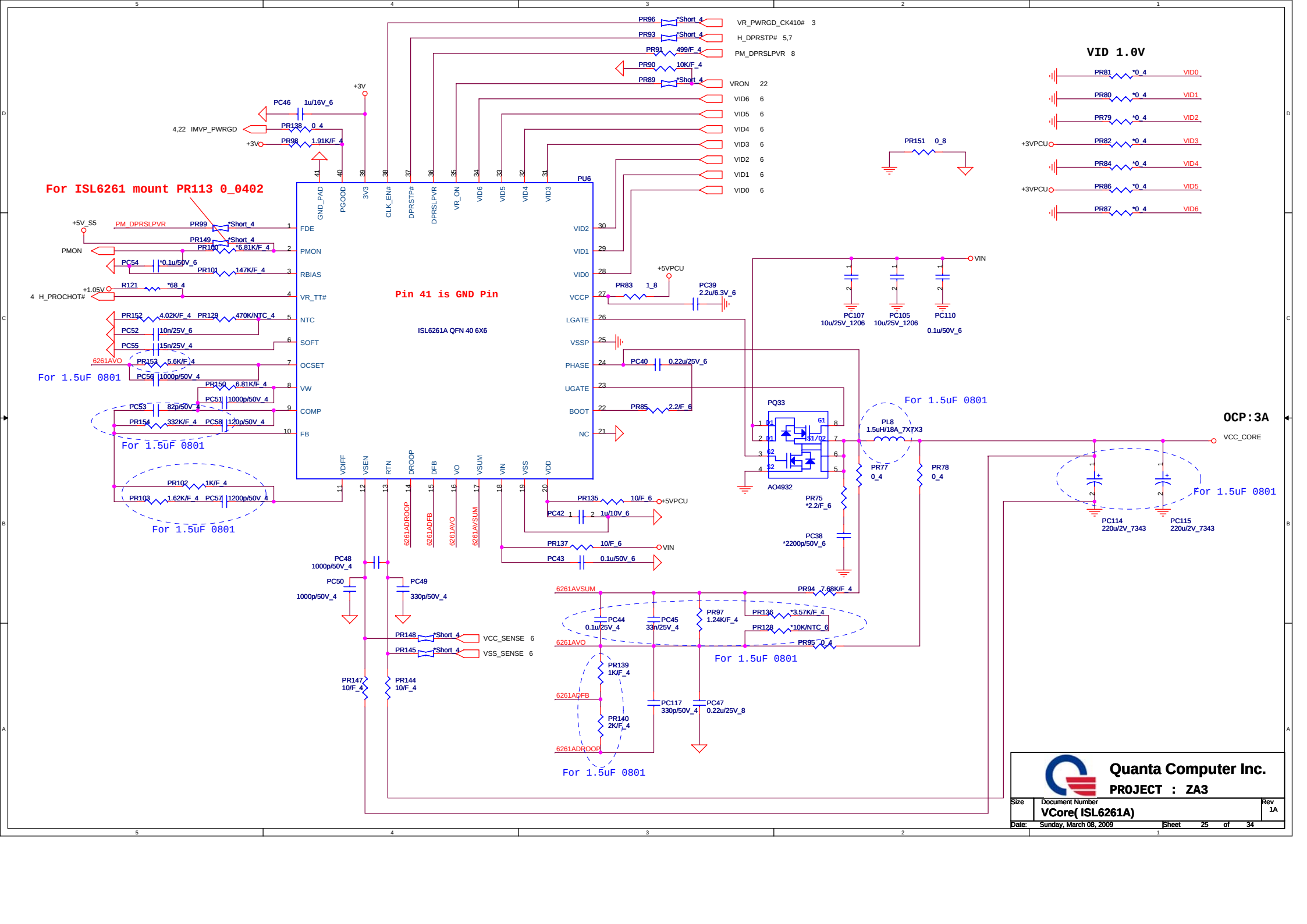
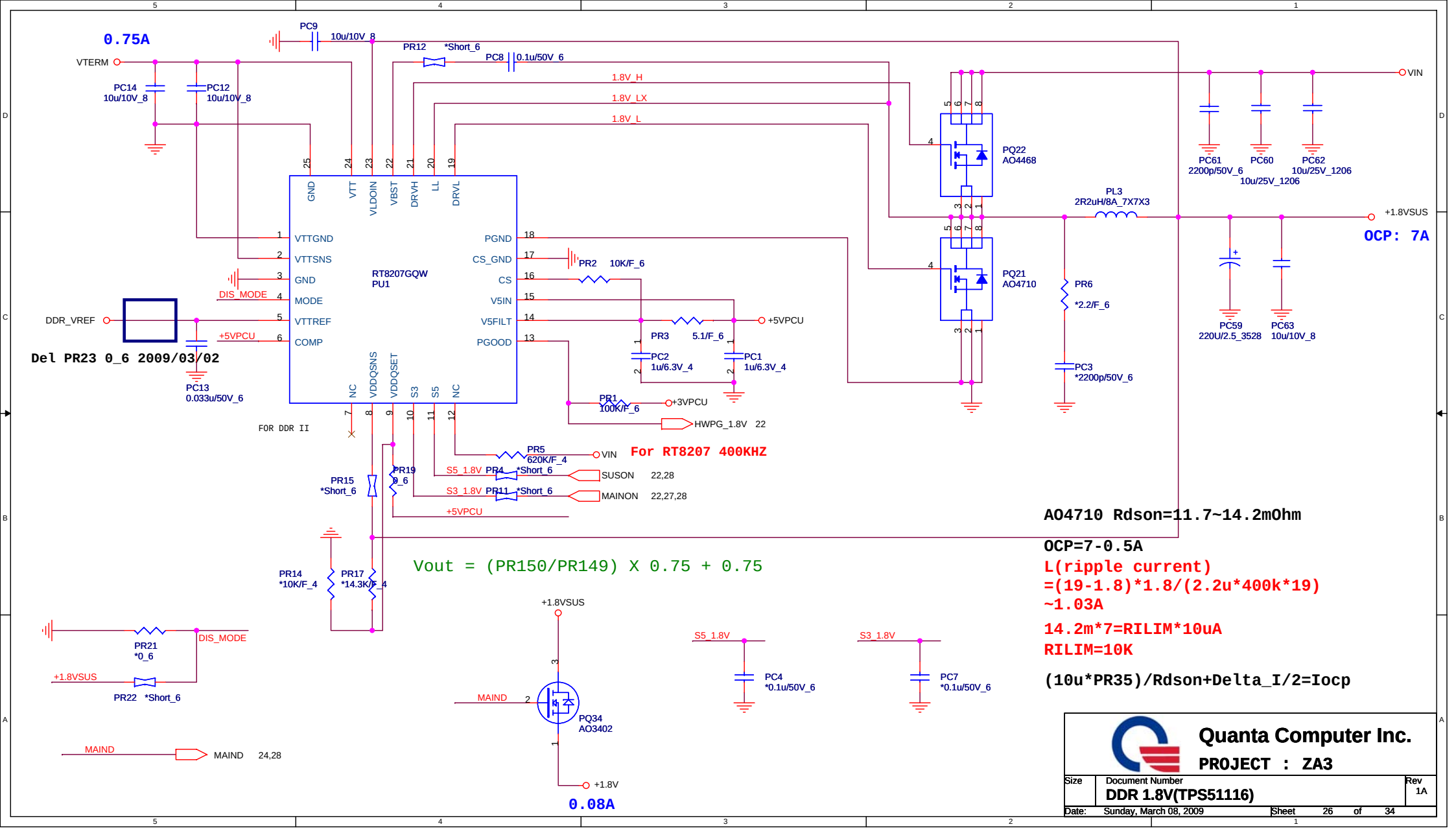
Rev 1A


OCP: 4A
AO4932 Rds=15.8~19.6mOhm
+5VPCU OCP:4A 400K
L(ripple current)
=(19-5)*5/(3.3u*400k*19)
~2.791A
Iocp=4-(2.791/2)~2.6045A
Vth=2.6045A*19.6mOhm=51.0482mV
R(Ilim)=(51.0482mV*10)/5uA
~102K
OCP : 4.5A
AO4932 Rds=15.8~19.6mOhm
+3VPCU OCP:4.5A 500K
L(ripple current)
=(19-3.3)*3.3/(3.3u*500k*19)
~1.653A
Iocp=4.5-(1.653/2)~3.6735A
Vth=3.6735A*19.6mOhm=72mV
R(Ilim)=(72mV*10)/5uA
~143K
0.946A
1.639A
0.825A
0.576A
0.008A
Quanta Computer Inc.
PROJECT : ZA3
SYSTEM 5V/3V (ISL6237)
Sunday, March 08, 2009


VID 1.0V
PR81 *0_4 VID0
PR80 *0_4 VID1
PR79 *0_4 VID2
+3VPCU PR82 *0_4 VID3
PR84 *0_4 VID4
+3VPCU PR86 *0_4 VID5
PR87 *0_4 VID6
PR96 *Short_4 VR_PWRGD_CK410# 3
PR93 *Short_4 H_DPRSTP# 5,7
PR91 499/F_4 PM_DPRSLPVR 8
PR90 10K/F_4
PR89 *Short_4 VRON 22
VID6 6
VID5 6
VID4 6
VID3 6
VID2 6
VID1 6
VID0 6
PR151 0_8
For ISL6261 mount PR113 0_0402
Pin 41 is GND Pin
ISL6261A QFN 40 6X6
PU6
GND_PAD PGOOD 3V3 CLK_EN# DPRSTP# DPRSLPVR VR_ON VID6 VID5 VID4 VID3
FDE PMON RBIAS VR_TT# NTC SOFT OCSET VW COMP FB
VID2 VID1 VID0 VCCP LGATE VSSP PHASE UGATE BOOT NC
VDIFF VSEN RTN DROOP DFB VO VSUM VIN VSS VDD
+3V PC46 1u/16V_6
4,22 IMVP_PWRGD PR138 0_4
+3V PR98 1.91K/F_4
+5V_S5 PM_DPRSLPVR PR99 *Short_4
PR149 *Short_4
PMON PR100 *6.81K/F_4
PC54 *0.1u/50V_6
PR101 147K/F_4
+1.05V R121 *68_4
4 H_PROCHOT#
PR152 4.02K/F_4 PR129 470K/NTC_4
PC52 10n/25V_6
PC55 15n/25V_4
6261AVO PR153 5.6K/F_4
PC56 1000p/50V_4
PR150 6.81K/F_4
PC51 1000p/50V_4
PC53 82p/50V_4
PR154 332K/F_4 PC58 120p/50V_4
For 1.5uF 0801
PR102 1K/F_4
PR103 1.62K/F_4 PC57 1200p/50V_4
For 1.5uF 0801
+5VPCU PR83 1_8
PC39 2.2u/6.3V_6
PC40 0.22u/25V_6
PR85 2.2/F_6
PR135 10/F_6 +5VPCU
PC42 1u/10V_6
PR137 10/F_6 VIN
PC43 0.1u/50V_6
6261ADROOP 6261ADFB 6261AVO 6261AVSUM
PC48 1000p/50V_4
PC50 1000p/50V_4
PC49 330p/50V_4
PR148 *Short_4 VCC_SENSE 6
PR145 *Short_4 VSS_SENSE 6
PR147 10/F_4
PR144 10/F_4
6261AVSUM PR94 7.68K/F_4
PC44 0.1u/25V_4
PC45 33n/25V_4
PR97 1.24K/F_4
PR136 *3.57K/F_4
PR128 *10K/NTC_6
6261AVO PR95 0_4
For 1.5uF 0801
PR139 1K/F_4
6261ADFB
PC117 330p/50V_4
PC47 0.22u/25V_8
PR140 2K/F_4
6261ADROOP
For 1.5uF 0801
VIN
PC107 10u/25V_1206
PC105 10u/25V_1206
PC110 0.1u/50V_6
PQ33
AO4932
For 1.5uF 0801
PL8 1.5uH/18A_7X7X3
PR77 0_4
PR78 0_4
PR75 *2.2/F_6
PC38 *2200p/50V_6
OCP:3A
VCC_CORE
PC114 220u/2V_7343
PC115 220u/2V_7343
For 1.5uF 0801
Quanta Computer Inc.
PROJECT : ZA3
Size
Document Number
VCore(ISL6261A)
Rev 1A
Date: Sunday, March 08, 2009
Sheet 25 of 34


0.75A
PC9
10u/10V_8
PR12
*Short_6
PC8
0.1u/50V_6
VTERM
PC14
10u/10V_8
PC12
10u/10V_8
1.8V_H
1.8V_LX
1.8V_L
VIN
PC61
2200p/50V_6
PC60
10u/25V_1206
PC62
10u/25V_1206
PQ22
AO4468
PL3
2R2uH/8A_7X7X3
+1.8VSUS
OCP: 7A
PQ21
AO4710
PR6
*2.2/F_6
PC59
220U/2.5_3528
PC63
10u/10V_8
PC3
*2200p/50V_6
GND
VTT
VLDOIN
VBST
DRVH
LL
DRVL
VTTGND
VTTSNS
GND
MODE
VTTREF
COMP
RT8207GQW
PU1
PGND
CS_GND
CS
V5IN
V5FILT
PGOOD
DIS_MODE
DDR_VREF
+5VPCU
PR2
10K/F_6
PR3
5.1/F_6
PC2
1u/6.3V_4
PC1
1u/6.3V_4
Del PR23 0_6 2009/03/02
PC13
0.033u/50V_6
NC
VDDQSNS
VDDQSET
S3
S5
NC
PR1
100K/F_6
+3VPCU
HWPG_1.8V 22
FOR DDR II
PR5
620K/F_4
VIN
For RT8207 400KHZ
PR15
*Short_6
PR19
0_6
S5_1.8V
PR4
*Short_6
SUSON 22,28
S3_1.8V
PR11
*Short_6
MAINON 22,27,28
+5VPCU
PR14
*10K/F_4
PR17
*14.3K/F_4
Vout = (PR150/PR149) X 0.75 + 0.75
AO4710 Rdson=11.7~14.2mOhm
OCP=7-0.5A
L(ripple current)
=(19-1.8)*1.8/(2.2u*400k*19)
~1.03A
14.2m*7=RILIM*10uA
RILIM=10K
(10u*PR35)/Rdson+Delta_I/2=Iocp
PR21
*0_6
DIS_MODE
+1.8VSUS
PR22
*Short_6
MAIND
MAIND 24,28
+1.8VSUS
MAIND
PQ34
AO3402
+1.8V
0.08A
S5_1.8V
PC4
*0.1u/50V_6
S3_1.8V
PC7
*0.1u/50V_6
Quanta Computer Inc.
PROJECT : ZA3
Size
Document Number
DDR 1.8V(TPS51116)
Rev
1A
Date: Sunday, March 08, 2009
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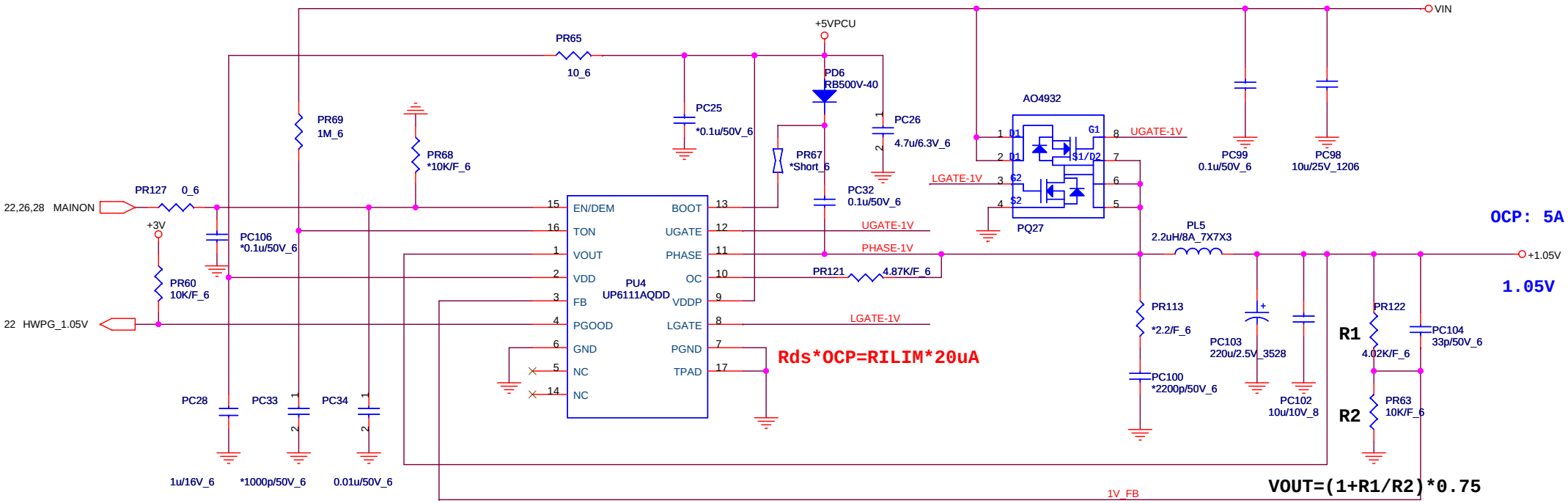


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4932 Rdson=15.8~19.6mOhm

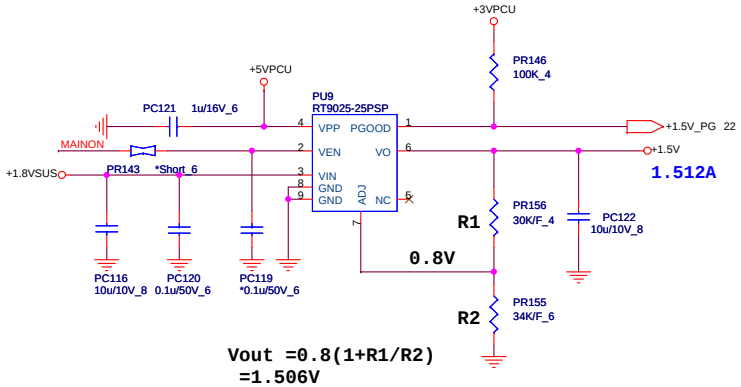
OCP=7.2-0.8A

L(ripple current)
=(19-1.05)*1.05/(3.3u*272k*19)
~1.105A

19.6m*5=RILIM*20uA

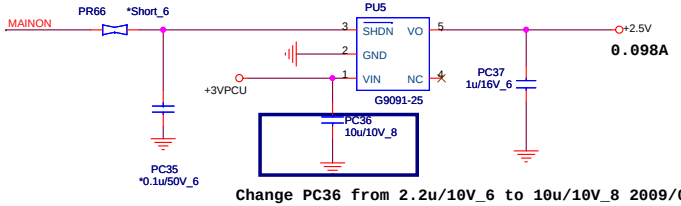
RILIM=4.9K(4.87K)

Quanta Computer Inc.		
PROJECT : ZA3		
Size	Document Number: VCCP 1.05V(UP6111AQDD)	Rev: 1A
Date: Sunday, March 08, 2009	Sheet 27 of 34	



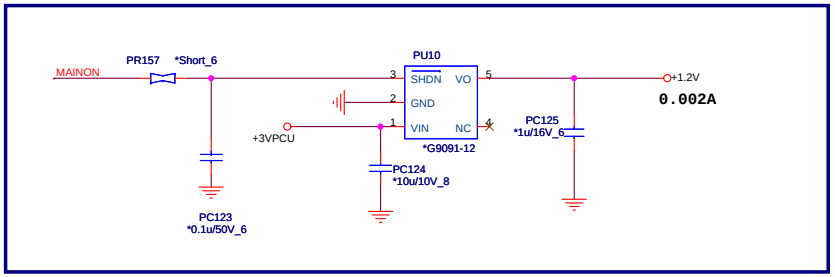
1.512A

Vout =0.8(1+R1/R2)
=1.506V



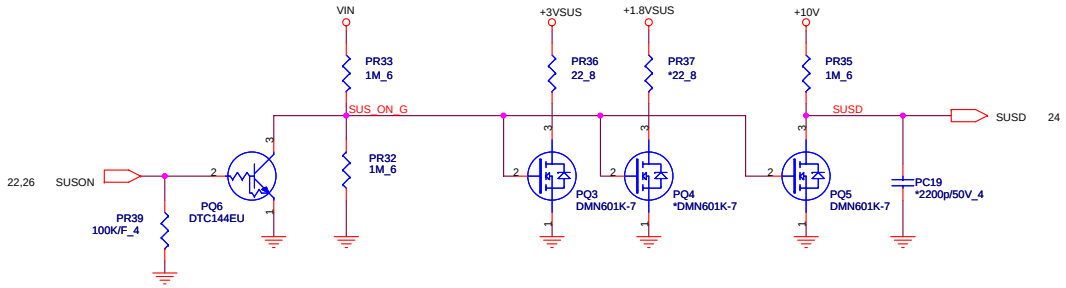
0.098A

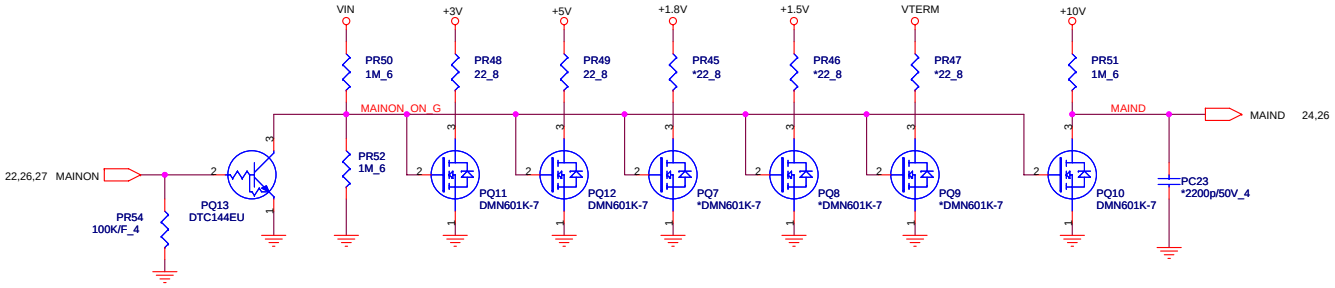
Change PC36 from 2.2u/10V_6 to 10u/10V_8 2009/03/02



0.002A

Addition +1.2v LDO 2009/03/02





Quanta Computer Inc.

PROJECT : ZA3

Size	Document Number	Rev
	Discharge/1.5/2.5V	1A

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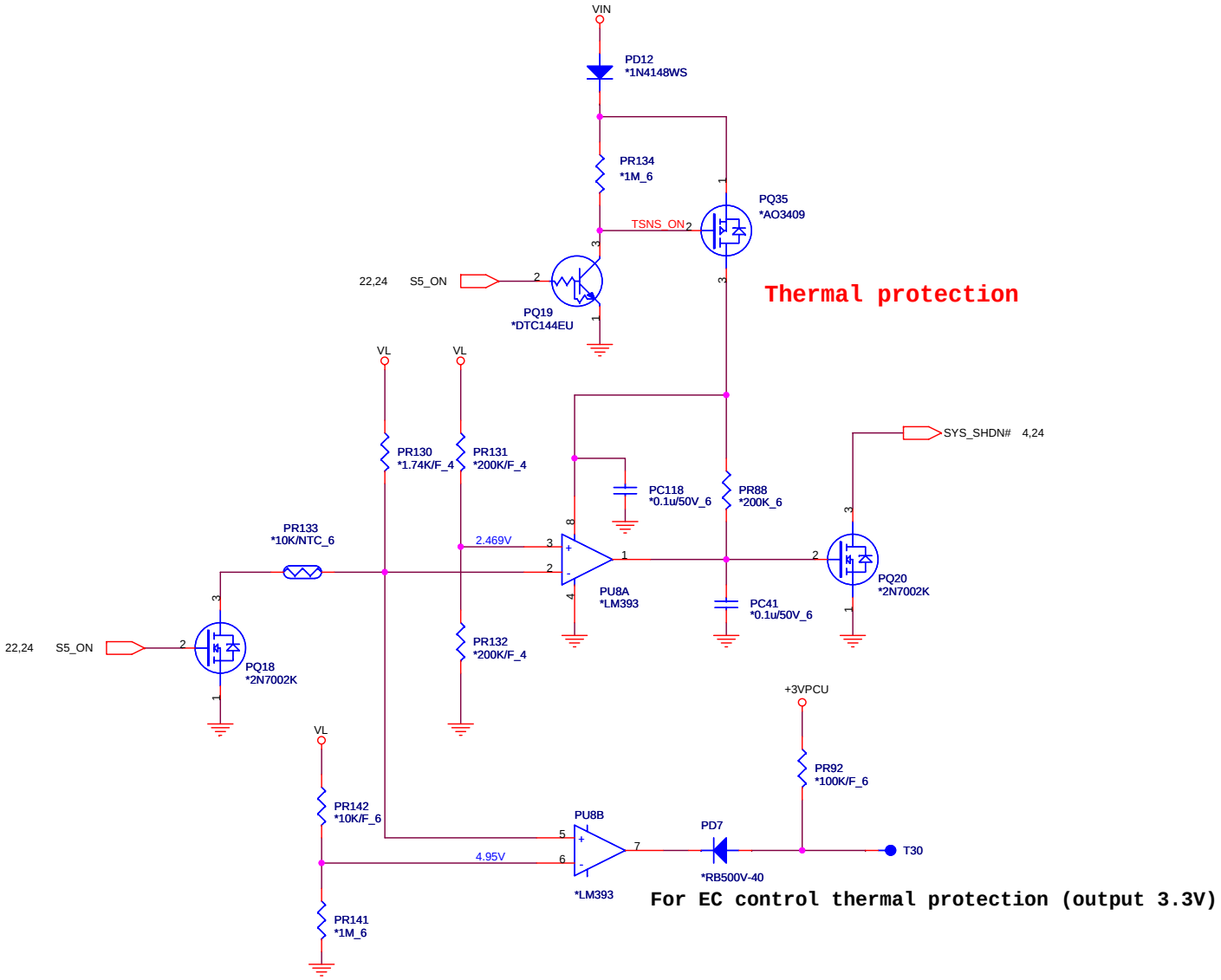

Quanta Computer Inc.

PROJECT : ZA3

Size	Document Number	Rev
	Thermal protect	1A

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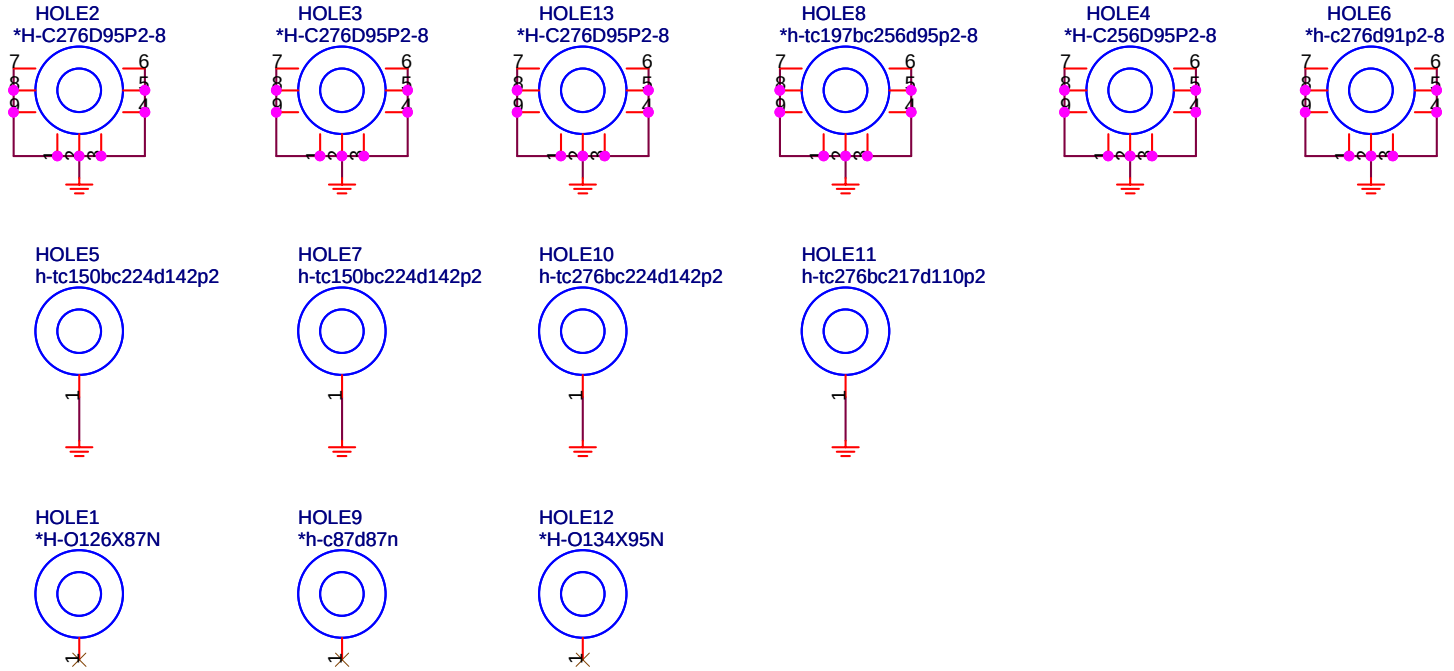
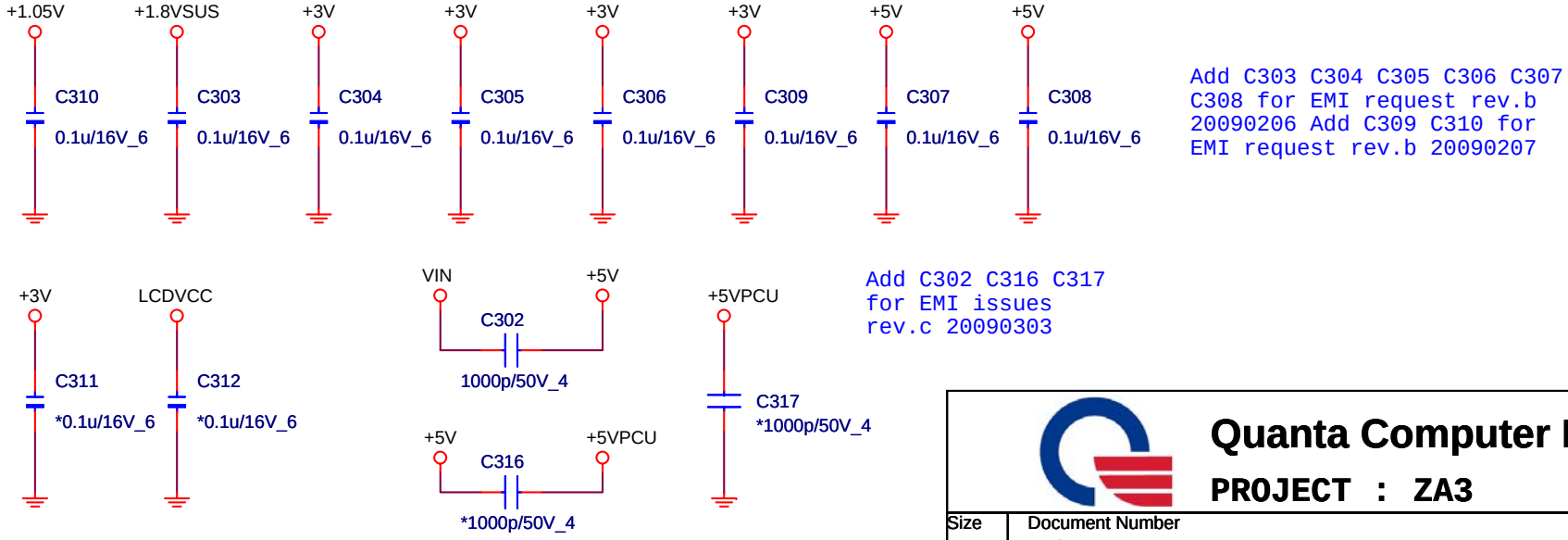
HOLES



EMI



Add C303 C304 C305 C306 C307 C308 for EMI request rev.b 20090206 Add C309 C310 for EMI request rev.b 20090207

Add C302 C316 C317 for EMI issues rev.c 20090303

Quanta Computer Inc.

PROJECT : ZA3

Size	Document Number	Rev
	HOLE	1A
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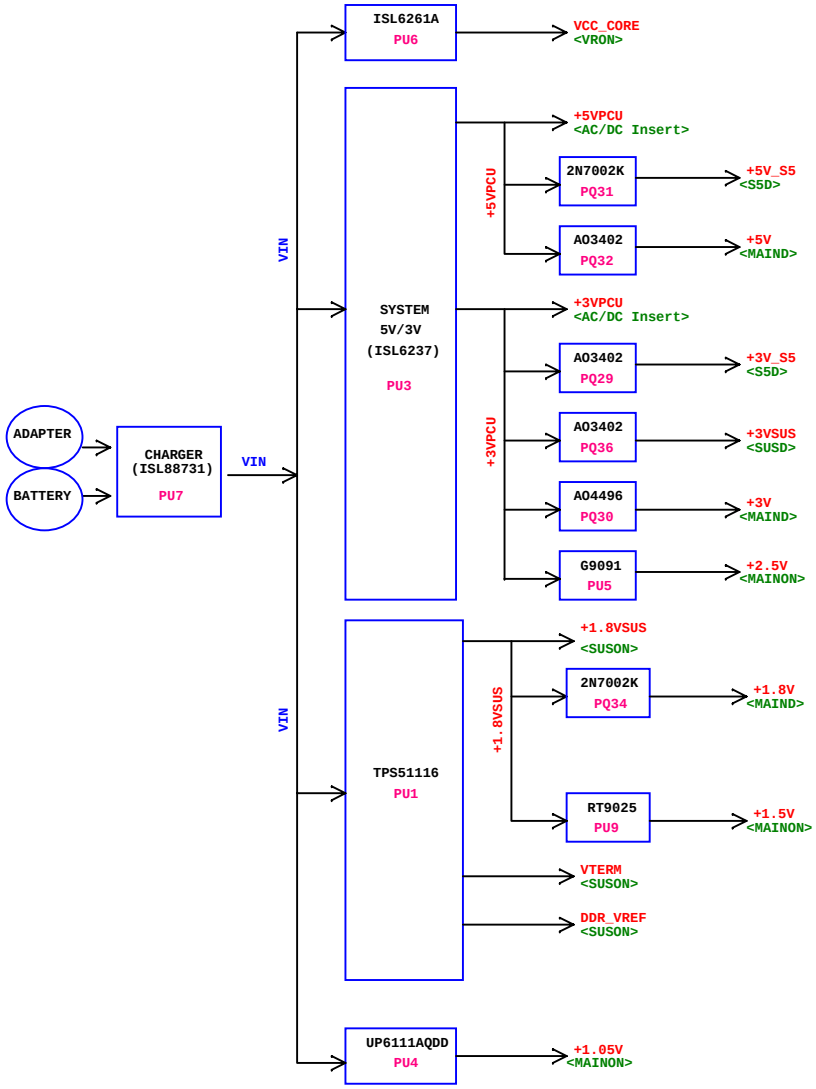
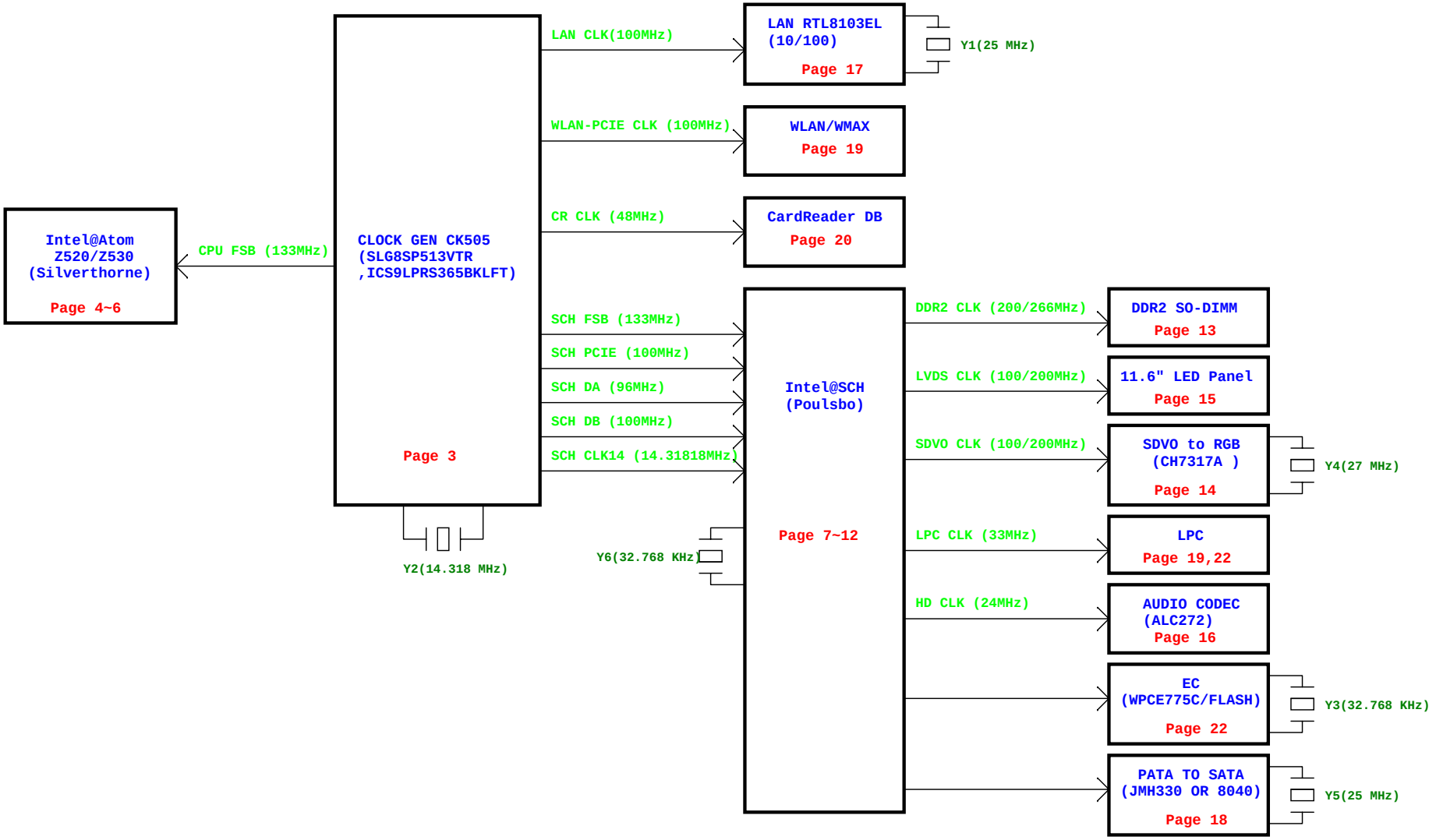


POWER	Distribution
VCC_CORE	CPU
+5VPCU	RTC, USB Connecter
+5V_S5	SCH Power
+5V	CPU C6-Power Circuit, SCH Power, CRT, LCD, CAMERA ,Audio Code, INT SPK AMP, SATA HDD,Touch Pad
+3VPCU	RTC, LED Power, HALL SENSOR, EC, ID , SPI Flash ,
+3V_S5	SCH USB Power, LAN, ID
+3VSUS	WLAN/WMAX, 3G
+3V	CLK_GEN Power, Thermal Sensor Power, CPU Pull Up Power, SCH Pull Up Power, SCH Power, DDRII Power, SDVO to CRT Power, LCD Power, INT SPK AMP, PATA To SATA Bridge, SATA, WLAN/WMAX, 3G, Card Reader, BT, EC,
+2.5V	SDVO to CRT
+1.8VSUS	SCH Power, DDRII SO-DIMM
+1.8V	PATA To SATA Bridge
+1.5V	CPU, SCH, WLAN/WMAX, 3G
VTERM	DDRII SO-DIMM
DDR_VREF	DDRII SO-DIMM
+1.05V	CLK_GEN, CPU, SCH,

Quanta Computer Inc.
PROJECT : ZA3
Size | Document Number: Power Tree | Rev: 1A
Date: Sunday, March 08, 2009 | Sheet 31 of 34



Quanta Computer Inc.

PROJECT : ZA3

Size	Document Number	Rev
	Clock Distribution Diagram	1A
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Model	REV	DATE	CHANGE LIST	NOTE
ZA3	A1A	20090107	PAGE16 : Reverse C301 R322 U19 R323 R324 for SPK AMP Power	ECN Release
		20090112	PAGE23 : Change PJ1 P/N and Footprint	
		20090113	PAGE18 : Del RN20 and add RN21 RN22 for HDD issues	
			PAGE18 : Add R325 for JMH330 XTAL issues	
			PAGE21 : Change CN4 P/N from DFFC24FR023 to DFFC24FR017	
			PAGE21 : Change CN4 footprint	
			PAGE20 : Change CN5 P/N from DFFC14FR080 to DFFC14FR047	
			PAGE20 : Change CN6 P/N from DFFC12FR293 to DFFC12FR019	
			PAGE17 : Change CN2 P/N from DFFC12FR293 to DFFC12FR019	
			PAGE20 : Change CN5 footprint from BL121-14R-TAND-14P-L-BU1 to af714l-n2g1x-14p-l	
			PAGE19 : Change ESD1 value to U20	
			PAGE16 : Change CN7 P/N from DFHS04FS969 to DFHD04MRA75	
			PAGE16 : Change CN7 footprint from 88460-0401-4p-l to 88266-040xx-xxx-4p-l	
			PAGE4 : Change CN7 P/N from DFHS04FS969 to DFHD04MRA75	
			PAGE4 : Change CN7 footprint from 88460-0401-4p-l to 88266-040xx-xxx-4p-r	
			PAGE21 : Change CN8 P/N from DFHS05FS000 to DFHD05MRD98	
			PAGE21 : Change CN8 footprint from 88460-0501-5P-L to 88266-0500x-5p-l	
			PAGE6 : Del Q10 R138R139 for modify +1.05V_C6_OFF circuit	
			PAGE6 : Change R168 P/N from CS41002FB28 to CS31002JB28 for modify +1.05V_C6_OFF circuit	
			PAGE6 : Add R326 for modify +1.05V_C6_OFF circuit	
			PAGE6 : Change R148 P/N from CS41002FB28 to CS33302JB16 for modify +1.05V_C6_OFF circuit	
			PAGE6 : Add Q26 for modify +1.05V_C6_OFF circuit	
		20090114	PAGE22 : Add R138 R139 R327 R328 for power sequence debug	
			PAGE5 : Add T54 T56 T57 T58 for power sequence debug	
			PAGE4 : Add T55 T59 for power sequence debug	
			PAGE14 : Change Y4 footprint from XTAL-3_2X2_5-2_3X1_9 to xtl-5x3_2-3_7 for cost down issues	
			PAGE14 : Change Y4 P/N from BG627000011 to BG627000505 for cost down issues	
			PAGE17 : Change U1 P/N from AL08103EB00 to AL008103B00	
		20090115	PAGE15 : Change CN1 footprint from MSC-RB30-5-FG-30P-L to msc-rb30-5-fg-30p-l-za3 for ZA3 A-test SMT issues	
			PAGE19 : Change JSIM1 footprint from SIM-CE01X-3-14P to sim-ce01x-3-14p-za3 for ZA3 A-test SMT issues	
			PAGE19 : Change CN18 footprint from mipcie-88956-5204-52p-ruv-v to mipcie-88956-5204-52p-ruv-v-za3 for ZA3 A-test SMT issues	
			PAGE19 : Change CN19 footprint from mipcie-88956-5204-52p-ruv-v to mipcie-88956-5204-52p-ruv-v-za3 for ZA3 A-test SMT issues	
			PAGE20 : Change CN11 footprint from usb-020173mr004s555zl-4p-r-v to usb-020173mr004s555-4p-r-v-za3 for ZA3 A-test SMT issues	
			PAGE20 : Change CN14 footprint from usb-020173mr004s555zl-4p-r-v to usb-020173mr004s555-4p-r-v-za3 for ZA3 A-test SMT issues	
			PAGE23 : Change PJ2 footprint from dcjk-2dc3003-001211-5p to dcjk-2dc3003-001211-5p-v-za3 for ZA3 A-test SMT issues	
			PAGE23 : Change PR104 footprint from RC3720 to rc3720-0_8h for ZA3 A-test SMT issues	
			PAGE23 : Change PR112 footprint from RC3720 to rc3720-0_8h for ZA3 A-test SMT issues	
			PAGE14 : Change U9 footprint from QFN64-8X8-4-65P-0_85H to qfn64-8X8-4-65p-0_85h-za3 for ZA3 A-test SMT issues	
			PAGE23 : Change PU7 footprint from QFN28-5X5-5-33P to qfn28-5x5-5-33p-za3 for ZA3 A-test SMT issues	
			PAGE22 : Change U12 footprint from LQFP128-16X16-4 to lqfp128-16x16-4-za3 for ZA3 A-test SMT issues	
			PAGE23 : Change PJ1 footprint from bat-c144f8-108a1-l-8p-l-v-zg8 to bat-c144f8-108a1-l-8p-l-v-za3 for ZA3 A-test SMT issues	
			PAGE30 : Change HOLE8 HOLE9 HOLE10 footprint	
			PAGE16 : Modify SPK circuit	
		20090116	PAGE21 : Add CN8 PIN6 PIN7 to GND	
			PAGE30 : Modify HOLE8 HOLE9 HOLE10 symbol	
			PAGE21 : Change CN3 footprint from BL123-04R-4P-R-BL5 to 88513-0401-4p-r	
			PAGE21 : Change CN3 P/N	
		20090117	PAGE16 : Change CN7 P/N from DFHS04FS969 to DFHD04MRA75	
			PAGE4 : Change CN9 P/N from DFHS04FS969 to DFHD04MRA75	
		20090119	PAGE23 : stuff PR10 for Battery issues	
		20090121	PAGE22 : Modify SUSLED# from GPIO30 to GPIO40	
			PAGE27 : Change PL5 P/N from DC-33D5M000 to DC-2280M002	
		20090129	PAGE15 : Change C209 P/N from CH62202Z233 to CH52202MA91	
			PAGE15 : Change C209 footprint from CC1206 to CC0805	
			PAGE19 : Change CN18 P/N from DG052000031 to DFHS52FR025 for cost issues	
			PAGE19 : Change CN19 P/N from DG052000031 to DFHS52FR025 for cost issues	
			PAGE20 : Add R329 and C302 for EMI 48MHz issues	
			PAGE19 : Change C182 P/N from CH44702K912 to CH4472K9B00	
		20090205	PAGE8 : Add T60 T61 T62 T63 test point for Boundary Scan	
			PAGE4 : Modify JETC pins for Boundary Scan	
			PAGE9 : Modify JETC pins for Boundary Scan	
			PAGE16 : Modify CN7 pin5 pin6 for ESD issues	
			PAGE14 : Change CN10 P/N form DFWF20MS000 to DFWF20MS002	
			PAGE14 : Change CN10 footprint form 88442-2001-20p-luv to 87242-2001-20p-luv	
			PAGE8 : No stuff C160 for C6 issues	
		20090206	PAGE15: Add R255 for EMI request	

Quanta Computer Inc.
PROJECT : ZA3

Size	Document Number	Rev
	Change List01	1A

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Model	REV	DATE	CHANGE LIST	NOTE
ZA3	B1A	20090206	PAGE16 : Reverse C301 R322 U19 R323 R324 for SPK AMP Power	ECN Release
			PAGE30 : Add C303 C304 C305 C306 C307 C308 for EMI Request	
		20090207	PAGE15 : No stuff R208 for EC not use BL_STATE rev.b 20090207	
			PAGE30 : C309 C310 for EMI Request	
			PAGE4 : Change R98 R87 R97 P/N from CS05102FB09 to CS05602JB17 rev.b 20090207	
			PAGE9 : Change R260 R259 R256 P/N from CS05102FB09 to CS05602JB17	
			PAGE9 : Change R257 P/N from CS02702JB21 to CS05602JB17 rev.b 20090207	
		20090209	PAGE8 : Change T60 T61 T62 T63 footprint from TP3075 to TP3050	
			PAGE8 : Modify HOLE10 HOLE5 HOLE7 footprint	
			PAGE15 : Change U8 P/N from AL005243000 to AL005243001	
		20090210	PAGE16 : Change R181 R176 P/N from CS07502FB17 to CS05102JB35	
			PAGE7 ~ PAGE12 : Change U15 P/N from AJSLGFQ0T02 to AJ0QV230T01	
		20090211	PAGE30 : C311 C312 for EMI Request	
			PAGE30 : Modify CN10 P/N and footprint for EMI request	
		20090212	PAGE16 : Change R204, R187, R313, R304 P/N from CS32003F933 to CS33603F911	
			PAGE17 : Change C4 C5 P/N from CH02706JB06 to CH03306JBD7 for vender suggest	
			PAGE3 : Change C42 C43 P/N from CH02706JB06 to CH03306JBD7 for vender suggest	
			PAGE18 : Change C250 C251 P/N from CH02206JB08 to CH02706JB06 for vender suggest	
		20090213	PAGE16 : Change R164 P/N from CS21002JB34 to CS22002JB02 for Ben check	
			PAGE16 : Change R167 P/N from CS00002JB38 to CS33602JB17 for Ben check	
	C1A	20090213	PAGE11 : Change C163 C136 connect SCH_VCCSUS3 power net	
		20090228	PAGE22 : Change U16 Pin5 from +3VPCU to +3V_S5	
			PAGE22 : Stuff D17, Reserve R262, Change C267 C270 connect from 3V_VDD_EC to +3V	
			PAGE6 : Modify R326 from 10K to 100K and pull up +3V and Change R168 from 10K to 100K	
		20090301	PAGE21 : Modify CN8 footprint and pin define	
			PAGE18 : Modify 8040 circuit to 88SA8052 add L22 R330 R331 R99 R339	
			PAGE4 : Modify R150 from CPU side to SCH side	
			PAGE4 : Change R88 P/N from CS05602JB17 to CS11202JB21	
			PAGE4 : Change R81 P/N from CS00002JB38 to CS02402JB11	
			PAGE6 : Change R100 R101 P/N from CS11002FB22 to CS11002JB32	
			PAGE13 : Add R112 R332 of RAM RST issues for intel suggest	
			PAGE15 : Change R215 P/N from CS41002JB20 to CS41002FB28	
			PAGE8 : Add R333 R334 R335 R336 for LPC AD0~AD3	
			PAGE8 : Change C233 C231 C243 C240 C239 C238 C237 C235 from SDVO chip side to SCH side	
			PAGE3 : Change R43 P/N from CS00002JB38 to CS31002JB28	
			PAGE9 : Change R186 R184 R309 R296 P/N from CS31002JB28 to CS21002JB34	
			PAGE9 : Del RN8 and Add R337 R338 to SCH SMBUS	
			PAGE15 : Modify R210 R23 footprint from RC0402 to SHORT0402 for 0 ohm cost down	
			PAGE16 : Modify R275 footprint from RC0402 to SHORT0402 for 0 ohm cost down	
			PAGE22 : Modify R138 R139 R207 R327 R328 R65 R82 R83 R92 footprint from RC0402 to SHORT0402 for 0 ohm cost down	
			PAGE10 : Modify R111 footprint from RC0402 to SHORT0402 for 0 ohm cost down	
			PAGE19 : Modify R160 R161 R162 R178 R179 R180 footprint from RC0402 to SHORT0402 for 0 ohm cost down	
			PAGE3 : Modify R39 R36 footprint from RC0402 to SHORT0402 for 0 ohm cost down	
			PAGE22 : Modify R110 footprint from RC0603 to SHORT0603 for 0 ohm cost down	
			PAGE11 : Modify R126 footprint from RC0603 to SHORT0603 for 0 ohm cost down	
			PAGE16 : Modify R144 R149 R170 R183 R246 R251 R197 R198 R199 R200 footprint from RC0603 to SHORT0603 for 0 ohm cost down	
		20090302	PAGE16 : Modify R168 P/N from CS31002JB28 to CS41002JB20	
			PAGE23 : Modify PJ1 footprint from bat-c144f8-108a1-l-8p-l-v-za3 to bat-c144f8-108a1-l-8p-l-v for SMT issues	
			PAGE14 : Add C313 C314 C315 for EMI issues	
		20090303	PAGE16 : Add R340 for EC PCBEEP	
			PAGE3 : Del R27 for CR DB +3VSUS issues	
			PAGE20 : Del R329 C302 for CR DB +3VSUS issues and modify CN5 pin12 to +3VSUS	
			PAGE6 : Add and revrse Q27 R329 for C6 circuit	
			PAGE19 : Add C318 for LPC issues	
			PAGE30 : Add C302 C316 C317 for EMI issues	
			PAGE13 : Del RN4 and Add R341 R342 for RAM issues	
			PAGE9 : Stuff R297 for SMI#	
			PAGE9 : No stuff R239 for SWI#	
			PAGE22 : Del D6 for SWI# issues	
		20090304	PAGE9 : Change R297 from +3V_S5 to +3V for SMI#	
			PAGE22 : Del SWI# net and Add test point T36	
			PAGE19 : No stuff C182 and change P/N from CH4472K9B00 to CH4471Z3B07	
		20090305	PAGE16 : Change U18 P/N from AL001453000 to AL001454001	
			PAGE19 : Change CN18 CN19 P/N from DFHS52FR025 to DG052000031	
			PAGE15 : Change CN1 P/N from DFHS30FR299 to DFHS30FR014 for SMT issues	

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