Husk/Petra
UMA/Muxless Schematics Document
Ivy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

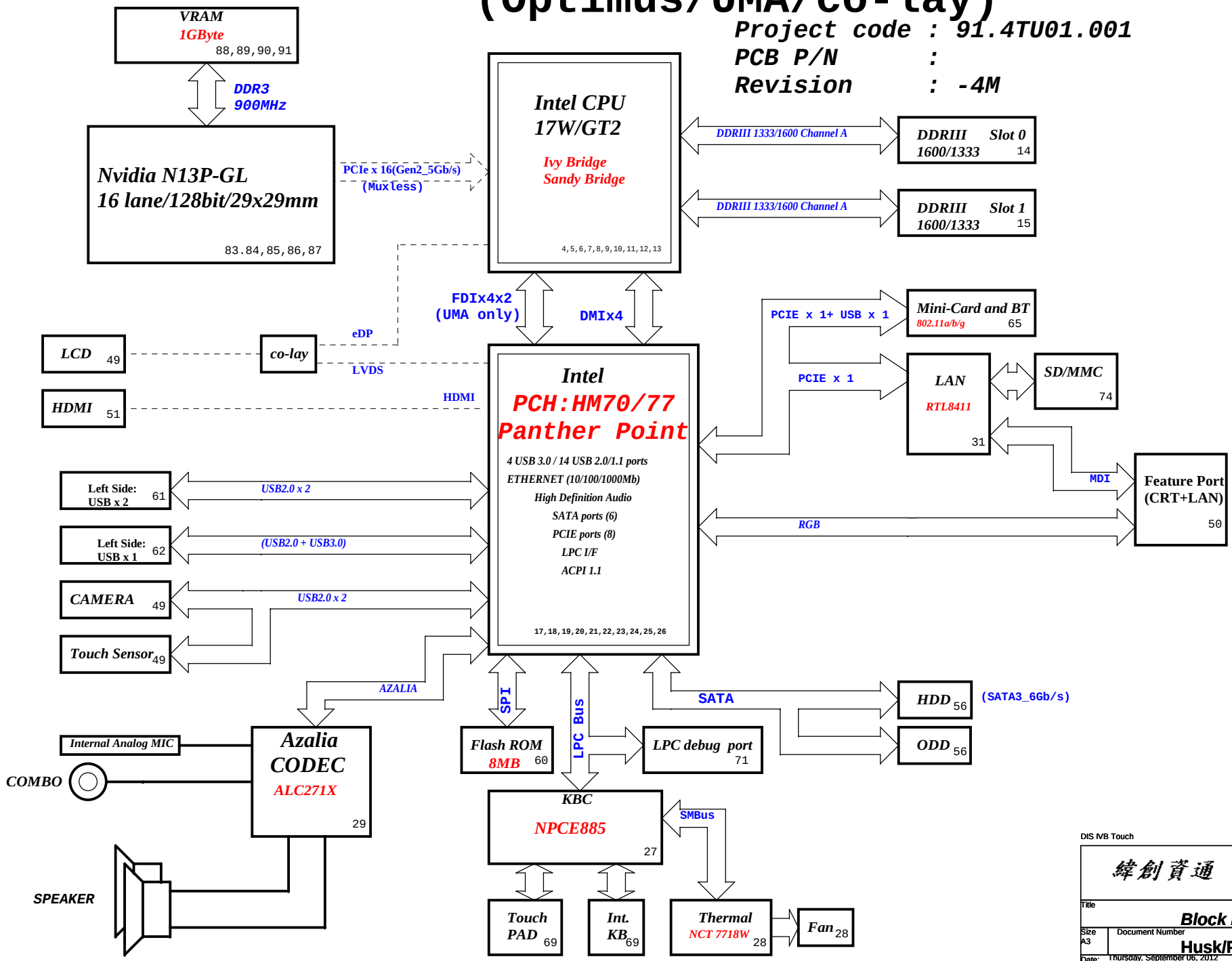
Title: *Cover Page*

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 1 of 103

Husk and Petra Block Diagram (Optimus/UMA/co-lay)

Project code : 91.4TU01.001
PCB P/N :
Revision : -4M



CHARGER BQ24727 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT8223MGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

CPU DC/DC ISL95836HRTZ 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC ISL95836HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC TPS51218DSCR 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

LDO RT9025-25ZSP 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

LDO G978 48	
INPUTS	OUTPUTS
1D05_VTT	0D85V_S0

VGA ISL62882CHRTZ 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

Switches 93	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D05V_VTT	1D05V_VGA_S0
1D5V_S3	1D5V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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Title: Block Diagram
Size: A3 | Document Number: Husk/Petra | Rev: -4M
Date: Thursday, September 06, 2012 | Sheet 2 of 103

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

DIS IVB Touch

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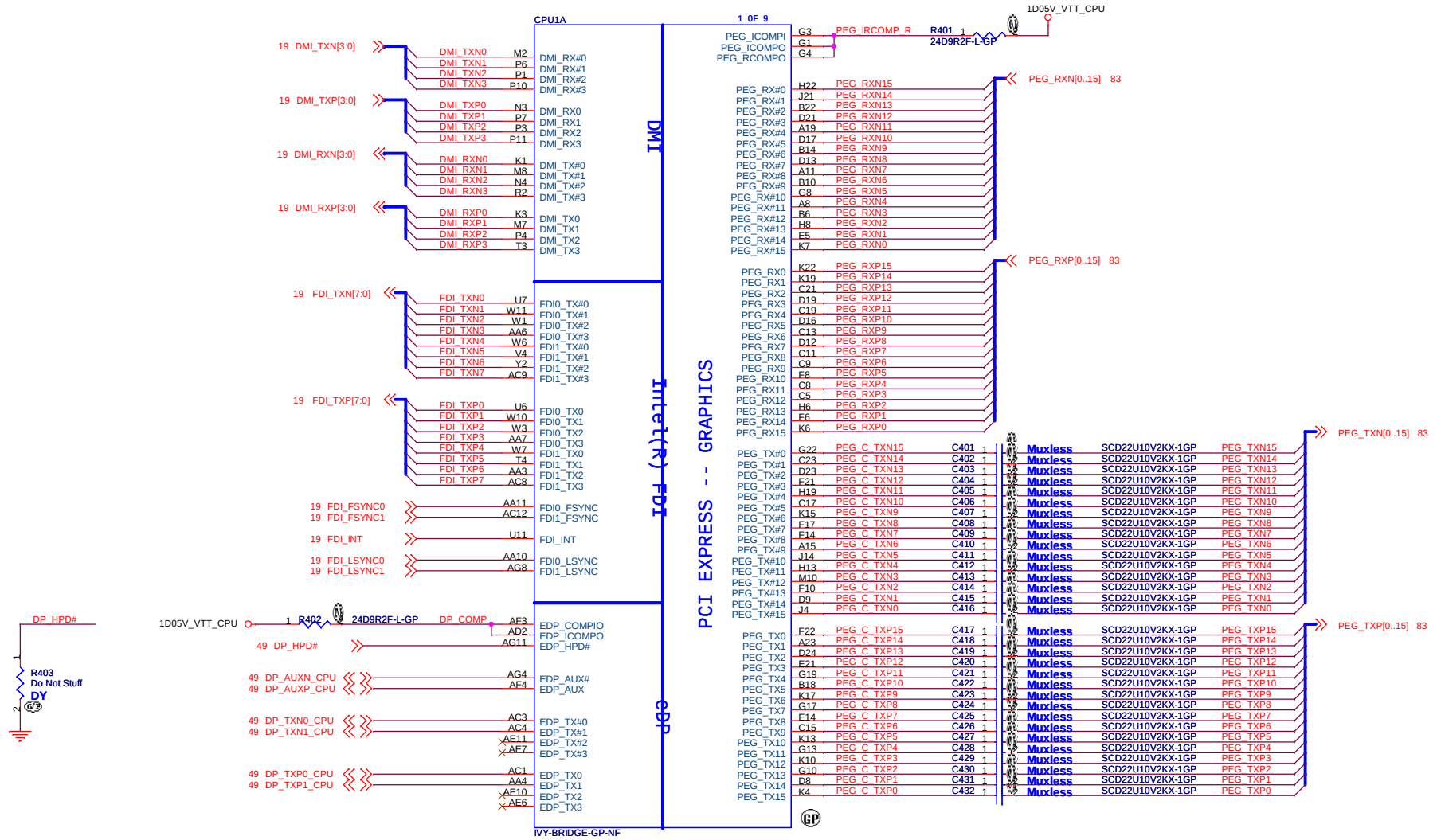
Title: Table of Content

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 3 of 103

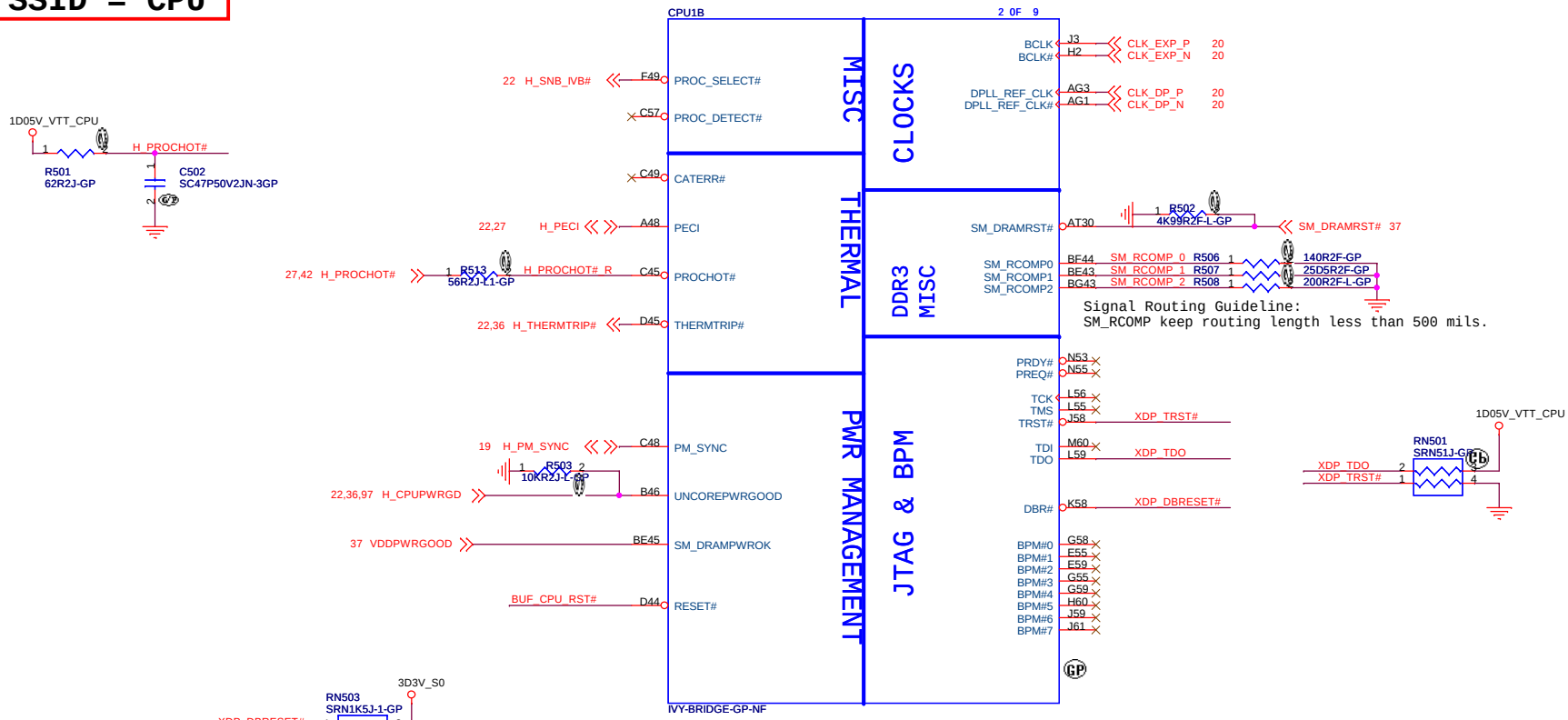
SSID = CPU



DIS IVB Touch

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU (PCIE/DMI/FDI)***
Size A3 / Document Number	**Husk/Petra** / Rev **-4M**
Date: Thursday, September 06, 2012	Sheet 4 of 103

SSID = CPU



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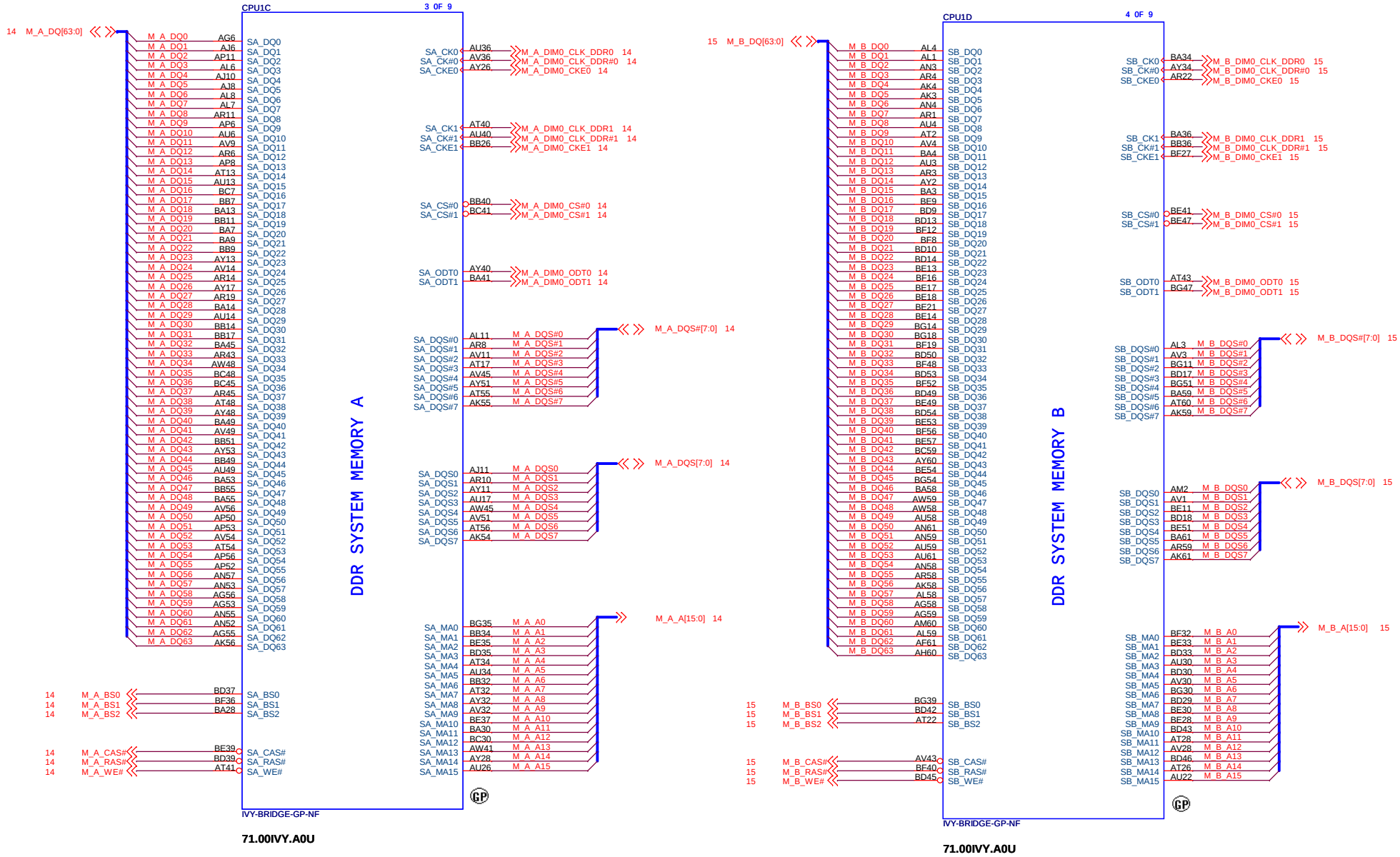
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (THERMAL/CLOCK/PM)**

Size: Custom | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Thursday, September 06, 2012 | Sheet 5 of 103

SSID = CPU



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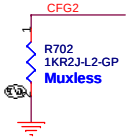
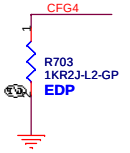
Title		
CPU (DDR)		
Size: A3	Document Number: **Husk/Petra**	Rev: **-4M**
Date: Thursday, September 06, 2012	Sheet 6 of 103	

SSID = CPU

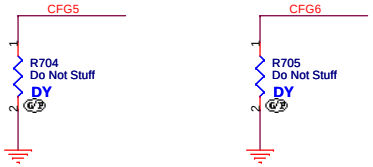
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



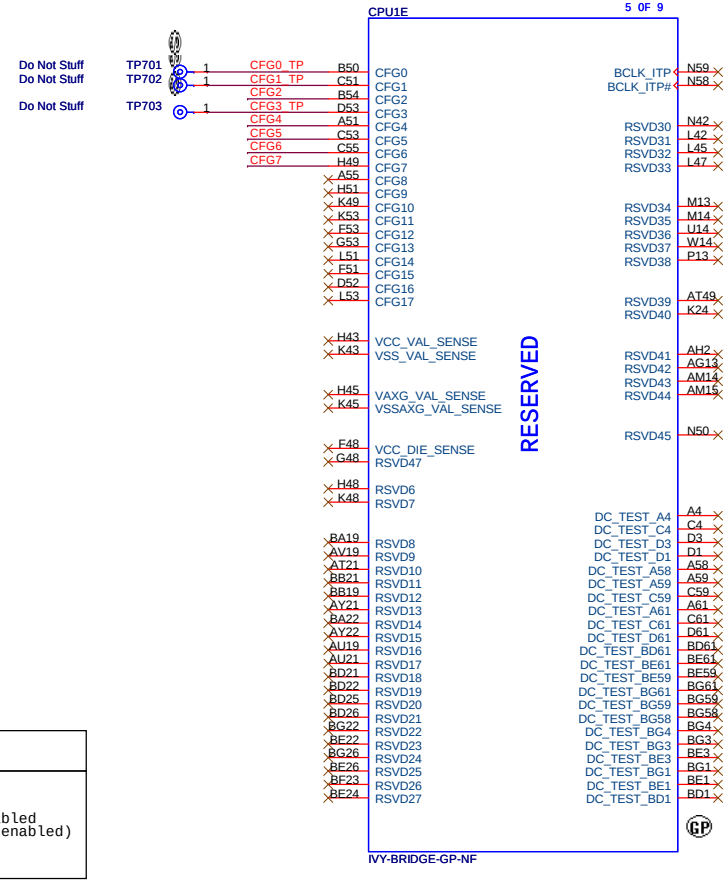
Enabl EDP function	
CFG4	1:Disable 0:Enable



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



71.00IVY.A0U

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Title: *CPU (RESERVED)*

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 7 of 103

SSID = CPU

POWER

ULV:17W
Iccmax:33A
ICC_TDC:25A

Iccmax:8.5A
ICC_TDC:8.5A

CPU1F

6 OF 9

CORE SUPPLY

PEG IO AND DDR IO

QUIET RAILS

SVID

SENSE LINES

IVY-BRIDGE-GP-NF

71.00IVY.A0U

Place near processor

Place near processor

DIS IVB Touch

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Monday, September 17, 2012 | Sheet 8 of 103

SSID = CPU

POWER

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

Iccmax:18A(GT1)
ICC_TDC:12A(GT1)

CPU1G — 7 OF 9

VCC_GFXCORE

SC10U6D3V5KX-1GP ×10 (C902, C903, C904, C905, C908, C919, C920, C921) — DY
SC1U6D3V2KX-1-GP ×5 (C907, C909, C914, C916) — DY

VAXG1, VAXG2, VAXG3, VAXG4, VAXG5, VAXG6, VAXG7, VAXG8, VAXG9, VAXG10, VAXG11, VAXG12, VAXG13, VAXG14, VAXG15, VAXG16, VAXG17, VAXG18, VAXG19, VAXG20, VAXG21, VAXG22, VAXG23, VAXG24, VAXG25, VAXG26, VAXG27, VAXG28, VAXG29, VAXG30, VAXG31, VAXG32, VAXG33, VAXG34, VAXG35, VAXG36, VAXG37, VAXG38, VAXG39, VAXG40, VAXG41, VAXG42, VAXG43, VAXG44, VAXG45, VAXG46, VAXG47, VAXG48, VAXG49, VAXG50, VAXG51, VAXG52, VAXG53, VAXG54, VAXG55, VAXG56

GRAPHICS

VREF

SM_VREF — AY43 — +V_SM_VREF_CNT 37

SA_DIMM_VREFDQ — BE7 — M_VREF_DQ_DIMM0_C — M_VREF_DQ_DIMM0_C 37
SB_DIMM_VREFDQ — BG7 — M_VREF_DQ_DIMM1_C — M_VREF_DQ_DIMM1_C 37

BE7 and BG7 is NC ball in HR

RN902 SRN1KJ-7-GP DY

DDR3 - 1.5V RAILS

Iccmax:5A

VDDQ1 AJ28, VDDQ2 AJ33, VDDQ3 AJ36, VDDQ4 AJ40, VDDQ5 AL30, VDDQ6 AL34, VDDQ7 AL38, VDDQ8 AL42, VDDQ9 AM33, VDDQ10 AM36, VDDQ11 AM40, VDDQ12 AN30, VDDQ13 AN34, VDDQ14 AN38, VDDQ15 AR26, VDDQ16 AR28, VDDQ17 AR30, VDDQ18 AR32, VDDQ19 AR34, VDDQ20 AR36, VDDQ21 AR40, VDDQ22 AV41, VDDQ23 AW26, VDDQ24 BA40, VDDQ25 BB28, VDDQ26 BG33

1D5V_S0

SC10U6D3V5KX-1GP ×9 (C910, C911, C912, C913, C918, C925) — DY
SC1U6D3V2KX-1-GP ×5 (C924, C917, C926) — DY

QUIET RAILS

PROCESSOR DDR 1.5V QUIET RAIL (BGA only)
+V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board

VCCDQ1 AM28, VCCDQ2 AN26 — +1.5S_VCCD_Q — R909 0R0402-PAD — C923 SC1U6D3V2KX-L-1-GP

1D5V_S0

SENSE LINES

VAXG_SENSE F45, VSSAXG_SENSE G45

42 VCC_AXG_SENSE
42 VSS_AXG_SENSE

VCC_GFXCORE
R906 100R2F-L1-GP-U
R907 100R2F-L1-GP-U
R906,R907 close to CPU

1.8V RAIL

1D8V_S0
ICC_MAX:1.2A
C922 SC1U10V2KX-1GP
VCCPLL1 BB3, VCCPLL2 BC1, VCCPLL3 BC4

SA RAIL

0D85V_S0
ICC_MAX:6A
C915 SC10U6D3V5KX-1GP
VCCSA1 L17, VCCSA2 L21, VCCSA3 N16, VCCSA4 N20, VCCSA5 N22, VCCSA6 P17, VCCSA7 P20, VCCSA8 R16, VCCSA9 R18, VCCSA10 R21, VCCSA11 U15, VCCSA12 V16, VCCSA13 V17, VCCSA14 V18, VCCSA15 V21, VCCSA16 W20

SENSE LINES

VDDQ_SENSE BC43 TP_VDDQ_SENSE — TP901 TPAD14-OP-GP
VSS_SENSE_VDDQ BA43 TP_VDDQ_VSS — TP902 TPAD14-OP-GP

0D85V_S0
R902 100R2F-L1-GP-U
R902 need be close to pin U10.
VCCSA_SENSE U10 — VCCSA_SENSE

VCCSA VID lines

VCCSA_VID0 D48 — VCCSA_VID0
VCCSA_VID1 D49 — VCCSA_VID1

VCCSA_VID[0]	VCCSA_VID[1]	Selected VCCSA (XE & SV segments)	Selected VCCSA (ULV segment)
0	0	0.9 V	0.9 V
0	1	0.8 V	0.85 V
1	0	0.725 V	0.775 V
1	1	0.675 V	0.75 V

1D05V_VTT_CPU
R908 10KR2J-L-GP DY
R912 10KR2J-L-GP DY
R913 10KR2J-L-GP
R914 10KR2J-L-GP
VCCSA_VID0 48
VCCSA_VID1 48

IVY-BRIDGE-GP-NF

71.00IVY.A0U

DIS IVB Touch

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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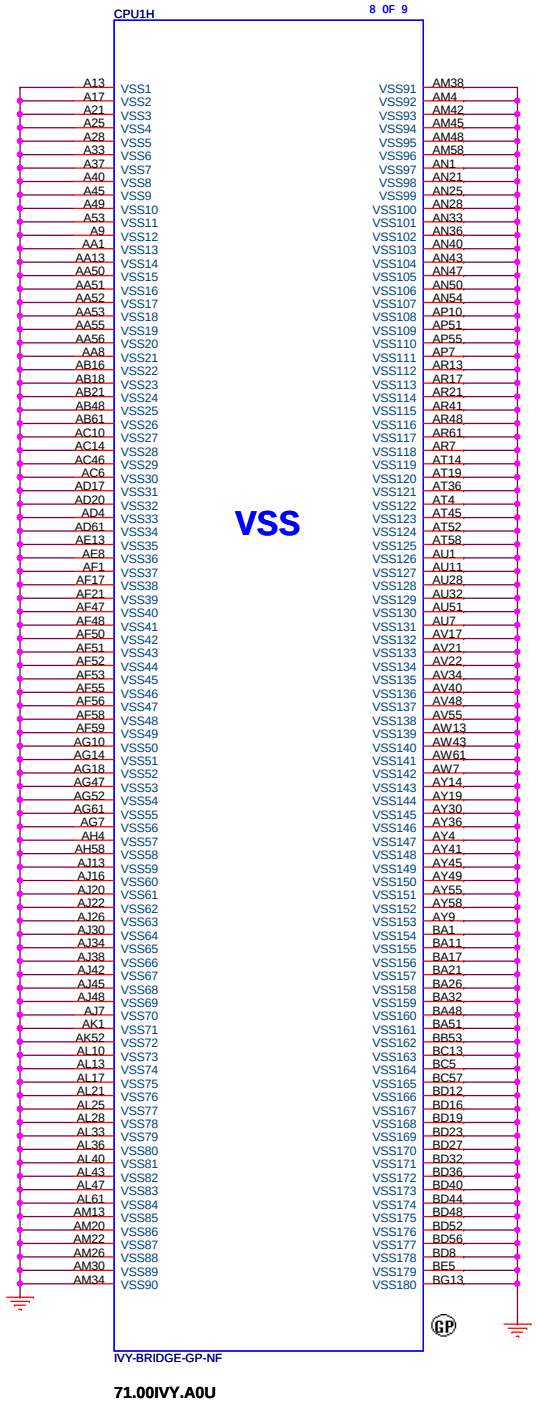
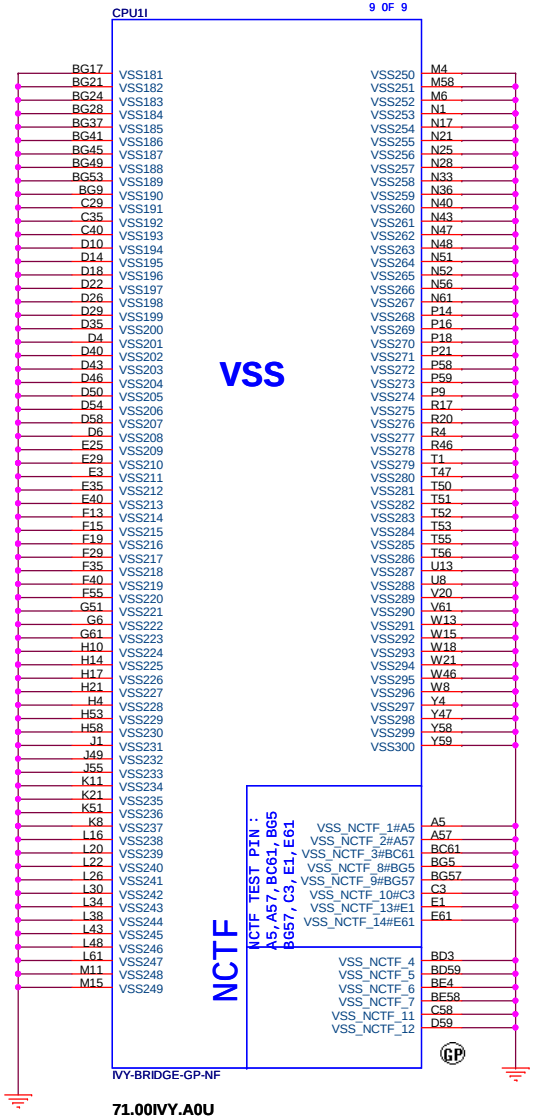
Title: CPU (VCC_GFXCORE)
Size: Custom | Document Number: Husk/Petra | Rev: -4M
Date: Monday, September 17, 2012 | Sheet 9 of 103

SSID = CPU





DIS IVB Touch

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Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 10 of 103

DIS IVB Touch

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Title: ***XDP***		
Size: A3	Document Number: **Husk/Petra**	Rev: **-4M**
Date: Thursday, September 06, 2012	Sheet 11 of 103	

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Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 12 of 103

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DIS IVB Touch

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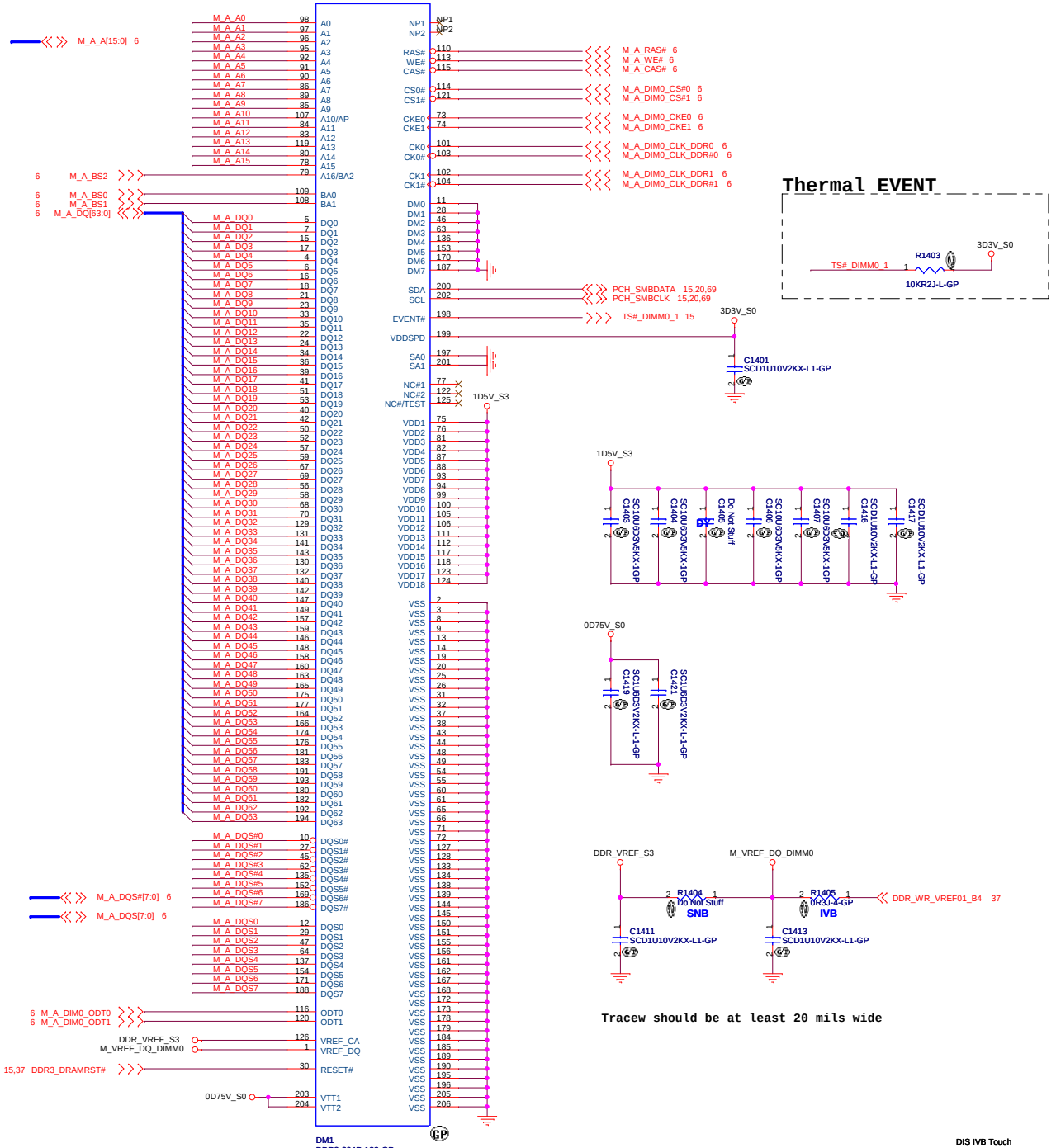
Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 13 of 103

SSID = MEMORY



Thermal EVENT

Tracew should be at least 20 mils wide

DIS IVB Touch

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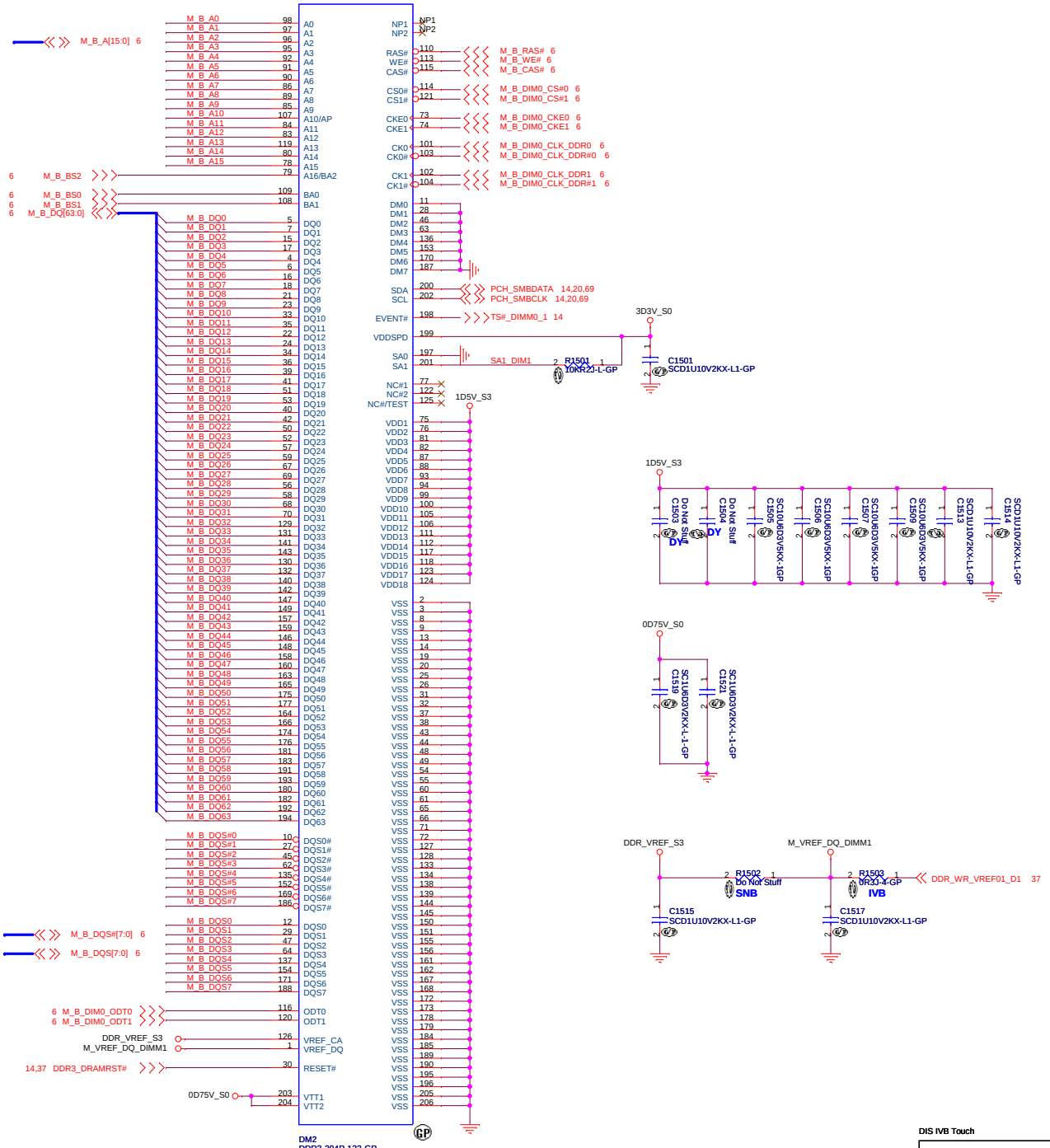
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM1***

Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 14 of 103

SSID = MEMORY



DIS IVB Touch

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Title: ***DDR3-SODIMM2***

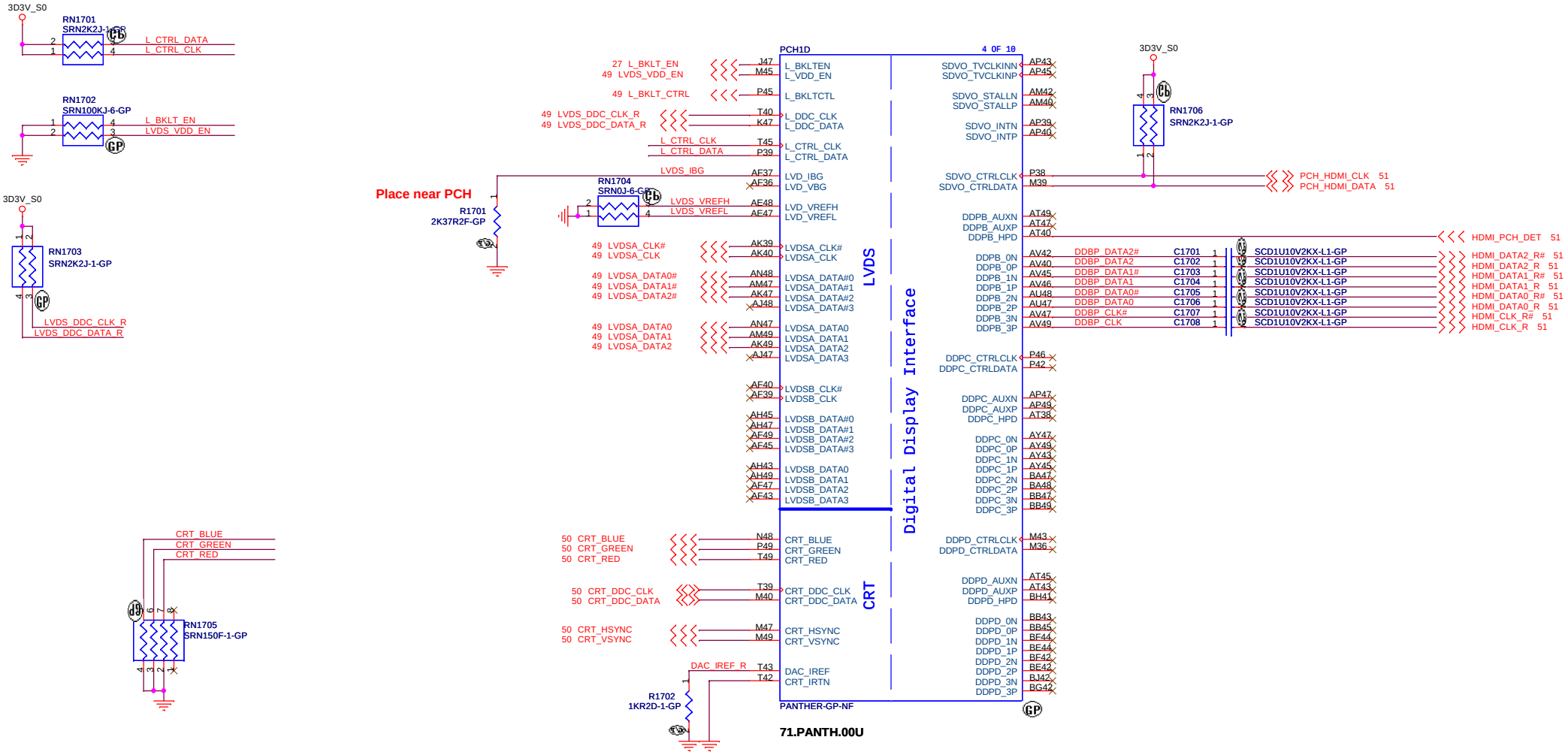
Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 15 of 102

(Blanking)

DIS IVB Touch

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***DDR3-SODIMM2***		
Size: A4	Document Number: **Husk/Petra**	Rev: **-4M**
Date: Thursday, September 06, 2012	Sheet 16 of 103	



DIS IVB Touch

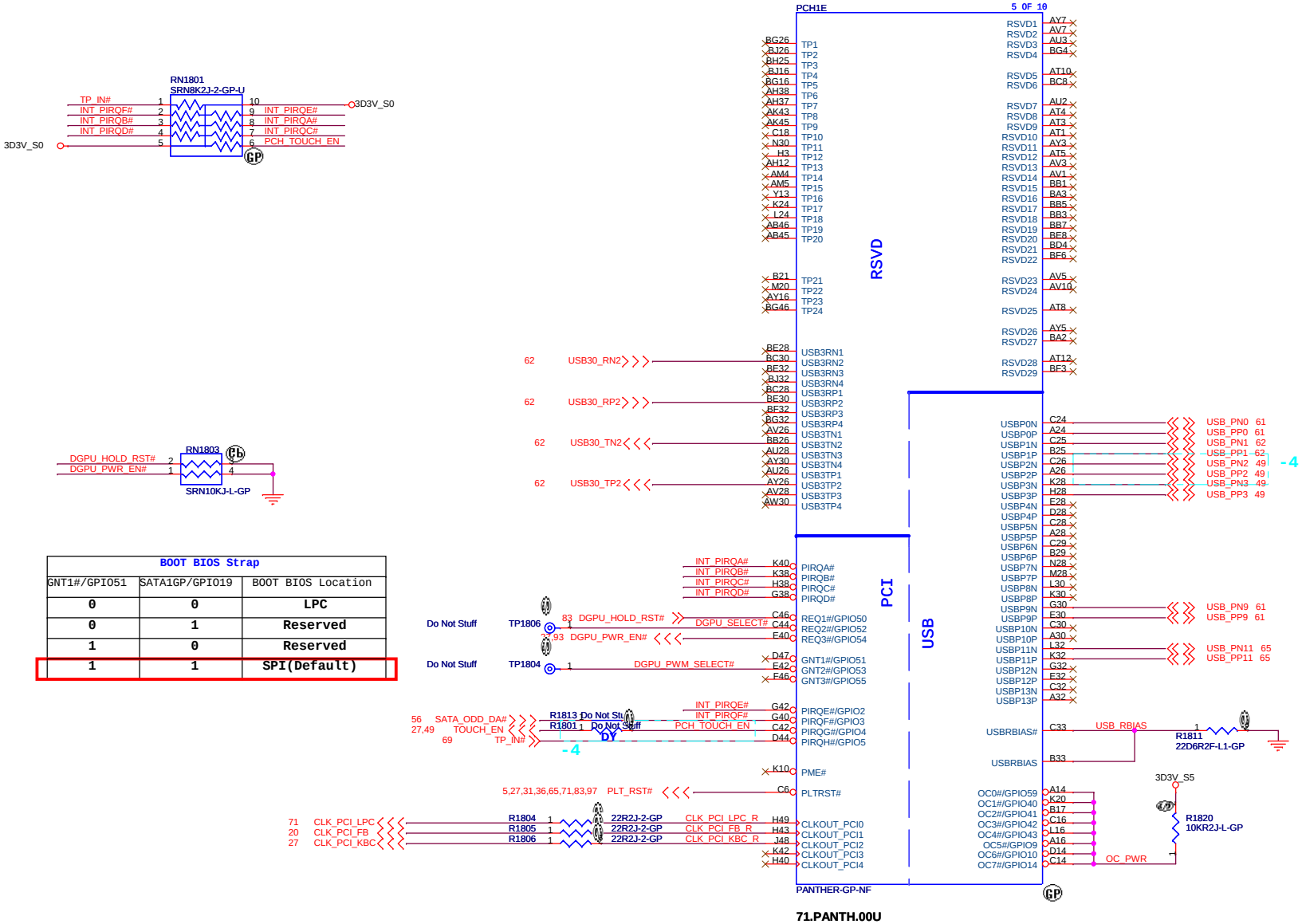
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (LVDS/CRT/DDI)**

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 17 of 103

SSID = PCH



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB Table

Pair	Device
0	USB2.0 Ext. port 1
1	USB3.0/USB2.0 Ext. port 2
2	Touch panel
3	CCD
4	
5	
6	may not be available
7	may not be available
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

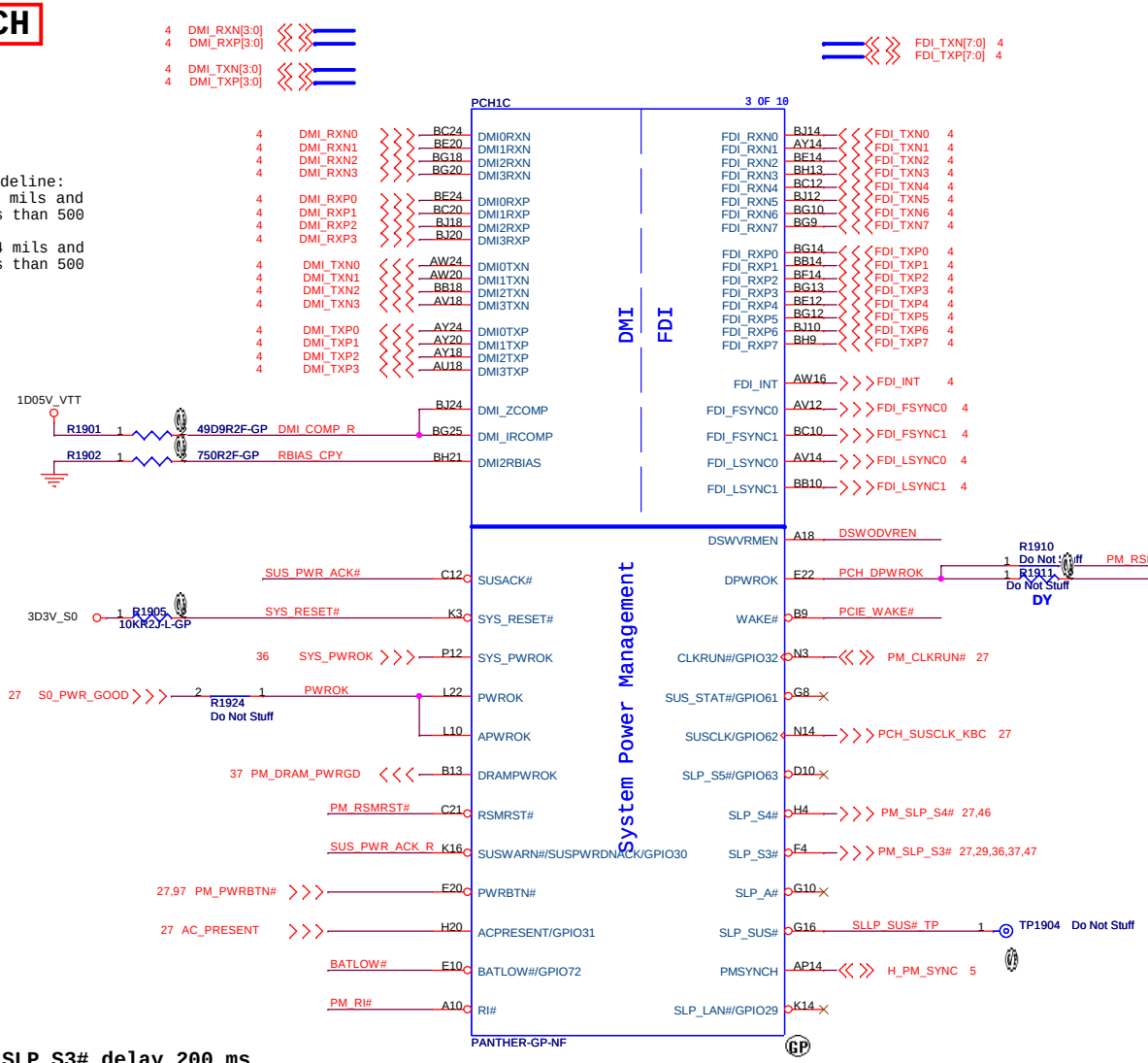
Title: **PCH (PCI/USB/NVRAM)**

Size	Document Number	Rev
Custom	Husk/Petra	-4M

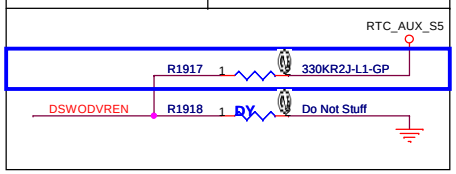
Date: Thursday, September 06, 2012 Sheet 18 of 103

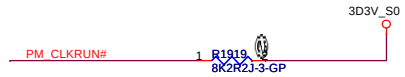
SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

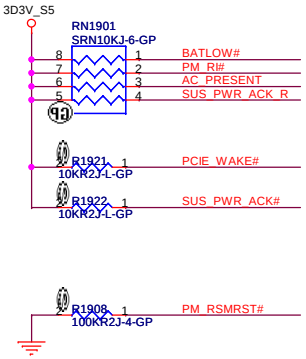


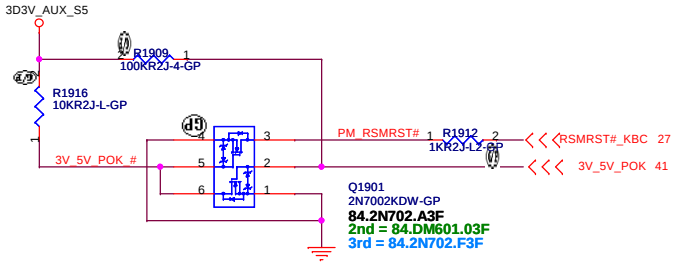
DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled





S0_PWR_GOOD after PM_SLP_S3# delay 200 ms



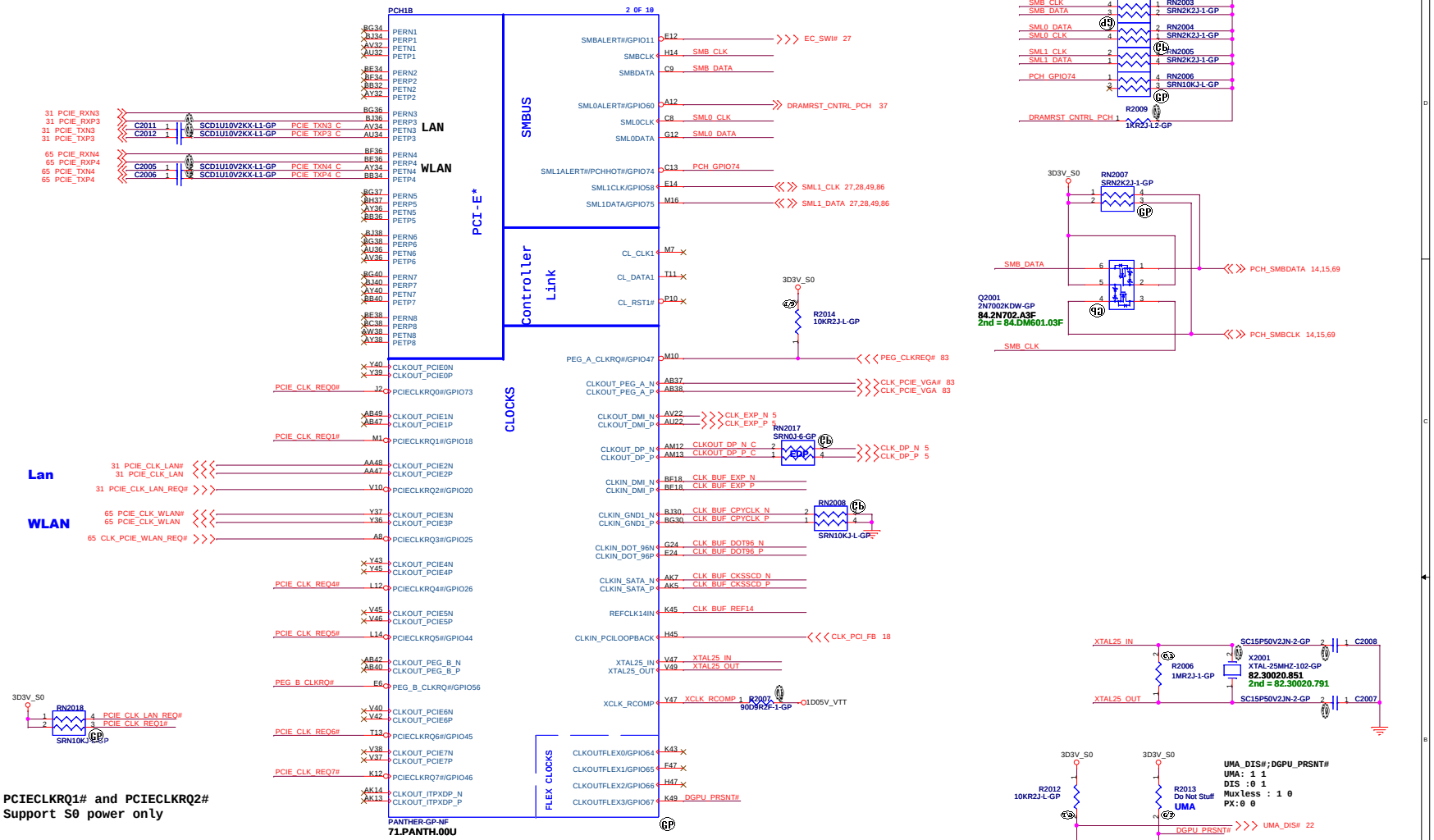


71.PANTH.00U

DIS IVB Touch

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (DM I/FDI/PM)		
Size: A3	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 19 of 103	

SSID = PCH



DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 20 of 103

SSID = PCH

RTC_AUX_S5

R2115 1 20KR2F-L-GP
R2116 1 20KR2F-L-GP
C2103 SC1U16V3KX-5GP

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

RTC_X1 — R2101 10MR2J-L-GP — RTC_X2
X2101 X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.B21
C2101 SC6P50V2CN-1GP
C2102 SC6P50V2CN-1GP

C2104 SC1U16V3KX-5GP
G2101 Do Not Stuff
R2104 1MR2J-L-GP
R2105 330KR2F-L-GP
RTC_AUX_S5

RTC Reset

27 RTCRST_ON — Q2102 2N7002K-2-GP — RTC_RST#
R2106 100KR2F-L1-GP
R2111 2KR2F-3-GP
84.2N702.J31
2ND = 84.2N702.031

PCH1A — 1 OF 10

RTC_X1	A20	RTCX1	RTC
RTC_X2	C20	RTCX2	
RTC_RST#	D20	RTCRST#	
SRTC_RST#	G22	SRTCRST#	
SM_INTRUDER#	K22	INTRUDER#	
PCH_INTVRMEN	C17	INTVRMEN	
HDA_BITCLK	N34	HDA_BCLK	IHDA
HDA_SYNC	L34	HDA_SYNC	
29 HDA_SPKR	T10	SPKR	
HDA_RST#	K34	HDA_RST#	
29 HDA_SDIN0	E34	HDA_SDIN0	
	G34	HDA_SDIN1	
	C34	HDA_SDIN2	
	A34	HDA_SDIN3	
27 ME_UNLOCK — R2107 1KR2J-L2-GP	HDA_SDOUT	A36 HDA_SDO	
	C36	HDA_DOCK_EN#/GPIO33	
	N32	HDA_DOCK_RST#/GPIO13	
R2121 4K7R2J-L-GP	PCH_JTAG_TCK_BUF	J3 JTAG_TCK	JTAG
		H7 JTAG_TMS	
		K5 JTAG_TDI	
		H1 JTAG_TDO	
27,60 SPI_CLK_R — R2108 33R2J-L1-GP	PCH_SPI_CLK	T3 SPI_CLK	SPI
27,60 SPI_CS0#_R — R2109 33R2J-L1-GP	PCH_SPI_CS0#	Y14 SPI_CS0#	
		T1 SPI_CS1#	
27,60 SPI_SI_R — R2110 33R2J-L1-GP	PCH_SPI_SI	V4 SPI_MOSI	
27,60 SPI_SO_R		U3 SPI_MISO	

PANTHER-GP-NF

71.PANTH.00U

		FWH0/LAD0 C38 LPC_AD0	LPC
		FWH1/LAD1 A38 LPC_AD1	
		FWH2/LAD2 B37 LPC_AD2	
		FWH3/LAD3 C37 LPC_AD3	
		FWH4/LFRAME# D36 LPC_FRAME# 27,71	
		LDRQ0# E36	
		LDRQ1#/GPIO23 K36	
		SERIRQ V5 INT_SERIRQ 27	
		SATA0RXN AM3 SATA_RXN0 56	SATA 6G
		SATA0RXP AM1 SATA_RXP0 56	
		SATA0TXN AP7 SATA_TXN0 56	
		SATA0TXP AP5 SATA_TXP0 56	
		SATA1RXN AM10	
		SATA1RXP AM8	
		SATA1TXN AP11	
		SATA1TXP AP10	
		SATA2RXN AD7	
		SATA2RXP AD5	
		SATA2TXN AH5	
		SATA2TXP AH4	
		SATA3RXN AB8	
		SATA3RXP AB10	
		SATA3TXN AF3	
		SATA3TXP AF1	
		SATA4RXN Y7 SATA_RXN4 56	SATA
		SATA4RXP Y5 SATA_RXP4 56	
		SATA4TXN AD3 SATA_TXN4 56	
		SATA4TXP AD1 SATA_TXP4 56	
		SATA5RXN Y3	
		SATA5RXP Y1	
		SATA5TXN AB3	
		SATA5TXP AB1	
		SATAICOMPO Y11	
		SATAICOMPI Y10 SATA_COMP R2112 37D4R2F-GP	
		SATA3RCOMPO AB12	
		SATA3COMPI AB13 SATA3_COMP R2113 49D9R2F-GP	
		SATA3RBIAS AH1 RBIAS_SATA3 R2114 750R2F-GP	
		SATALED# P3 SATA_LED#	
		SATA0GP/GPIO21 V14 SATA_DET#0	
		SATA1GP/GPIO19 P1	

1D05V_VTT

HDD1

ODD

29 HDA_CODEC_SYNC — R2122 DY 1 Do Not Stuff — HDA_SYNC
29 HDA_CODEC_SDOUT — R2123 33R2J-L1-GP — HDA_SDOUT
29 HDA_CODEC_RST# — HDA_RST#
29 HDA_CODEC_BITCLK — HDA_BITCLK
RN2102 SRN33J-5-GP-U

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

+3VS_+1.5VS_HDA_IO — R2102 Do Not Stuff DY — HDA_SDOUT

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

+3VS_+1.5VS_HDA_IO — R2103 1KR2J-L2-GP — HDA_SYNC

5V_S0 — Q2101 2N7002K-2-GP — HDA_SYNC_R — R2124 33R2J-L1-GP — HDA_SYNC
HDA_CODEC_SYNC
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31

HDA_CODEC_BITCLK — EC2102 Do Not Stuff DY
HDA_CODEC_SDOUT — EC2103 Do Not Stuff DY
SPI_CS0#_R — EC2101 Do Not Stuff DY

LPC_AD[0..3] 27,71

3D3V_S0
RN2103 SRN10KJ-6-GP
22 PSW_CLR#
SATA_LED#
INT_SERIRQ
SATA_DET#0

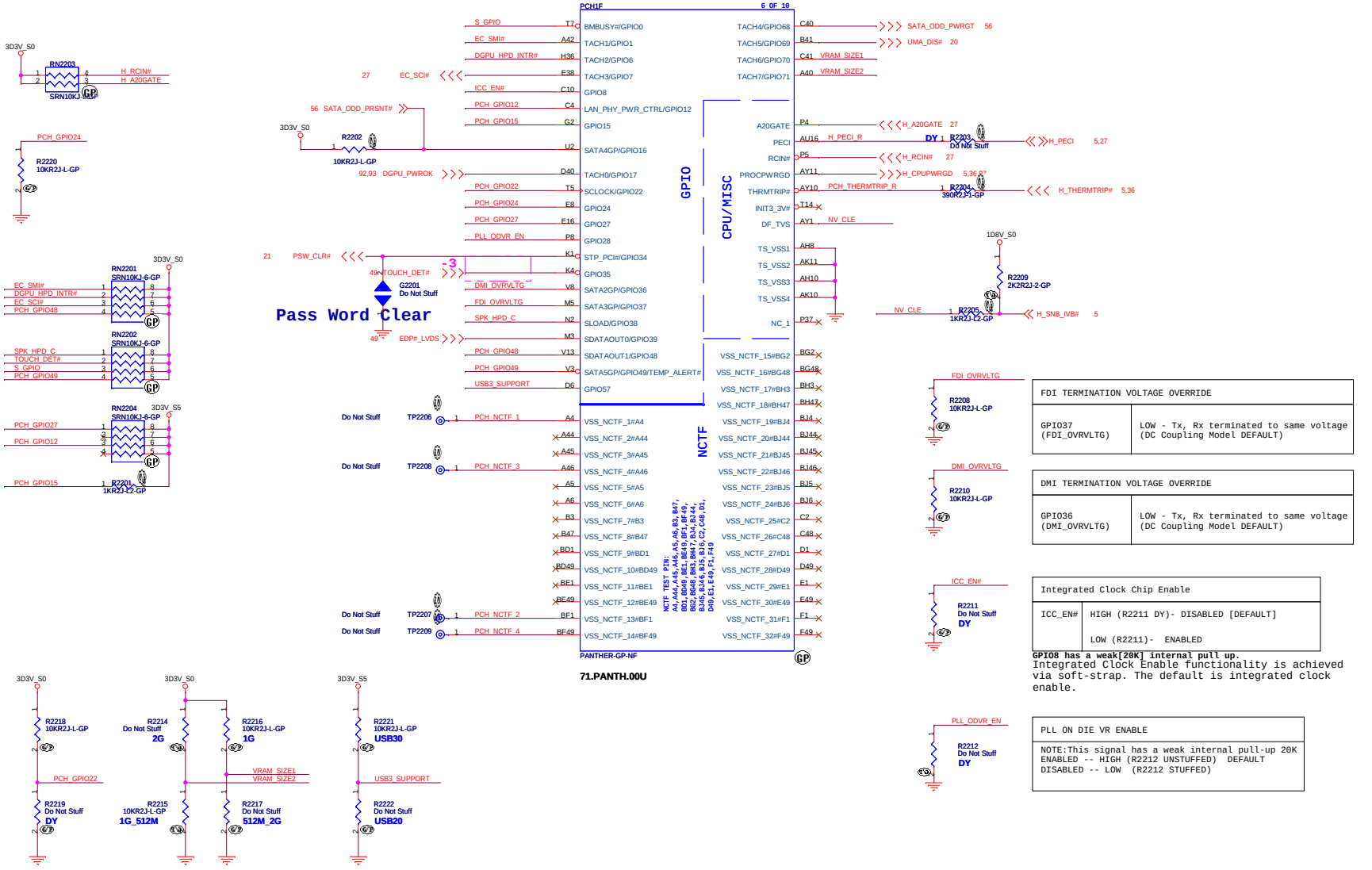
HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: Custom | Document Number: Husk/Petra | Rev: -4M
Date: Thursday, September 06, 2012 | Sheet 21 of 103

SSID = PCH



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

DIS IVB Touch

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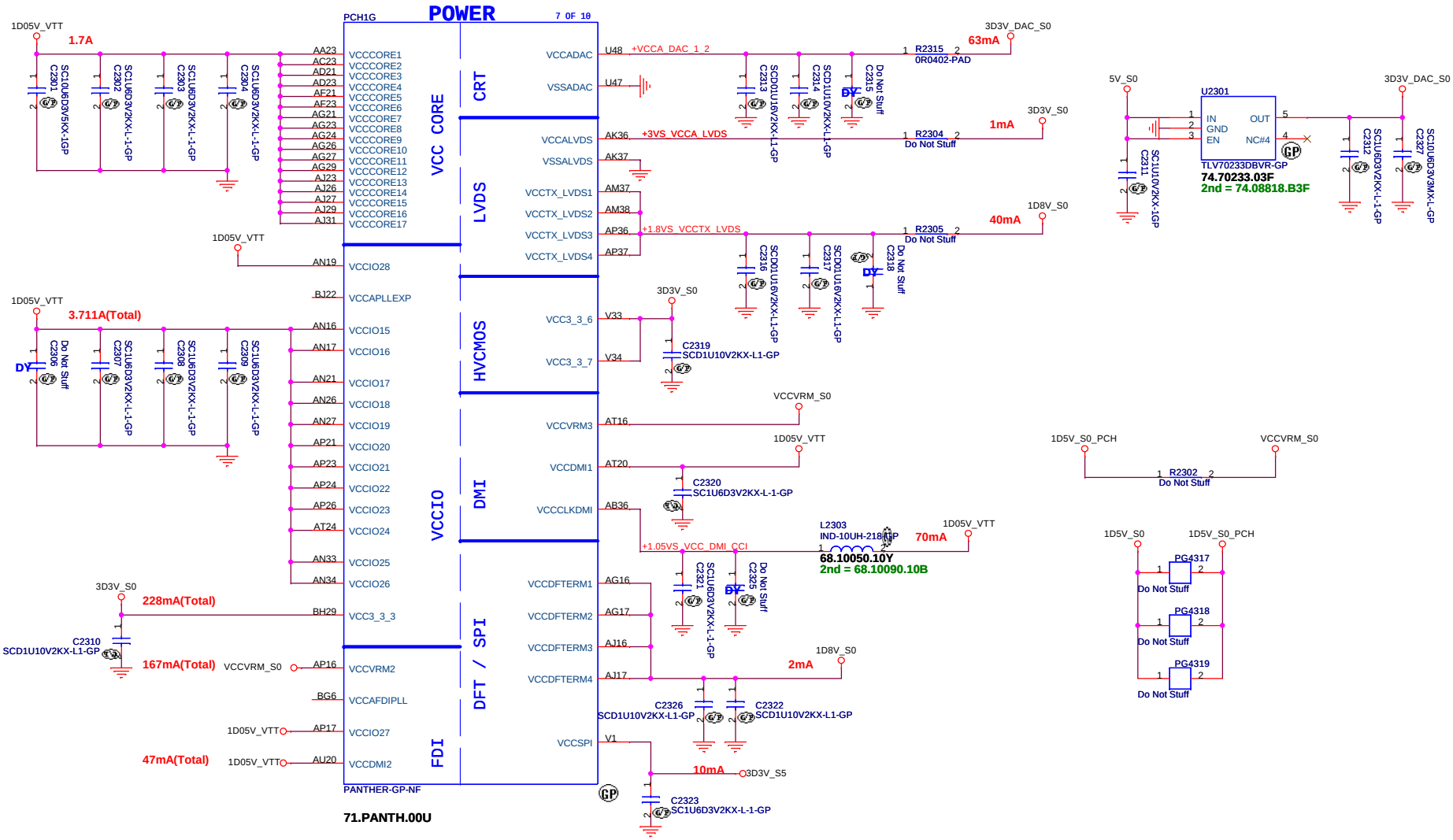
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 22 of 103

SSID = PCH



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 23 of 103

SSID = PCH

POWER

PCH1J — 10 OF 10 — PANTHER-GP-NF

USB

AD49	VCCACLK
T16	VCCDSW3_3
V12	DCPSUSBYP
T38	VCC3_3_5
BH23	VCCAPLLDMI2
AL29	VCCIO14
AL24	DCPSUS3
N26	VCCIO29
P26	VCCIO30
P28	VCCIO31
T27	VCCIO32
T29	VCCIO33
T23	VCCSUS3_3_7
T24	VCCSUS3_3_8
V23	VCCSUS3_3_9
V24	VCCSUS3_3_10
P24	VCCSUS3_3_6
T26	VCCIO34
M26	V5REF_SUS
AN23	DCPSUS4
AN24	VCCSUS3_3_1

Clock and Miscellaneous

AA19	VCCASW1
AA21	VCCASW2
AA24	VCCASW3
AA26	VCCASW4
AA27	VCCASW5
AA29	VCCASW6
AA31	VCCASW7
AC26	VCCASW8
AC27	VCCASW9
AC29	VCCASW10
AC31	VCCASW11
AD29	VCCASW12
AD31	VCCASW13
W21	VCCASW14
W23	VCCASW15
W24	VCCASW16
W26	VCCASW17
W29	VCCASW18
W31	VCCASW19
W33	VCCASW20
P34	V5REF

PCI/GPIO/LPC

N20	VCCSUS3_3_2
N22	VCCSUS3_3_3
P20	VCCSUS3_3_4
P22	VCCSUS3_3_5
AA16	VCC3_3_1
W16	VCC3_3_8
T34	VCC3_3_4

SATA

N16	DCPRTC
Y49	VCCVRM4
BD47	VCCADPLLA
BF47	VCCADPLLB
AJ2	VCC3_3_2
AF13	VCCIO5
AH13	VCCIO12
AH14	VCCIO13
AF14	VCCIO6
AK1	VCCAPLLSATA
AF11	VCCVRM1

MISC

AF17	VCCIO7
AF33	VCCDIFFCLKN1
AF34	VCCDIFFCLKN2
AG34	VCCDIFFCLKN3
AG33	VCCSSC
V16	DCPSST
T17	DCPSUS1
V19	DCPSUS2
AC16	VCCIO2
AC17	VCCIO3
AD17	VCCIO4
T21	VCCASW22
V21	VCCASW23
T19	VCCASW21

CPU

BJ8	V_PROC_IO

RTC

A22	VCCRTC

HDA

P32	VCCSUSHDA

71.PANTH.00U

Power rails and components

- 3D3V_S5 — R2402 0R0402-PAD — VCCDSW3_3 — 1mA
- 3D3V_AUX_S5 — R2403 0R2J-L-GP — DY
- 3D3V_S0 — C2402 SC1U10V2KX-1GP
- 1D05V_VTT — VCCIO14
- DCPSUS3
- VCCIO29 N26 — C2423 SC1U6D3V2KX-L-1-GP
- VCCIO30 P26
- VCCIO31 P28
- VCCIO32 T27
- VCCIO33 T29
- 3D3V_S5 — C2424 SCD1U10V2KX-L1-GP
- VCCSUS3_3_7 T23
- VCCSUS3_3_8 T24
- VCCSUS3_3_9 V23
- VCCSUS3_3_10 V24
- VCCSUS3_3_6 P24 — 3D3V_S5 — 95mA — C2425 SCD1U10V2KX-L1-GP
- VCCIO34 T26 — 1D05V_VTT
- V5REF_SUS M26 — +5VA_PCH_VCC5REFSUS — 1mA
- DCPSUS4 AN23
- VCCSUS3_3_1 AN24 — 3D3V_S5
- 1D05V_VTT — 903mA — C2403 SC10U6D3V5KX-1GP; C2404 SC10U6D3V5KX-1GP; C2406 SC1U6D3V2KX-1-GP; C2407 SC1U6D3V2KX-1-GP; C2408 SC1U6D3V2KX-1-GP — DY / DY
- V5REF P34 — +5VS_PCH_VCC5REF — 1mA
- VCCASW1 AA19
- VCCASW2 AA21
- VCCASW3 AA24
- VCCASW4 AA26
- VCCASW5 AA27
- VCCASW6 AA29
- VCCASW7 AA31
- VCCASW8 AC26
- VCCASW9 AC27
- VCCASW10 AC29
- VCCASW11 AC31
- VCCASW12 AD29
- VCCASW13 AD31
- VCCASW14 W21
- VCCASW15 W23
- VCCASW16 W24
- VCCASW17 W26
- VCCASW18 W29
- VCCASW19 W31
- VCCASW20 W33
- VCCSUS3_3_2 N20
- VCCSUS3_3_3 N22
- VCCSUS3_3_4 P20
- VCCSUS3_3_5 P22
- 3D3V_S5 — C2428 SC1U6D3V2KX-L-1-GP
- VCC3_3_1 AA16
- VCC3_3_8 W16
- VCC3_3_4 T34 — C2430 SCD1U10V2KX-L1-GP
- 3D3V_S0 — C2431 SCD1U10V2KX-L1-GP
- 3D3V_S0 — VCC3_3_2 AJ2 — C2429 SCD1U10V2KX-L1-GP
- VCCIO5 AF13
- VCCIO12 AH13
- VCCIO13 AH14 — 1D05V_VTT — C2432 SC1U6D3V2KX-L-1-GP
- VCCIO6 AF14
- VCCAPLLSATA AK1
- VCCVRM1 AF11 — VCCVRM_S0
- VCCIO2 AC16
- VCCIO3 AC17
- VCCIO4 AD17 — 1D05V_VTT — C2435 SC1U6D3V2KX-L-1-GP
- VCCASW22 T21
- VCCASW23 V21
- VCCASW21 T19
- 1D05V_VTT — C2434 SCD1U10V2KX-L1-GP
- VCCSUSHDA P32 — +3VS_+1.5VS_HDA_IO — 10mA — C2433 SCD1U10V2KX-L1-GP
- L2402 IND-10UH-218-GP — 80mA — 68.10050.10Y / 2nd = 68.10090.10B — +1.05VS_VCCA_A_DPL — C2409 SC1U6D3V2KX-L-1-GP
- L2403 IND-10UH-218-GP — 80mA — 68.10050.10Y / 2nd = 68.10090.10B — +1.05VS_VCCA_B_DPL — C2410 SC1U6D3V2KX-L-1-GP
- +VCCRTCEXT — C2411 SCD1U10V2KX-L1-GP
- VCCVRM_S0 — +1.05VS_VCCA_A_DPL — +1.05VS_VCCA_B_DPL
- C2412 — 1D05V_VTT — 55mA — SC1U6D3V2KX-L-1-GP
- C2414 SC1U6D3V2KX-L-1-GP
- C2413 — SC1U6D3V2KX-L-1-GP — +VCCSST — C2415 SCD1U10V2KX-L1-GP
- 1D05V_VTT — 1mA — SC407U6D3V3KX-L-GP; C2418 SCD1U10V2KX-L1-GP; C2419 SCD1U10V2KX-L1-GP — DY / DY
- RTC_AUX_S5 — 6uA — C2420 SC1U6D3V2KX-L-1-GP — DY
- 3D3V_S5 — D2401 CH751H-40PT-GP — 83.R0304.A8F / 2nd = 83.R0304.D8F — 5V_S5 — R2408 10R2J-2-GP — C2426 SCD1U10V2KX-L1-GP
- 3D3V_S0 — D2402 CH751H-40PT-GP — 83.R0304.A8F / 2nd = 83.R0304.D8F — 5V_S0 — R2407 10R2J-2-GP — C2427 SC1U10V2KX-1GP

Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
VSREF_SUS	VCCSUS3_3	a) VCCSREF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VCCSREF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
VSREF	VCC3_3	a) VSREF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCCSREF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms	a) VSREF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)

- 3D3V_S5 — U2401 G9090-150T11U-GP / 74.09090.A3F — 1D5V_S5
- C2437 SC1U10V3KX-L1-GP — DY
- C2421 SC1U10V3KX-L1-GP — DY
- C2416 SC10U6D3V5KX-1GP — DY
- +3VS_+1.5VS_HDA_IO — R2410 0R3J-4-GP — DY — 1D5V_S5
- R2409 0R0603-PAD — 3D3V_S5
- R2415 0R3J-4-GP — DY — 1D5V_S0_PCH

DIS IVB Touch

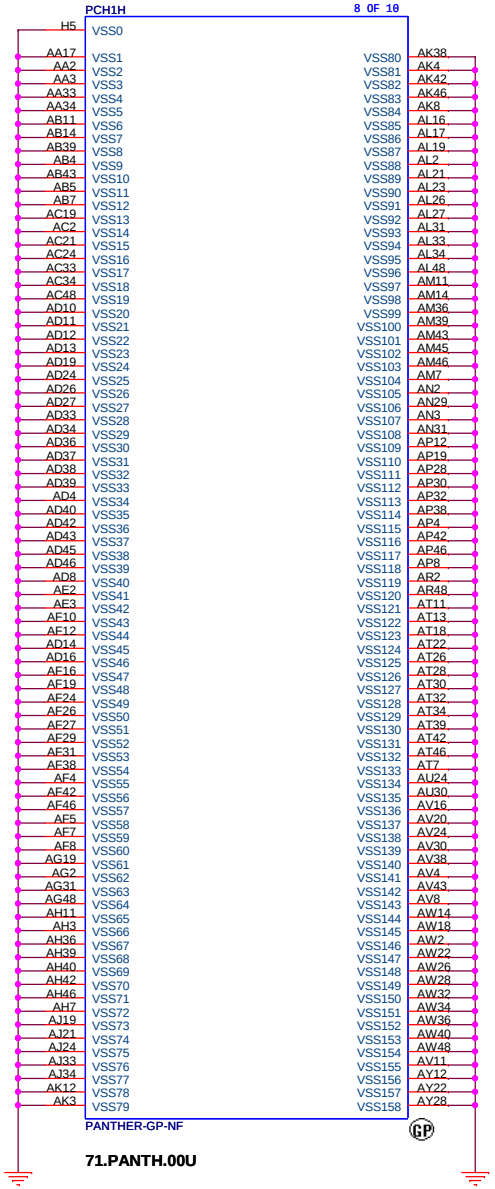
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

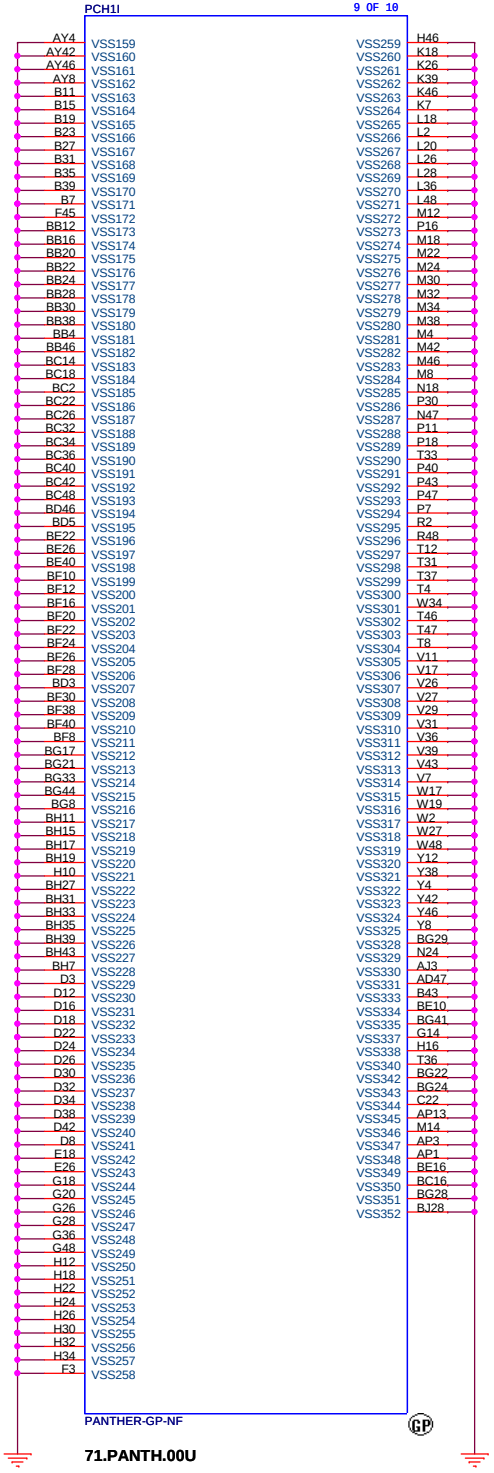
Title: PCH (POWER2)

Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Monday, September 17, 2012 Sheet 24 of 103

SSID = PCH





DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 25 of 103

DIS IVB Touch

緯創資通 **Wistron Corporation**
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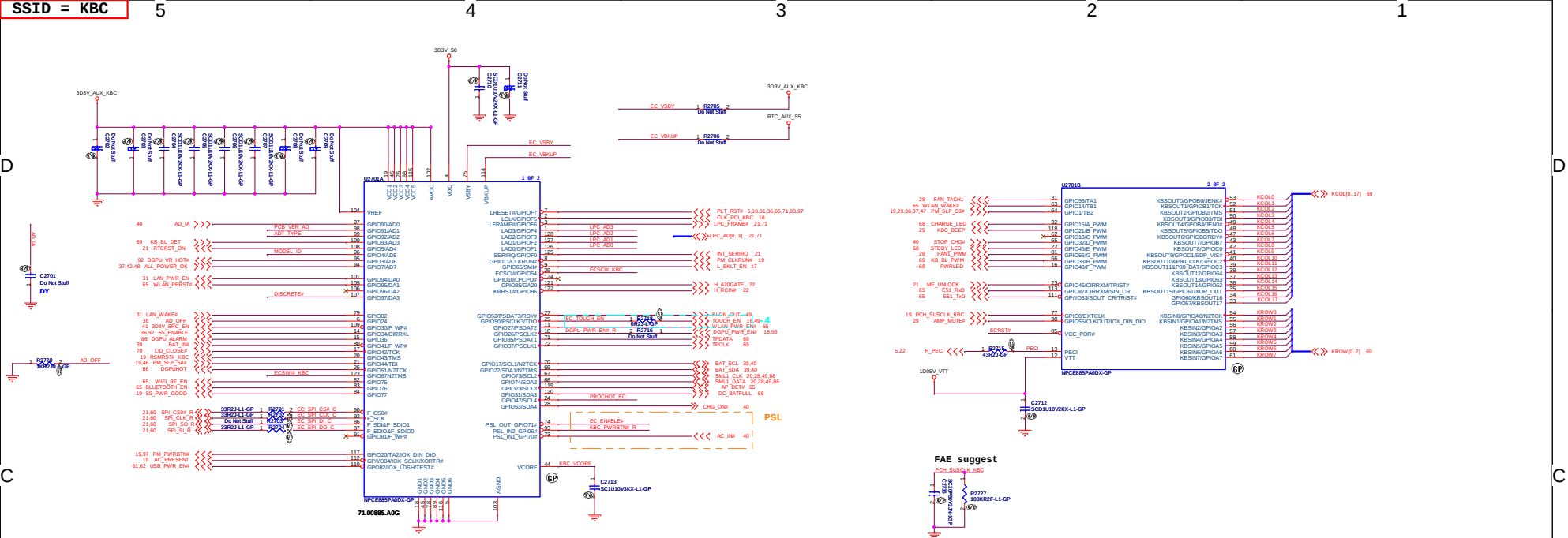
Taipei Hsien 221, Taiwan, R.O.C.

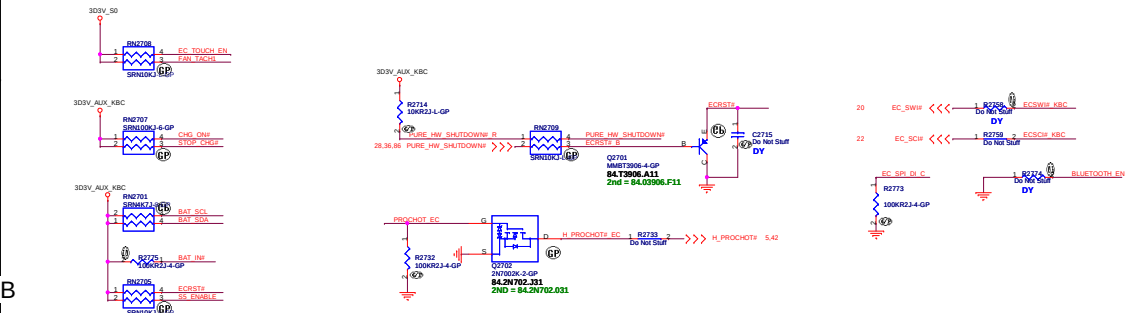
Title
Clock(colay)

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

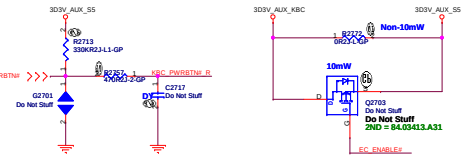
Date: Thursday, September 06, 2012 Sheet 26 of 103

SSID = KBC



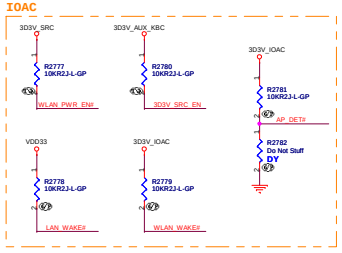


PSL Function

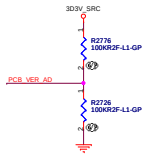


AC_IN#	KBC_PWRBTN#	EC_ENABLE#

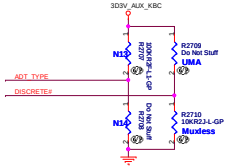
Inputs			Output
PSL_IN1_GPI70	PSL_IN2_GPI06	Bit 1 of P7DOUT Register	PSL_OUT_GPIO71
Low	X	X	Low
High	High-to-Low	X	Low
High	X	0-to-1	High



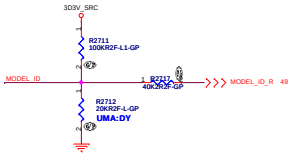
PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
-1	100.0K	33.0K	2.48V
-2	100.0K	47.0K	2.24V
-3	100.0K	64.9K	2.0V
-4	100.0K	76.8K	1.87V
-4M	100.0K	100K	1.65V
	100.0K	143.0K	1.358V
	100.0K	174.0K	1.204V
	100.0K	215.0K	1.047V



ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V



MODEL_ID	Pull-Low Register(R2712)	Pull-High Register(R2711)	SERIES RESISTOR(R2717)	Typical Voltage
14"(AMD)	30.0 K	100.0 K	40.2K	0.7615V
15"(AMD)	30.0 K	100.0 K	40.2K	0.4838V
14"(NV)	20.0 K	100.0 K	40.2K	0.55V
15"(NV)	20.0 K	100.0 K	40.2K	0.3888V
14"(UMA)	DY	100.0 K	40.2K	3.3V
15"(UMA)	DY	100.0 K	40.2K	0.9462V



DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC NPCE885

Size	Document Number	Rev
Custom	Husk/Petra	-4M

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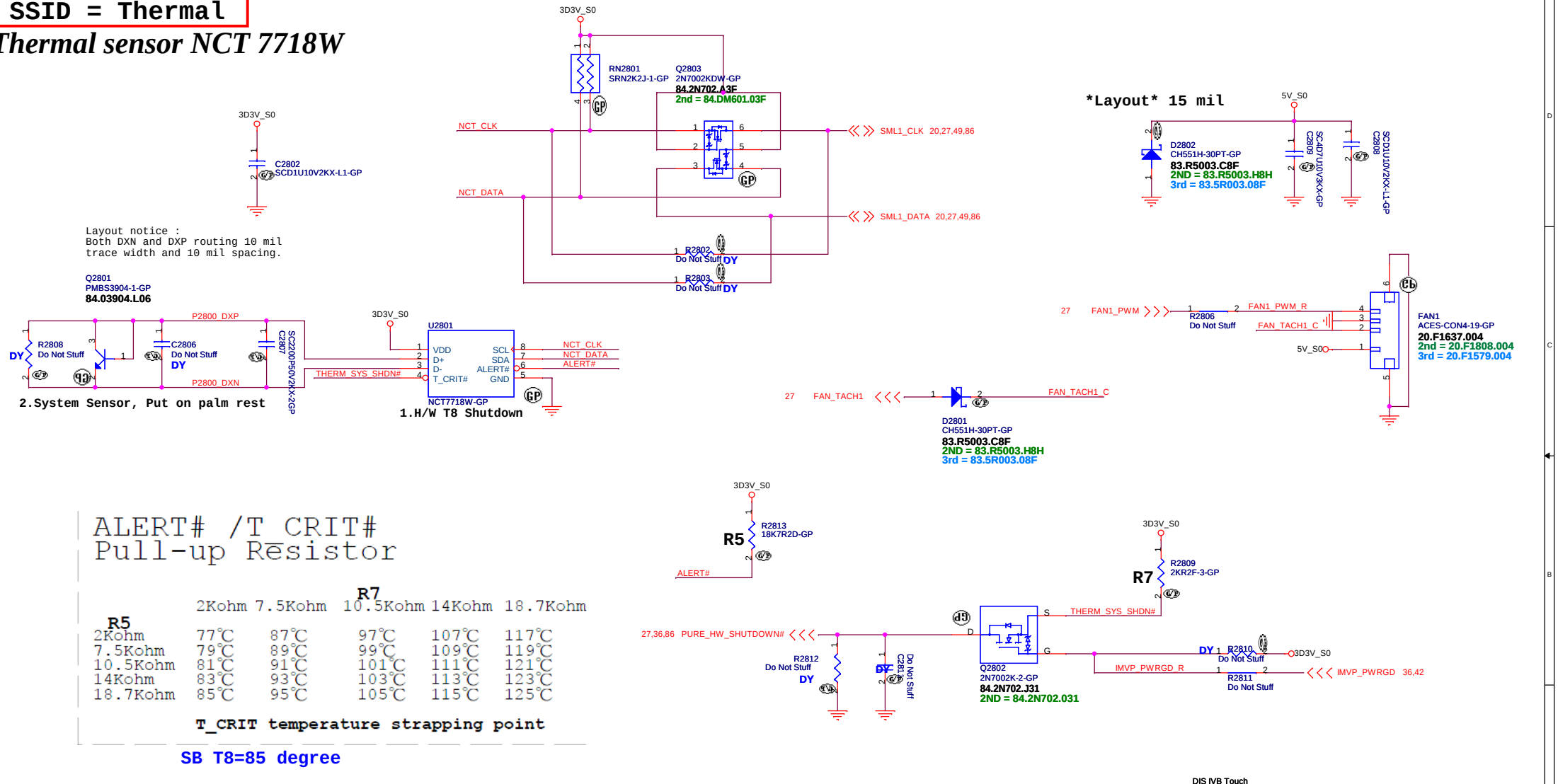
SSID = Thermal

Thermal sensor NCT 7718W



ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

SB T8=85 degree

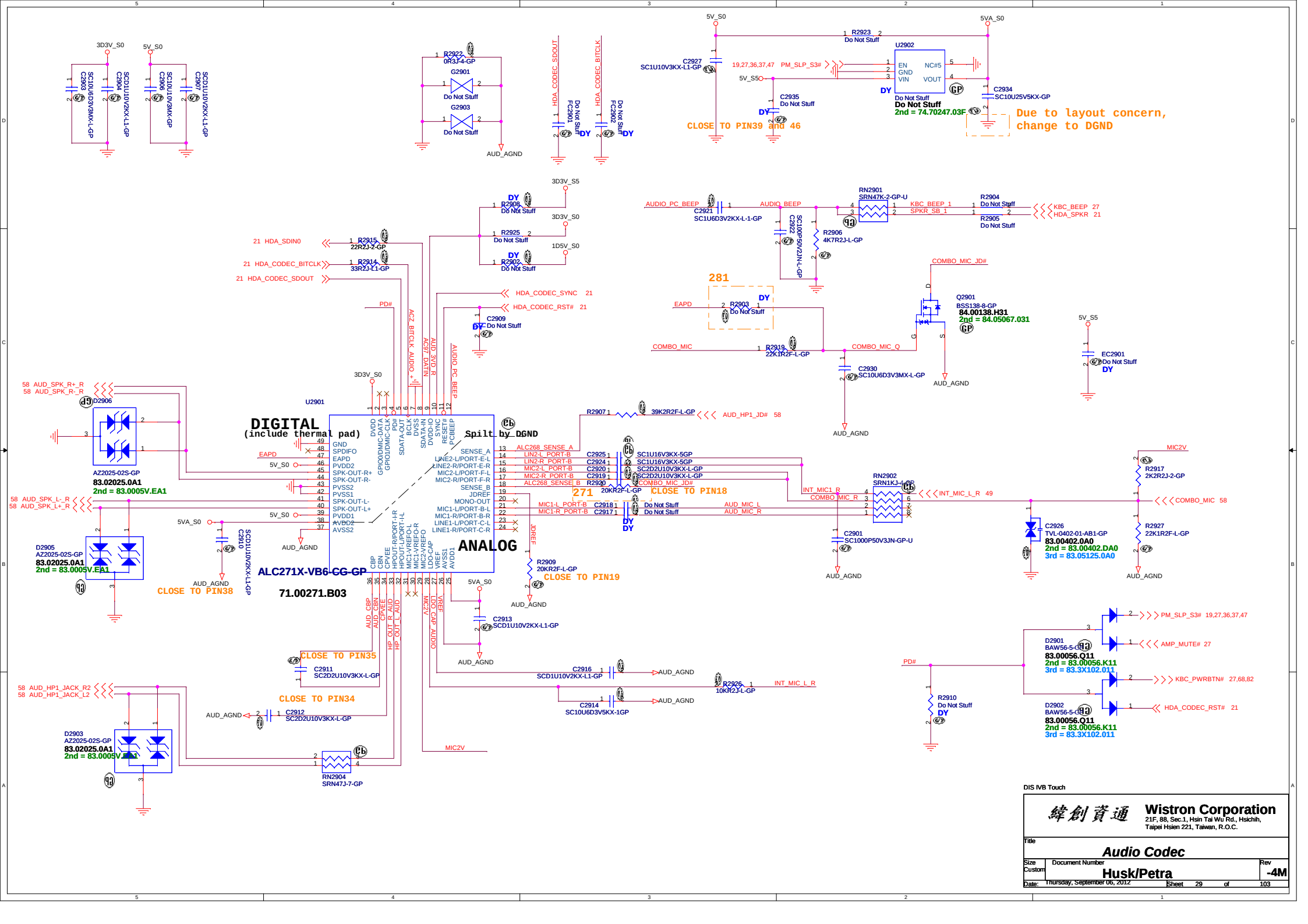
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal NCT7718*

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 28 of 103


DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB6-CG-GP
71.00271.B03
U2901
AZ2025-02S-GP
83.02025.0A1
2nd = 83.0005V.EA1
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
CLOSE TO PIN39 and 46
CLOSE TO PIN18
CLOSE TO PIN19
Due to layout concern, change to DGND
281
271
U2902
Do Not Stuff
2nd = 74.70247.03F
Q2901
BSS138-8-GP
84.00138.H31
2nd = 84.05067.031
RN2901
SRN47K-2-GP-U
RN2902
SRN1KJ-4-GP
RN2904
SRN47J-7-GP
D2901
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
3rd = 83.3X102.011
D2902
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
3rd = 83.3X102.011
C2926
TVL-0402-01-AB1-GP
83.00402.0A0
2nd = 83.00402.DA0
3rd = 83.05125.0A0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec
Husk/Petra
-4M
Thursday, September 06, 2012
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DIS IVB Touch

緯創資通 **Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio AMP

Size	Document Number	Rev
A3	**Husk/Petra**	**-4M**

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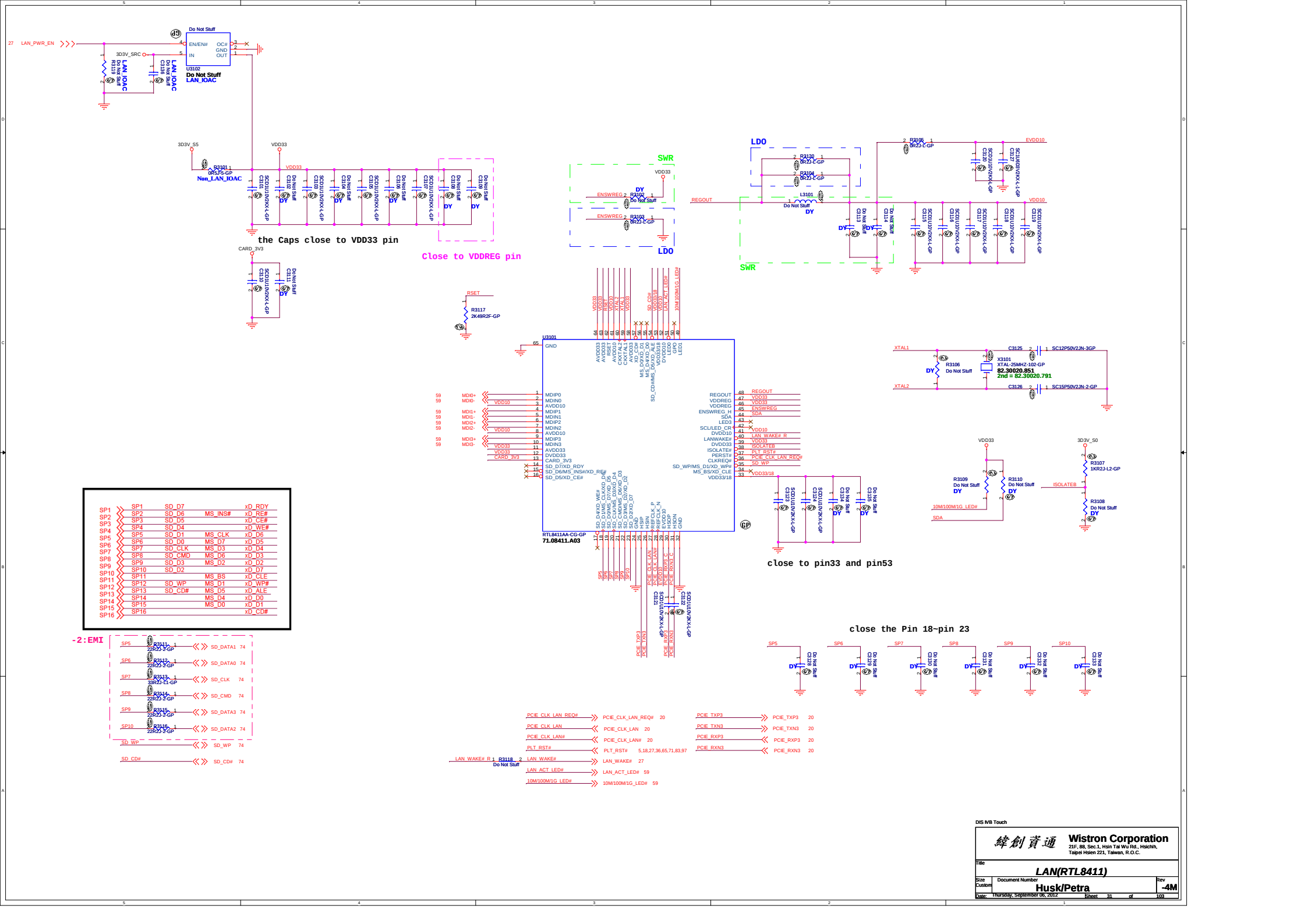


DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN(RTL8411)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 31 of 103

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5159 (CARD READER)***

Size	Document Number	Rev
Custom	**Husk/Petra**	**-4M**
Date: Thursday, September 06, 2012	Sheet 32 of 103	

(Blanking)

DIS IVB Touch

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size A4	Document Number **Husk/Petra**
Rev	**-4M**
Date: Thursday, September 06, 2012	Sheet 33 of 103

(Blanking)

DIS IVB Touch

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **Husk/Petra**	Rev: **-4M**
Date: Thursday, September 06, 2012	Sheet 34 of 103	

DIS IVB Touch

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

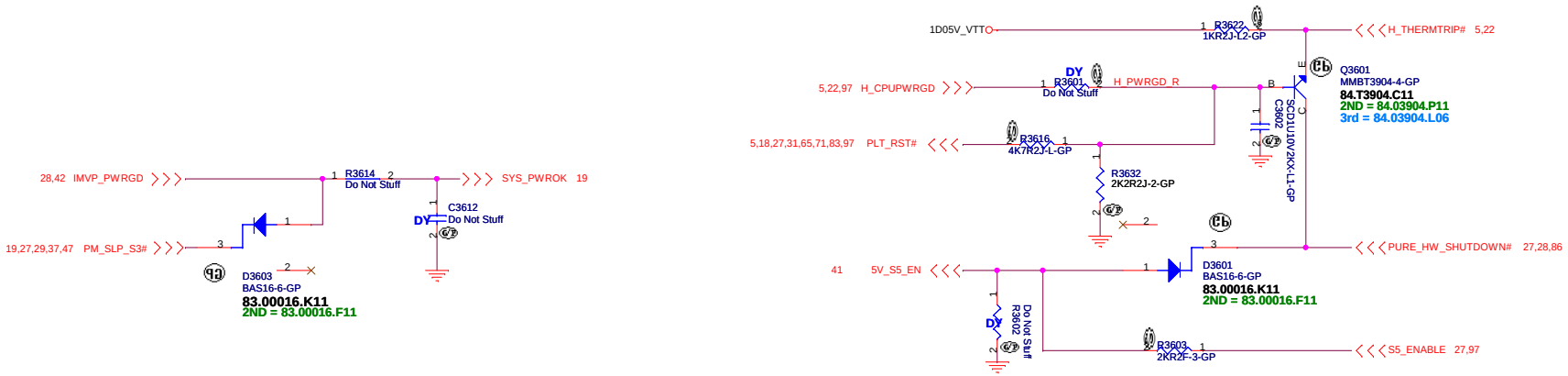
Title

USB 3.0 Controller

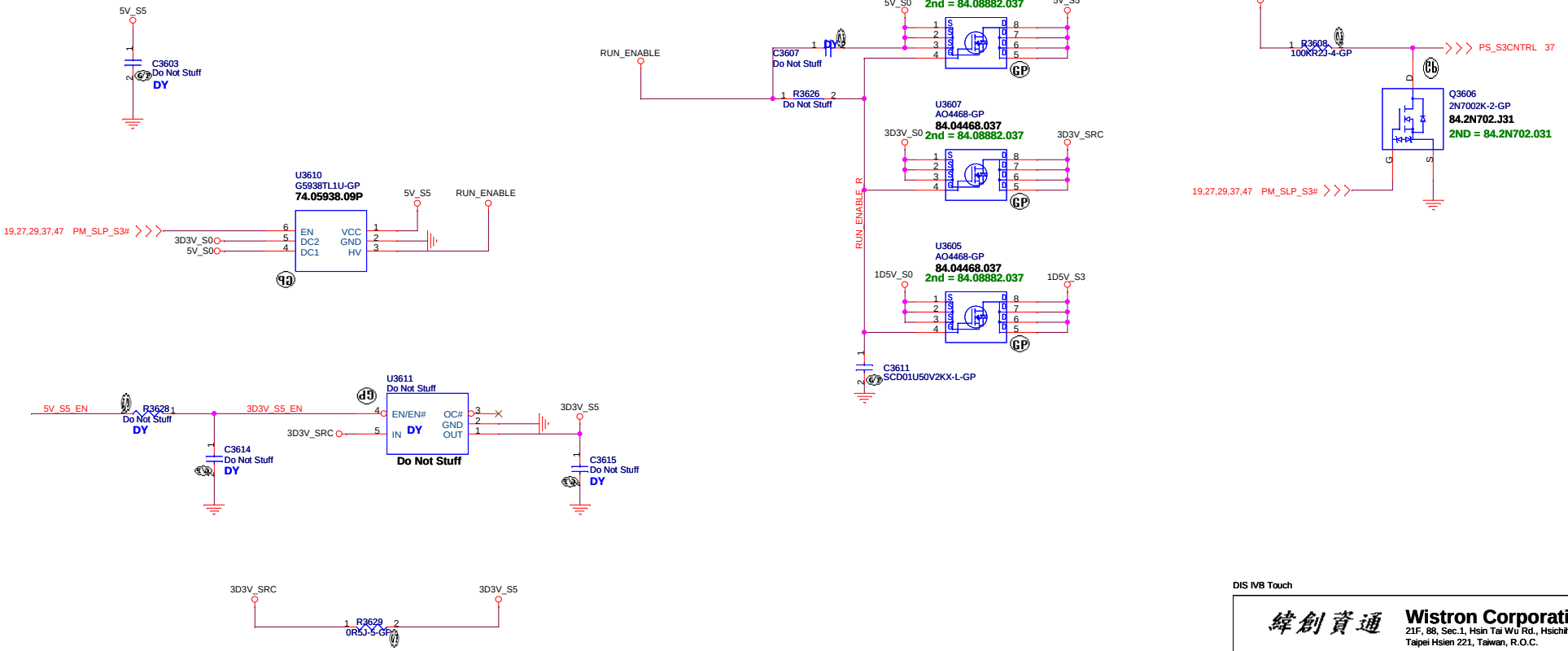
Size	Document Number	Rev
Custom	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 35 of 103

Power Sequence



ANNIE Run Power



DIS IVB Touch

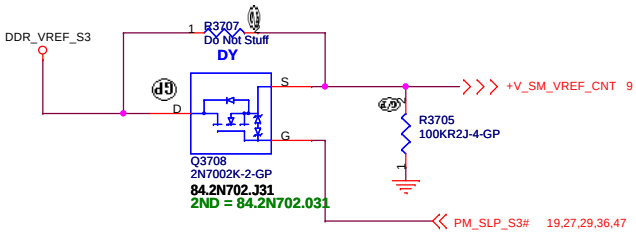
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

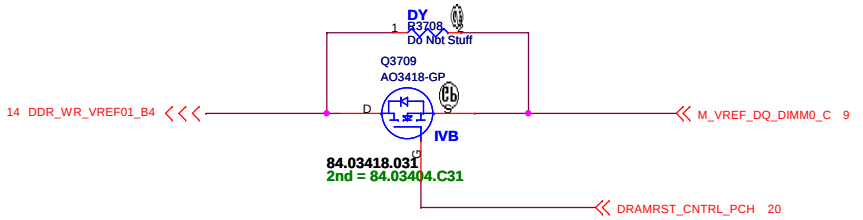
Title: **Power Plane Enable**

Size	Document Number	Rev
Custom	Husk/Petra	-4M

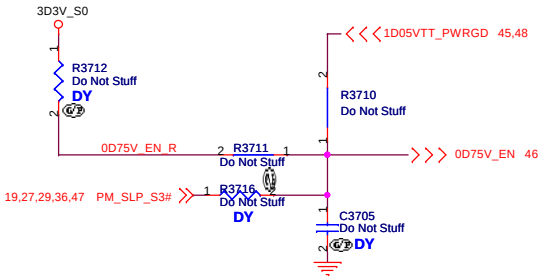
Date: Thursday, September 06, 2012 Sheet 36 of 103

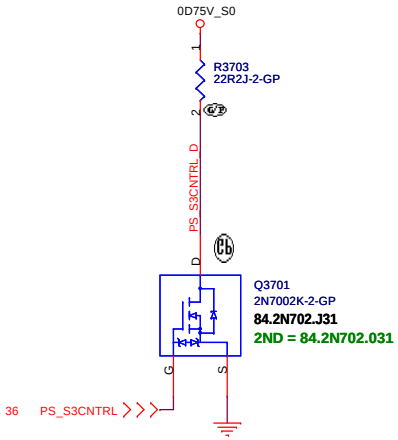
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

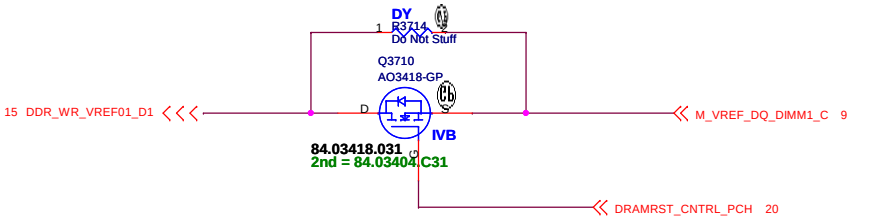




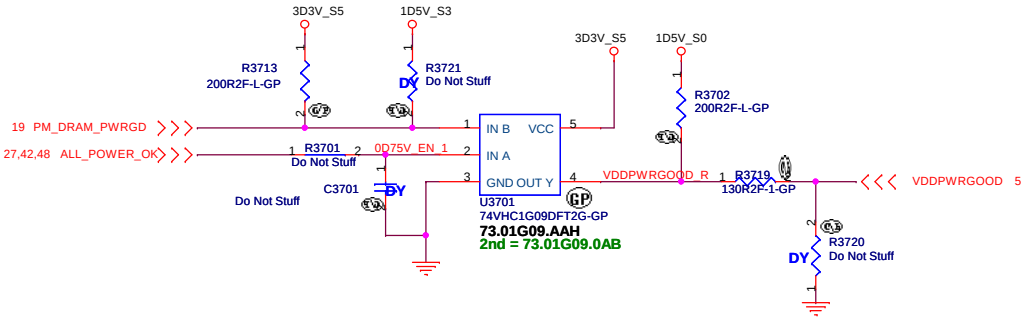
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



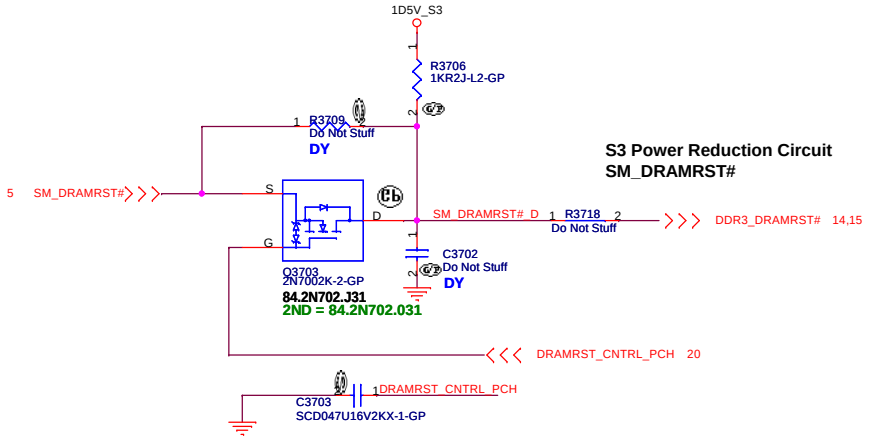




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



S3 Power Reduction Circuit
SM_DRAMRST#

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ADAPTER***		
Size: A3	Document Number: **Husk/Petra**	Rev: **-4M**
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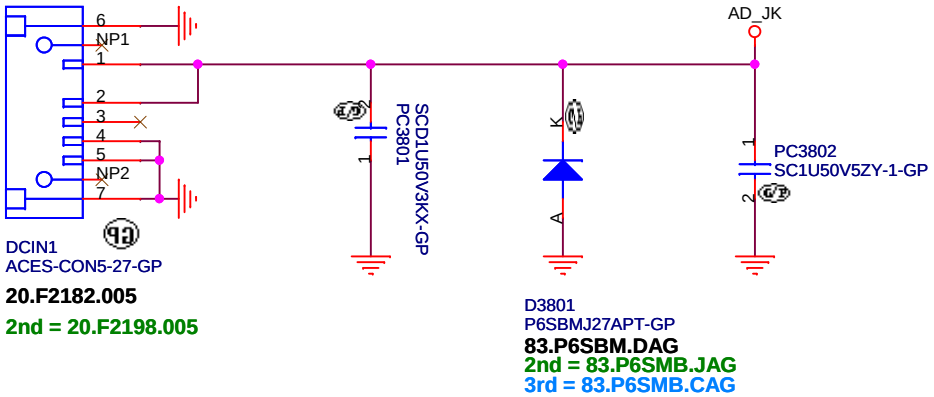
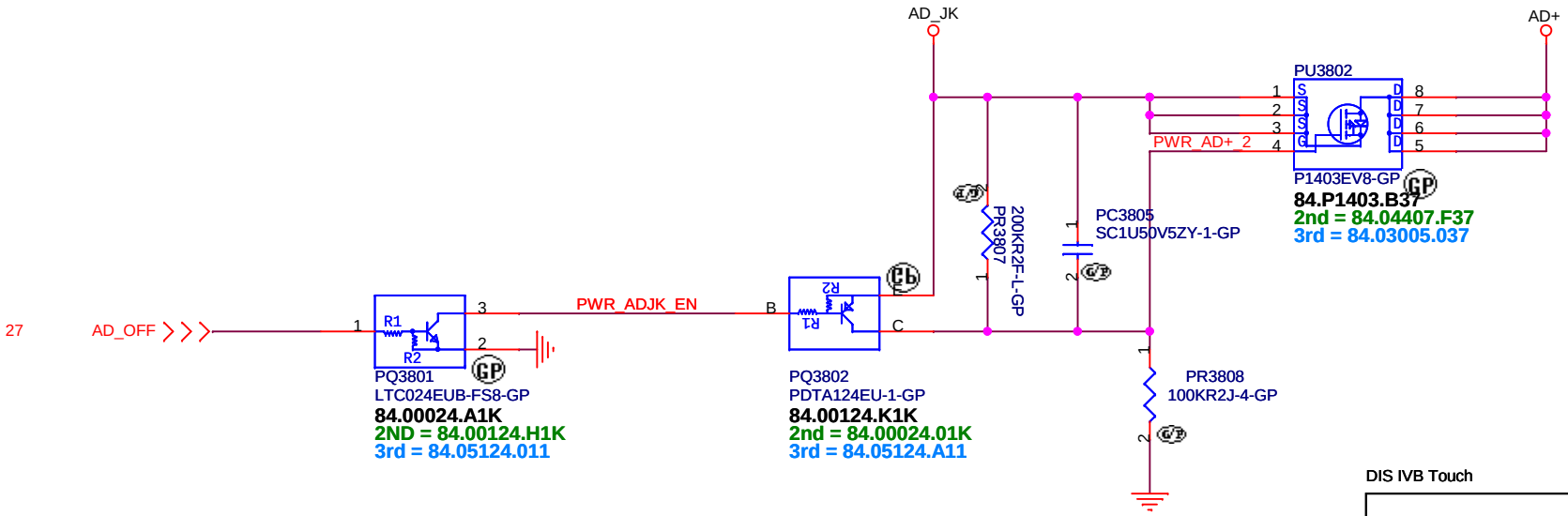
1Pin=3A





DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN JACK**

Size	Document Number	Rev
A4	Husk/Petra	-4M

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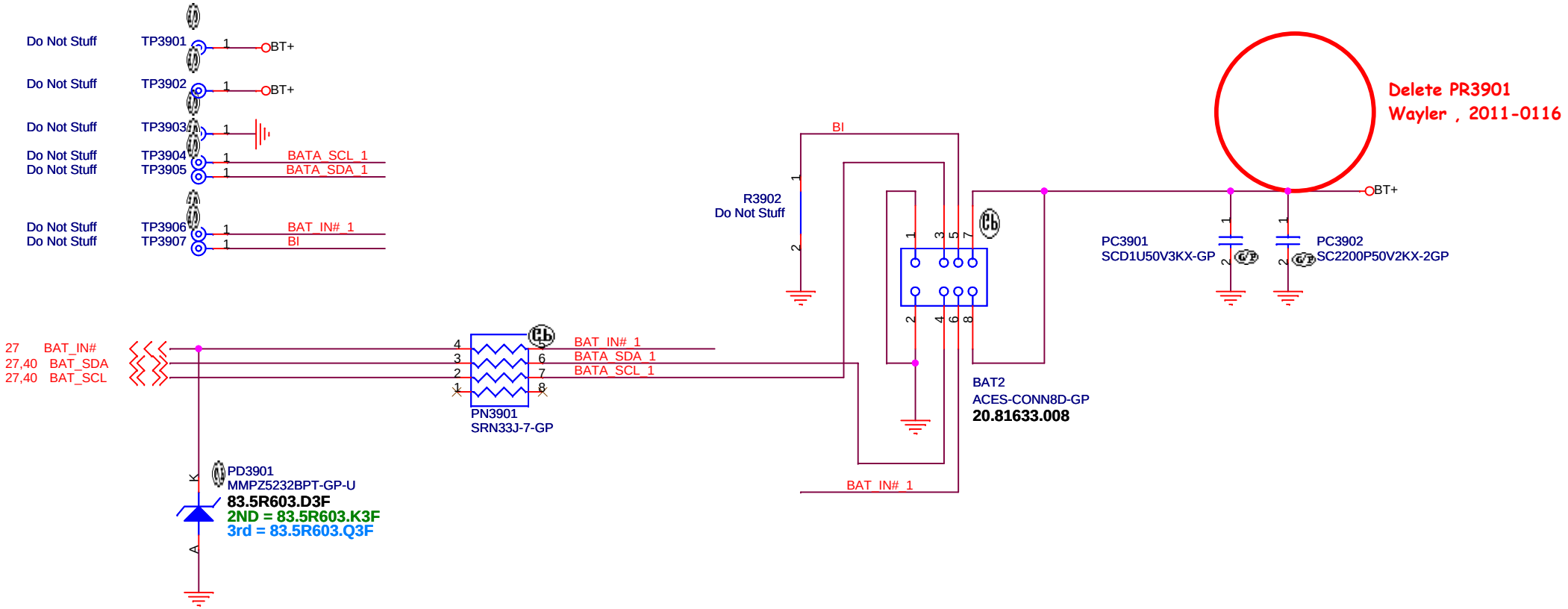
BATTERY CONNECTOR



DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BATT CONN***

Size	Document Number	Rev
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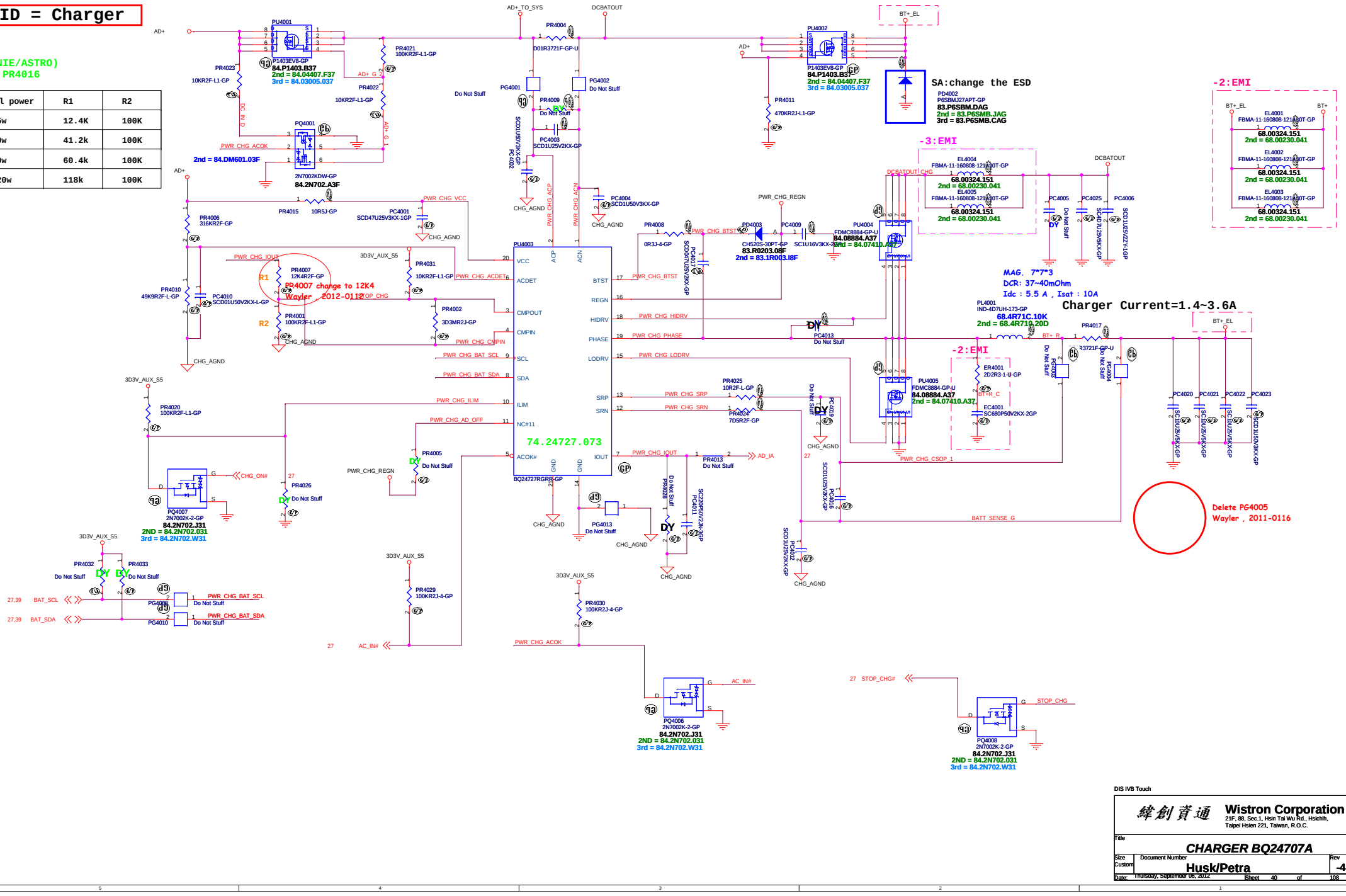
SSID = Charger

A8(ANNIE/ASTRO)
PR4014,PR4016

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



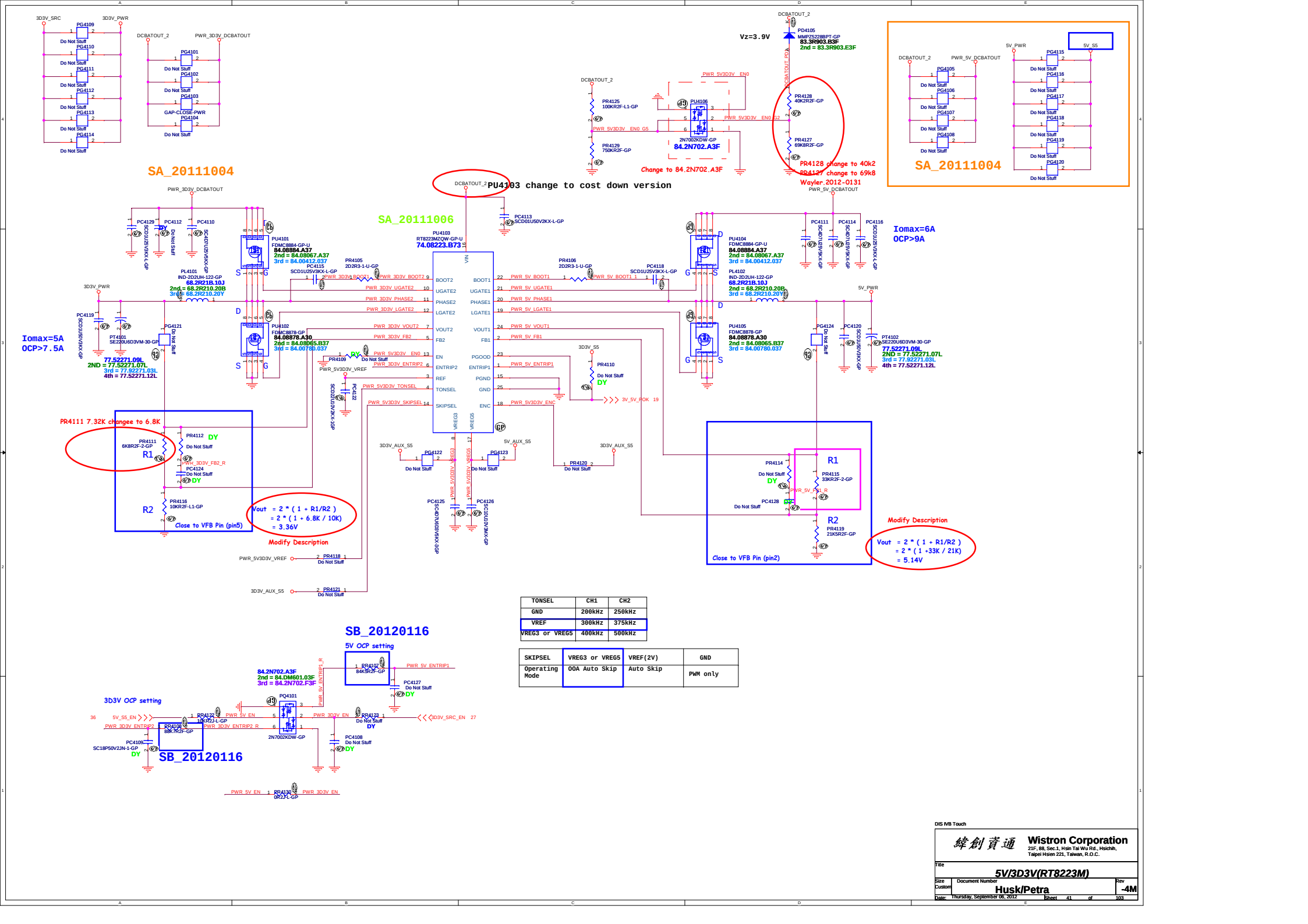
DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24707A

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 40 of 108


SA_20111004
SA_20111006
SB_20120116
PU4103 change to cost down version
Wayler_2012-0131
Vz=3.9V
PD4105
MMPZ5228BPT-GP
83.3R903.B3F
2nd = 83.3R903.E3F
PR4128 change to 40k2
PR4127 change to 69k8
Change to 84.2N702.A3F
84.2N702.A3F
Iomax=6A
OCP>9A
Iomax=5A
OCP>7.5A
PR4111 7.32K change to 6.8K
Vout = 2 * (1 + R1/R2)
= 2 * (1 + 6.8K / 10K)
= 3.36V
Close to VFB Pin (pin5)
Modify Description
Vout = 2 * (1 + R1/R2)
= 2 * (1 +33K / 21K)
= 5.14V
Close to VFB Pin (pin2)
5V OCP setting
3D3V OCP setting
84.2N702.A3F
2nd = 84.DM601.03F
3rd = 84.2N702.F3F
TONSEL | CH1 | CH2
GND | 200kHz | 250kHz
VREF | 300kHz | 375kHz
VREG3 or VREG5 | 400kHz | 500kHz
SKIPSEL | VREG3 or VREG5 | VREF(2V) | GND
Operating Mode | OOA Auto Skip | Auto Skip | PWM only
DIS IVB Touch
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
5V/3D3V(RT8223M)
Size Custom
Document Number
Husk/Petra
Rev
-4M
Date: Thursday, September 06, 2012
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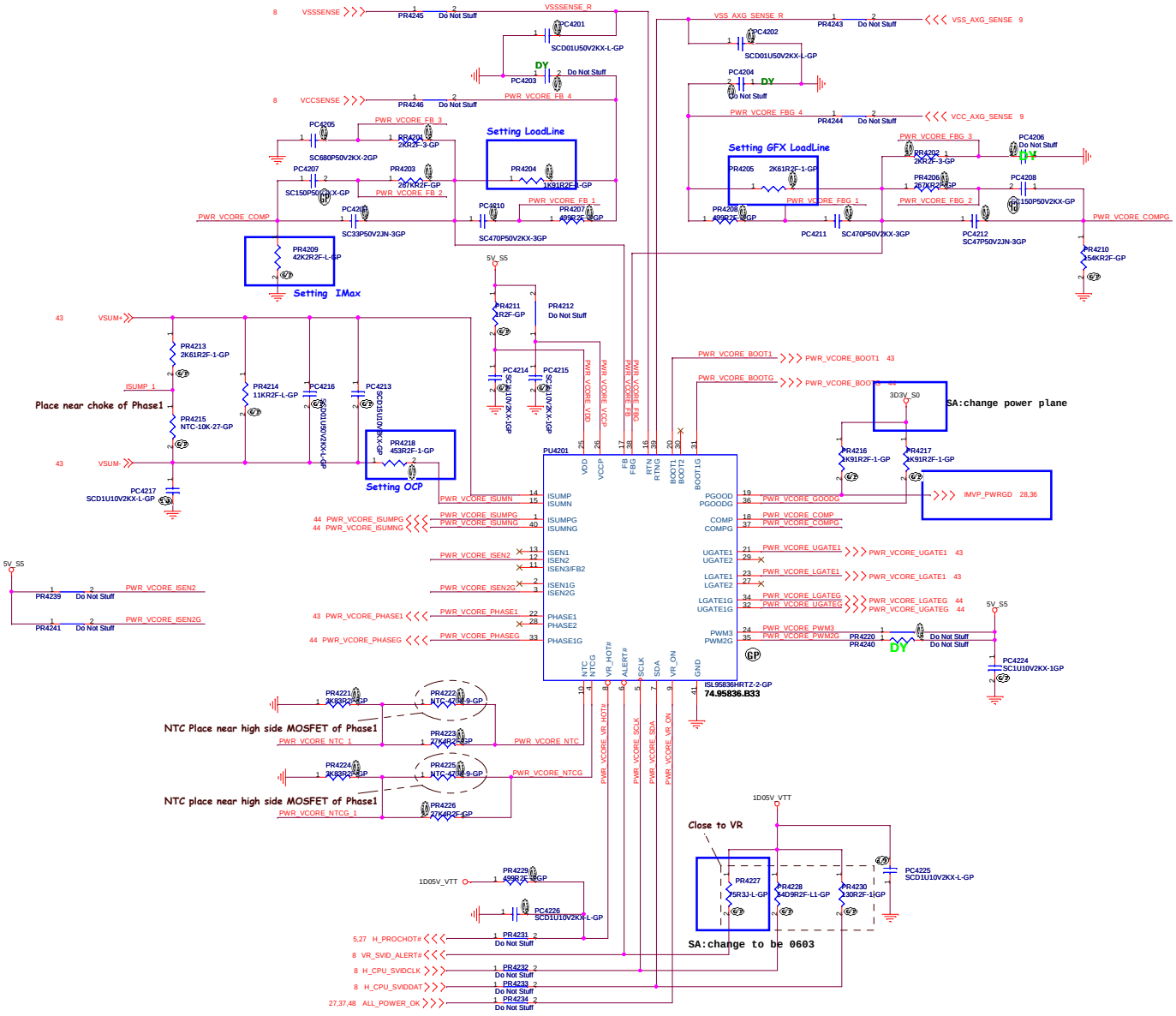
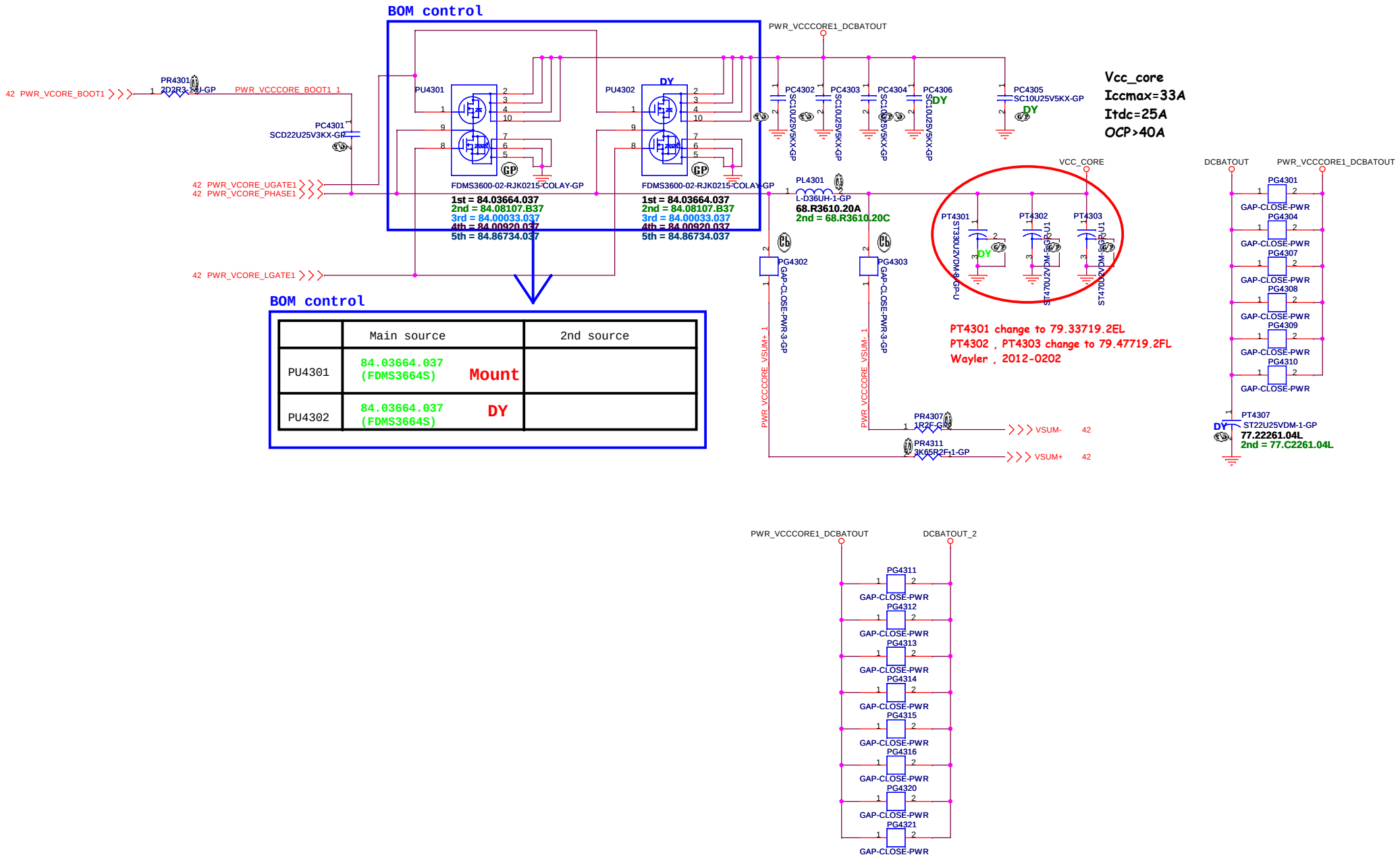
SSID = CPU.Regulator



DIS IVB Touch

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL95836_CPU_CORE(1/3)
Size: Custom	Document Number: Husk/Petra
Rev	-4M
Date: Thursday, September 06, 2012	Sheet 42 of 102



BOM control

	Main source	2nd source
PU4301	84.03664.037 (FDMS3664S) Mount	
PU4302	84.03664.037 (FDMS3664S) DY	

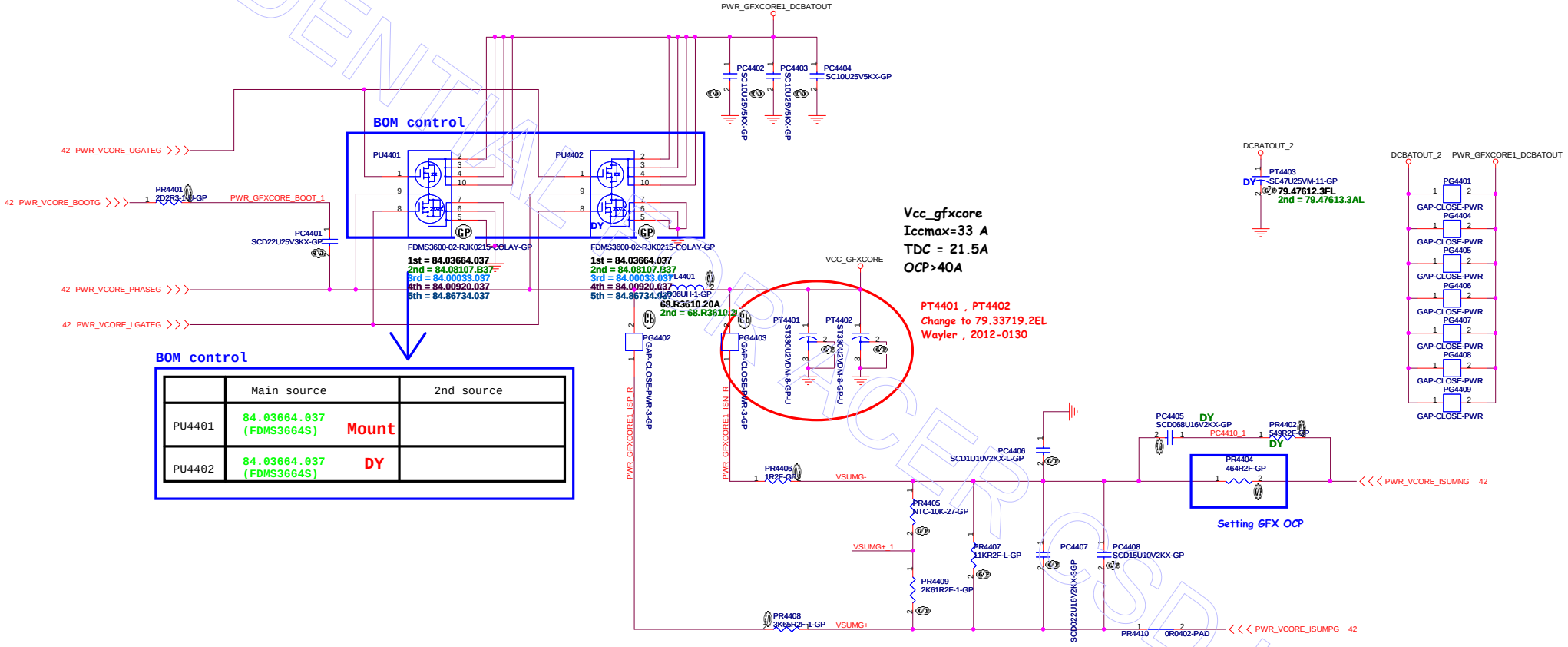
DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(2/3)

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Monday, September 17, 2012 | Sheet 43 of 102



BOM control

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S) Mount	
PU4402	84.03664.037 (FDMS3664S) DY	

DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

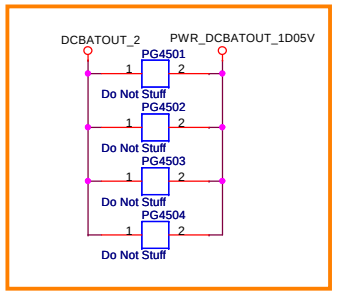
Title: ISL95836_CPU_CORE(3/3)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

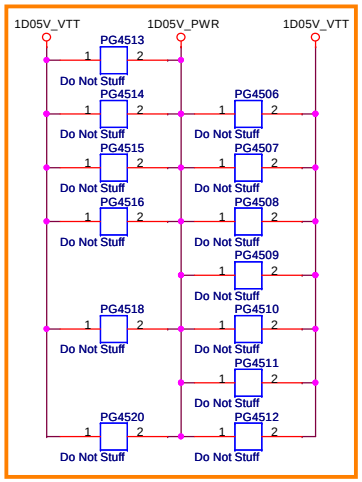
Date: Monday, September 17, 2012 | Sheet 44 of 102

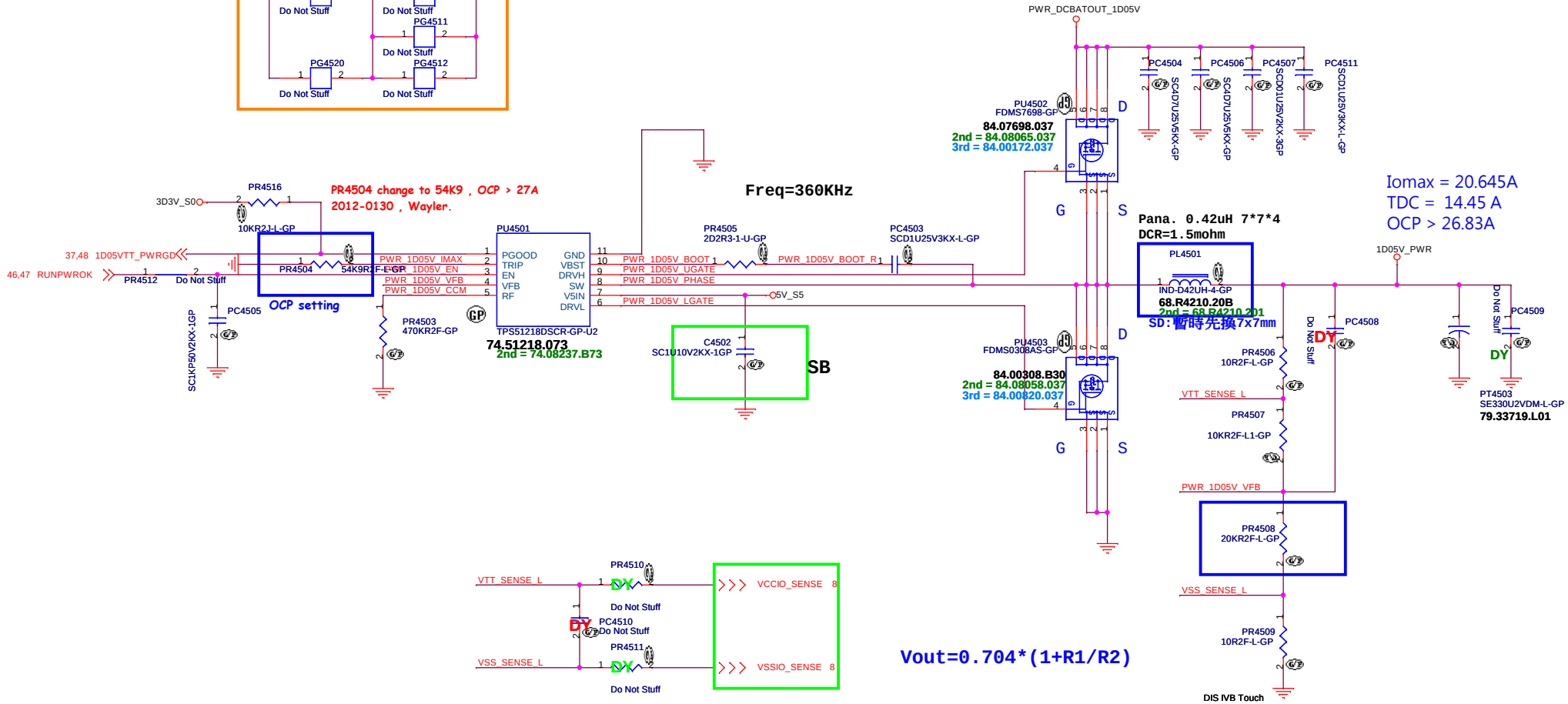
TPS51218D for 1D05V

SA_20111004



SA_20111013





緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DC to DC 1D05V(TPS51218D)	
Size A3	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 45 of 103	

SSID = PWR.Plane.Regulator_1p5v0p75v

Change power source

SA_20111004

SC:delete PT4601

RT8207L for 1D5V

OCP setting

PR4603 change to 8K87 , OCP>24A
2012 - 0111 - Wayler

Close to pin23

Close to pin23

20100728

Iomax=1A
OCP>1.5A

Close to output cap pin1, not inside of the output cap

PU4601 change to 74.08207.D73
2012 - 0111 - Wayler

PR4608 change to 30.9K
2012 - 0111 - Wayler

Close to PIN9

+0.75VS
Iomax: 1.2A

CYNTEC. 0.68uH 7*7*3
DCR= 5 ~ 5.5 mohm
Idc=15.5A, Isat=25A

IccMAX = 18.38A
IccTDC = 12.86A
OCP > 23.89A

SD:暫時先換7x7mm

Vout=0.75*(1+R1/R2)

DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

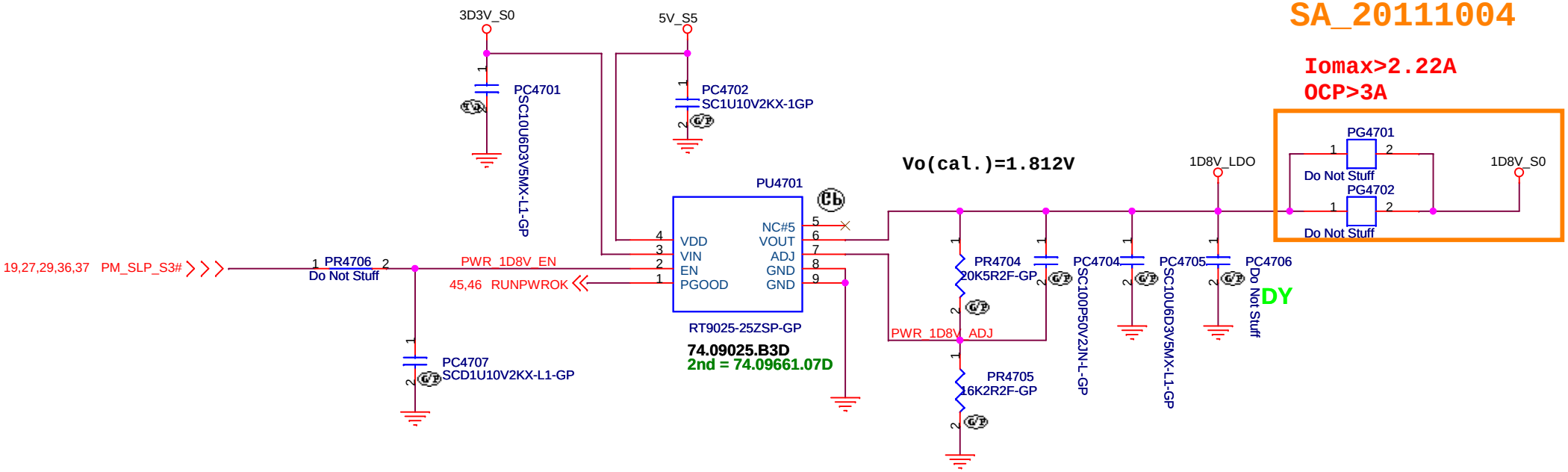
Title: RT8207

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 46 of 103

SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



DIS IVB Touch

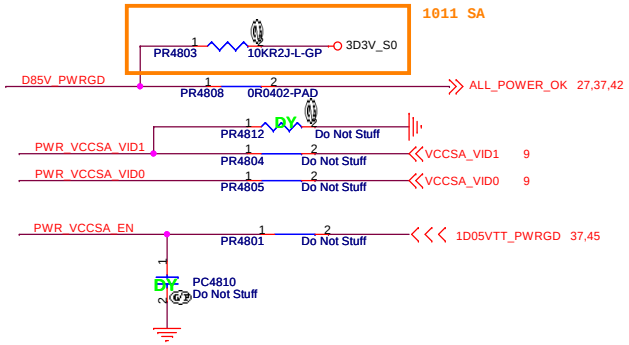
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LDO_1D8V(RT9025)***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 47 of 103

LDO G978 for VCCSA



D0, D1 V_O Selection Table

D0	D1	V_O MODE=0	V_O MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

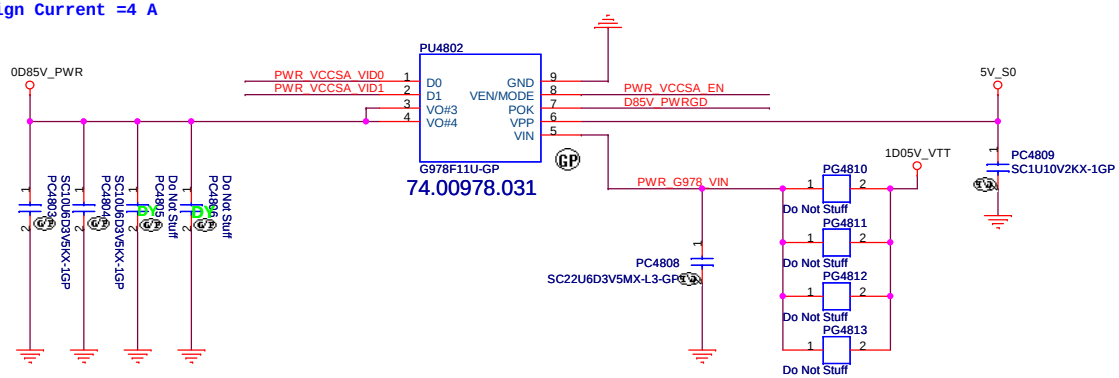
"x" means "don't care".

VEN/MODE Logic

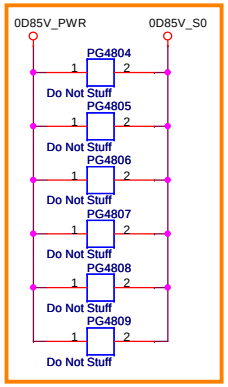
VEN/MODE (VPP=5V)	EN logic
<0.6V	0
>1.0V	1

VEN/MODE (VPP=5V)	MODE logic
<2.0V	0
>2.6V	1

Design Current =4 A



1011 SA



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

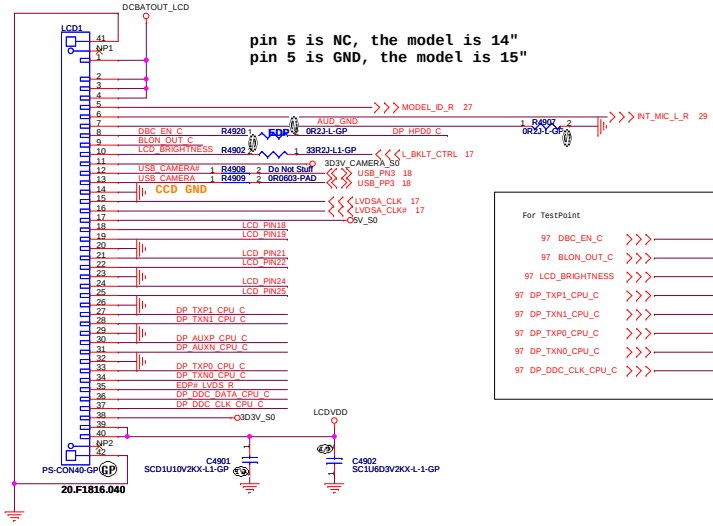
Title: VCCSA LDO G978

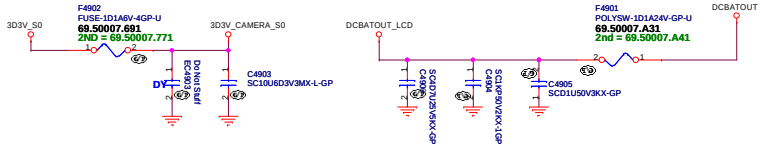
Size: A3 | Document Number: Husk/Petra | Rev: -4M

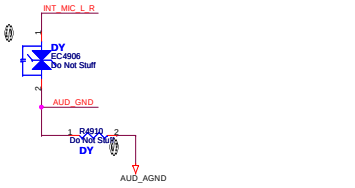
Date: Thursday, September 06, 2012 | Sheet 48 of 103

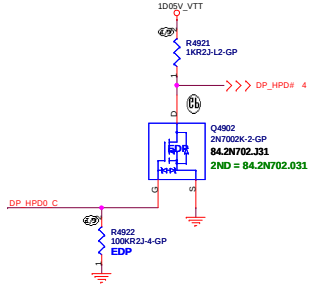
SSID = VIDEO

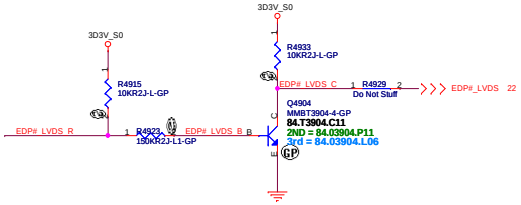
pin 5 is NC, the model is 14"
pin 5 is GND, the model is 15"





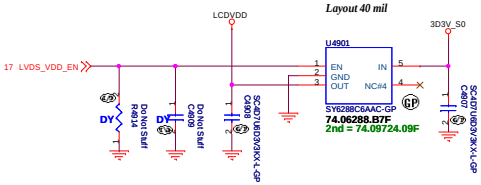


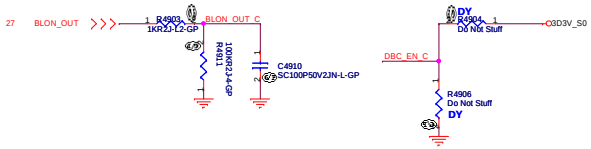


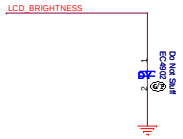


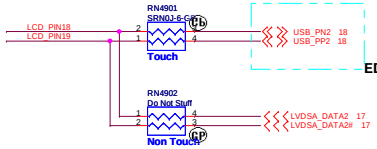
EDP: pin35 NC
LVDS: pin35 GND

Layout 40 mil

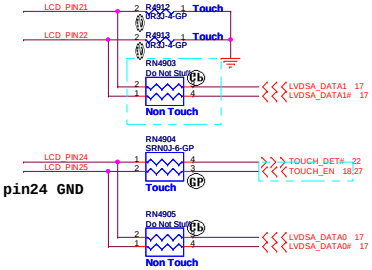


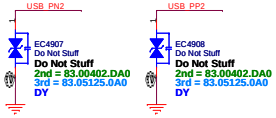






EDP:pin24 GND





DIS IVB Touch

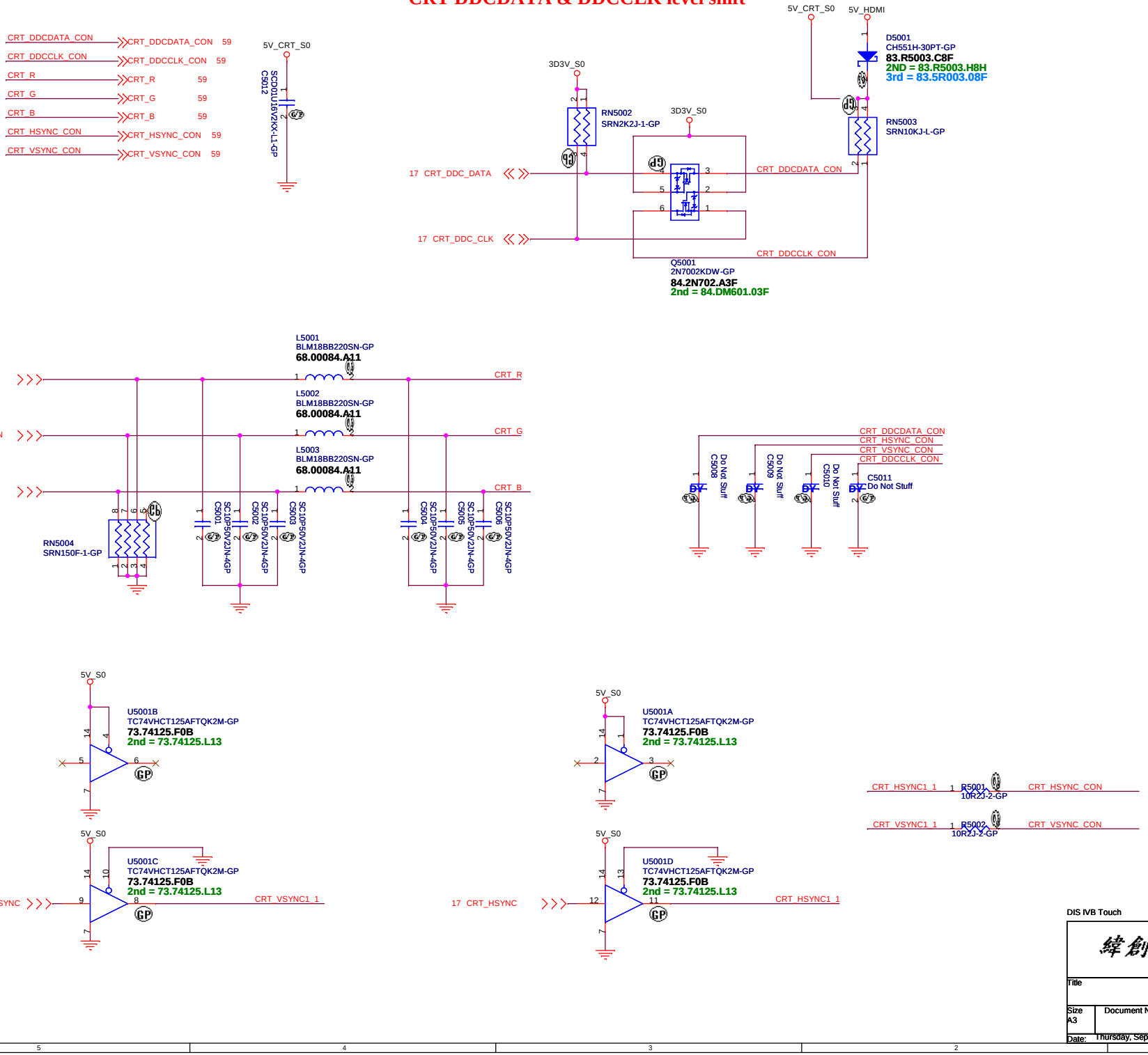
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD Connector**

Size	Document Number	Rev
A2	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 49 of 103

CRT DDCDATA & DDCCLK level shift



DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 50 of 103

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

Close to HDMI Connector

change = DIS:499 ohm
Fist = UMA Muxless:680 ohm

17 HDMI_CLK_R#
17 HDMI_CLK_R
17 HDMI_DATA0_R#
17 HDMI_DATA0_R
17 HDMI_DATA1_R#
17 HDMI_DATA1_R
17 HDMI_DATA2_R#
17 HDMI_DATA2_R

HDMI_DATA2_R#
HDMI_DATA2_R
HDMI_DATA0_R#
HDMI_DATA0_R
HDMI_DATA1_R
HDMI_DATA1_R#
HDMI_CLK_R
HDMI_CLK_R#

RN5114
SRN499F-GP

RN5115
SRN499F-GP

HDMI_PLL_GND

Q5105
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031

5V_S0

HDMI1
SKT-HDMI23-45-GP
22.10296.631
2nd = 22.10296.821

HDMI_DATA2_R
HDMI_DATA2_R#
HDMI_DATA1_R
HDMI_DATA1_R#
HDMI_DATA0_R
HDMI_DATA0_R#
HDMI_CLK_R
HDMI_CLK_R#
DDC_CLK_HDMI
DDC_DATA_HDMI
5V_HDMI

5V_HDMI
5V_S0
F5101
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771

HPD_HDMI_CON
R5111
150KR2J-L1-GP
HDMI_HPD_B

3D3V_S0
Q5102
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.P11
3rd = 84.03904.L06

R5110
Do Not Stuff

HDMI_HPD_E
R5129
Do Not Stuff
HDMI_PCH_DET 17

R5112
10KR2J-L-GP

D5103
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
3rd = 83.3X102.011

5V_S0_D1
5V_S0_D2
5V_S0

RN5102
SRN2K2J-1-GP

Q5106
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F

3D3V_S0

17 PCH_HDMI_CLK
17 PCH_HDMI_DATA

DDC_CLK_HDMI
DDC_DATA_HDMI

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 51 of 103

LED BACKLIGHT CONVERTER POWER

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***eDP***		
Size: A3	Document Number: **Husk/Petra**	Rev: **-4M**
Date: Thursday, September 06, 2012	Sheet 52 of 103	

(Blanking)

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 53 of 103

(Blanking)

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

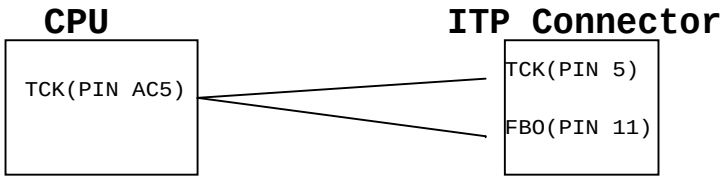
Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close ITP connector 500 mil (max), others place near CPU side.



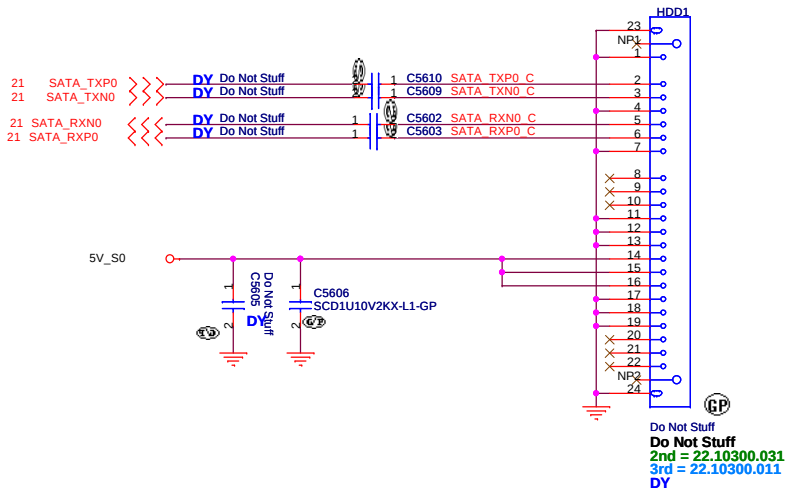
DIS IVB Touch

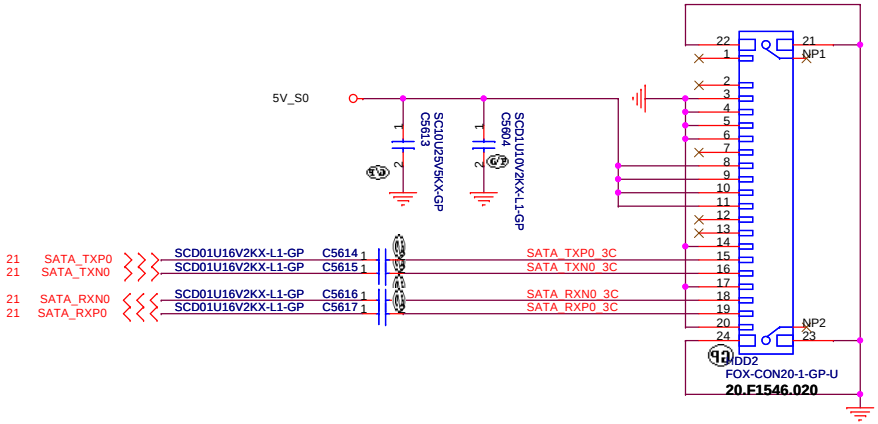
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ITP*		
Size: A4	Document Number: **Husk/Petra**	Rev: **-4M**
Date: Thursday, September 06, 2012	Sheet 55 of 103	

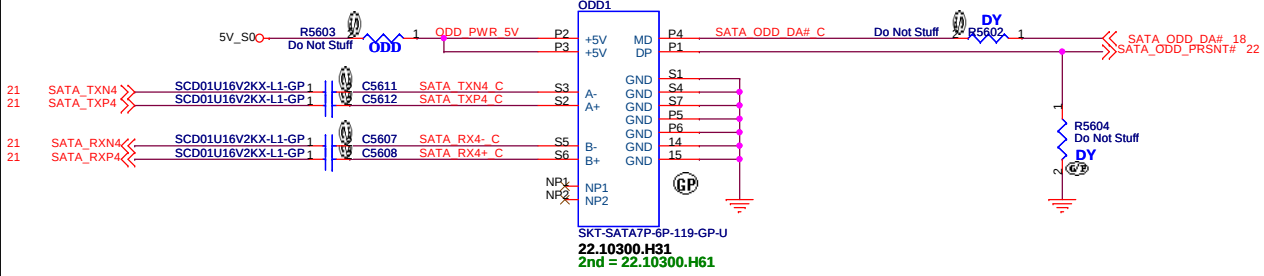
SSID = SATA

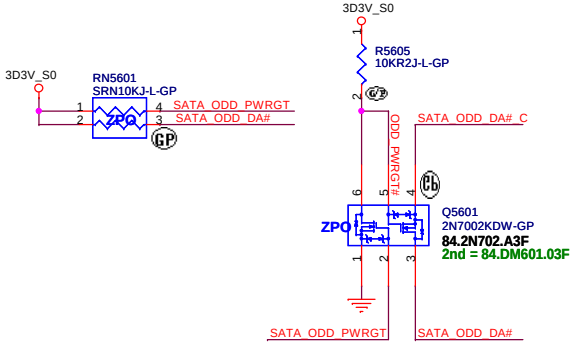
SATA HDD Connector



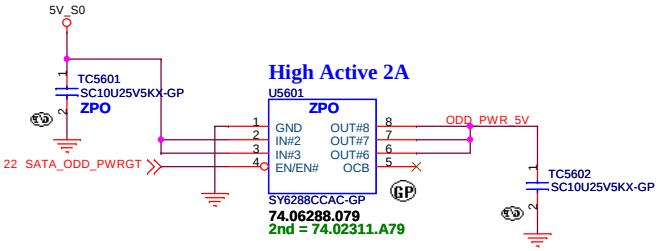


ODD Connector





SATA Zero Power ODD



DIS IVB Touch

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD/ODD		
Size: A3	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 56 of 103	

DIS IVB Touch

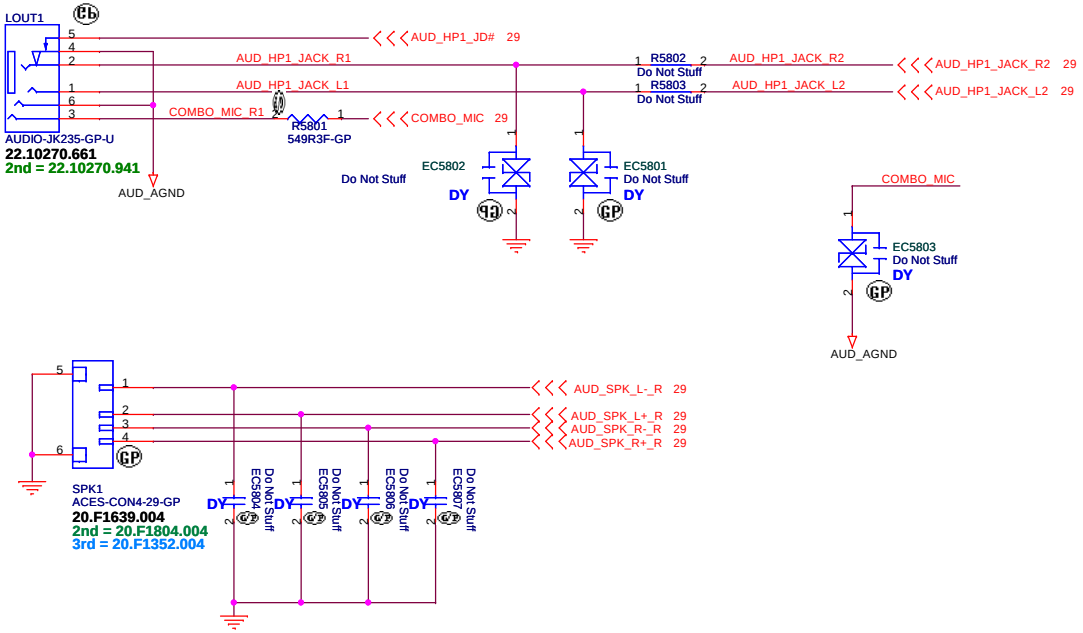
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***E-SATA/USB CHARGER***

Size	Document Number	Rev
A3	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 57 of 103

SSID = AUDIO

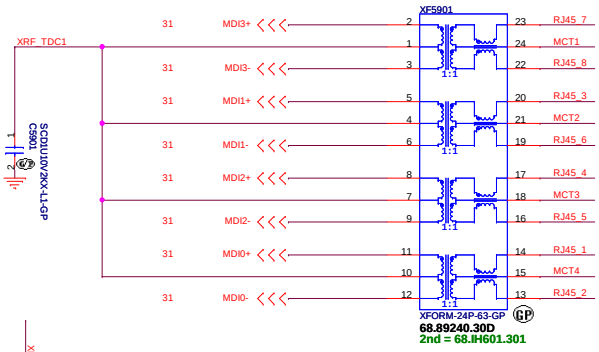


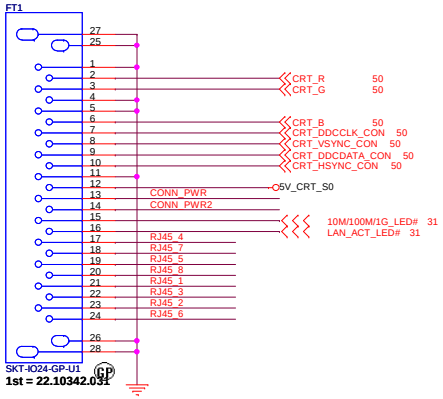
DIS IVB Touch

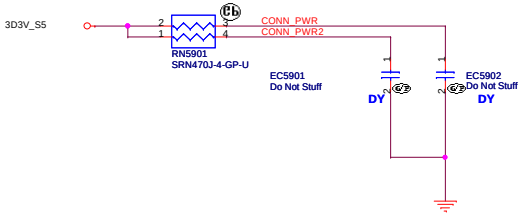
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

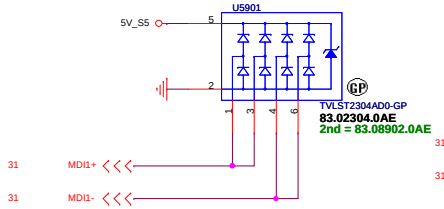
Title: ***Audio Jack***		
Size: A3	Document Number: **Husk/Petra**	Rev: **-4M**
Date: Thursday, September 06, 2012	Sheet 58 of 103	

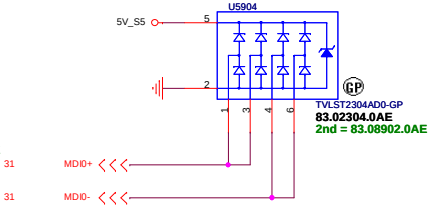
SSID = LAN

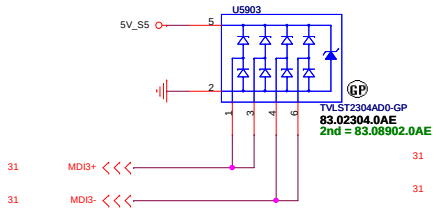


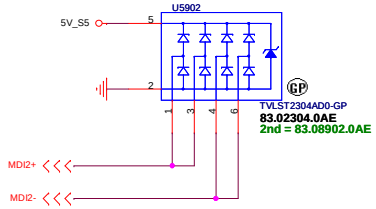


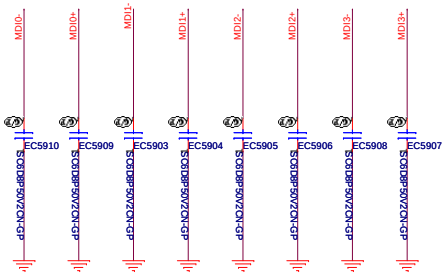


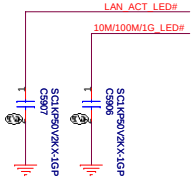


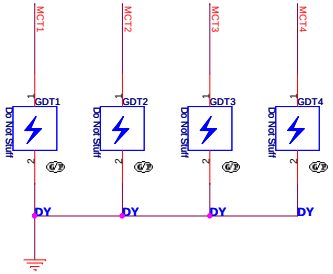


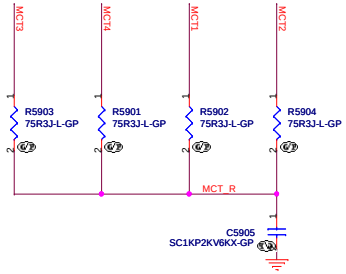












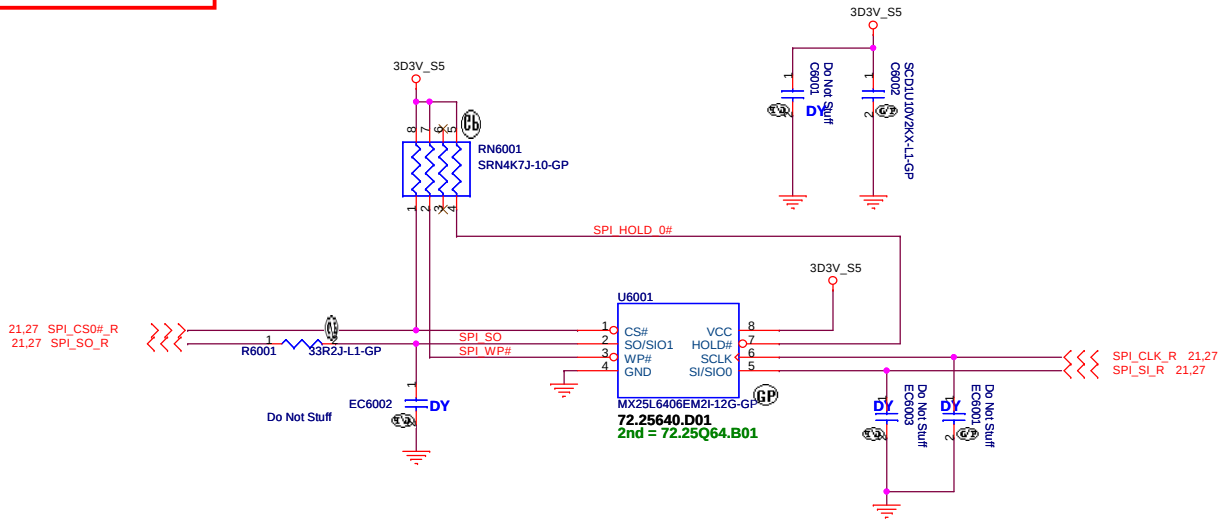
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

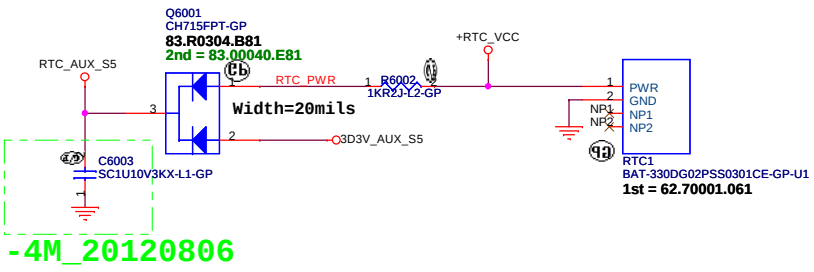
Title: **LAN CONNECTOR**

Size	Document Number	Rev
Custom	Husk/Petra	-4M
Date: Monday, November 12, 2012	Sheet 59 of 103	

SSID = Flash.ROM



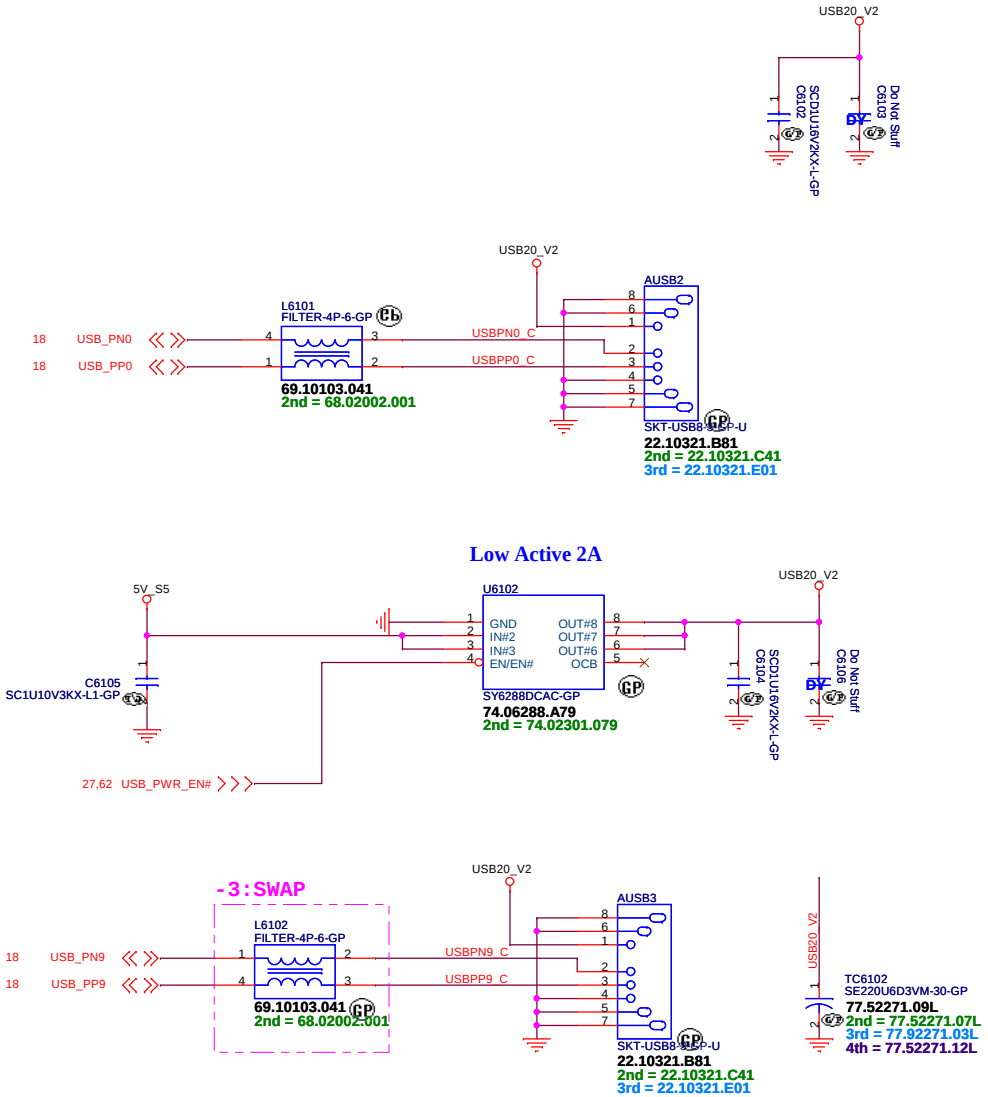
SSID = RTC



DIS IVB Touch

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Flash/RTC*		
Size: Custom	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 60 of 103	

SSID = USB



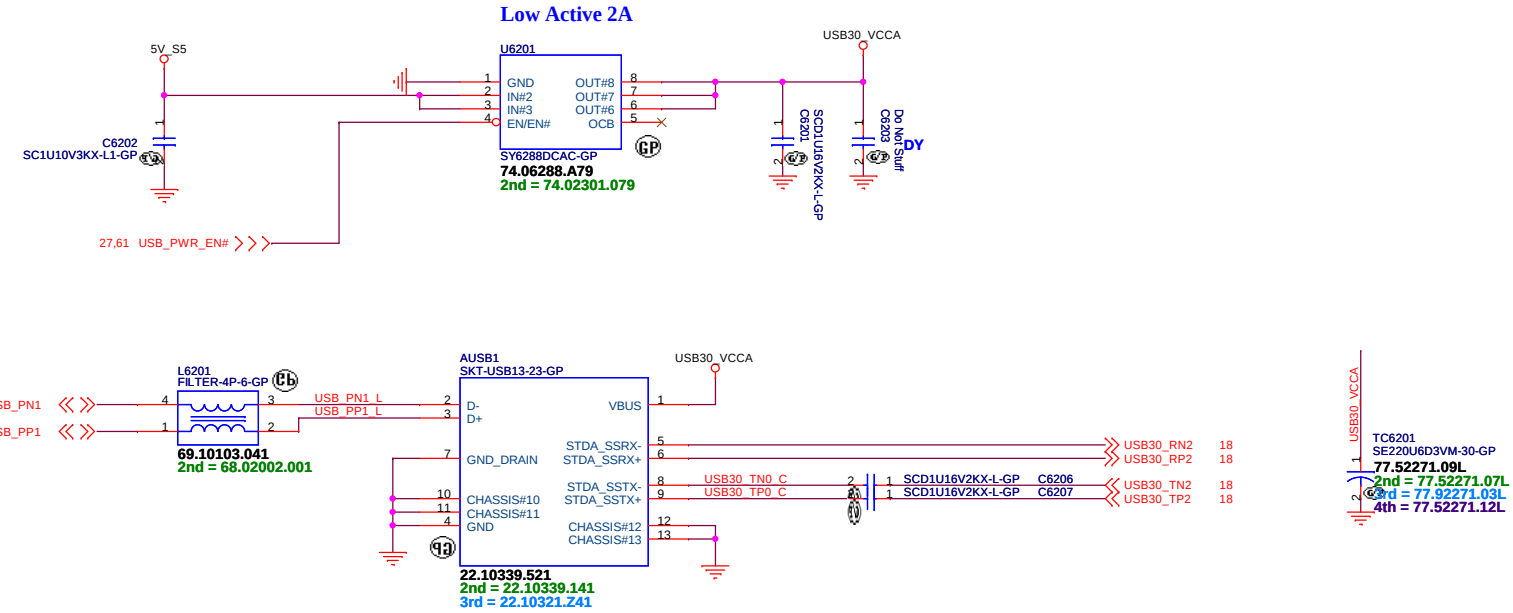
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 13, 2012 Sheet 61 of 103



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0 Port

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 13, 2012 | Sheet 62 of 103

SSID = User.Interface

Bluetooth Module conn.

ANNIE Bluetooth Module

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 63 of 103

DIS IVB Touch

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

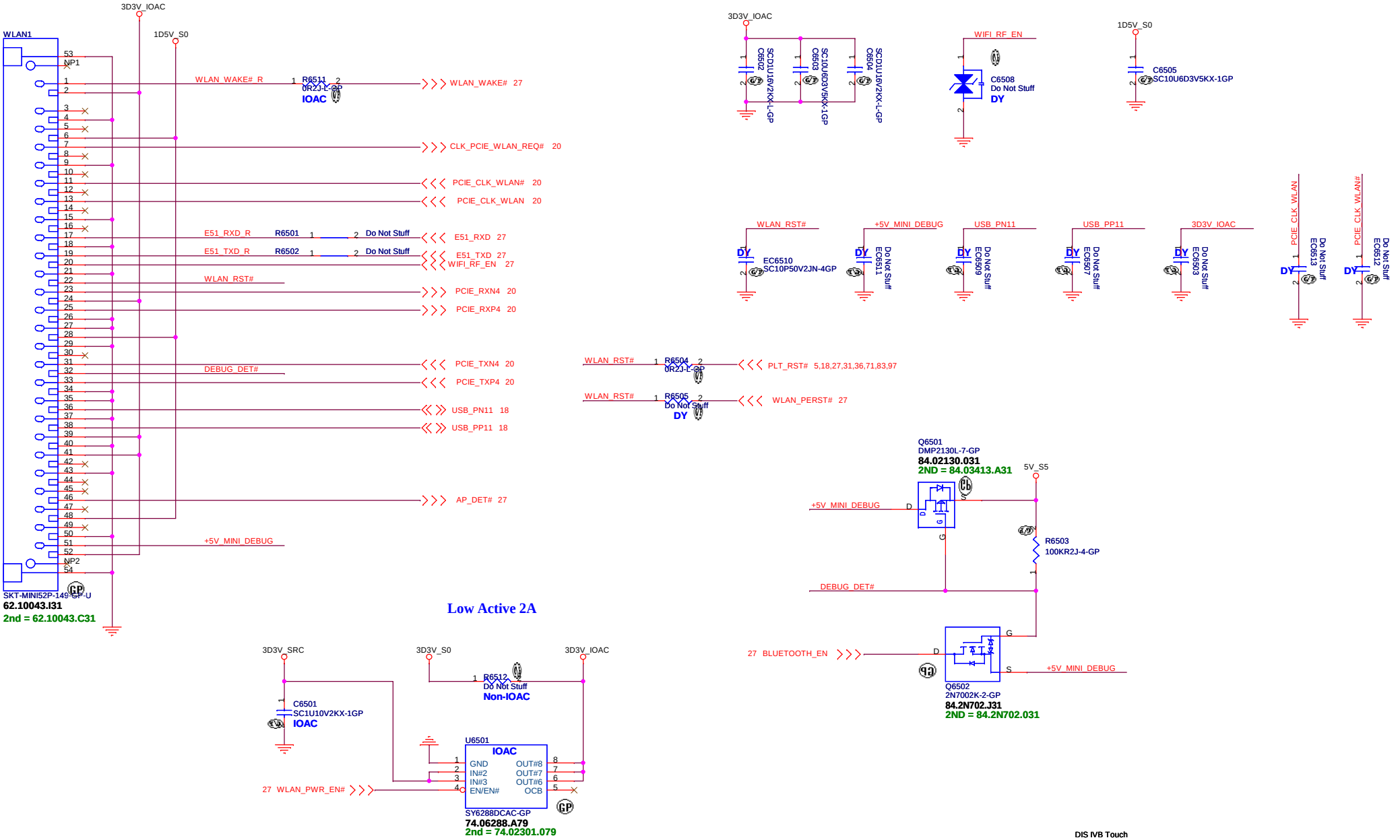
RESERVED

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 64 of 103

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Friday, December 21, 2012 Sheet 65 of 103

SSID = Wireless

Mini Card Connector(WWAN)

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***WWAN Connector***		
Size: A4	Document Number: **Husk/Petra**	Rev: **-4M**
Date: Thursday, September 06, 2012	Sheet 66 of 103	

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DIS IVB Touch

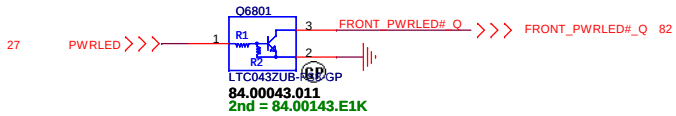
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

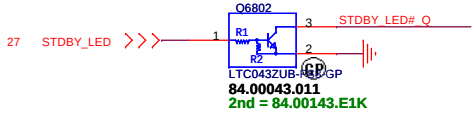
Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 67 of 103

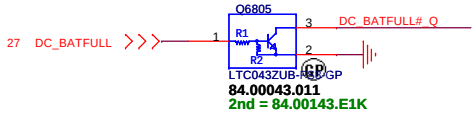
Power button LED



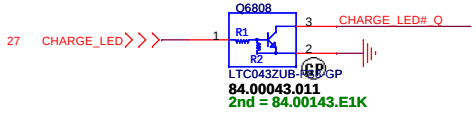
Power STDBY_LED

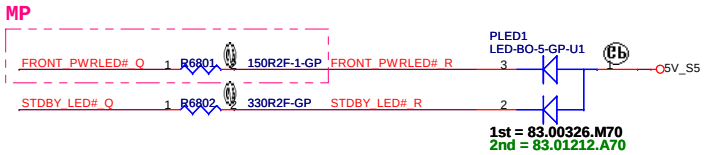


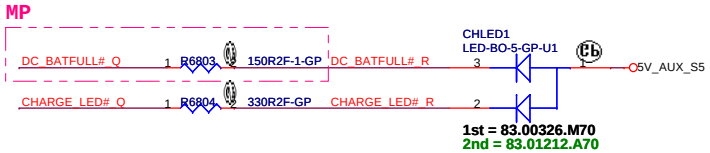
Battery LED2(DC_BATFULL)

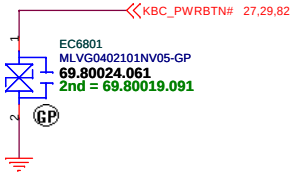


Battery LED1(CHARGE)









DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

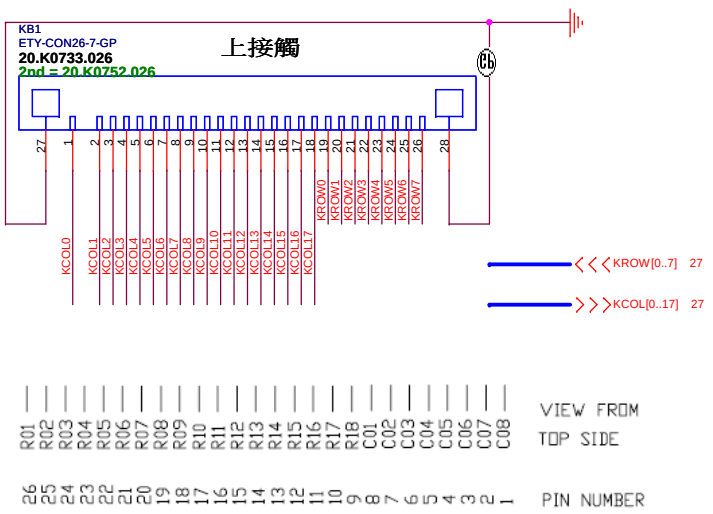
Title: ***LED Bard/Power Button***

Size	Document Number	Rev
Custom	Husk/Petra	-4M

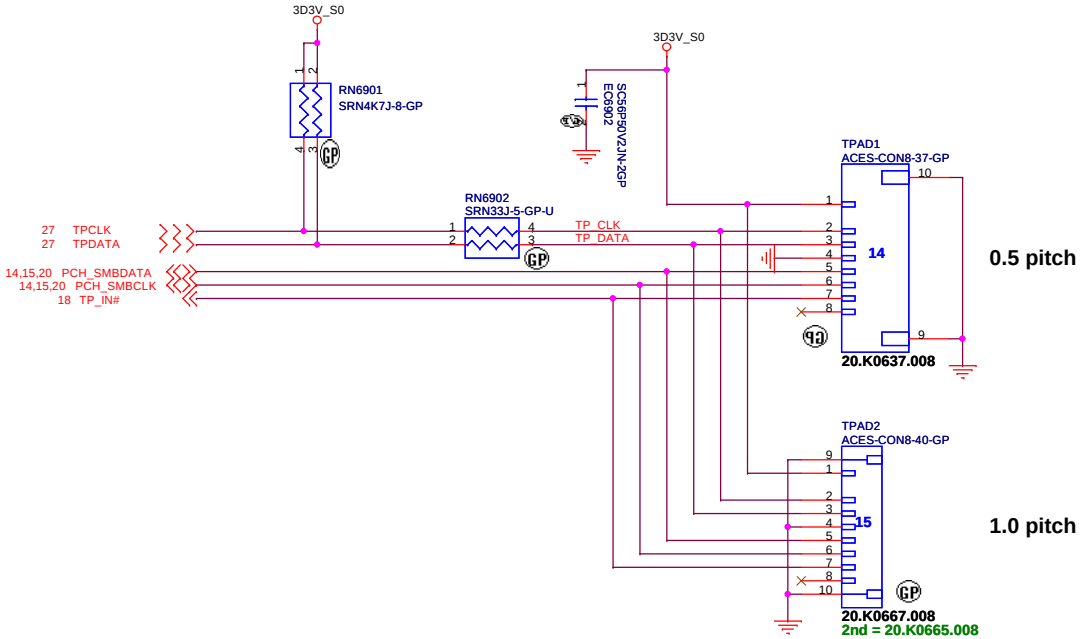
Date: Thursday, September 06, 2012 Sheet 68 of 103

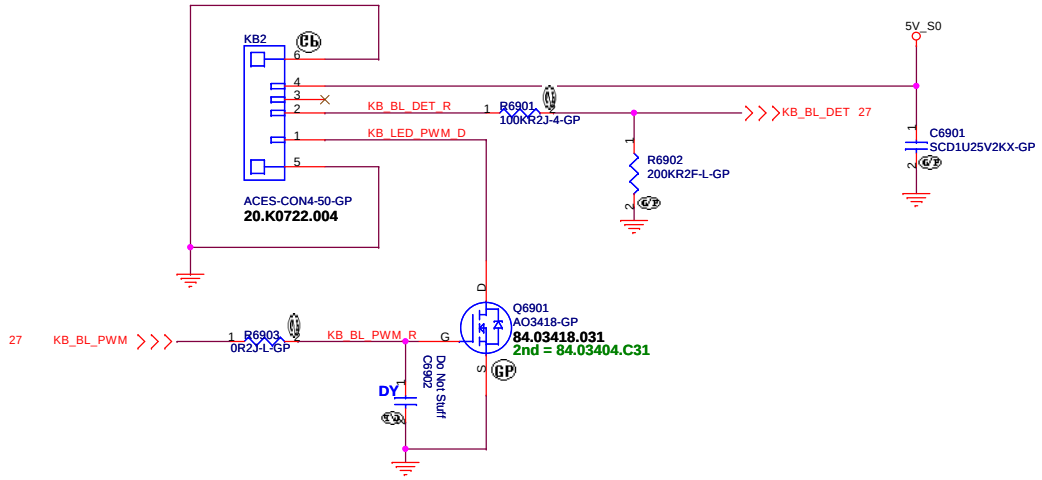
SSID = KBC

Internal KeyBoard Connector



TOUCH PAD





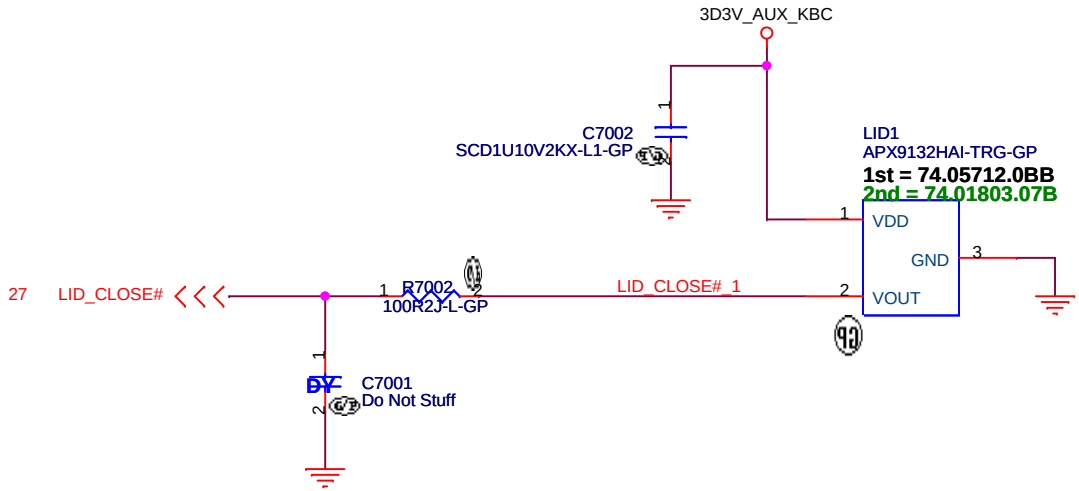
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Key Board/Touch Pad***

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 69 of 103



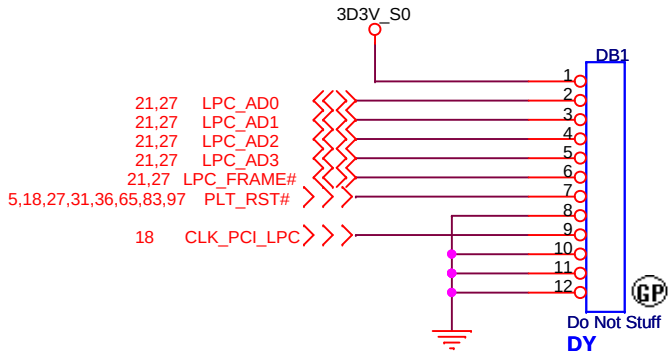
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 70 of 103



DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 71 of 103

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DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Husk/Petra	-4M

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DIS IVB Touch

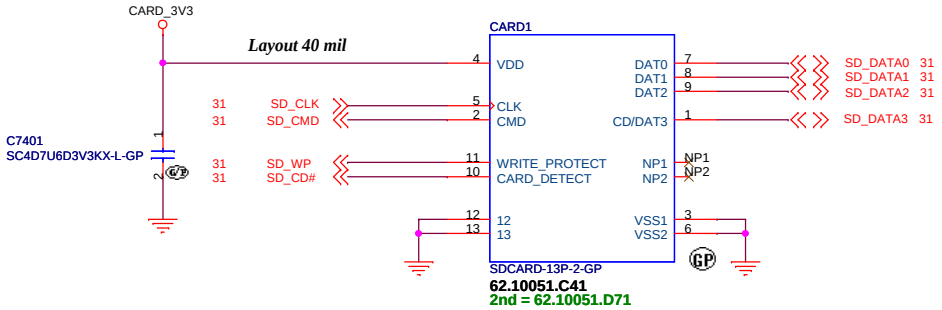
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Husk/Petra	-4M

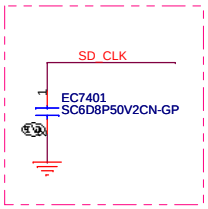
SSID = SDIO

SD/MMC Card Reader



SP1	SP1	SD_D7		xD_RDY
SP2	SP2	SD_D6	MS_INS#	xD_RE#
SP3	SP3	SD_D5		xD_CE#
SP4	SP4	SD_D4		xD_WE#
SP5	SP5	SD_D1	MS_CLK	xD_D6
SP6	SP6	SD_D0	MS_D7	xD_D5
SP7	SP7	SD_CLK	MS_D3	xD_D4
SP8	SP8	SD_CMD	MS_D6	xD_D3
SP9	SP9	SD_D3	MS_D2	xD_D2
SP10	SP10	SD_D2		xD_D7
SP11	SP11		MS_BS	xD_CLE
SP12	SP12	SD_WP	MS_D1	xD_WP#
SP13	SP13	SD_CD#	MS_D5	xD_ALE
SP14	SP14		MS_D4	xD_D0
SP15	SP15		MS_D0	xD_D1
SP16	SP16			xD_CD#

-2:EMI



DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size: Custom | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Thursday, September 06, 2012 | Sheet 74 of 103

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *New Card*

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 75 of 103

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DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 76 of 103

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DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 77 of 103

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DIS IVB Touch

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size: A4	Document Number: **Husk/Petra**
Rev: **-4M**	
Date: Thursday, September 06, 2012	Sheet 78 of 103

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *G- Sensor*

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 79 of 103

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 80 of 103

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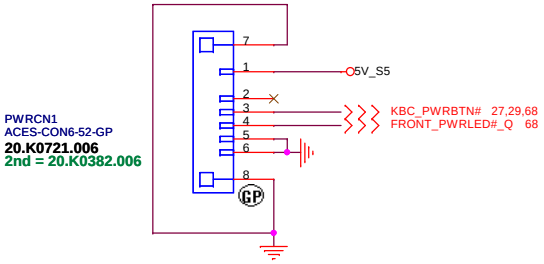
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 81 of 103



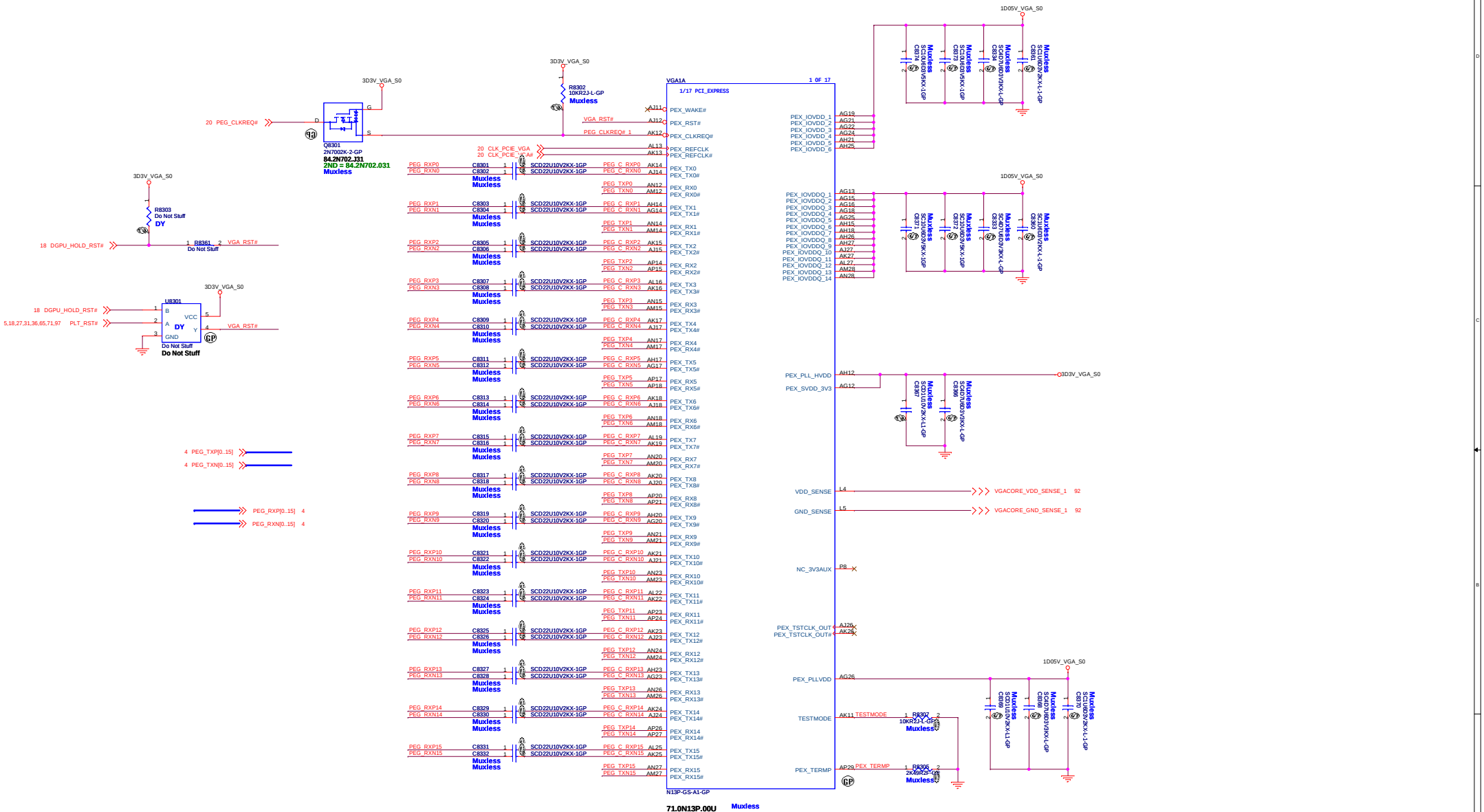
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

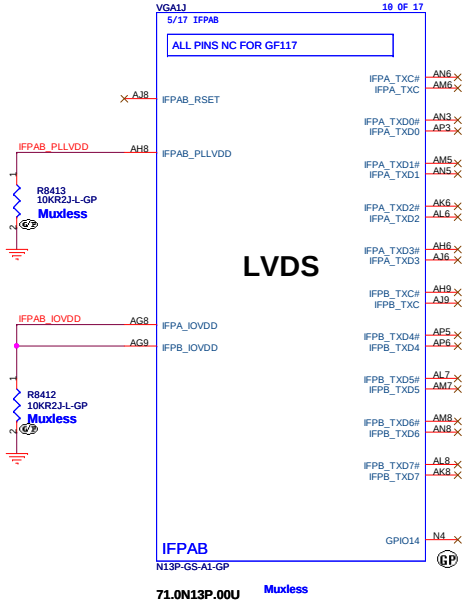
Size	Document Number	Rev
A3	Husk/Petra	-4M

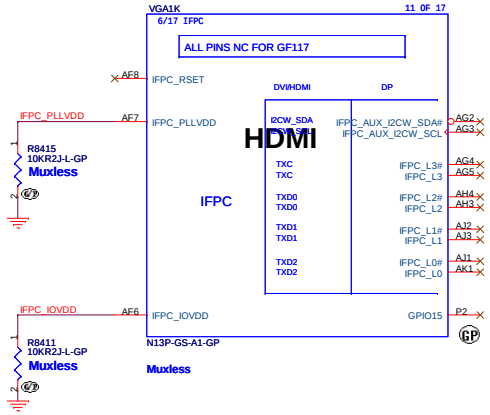
Date: Thursday, September 06, 2012 Sheet 82 of 103

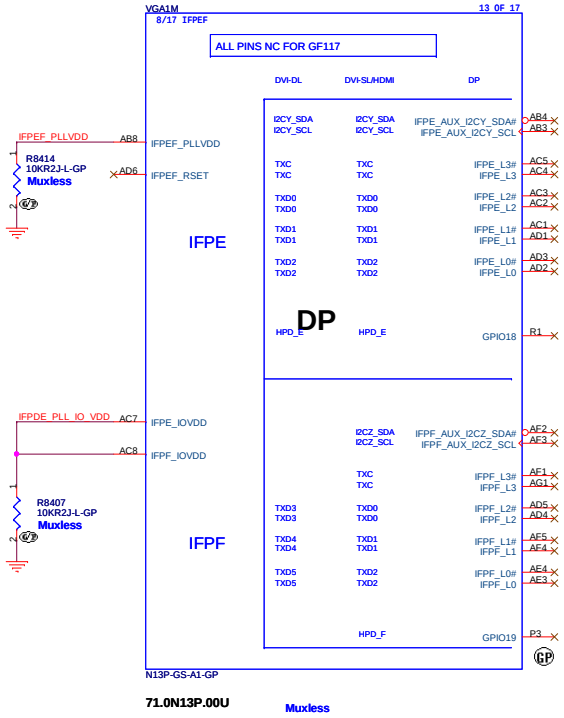


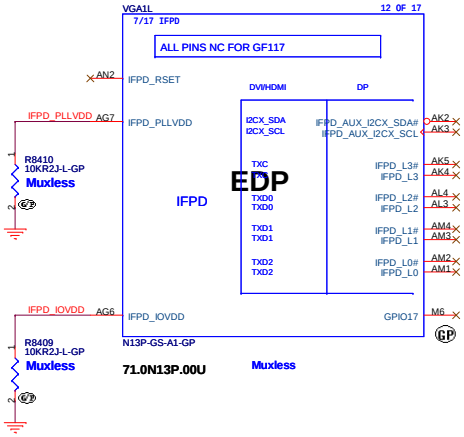
DIS IVB Touch

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU_PCIE/STRAPPING(1/5)	
Size: A2	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 83 of 103	



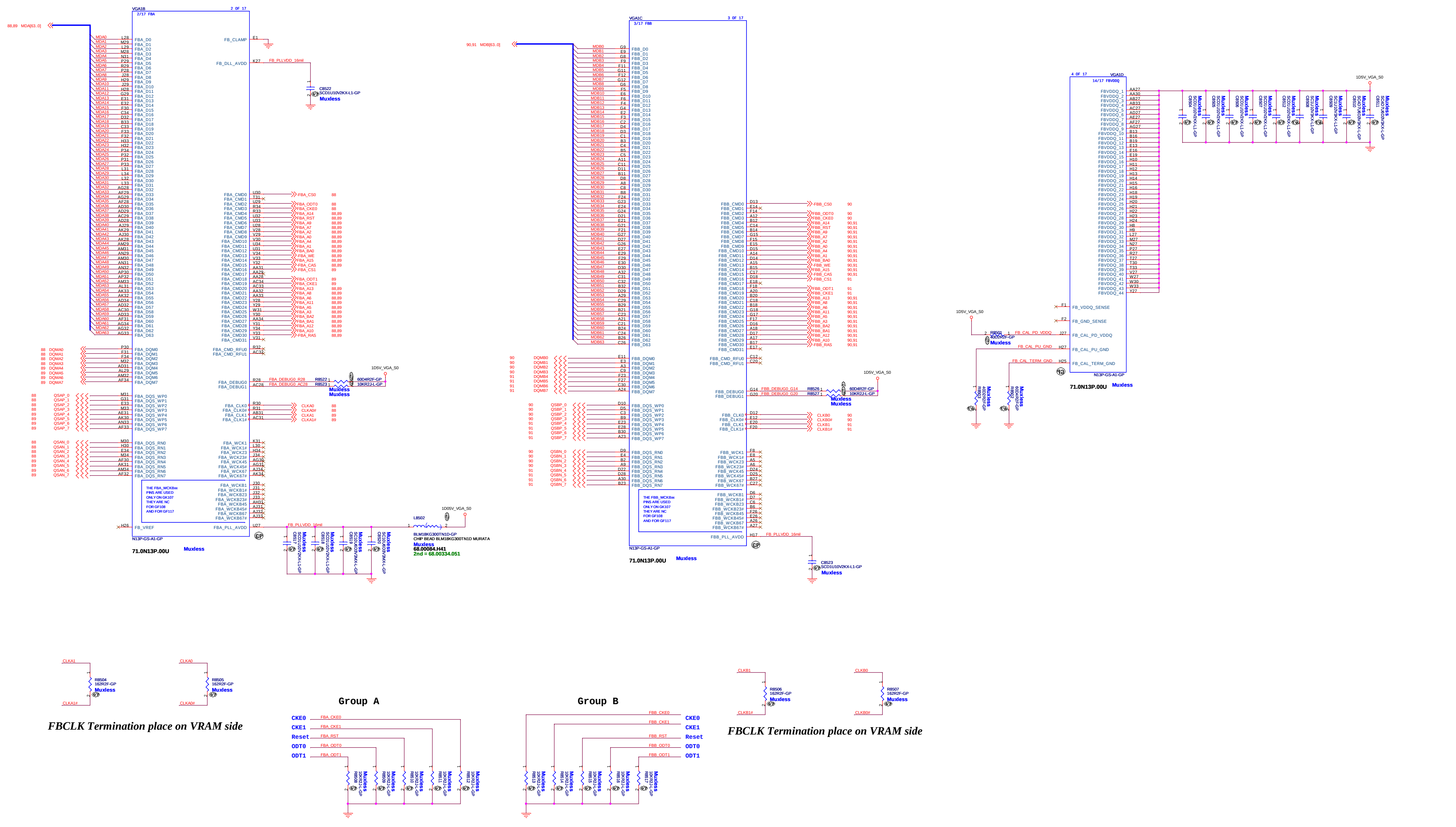






DIS IVB Touch

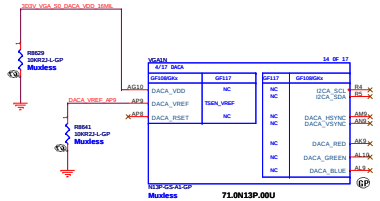
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU Memory(2/5)***	
Size: Custom	Document Number: **Husk/Petra**	Rev: **-4M**
Date: Thursday, September 06, 2012	Sheet 84 of 103	

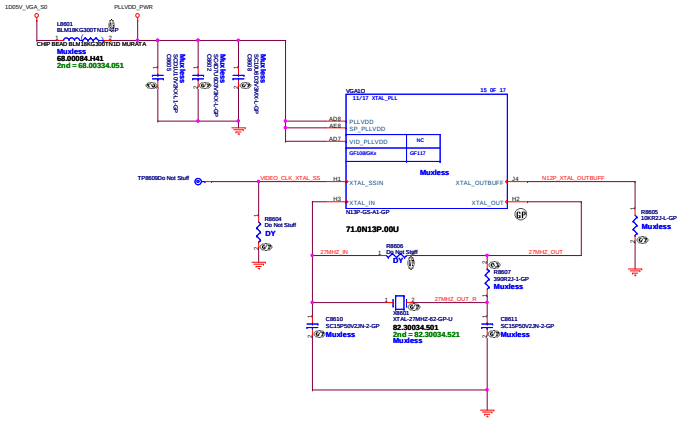


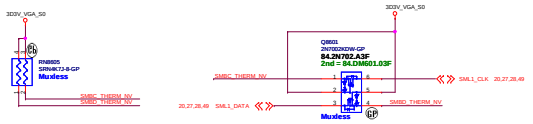
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

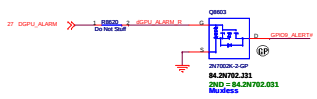
Title			
GPU_DP/LVDS/CRT/GPIO(3/5)			
Size A1	Document Number: Husk/Petra		Rev -4M
Date: Thursday, September 06, 2012	Sheet 85	of 103	



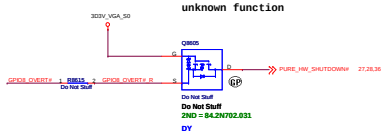




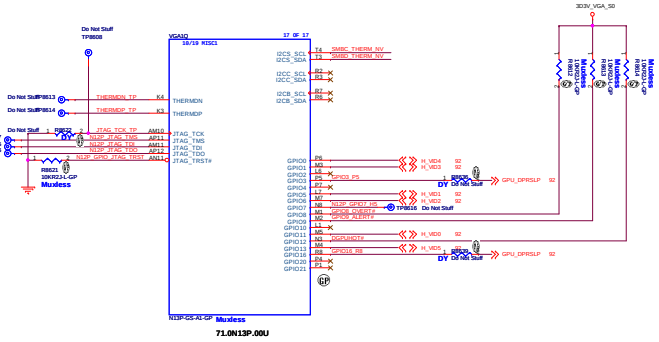
unknown function



unknown function



GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw Input



VRAM Table(N13P-GS/GT/LP/GL/GLP/NS/GE)

	Hynix 2G_B-Die 0110(0x6) 128*16	Hynix 1G_D-die 0010(0x2) 64*16	Samsung 2G_C-Die 0111(0x7) 128*16	Samsung 1G_G-die 0011(0x3) 64*16
ROM_SI R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	45Kohm 64.45325.6DL	20Kohm 64.20025.6DL

5Kohm 64.49915.6DL

10Kohm 64.10025.L0L

VRAM Table(N13M-GS/NS)

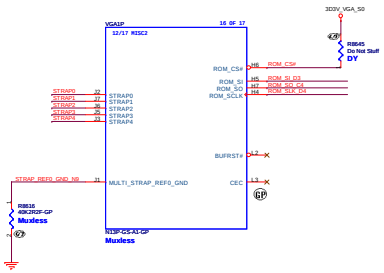
Hynix 2G_D-die 1100(0xC) 128*16	Hynix 2G_B-die 0110(0x6) 128*16

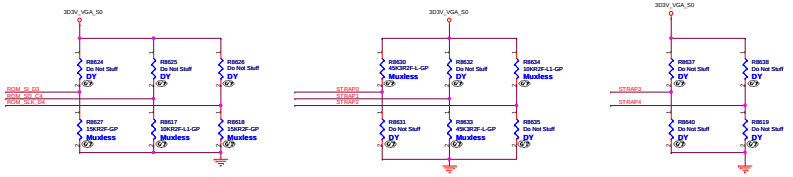
Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

Mode	Product	NVCLK (MHz)	MCLK (MHz)	NVVDD (V)
MAX Point (MP)	N13P-GL/-NS1	800	900	--
	N13P-GLP	660	900	--
TDP Point (TP)	N13P-GL/-NS1	660	900	--
	N13P-GLP	475	900	--
HW Boot Voltage	N13P-GL/-NS1	--	--	0.95
	N13P-GLP	--	--	0.90

Strap Pin Nmae	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0	
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/	PEX_PLL_EN_TERM	
	0	0	1	0	15K ohm pull-down
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	
	0	0	0	1	10K ohm pull-down
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	
	1	1	1	1	45K ohm pull-up
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	
	0	1	1	1	45K ohm pull-down
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	
	1	0	0	1	10K ohm pull-up
STRAP3	N/A	N/A	N/A	N/A	
STRAP4	N/A	N/A	N/A	N/A	





DIS MB Touch

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GPU_POWER(4/5)

Husk/Petra

Size: X1 | Document Number | Rev: -4M

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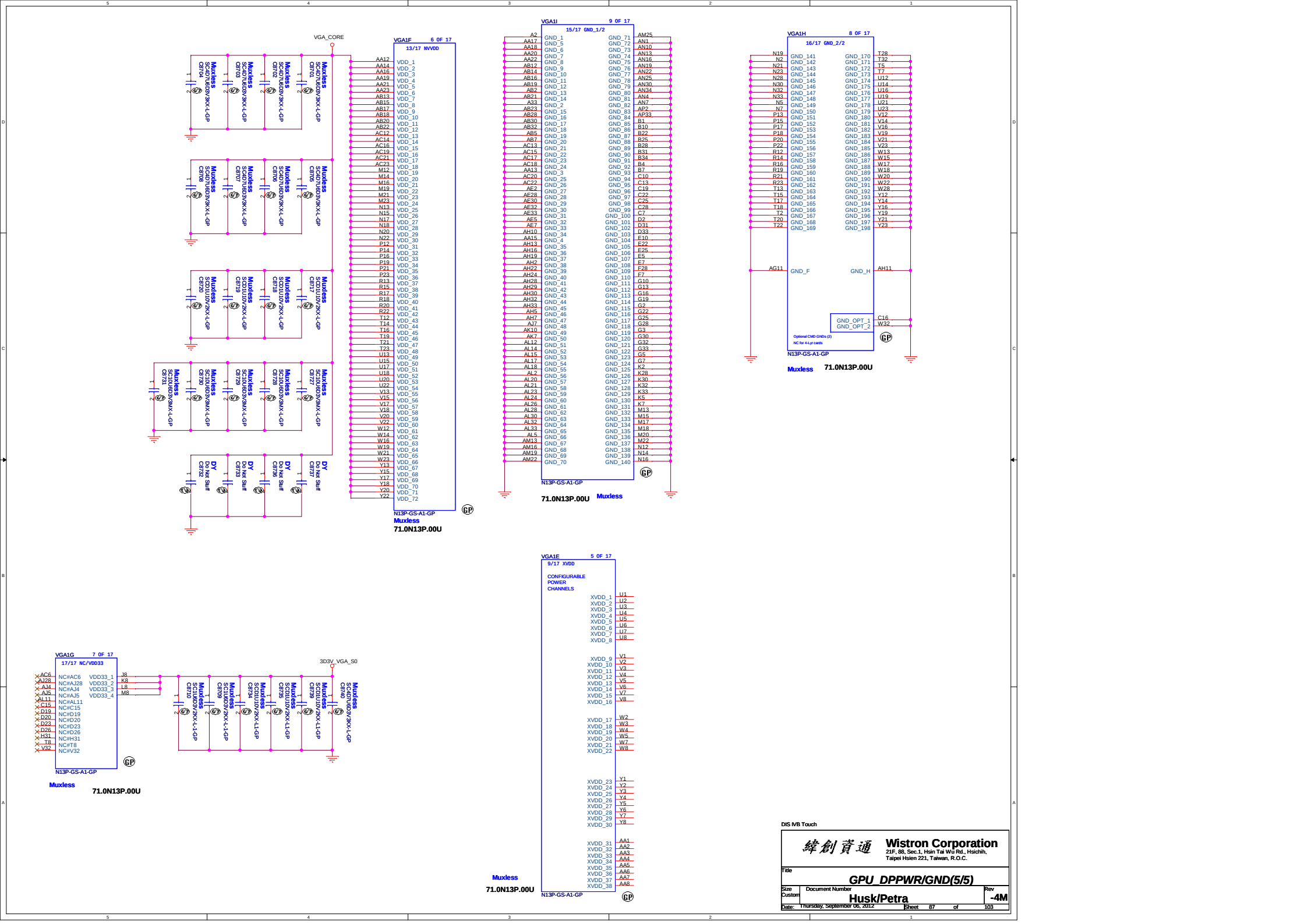
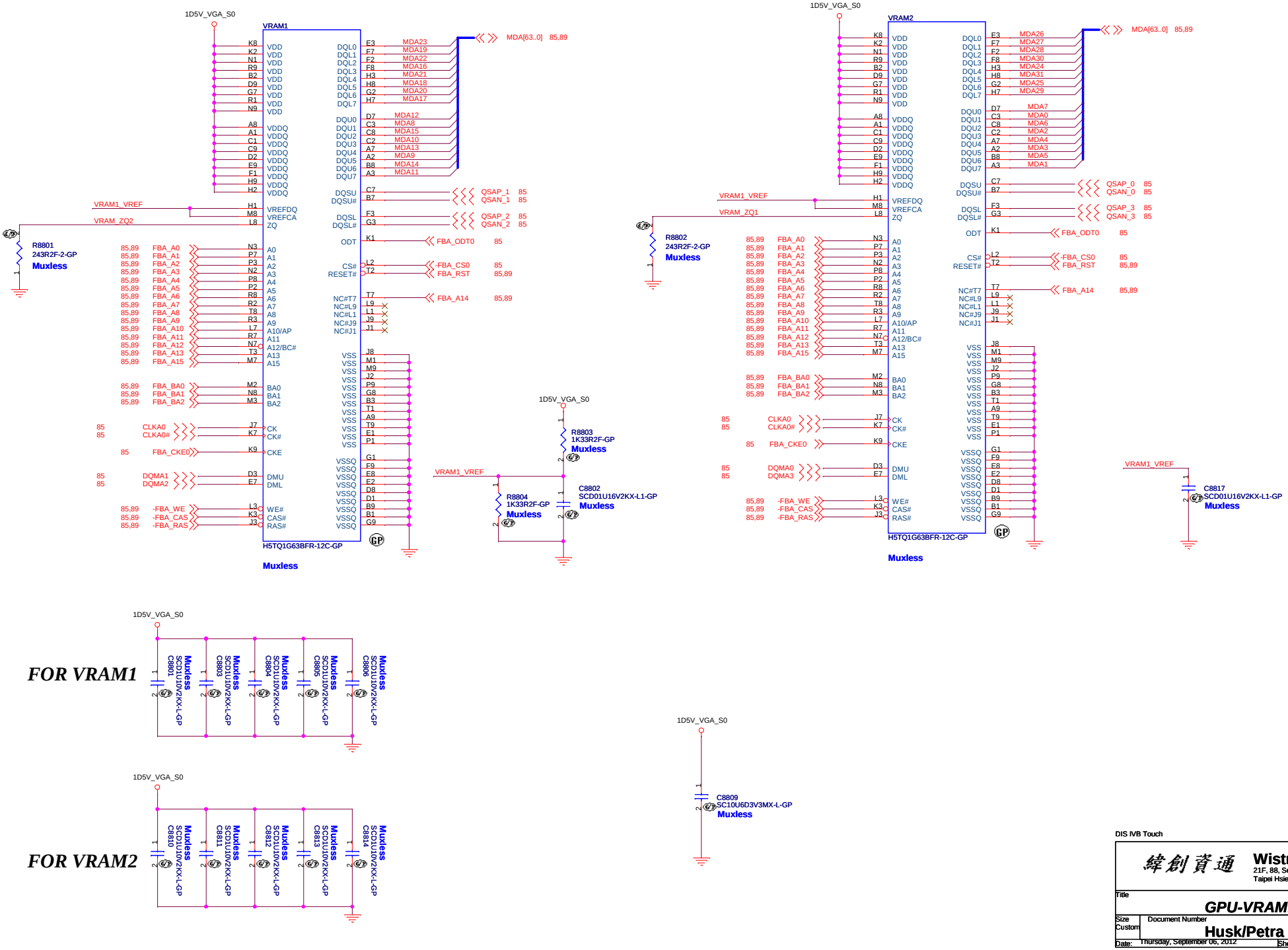

VGA_CORE
VGA1F 6 OF 17
13/17 NVVDD
VGA1I 9 OF 17
15/17 GND_1/2
VGA1H 8 OF 17
16/17 GND_2/2
VGA1E 5 OF 17
9/17 XVDD
CONFIGURABLE POWER CHANNELS
VGA1G 7 OF 17
17/17 NC/VDD33
3D3V_VGA_S0
N13P-GS-A1-GP
Muxless
71.0N13P.00U
Optional GND's (2) NC for 4-Lyr cards
DIS IVB Touch
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU_DPPWR/GND(5/5)
Size Custom
Document Number
Husk/Petra
Rev
-4M
Date: Thursday, September 06, 2012
Sheet 87 of 103



FOR VRAM1

FOR VRAM2

DIS IVB Touch

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM1,2 (1/4)***

Size	Document Number	Rev
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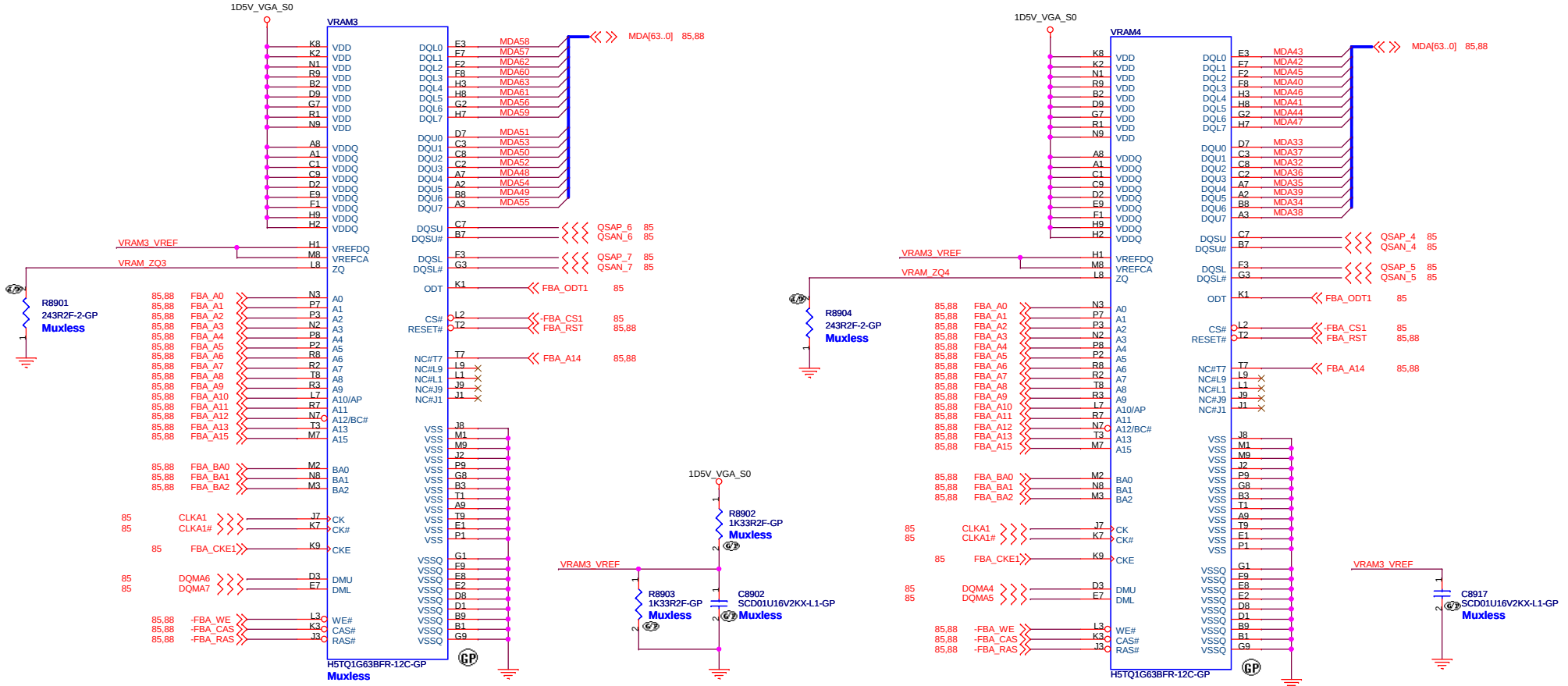
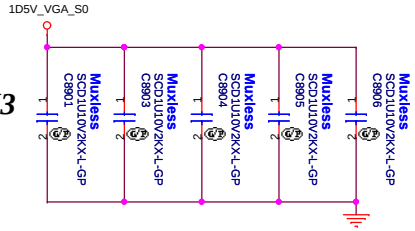
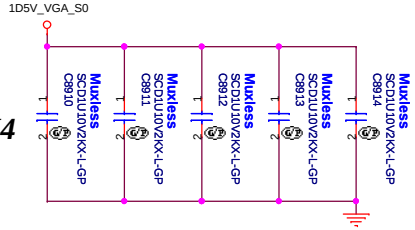
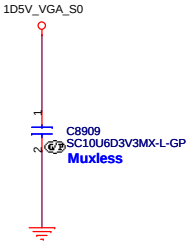


FOR VRAM3



FOR VRAM4





DIS IVB Touch

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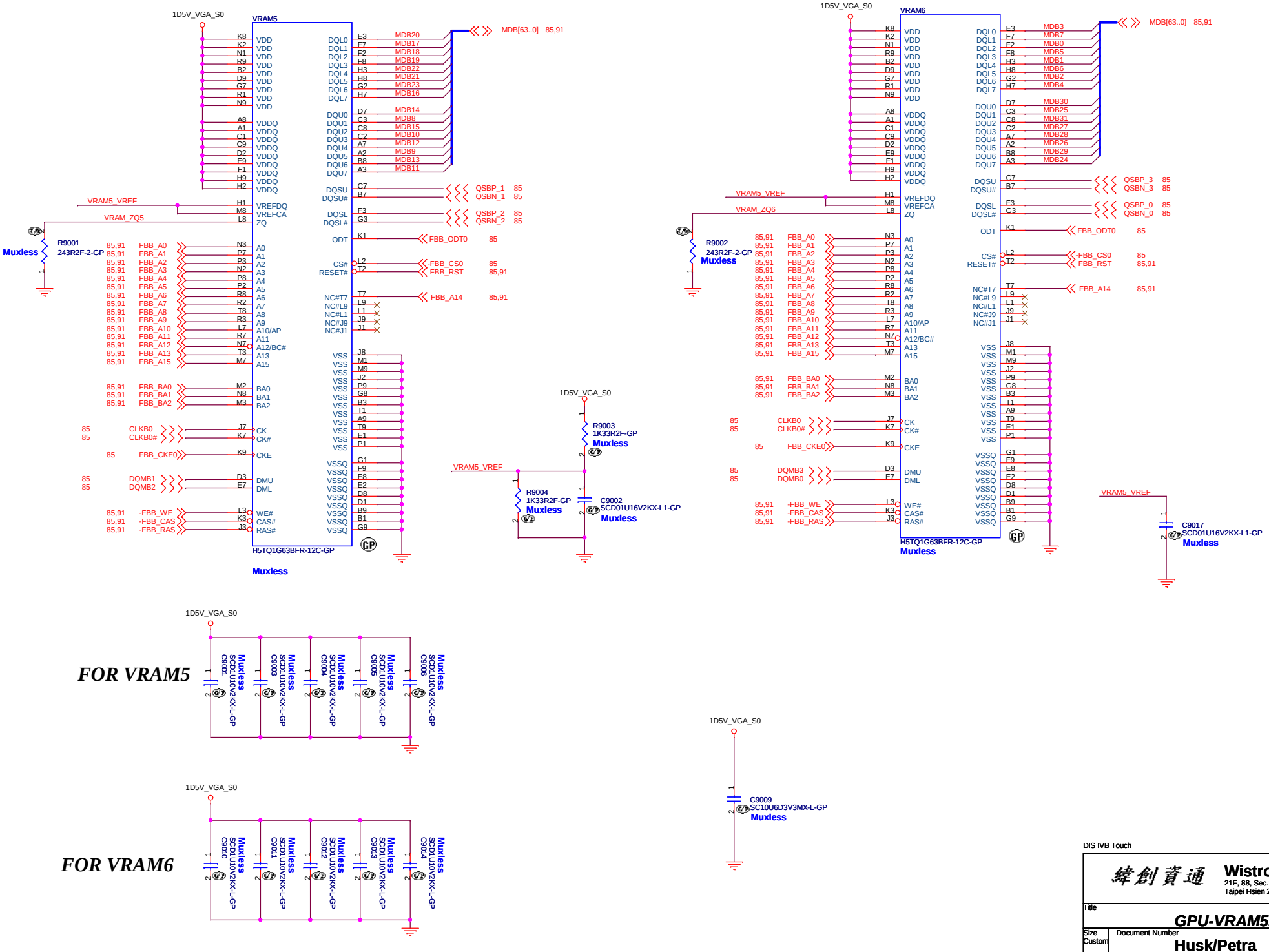
Title: *GPU-VRAM3,4 (2/4)*		
Size: Custom	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 89 of 103	



DIS IVB Touch

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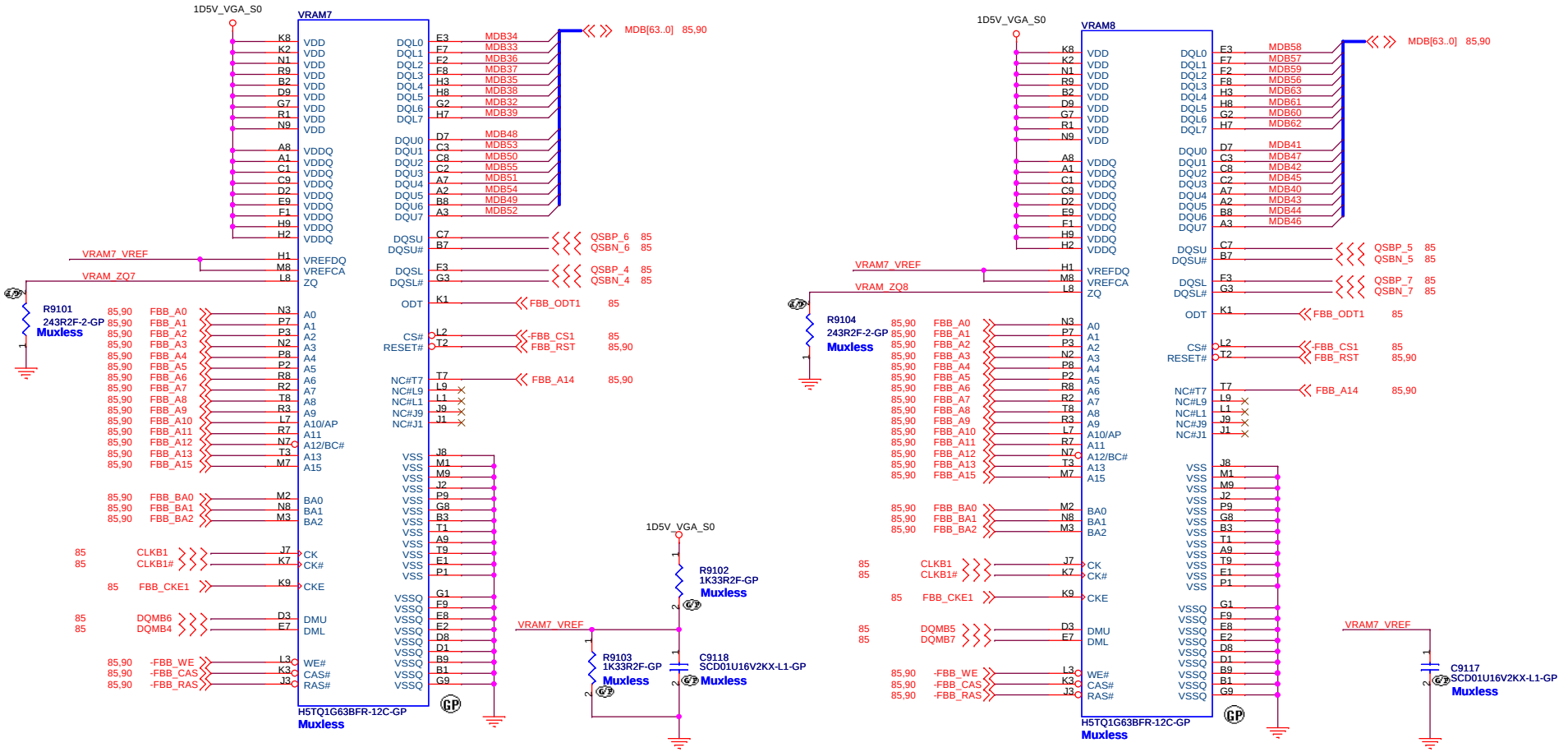
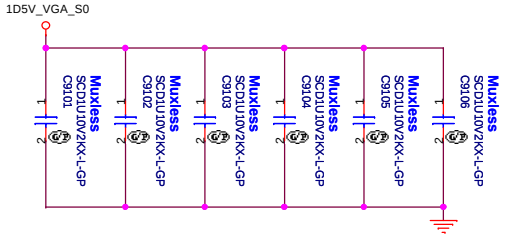
Title: GPU-VRAM5,6 (3/4)

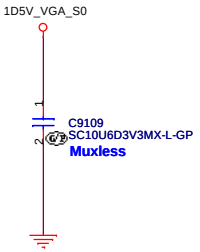
Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 90 of 103

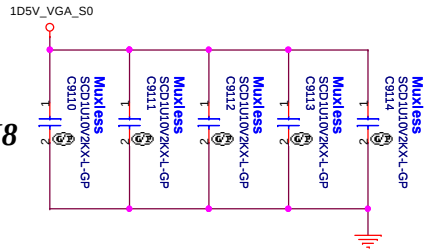


FOR VRAM7





FOR VRAM8



DIS IVB Touch

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Title: ***GPU-VRAM7,8 (4/4)***

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SSID = PWR.Plane.Regulator_GFX

		N13P-GS-LP 71.0N13P.00U	N13P-GL 71.0N13P.B0U	N13M-GS 71.0N13M.E0U
NVVDD Boot Voltage		0.9V VID[6:0]=0110000	0.95V VID[6:0]=0101100	0.875V VID[6:0]0110010
NV_VID1	PR9215	DY	DY	63.10334.L0L
	PR9230	63.10334.L0L	63.10334.L0L	DY
NV_VID3	PR9217	DY	63.10334.L0L	DY
	PR9232	63.10334.L0L	DY	63.10334.L0L
NV_VID4	PR9218	63.10334.L0L	DY	63.10334.L0L
	PR9233	DY	63.10334.L0L	DY

PR9218 Mount , PR9233 DY For N13M-GS Vboot = 0.875V

Change power source Net
Wayler 12/07

1 phase change 0ohm

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

Vga_core
Iccmax=24A
OCP>40A

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

1phase PR9261 mount
2phase PR9261 DY

1phase PR9259 , PR9260 mount
2phase PR9259 , PR9260 DY

DIS IVB Touch

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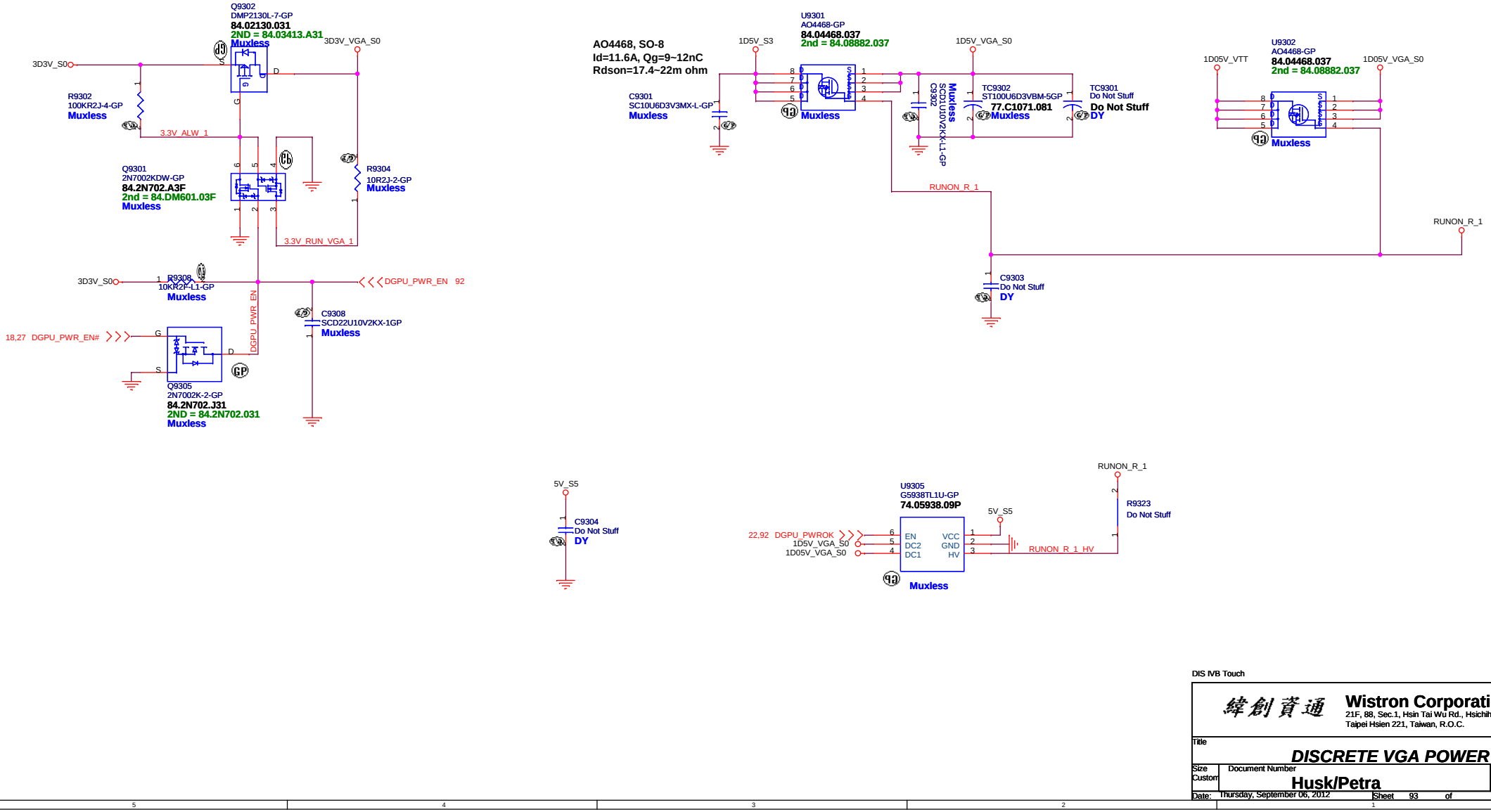
Title: TPS51728_VGA_CORE

Size: | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 92 of 103



DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **DISCRETE VGA POWER**

Size	Document Number	Rev
Custom	Husk/Petra	-4M
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DIS IVB Touch

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

LVDS_Switch

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

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DIS IVB Touch

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Title

CRT_Switch

Size	Document Number	Rev
A3	**Husk/Petra**	**-4M**

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SSID = SDIO

DIS IVB Touch

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TOUCH PANEL***

Size	Document Number	Rev
A2	Husk/Petra	-4M

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H1 Do Not Stuff
H2 Do Not Stuff
H3 Do Not Stuff
H4 Do Not Stuff
H5 Do Not Stuff
H6 Do Not Stuff
H10 Do Not Stuff
H11 Do Not Stuff
H12 Do Not Stuff

CPU

HS3 STF237R128H41-GP
HS2 STF237R128H41-GP
HS1 STF237R128H41-GP

34.4TU18.001
2nd = 34.4TU18.101

34.4TU18.001
2nd = 34.4TU18.101

34.4TU18.001
2nd = 34.4TU18.101

HS4 STF237R128H41-GP
HS5 STF237R128H41-GP

34.4TU18.001
2nd = 34.4TU18.101
Muxless

34.4TU18.001
2nd = 34.4TU18.101
Muxless

VGA

Check test point

3D3V_S0	1	AFTP1
3D3V_AUX_S5	1	AFTP7
3D3V_S5	1	AFTP8
5V_S5	1	AFTP9
19,27 PM_PWRBTN#	1	AFTP10
5,22,36 H_CPUPWRGD	1	AFTP11
27,36 S5_ENABLE	1	AFTP12
5,18,27,31,36,65,71,83 PLT_RST#	1	AFTP13

Test Point放在Dimm Door打開可量測處

-4

PWR_VCCCORE1_DCBATOUT
EC9704 Do Not Stuff
EC9709 Do Not Stuff DY

PWR_GFXCORE1_DCBATOUT
EC9710 Do Not Stuff
EC9724 Do Not Stuff DY

1D05V_VTT
EC9705 Do Not Stuff DY
EC9706 Do Not Stuff DY

DCBATOUT
EC9701 SCD1U50V3KX-GP

DCBATOUT_2
EC9702 Do Not Stuff DY
EC9707 SCD1U50V3KX-GP
EC9723 Do Not Stuff DY
EC9722 SCD1U50V3KX-GP
EC9721 SCD1U50V3KX-GP

EC9728 Do Not Stuff DY
EC9729 Do Not Stuff DY
AUD_AGND

AD_JK AFTP41
AD_JK AFTP42

-4M_201208070840

39 BATA_SDA_1	1	AFTP2
39 BI	1	AFTP3
39 BAT_IN#_1	1	AFTP4
BT+	1	AFTP5
BT+	1	AFTP6
BT+	1	AFTP14
BT+	1	AFTP15
27,29,68,82 KBC_PWRBTN#	1	AFTP16
68,82 FRONT_PWRLED#_Q	1	AFTP17
DCBATOUT_LCD	1	AFTP18
DCBATOUT_LCD	1	AFTP19
49 DBC_EN_C	1	AFTP22
49 BLON_OUT_C	1	AFTP23
49 LCD_BRIGHTNESS	1	AFTP24
49 DP_TXP1_CPU_C	1	AFTP32
49 DP_TXN1_CPU_C	1	AFTP33
49 DP_TXP0_CPU_C	1	AFTP34
49 DP_TXN0_CPU_C	1	AFTP35
49 DP_DDC_CLK_CPU_C	1	AFTP37
LCDVDD	1	AFTP38
LCDVDD	1	AFTP39
50,59 CRT_DDCCLK_CON	1	AFTP44
50,59 CRT_VSYNC_CON	1	AFTP45
50,59 CRT_DDCDATA_CON	1	AFTP46
50,59 CRT_HSYNC_CON	1	AFTP47

-4M-201208031615

1D5V_S3
EC9711 Do Not Stuff DY
EC9712 Do Not Stuff DY
EC9713 Do Not Stuff DY
EC9714 Do Not Stuff DY
EC9715 Do Not Stuff DY
EC9716 Do Not Stuff DY

5V_S0
EC9717 Do Not Stuff DY
EC9718 Do Not Stuff DY
EC9719 SCD1U10V2KX-L1-GP
EC9720 Do Not Stuff DY

-2:EMI

DCBATOUT
EC9703 SCD1U50V3KX-GP

LCDVDD
EC9726 SCD1U10V2KX-L1-GP

DCBATOUT
EC9730 SCD1U50V3KX-GP
EC9731 SCD1U50V3KX-GP

5V_S5
EC9725 Do Not Stuff DY

3D3V_S0
EC9708 Do Not Stuff DY

DIS IVB Touch

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Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: Husk/Petra
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Date: Thursday, September 06, 2012
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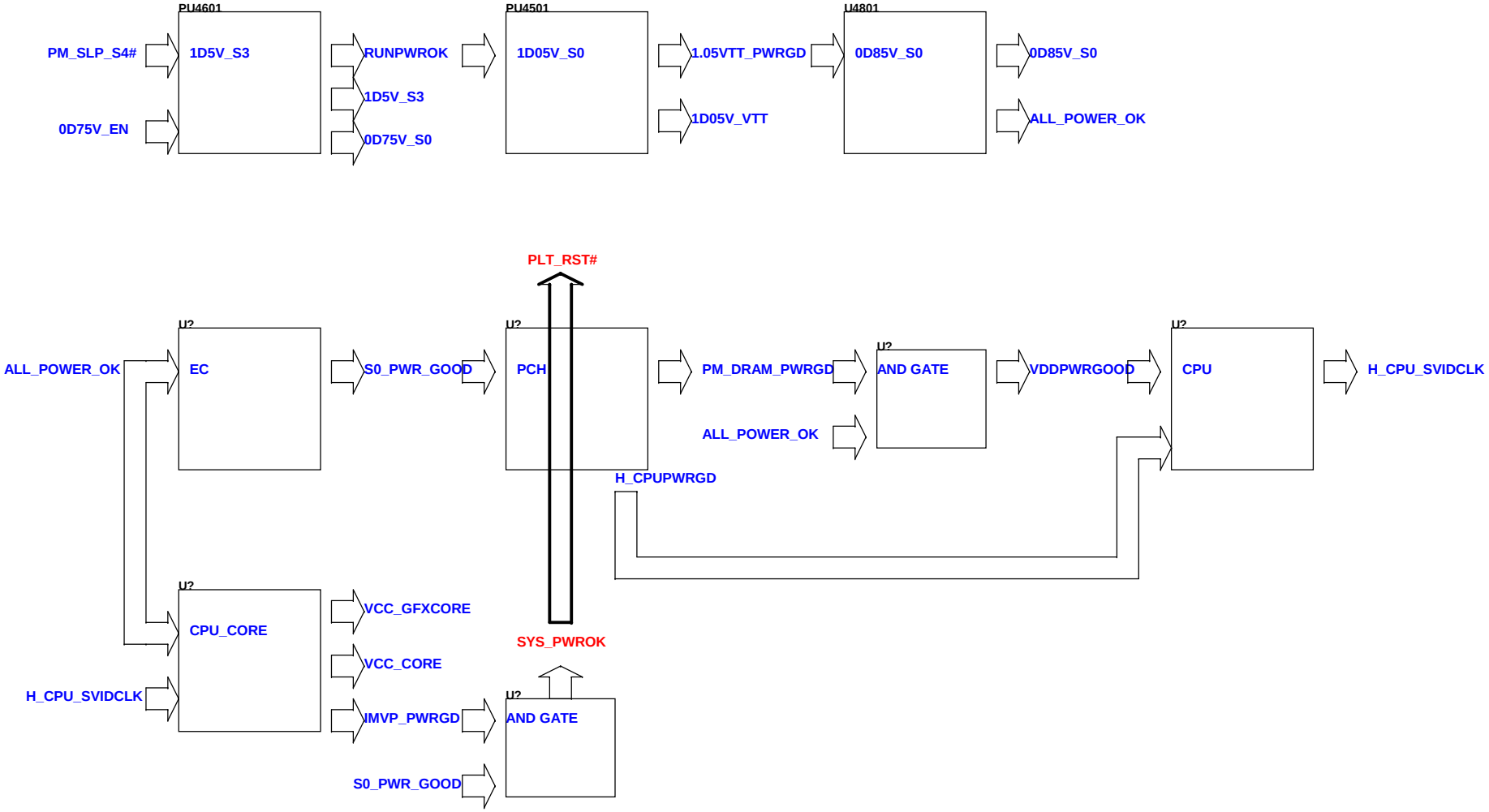
Power Sequence



DIS IVB Touch

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size	Document Number	Rev
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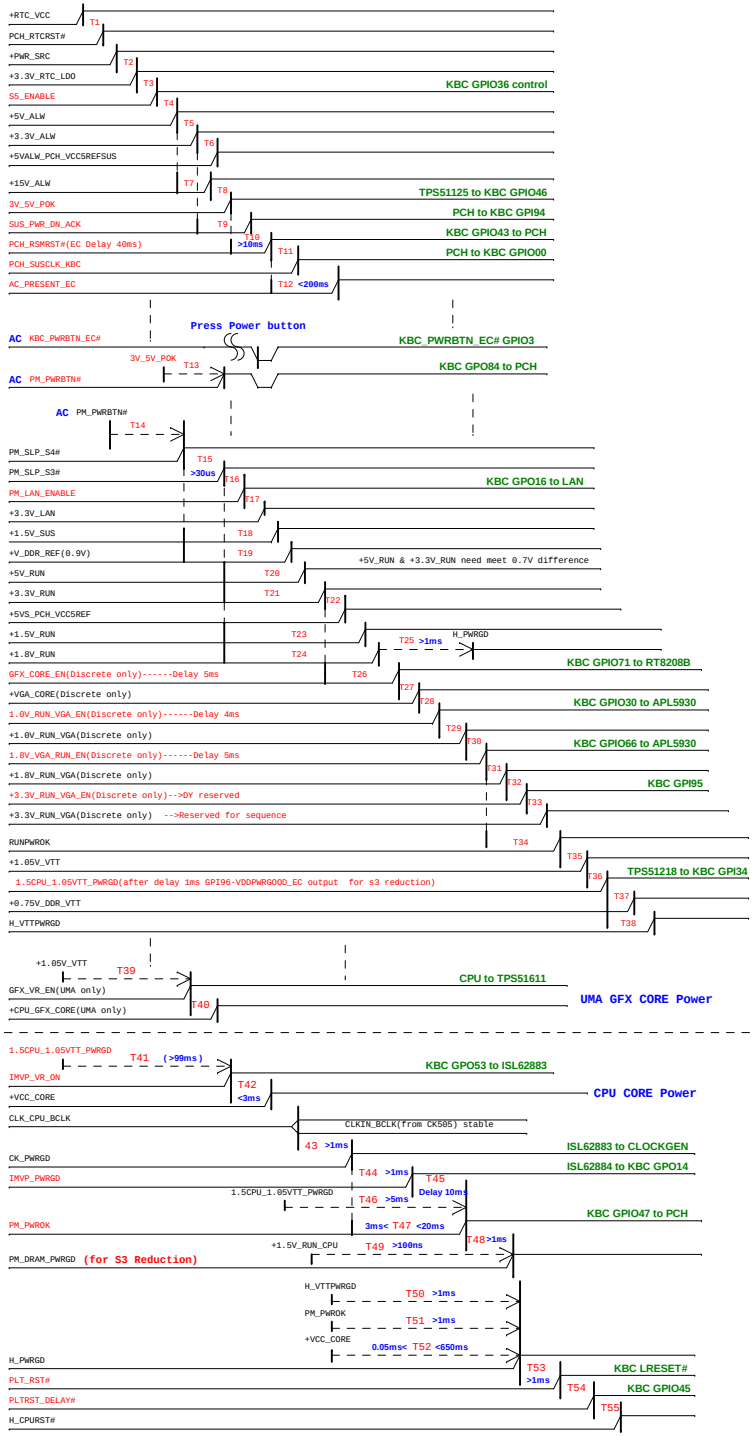
Intel-Power Up Sequence

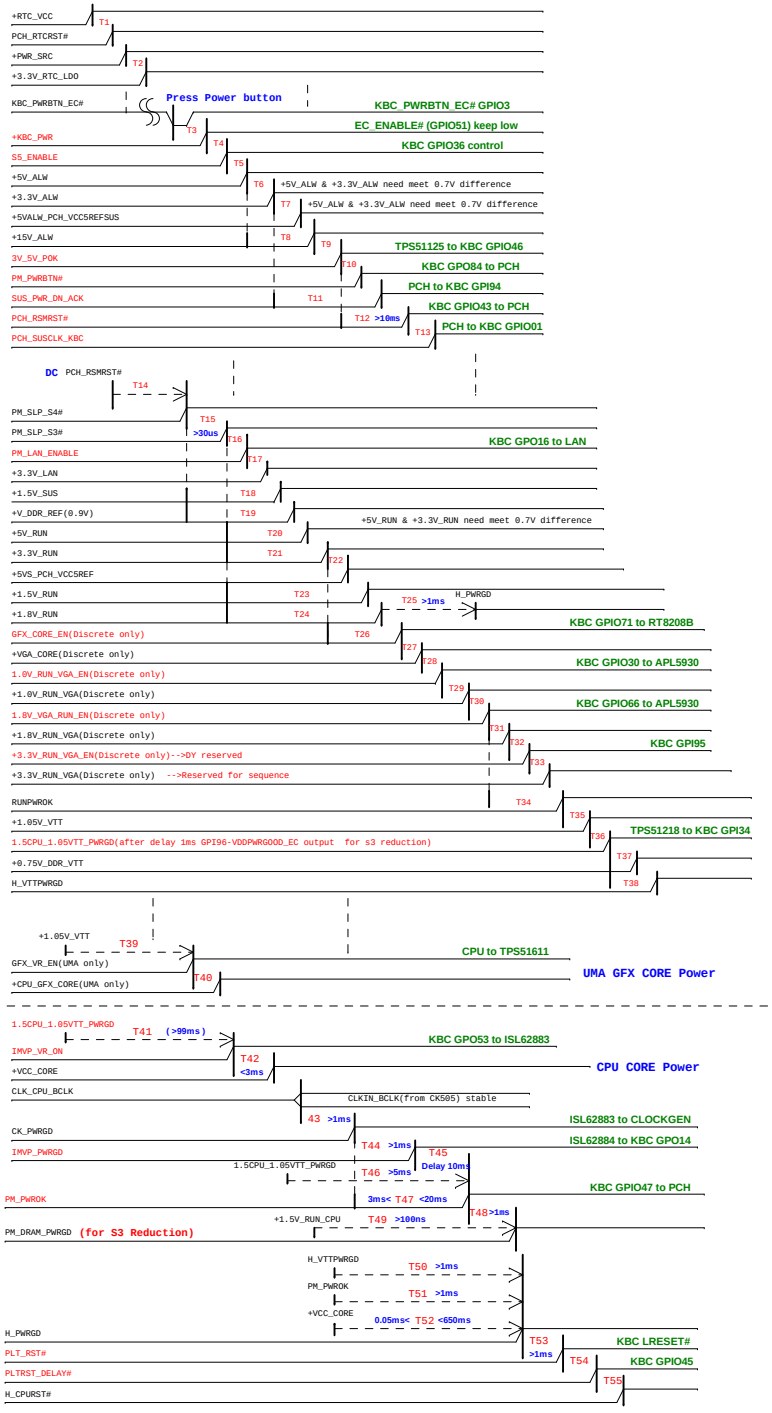
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



DIS NB Touch

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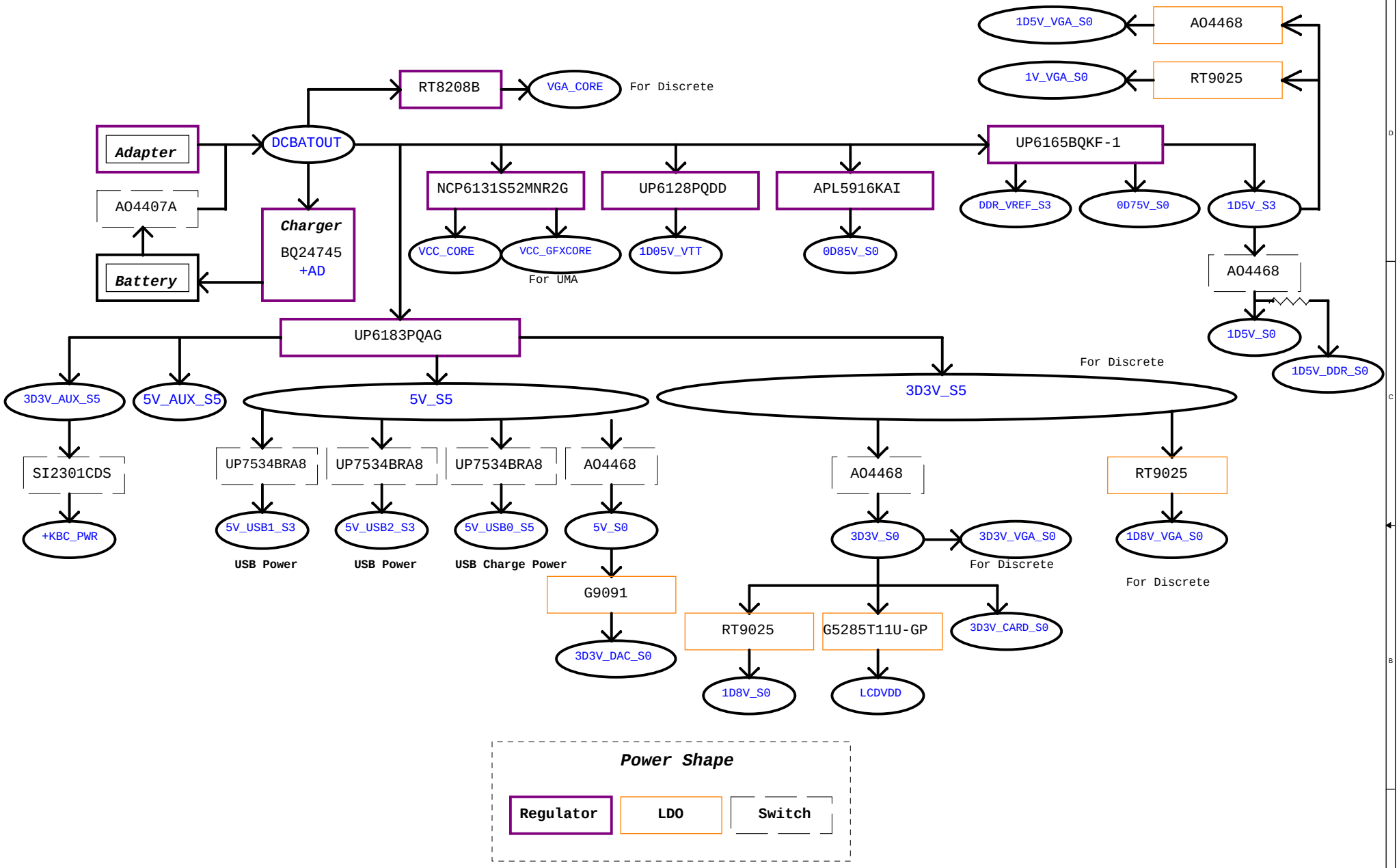
Title: Power Sequence		
Size: A3	Document Number: Husk/Petra	Rev: 4M
Date: Thursday, September 06, 2012	Sheet 39 of 103	



DIS IVB Touch

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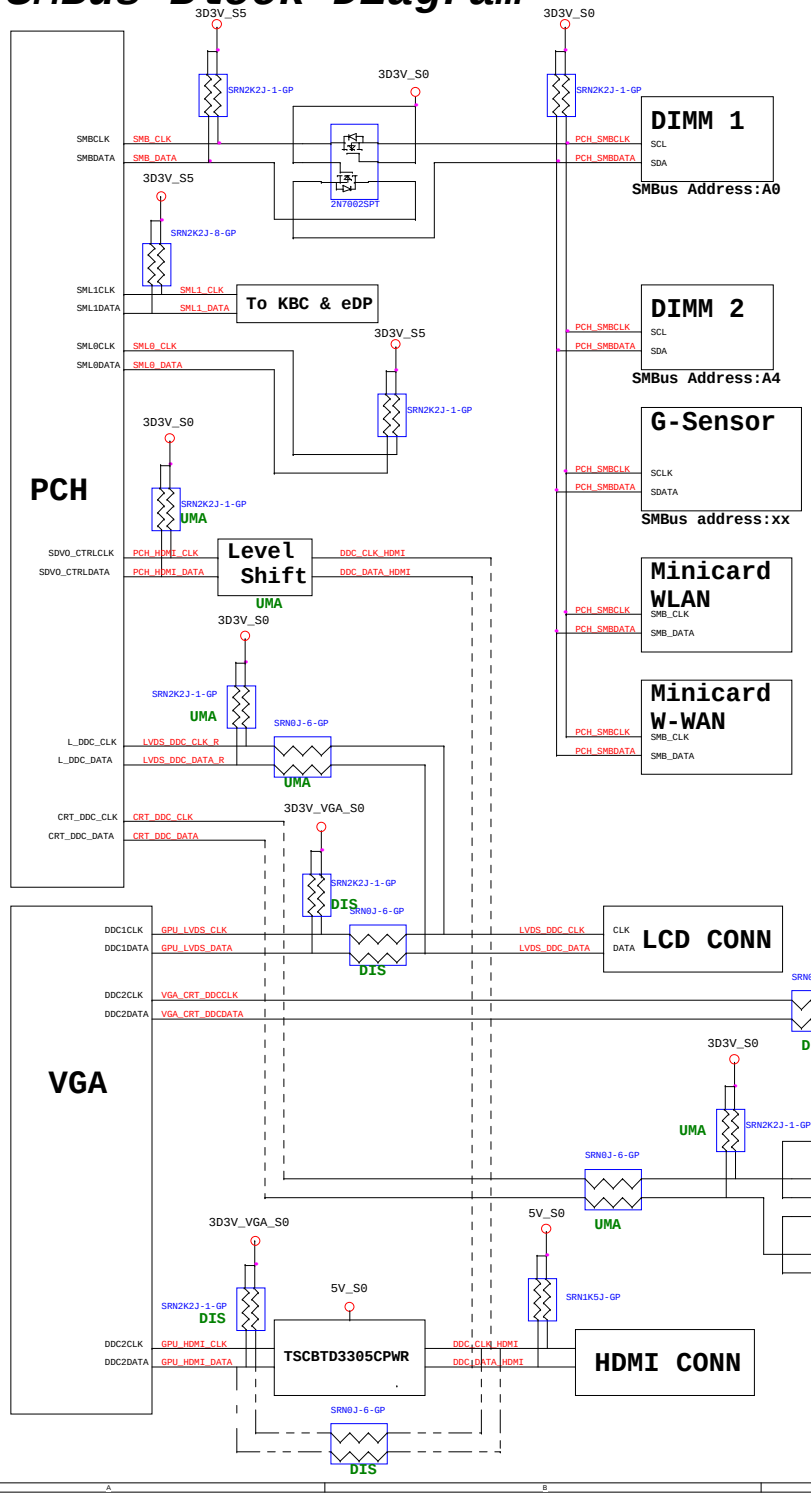
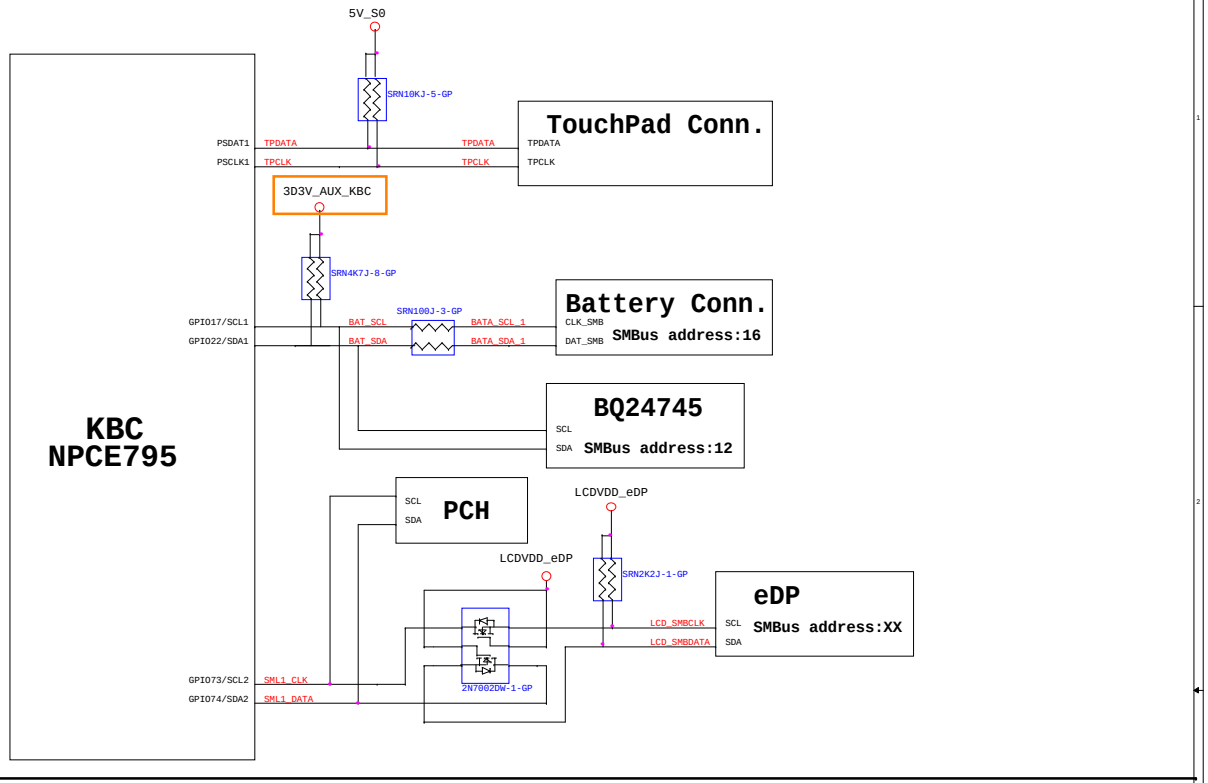
Title: Power Block Diagram		
Size: A3	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 100 of 103	

PCH SMBus Block Diagram



KBC SMBus Block Diagram



DIS IVB Touch

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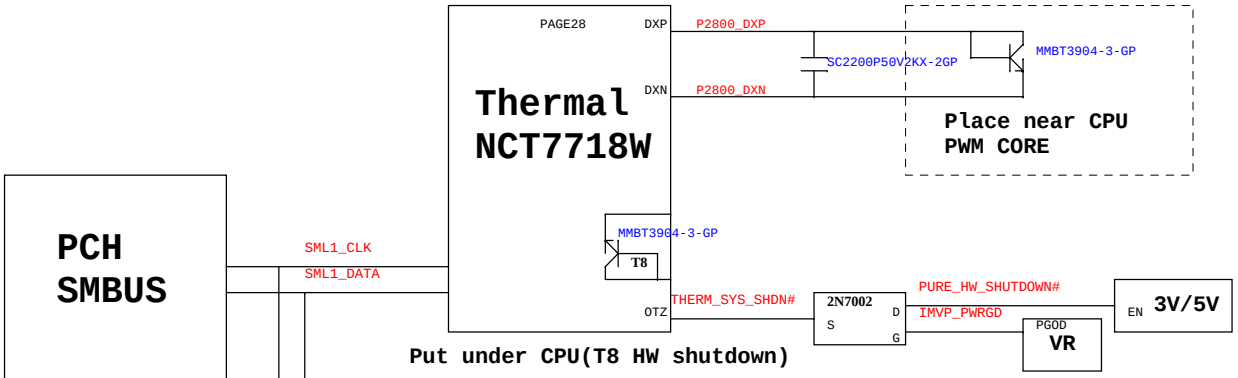
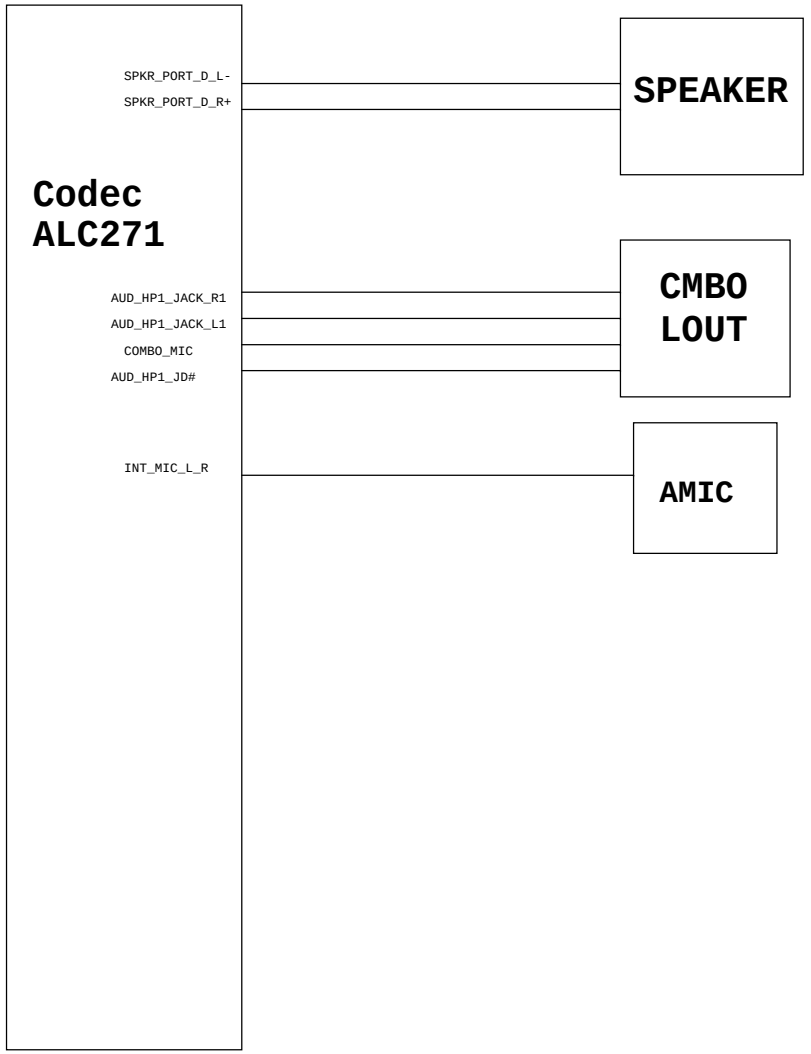
Title: SMBUS Block Diagram		
Size: A2	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 101 of 103	

Thermal Block Diagram



Audio Block Diagram



DIS IVB Touch

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Title: *Thermal/Audio Block Diagram*		
Size: Custom	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 102 of 103	

DIS IVB Touch

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB charger

Size	Document Number	Rev
A3	**Husk/Petra**	**-4M**

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