Poseidon

Schematics Document

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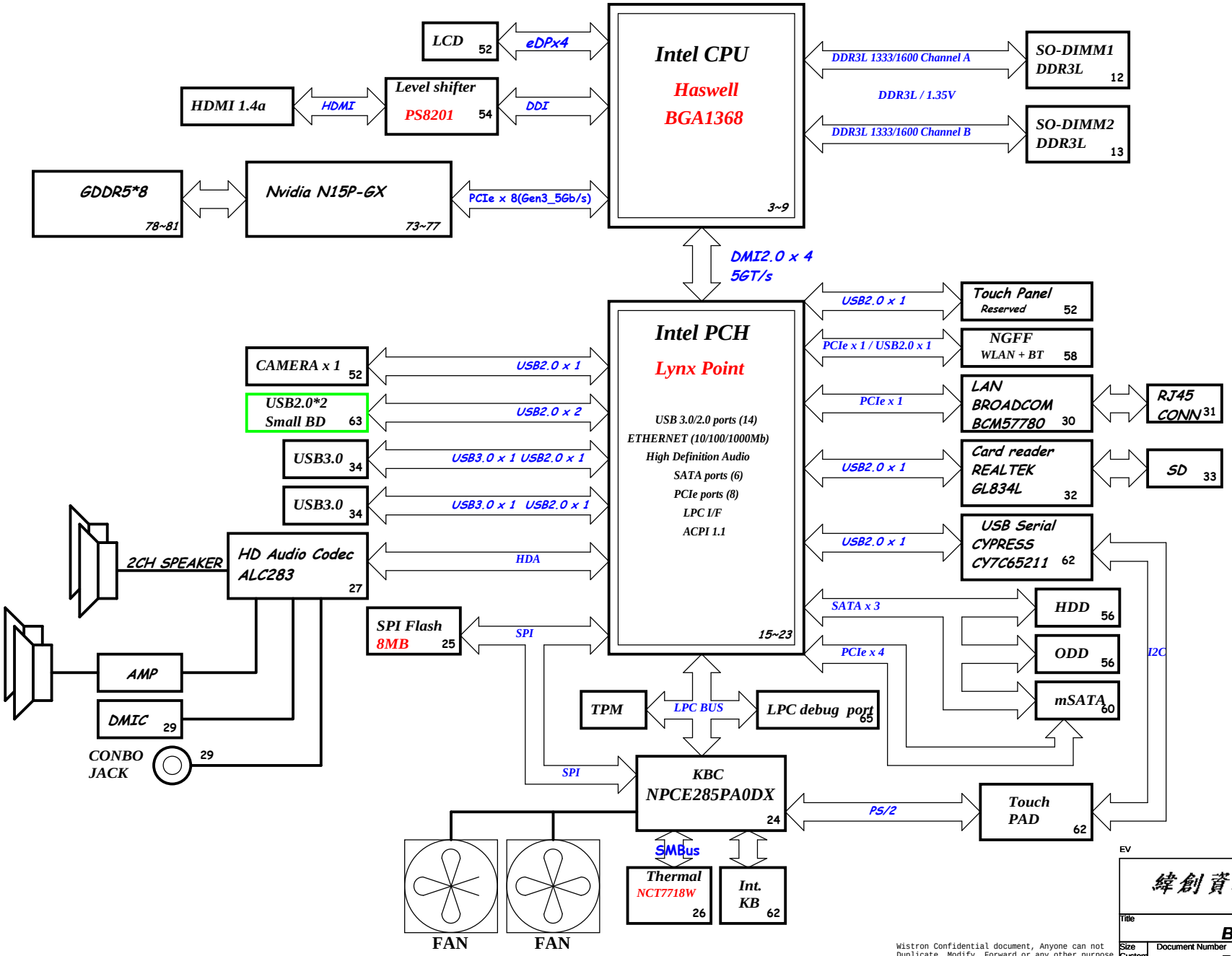
Title: ***Cover Page***

Size	Document Number	Rev
A3	**Poseidon_860M**	-1

Date: Tuesday, June 17, 2014 Sheet 1 of 102

Poseidon Board Block Diagram

Project code : 4PD02G010001
PCB NO : 14203
Revision : -2



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Title: Block Diagram

Size	Document Number	Rev
Custom	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 2 of 102

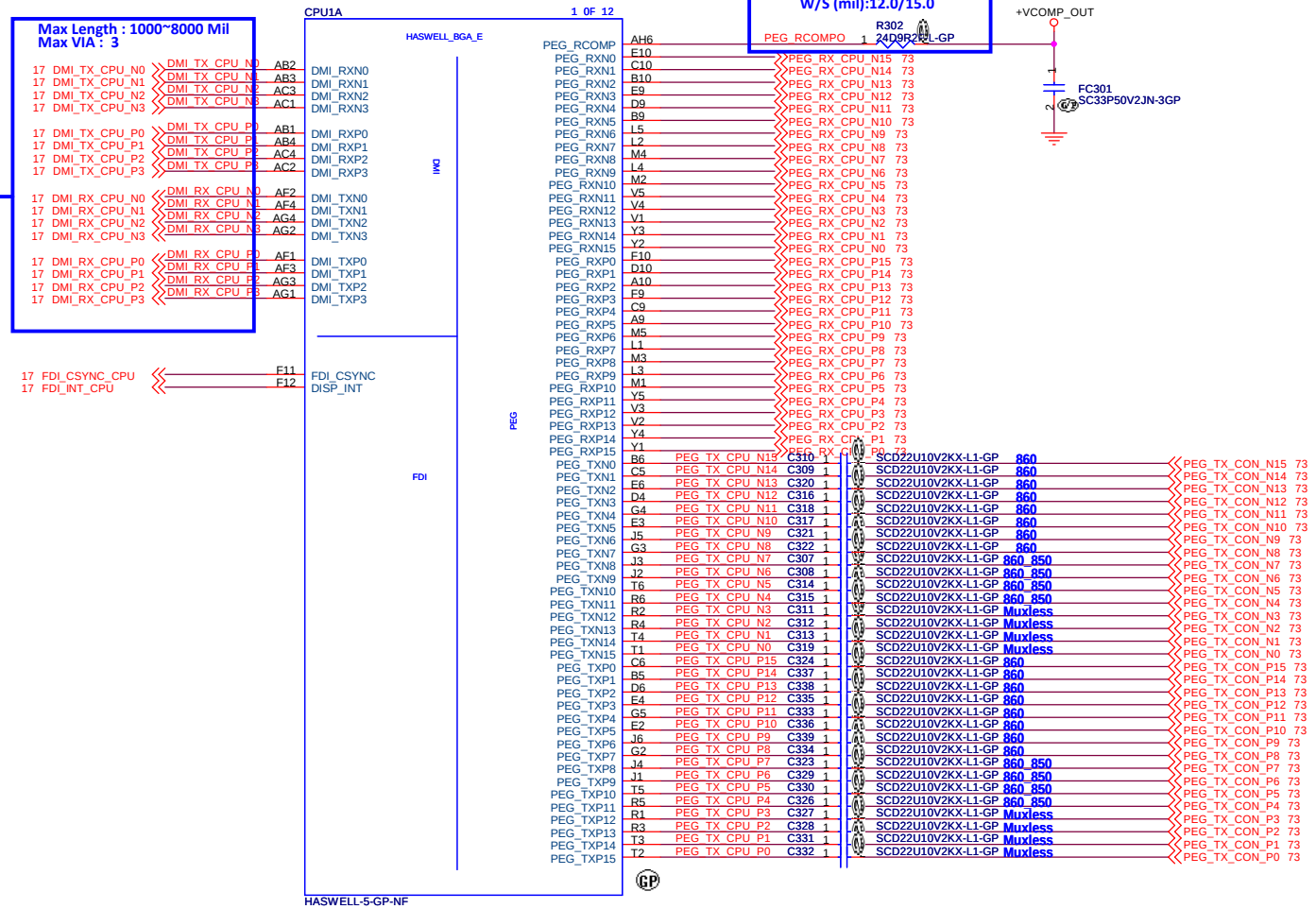
SSID = CPU

Layout Note:

Max Length : 400 Mil
W/S (mil):12.0/15.0

Layout Note:

Max Length : 1000~8000 Mil
Max VIA : 3



71.HASWE.D0U

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

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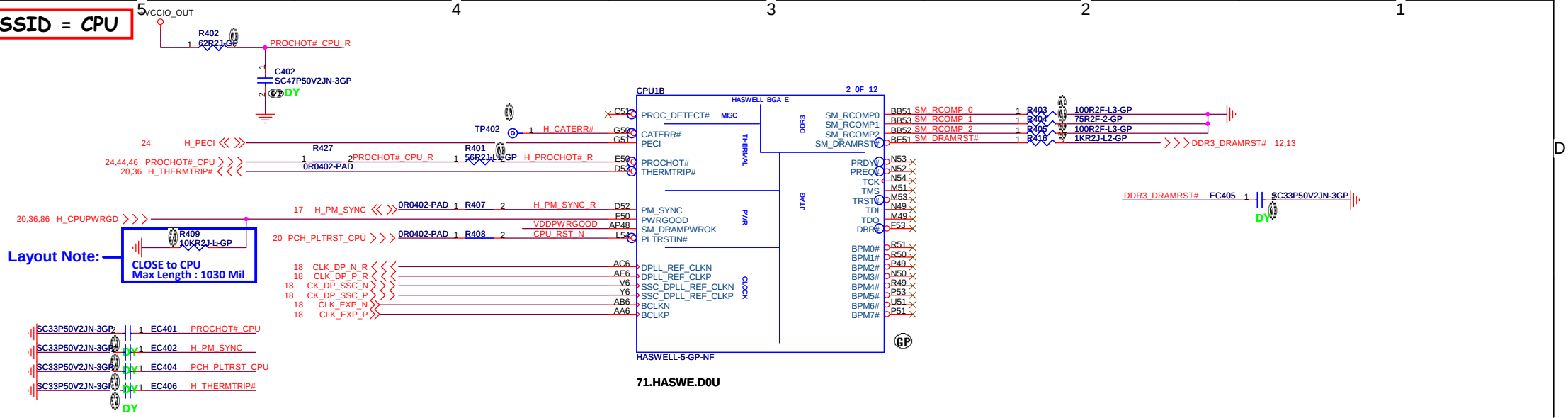
Title: **CPU (PCIE/DMI/FDI)**

Size: A3 | Document Number: **Poseidon 860M** | Rev: -1

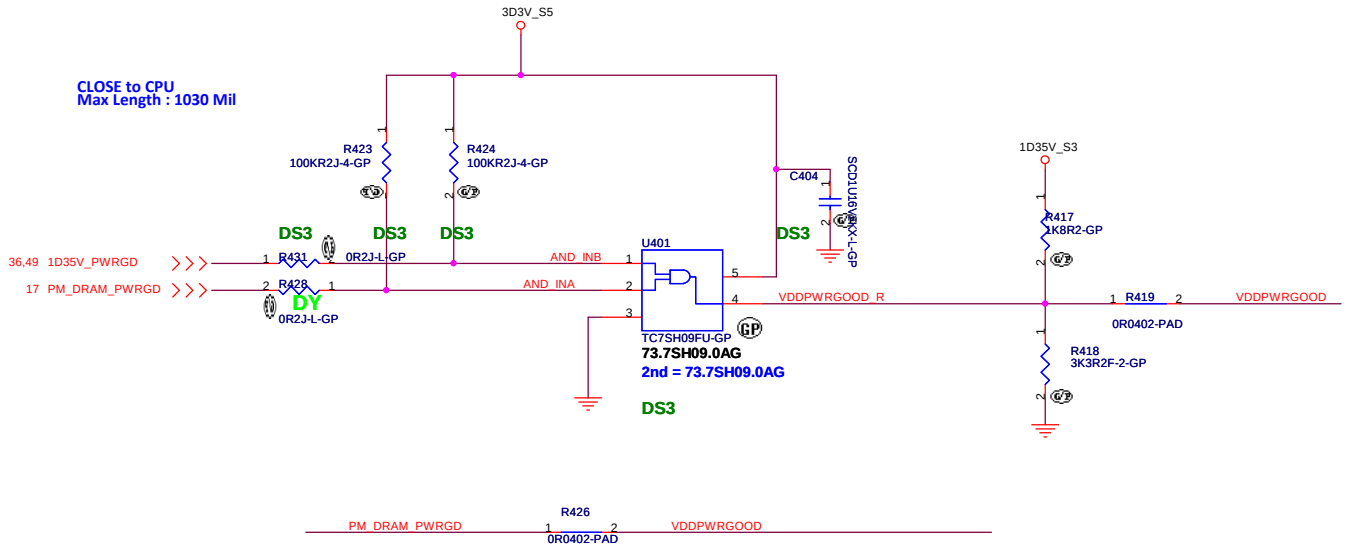
Date: Tuesday, June 17, 2014 | Sheet 3 of 102

SSID = CPU

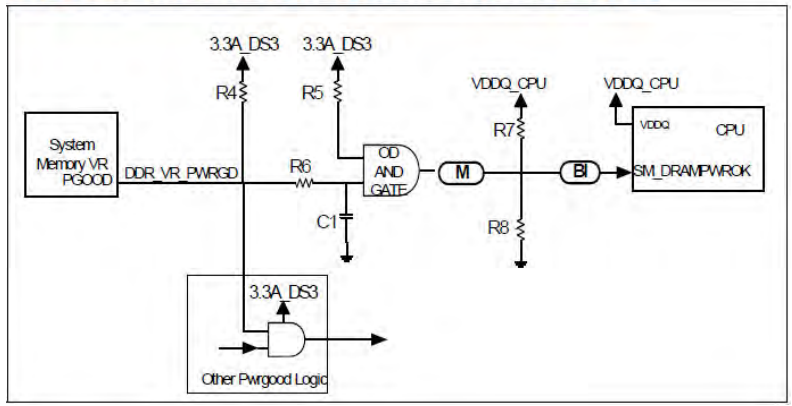


Layout Note:
CLOSE to CPU
Max Length : 1030 Mil

71.HASWE.D0U



.SM_DRAMPWROK Topology for platforms supporting Deep S3



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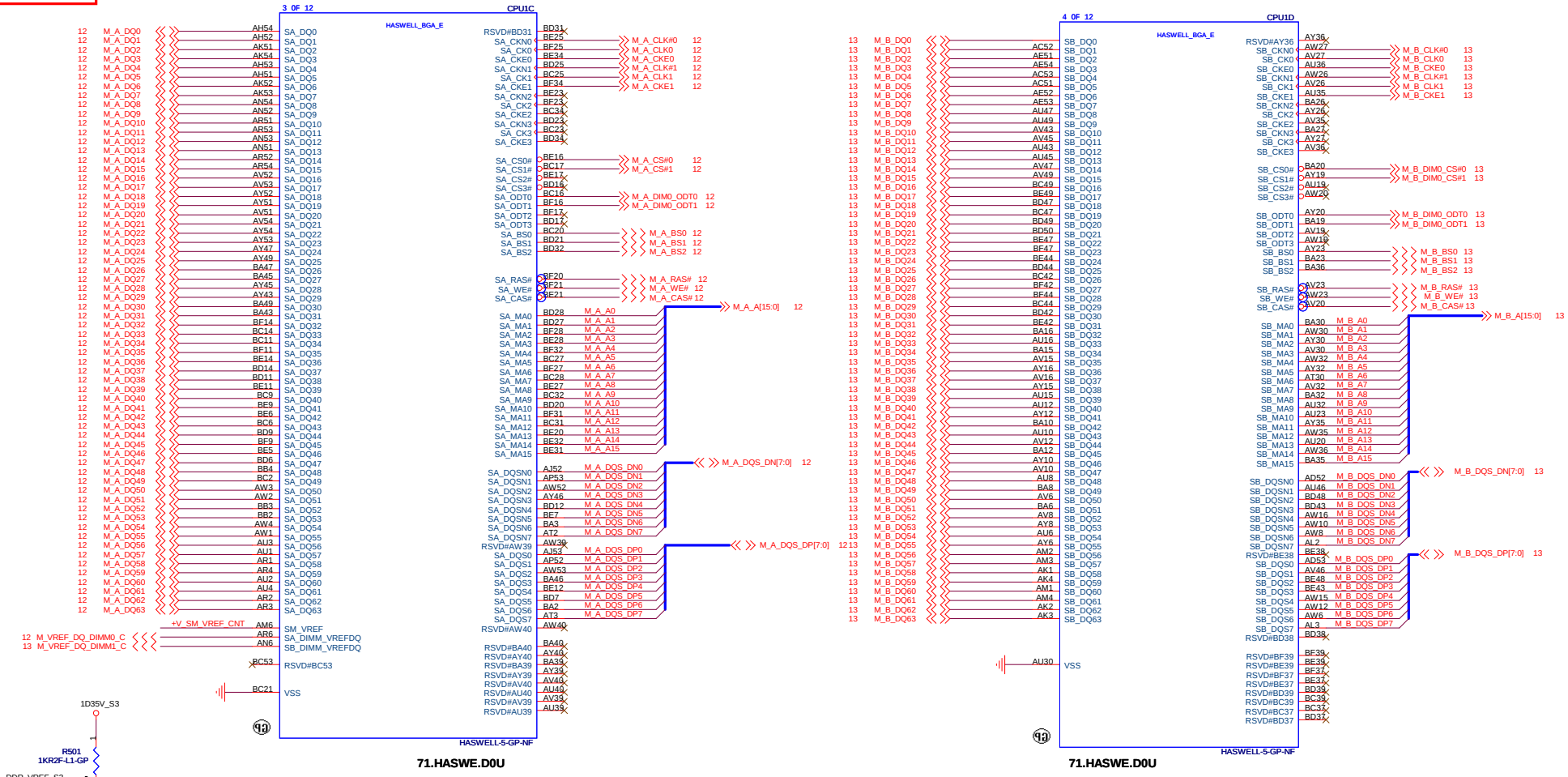
Title: **CPU (THERMAL/CLOCK/PM)**

Size	Document Number	Rev
A3	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 4 of 102

SSID = CPU



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Title: **CPU (DDR)**

Size	Document Number	Rev
Custom	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 5 of 102

SSID = CPU

PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

RN601 SRN1KJ-7-GP: CFG2, CFG4

eDP Enable	
CFG4	1:Disable 0:Enable

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

R606 1KR2J-L2-GP: CFG5, 850_840
R607 1KR2J-L2-GP: CFG6, 840
R608 1KR2J-L2-GP: CFG7, DY
R609 1KR2J-L2-GP: CFG9, DY

Reserved configuration lanes. A test point may be placed on the board for these lands.	
CFG[19:7]	

1V_CPU_CORE

CPU1K — 11 OF 12 — HASWELL_BGA_E

F22 VCC

BE4 RSVD_TP#BE4; BD3 RSVD_TP#BD3; F6 RSVD_TP#F6; G6 RSVD_TP#G6; G21 RSVD_TP#G21; G24 RSVD_TP#G24; F21 TESTLO_F21; G19 VSS; F51 VSS; F52 VSS; L52 RSVD_TP#L52; L53 RSVD_TP#L53; L51 RSVD_TP#L51; F24 RSVD_TP#F24; F25 RSVD_TP#F25; F20 TESTLO_F20

R601 49D9R2F-L1-GP: H_CPU_TESTLO_F21
R605 49D9R2F-L1-GP: H_CPU_TESTLO_F20

AG49 CFG0; AD49 CFG1; AC49 CFG2; AE49 CFG3; Y50 CFG4; AB49 CFG5; V51 CFG6; W51 CFG7; Y49 CFG8; Y54 CFG9; Y53 CFG10; W53 CFG11; U53 CFG12; V54 CFG13; R53 CFG14; R52 CFG15

CFG2, CFG4, CFG5, CFG6, CFG7, CFG9

L50 RSVD#L50; L49 RSVD#L49; E5 RSVD#E5

F1 RSVD_TP#F1; E1 RSVD_TP#E1; A5 RSVD_TP#A5; A6 RSVD_TP#A6; R54 CFG_RCOMP; Y52 CFG16; Y51 CFG17; V53 CFG18; V52 CFG19

!! Notice: CFG17/18

R603 CFG_RCOMP 49D9R2F-L1-GP

B50 RSVD#B50; AH49 RSVD#AH49; AM48 RSVD#AM48; AU27 RSVD#AU27; AU26 RSVD#AU26; BD4 RSVD#BD4; BC4 RSVD#BC4; AL6 RSVD#AL6; F8 RSVD#F8; F16 RSVD#F16; G12 RSVD_TP#G12; G10 RSVD_TP#G10; H54 VSS; H53 VSS; H51 VSS; H52 VSS; N51 RSVD#N51; G53 RSVD#G53; H50 RSVD#H50

HASWELL-5-GP-NF

71.HASWE.D0U

CPU1L — 12 OF 12 — HASWELL_BGA_E

NCTF TEST PIN: A3,A53,B2,B54,,C1,BE1, BE54,BF2,BF53

TP601 TP_A4 — A4 DAISY_CHAIN_NCTF_A4
TP602 TP_A51 — A51; NCTF_A52_B52 — A52; DAISY_CHAIN_NCTF_A51; DAISY_CHAIN_NCTF_A52

BF51 DAISY_CHAIN_NCTF_BF51; BF52 DAISY_CHAIN_NCTF_BF52 — TP_BF51 — TP606; NCTF_BE52_BF52

C2 DAISY_CHAIN_NCTF_C2 — NCTF_C1_C2; C3 DAISY_CHAIN_NCTF_C3 — NCTF_C3_B2

NCTF_B3_A3 — B3 DAISY_CHAIN_NCTF_B3; NCTF_A52_B52 — B52 DAISY_CHAIN_NCTF_B52; NCTF_A53_B53 — B53 DAISY_CHAIN_NCTF_B53

C54 DAISY_CHAIN_NCTF_C54 — NCTF_B54_C54; D1 DAISY_CHAIN_NCTF_D1 — TP_D1 — TP607

D54 DAISY_CHAIN_NCTF_D54 — TP_D54 — TP608

TP603 TP_BC1 — BC1 DAISY_CHAIN_NCTF_BC1
TP604 TP_BC54 — BC54 DAISY_CHAIN_NCTF_BC54; NCTF_BE1_BD1 — BD1 DAISY_CHAIN_NCTF_BD1

NCTF_BE54_BD54 — BD54 DAISY_CHAIN_NCTF_BD54

NCTF_BE2_BF2 — BE2 DAISY_CHAIN_NCTF_BE2; NCTF_BE3_BF3 — BE3 DAISY_CHAIN_NCTF_BE3; NCTF_BE52_BF52 — BE52 DAISY_CHAIN_NCTF_BE52; NCTF_BE53_BF53 — BE53 DAISY_CHAIN_NCTF_BE53

TP605 TP_BF4 — BF4 DAISY_CHAIN_NCTF_BF4; NCTF_BE3_BF3 — BF3 DAISY_CHAIN_NCTF_BF3

DAISY_CHAIN_NCTF#A3 A3 — NCTF_B3_A3
DAISY_CHAIN_NCTF#A53 A53 — NCTF_A53_B53
DAISY_CHAIN_NCTF#B2 B2 — NCTF_C3_B2
DAISY_CHAIN_NCTF#B54 B54 — NCTF_B54_C54
DAISY_CHAIN_NCTF#C1 C1 — NCTF_C1_C2
DAISY_CHAIN_NCTF#BE1 BE1 — NCTF_BE1_BD1
DAISY_CHAIN_NCTF#BE54 BE54 — NCTF_BE54_BD54
DAISY_CHAIN_NCTF#BF2 BF2 — NCTF_BE2_BF2
DAISY_CHAIN_NCTF#BF53 BF53 — NCTF_BE53_BF53

AN35 RSVD#AN35; AN37 RSVD#AN37; AF9 RSVD#AF9; AE9 RSVD#AE9; G14 RSVD#G14; G17 RSVD#G17; AD45 RSVD#AD45; AG45 RSVD#AG45

HASWELL-5-GP-NF

71.HASWE.D0U

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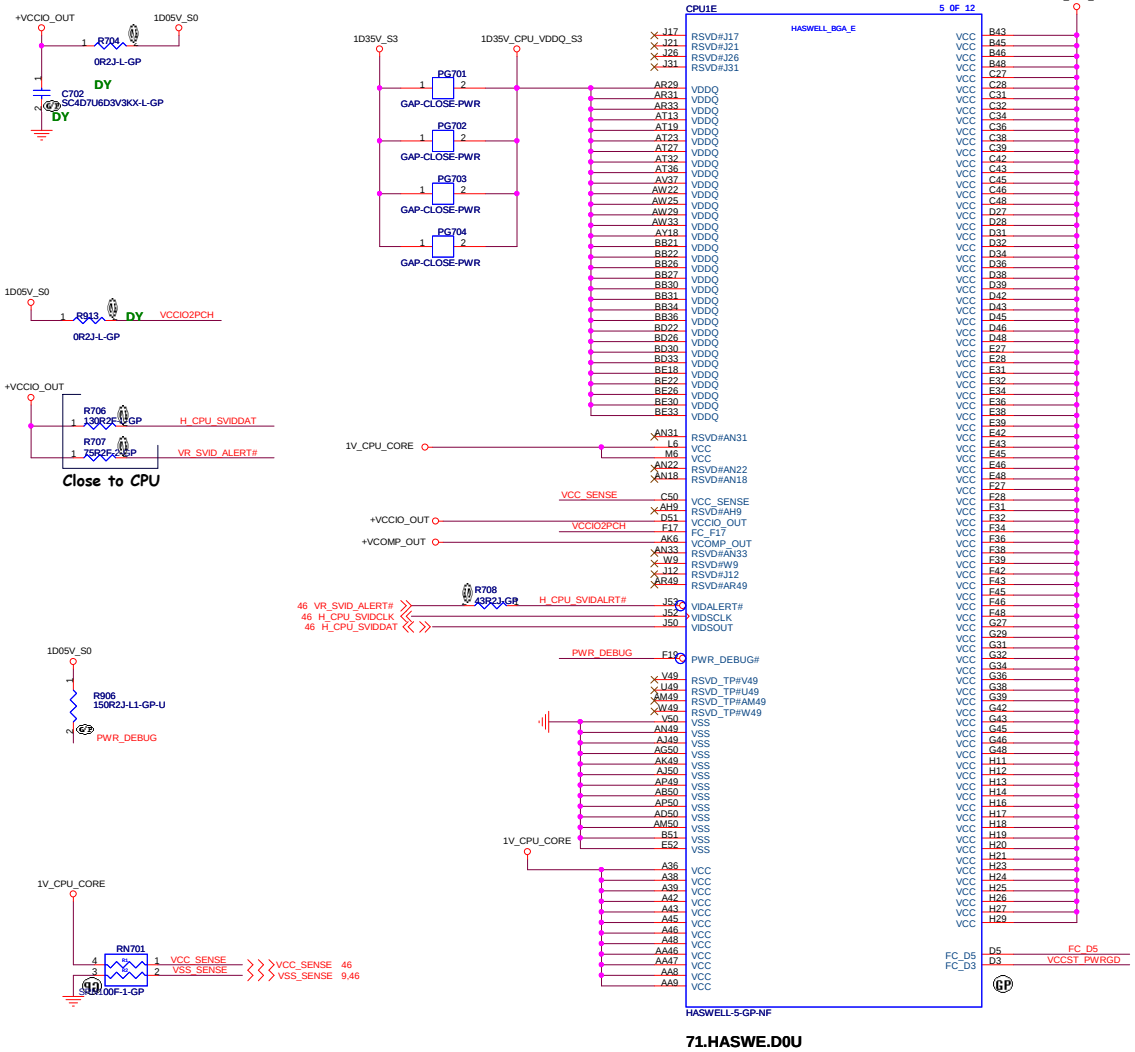
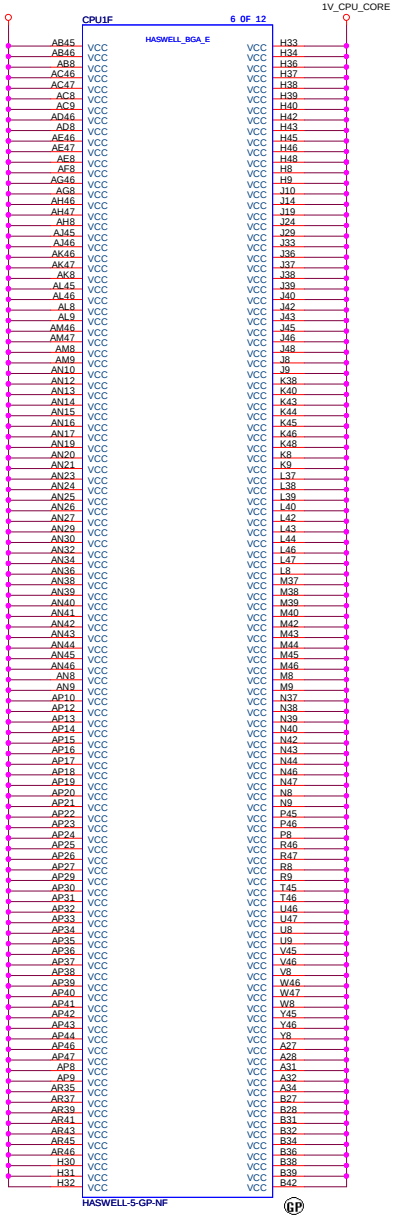
Title: **CPU (CFG)**

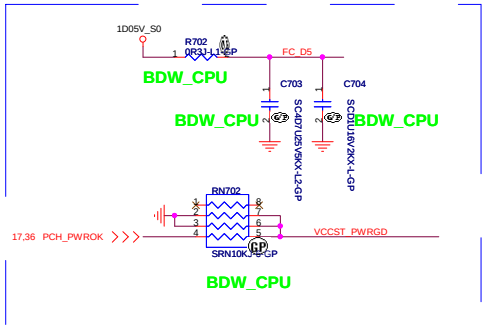
Size: Custom | Document Number: **Poseidon_860M** | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 6 of 102

SSID = CPU







For Broadwell Processor Compatibility

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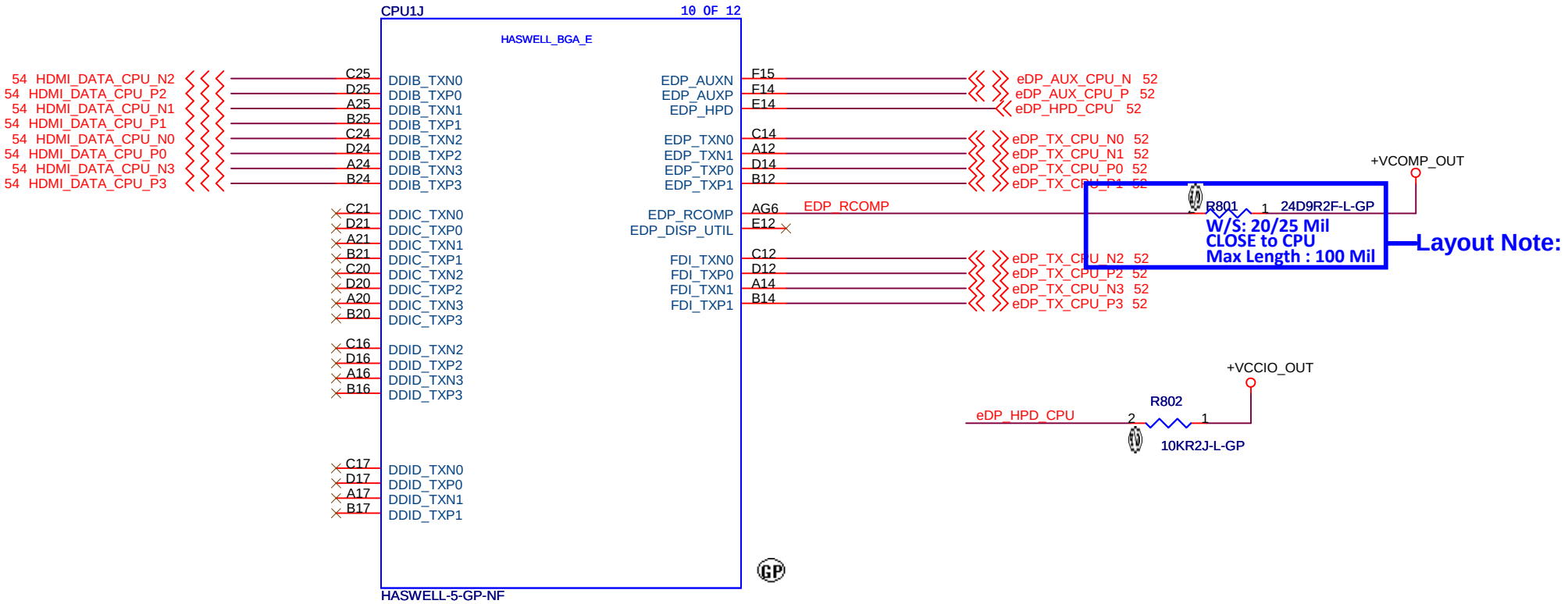
Title: CPU (VCC_CORE)

Size	Document Number	Rev
Custom	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 7 of 102

SSID = CPU

HDMI



71.HASWE.D0U

+VCOMP_OUT

R801 1 24D9R2F-L-GP

W/S: 20/25 Mil
CLOSE to CPU
Max Length : 100 Mil

Layout Note:

+VCCIO_OUT

R802

eDP_HPD_CPU 2 1

10KR2J-L-GP

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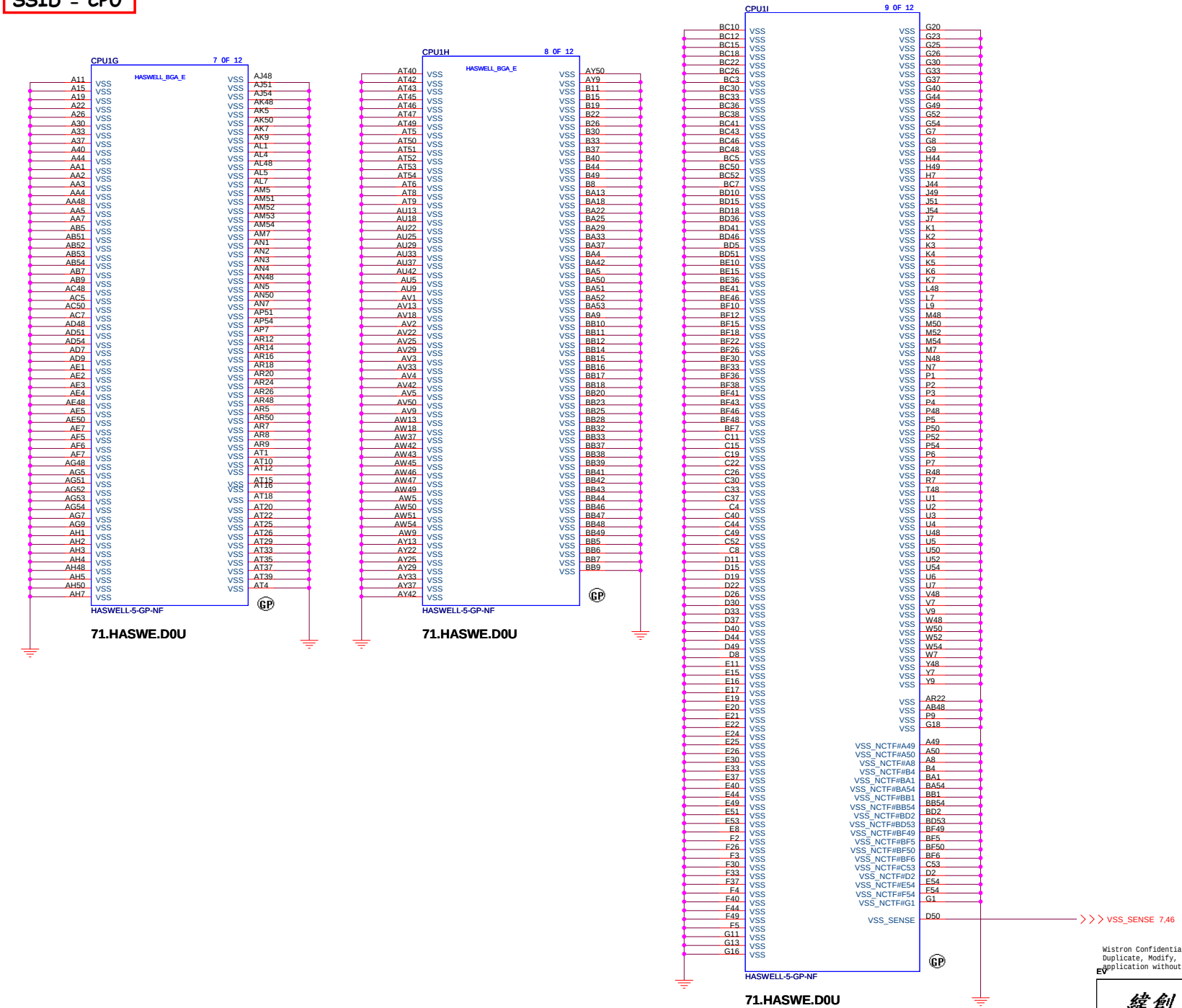
Title: CPU (DDI/EDP)		
Size: A4	Document Number: Poseidon_860M	Rev: -1
Date: Tuesday, June 17, 2014	Sheet 8 of 102	

SSID = CPU



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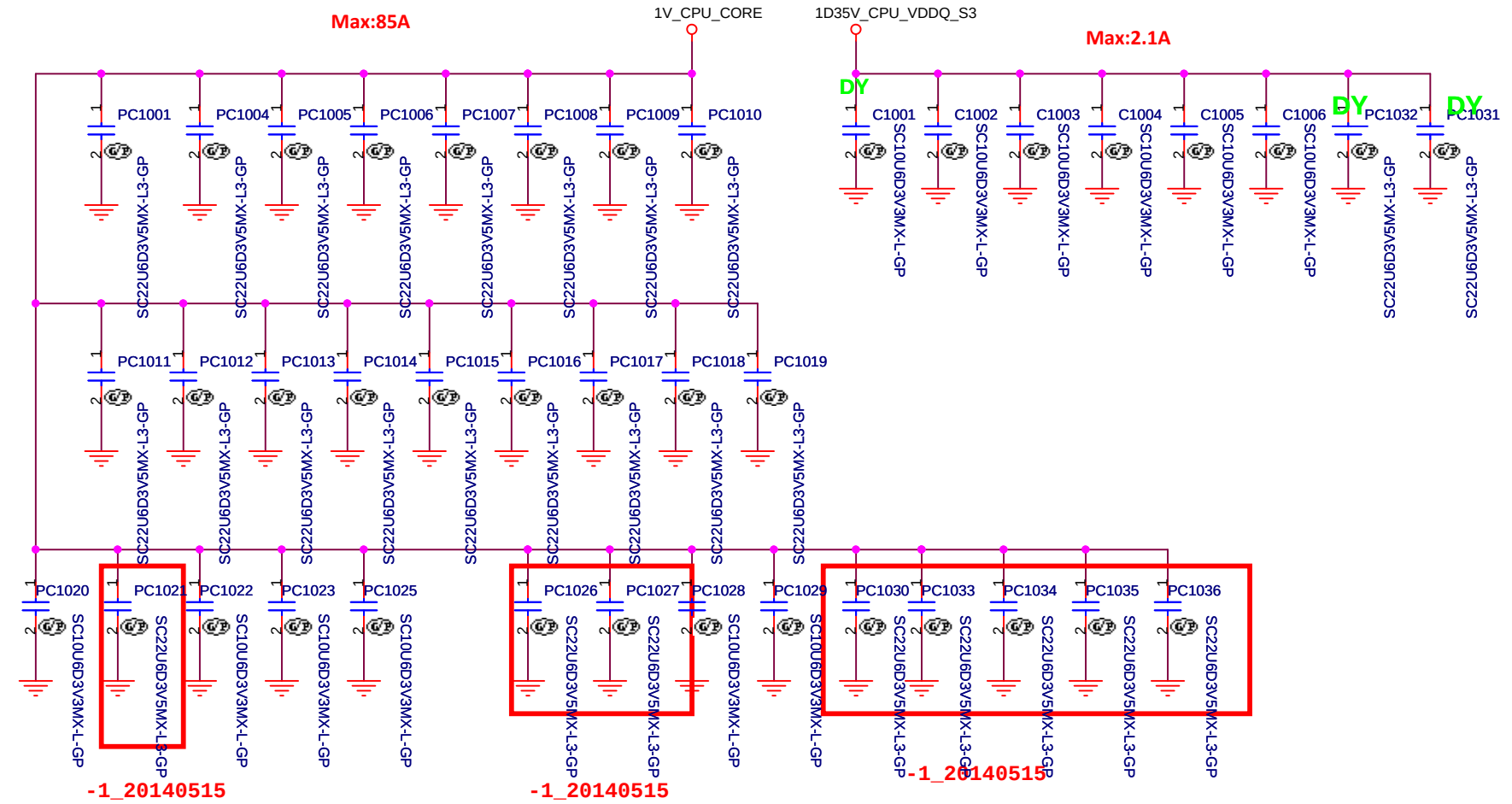
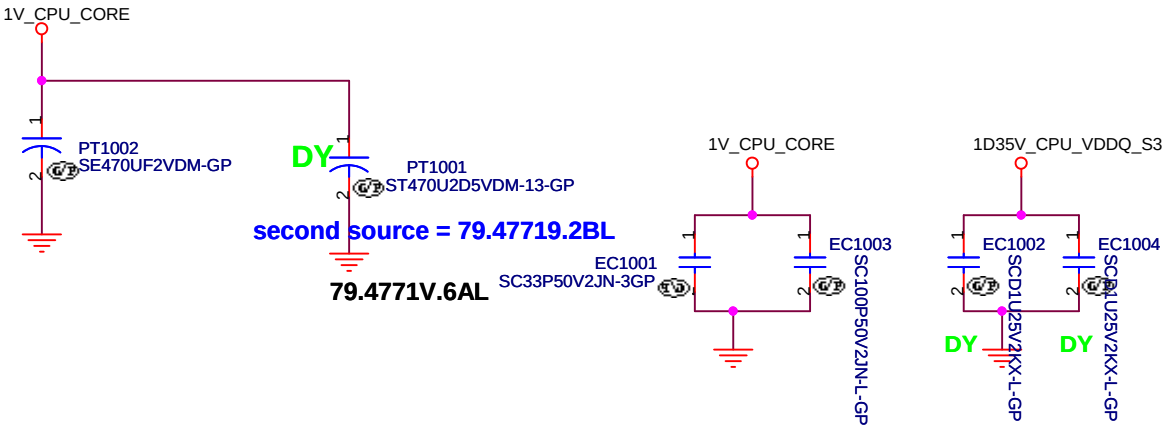
Title: CPU (VSS)

Size: Custom | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 9 of 102





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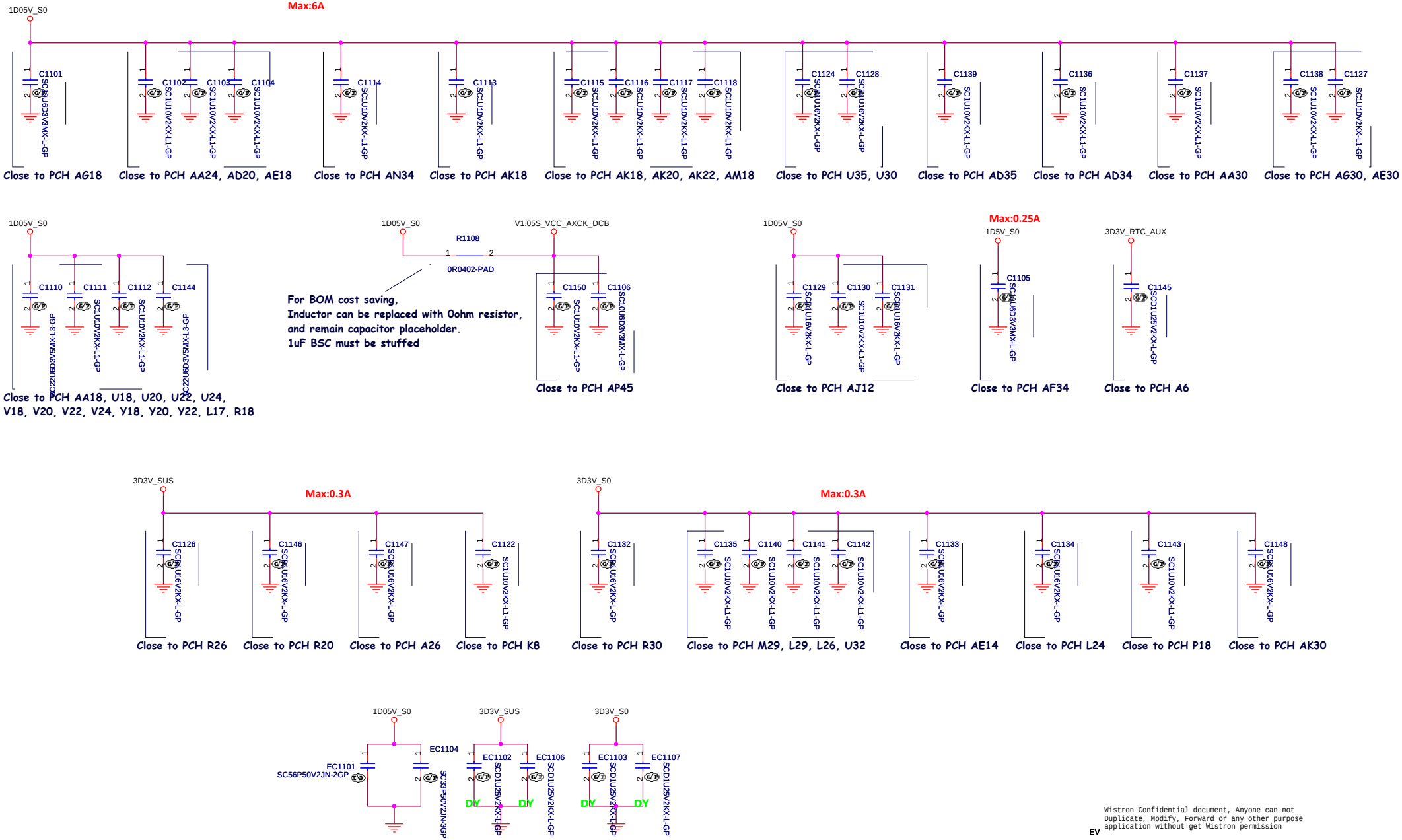
Title

CPU (Power CAP1)

Size	Document Number	Rev
A4	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 10 of 102



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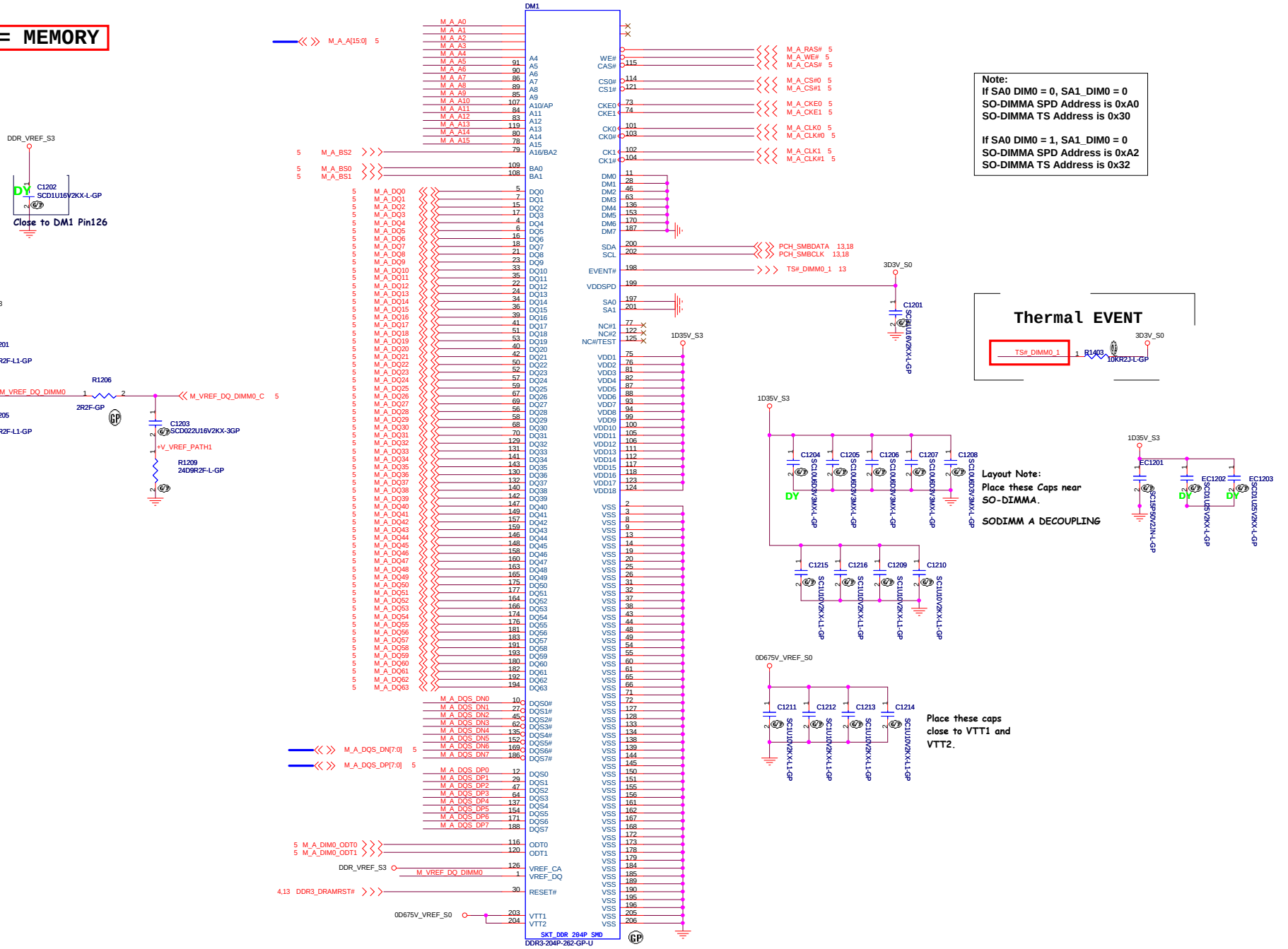
Title: **CPU (Power CAP2)**

Size	Document Number	Rev
A3	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 11 of 102

SSID = MEMORY



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

Layout Note:
Place these Caps near SO-DIMMA.

SODIMM A DECOUPLING

Place these caps close to VTT1 and VTT2.

62.10024.S21

2nd = 62.10024.M31

3rd = 62.10024.Q61

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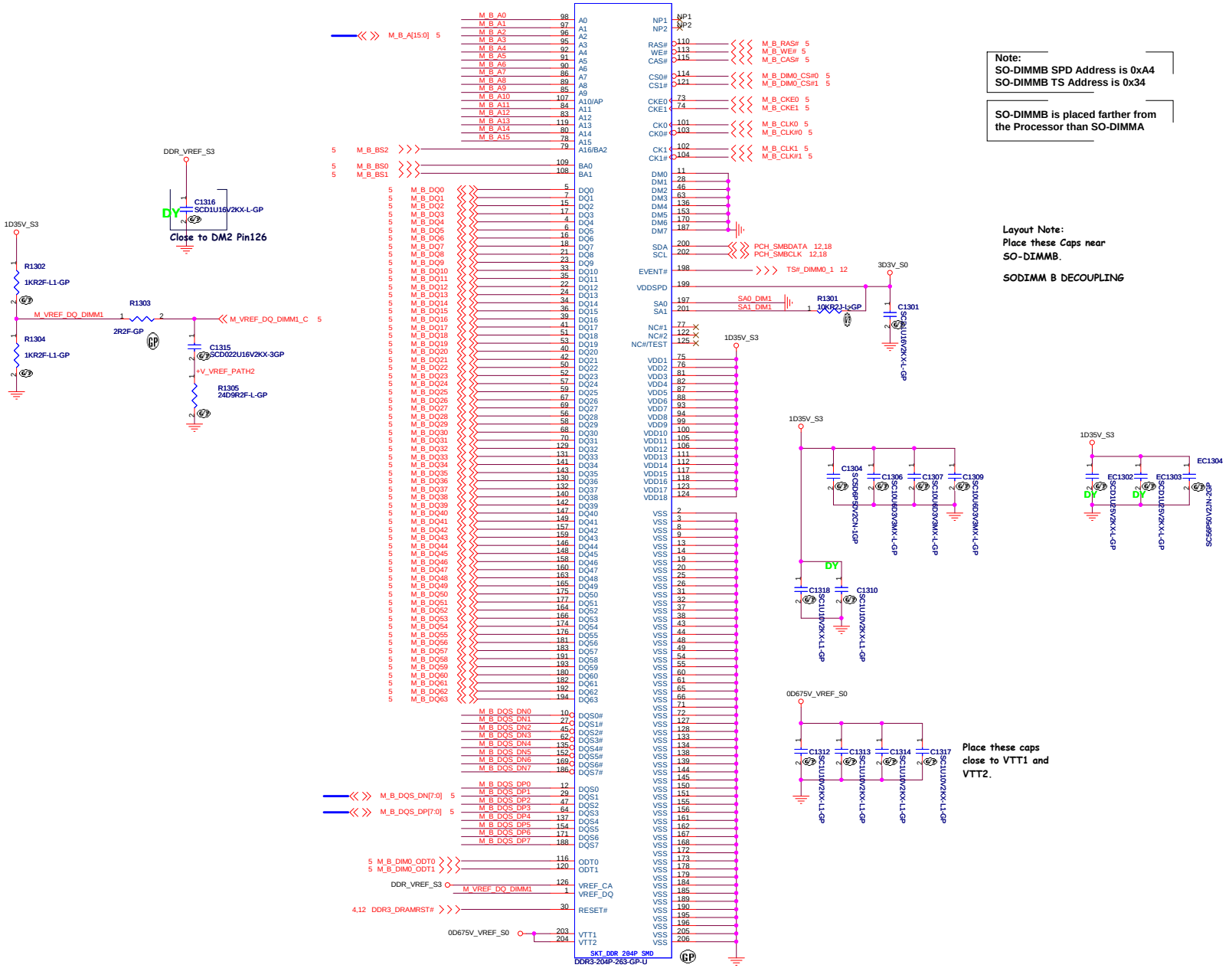
Title: **DDR3-SODIMM1**

Size: Custom | Document Number: **Poseidon_860M** | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 12 of 102

SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

Layout Note:
Place these Caps near SO-DIMMB.

SODIMM B DECOUPLING

Place these caps close to VTT1 and VTT2.

62.10024.S61

2nd = 62.10024.M51

3rd = 62.10024.Q71

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Title: DDR3-SODIMM2

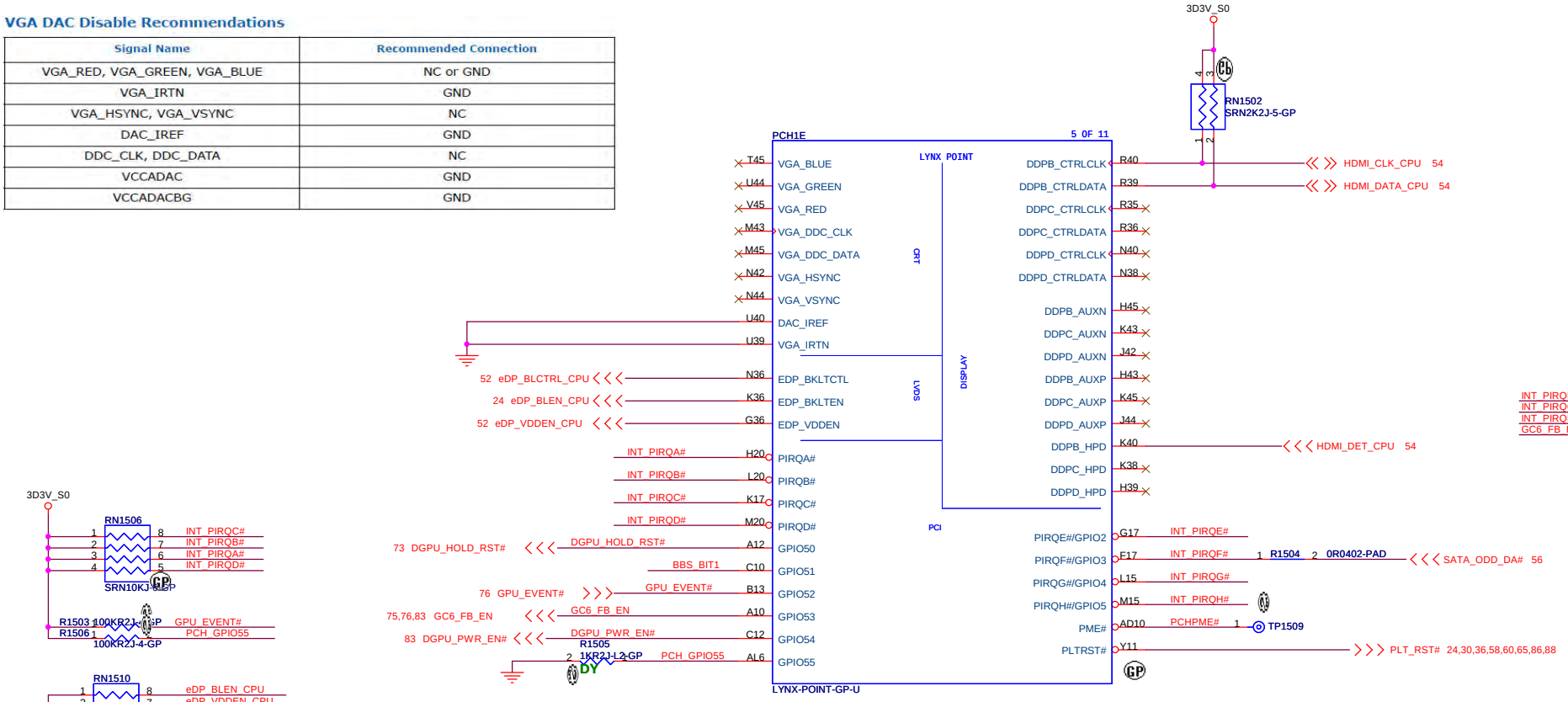
Size: Custom | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 13 of 102

SSID = CPU

VGA DAC Disable Recommendations

Signal Name	Recommended Connection
VGA_RED, VGA_GREEN, VGA_BLUE	NC or GND
VGA_IRTN	GND
VGA_HSYNC, VGA_VSYNC	NC
DAC_IREF	GND
DDC_CLK, DDC_DATA	NC
VCCADAC	GND
VCCADACBG	GND



BOOT BIOS Strap		
GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

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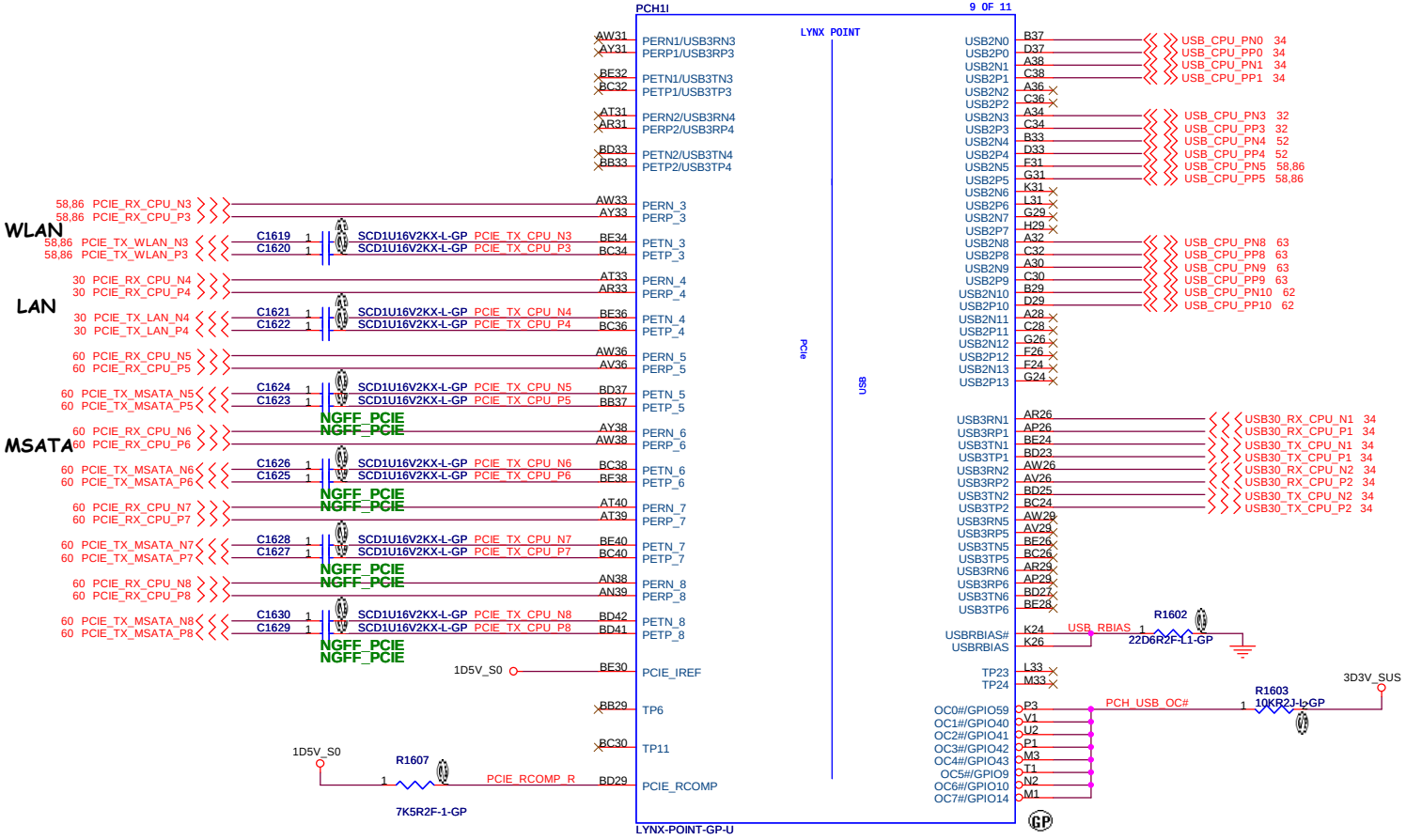
Title: **CPU(EDP SIDEBAND/GPIO/DDI)**

Size	Document Number	Rev
A3	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 15 of 102

SSID = PCH



USB Table

Pair	Device
0	USB3.0(port0)
1	USB3.0(port1)
2	
3	Card Reader
4	CCD
5	Mini Card1 (WLAN)
6	TOUCH PANEL
7	
8	USB2.0
9	USB2.0
10	TOUCH PAD
11	
12	
13	

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Title: CPU (PCI/USB)

Size: Custom | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 16 of 102

SSID = PCH

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

3D3V_RTC_AUX — R1706 330KR2J-L-GP — DSWODVREN

Intel® FDI Signal Disabling and Termination Guidelines

Signal	Description	Disable Guidelines
FDI_RXP[0:1] FDI_RXN[0:1]	Intel FDI Receive Differential Pair on PCH	Float
FDI_TXP[0:1] FDI_TXN[0:1]	Intel FDI Transmit Differential Pair on Processor	Float
FDI_CSYNC	Intel FDI Composite Sync	Connect to Processor and PCH
DISP_INT	Intel FDI Hot Plug Interrupt	Connect to Processor and PCH
FDI_RCOMP	FDI Resistor Compensation	Float
FDI_IOREF	FDI Reference Voltage	Float

PCH1B — 2 OF 11 — LYNX POINT

DMI_RXN_0 AW22 ← 3 DMI_RX_CPU_N0
DMI_RXN_1 AR20 ← 3 DMI_RX_CPU_N1
DMI_RXN_2 AP17 ← 3 DMI_RX_CPU_N2
DMI_RXN_3 AV20 ← 3 DMI_RX_CPU_N3
DMI_RXP_0 AY22 ← 3 DMI_RX_CPU_P0
DMI_RXP_1 AP20 ← 3 DMI_RX_CPU_P1
DMI_RXP_2 AR17 ← 3 DMI_RX_CPU_P2
DMI_RXP_3 AW20 ← 3 DMI_RX_CPU_P3
DMI_TXN_0 BD21 → 3 DMI_TX_CPU_N0
DMI_TXN_1 BE20 → 3 DMI_TX_CPU_N1
DMI_TXN_2 BD17 → 3 DMI_TX_CPU_N2
DMI_TXN_3 BE18 → 3 DMI_TX_CPU_N3
DMI_TXP_0 BB21 → 3 DMI_TX_CPU_P0
DMI_TXP_1 BC20 → 3 DMI_TX_CPU_P1
DMI_TXP_2 BB17 → 3 DMI_TX_CPU_P2
DMI_TXP_3 BC18 → 3 DMI_TX_CPU_P3
DMI_IREF BE16 ← 1D5V_S0
TP7 AV17
TP12 AW17
DMI_RCOMP AY17 ← R1707 7K5R2F-1-GP ← 1D5V_S0 (DS3)

FDI_RXN_0 AJ35
FDI_RXN_1 AL35
FDI_RXP_0 AJ36
FDI_RXP_1 AL36
TP5 AY45
TP10 AW44
TP15 AV45
TP16 AV43
FDI_CSYNC AL39 → FDI_CSYNC_CPU 3
FDI_INT AL40 → FDI_INT_CPU 3
FDI_IREF AT45
TP13 AU44
TP17 AU42
FDI_RCOMP AR44

System Power Management

SUSACK# R6 ← PM_SUSACK# 24 (3D3V_S0; R1710 10KR2J-L-GP)
SYS_RESET# AM1 ← SYS_RESET#
SYS_PWROK AD7 ← SYS_PWROK_R (24 S0_PWR_GOOD; R1712 0R0402-PAD)
PWROK F10 ← 7,36 PCH_PWROK
APWROK AB7 ← MEPWROK (R1714 0R0402-PAD)
DRAMPWROK H3 ← 4 PM_DRAM_PWRGD
RSMRST# J2 ← PM_RSMRST#
SUSWARN#/SUSPWRNACK/GPIO30 J4 ← PM_SUSWARN# (DS3; 24)
PWRBTN# K1 ← 24,86 PM_PWRBTN#
ACPRESENT/GPIO31 E6 ← 24 AC_PRESENT
BATLOW#/GPIO72 K7 ← BATLOW#
RI# N4 ← PM_RI#
TP21 AB10
SLP_WLAN#/GPIO29 D2

DSWVRMEN C8 ← DSWODVREN
DPWROK L13 → PCH_DPWROK
WAKE# K3 → PCIE_WAKE# 30,58,60
CLKRUN# AN7 ↔ PM_CLKRUN#_EC 24,88
SUS_STAT#/GPIO61 U7 → PM_SUS_STAT# 88
SUSCLK/GPIO62 Y6 → SUS_CLK_CPU_R (R1721 0R0402-PAD) → SUS_CLK_CPU 58,60
SLP_S5#/GPIO63 Y7
SLP_S3# H1 → PM_SLP_S3# 24,36,48,51
SLP_S4# C6 → PM_SLP_S4# 24,49
SLP_A# F3
SLP_SUS# F1 → PM_SLP_SUS# → PM_SLP_SUS# 24,38 (DS3)
PMSYNCH AY3 ↔ H_PM_SYNC 4
SLP_LAN# G5

LYNX-POINT-GP-U

Non_DS3: PM_SUSWARN# — R1719 0R0402-PAD — PM_SUSACK#

PCH_DPWROK — R1713 0R0402-PAD — PM_RSMRST# (Non_DS3)
R1716 0R2J-L-GP (DS3) → KBC_DPWROK 24
R1717 10KR2J-L-GP (DS3)

3D3V_S0 / 3D3V_S5 — RN1812 SRN10KJ-L-GP: AC_PRESENT, PCIE_WAKE#, BATLOW#, PM_CLKRUN#_EC

3D3V_SUS — R1724 10KR2J-L-GP (DY) — PM_SUSACK#

3D3V_AUX_S5 — R1709 100KR2J-4-GP (Non_DS3) — PM_RSMRST# — R1720 10KR2J-L-GP → RSMRST#_KBC 24
R1732 100KR2J-4-GP

Non_DS3: D1701 RB751V-40H-GP — 3V_5V_POK_C — R1730 0R0402-PAD → 3V_5V_POK 45
DS3: R1722 0R2J-L-GP — PM_SLP_SUS#

3D3V_SUS — RN1814 SRN10KJ-L-GP: PM_RI#, PM_SUSWARN#

EV

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DMI/FDI/PM)
Size: A3 | Document Number: Poseidon_860M | Rev: -1
Date: Tuesday, June 17, 2014 | Sheet 17 of 102

SSID = PCH

3D3V_SUS

RN1802 SRN10KJ-GP
1 PCIE_CLKRQ0#
2 EC_SW#
3 LAN_CLKREQ_CPU#
4 PEG_CLKREQ_CPU#

RN1805 SRN10KJ-GP
1 PCIE_CLKRQ6#
2 MSATA_CLKREQ_CPU#
3 PCIE_CLKRQ7#
4 PCIE_CLKRQ5#

3D3V_S0

RN1807 SRN10KJ-GP
1 PCIE_CLKRQ1#
2 WLAN_CLKREQ_CPU#

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

WLAN
58,86 WLAN_CLK_CPU#
58,86 WLAN_CLK_CPU
58,86 WLAN_CLKREQ_CPU#

LAN
30 LAN_CLK_CPU#
30 LAN_CLK_CPU
30 LAN_CLKREQ_CPU#

MSATA
60 MSATA_CLK_CPU#
60 MSATA_CLK_CPU
60 MSATA_CLKREQ_CPU#

PCH1C 3 OF 11
LYNX POINT

Y43	CLKOUT_PCIE_N_0	
Y45	CLKOUT_PCIE_P_0	
PCIE_CLKRQ0# AB1	PCIECLKRQ0#/GPIO73	
AA44	CLKOUT_PCIE_N_1	
AA42	CLKOUT_PCIE_P_1	
PCIE_CLKRQ1# AF1	PCIECLKRQ1#/GPIO18	
AB43	CLKOUT_PCIE_N_2	
AB45	CLKOUT_PCIE_P_2	
WLAN_CLKREQ_CPU# AF3	PCIECLKRQ2#/GPIO20/SMI#	
AD43	CLKOUT_PCIE_N_3	
AD45	CLKOUT_PCIE_P_3	
LAN_CLKREQ_CPU# T3	PCIECLKRQ3#/GPIO25	
AF43	CLKOUT_PCIE_N_4	
AF45	CLKOUT_PCIE_P_4	
MSATA_CLKREQ_CPU# V3	PCIECLKRQ4#/GPIO26	
AE44	CLKOUT_PCIE_N_5	
AE42	CLKOUT_PCIE_P_5	
PCIE_CLKRQ5# AA2	PCIECLKRQ5#/GPIO44	
AB40	CLKOUT_PCIE_N_6	
AB39	CLKOUT_PCIE_P_6	
PCIE_CLKRQ6# AE4	PCIECLKRQ6#/GPIO45	
AJ44	CLKOUT_PCIE_N_7	
AJ42	CLKOUT_PCIE_P_7	
PCIE_CLKRQ7# Y3	PCIECLKRQ7#/GPIO46	
AH43	CLKOUT_ITPXDP_N	
AH45	CLKOUT_ITPXDP_P	
D44	CLKOUT_33MHZ0	
E44	CLKOUT_33MHZ1	
B42	CLKOUT_33MHZ2	
F41	CLKOUT_33MHZ3	
A40	CLKOUT_33MHZ4	

CLOCK SIGNAL

AB35	CLKOUT_PEG_A_N	PEG_CLK_CPU# 73
AB36	CLKOUT_PEG_A_P	PEG_CLK_CPU 73
AF6	PEGA_CLKRQ#/GPIO47	PEG_CLKREQ_CPU# 73
Y39	CLKOUT_PEG_B_N	
Y38	CLKOUT_PEG_B_P	
U4	PEGB_CLKRQ#/GPIO56	RTC_DET# 25
AF39	CLKOUT_DMI_N	CLK_EXP_N 4
AF40	CLKOUT_DMI_P	CLK_EXP_P 4
AJ40	CLKOUT_DP_N	CK_DP_SSC_N 4
AJ39	CLKOUT_DP_P	CK_DP_SSC_P 4
AF35	CLKOUT_DPNS_N	CLK_DP_N_R 4
AF36	CLKOUT_DPNS_P	CLK_DP_P_R 4
AY24	CLKIN_DMI_N	CLK_BUF_EXP_N
AW24	CLKIN_DMI_P	CLK_BUF_EXP_P
AR24	CLKIN_GND_N	CLK_BUF_CPYCLK_N
AT24	CLKIN_GND_P	CLK_BUF_CPYCLK_P
H33	CLKIN_DOT96N	CLK_BUF_DOT96_N
G33	CLKIN_DOT96P	CLK_BUF_DOT96_P
BE6	CLKIN_SATA_N	CLK_BUF_CKSSCD_N
BC6	CLKIN_SATA_P	CLK_BUF_CKSSCD_P
F45	REFCLK14IN	CLK_BUF_REF14
D17	CLKIN_33MHZLOOPBACK	CLK_PCI_FB
AL44	XTAL25_OUT	XTAL25_IN
AM43	XTAL25_IN	XTAL25_OUT
C40	CLKOUTFLEX0/GPIO64	
F38	CLKOUTFLEX1/GPIO65	
F36	CLKOUTFLEX2/GPIO66	
F39	CLKOUTFLEX3/GPIO67	DGPU_TYPE1 20
AM45	ICLK_IREF	1D5V_S0
AD38	TP18	
AD39	TP19	
AN44	DIFFCLK_BIASREF	DIFFCLK_R

LYNX-POINT-GP-U

GPU PEG BUS

RTC_DET# 1 R1804 10KR2J-L-GP 3D3V_S5

SRN10KJ-L-GP RN1806

TP1813 CLK_33MHZ0
88 CLK_PCI_TPM R1805 22R2J-1-GP CLK_PCI_TPM_R
CLK_PCI_FB R1801 22R2J-L1-GP CLK_PCI_FB_R
65 CLK_PCI_LPC R1809 22R2J-L1-GP CLK_PCI_LPC_R
24 CLK_PCI_KBC R1808 22R2J-L1-GP CLK_PCI_KBC_R

DIFFCLK_R R1810 7K5R2F-1-GP 1D5V_S0

RN1803 SRN10KJ-6-GP
CLK_BUF_REF14
CLK_BUF_DOT96_N
CLK_BUF_DOT96_P

Need very close to PCH

RN1804 SRN10KJ-6-GP
CLK_BUF_CKSSCD_P
CLK_BUF_CKSSCD_N
CLK_BUF_EXP_P
CLK_BUF_EXP_N

XTAL25_IN
R1806 1MR2F-GP
X1801 XTAL-25MHZ-96GP
2nd = 82.30020.851
XTAL25_OUT
C1801 SC15P50V2JN-L-GP
C1802 SC15P50V2JN-L-GP

3D3V_SUS

RN1809 SRN2K2J-5-GP
SMB_CLK
SMB_DATA

RN1810 SRN2K2J-5-GP
SML0_DATA
SML0_CLK

RN1811 SRN2K2J-5-GP
SML1_CLK
SML1_DATA

RN1813 SRN10KJ-L-GP
PCH_GPIO74
PCH_GPIO60

PCH1D 4 OF 11
LYNX POINT

24,65,88 LPC_AD_CPU_P0	A20	LAD_0
24,65,88 LPC_AD_CPU_P1	C20	LAD_1
24,65,88 LPC_AD_CPU_P2	A18	LAD_2
24,65,88 LPC_AD_CPU_P3	C18	LAD_3
24,65,88 LPC_FRAME#_CPU	B21	LFRAME#
	D21	LDRQ0#
	G20	LDRQ1#/GPIO23
24,88 INT_SERIRQ	AL11	SERIRQ

LPC

24,25 SPI_CLK_CPU	AJ11	SPI_CLK
24,25 SPI_CS_CPU_N0	AJ7	SPI_CS0#
	AL7	SPI_CS1#
	AJ10	SPI_CS2#
24,25 SPI_SI_CPU	AH1	SPI_MOSI
24,25 SPI_SO_CPU	AH3	SPI_MISO
25 SPI_WP_CPU	AJ4	SPI_IO2
25 SPI_HOLD_CPU	AJ2	SPI_IO3

SPI

SMBus

	N7	SMBALERT#/GPIO11 EC_SW1#
	R10	SMBCLK SMB_CLK
	U11	SMBDATA SMB_DATA
	N8	SML0ALERT#/GPIO60 PCH_GPIO60
	U8	SML0CLK SML0_CLK
	R7	SML0DATA SML0_DATA
	H6	SML1ALERT#/PCHHOT#/GPIO74 PCH_GPIO74
	K6	SML1CLK/GPIO58 SML1_CLK 24,26,76
	N11	SML1DATA/GPIO75 SML1_DATA 24,26,76

C-Link

	AF11	CL_CLK
	AF10	CL_DATA
	AF7	CL_RST#

Thermal

	BA45	TP1
	BC45	TP2
	BE44	TP3
	BE43	TP4
	AY43	TD_IREF TS_IREF

R1818 8K2R2F-1-GP

LYNX-POINT-GP-U

3D3V_S0 R1813 10KR2J-L-GP INT_SERIRQ

3D3V_S0 RN1808 SRN2K2J-5-GP

Q1801 DN7002KDW-GP
84.2N702.A3F
2nd = 75.00601.07C

SMB_DATA PCH_SMBDATA 12,13
SMB_CLK PCH_SMBCLK 12,13

EV

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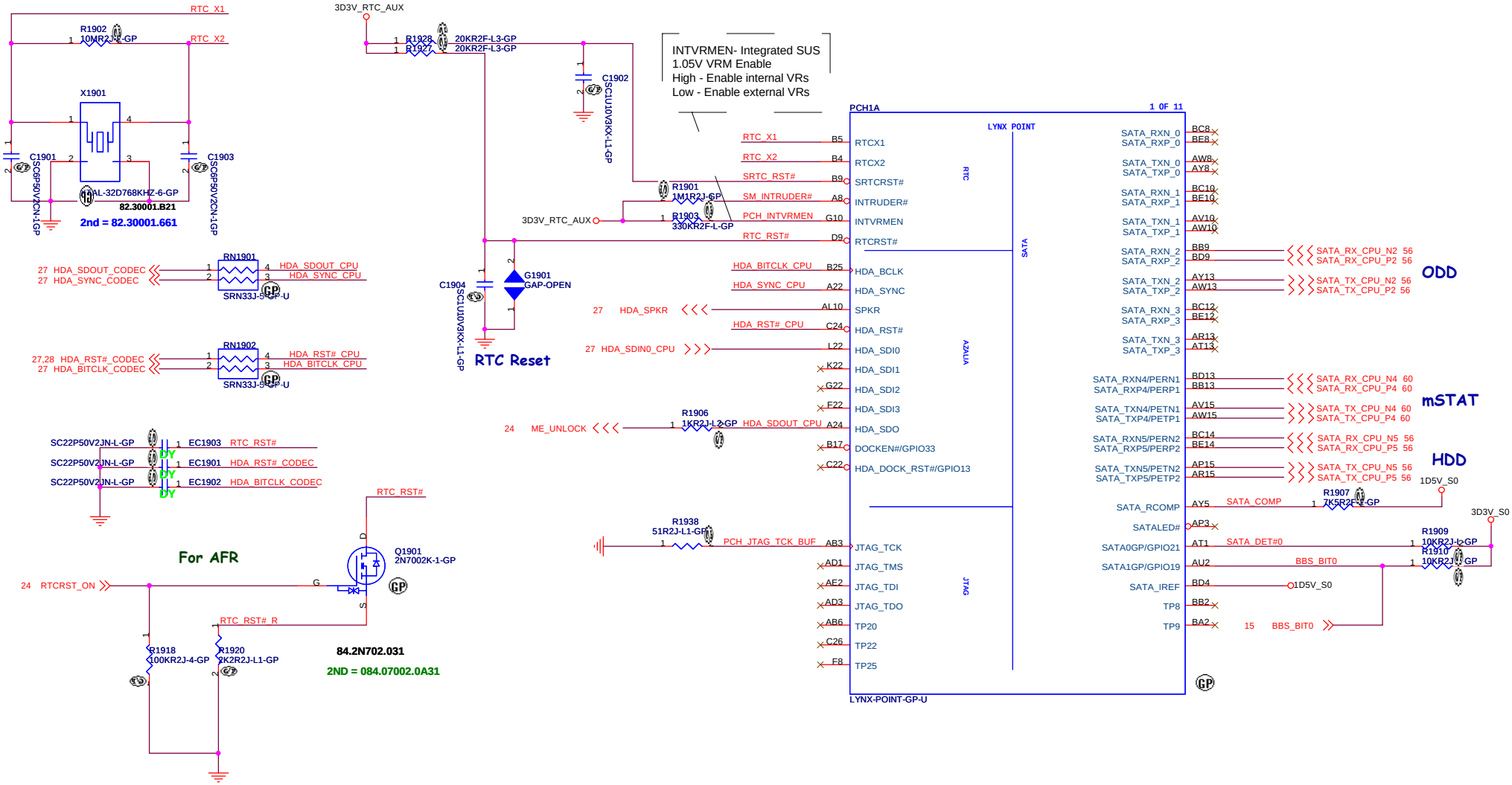
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCI-E/SMBUS/CLOCK/CL)

Size: Custom | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 18 of 102

SSID = PCH



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

EV

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (RTC/LPC/SATA/HDA)**

Size	Document Number	Rev
Custom	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 19 of 102

SSID = PCH

3D3V_S5 / 3D3V_S0 — RN2004 — SRN10KJ-6-GP
- PCH_GPIO12
- PCH_GPIO27
- H_A20GATE
- H_RCIN#

3D3V_SUS / 3D3V_S0 — RN2005 — SRN10KJ-6-GP
- PCH_GPIO24
- PCH_GPIO8
- PCH_GPIO57
- TOUCH_DET#

3D3V_S0 — RN2002 — SRN10KJ-6-GP
- PCH_GPIO6
- EC_SMI#
- EC_SCI#
- PCH_GPIO48

RN2003 — SRN10KJ-6-GP
- PCH_GPIO38
- PCH_GPIO49
- MSATA_PEDET
- SATA_ODD_PRSNT#

3D3V_S0 — R2008 1KR2F-L-2-GP — S_GPIO

PCH1F — 6 OF 11 — LYNX POINT — LYNX-POINT-GP-U

	AT8	BMBUSY#/GPIO0
24 EC_SMI#	F13	TACH1/GPIO1
PCH_GPIO6	A14	TACH2/GPIO6
24 EC_SCI#	G15	TACH3/GPIO7
PCH_GPIO8	Y1	GPIO8
PCH_GPIO12	K13	LAN_PHY_PWR_CTRL/GPIO12
	AB11	GPIO15
60 MSATA_PEDET	AN2	SATA4GP/GPIO16
24,82,83 DGPU_PWROK	C14	TACH0/GPIO17
TOUCH_DET#	BB4	SCLOCK/GPIO22
PCH_GPIO24	Y10	GPIO24
PCH_GPIO27	R11	GPIO27
PCH_GPIO28	AD11	GPIO28
PSW_CLR#	AN6	GPIO34
	AP1	GPIO35/NMI#
56 SATA_ODD_PRSNT#	AT3	SATA2GP/GPIO36
PCH_GPIO37	AK1	SATA3GP/GPIO37
PCH_GPIO38	AT7	SLOAD/GPIO38
PCH_GPIO39	AM3	SDATAOUT0/GPIO39
PCH_GPIO48	AN4	SDATAOUT1/GPIO48
PCH_GPIO49	AK3	SATA5GP/GPIO49
PCH_GPIO57	U12	GPIO57
56 SATA_ODD_PWRGT	C16	TACH4/GPIO68
DGPU_TYPE2	D13	TACH5/GPIO69
	G13	TACH6/GPIO70
	H15	TACH7/GPIO71

CPU/Misc

TP14	AN10	H_A20GATE → H_A20GATE 24
PECI	AY1	PCH_PECI → 1 TP2001
RCIN#	AT6	H_RCIN# 24
PROCPWRGD	AV3	H_CPUPWRGD 4,36,86
THRMTRIP#	AV1	PCH_THERMTRIP_R → R2004 390R2F-2GP → H_THERMTRIP# 4,36
PLTRST_PROC#	AU4	PCH_PLTRST_CPU 4
VSS	N10	

GPIO

NCTF

BE41	VSS
BE5	VSS
C45	VSS
A5	VSS

VSS: A2, A41, A43, A44, B1, B2, B44, B45, BA1, BC1, BD1, BD2, BD44, BD45, BE2, BE3, D1, E1, E45, A4

SC33P50V2JN-3GP — EC2003 H_CPUPWRGD — DY
SC33P50V2JN-3GP — EC2002 DGPU_PWROK — DY

3D3V_S0 — 10KR2J-L-GP R2030 — PSW_CLR# — G2002 GAP-OPEN

Pass Word Clear

PCH_GPIO37 — R2020 10KR2J-L-GP (DY) — 3D3V_S0
PCH_GPIO37 — R2029 100KR2J-4-GP

TLS Confidentiality
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality)

R2014 1KR2J-L2-GP — DY — PCH_GPIO28

PLL ON DIE VR ENABLE
ENABLED -- HIGH (R2013 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2013 STUFFED)

3D3V_S0 / 3D3V_S0

R2034 10KR2J-L-GP	R2032 10KR2J-L-GP	
840	840_850	DGPU_TYPE2
R2033 10KR2J-L-GP	R2031 10KR2J-L-GP	DGPU_TYPE1 18
860_850	860	

DGPU_TYPE1:DGPU_TYPE2
HH:840M LL=860
HL:850M LH=RESERE

PCH_GPIO8 — R2010 10KR2J-L-GP — DY

3D3V_S0 — R2011 10KR2J-L-GP — PCH_GPIO39
R2016 10KR2J-L-GP — DY

Pull up --> External GFX
Pull down --> Internal GFX

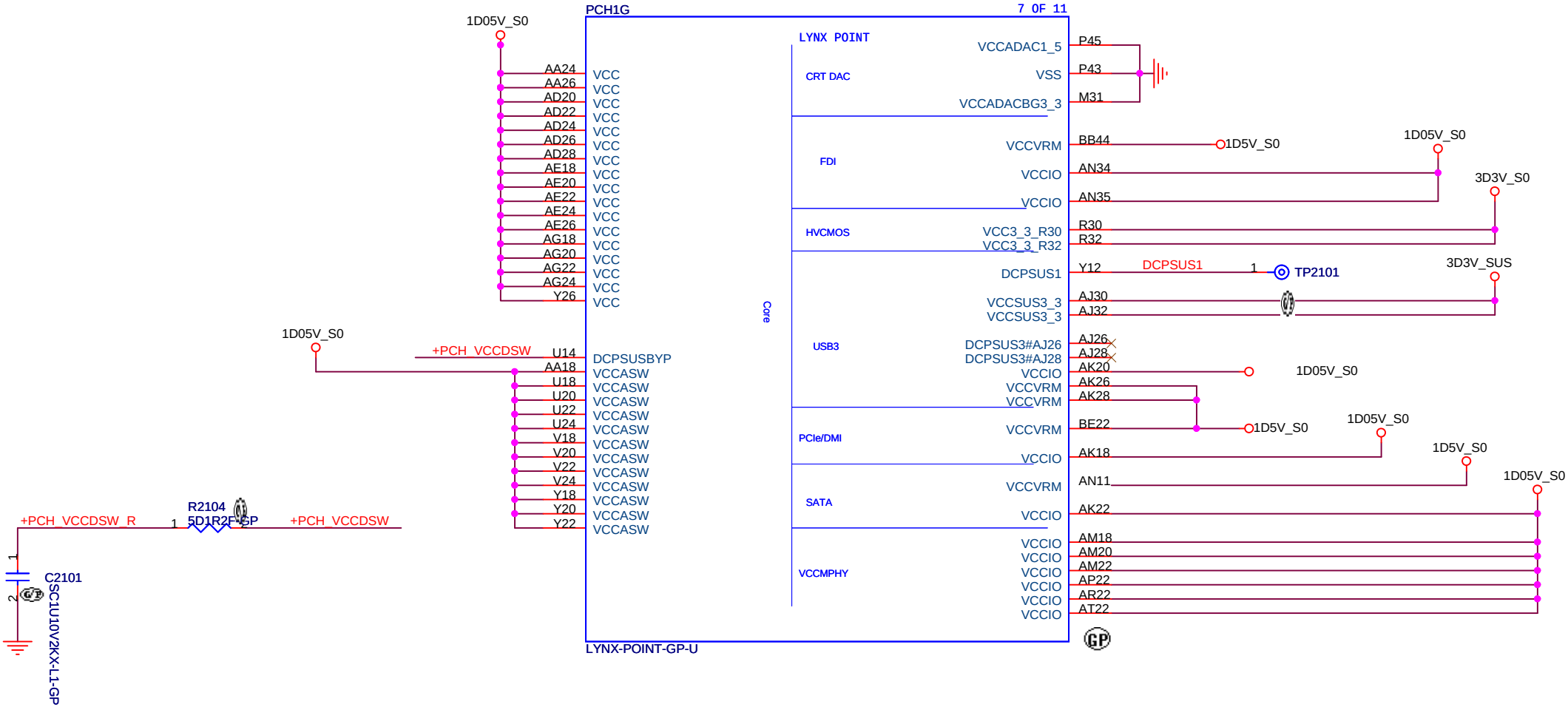
EV

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (GPIO/MISC)**

Size	Document Number	Rev
A3	Poseidon 860M	-1

Date: Tuesday, June 17, 2014 Sheet 20 of 102



EV

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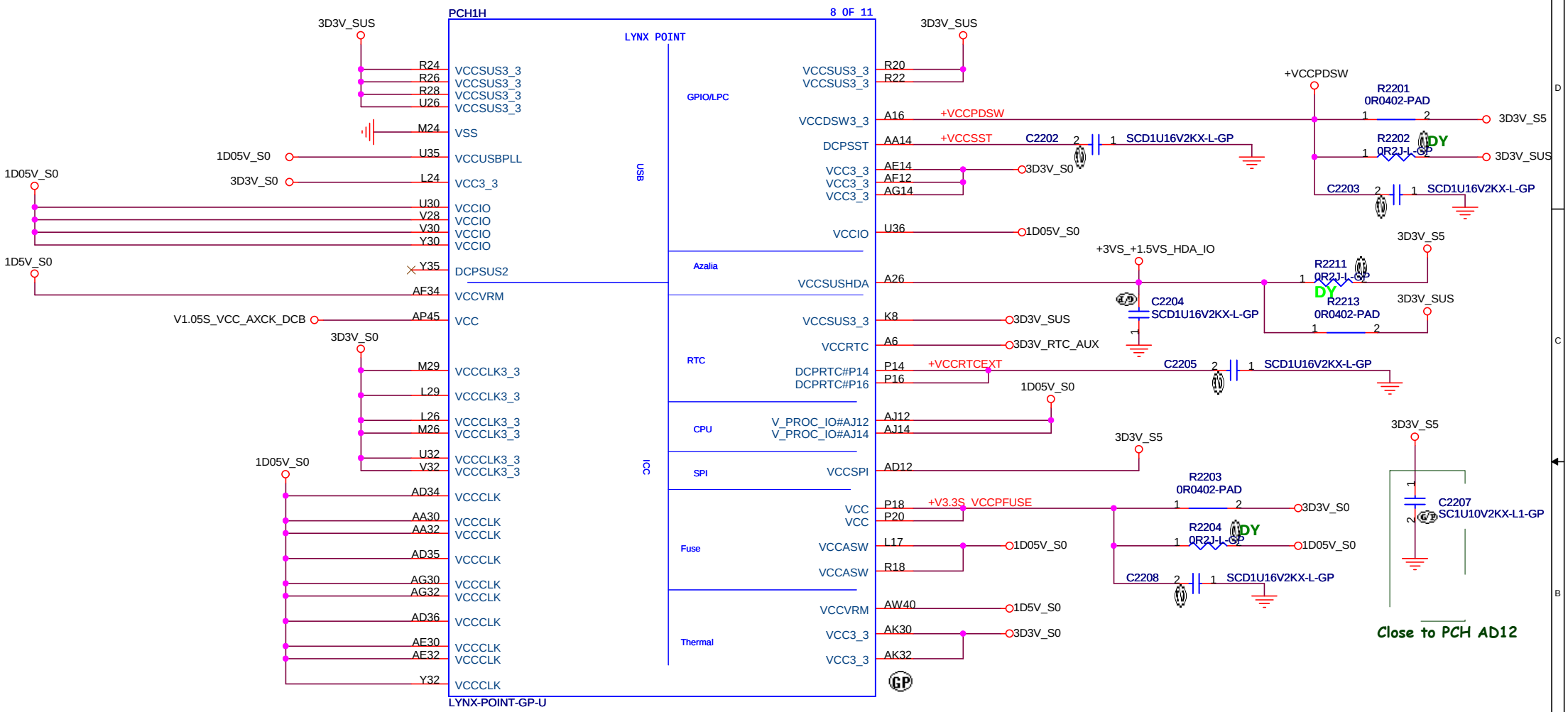
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (POWER1)

Size	Document Number	Rev
A4	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 21 of 102



EV

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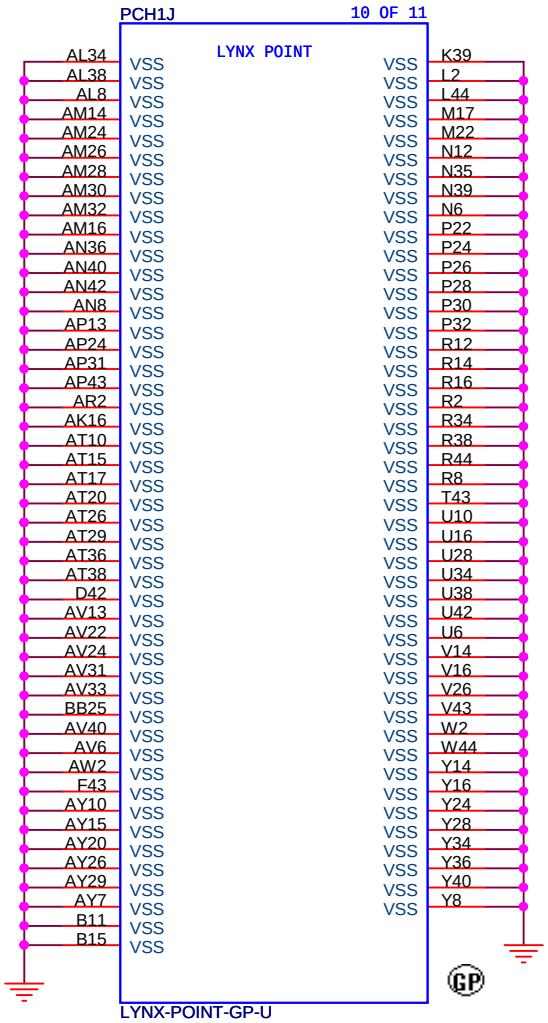
Taipei Hsien 221, Taiwan, R.O.C.

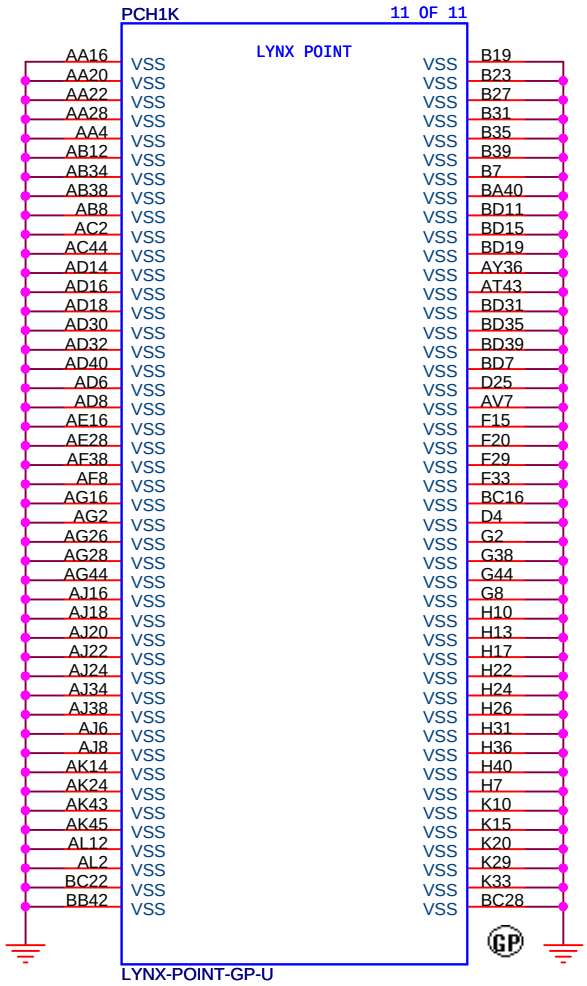
Title: CPU (RSVD)

Size: Custom | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 22 of 102

SSID = PCH





EV

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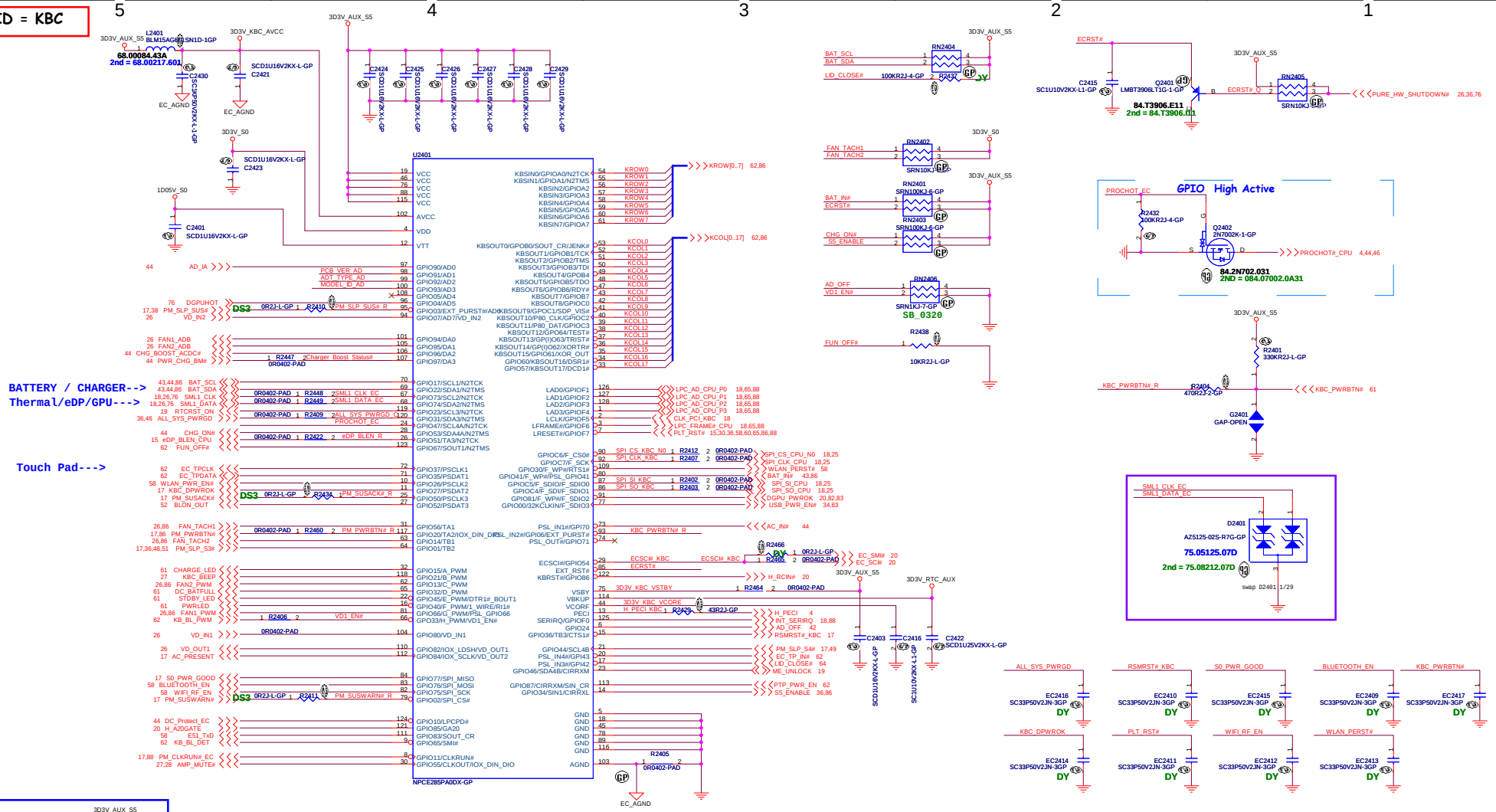
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

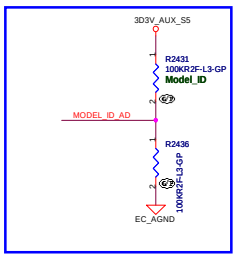
Title: ***CPU (VSS)***

Size	Document Number	Rev
A4	Poseidon_860M	-1

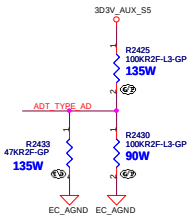
Date: Tuesday, June 17, 2014 Sheet 23 of 102

SSID = KBC

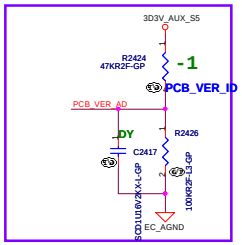




Model_ID	Pull-Low Register	Pull-High Register	Typical Voltage
VA30	100.0 K	10.0 K	3.000 V
Hades UMA	100.0 K	20.0 K	2.750 V
Hades DIS 840	100.0 K	33.0 K	2.481 V
Hades DIS 850	100.0 K	47.0 K	2.245 V
Poseidon UMA	100.0 K	64.9 K	2.001 V
Poseidon DIS 840	100.0 K	76.8 K	1.867 V
Poseidon DIS 860	100.0 K	100.0 K	1.650 V
Poseidon DIS 850	100.0 K	143.0 K	1.358 V
Reserved for project use	100.0 K	174.0 K	1.204 V
Reserved for project use	100.0 K	215.0 K	1.048 V



ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V			>= 3.000 V	
90W	100.0 K	N/A	0.000 V				< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.3055	0.2946	>= 0.150 V	< 0.425 V
40W	20.0 K	100.0 K	0.550 V	0.5592	0.5409	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.8312	0.8065	>= 0.684 V	< 0.937 V
130W	47.0 K	100.0 K	1.055 V	1.0695	1.0408	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.3146	1.2831	>= 1.177 V	< 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.4497	1.4173	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.542 V	< 1.842 V



PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	>= 0.524 V	< 1.126 V

EV

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_NPCE285PA0DX

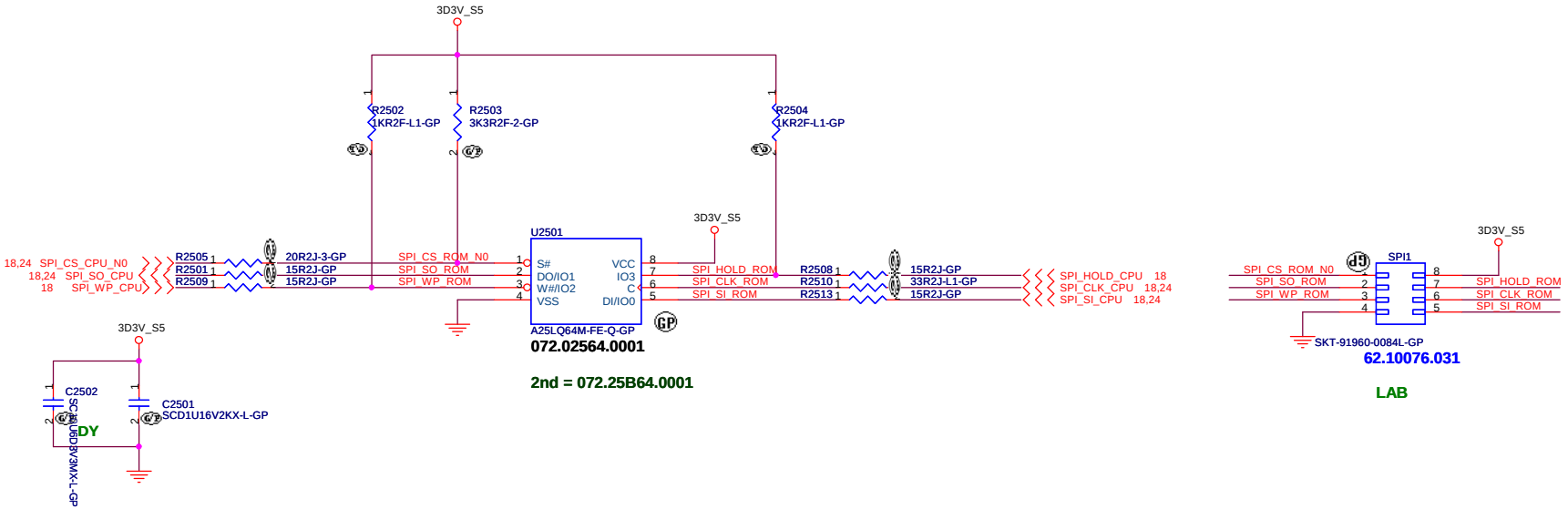
Size: Custom | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 24 of 102

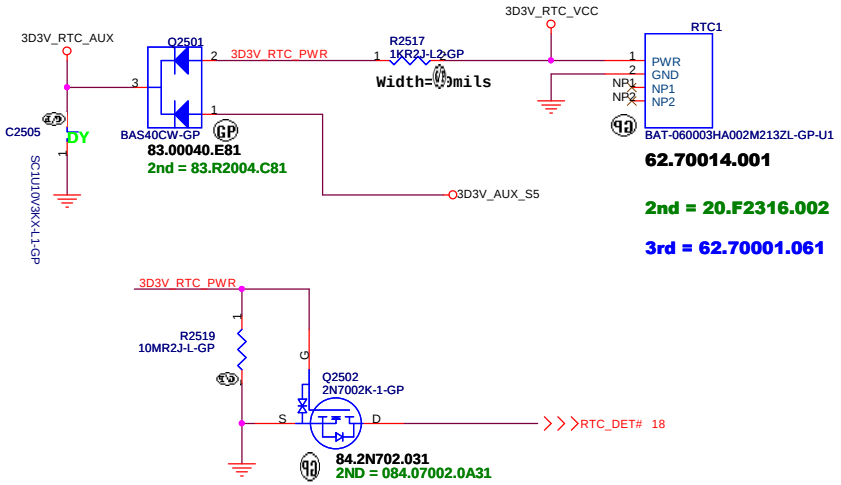
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil



SSID = RBAT



EV

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

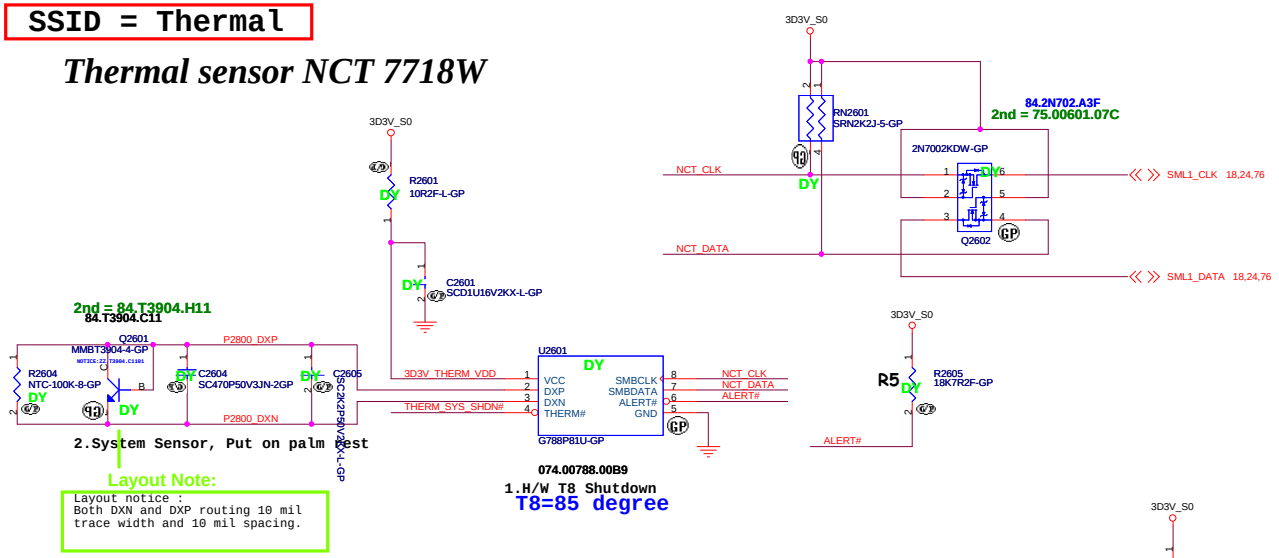
Title: *Flash(KBC+PCH)/RTC*

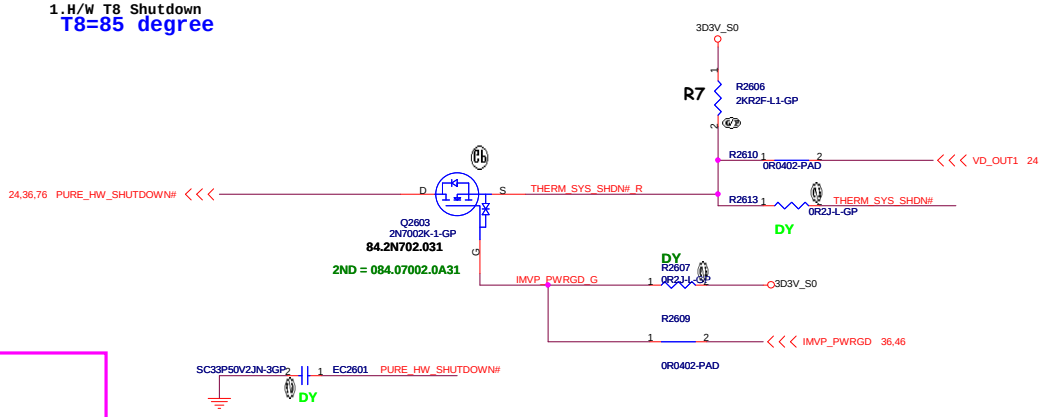
Size	Document Number	Rev
A3	Poseidon_860M	-1

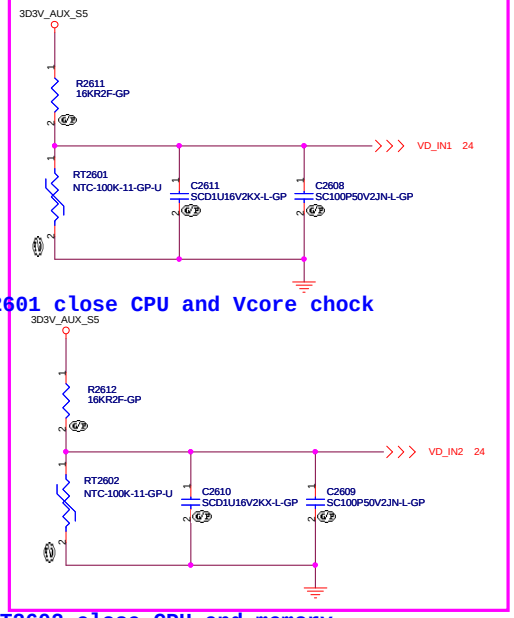
Date: Tuesday, June 17, 2014 Sheet 25 of 102

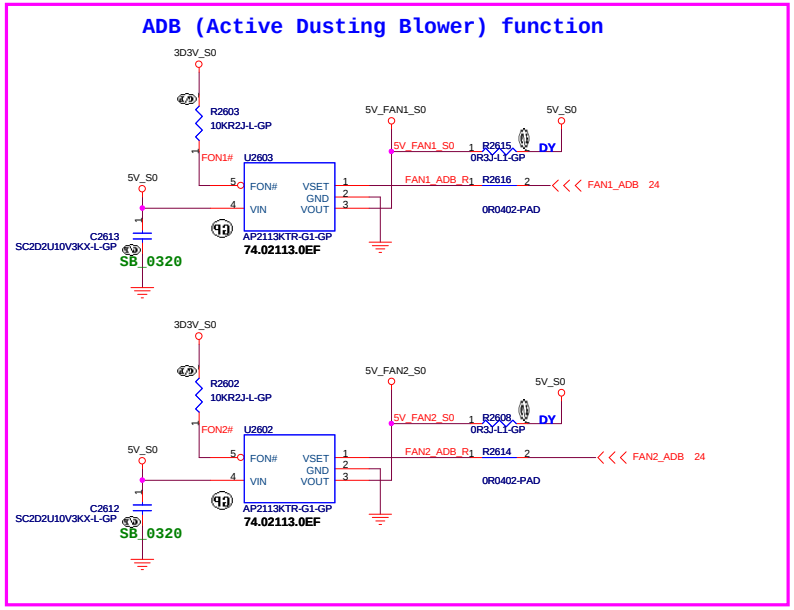
SSID = Thermal

Thermal sensor NCT 7718W

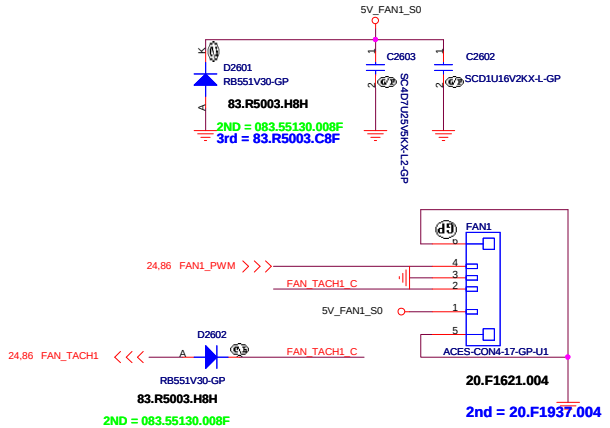




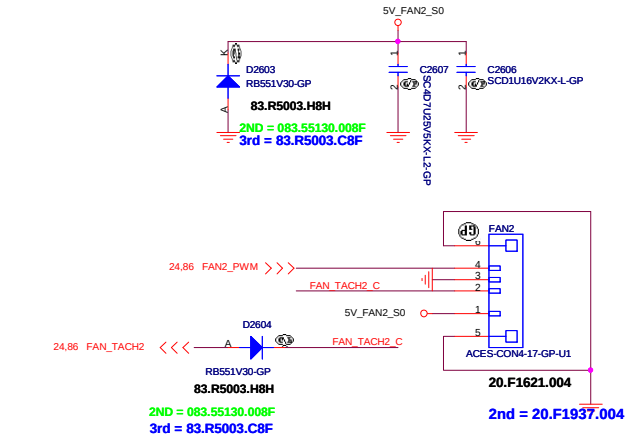




Layout 15 mil



Layout 15 mil



ALERT# /T_CRIT#
Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T8=85 degree T_CRIT temperature strapping point

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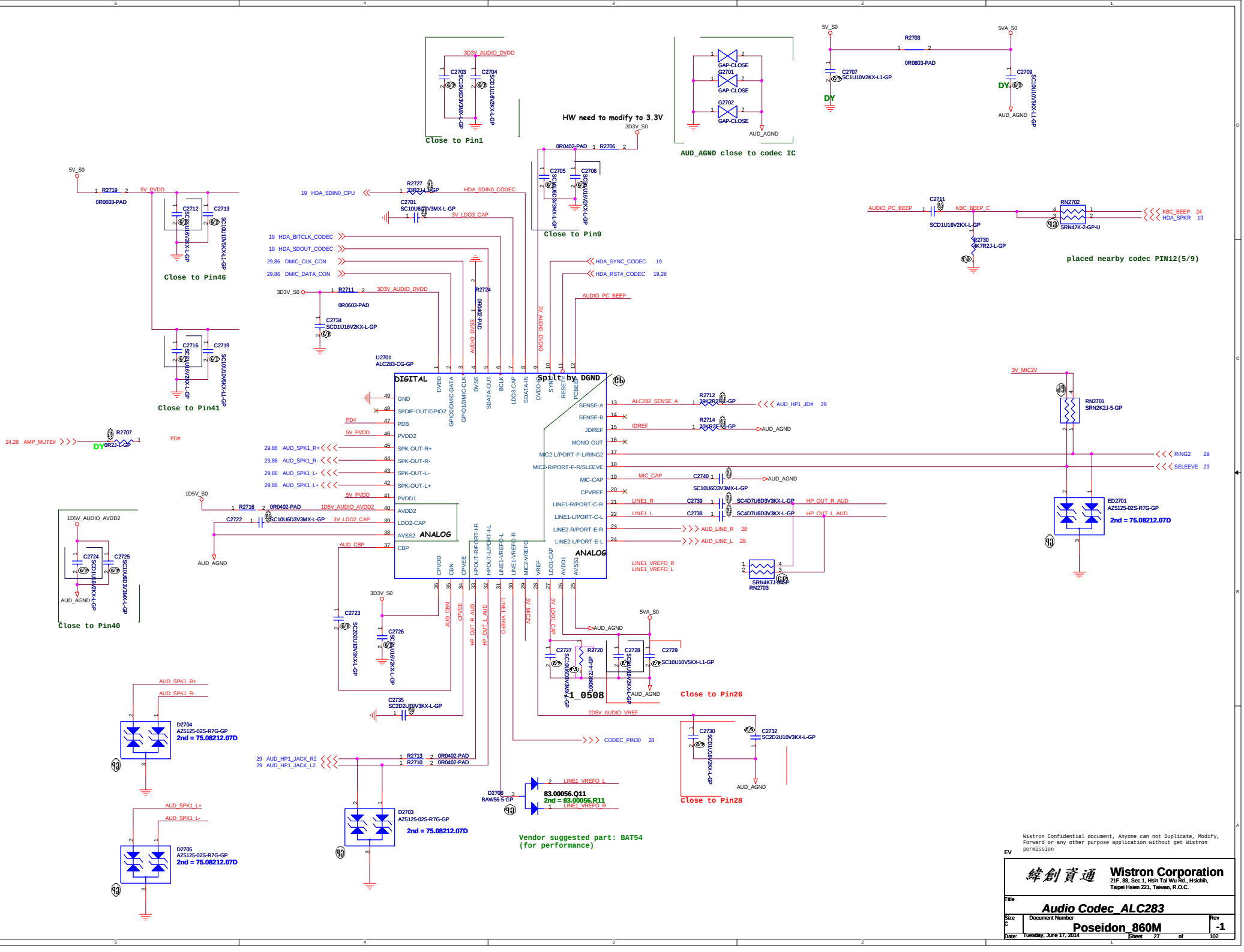
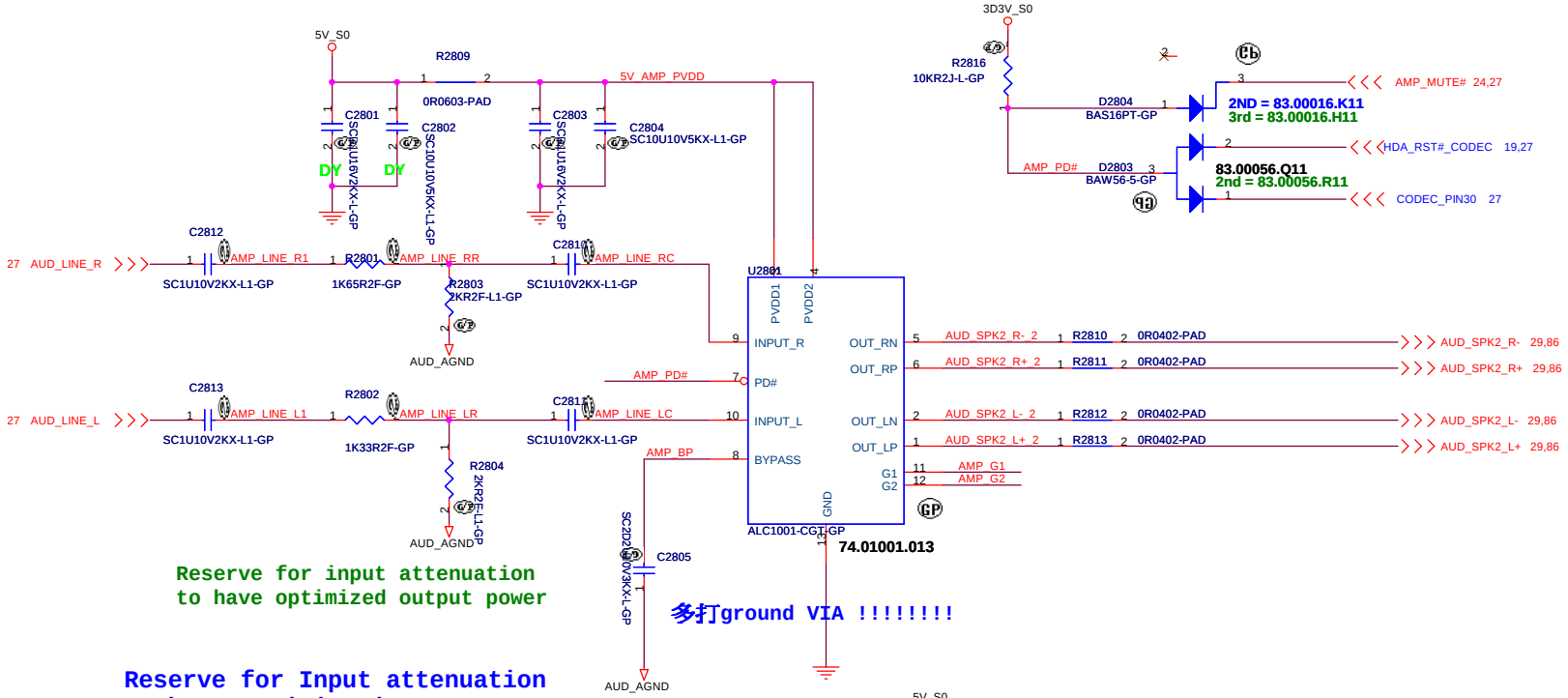
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal 7718/Fan Controllor P2793*

Size: Custom | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 26 of 102





Reserve for input attenuation to have optimized output power

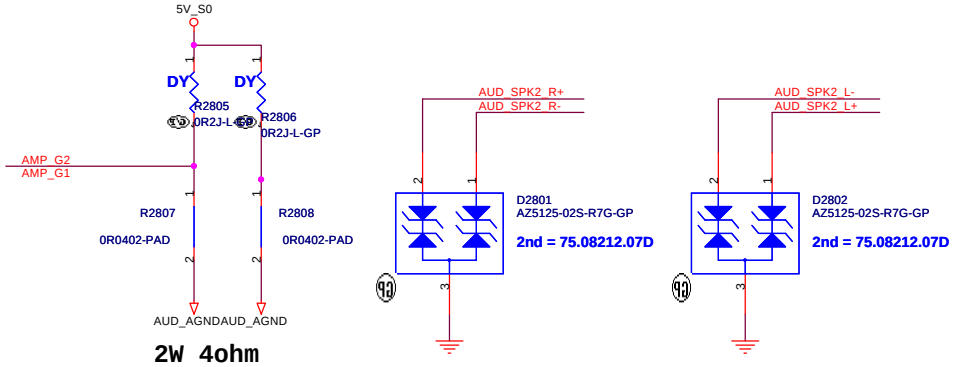
多打ground VIA !!!!!!!!

Reserve for Input attenuation To have optimization output power

Table 6. Amplifier Gain

G2	G1	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

*Condition is at 5V/4Ohm



2W 4ohm

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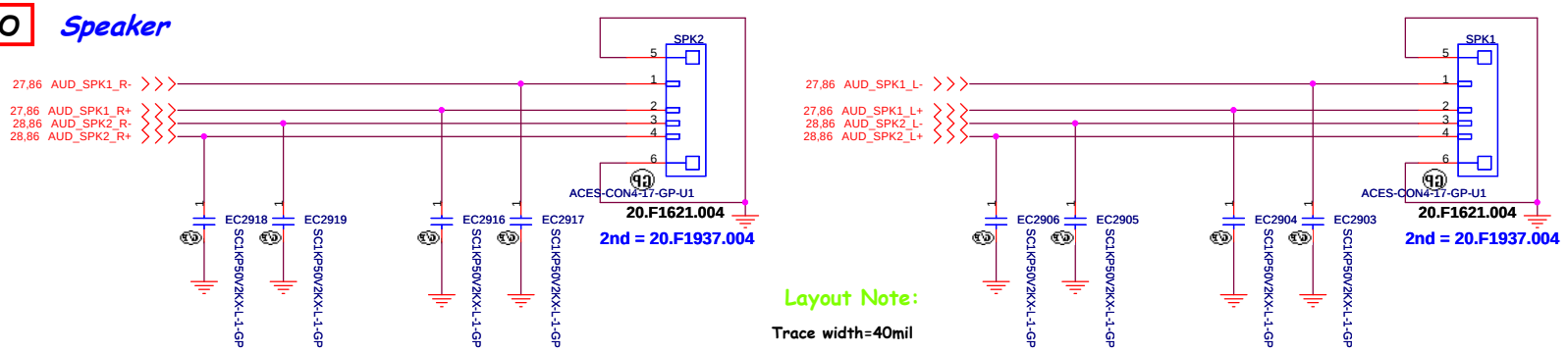
Title: ***Audio AMP_1001***

Size	Document Number	Rev
A3	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 28 of 102

SSID = AUDIO

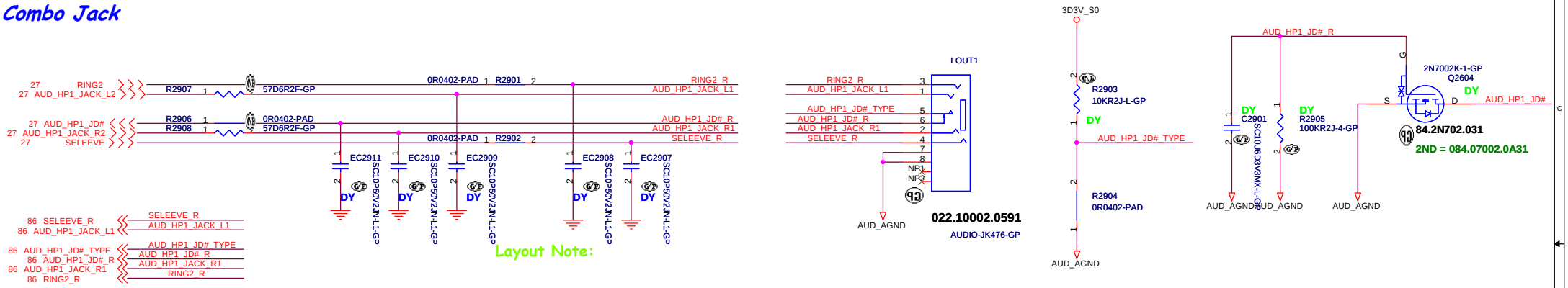
Speaker



Layout Note:

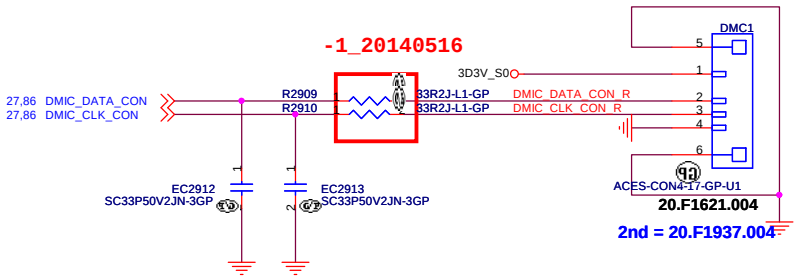
Trace width=40mil

Combo Jack



Layout Note:

DMIC



EV

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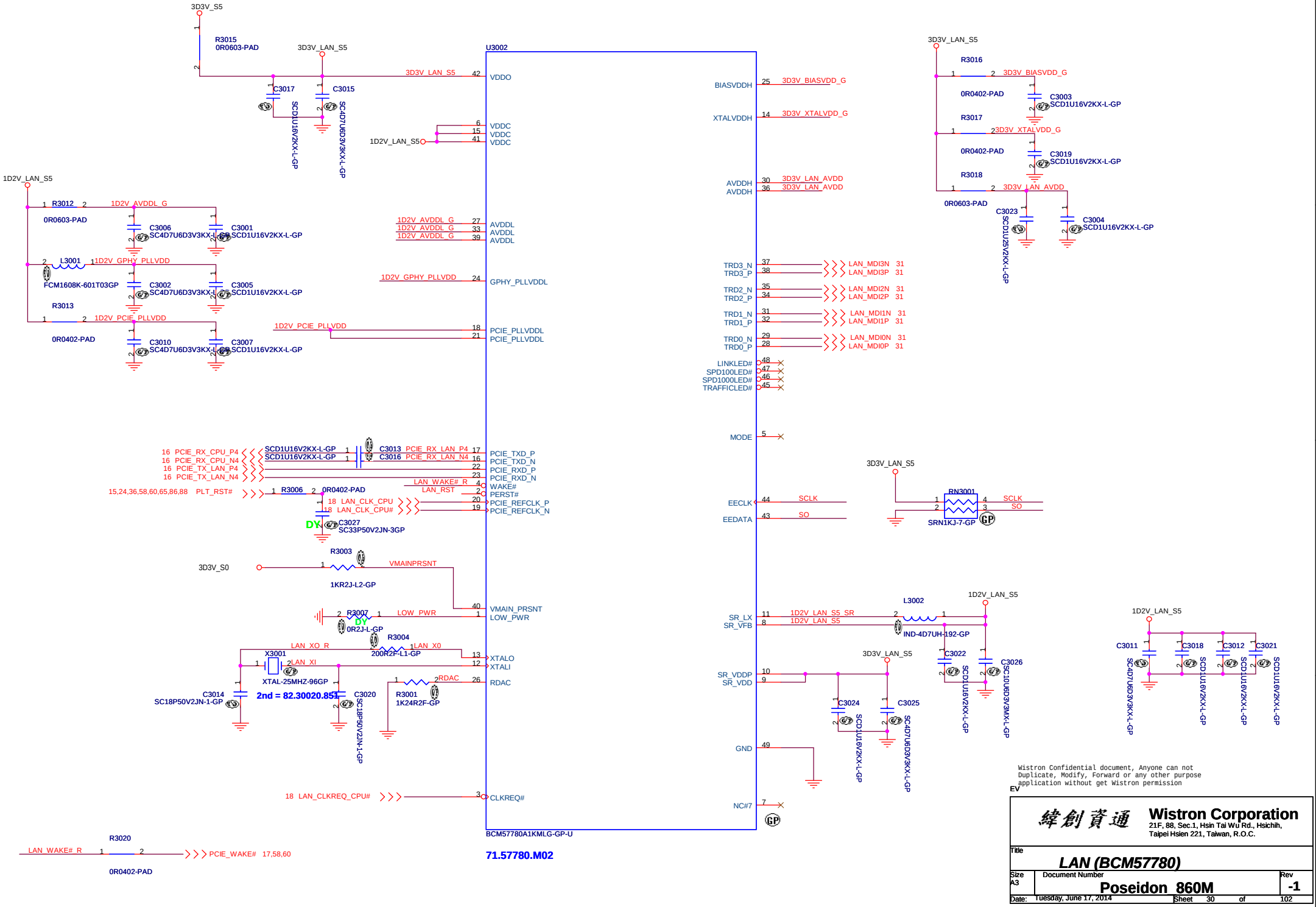
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size: Custom | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 29 of 102


U3002
BCM57780A1KMLG-GP-U
71.57780.M02
3D3V_S5
3D3V_LAN_S5
1D2V_LAN_S5
R3015
0R0603-PAD
C3017
C3015
SCD1U16V2KX-L-GP
SC4D7U6D3V3KX-L-GP
VDDO
VDDC
1D2V_AVDDL_G
AVDDL
1D2V_GPHY_PLLVDD
GPHY_PLLVDDL
1D2V_PCIE_PLLVDD
PCIE_PLLVDDL
R3012
1D2V_AVDDL_G
C3006
C3001
SC4D7U6D3V3KX-L-GP
L3001
FCM1608K-601T03GP
C3002
C3005
R3013
1D2V_PCIE_PLLVDD
C3010
C3007
BIASVDDH
3D3V_BIASVDD_G
XTALVDDH
3D3V_XTALVDD_G
AVDDH
3D3V_LAN_AVDD
TRD3_N
TRD3_P
TRD2_N
TRD2_P
TRD1_N
TRD1_P
TRD0_N
TRD0_P
LAN_MDI3N 31
LAN_MDI3P 31
LAN_MDI2N 31
LAN_MDI2P 31
LAN_MDI1N 31
LAN_MDI1P 31
LAN_MDI0N 31
LAN_MDI0P 31
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
MODE
EECLK
EEDATA
SCLK
SO
R3016
R3017
R3018
0R0402-PAD
0R0603-PAD
C3003
C3019
C3023
C3004
SCD1U25V2KX-L-GP
RN3001
SRN1KJ-7-GP
16 PCIE_RX_CPU_P4
16 PCIE_RX_CPU_N4
16 PCIE_TX_LAN_P4
16 PCIE_TX_LAN_N4
SCD1U16V2KX-L-GP
C3013 PCIE_RX_LAN_P4
C3016 PCIE_RX_LAN_N4
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
LAN_WAKE# R
LAN_RST
WAKE#
PERST#
15,24,36,58,60,65,86,88 PLT_RST#
R3006
0R0402-PAD
18 LAN_CLK_CPU
18 LAN_CLK_CPU#
PCIE_REFCLK_P
PCIE_REFCLK_N
DY
C3027
SC33P50V2JN-3GP
R3003
3D3V_S0
VMAINPRSNT
1KR2J-L2-GP
VMAIN_PRSNT
LOW_PWR
R3007
0R2J-L-GP
R3004
200R2F-L1-GP
LAN_XO_R
LAN_X0
LAN_XI
X3001
XTAL-25MHZ-96GP
XTALO
XTALI
RDAC
C3014
SC18P50V2JN-1-GP
2nd = 82.30020.853
C3020
R3001
1K24R2F-GP
18 LAN_CLKREQ_CPU#
CLKREQ#
R3020
LAN_WAKE# R
PCIE_WAKE# 17,58,60
0R0402-PAD
SR_LX
SR_VFB
SR_VDDP
SR_VDD
1D2V_LAN_S5_SR
1D2V_LAN_S5
L3002
IND-4D7UH-192-GP
C3022
C3026
SC10U6D3V3MX-L-GP
C3024
C3025
GND
NC#7
C3011
C3018
C3012
C3021
SCD1U16V2KX-L-GP
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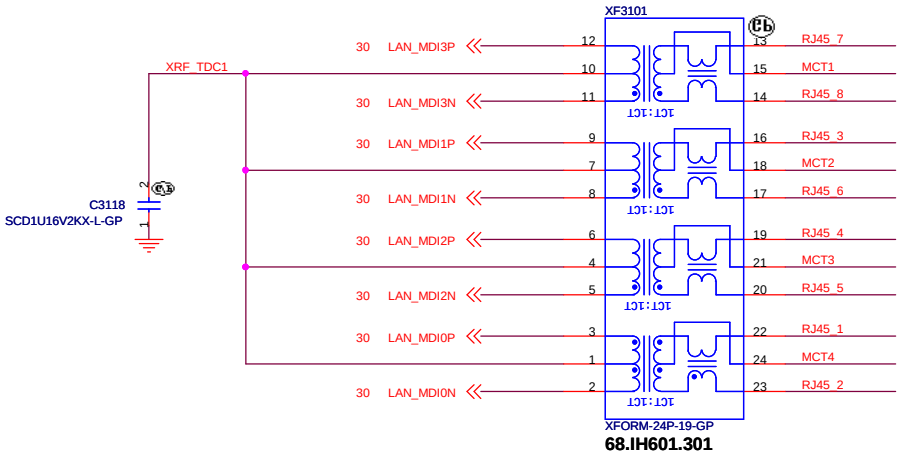
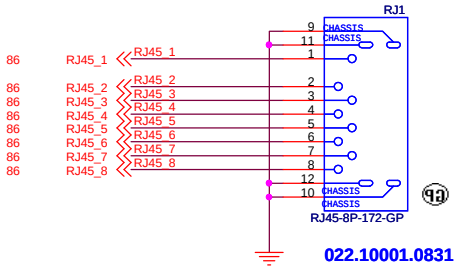
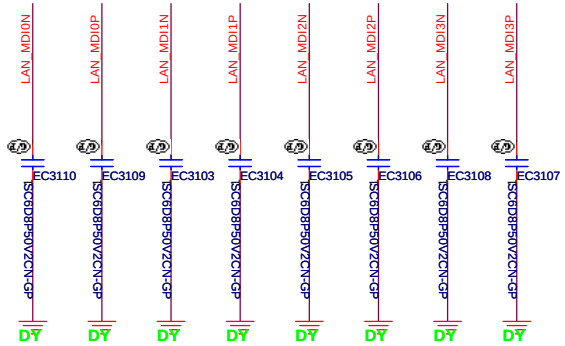
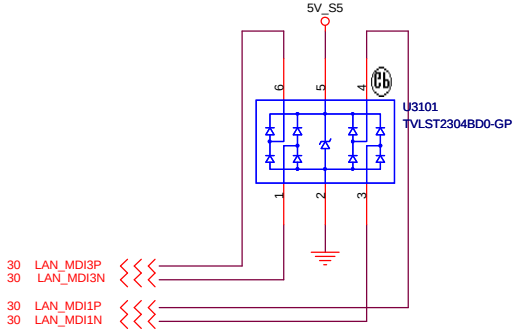
Title
LAN (BCM57780)
Size A3
Document Number
Poseidon_860M
Rev
-1
Date: Tuesday, June 17, 2014
Sheet 30 of 102

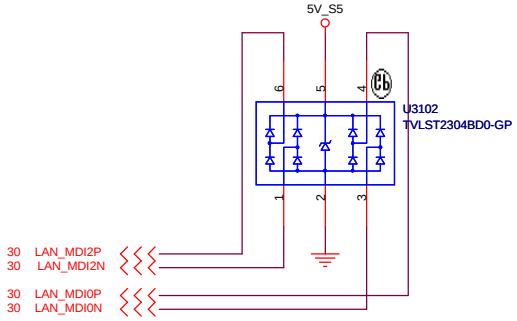
SSID = LAN

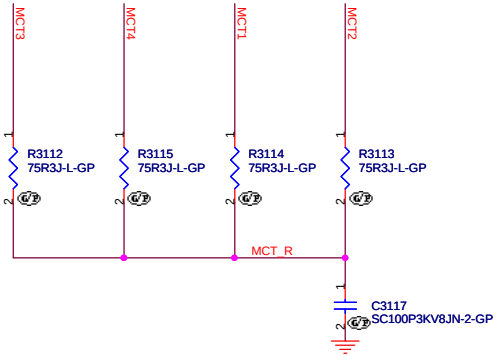












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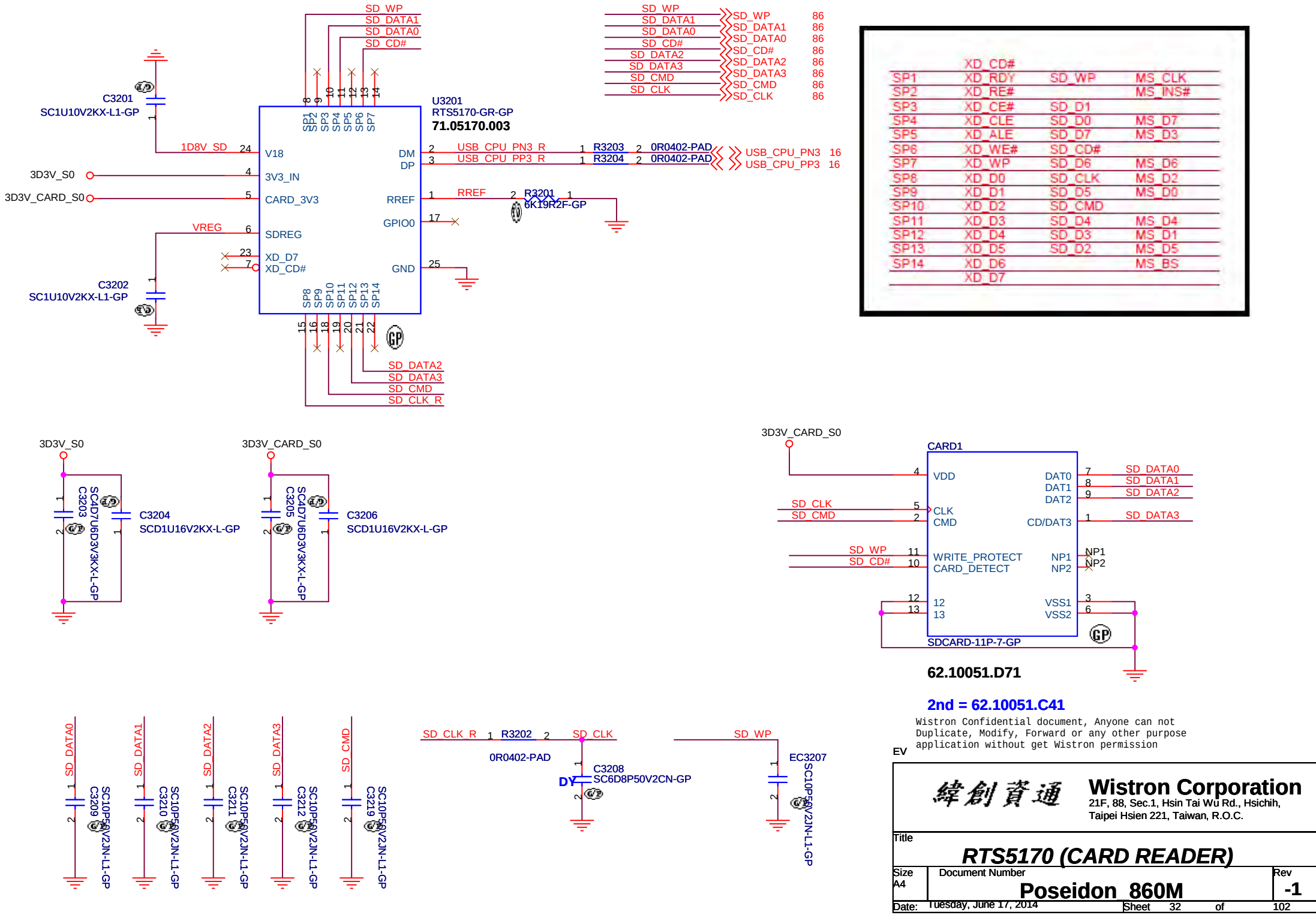
Title: ***(LAN+VGA) CONNECTOR***

Size	Document Number	Rev
Custom	**Poseidon_860M**	-1

Date: Tuesday, June 17, 2014 Sheet 31 of 102



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Title

RTS5170 (CARD READER)

Size	Document Number	Rev
A4	Poseidon_860M	-1

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Low Active 2A
RDSon = 80mΩ (Typ)

5V_S5
U3401
IN
OUT
GND
EN#
OC#
SY6288DAAC-GP
074.06288.009B
C3401
SC10U10V5KX-L1-GP
24,63 USB_PWR_EN#
5V_USB30
C3402
C3416
C3417
SC100J063V6MX-GP
-1_20140520

USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

USB port0

16 USB30_RX_CPU_N1
16 USB30_RX_CPU_P1
16 USB30_TX_CPU_N1
16 USB30_TX_CPU_P1
FC3401 FC3402 0R0402-PAD
C3408 C3409
USB30_TX_CPU_N1_R
USB30_TX_CPU_P1_R
FC3403 FC3404 0R0402-PAD
SCD1U16V2KX-L-GP
SCD1U16V2KX-L-GP
EU3401 DY
LINE_1 LINE_2 GND LINE_3 LINE_4
NC#10 NC#9 GND NC#7 NC#6
AZ1045-04F-R7G-GP
75.01045.073
2nd = 83.3V3U4.0A0
USB_CON_PN1
USB_CON_PP1
USB30_RX_CON_N1
USB30_RX_CON_P1
USB30_TX_CON_N1
USB30_TX_CON_P1
5V_USB30
USB1
VBUS D- D+ SSRX- SSRX+ SSTX- SSTX+
CHASSIS#10 CHASSIS#11 CHASSIS#12 CHASSIS#13 PGND GND
USB3.0
SKT-USB13-195-GP
022.10005.00G1

USB port1

16 USB30_RX_CPU_N2
16 USB30_RX_CPU_P2
16 USB30_TX_CPU_N2
16 USB30_TX_CPU_P2
FC3408 FC3405 0R0402-PAD
C3410 C3411
USB30_TX_CPU_N2_R
USB30_TX_CPU_P2_R
FC3406 FC3407 0R0402-PAD
SCD1U16V2KX-L-GP
SCD1U16V2KX-L-GP
EU3402 DY
LINE_1 LINE_2 GND LINE_3 LINE_4
NC#10 NC#9 GND NC#7 NC#6
AZ1045-04F-R7G-GP
75.01045.073
2nd = 83.3V3U4.0A0
USB_CON_PN2
USB_CON_PP2
USB30_RX_CON_N2
USB30_RX_CON_P2
USB30_TX_CON_N2
USB30_TX_CON_P2
5V_USB30
USB2
VBUS D- D+ SSRX- SSRX+ SSTX- SSTX+
CHASSIS#10 CHASSIS#11 CHASSIS#12 CHASSIS#13 PGND GND
USB3.0
SKT-USB13-195-GP
022.10005.00G1

SCD1U16V2KX-L-GP C3404 USB30_RX_CPU_N1
SCD1U16V2KX-L-GP C3405 USB30_RX_CPU_P1
SCD1U16V2KX-L-GP C3406 USB30_TX_CPU_N1_R
SCD1U16V2KX-L-GP C3407 USB30_TX_CPU_P1_R
DY

SCD1U16V2KX-L-GP C3414 USB30_RX_CPU_N2
SCD1U16V2KX-L-GP C3413 USB30_RX_CPU_P2
SCD1U16V2KX-L-GP C3415 USB30_TX_CPU_N2_R
SCD1U16V2KX-L-GP C3412 USB30_TX_CPU_P2_R
DY

EL3402
MCM1012B900FBP-GP-U
USB_CON_PN1
USB_CON_PP1
USB_CPU_PN0 16
USB_CPU_PP0 16
68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001

EU3403
DY
I/O1 GND I/O2 I/O4 VDD I/O3
USB_CON_PN1
USB_CON_PN2
USB_CON_PP1
USB_CON_PP2
5V_USB30
AZC099-04S-1-GP
75.09904.07C
2ND = 75.04285.07C

EL3403
MCM1012B900FBP-GP-U
USB_CON_PN2
USB_CON_PP2
USB_CPU_PN1 16
USB_CPU_PP1 16
68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001

EV

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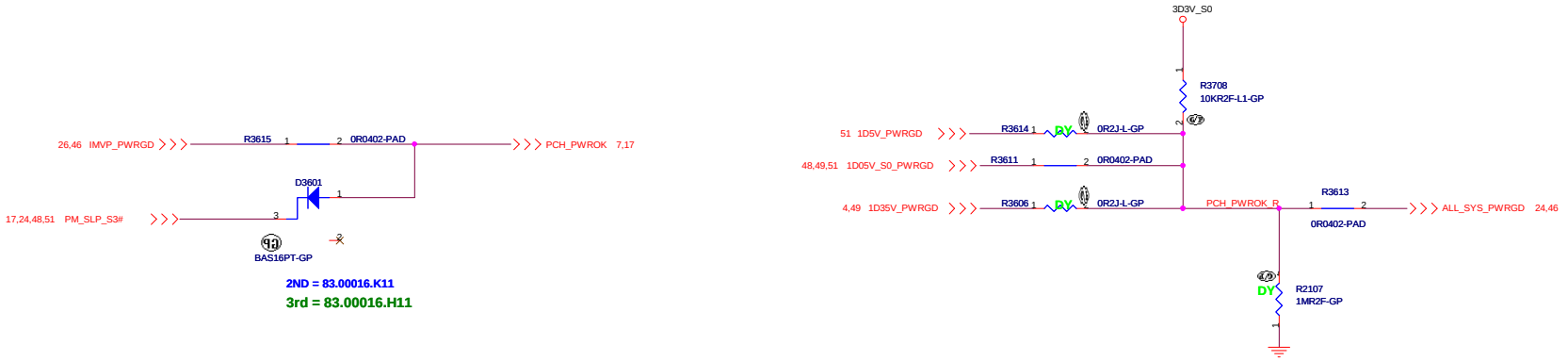
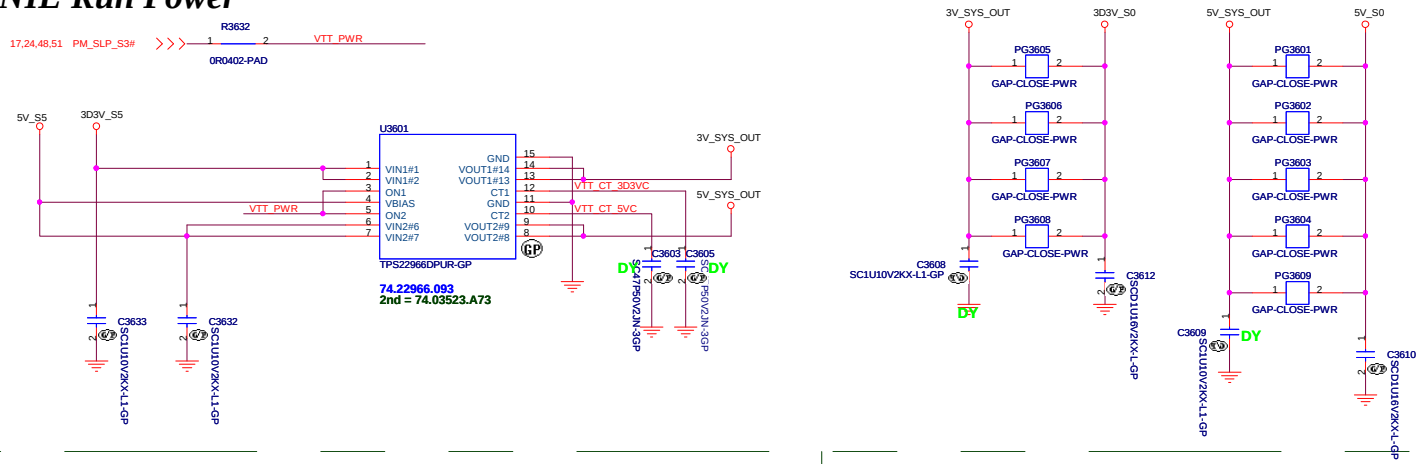
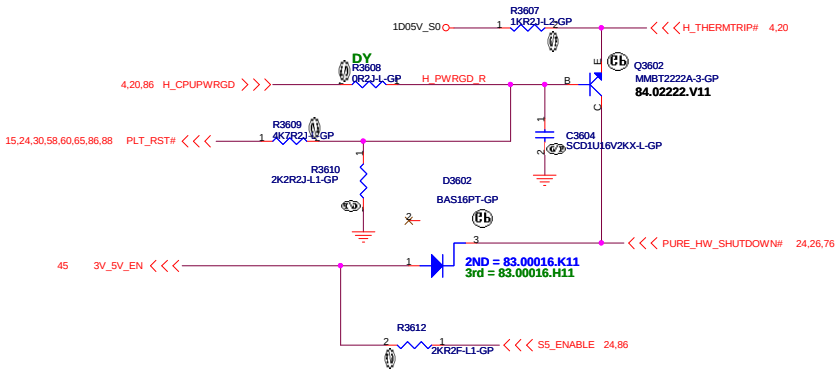
Title: USB 2.0 / 3.0 Port
Size: A3
Document Number: Poseidon_860M
Rev: -1
Date: Tuesday, June 17, 2014
Sheet 34 of 102

Power Sequence

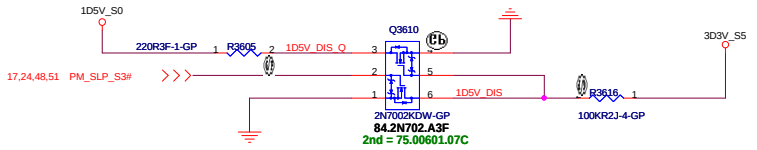


ANNIE Run Power





Discharge circuit



EV

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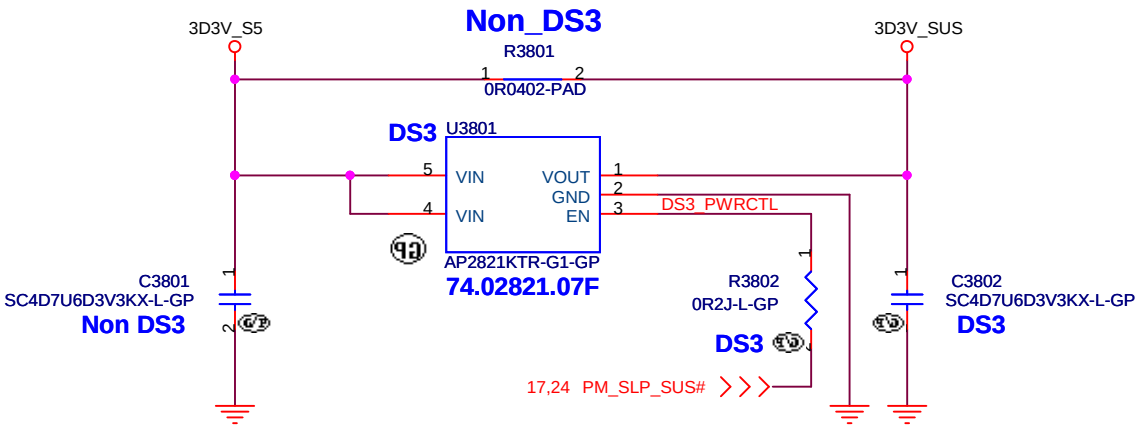
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size: Custom | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 36 of 102



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Taipei Hsien 221, Taiwan, R.O.C.

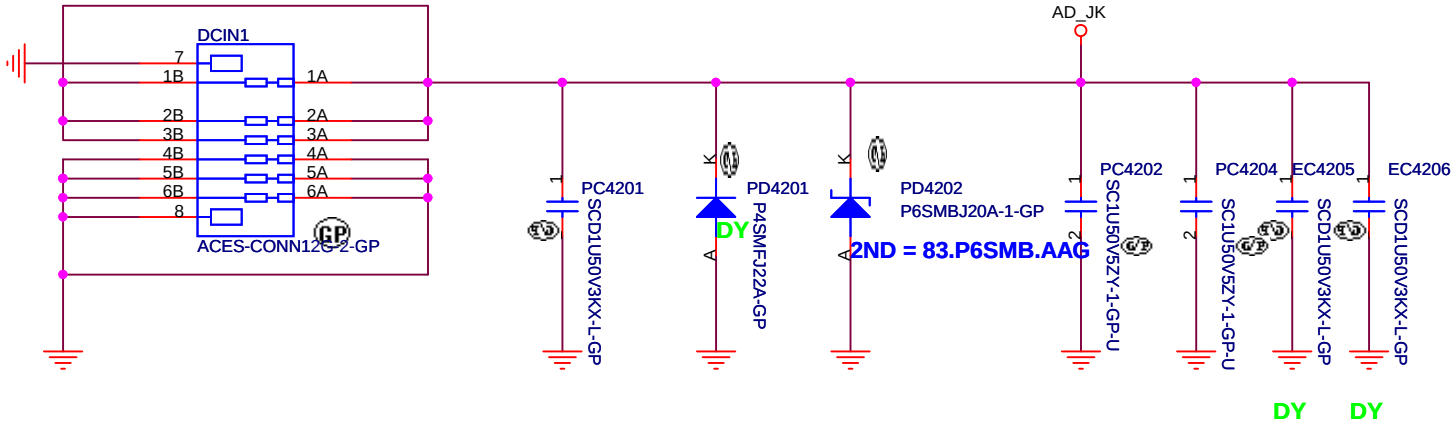
Title: DS3

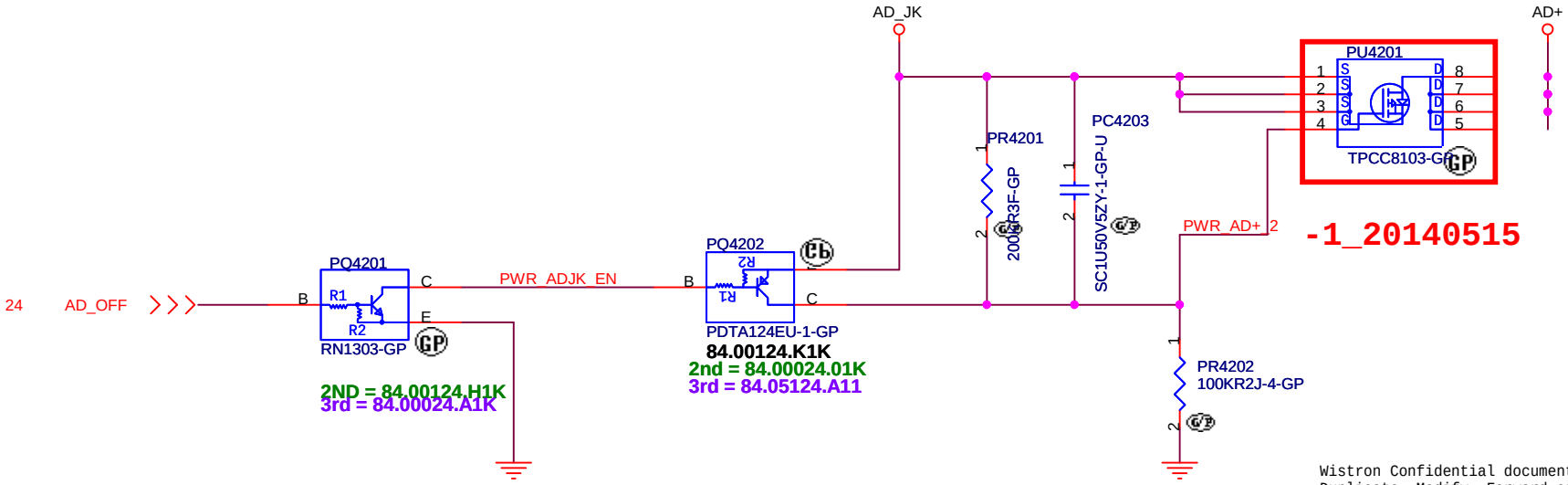
Size	Document Number	Rev
A4	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 38 of 102

ANNIE solution

Adaptor in to generate DCBATOUT





EV

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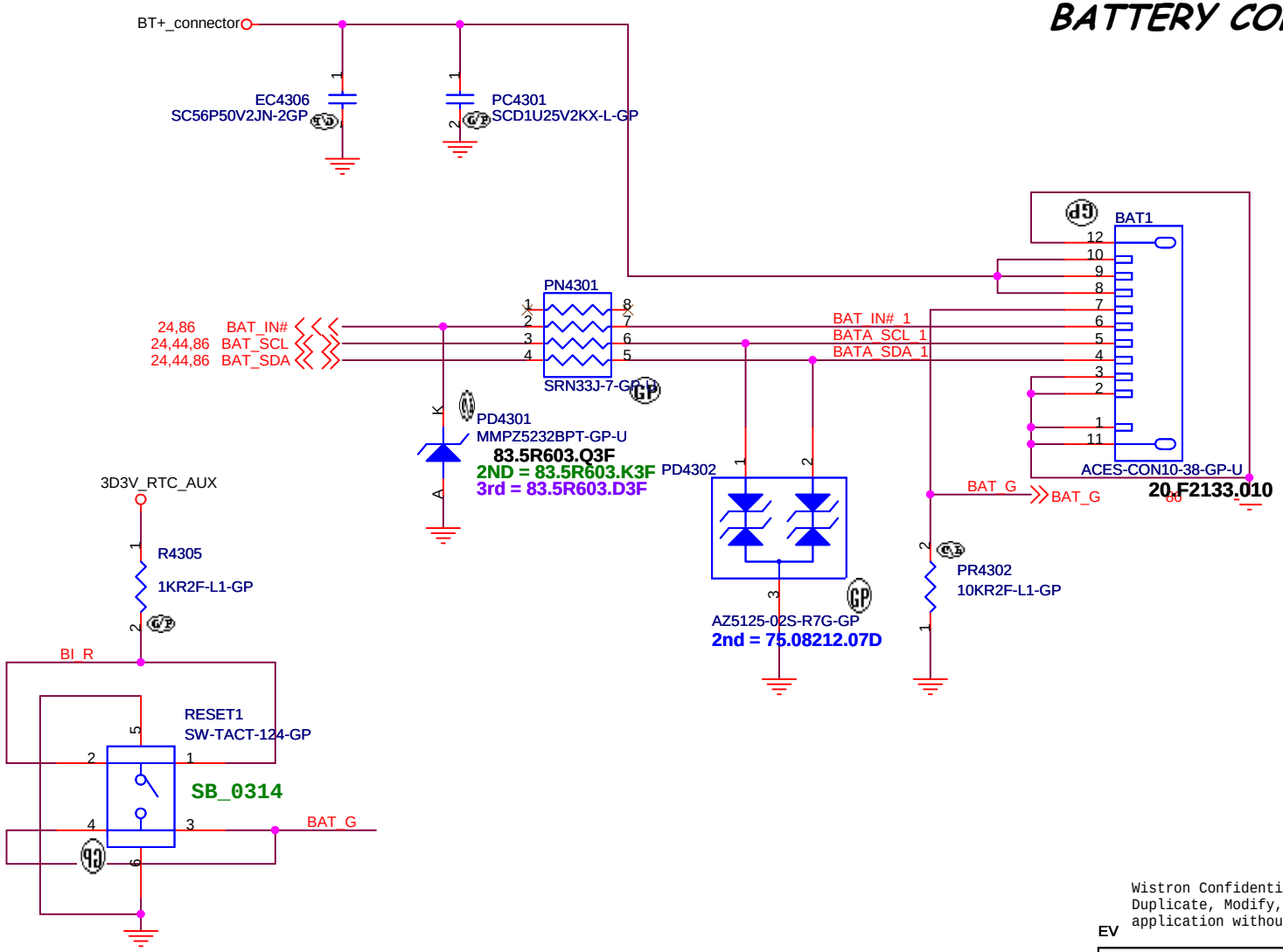
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN JACK

Size	Document Number	Rev
A4	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 42 of 102

BATTERY CONNECTOR



EV

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size	Document Number	Rev
A4	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 43 of 102

SSID = Charger

	Stat	PM_SLP_A#	Adaptor Current	AC_Protect pasent (85% x 120%)	AC_Protect Current	PR4404 Sense resistor	Current to Voltage	R1 PR4407	R2 PR4401
40W	AC + Battery	High	2.1	102%	2.142	20 mOhm	0.8568	41.2	100
45W	AC + Battery	High	2.37	102%	2.4174	20 mOhm	0.96696	60.4	100
65W	AC + Battery	High	3.42	102%	3.4884	10 mOhm	0.69768	16.2	100
90W	AC + Battery	High	4.74	102%	4.8348	10 mOhm	0.96696	60.4	100
120W	AC + Battery	High	6.32	102%	6.4464	10 mOhm	1.28928	113	100
135W	AC + Battery	High	7.1	102%	7.242	10 mOhm	1.4484	180	100

-1_20140515

-1_20140515

AC mode (default:120%):
set up the value by PR4401 and PR4407

74.02224.073

84.00412.037

84.00412.037

CYNTEC, 7*7*3
DCR: 37~40mOhm
Idc : 5.5 A , Isat : 10A

Charger Current=1.4~3.6A

2nd = 068.4R710.1081

AC adapter detect current :
Ac input current = 20 x (Vacp - Vacn) / 10mohm

Deglicth Time Setting
125K -> Deglitch time : 5us
375K -> Deglitch time : 15us

-1_20140516

Battery OCP	R3	R4
6 Cell (3S2P)	7A	71.5K	52.3K
4 Cell (4S1P)	4A	165K	52.3K

Battery UVP	R5	R6
6 Cell (3S2P)	9V	165K	71.5K
4 Cell (4S1P)	12V	110K	71.5K

Battery OVP	R7	R8
6 Cell (3S2P)	14V	80.6K	71.5K
4 Cell (4S1P)	17.6V	51.1K	71.5K

-1_20140516

-1_20140522

-1_20140522

-1_20140520

Battery I Sense

Battery OCP setting

Battery UVP setting

Battery OVP setting

EV

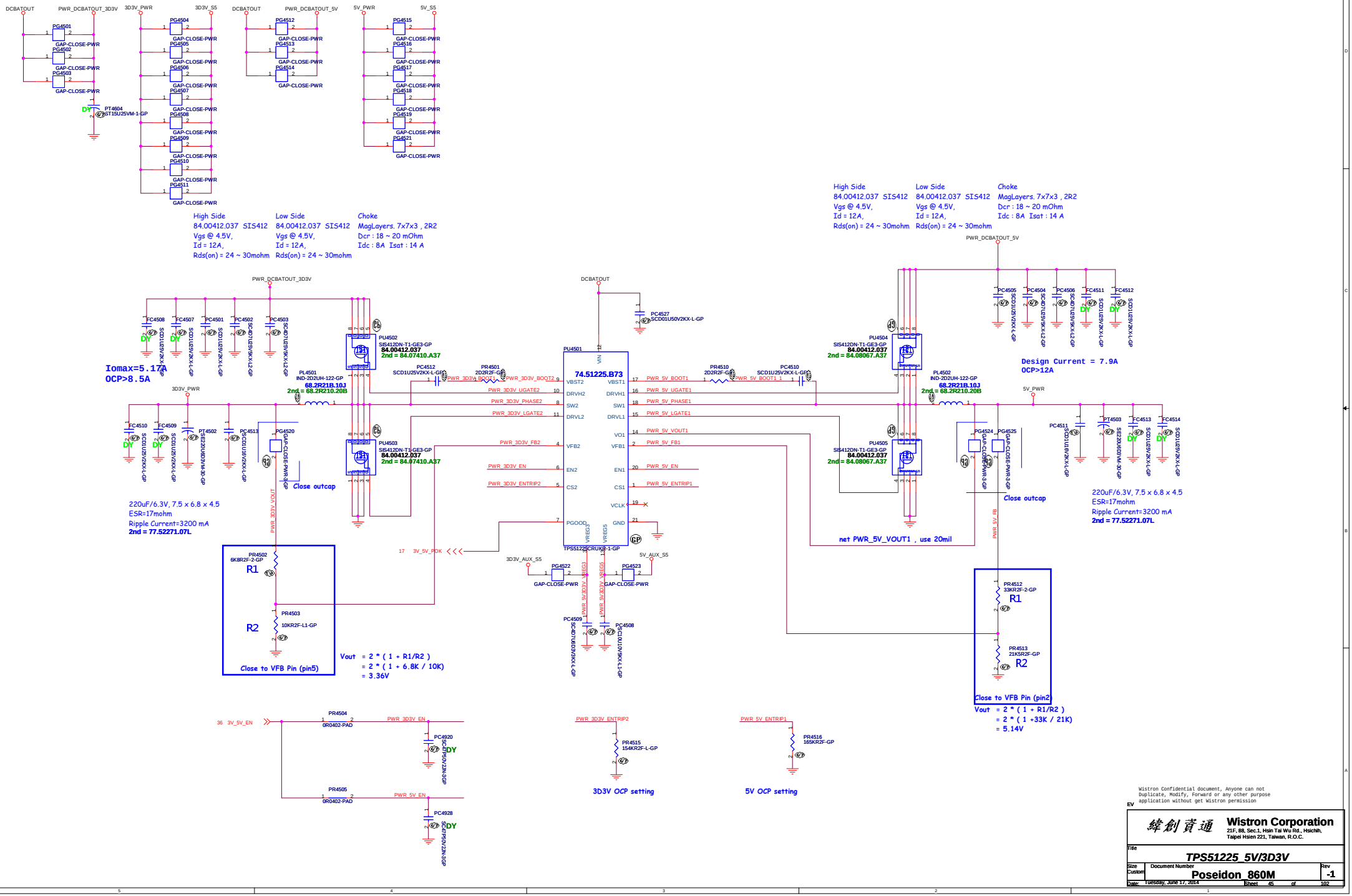
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER_HPA02224

Size: Custom | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 44 of 102

SSID = PWR.Plane.Regulator_3p3v5v



EV

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51225_5V/3D3V

Size: Custom | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 45 of 102

SSID = CPU.Regulator

	47W
PC4602	4.7nF 78.47224.2FL
PR4611	95.3k 64.95325.6DL
PR4614	150k 64.15035.6DL
PR4617	75k 63.75334.1DL
PR4615	36.5k 64.36525.6DL
PR4618	20k 64.20025.6DL
PR4626	DY
PR4630	DY
PR4602	6.98k 64.69815.6DL
PR4607	2.87k 64.28715.6DL

-1_20140515

074.51633.0073 for BDW CPU

2nd = 74.51631.073

HSW_BDW

TPS51631RSMR-1-GP

Close to VR

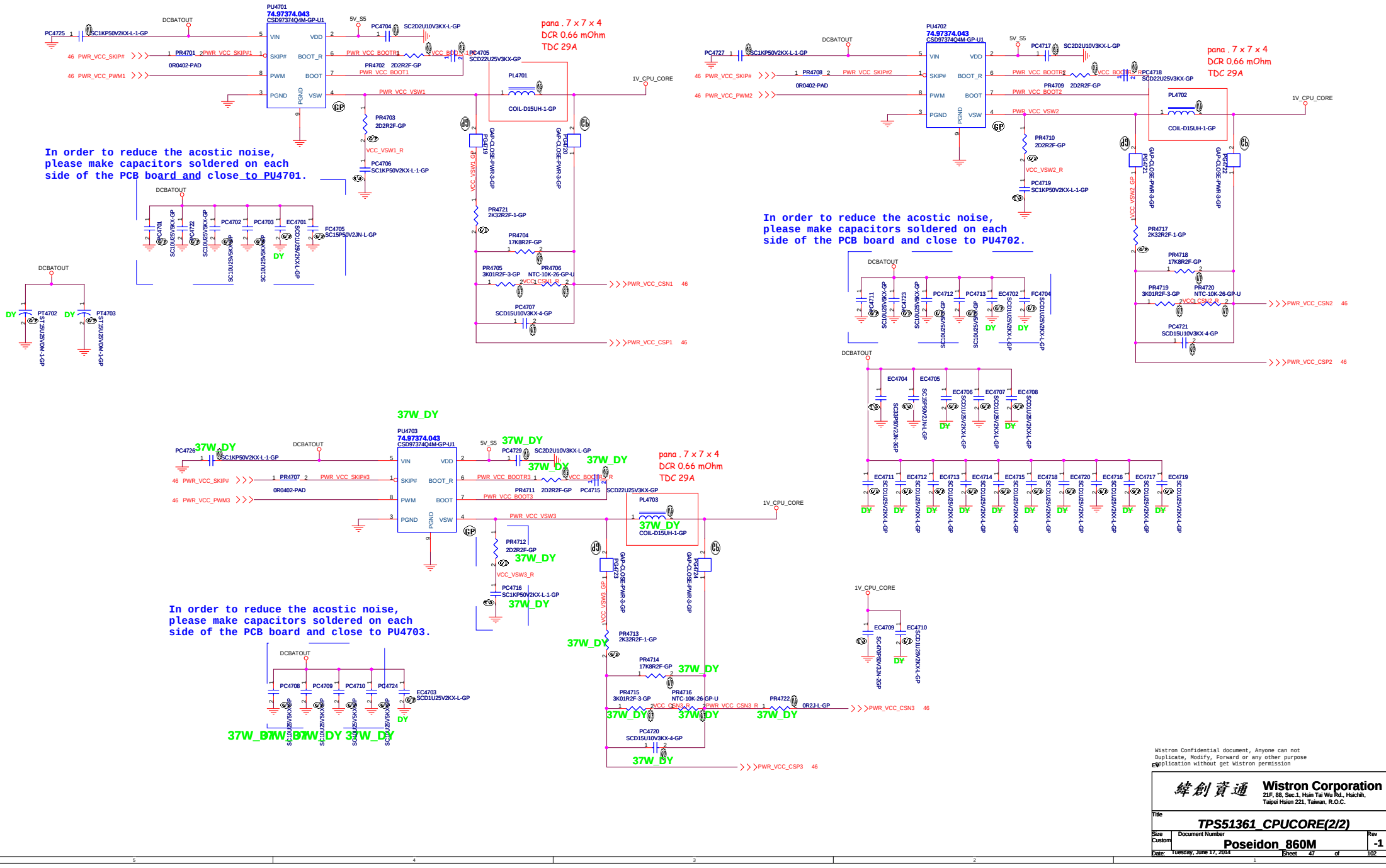
EV

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

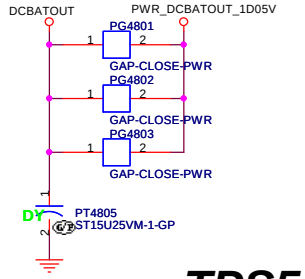
Title: TPS51361_CPUCORE(1/2)

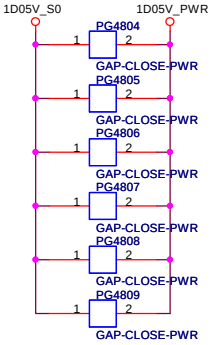
Size: Custom | Document Number: Poseidon_840M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 46 of 102



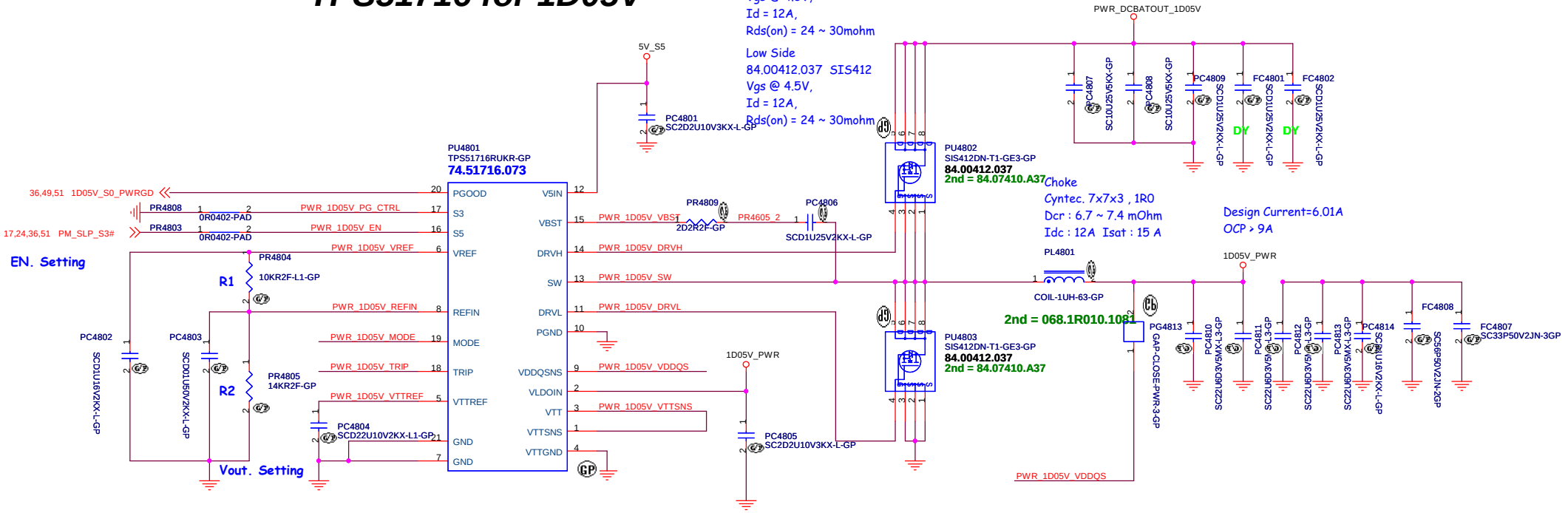
TPS51716 for 1D05V





High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

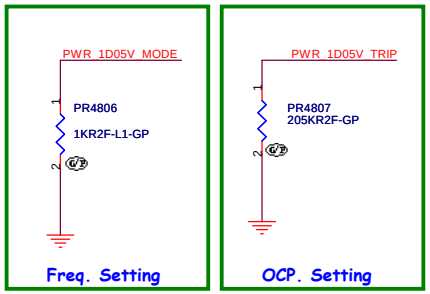
Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm



MODE

PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



EV

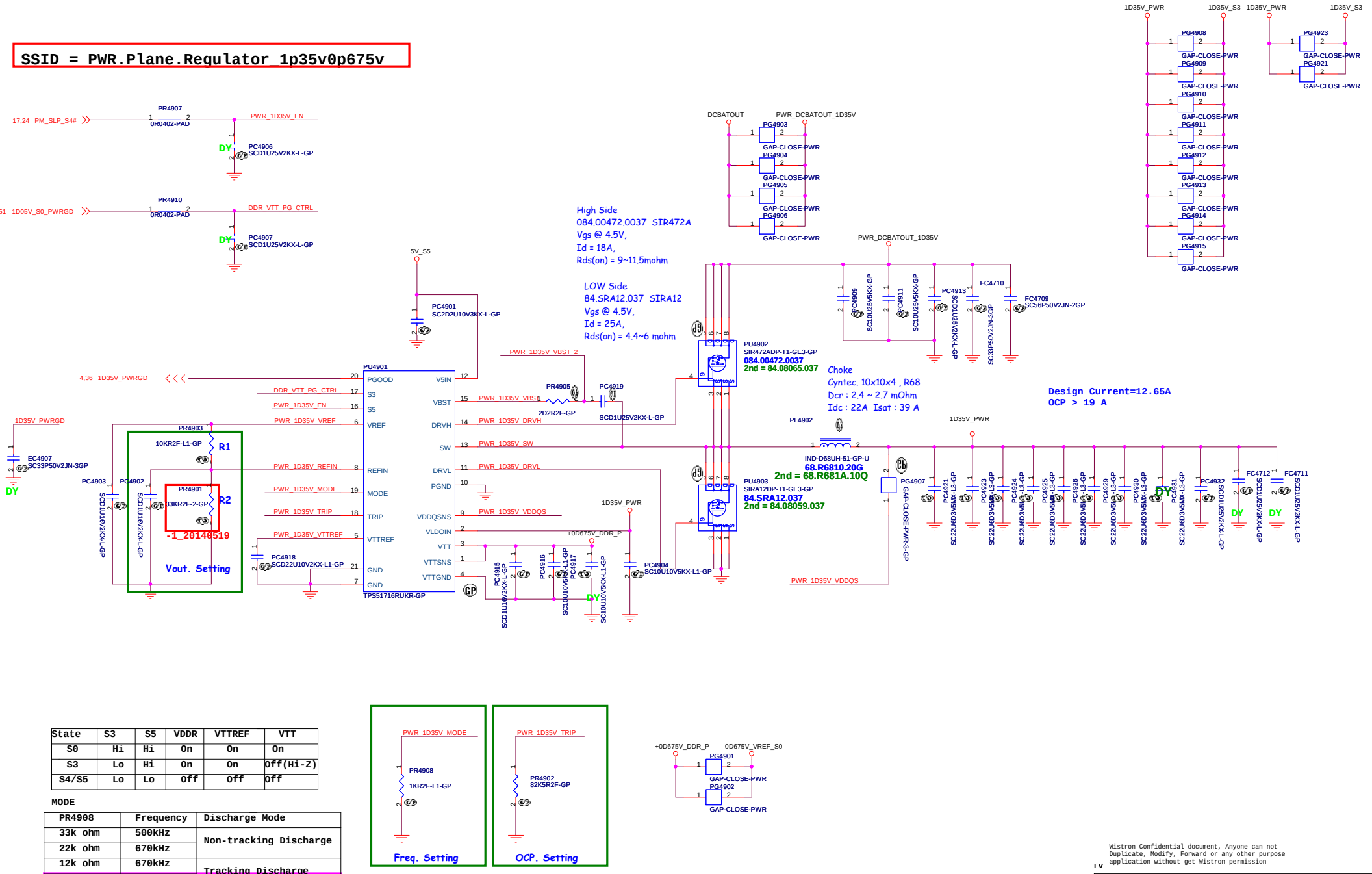
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC_1D05V(TPS51716)

Size: A3 | Document Number: Poseidon_860M | Rev: -1

Date: Wednesday, June 18, 2014 | Sheet 48 of 102

SSID = PWR.Plane.Regulator_1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4908	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

EV

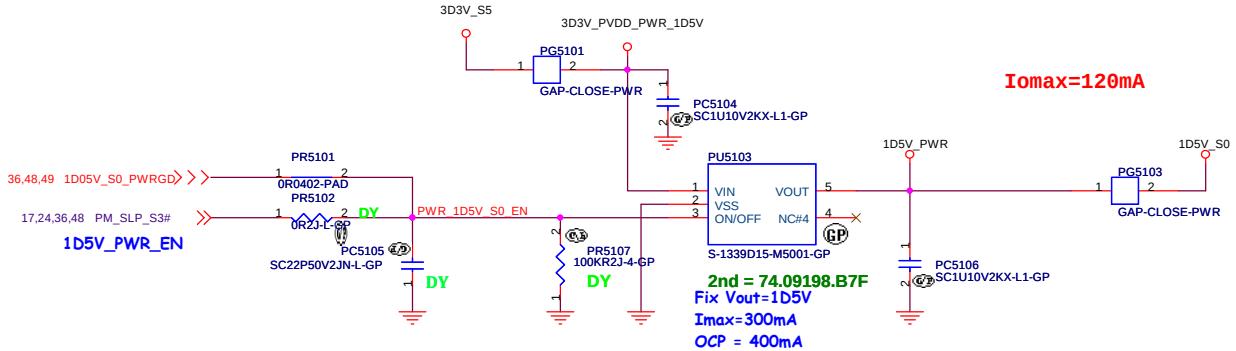
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

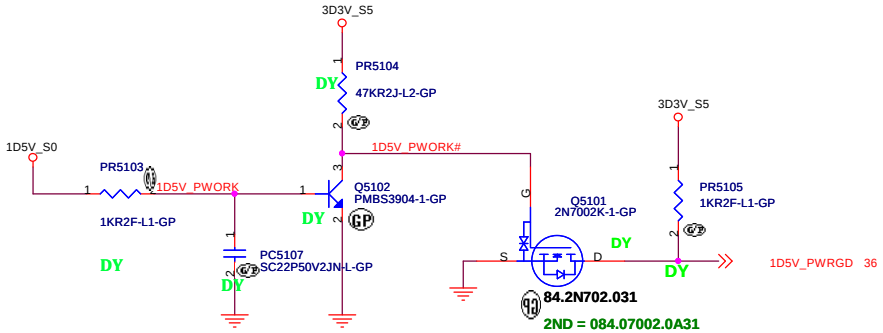
Title: TPS51716 (VDDQ_VTT)

Size: Custom | Document Number: Poseidon_860M | Rev: -1

Date: Wednesday, June 18, 2014 | Sheet 49 of 102

TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V





EV

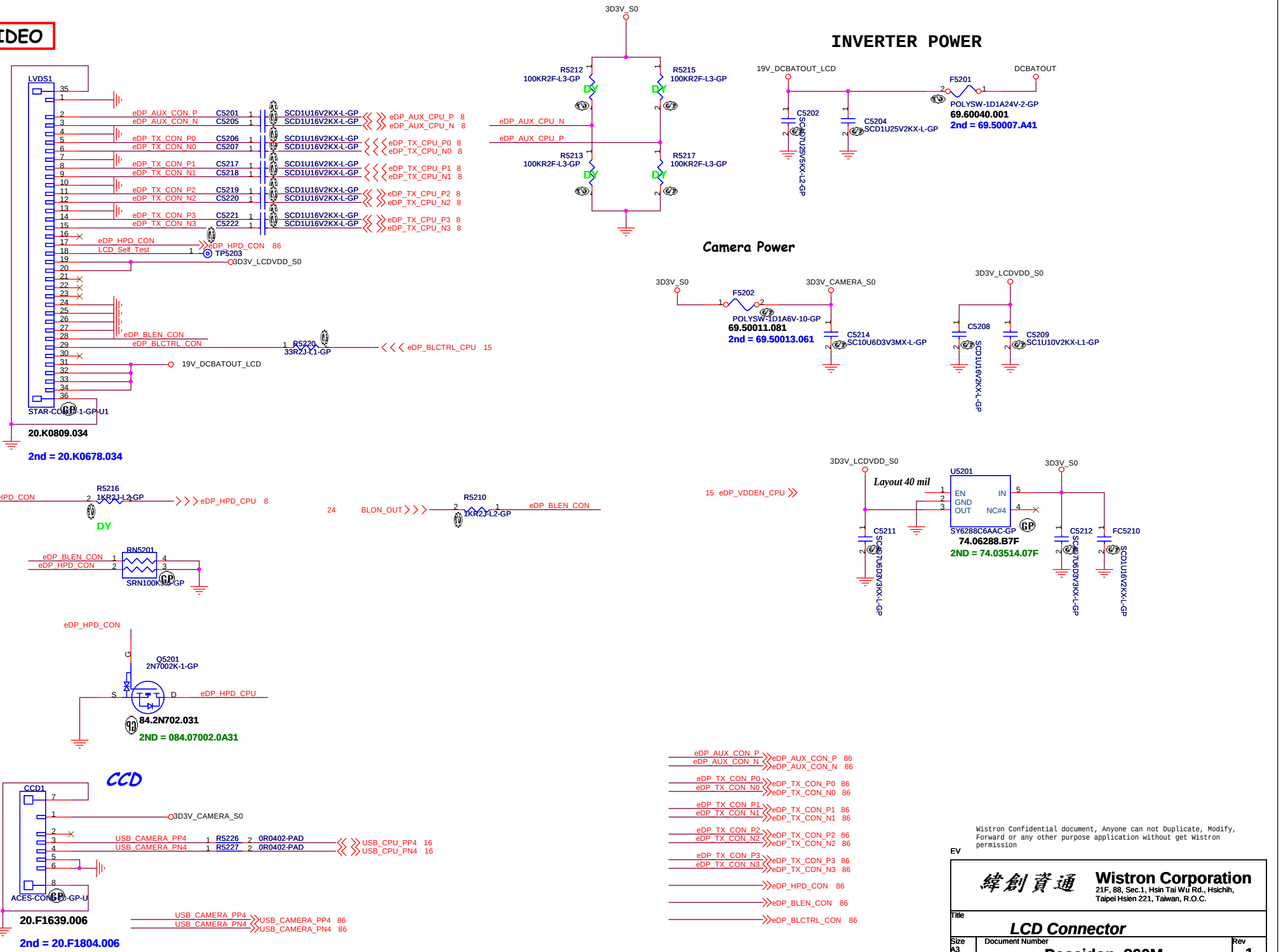
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D5V_S0 TLV70215

Size: A3 | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 51 of 102

SSID = VIDEO



EV

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LCD Connector***	
Size A3	Document Number **Poseidon_860M**	Rev **-1**
Date: Tuesday, June 17, 2014	Sheet 52 of 102	

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN

EV

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

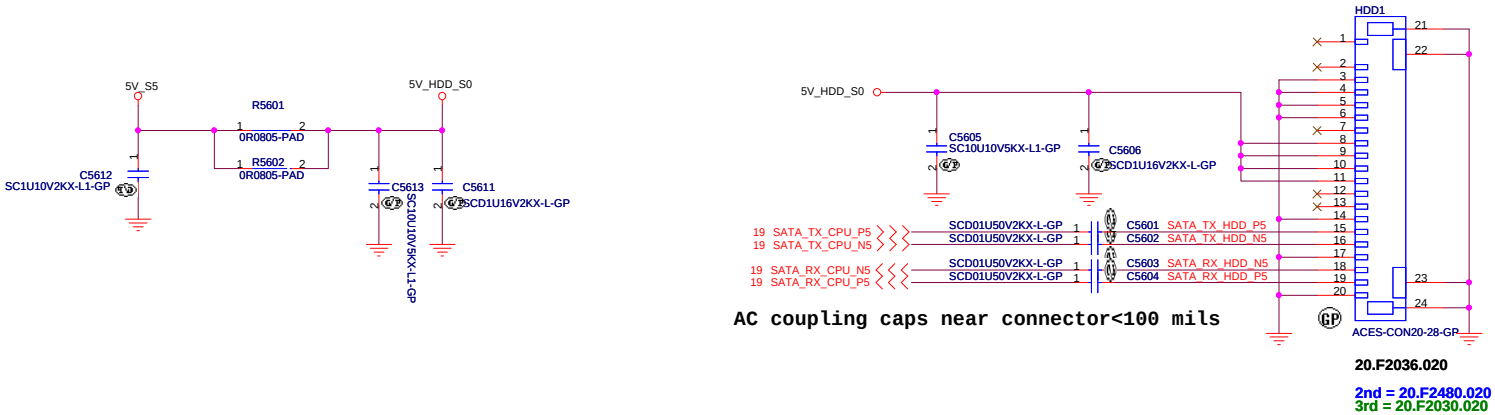
Size: A3 | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 54 of 102

SSID = SATA

SATA HDD Connector

SB_0327



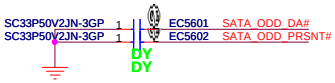
AC coupling caps near connector<100 mils

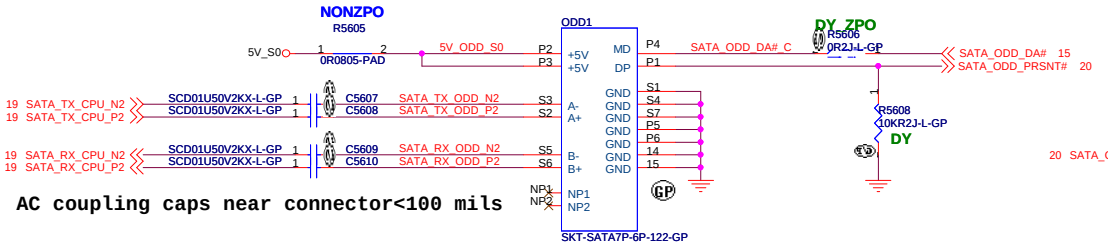
20.F2036.020

2nd = 20.F2480.020

3rd = 20.F2030.020

ODD Connector



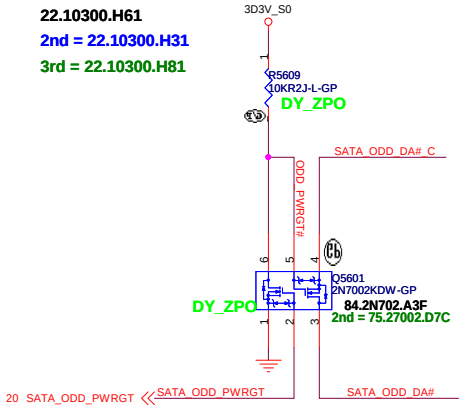


AC coupling caps near connector<100 mils

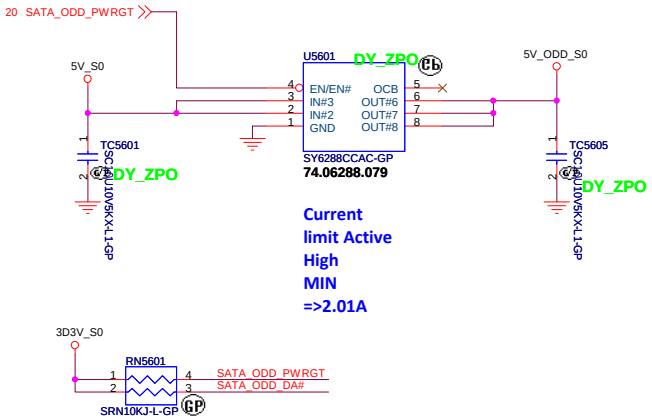
22.10300.H61

2nd = 22.10300.H31

3rd = 22.10300.H81



SATA Zero Power ODD



Current limit Active High MIN =>2.01A

EV

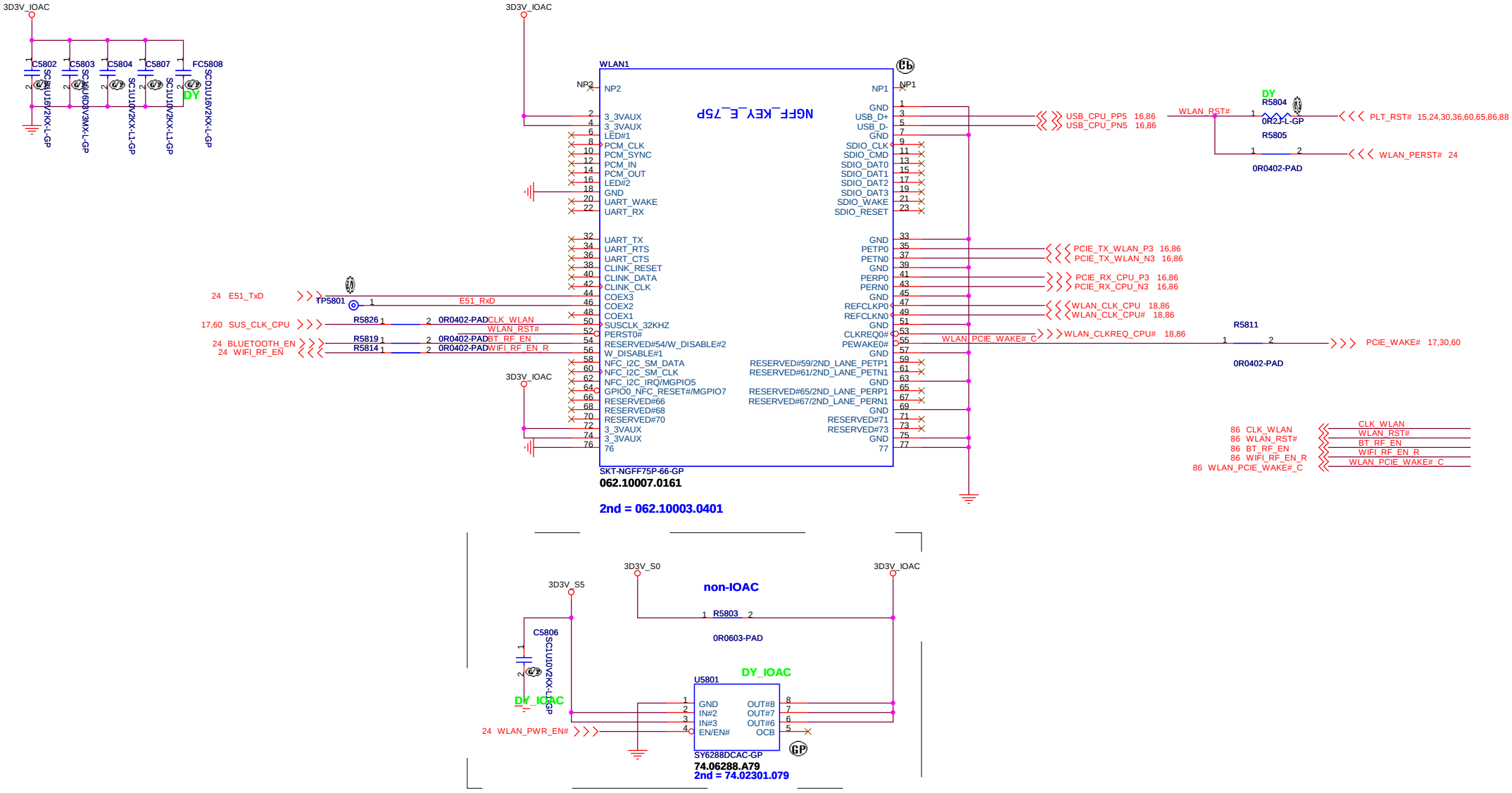
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD / ODD / NGFF_SSD

Size: Custom | Document Number: Poseidon_860M | Rev: -1

Date: Tuesday, June 17, 2014 | Sheet 56 of 102

SSID = Wireless Mini Card Connector(802.11a/b/g/n)



EV

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

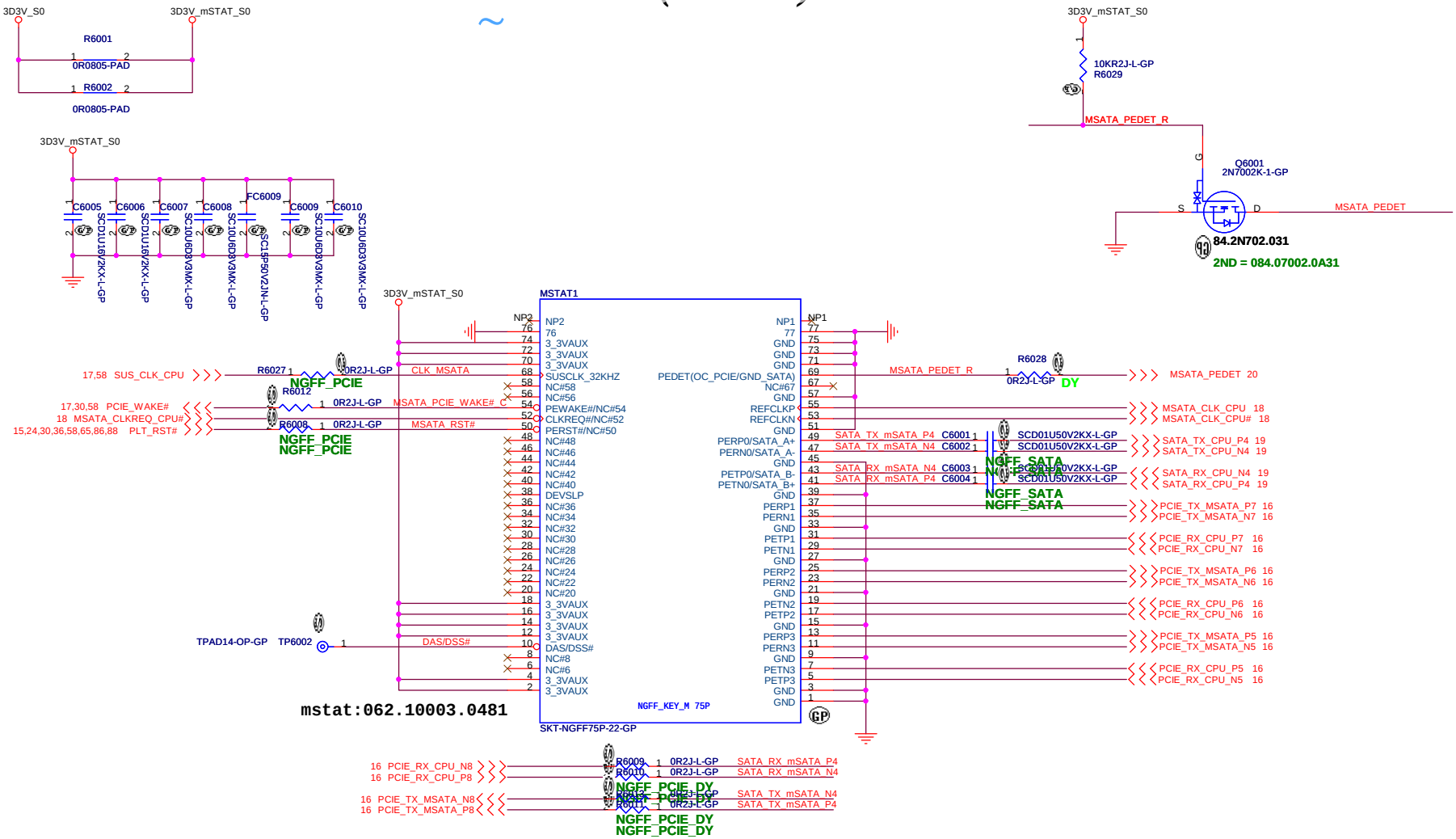
Title: MINICARD(WLAN)

Size	Document Number	Rev
A3	Poseidon_860M	-1

Date: Tuesday, June 17, 2014 Sheet 58 of 102

SSID = mSATA

Mini Card Connector(mSATA)



SATA/PCIe Gen 2 and Gen 3 Capacitor Values

Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF[2]	None[3]

EV

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

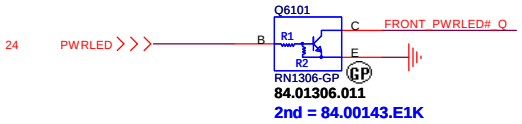
Title: mSATA Connector

Size: A3 | Document Number: Poseidon_860M | Rev: -1

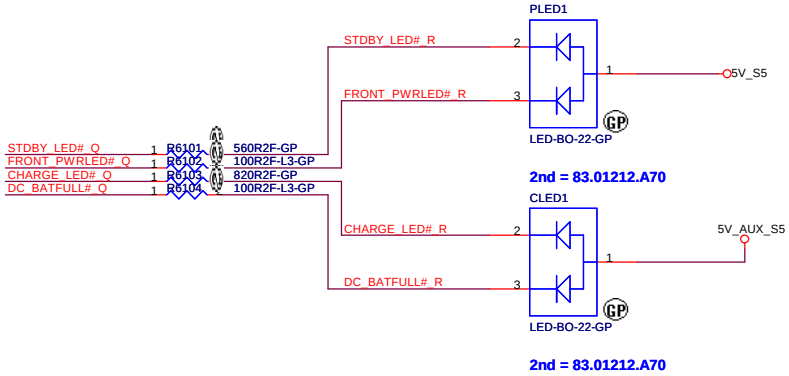
Date: Tuesday, June 17, 2014 | Sheet 60 of 102

SSID = User.Interface

Power button LED



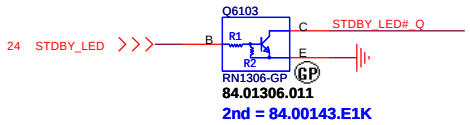
84.01306.011
2nd = 84.00143.E1K



2nd = 83.01212.A70

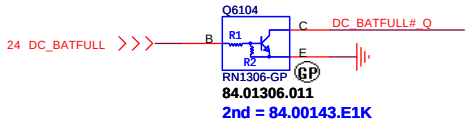
2nd = 83.01212.A70

Power STDBY_LED

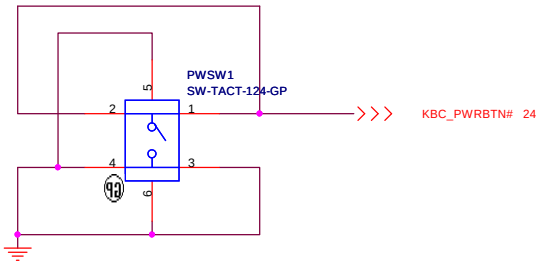


84.01306.011
2nd = 84.00143.E1K

Battery LED2(DC_BATFULL)

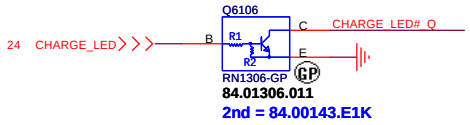


84.01306.011
2nd = 84.00143.E1K



62.40078.001
2nd = 62.40009.E51
3rd = 62.40009.D71

Battery LED1(CHARGE)



84.01306.011
2nd = 84.00143.E1K

EV

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LED Bard/Power Button***

Size	Document Number	Rev
A3	Poseidon_860M	-1

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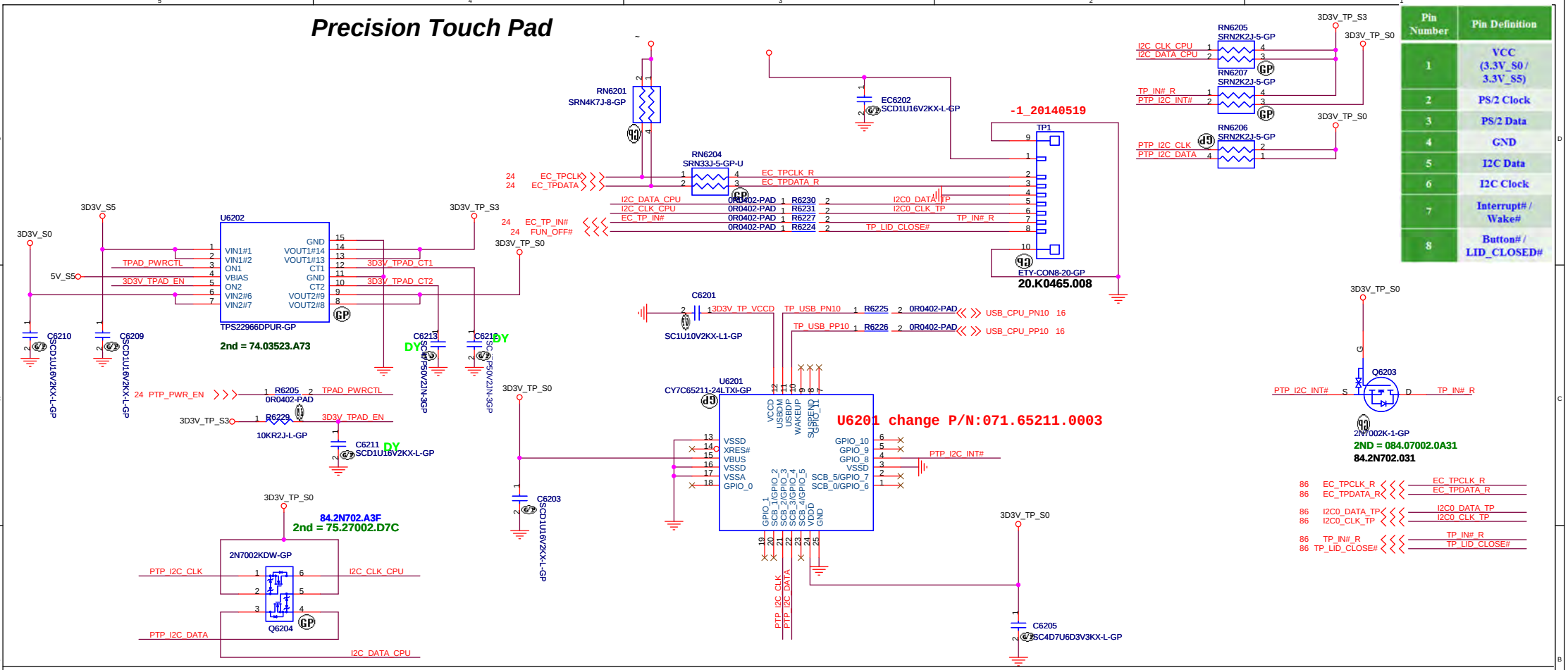
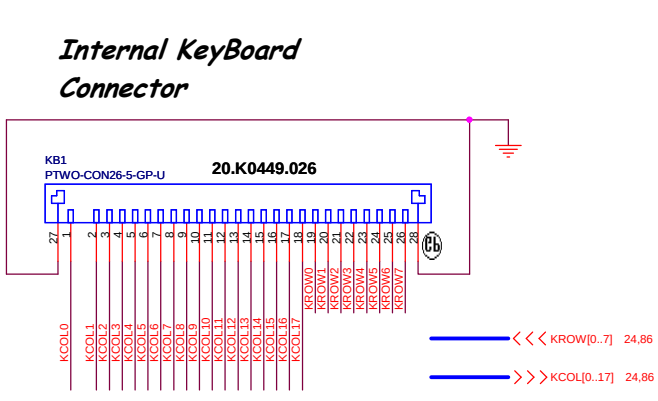
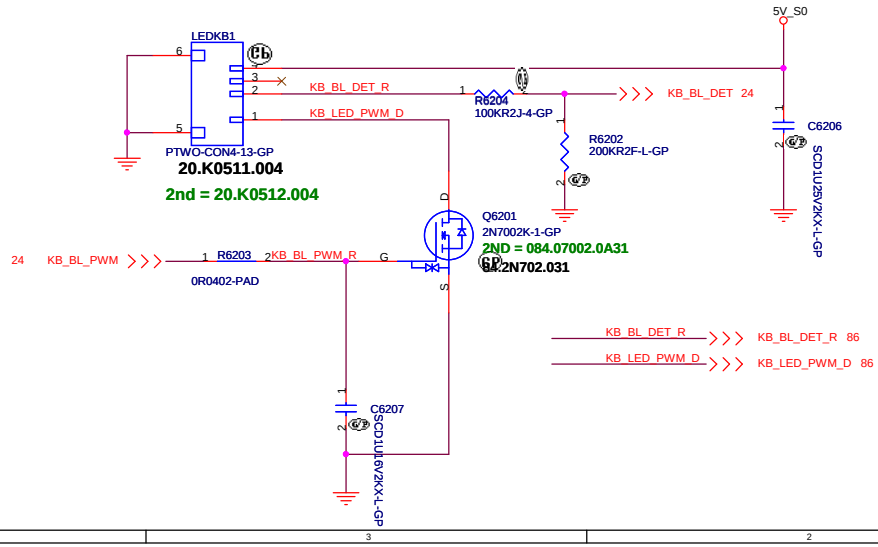
Precision Touch Pad



Pin Number	Pin Definition
1	VCC (3.3V_S0 / 3.3V_S5)
2	PS/2 Clock
3	PS/2 Data
4	GND
5	I2C Data
6	I2C Clock
7	Interrupt# / Wake#
8	Button# / LID_CLOSED#

Internal KeyBoard Connector





EV

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

Size: Custom | Document Number: **Poseidon_860M** | Rev: -1

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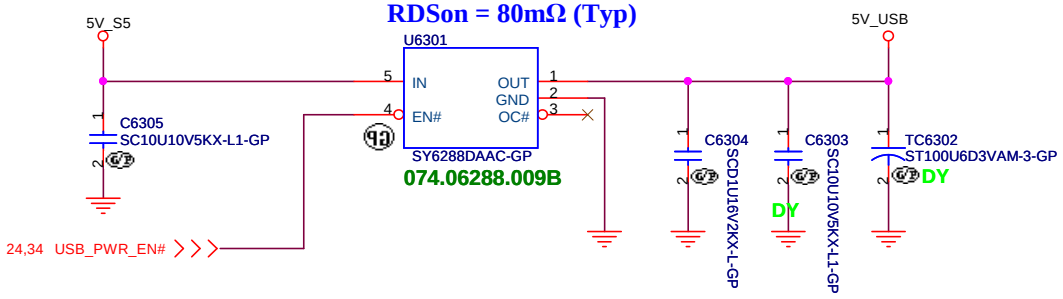
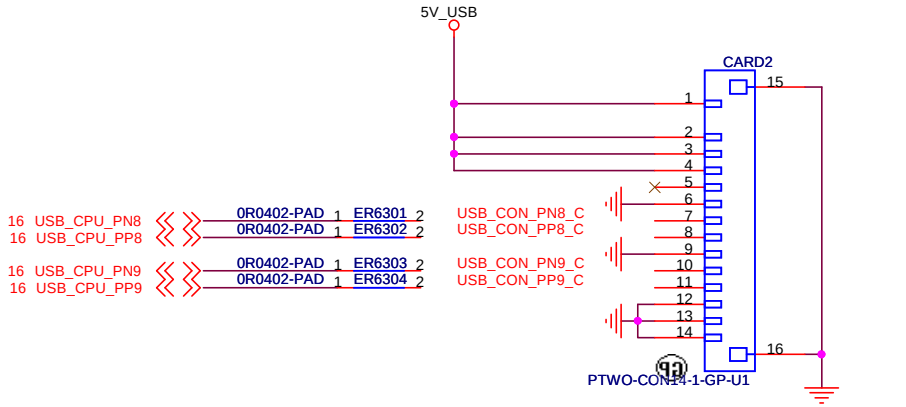
Low Active 2A

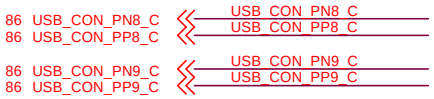
RDSon = 80mΩ (Typ)





20.K0426.014

2nd = 20.K0474.014



EV

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

Size	Document Number	Rev
Custom	**Poseidon_860M**	-1

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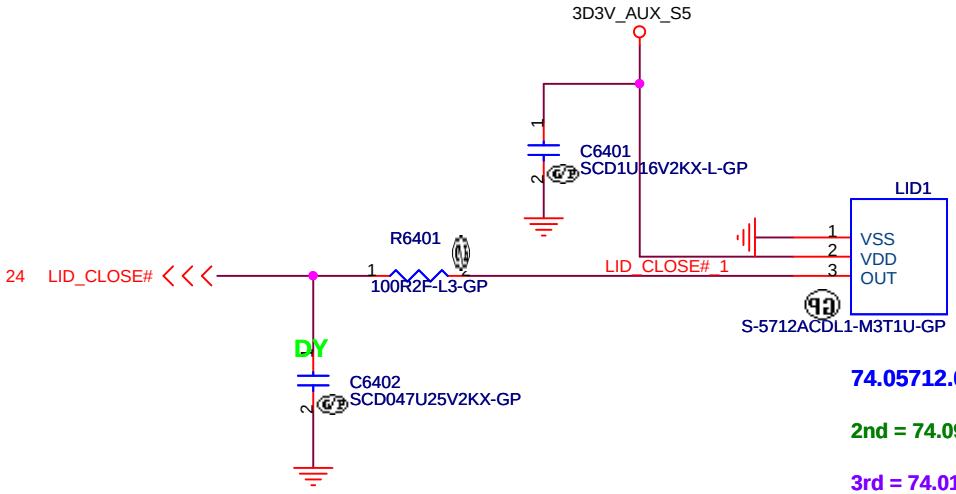

EV

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size	Document Number	Rev
A4	Poseidon_860M	-1

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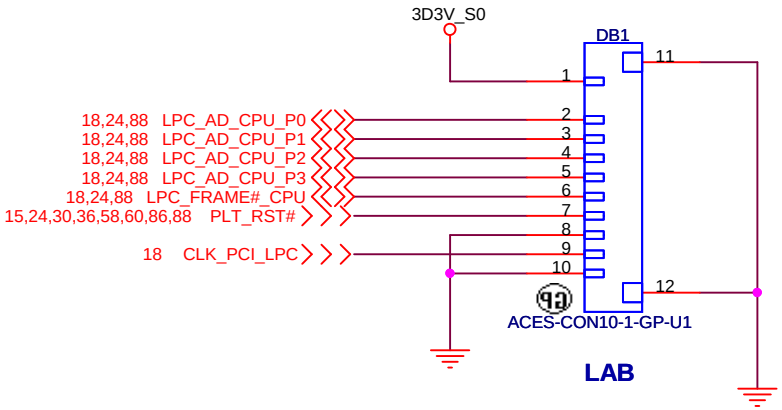

EV

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

Size	Document Number	Rev
A4	Poseidon_860M	-1

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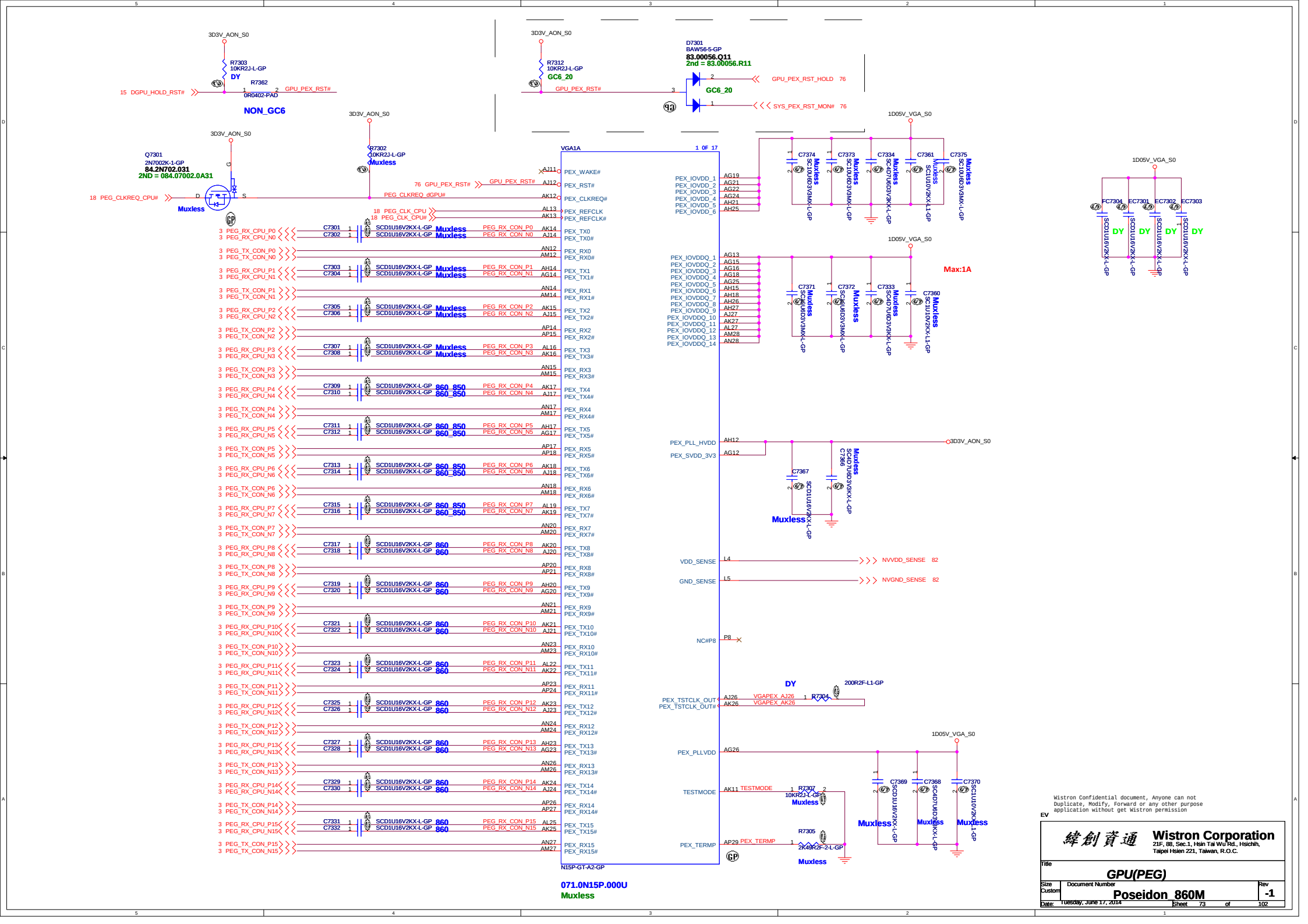
3D3V_AON_S0
R7303
10KR2J-L-GP
DY
R7362
0R0402-PAD
15 DGPU_HOLD_RST#
GPU_PEX_RST#
NON_GC6
3D3V_AON_S0
R7312
10KR2J-L-GP
GC6_20
GPU_PEX_RST#
D7301
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.R11
GPU_PEX_RST_HOLD 76
GC6_20
SYS_PEX_RST_MON# 76
3D3V_AON_S0
Q7301
2N7002K-1-GP
84.2N702.031
2ND = 084.07002.0A31
18 PEG_CLKREQ_CPU#
Muxless
3D3V_AON_S0
R7302
10KR2J-L-GP
Muxless
PEG_CLKREQ_dGPU#
76 GPU_PEX_RST#
GPU_PEX_RST#
18 PEG_CLK_CPU
18 PEG_CLK_CPU#
VGA1A
1 OF 17
PEX_WAKE#
PEX_RST#
PEX_CLKREQ#
PEX_REFCLK
PEX_REFCLK#
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
PEX_TX3#
PEX_RX3
PEX_RX3#
PEX_TX4
PEX_TX4#
PEX_RX4
PEX_RX4#
PEX_TX5
PEX_TX5#
PEX_RX5
PEX_RX5#
PEX_TX6
PEX_TX6#
PEX_RX6
PEX_RX6#
PEX_TX7
PEX_TX7#
PEX_RX7
PEX_RX7#
PEX_TX8
PEX_TX8#
PEX_RX8
PEX_RX8#
PEX_TX9
PEX_TX9#
PEX_RX9
PEX_RX9#
PEX_TX10
PEX_TX10#
PEX_RX10
PEX_RX10#
PEX_TX11
PEX_TX11#
PEX_RX11
PEX_RX11#
PEX_TX12
PEX_TX12#
PEX_RX12
PEX_RX12#
PEX_TX13
PEX_TX13#
PEX_RX13
PEX_RX13#
PEX_TX14
PEX_TX14#
PEX_RX14
PEX_RX14#
PEX_TX15
PEX_TX15#
PEX_RX15
PEX_RX15#
N15P-GT-A2-GP
071.0N15P.000U
Muxless
PEG_RX_CON_P0
PEG_RX_CON_N0
PEG_RX_CON_P1
PEG_RX_CON_N1
PEG_RX_CON_P2
PEG_RX_CON_N2
PEG_RX_CON_P3
PEG_RX_CON_N3
PEG_RX_CON_P4
PEG_RX_CON_N4
PEG_RX_CON_P5
PEG_RX_CON_N5
PEG_RX_CON_P6
PEG_RX_CON_N6
PEG_RX_CON_P7
PEG_RX_CON_N7
PEG_RX_CON_P8
PEG_RX_CON_N8
PEG_RX_CON_P9
PEG_RX_CON_N9
PEG_RX_CON_P10
PEG_RX_CON_N10
PEG_RX_CON_P11
PEG_RX_CON_N11
PEG_RX_CON_P12
PEG_RX_CON_N12
PEG_RX_CON_P13
PEG_RX_CON_N13
PEG_RX_CON_P14
PEG_RX_CON_N14
PEG_RX_CON_P15
PEG_RX_CON_N15
SCD1U16V2KX-L-GP
860_850
860
1D05V_VGA_S0
PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5
PEX_IOVDD_6
C7374
C7373
C7334
C7361
C7375
SC10U6D3V3MX-L-GP
SC10U6D3V3KX-L-GP
SCD1U10V2KX-L1-GP
Muxless
PEX_IOVDDQ_1
PEX_IOVDDQ_2
PEX_IOVDDQ_3
PEX_IOVDDQ_4
PEX_IOVDDQ_5
PEX_IOVDDQ_6
PEX_IOVDDQ_7
PEX_IOVDDQ_8
PEX_IOVDDQ_9
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14
C7371
C7372
C7333
C7360
SC4D7U6D3V3MX-L-GP
SC4D7U6D3V3KX-L-GP
Max:1A
PEX_PLL_HVDD
PEX_SVDD_3V3
3D3V_AON_S0
C7367
C7366
SC4D7U6D3V3KX-L-GP
VDD_SENSE
GND_SENSE
NVVDD_SENSE 82
NVGND_SENSE 82
NC#P8
DY
200R2F-L1-GP
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
VGAPEX_AJ26
VGAPEX_AK26
R7304
PEX_PLLVDD
C7369
C7368
C7370
SCD1U16V2KX-L-GP
SC4D7U6D3V3KX-L-GP
SCD1U10V2KX-L1-GP
TESTMODE
R7307
10KR2J-L-GP
PEX_TERMP
R7305
2K49R2F-2-L-GP
FC7304
EC7301
EC7302
EC7303
SCD1U16V2KX-L-GP
DY
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GPU(PEG)
Size
Custom
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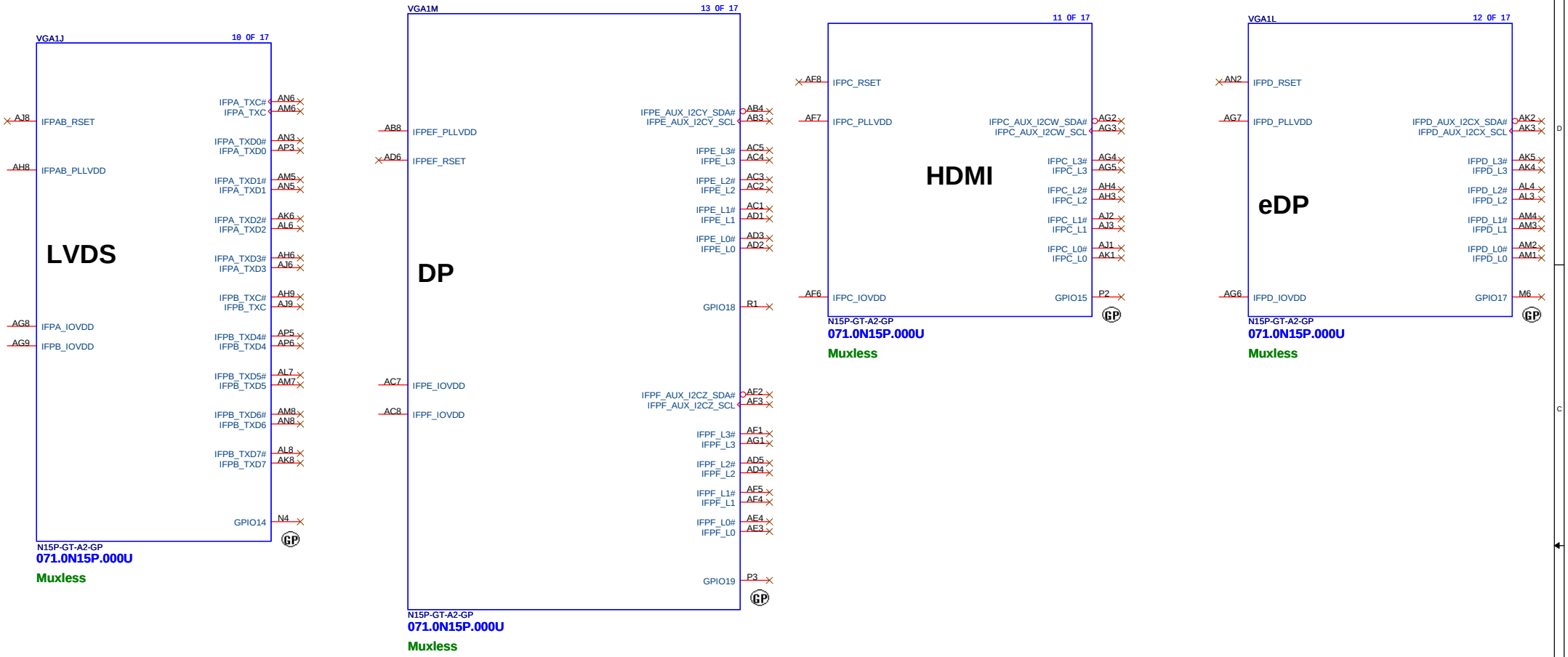

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Title: ***GPU (DIGITALOUT)***

Size	Document Number	Rev
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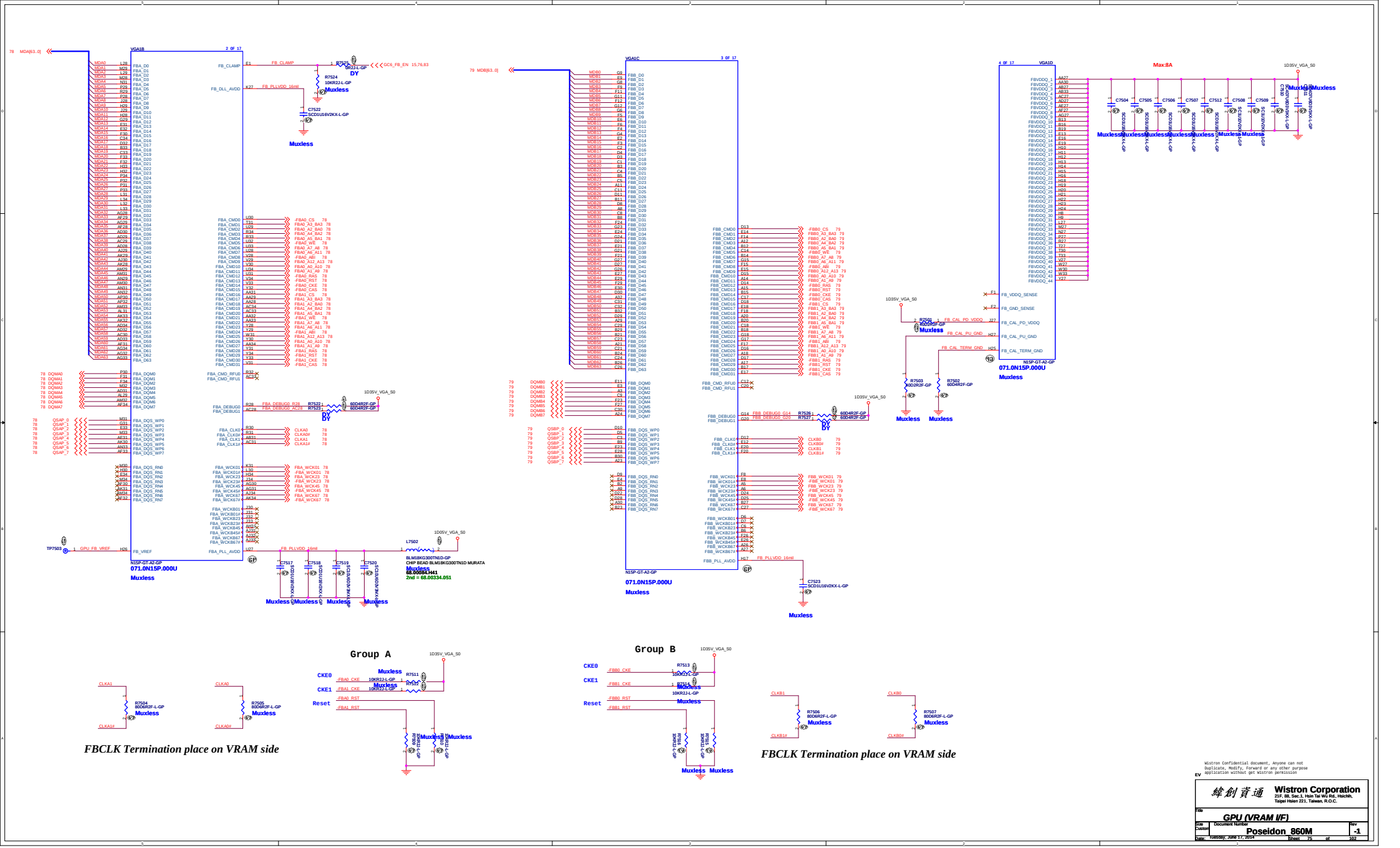

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Title: GPU (VRAM I/F)

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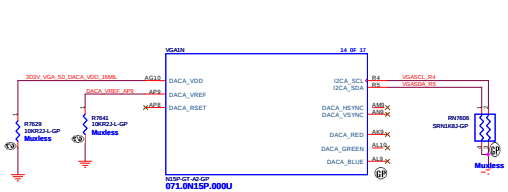
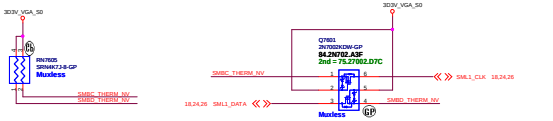
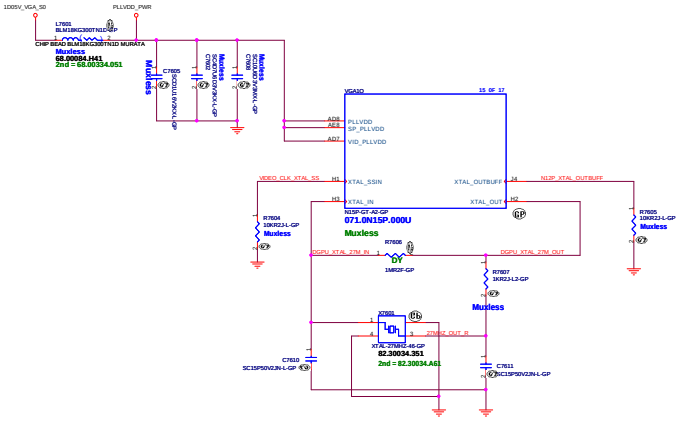
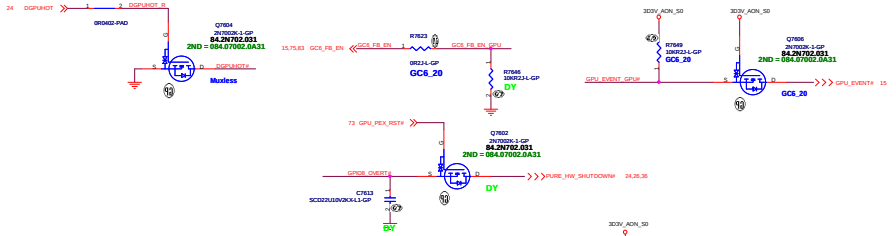
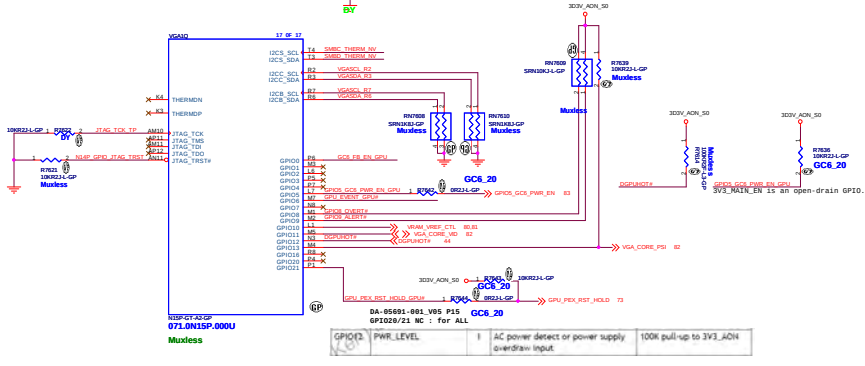










DA-05691-001_V05 P15
GPIO20/21 NC : for ALL

GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input. 100K pull-up to 3V3_AON

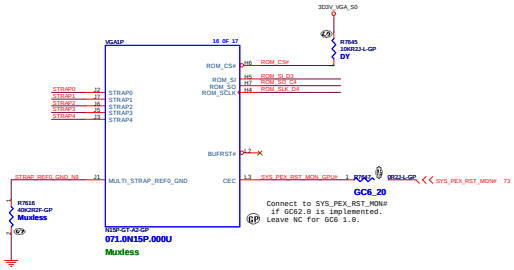


Table 2. Memory Configurations for Testing

Products	Type	VRAM Voltage	Vendor	Qty Parts	Memory Bus Width	Density	Speed Bin (MHz)	Part Number
H15S-GX	DDR3	1.5V	Hynix	8	128 bits	256MX16	1000	H5TC4G63AFR-11C
H15P-GT	DDR3	1.5V	Hynix	8	128 bits	256MX16	1000	H5TC4G63AFR-11C
	GDDR5	1.35V	Hynix	8	128 bits	256MX16	2500	H5GC4H24MFR-T2C
H15P-GX	GDDR5	1.35V	Hynix	8	128 bits	256MX16	2500	H5GC4H24MFR-T2C

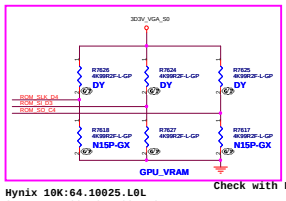
Table 15-3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

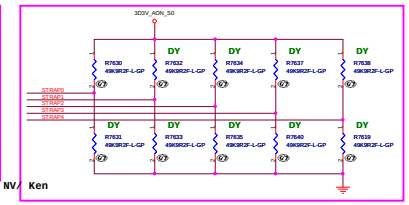
Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND and stuff 50kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND for forward compatibility.			

Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

4.99Kohm 64.49915.6DL
10Kohm 64.10025.L0L
15Kohm 64.15025.6DL
20Kohm 64.20025.6DL
24.9Kohm 64.24925.6DL
30.1Kohm 64.30125.6DL
34.8Kohm 64.34825.6DL
45Kohm 64.45325.6DL





Hynix 10K:64.10025.L0L
Samsung 4.99K:64.49915.6DL

Check with NV/ Ken

Table 11. N15P-GX/GT GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)
GDDR5	1.35V/ 1.35V	128Mx16	Samsung	K4G20325FD-FC03	D-die	0x0	2500
			Hynix	H5GC2H24BFR-T2C	B-die	0x1	2500
			Micron	EDW2032BBBG-6A-F	B-die	0x5	2500
		256Mx16	Hynix	H5GC4H24MFR-T2C	N-die	0x2	2500
			Samsung	K4G41325FC-HC03	C-die	0x3	2500
			Micron	EDW4032BABG-60-F	A-die	0x4	2500

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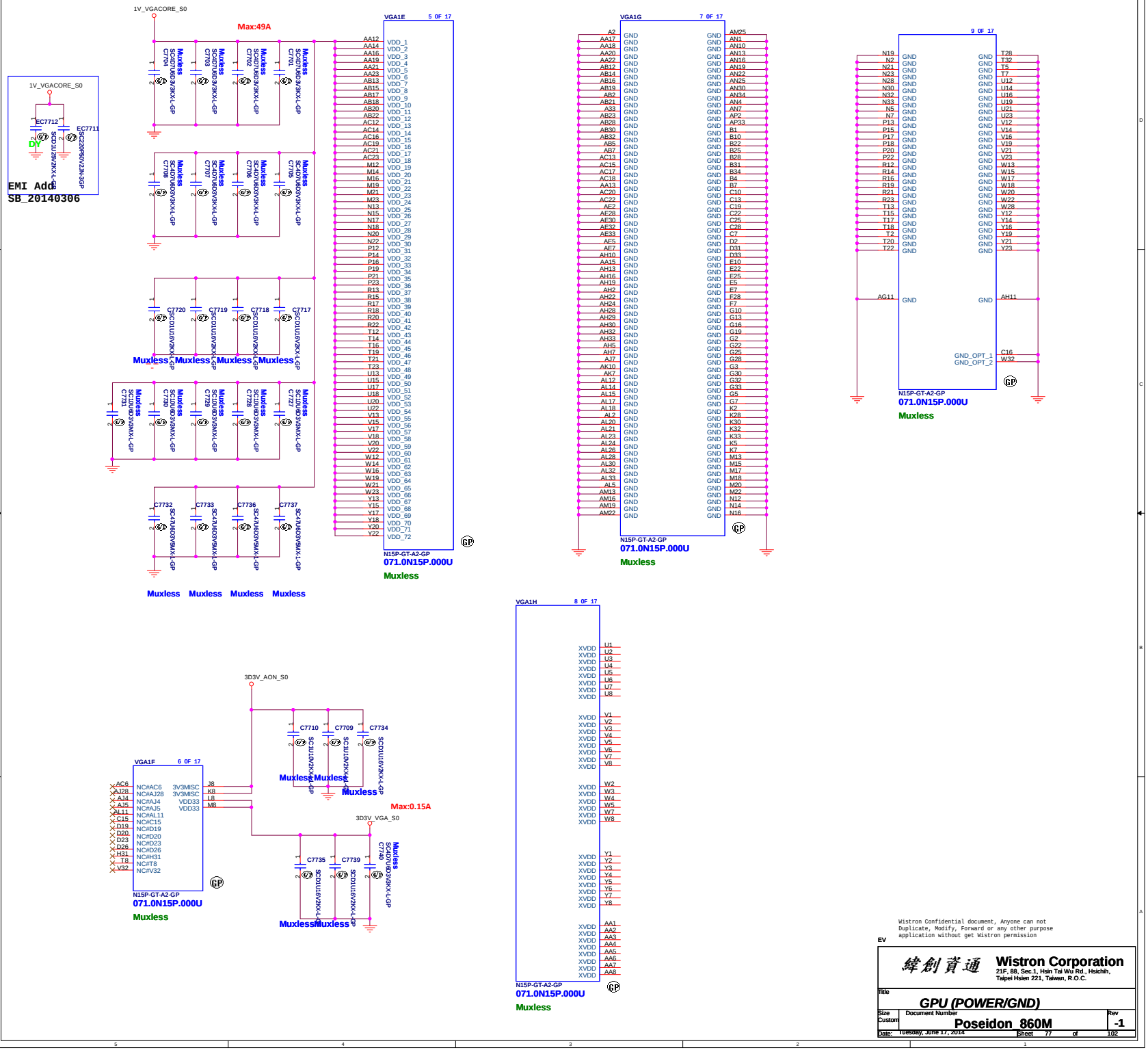

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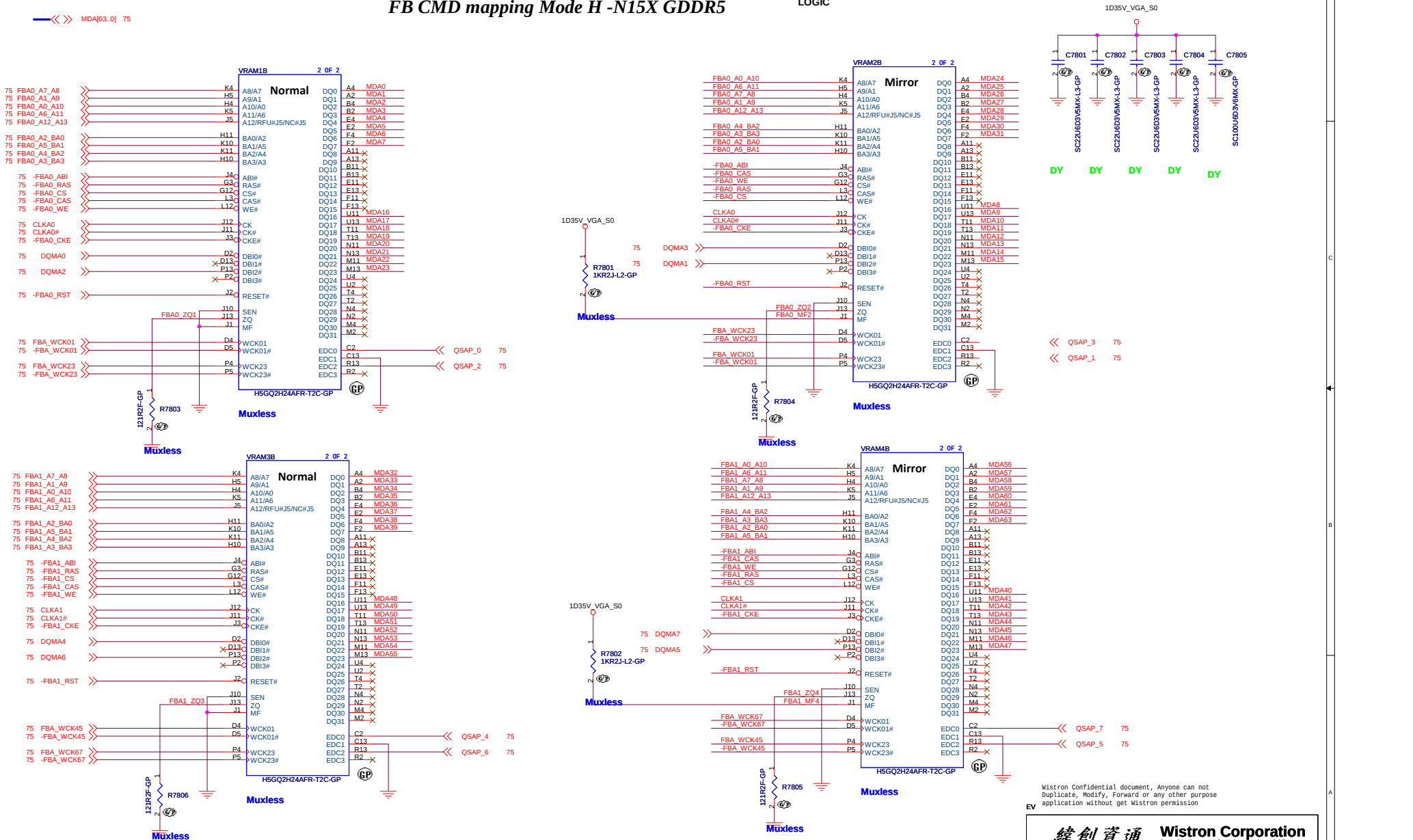
TABLE
GDDR5 VIDEO MEMORY 72.05224.A0U 72.20325.B0U

	HYNIX 2GBITS (64Mx32)	SAMSUNG 2GBITS (64Mx32)	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)
U91 U92 U93 U94 U95 U96 U97 U98	H5GQ2H24AFR-T2C	K4G20325FD-FC04	H5GC4H24MFR (tentative)	K4G41325FC-HC03 (tentative)

LOGIC

FB CMD mapping Mode H -N15X GDDR5

MDA[63..0] 75



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Title: VRAM_A

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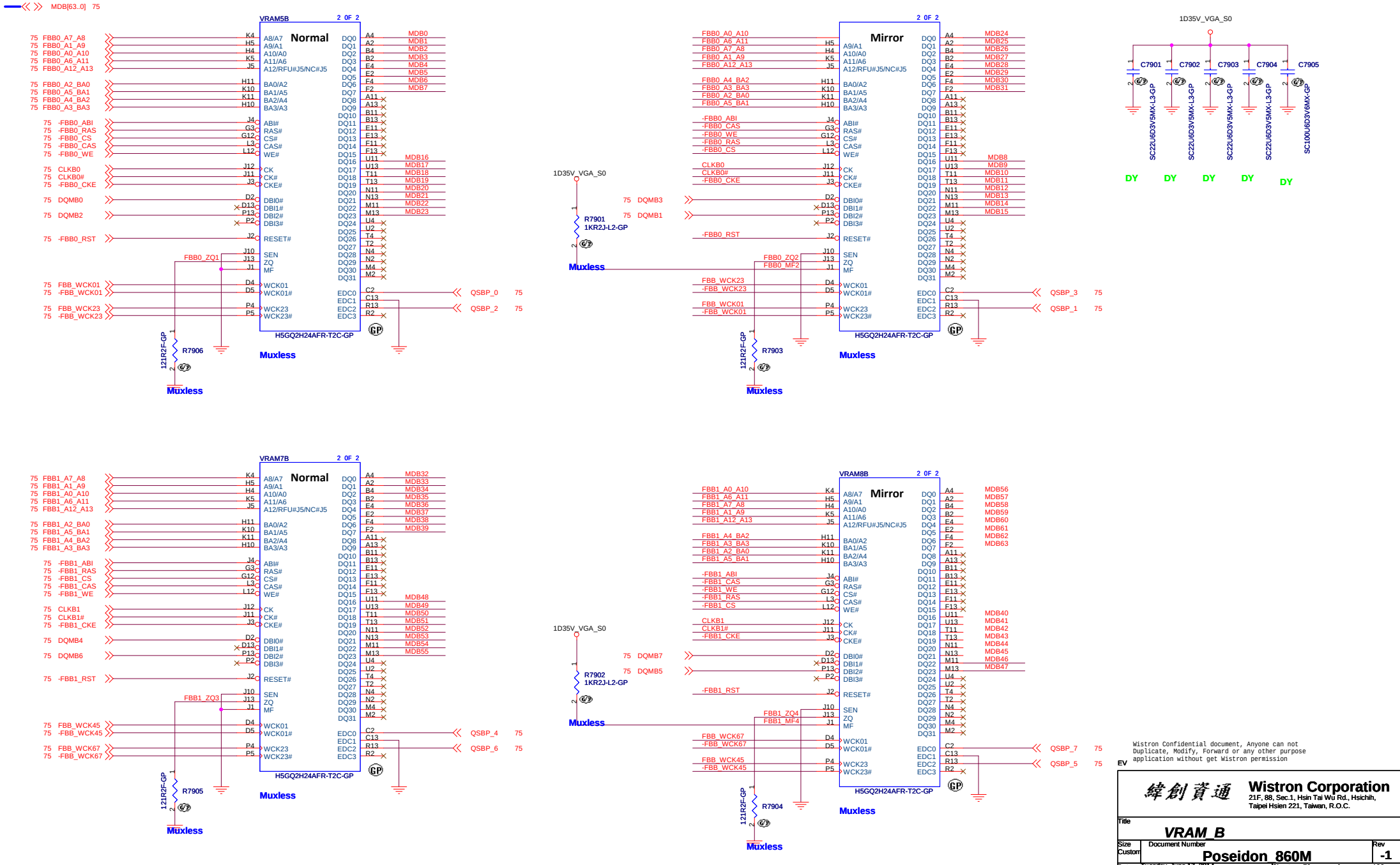
MDB[63..0] 75
VRAM5B
2 OF 2
Normal
H5GQ2H24AFR-T2C-GP
Muxless
R7906
121R2F-GP
FBB0_ZQ1
VRAM7B
R7905
FBB1_ZQ3
Mirror
R7903
FBB0_ZQ2
FBB0_MF2
R7904
FBB1_ZQ4
FBB1_MF4
1D35V_VGA_S0
R7901
1KR2J-L2-GP
R7902
C7901
C7902
C7903
C7904
C7905
SC22U6D3V5MX-L3-GP
SC100U6D3V6MX-GP
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Custom
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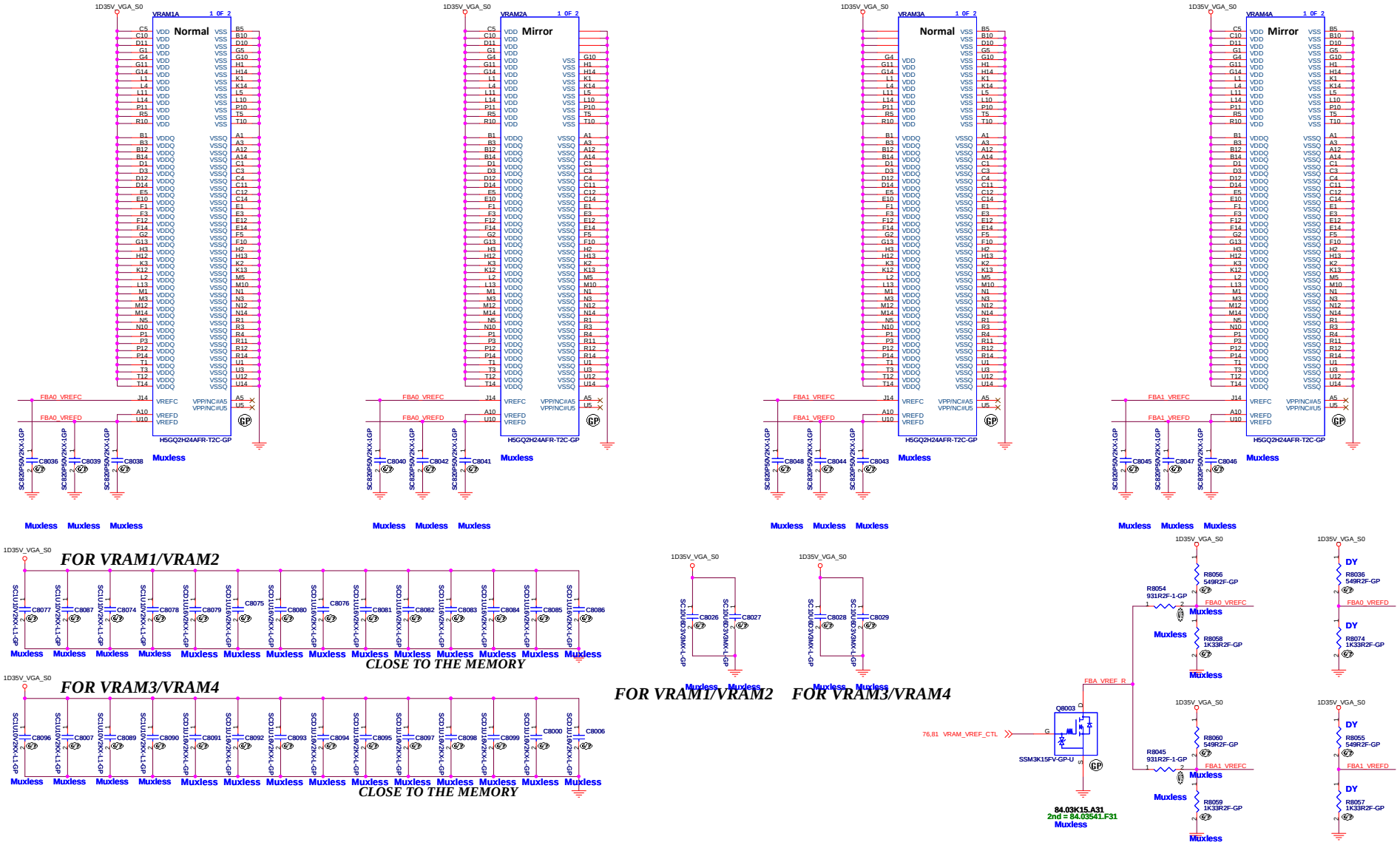

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Title: VGA_POWER_A

Size: Custom | Document Number: Poseidon_860M | Rev: -1

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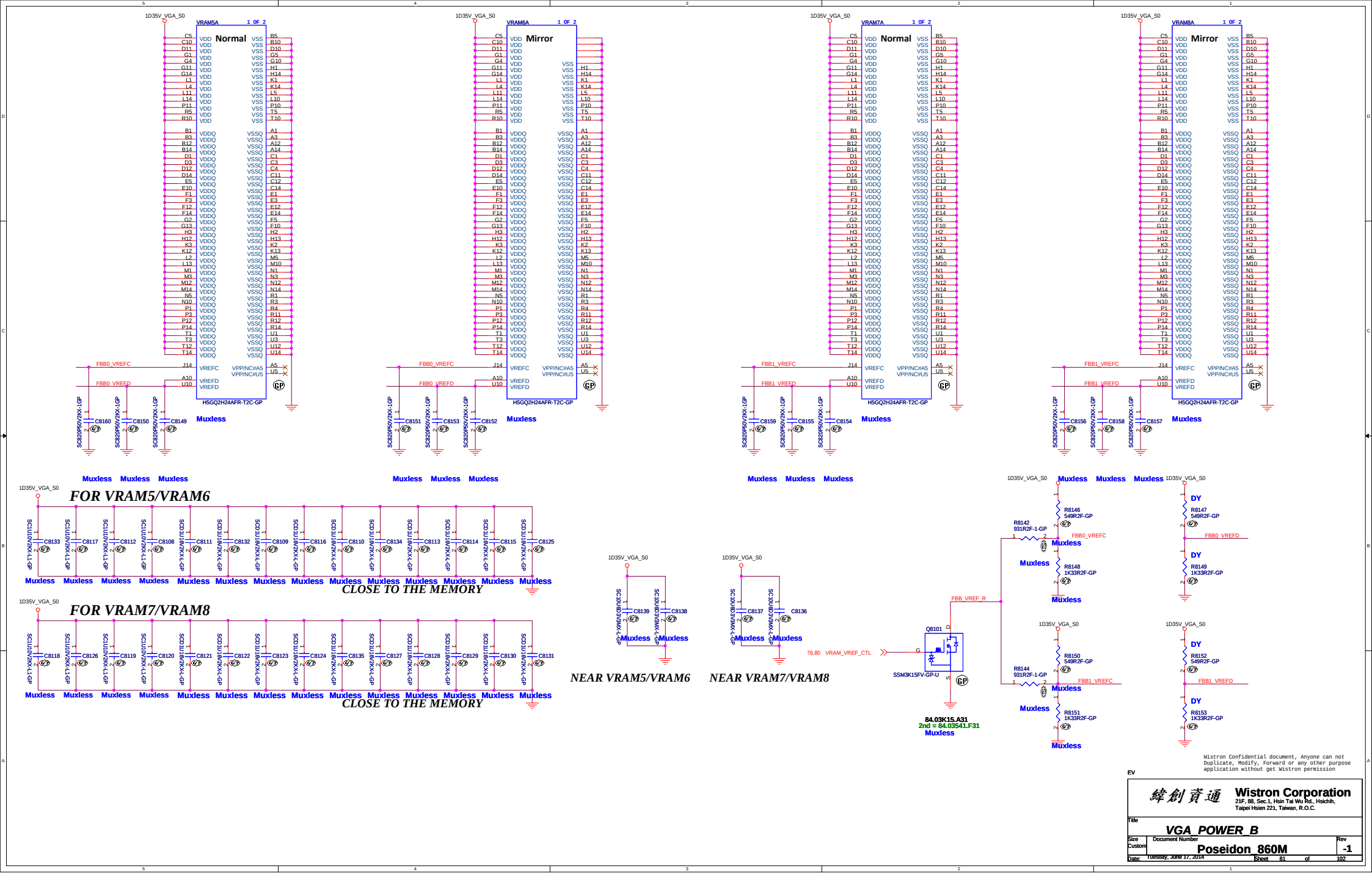

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Title: **VGA_POWER_B**

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VGA : N15P GX
Config : B
EDP-Continuous : 49A
EDP-Peak : 76A

	Config : D	Config : C	Config : B
EDP-Cont.	33.5 A	35 A	43 A
EDP-Peak	51.5 A	40.89 A	80 A
PR8222	27K ohm	39K ohm	20K ohm
PR8206	7.5K ohm	30K ohm	20K ohm
PR8208	0 ohm	3K ohm	2K ohm
PR8209	6.2K ohm	24K ohm	18K ohm
PR8214	1.74K ohm	3K ohm	0 ohm
PC8223	5.6nF	1.8nF	2.7nF

Dual NMOS
84.00916.037
2nd:84.03660.037
PU8202/PU8203/PU8205

DCBATOUT
PT8203 ST15U25VDM-1-GP DY DY PT8202 ST15U25VDM-1-GP

5V_S0
PR8223 2D2R3J-2-GP Muxless
VGA_PVCC_1
PC8207 SCD1U16V2KX-L-GP Muxless
PR8261 0R2J-L-GP 2_Phase
PC8202 SCD1U25V2KX-L-GP Muxless
PR8202 0R2R2F-GP Muxless
PR8201 499KR2F-1-GP Muxless
PR8203 10KR2J-L-GP Muxless
3D3V_VGA_S0
20,24,83 DGPU_PWROK
76 VGA_CORE_PSI
76 VGA_CORE_VID
PR8207 0R0402-PAD
PC8203 SC1KP50V2KX-L-1-GP DY
PC8201 SCD1U16V2KX-L-GP DY
PR8206 20KR2F-L3-GP Muxless
PR8222 20KR2F-L3-GP Muxless
PR8208 2KR2F-L1-GP Muxless
PC8223 SC2700P50V2KX-1-GP Muxless
PC8204 SCD01U50V2KX-L-GP DY
PR8209 18KR2F-GP Muxless
PR8214 0R0402-PAD
PU8201 RT8813AGQW-GP Muxless

PWR_VGA_CORE_TON_1
PWR_VGA_CORE_ISEN1
PWR_VGA_CORE_TON
PWR_VGA_CORE_EN
PWR_VGA_CORE_VID
PWR_VGA_CORE_RGND
PWR_VGA_CORE_VREF
PWR_VGA_CORE_REFIN
PWR_VGA_CORE_REFADJ
PWR_VGA_CORE_ISEN2
PWR_VGA_CORE_ISEN3
PWR_VGA_CORE_SS
PWR_VGA_CORE_VREF_R
PWR_VGA_CORE_VREF_L
PWR_VGA_CORE_RGND

VCC/ISEN1 TON PGOOD EN PSI VID VREF REFIN REFADJ TALERT#/ISEN2 TSNS/ISEN3 SS
PVCC UGATE1 BOOT1 PHASE1 LGATE1 UGATE2 BOOT2 PHASE2 LGATE2 VSNS RGND PWM3 GND

PWR_VGA_CORE_UGATE1
PWR_VGA_CORE_UGATE1_R
PR8218 0R3J-L1-GP Muxless
PWR_VGA_CORE_BOOT1
PR8210 0R3J-L1-GP Muxless
PC8211 SCD1U25V2KX-L-GP Muxless
PWR_VGA_CORE_PHASE1
PWR_VGA_CORE_LGATE1
PR8224 13K3R2F-L1-GP Muxless
OCP setting
PR8224=13.3K 'OCP = 102A
PWR_VGA_CORE_UGATE2
PWR_VGA_CORE_UGATE2_R
PR8219 0R3J-L1-GP Muxless
PWR_VGA_CORE_BOOT2
PR8211 0R3J-L1-GP Muxless
PWR_VGA_CORE_PHASE2
PWR_VGA_CORE_LGATE2
PC8216 SCD1U25V2KX-L-GP Muxless
PWR_VGA_CORE_VSNS
PWR_VGA_CORE_RGND
PWR_VGA_CORE_PWM3

PU8202 FDMS3600-02-RJK0215-COLAY-GP
PWR_VGA_CORE_UGATE1_R
PWR_VGA_CORE_PHASE1
PWR_VGA_CORE_LGATE1
PC8208 PC8209 PC8220 SCD1U25V2KX-L-GP Muxless Muxless Muxless
84.00920.037
2nd = 84.08107.B37
Muxless

1V_VGACORE_S0
Mag. 0.36uH 7*7*4
DCR=1.8~2.3mohm
Idc=23A, Isat=32A
PL8201 IND-D38UH-42-GP Muxless

PU8203 FDMS3600-02-RJK0215-COLAY-GP
PWR_VGA_CORE_UGATE2_R
PWR_VGA_CORE_PHASE2
PWR_VGA_CORE_LGATE2
PC8212 PC8213 PC8221 SCD1U25V2KX-L-GP Muxless Muxless Muxless
84.00920.037
2nd = 84.08107.B37
Muxless
Mag. 0.36uH 7*7*4
DCR=1.8~2.3mohm
Idc=23A, Isat=32A
PL8202 IND-D38UH-42-GP Muxless

1V_VGACORE_S0
PR8212 100R2F-L3-GP Muxless
PR8221 0R0402-PAD
NVVDD_SENSE 73
PR8220 0R0402-PAD
NVGND_SENSE 73
PR8213 100R2F-L3-GP Muxless
PC8219 SC47P50V2JN-3GP DY
PC8222 SC47P50V2JN-3GP DY
PC8217 SC47P50V2JN-3GP DY

1V_VGACORE_S0 -1_20140526
PT8207 PT8208 PT8209 STA70U2VMX-GP
470uF/2V, 7.5 x 4.5 x 2.1
ESR=9mohm
Ripple Current=3000 mA
Muxless Muxless Muxless

PC8205 SC47P50V2JN-3GP
SB_0320
Muxless

3D3V_VGA_S0
PR8256 10KR2J-L-GP Muxless
PWR_VGA_CORE_EN
83 DGPU_PWR_EN
PR8250 0R2J-L-GP DY
PC8225 SCD1U25V2KX-L-GP Muxless
PD8201 BAW56-S-GP DY DY

5V_S0
PR8226 2D2R3J-2-GP 3_Phase
VGA_PVCC_2
PC8210 SCD1U16V2KX-L-GP 3_Phase
PR8264 0R2J-L-GP DY
PWR_VGA_DRV_EN
PWR_VGA_CORE_PWM3
PR8262 0R2J-L-GP 2_Phase
PU8204 RT9610BZQW-GP 3_Phase
PWR_VGA_CORE_BOOT3
PWR_VGA_CORE_UGATE3
PWR_VGA_CORE_PHASE3
PWR_VGA_CORE_LGATE3
PR8215 0R3J-L1-GP 3_Phase
PWR_VGA_CORE_BOOT3_1
PC8218 SCD1U25V2KX-L-GP 3_Phase
PWR_VGA_CORE_UGATE3_R
PR8225 0R3J-L1-GP 3_Phase
1V_VGACORE_S0
Mag. 0.36uH 7*7*4
DCR=1.8~2.3mohm
Idc=23A, Isat=32A
PL8203 IND-D38UH-42-GP 3_Phase

PWR_VGA_CORE_PHASE1
PR8204 10KR2J-L-GP 3_Phase
PWR_VGA_CORE_ISEN1
PWR_VGA_CORE_PHASE2
PR8205 10KR2J-L-GP 3_Phase
PWR_VGA_CORE_ISEN2
PWR_VGA_CORE_PHASE3
PR8216 10KR2J-L-GP 3_Phase
PWR_VGA_CORE_ISEN3

PU8205 FDMS3600-02-RJK0215-COLAY-GP
PWR_VGA_CORE_UGATE3_R
PWR_VGA_CORE_PHASE3
PWR_VGA_CORE_LGATE3
PC8214 PC8215 PC8224 SCD1U25V2KX-L-GP 3_Phase 3_Phase 3_Phase
84.00920.037
2nd = 84.08107.B37
3_Phase

PWR_VGA_CORE_EN
PR8263 0R2J-L-GP
PWR_VGA_DRV_EN
3_Phase

EV

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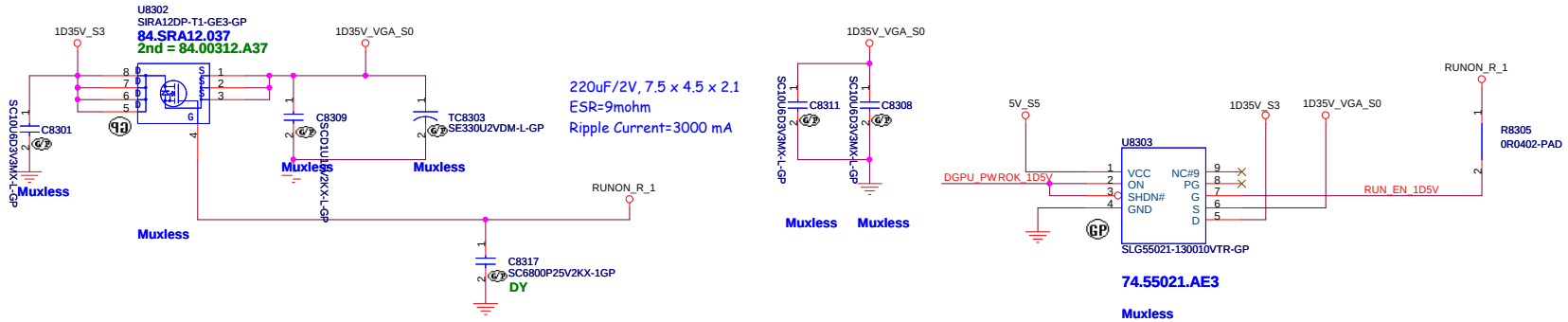
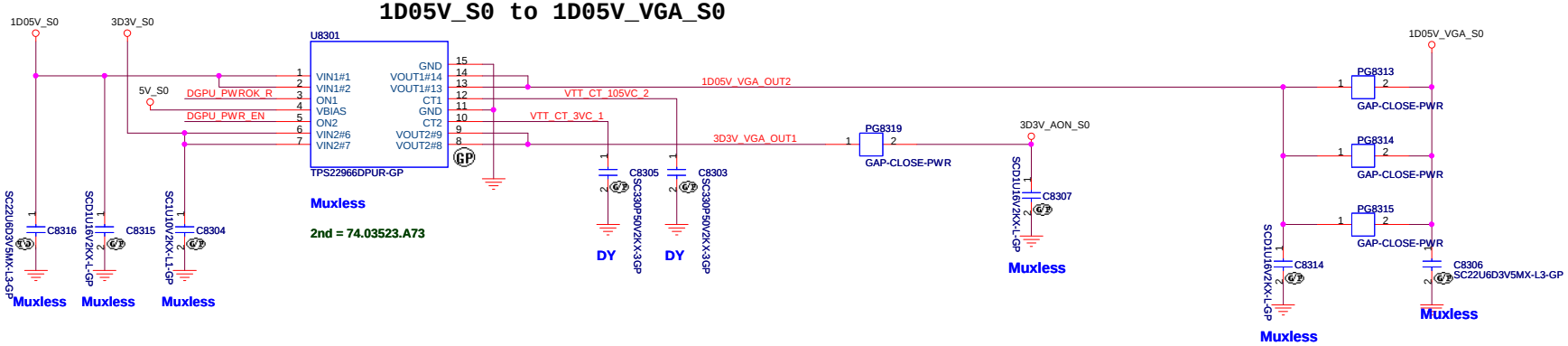
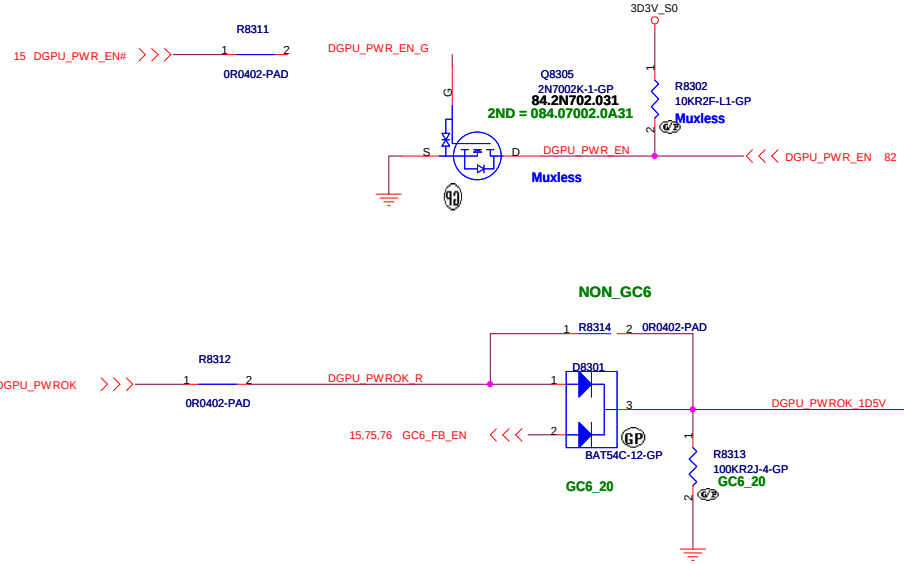
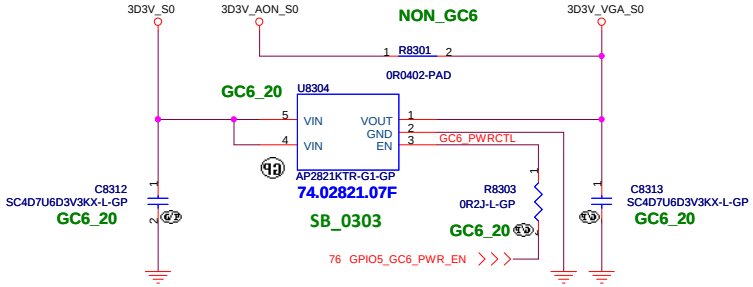
TPS22966 for VGA_1D35V(For VRAM GDDR5)



3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0







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Title: DISCRETE VGA POWER

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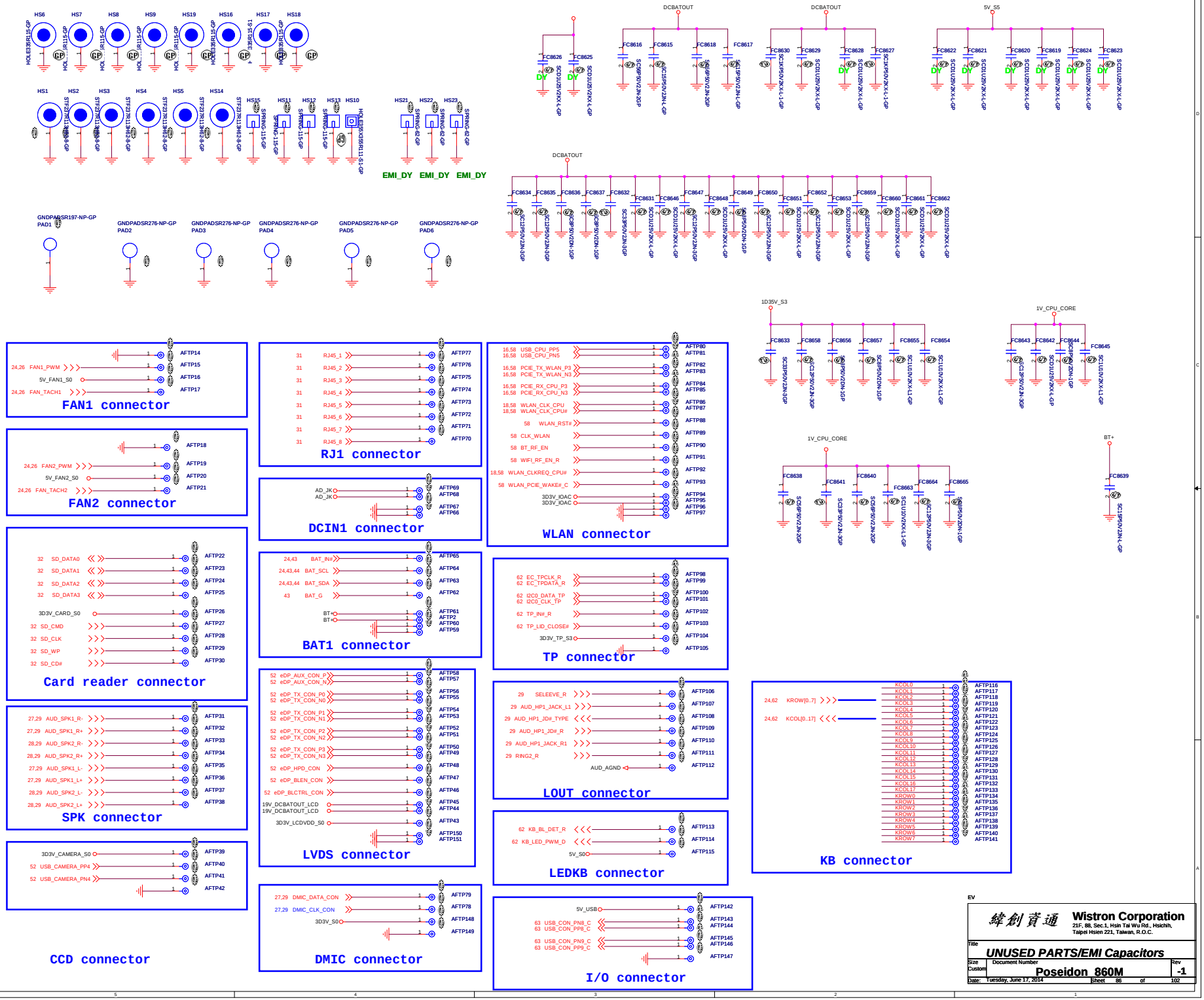
HS6 HS7 HS8 HS9 HS19 HS16 HS17 HS18
HS1 HS2 HS3 HS4 HS5 HS14 HS15 HS11 HS12 HS13 HS10
HS21 HS22 HS23
EMI_DY EMI_DY EMI_DY
GNDPADSR197-NP-GP PAD1
GNDPADSR276-NP-GP PAD2
GNDPADSR276-NP-GP PAD3
GNDPADSR276-NP-GP PAD4
GNDPADSR276-NP-GP PAD5
GNDPADSR276-NP-GP PAD6
DCBATOUT
DCBATOUT
5V_S5
DCBATOUT
1D35V_S3
1V_CPU_CORE
1V_CPU_CORE
BT+
FAN1 connector
FAN2 connector
RJ1 connector
DCIN1 connector
WLAN connector
BAT1 connector
Card reader connector
TP connector
SPK connector
LOUT connector
LVDS connector
KB connector
LEDKB connector
CCD connector
DMIC connector
I/O connector
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Title
UNUSED PARTS/EMI Capacitors
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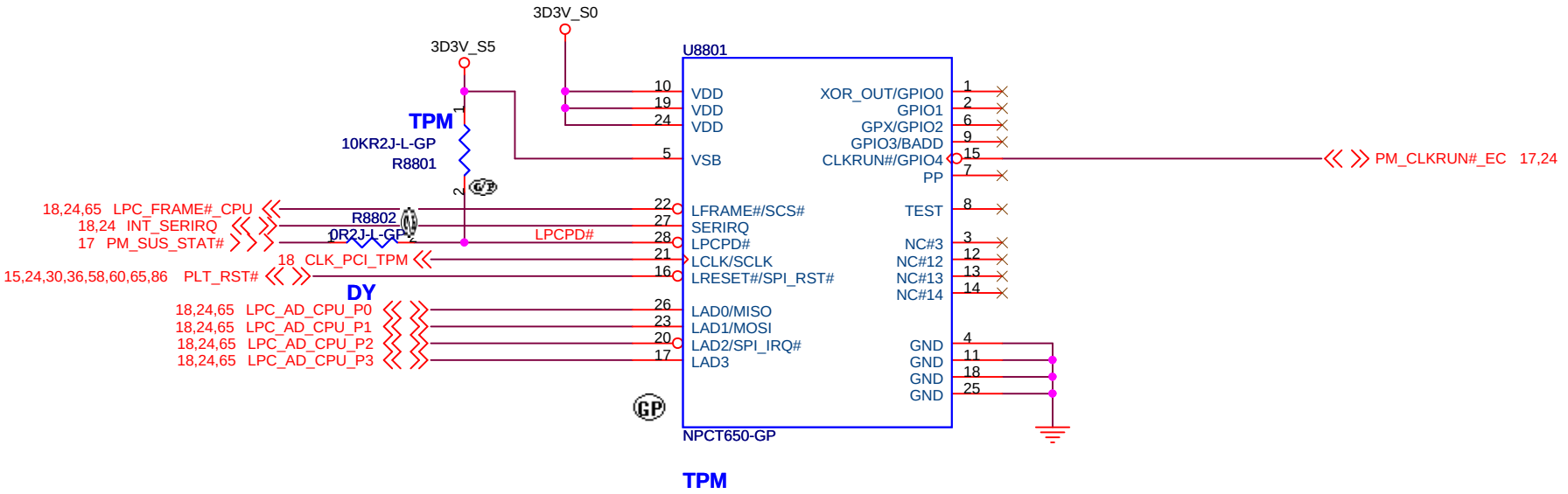

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Title: ***TPM (SLB655T)***

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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0[1]	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST#[1]	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4[1]	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST#[1]	0	System	18	HOOK7	DBR#[1]	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title

PCH_XDP

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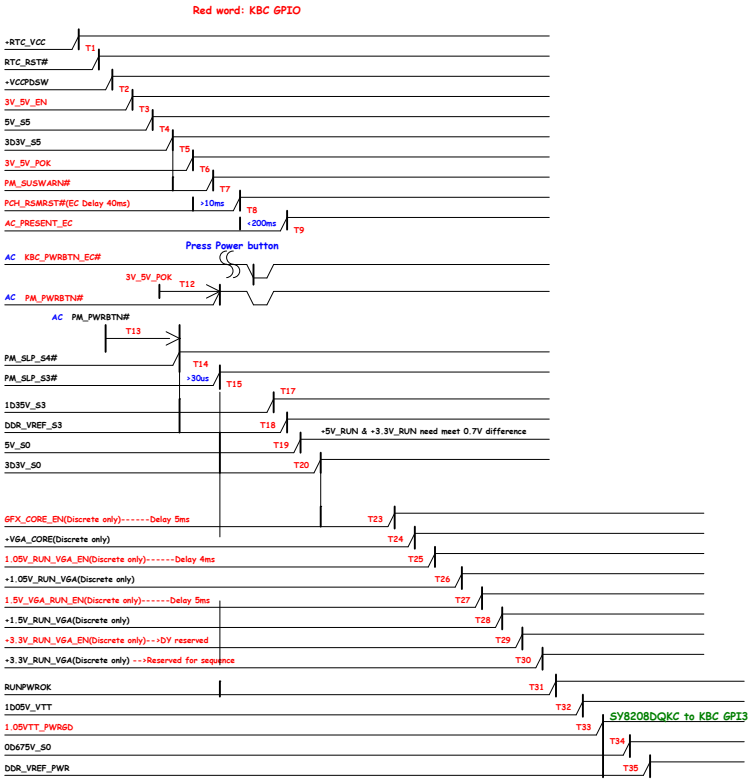
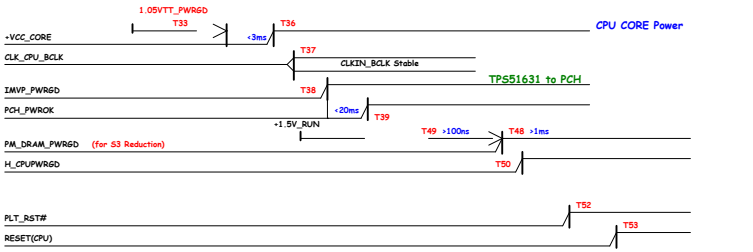
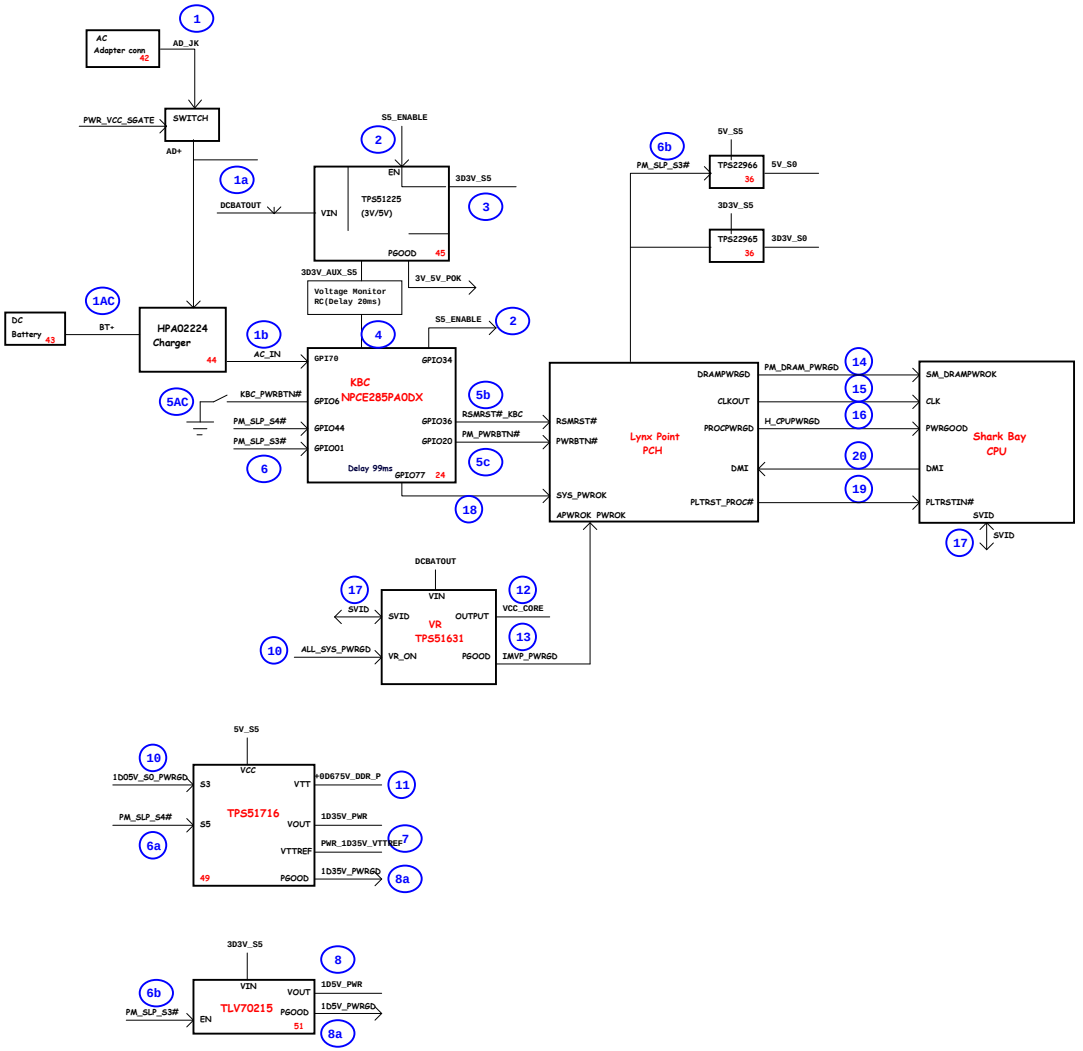
Intel-Power Up Sequence





SHARK BAY POWER UP SEQUENCE DIAGRAM



REV

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Title: Power Sequence

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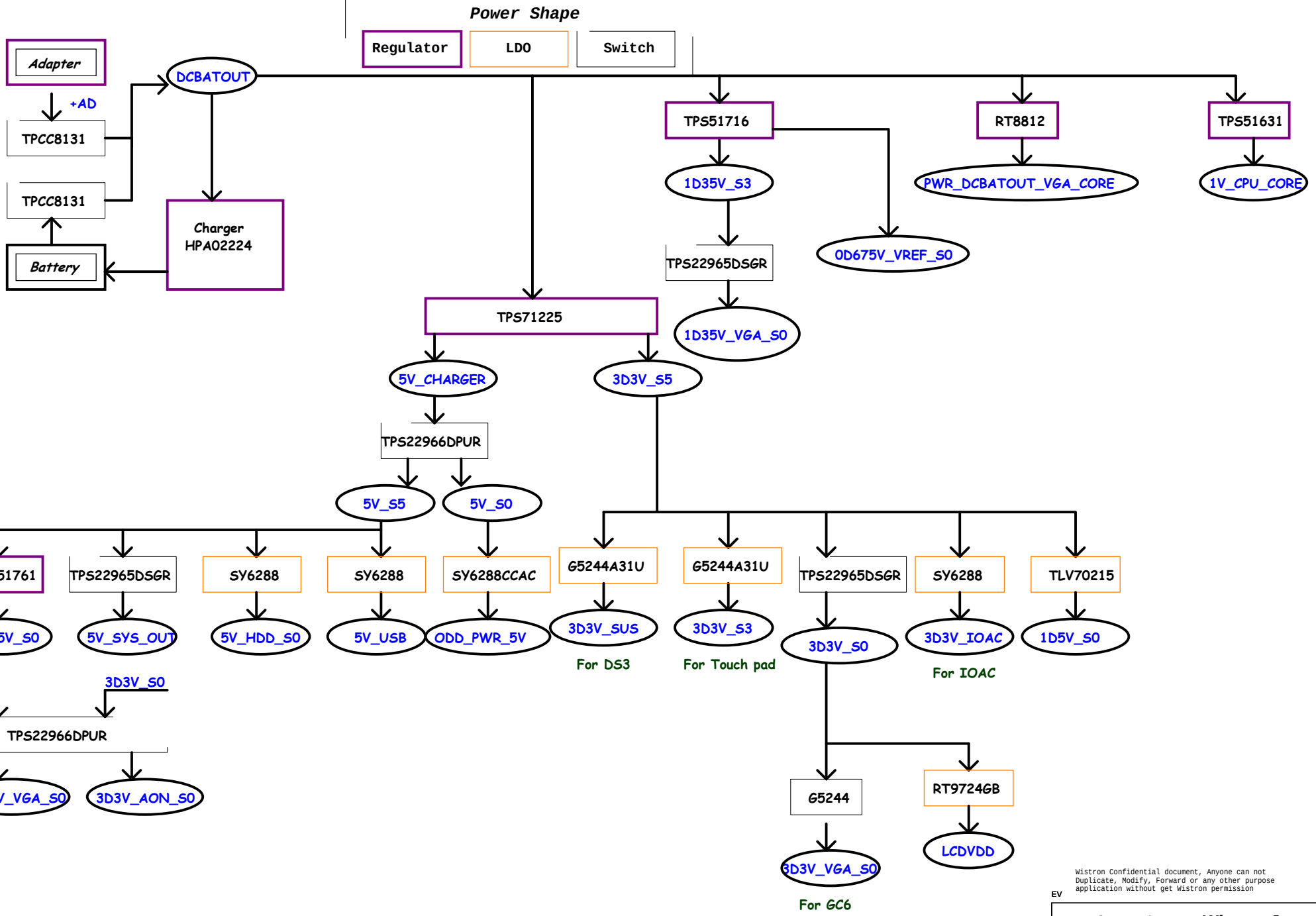

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Title: Power Block Diagram

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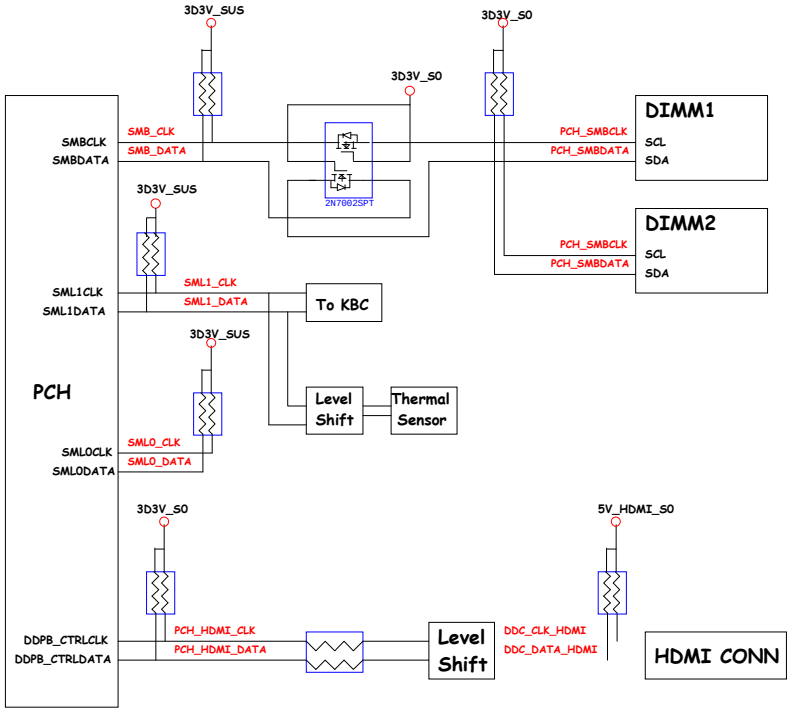
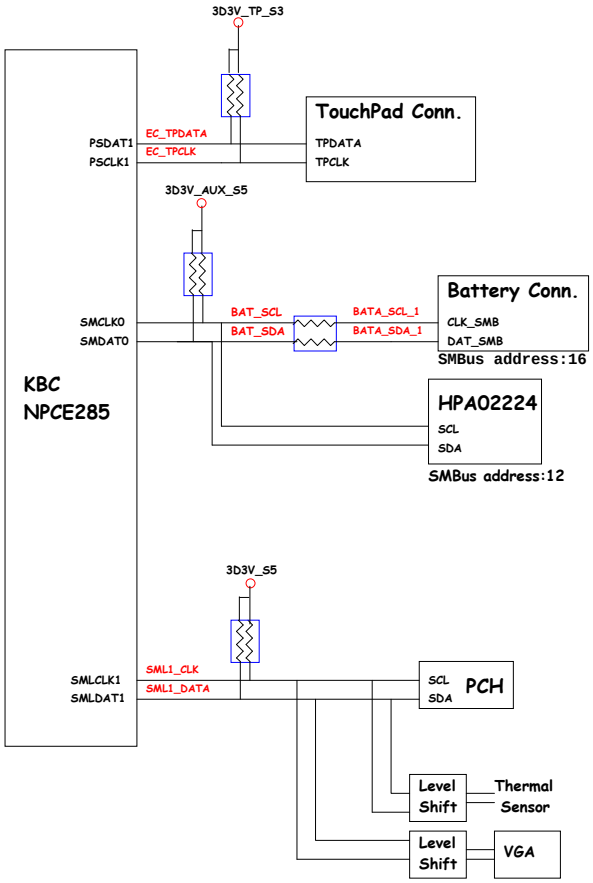
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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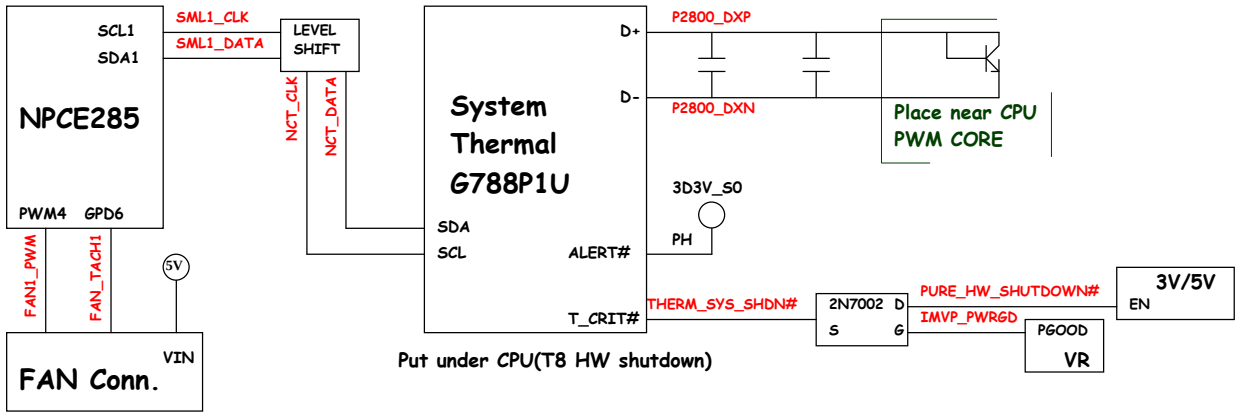
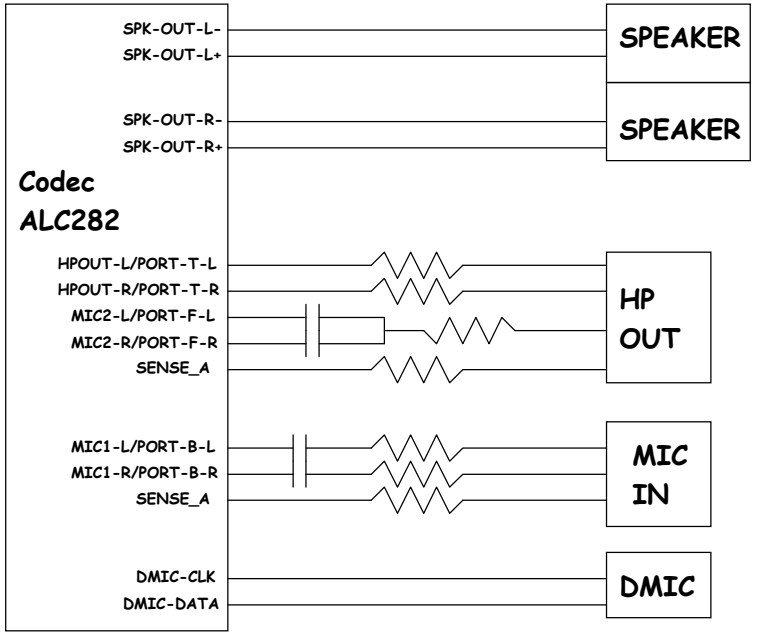
Thermal Block Diagram



Put under CPU(T8 HW shutdown)

Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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